888Z4.5 / LA-1302 Mother Board Rev : 0.5 for Layout

Intel (Northwood) with Intel 845M+ICH3

stencil not open:

J1
U24
PJP2
PJP4
C715
C716
PC155
C72
C94

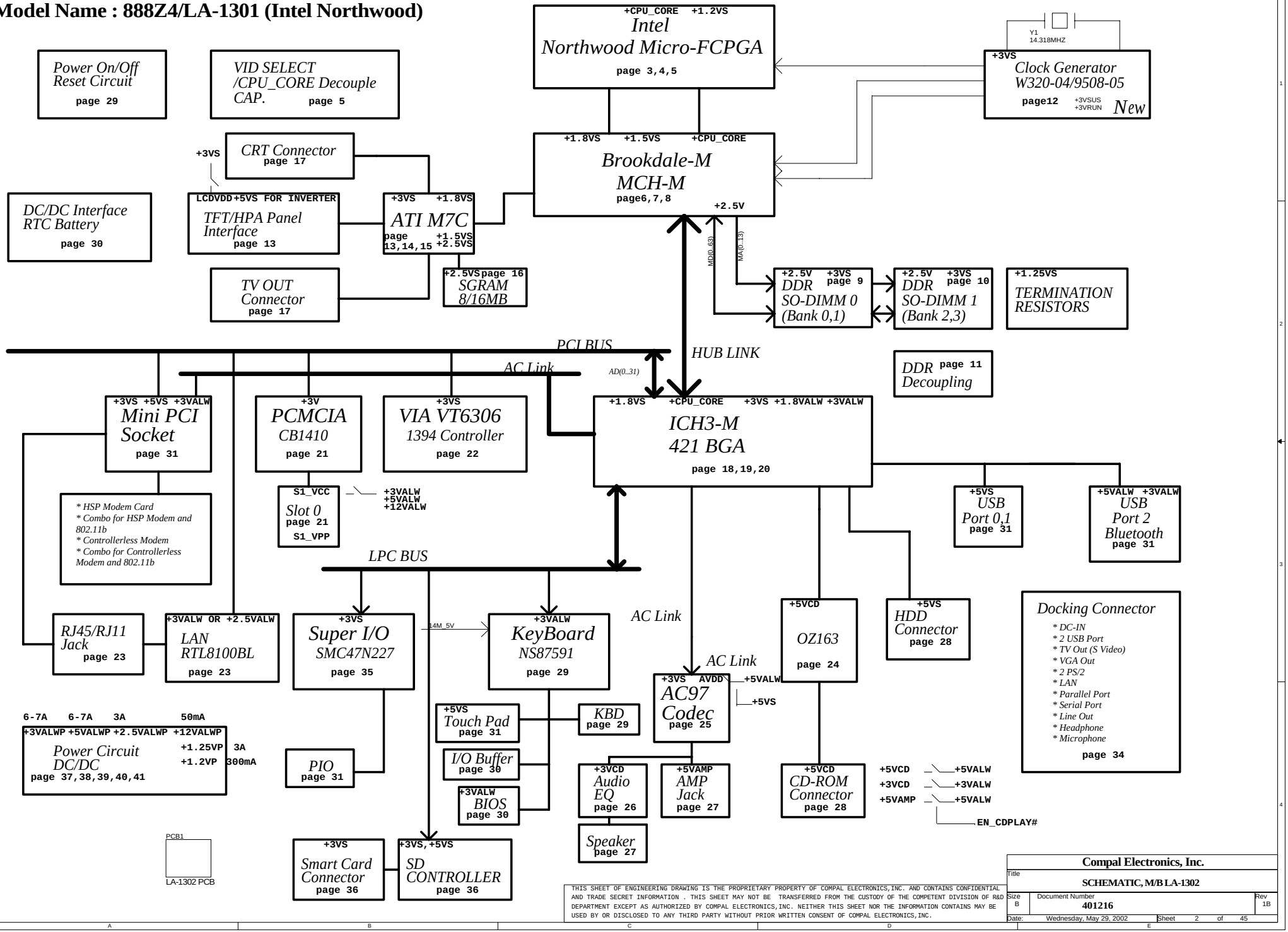
Compal Electronics, Inc.

Title: **SCHEMATIC, M/B LA-1302**

Size: B | Document Number: **401216** | Rev: 1B

Date: Wednesday, May 29, 2002 | Sheet 1 of 45

Model Name : 888Z4/LA-1301 (Intel Northwood)



Compal Electronics, Inc.		
Title: SCHEMATIC, M/B LA-1302		
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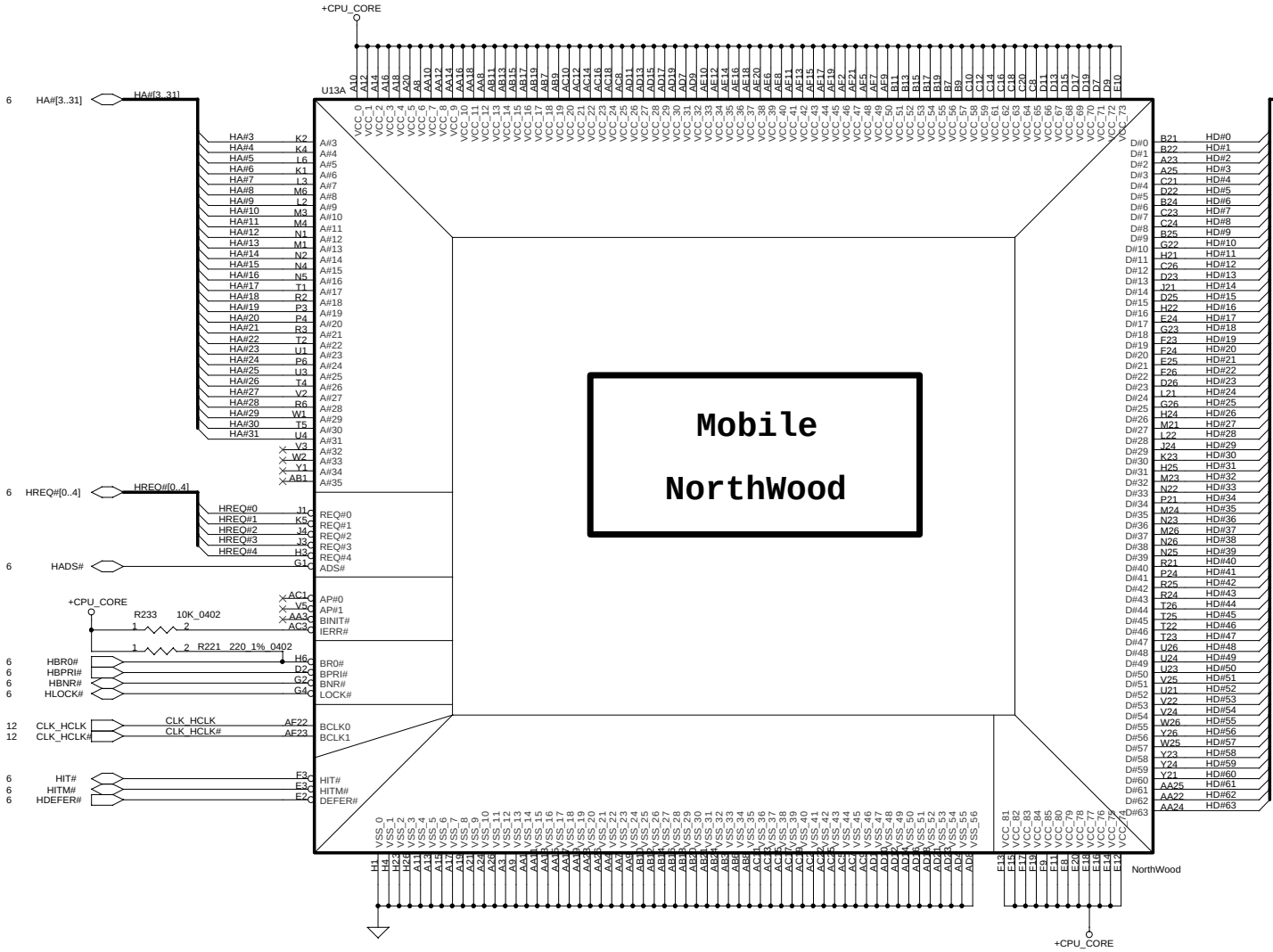
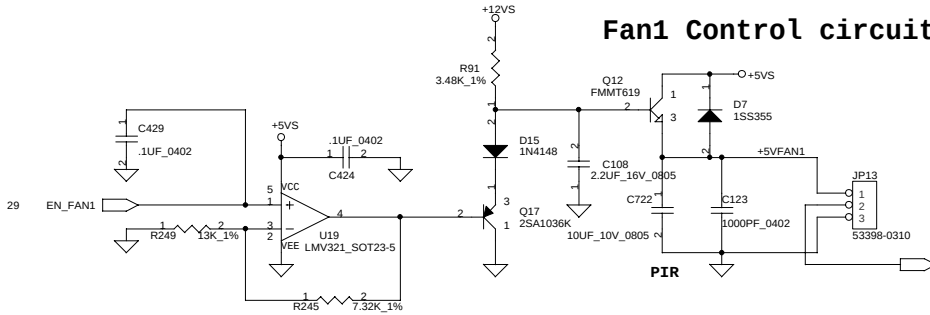
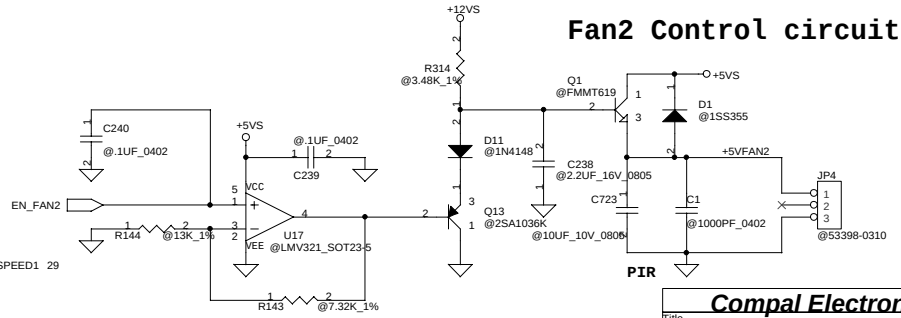


Fan1 Control circuit



Fan2 Control circuit



Compal Electronics, Inc.

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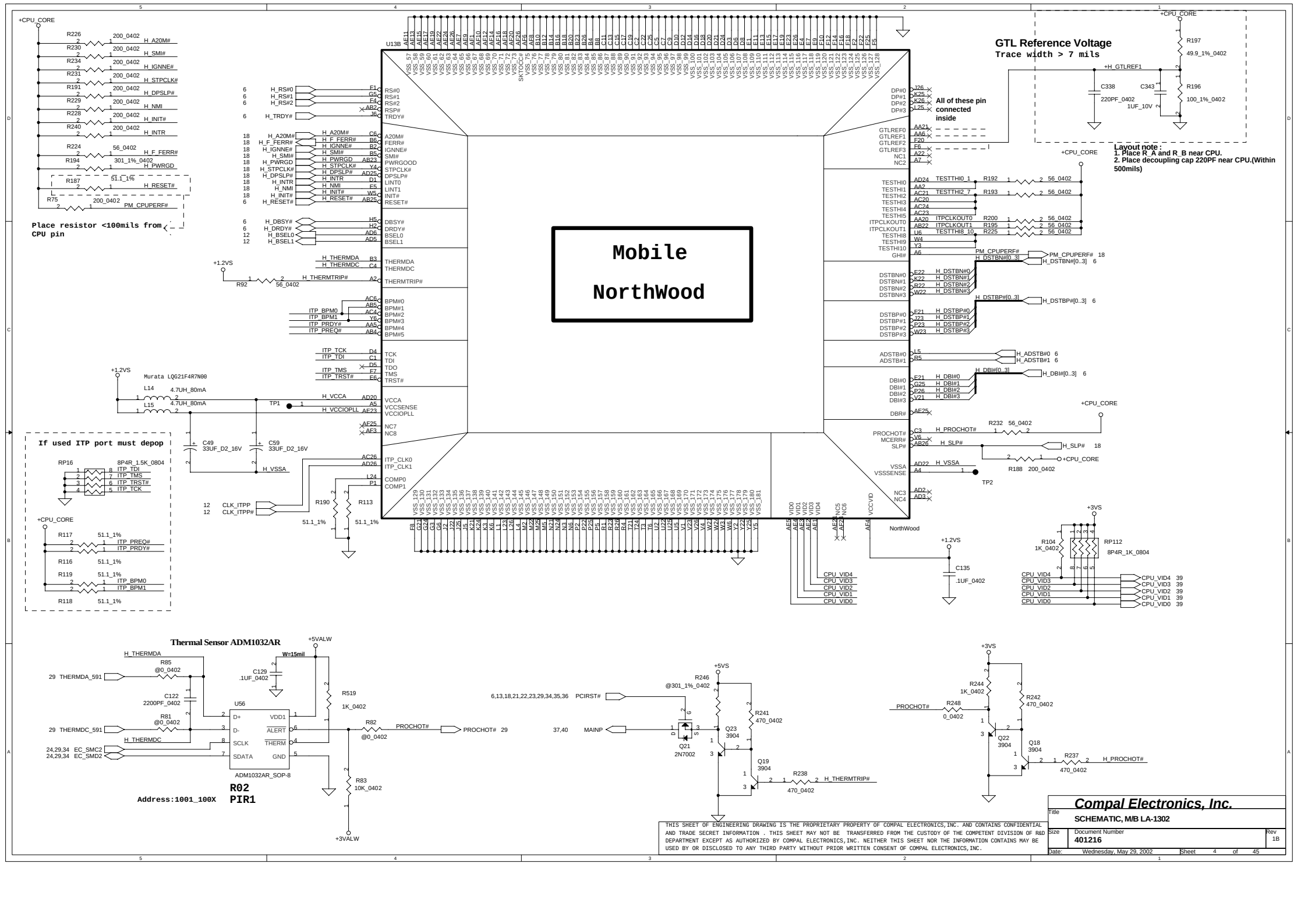
Mobile
NorthWood
GTL Reference Voltage
Trace width > 7 mils
All of these pin connected inside
Layout note :
1. Place R_A and R_B near CPU.
2. Place decoupling cap 220PF near CPU.(Within 500mils)
Place resistor <100mils from CPU pin
If used ITP port must depop
Thermal Sensor ADM1032AR
ADM1032AR_SOP-8
R02
PIR1
Address:1001_100X
Compal Electronics, Inc.
SCHEMATIC, M/B LA-1302
401216
Wednesday, May 29, 2002
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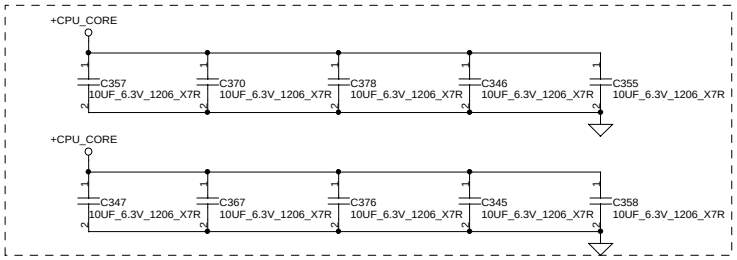
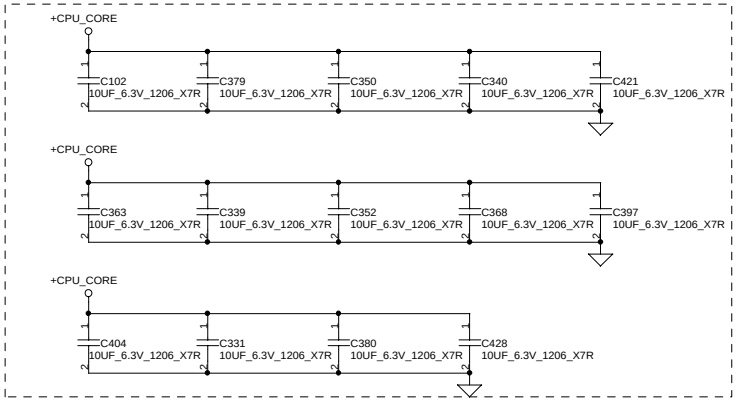
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

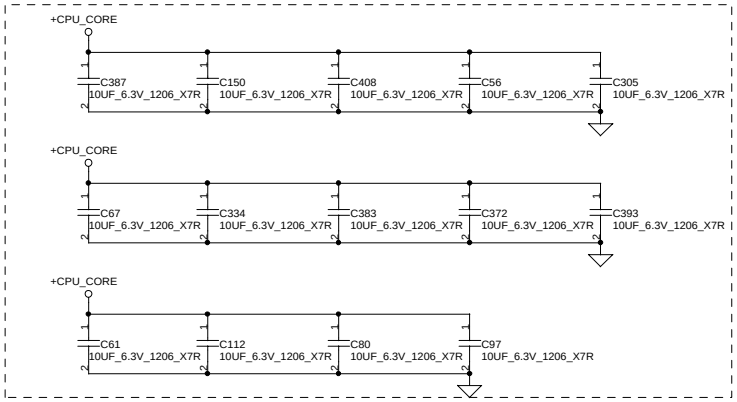
Please place these cap in the socket cavity area



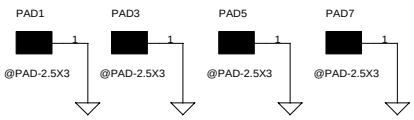
Please place these cap on the socket north side



Please place these cap on the socket south side



EMI Clip PAD for CPU

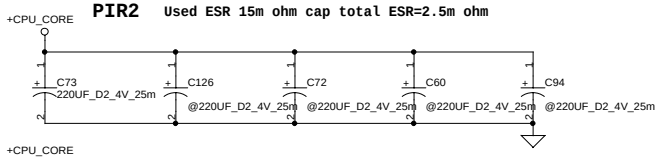


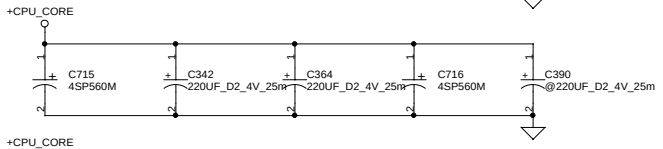
R03 PIR 30

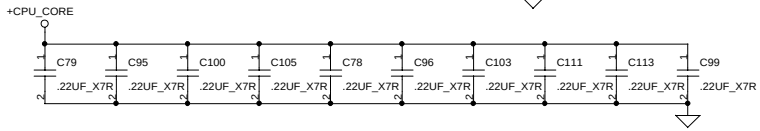
Layout note :

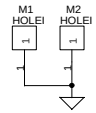
Place close to CPU power and ground pin as possible (<1inch)

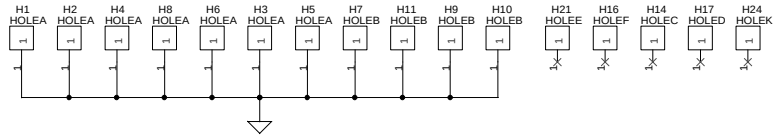
R02
PIR2 **Used ESR 15m ohm cap total ESR=2.5m ohm**



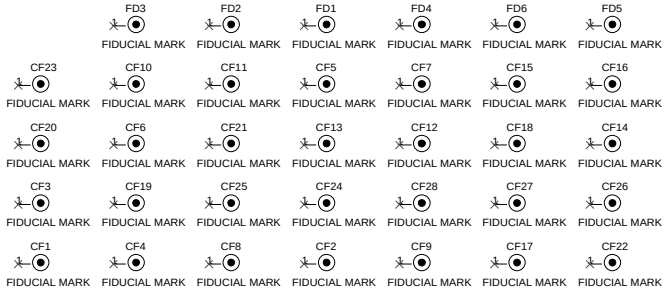


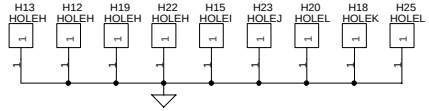






Fiducial Mark





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Title: **SCHEMATIC, M/B LA-1302**		
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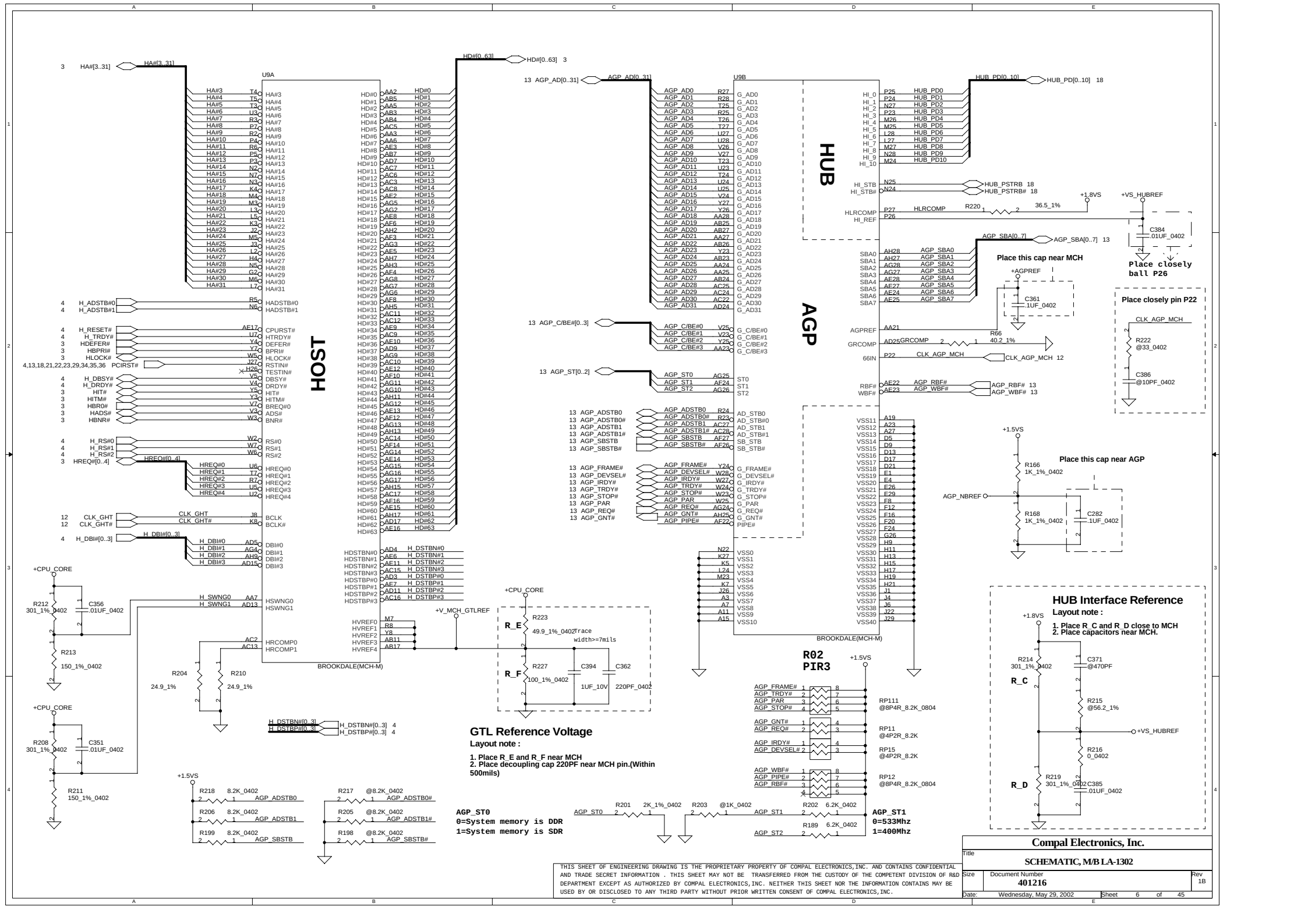
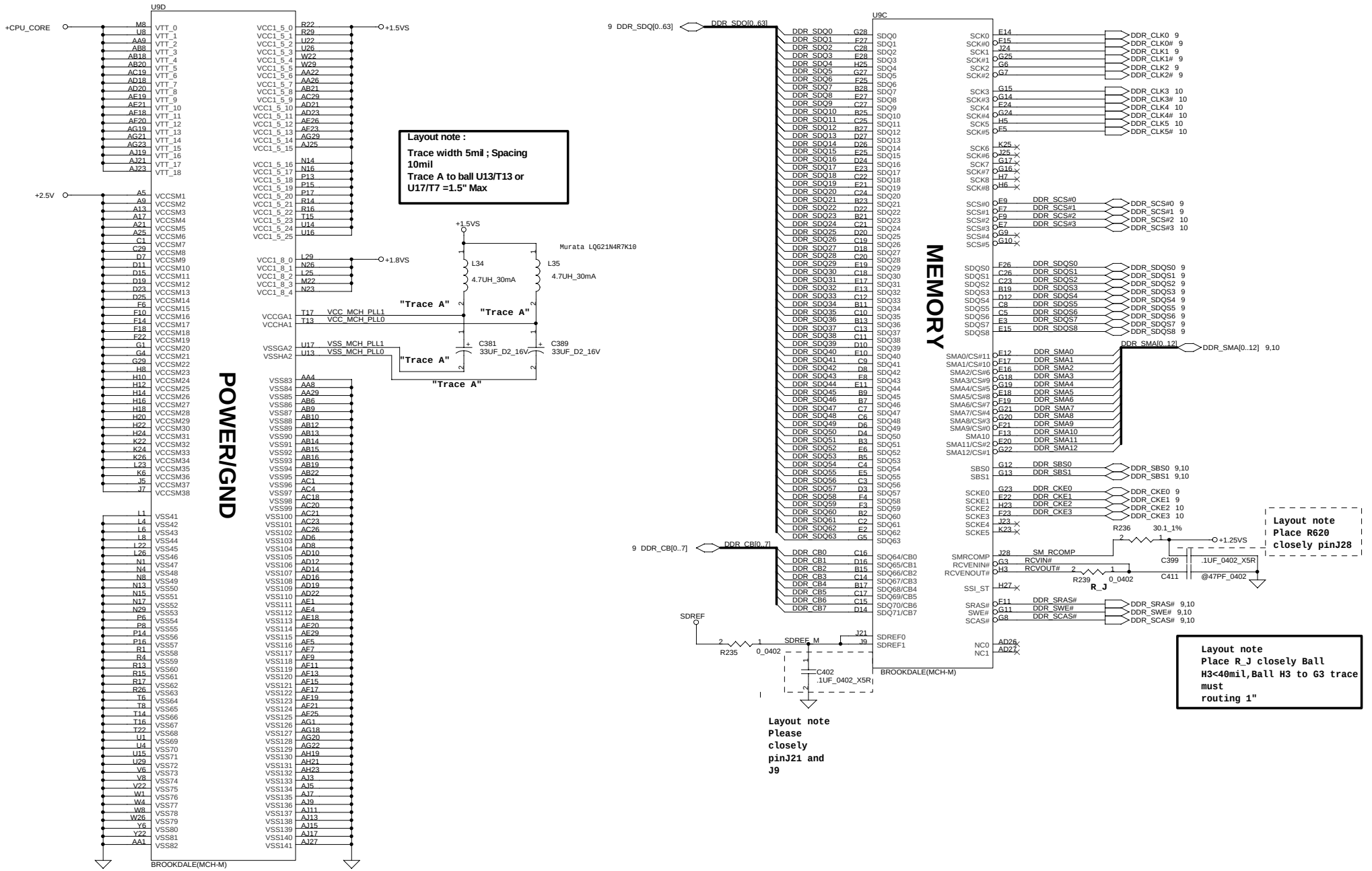


Compal Electronics, Inc.	
Title	SCHEMATIC, M/B LA-1302
Size	Document Number 401216 Rev 1B
Date: Wednesday, May 29, 2002	Sheet 6 of 45



Compal Electronics, Inc.	
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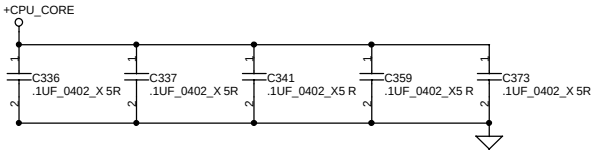
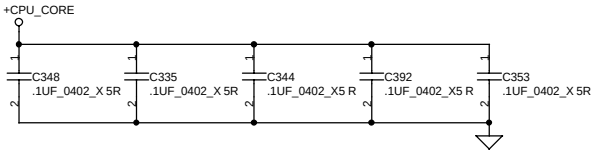
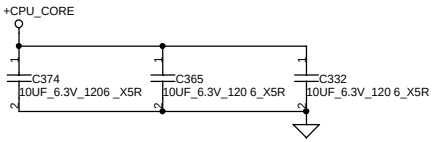
Layout note : Processor system bus

Distribute as close as possible to MCH Processor Quadrant.(between VTTFSB and VSS pin)

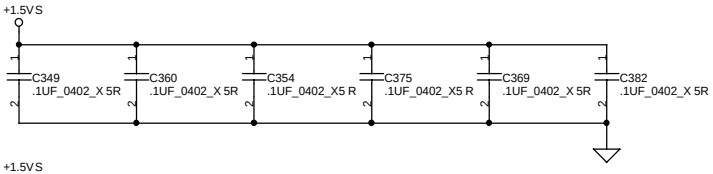


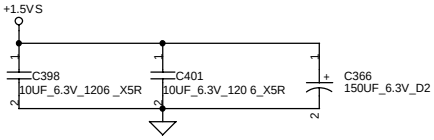




Layout note : AGP/CORE

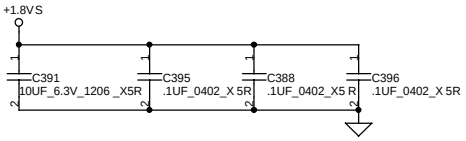
Distribute as close as possible to MCH Processor Quadrant.(between VCCAGP/VCCCORE and VSS pin)





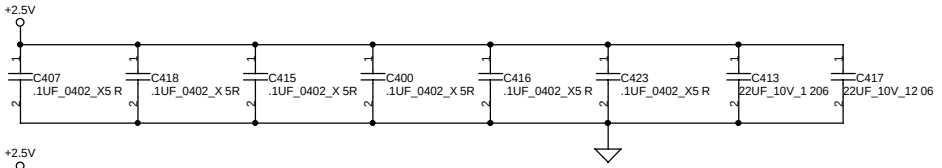
Layout note : Hub-Link

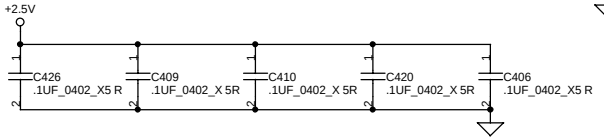
Distribute as close as possible to MCH Processor Quadrant.(between VCCHL and VSS pin)

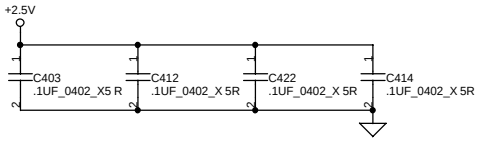


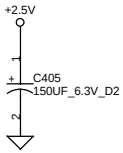
Layout note : DDR Memory interface

Distribute as close as possible to MCH Processor Quadrant.(between VCCSM and VSS pin)









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Layout note

Place these resistor closely DIMM0, all trace length<750mil

RP42 4P2R_22: DDR_SDQ0, DDR_SDQ4 → DDR_DQ0, DDR_DQ4
RP19 4P2R_22: DDR_SDQ1, DDR_SDQ5 → DDR_DQ1, DDR_DQ5
RP43 4P2R_22: DDR_SDQ6, DDR_SDQS0 → DDR_DQ6, DDR_DQS0
RP20 4P2R_22: DDR_SDQ2, DDR_SDQ3 → DDR_DQ2, DDR_DQ3
RP44 4P2R_22: DDR_SDQ8, DDR_SDQ7 → DDR_DQ8, DDR_DQ7
RP21 4P2R_22: DDR_SDQ9, DDR_SDQ12 → DDR_DQ9, DDR_DQ12
RP45 4P2R_22: DDR_SDQS1, DDR_SDQ13 → DDR_DQS1, DDR_DQ13
RP22 4P2R_22: DDR_SDQ10, DDR_SDQ14 → DDR_DQ10, DDR_DQ14
RP46 4P2R_22: DDR_SDQ15, DDR_SDQ11 → DDR_DQ15, DDR_DQ11
RP23 4P2R_22: DDR_SDQ16, DDR_SDQ20 → DDR_DQ16, DDR_DQ20
RP47 4P2R_22: DDR_SDQ21, DDR_SDQ17 → DDR_DQ21, DDR_DQ17
RP24 4P2R_22: DDR_SDQ18, DDR_SDQS2 → DDR_DQ18, DDR_DQS2
RP48 4P2R_22: DDR_SDQ19, DDR_SDQ22 → DDR_DQ19, DDR_DQ22
RP25 4P2R_22: DDR_SDQ24, DDR_SDQ23 → DDR_DQ24, DDR_DQ23
RP49 4P2R_22: DDR_SDQ25, DDR_SDQ28 → DDR_DQ25, DDR_DQ28
RP26 4P2R_22: DDR_SDQS3, DDR_SDQ29 → DDR_DQS3, DDR_DQ29

RP50 4P2R_22: DDR_SDQ30, DDR_SDQ26 → DDR_DQ30, DDR_DQ26
RP27 4P2R_22: DDR_SDQ31, DDR_SDQ27 → DDR_DQ31, DDR_DQ27
RP51 4P2R_22: DDR_CB5, DDR_CB4 → DDR_F_CB5, DDR_F_CB4
RP28 4P2R_22: DDR_CB1, DDR_CB0 → DDR_F_CB1, DDR_F_CB0
RP52 4P2R_22: DDR_CB2, DDR_SDQS8 → DDR_F_CB2, DDR_DQS8
RP29 4P2R_22: DDR_CB3, DDR_CB6 → DDR_F_CB3, DDR_F_CB6
RP53 4P2R_22: DDR_CB7 → DDR_F_CB7
RP40 4P2R_22: DDR_SDQ36, DDR_SDQ32 → DDR_DQ36, DDR_DQ32
RP55 4P2R_22: DDR_SDQ33, DDR_SDQ37 → DDR_DQ33, DDR_DQ37
RP32 4P2R_22: DDR_SDQ38, DDR_SDQS4 → DDR_DQ38, DDR_DQS4
RP56 4P2R_22: DDR_SDQ39, DDR_SDQ34 → DDR_DQ39, DDR_DQ34
RP33 4P2R_22: DDR_SDQ44, DDR_SDQ35 → DDR_DQ44, DDR_DQ35
RP57 4P2R_22: DDR_SDQ45, DDR_SDQ40 → DDR_DQ45, DDR_DQ40
RP34 4P2R_22: DDR_SDQS5, DDR_SDQ41 → DDR_DQS5, DDR_DQ41
RP58 4P2R_22: DDR_SDQ43, DDR_SDQ42 → DDR_DQ43, DDR_DQ42
RP35 4P2R_22: DDR_SDQ47, DDR_SDQ46 → DDR_DQ47, DDR_DQ46

7 DDR_SDQ[0..63] → DDR_SDQ[0..63]
7 DDR_CB[0..7] → DDR_CB[0..7]
7 DDR_SDQS[0..8] → DDR_SDQS[0..8]

RP59 4P2R_22: DDR_SDQ49, DDR_SDQ48 → DDR_DQ49, DDR_DQ48
RP36 4P2R_22: DDR_SDQ53, DDR_SDQ52 → DDR_DQ53, DDR_DQ52
RP60 4P2R_22: DDR_SDQ54, DDR_SDQS6 → DDR_DQ54, DDR_DQS6
RP37 4P2R_22: DDR_SDQ55, DDR_SDQ50 → DDR_DQ55, DDR_DQ50

RP61 4P2R_22: DDR_SDQ56, DDR_SDQ51 → DDR_DQ56, DDR_DQ51
RP38 4P2R_22: DDR_SDQ60, DDR_SDQ57 → DDR_DQ60, DDR_DQ57
RP62 4P2R_22: DDR_SDQS7, DDR_SDQ61 → DDR_DQS7, DDR_DQ61
RP39 4P2R_22: DDR_SDQ62, DDR_SDQ58 → DDR_DQ62, DDR_DQ58
RP63 4P2R_22: DDR_SDQ63, DDR_SDQ59 → DDR_DQ63, DDR_DQ59

+2.5V
+3VS
JP17
DDR-SODIMM_200_Normal

DDR_DQ4 DDR_DQ5 DDR_DQS0 DDR_DQ3 DDR_DQ7 DDR_DQ12 DDR_DQ13 DDR_DQS1 DDR_DQ14 DDR_DQ11
7 DDR_CLK1 7 DDR_CLK1#
DDR_DQ20 DDR_DQ17 DDR_DQS2 DDR_DQ22 DDR_DQ23 DDR_DQ28 DDR_DQ29 DDR_DQS3 DDR_DQ26 DDR_DQ27 DDR_F_CB4 DDR_F_CB0 DDR_DQS8 DDR_F_CB6 DDR_F_CB7
7 DDR_CLK0 7 DDR_CLK0# 7 DDR_CKE1
DDR_SMA12 DDR_SMA9 DDR_SMA7 DDR_SMA5 DDR_SMA3 DDR_SMA1 DDR_SMA10 DDR_SBS0 DDR_SWE# DDR_SCS#0
7 DDR_SCS#0
DDR_DQ36 DDR_DQ33 DDR_DQS4 DDR_DQ38 DDR_DQ39 DDR_DQ44 DDR_DQ45 DDR_DQS5 DDR_DQ43 DDR_DQ47
DDR_DQ49 DDR_DQ53 DDR_DQS6 DDR_DQ54 DDR_DQ55 DDR_DQ56 DDR_DQ60 DDR_DQS7 DDR_DQ62 DDR_DQ63
10,12 DIMM_SMDATA 10,12 DIMM_SMCLK +3VS

DDR_DQ0 DDR_DQ1 DDR_DQ6 DDR_DQ2 DDR_DQ8 DDR_DQ9 DDR_DQ10 DDR_DQ15
DDR_DQ16 DDR_DQ21 DDR_DQ18 DDR_DQ19 DDR_DQ24 DDR_DQ25 DDR_DQ30 DDR_DQ31 DDR_F_CB5 DDR_F_CB1 DDR_F_CB2 DDR_F_CB3
DDR_CKE0 7 DDR_CKE0
DDR_SMA11 DDR_SMA8 DDR_SMA6 DDR_SMA4 DDR_SMA2 DDR_SMA0 DDR_SBS1 DDR_SRAS# DDR_SCAS# DDR_SCS#1
DDR_SCS#1 7
DDR_DQ32 DDR_DQ37 DDR_DQ34 DDR_DQ35 DDR_DQ40 DDR_DQ41 DDR_DQ42 DDR_DQ46
DDR_CLK2# 7 DDR_CLK2 7
DDR_DQ48 DDR_DQ52 DDR_DQ50 DDR_DQ51 DDR_DQ57 DDR_DQ61 DDR_DQ58 DDR_DQ59

SDREF_DIMM — C184 .1UF_0402 — R136 0_0402 → SDREF

LENGTH < 3 "

SDREF width 12 mil, space 12 mil

DDR_DQ[0..63] → DDR_DQ[0..63] 10
DDR_F_CB[0..7] → DDR_F_CB[0..7] 10
DDR_DQS[0..8] → DDR_DQS[0..8] 10

DDR_SMA[0..12] 7,10

RP30 4P2R_10: DDR_SMA12, DDR_SMA9 → DDR_F_SMA12, DDR_F_SMA9
RP31 4P2R_10: DDR_SMA7, DDR_SMA8 → DDR_F_SMA7, DDR_F_SMA8
RP41 4P2R_10: DDR_SMA10, DDR_SMA0 → DDR_F_SMA10, DDR_F_SMA0
RP54 4P2R_10: DDR_SMA2, DDR_SMA5 → DDR_F_SMA2, DDR_F_SMA5
RP18 4P2R_10: DDR_SMA1, DDR_SMA3 → DDR_F_SMA1, DDR_F_SMA3
RP115 4P2R_10: DDR_SMA6, DDR_SMA4 → DDR_F_SMA6, DDR_F_SMA4
R133 10_0402: DDR_SMA11 → DDR_F_SMA11

10 DDR_F_SMA[0..12]

Layout note

Place these resistor closely DIMM0, all trace length<=750mil

Layout note

Place these resistor closely DIMM0, all trace length Max=1.3"

+1.25VS

RP127 4P2R_56: DDR_CKE0, DDR_CKE1
RP124 4P2R_56: DDR_SCS#0, DDR_SCS#1

Layout note

Place these resistor closely DIMM0, all trace length<=750mil

7,10 DDR_SBS0 7,10 DDR_SWE# → RP114 4P2R_10: DDR_SBS0, DDR_SWE# → DDR_F_SBS0, DDR_F_SWE# → DDR_F_SBS0 10, DDR_F_SWE# 10
7,10 DDR_SCAS# 7,10 DDR_SRAS# → RP113 4P2R_10: DDR_SCAS#, DDR_SRAS# → DDR_F_SCAS#, DDR_F_SRAS# → DDR_F_SCAS# 10, DDR_F_SRAS# 10
7,10 DDR_SBS1 → R134 10_0402: DDR_SBS1 → DDR_F_SBS1 → DDR_F_SBS1 10

DIMM0

top side

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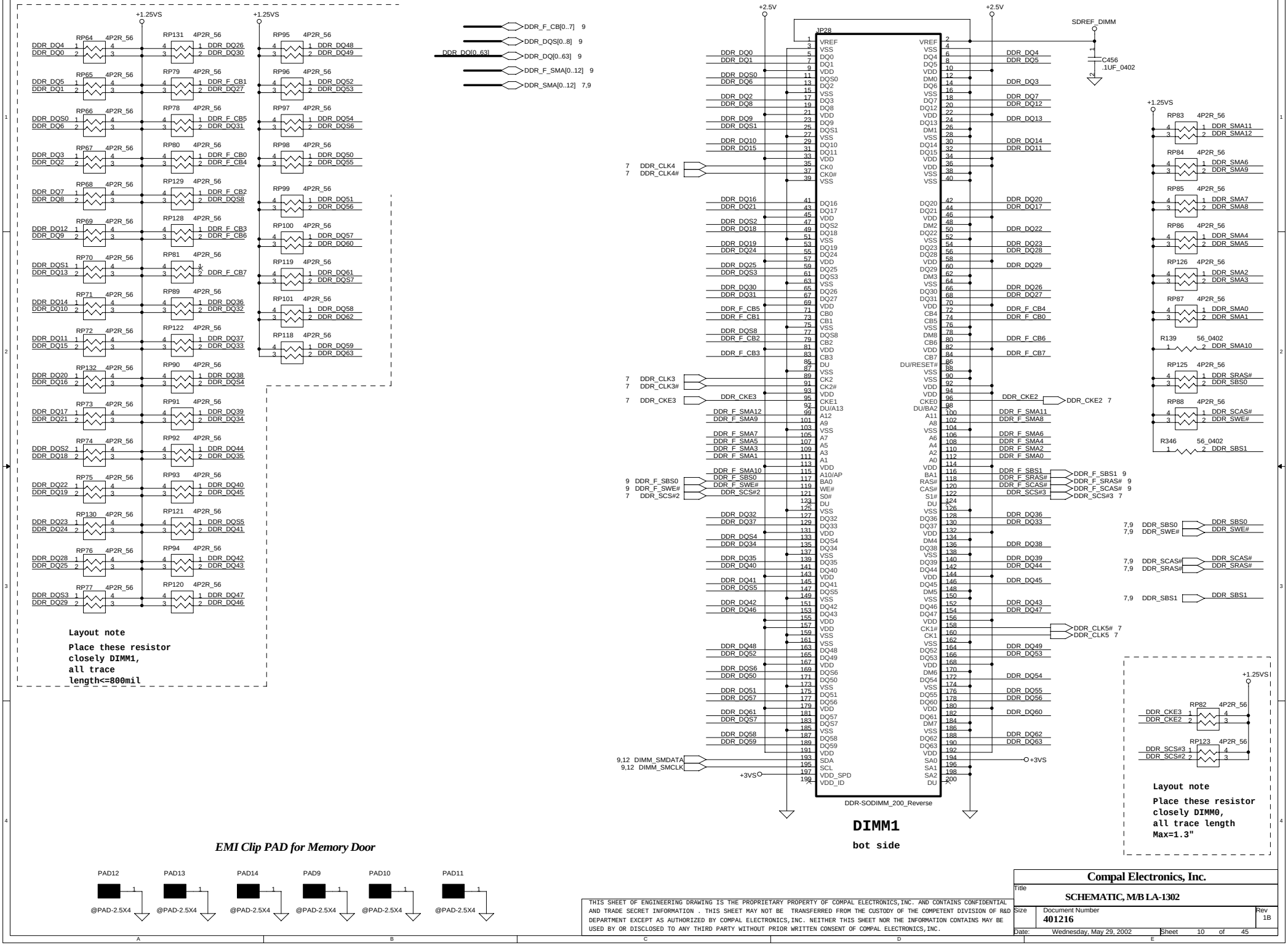

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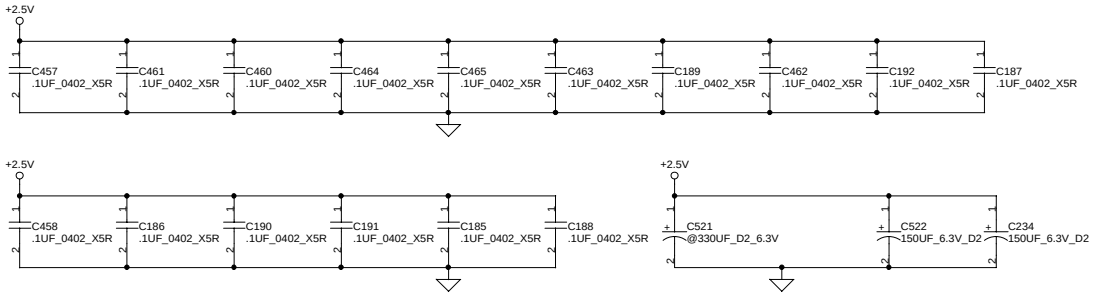
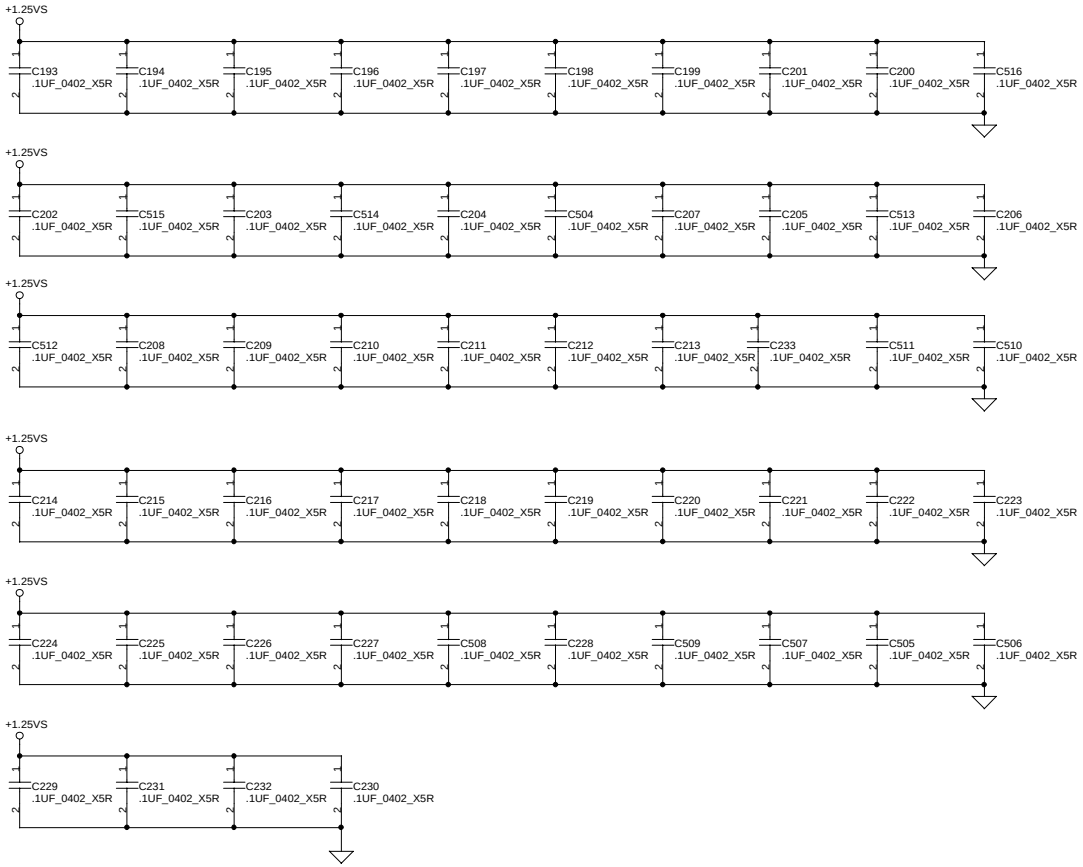
Layout note :

Distribute as close as possible to DDR-SODIMM.



Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25V



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Title: **SCHEMATIC, M/B LA-1302**

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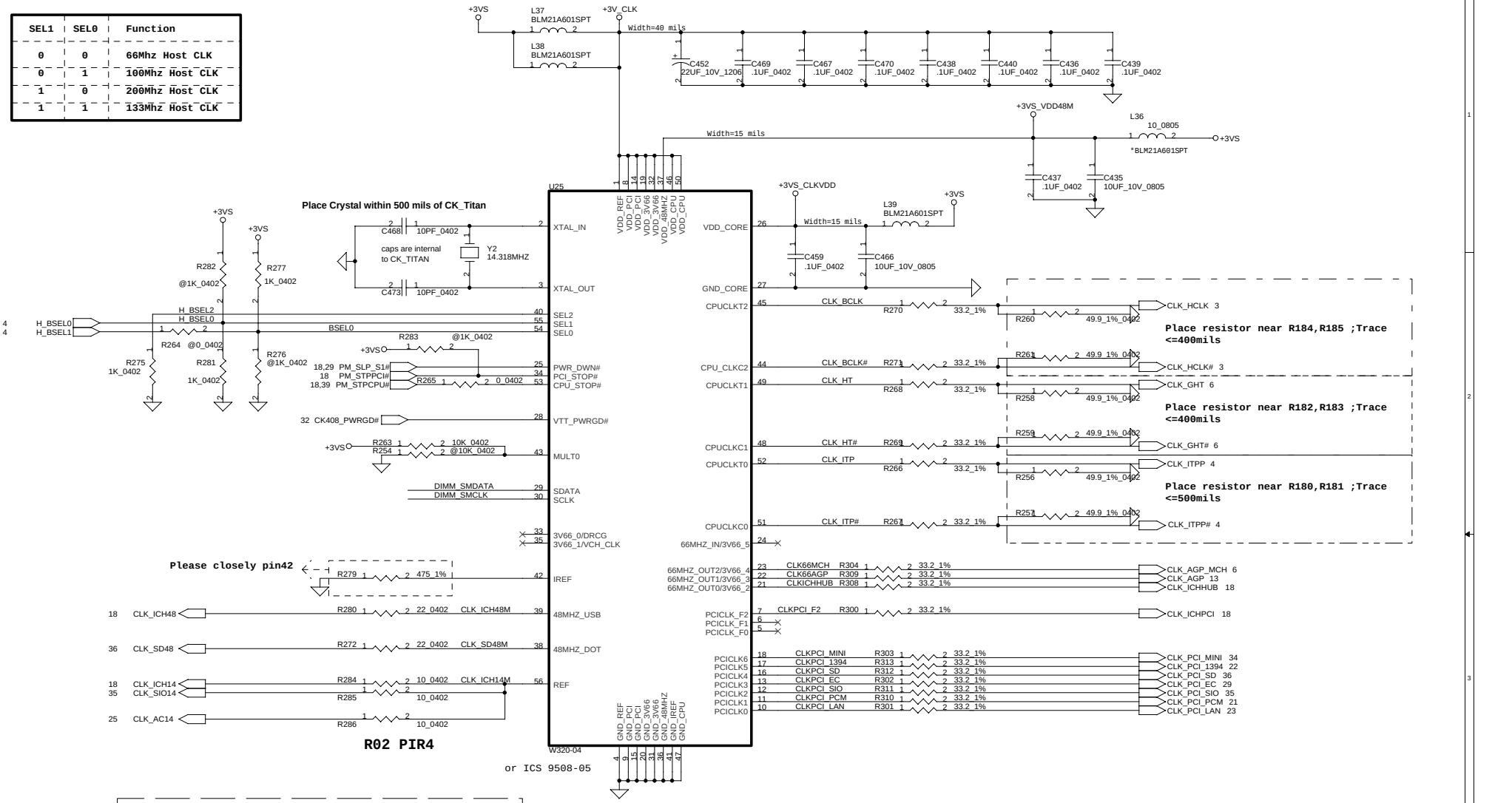
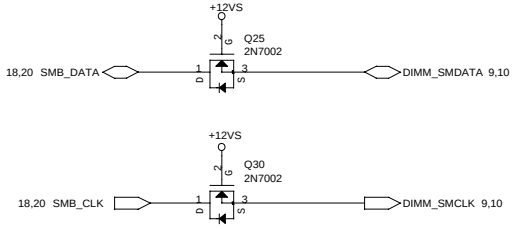
SEL1	SEL0	Function
0	0	66Mhz Host CLK
0	1	100Mhz Host CLK
1	0	200Mhz Host CLK
1	1	133Mhz Host CLK



Note:
CPU_CLK[2:0] needs to be running in C3, C4.



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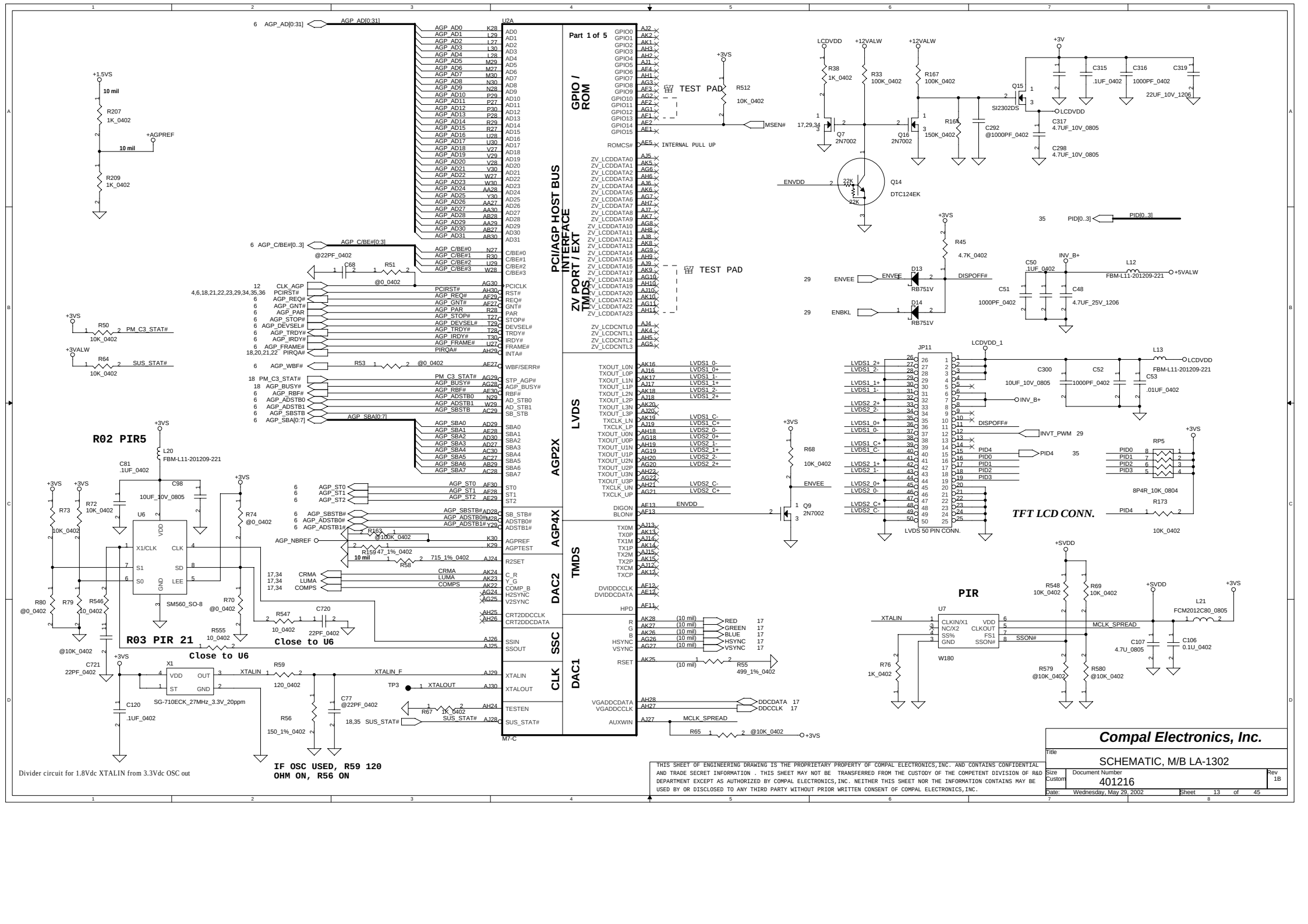

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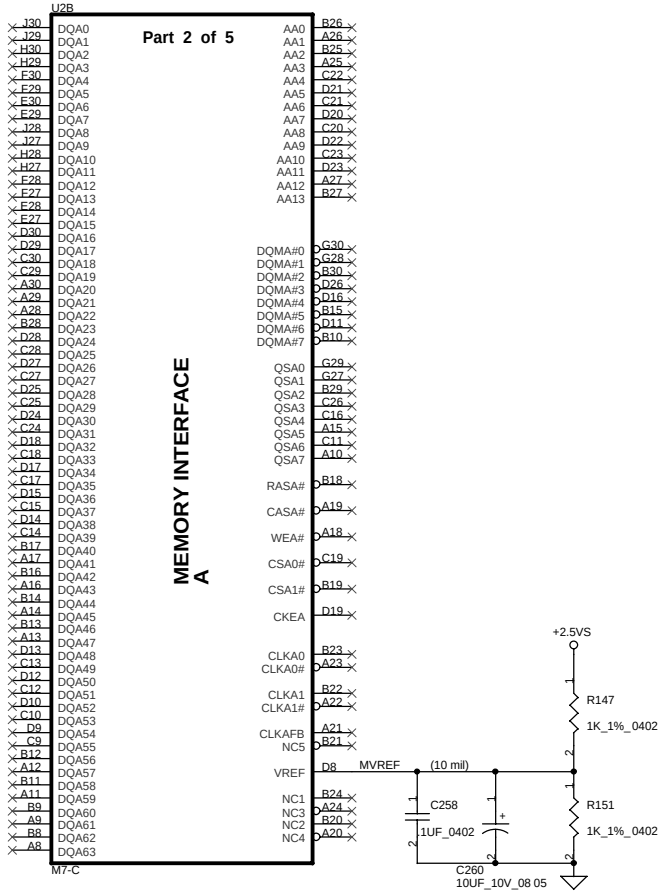
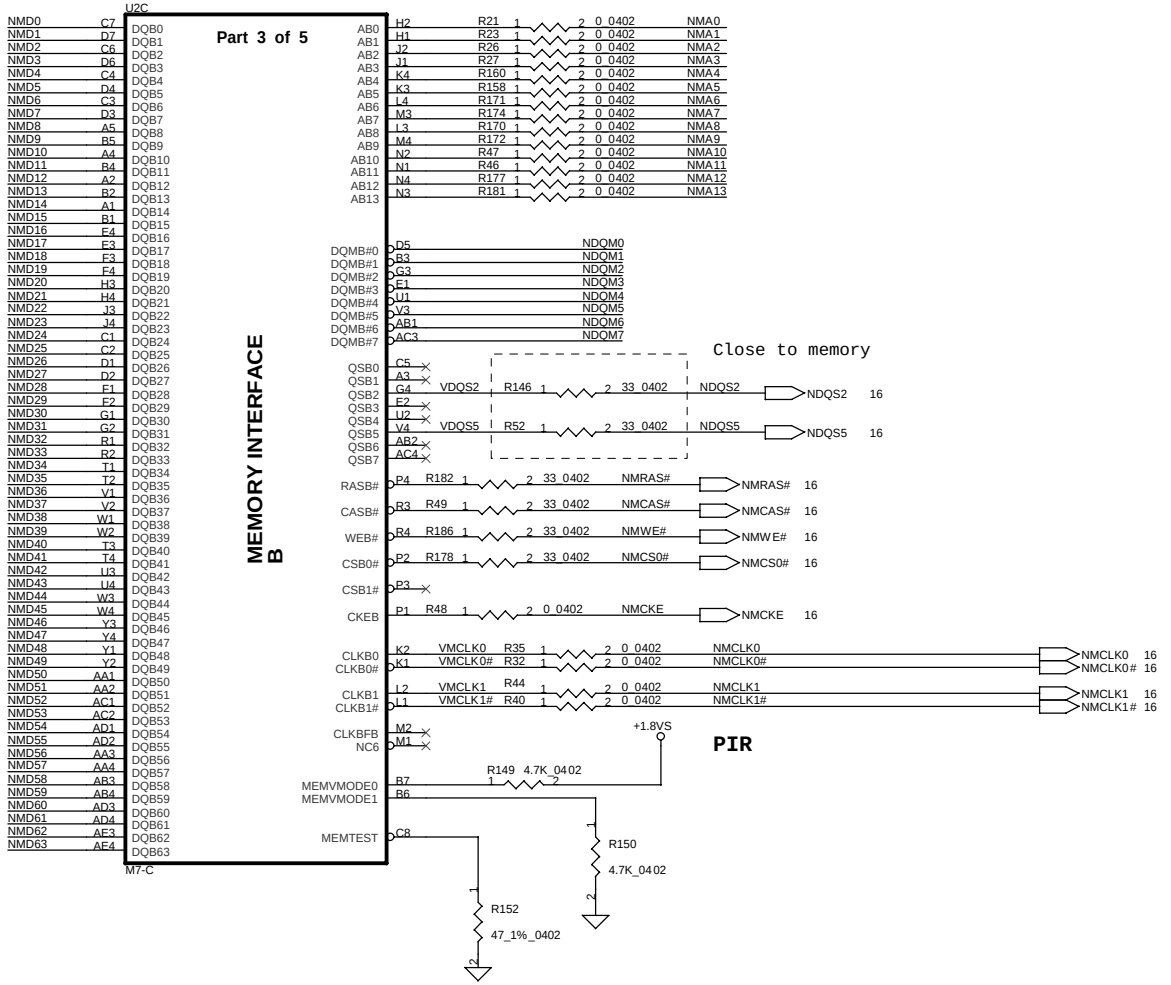
MEMORY INTERFACE

NMD[0:63] → NMD[0:63] 16
NMA[0:13] → NMA[0:13] 16
NDQM[0:7] → NDQM[0:7] 16





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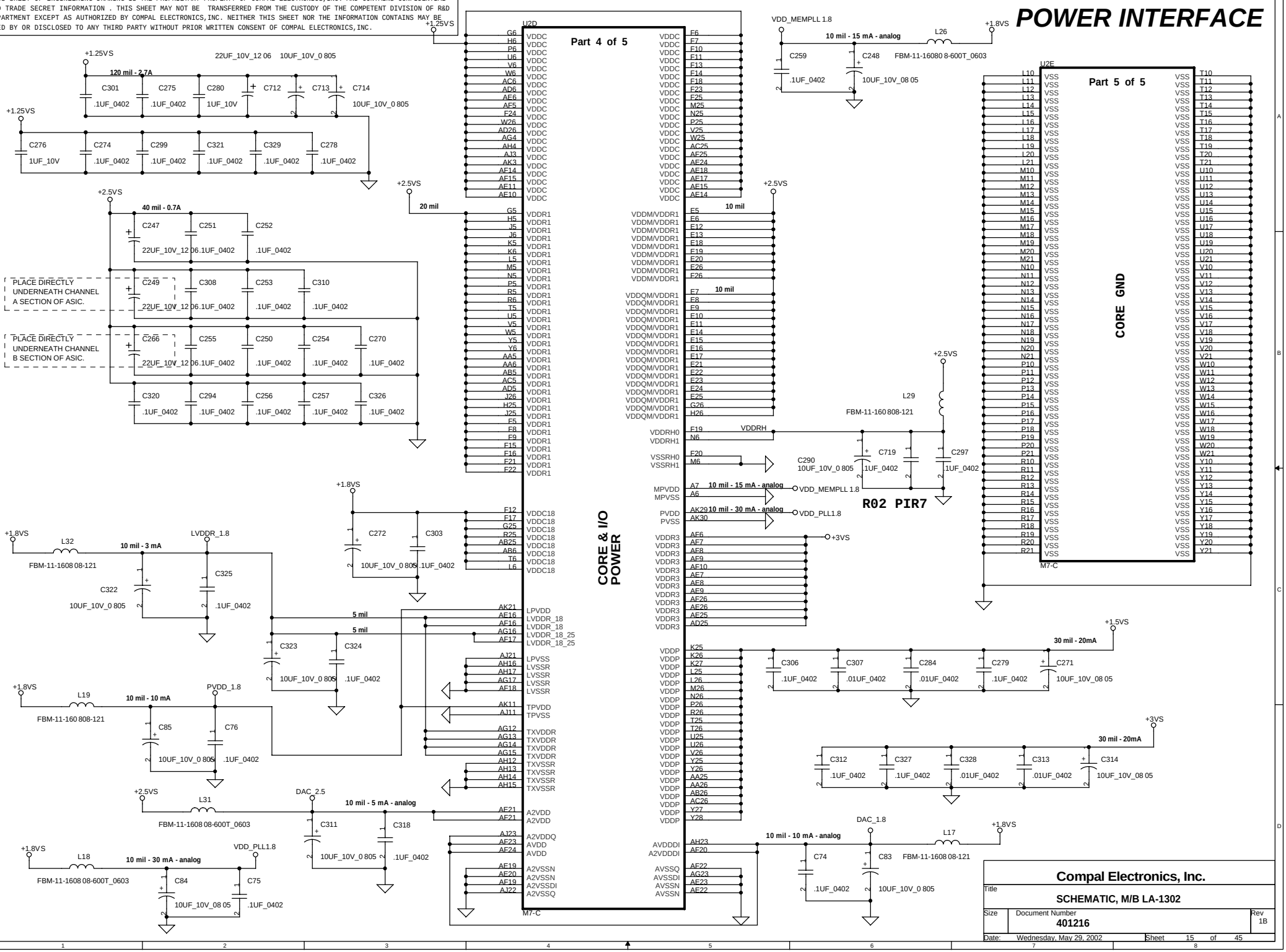
POWER INTERFACE



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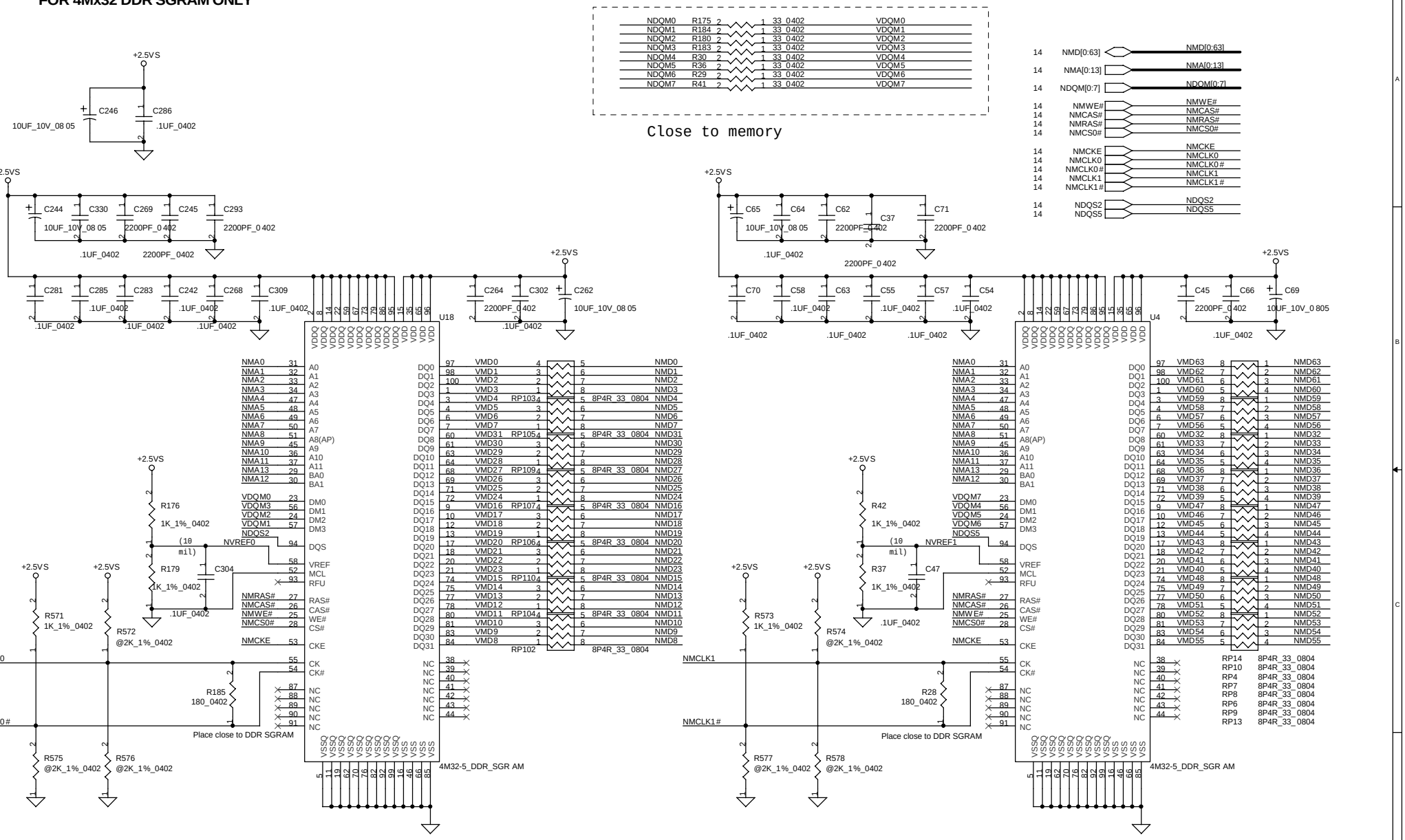
NOTE : MA11 CONNECTION REQUIRED FOR 4Mx32 DDR SGRAM ONLY

DDR SGRAM



NOTE : Resistors of NDQS0 and NDQS4 closed to the 94 pin of every DDR SGRAM

16/32MB DDR 2/4MX32 SGRAM

16MB 64 BIT INTERFACE WITH TWO PIECES 2MX32
32MB 64 BIT INTERFACE WITH TWO PIECES 4MX32

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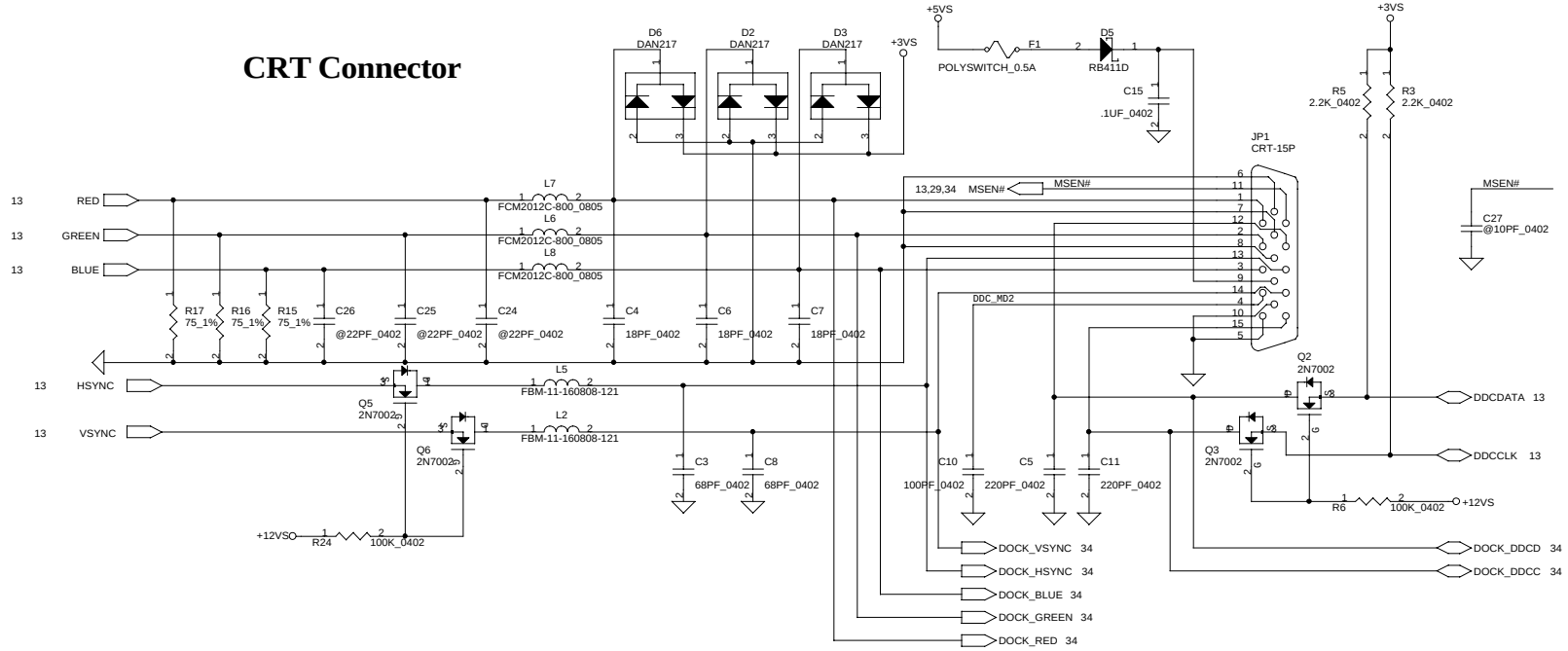
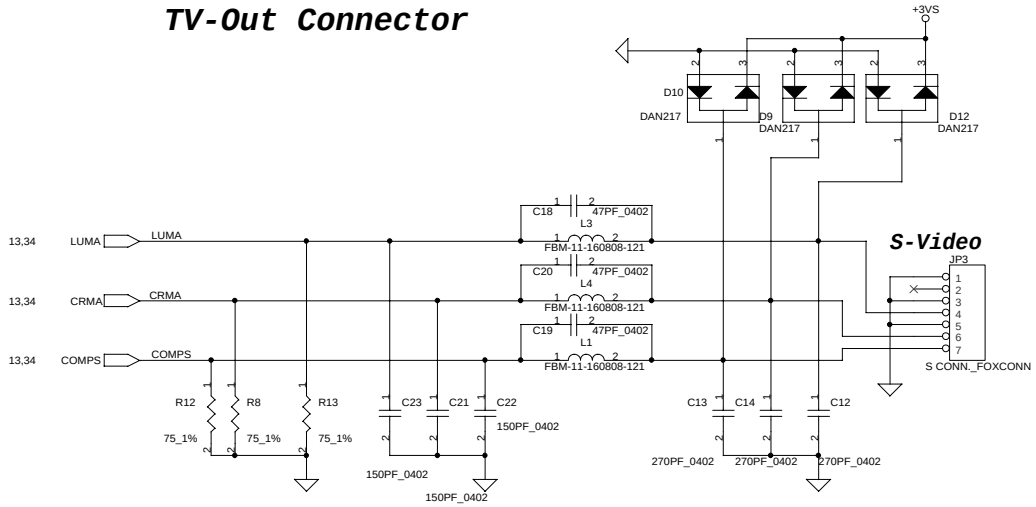
CRT Connector



TV-Out Connector



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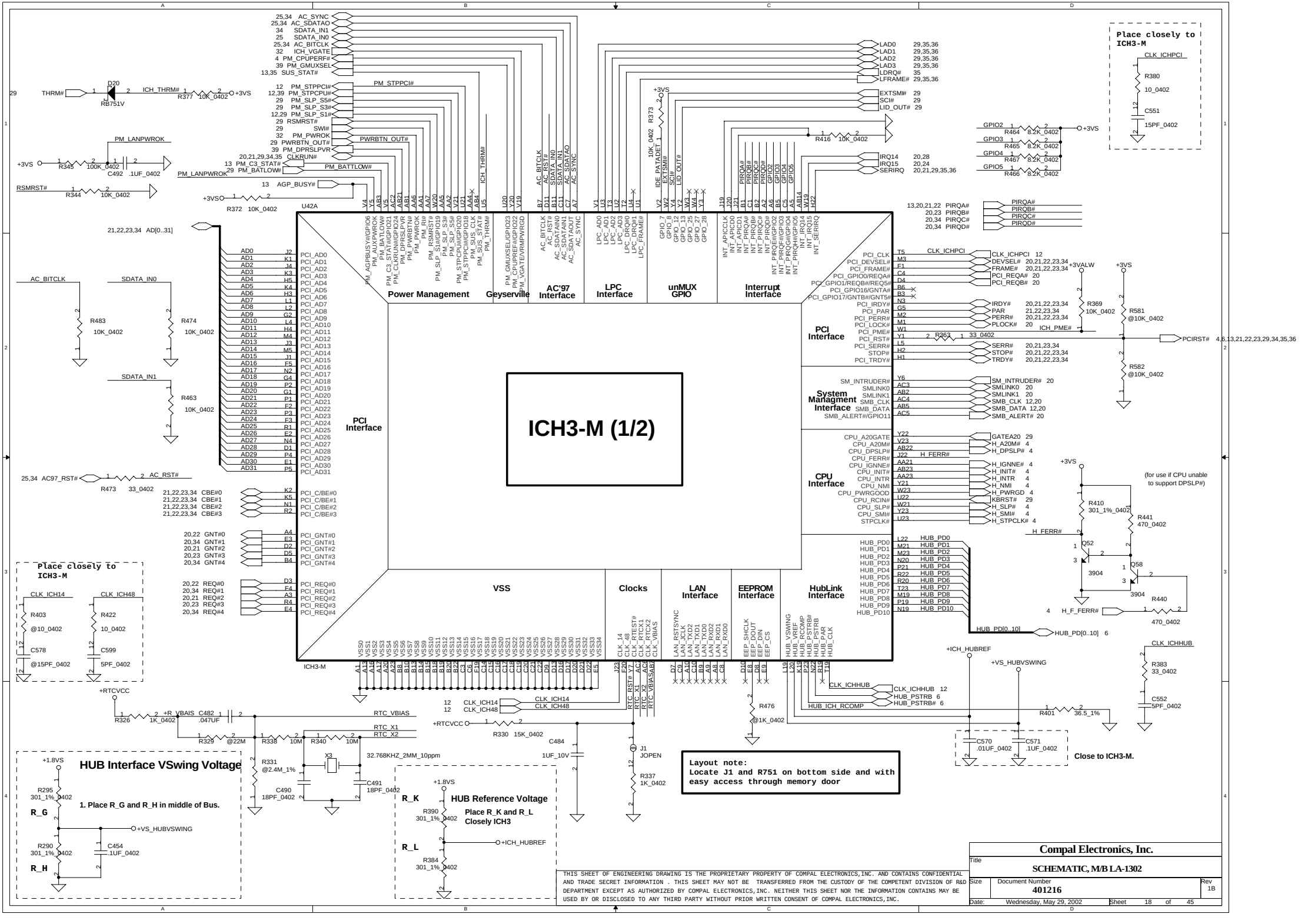

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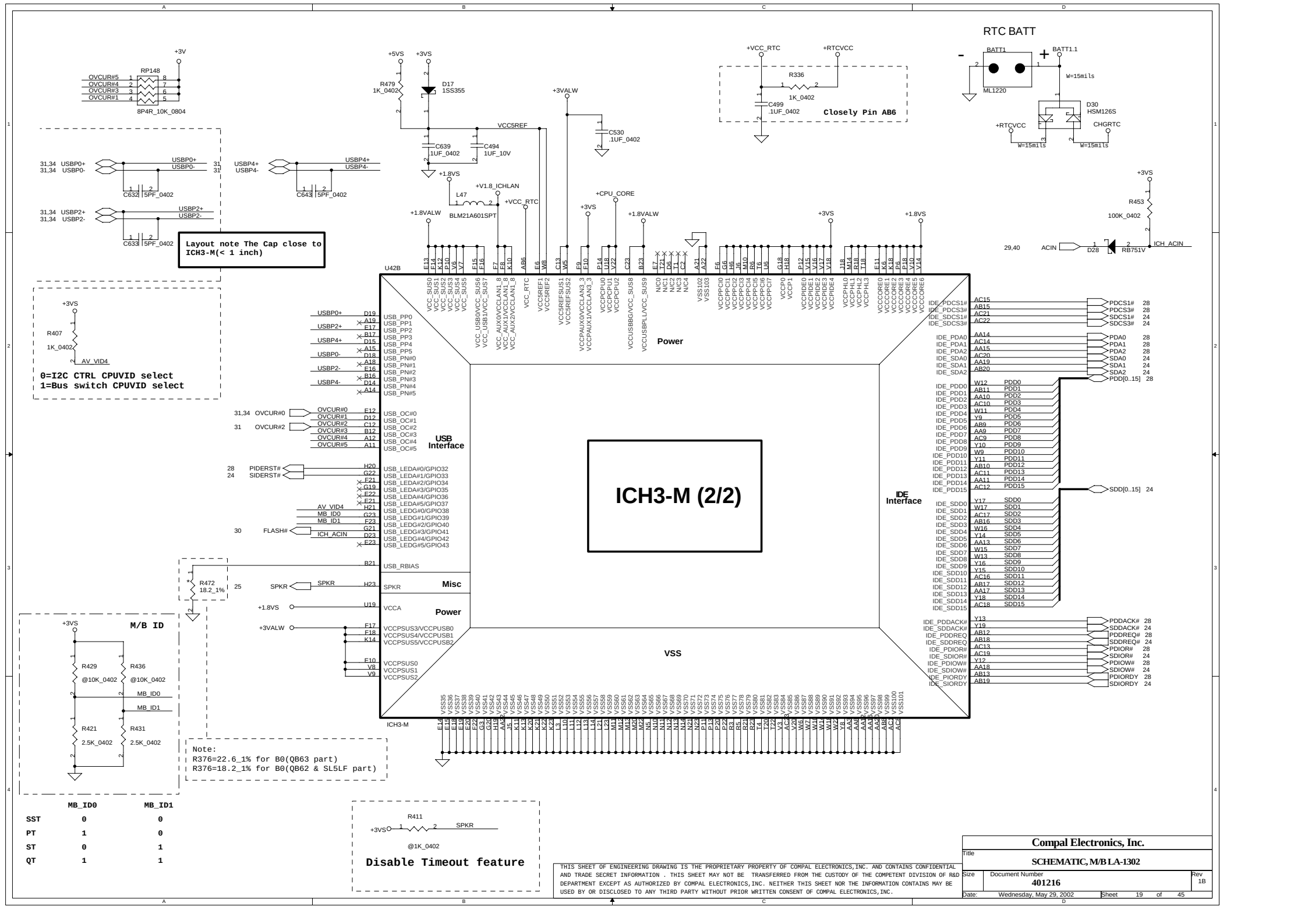
RTC BATT
BATT1
BATT1.1
ML1220
W=15mils
D30
HSM126S
CHGRTC
+RTCVCC
+VCC_RTC
R336
1K_0402
C499
.1UF_0402
Closely Pin AB6
RP148
OVCUR#5
OVCUR#4
OVCUR#3
OVCUR#1
8P4R_10K_0804
R479
1K_0402
D17
1SS355
C639
.1UF_0402
C494
1UF_10V
C530
.1UF_0402
VCC5REF
+5VS
+3VS
+3VALW
+1.8VS
+1.8VALW
+V1.8_ICHLAN
L47
BLM21A601SPT
+CPU_CORE
USBP0+
USBP0-
USBP2+
USBP2-
USBP4+
USBP4-
C632
C633
C643
5PF_0402
Layout note The Cap close to ICH3-M(< 1 inch)
R453
100K_0402
ACIN
D28
RB751V
ICH_ACIN
R407
1K_0402
AV_VID4
0=I2C CTRL CPUVID select
1=Bus switch CPUVID select
U42B
ICH3-M (2/2)
Power
VSS
USB Interface
IDE Interface
Misc
Power
R472
18.2_1%
SPKR
M/B ID
R429
@10K_0402
R436
@10K_0402
MB_ID0
MB_ID1
R421
2.5K_0402
R431
2.5K_0402
MB_ID0 MB_ID1
SST 0 0
PT 1 0
ST 0 1
QT 1 1
Note:
R376=22.6_1% for B0(QB63 part)
R376=18.2_1% for B0(QB62 & SL5LF part)
R411
@1K_0402
Disable Timeout feature
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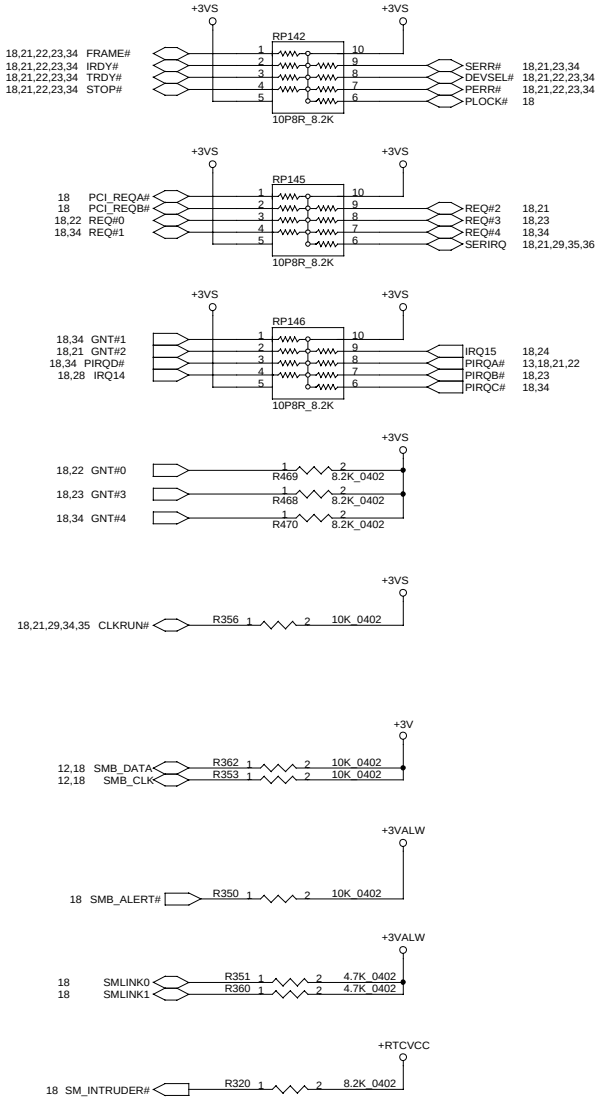

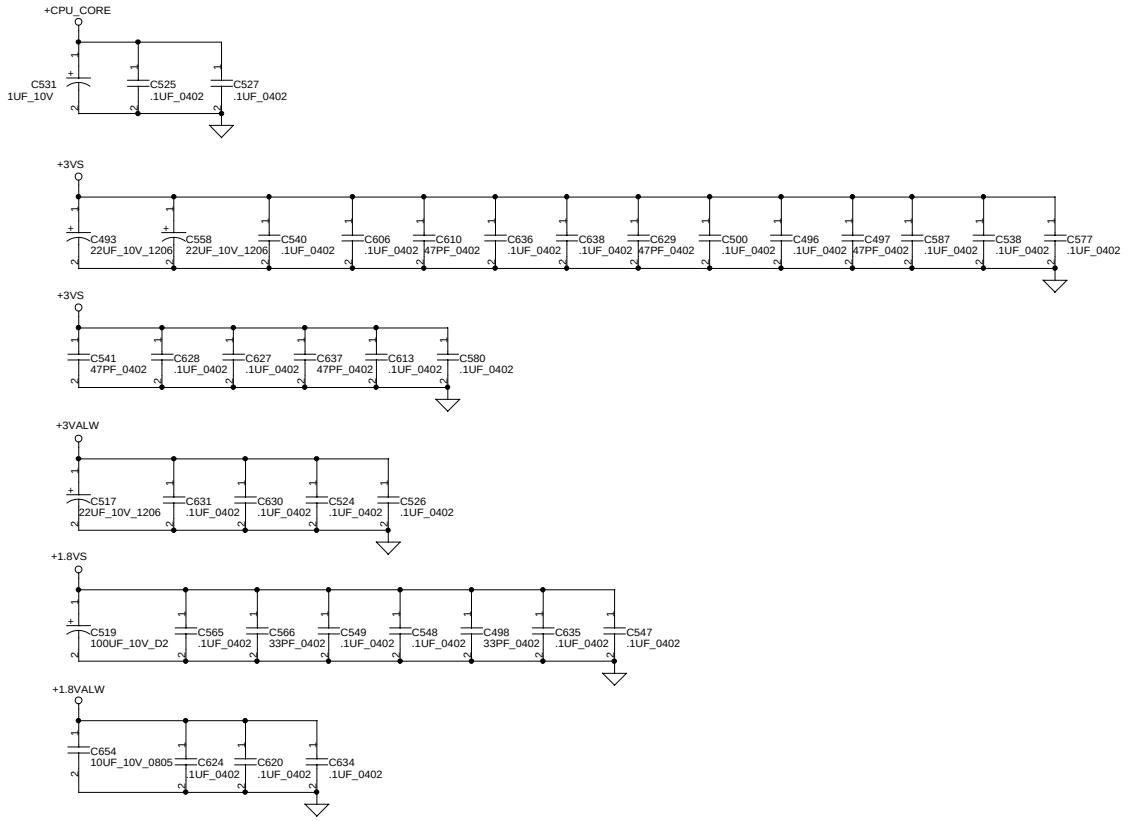

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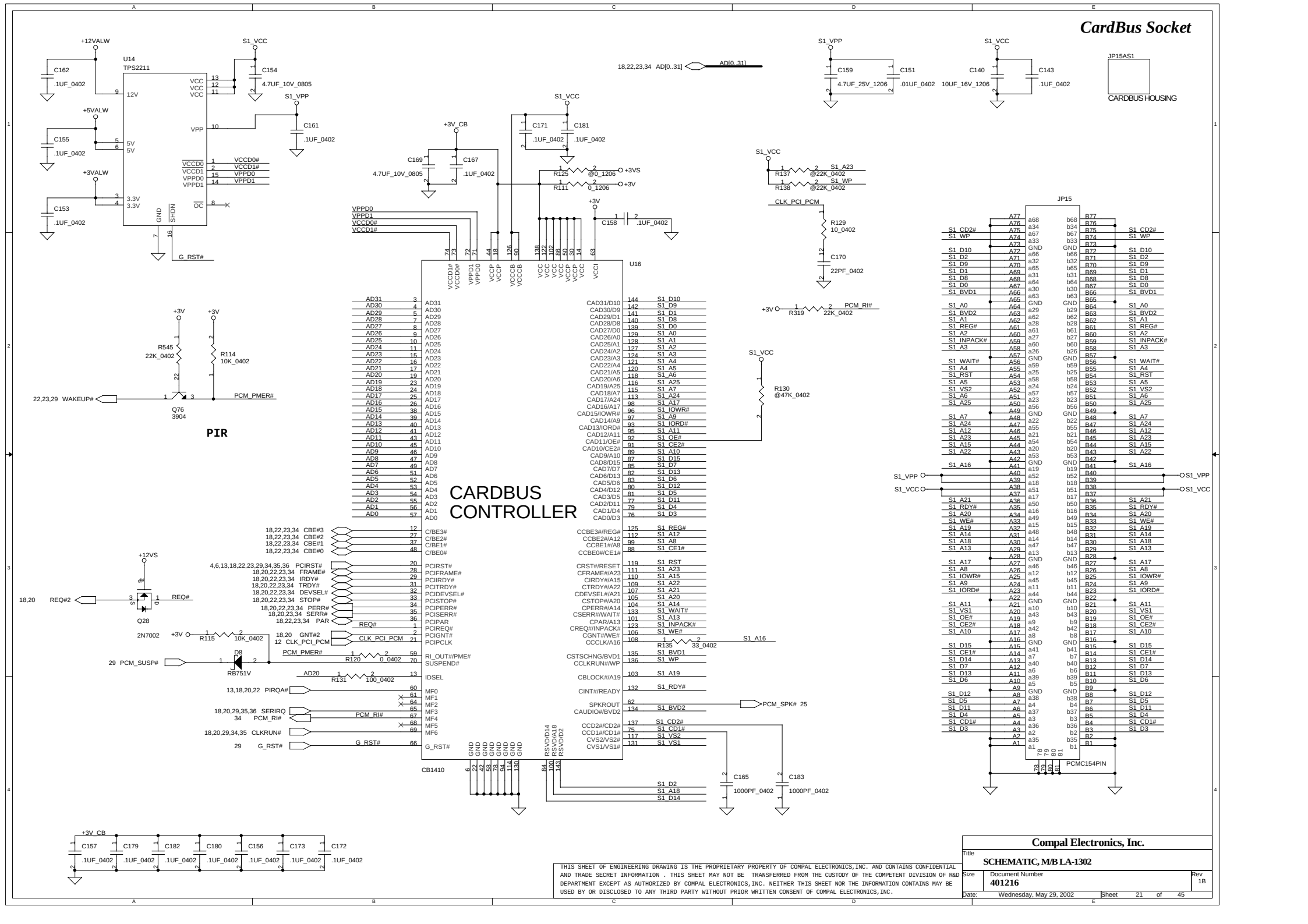
CardBus Socket



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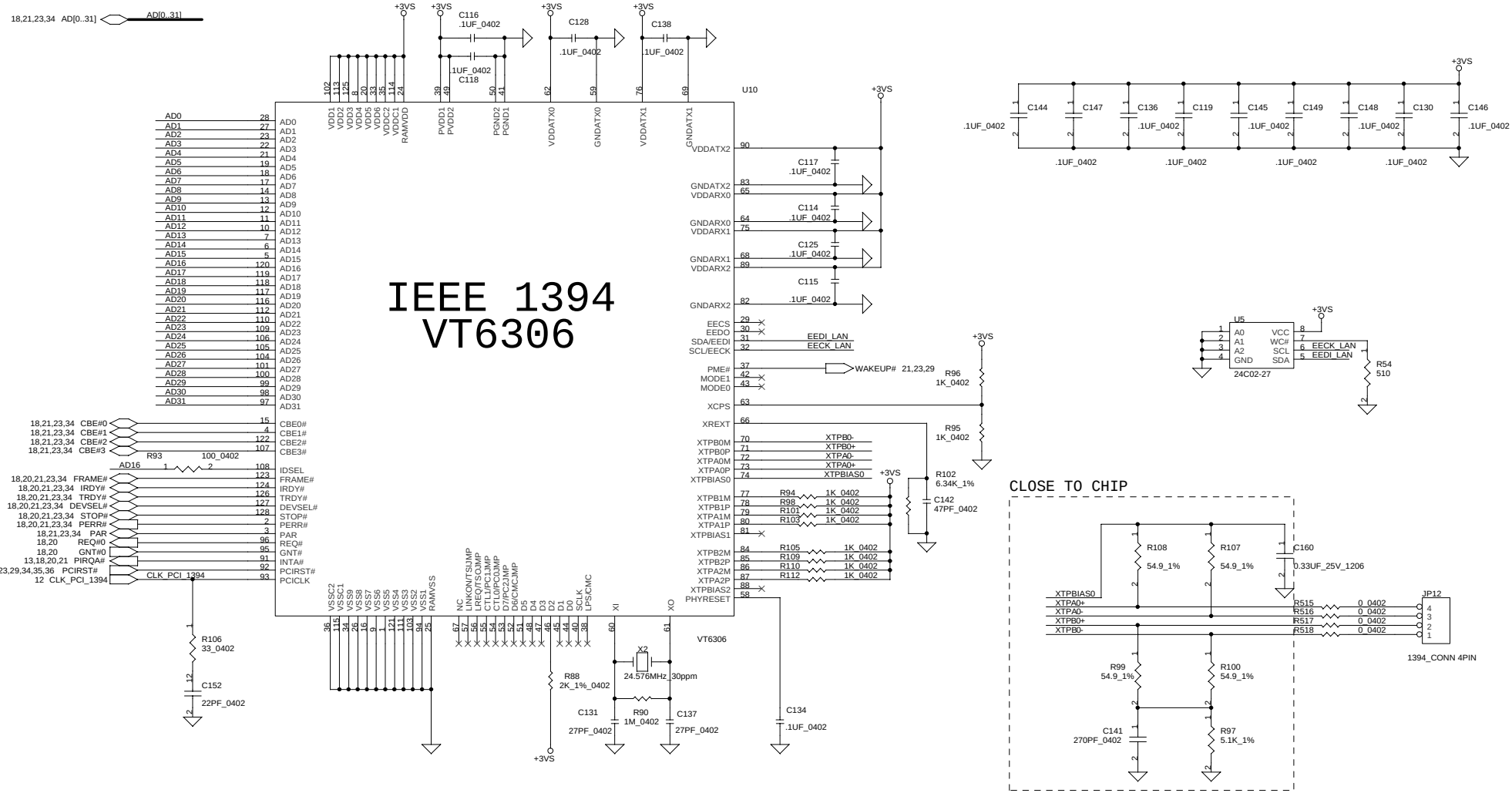

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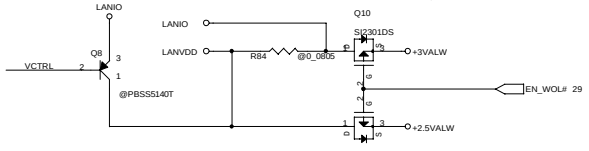
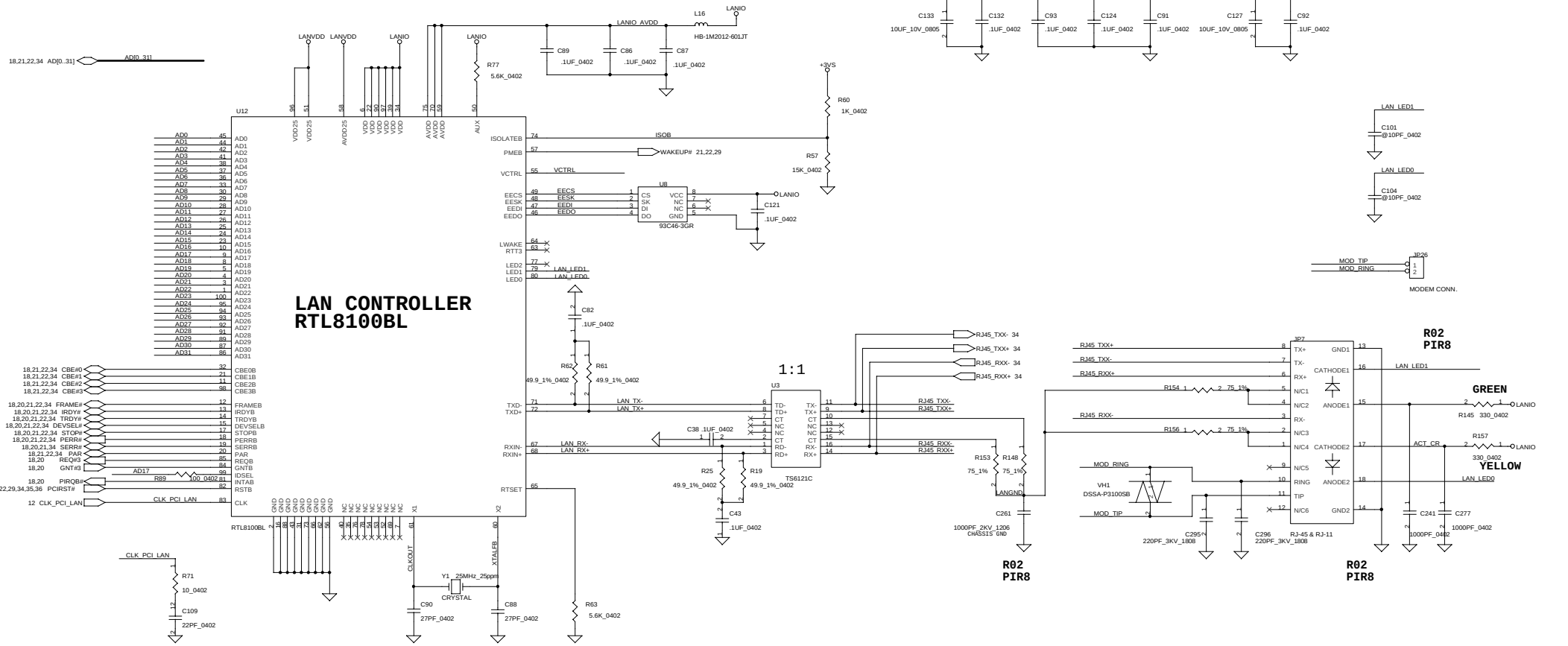
LAN Realtek RTL8100

PMOS , Rdson = 0.19@Vgs=2.5V





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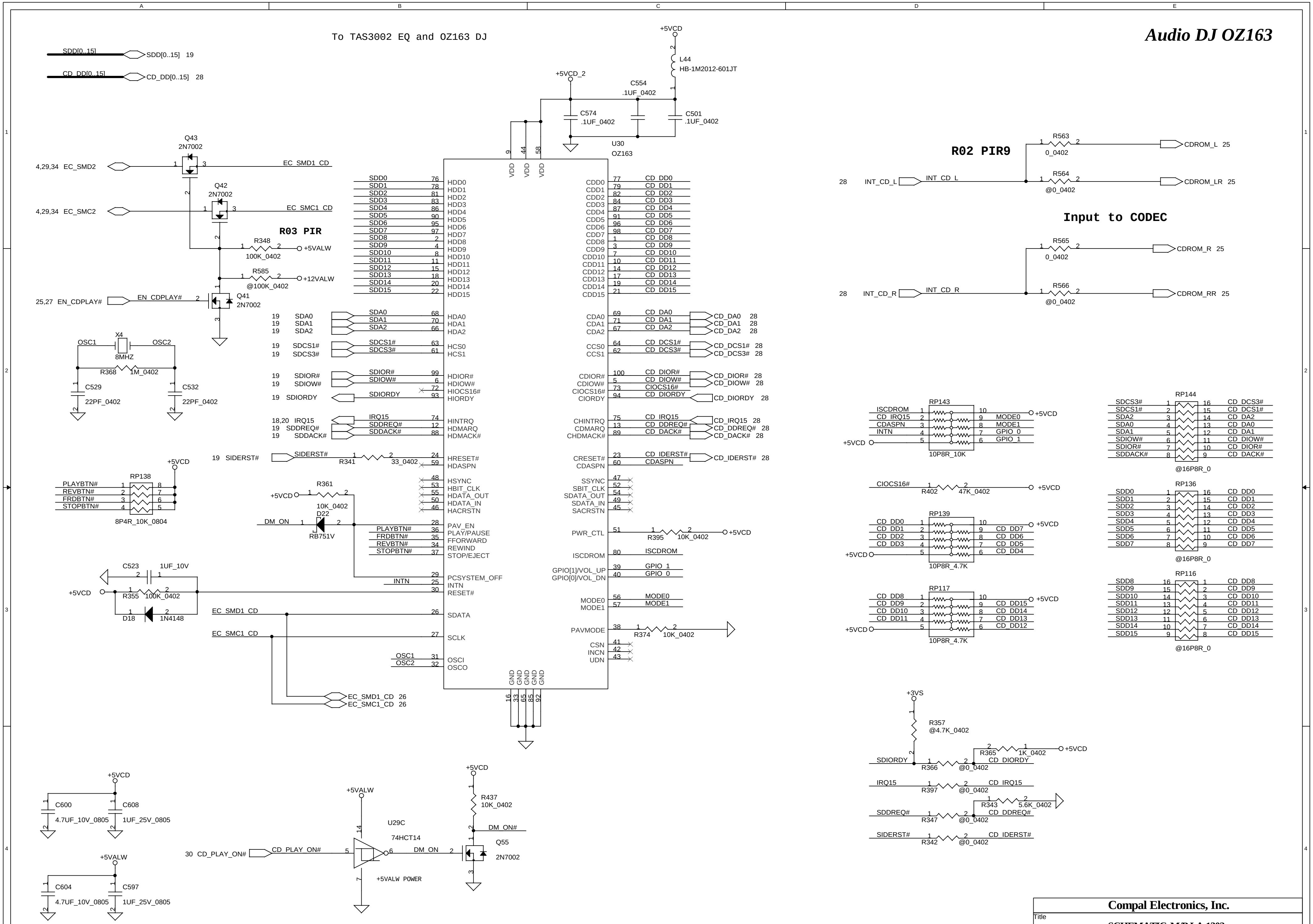

Audio DJ OZ163
To TAS3002 EQ and OZ163 DJ
SDD[0..15] 19
CD_DD[0..15] 28
R03 PIR
R02 PIR9
Input to CODEC
U30
OZ163
L44
HB-1M2012-601JT
+5VCD
+5VCD_2
C554 .1UF_0402
C574 .1UF_0402
C501 .1UF_0402
Q43 2N7002
Q42 2N7002
Q41 2N7002
4,29,34 EC_SMD2
4,29,34 EC_SMC2
25,27 EN_CDPLAY#
EC_SMD1_CD
EC_SMC1_CD
R348 100K_0402 +5VALW
R585 @100K_0402 +12VALW
X4 8MHZ
OSC1
OSC2
R368 1M_0402
C529 22PF_0402
C532 22PF_0402
RP138 8P4R_10K_0804
PLAYBTN#
REVBTN#
FRDBTN#
STOPBTN#
R361 10K_0402
D22 RB751V
DM_ON
C523 1UF_10V
R355 100K_0402
D18 1N4148
R341 33_0402
SIDERST#
HDD0 … HDD15
CDD0 … CDD15
HDA0 HDA1 HDA2
HCS0 HCS1
HDIOR# HDIOW# HIOCS16# HIORDY
HINTRQ HDMARQ HDMACK#
HRESET# HDASPN
HSYNC HBIT_CLK HDATA_OUT HDATA_IN HACRSTN
PAV_EN PLAY/PAUSE FFORWARD REWIND STOP/EJECT
PCSYSTEM_OFF INTN RESET#
SDATA SCLK OSCI OSCO
CDA0 CDA1 CDA2
CCS0 CCS1
CDIOR# CDIOW# CIOCS16# CIORDY
CHINTRQ CDMARQ CHDMACK#
CRESET# CDASPN
SSYNC SBIT_CLK SDATA_OUT SDATA_IN SACRSTN
PWR_CTL ISCDROM GPIO[1]/VOL_UP GPIO[0]/VOL_DN
MODE0 MODE1 PAVMODE CSN INCN UDN
R395 10K_0402
R374 10K_0402
EC_SMD1_CD 26
EC_SMC1_CD 26
R563 0_0402 CDROM_L 25
R564 @0_0402 CDROM_LR 25
R565 0_0402 CDROM_R 25
R566 @0_0402 CDROM_RR 25
28 INT_CD_L
28 INT_CD_R
RP143 10P8R_10K
RP144 @16P8R_0
R402 47K_0402
RP139 10P8R_4.7K
RP136 @16P8R_0
RP117 10P8R_4.7K
RP116 @16P8R_0
+3VS
R357 @4.7K_0402
R365 1K_0402
R366 @0_0402
R397 @0_0402
R343 5.6K_0402
R347 @0_0402
R342 @0_0402
C600 4.7UF_10V_0805
C608 1UF_25V_0805
C604 4.7UF_10V_0805
C597 1UF_25V_0805
+5VALW
U29C 74HCT14
30 CD_PLAY_ON#
+5VALW POWER
R437 10K_0402
DM_ON#
Q55 2N7002

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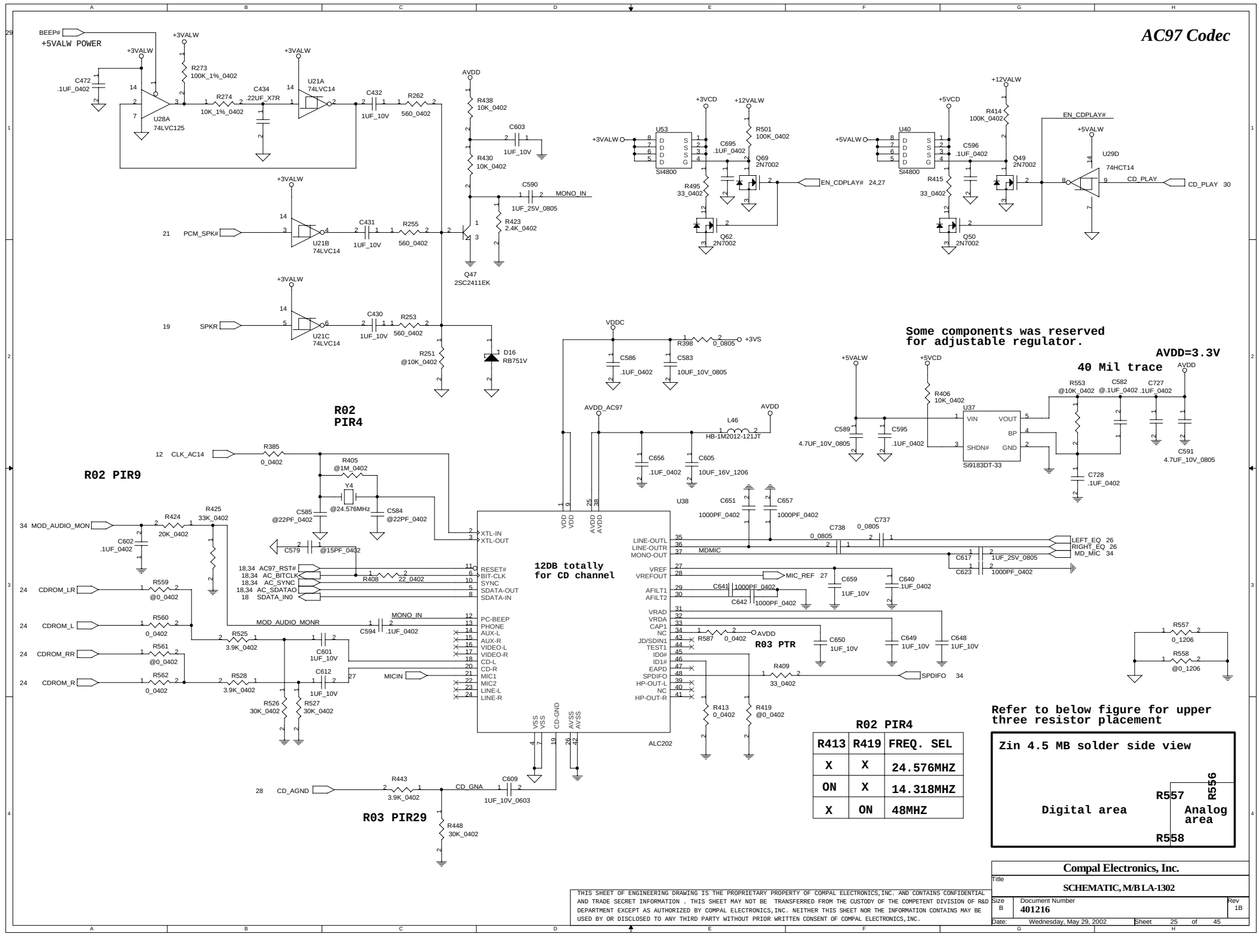
AC97 Codec



R413	R419	FREQ. SEL
X	X	24.576MHZ
ON	X	14.318MHZ
X	ON	48MHZ

R02 PIR4

Refer to below figure for upper three resistor placement

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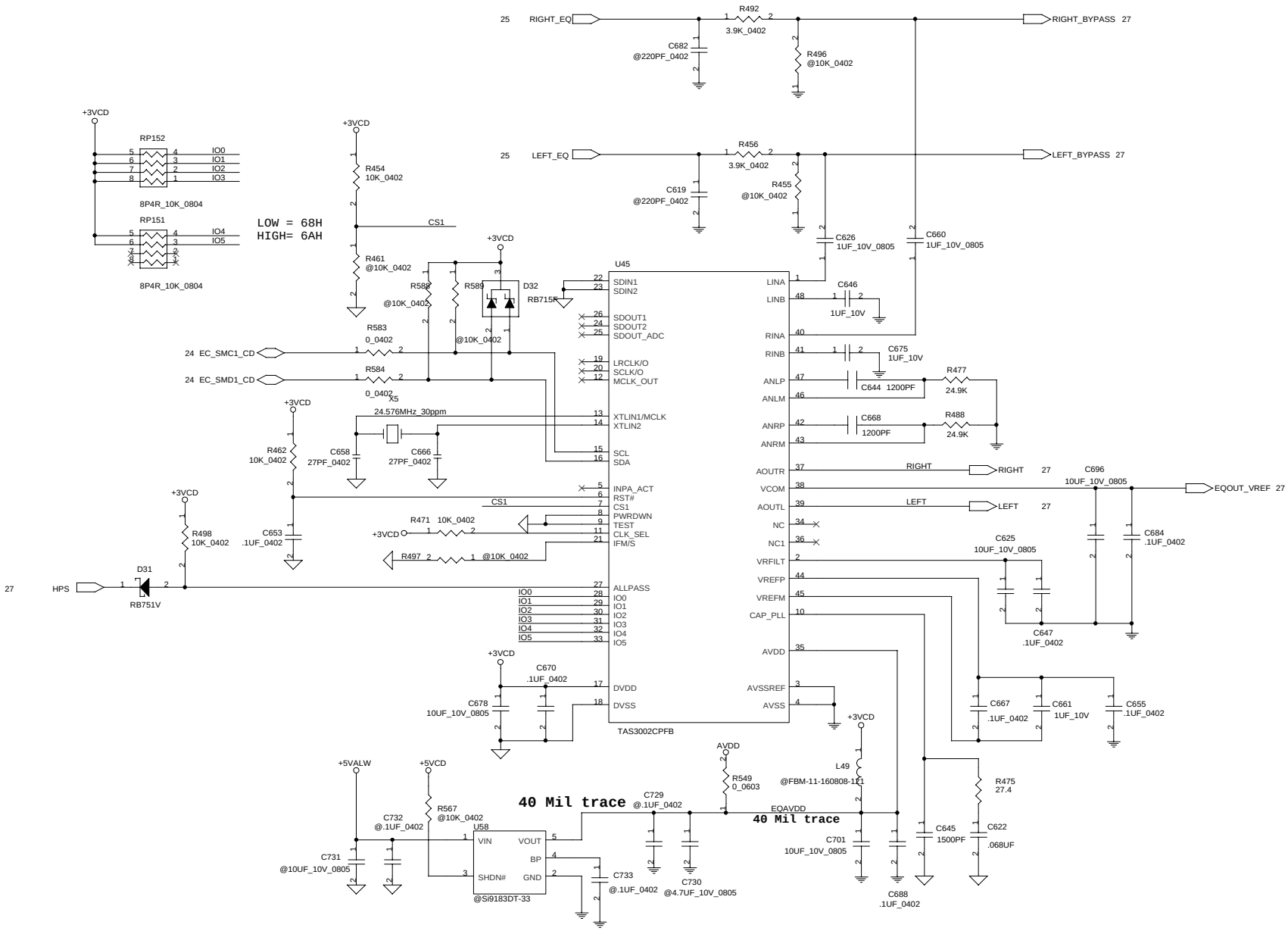

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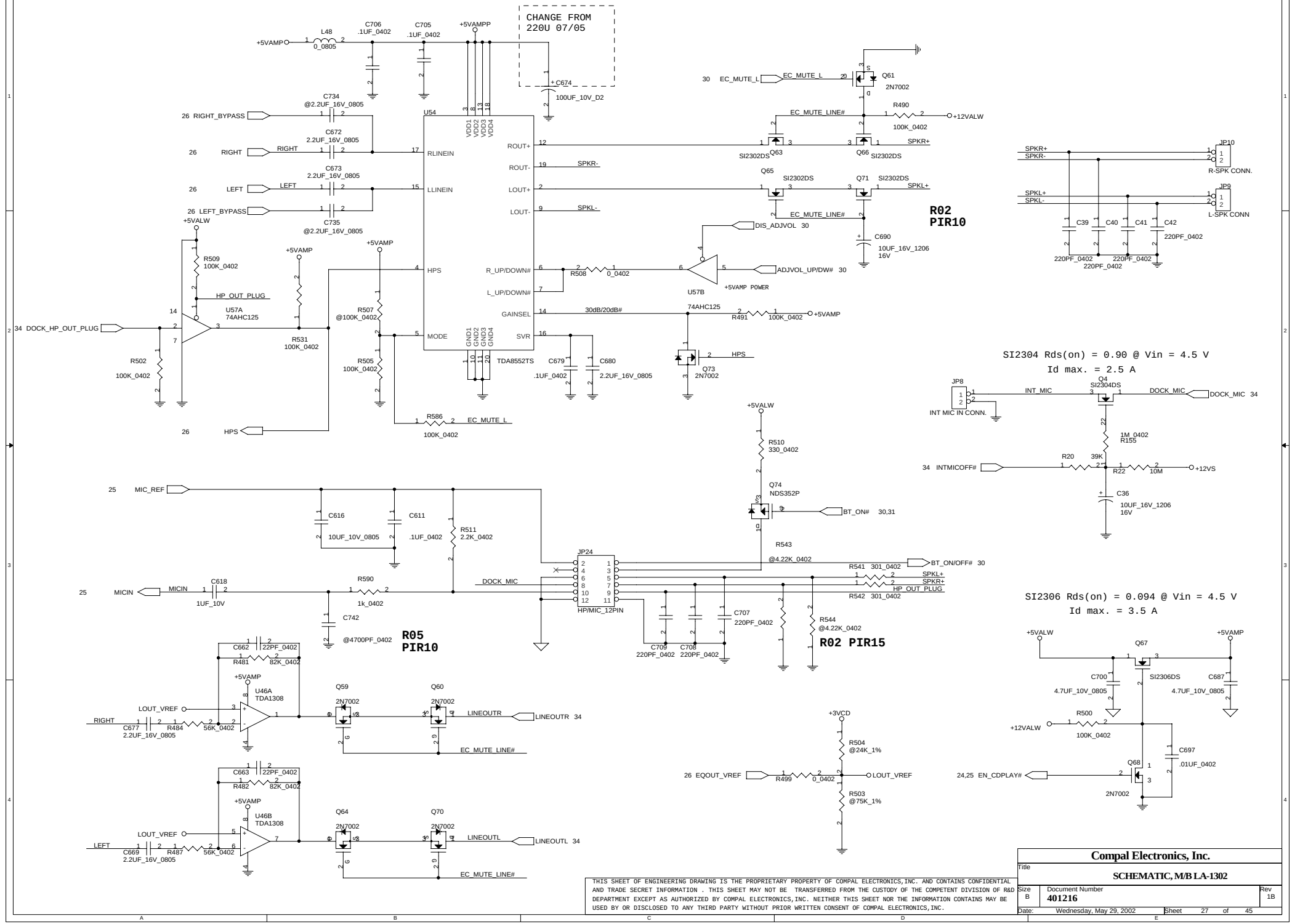
AMP & Audio Jack



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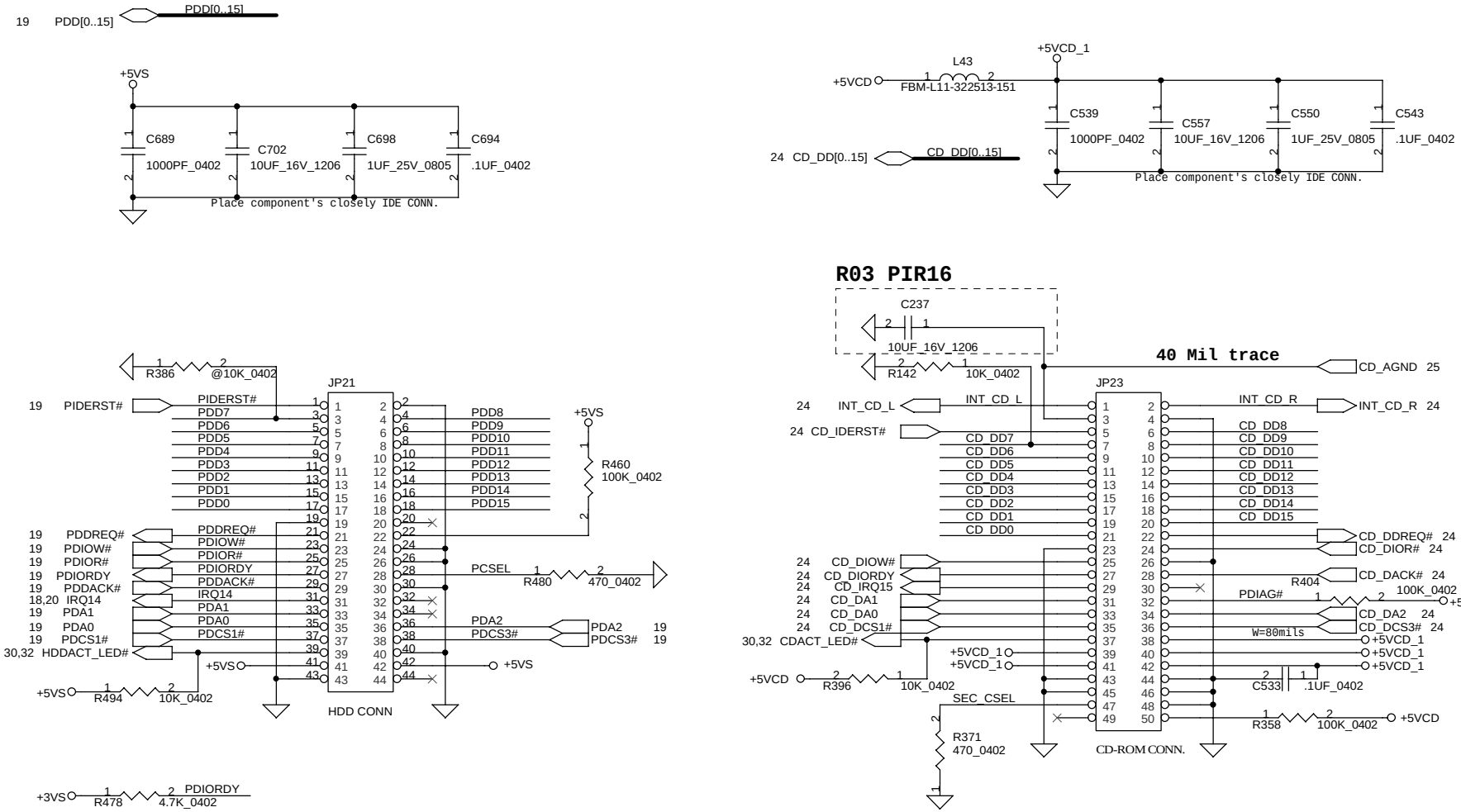
HDD/CD-ROM Module



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PC87591

INT_KBD CONN.

R03 PIR 17

R02 R429,433 MOUNTED, R428 NOT

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)(HCFGBAH, HCFGBAL)+1	
1 1	Reserved	

NS RECOMMEND

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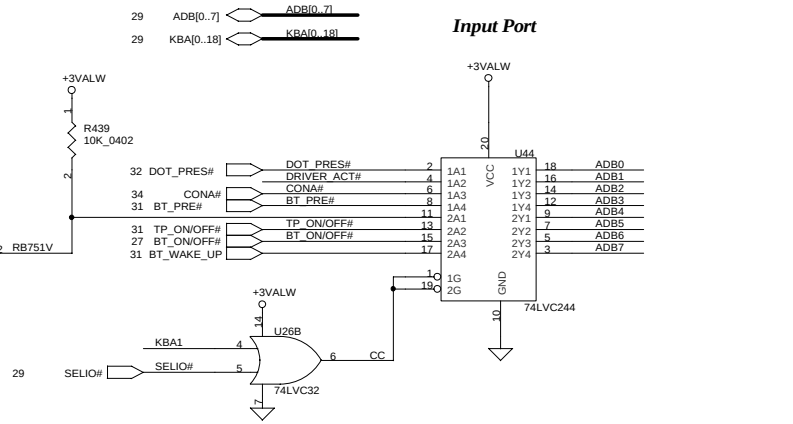
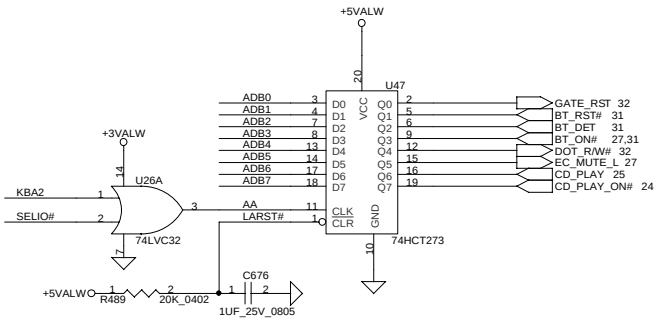
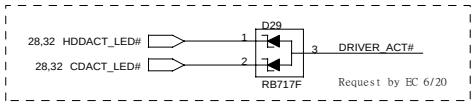
BIOS & I/O Port

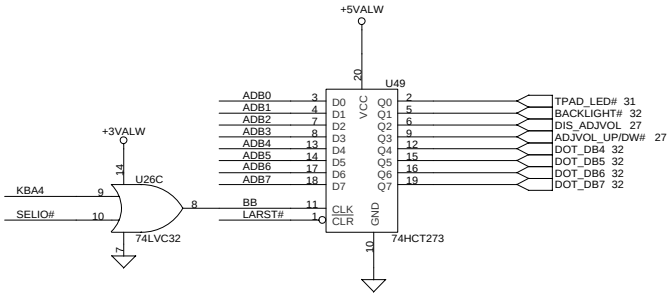
Input Port

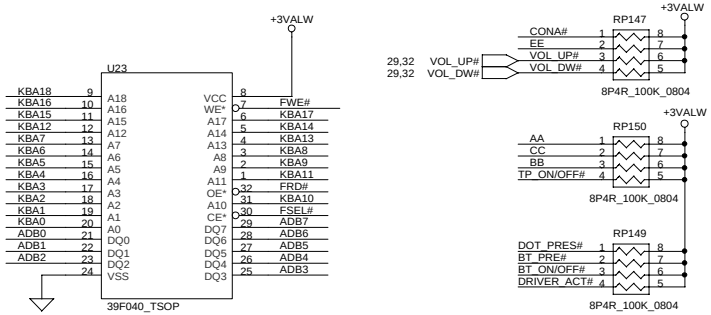


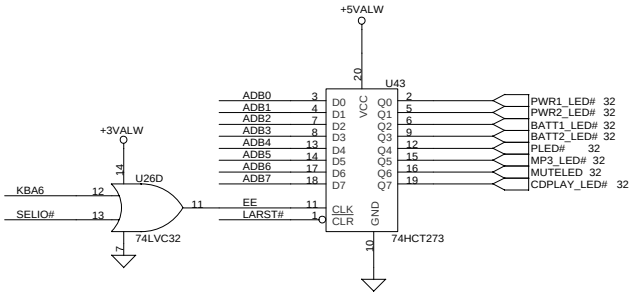
Output Port

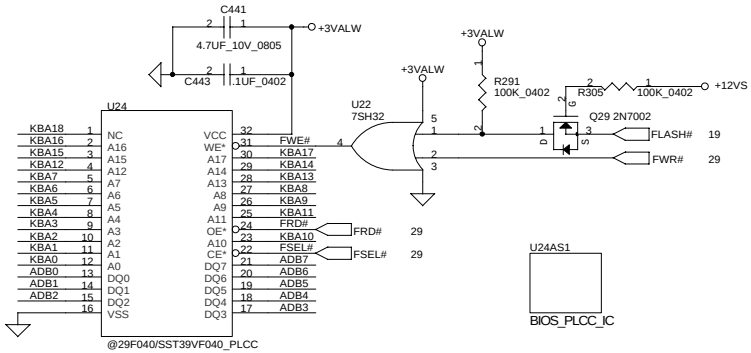


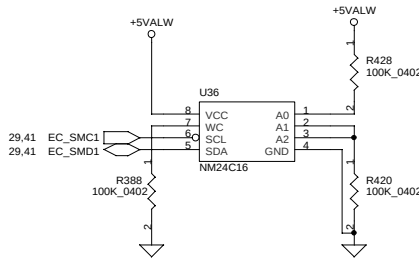












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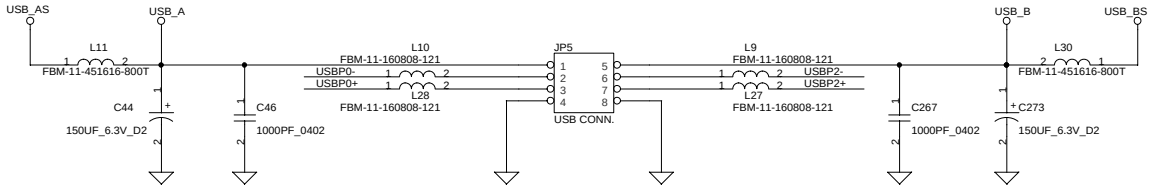
Printer Port/USB

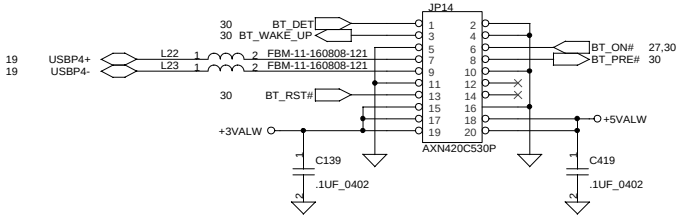
USB A

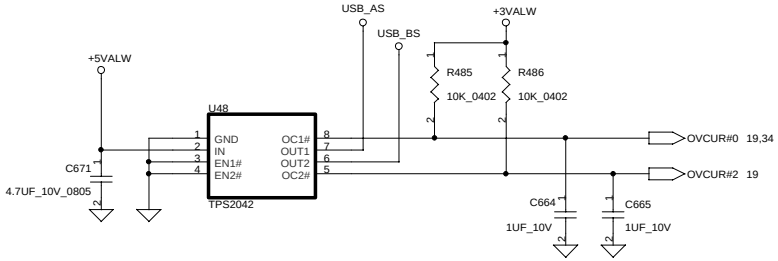
USB Port

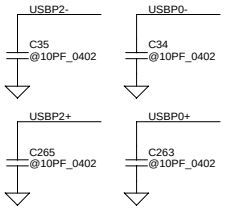
USB B

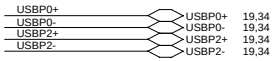


Bluetooth Connector



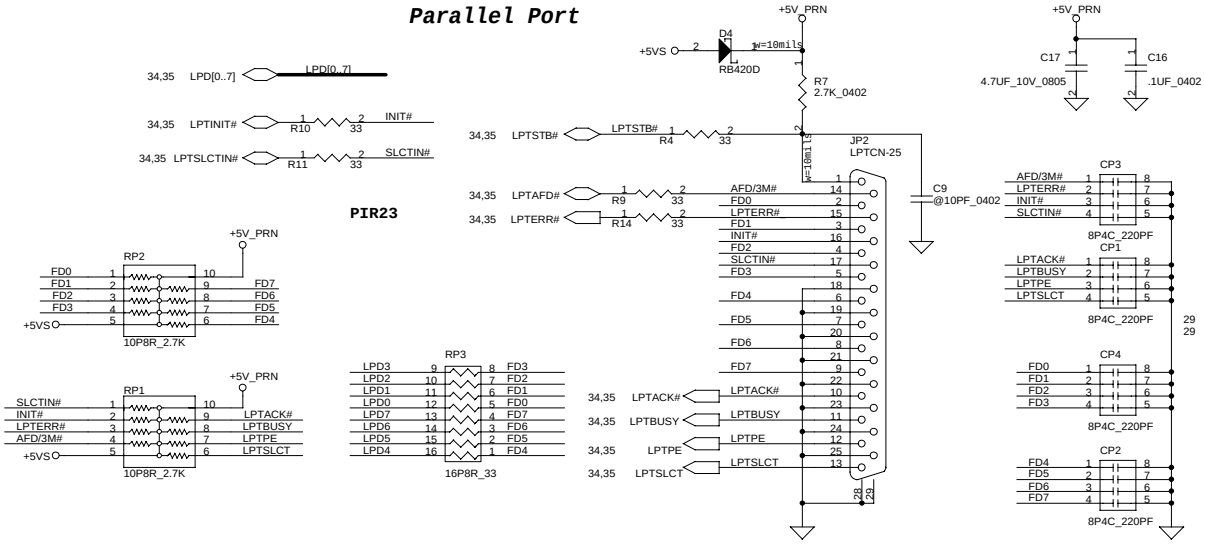


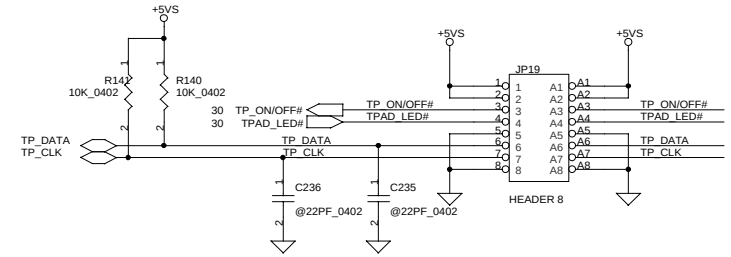




Parallel Port

PIR23





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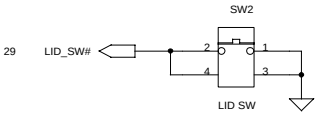
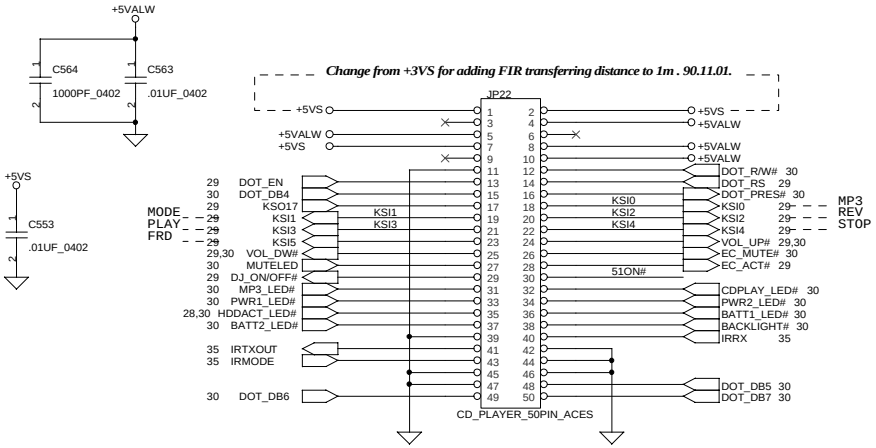
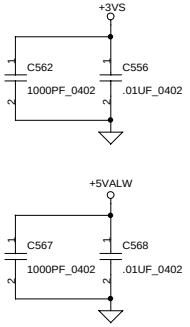
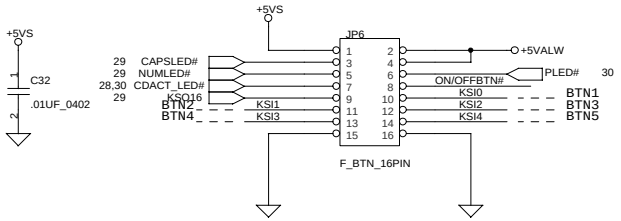
Dot Matrix LCD/FIR

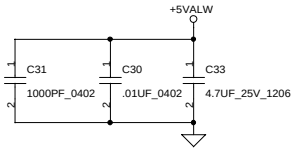
LID Switch



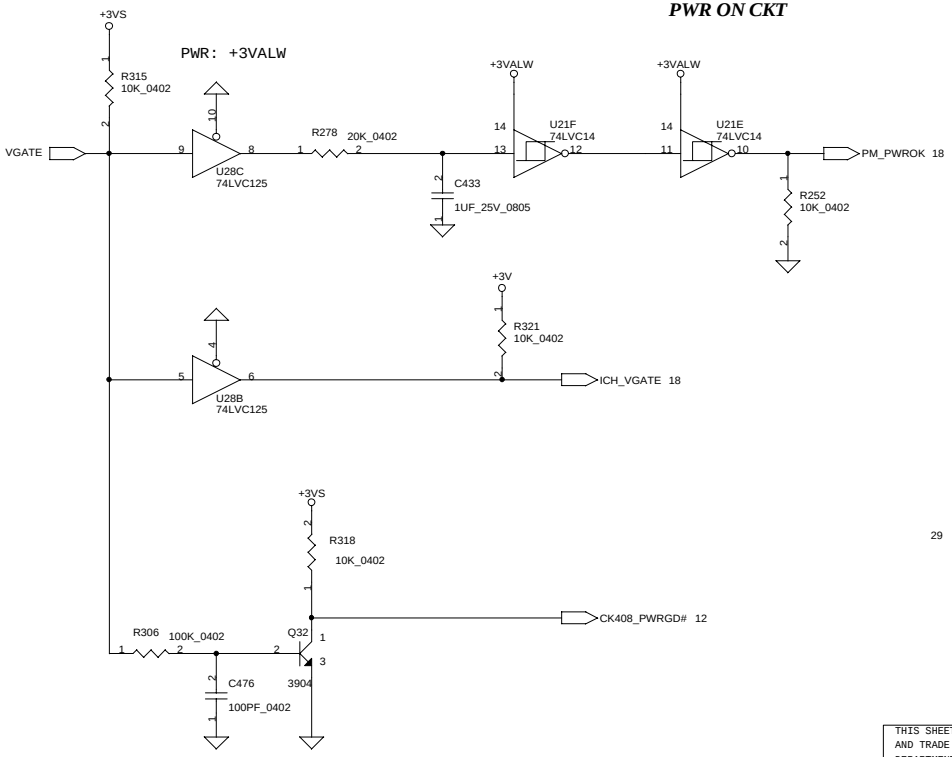


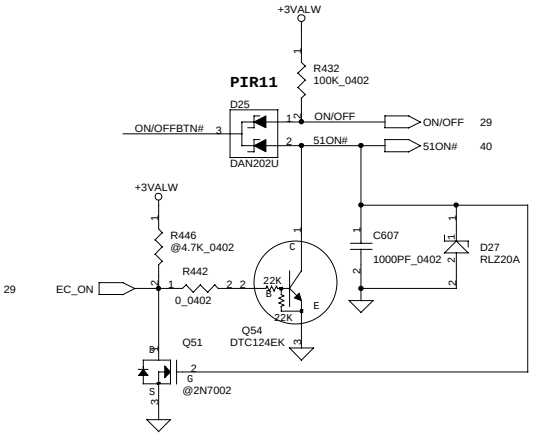




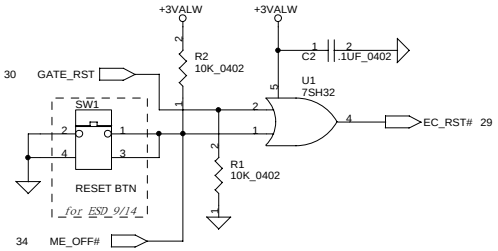


PWR ON CKT





M/E OFF Button



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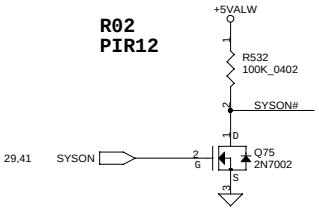
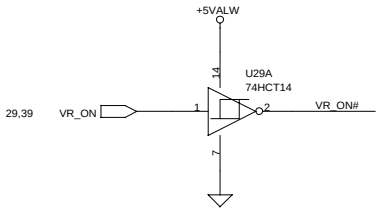
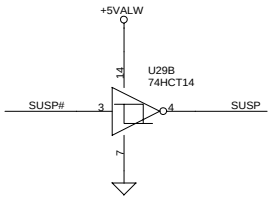
DC/DC Interface & RTC

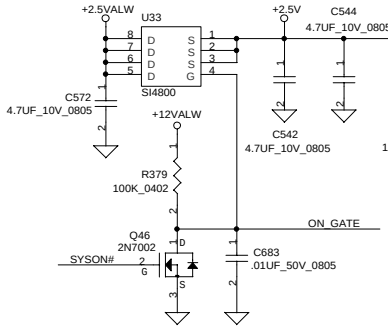
R02
PIR12

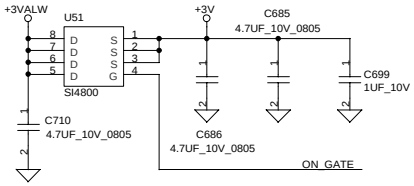


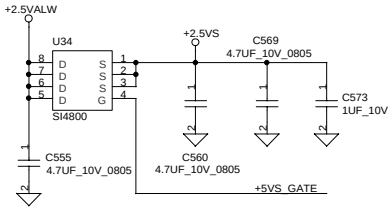


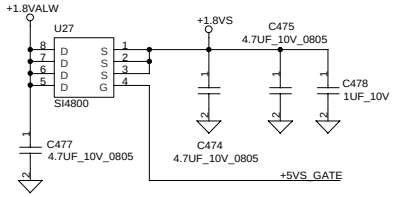


+2.5V tolerence +- 200 mV

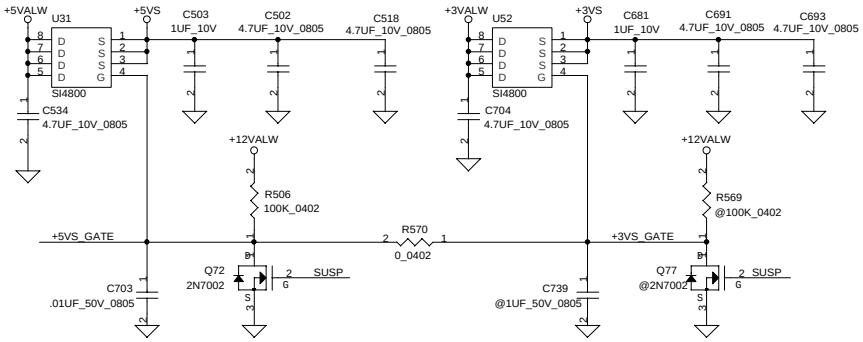




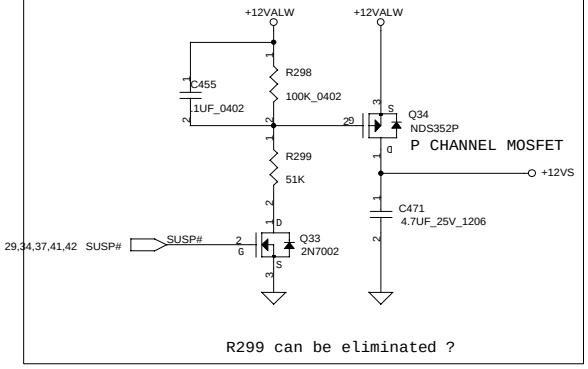




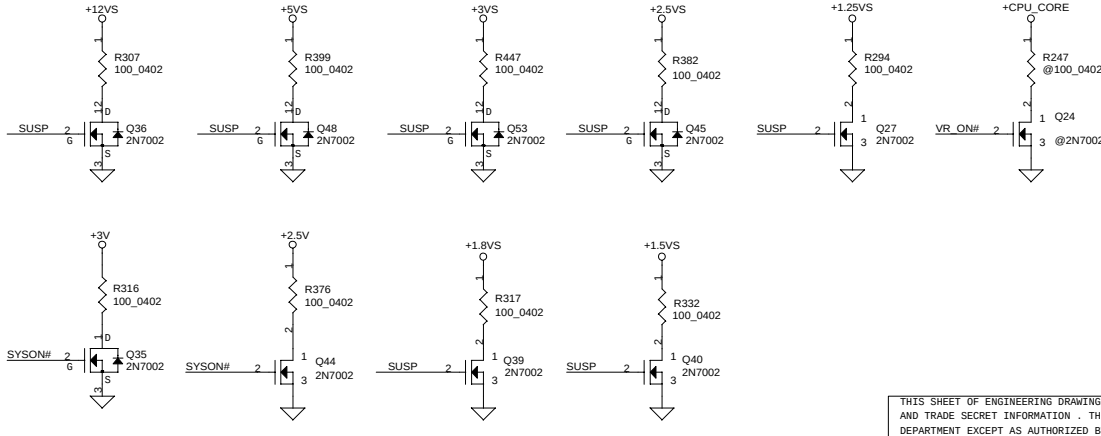
3VS and 5VS are seperated control to achieve maximum power sequence flexibility

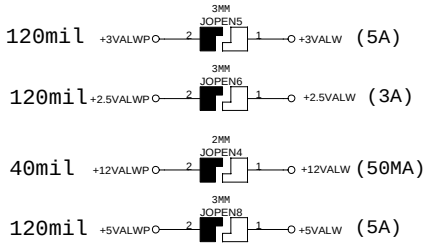


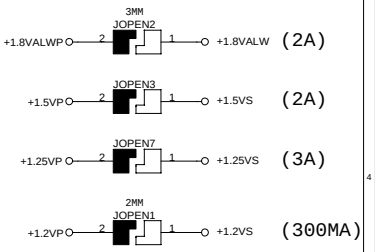
+12VALW To +12VS Transfer



R299 can be eliminated ?







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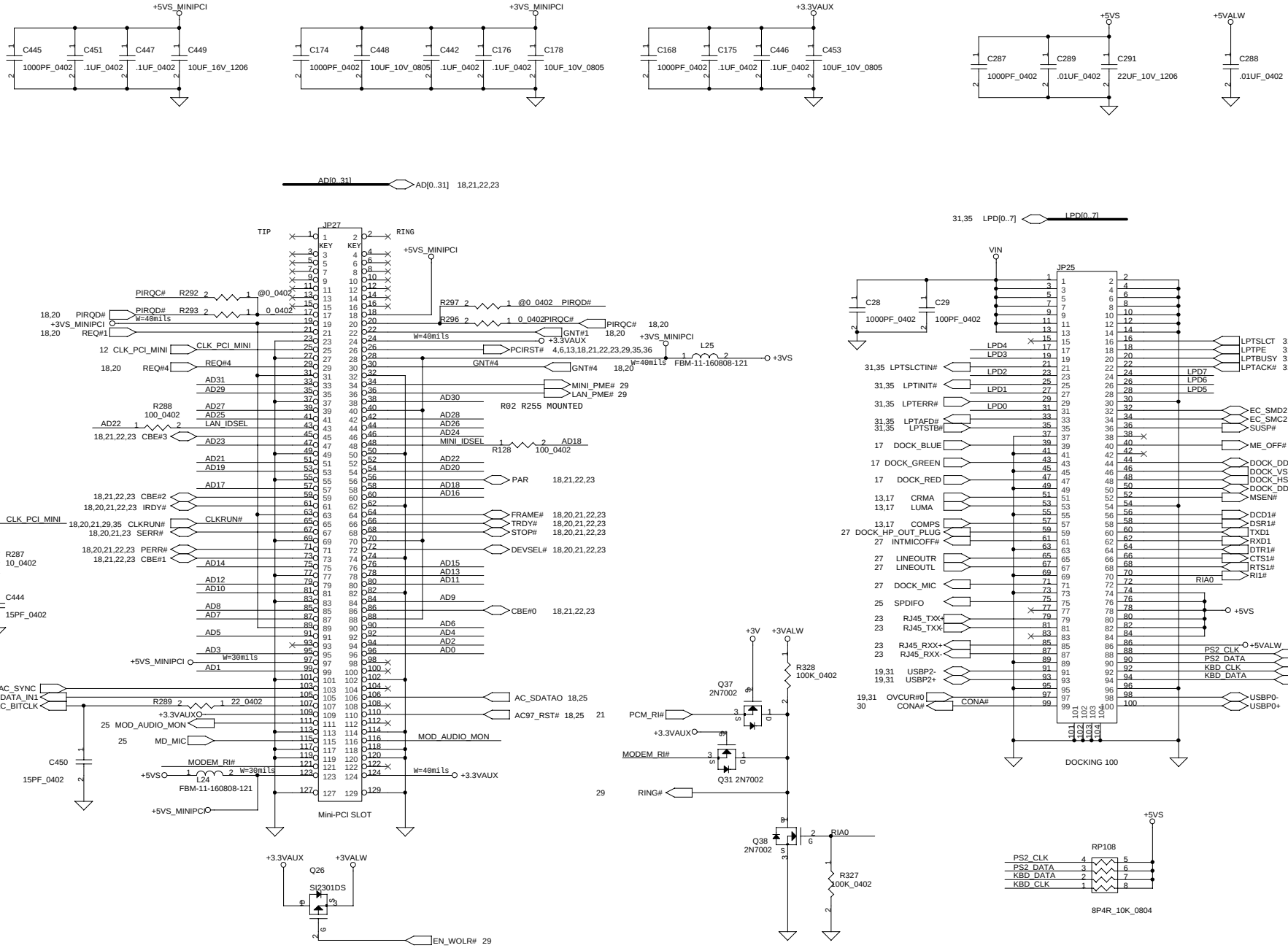
Mini-PCI Slot



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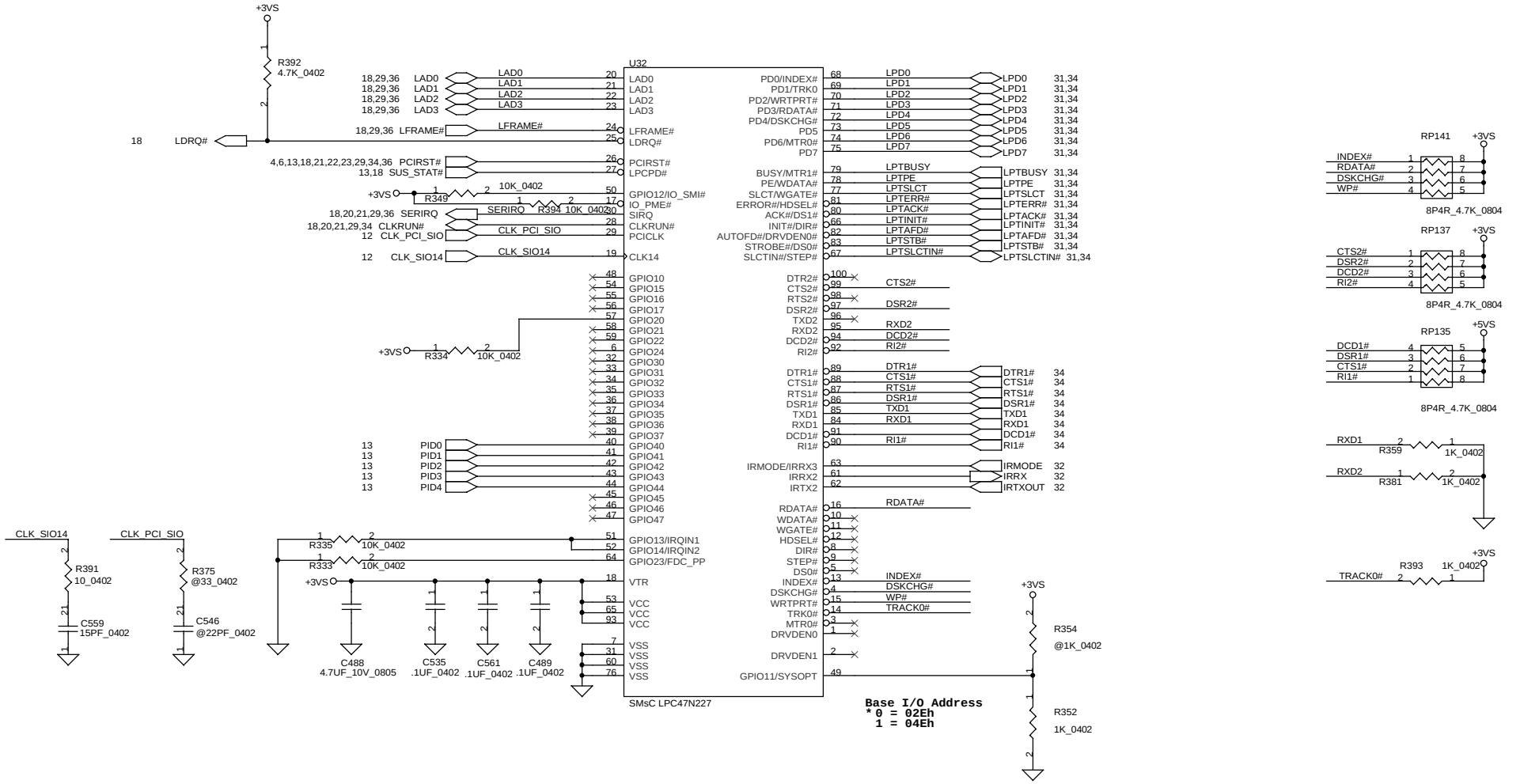
SUPER I/O SMC FDC47N227



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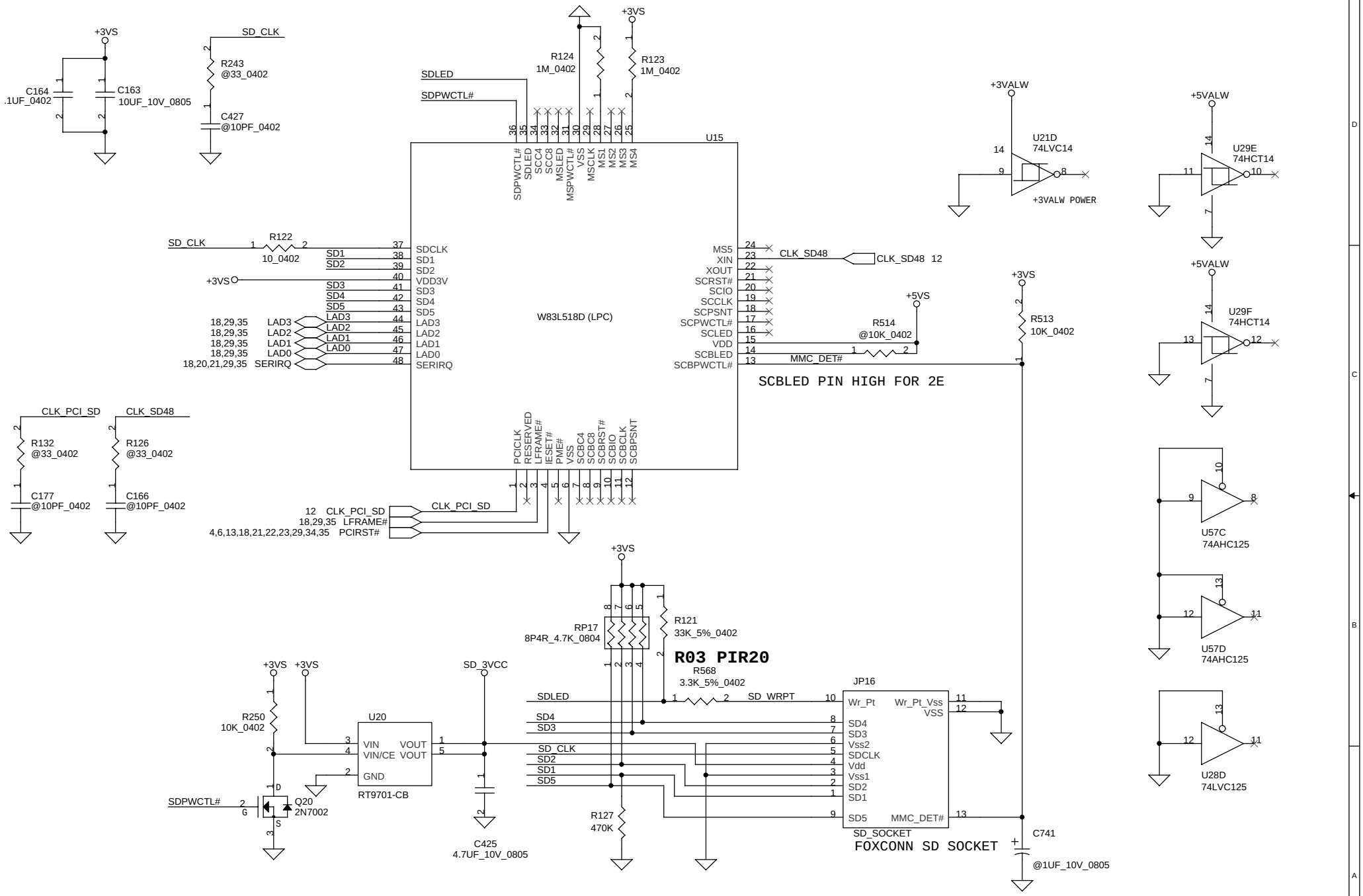

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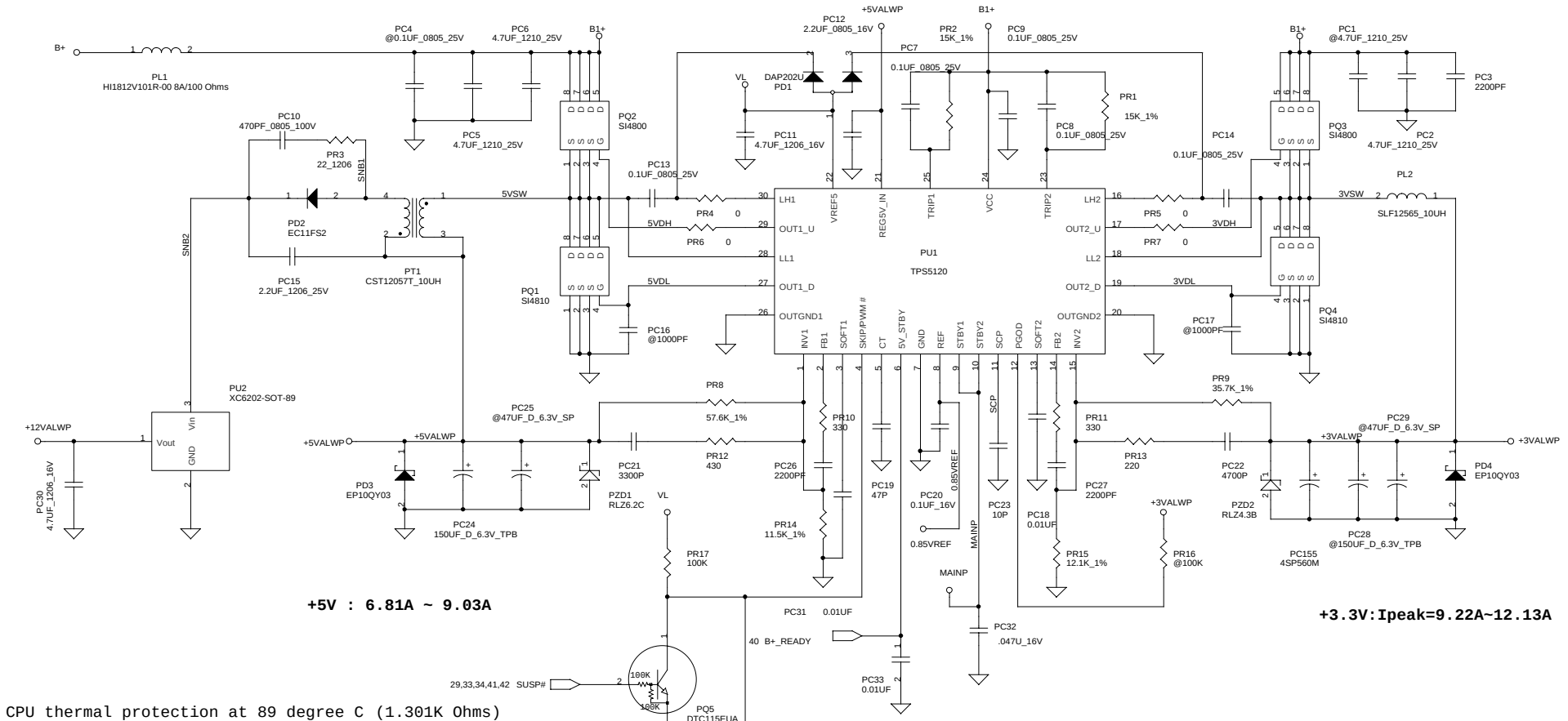
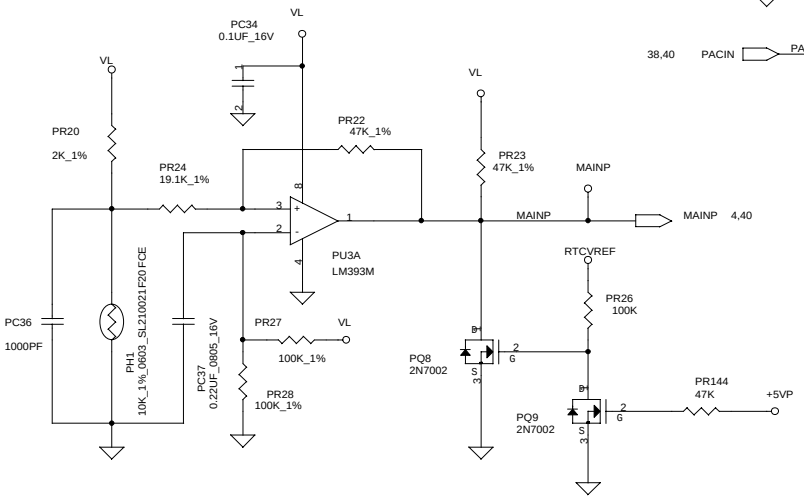
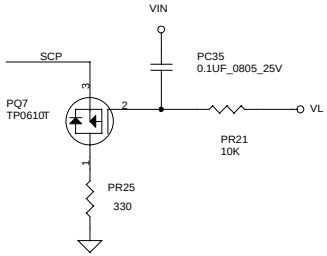
5V/3V/12V



CPU thermal protection at 89 degree C (1.301K Ohms)
Recovery at 44 degree C (5.084K Ohms)





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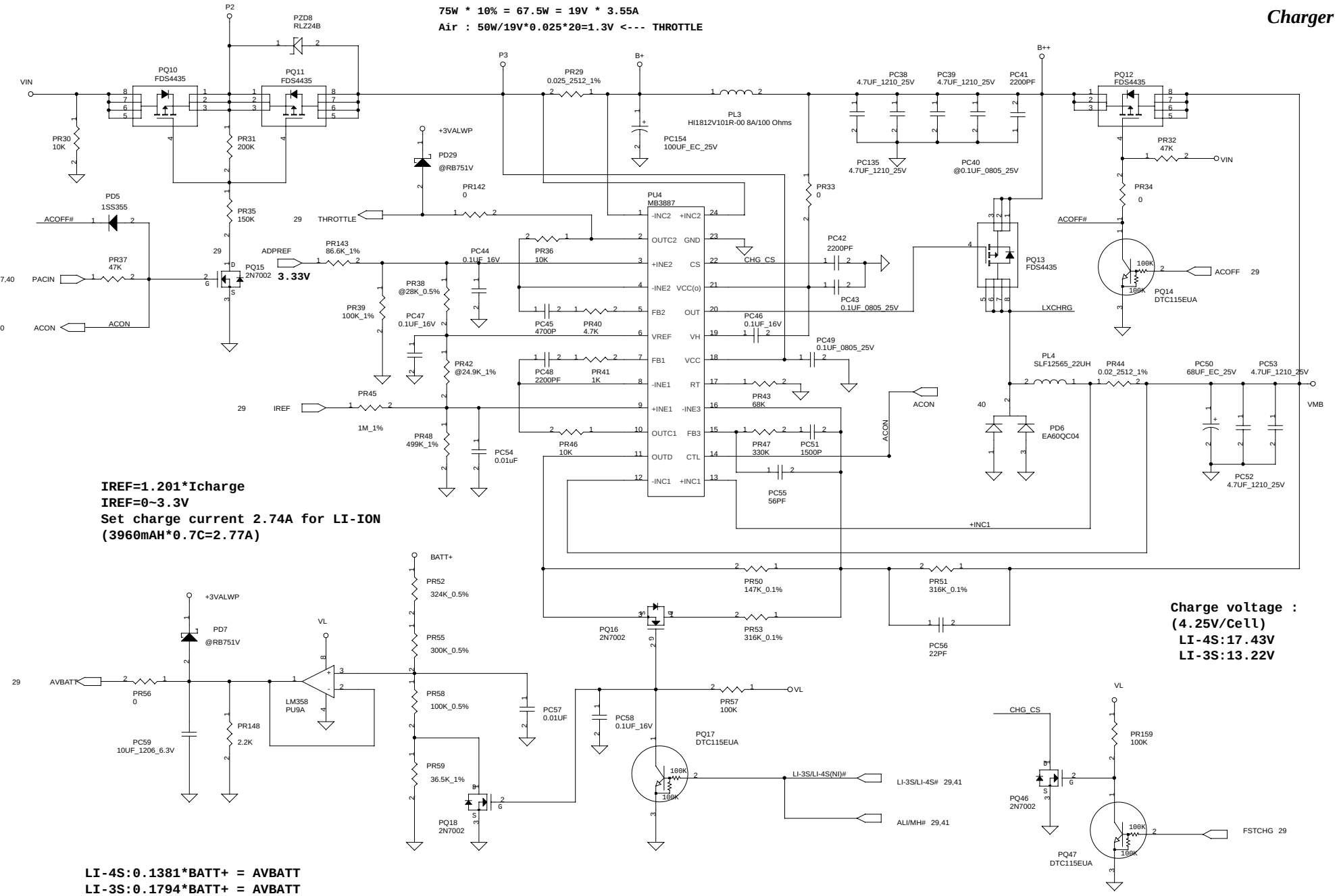
Charger

75W * 10% = 67.5W = 19V * 3.55A
Air : 50W/19V*0.025*20=1.3V <--- THROTTLE



IREF=1.201*Icharge
IREF=0~3.3V
Set charge current 2.74A for LI-ION
(3960mAH*0.7C=2.77A)

Charge voltage :
(4.25V/Cell)
LI-4S:17.43V
LI-3S:13.22V

LI-4S:0.1381*BATT+ = AVBATT
LI-3S:0.1794*BATT+ = AVBATT

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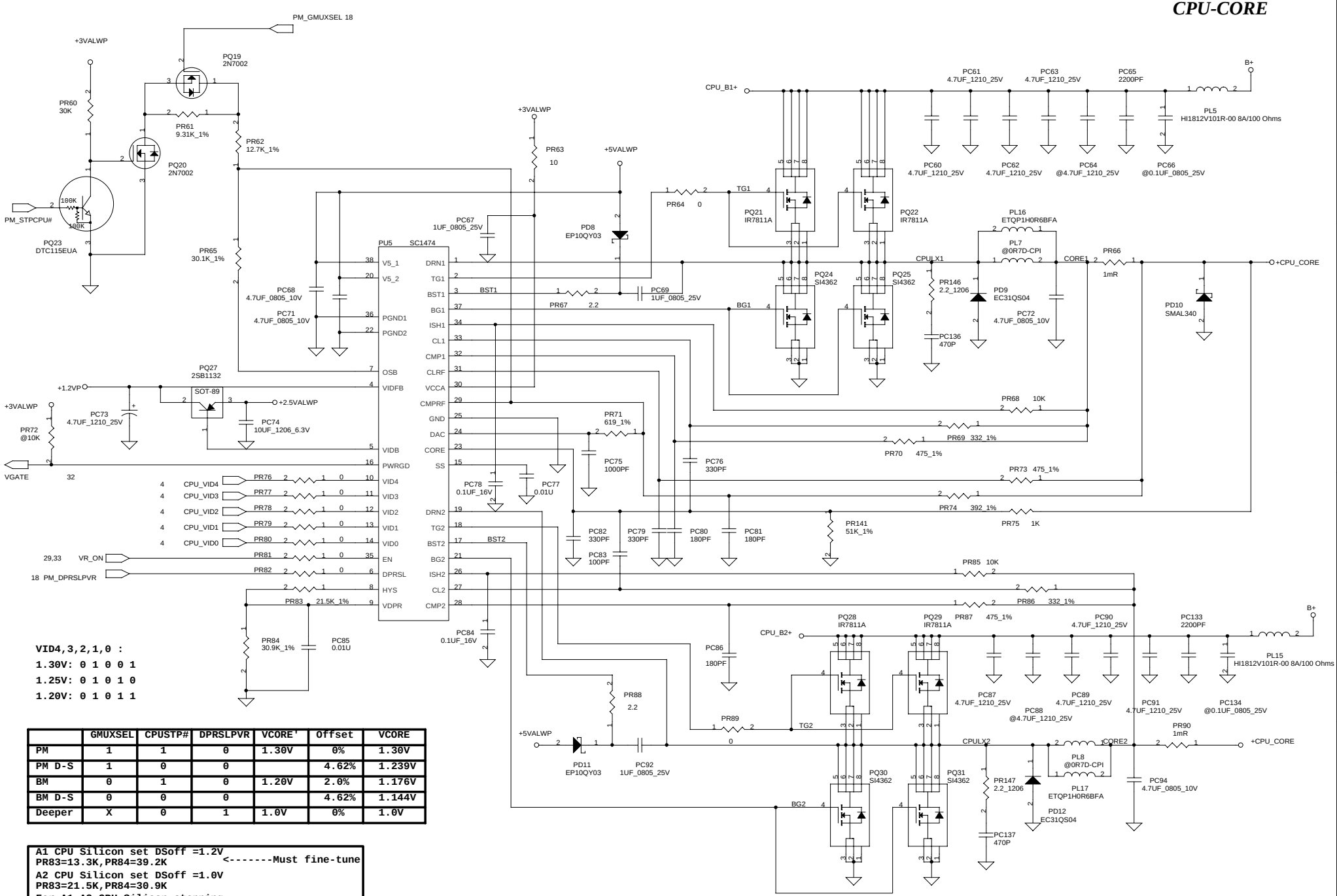
CPU-CORE



VID4,3,2,1,0 :
1.30V: 0 1 0 0 1
1.25V: 0 1 0 1 0
1.20V: 0 1 0 1 1

	GMUXSEL	CPUSTP#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

A1 CPU Silicon set DSoff =1.2V
PR83=13.3K,PR84=39.2K <-------Must fine-tune
A2 CPU Silicon set DSoff =1.0V
PR83=21.5K,PR84=30.9K
For A1,A2 CPU Silicon stepping
PQ19 is nopop, PR61=0, PR62=13K and PR65 is nopop
For B0 CPU Silicon stepping
PQ19 is pop, PR61=9.31K,PR62=12.7K and PR65=30.1K

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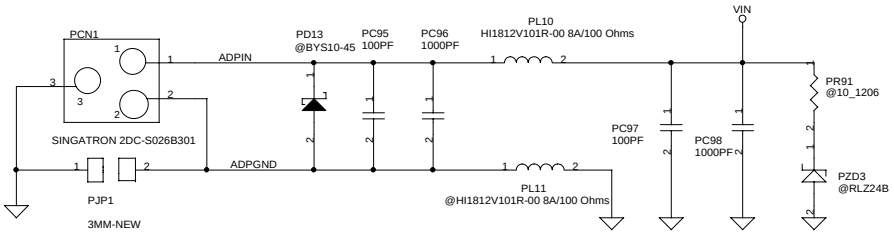
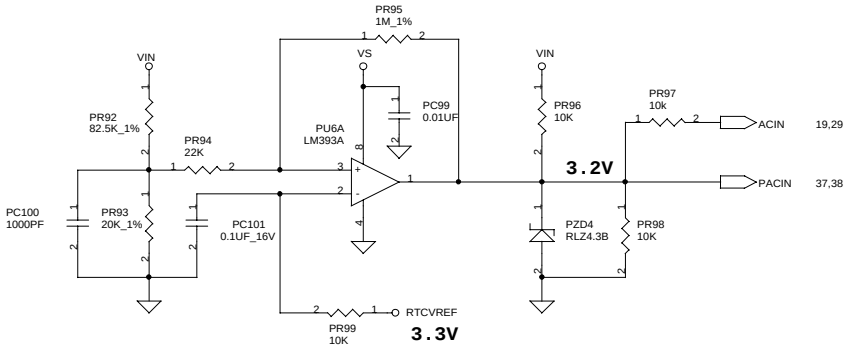
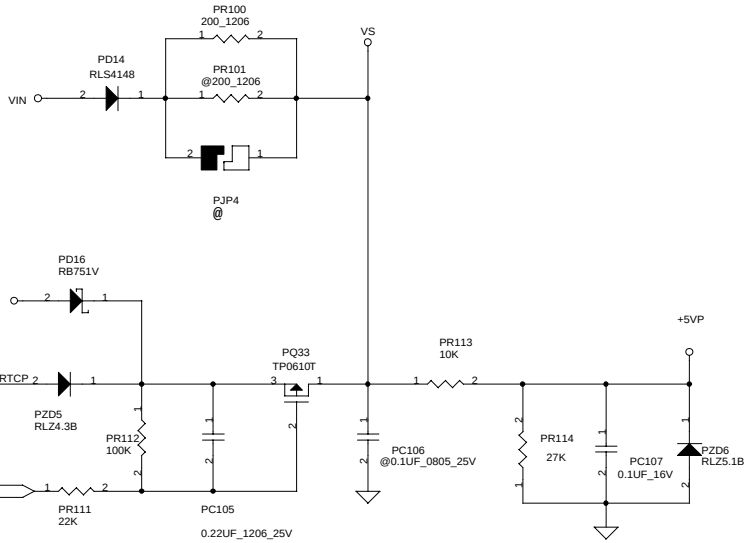
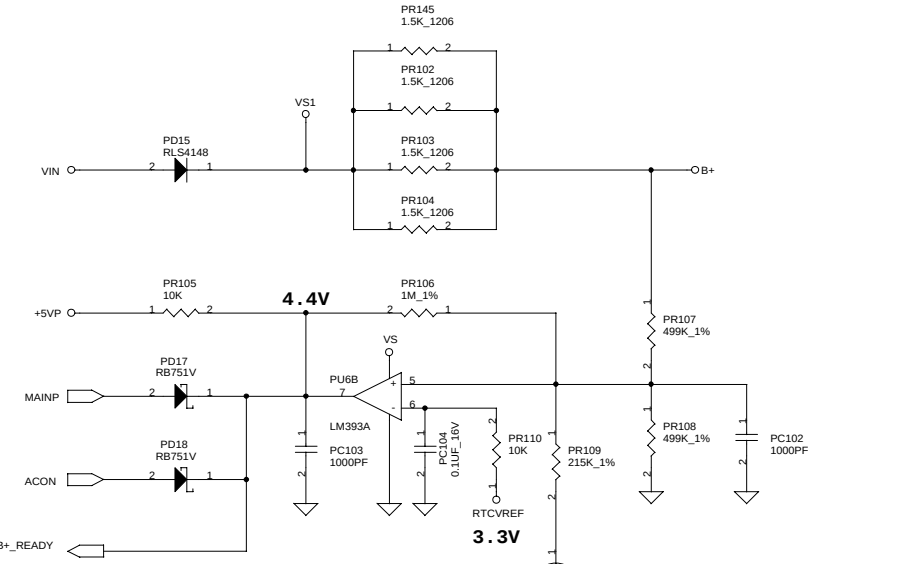
Detector

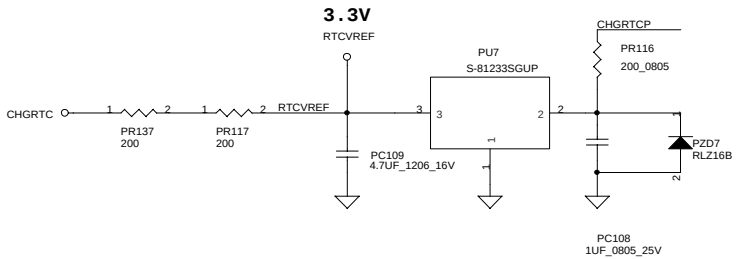
VIN detector		
16.90	17.55	18.22
16.46	17.08	17.72











Precharge detector		
15.34	15.90	16.48
13.13	13.71	14.20

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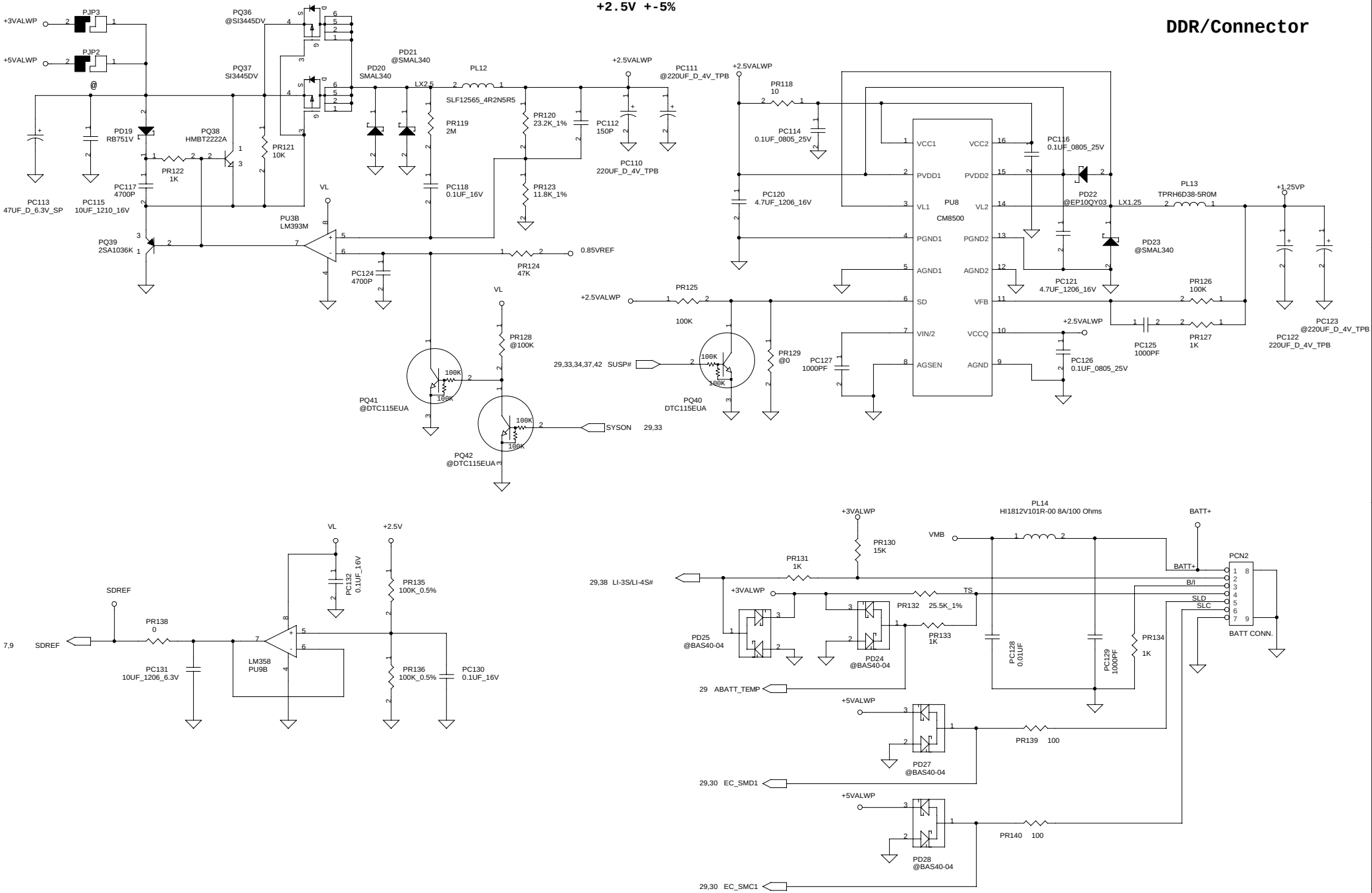
DDR/Connector

+2.5V +-5%



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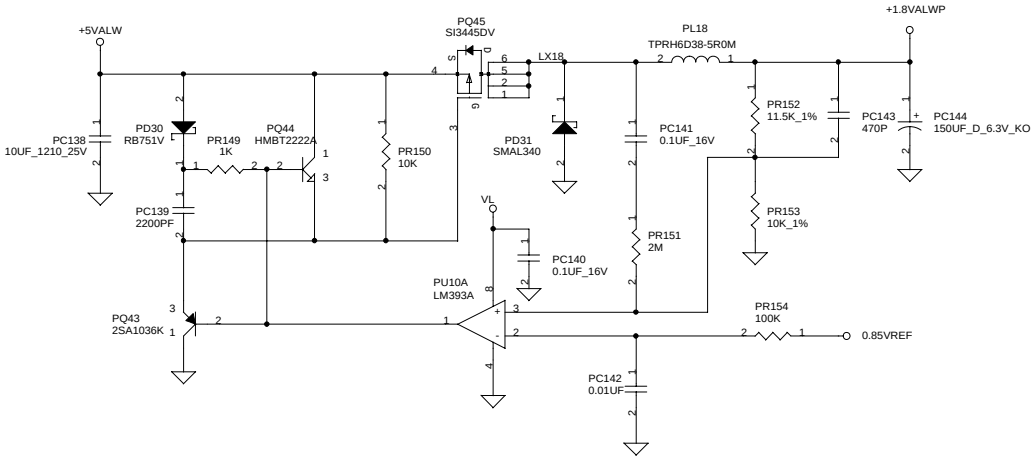
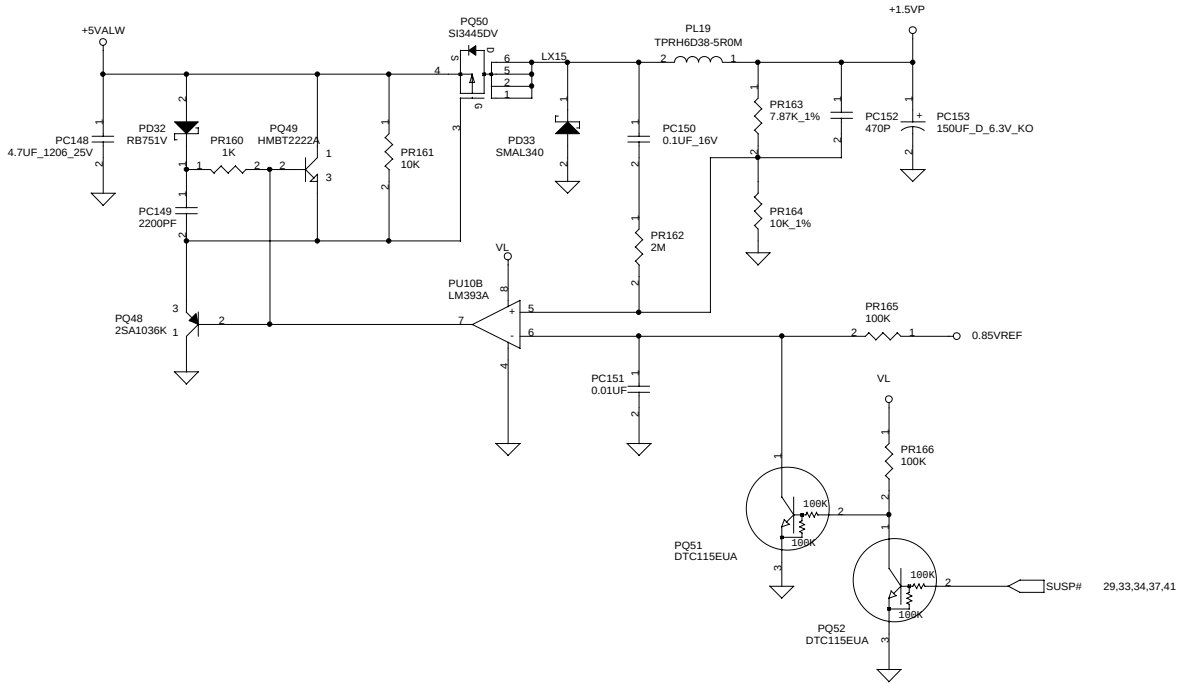
+1.8V+-5%



+1.5V+-5%



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Voltage Rails

Power Plane	Description	S1	S3	S5	FUNCTION	RELATED POWER NET NAME
VIN	Adapter power supply (19V)	N/A	N/A	N/A	Pullhigh,Switch,DOCKING,VL,AC IN.	VIN1
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A	Pullhigh,Switch,B1+,PWR MB3878,PWR MAX1718.	B++,B1+,CPU_B1+,CPU_B2+
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	Pullhigh,Switch,NB,CPU.	
+2.5VALW	2.5V always on power rail	ON	ON	ON*	Pullhigh,Switch,NB,DDR SODIMM.	LANVDD
+2.5V	2.5V power rail	ON	ON	OFF	Pullhigh,Switch,NB,DDR SODIMM.	
+2.5VS	2.5V switched power rail	ON	OFF	OFF	Pullhigh,Switch,NB,CLK Buffer,SB,LANVDD.	+VCCHCK,+VCCMCK,+VCCMDLL,+2.5VRGBPLL,+2.5VRGBDAC,+2.5VSBRAM ,+SB_PLLVDD
+3VALW	3.3V always on power rail	ON	ON	ON*	Pullhigh,Switch,PCMCIA Switch,LAN,CMOS,KBD CTRL, SMBus,BIOS,BlueTooth, USB	+3VCD(+3VCD_A), LANIO, +3.3VAUX
+3V	3.3V power rail	ON	ON	OFF	Pullhigh,Switch,SB,PCMCIA CTRL,CMOS,PANEL.	LCDVDD,+3V_CB
+3VS	3.3V switched power rail	ON	OFF	OFF	Pullhigh,DJ,Switch,LOGIC,KBD,SIO,LAN,1394,	VDDC,+3VS_MINIPCI,LCDVDD(LCDVDD_1),TV_DVDD,LVDS_PLLVCC(LVDS_VCC)
+5VALW	5V always on power rail	ON	ON	ON*	Pullhigh,Docking,DJ,Switch,BT,LOGIC,AVDD(Audio),Thermal,FAN.	+5VCD(+5VCD_1,+5VCD_2),AVDD(AVDD_AC97),S1_VCC,+5VAMP,INV_B+
+5V	5V power rail	ON	ON	OFF	Pullhigh,Switch.	
+5VS	5V switched power rail	ON	OFF	OFF	Pullhigh,Docking,MiniPCI,+5VALW, USB,T/P,LPT,DJ,HDD,TV,CRT,Inverter,Switch,VID.	+5VFAN1,+5VFAN2,CRTVDD,+5V_PRN,+5VS_MINIPCI,USB_AS(USB_A), USB_BS(USB_B),TV_VDD,TV_AVDD
+12VALW	12V always on power rail	ON	ON	ON*	PC CARD,Pullhigh,Switch,MOS	
+12VS	12V switched power rail	ON	OFF	OFF	Switch,Power MOS.	
+RTCVCC	RTC power	ON	ON	ON	RTC Power.	
+1.25VS	1.25V switched power rail	ON	OFF	OFF	Pullhigh,DDR termination.	1.25VP
+1.2VS	1.2V switched power rail	ON	OFF	OFF	CPU	1.2VP,+H_VCCA,+HVCCIOPLL

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
LAN	AD17	3	PIRQB
CardBus	AD20	2	PIRQA
Mini-PCI	AD18	4	PIRQD
Mini-PCI LAN	AD22	1	PIRQC
IEEE-1394 Controller	AD16	0	PIRQA
AGP VGA			PIRQA

VGA LCD PANEL ID LIST

EC SM Bus1 address

Device	
Smart Battery	**0001 011X b**
EEPROM	**1010 000X b**

EC SM Bus2 address

Device	
AD1032	**1001 100X b**
OZ163	**0011 0100 b**
Docking	**0011 011X b**
EQ TAS3002	**0110 011X b**

ICH3-M SM Bus address

Device	
SODIMM	**1010 000X b**
Clock Gen	**1101 001x b**

P.S:Default Resistor & Capacitor's package are 0603.
Default 8P4R package is 0402.

Compal Electronics, Inc.
Title: **SCHEMATIC, M/B LA-1302**
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PIR listing :

PAGE 4	PIR1	CHANGE THERMAL SENSOR FROM MAX6654 TO ADM1032	DEL U11, R78, R86; ADD U56, R519
PAGE 5	PIR2	COST DOWN CPU CAPS	DEL C110, C377 ADD DIP 560UF_4V_14m C715, C716; C72, C97, C126 NOT ON
PAGE 6	PIR3	REMOVE AGP_BUS PULLUPS	RP111, RP11, RP12, RP15 NOT ON
PAGE 12			CHANGE R284, R285 FROM 33 OHM TO 10 OHM
PAGE 24 PAGE 25	PIR4	AUDIO CODEC CHANGED FROM ALC201 TO ALC202	ADD R286 10_0402; U41, C592, C615, C593, R459, R458, C621, R433, R417, C598, R449, R444 NOT ON; CHANGE R450, R444 TO 0_0402, ADD R522, R523 0_0402
PAGE 13	PIR5	EMI REQUEST TO PULL HIGH ON MK1709	ADD R385 0_0402, RESERVE R405, C585, C584, Y4; ADD 20K_0402 R525, R528 33K_0402 R526, R527; ADD R413 0_0402, R524 10K_0402, Q75 PDTA114EK
PAGE 15	PIR7	DECREASE THE NOISE ON VDDRH	ADD A .1UF_0402 CAP C719
PAGE 23	PIR8	REMOVE LAN CHASIS GROUND PER EMI'S REQUEST	DEL C243
PAGE 27	PIR10	MOVE SPKR CAPS TO AUDIO BOARD FOR COST DOWN	C692, C711 NOT ON, ADD 0_0805 R531, R532
PAGE 26	PIR11	FOR AUDIO NOISE, ISOLATE LEFT_EQ , GET_EQ , CHANGE C237'S GND TO AGND	RESERVE R529, R530
PAGE 33	PIR12	+3V, +2.5V RISES AS AC_IN, USE 2N7002 AS INVERTER INSTEAD OF 7414	ADD Q75, R532
PAGE 27	PIR13	COST DOWN, USE 74AHC125 TO REPLACED 7SH32	ADD U57, DEL U56, U50
PAGE 25	PIR14	RESERVE A JUMPER FOR AGND TO DGND	
PAGE 27	PIR15	DECREASE EARPHONE'S VOLUME	ADD R541, 542, 543, 544
PAGE 28	PIR16	Add bead for CD ROM analog grounding option	Del C237 , add L50 , change bead connection from Analog to Digital ground
PAGE 29	PIR17	Add capacitor to filter out noise on AVBATT_TEMP to prevent shut_down bug	Add C736 1uF capacitor
PAGE 5	PIR18	EMI team agree to delete all EMI clip Still reserve four clip for backup	Del EMI clip PAD2,4,6,8
PAGE 36	PIR19	Add JAE SD/MMC socket as 2nd source	Add JP29
PAGE 36	PIR20	1.Chang R121 from 499 1% 0402 Resistor to 33K 5% 0402 resistor 2.Add R568 to prevent SDLED signal directly short with Ground while write protect tag enabled.	Change R121 Add R568 3.3K , 5% , 0402
PAGE 13	PIR21	Some additional RC on SPECTRUM IC was requested by EMI to reduce interference .	Add R547 -> 10 Ohm , R546 -> 10 Ohm , R555 -> 10 Ohm , C720 -> 22p , C721 -> 22p

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	B.Ver#
1	For thermal teem request that thermal setting point changed from 96 to 90 degree C.	37	PR20 changed from 1.74k into 2k_1%_0603(SD014200101) PR24 changed from 21k into 19.1k_1%_0603(SD014191209)	B test BOM
2	+2.5VALWP is always power plane	41	PQ41,PQ42,PR128 should not be POP	B test BOM
3	For cost down issue	37	PC28,PC29 should not be POP PC155 should be POP (CB5600NM000)	B test BOM
4	Prevent PU4 leakage lock pre-charge circuit	38	PU4 pin14 changed from PACIN into ACON	B gerber
5				
6				

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