

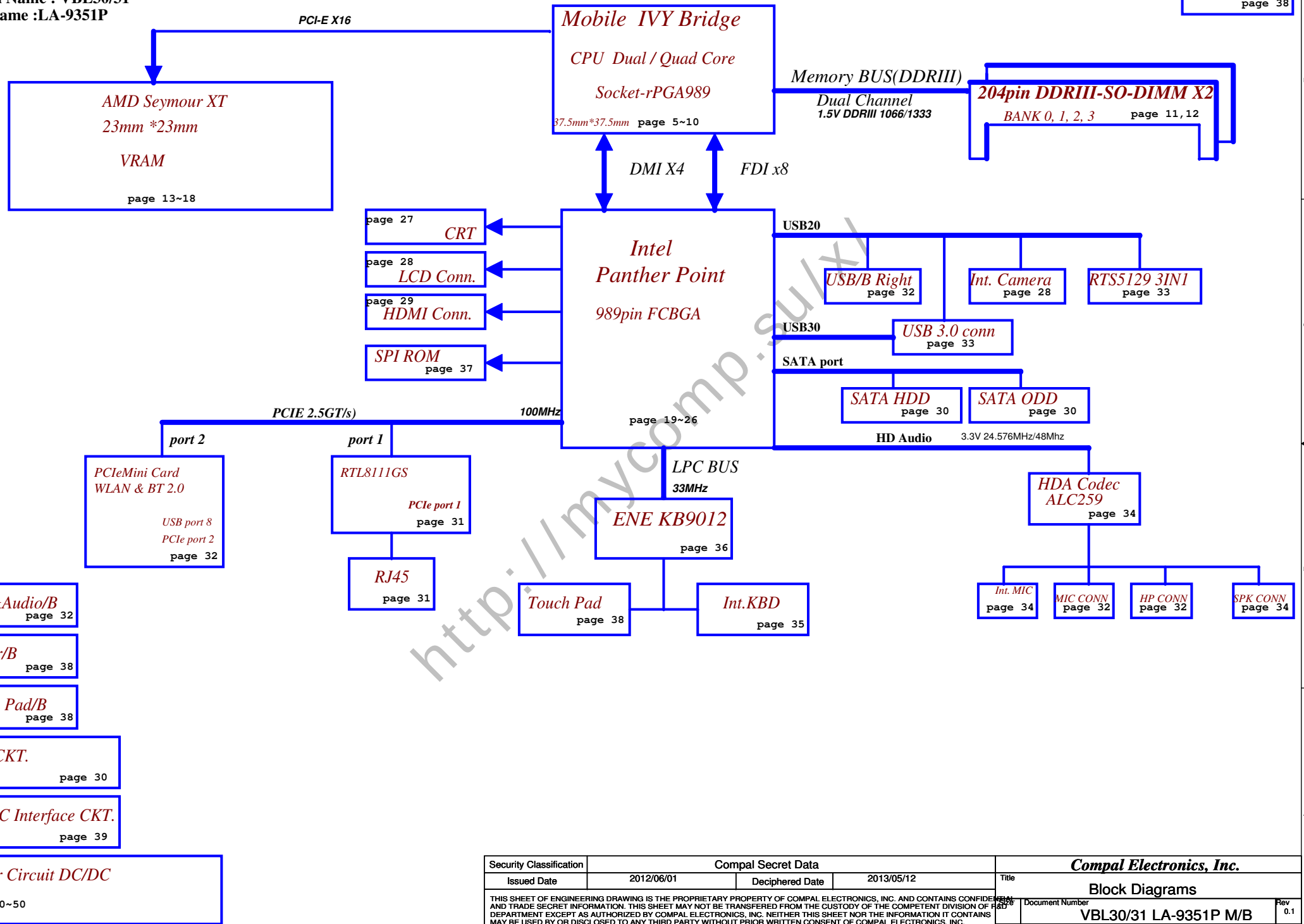
Compal Confidential

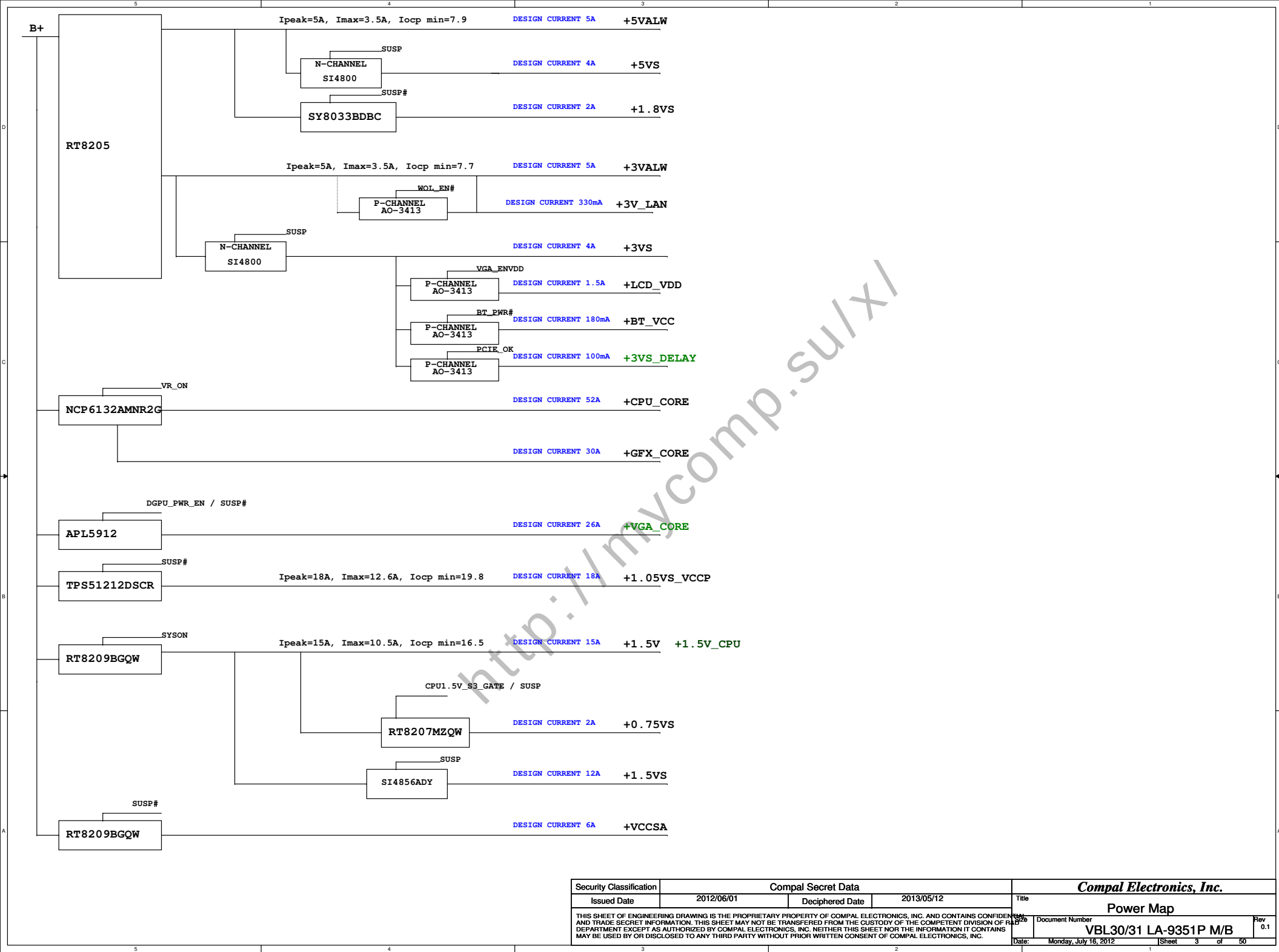
VBL30/31

LA-9351P REV0.1 Schematic

Intel Ivy Bridge/Panther Point
AMD Seymour XT
2012-05-08 Rev 0.1

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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	Cover Page	
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Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS
State		+3VALW	+1.5V_IO	
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

@	Reserve
CONN@	ME CONNECTOR
KB9012@	ENE EC
Nuvton@	Nuvton EC
NOW8@	not Support Win8
WIN8@	Support Win8
UMA@	UMA Sku
PX@	PX Sku

EC SM Bus1 address

Power	Device	Address
+3VALW	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	VGA Internal thermal sensor	1001 111Xb (0x9E)

PCH SM Bus address

Power	Device	Address
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b

SMBUS Control Table

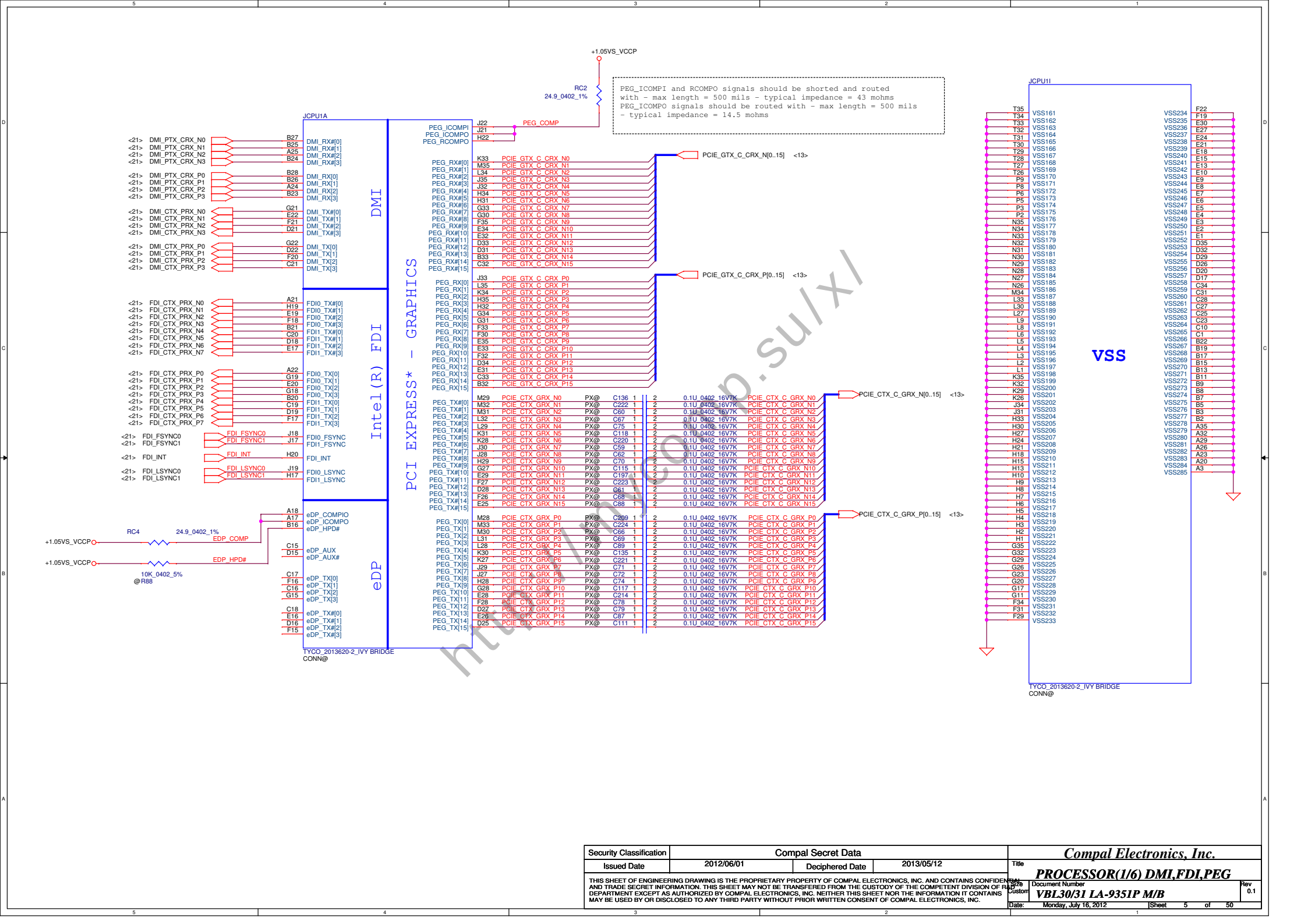
	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	✗	V	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW	+3VALW						
SMB_EC_CK2	KB9012	✗	✗	✗	✗	✗	✗	V
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	✗	✗	✗	V	V	✗	✗
SMBDATA	+3VALW				+3VS	+3VS		
SMLCLK	PCH	✗	✗	✗	✗	✗	✗	✗
SMLDATA	+3VALW							
SML1CLK	PCH	V	✗	V	✗	✗	V	✗
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

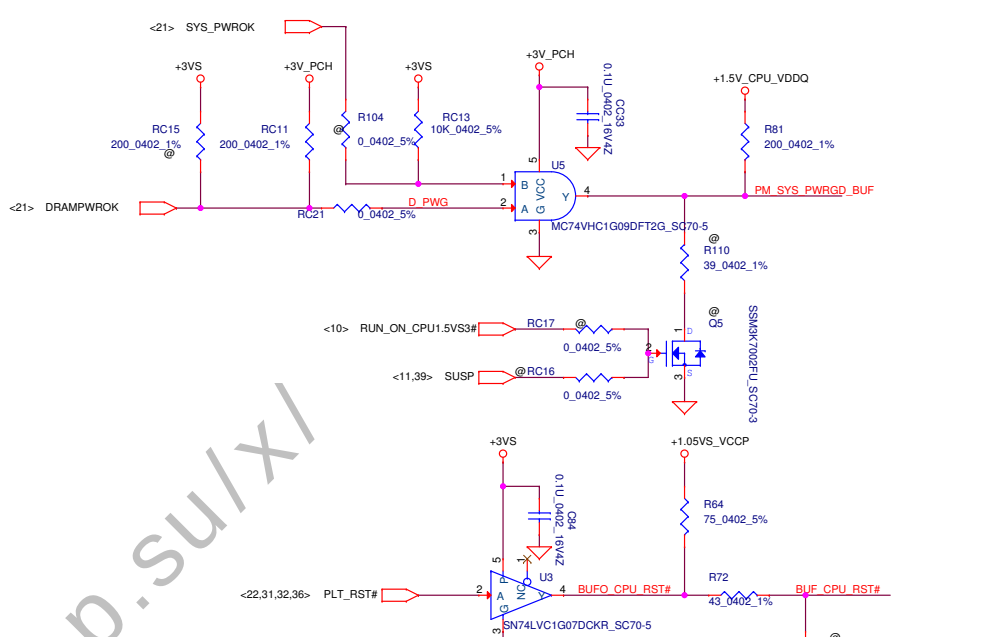
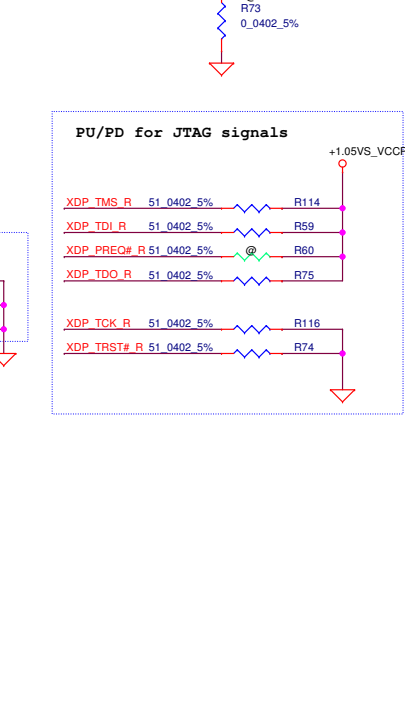
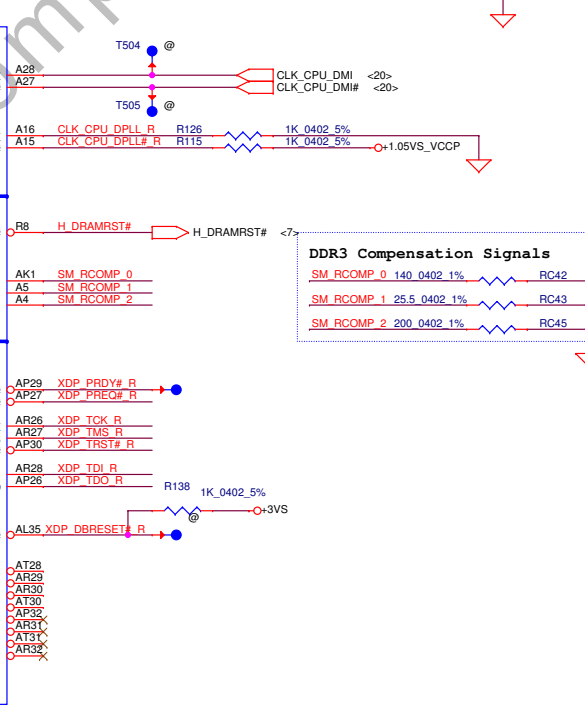
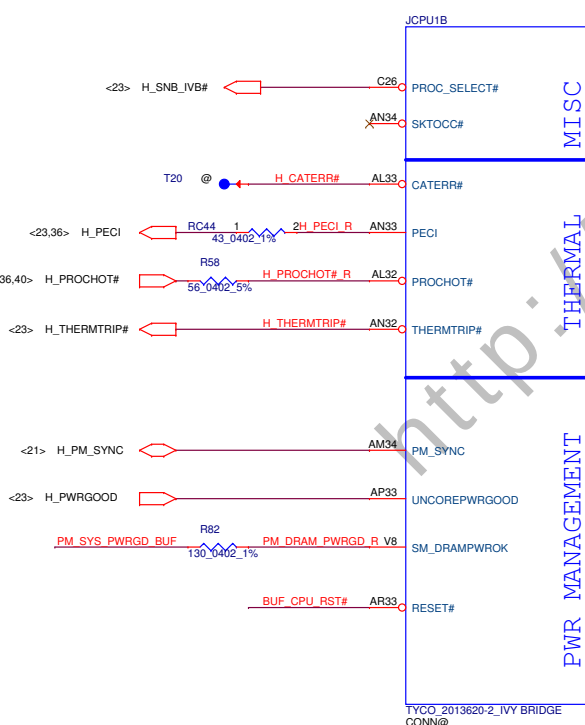
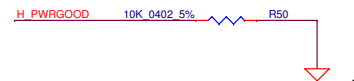
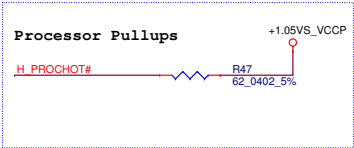
PCH X76 and PCBA table

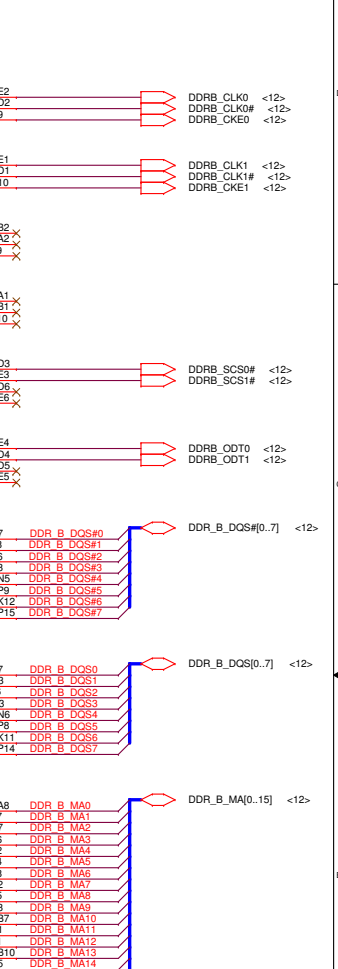
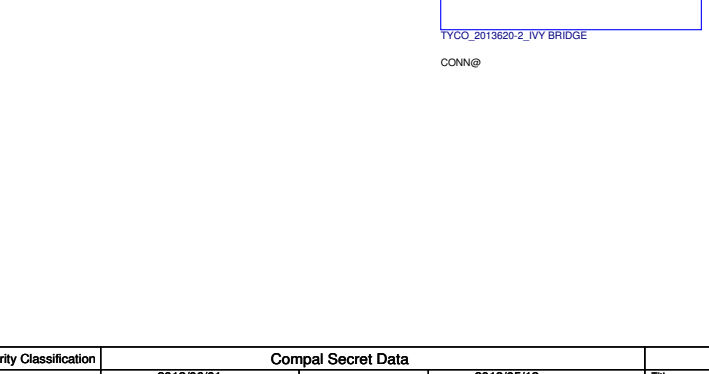
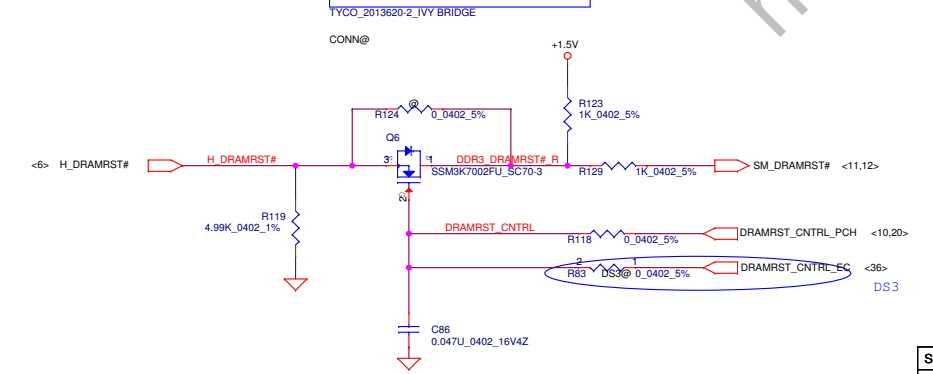
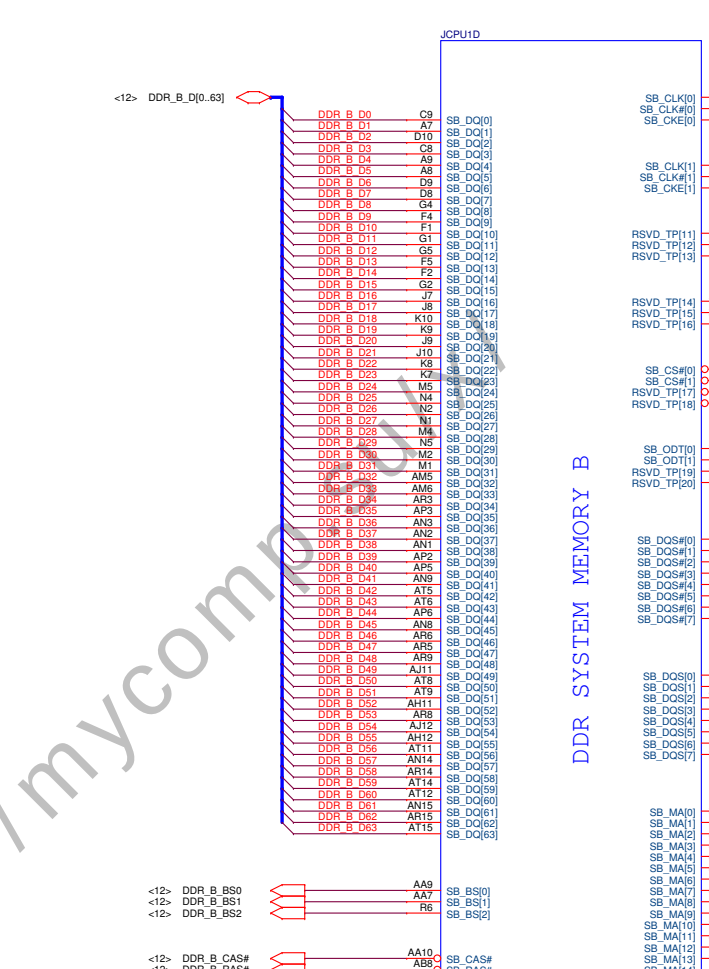
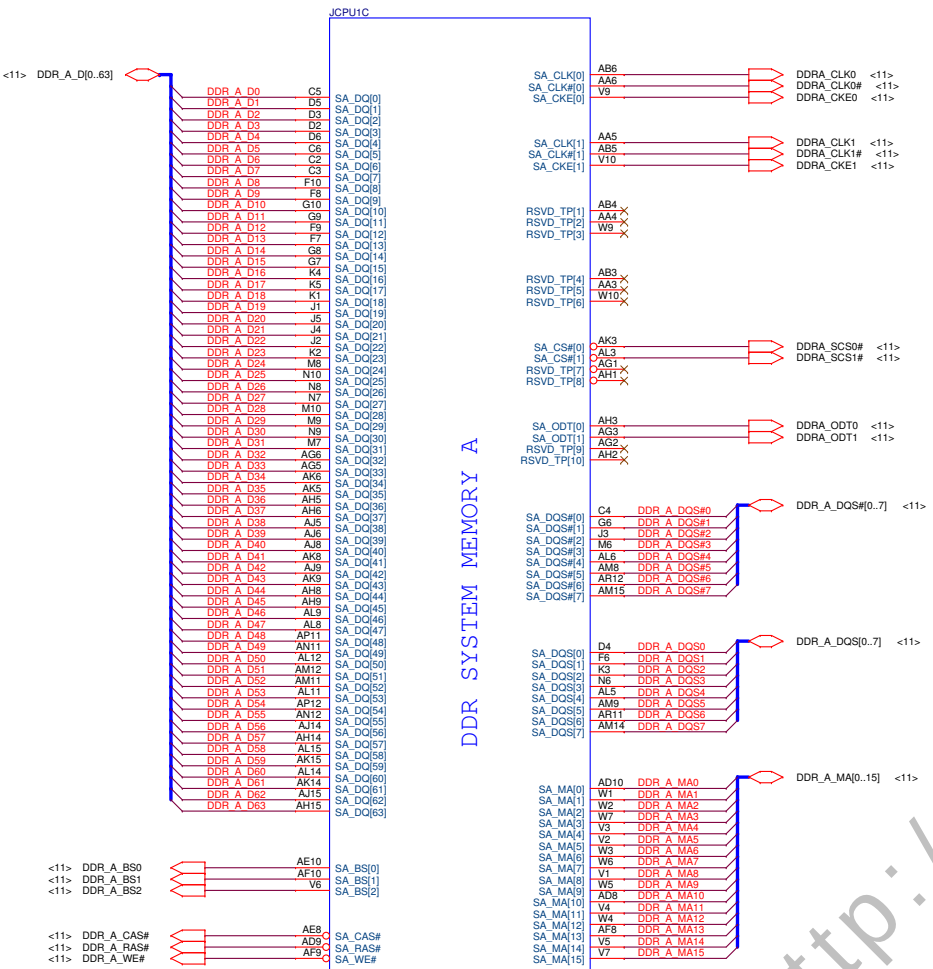
		config
X76	ZZZ X76@ HYN 1G	ZZZ @ HYN 1G R359 @ 10K_0402_5% R361 @ 10K_0402_5% R462 @ 10K_0402_5%
	ZZZ X76@ SAM 1G	ZZZ @ SAM 1G R360 @ 10K_0402_5% R361 @ 10K_0402_5% R461 @ 10K_0402_5%
PCH	UH1 BD82HM70 QPXH C1 BGA 989P PCH@	
PCB	ZZZ DA2@ PCB LA-6732P REV10	ZZZ DA8@ PCB LA-9351P REV01
		ZZZ DA4@ PCB LS-6732P REV10
		ZZZ DA2@ PCB LS-6731P REV10

(@/CONN@/DA2@/DA4@/DA8@/DAZ@/KB9012@/NOW8@/Nuvton@/PCH@/PX@/Rev01@/Rev02@/Rev03@/Rev04@/Rev10@/UMA@/WIN8@/X76@)

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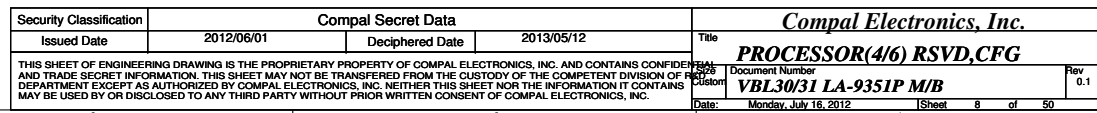
A circuit diagram showing a resistor labeled RC51 with a value of 1K_0402_1%. The resistor is connected to a pin labeled CFG2 and the other end is connected to ground, represented by a triangle symbol.

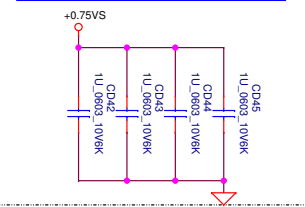
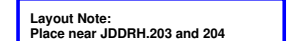
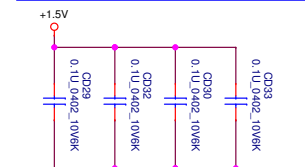
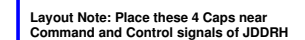
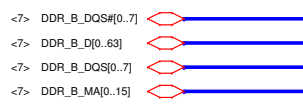
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed
------	---

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	---

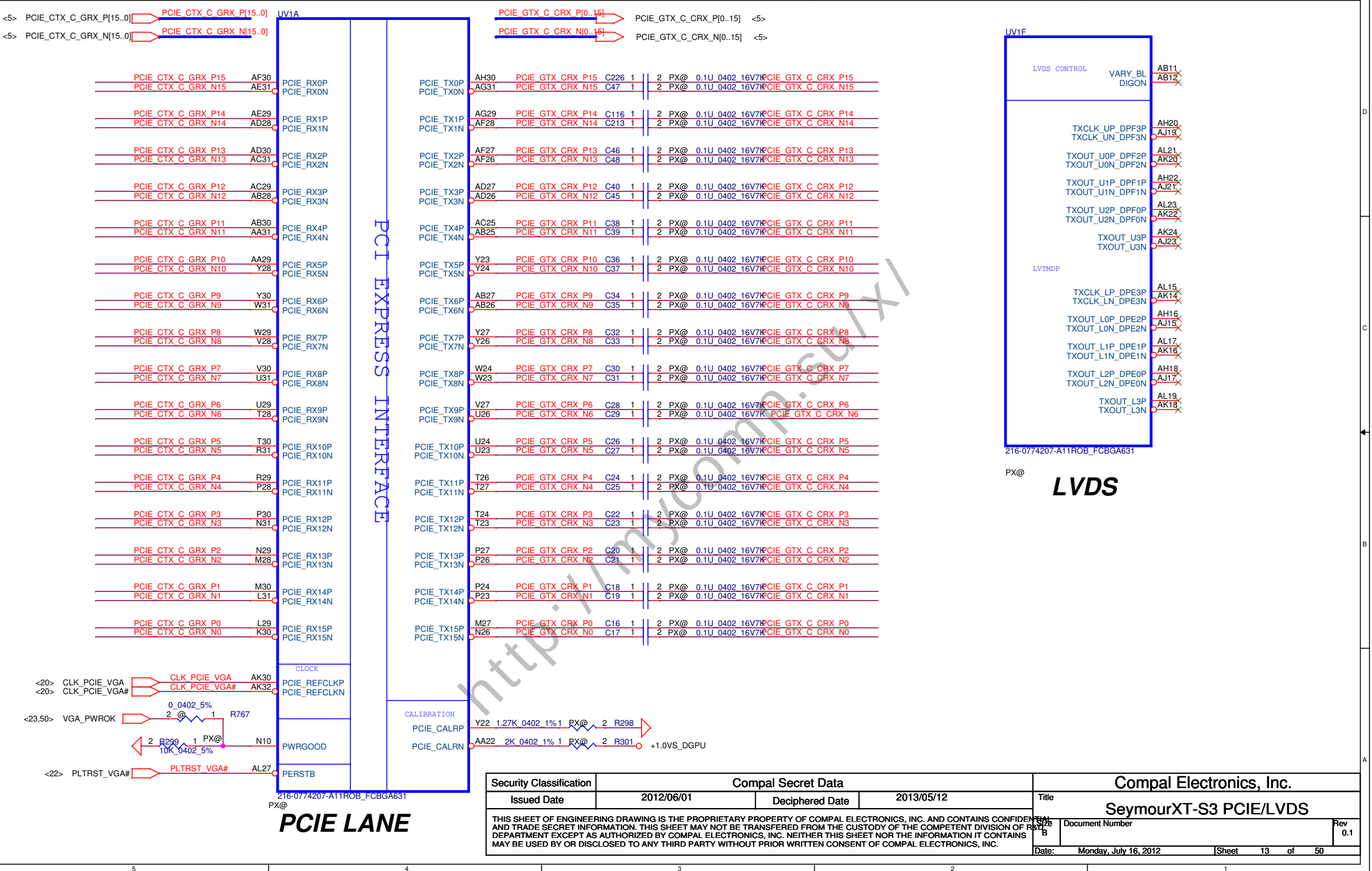
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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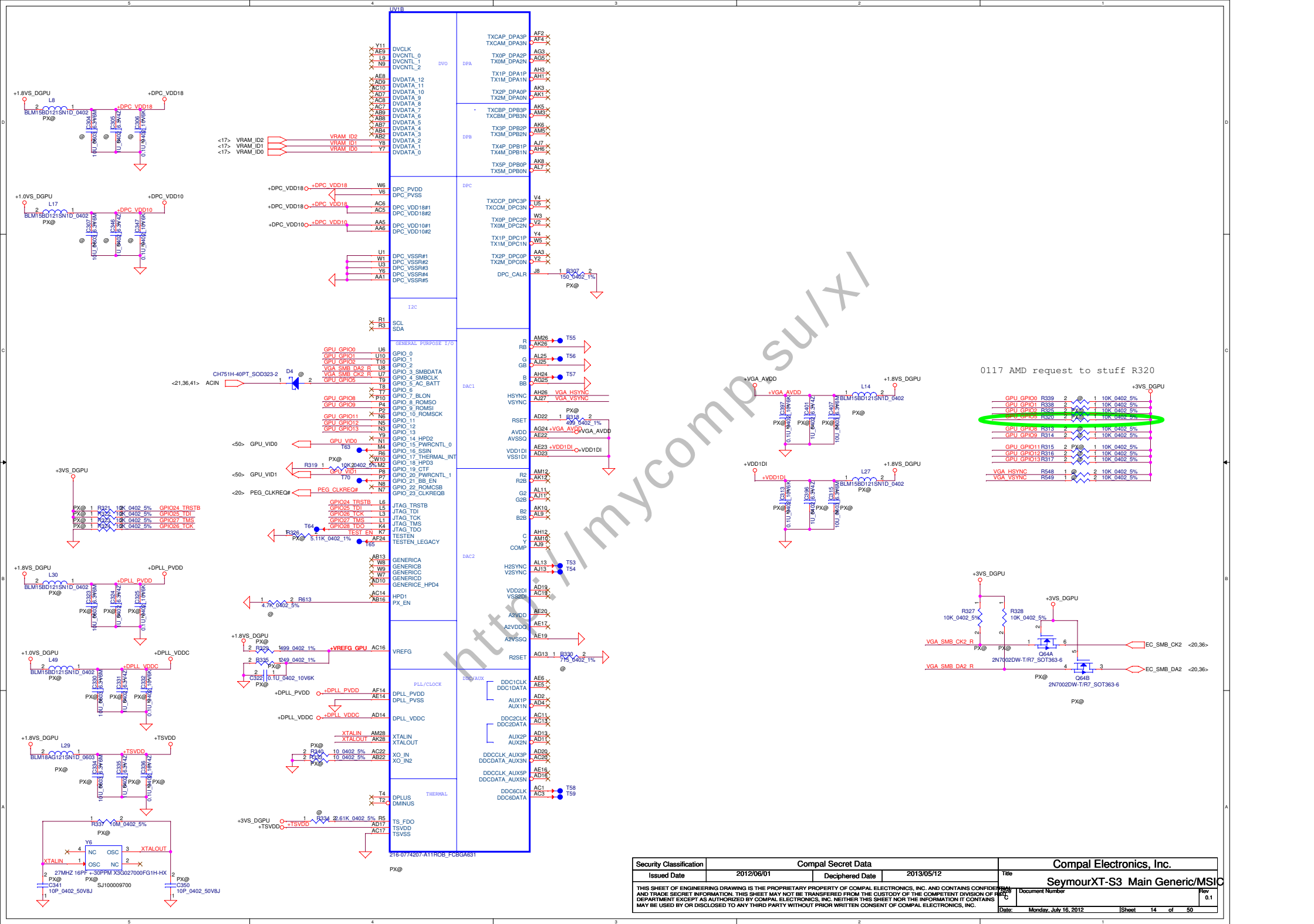
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training
------	---

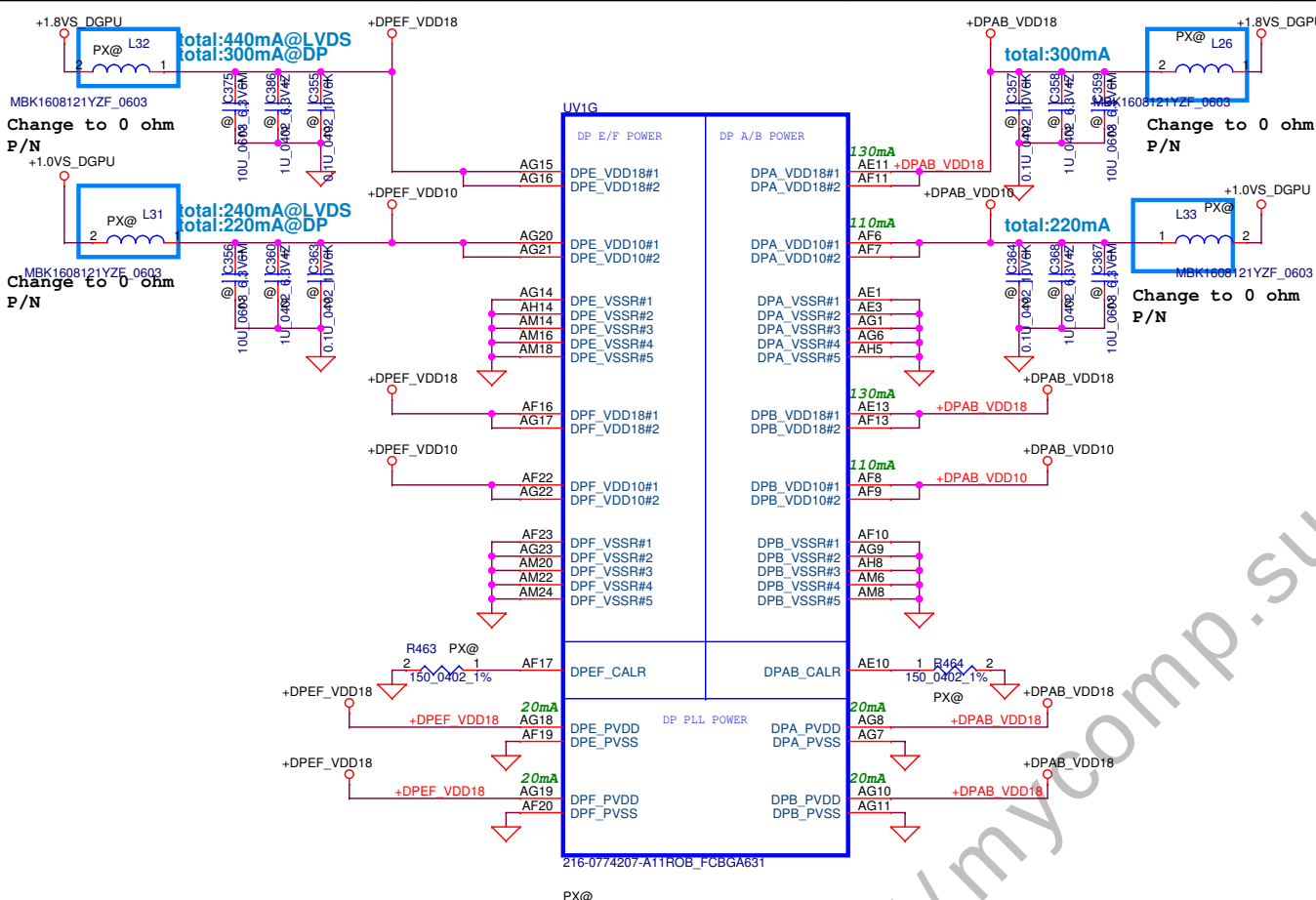




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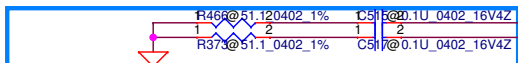
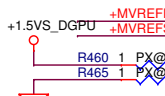
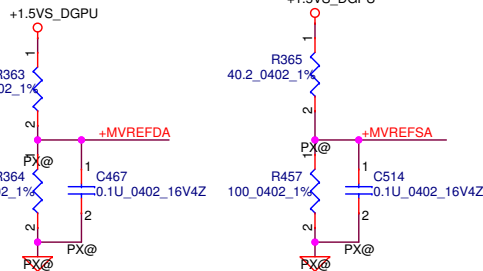
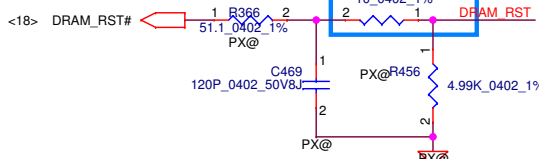




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<18> M_DA[63..0] M_DA[63..0]
<18> M_MA[13..0] M_MA[13..0]
<18> M_DQM[7..0] M_DQM[7..0]
<18> M_DQS[7..0] M_DQS[7..0]
<18> M_DQS# [7..0] M_DQS# [7..0]

PARK SCL has different recommend
9/28 change P/N to SD034100A00 R455



Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation, if not need, DNI.

M_DA0 K27
M_DA1 J29
M_DA2 H30
M_DA3 H32
M_DA4 G29
M_DA5 F28
M_DA6 F32
M_DA7 F30
M_DA8 C30
M_DA9 F27
M_DA10 A28
M_DA11 C28
M_DA12 E27
M_DA13 G26
M_DA14 D26
M_DA15 F25
M_DA16 A25
M_DA17 C25
M_DA18 E25
M_DA19 D24
M_DA20 E23
M_DA21 F23
M_DA22 D22
M_DA23 F21
M_DA24 E21
M_DA25 D20
M_DA26 F19
M_DA27 A19
M_DA28 D18
M_DA29 F17
M_DA30 A17
M_DA31 C17
M_DA32 E17
M_DA33 D16
M_DA34 F15
M_DA35 A15
M_DA36 D14
M_DA37 F13
M_DA38 A13
M_DA39 C13
M_DA40 E11
M_DA41 A11
M_DA42 C11
M_DA43 F11
M_DA44 A9
M_DA45 C9
M_DA46 F9
M_DA47 D8
M_DA48 E7
M_DA49 A7
M_DA50 C7
M_DA51 F7
M_DA52 A5
M_DA53 E5
M_DA54 C3
M_DA55 F1
M_DA56 G7
M_DA57 G6
M_DA58 G1
M_DA59 G3
M_DA60 J6
M_DA61 J1
M_DA62 J3
M_DA63 J5

UVIC
GDDR5/DDR3
GDDR5/DDR3
MEMORY INTERFACE
WCKA0_0/DQA_0
WCKA0_1/DQA_1
WCKA0_2/DQA_2
WCKA0_3/DQA_3
WCKA0_4/DQA_4
WCKA0_5/DQA_5
WCKA0_6/DQA_6
WCKA0_7/DQA_7
WCKA0_8/DQA_8
WCKA0_9/DQA_9
WCKA0_10/DQA_10
WCKA0_11/DQA_11
WCKA0_12/DQA_12
WCKA0_13/DQA_13
WCKA0_14/DQA_14
WCKA0_15/DQA_15
WCKA0_16/DQA_16
WCKA0_17/DQA_17
WCKA0B_0/DQMA_0
WCKA0B_1/DQMA_1
WCKA0B_2/DQMA_2
WCKA0B_3/DQMA_3
WCKA0B_4/DQMA_4
WCKA0B_5/DQMA_5
WCKA0B_6/DQMA_6
WCKA0B_7/DQMA_7
EDCA0_0/RDQSA_0
EDCA0_1/RDQSA_1
EDCA0_2/RDQSA_2
EDCA0_3/RDQSA_3
EDCA0_4/RDQSA_4
EDCA0_5/RDQSA_5
EDCA0_6/RDQSA_6
EDCA0_7/RDQSA_7
EDCA1_0/RDQSA_0
EDCA1_1/RDQSA_1
EDCA1_2/RDQSA_2
EDCA1_3/RDQSA_3
EDCA1_4/RDQSA_4
EDCA1_5/RDQSA_5
EDCA1_6/RDQSA_6
EDCA1_7/RDQSA_7
DBBIA0_0/WQDSA_0
DBBIA0_1/WQDSA_1
DBBIA0_2/WQDSA_2
DBBIA0_3/WQDSA_3
DBBIA0_4/WQDSA_4
DBBIA0_5/WQDSA_5
DBBIA0_6/WQDSA_6
DBBIA0_7/WQDSA_7
DBBIA1_0/WQDSA_0
DBBIA1_1/WQDSA_1
DBBIA1_2/WQDSA_2
DBBIA1_3/WQDSA_3
DBBIA1_4/WQDSA_4
DBBIA1_5/WQDSA_5
DBBIA1_6/WQDSA_6
DBBIA1_7/WQDSA_7
ADBIA0/ODTA0
ADBIA1/ODTA1
CLKA0
CLKA0B
CLKA1
CLKA1B
RASA0B
RASA1B
CASA0B
CASA1B
CSA0B_0
CSA0B_1
CSA1B_0
CSA1B_1
CKEA0
CKEA1
WEA0B
WEA1B
G25
H10
G14
G20

MAA0_0/MAA_0
MAA0_1/MAA_1
MAA0_2/MAA_2
MAA0_3/MAA_3
MAA0_4/MAA_4
MAA0_5/MAA_5
MAA0_6/MAA_6
MAA0_7/MAA_7
MAA0_8/MAA_8
MAA0_9/MAA_9
MAA0_10/MAA_10
MAA0_11/MAA_11
MAA0_12/MAA_12
MAA0_13/MAA_13
MAA0_14/MAA_14
MAA0_15/MAA_15
MAA1_0/MAA_1
MAA1_1/MAA_1
MAA1_2/MAA_10
MAA1_3/MAA_11
MAA1_4/MAA_12
MAA1_5/MAA_13/BA2
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MAA1_7/MAA_15/BA1
WCKA1B_0/DQMA_5
WCKA1B_1/DQMA_6
WCKA1B_1/DQMA_7
EDCA1_0/RDQSA_0
EDCA1_1/RDQSA_1
EDCA1_2/RDQSA_2
EDCA1_3/RDQSA_3
EDCA1_4/RDQSA_4
EDCA1_5/RDQSA_5
EDCA1_6/RDQSA_6
EDCA1_7/RDQSA_7
DBBIA1_0/WQDSA_0
DBBIA1_1/WQDSA_1
DBBIA1_2/WQDSA_2
DBBIA1_3/WQDSA_3
DBBIA1_4/WQDSA_4
DBBIA1_5/WQDSA_5
DBBIA1_6/WQDSA_6
DBBIA1_7/WQDSA_7
ADBIA0/ODTA0
ADBIA1/ODTA1
CLKA0
CLKA0B
CLKA1
CLKA1B
RASA0B
RASA1B
CASA0B
CASA1B
CSA0B_0
CSA0B_1
CSA1B_0
CSA1B_1
CKEA0
CKEA1
WEA0B
WEA1B
G25
H10
G14
G20

M_MA0 J20
M_MA1 H23
M_MA2 G23
M_MA3 G24
M_MA4 H24
M_MA5 J19
M_MA6 K19
M_MA7 J14
M_MA8 K14
M_MA9 J11
M_MA10 J13
M_MA11 H11
M_MA12 G11
M_BA0 J16
M_BA1 L15
M_DQM0 E32
M_DQM1 E30
M_DQM2 A21
M_DQM3 C21
M_DQM4 E13
M_DQM5 D12
M_DQM6 E3
M_DQM7 F4
M_DQS0 H28
M_DQS1 C27
M_DQS2 A23
M_DQS3 E19
M_DQS4 E15
M_DQS5 D10
M_DQS6 D6
M_DQS7 G5
M_DQS#0 H27
M_DQS#1 A27
M_DQS#2 C23
M_DQS#3 C19
M_DQS#4 C15
M_DQS#5 E9
M_DQS#6 C5
M_DQS#7 H4
VRAM_ODT0 L18
VRAM_ODT1 K16
M_CLK0 H26
M_CLK#0 H25
M_CLK1 G9
M_CLK#1 H9
M_RAS#0 G22
M_RAS#1 G17
M_CAS#0 G19
M_CAS#1 G16
M_CS#0 H22
M_CS#1 G13
M_CKE0 K20
M_CKE1 J17
M_WE#0 G25
M_WE#1 H10
M_MA13 G14
G20

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M_BA0 <18>
M_BA1 <18>

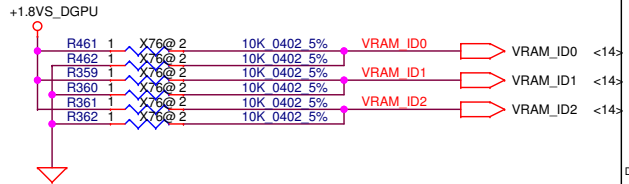
64MX16 (512MB)

64MX16 (512MB)

128M16 (1GB)

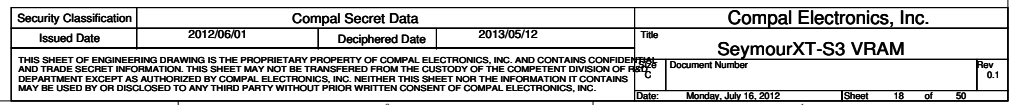
128M16 (1GB)

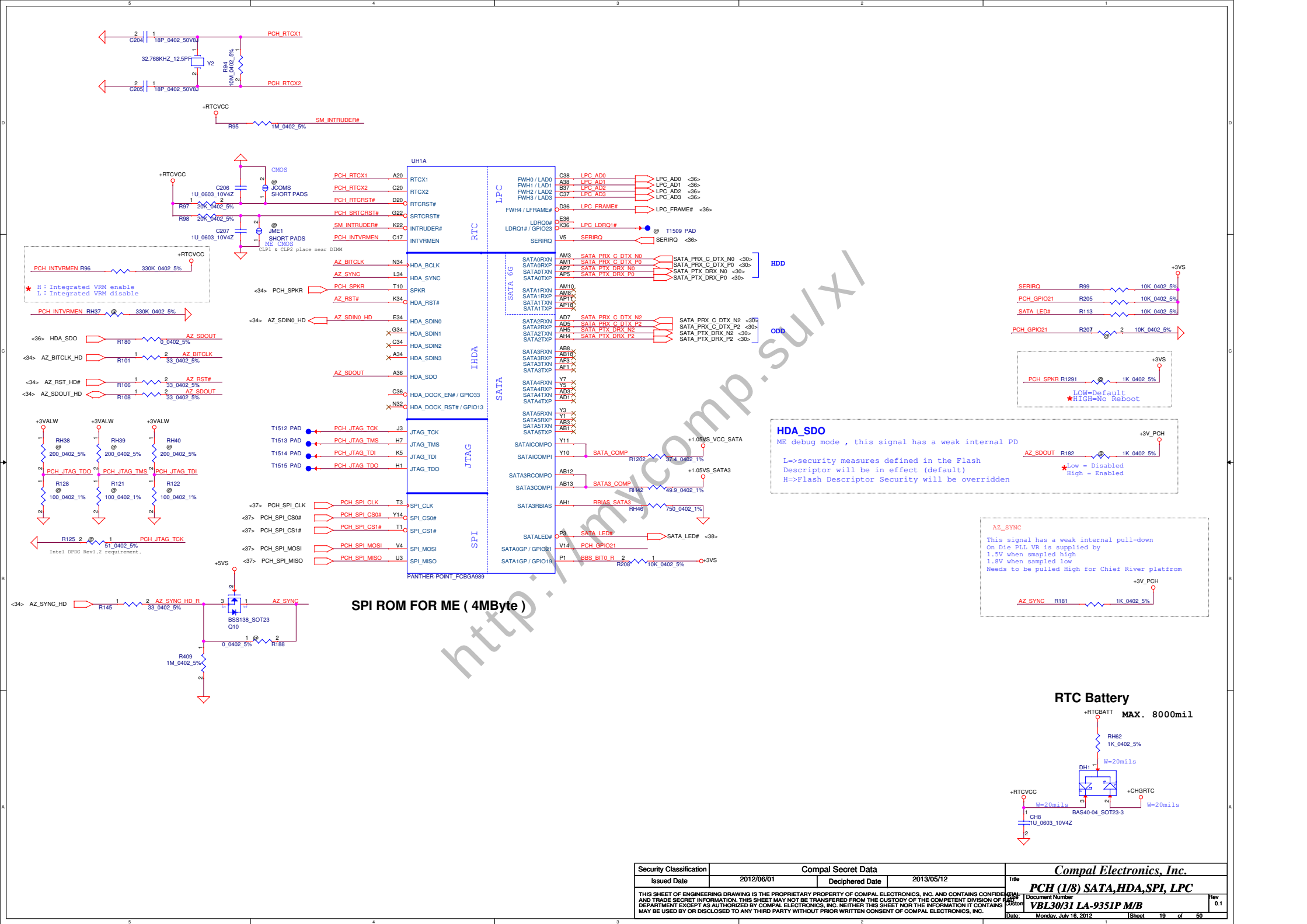
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M_RAS#0 <18>
M_RAS#1 <18>
M_CAS#0 <18>
M_CAS#1 <18>
M_CS#0 <18>
M_CS#1 <18>
M_CKE0 <18>
M_CKE1 <18>
M_WE#0 <18>
M_WE#1 <18>

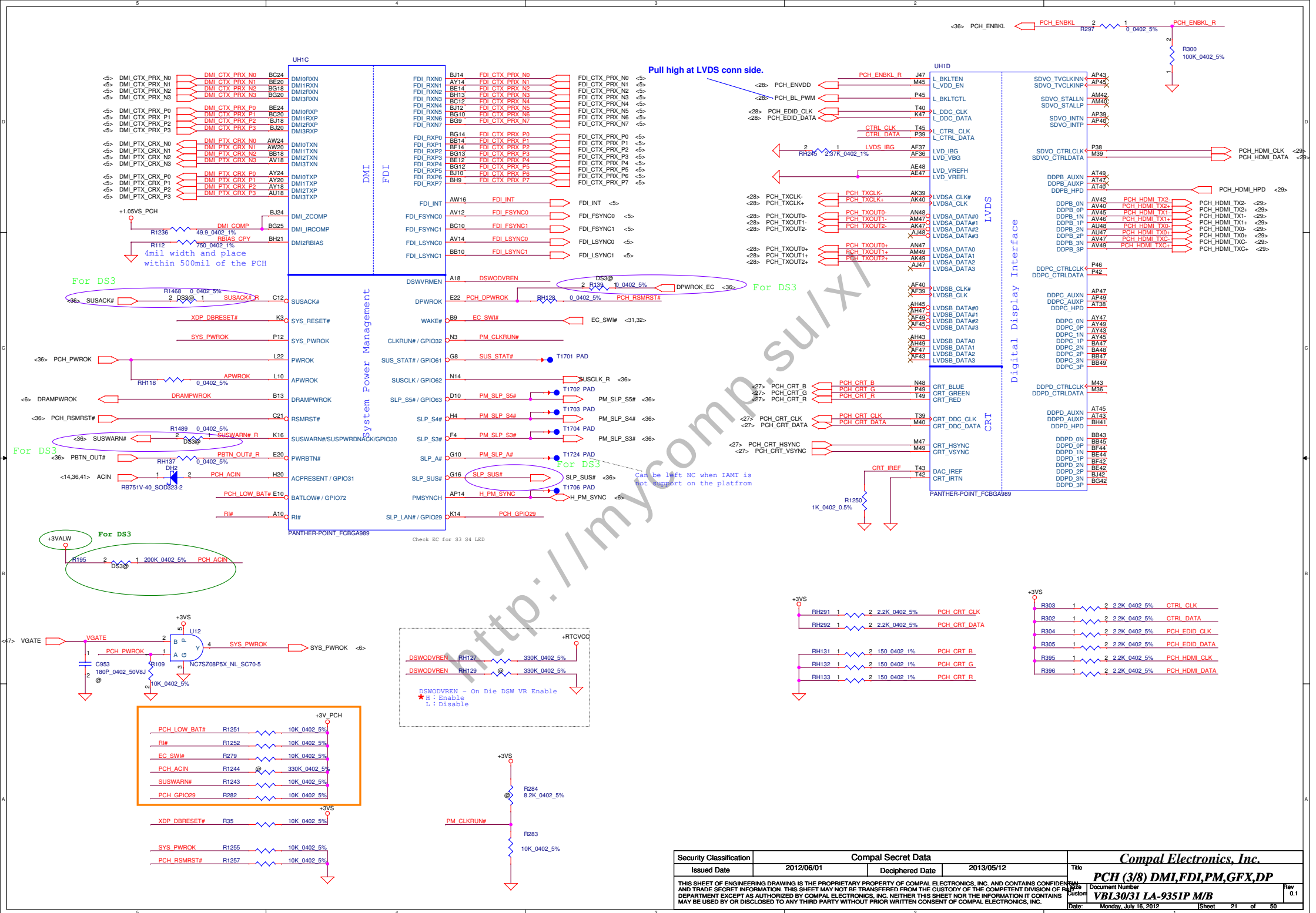


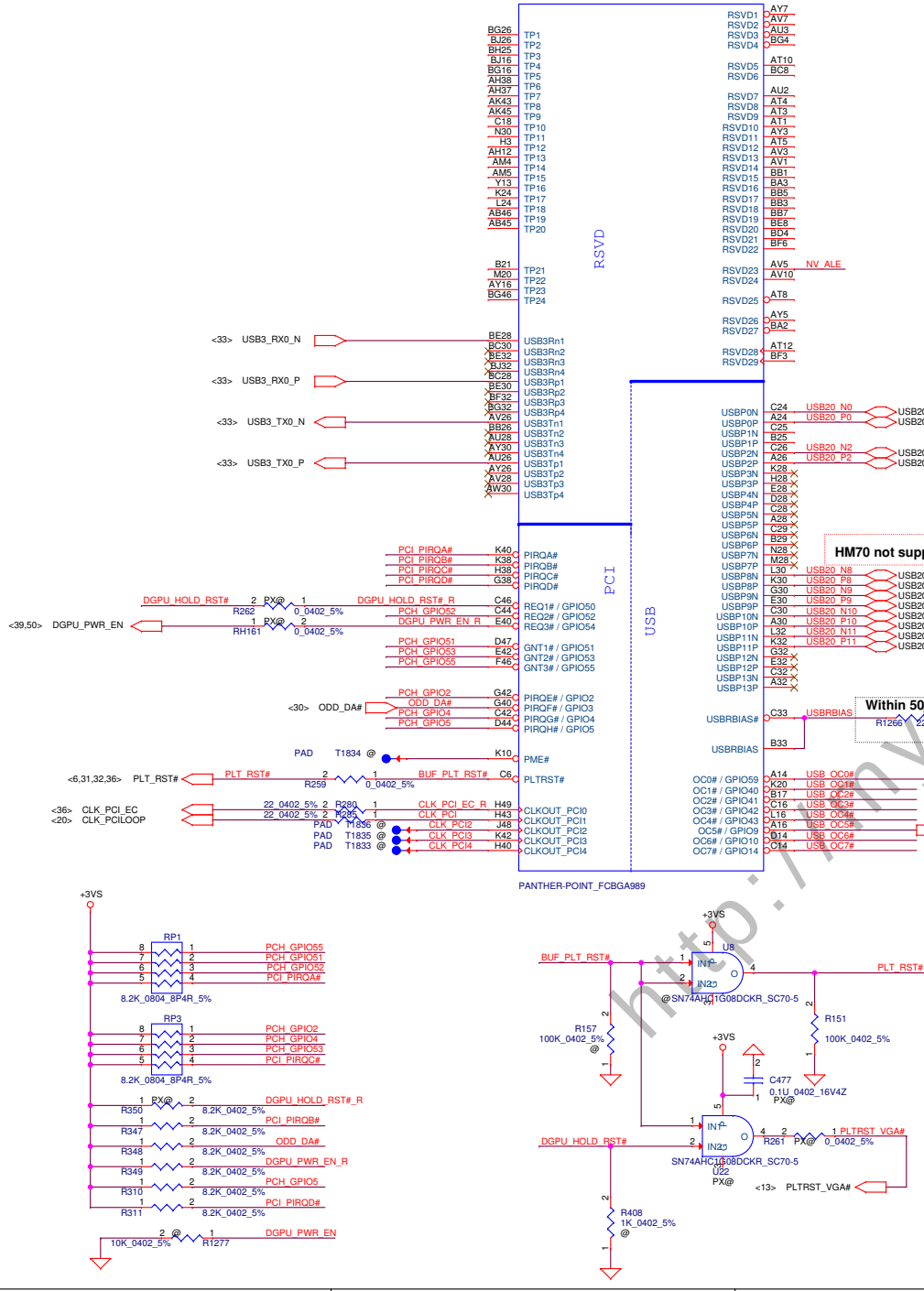
Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
K4W1G1646G-BC11 Samsung 128MB PN:SA00004GS00	R461	R360	R362
H5TQ1G63DFR-11C Hynix 128MB PN:SA000041S20	R462	R359	R362
K4W2G1646C-BC11 Samsung 256MB PN:SA000047Q00	R461	R360	R361
H5TQ2G63BFR-11C/H5TQ2G63DFR-11C Hynix 256MB PN:SA00003YO10/ SA00003Y0A0	R462	R359	R361

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				Document Number
				Rev 0.1
				Date: Monday, July 16, 2012
				Sheet 17 of 50









GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI ★

Intel Anti-Theft Techonlogy

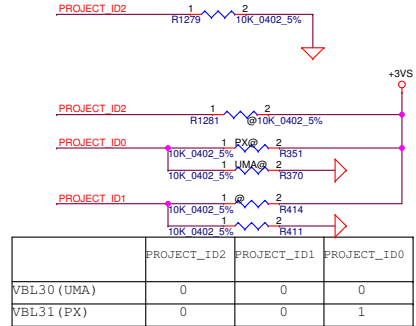
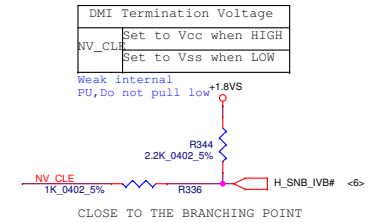
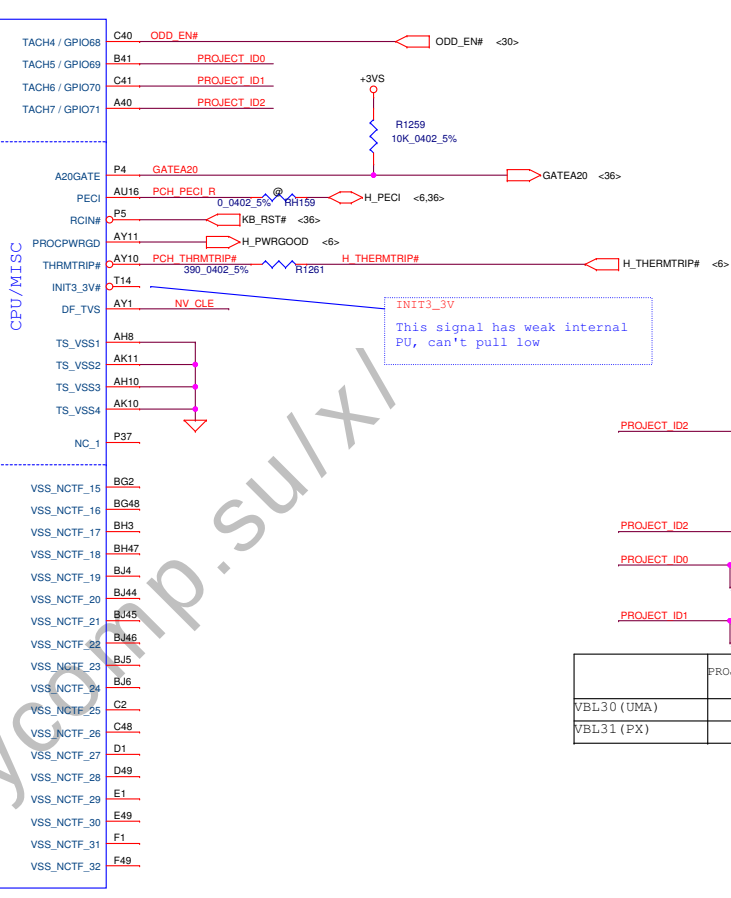
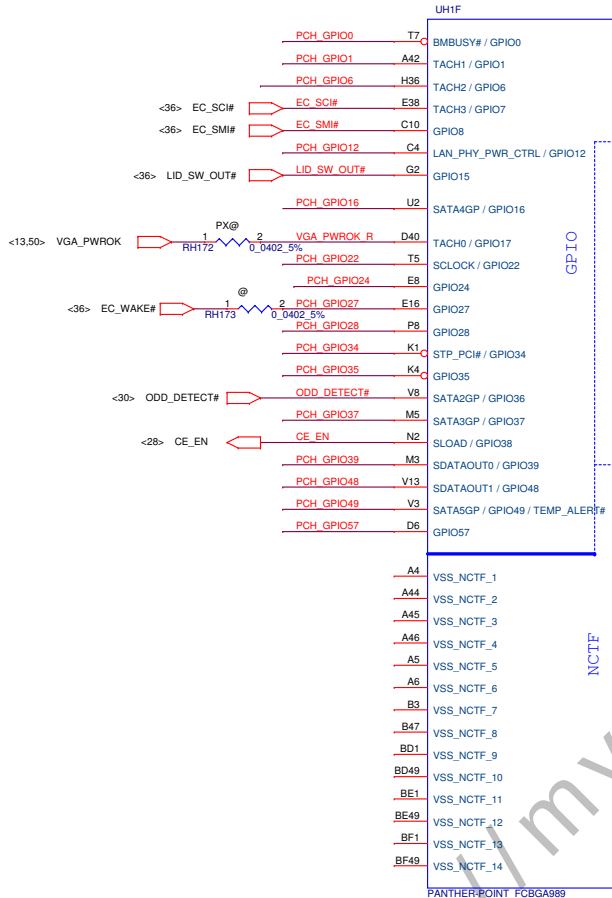
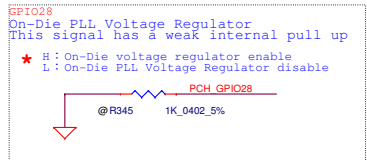
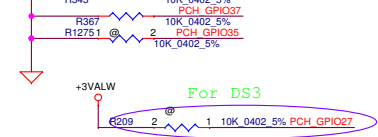
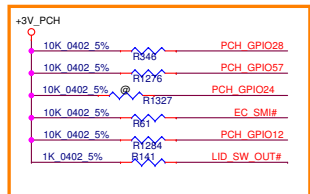
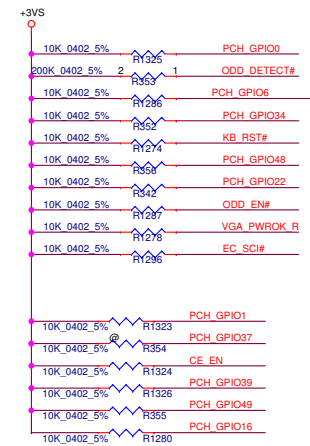
NV_AL#	High=Enabled	Low=Disable(floating) ★
1	0	1

NV_AL# @R341 1K 0402 5% +1.8VS

USB_OC0#

USB_OC0#	1	2
USB_OC1#	1	2
USB_OC5#	1	2
USB_OC6#	1	2
USB_OC2#	1	2
USB_OC3#	1	2
USB_OC4#	1	2
USB_OC7#	1	2

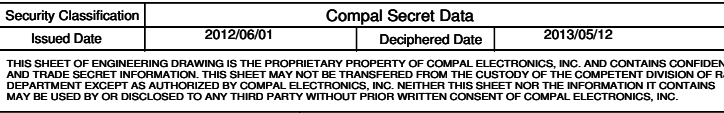
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	PCH (4/8) PCI, USB, NVRAM
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				Rev	0.1
				Date	Monday, July 16, 2012
				Sheet	22 of 50

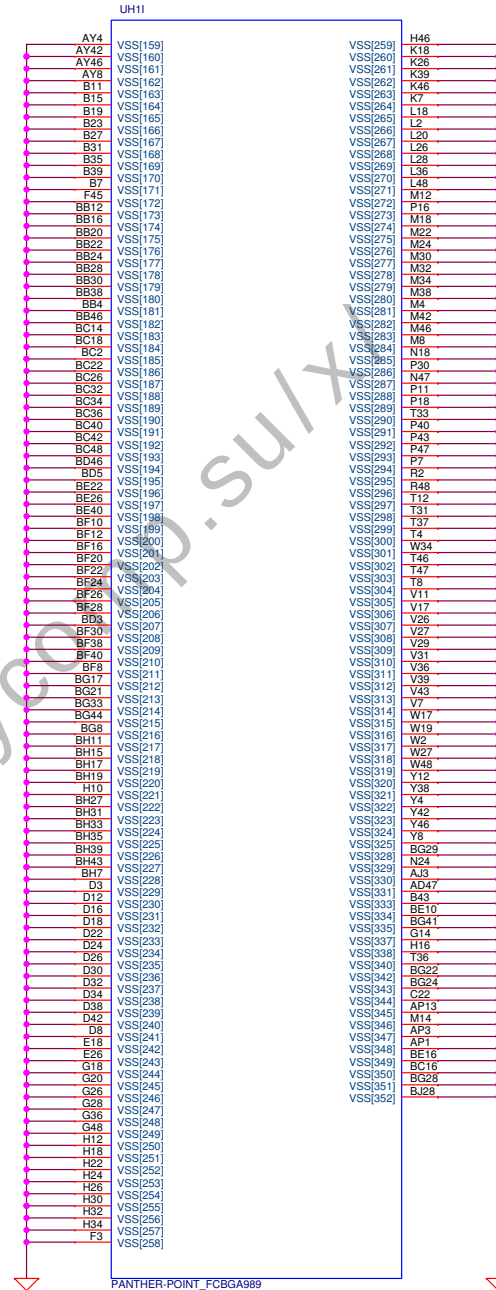
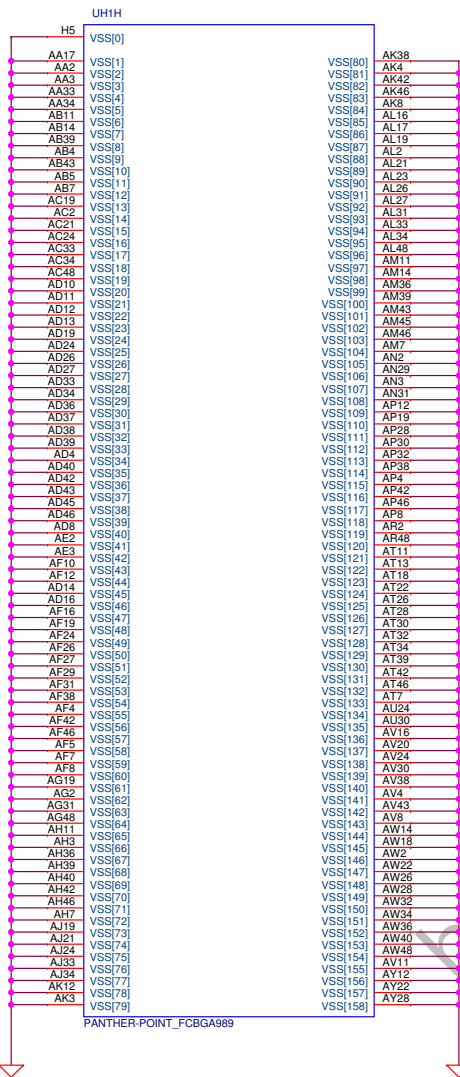


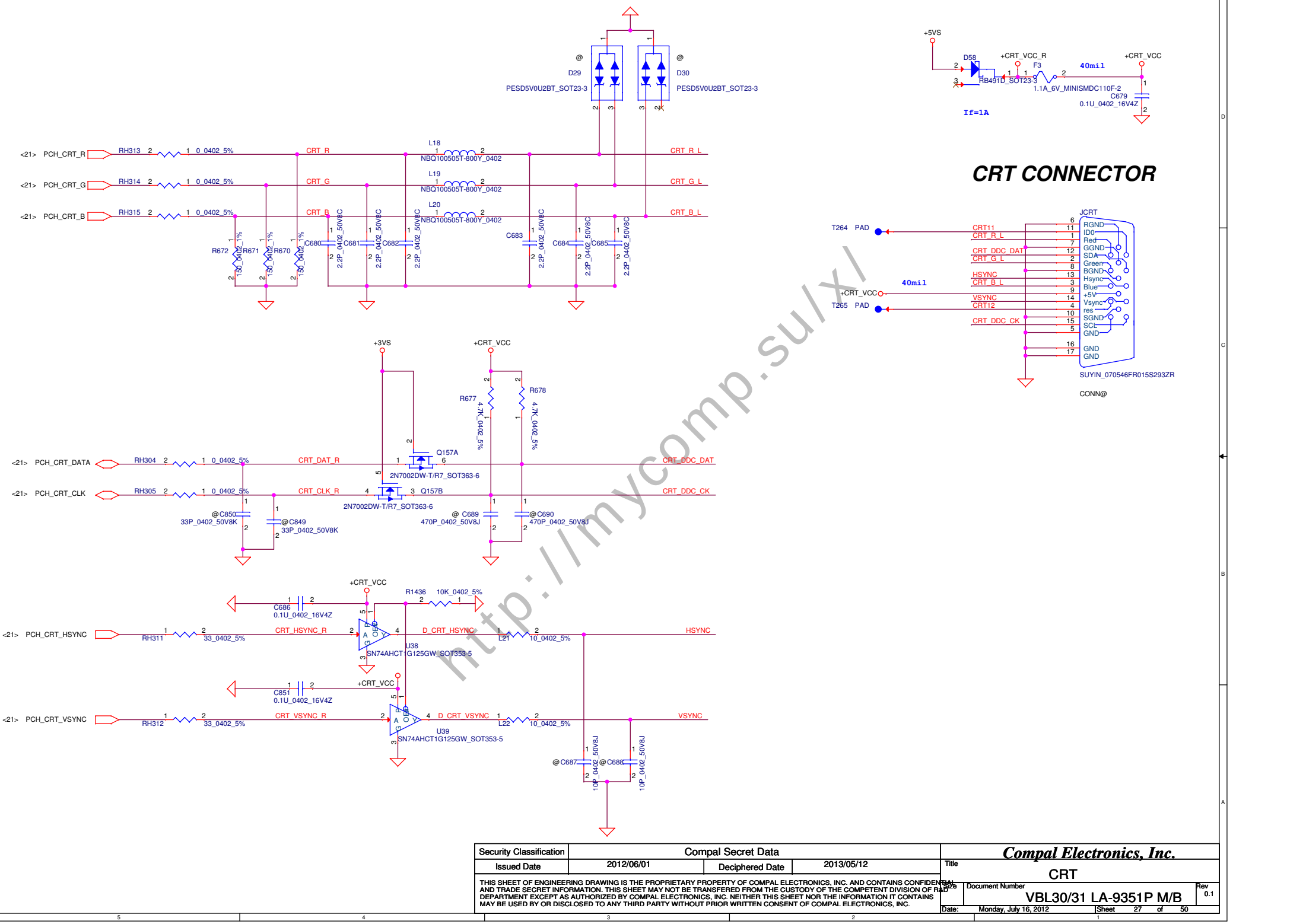
	PROJECT_ID2	PROJECT_ID1	PROJECT_ID0
VBL30 (UMA)	0	0	0
VBL31 (PX)	0	0	1

PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16
Please refer to Huron River Debug Board DG 1.2

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	PCH (5/8) GPIO, CPU, MISC
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				Date	Monday, July 16, 2012
				Sheet	23 of 50

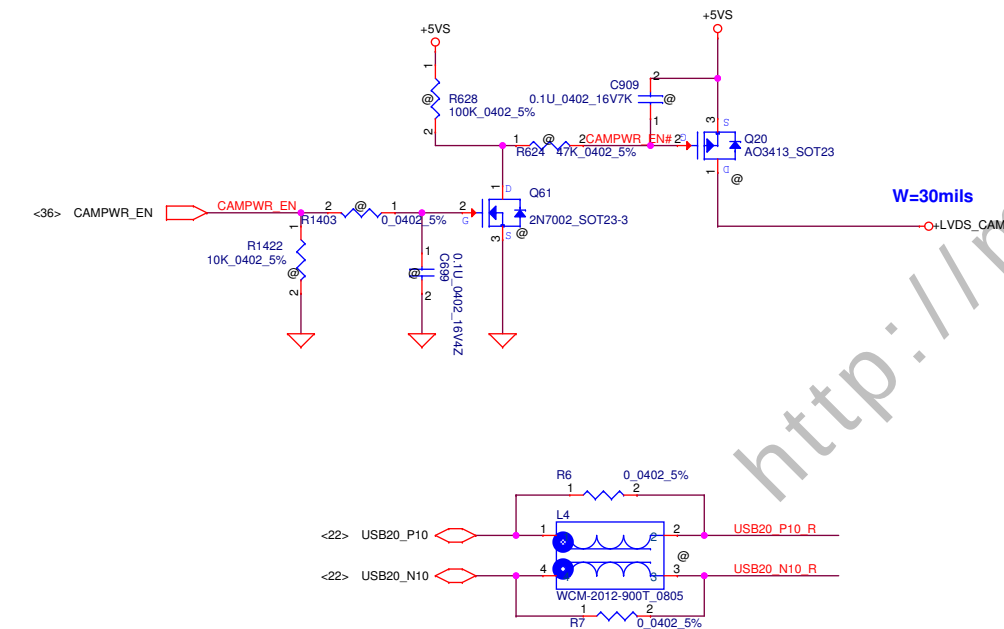
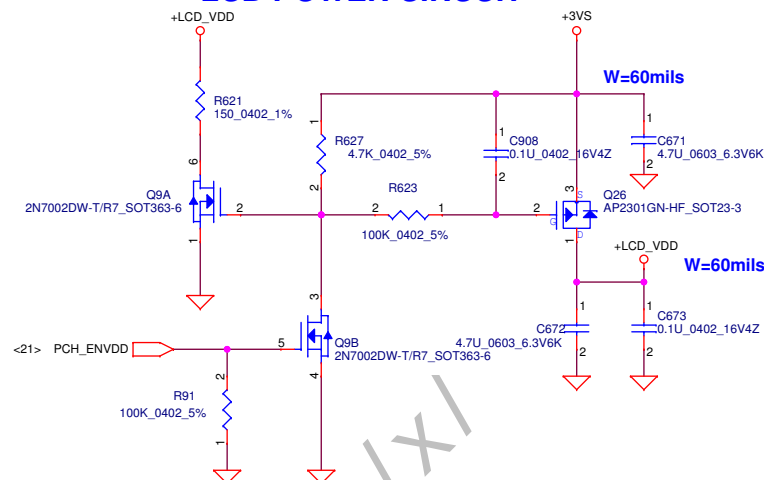
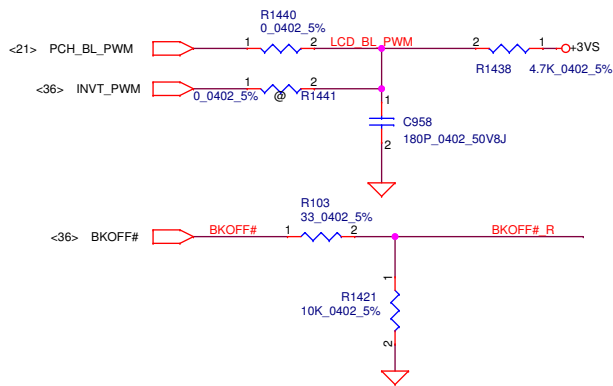




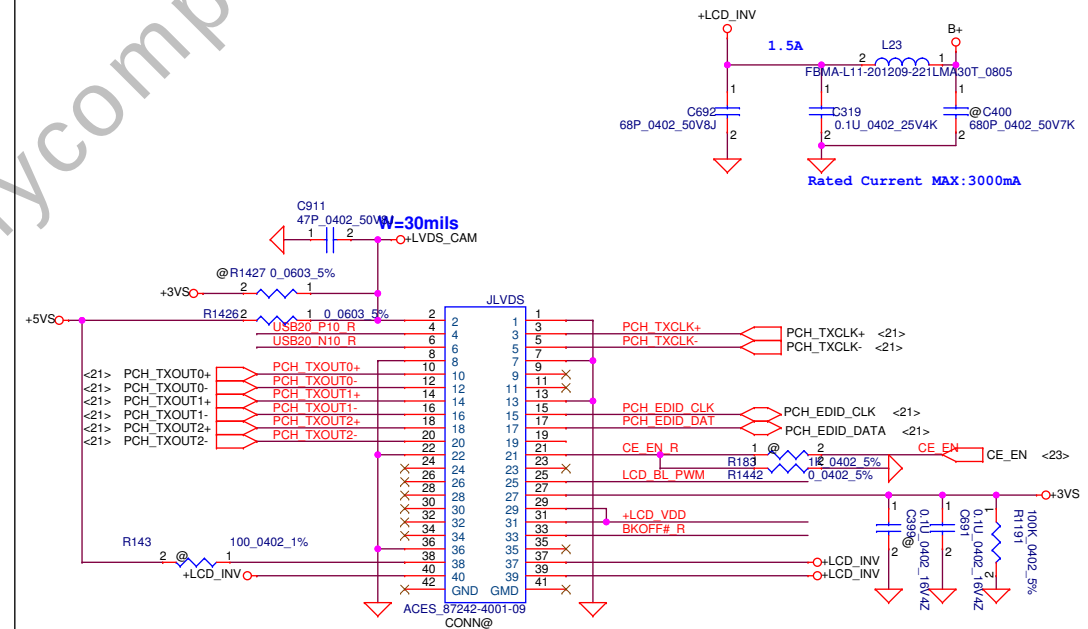


CRT CONNECTOR

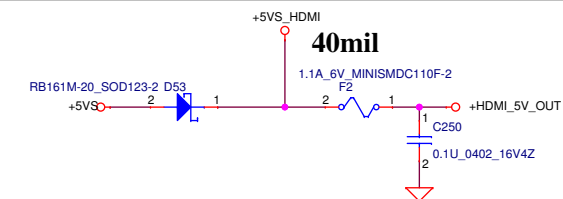
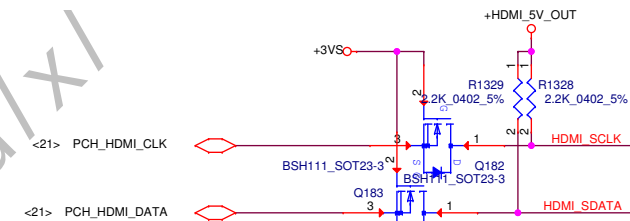
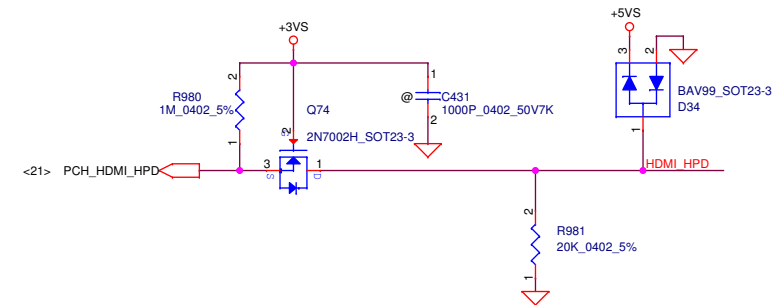
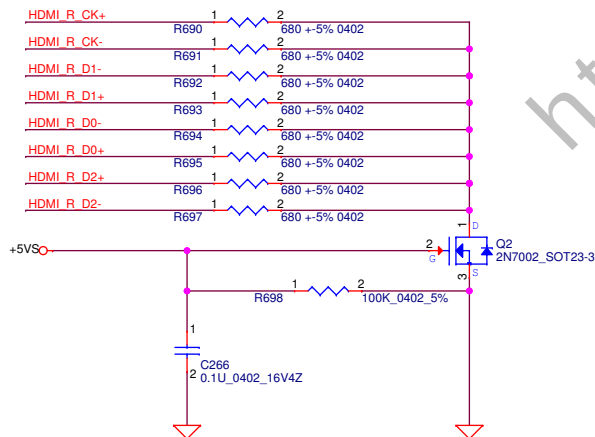
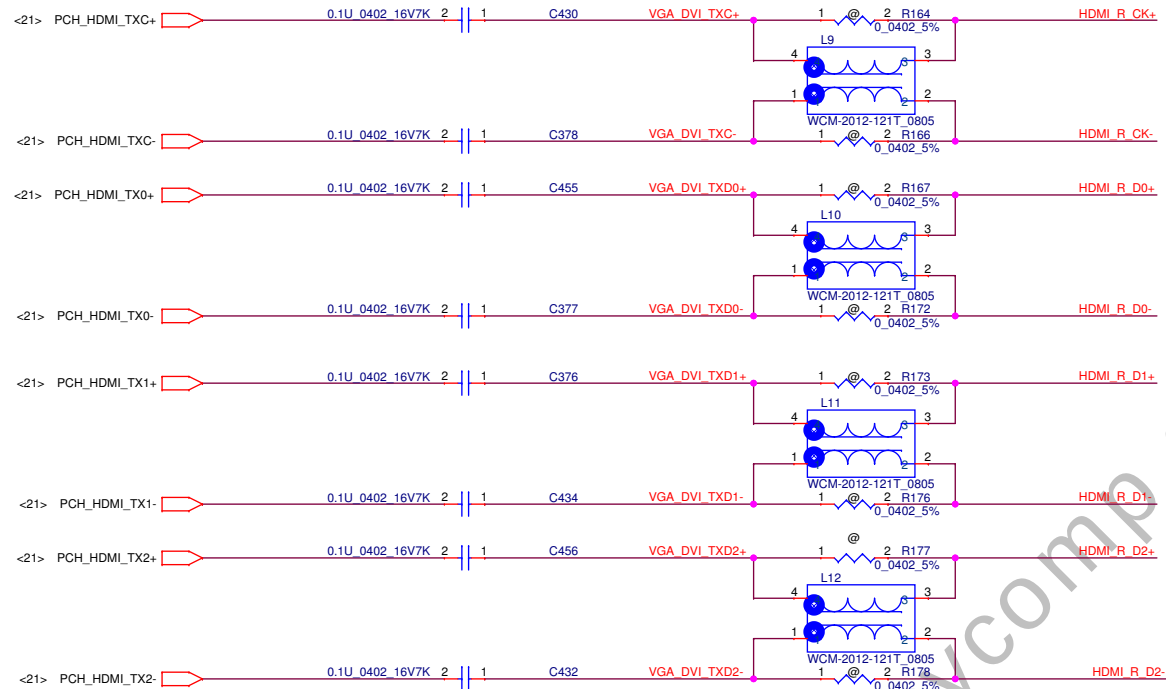
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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	CRT
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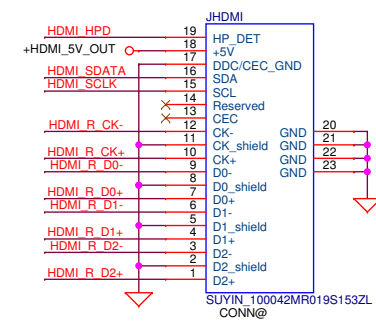
LCD/PANEL BD. Conn.



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				Date:	Monday, July 16, 2012	Sheet	28	of 50

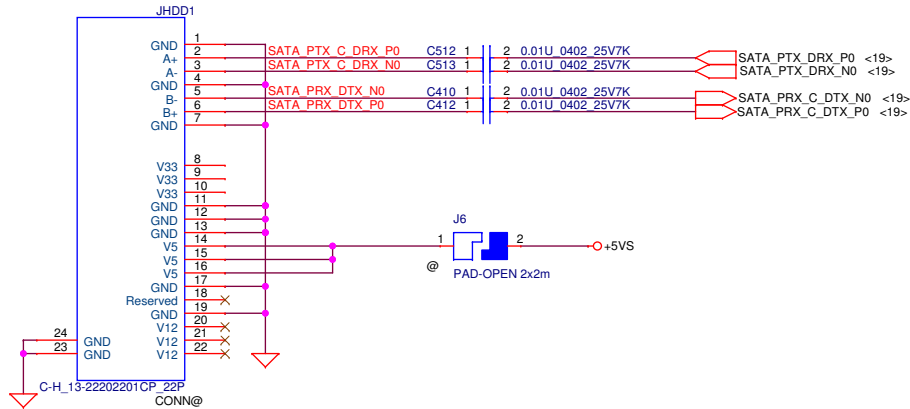
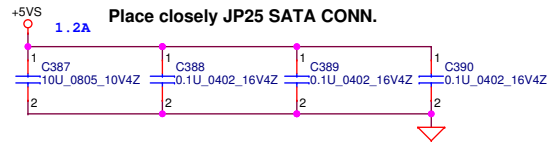


HDMI Connector

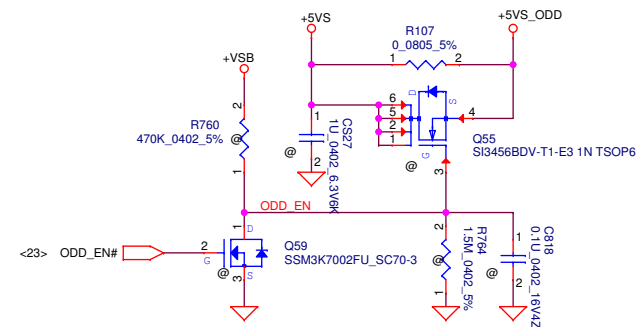
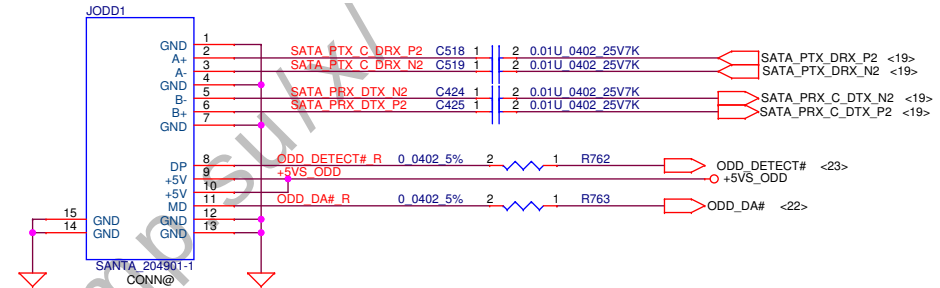
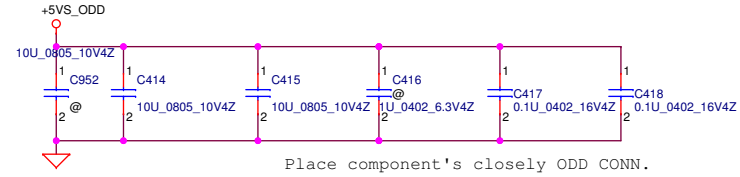


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				Date	Monday, July 16, 2012
				Sheet	29 of 50

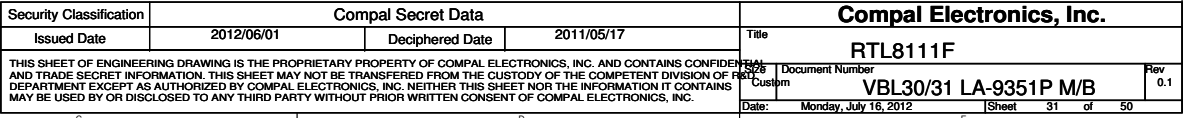
SATA HDD1 Conn.



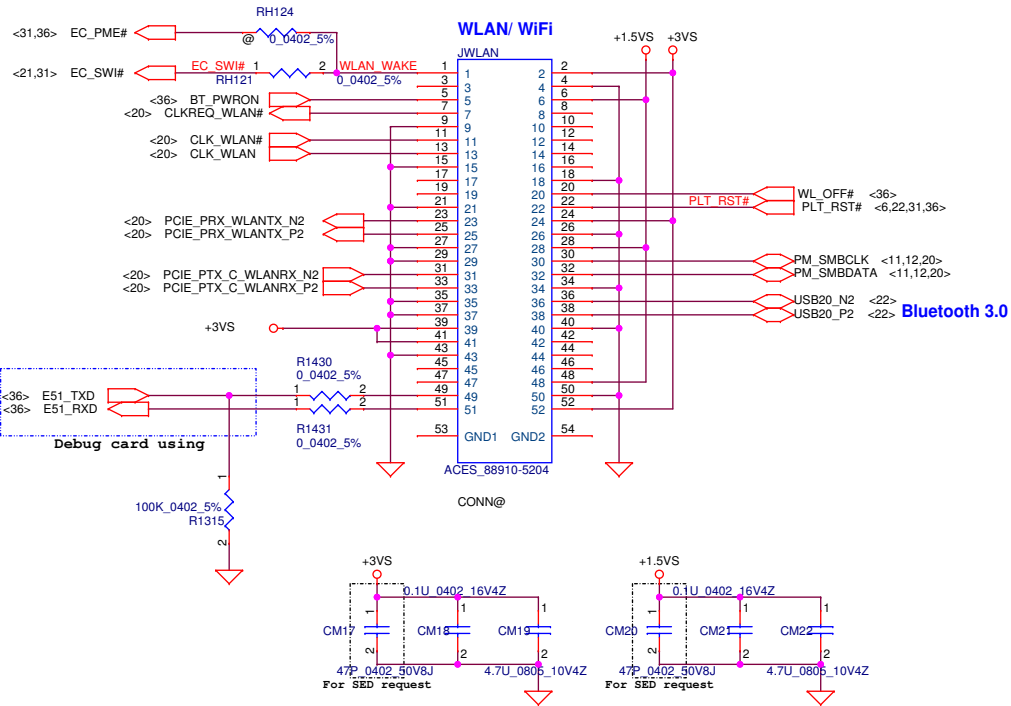
SATA ODD Conn



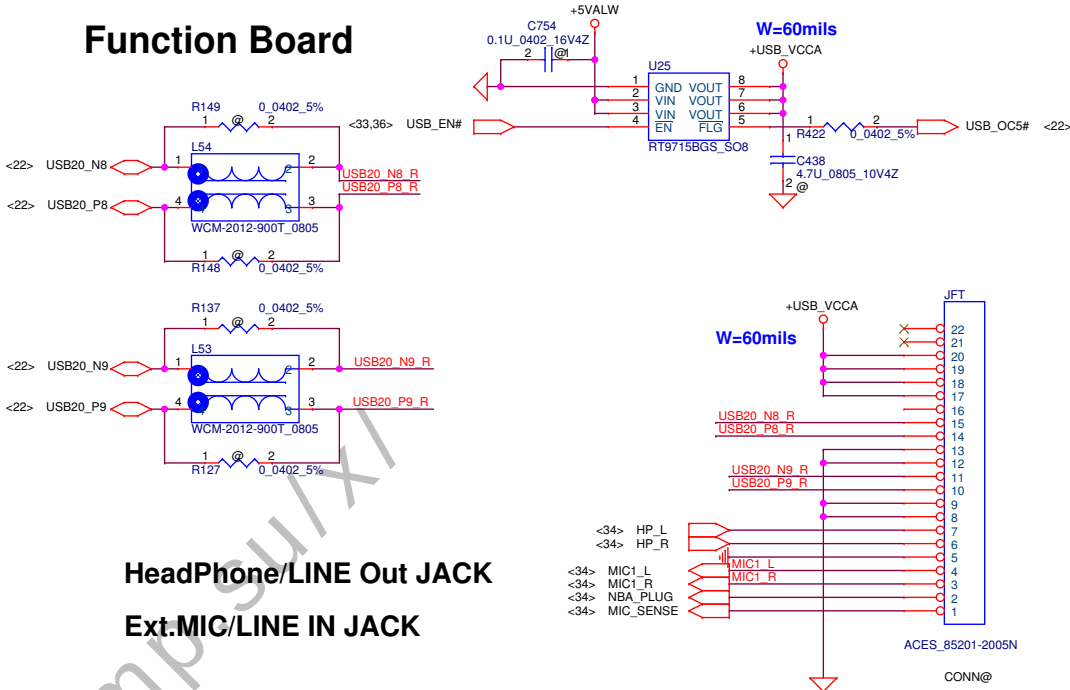
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	SATA-HDD/ODD
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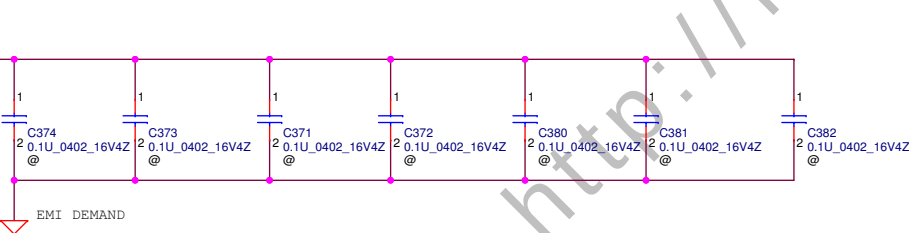
Slot 1 Half PCIe Mini Card-WLAN & BT3.0



Function Board

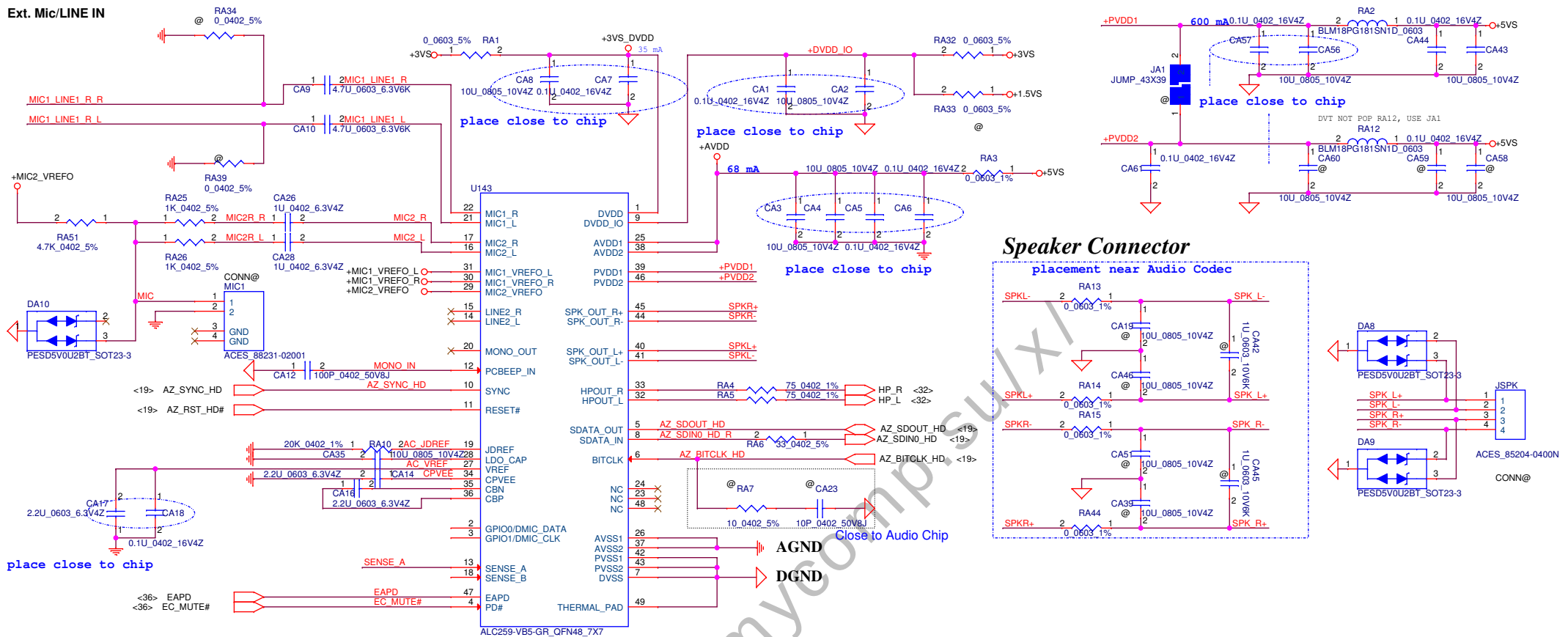


HeadPhone/LINE Out JACK
Ext.MIC/LINE IN JACK

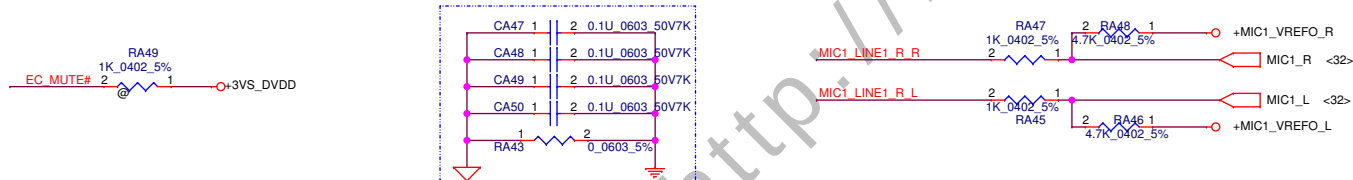


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				Date	Monday, July 16, 2012
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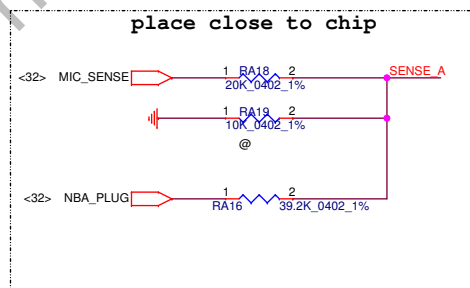
Ext. Mic/LINE IN



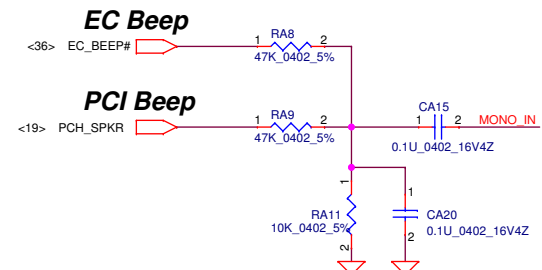
Ext.MIC/LINE IN JACK



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

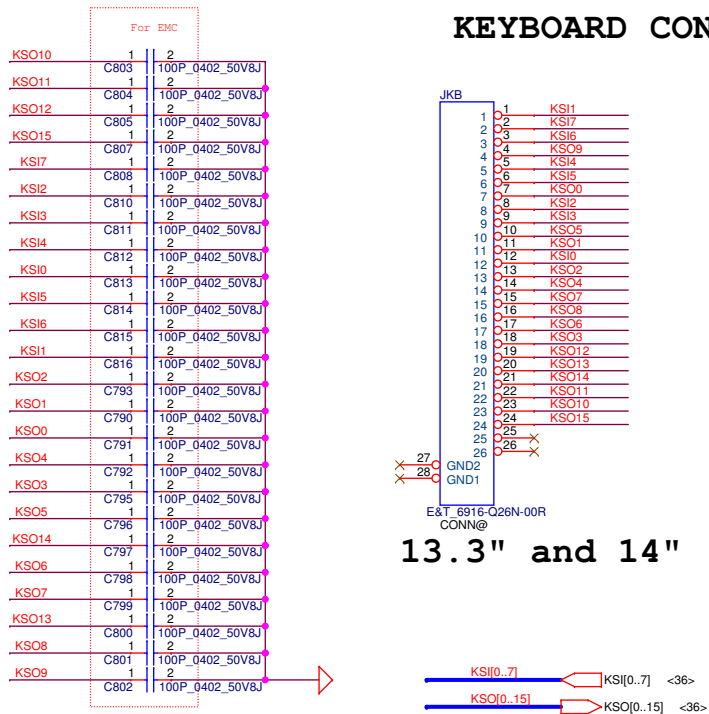


Beep sound

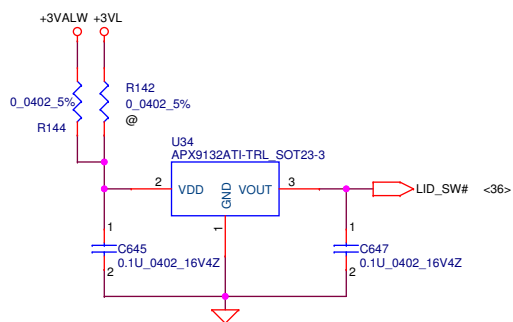


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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	
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				VBL30/31 LA-9351P M/B Date: Monday, July 16, 2012	0.1 Sheet 34 of 50

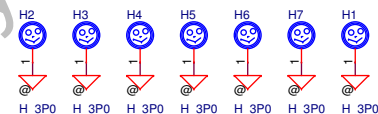
KEYBOARD CONN.



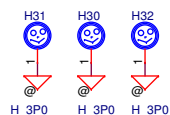
Lid SW



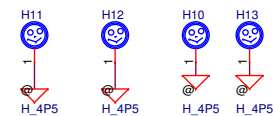
Screw Hole



Break hole



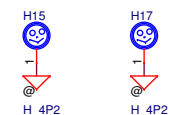
CPU



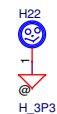
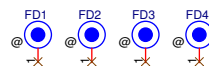
JWLAN



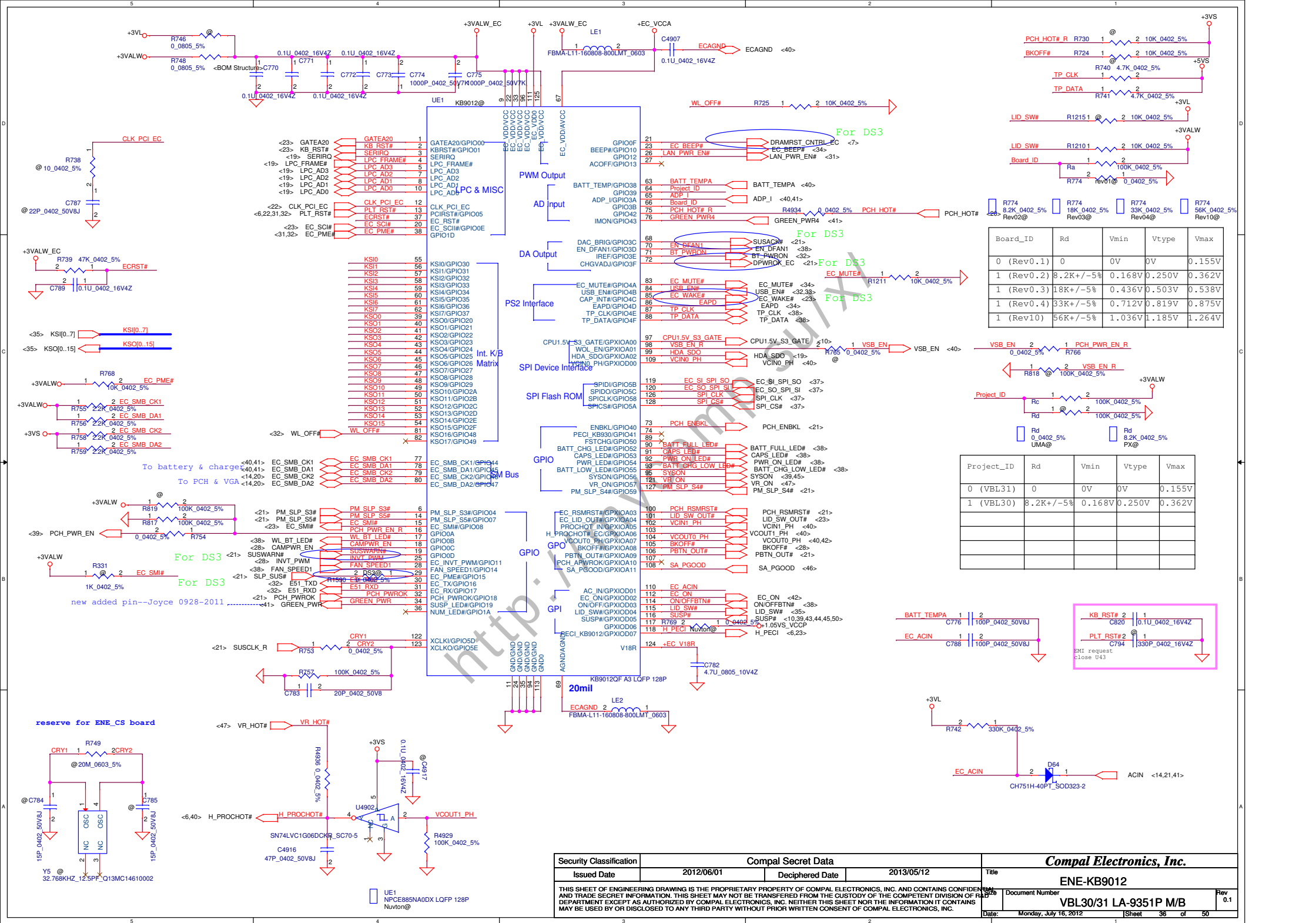
VGA



PCB Fedical Mark PAD



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				Date: Monday, July 16, 2012	Sheet 35 of 50



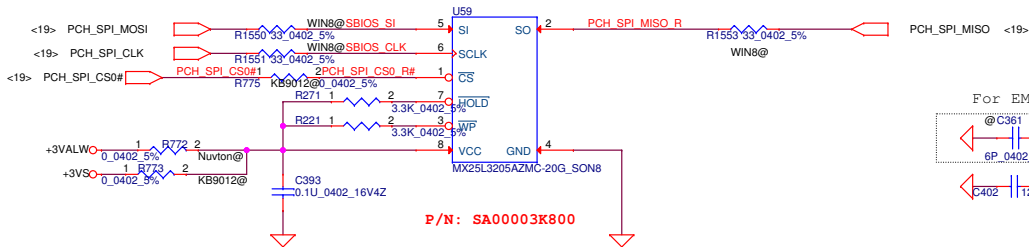
BIOS Bus switch

<36> EC_SI SPI_SO R266 1 Nuvton@233 0402 5% PCH_SPI_MISO_R
 <36> EC_SO SPI_SI R267 1 Nuvton@233 0402 5% SBIOS_SI
 <36> SPI_CLK R268 1 Nuvton@233 0402 5% SBIOS_CLK
 <36> SPI_CS# R270 1 Nuvton@233 0402 5% PCH_SPI_CS0_R#

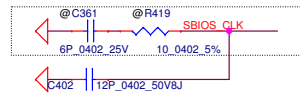
R1550 0.0402 5% R1551 0.0402 5% R1553 0.0402 5%
 NOW8@ NOW8@ NOW8@

When use single ROM, R1550 R1551 R1553 use 0 ohm.

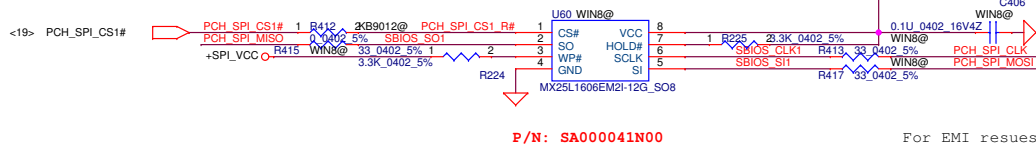
BIOS SPI Flash (4MByte*1)



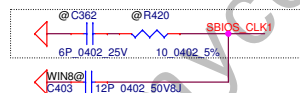
For EMI resuest.



BIOS SPI Flash (2MByte*1) For Win8

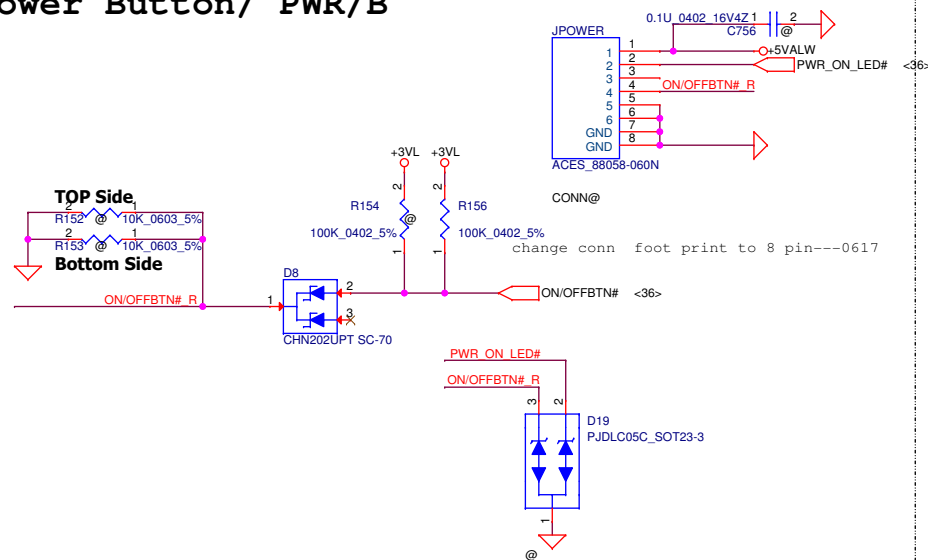


For EMI resuest.

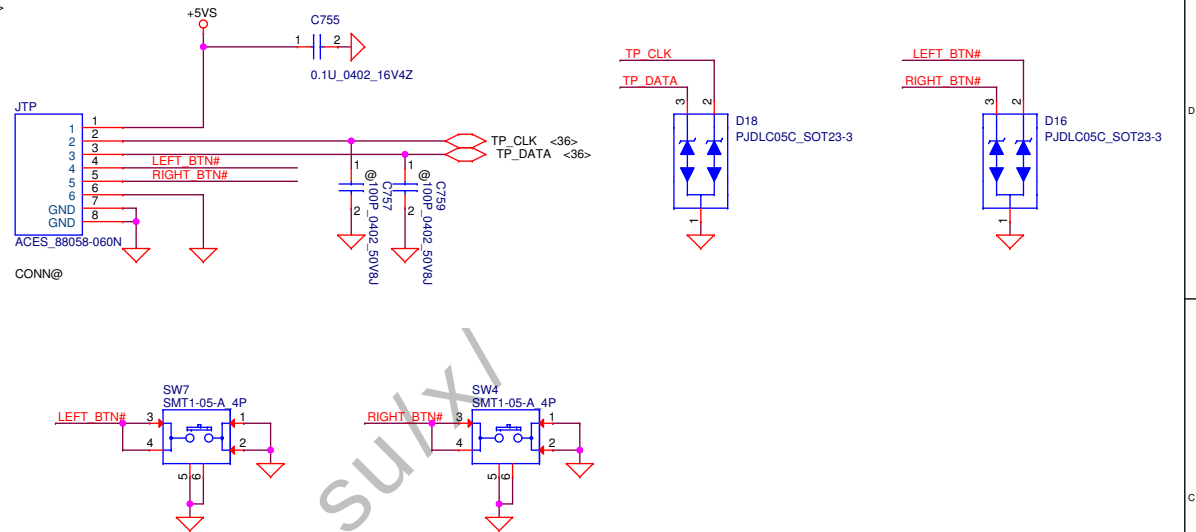


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Issued Date				2012/06/01				Deciphered Date			
2012/06/01				2013/05/12				Title			
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Date: Monday, July 16, 2012				VBL30/31 LA-9351P M/B				Rev			
1				37				0.1			

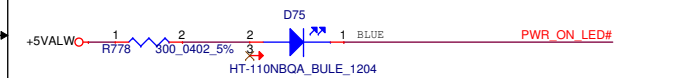
Power Button/ PWR/B



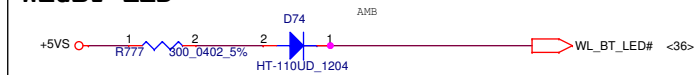
Touch/B Connector



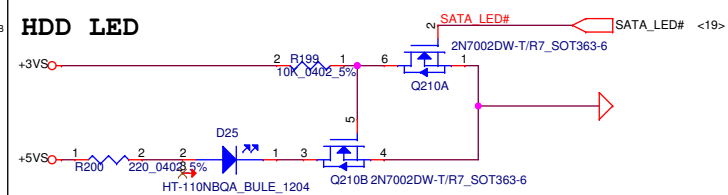
DC-IN LED



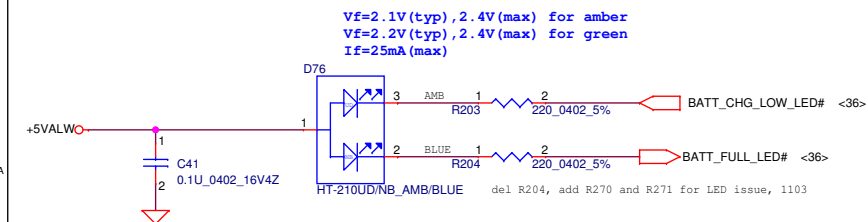
WL&BT LED



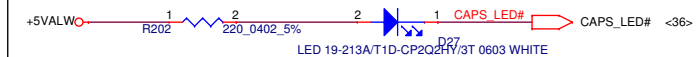
HDD LED



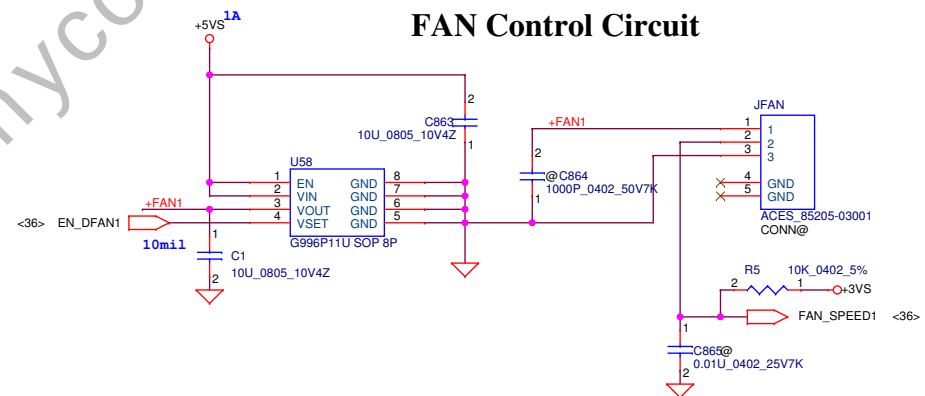
BATT CHARGE/FULL LED



CAP LOCK LED



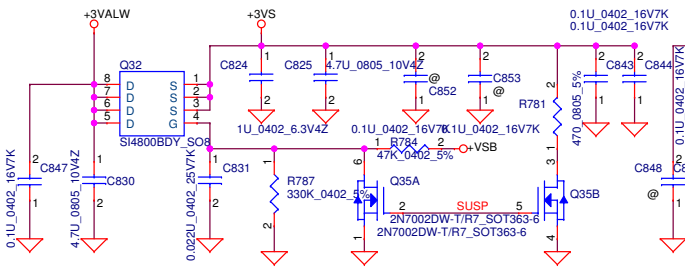
FAN Control Circuit



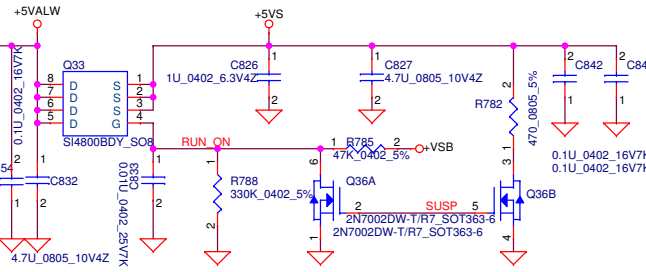
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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	PWR/TP/LED/FAN	
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				Date:	Monday, July 16, 2012	Sheet 38 of 50

+3VALW TO +3VS

Vgs=-0V, Id=9A, Rds=18.5mohm

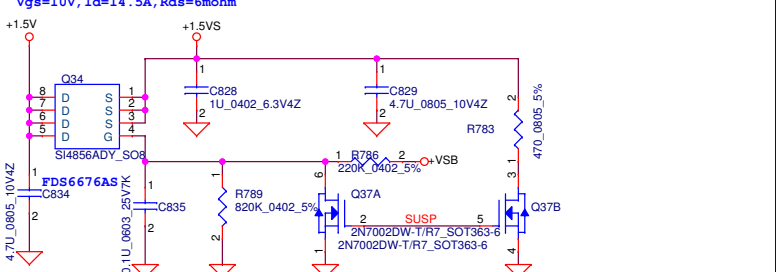


+5VALW TO +5VS

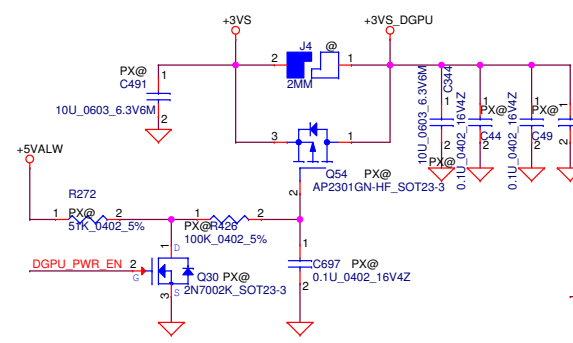


+1.5V to +1.5VS

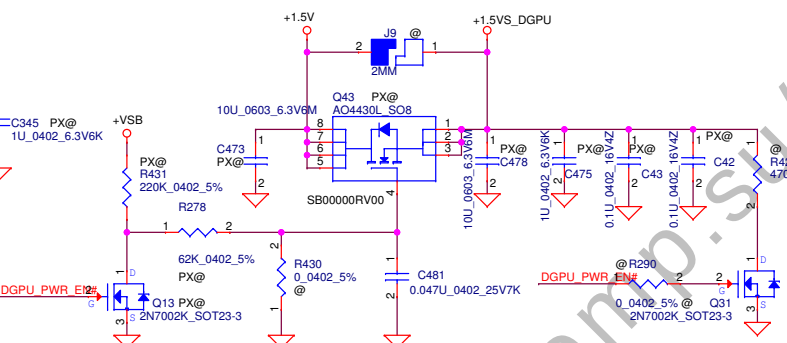
Vgs=10V, Id=14.5A, Rds=6mohm



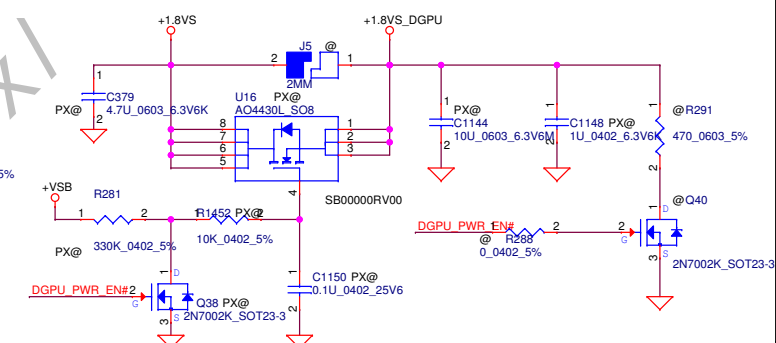
+3VS TO +3VS_DGPU

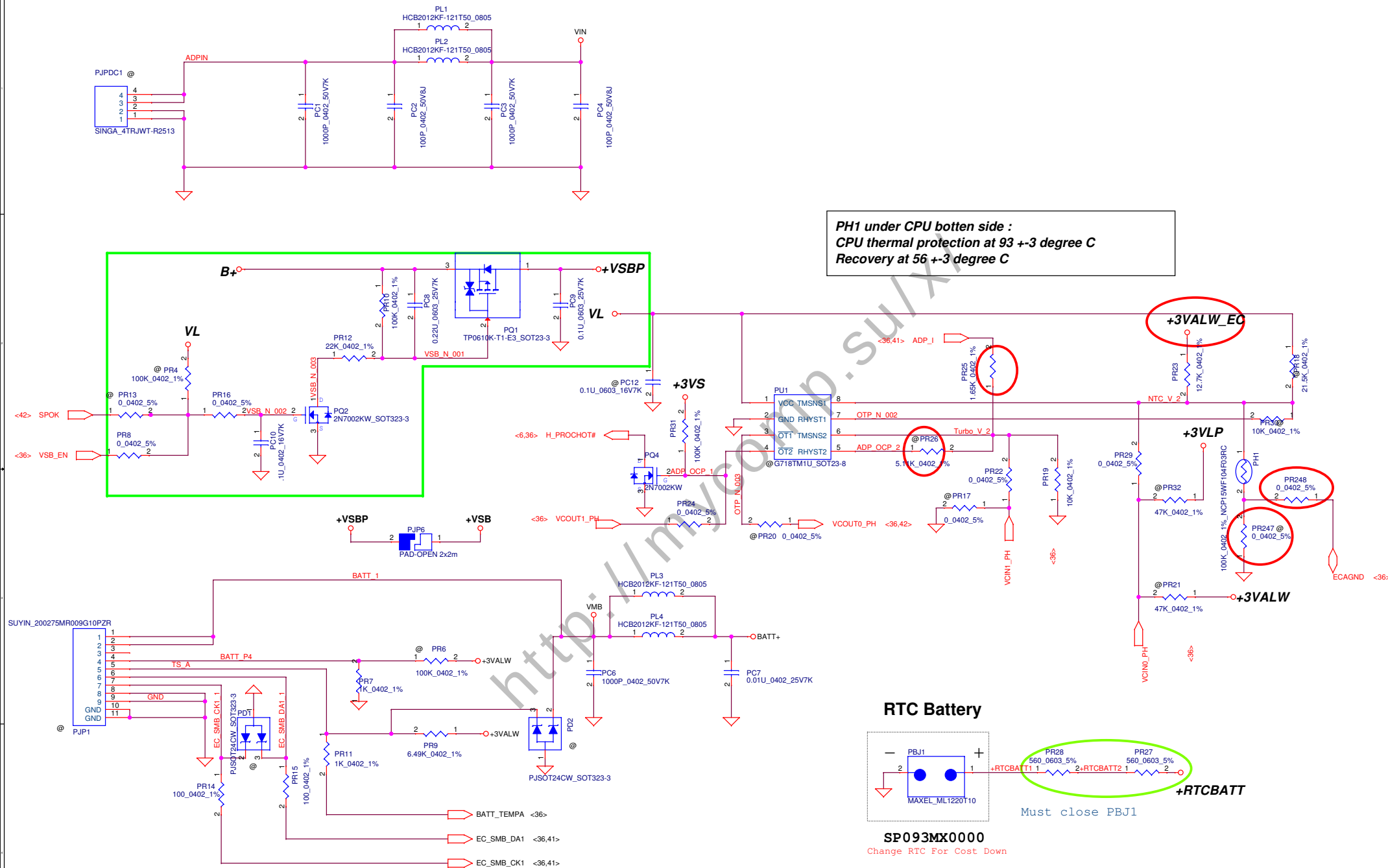


+1.5V TO +1.5VS_DGPU

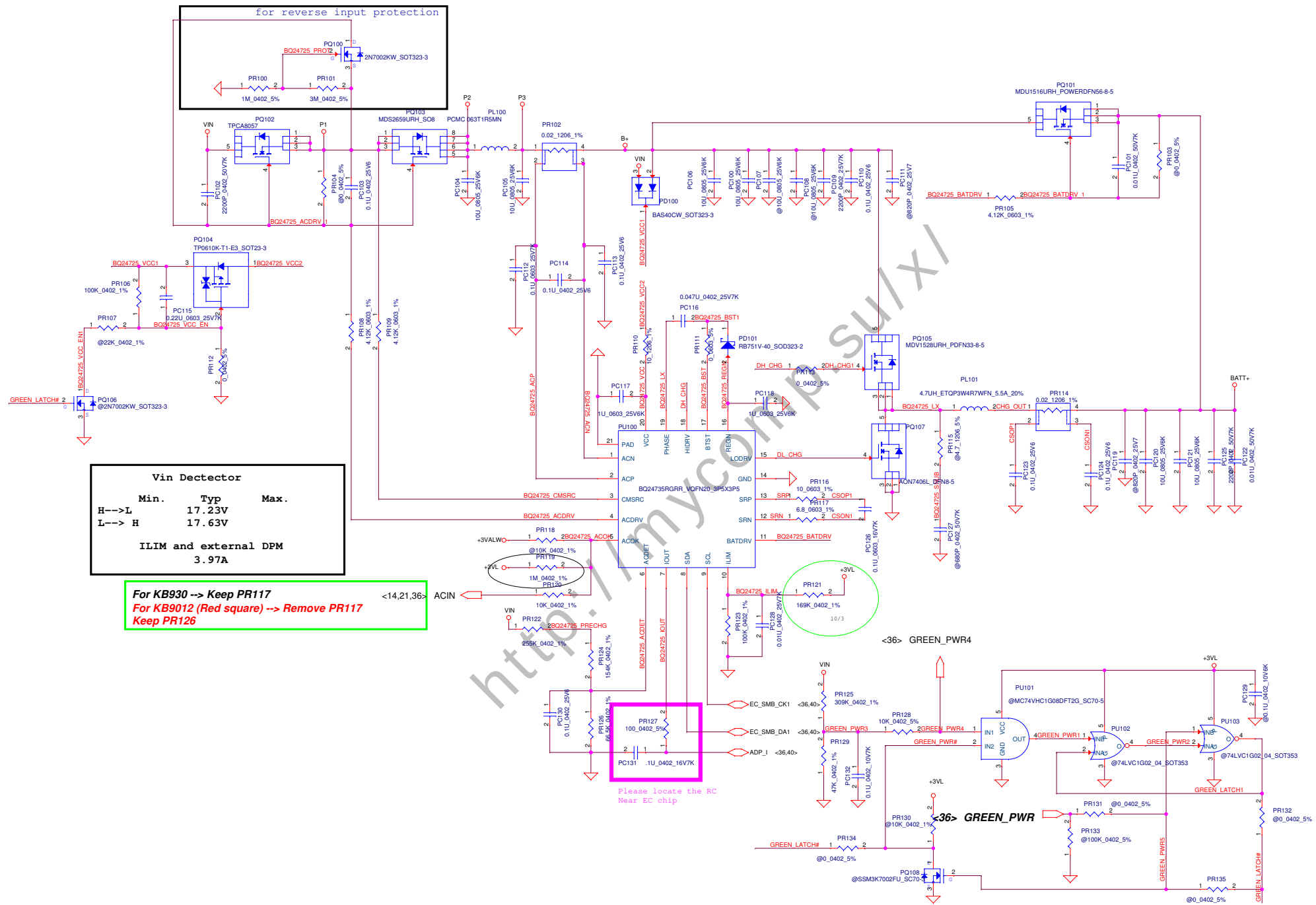


+1.8VS TO +1.8VS_DGPU

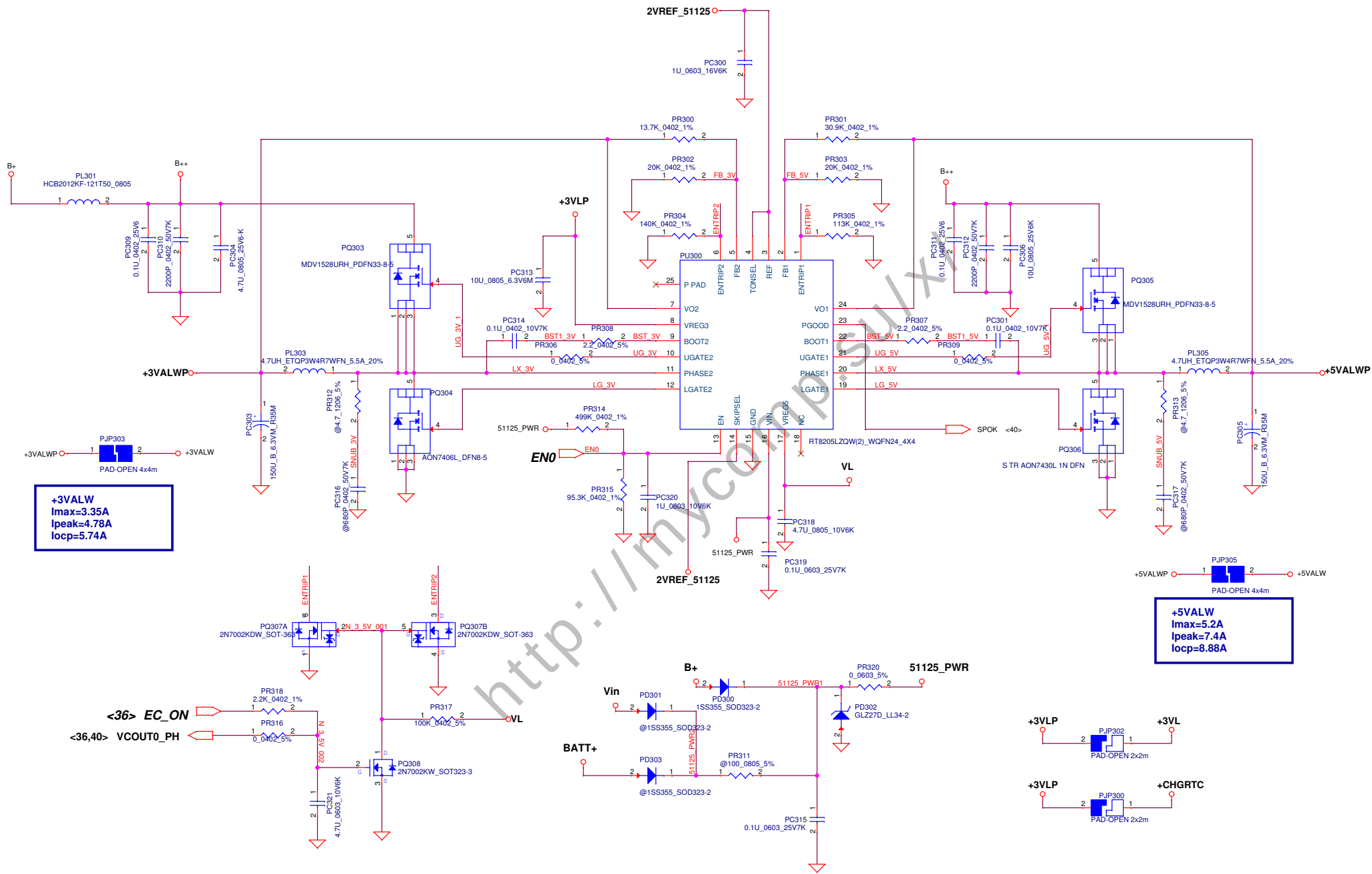




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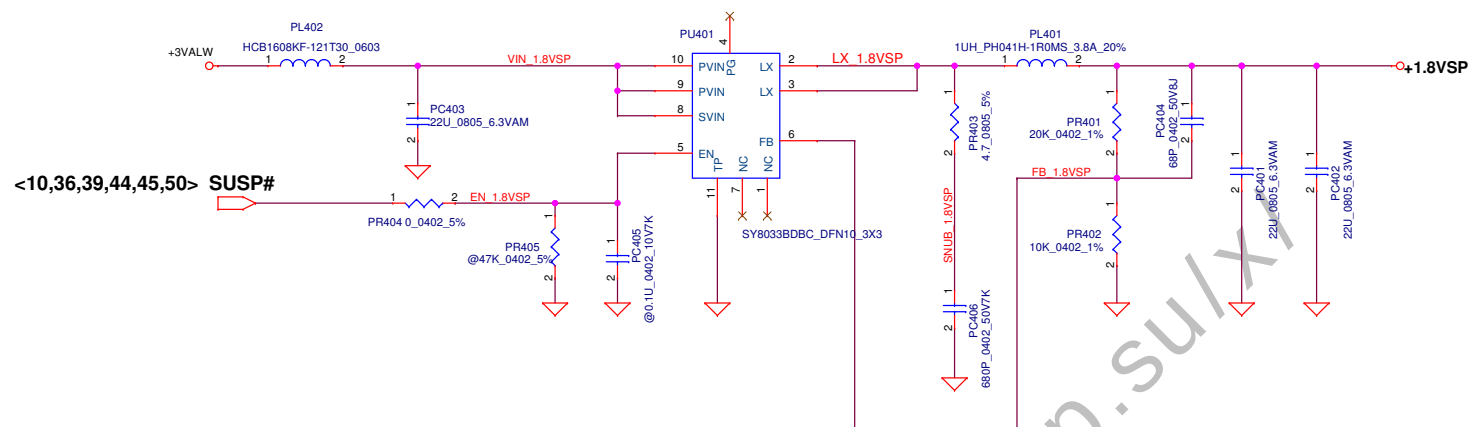


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						Date:	Monday, July 16, 2012	Sheet 42 of 50

Compal Electronics, Inc.

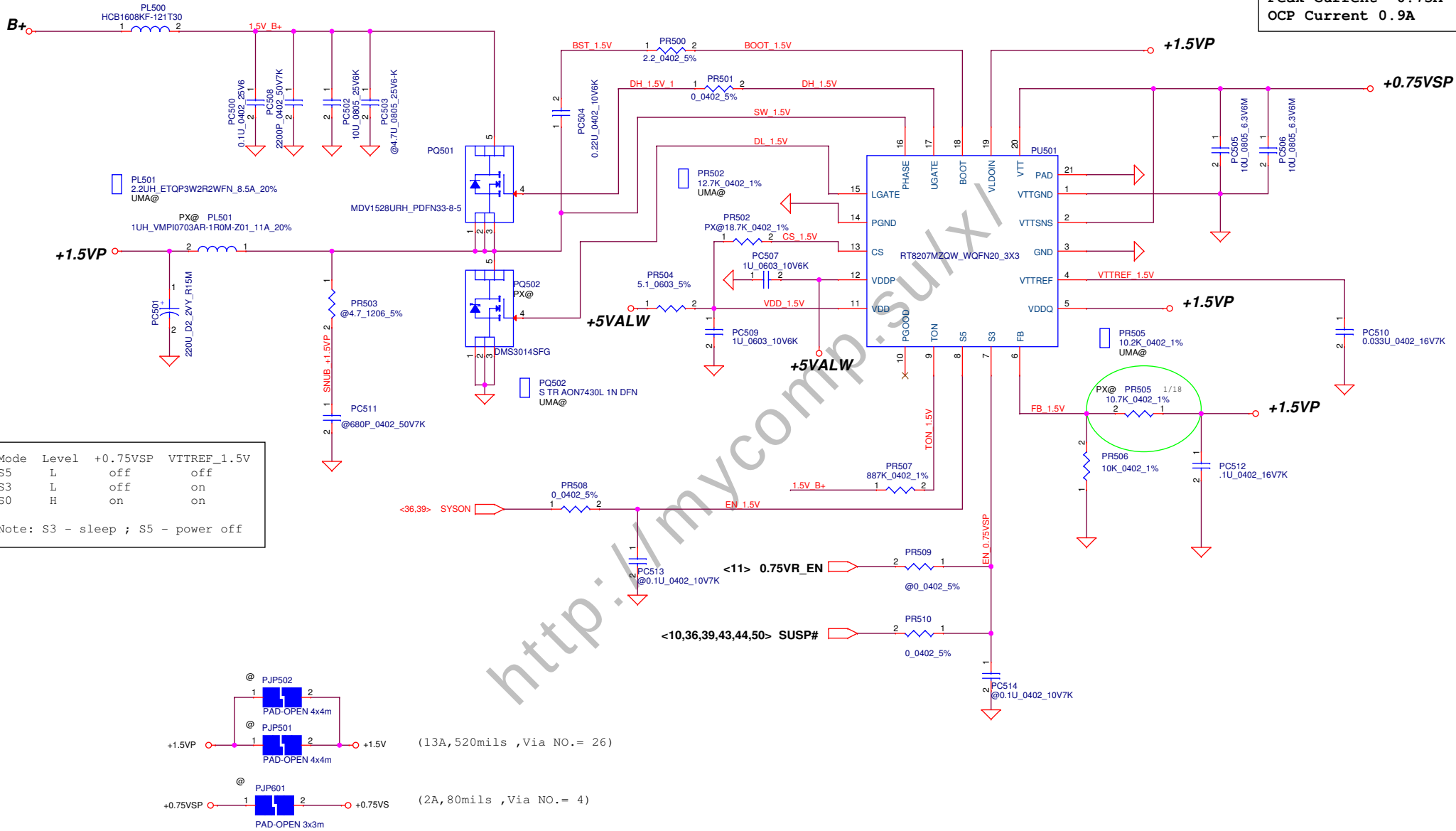
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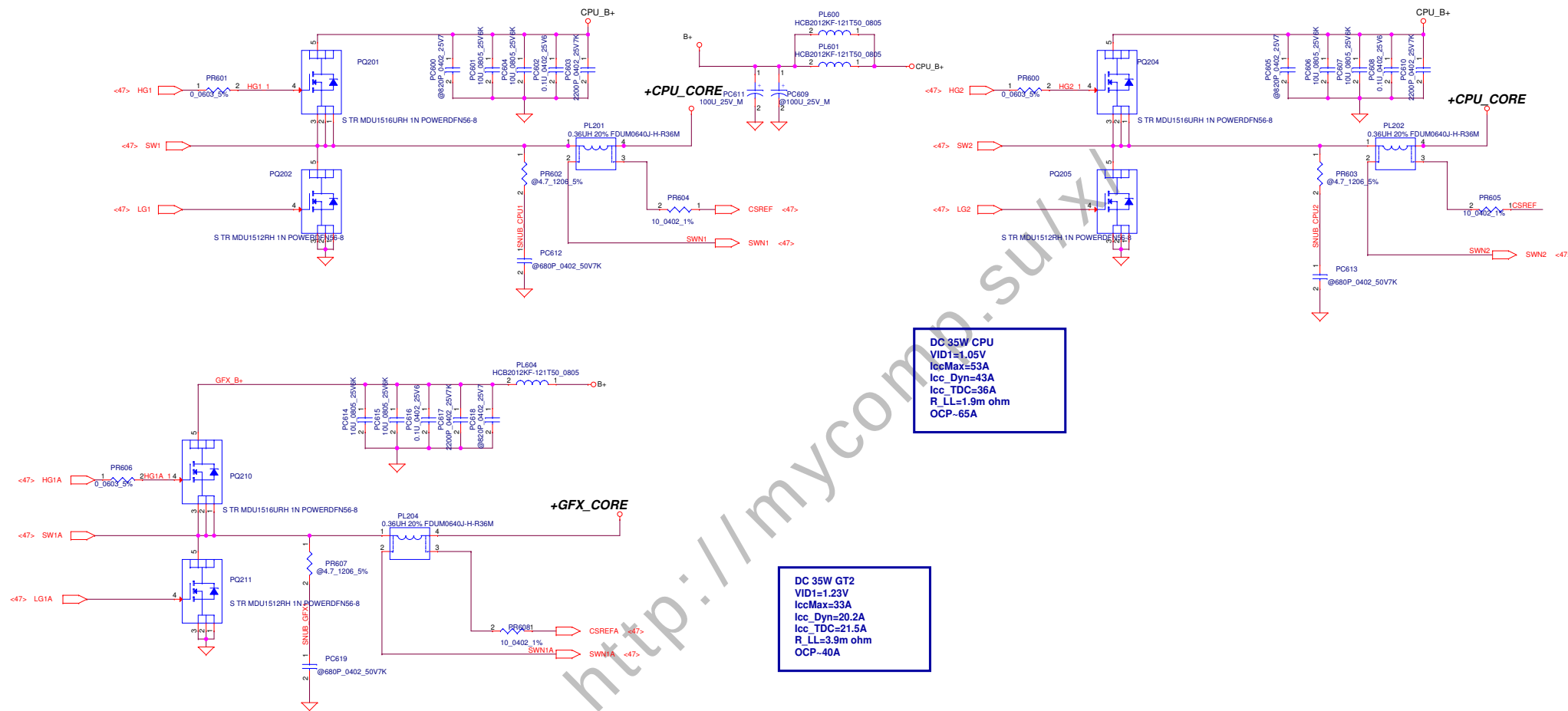
VBL30/31



+1.8VSP 1 PJP401 2 +1.8VS
 PAD-OPEN 3x3mm
 (3.5A, 140mils, Via NO.= 7)

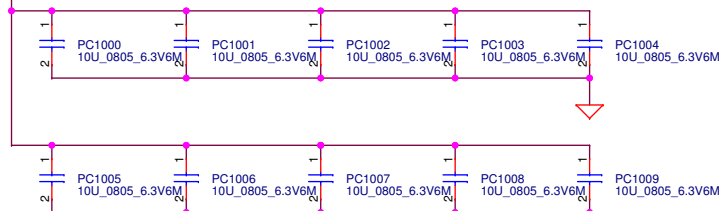
+1.8V
 I_{max}=2.25A
 I_{peak}=3.22A



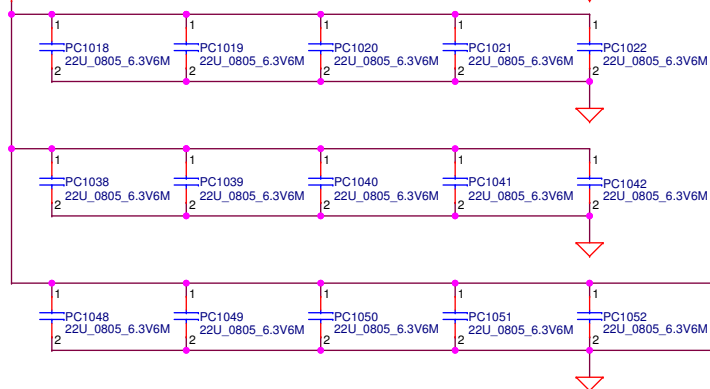


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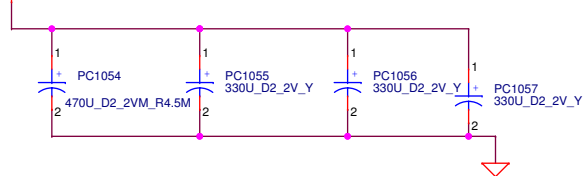
+CPU_CORE



+CPU_CORE



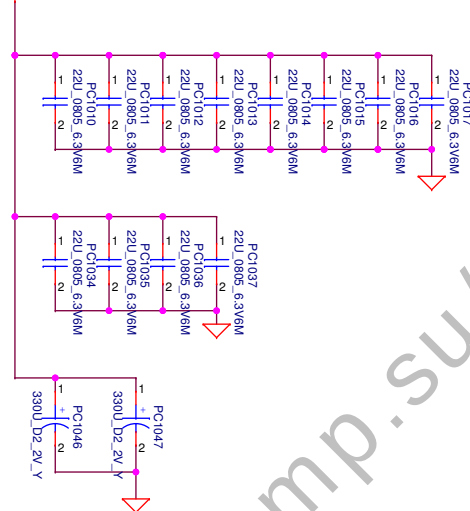
+CPU_CORE



+CPU_CORE

+GFX_CORE

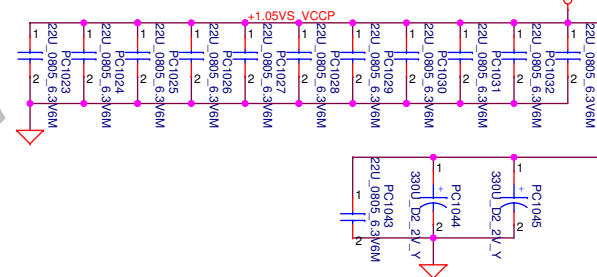
+GFX_CORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805)
	5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805)
	2 x (0805) no-stuff sites

+1.05VS_VCCP



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										PWR - PROCESSOR DECOUPLING	
										Document Number	
										VBL30/31	
										Date	
										Monday, July 16, 2012	
										Sheet 49 of 50	
										Rev 0.1	

connect PR924 pin1 to VGA chip

connect PR925 GND to VGA chip

