

LAGUNA

REV : X03

@ : Depop Component

PRELIMINARY

LA-2112 (8 Layer M/B for LAGUNA)

Dothan Schematic with Capture CIS and Function field

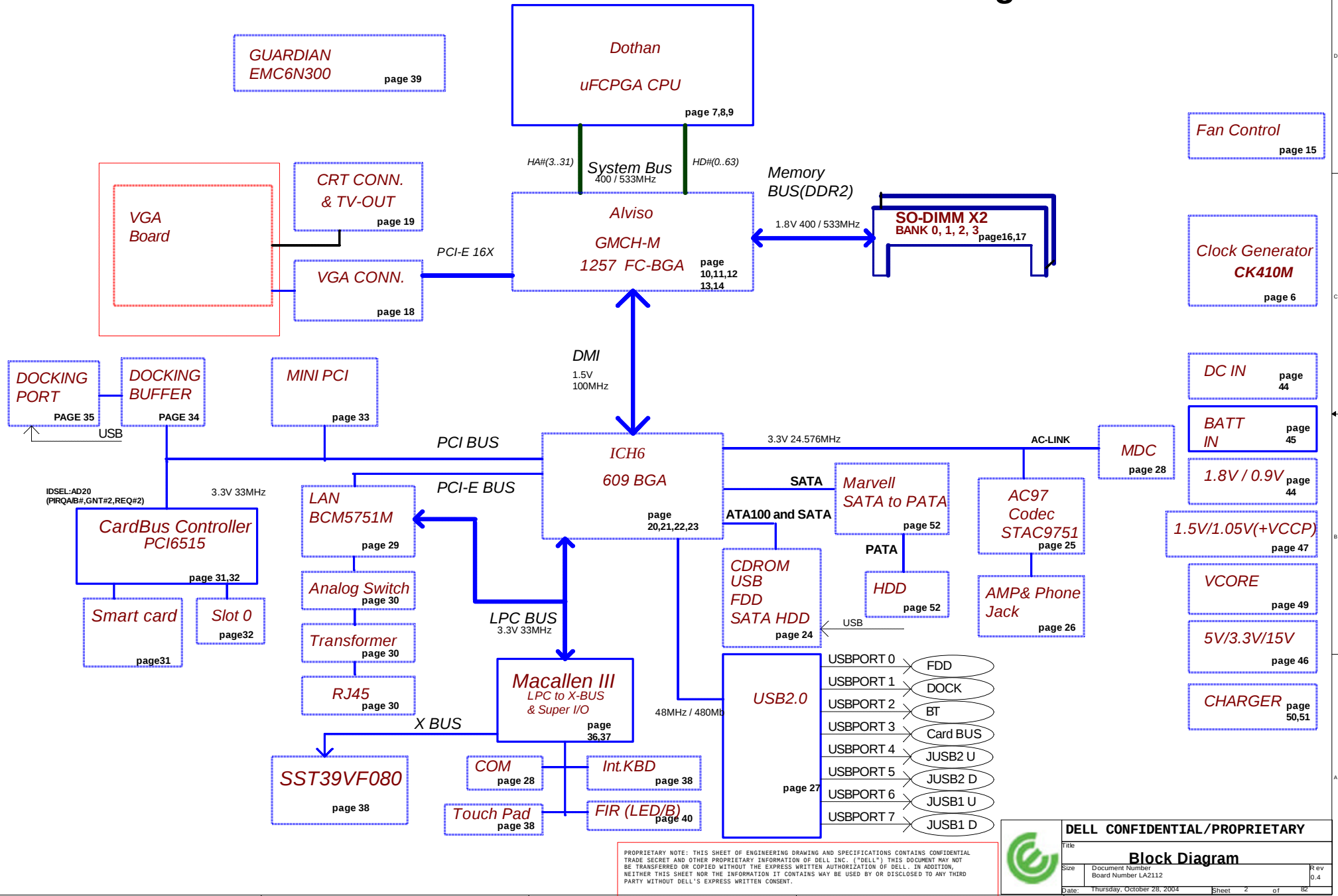
uFCPGA Dothan
10-07-2004
REV: 0.4

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Block Diagram



PM TABLE

State \ power plane	+3VALW +5VALW +RTC_CELL +3.3VX	+3VSUS +5VSUS +1.8VSUS +1.5VSUS +15V	+5VRUN +3VRUN +0.9V_DDR_VTT +2.5VRUN +1.8VRUN +1.5VRUN +VCC_CORE +VCCP
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	D,C
DOCK	AD24	0	A
MINI PCI	AD19	3	D,B

USB TABLE

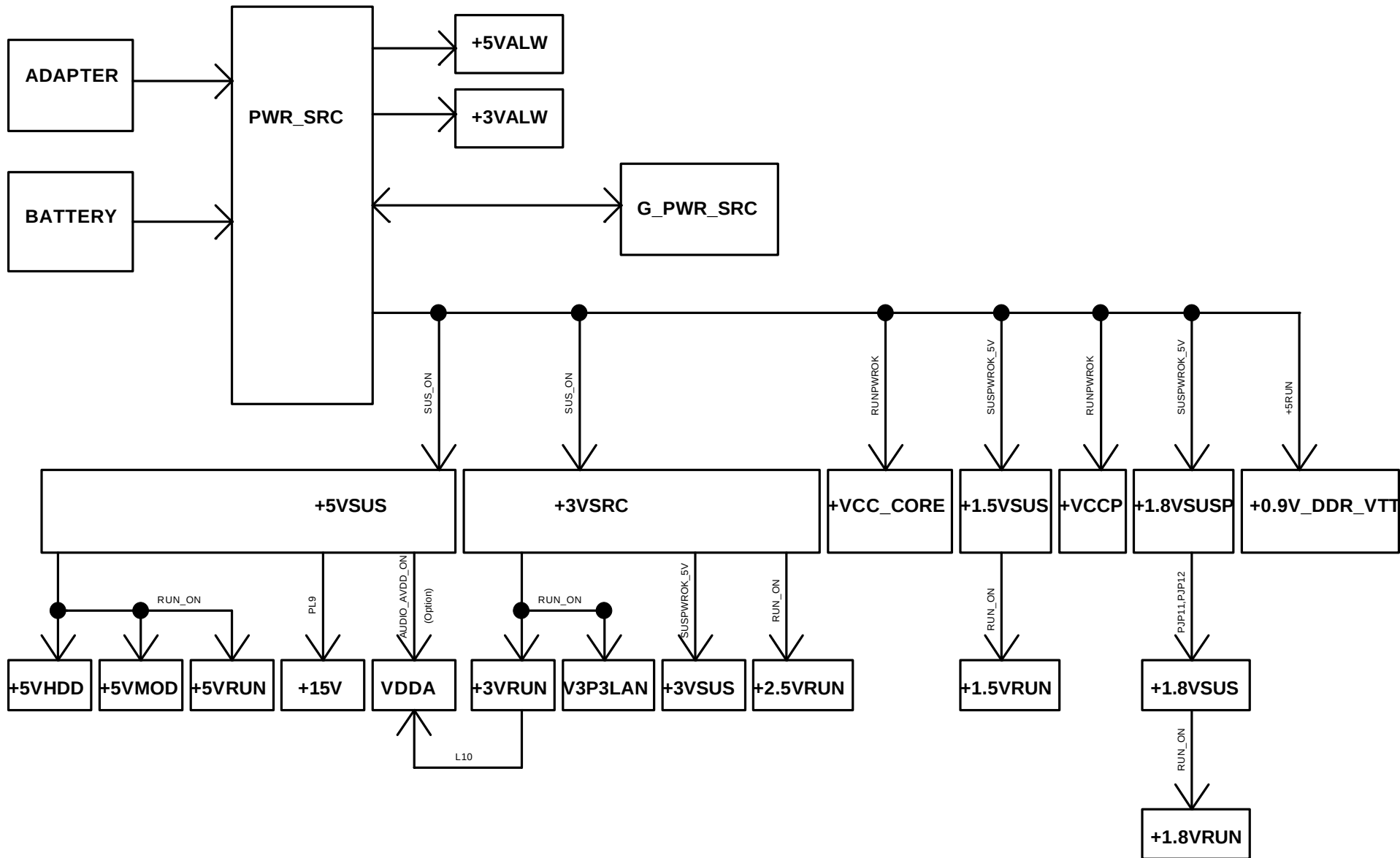
USB PORT#	DESTINATION
0	FDD (module bay)
1	DOCK
2	MPCI (BlueTooth)
3	NEW Connector
4	USB Port 2(Top)
5	USB Port 2(Bottom)
6	USB Port 1(Top)
7	USB Port 1(Bottom)

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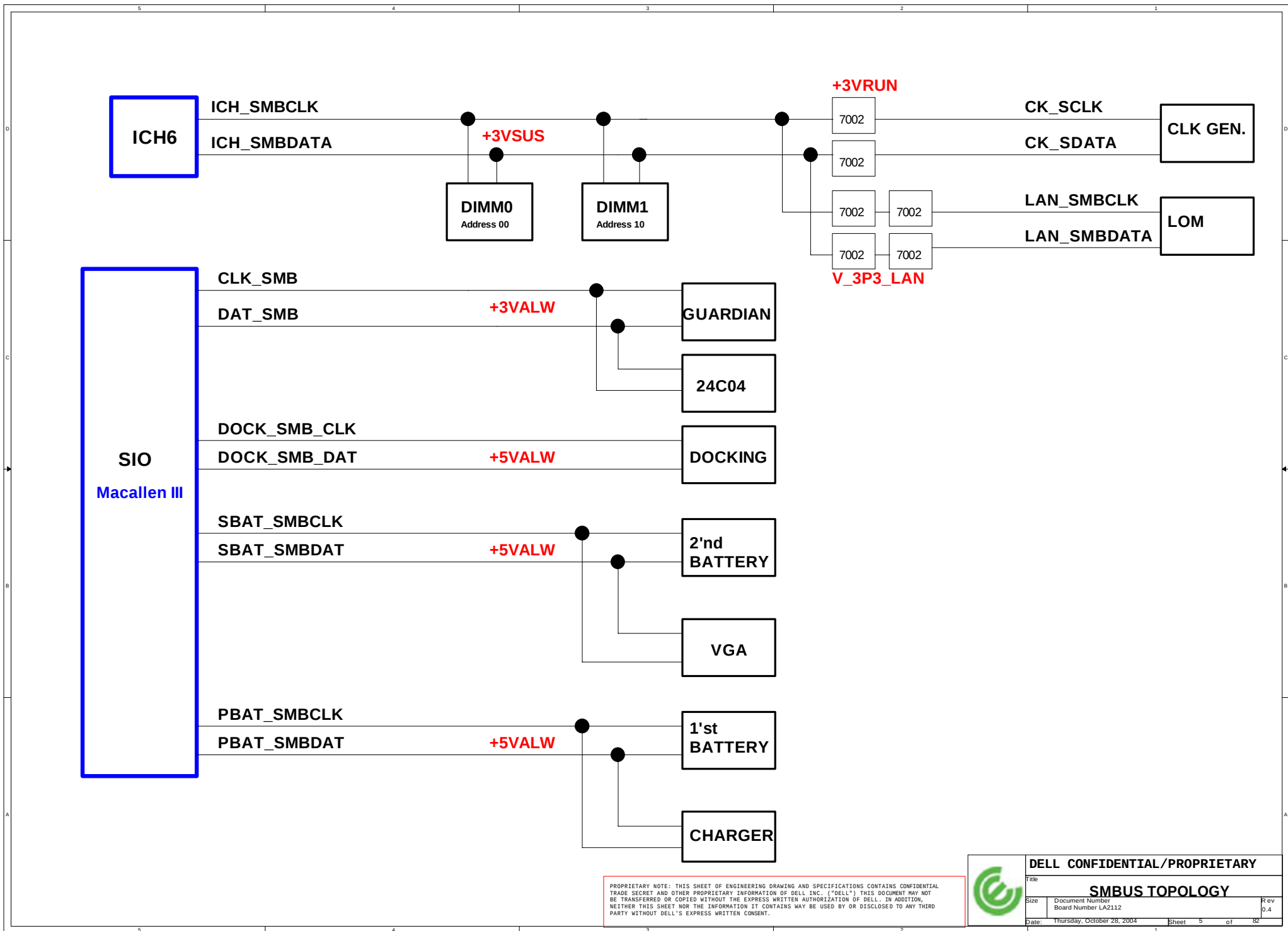
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Title Index and Config.		
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Title: Power Rail			
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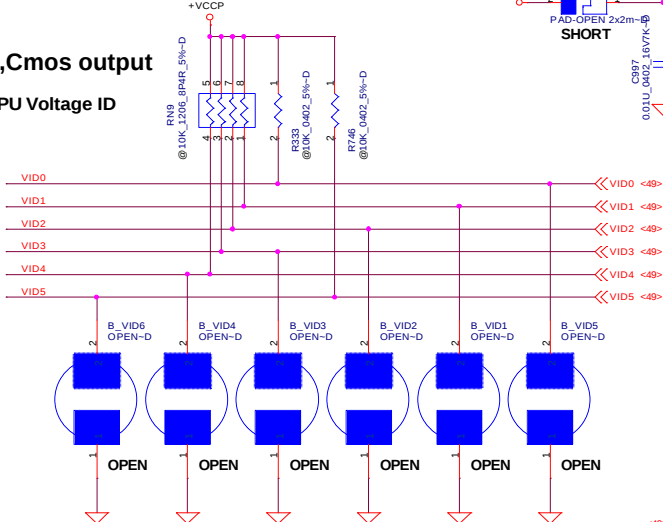


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Title		SMBUS TOPOLOGY	
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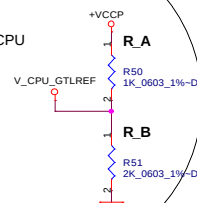
Dothan-A2 w/ 533Mhz supports both 1.5V and 1.8V.
Dothan-B step w/533Mhz supports only 1.5V

For test only ,Cmos output

CPU Voltage ID



Layout close CPU



Resistor placed within 0.5" of CPU pin. Trace should be at least 25 miles away from any other toggling signal.

Dothan

POWER, GROUND, RESERVED SIGNALS AND NC

Dothan

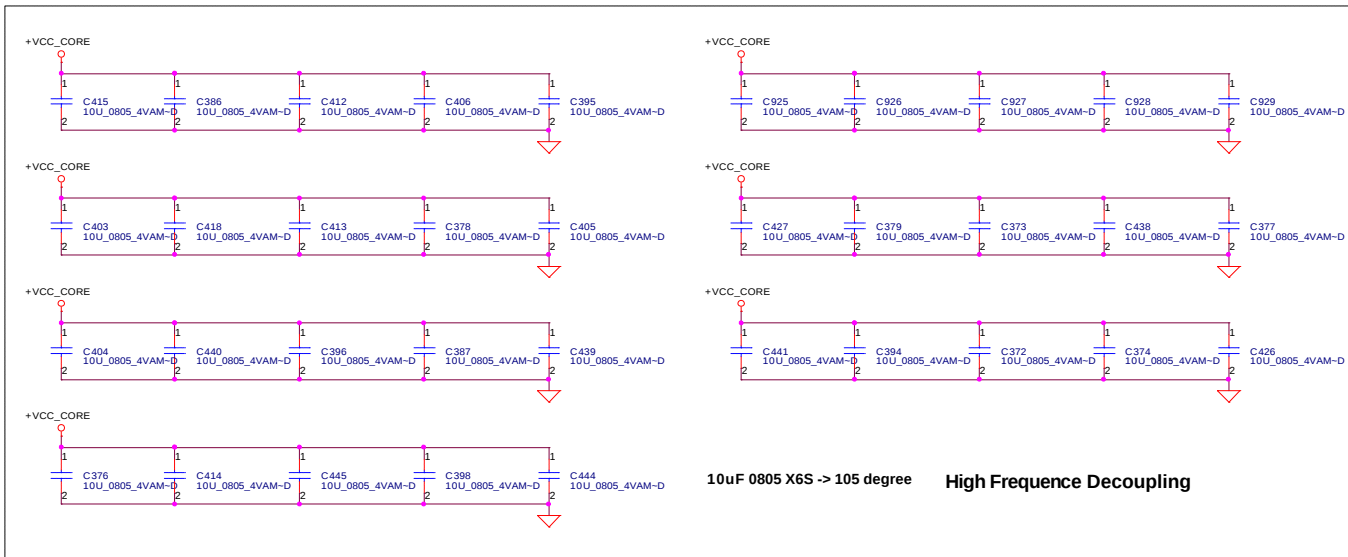
POWER, GROUND

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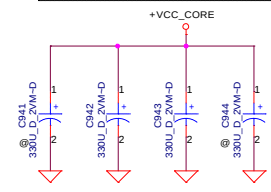
Dothan Processor in mFCPGA479

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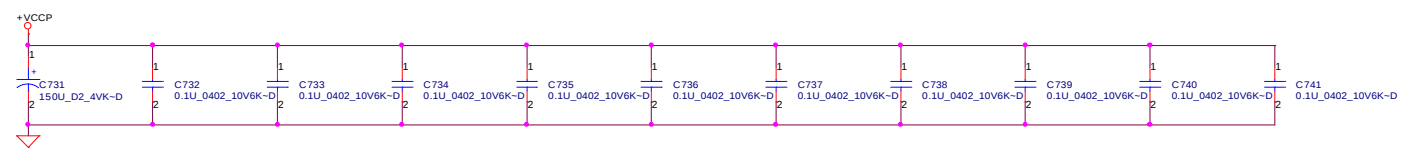


Near VCORE regulator.

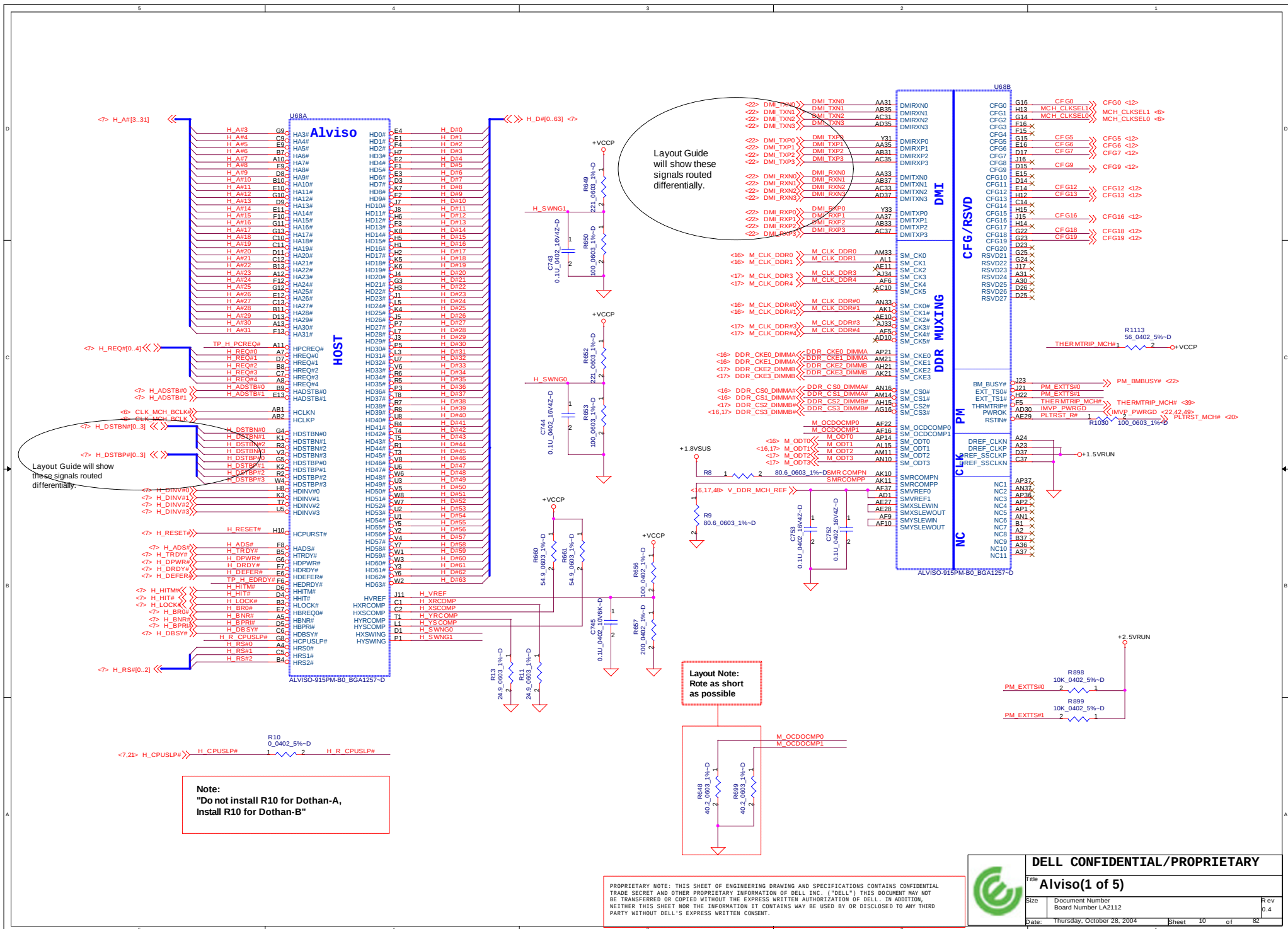


ESR <= 3m ohm
Capacitor > 880uF

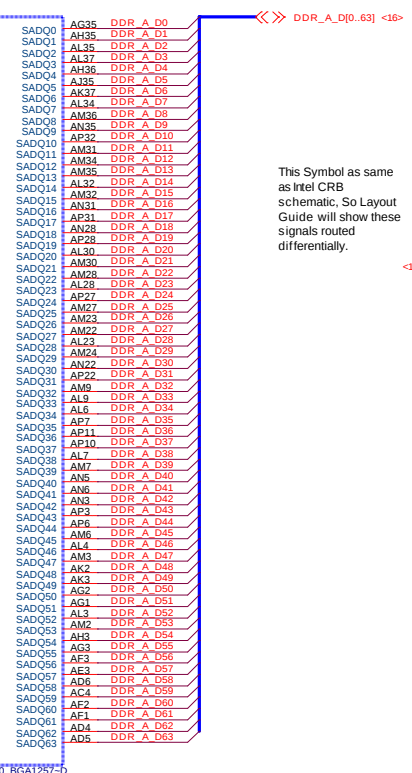
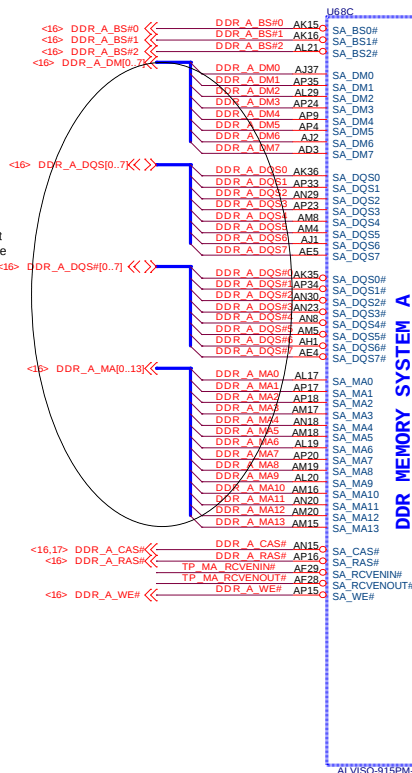
9mOhm 9mOhm 9mOhm
7343 7343 7343
PS CAP PS CAP PS CAP



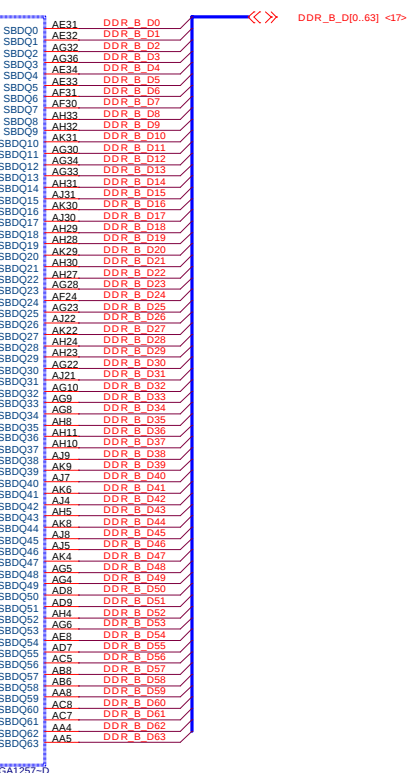
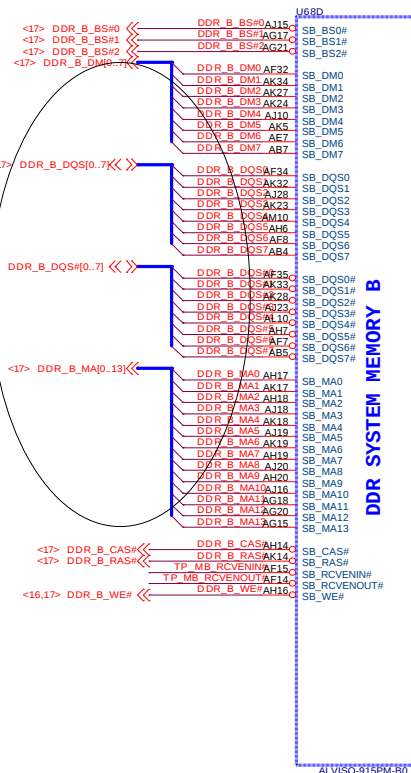
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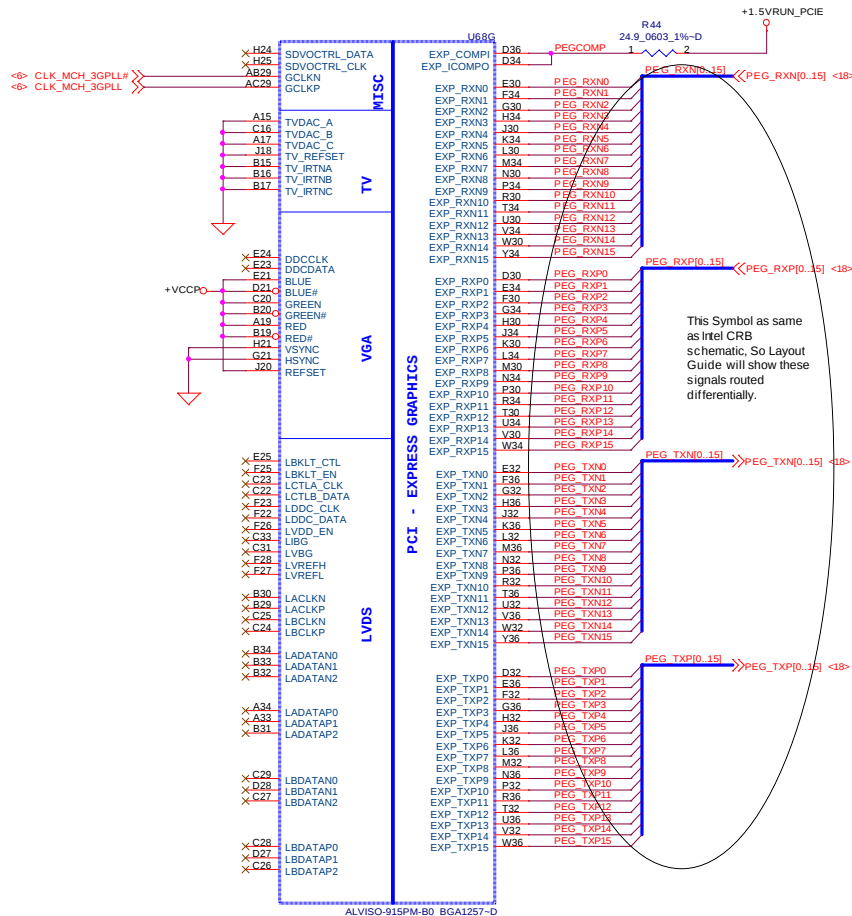


This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.

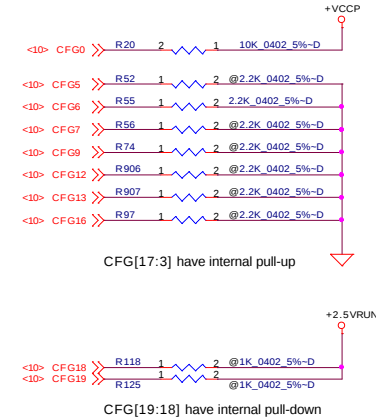


This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.





CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V



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POWER

W=20 mils

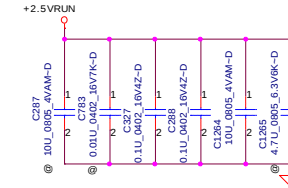
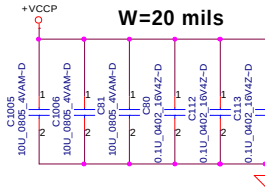
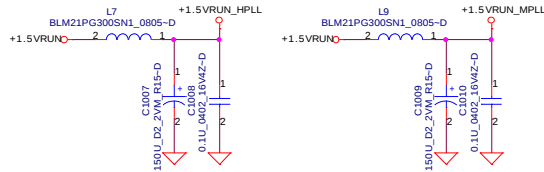
POWER

Note : All VCCSM pin shorted internally.

+1.5VVRUN
Close B26,B25,A25
C1266
@10U_0805_4VAM-D

Route VSSA3GBG gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

Remove L6, C48, C51, Connect DPLL2 directly to +1.5vrun
Remove L29, C47, C8, Connect DPLLA directly to +1.5vrun
Steven-01/09/2004



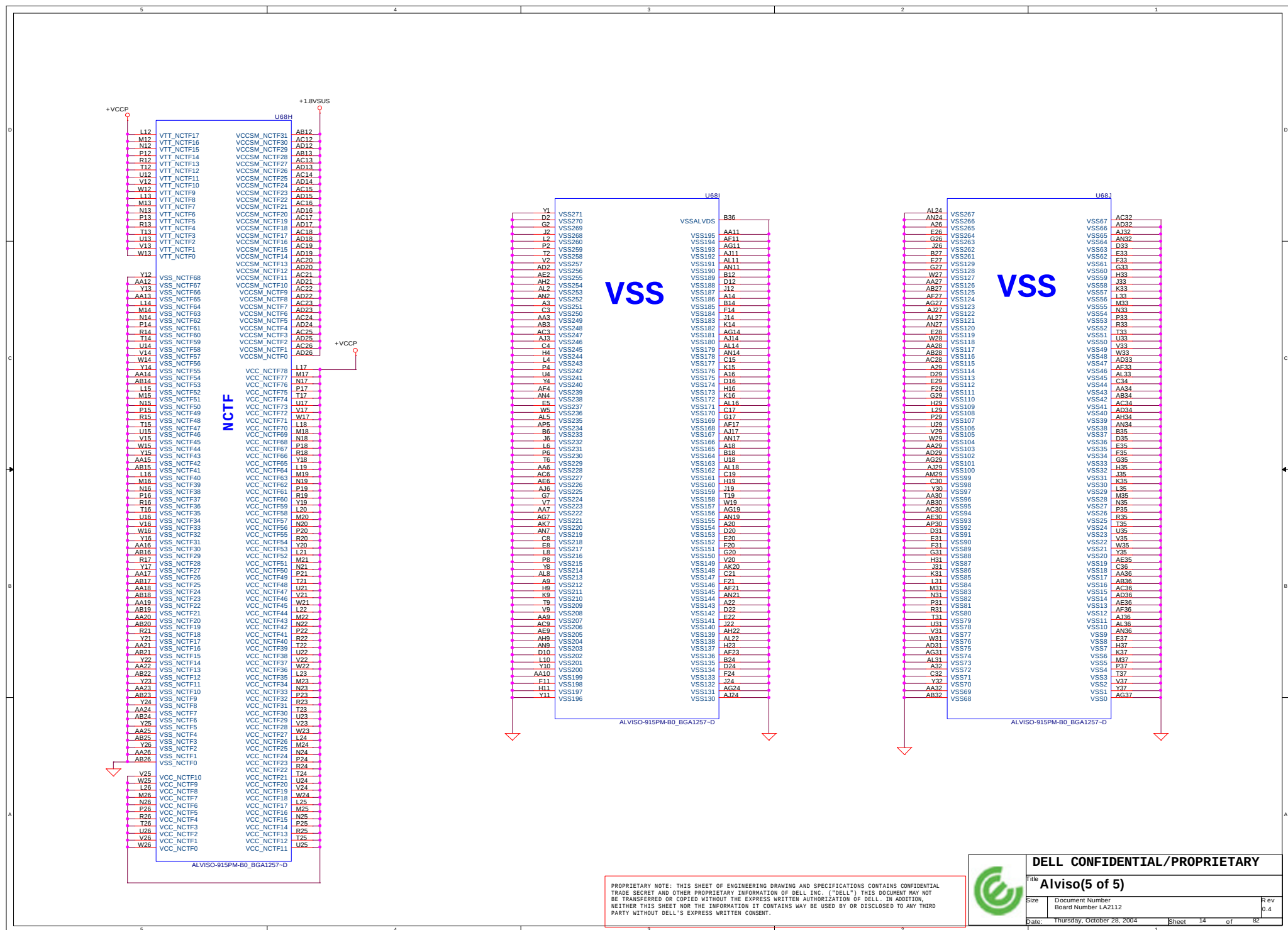
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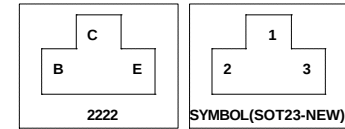
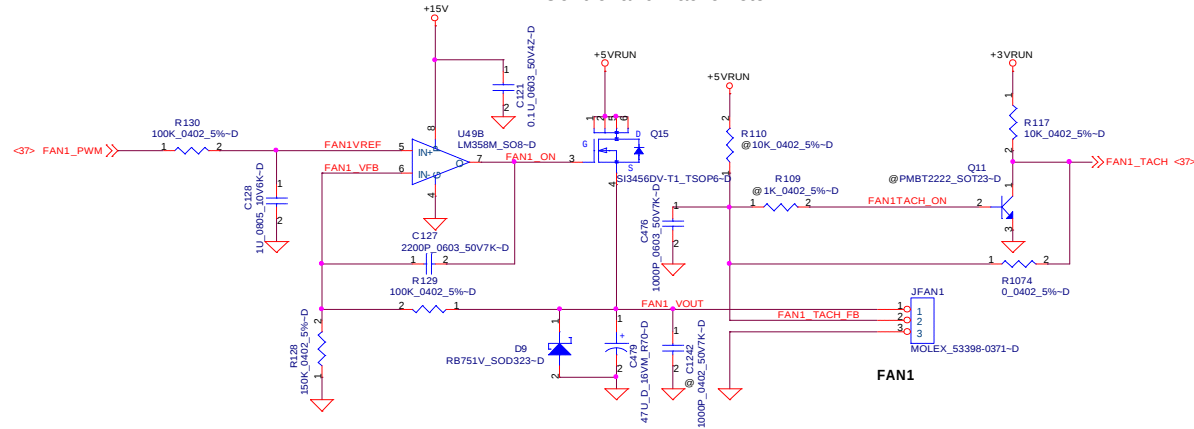
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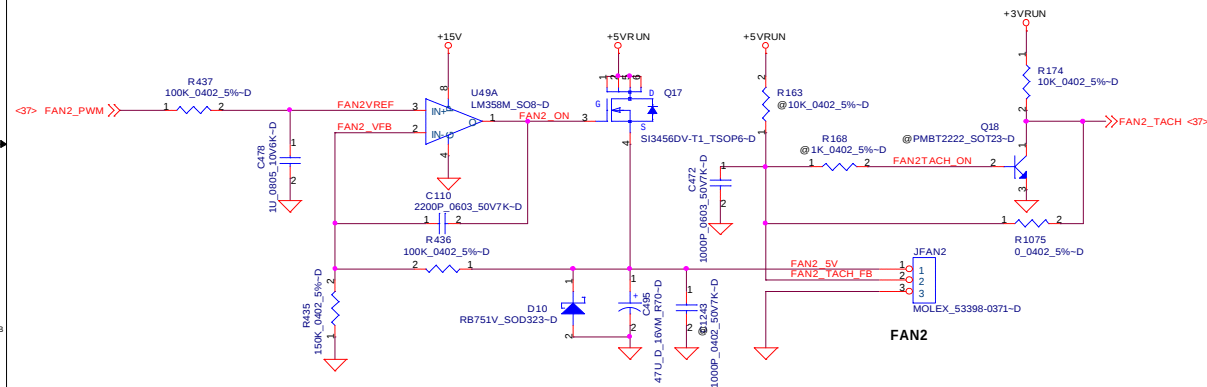
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FAN1 Control and Tachometer

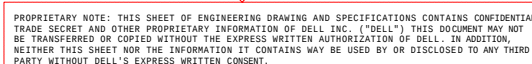


FAN2 Control and Tachometer



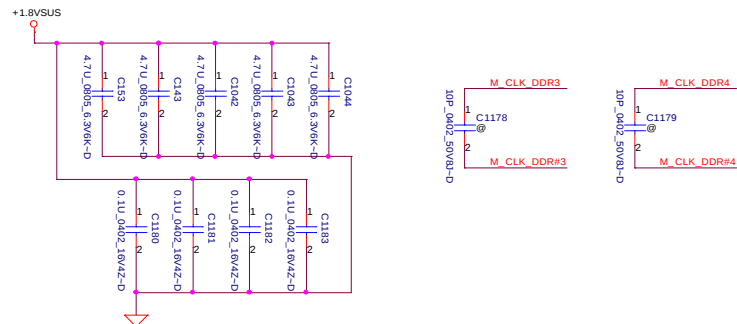
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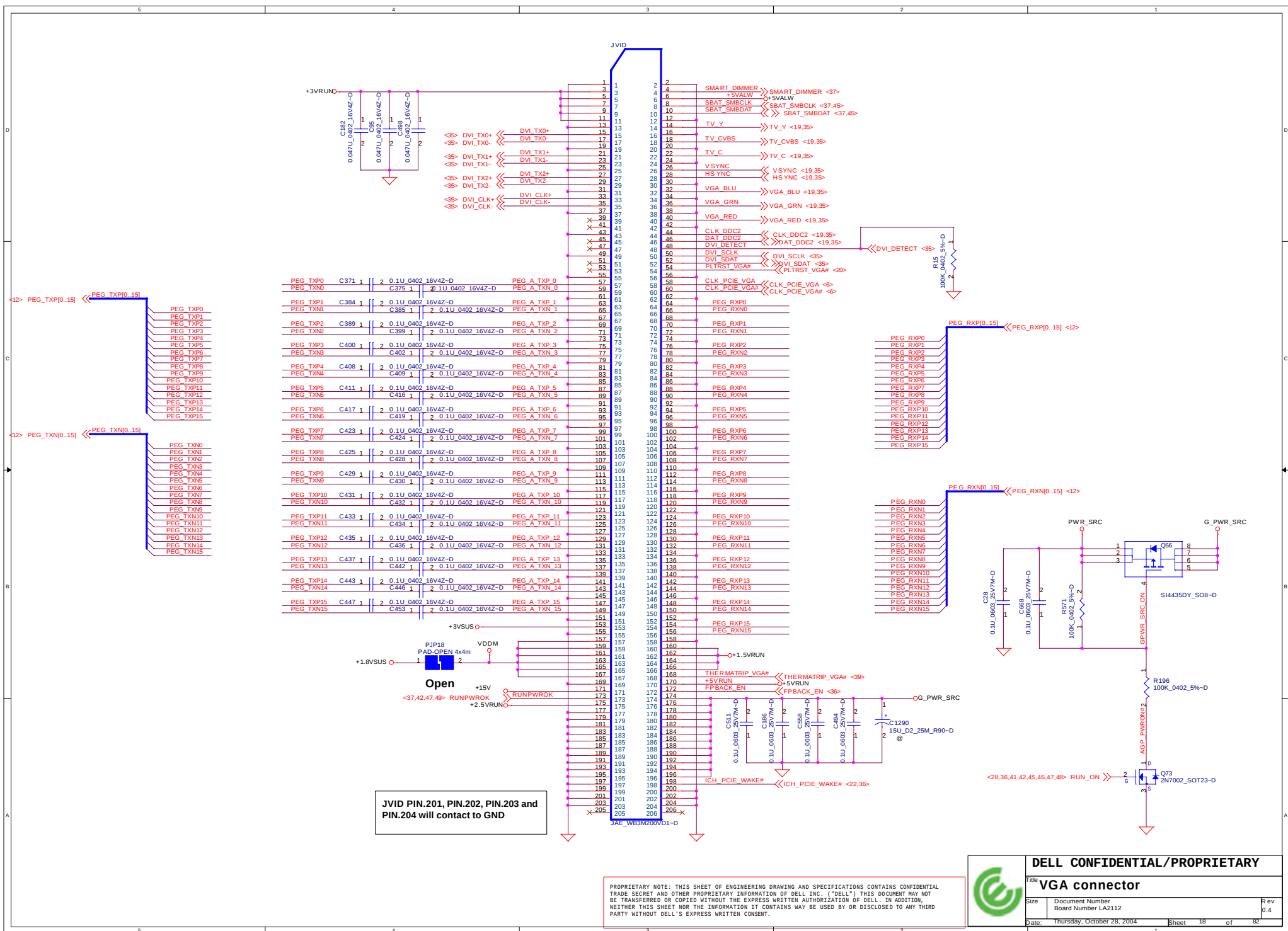
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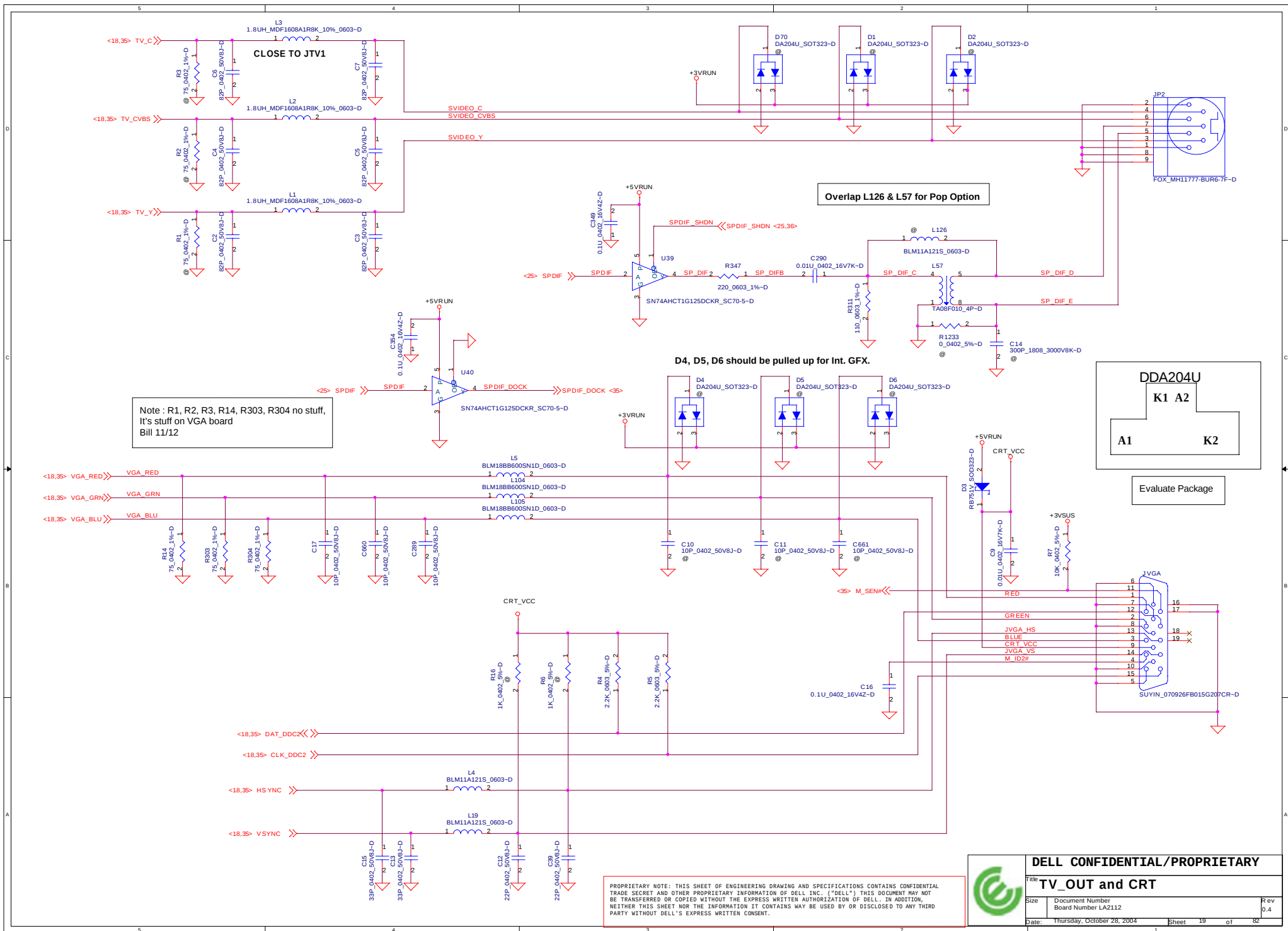


<11> DDR_B_DQS#0..7 <<>>
 <11> DDR_B_D0..63 <<>>
 <11> DDR_B_DM0..7 <<>>
 <11> DDR_B_DQS#0..7 <<>>
 <11> DDR_B_MA0..13 <<>>

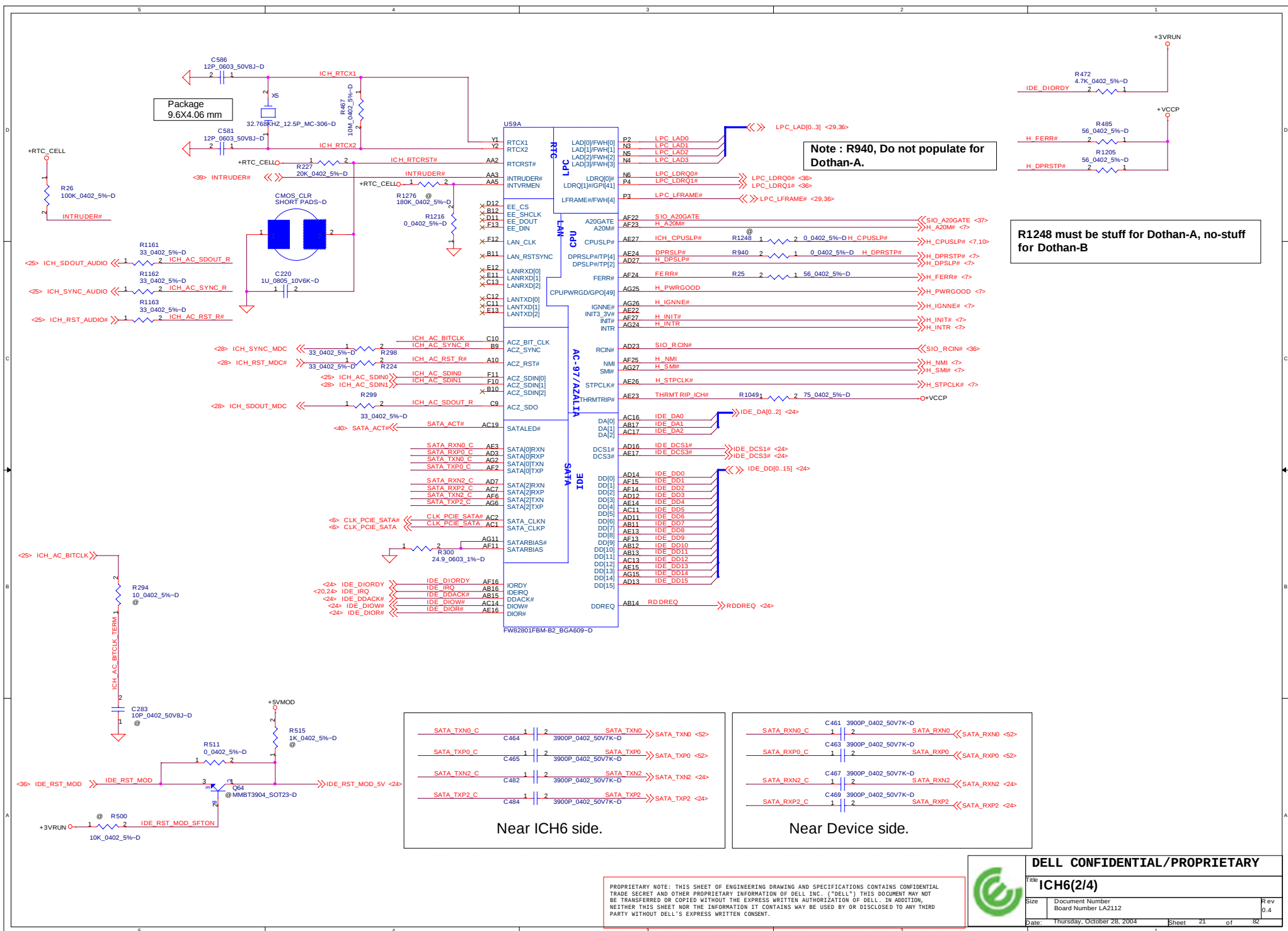
Layout Note:
Place near JDIM2

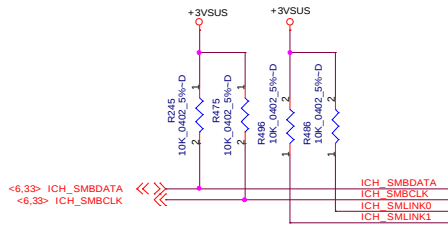




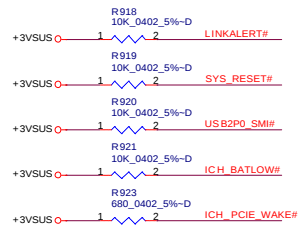
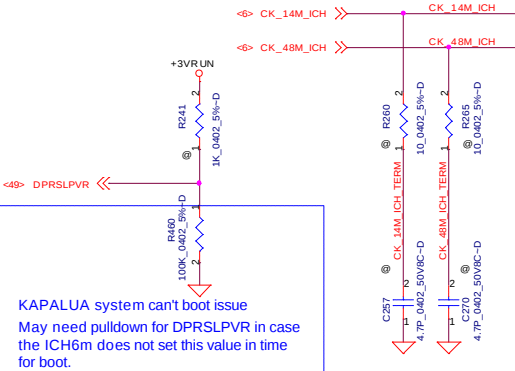
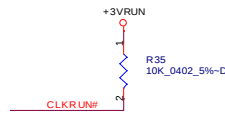


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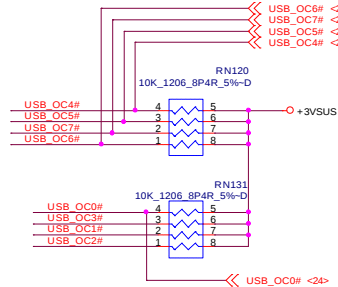
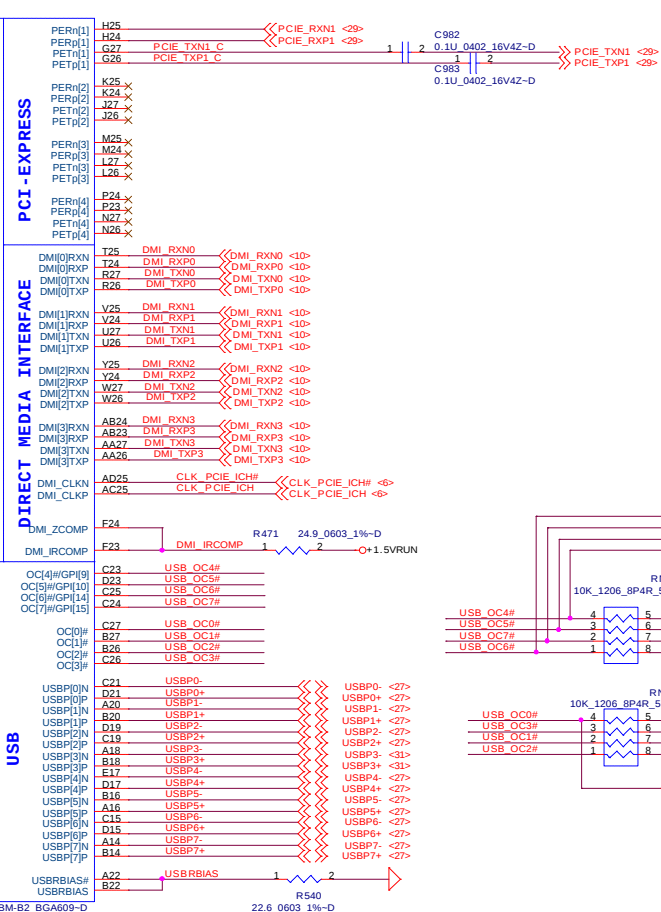
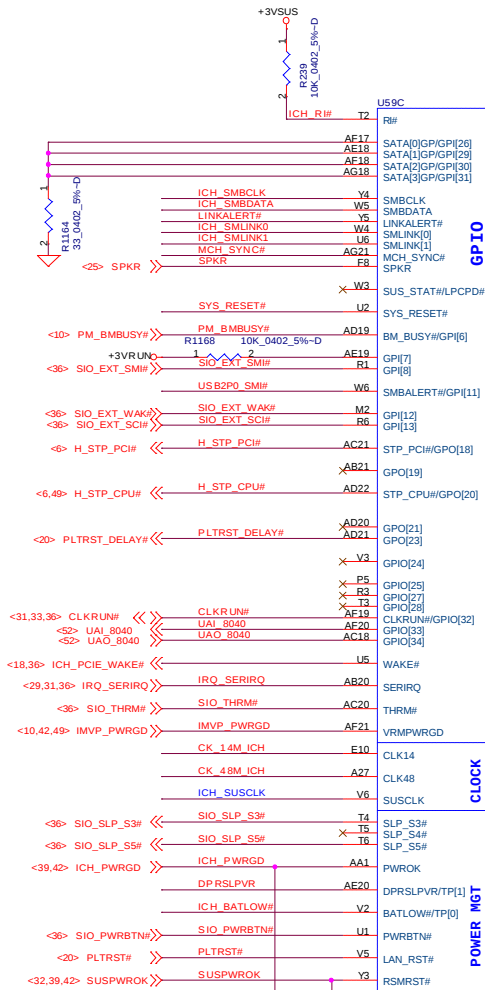


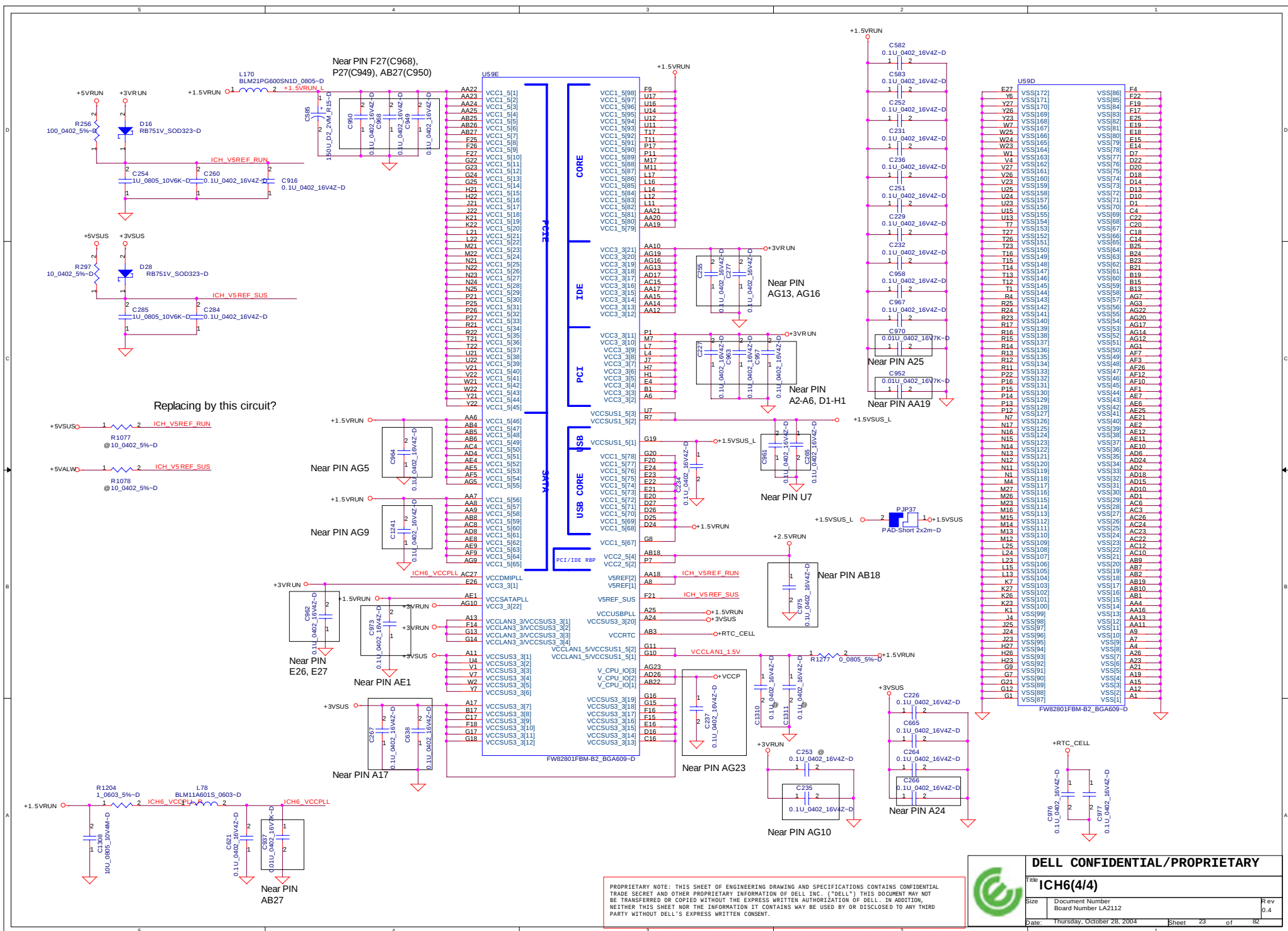


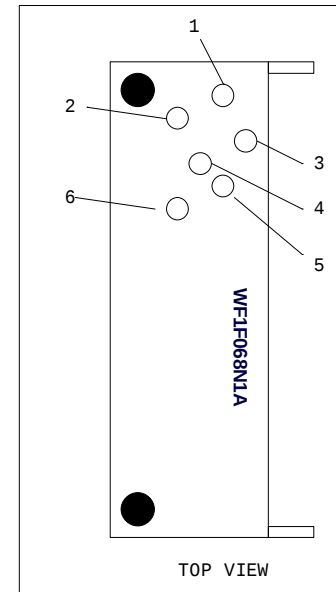
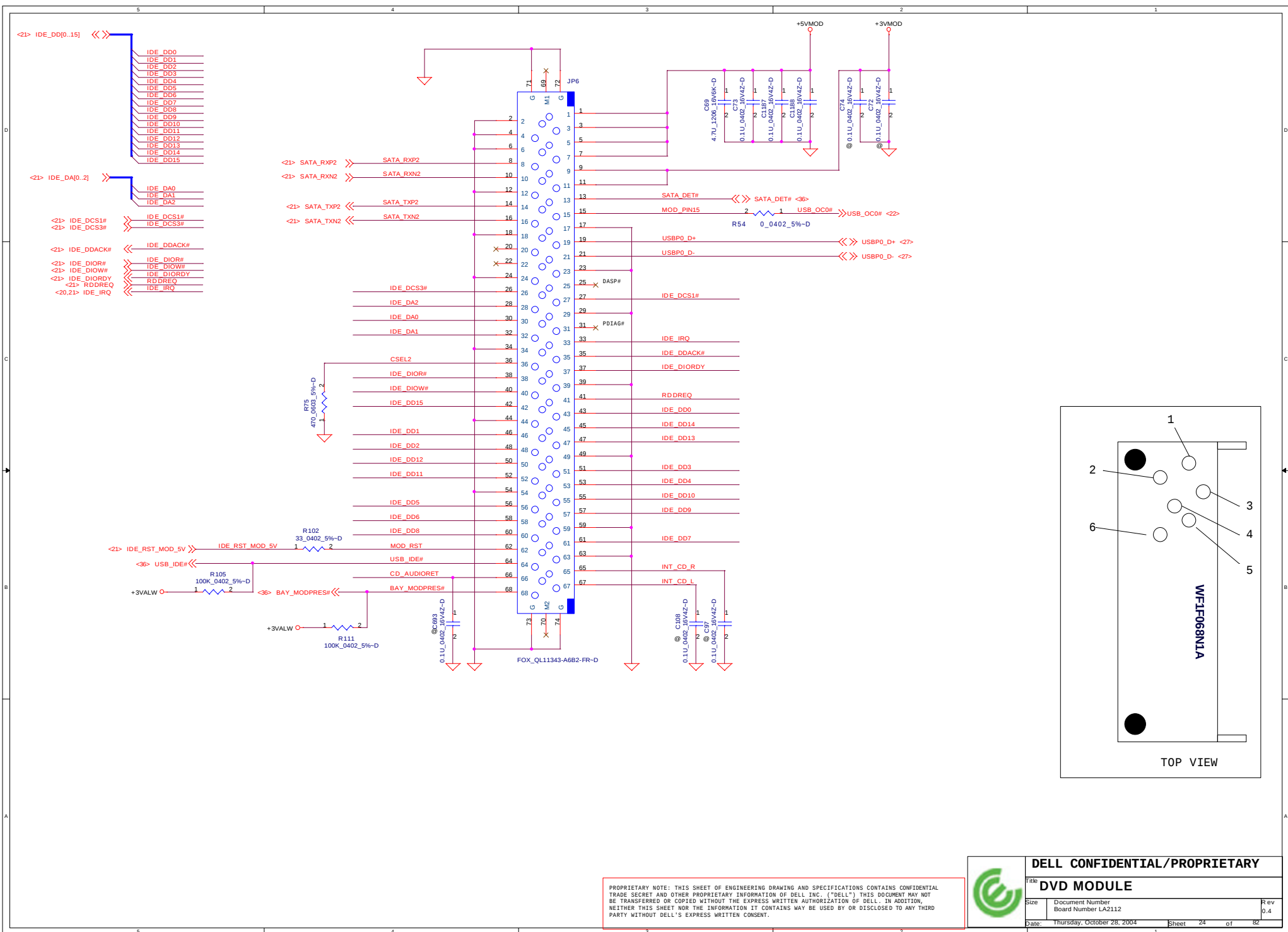
(PCI Express Wake Event)



Check List suggest pop 10/16





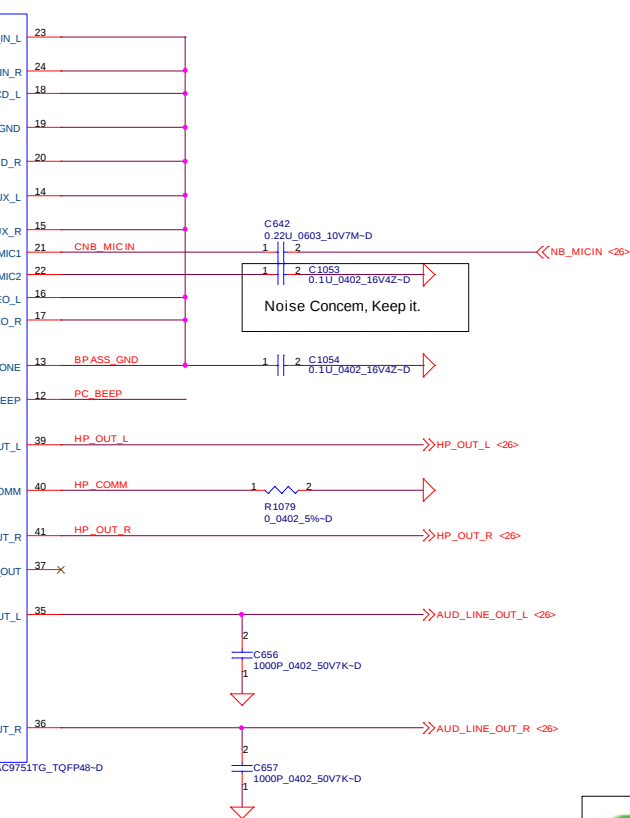
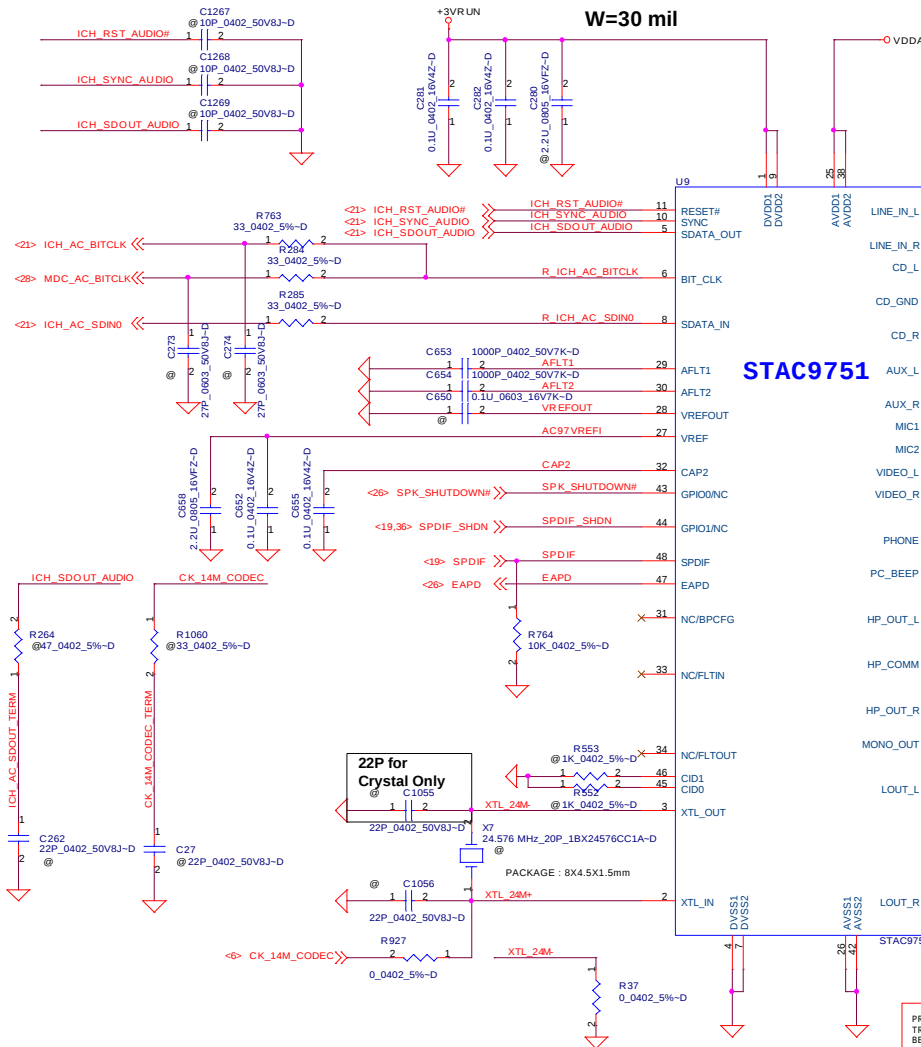
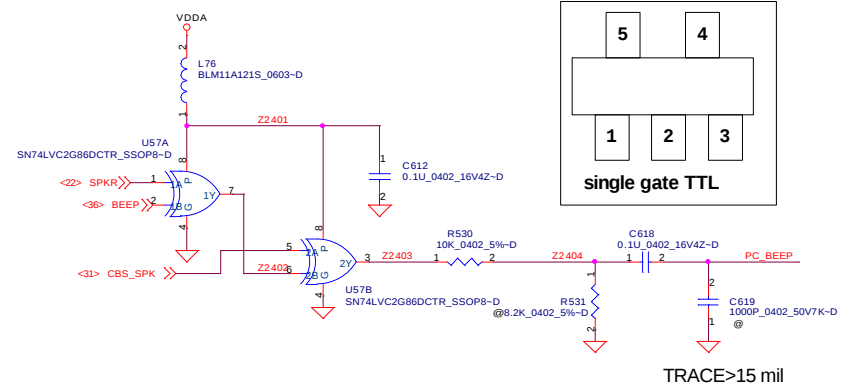
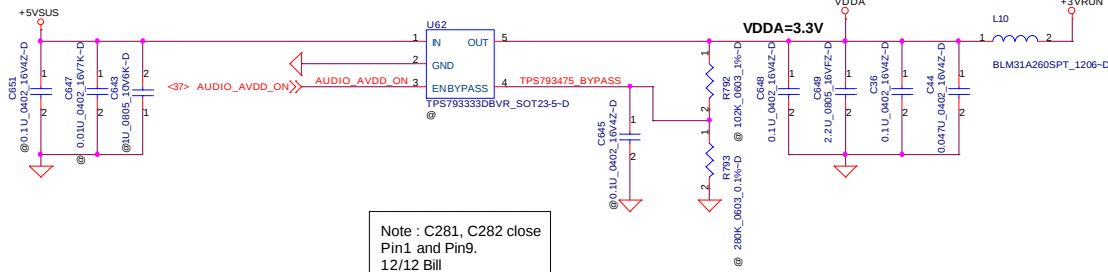


TOP VIEW

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Title **DVD MODULE**

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CLOCK SOURCE	Pin46 CID1	Pin45 CID0	Pin3 XTL_OUT
14.318 MHz	OPEN	OPEN	GND
27 MHz	OPEN	1K	GND
48 MHz	1K	OPEN	GND
24.576 MHz	1K	1K	GND

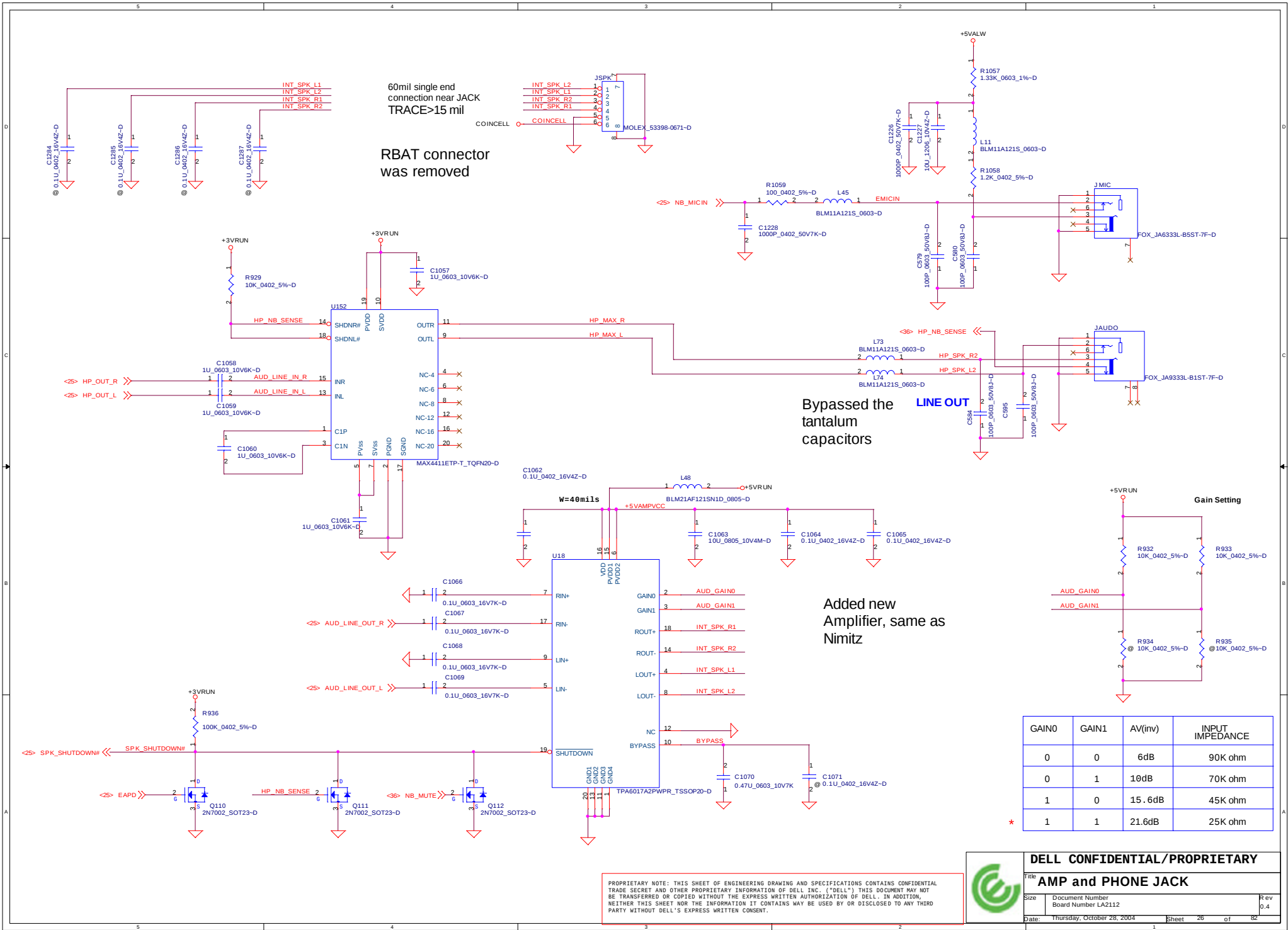
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GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm

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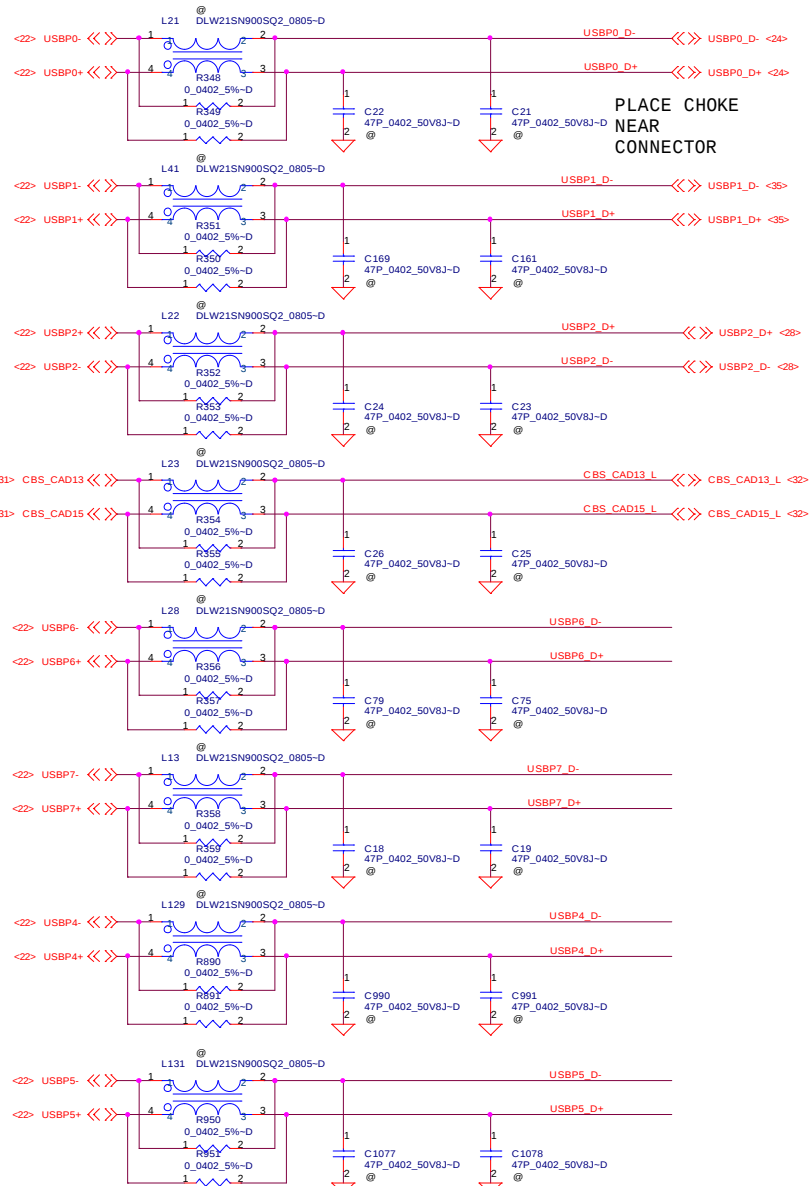


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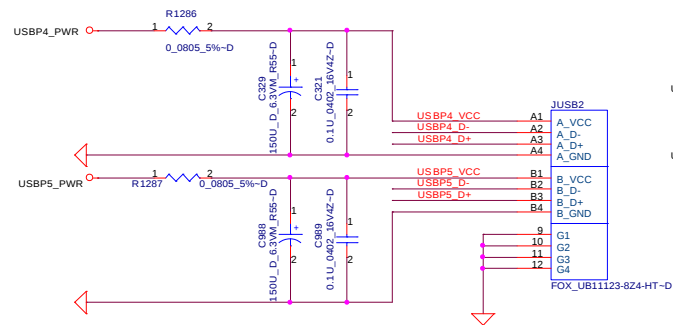
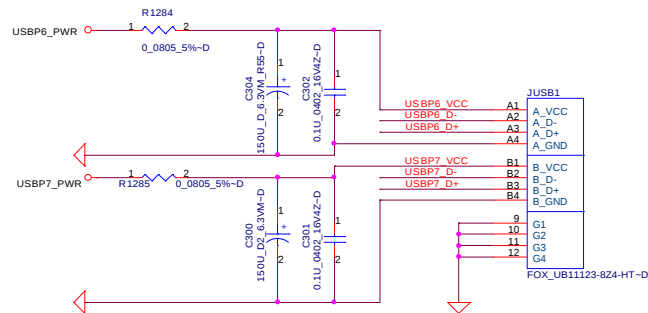
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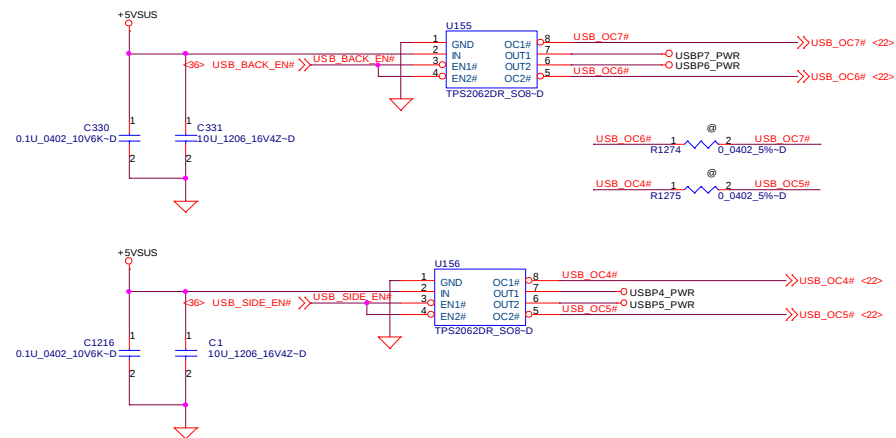
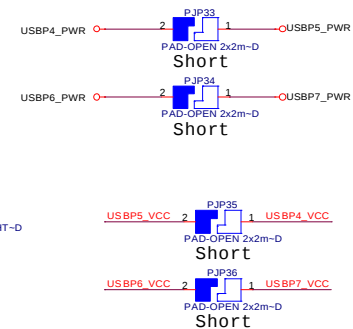
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PLACE CHOKE
NEAR
CONNECTOR



USB PORT#	DESTINATION
0	FDD (module bay)
1	DOCK
2	MPCI (BlueTooth)
3	NEW Connector
4	USB Port 2(Top)
5	USB Port 2(Bottom)
6	USB Port 1(Top)
7	USB Port 1(Bottom)

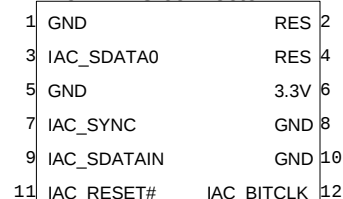
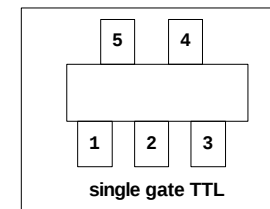
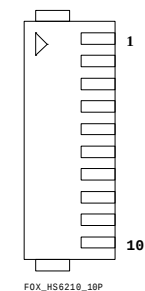
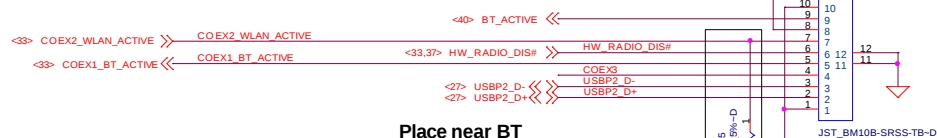


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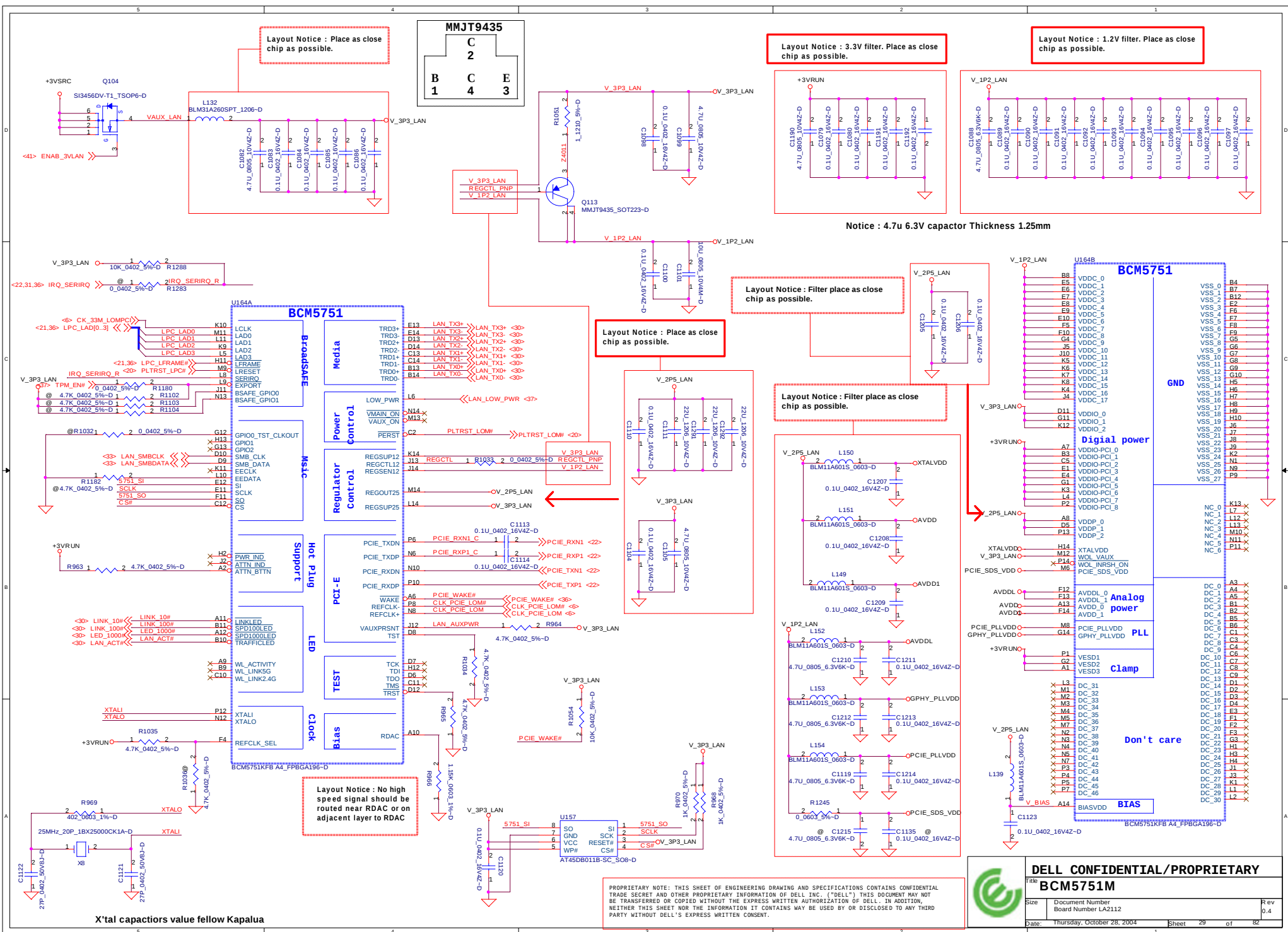


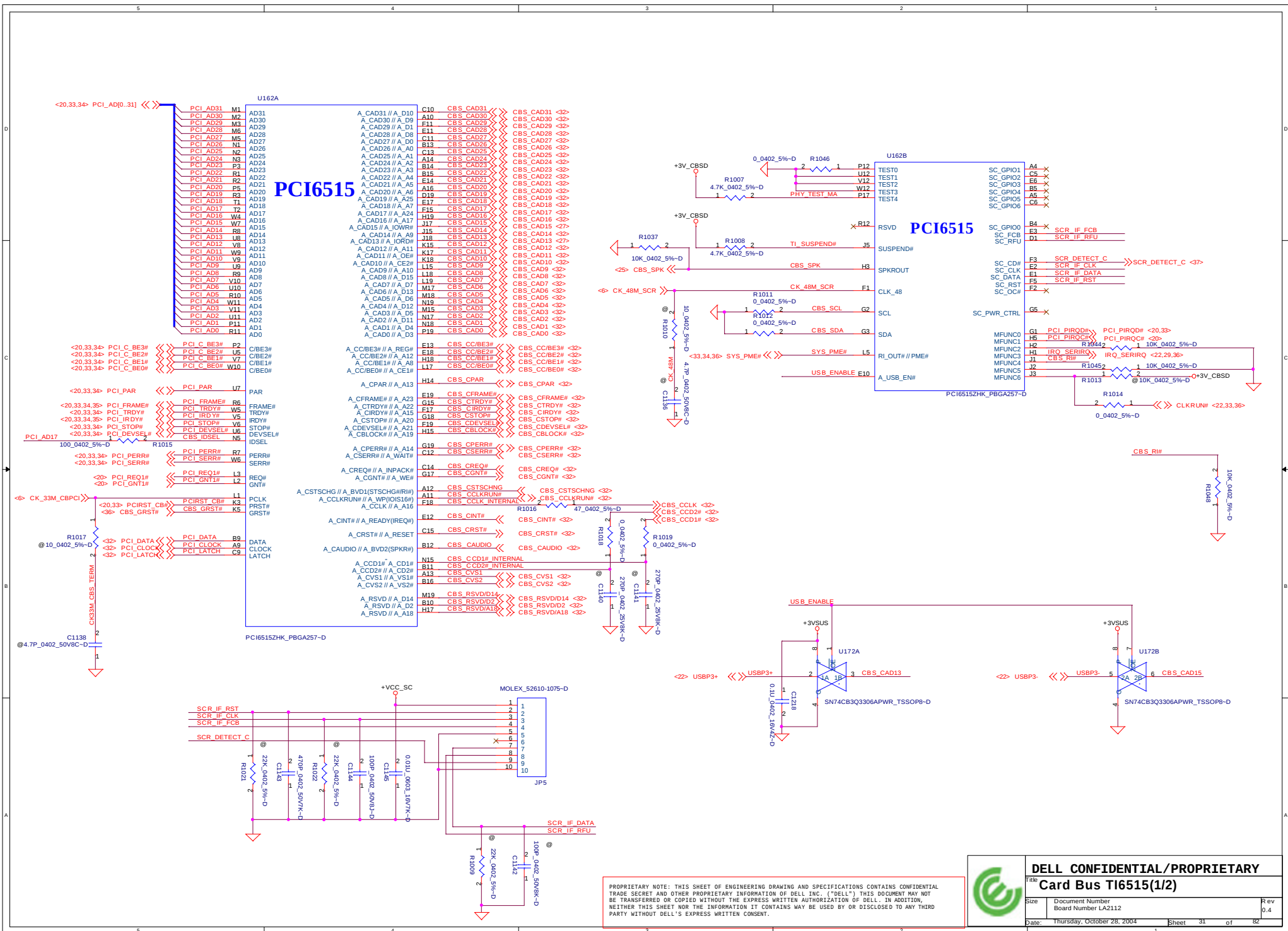
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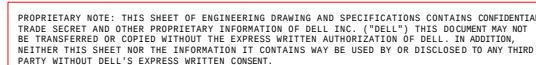
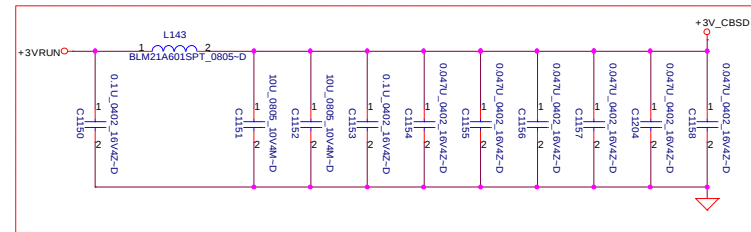
Title	BT PORT and MDC
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Size	Document Number Board Number LA2112	Rev 0.4
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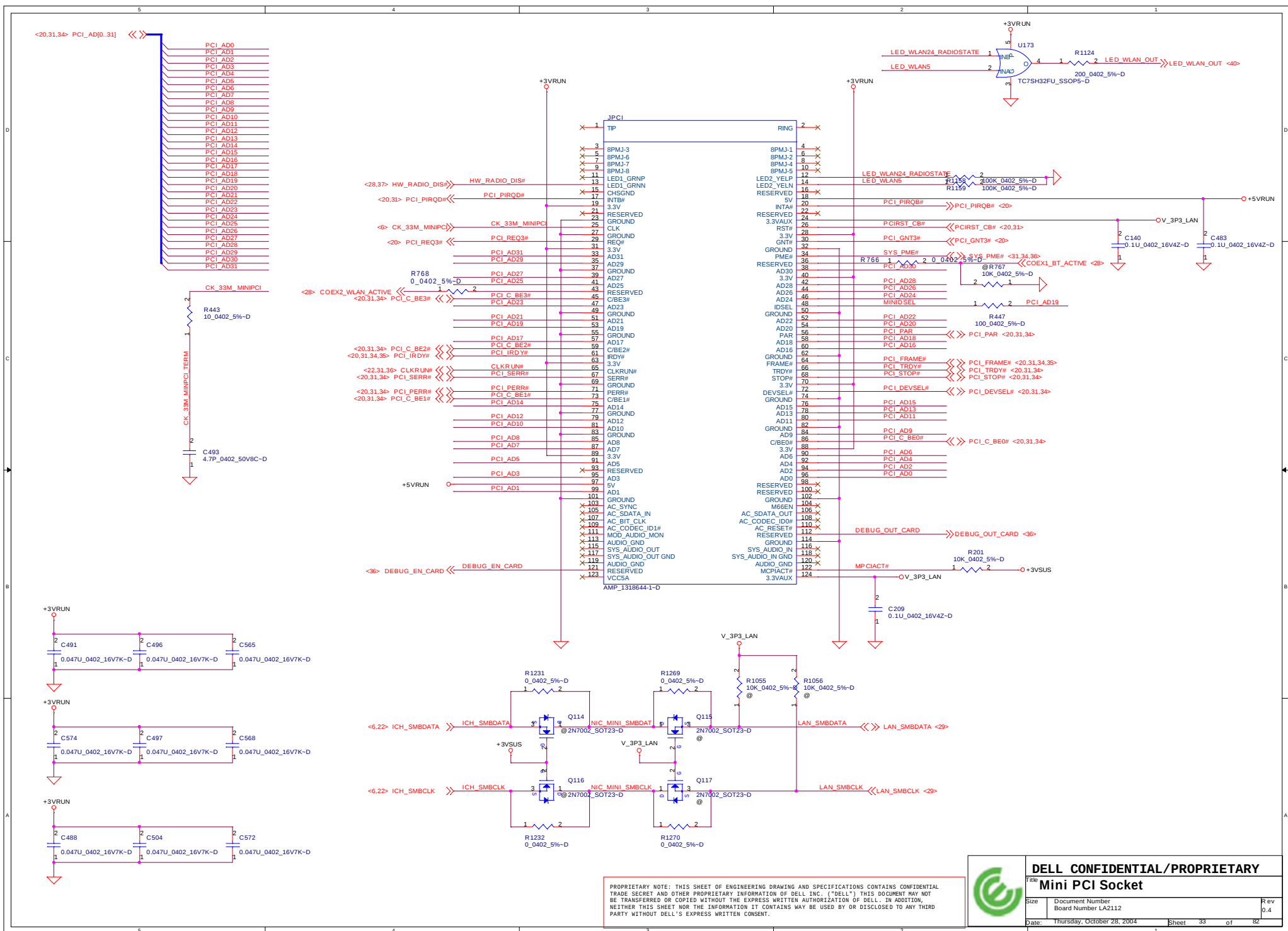






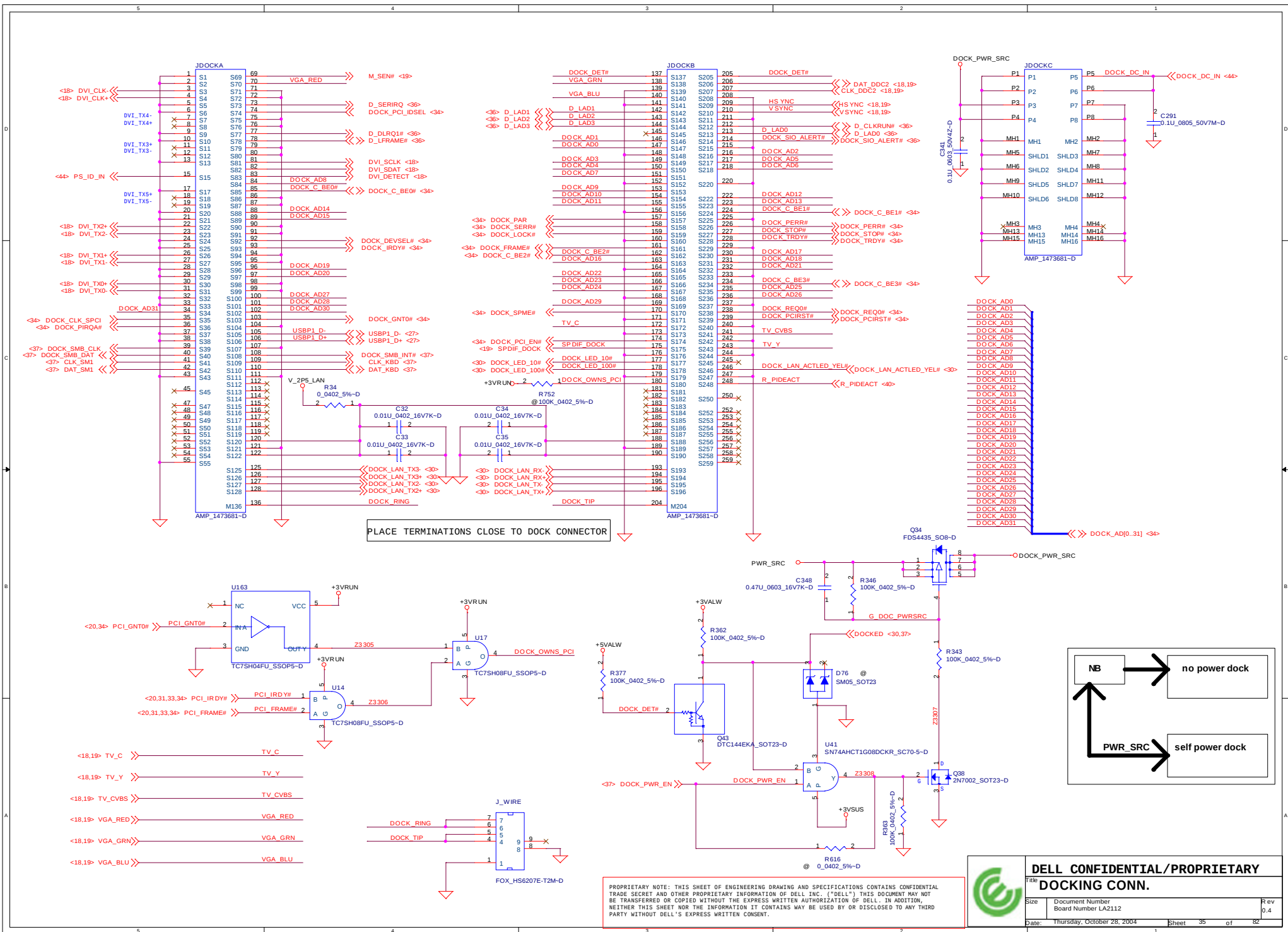
DELL CONFIDENTIAL/PROPRIETARY
 Title Card Bus TI6515(2/2)

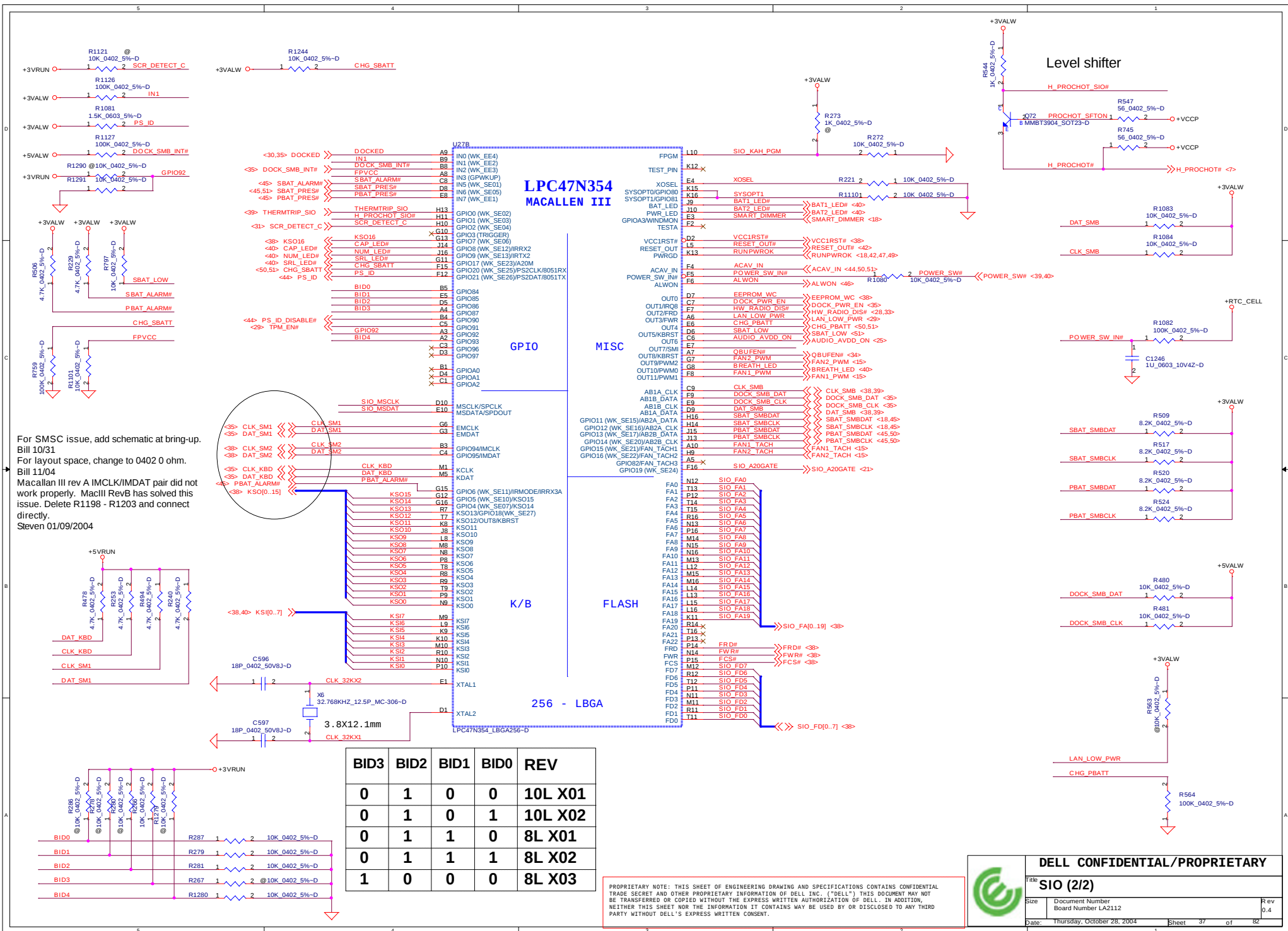
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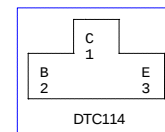
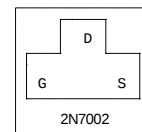
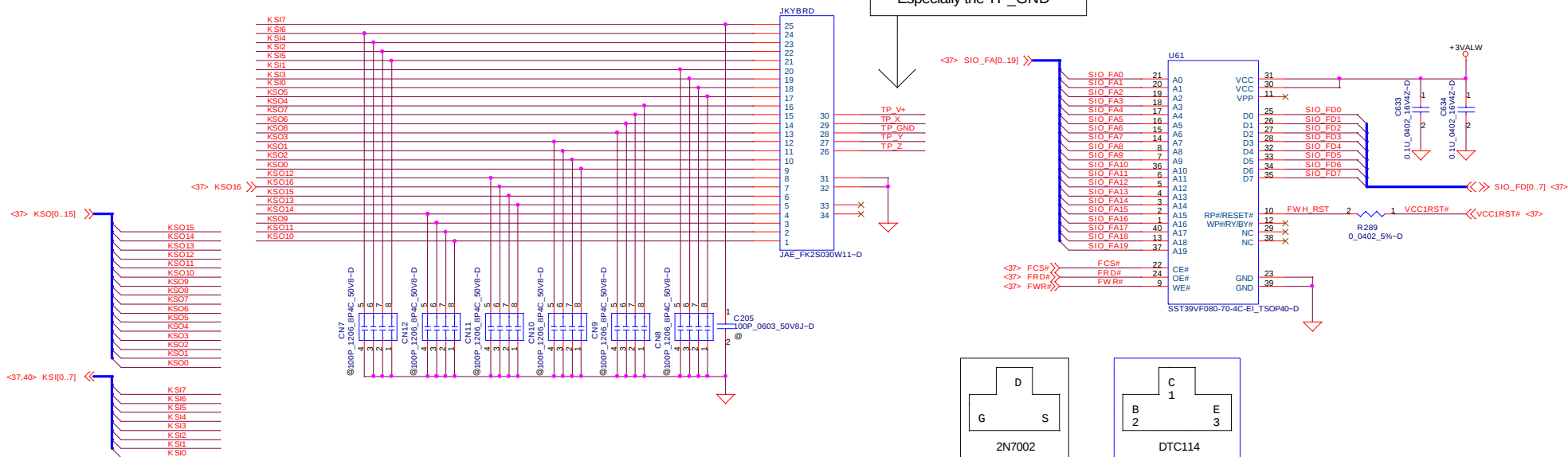
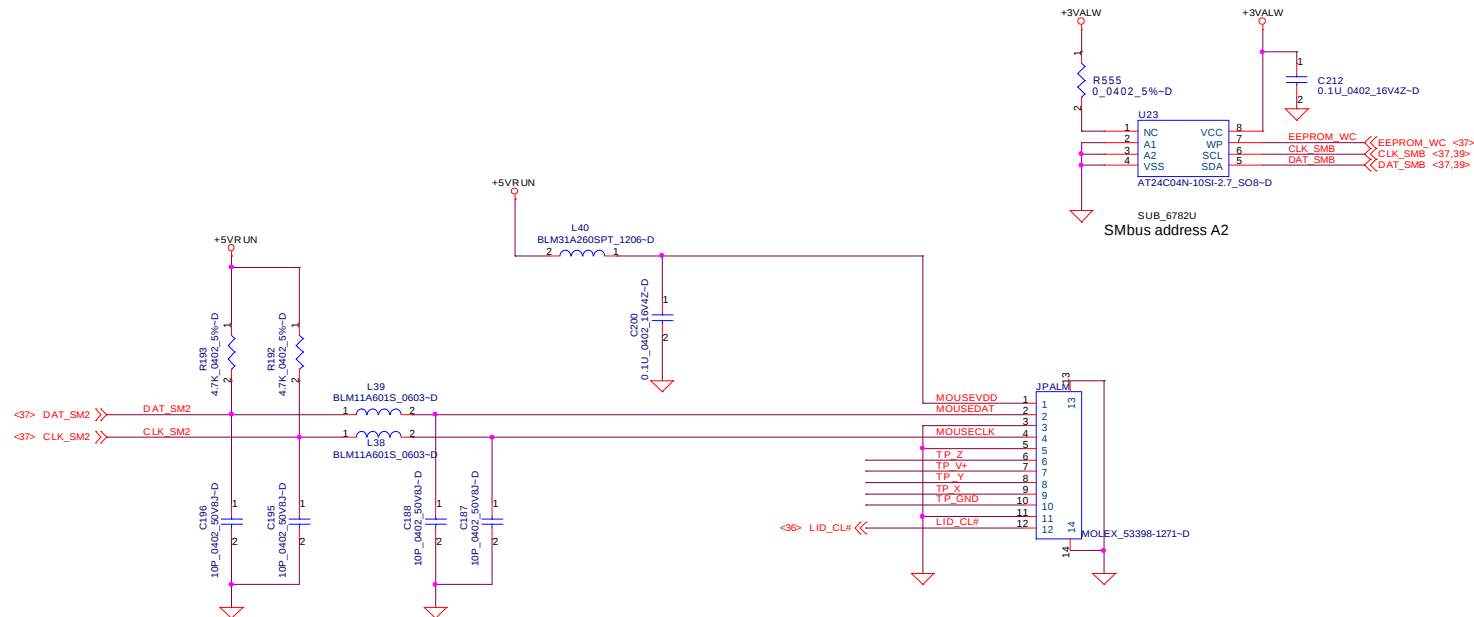




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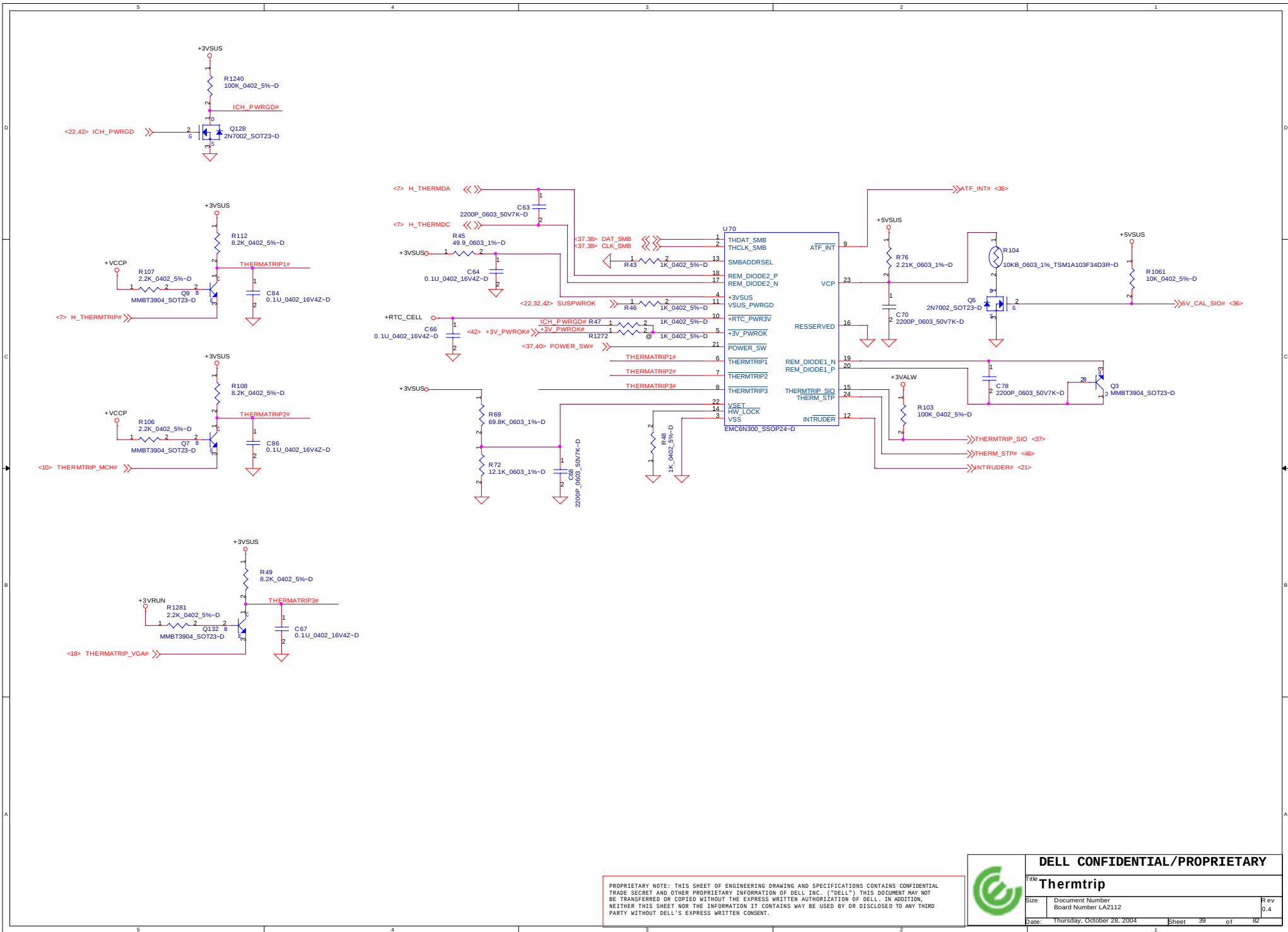


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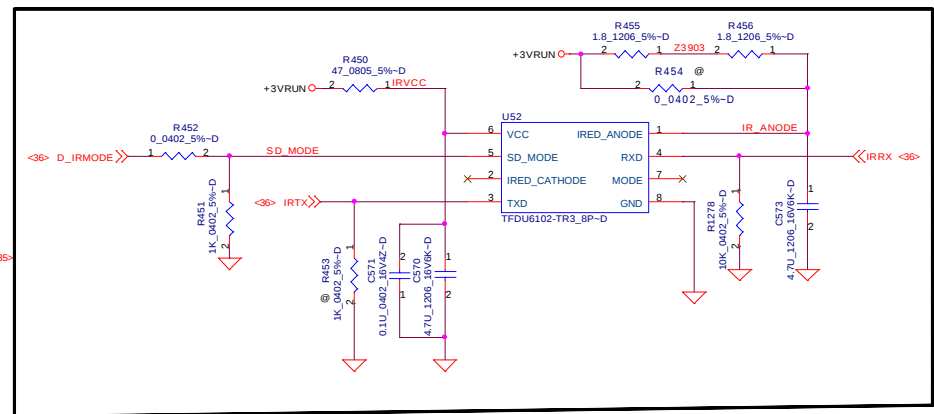
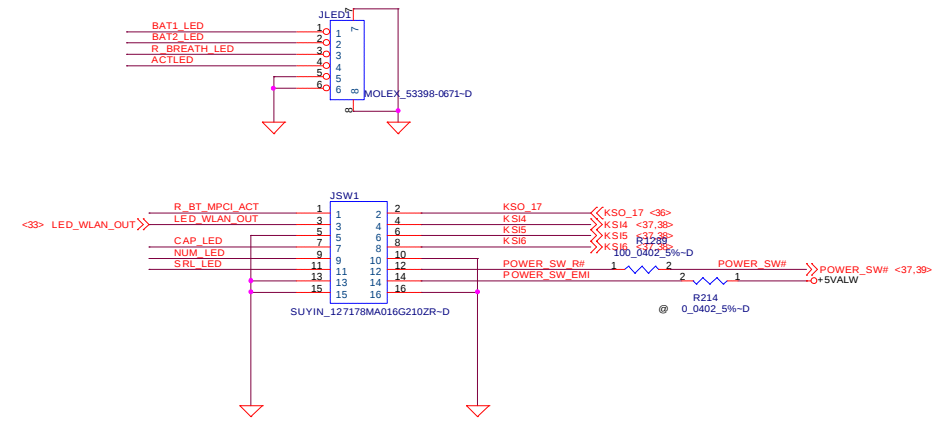
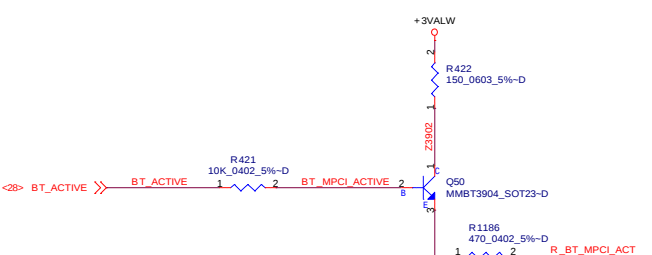
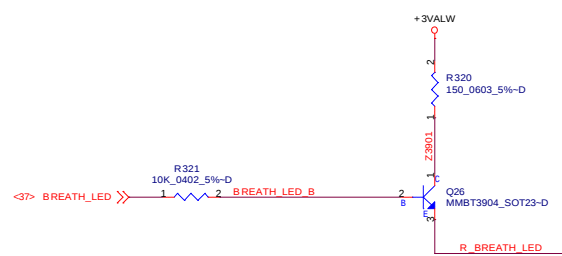
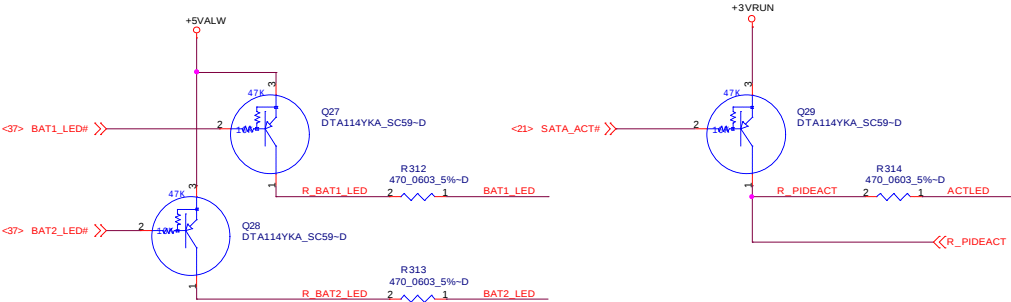
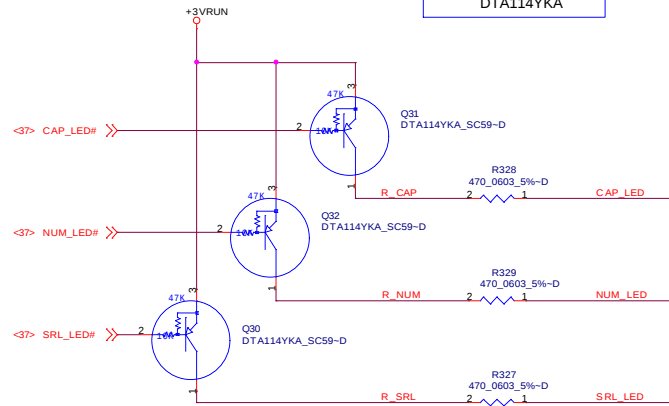
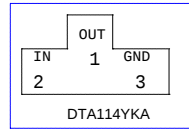
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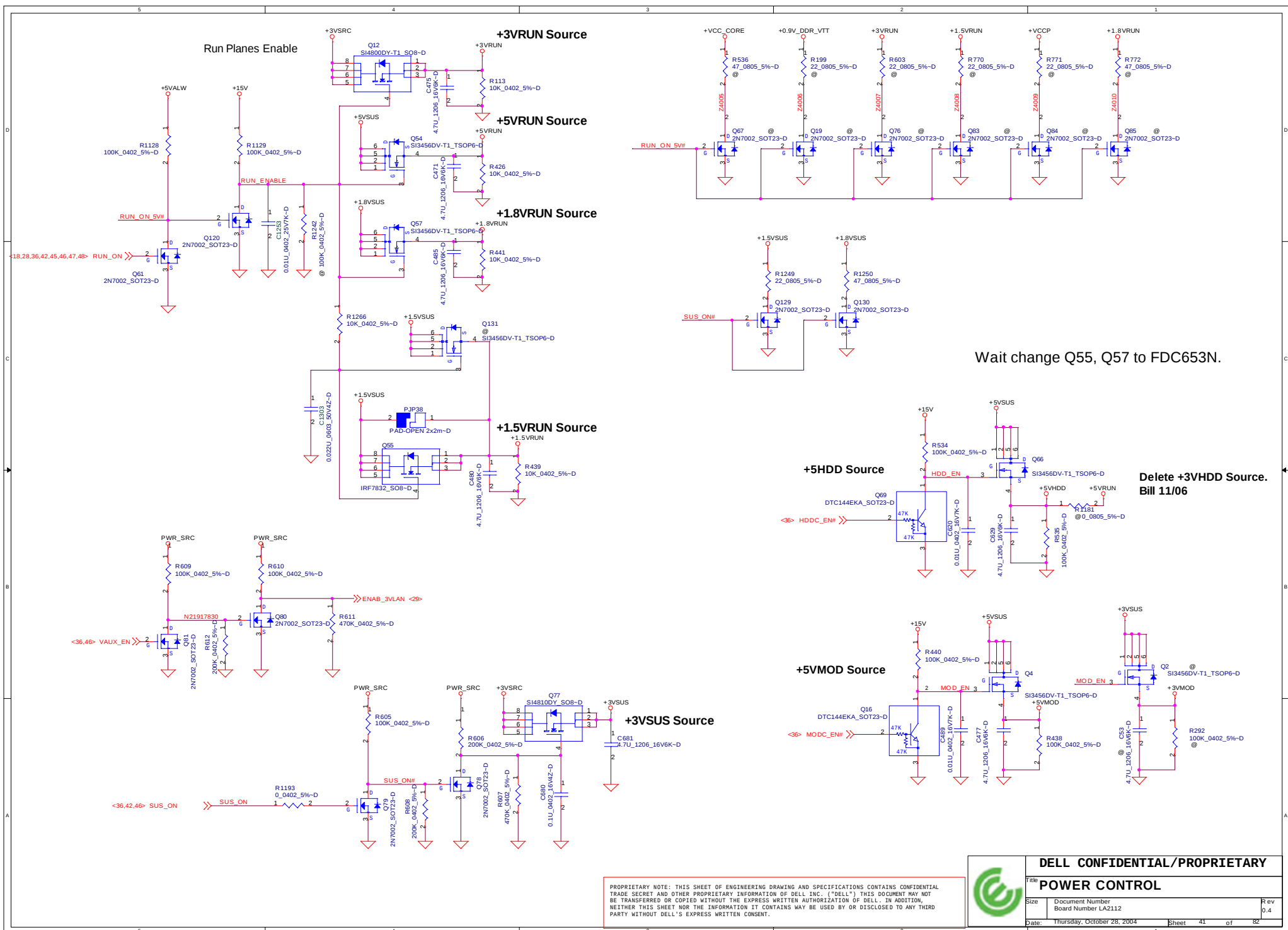
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Size	Document Number	Rev
	Board Number LA2112	0.4
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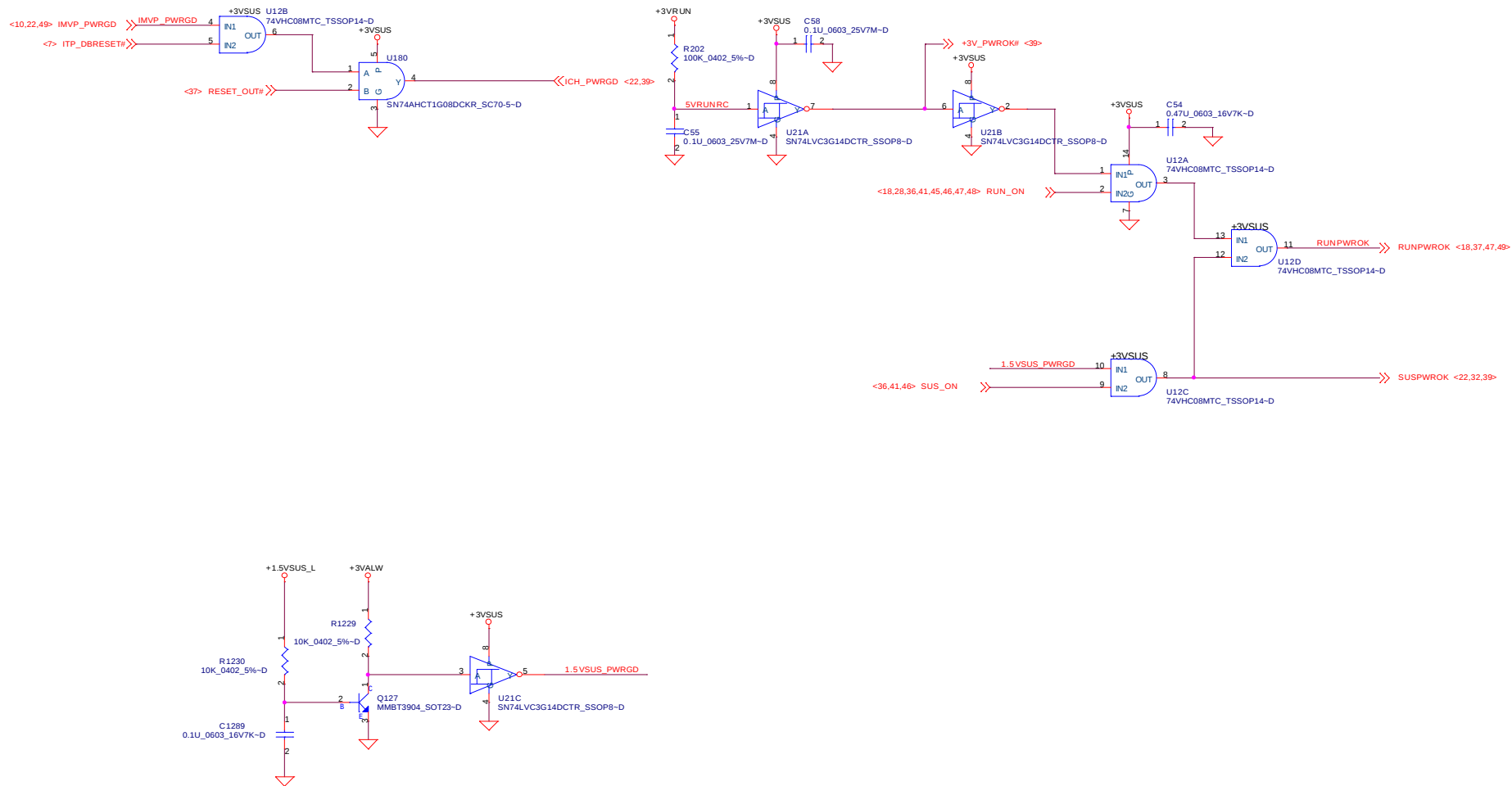


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Title: JLED/IR/PS2		
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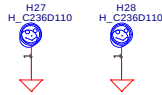
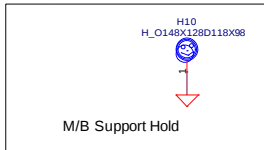
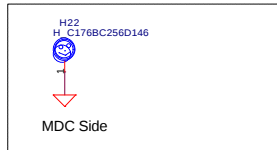
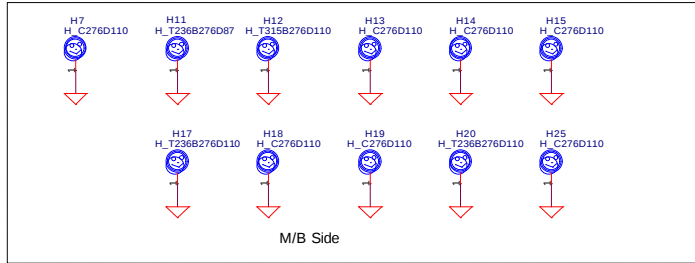
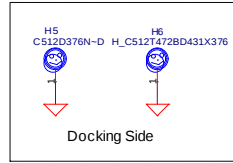
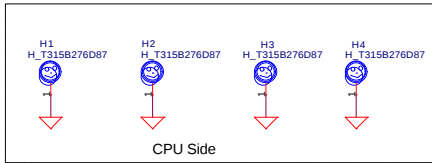
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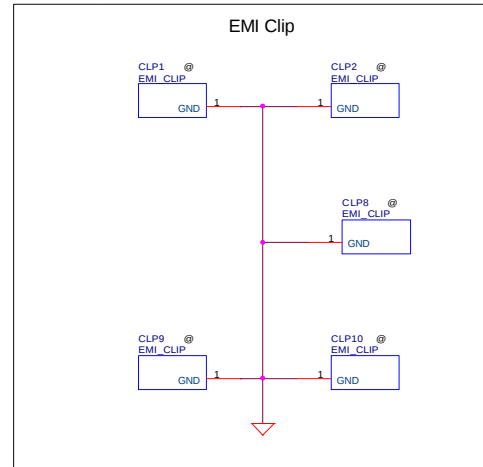
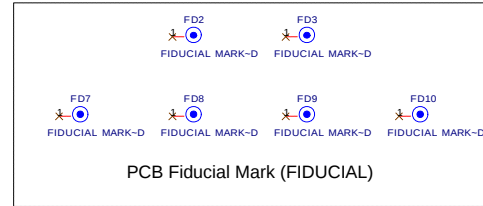
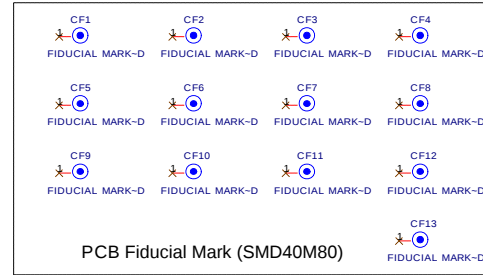
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Power Sequence

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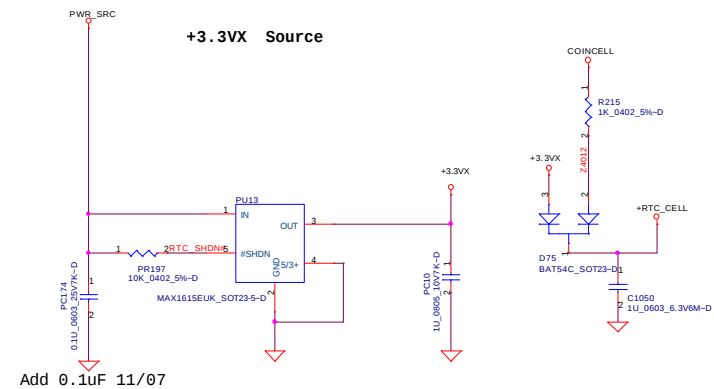
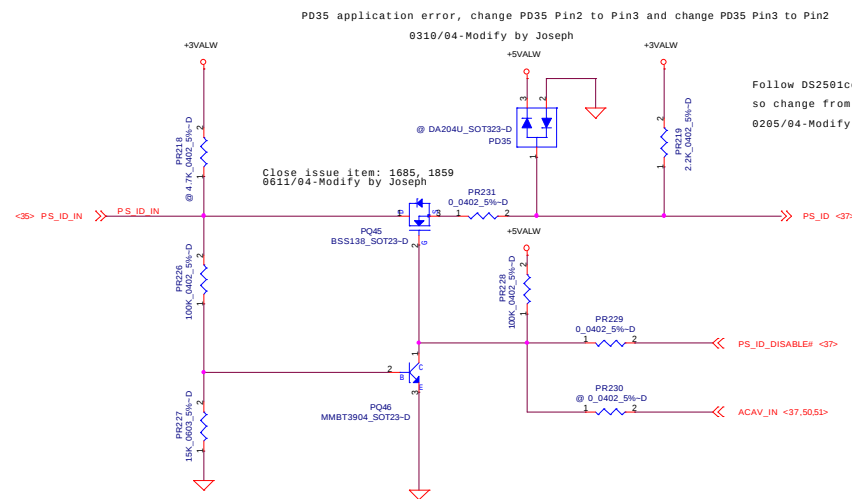
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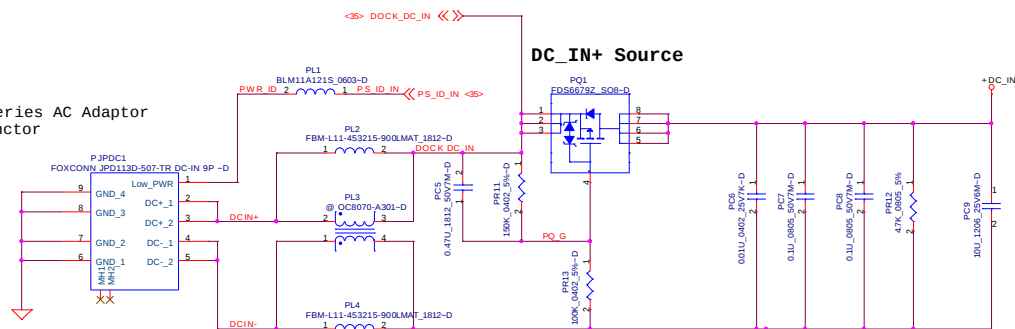
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Z-series AC Adaptor Connctor



Delete PL3 and Adding PL4 2004/03/09 modify by Joseph

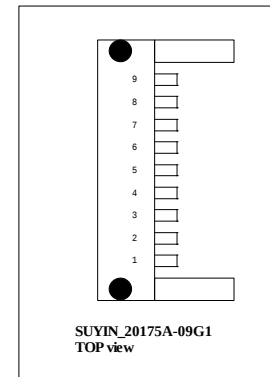
THE POINT
 NOTE: "THE POINT LOCATED
 AT PS MODULE

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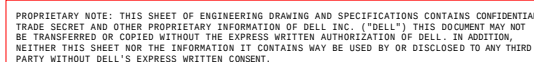


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Title		+DCIN	
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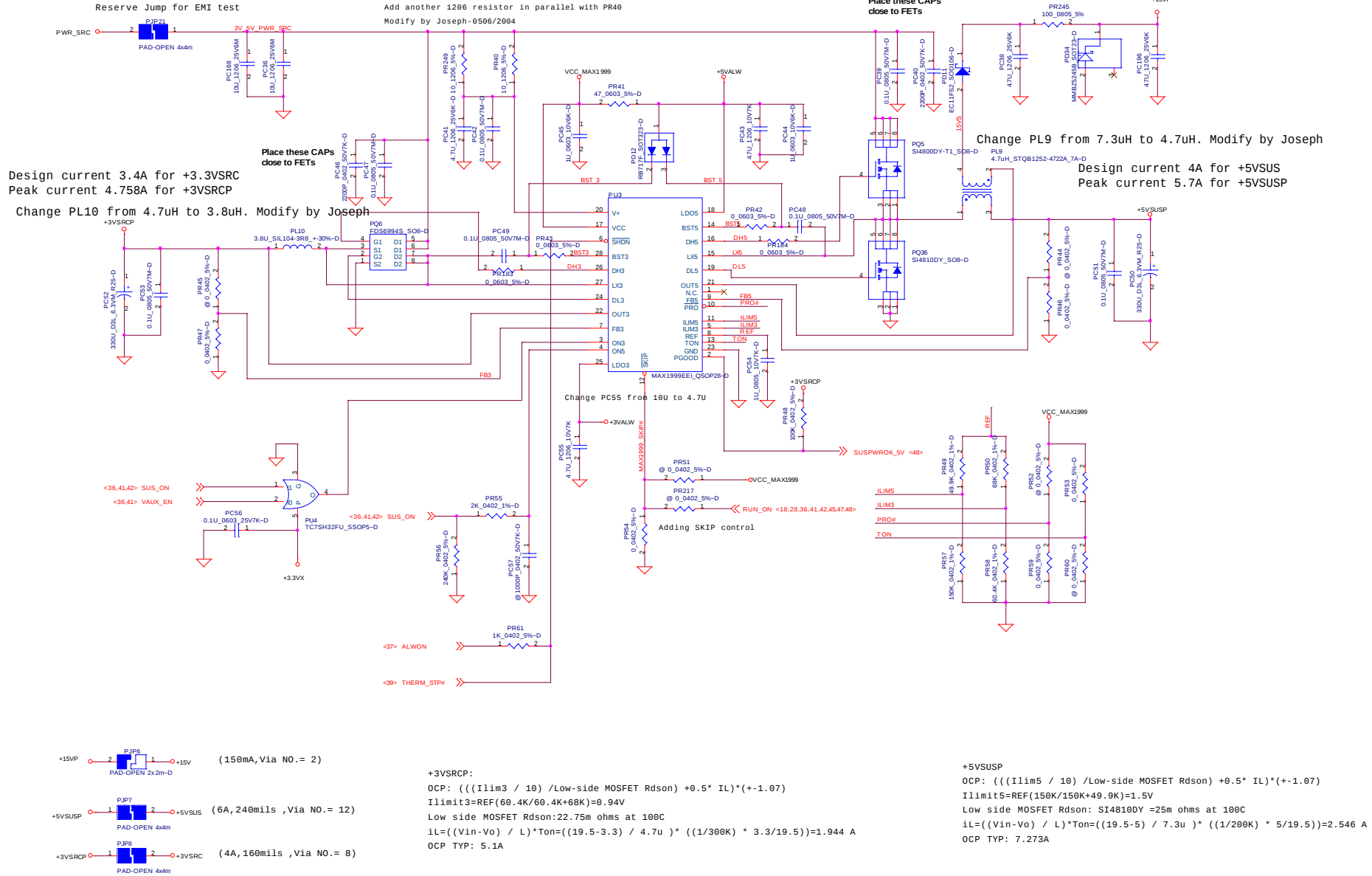


+2.5V_{RUN} $R1=R2 \cdot (V_o / 0.8 - 1)$, $R2: 25K \sim 100K$.



DC/DC +3V/ +5V/ +15V

Modify by Joseph 01/28/04



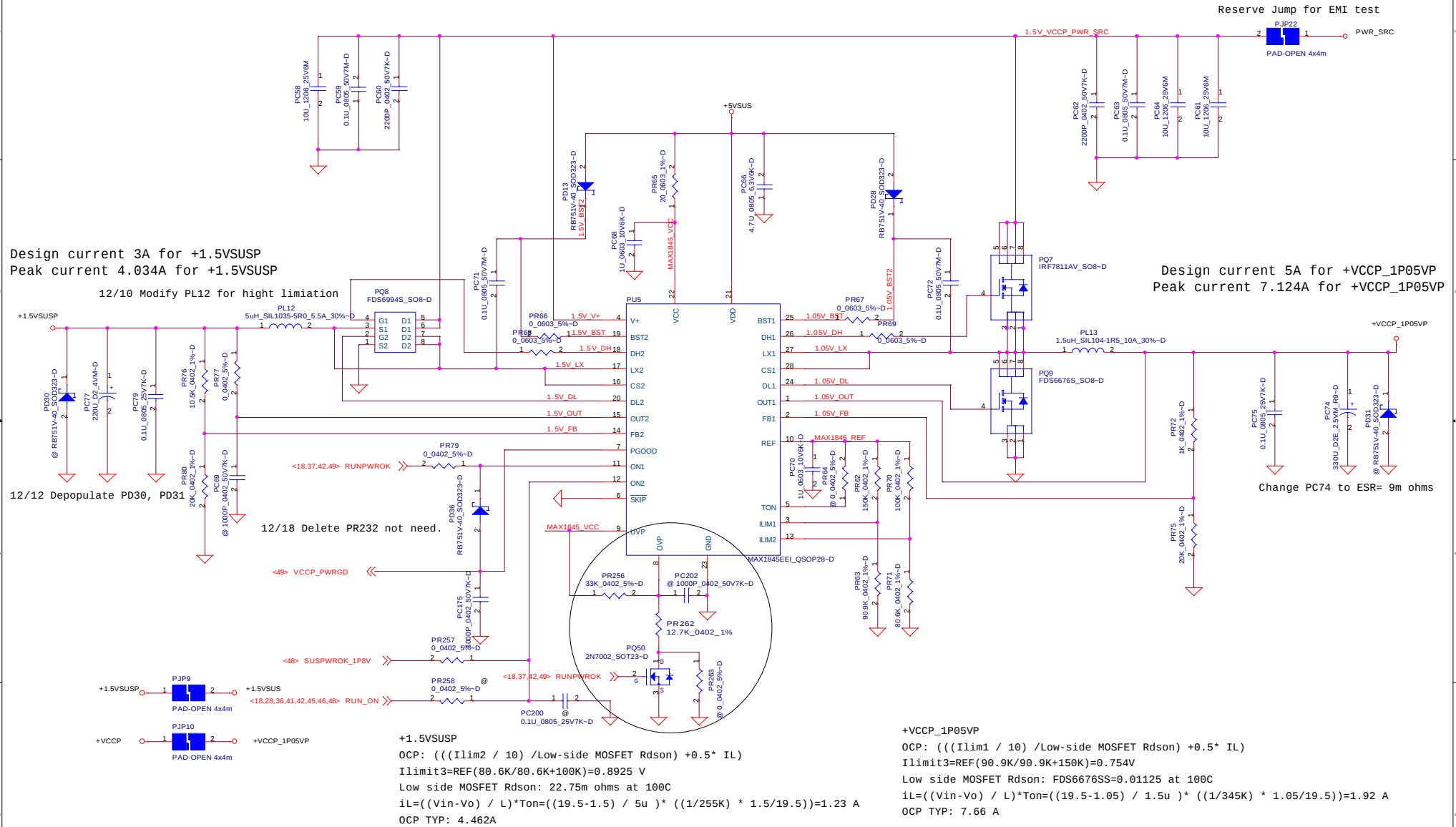
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+1.5VSUSP / +VCCP_1P05VP



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ev

+1.8VSUSP/ +0.9V_DDR_VTT DDR2 Termination

MAX8550	MAX8550A
POP PR239	DEPOP PR239
POP PQ49	DEPOP PQ49
DEPOP PR250	POP PR250
POP PR254	DEPOP PR254
DEPOP PR255	POP PR255

Modify by Joseph -06/11/2004

Reserve when use MAX8550A
Modify by Joseph -05/12/2004

Update design current to 10.6A -0128/04
Design current 10.6A for +1.8V_SUSP

Update symbol -0502
Modify by Joseph -0502

0305/2004-Modify by Joseph.

0202/04-Modify by Joseph

Install jumper on PJP32 pad and depop PJP31
0207/2004

0205/04- Reserve PC198. Modify by Joseph
Change from 22uF to 10uF for cost down.
Pop PC198. Modify by Joseph -06/02/2004

For issue 1807 Add a 0-ohm No Pop Resistor that
connects to pin 1 of PR243 and to 1.8_VDD at pin 2 of PC182
Modify by Joseph -0502

0128/04-Modify by Joseph for updated OCP.
0202/04-Modify by Joseph

Install jumper on PJP30 pad.

+1.8VSUSP
OCP: $((I_{lim} / 10) / \text{Low-side MOSFET } R_{ds(on)} + 0.5) \cdot I_L$
 $I_{limit} = \text{REF}(53.6K/53.6K+100K)=0.6979 \text{ V}$
Low side MOSFET $R_{ds(on)}$: 6.5m ohms at 100C
 $I_L = ((V_{in} - V_o) / L) \cdot T_{on} = ((19.5 - 1.8) / 1.4 \mu) \cdot ((1/450K) \cdot 1.8/19.5) = 2.59A$
OCP TYP: 11.37A

(10A, 320mils, Via NO.=20)

(2A, 200mils, Via NO.=4)

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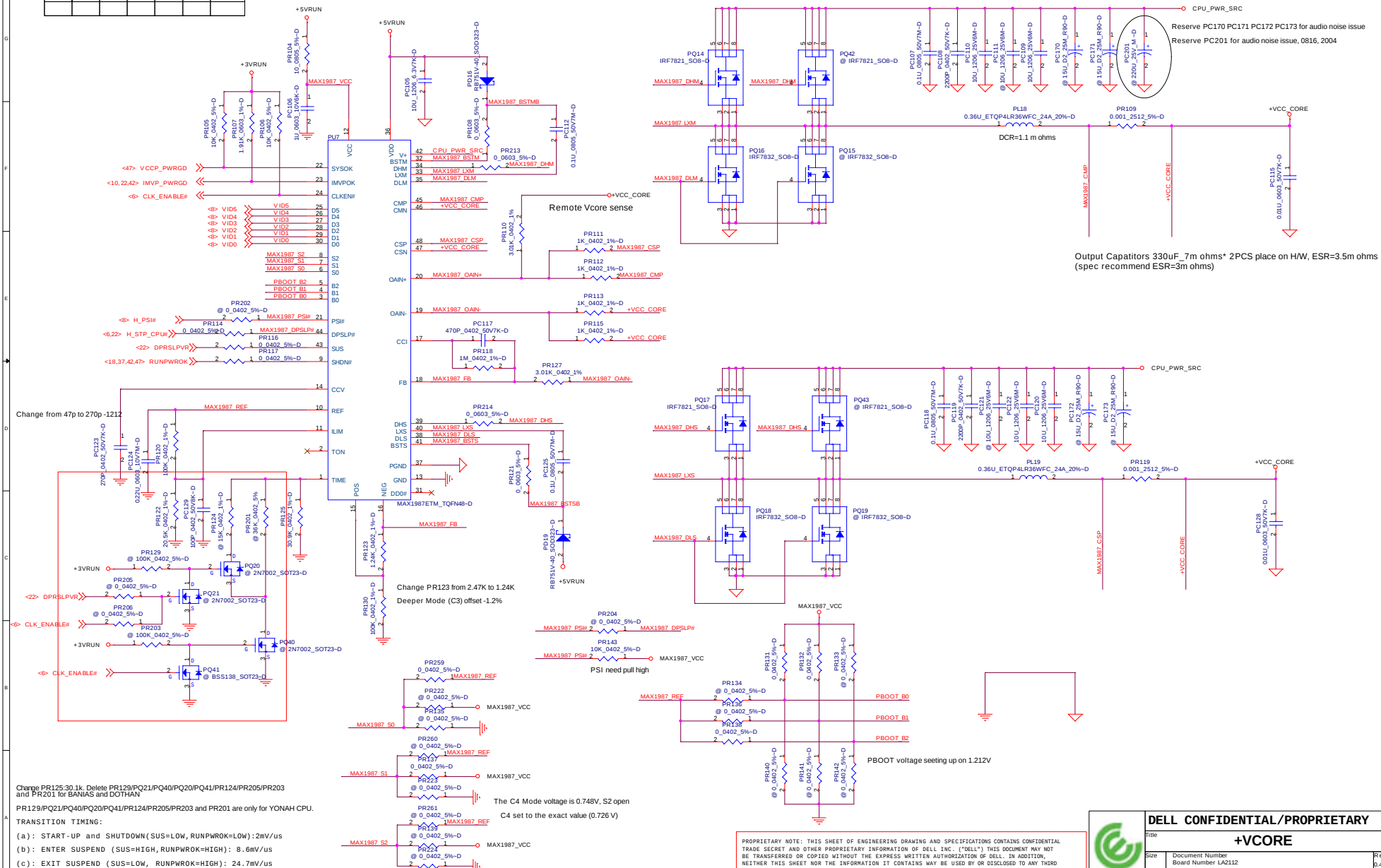
DELL CONFIDENTIAL/PROPRIETARY

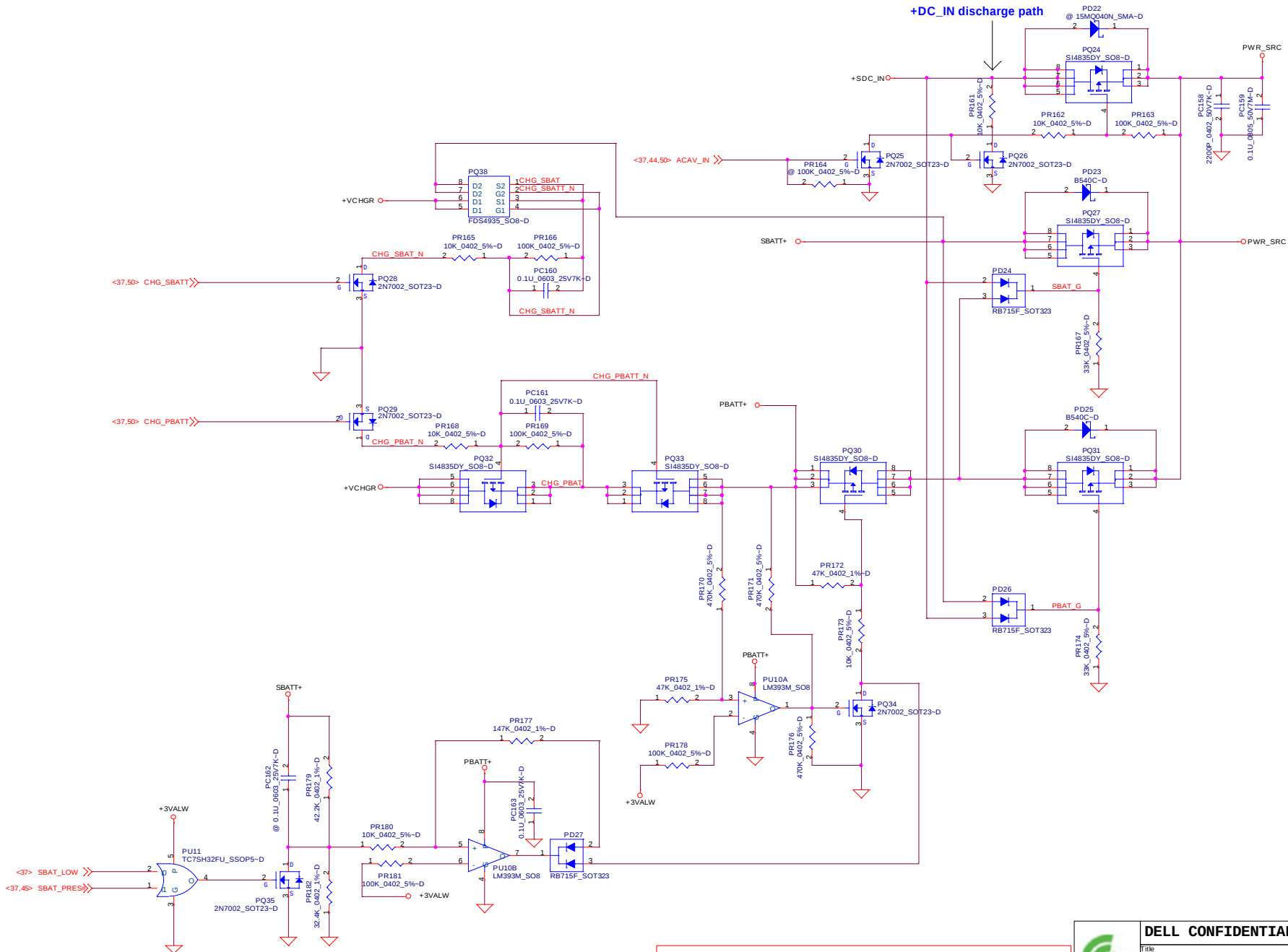
Title: +1.8VSUSP/ +0.9V_DDR_VT

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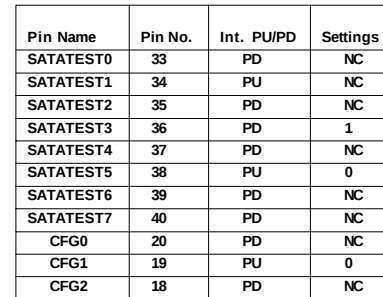
V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	v
0	1	1	1	1	0	1.484
0	1	1	0	0	1	1.398
1	0	1	1	1	1	0.956
1	1	1	1	0	0	0.748





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Sets maximum transfer rate and UDMA mode

	CNFG2	CNFG1	CNFG0	NOTE
*	0	0	0	Device Mode 100MB/s
	0	0	1	Device Mode 133MB/s
	0	1	0	Device Mode 150MB/s
	1	0	0	Host Mode 100MB/s
	1	0	1	Host Mode 133MB/s
	1	1	0	Host Mode 150MB/s
	0	1	1	Reserved
	1	1	1	Reserved

