

Compal Confidential

QBL50 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

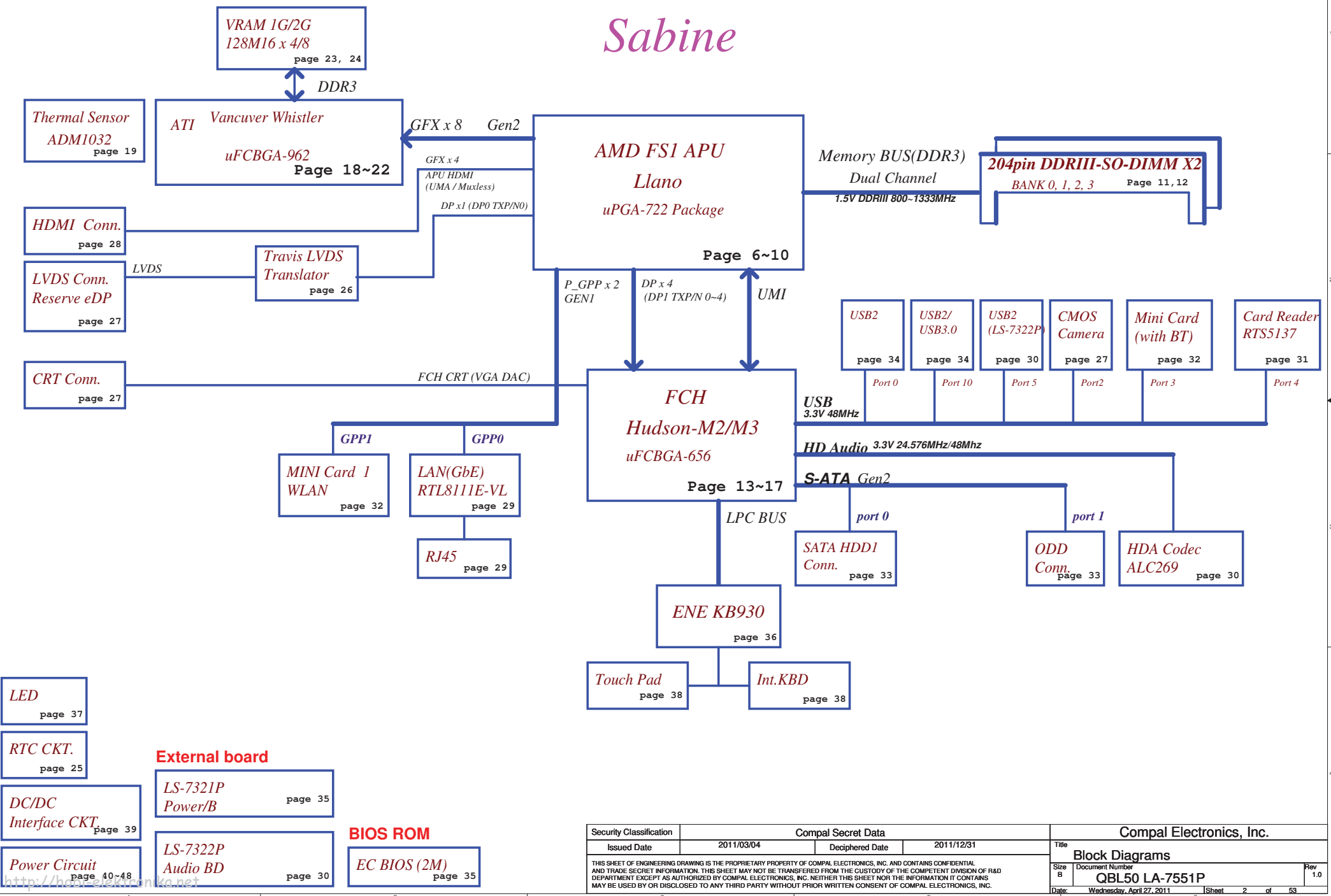
2011-04-25

Rev : 1 . 0

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				Size B	Document Number QBL50 LA-7551P Date: Wednesday, April 27, 2011
				Rev 1.0	Sheet 1 of 53

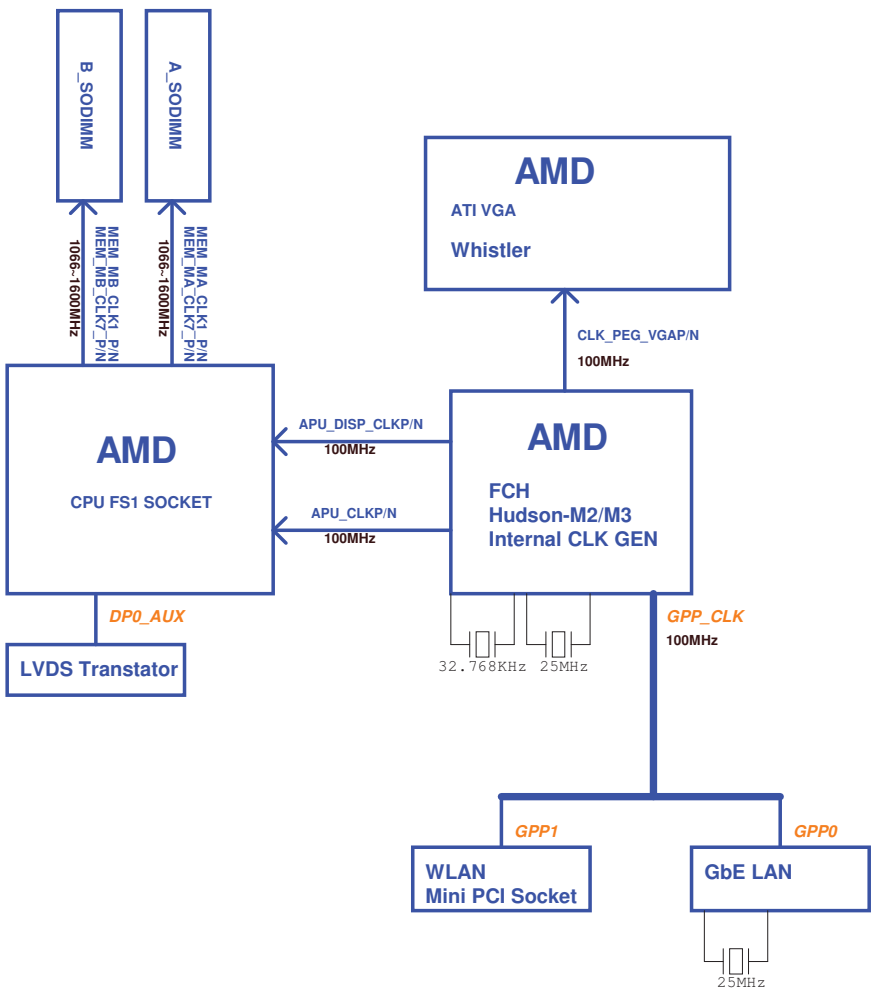
Compal Confidential

Model Name : QBL50

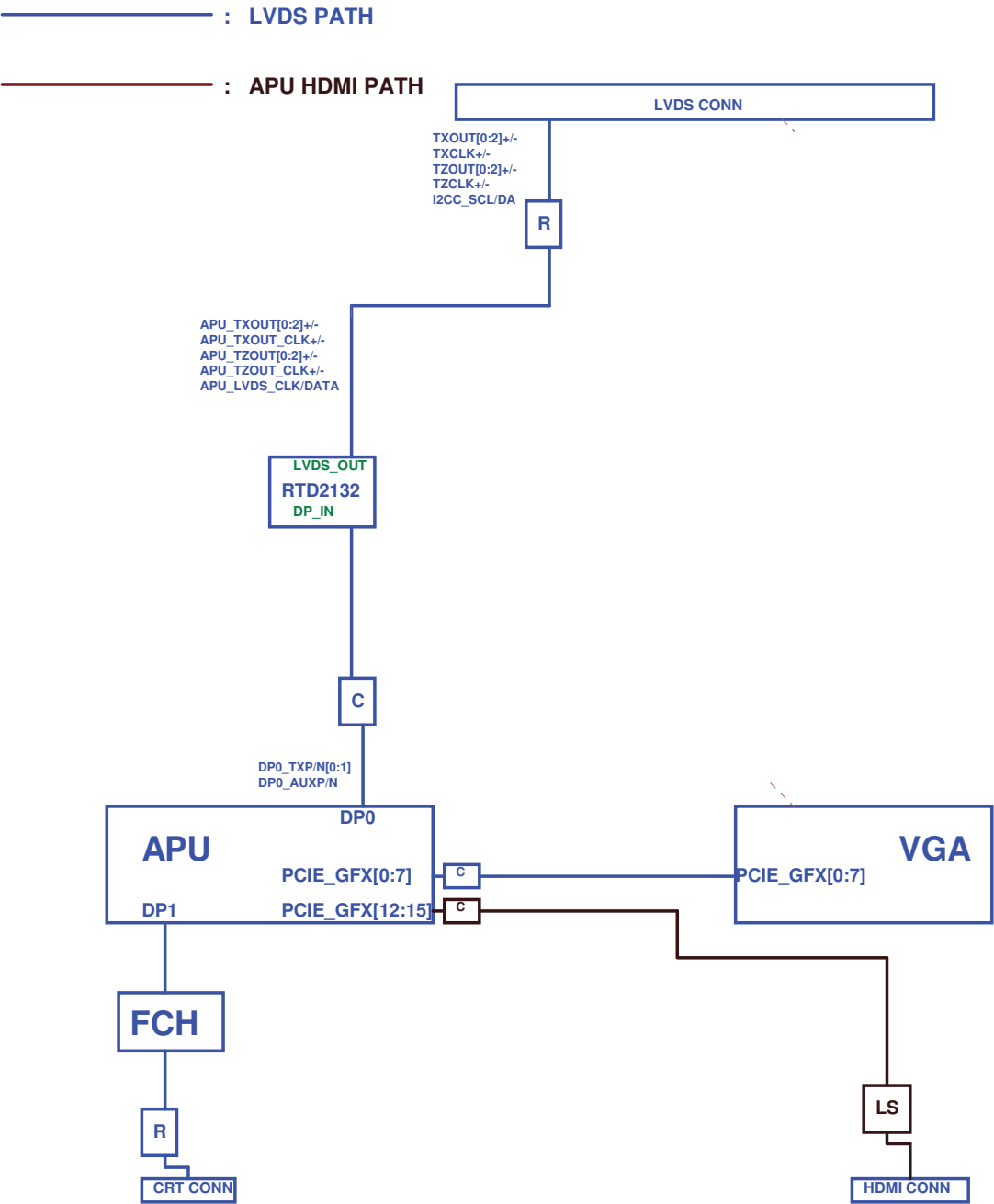


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				Size B	Document Number
				QBL50 LA-7551P	
Date: Wednesday, April 27, 2011				Sheet 2	Rev 1.0
				of 53	

CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



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				Date:	Wednesday, April 27, 2011
				Sheet	3 of 53
				Rev	1.0

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (VGA)	1001 101X b	9AH
			(APU)		
			RTD2132S (TL)		

FCH
SM Bus 0 address

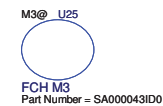
FCH
SM Bus 1 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	D0			
DDR DIMM2	1101 001X b	D2			

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

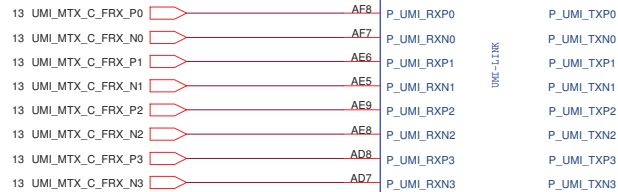
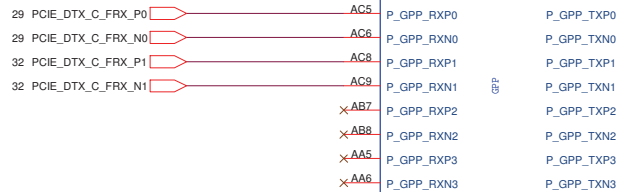
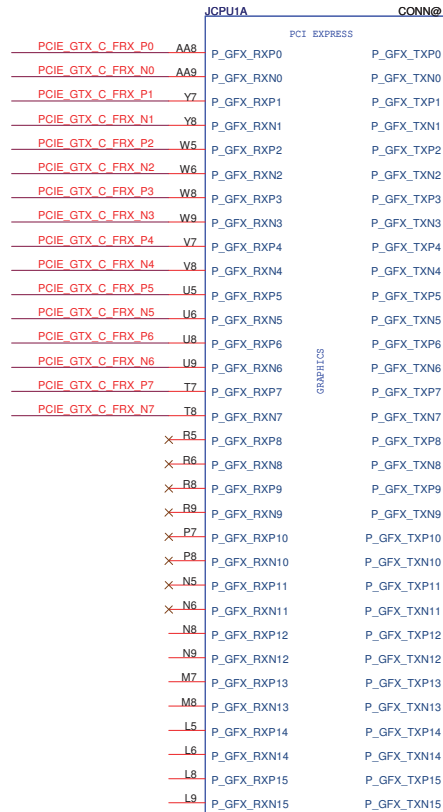
BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

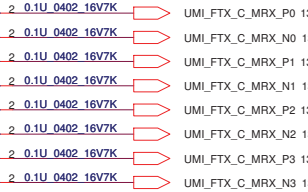
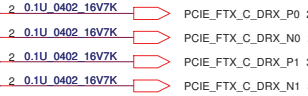


BOM Config

18 PCIE_GTX_C_FRX_P[0..7] 18 PCIE_GTX_C_FRX_N[0..7]



PCIE_FTX_C_GRX_P[0..7] 18 PCIE_FTX_C_GRX_N[0..7] 18

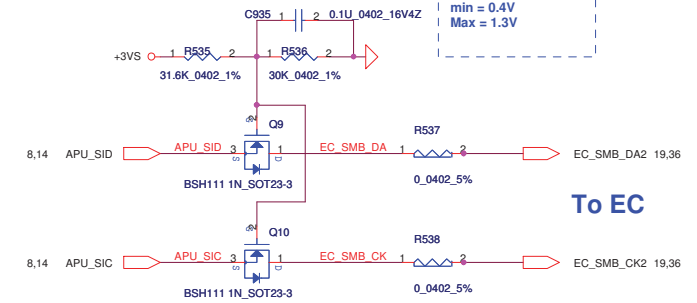


APU To HDMI

PCIE_FTX_GRX_P[12..15] 28 PCIE_FTX_GRX_N[12..15] 28

For UMA Mux.

CPU TSI interface level shift



To EC

Power Sequence of APU

+1.5V

+2.5VS

+1.5VS

+CPU_CORE

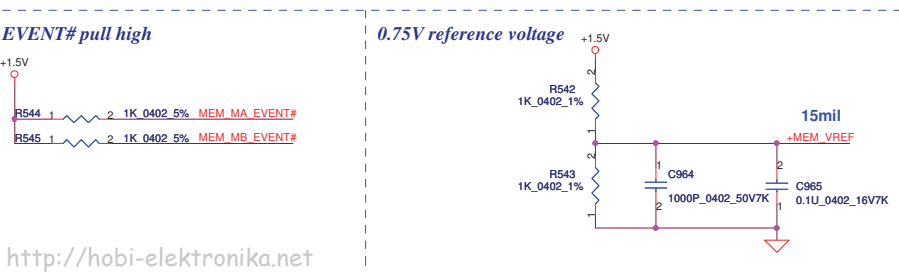
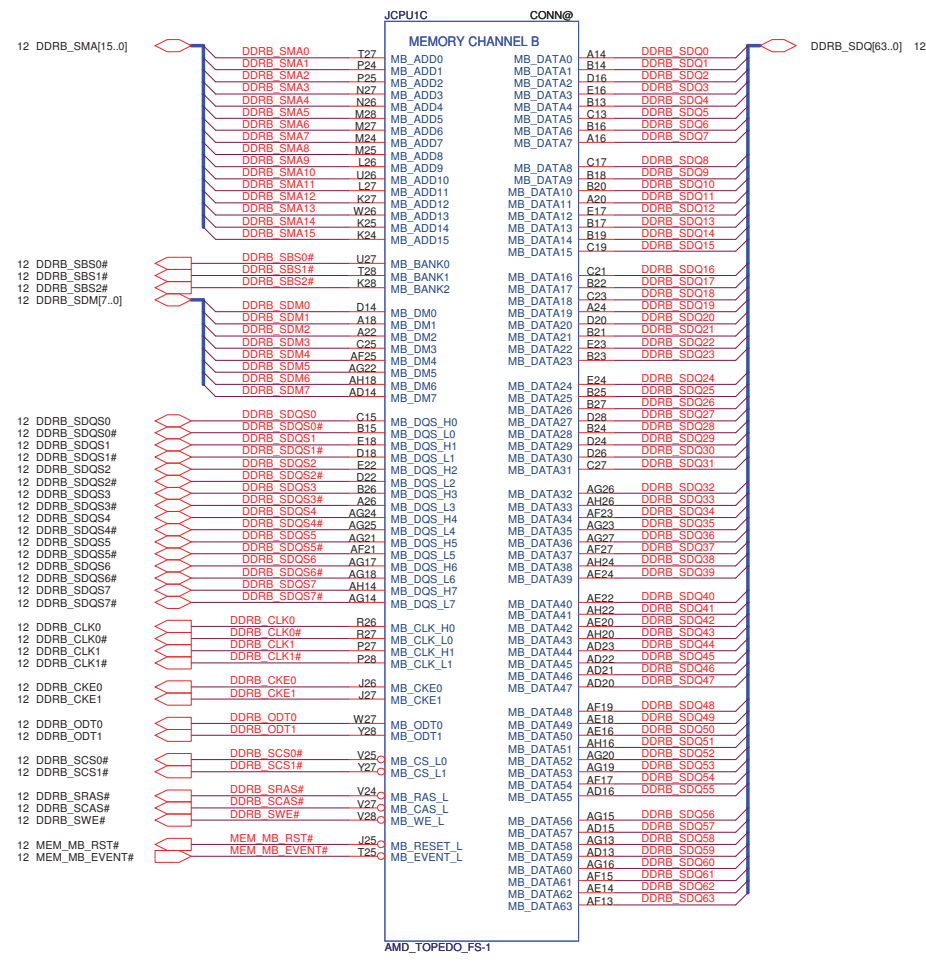
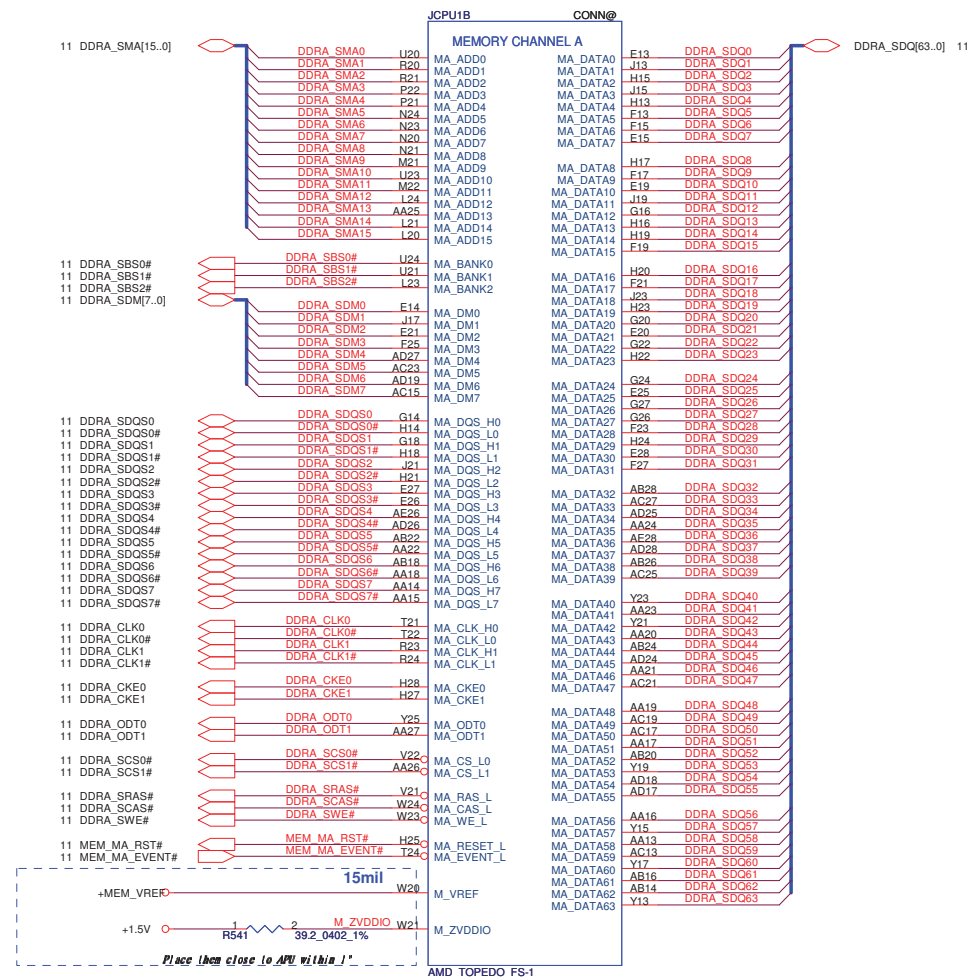
+CPU_CORE_NB

+1.2VS

Group A

Group B

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Issued Date	2010/08/04	Deciphered Date	2011/12/31	Title	AMD FS1 PCIE / UMI / TSI
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				Date	Wednesday, April 27, 2011
				Sheet	6 of 53
				Rev	1.0



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				Custom	1.0
				QBL50 LA-7551P	
				Date	Wednesday, April 27, 2011
				Sheet	7 of 53

To LVDS Translator

To FCH VGA ML

100MHz

100MHz_NSS

TSI

Serial VID

Close to Header

Route as differential with VSS_SENSE

route as differential

route as differential

http://hobi-elektronik.net

Place near APU

Place near APU

System DP

TSI

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

JCPU1D

JCPU1D

System DP

TSI

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

CONN@

CONN@

System DP

TSI

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Place near APU

Place near APU

System DP

TSI

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

Serial VID

To LVDS Translator

To FCH

AUX 2-5 are for GFX interface use, they could be selected to I2C or AUX logic

VDDIO level Need Level shift

VDDIO level Need Level shift

HDMI

VDDIO level Need Level shift

HDMI

VDDIO level Need Level shift

HDMI

VDDIO level Need Level shift

HDMI

VDDIO level Need Level shift

HDMI

VDDIO level Need Level shift

HDMI

VDDIO level Need Level shift

HDMI

VDDIO level Need Level shift

HDMI

VDDIO level Need Level shift

VDDIO level Need Level shift

If not used, pins are left unconnected (DG ref.)

20101111

DP0_AUXP R554 2 1.8K 0402 5%
DP0_AUXN R555 2 1.8K 0402 5%
ML_VGA_AUXP R547 2 1.8K 0402 5%
ML_VGA_AUXN R556 2 1.8K 0402 5%

TEST25_L R548 1 2 510 0402 1%
TEST25_H R557 1 2 510 0402 1%

TEST35 R558 1 2 300 0402 5%
R559 1 @ 2 300 0402 5%

M_TEST R564 1 @ 2 39.2 0402 1%
R567 1 2 39.2 0402 1%

FS1R1 R571 1 2 10K 0402 5%

ALLOW_STOP R612 1 2 1K 0402 5%
APU_RST# R577 1 @ 2 1K 0402 5%
APU_PWRGD R578 1 2 300 0402 5%
APU_PWRGD R580 1 2 300 0402 5%

MISC

Asserted as an input to force the processor into the HTC-active state

APU_PROCHOT# R591 1 2 0.0402 5%
EC_THERM# 13,36,47

APU_THERMTRIP# R615 1 2 1K 0402 5%
H_THERMTRIP# 14

HDT Debug conn

APU_TRST# R598 2 0.0402 5%
R601 1 2 10K 0402 5%
R603 1 2 10K 0402 5%
R605 1 2 10K 0402 5%

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				QBL50 LA-7551P	Rev 1.0
				Date: Wednesday, April 27, 2011	Sheet 8 of 53

HPD

Translator HPD

From Translator



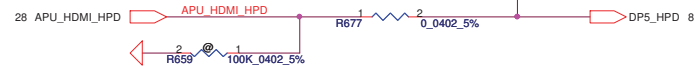
CRT HPD

From FCH

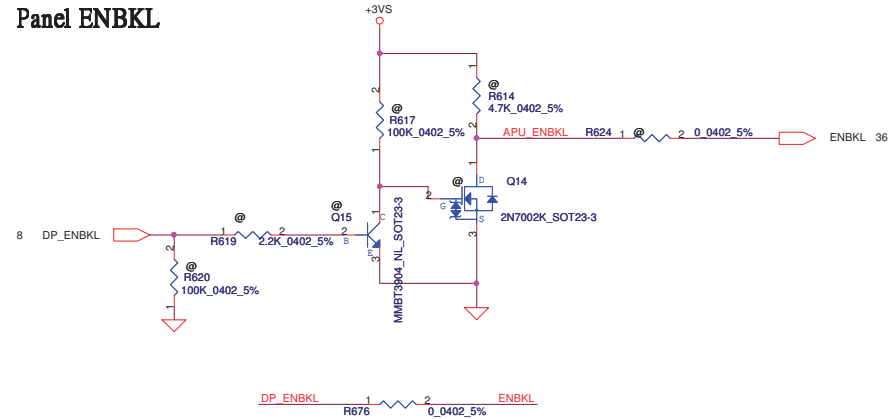


HDMI HPD

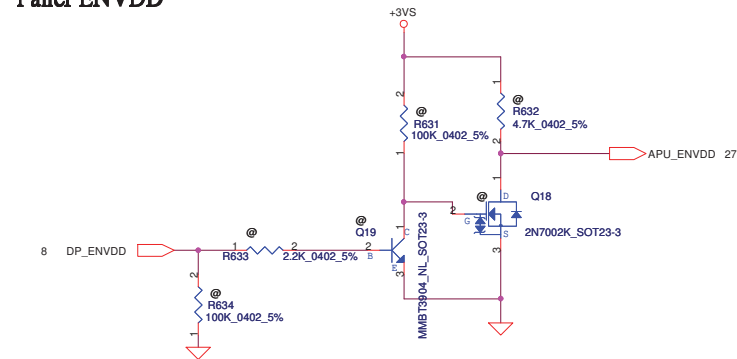
From HDMI Conn



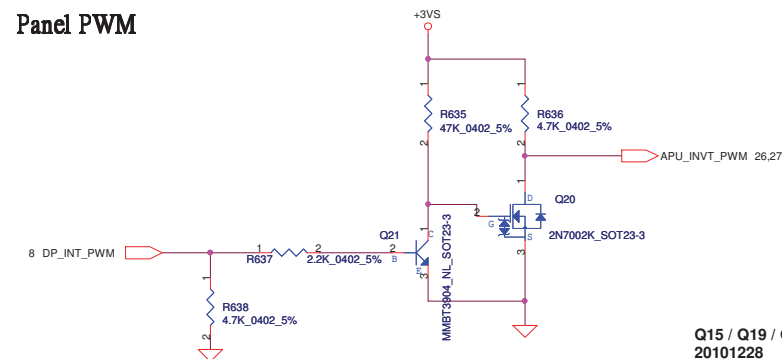
Panel ENBKL



Panel ENVDD

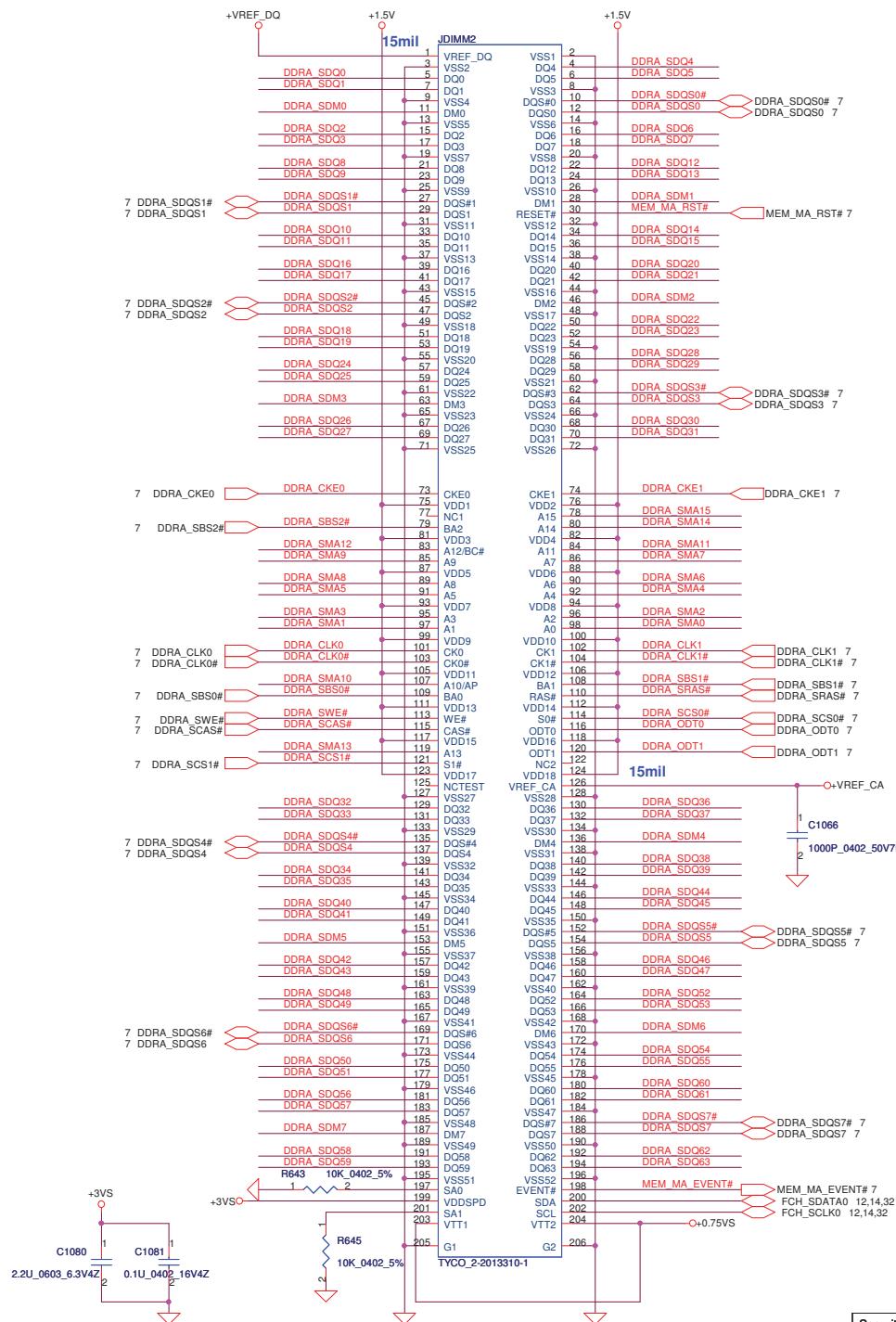


Panel PWM



Q15 / Q19 / Q21 change to SB000006A00
20101228

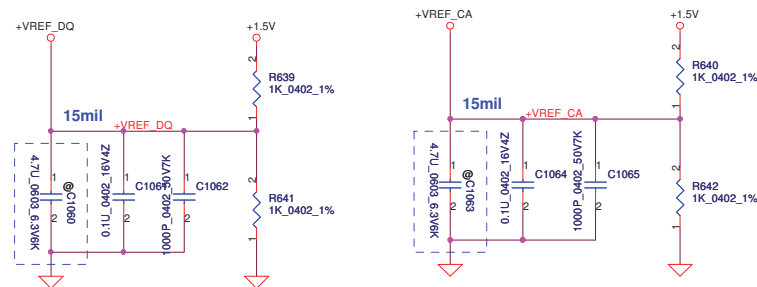
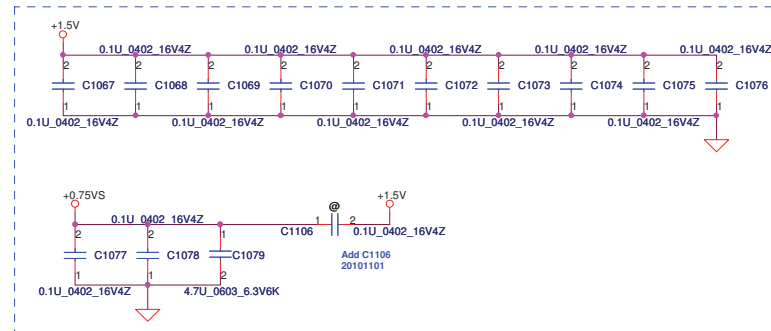
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Issued Date	2010/08/04	Deciphered Date	2011/12/31	Title AMD FS1 Singal Level Shifter		
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				QBL50 LA-7551P		
				Date	Wednesday, April 27, 2011	Sheet



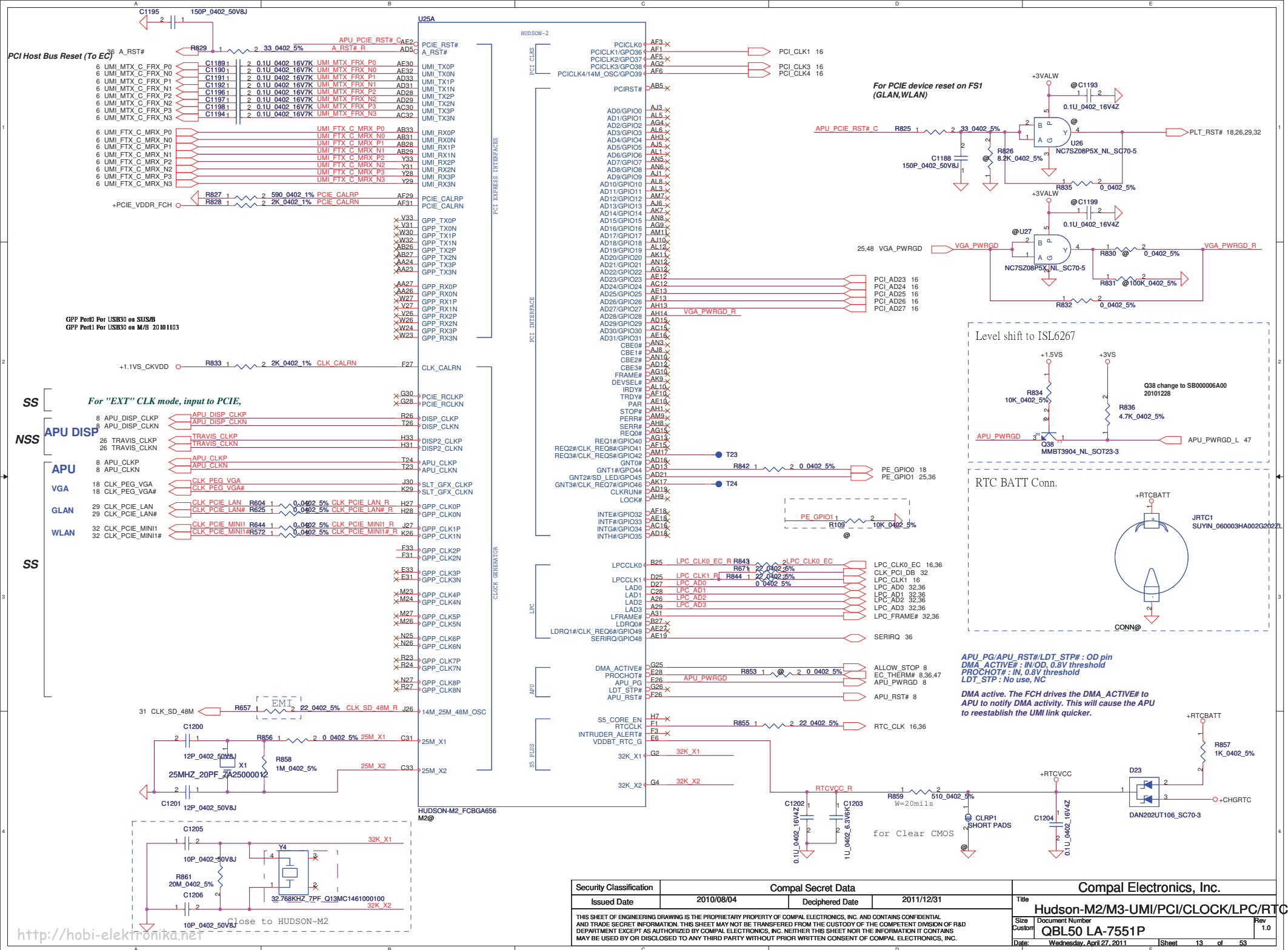
DIMM_A STD H:9.2mm
 <Address: 00>

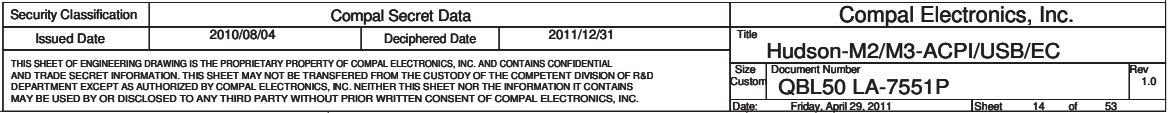
DDRA_SDQ[0.63] DDRA_SDQ[0.63] 7
 DDRA_SDM[0.7] DDRA_SDM[0.7] 7
 DDRA_SMA[0.15] DDRA_SMA[0.15] 7

Place near DIMM1



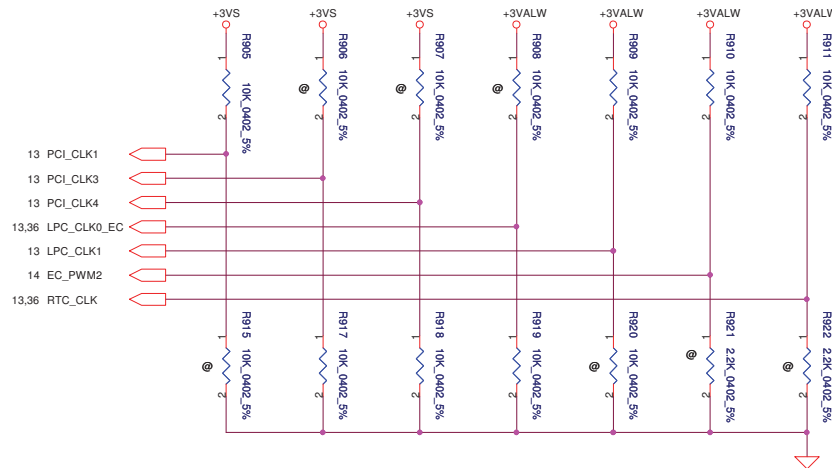
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Custom	QBL50 LA-7551P	1.0		Wednesday, April 27, 2011	
Sheet		11		of	
53					





STRAP PINS

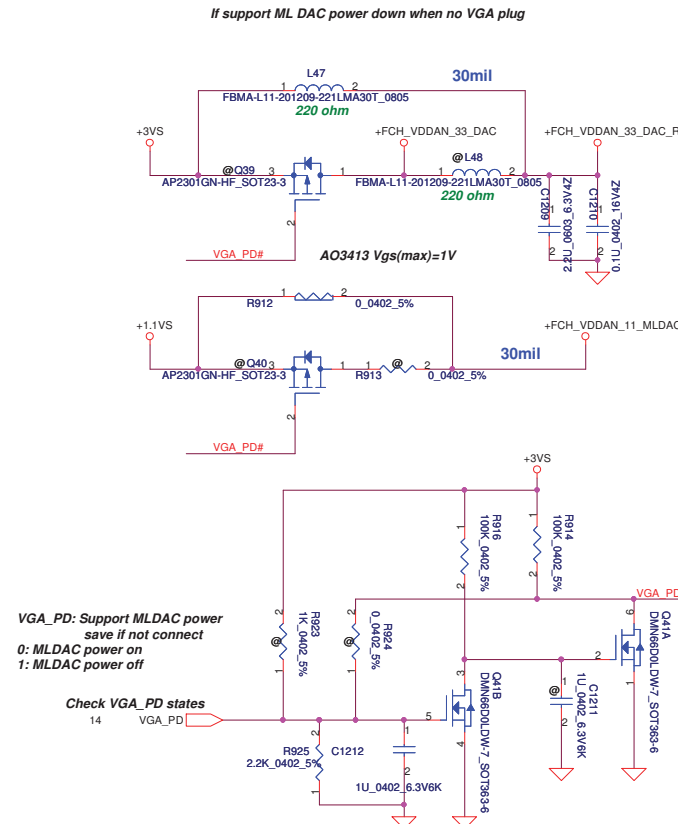
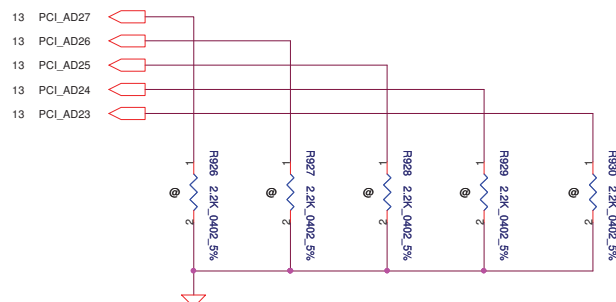
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM2 DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED



DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26		PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
	PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
	PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

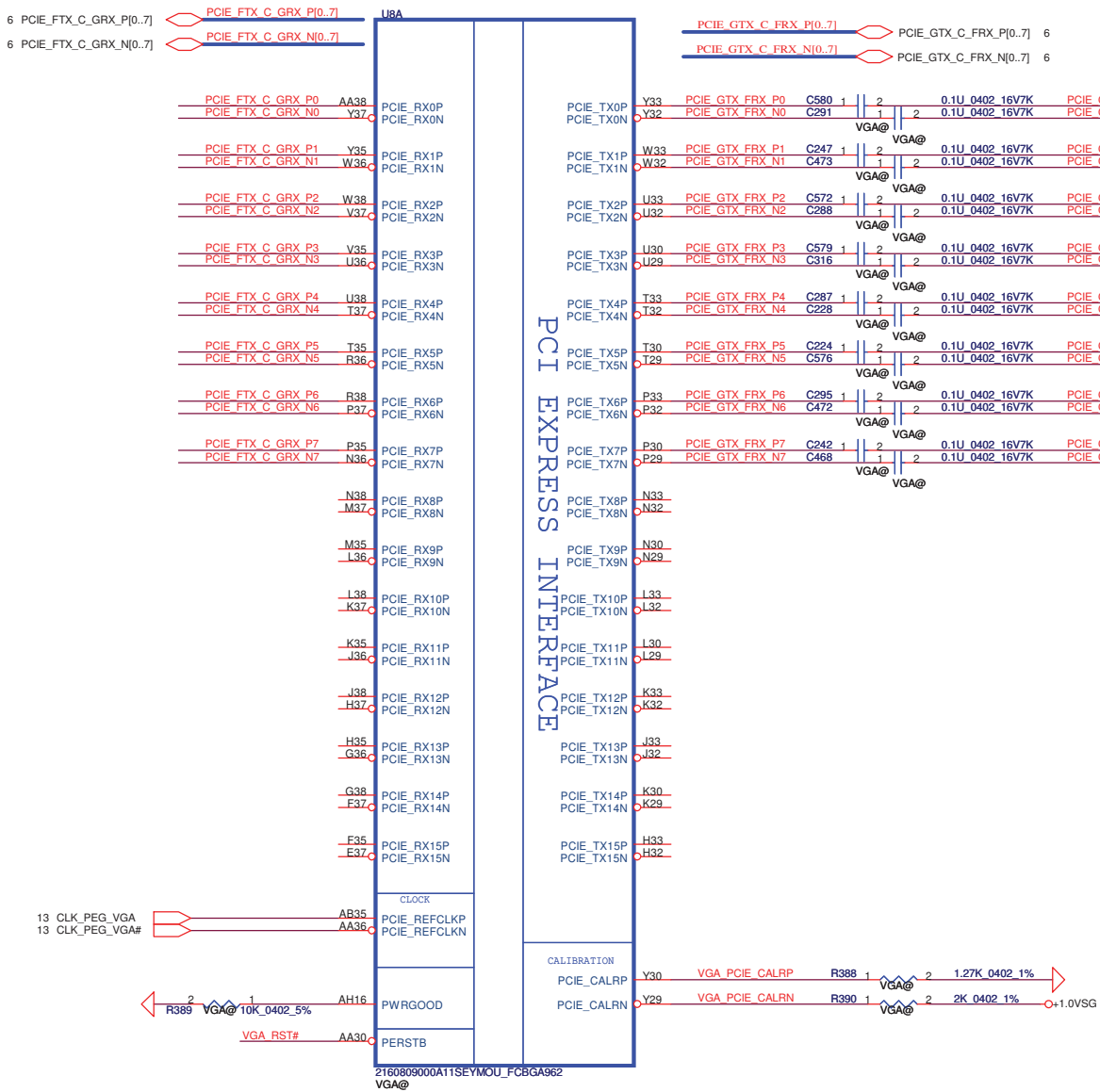




Connected to VSS through a dedicated via.

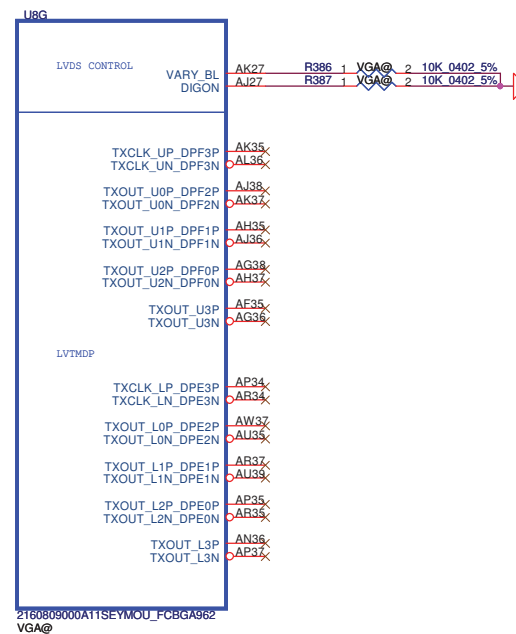
<http://hobi-elektronika.net>

GFX PCIE LANE REVERSAL

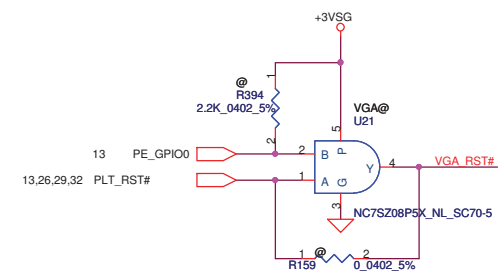


<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High ,external PD need



For UMA Mux.



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				Customer	QBL50 LA-7551P
				Date:	Wednesday, April 27, 2011
				Sheet	18 of 53

Strap Name	Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNCK (GENLK_VSYNCK) VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHA0_0 during reset 1: VHA0_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPI09 VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPI00 Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	GPI01 PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPI013 GPIO13,12,11 (config 2,1,0) : (Internal PD) a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. memory apertures CONFIG[3:0] 128 MB 000	001
CONFIG[1]	GPI012	
CONFIG[0]	GPI011	
BIOS_ROM_EN	GPI022 Enable external BIOS ROM device (Internal PD) 0: Disable, 1: Enable	0
AUD[1]	HSYNCK 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
AUD[0]	VSYNCK	
BIF_GEN2_EN	GPI02 0: Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNCK GPI08 GPI021 Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

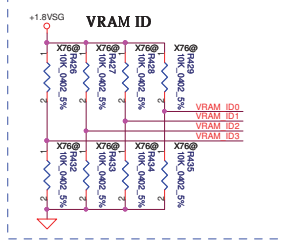
Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

Move to DDCLKL_AUX3P.DCDDATA_AUX3N, AK28



GPI05 fast-power reduction:
HW control will cause display disturb
should use SW method control
GPI06 voltage control signal, No use can NC!

GPI07 Controls backlight on/off.
Active High, need external PD
If GPI022 High, GPI0 11-13->CFG[0:2]
Config ROM type, GPU has internal PD

GPI06,15,16,20
Voltage control signal
GPI06,15 no use can NC
Thermal monitor interrupt

Critical temperature fault

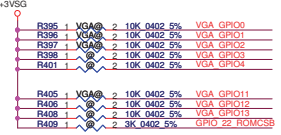
Reserved

External BIOS device
ON(1)/OFF(0) Inter PD

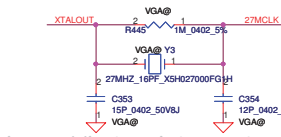
Internal Debug
no use can floating
ON(1)/OFF(0)

Stereo Sync
no use can NC

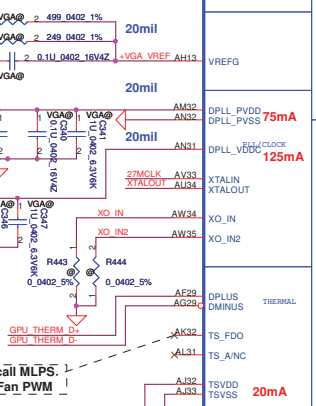
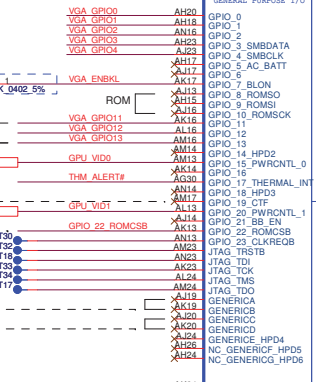
For ATI Cross fire
no use can NC



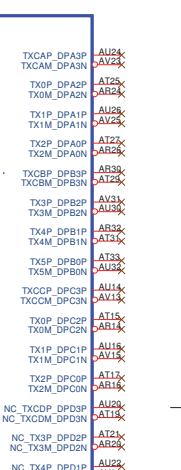
VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung BA100146350 K4M1G16460-BC11		0	0	0	0
Samsung BA0000470A0 K4M2G16460-BC11		0	0	0	1
Hynix BA100041560 H5TQ1G63DFR-11C		0	1	0	0
Hynix BA000039030 H5TQ2G63BFR-11C		0	1	0	1



http://hobi-elektronik.net

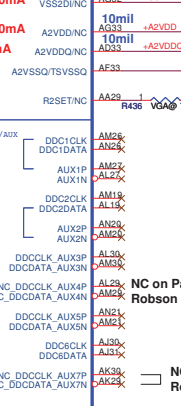
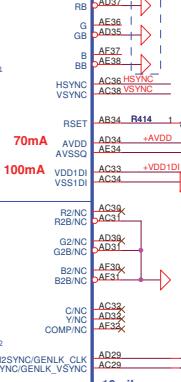


Future ASIC call MLPS.
OLD ASIC is Fan PWM



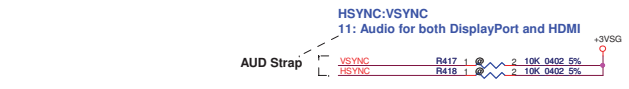
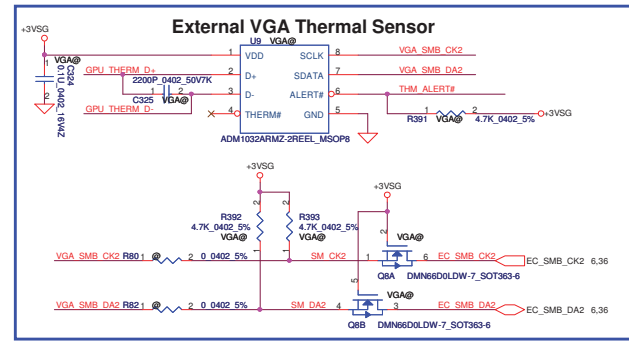
NC on Park, Robson and Seymour

Not share via for other GND



NC on Park, Robson and Seymour

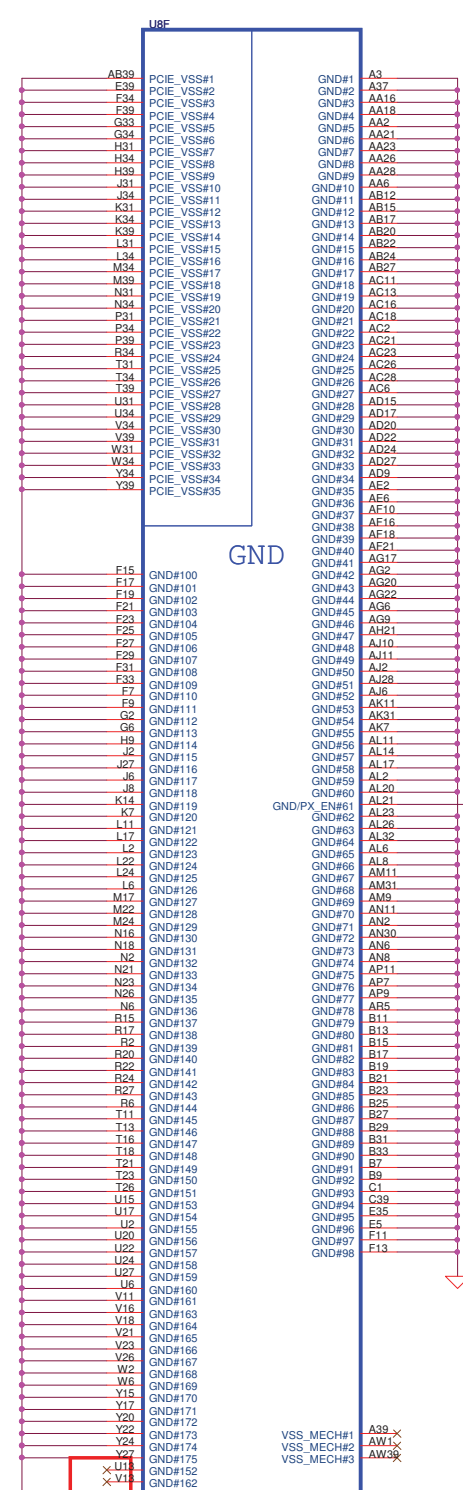
NC on Park, Robson and Seymour



NC on Whistler and Seymour

Whistler and Seymour
Except A2VSSQ change to TSVSSQ,
others are NC

GPI08 Serial-ROM output from ROM
GPI09 Serial-ROM input to ROM.
GPI010 Serial-ROM clock to ROM.
GPI022 external BIOS-ROM enable
if GPI022 High, GPI0 11-13->CFG[0:2]
Config ROM type, GPU has internal PD
if GPI022 Low, GPI0 11-13->CFG[0:2]
Config Primary memory-aperture size
CFG[3:0] 128MB 000
256MB 001 *
64MB 010



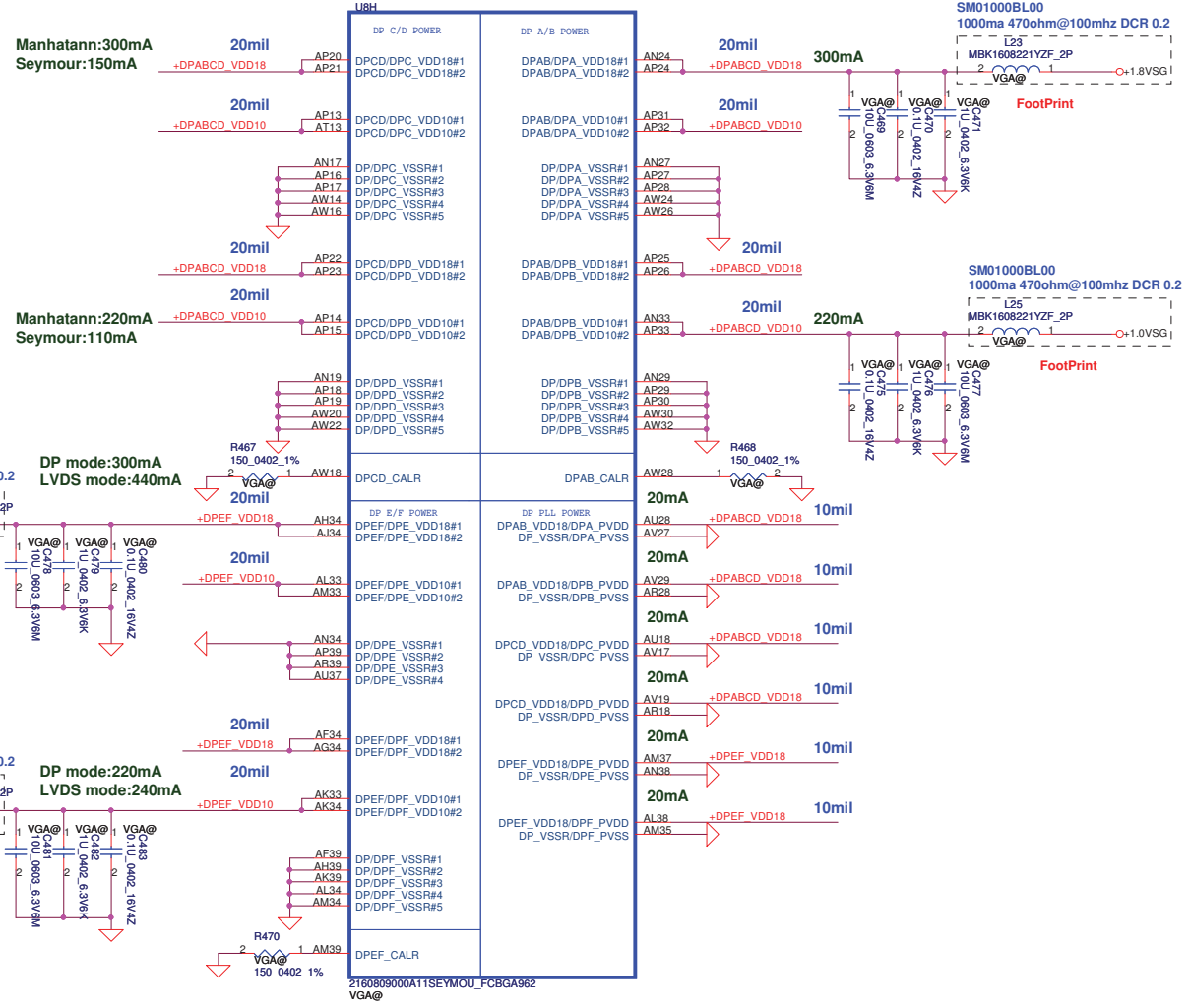
DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

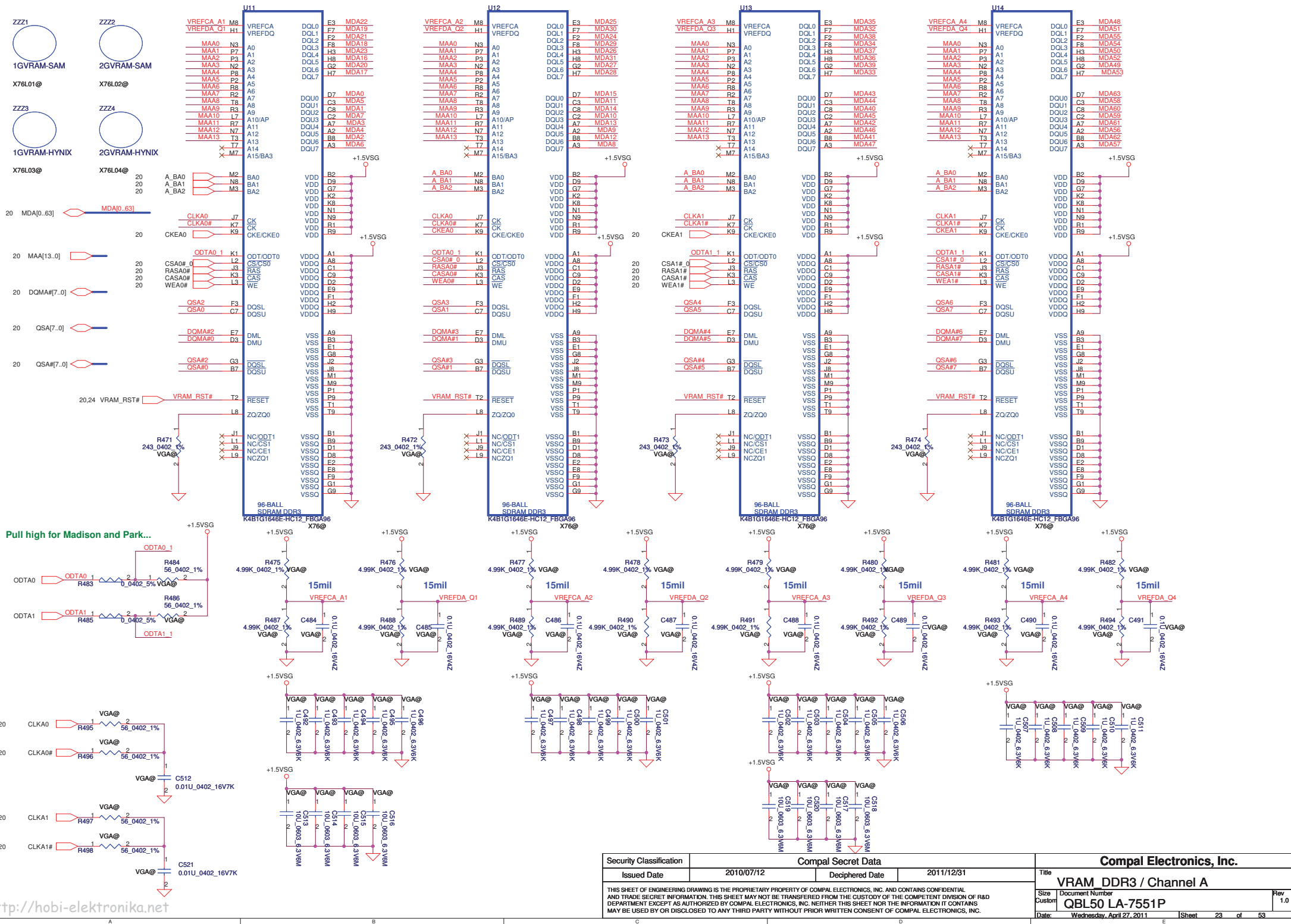
Seymour/Whistler :
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

Park/Madison :AL21:left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

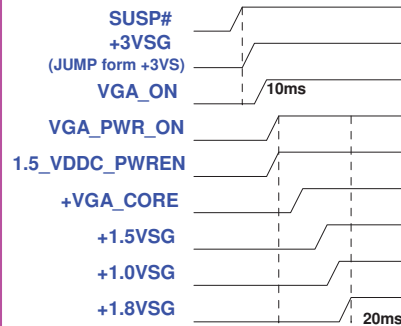


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				Date:	Wednesday, April 27, 2011	Sheet	22	of 53		

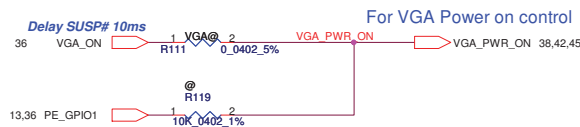
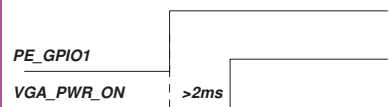




Power Sequence of Whistler and Seymour



For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

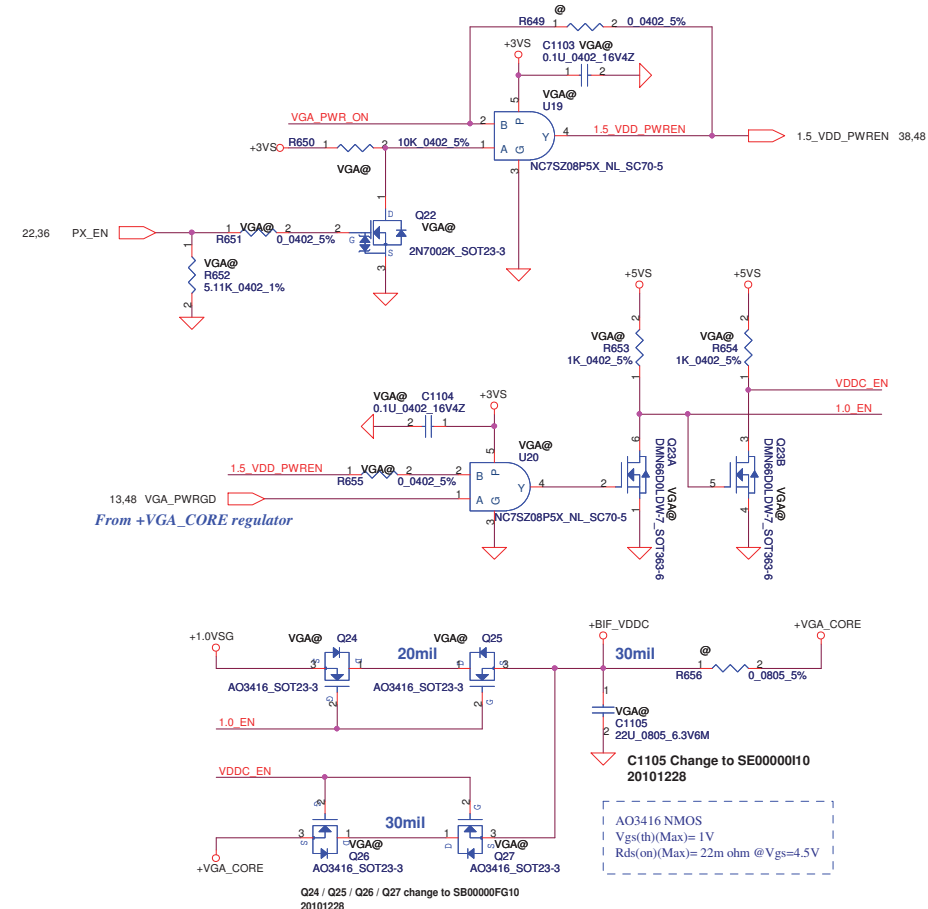


VGA Muxless with BACO Status Mapping table

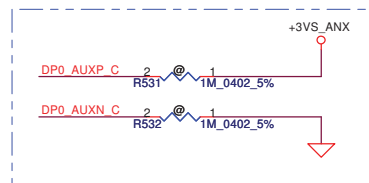
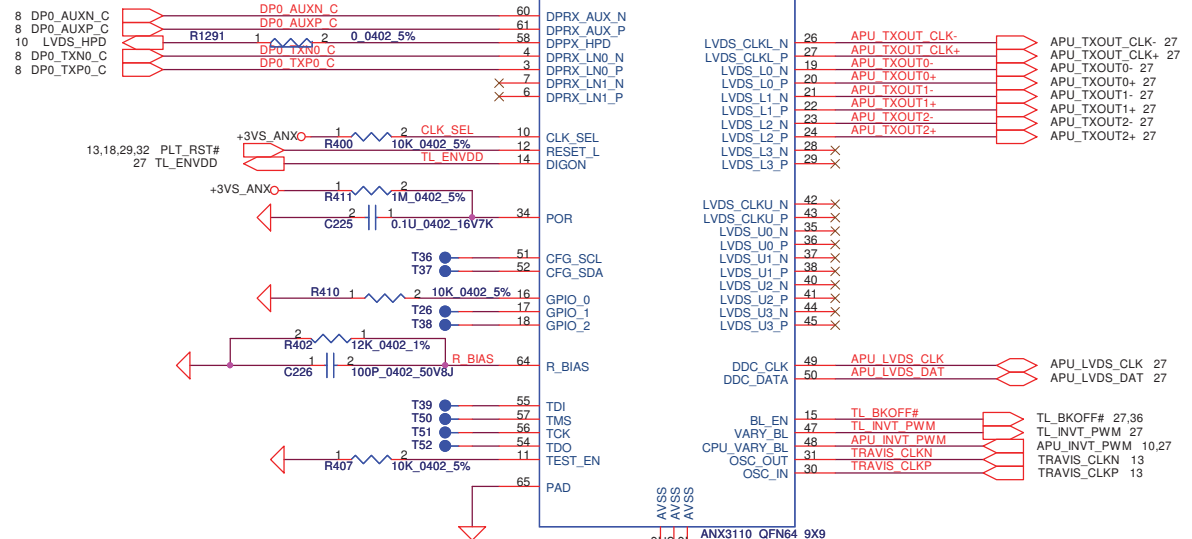
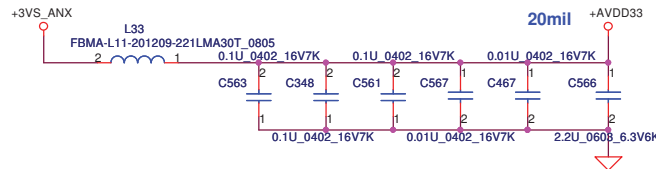
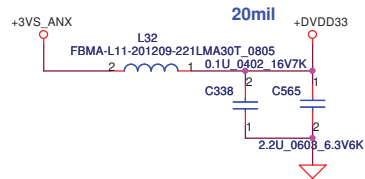
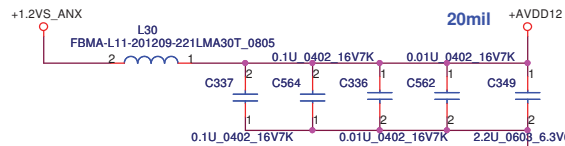
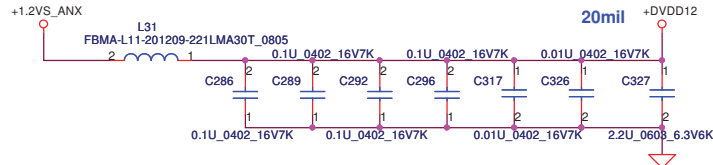
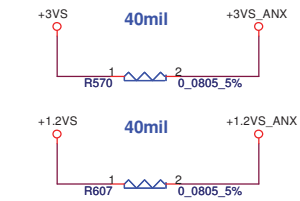
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table

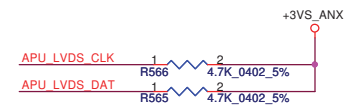
VGA_PWR_ON source signal	Whistler
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN



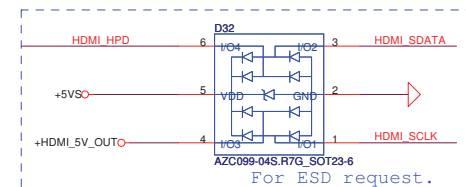
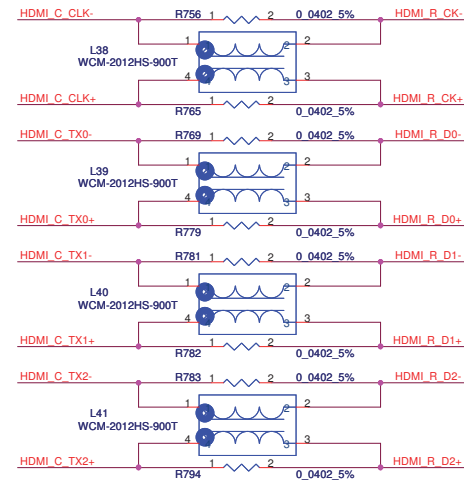
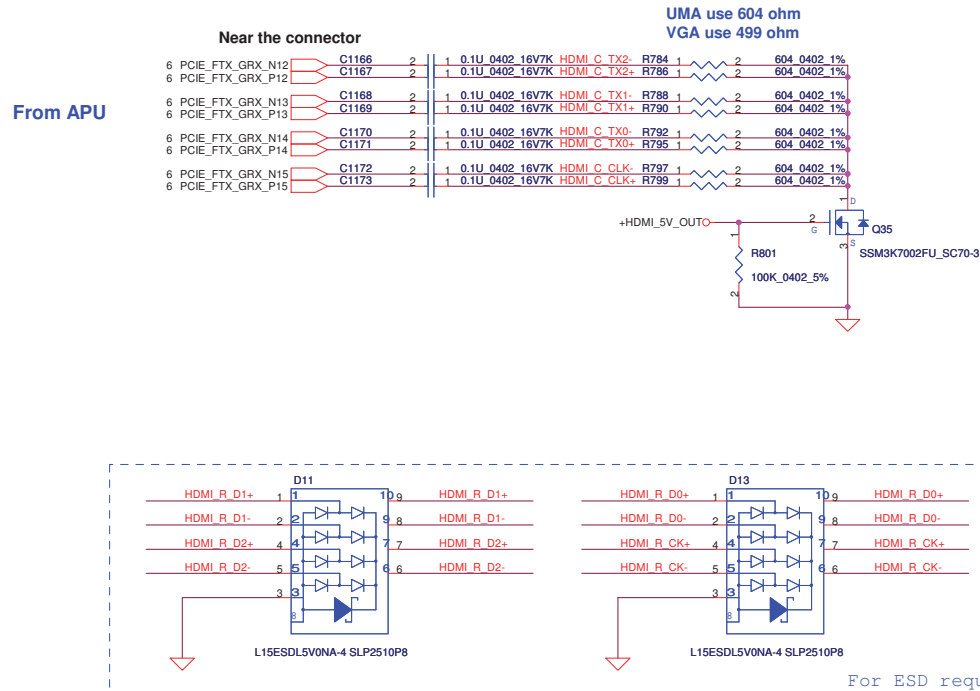
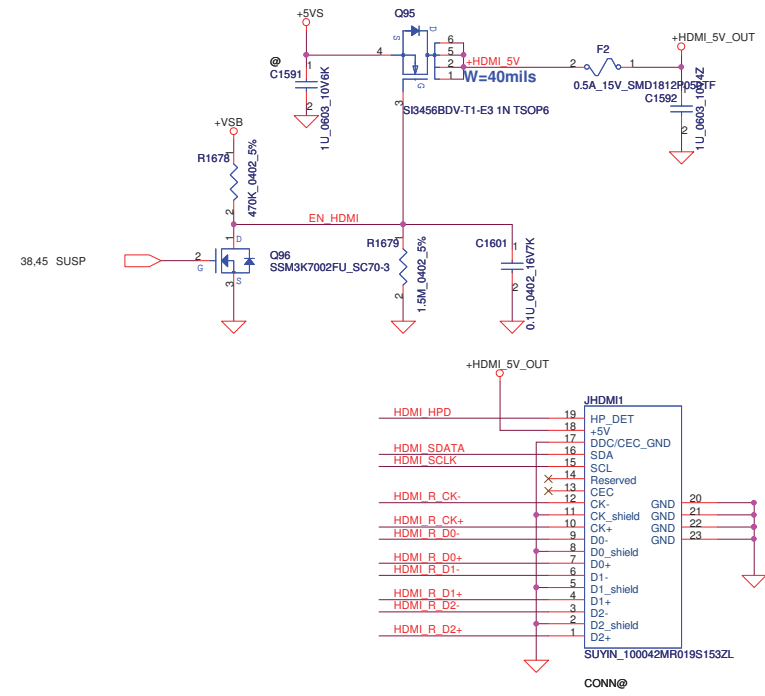
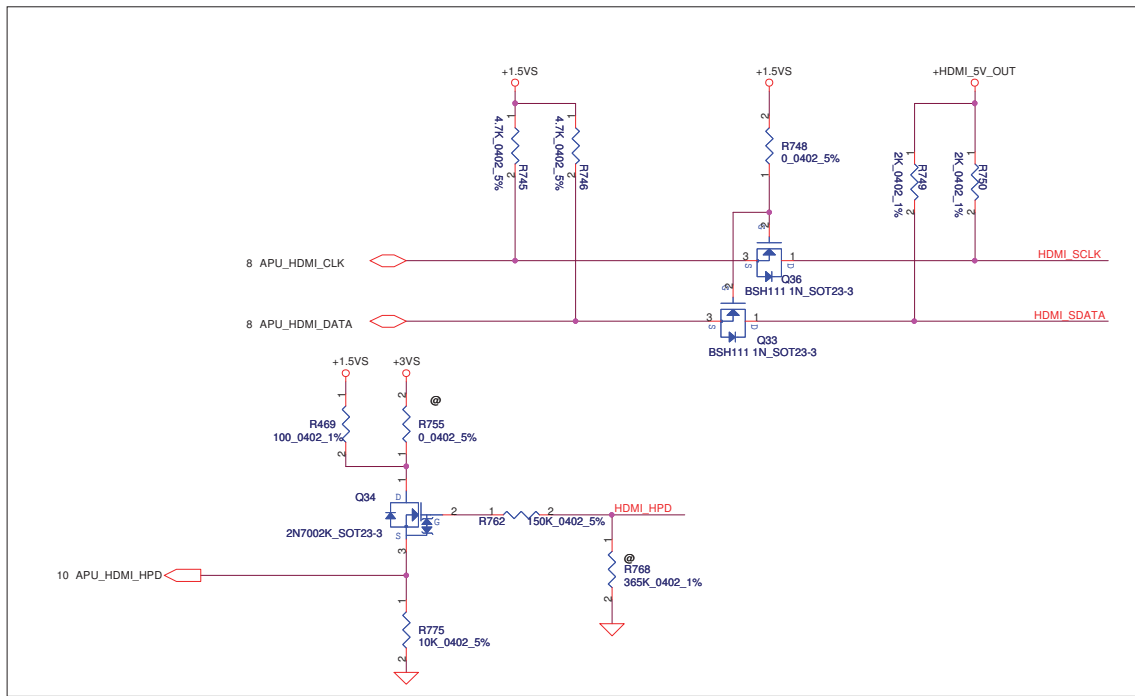
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Issued Date				2010/08/04				Title			
Deciphered Date				2011/12/31				VGA power sequence and BACO			
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				QBL50 LA-7551P				Rev			
				Date: Wednesday, April 27, 2011				Sheet 25 of 53			



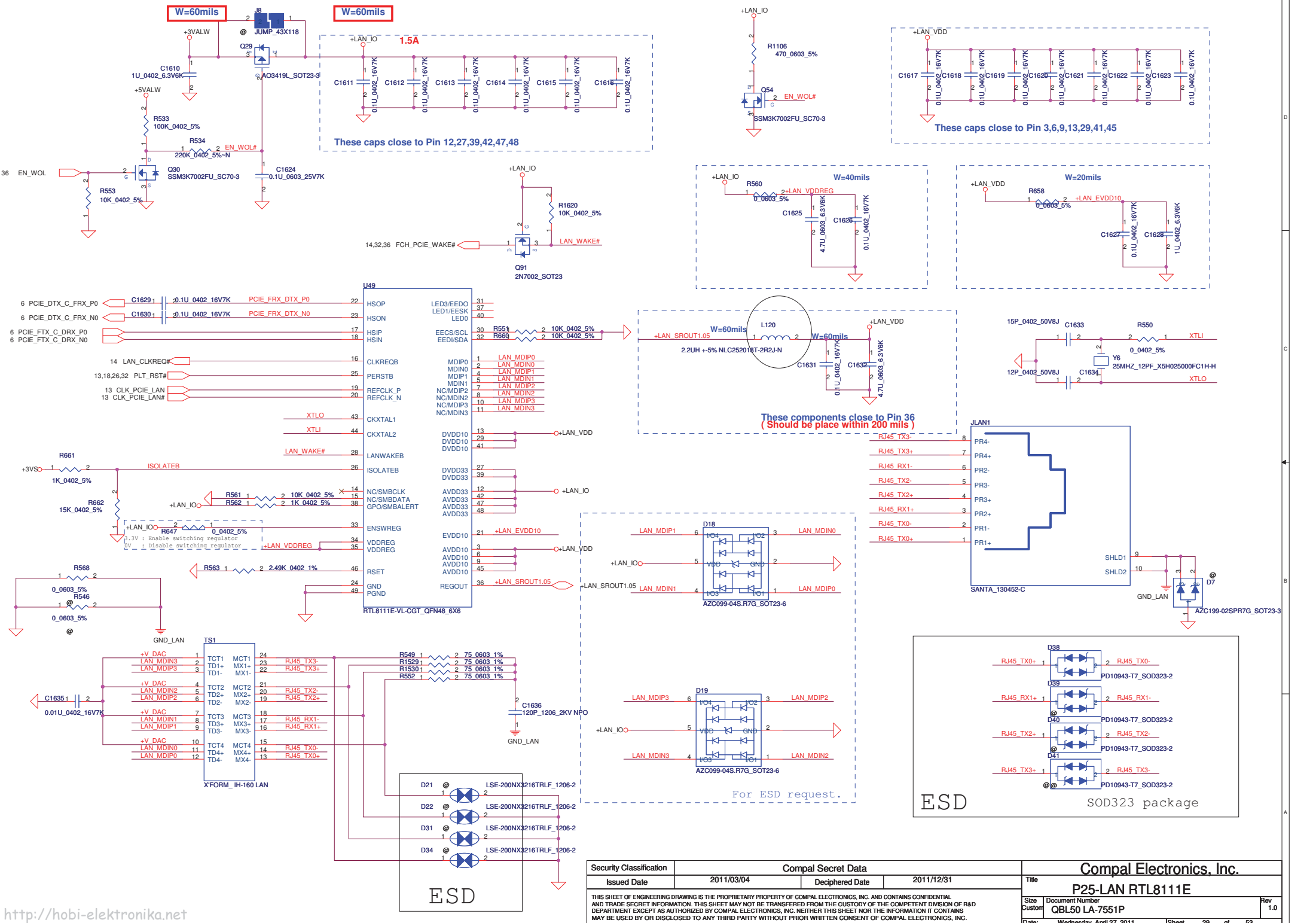
Place via on each trace bus and let resistor very close the via



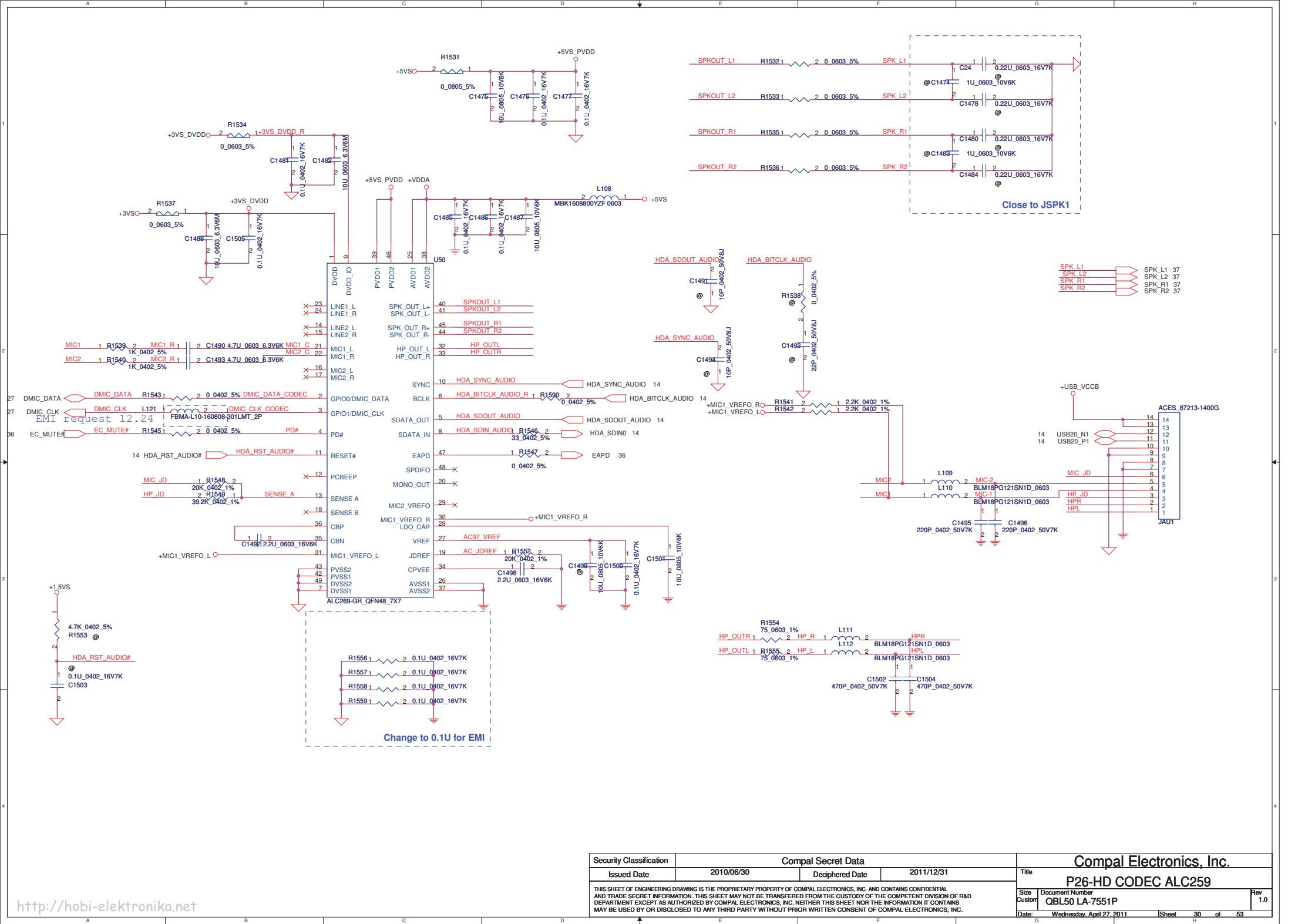
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Date	Wednesday, April 27, 2011	Sheet	26	of 53	



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				QBL50 LA-7551P	Wednesday, April 27, 2011
				1 Sheet	28 of 53



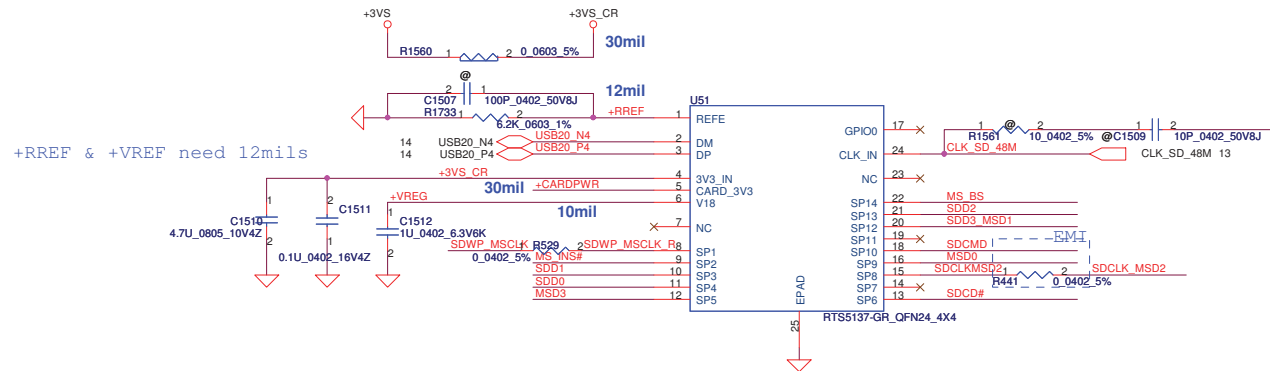
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Size	Customer	Document Number	Rev	Date	
		QBL50 LA-7551P	1.0	Wednesday, April 27, 2011	
		Sheet		29 of 53	



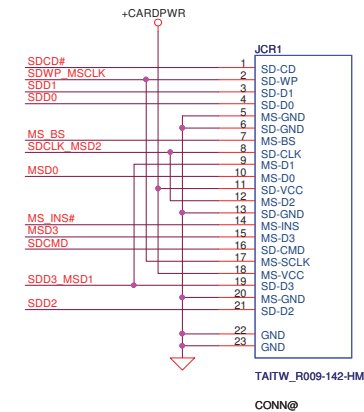
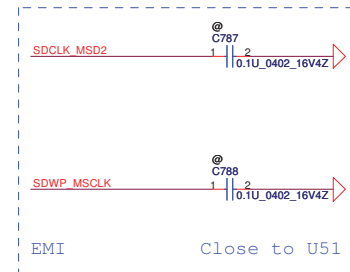
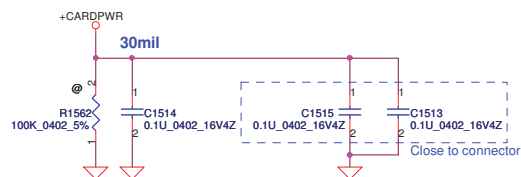
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/06/30				P26-HD CODEC ALC259			
Deciphered Date				2011/12/31				QBL50 LA-7551P			
Title				QBL50 LA-7551P				Rev 1.0			
Date				Wednesday, April 27, 2011				Sheet 30 of 53			

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Card Reader RTS5137
(only SD/MMC/MS function)



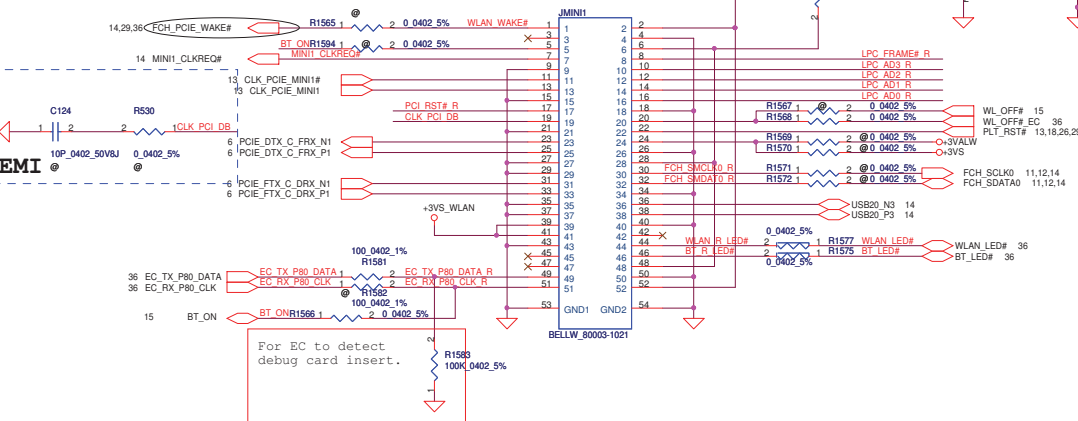
Card Reader Connector



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				Custom	1.0
				Document Number QBL50 LA-7551P	
Date: Wednesday, April 27, 2011				Sheet	31 of 53

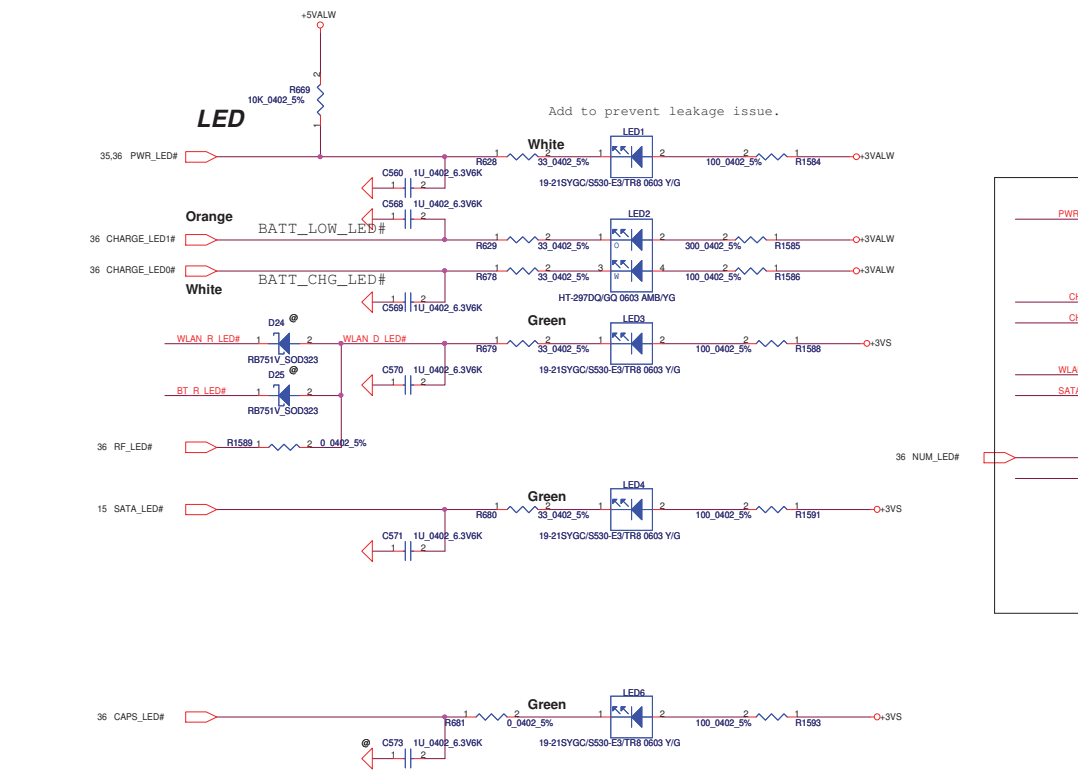
Mini-Express Card for WLAN/WiMAX(Half)

Mini-Express Card(WLAN/WiMAX)



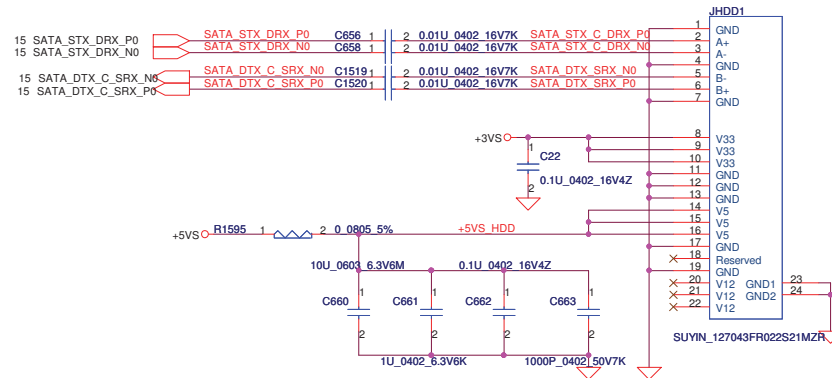
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R1573	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME#	13.36
LPC_AD3 R	R1574	1	2	0.0402 5%	LPC_AD3	LPC_AD3	13.36
LPC_AD2 R	R1576	1	2	0.0402 5%	LPC_AD2	LPC_AD2	13.36
LPC_AD1 R	R1578	1	2	0.0402 5%	LPC_AD1	LPC_AD1	13.36
LPC_AD0 R	R1579	1	2	0.0402 5%	LPC_AD0	LPC_AD0	13.36
PCI_RST# R	R1580	1	2	0.0402 5%	PLT_RST#	PLT_RST#	13.36
CLK_PCI_DB					CLK_PCI_DB	CLK_PCI_DB	13

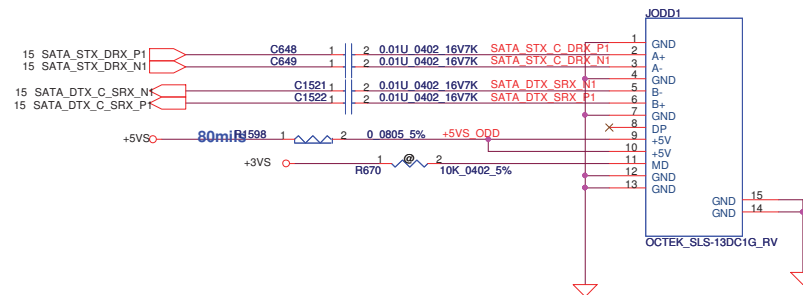


ESD

SATA HDD Conn.



SATA ODD FFC Conn.



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				QBL50 LA-7551P	
				Date: Wednesday, April 27, 2011	Rev 1.0
				Sheet 33 of 53	

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P29-HDD & ODD CONN

Size B

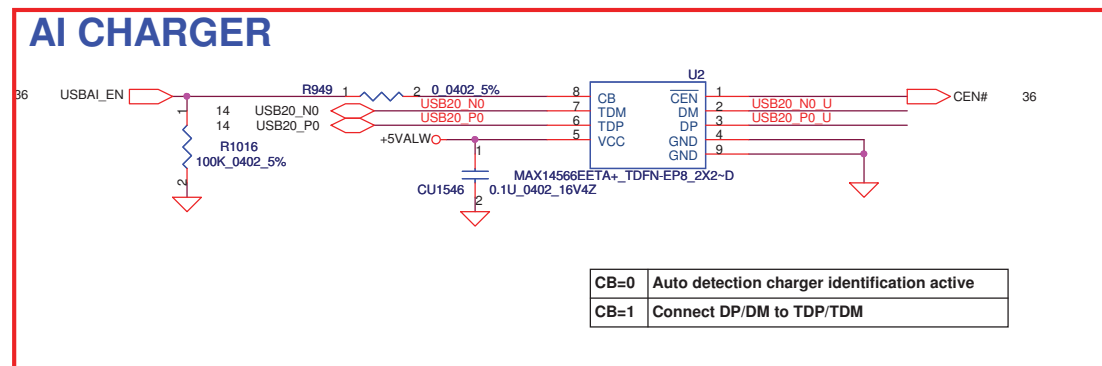
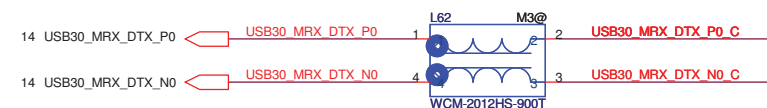
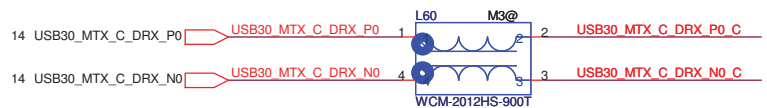
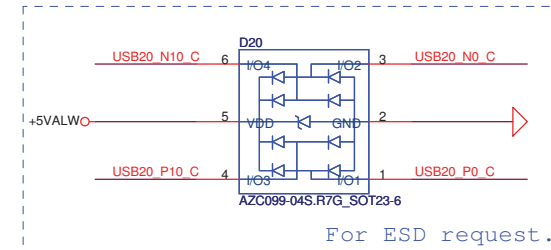
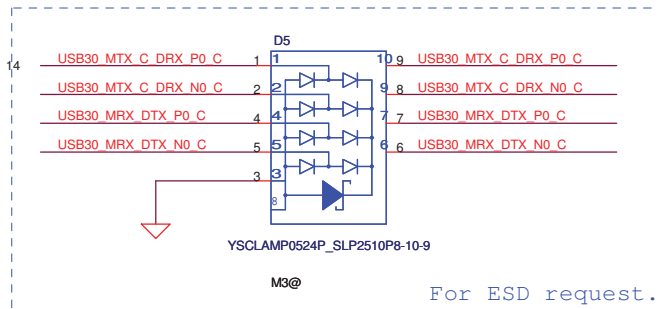
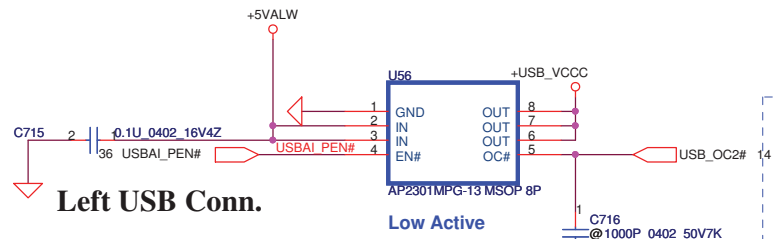
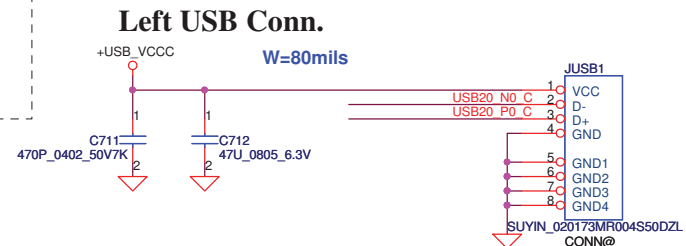
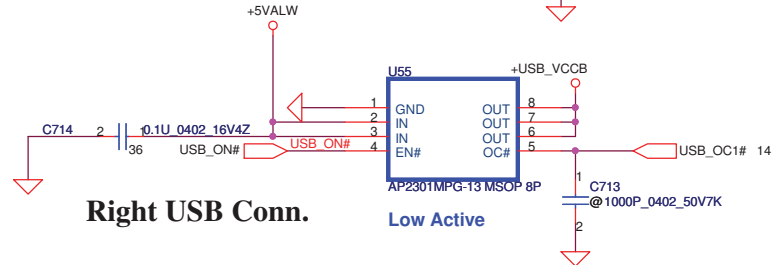
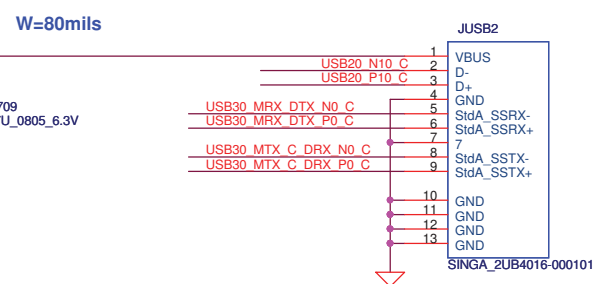
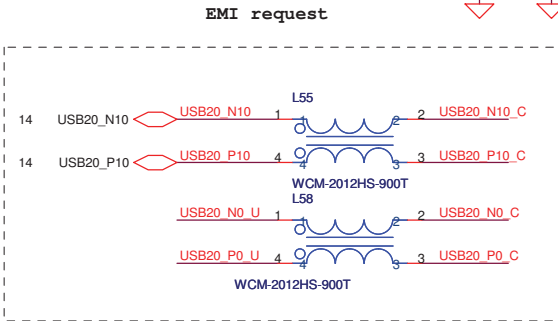
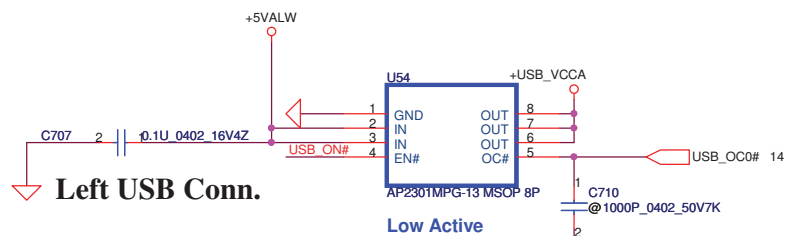
Document Number

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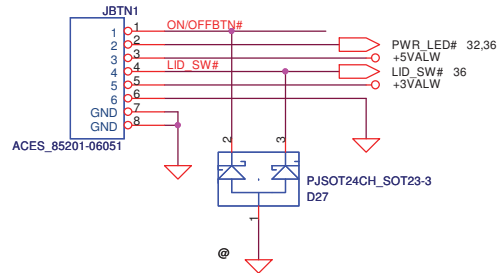
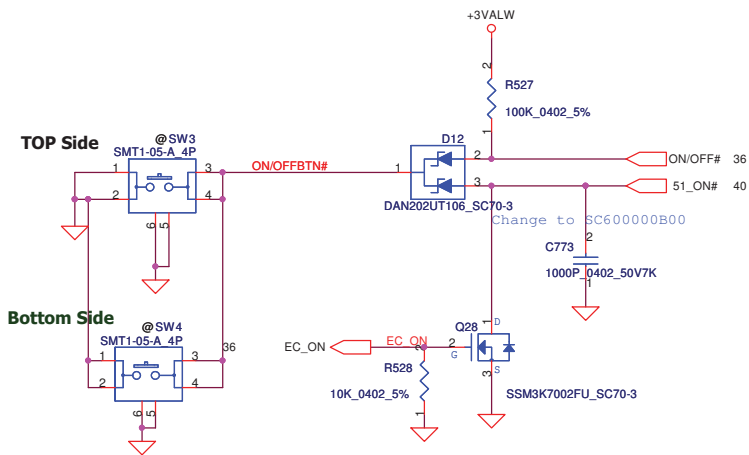
Date: Wednesday, April 27, 2011

Sheet 33 of 53

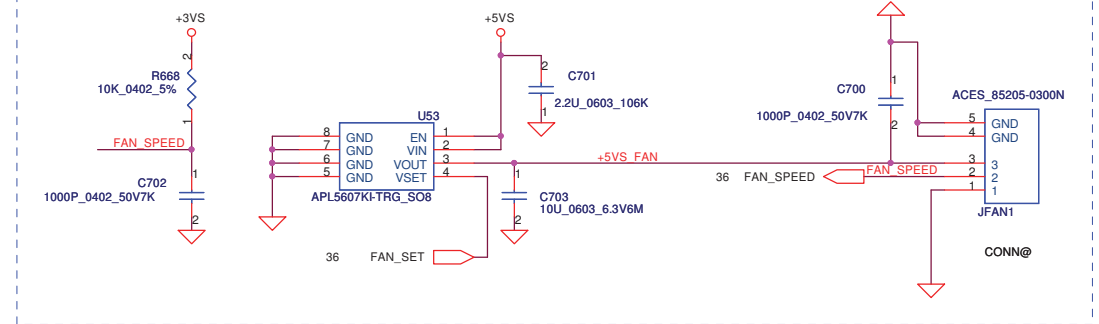


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Custom		QBL50 LA-7551P		1.0	
Date:		Friday, April 29, 2011		Sheet 34 of 53	

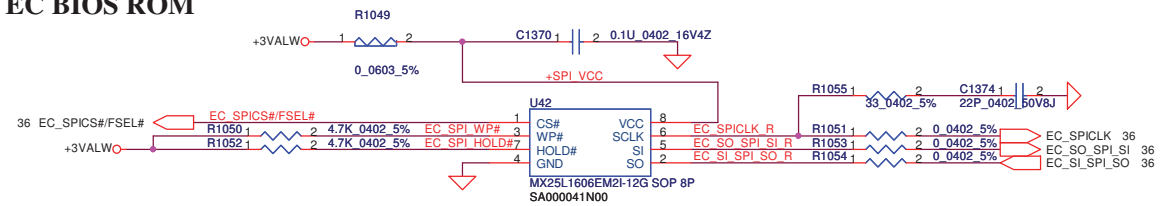
ON/OFF switch **Power Button**



Fan Control Circuit



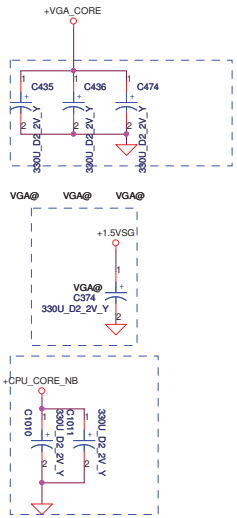
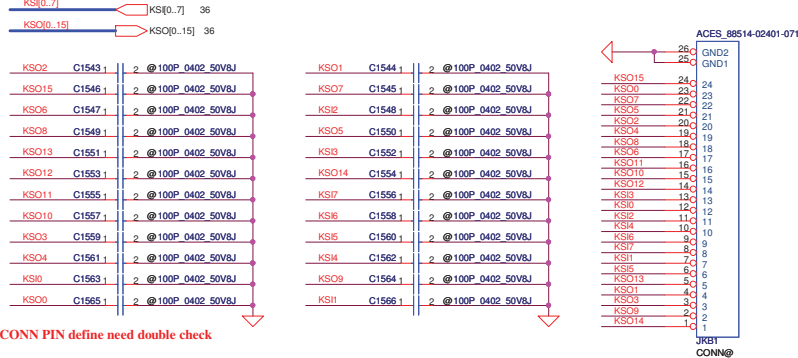
EC BIOS ROM



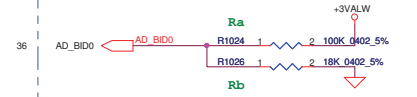
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				Date: Wednesday, April 27, 2011	Sheet 35 of 53



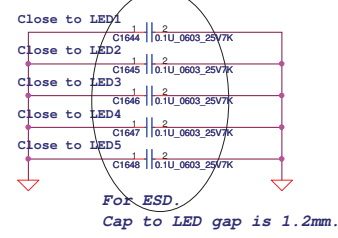
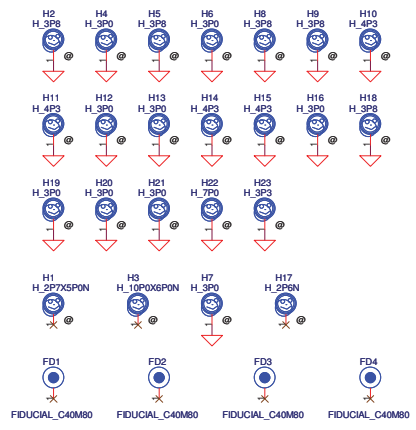
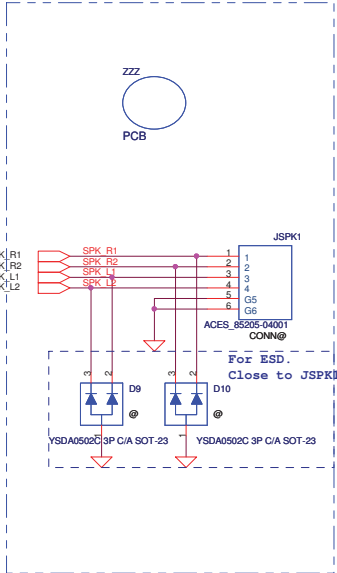
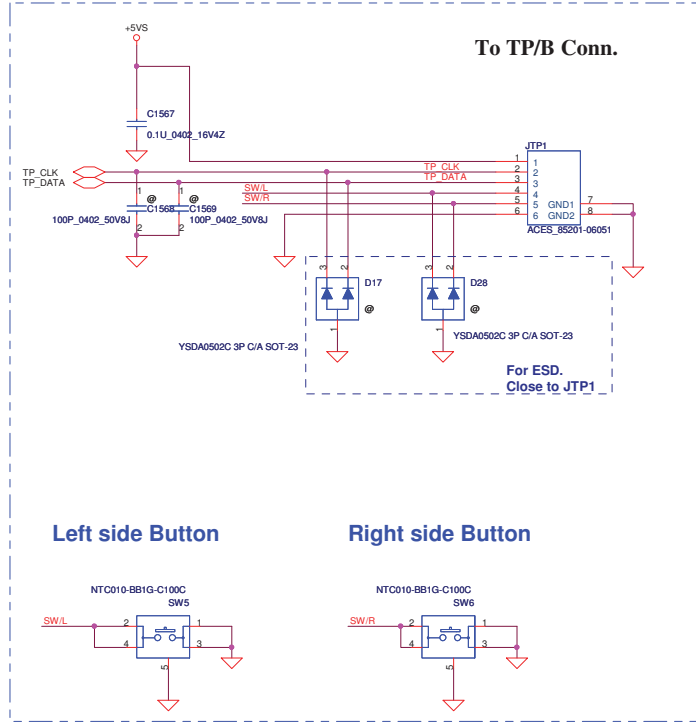
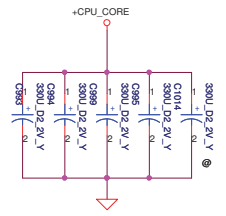
INT_KBD Conn.



ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R10 MP	100K	18K	0.5V
3	Reserve	100K	33K	0.82V

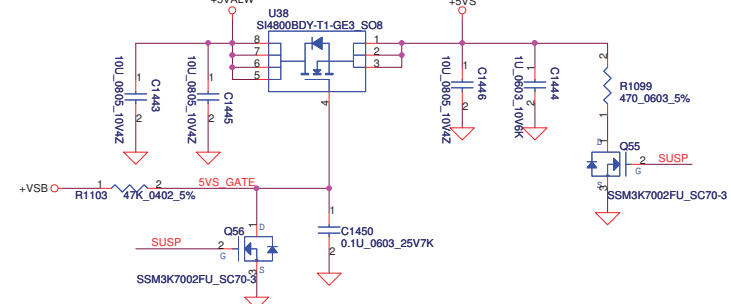


P9 FS1 PWR/GND

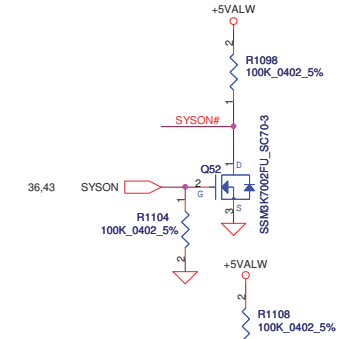
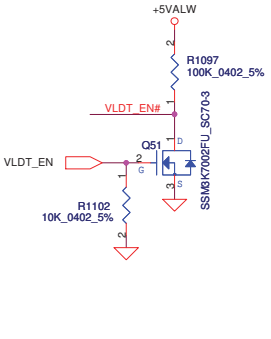
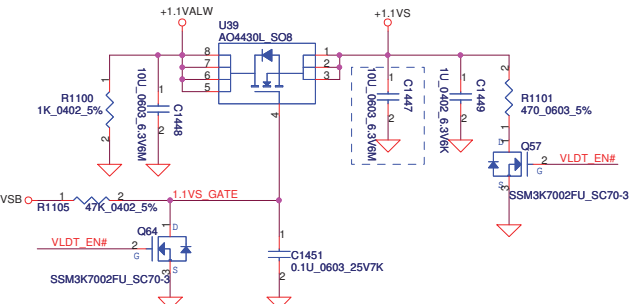


Note: Differential page:
P1,P2,P9,P29,P37
And Power schematic.

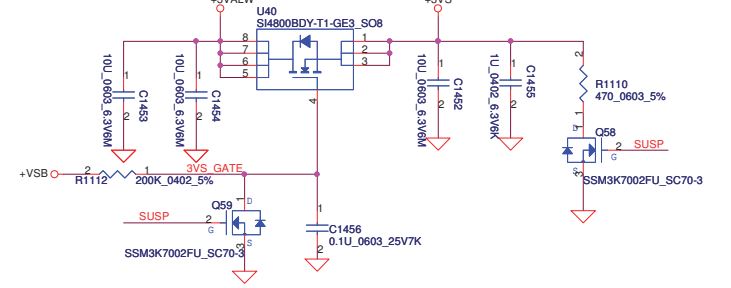
+5VALW TO +5VS (5A)



+1.1VALW TO +1.1VS (1.1A)

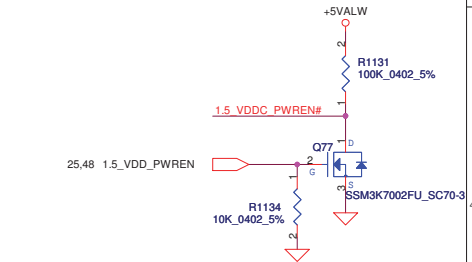
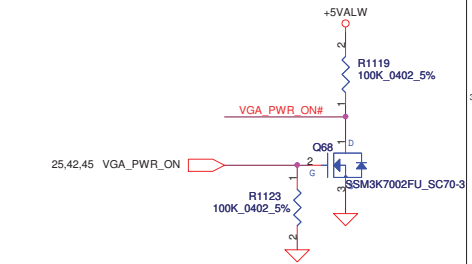
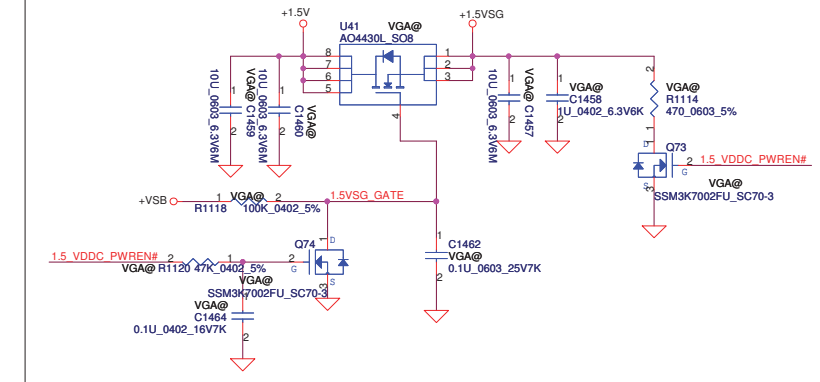


+3VALW TO +3VS (3.3A)

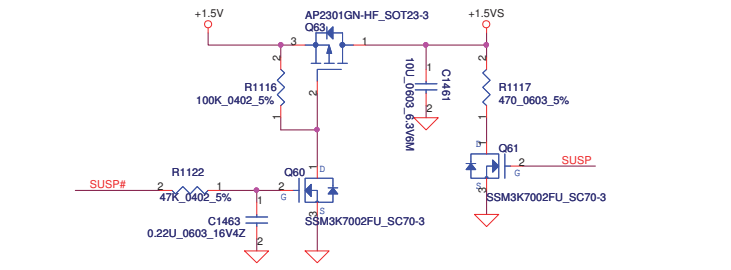


VGA Power

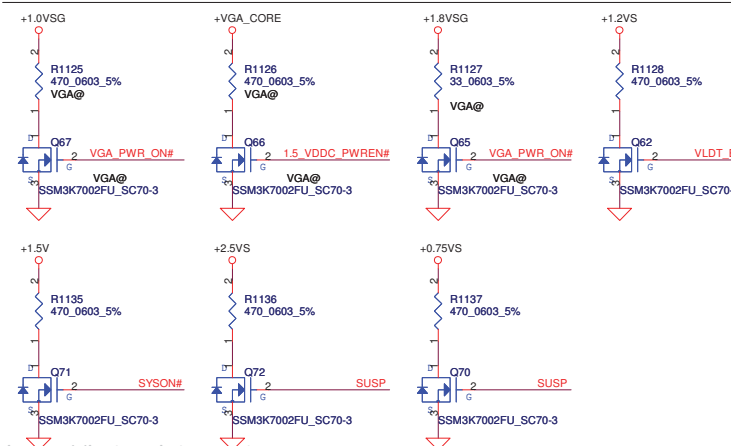
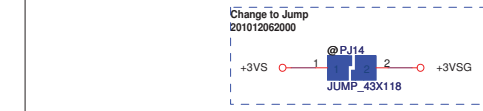
+1.5V to +1.5VSG (1.5A)



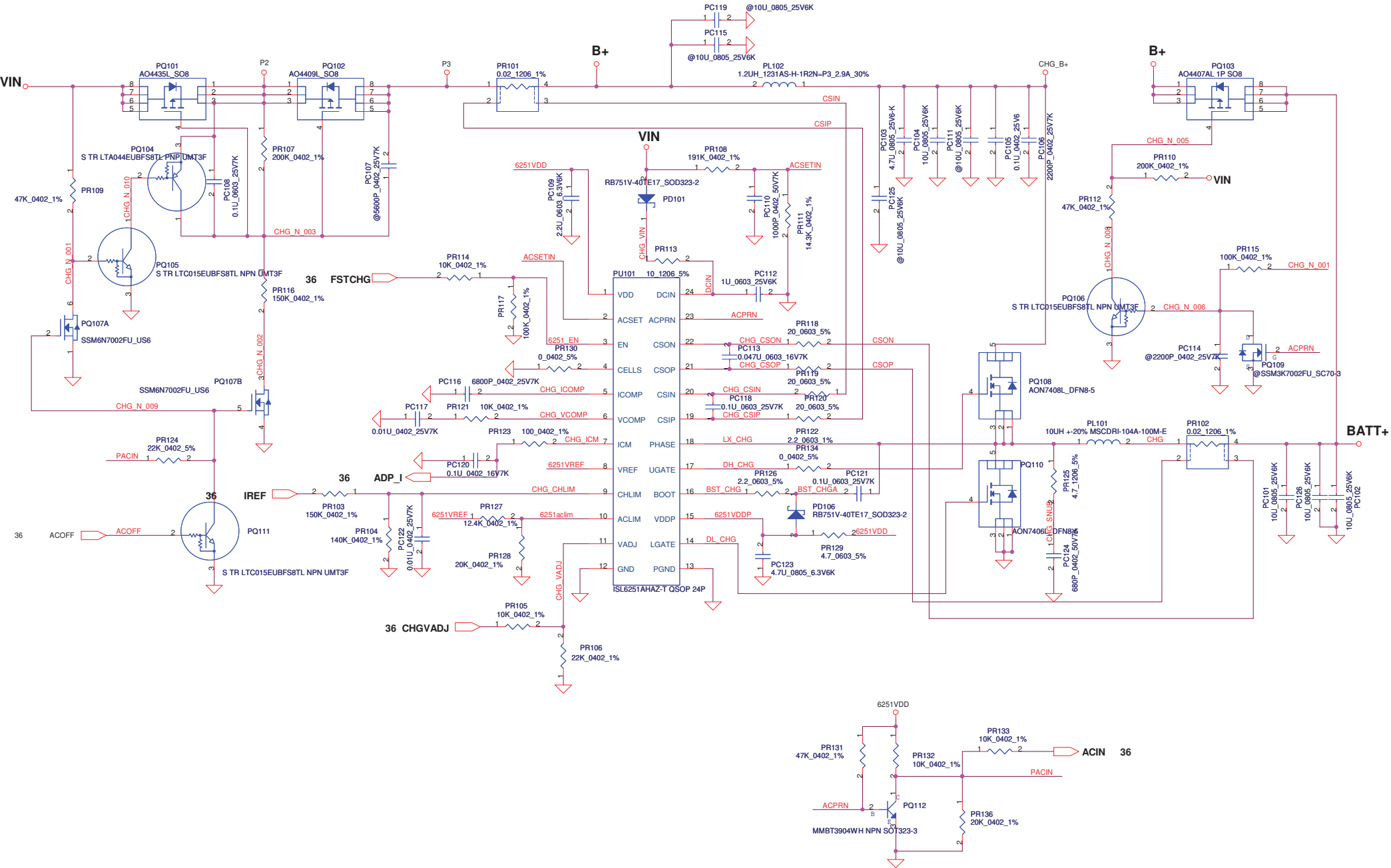
+1.5V TO +1.5VS (1.5A)



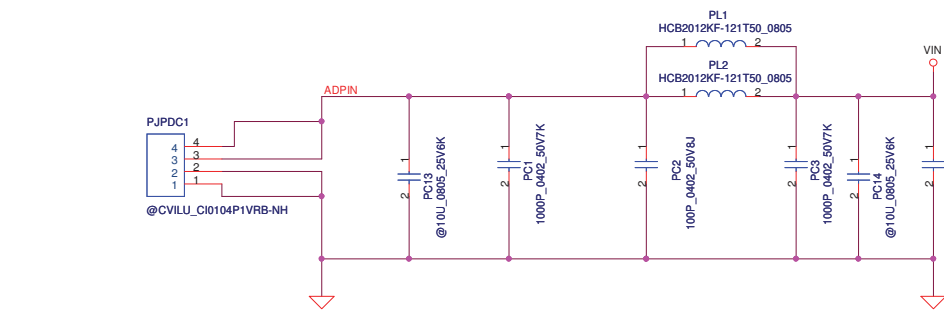
+3VS to +3VSG (3.3A)



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				Date: Wednesday, April 27, 2011	Rev 1.0
				Sheet 38 of 53	

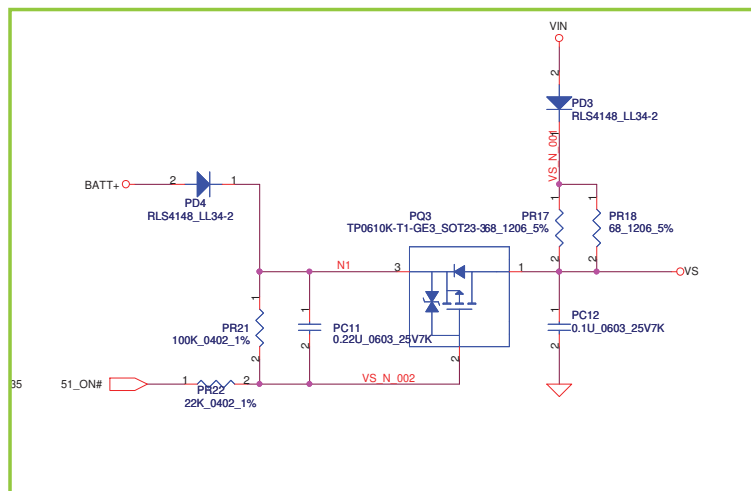
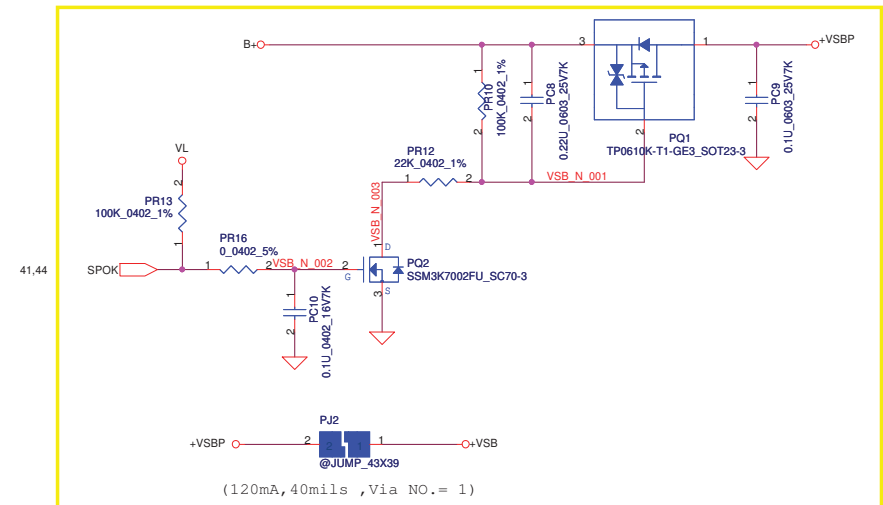
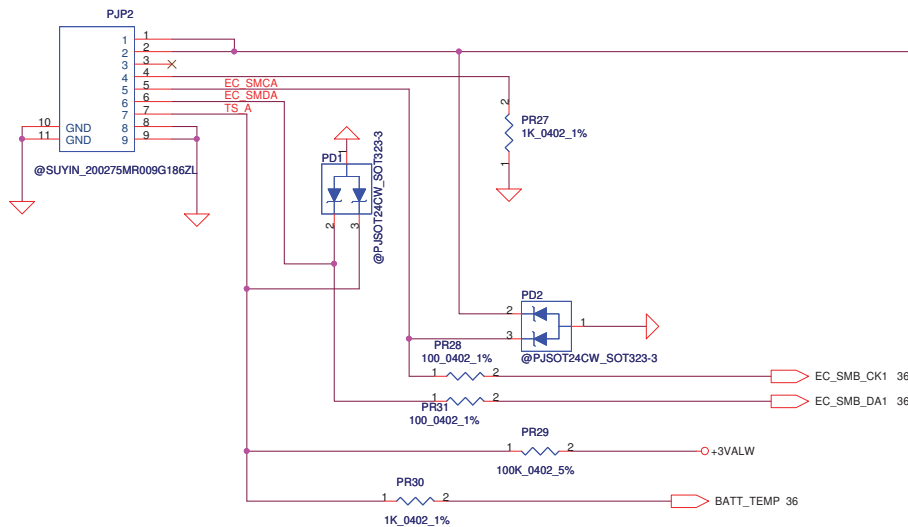
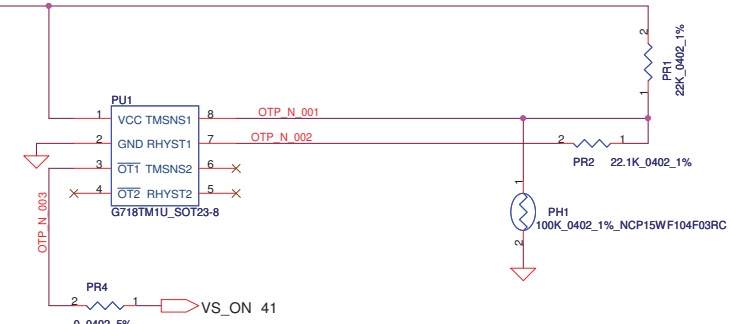


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					Size	Document Number
Date:		Wednesday, April 27, 2011		Sheet 39	of 53	

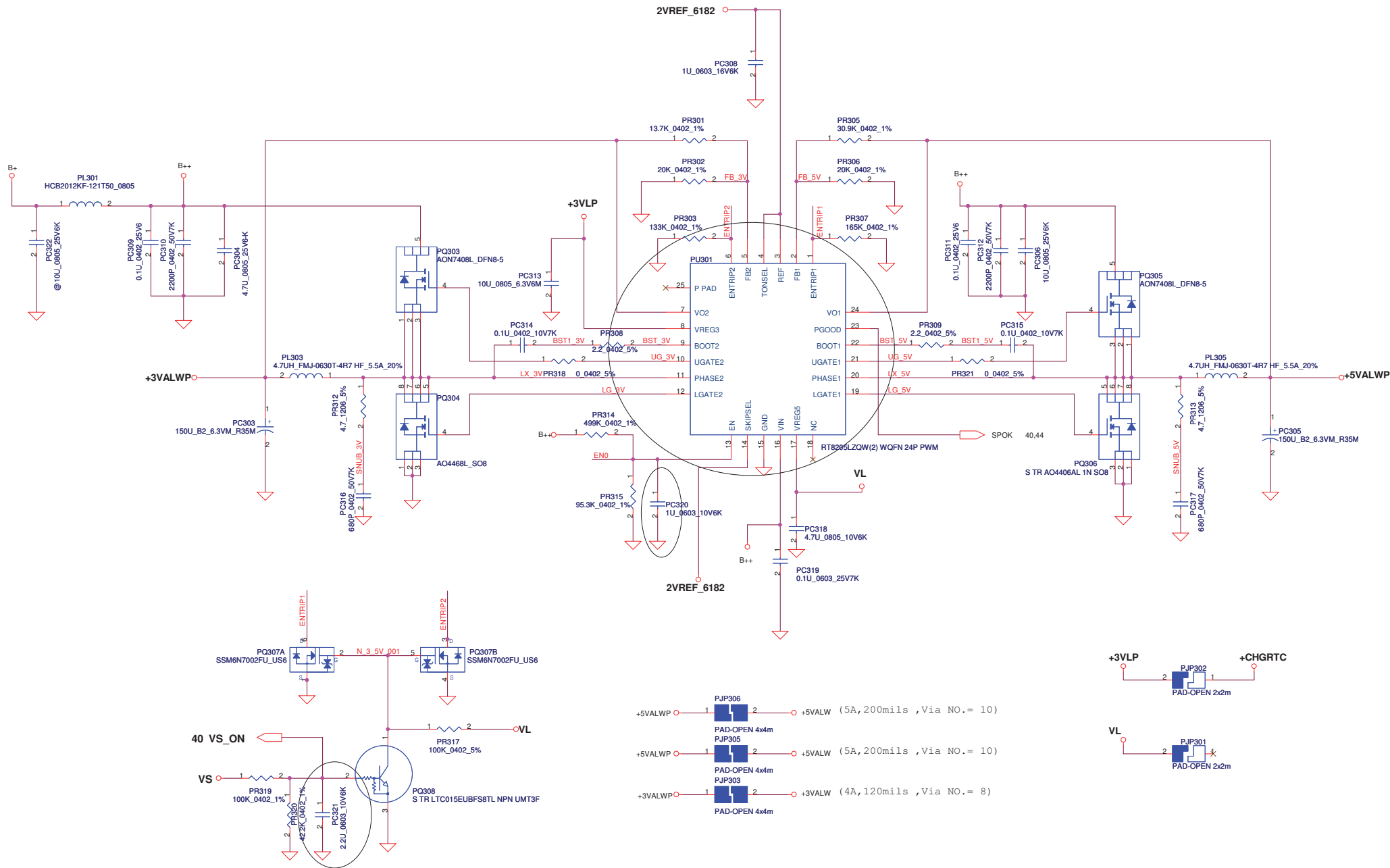


PH1 under CPU botten side :
CPU thermal protection at 92 +/-3 degree C
Recovery at 80 +/-3 degree C

PC5
0.1U_0603_16V7K
X7R type

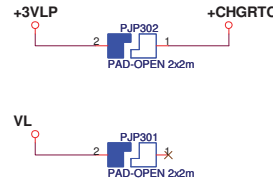


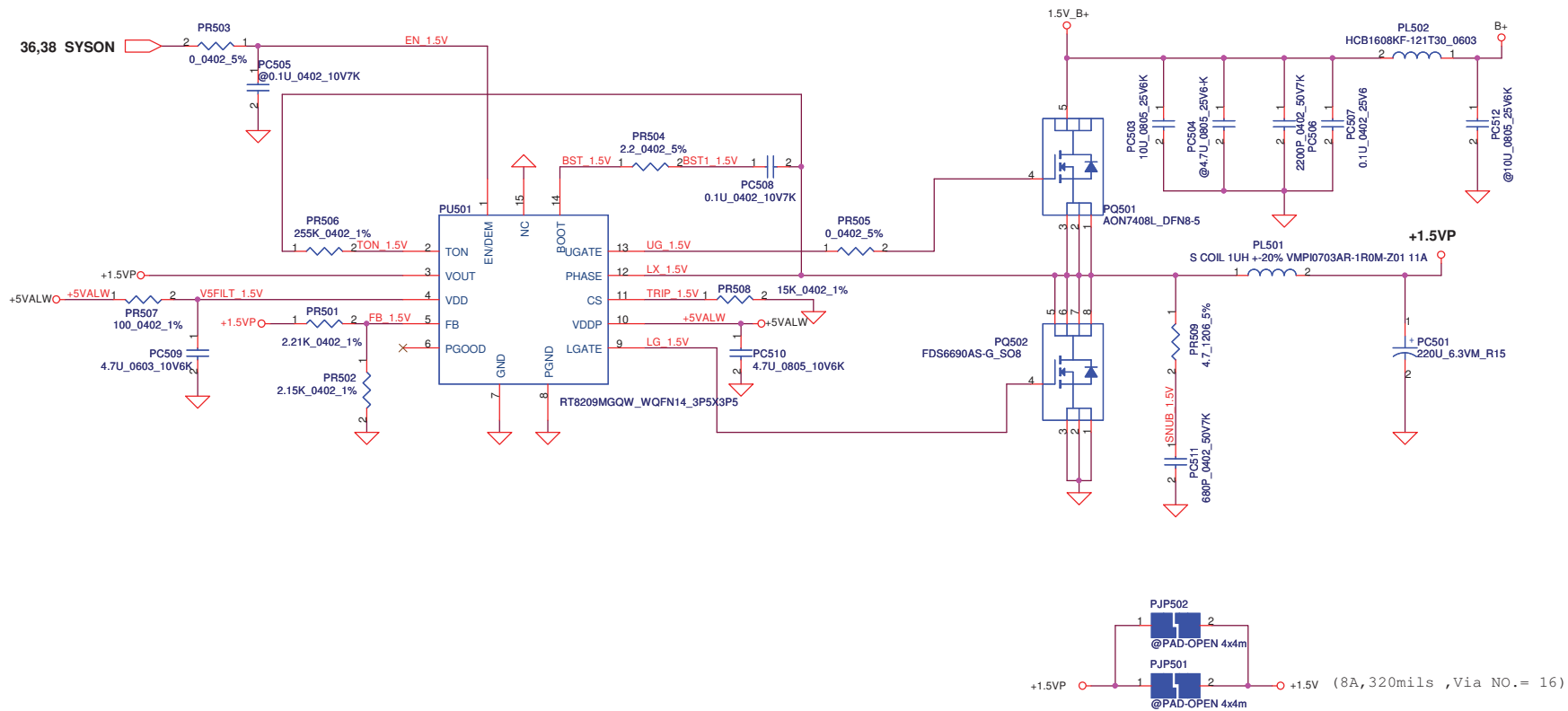
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					NCL61 LA-6321P M/B	1.0
				Date	Wednesday, April 27, 2011	Sheet 40 of 53



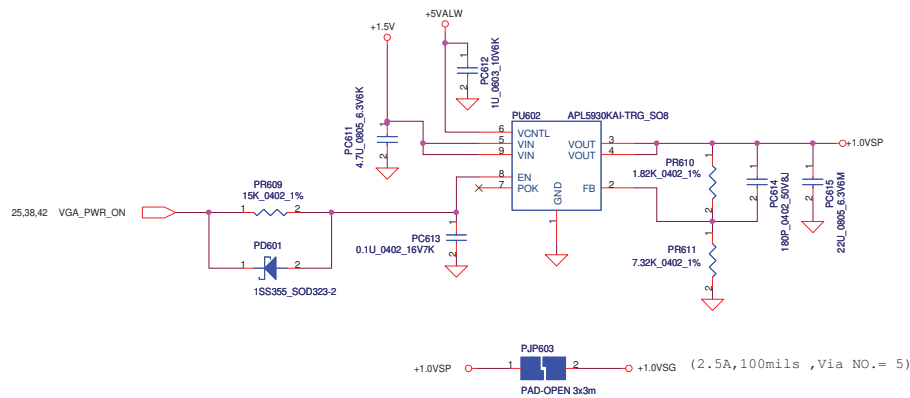
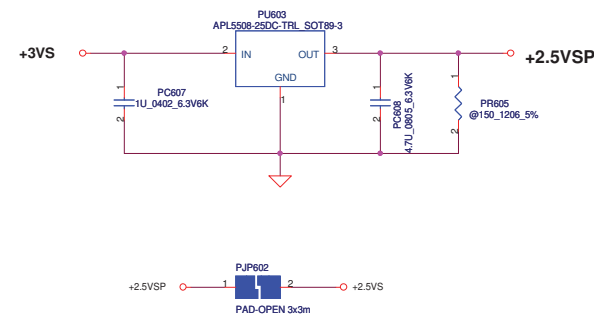
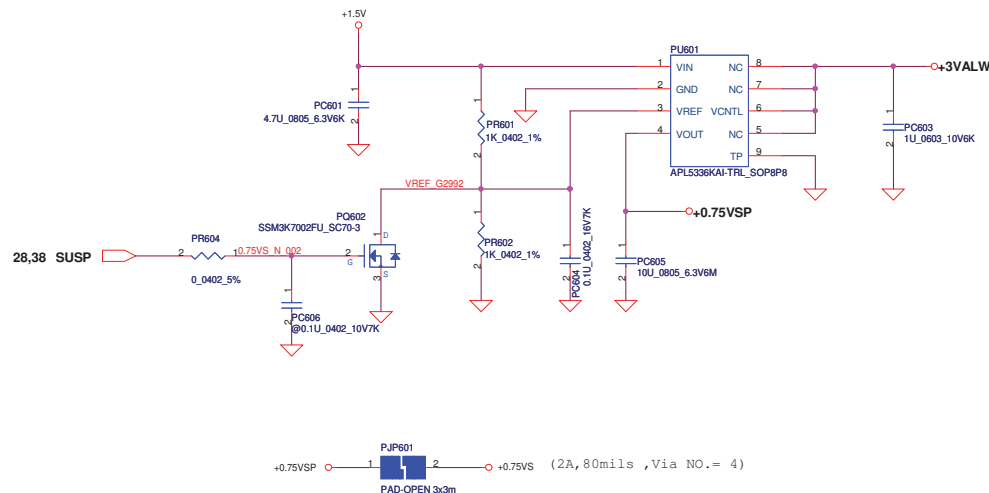
EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

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				Cust	QBL50 LA-7551P
Date: Wednesday, April 27, 2011				Sheet	41 of 53

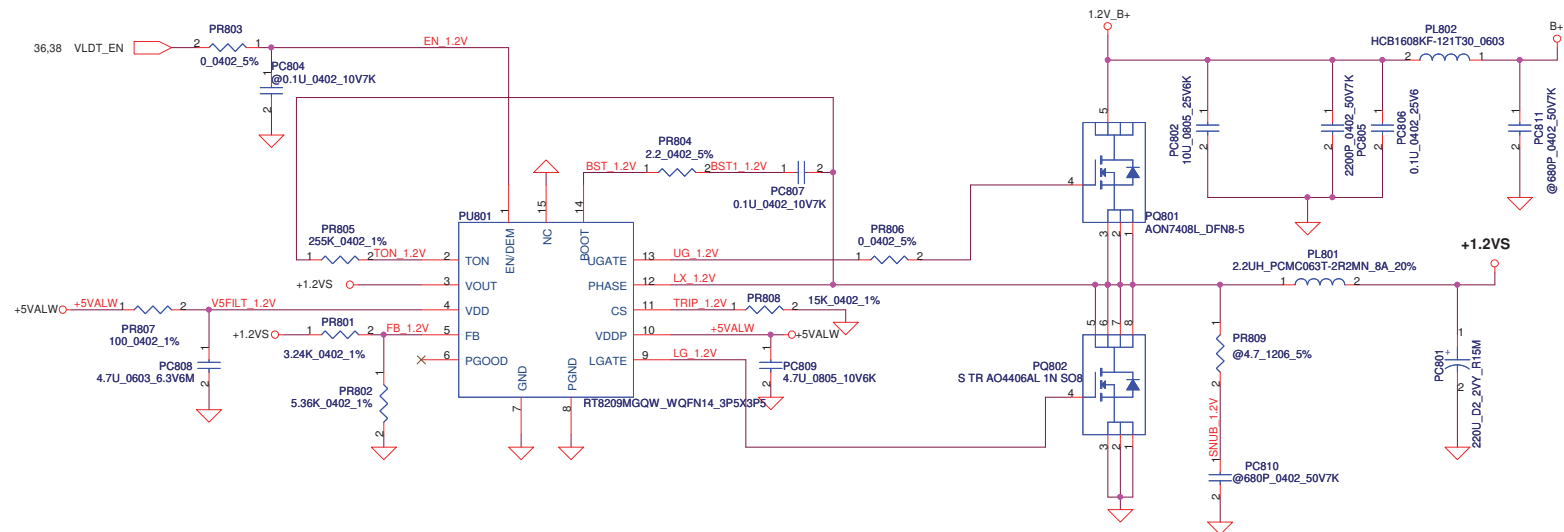




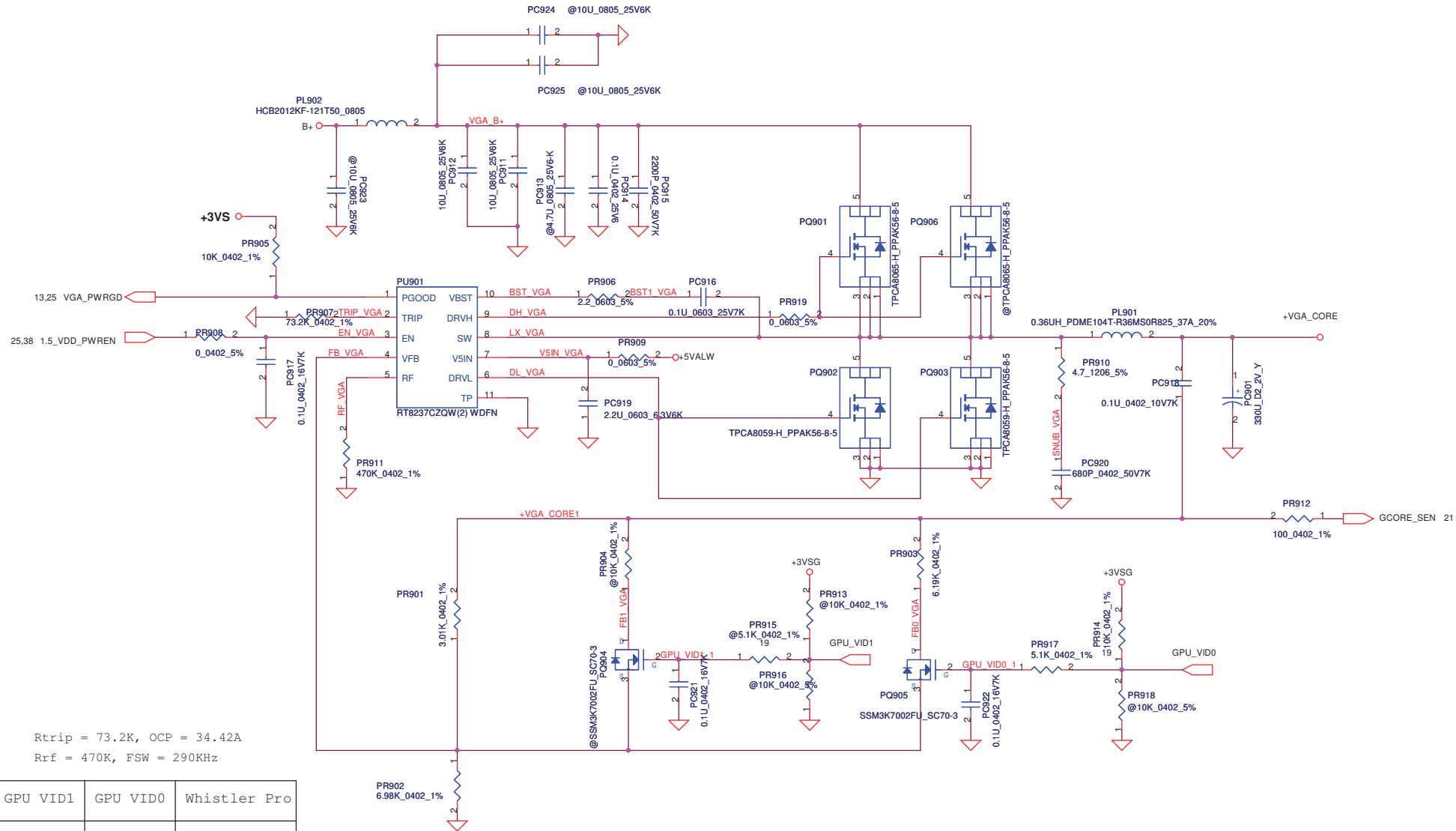
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				Size	Document Number
				QBL50 LA-7551P	
				Date:	Wednesday, April 27, 2011
				Sheet	43 of 53
				Rev	1.0



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Size	Document Number	QBL50 LA-7551P		Rev
Date:	Wednesday, April 27, 2011	Sheet	45	of 53



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					NCL61 LA-6321P M/B
				Date:	Wednesday, April 27, 2011
				Sheet	46 of 53
				Rev	1.0



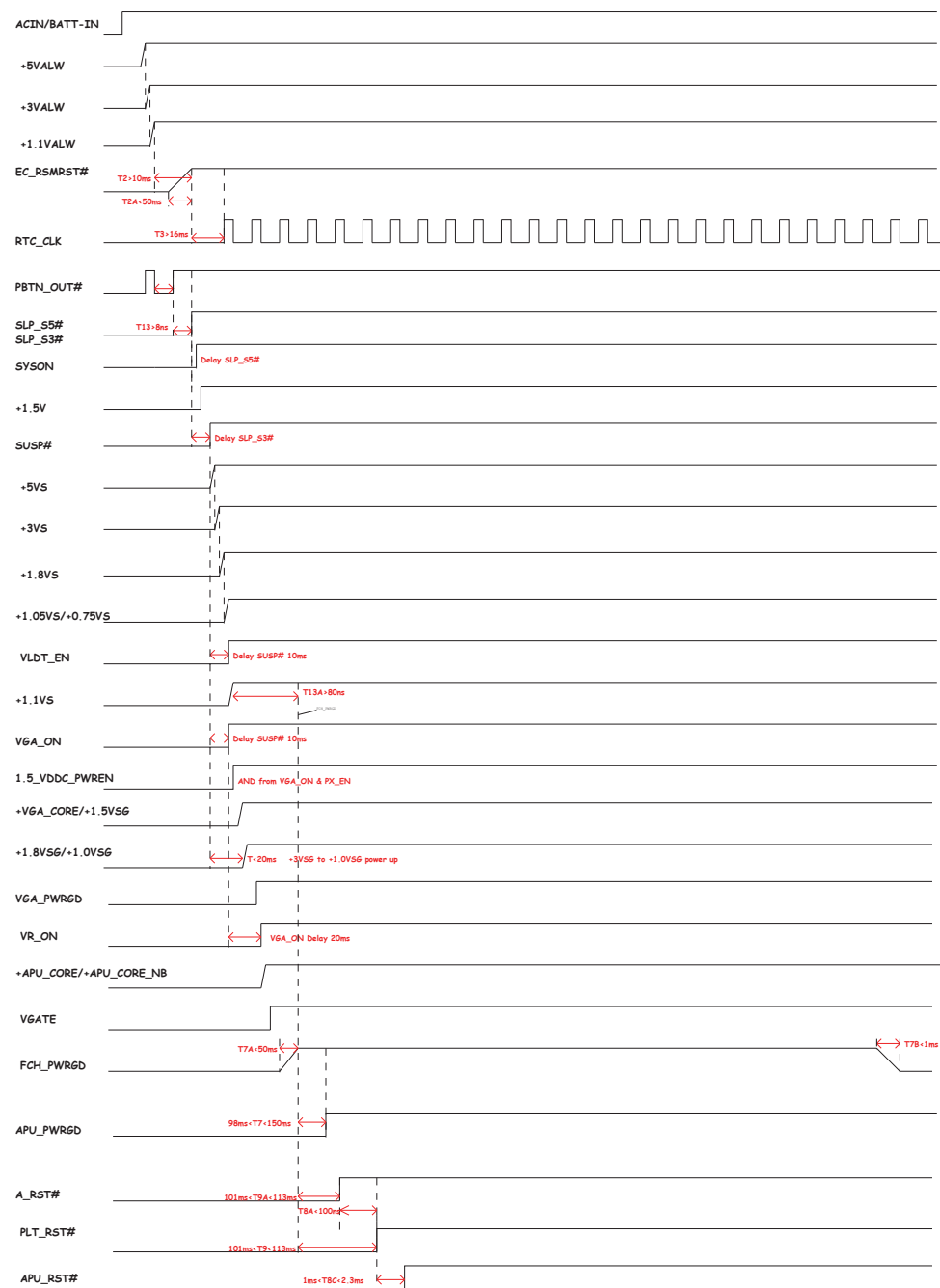
Rtrip = 73.2K, OCP = 34.42A
Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

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POWER SEQUENCE

[illegible]

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For AMD request	0.11	PG#26	Translator change to ANX3110	03/15	ER
2		For AI charge function	0.11	PG#34	Add U2 & U56	03/15	ER
3		For PBL60 MEMO	0.11	PG#32	Change LED1 to Green color.	03/15	ER
4		For switch quality of ME.	0.11	PG#37	Change SW5,SW6 to 100g switch for ME.	03/15	ER
5		For LED brightness.	0.11	PG#32	Change R1584 to 200 ohm. Change R1586,R1588,R1591,R1592,R1593 to 100 ohm	03/15	ER
6		For DFB.	0.12	PG#11	JDIMM1 footprint change to FOX_AS0A626-J8SG-7H_204P-T	03/17	ER
7		For USB3.0 & AI charge.	0.12	PG#34	USBP0 connect to JUSB1 and USBP10 connect to JUSB2.	03/17	ER
8		For Back light function.	0.12	PG#36	U31.15 connect to ENBKL from APU.	03/17	ER
9		For HDMI HPD issue.	0.12	PG#10	Q34 change to 2N7002(ESD) Add R469 to +1.5VS.	03/19	ER
10		For DP0_HPD & DP1_HPD from AMD recommend.	0.12	PG#10	Swap Q13.1 & Q13.3, R618 unmount. Swap Q16.1 & Q16.3, R627 unmount.	03/19	ER
11		For Travis Vendor request	0.12	PG#26	Del DP0_TXN0_C & DP0_TXP0_C	03/22	ER
12		For LED1	0.12	PG#32	LED1 connect to +3VALW	03/22	ER
13		For EC SMBUS	0.2	PG#36	R1021,R1022 change to install.	03/24	ER
14		For Sourcer recommend	0.2		SE100105Z80 change to SE000000K80	03/24	ER
15		For Sourcer recommend	0.2		SE103225Z80 change to SE000008880	03/24	ER
16		For Sourcer recommend	0.2		SB000006A00 change to SB000006A10	03/24	ER
17		For Thermal	0.2	PG#37	Del H4	03/24	ER
18		For +5VS rising time	0.2	PG#38	R1103 change to 47K	03/24	ER
19		For Crystal EA	0.2	PG#29	C1634 change to 12P & C1633 change to 15P	03/24	ER
20		For Crystal EA	0.2	PG#13	C1200 & C1201 change to 12P	03/24	ER
21		For Crystal EA	0.2	PG#19	C353 change to 15P & C354 change to 12P	03/24	ER
22		For EMI request	0.2	PG#36	R1033 change to SM01000DI00 R1055 change to 33 ohm	03/24	ER
23		For EMI request	0.2	PG#28	L38,L39,L40,L41 change to SM070001S00	03/24	ER
24		For EMI request	0.2	PG#27	D1,D2,D3,D6 change to install	03/24	ER
25		For Crystal EA	0.2	PG#13	C1205,C1206 change to 10P	03/24	ER
26		For AI charge	0.2	PG#36 PG#34	U2 reserve CEN# to EC	03/25	ER
27		For AMD spec	0.2	PG#27	R1642 & R1646 change to 4.6K ohm	03/29	ER

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				Date: Wednesday, April 27, 2011	Rev 1.0
				Sheet 51 of 53	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For EMI reuquest	0.2	PG#30	R1555,R1556,R1557,R1558 change to 0.1uF	03/29	ER
2		For share ROM reuquest	0.2	PG#15 PG#16	U28,R626,R934,R935,R35 change to Un-install R921 change un-install & U910 change to install	03/29	ER
3		For EMI reuquest	0.2	PG#34	D5 change to SC300001Y00 (YSCLAMP0524P)	03/29	ER
4		For Crystal vendor recommend	0.21	PG#13	Y4 change to SJ100007N00 (32.768K 7PF)	04/07	PR
5		For EMI recommend	0.21	PG#29	TS1 change to SP050006F00 (IH-160)	04/07	PR
6		For discharge EA	0.21	PG#38	R1127 change from 470 ohm to 33 ohm	04/07	PR
7		For leakage current	0.21	PG#27	R1644,R1645,Q101 change to install R4,R31 change to un-install	04/07	PR
8		For EMI recommend	0.21	PG#29	C1636 change from 1000P to 120P	04/08	PR
9		For thermal recommend	0.21	PG#19	Add R78, R79, R80, R82	04/18	PR
10		Reserve PX_EN signal	0.21	PG#36	Reserve signal PX_EN to EC pin 74	04/18	PR
11		Swap JDIMM1 & JDIMM2 location	0.21	PG#11 PG#12	Follow ME BOM	04/18	PR
12		Do not use for MP	0.21	PG#35	Del SW3 SW4	04/18	PR
13		Change Boarrrd ID to PR10	0.21	PG#37	Change R1036 to 18k	04/18	PR
14		For DFB request del co-lay schematiic	0.21	PG#34	Del R672~R675, R664~R667	04/18	PR
15		For EMI request	0.22	PG#29	ADD D7	04/19	PR
16		For EMI request	1.0	PG#13	unstuff C1193	04/25	PR
17		For Customer change FCH P/N	1.0	PG#13 ~17	location U25, for M2 change to SA000042C80, M3 change to SA000043ID0	04/25	PR
18		For ESD request	1.0	PG#32	R628,R629,R678,R679,R680,R681 change from 0ohm to 33ohm & Add 1uF for C560,C568,C569,C570,C573,C571	04/27	PR
19							
20							
21							
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24							
25							
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27							

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				QBL50 LA-7551P	
Date: Wednesday, April 27, 2011				Sheet	52 of 53
				Rev	1.0

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For MP cost down	1.0		As picture	03/15	PR
2							
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				Date Wednesday, April 27, 2011	Rev 1.0
				Sheet 53	of 53