

Compal Confidential

QBL50 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2010-02-16

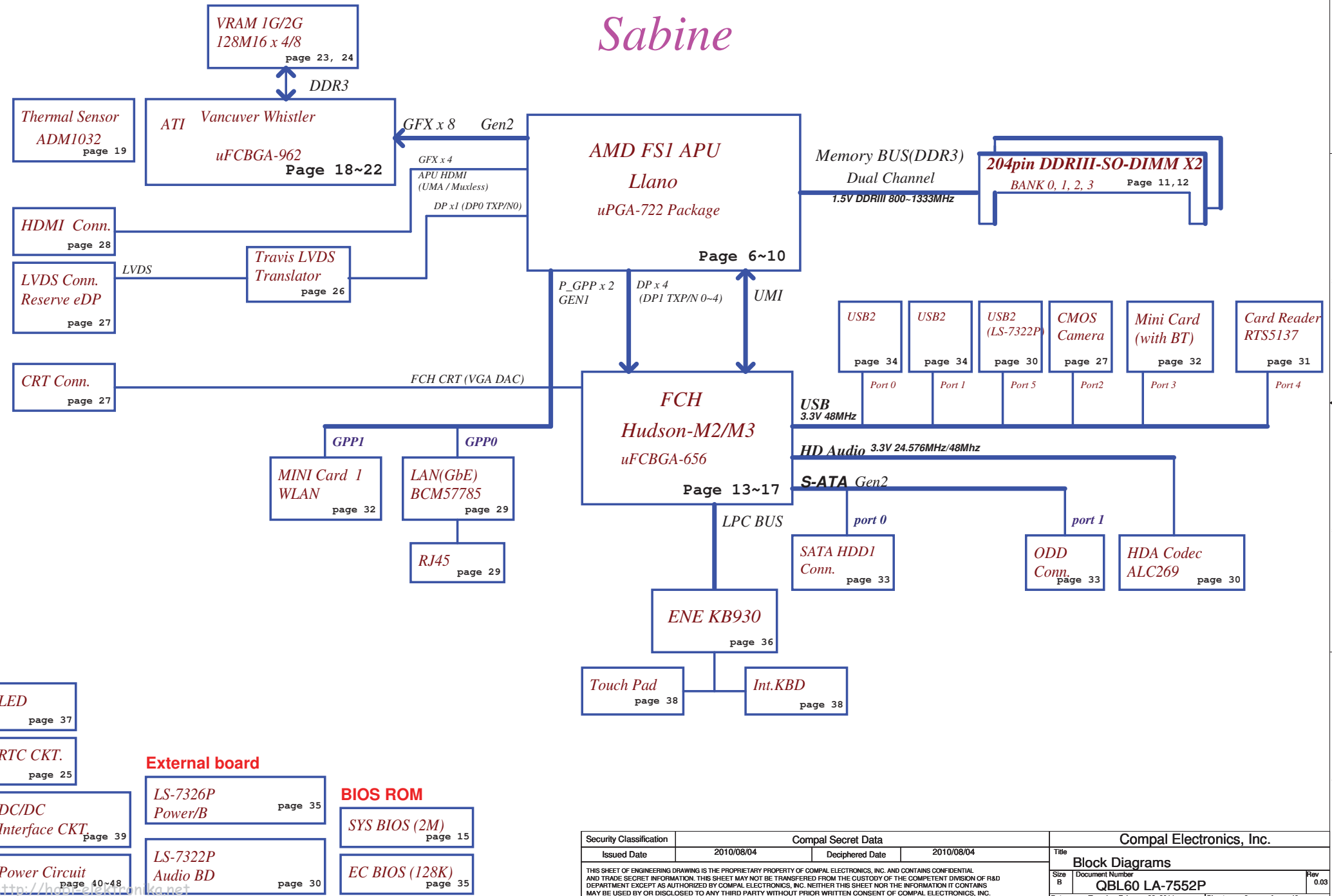
LA-7552P REV: 0.03

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				Size B	Document Number QBL60 LA-7552P Rev 0.03
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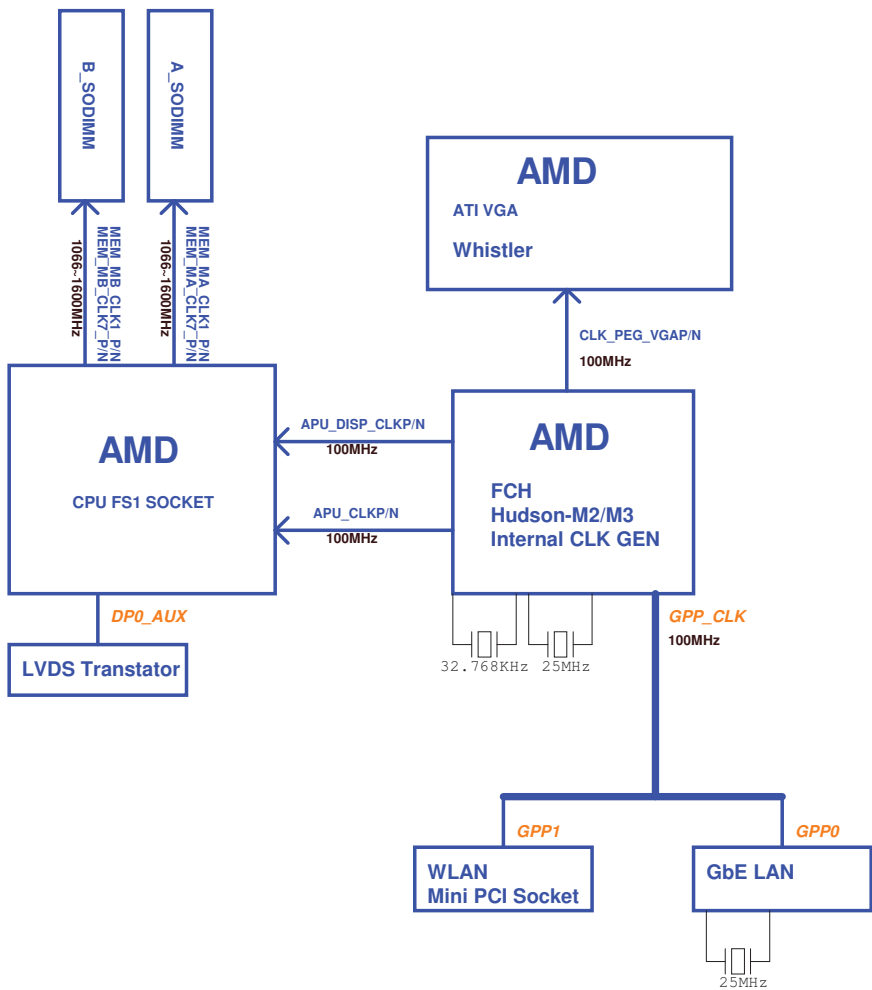
Model Name : QBL60

Sabine

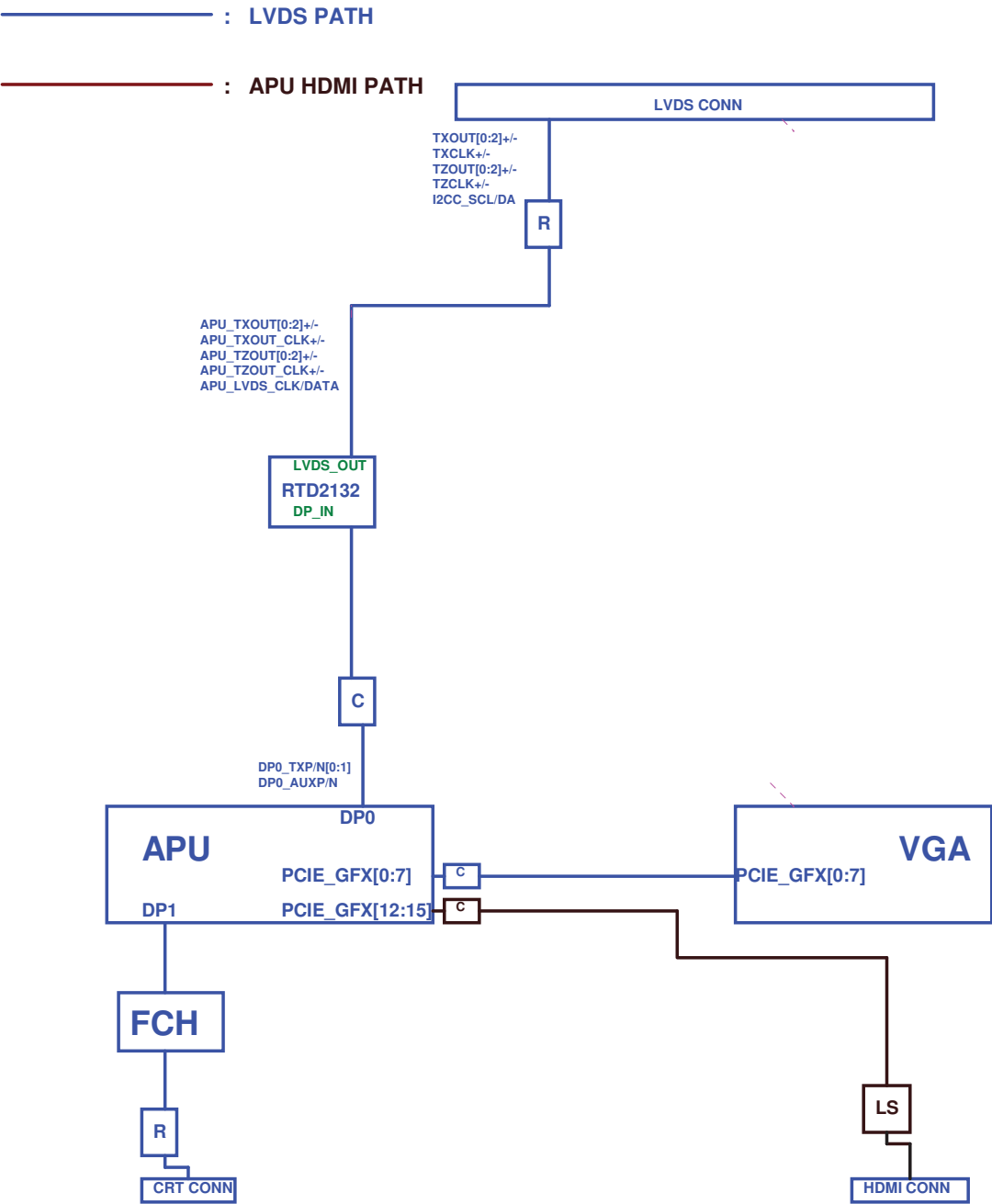


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Issued Date	2010/08/04	Deciphered Date	2010/08/04	Title	Block Diagrams
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CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (VGA)	1001 101X b	9AH
			(APU)		
			RTD2132S (TL)		

FCH
SM Bus 0 address

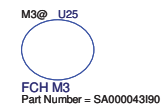
FCH
SM Bus 1 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	D0			
DDR DIMM2	1101 001X b	D2			

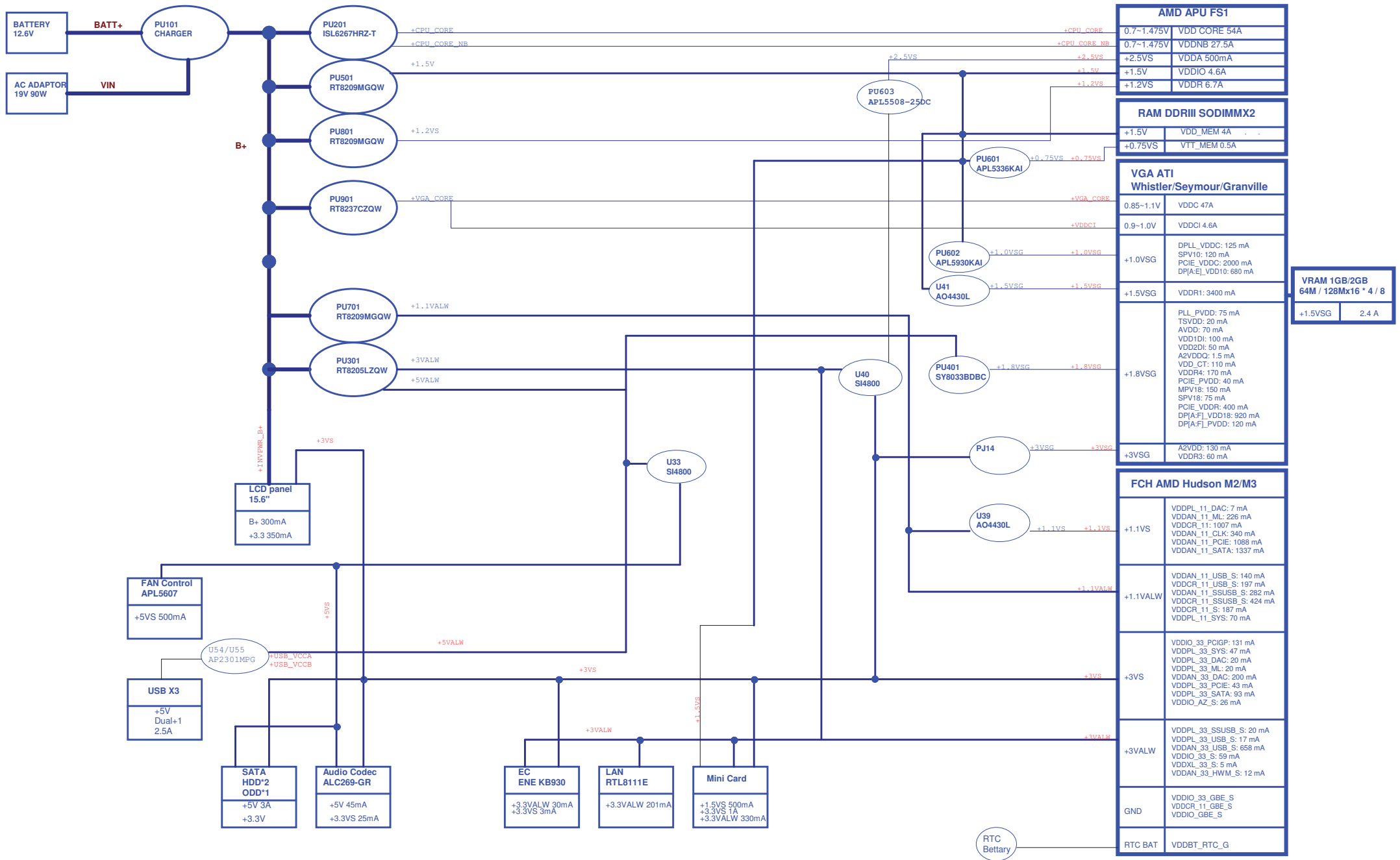
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

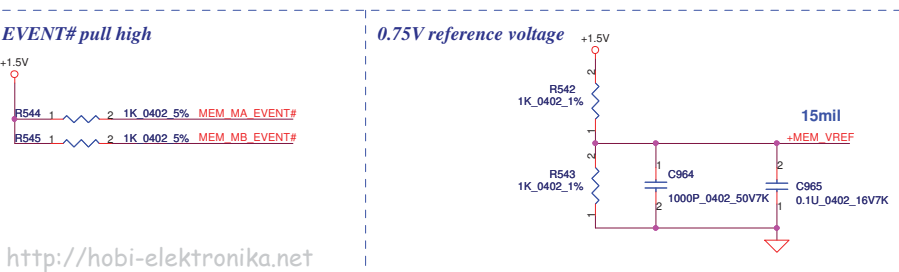
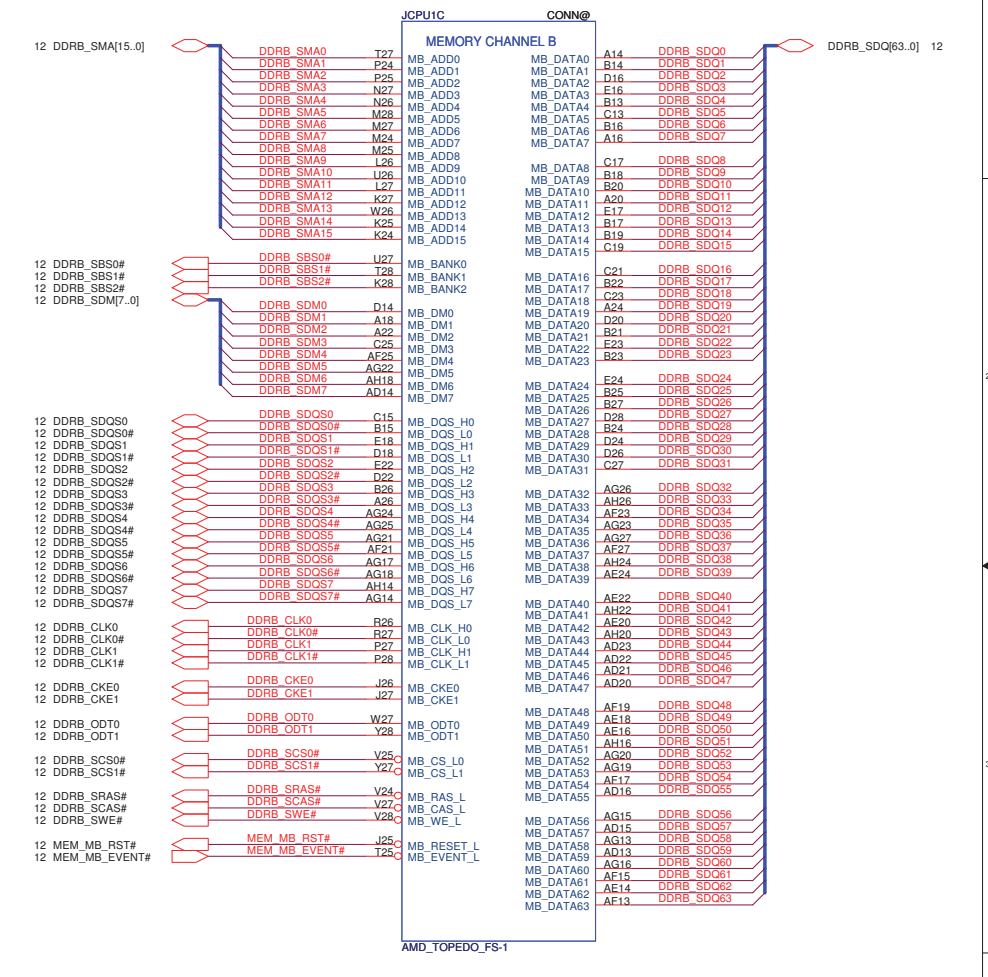
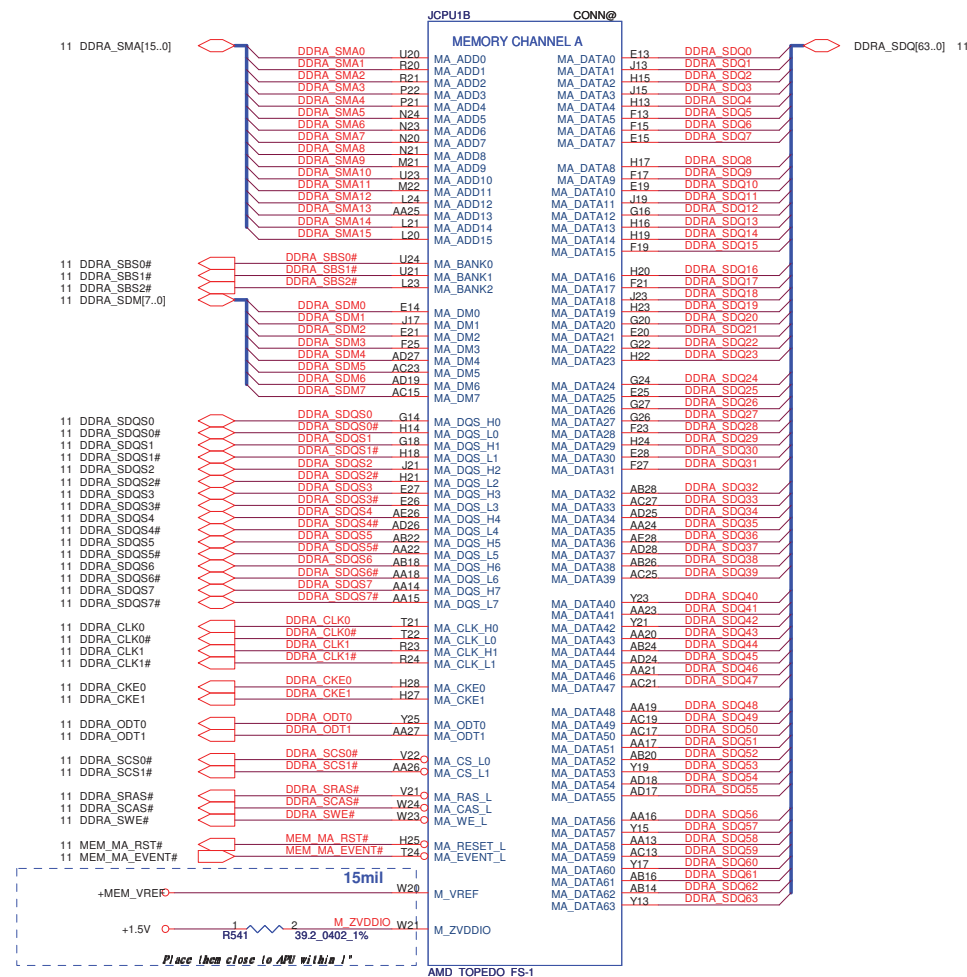


BOM Config



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						POWER DELIVERY CHART	
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To LVDS
Translator

To FCH VGA ML

100MHz

100MHz_NSS

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

route as differential

route as differential

http://hobi-elektronik.net

Place near APU

Place near APU

System DP

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

route as differential

route as differential

JCPU1D

JCPU1D

System DP

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

route as differential

route as differential

AMD_TOPEDO_FS-1

CONN@

CONN@

System DP

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

route as differential

route as differential

AMD_TOPEDO_FS-1

Place near APU

Place near APU

System DP

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

route as differential

route as differential

AMD_TOPEDO_FS-1

AUX 2-5 are for GFX interface
use, they could be selected to I2C
or AUX logic

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

HDT Debug conn

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

If not used, pins are left unconnected (DG ref.)
20101111

DP0_AUXP R554 2 1.8K 0402 5%
DP0_AUXN R555 2 1.8K 0402 5%
ML_VGA_AUXP R547 2 1.8K 0402 5%
ML_VGA_AUXN R556 2 1.8K 0402 5%

TEST25_L R548 1 2 510 0402 1%
TEST25_H R557 1 2 510 0402 1%

TEST35 R558 1 2 300 0402 5%
R559 1 2 300 0402 5%

M_TEST R564 1 2 39.2 0402 1%
R567 1 2 39.2 0402 1%

FS1R1 R571 1 2 10K 0402 5%

FS1R1 : Control S5 Dual PWR plane
in laptop, seems no use

ALLOW_STOP R612 1 2 1K 0402 5%
APU_RST# R577 1 2 1K 0402 5%
APU_PWRGD R578 1 2 300 0402 5%
APU_PWRGD R580 1 2 300 0402 5%

APU_PWRGD R580 1 2 300 0402 5%

APU_PWRGD R580 1 2 300 0402 5%

APU_PWRGD R580 1 2 300 0402 5%

APU_PWRGD R580 1 2 300 0402 5%

APU_PWRGD R580 1 2 300 0402 5%

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APU_PWRGD R580 1 2 300 0402 5%

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APU_PWRGD R580 1 2 300 0402 5%

APU_PWRGD R580 1 2 300 0402 5%

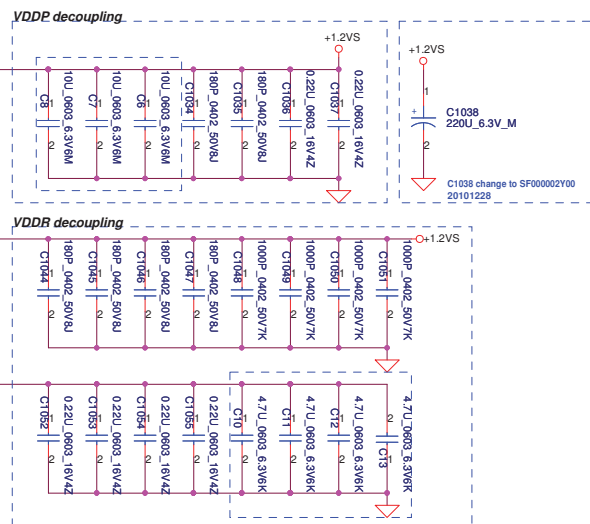
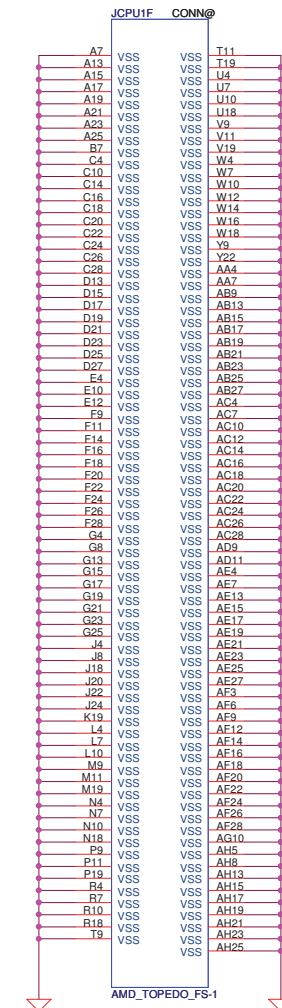
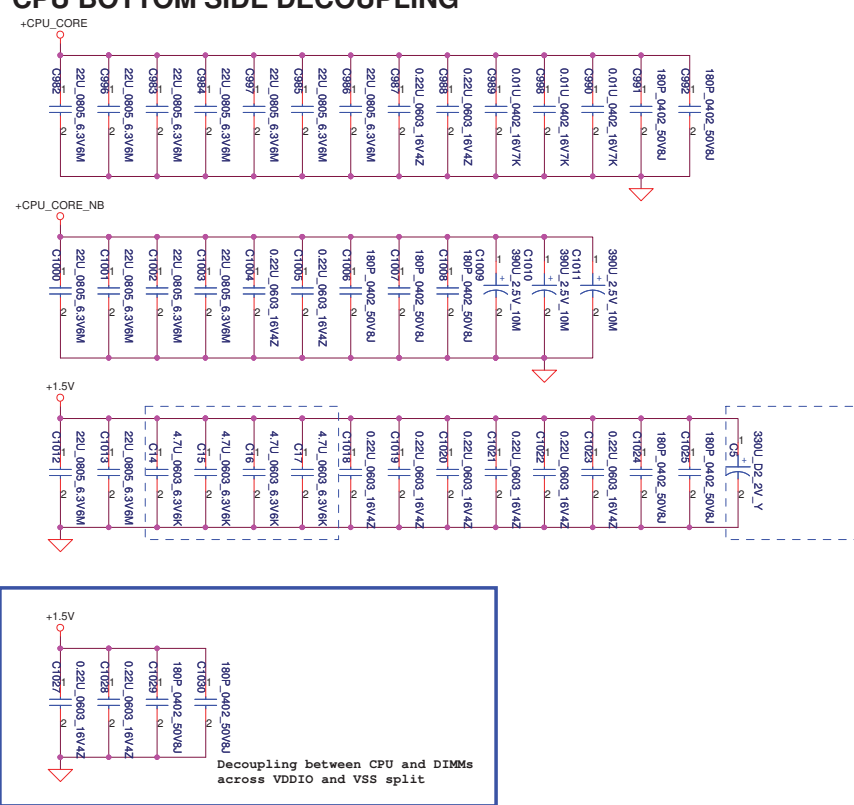
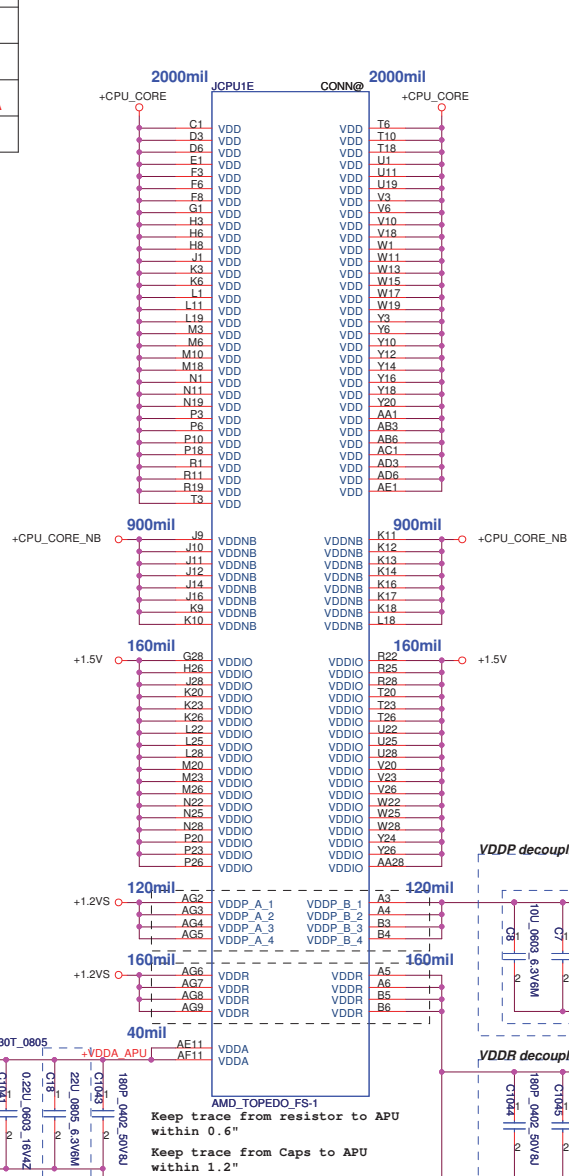
APU_PWRGD R580 1 2 300 0402 5%

APU_PWRGD R580 1 2 300 0402 5%

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Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11



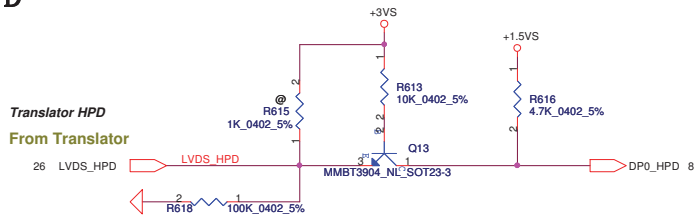
Demo Board Capacitor (include PWM side)						
CPU_CORE	CORE_NB	VDDIO_SUS	VDDIO_SUS	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	(CPU side)	(DIMM x2)	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	680uF x 1	100uF x 4	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	330uF x 1	0.1uF		180pF x 2	1nF x 4
180pF x 2	180uF x 3	22uF x 3				180pF x 4
10nF x 3		4.7uF x 4				
		0.22uF x 6				
		180pF x 4				

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				Customer	QBL60 LA-7552P
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HPD

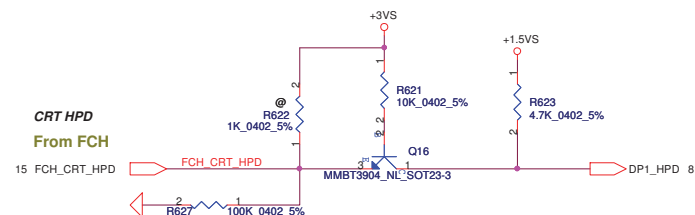
Translator HPD

From Translator



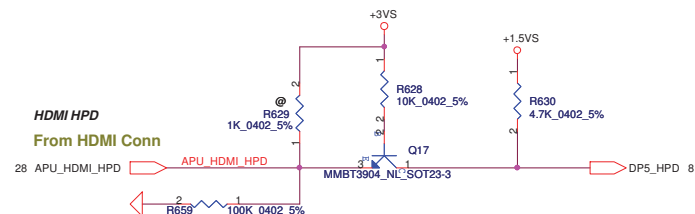
CRT HPD

From FCH

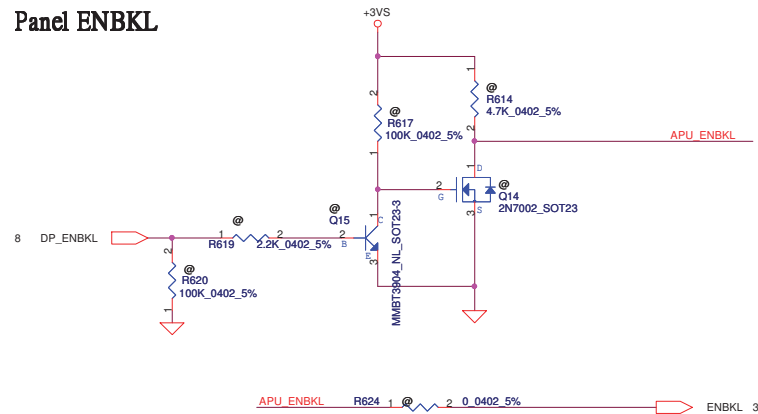


HDMI HPD

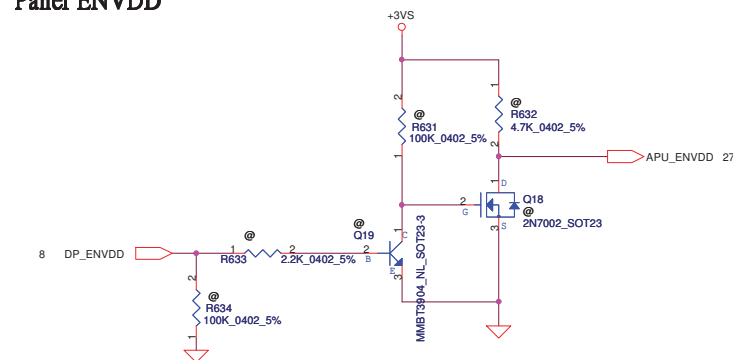
From HDMI Conn



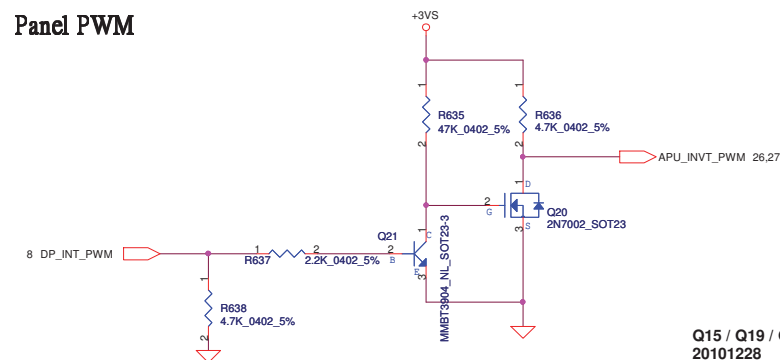
Panel ENBKL



Panel ENVDD

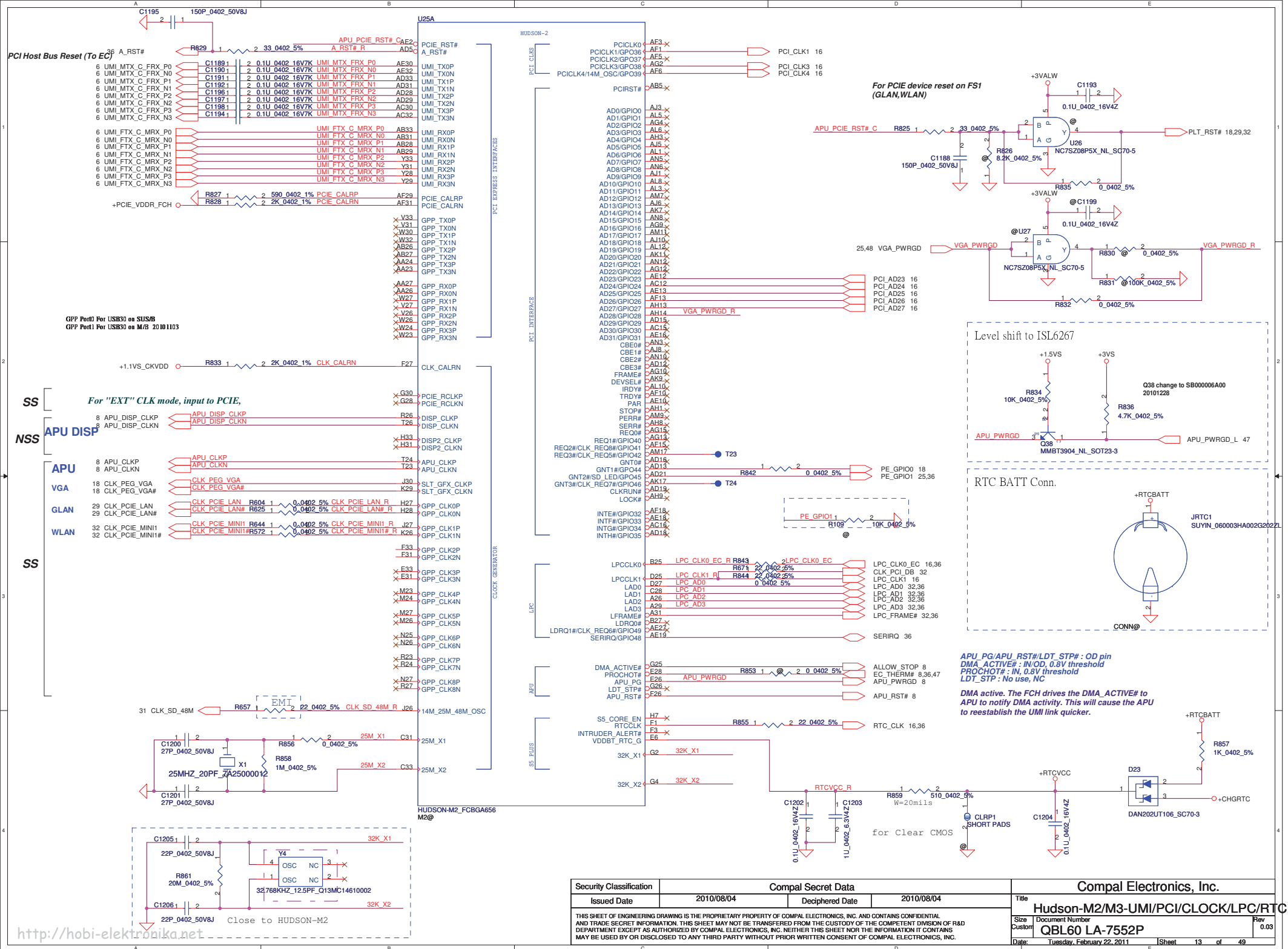


Panel PWM

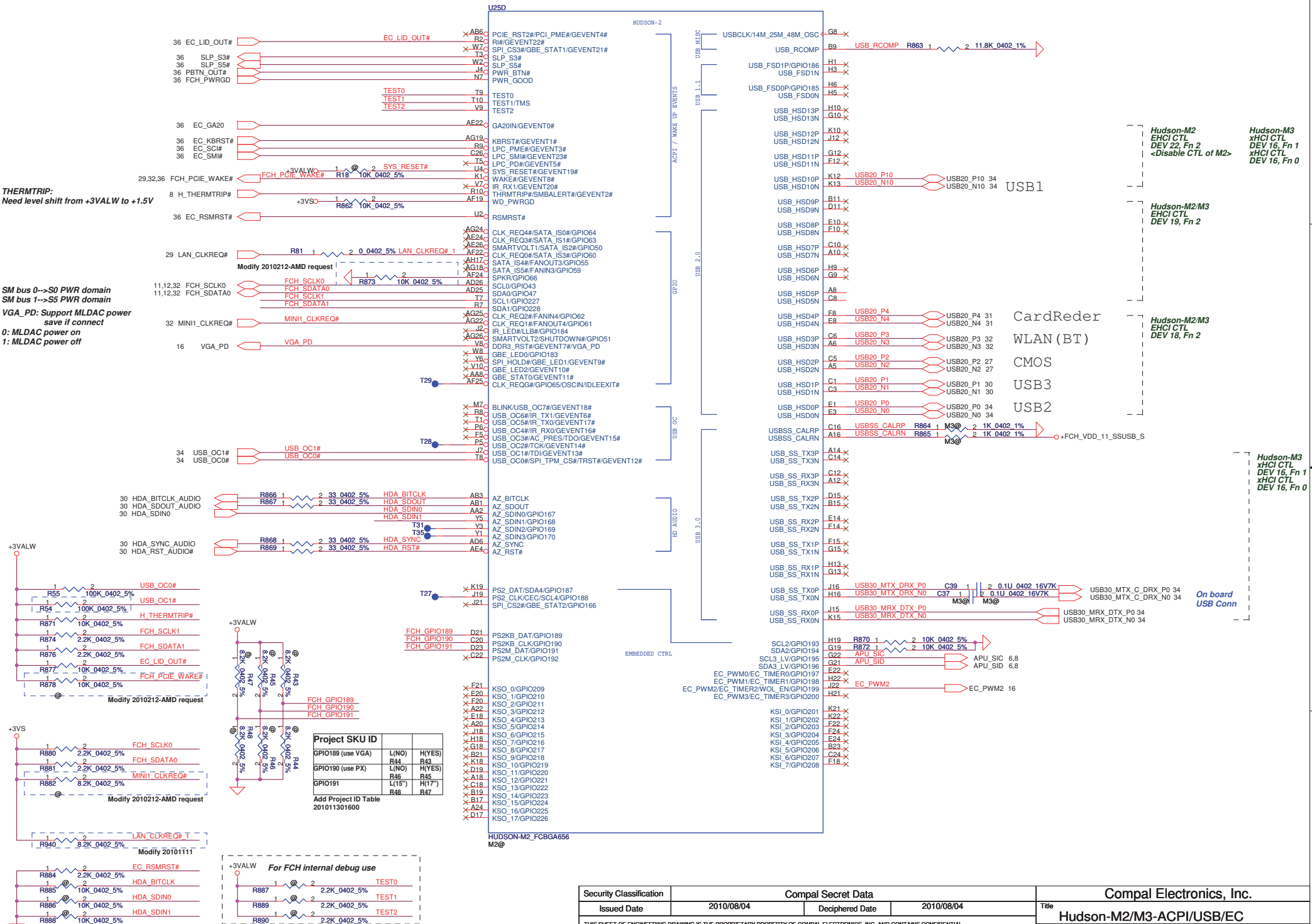


Q15 / Q19 / Q21 change to SB000006A00
20101228

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				AMD FS1 Singal Level Shifter	
				Size	
				Document Number	
				Rev	
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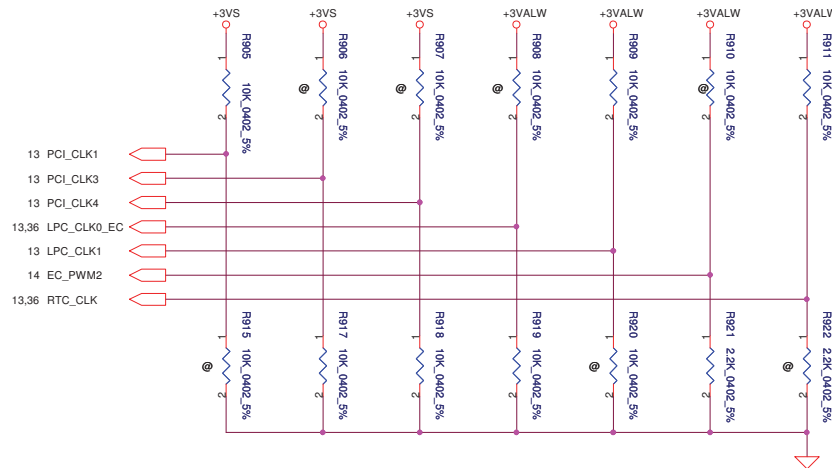
PCIE_RST2 : Reset PCIE device on Hudson2



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STRAP PINS

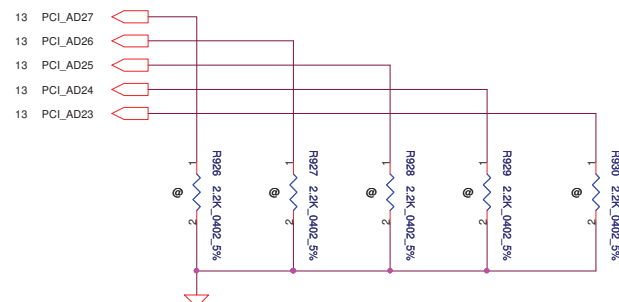
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



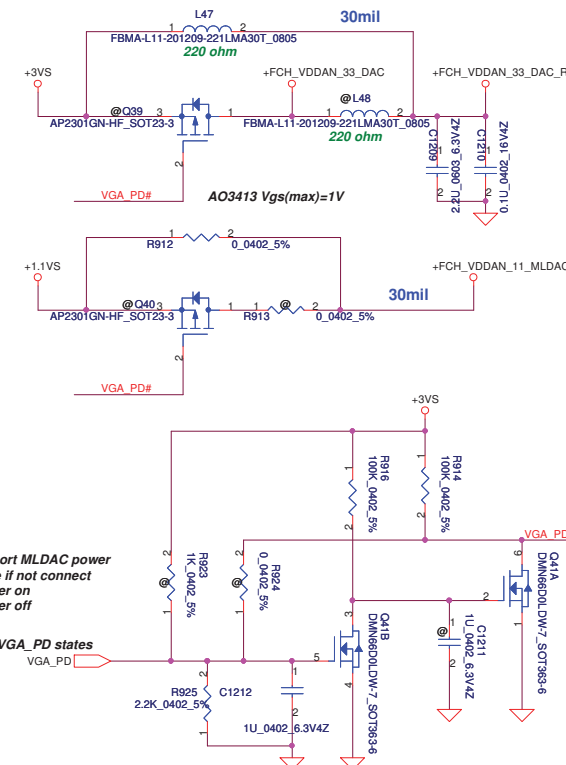
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



If support ML DAC power down when no VGA plug



VGA_PD: Support MLDAC power
save if not connect
0: MLDAC power on
1: MLDAC power off

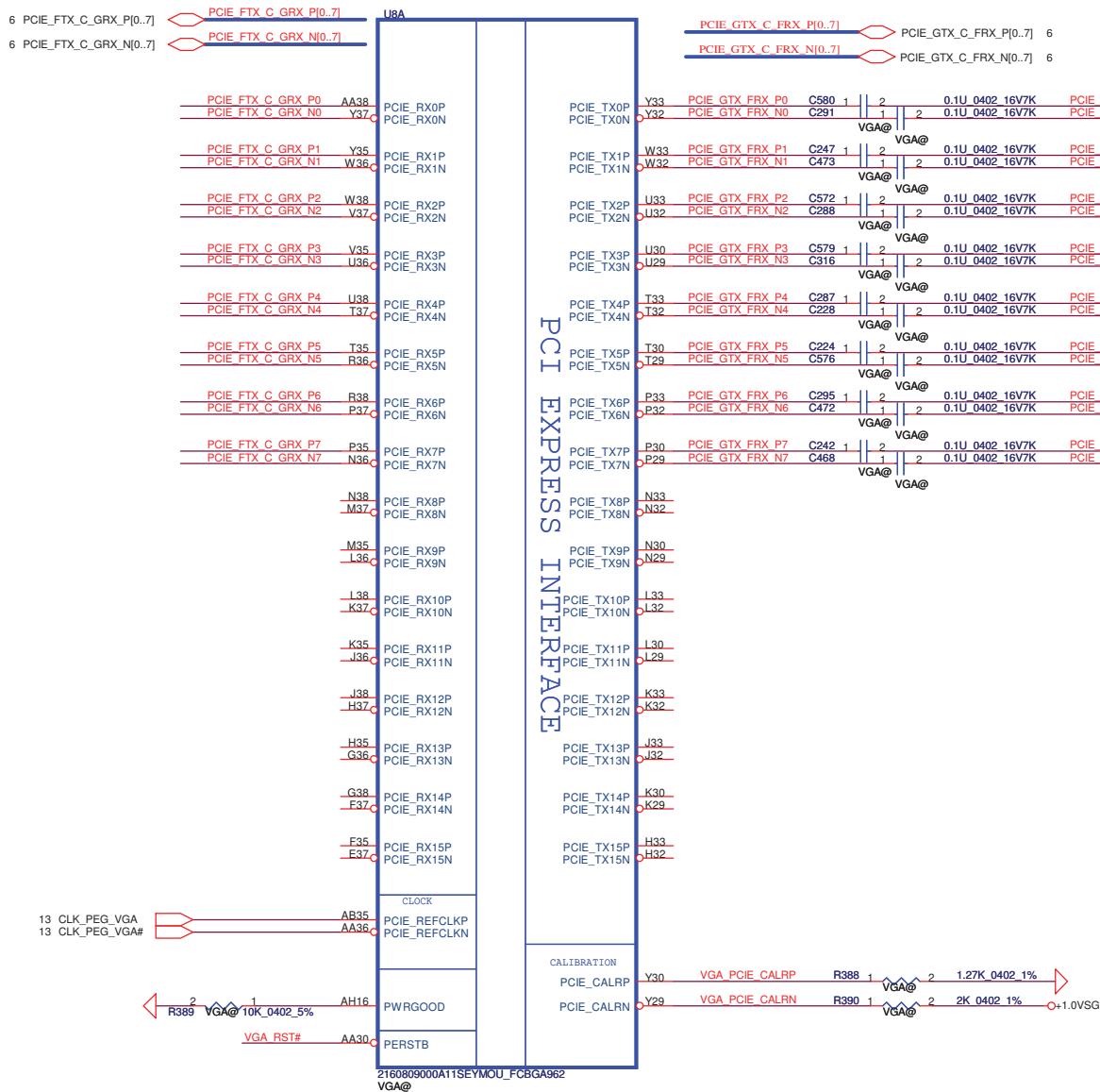
Check VGA_PD states
14 VGA_PD

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[illegible]

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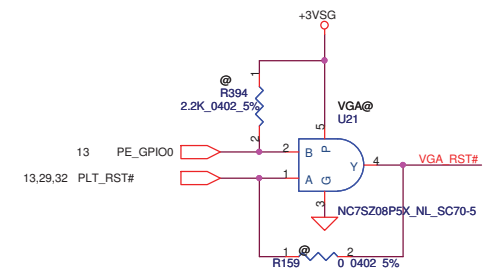
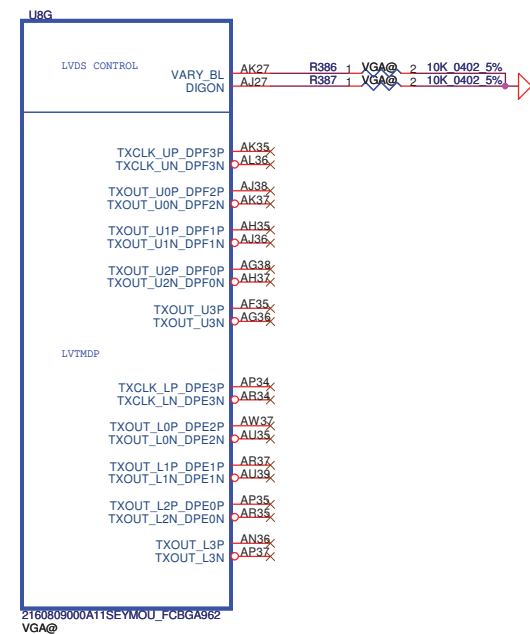
GFX PCIE LANE REVERSAL



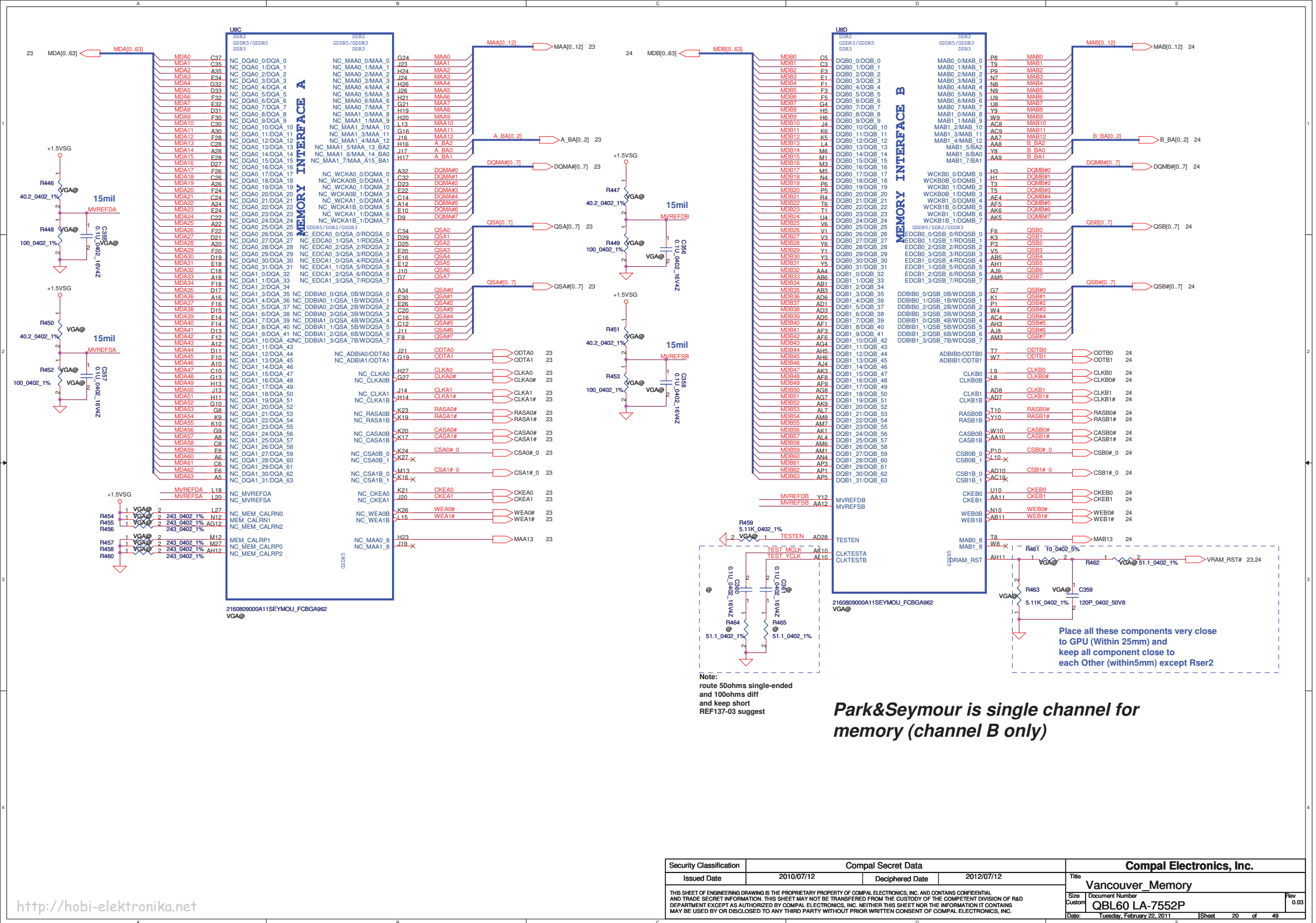
For UMA Mux.

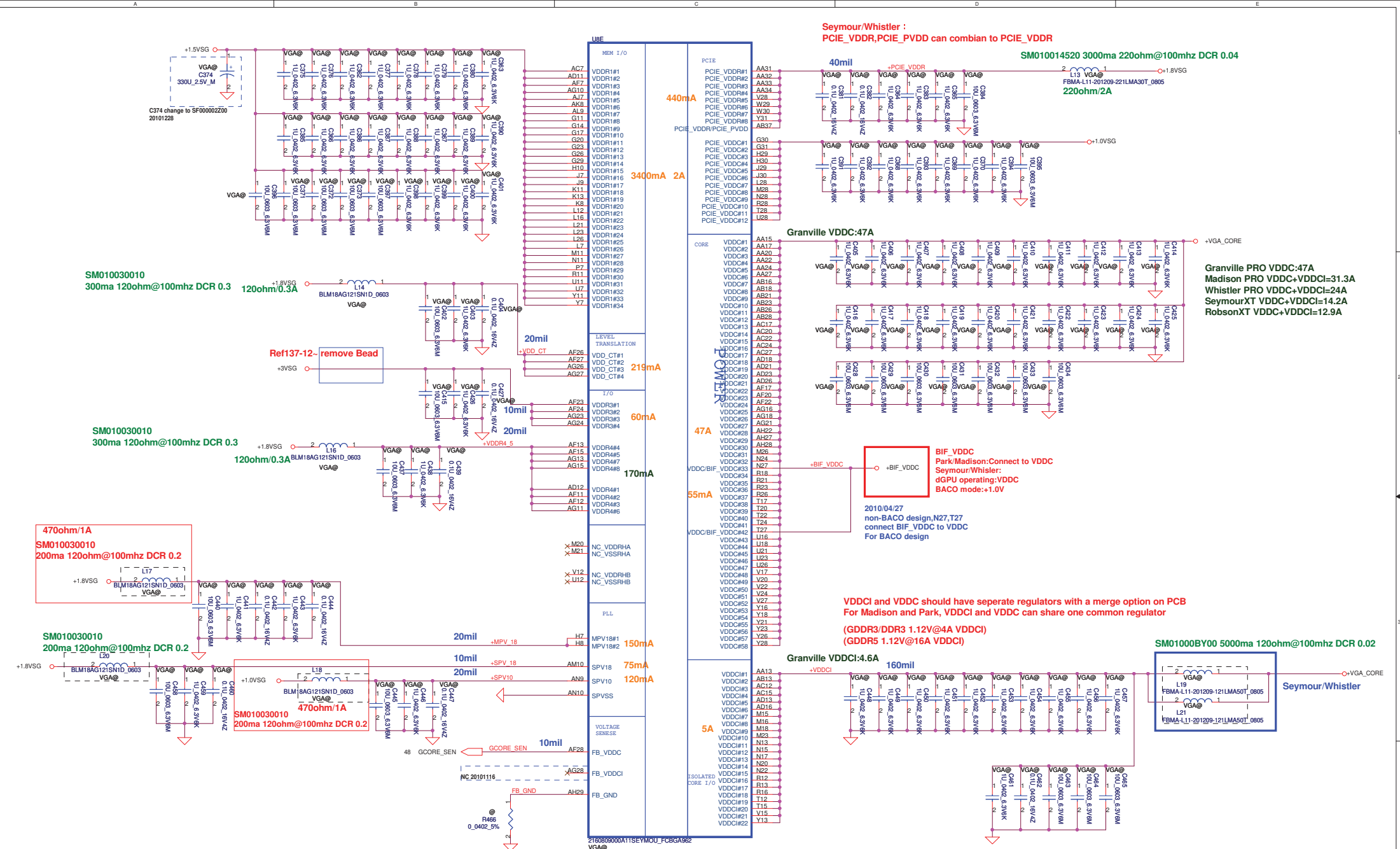
<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High ,external PD need

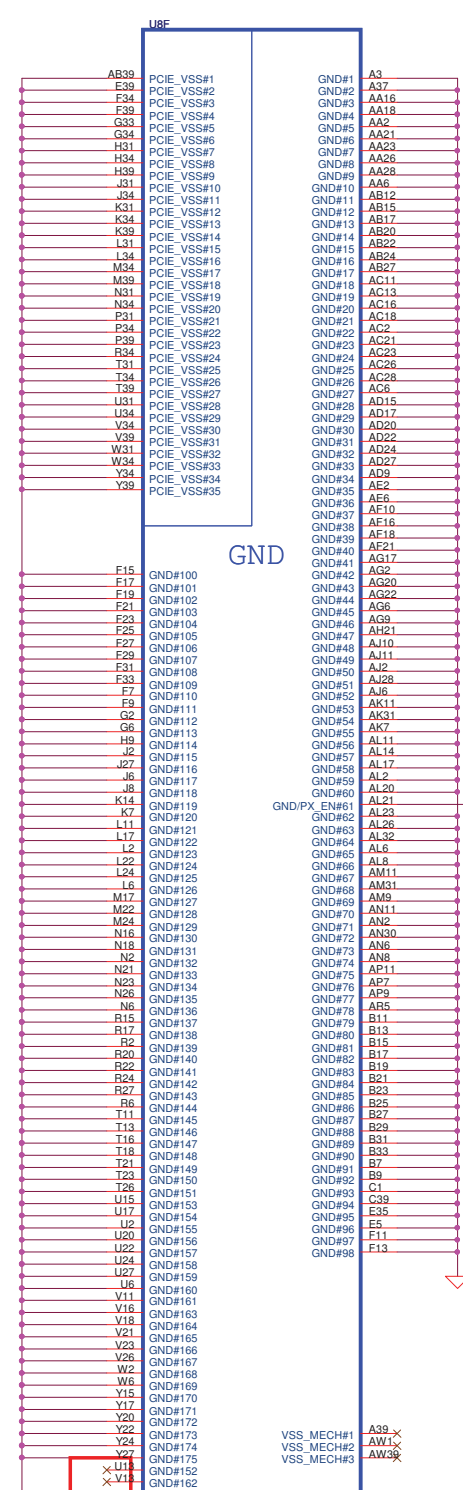


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DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler :
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

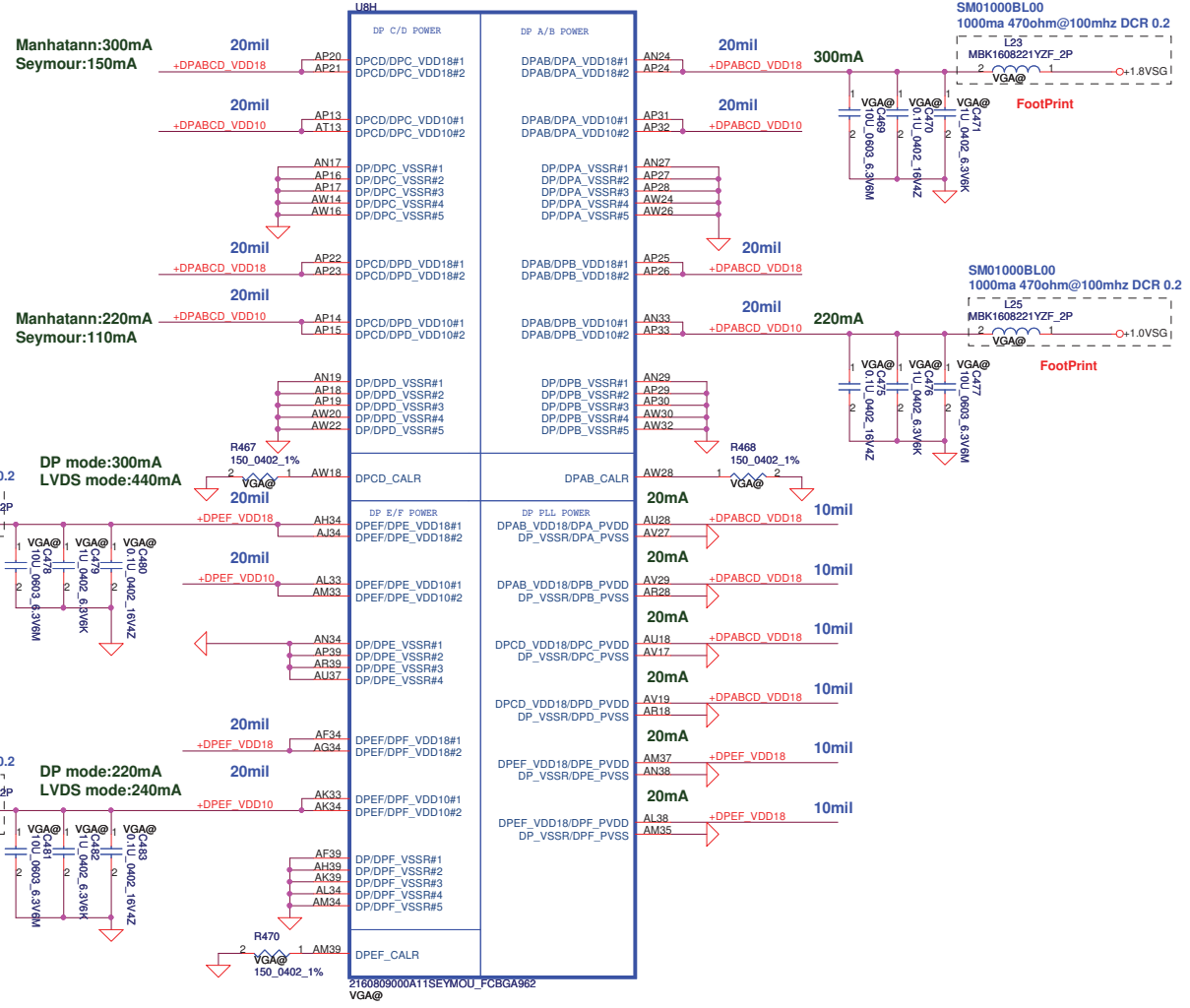
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
MBK1608221YZF_2P
+1.8VSG
VGA@
FootPrint

PX_EN: PU at P.20
SBIOS will control VGA power on/off.
High :BACO mode enable
LOW:BACO disable

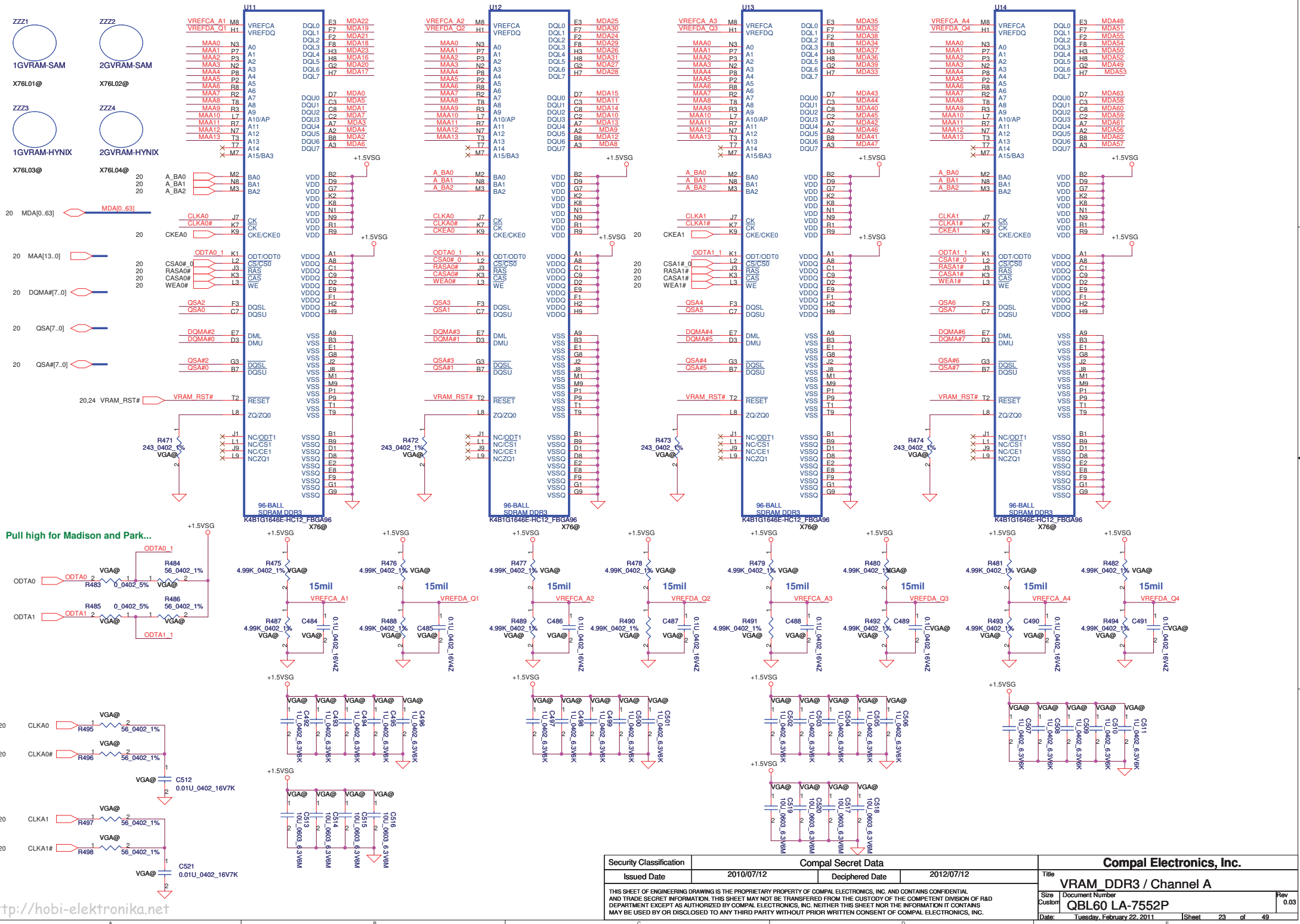
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
MBK1608221YZF_2P
+1.0VSG
VGA@
FootPrint

Park/Madison :AL21:left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

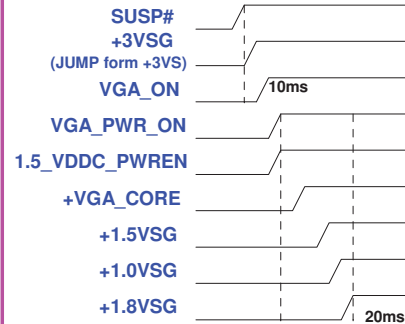


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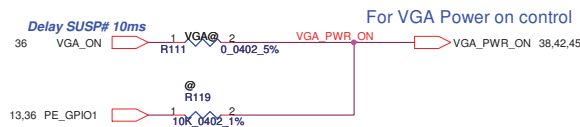
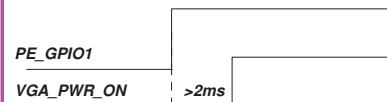




Power Sequence of Whistler and Seymour



For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

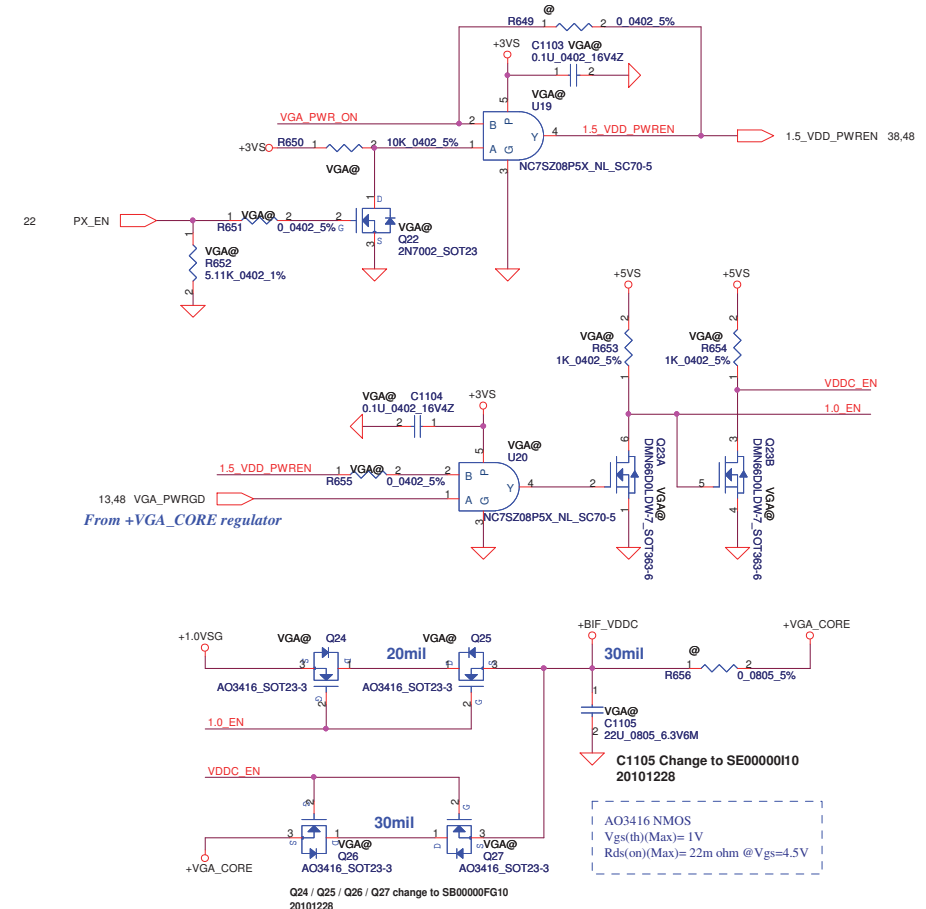


VGA Muxless with BACO Status Mapping table

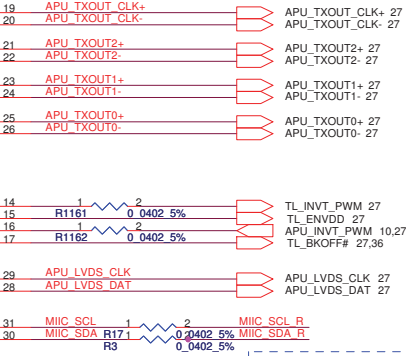
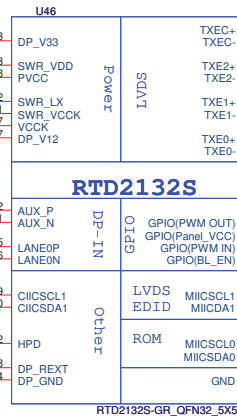
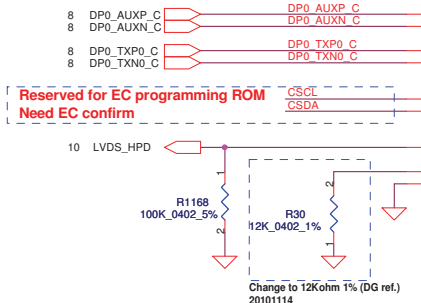
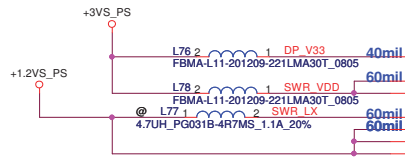
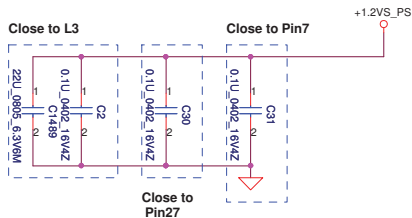
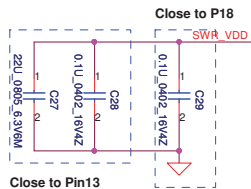
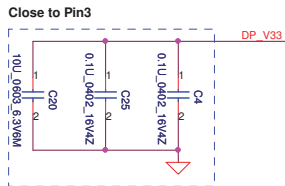
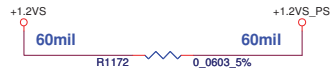
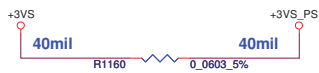
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table

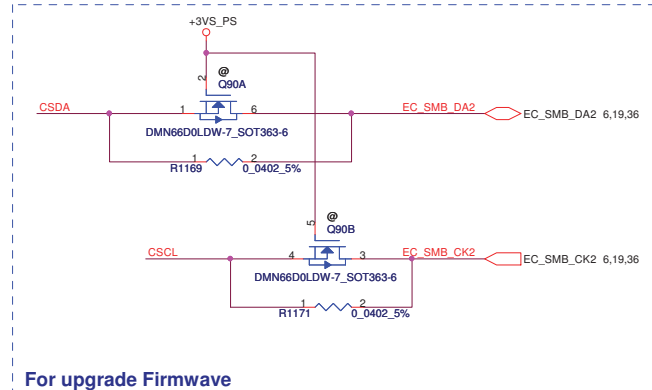
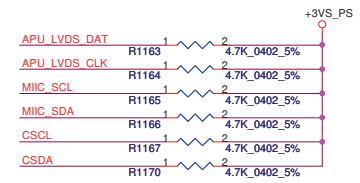
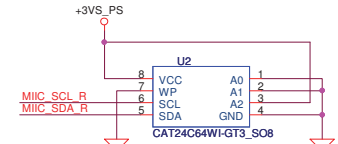
VGA_PWR_ON source signal	Whistler
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN



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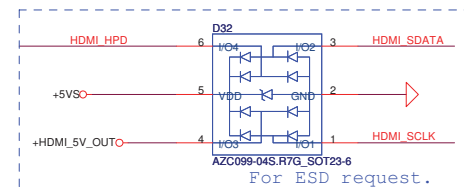
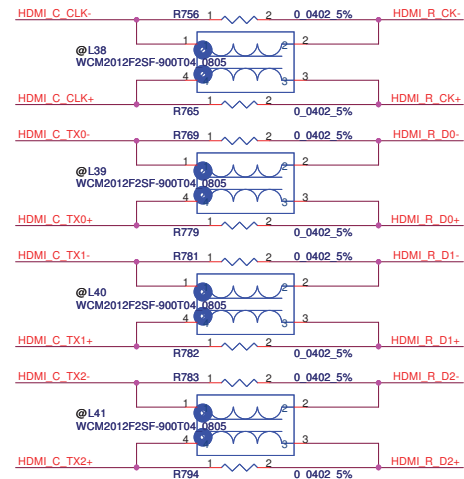
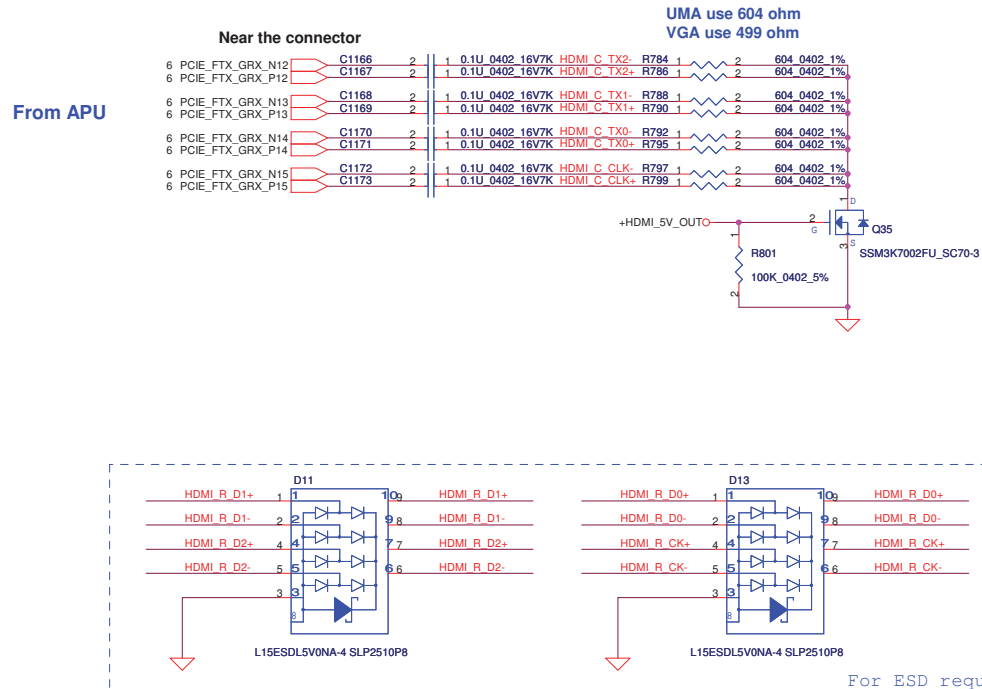
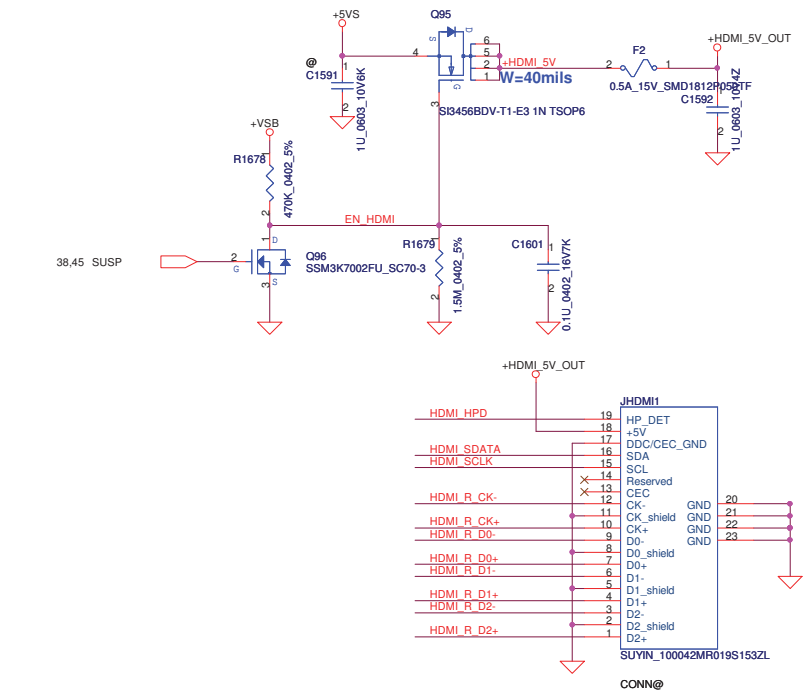
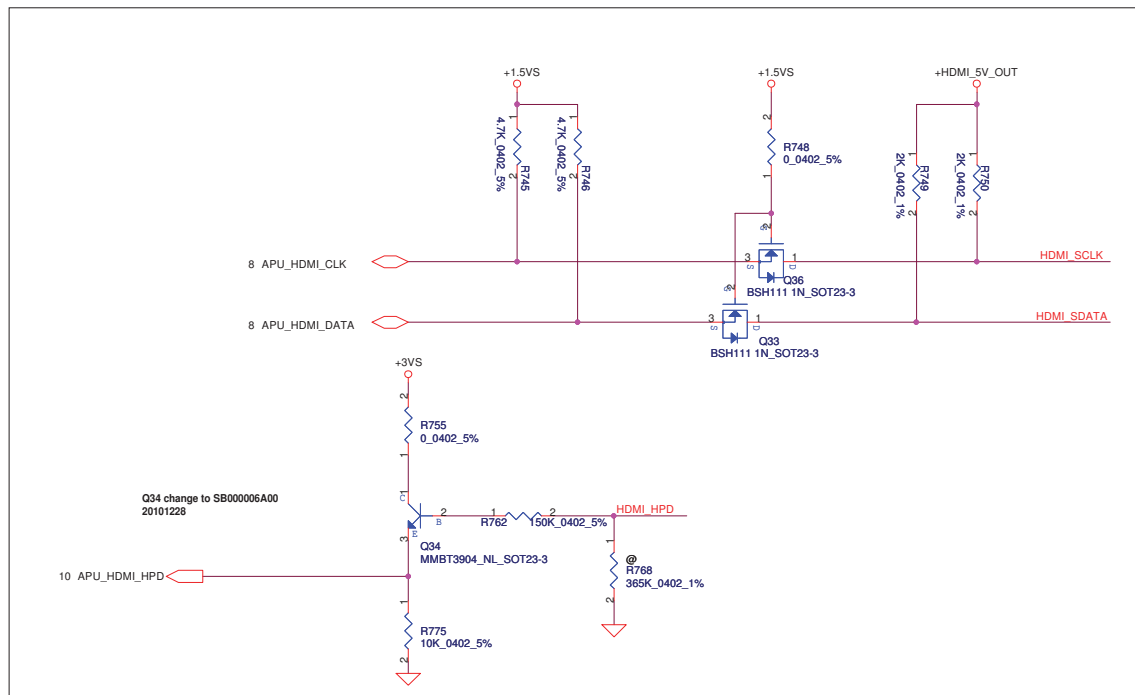
EEROM



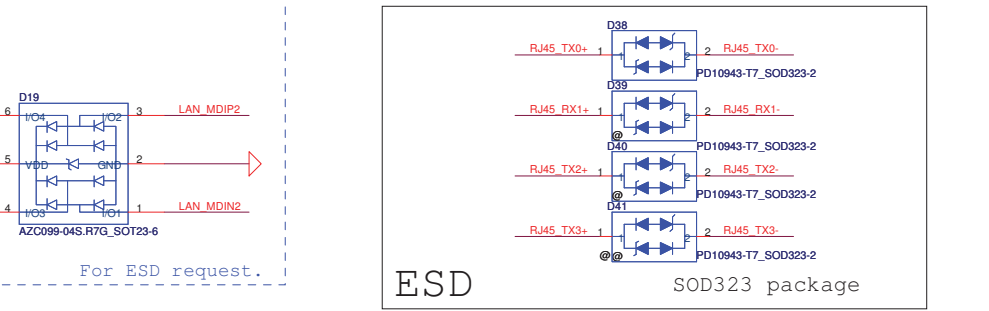
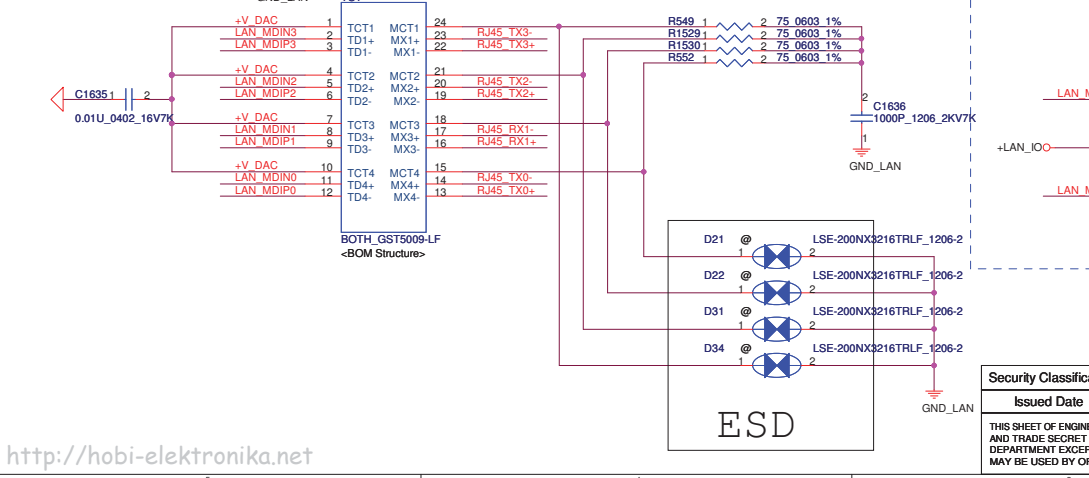
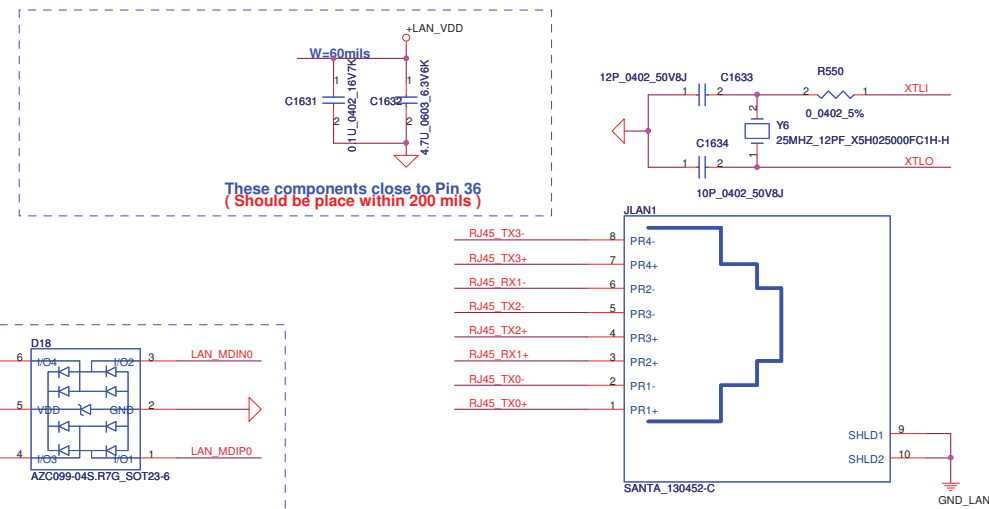
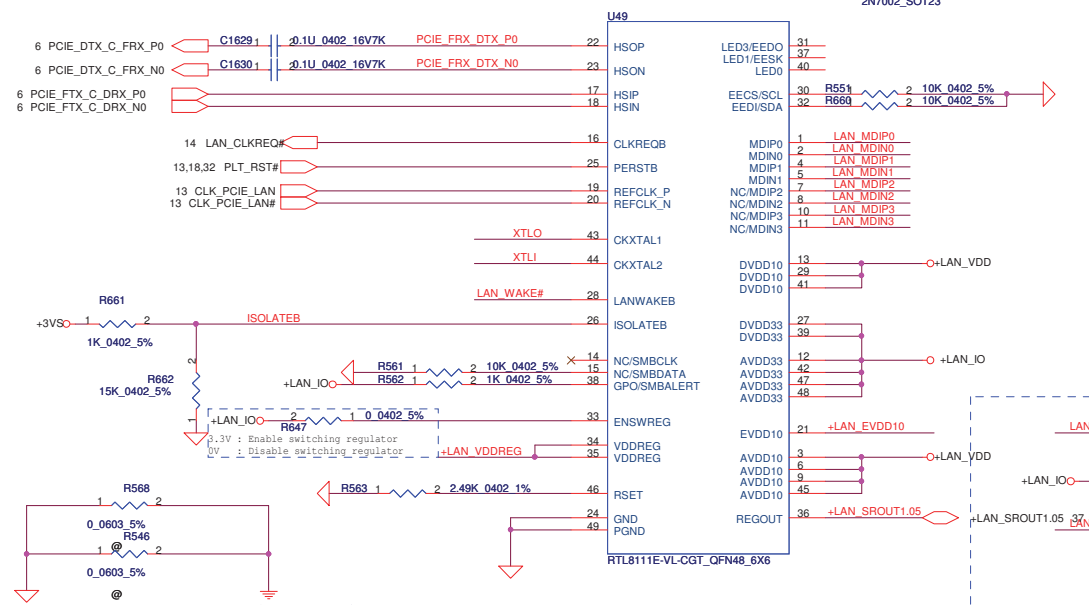
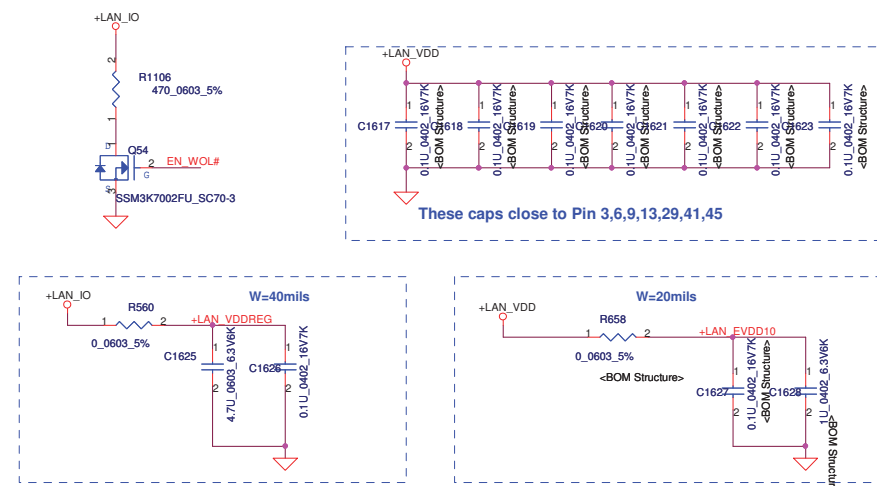
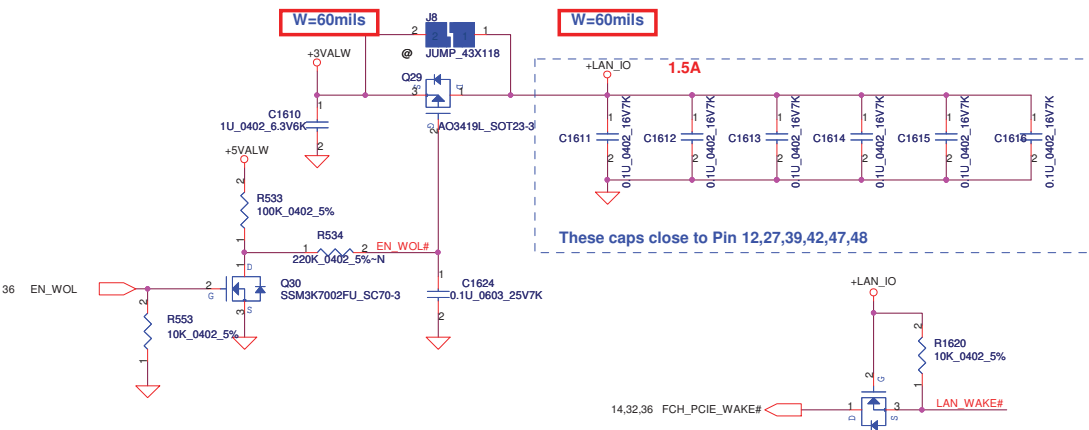
For upgrade Firmwave



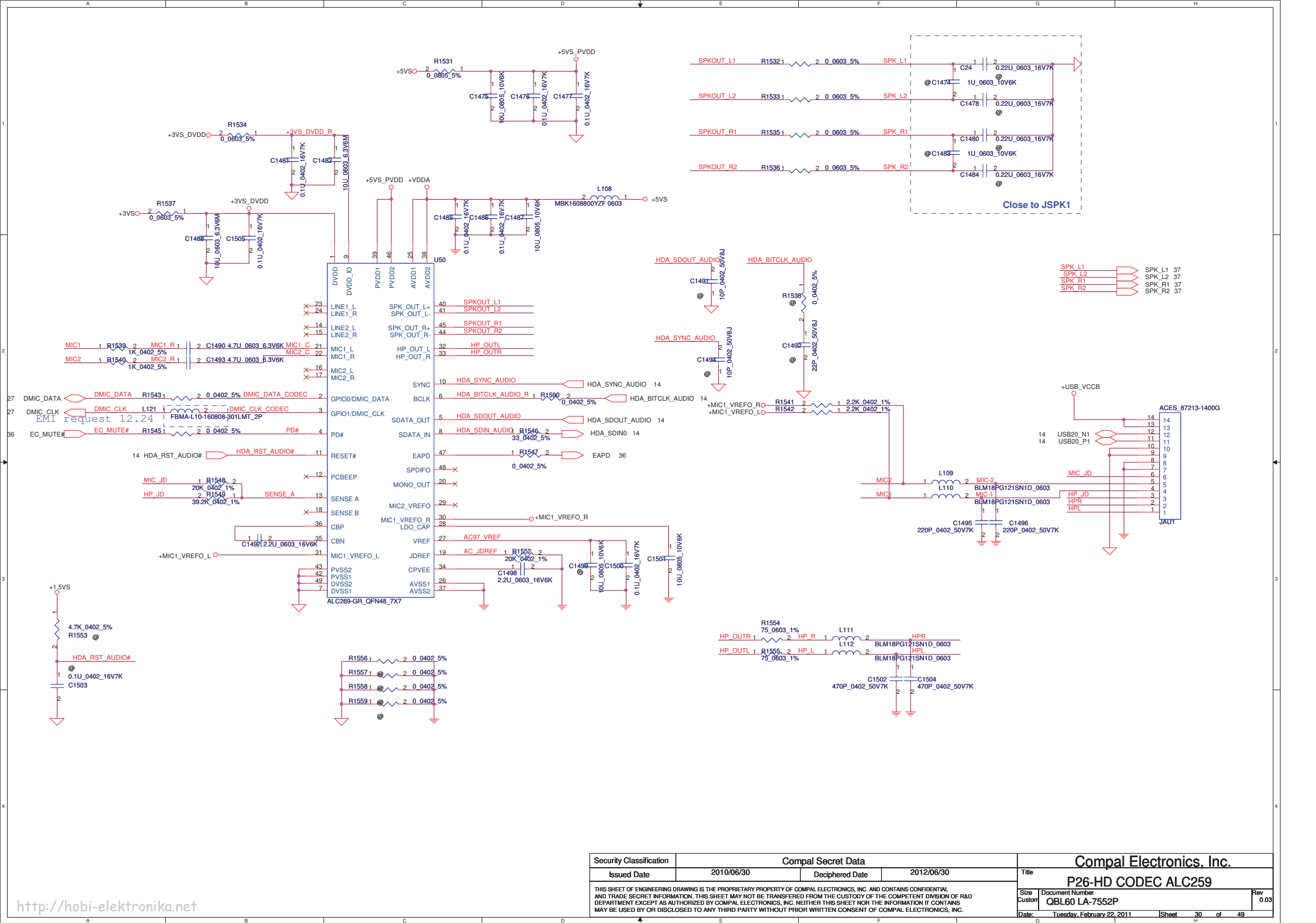
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						Size	Document Number	Rev 0.03
						Custord	QBL60 LA-7552P	
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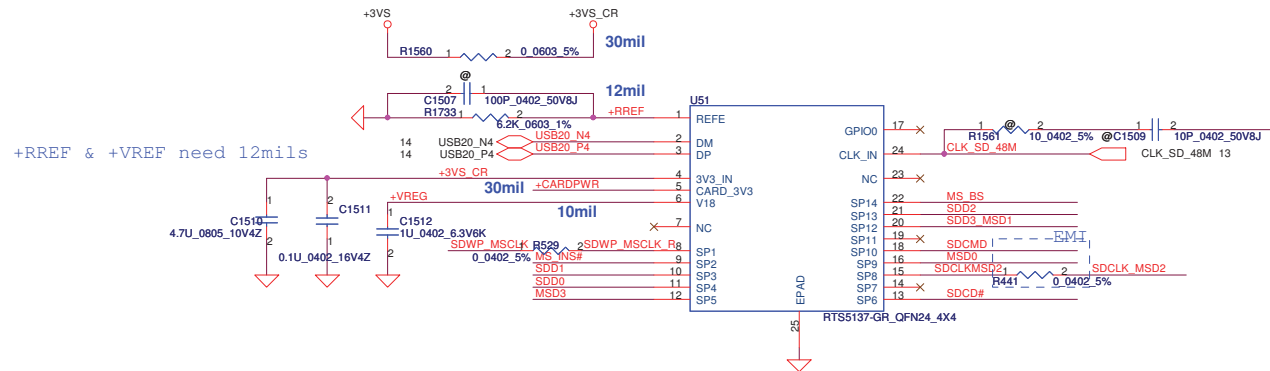
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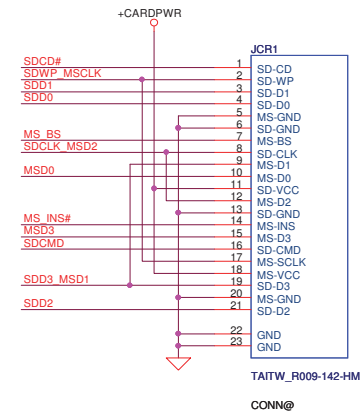
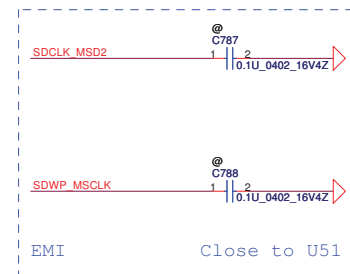
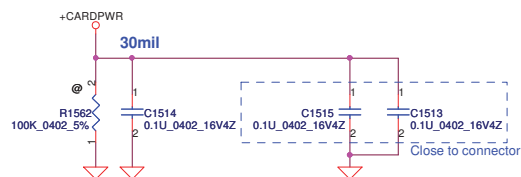
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Issued Date				2010/06/30				P26-HD CODEC ALC259			
Deciphered Date				2012/06/30				QBL60 LA-7552P			
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Card Reader RTS5137
(only SD/MMC/MS function)

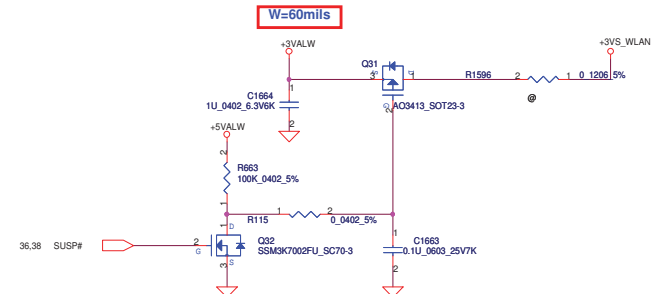


Card Reader Connector

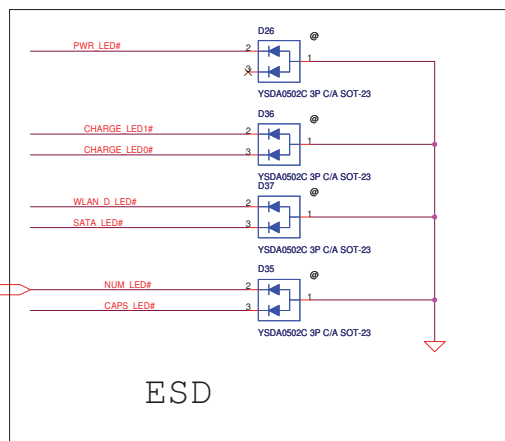


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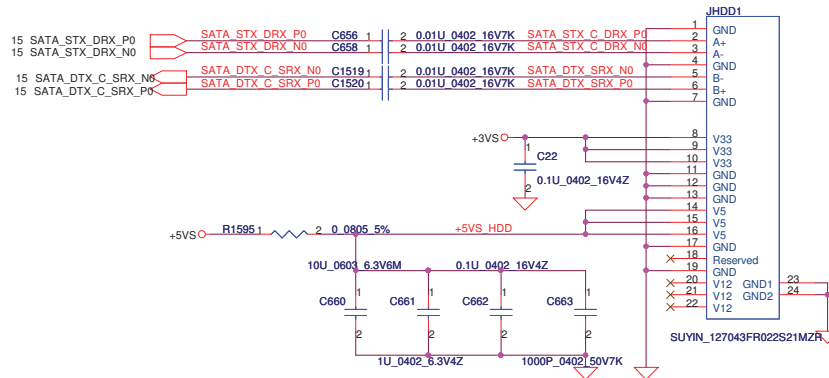
Mini-Express Card(WLAN/WiMAX)



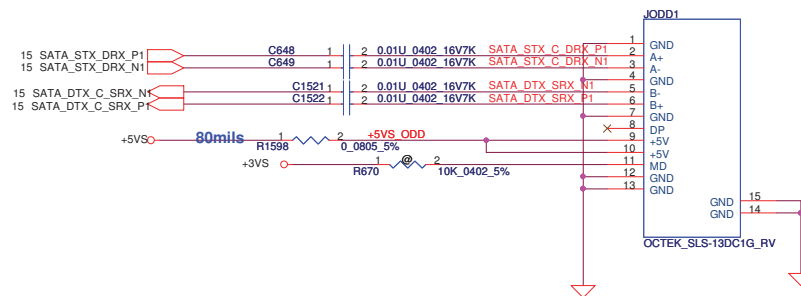
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LPC_A03	R1574	1	2 0 0402 5%	LPC_A03	1336	1	2 0 0402 5%
LPC_A02	R1576	1	2 0 0402 5%	LPC_A02	1336	1	2 0 0402 5%
LPC_A01	R1578	1	2 0 0402 5%	LPC_A01	1336	1	2 0 0402 5%
LPC_A00	R1579	1	2 0 0402 5%	LPC_A00	1336	1	2 0 0402 5%
PCI_RST#	R1580	1	2 0 0402 5%	PLT_RST#	1336	1	2 0 0402 5%
CLK_PCI_DB				CLK_PCI_DB	1336	1	2 0 0402 5%



SATA HDD Conn.



SATA ODD FFC Conn.

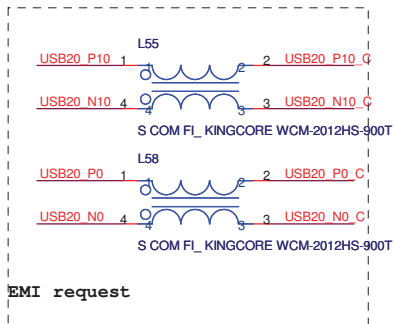
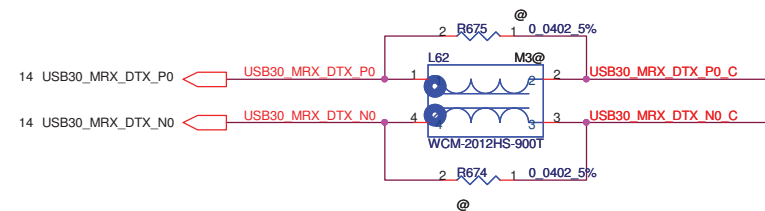
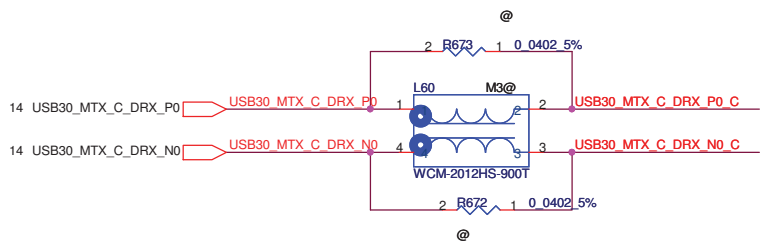
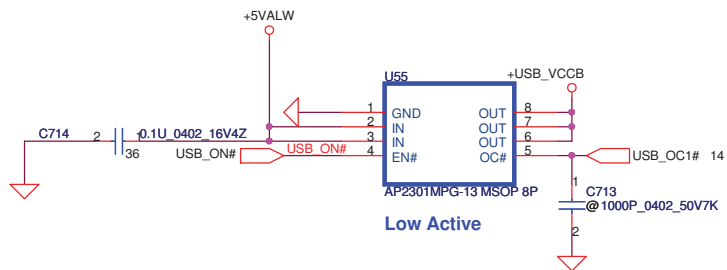
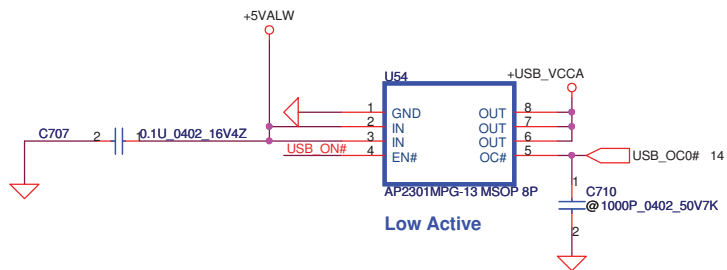


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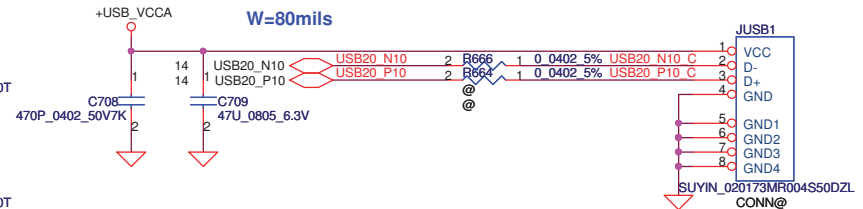
Compal Electronics, Inc.

P29-HDD & ODD CONN

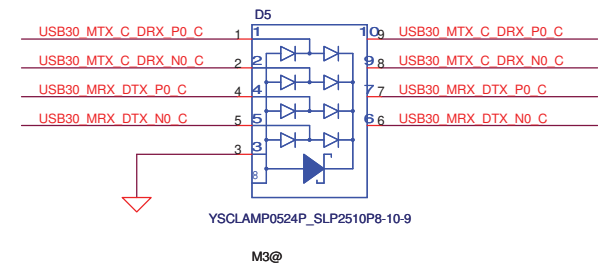
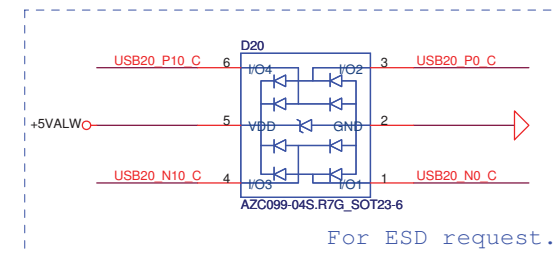
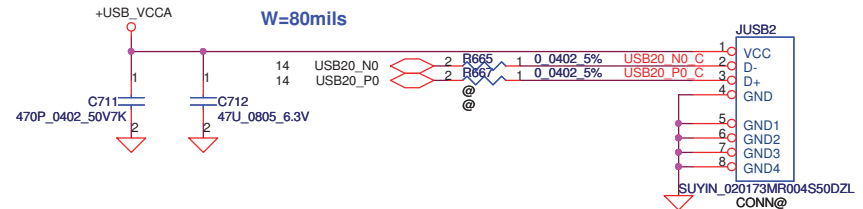
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Left USB Conn.

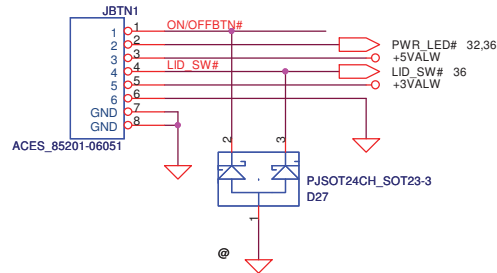
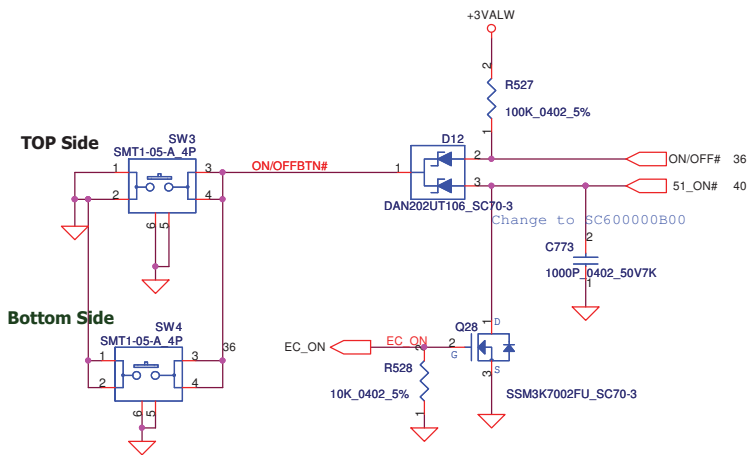


Left USB Conn.

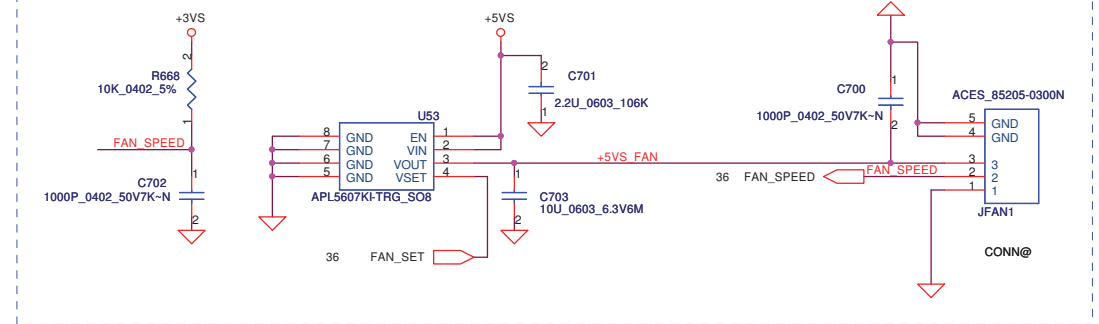


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Size	Custom	Document Number	QBL60 LA-7552P	Rev	0.03
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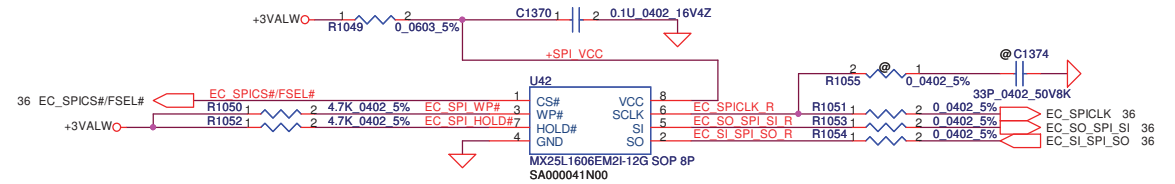
ON/OFF switch **Power Button**



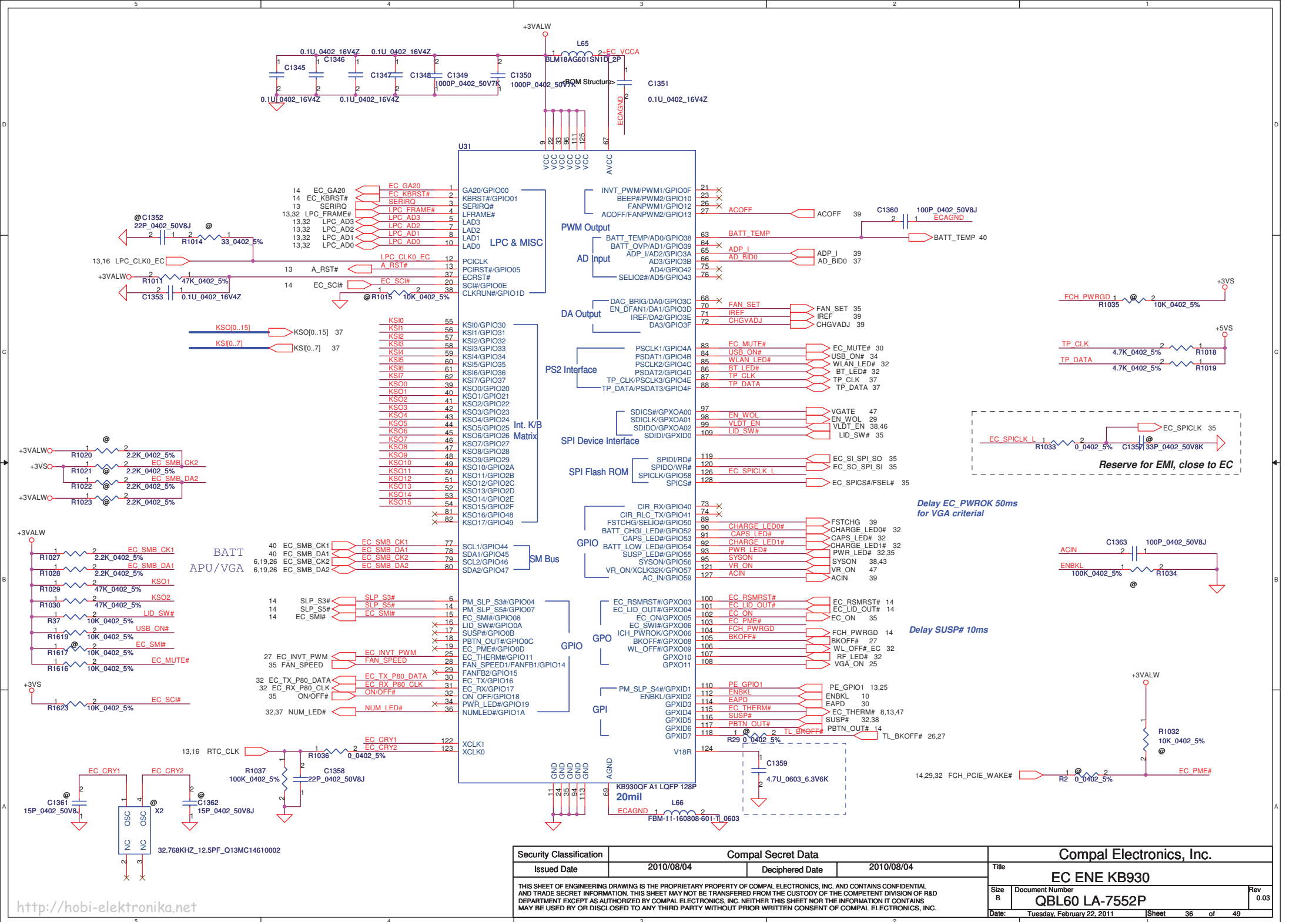
Fan Control Circuit



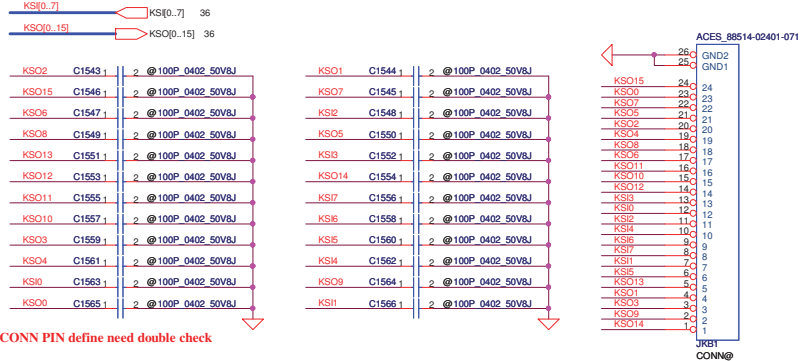
EC BIOS ROM



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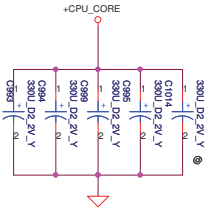


INT_KBD Conn.

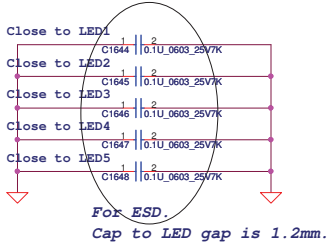
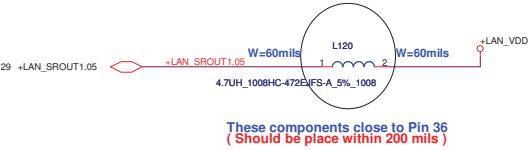
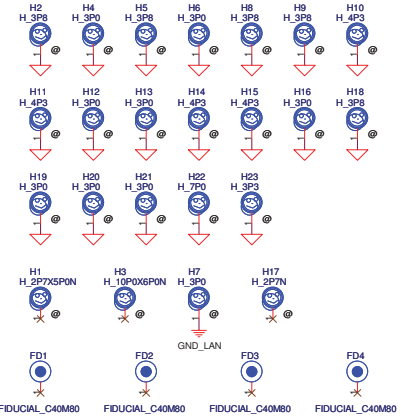
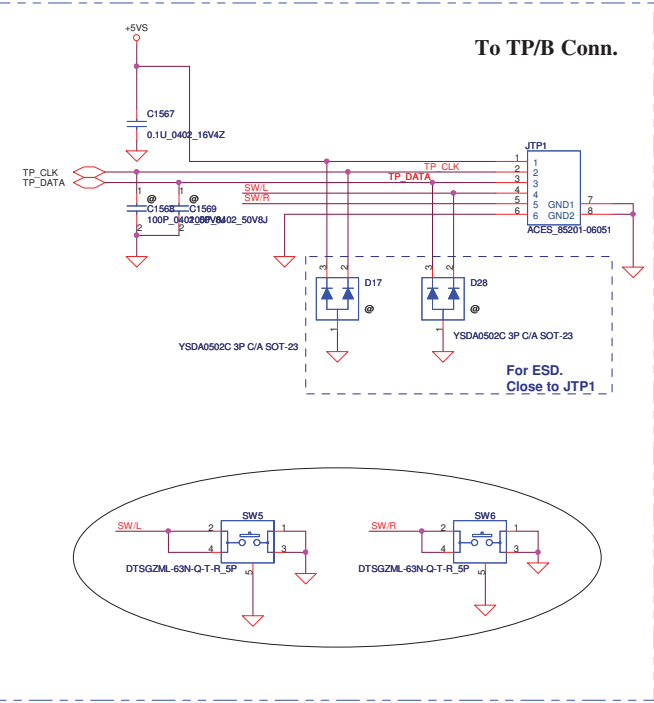


ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V

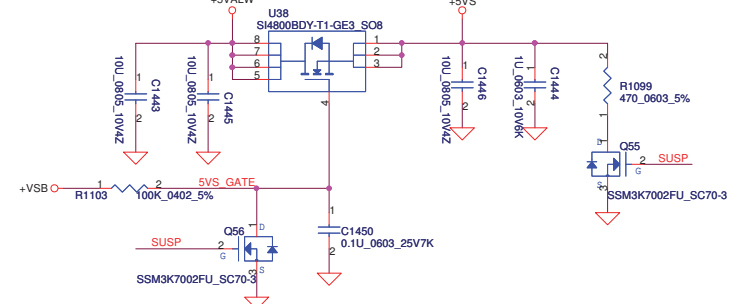
P9 FS1 PWR/GND



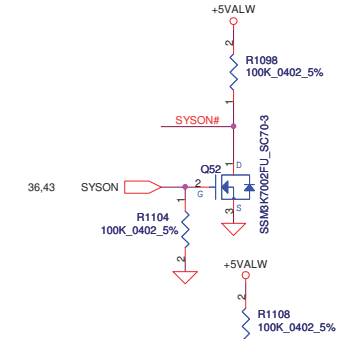
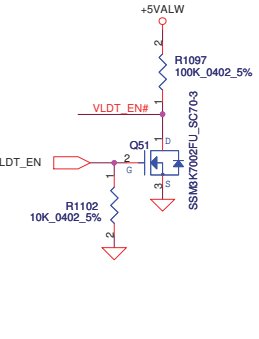
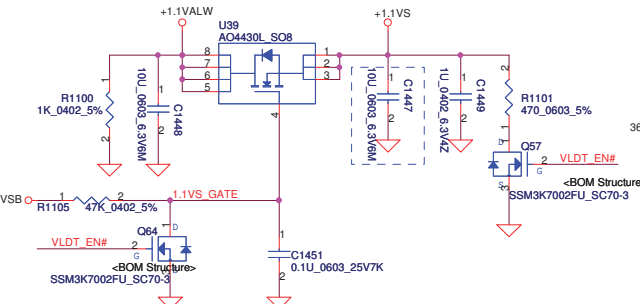
To TP/B Conn.



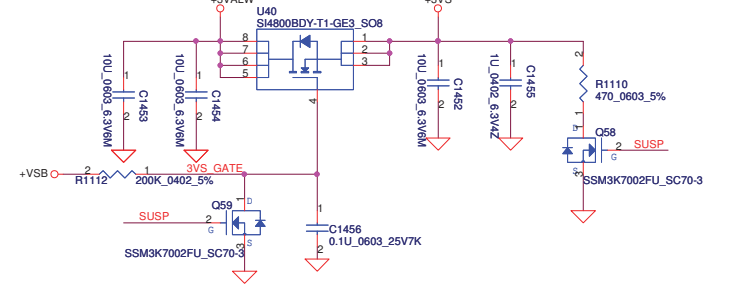
+5VALW TO +5VS (5A)



+1.1VALW TO +1.1VS (1.1A)

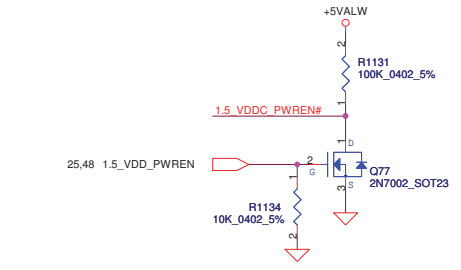
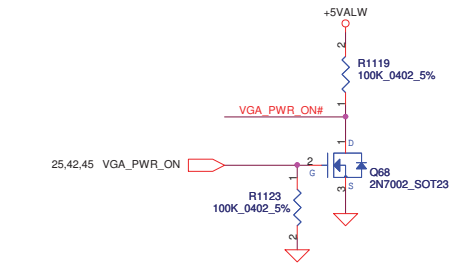
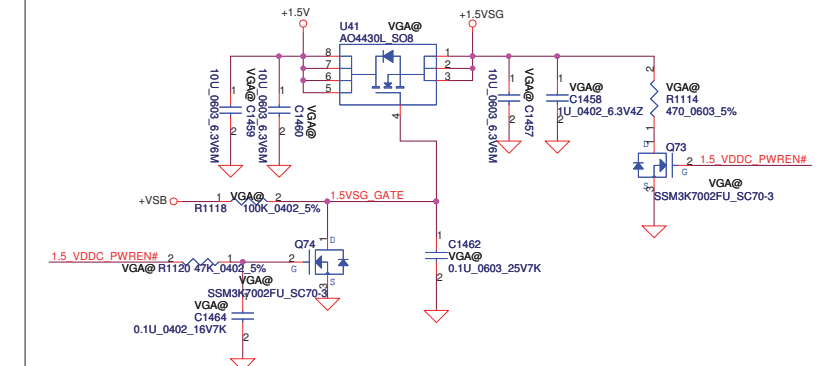


+3VALW TO +3VS (3.3A)

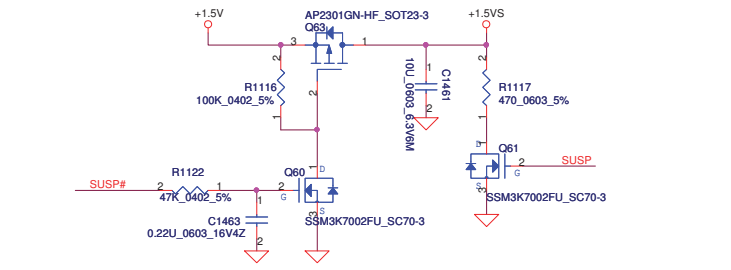


VGA Power

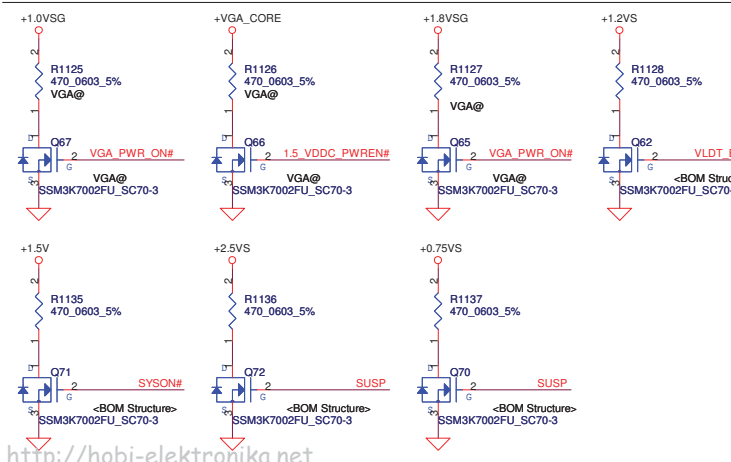
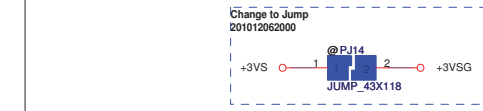
+1.5V to +1.5VSG (1.5A)



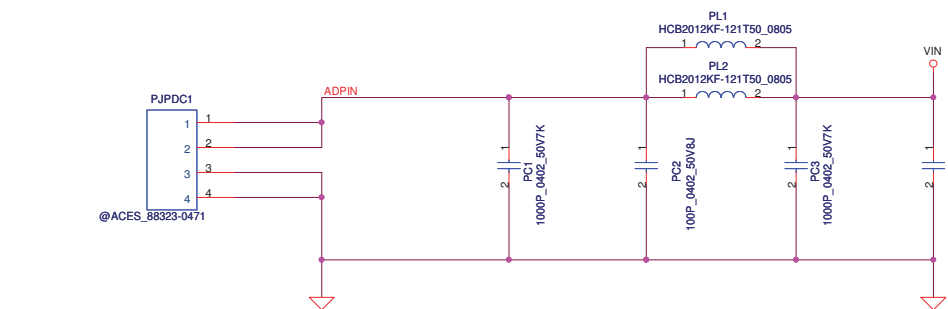
+1.5V TO +1.5VS (1.5A)



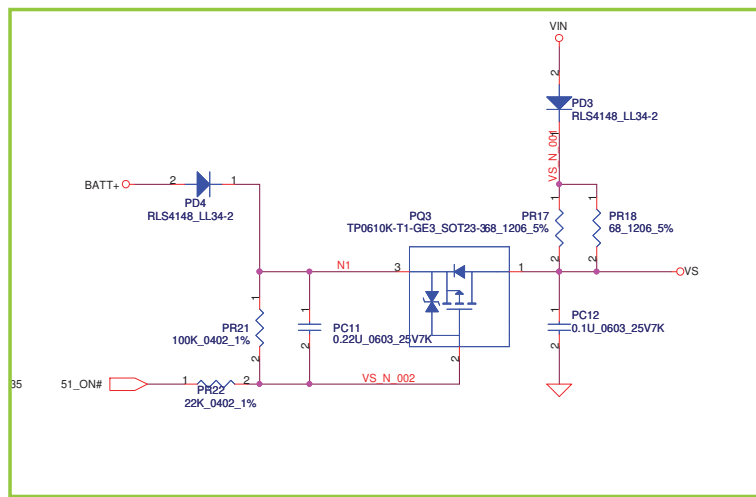
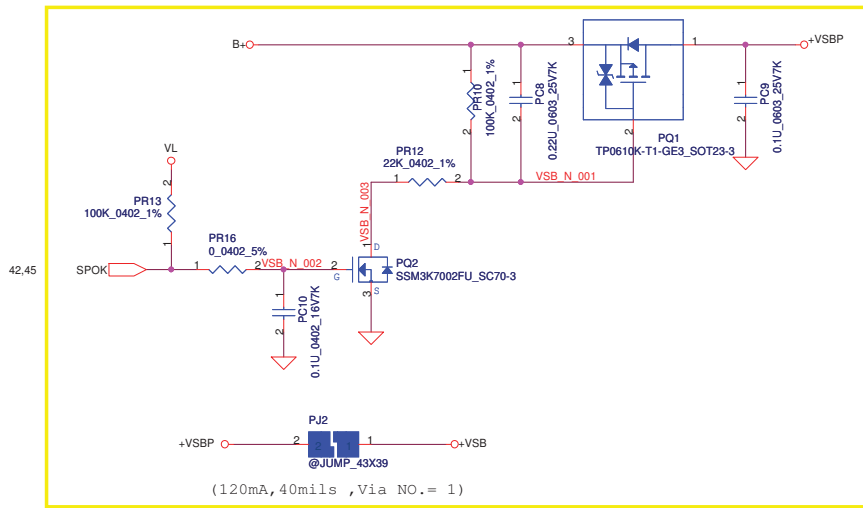
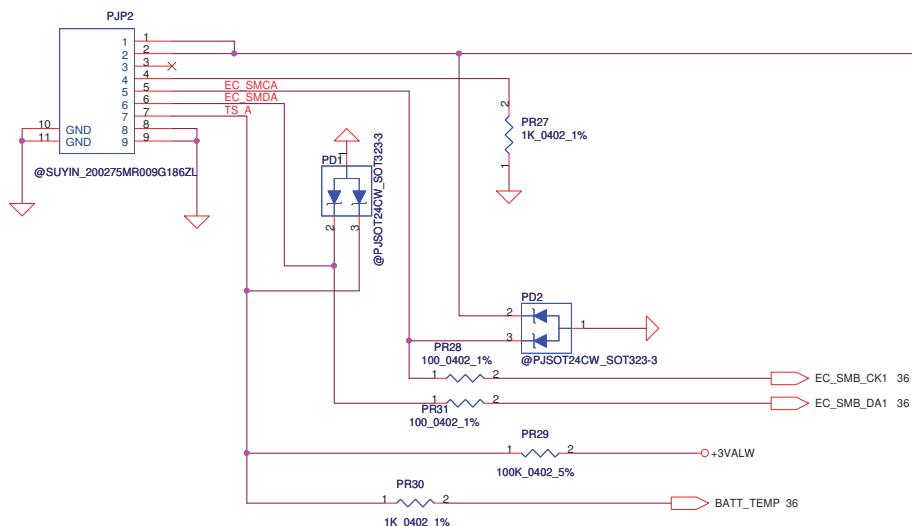
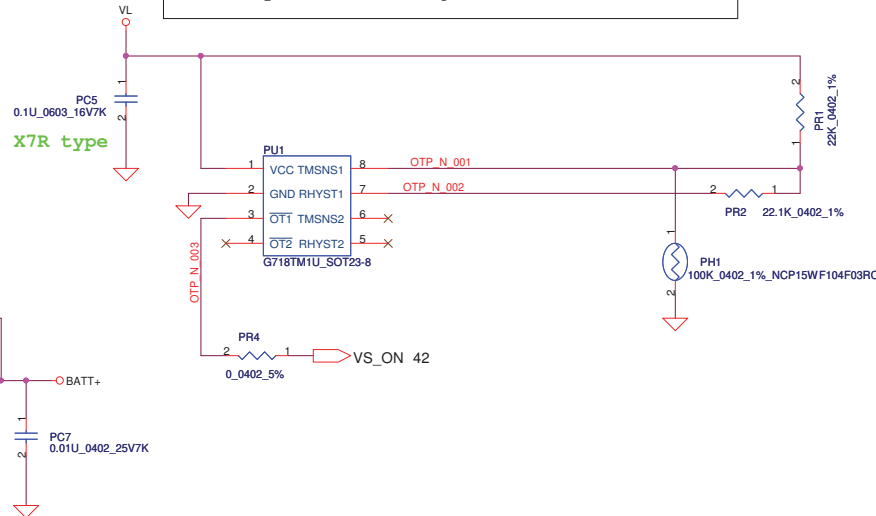
+3VS to +3VSG (3.3A)



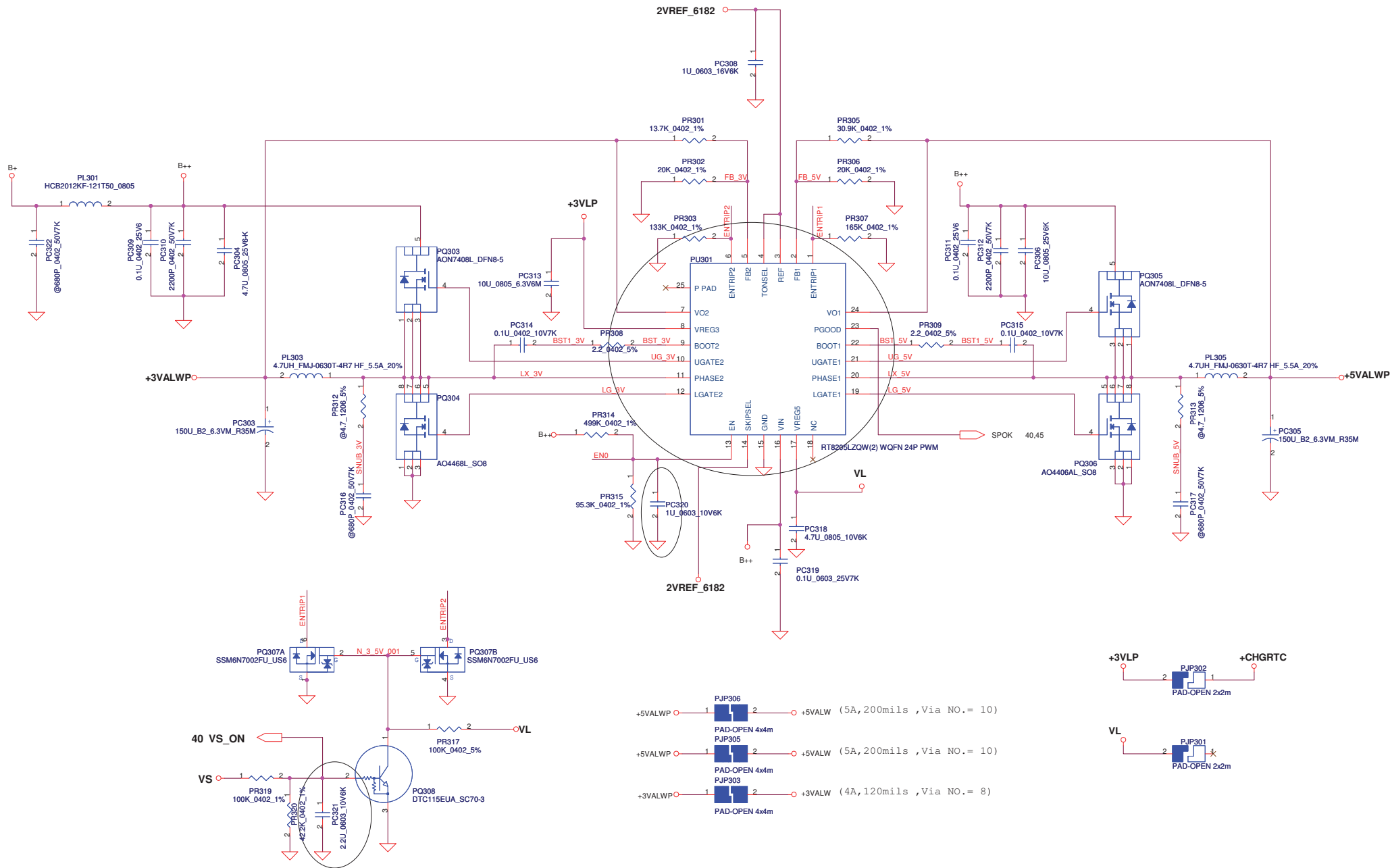
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PH1 under CPU botten side :
CPU thermal protection at 92 + -3 degree C
Recovery at 80 + -3 degree C

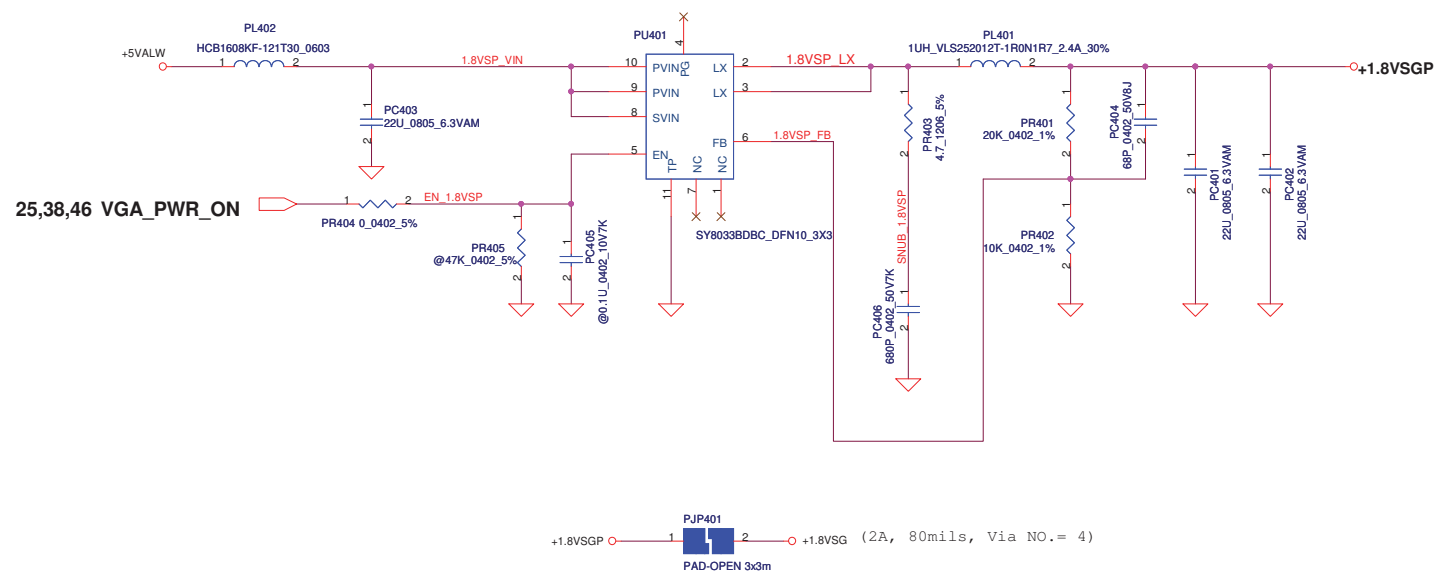


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EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

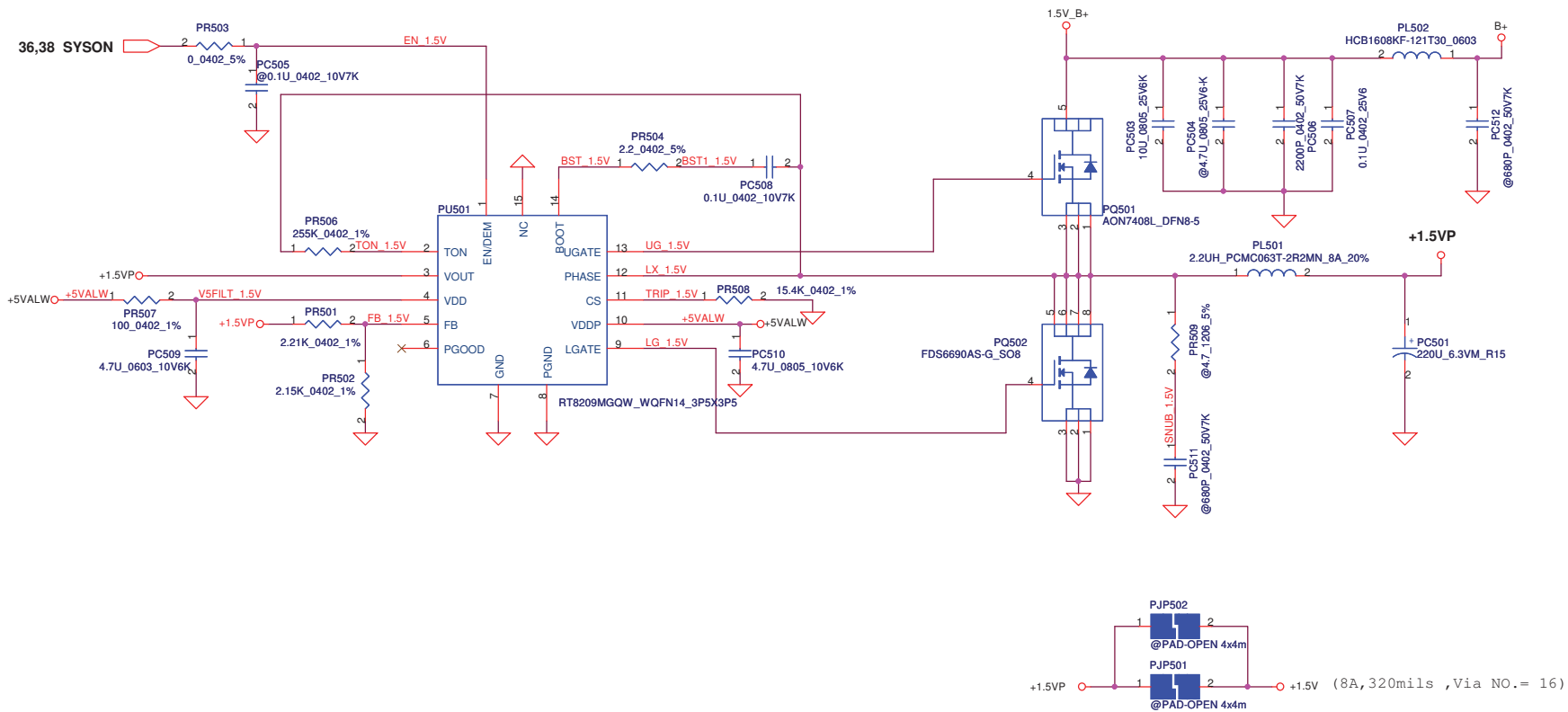
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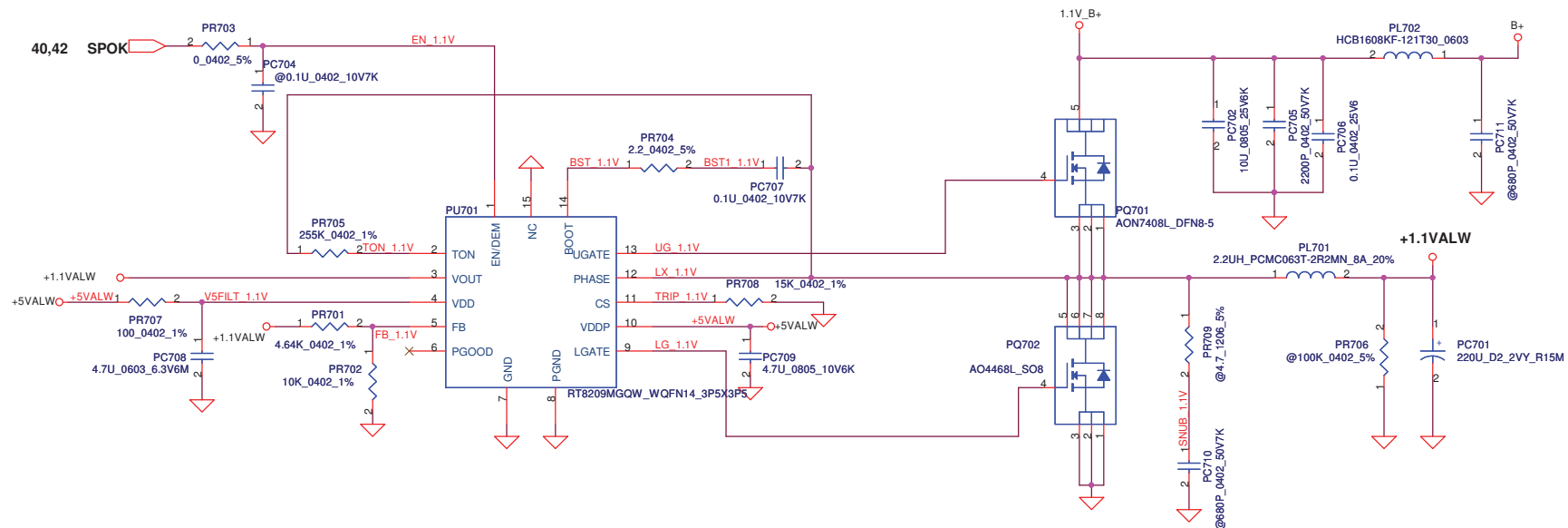
$$\langle V_o = 1.8V \rangle \quad V_{FB} = 0.6V$$

$$V_o = V_{FB} * (1 + PR401 / PR402) = 0.6 * (1 + 20K / 10K) = 1.8V$$

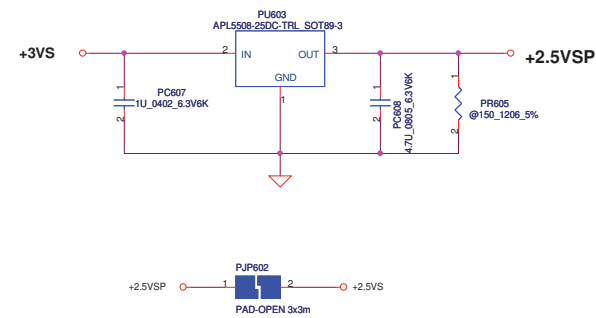
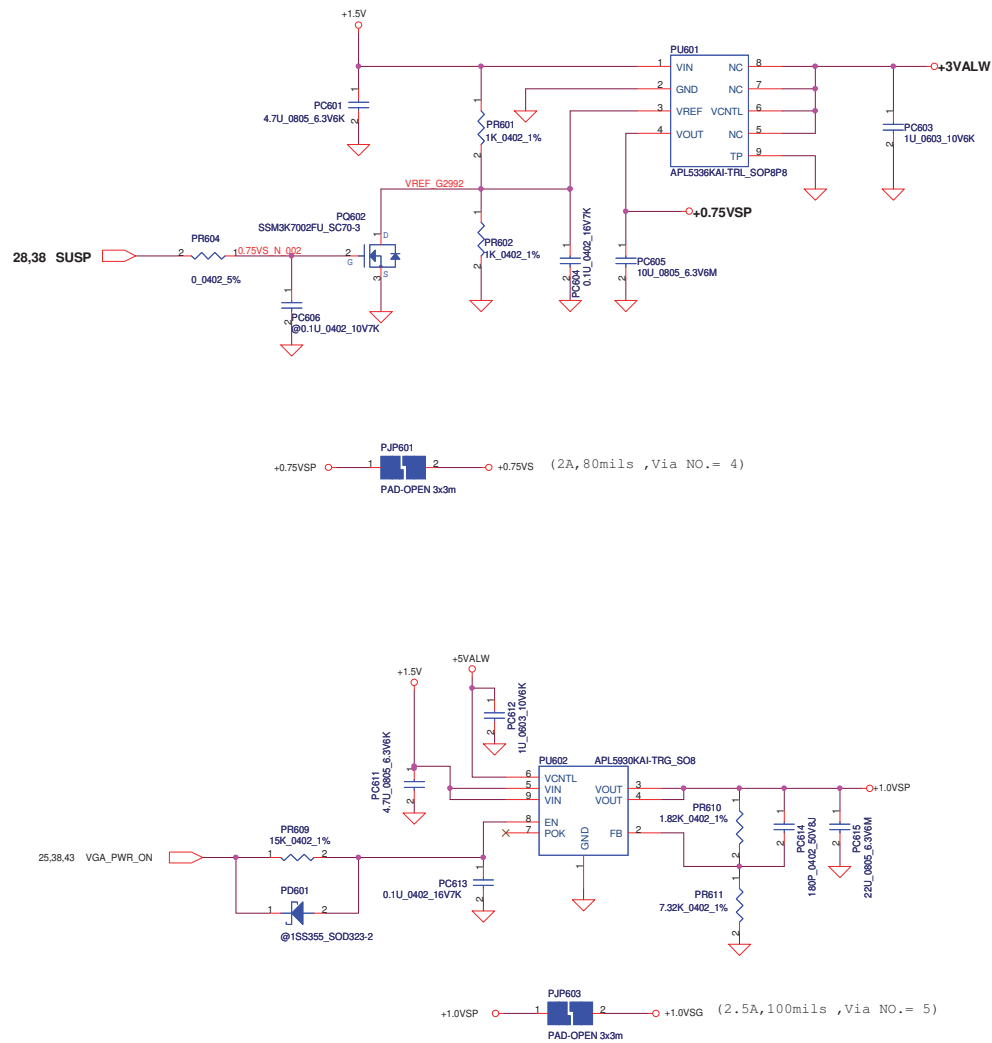
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					0.1



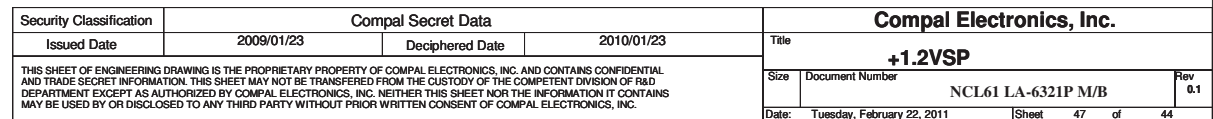
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				PWR_+CPU_CORE+CPU_CORE_NB			
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