

Greenland Napa

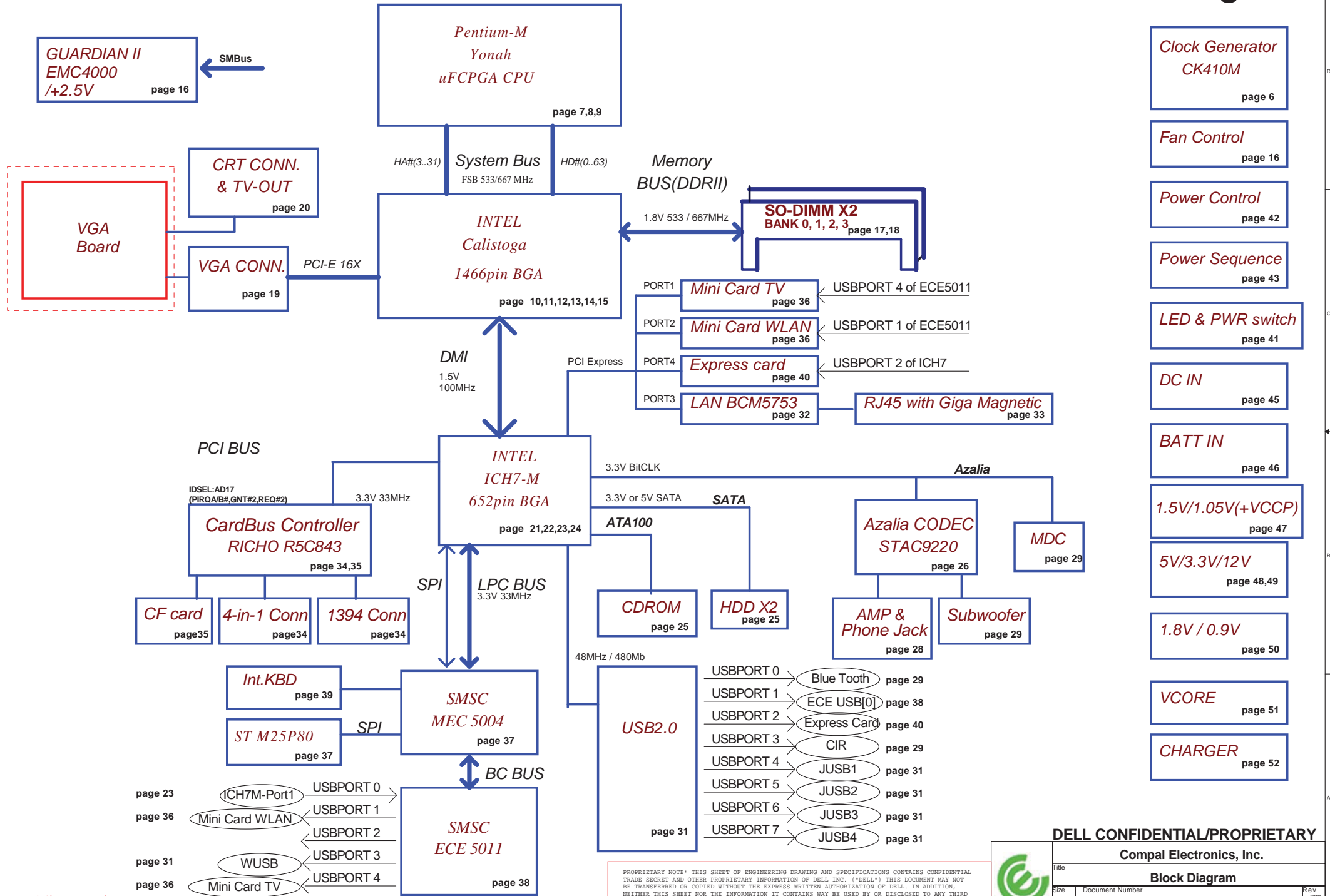
REV : X03G
12/28/2005

@ : Nopop Component

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DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
Title			
Cover Sheet			
Size	Document Number		Rev
Custom	Greenland-LA2732P		X03
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Block Diagram

Greenland-LA2732P

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PM TABLE

power plane State	+3VALW +5VALW	+3VSUS +5VSUS +1.8VSUS	+12VRUN +5VRUN +3VRUN +2.5VRUN +1.8VRUN +1.5VRUN +VCC_CORE +VCCP +0.9V_DDR_VTT
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	2	D,C

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD TV
Lane 2	MINI CARD WLAN
Lane 3	GIGA LAN
Lane 4	EXPRESS CARD

ICH7M USB TABLE

USB PORT#	DESTINATION
0	BLUETOOTH
1	USB[0] of ECE5011
2	Express Card
3	CIR
4	JUSB1(M/B)
5	JUSB2(M/B)
6	JUSB3(USB/BD)
7	JUSB4(USB/BD)

ECE5011 USB TABLE

USB PORT#	DESTINATION
0	USB[1] of ICH7M
1	Mini Card WLAN
2	
3	WUSB
4	Mini Card TV

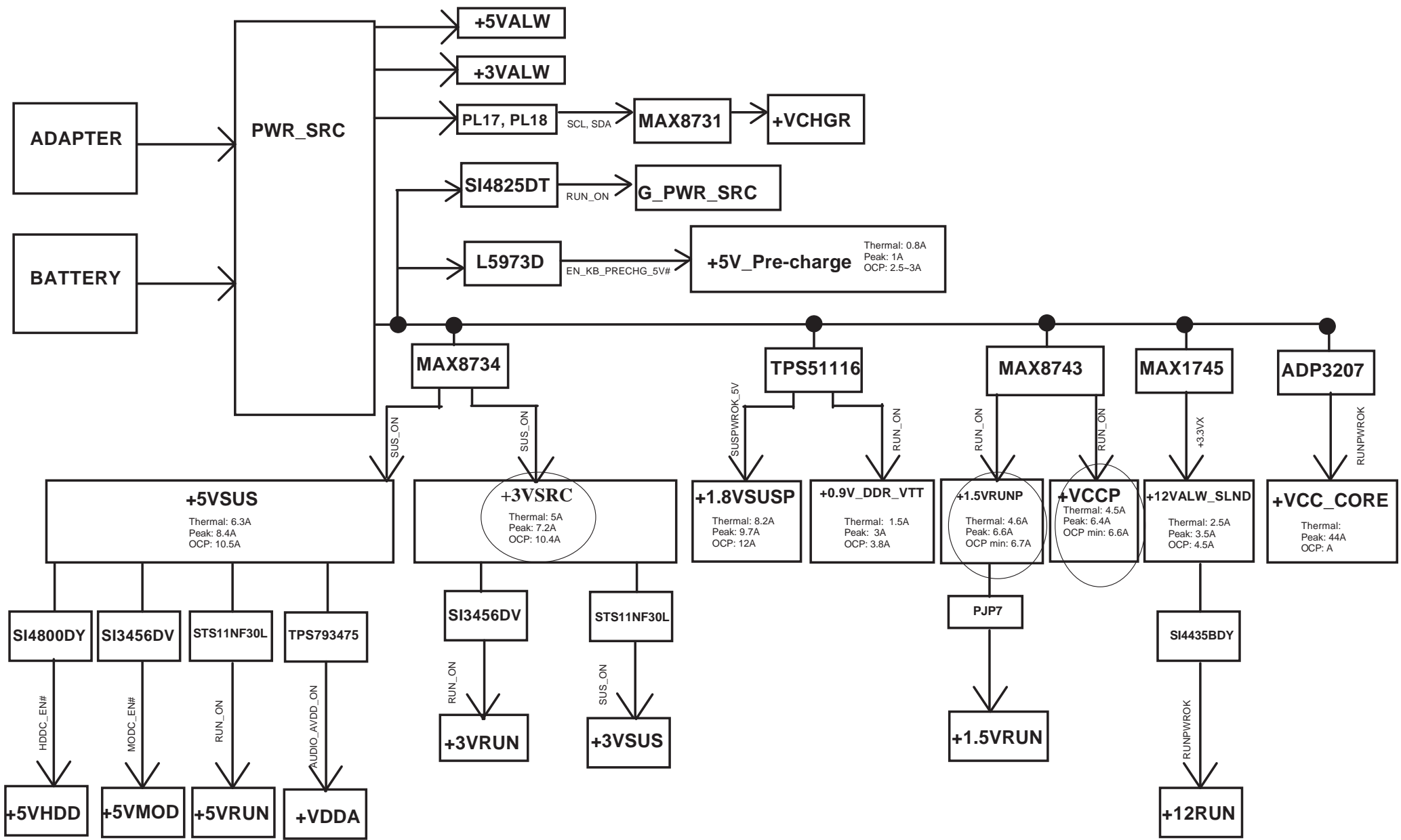
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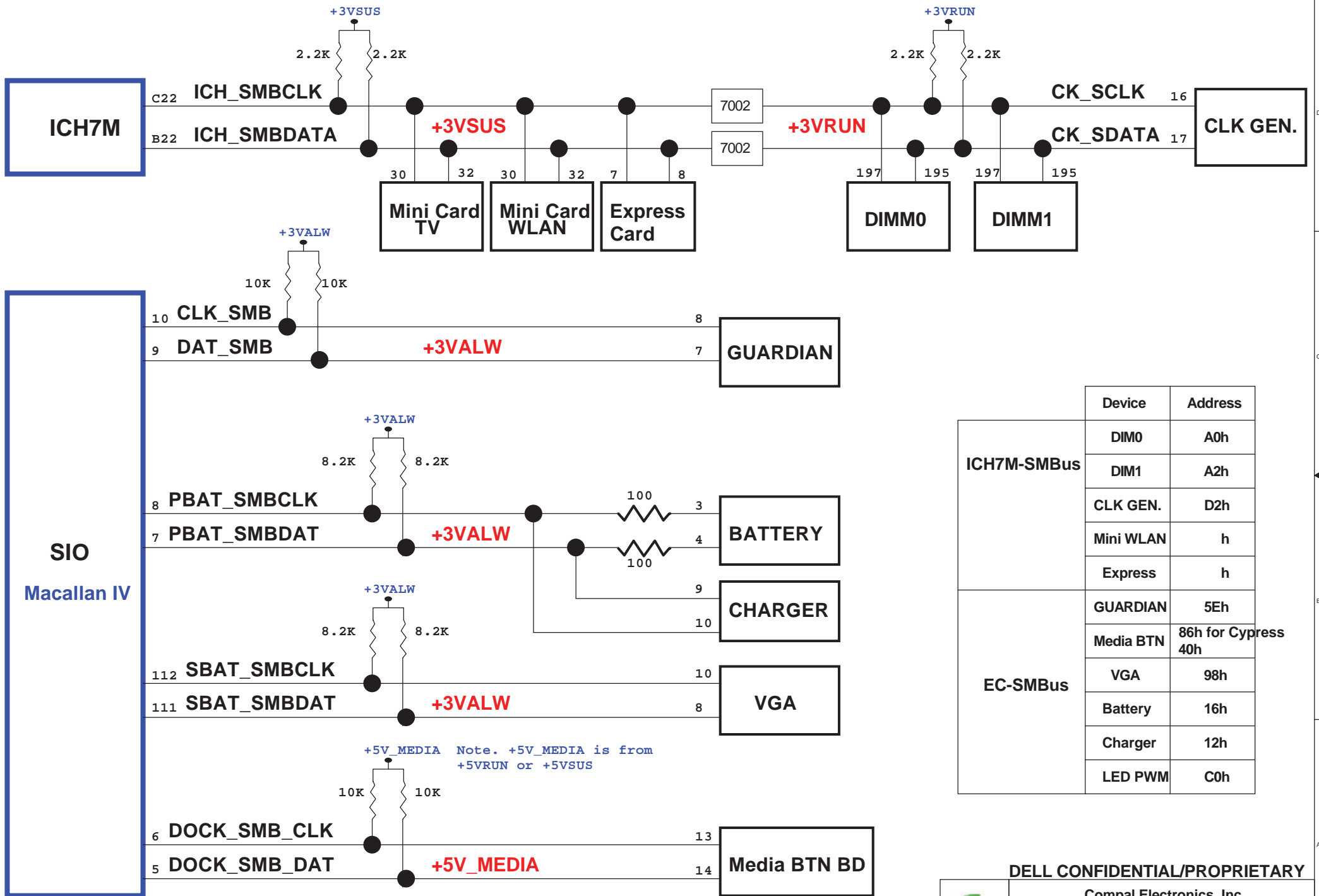
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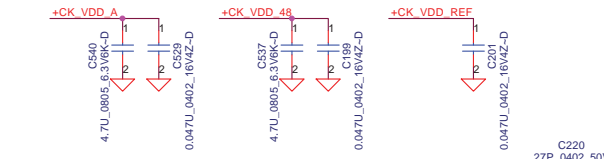
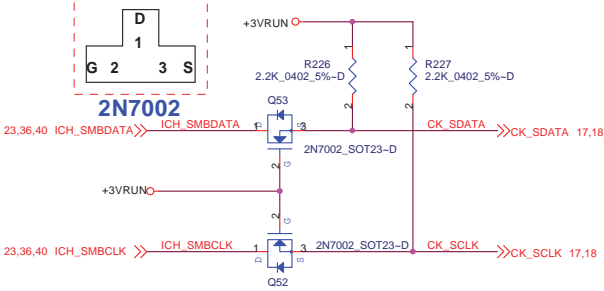




	Device	Address
ICH7M-SMBus	DIM0	A0h
	DIM1	A2h
	CLK GEN.	D2h
	Mini WLAN	h
	Express	h
EC-SMBus	GUARDIAN	5Eh
	Media BTN	86h for Cypress 40h
	VGA	98h
	Battery	16h
	Charger	12h
	LED PWM	C0h

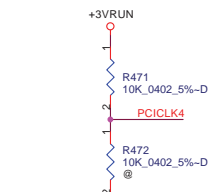
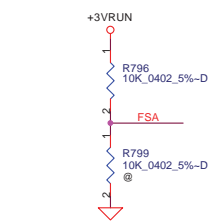
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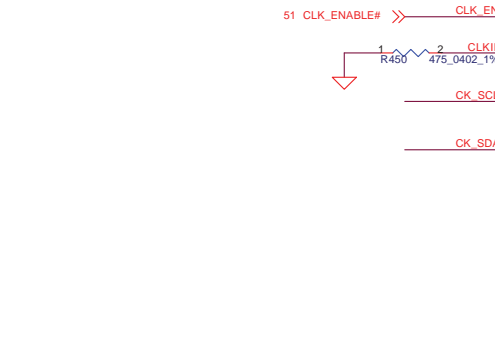
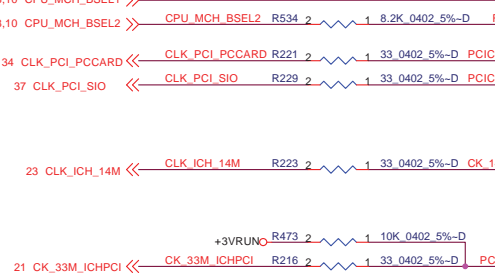
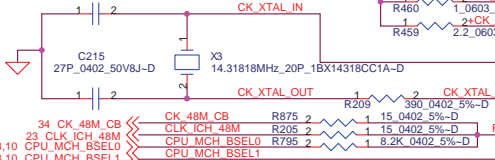
FSC	FSB	FSA	CPU MHz	SRC MHz	PCI MHz
CLKSEL0	CLKSEL1	CLKSEL2			
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	0	RESERVED		

Table : ICS 954305AK / Silero SLG84450VTR



<http://tobi-elektronika.net>

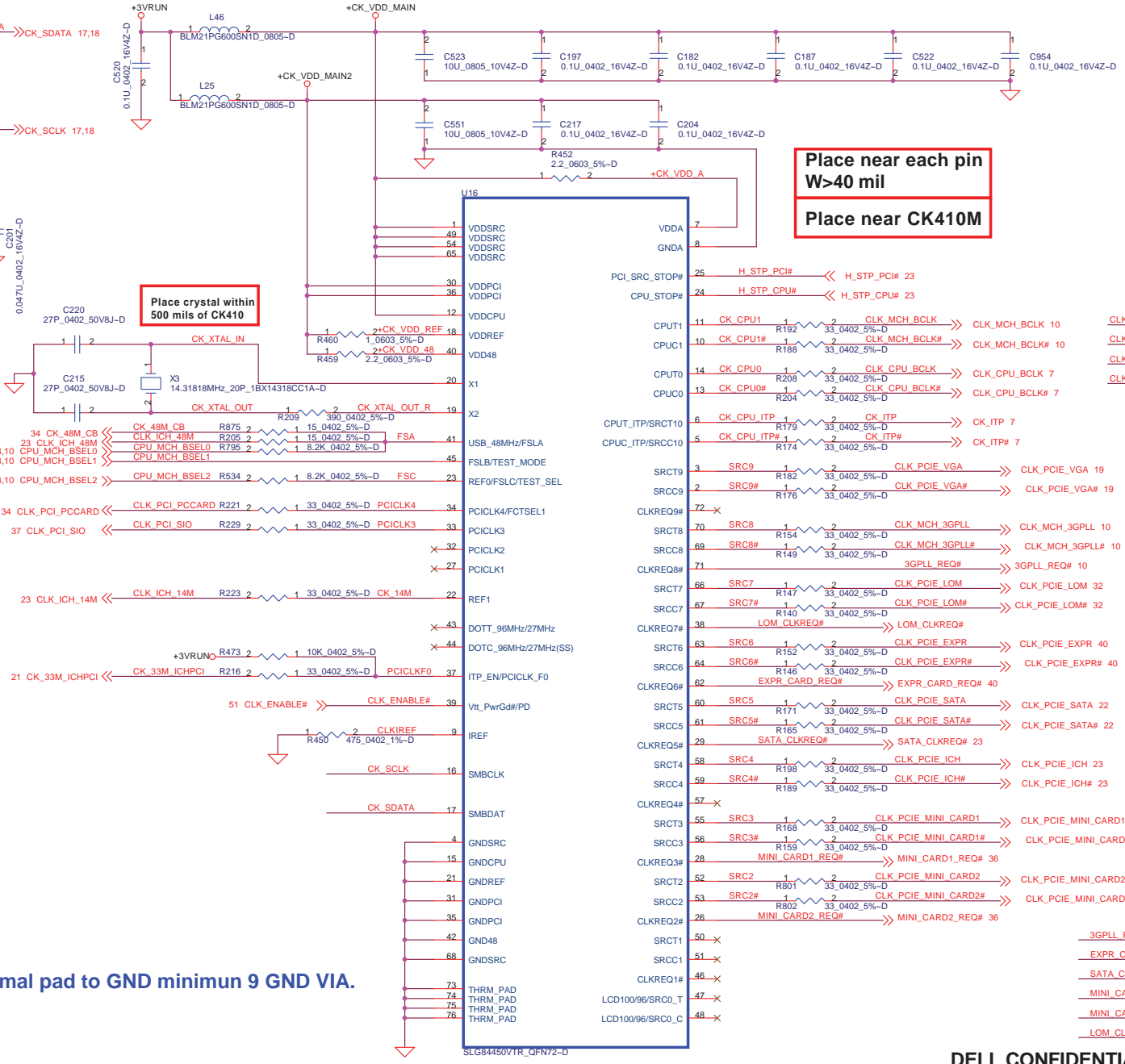
Place crystal within 500 mils of CK410



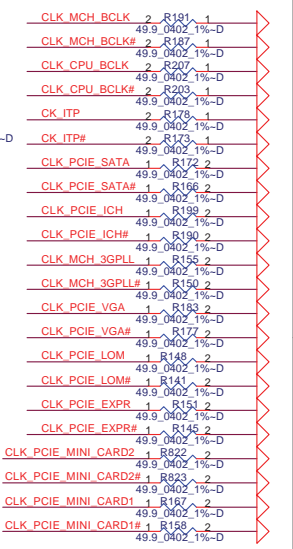
Note: Solder Thermal pad to GND minimum 9 GND VIA.

PCICLK4 = FCTSEL1

FCTSEL1	Pin 43	Pin 44	Pin 47	Pin 48
UMA	0	DOT96T	LCD100/96T	LCD100/96C
Discrete	1	27MHz	SRC0_T	SRC0_C



Place near each pin
W>40 mil
Place near CK410M

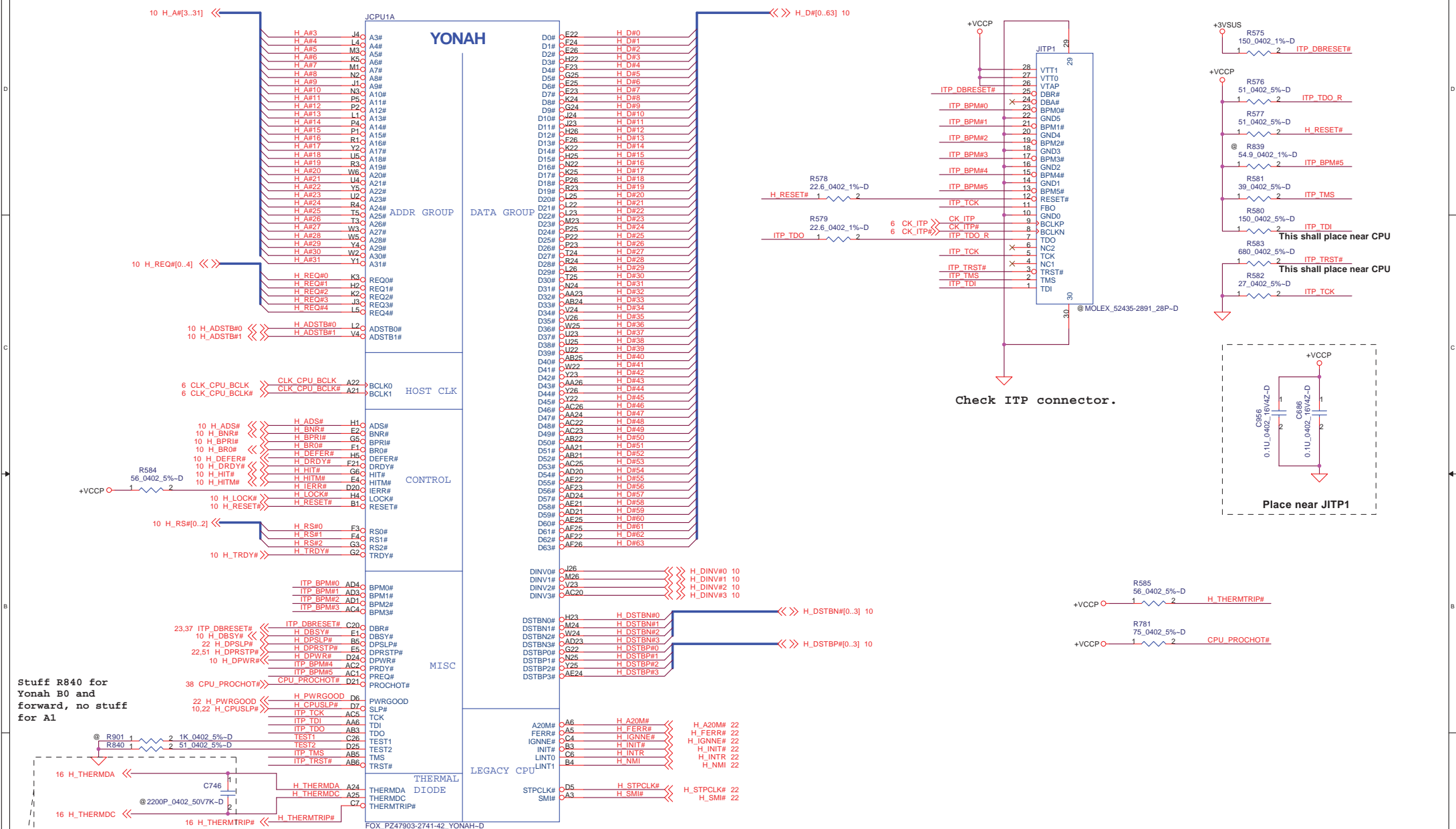


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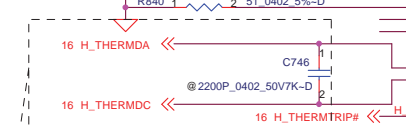


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Clock Generator		
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Stuff R840 for Yonah B0 and forward, no stuff for A1



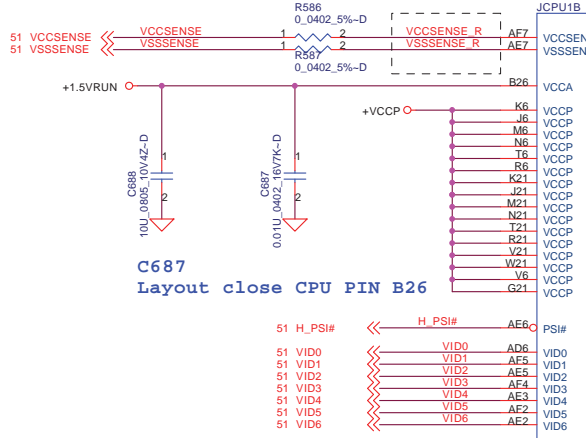
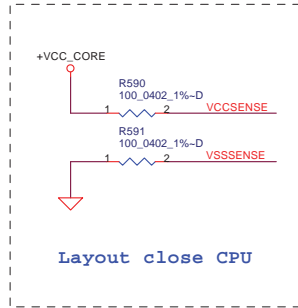
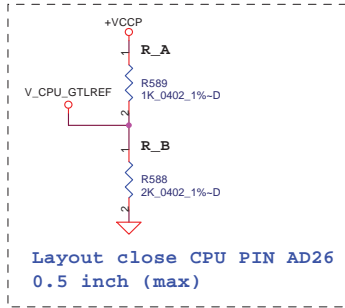
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil
C746 close to CPU

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Title Yonah in mFCPGA479		
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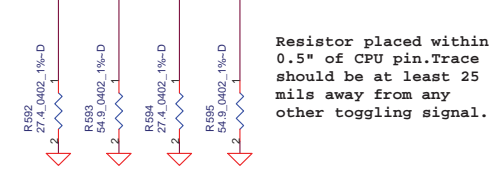
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Length match within 25 mils

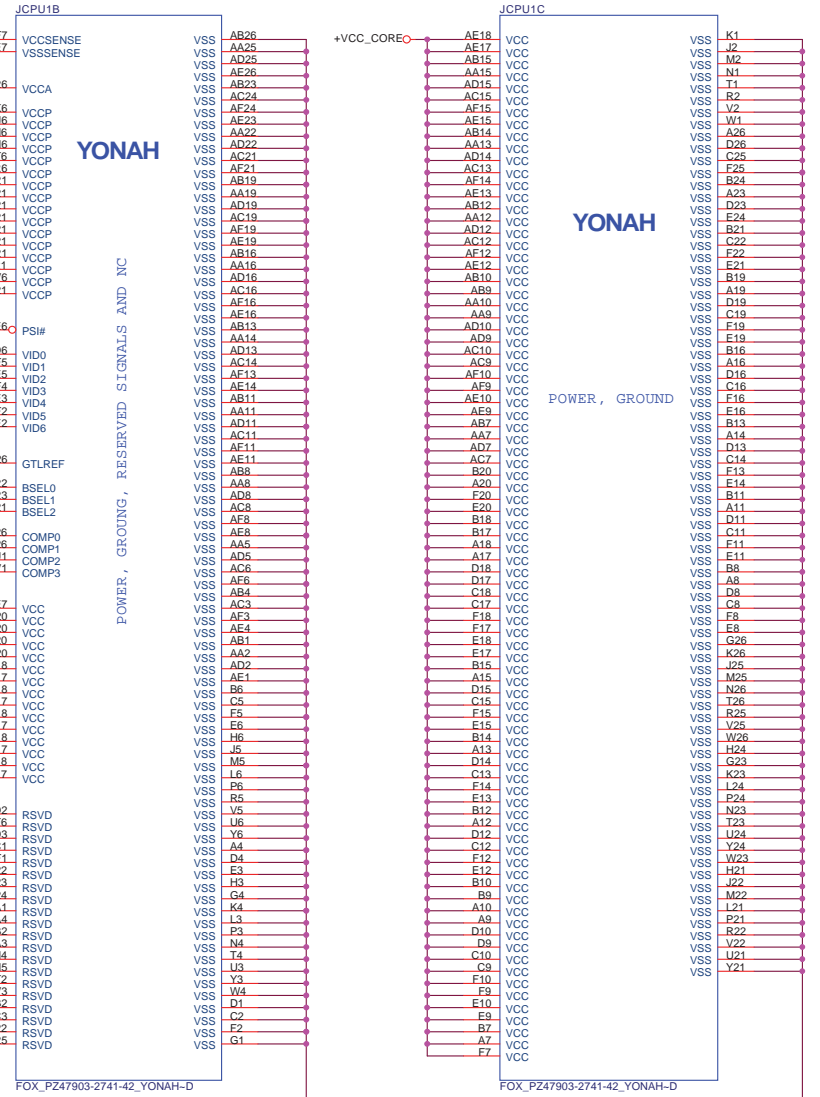


- 51 H_PSI# << H_PSI# AE6<
- 51 VID0 << VID0 AD6<
- 51 VID1 << VID1 AE5<
- 51 VID2 << VID2 AE5<
- 51 VID3 << VID3 AE4<
- 51 VID4 << VID4 AE3<
- 51 VID5 << VID5 AE2<
- 51 VID6 << VID6 AE2<

- V_CPU_GTLREF << AD26<
- 6,10 CPU_MCH_BSEL0 << CPU_MCH_BSEL0 B22<
- 6,10 CPU_MCH_BSEL1 << CPU_MCH_BSEL1 B23<
- 6,10 CPU_MCH_BSEL2 << CPU_MCH_BSEL2 C21<



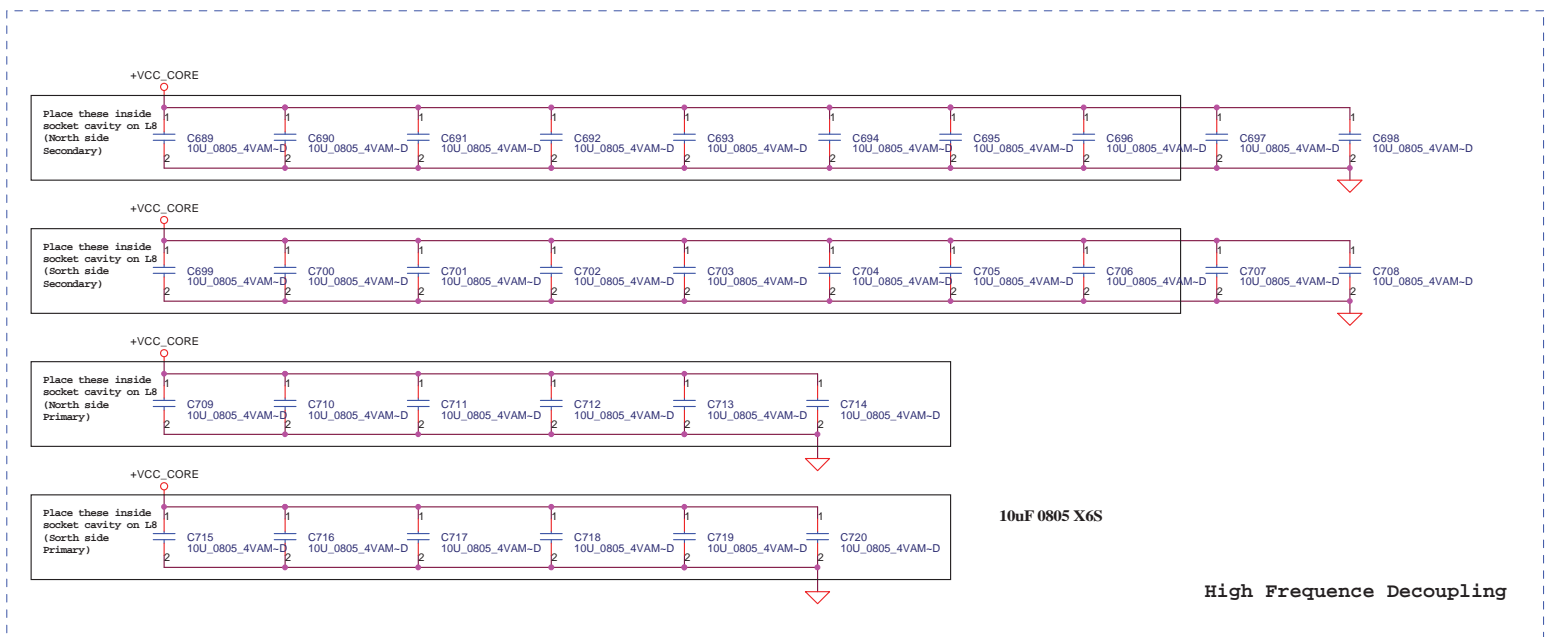
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



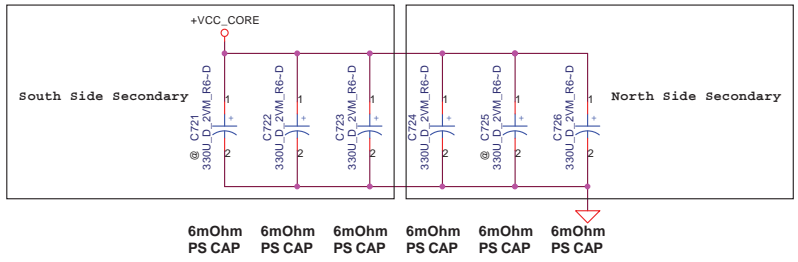
FOX_PZ47903-2741-42_YONAH-D

FOX_PZ47903-2741-42_YONAH-D

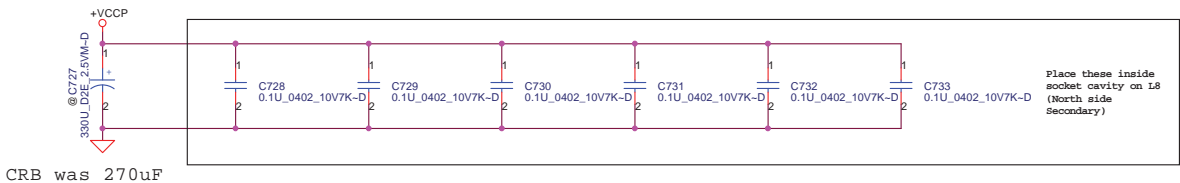




Near VCORE regulator.



ESR <= 1.5m ohm



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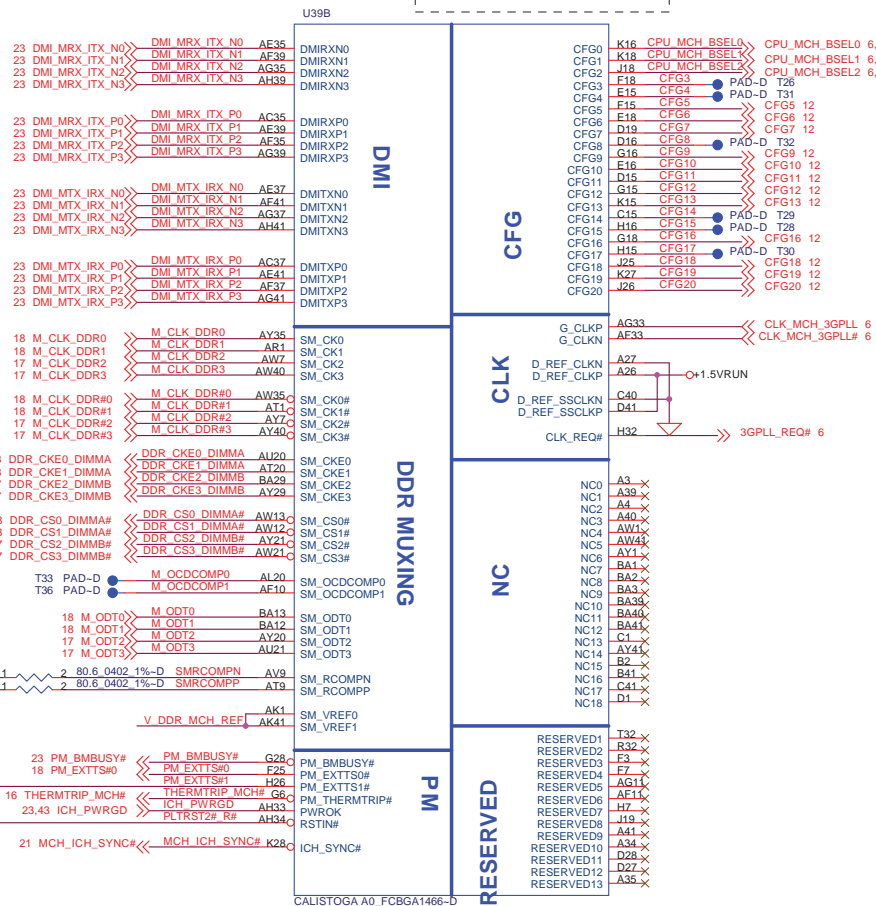
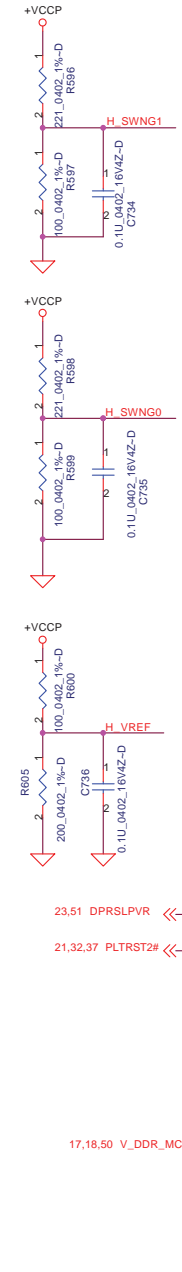
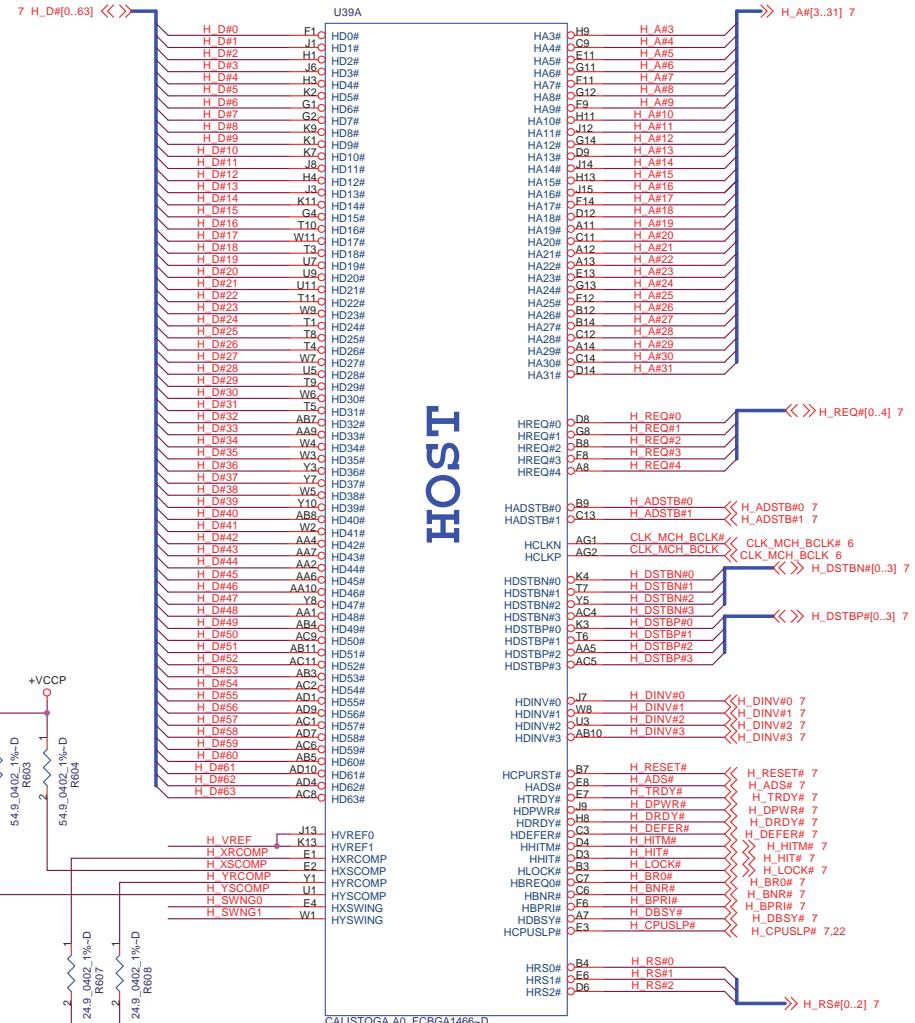
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CPU Bypass

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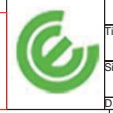
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Description at page12
 Note :
 CFG3:17 has internal pullup,
 CFG18:19 has internal pulldown

Layout Note:
 H_XRCOMP & H_YRCOMP trace width and spacing is 10/20

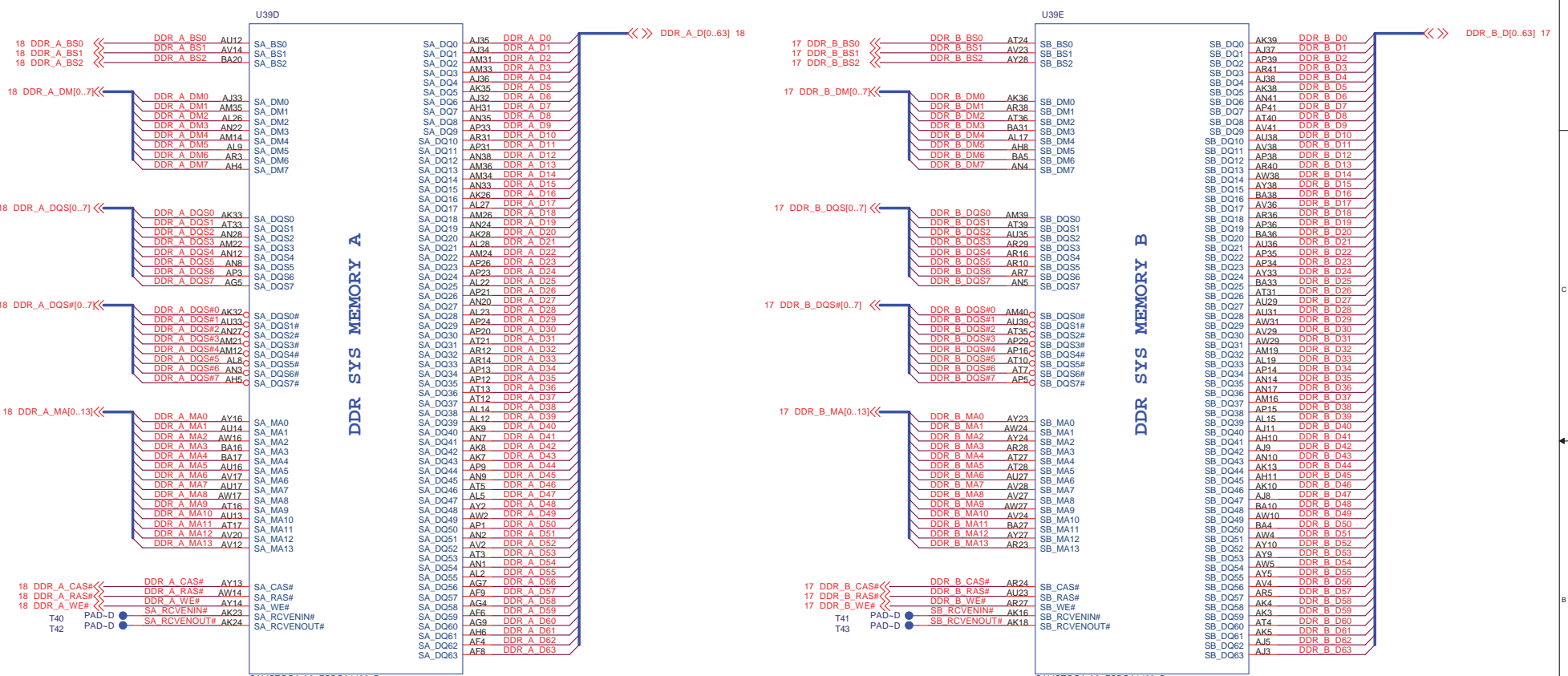
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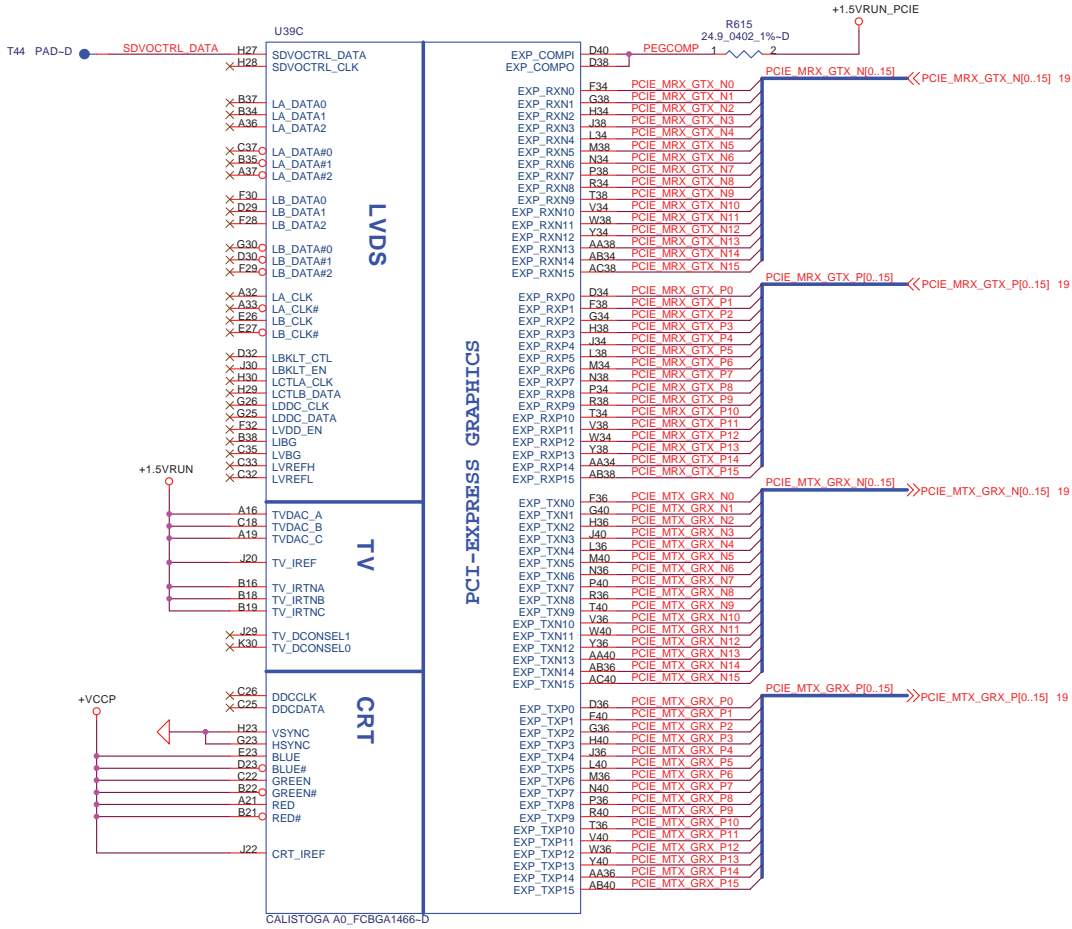
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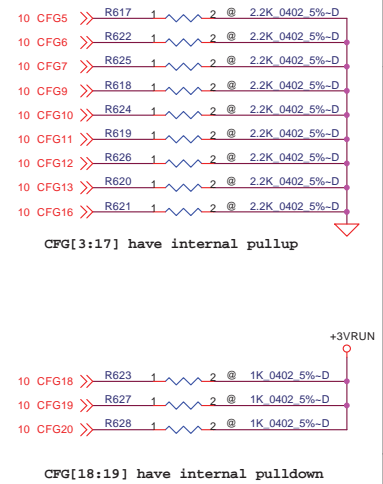
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Strap Pin Table

CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = Moby Dick High = Calistoga *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation*
CFG10	Low = Reserved High = Mobility*
CFG11	PSB 4x Clock Enable Low = Calistoga * High = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (DMI Lane Reversal)	Low = Normal * Operation (Default): Lane number in Order High = Reverse Lane
SDVO_CTRLDATA	Low = No SDVO Device Present (Default)* High = SDVO Device Present
CFG20 (PCIE/SDVO select)	Low = Only PCIE or SDVO is operational. (Default)* High = PCIE/SDVO are operating simu.



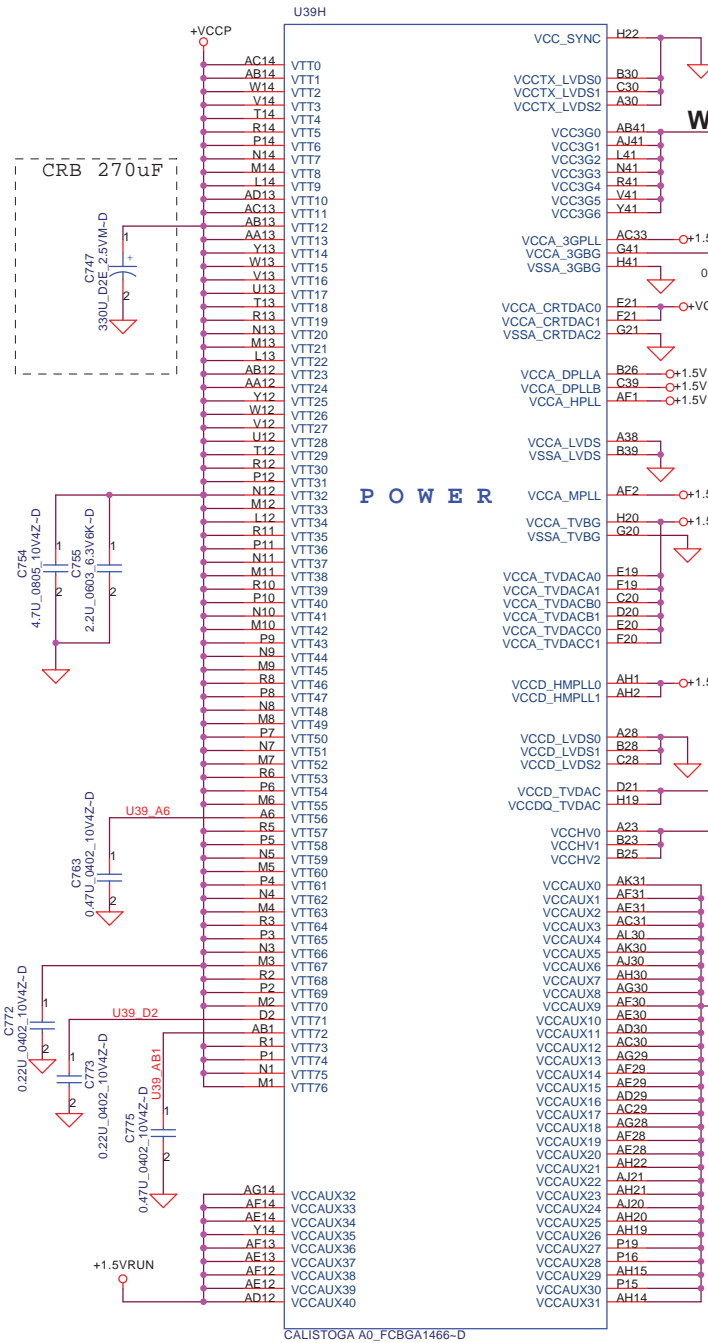
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Calistoga(3 of 6)

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W=30 mils


Should be placed on top

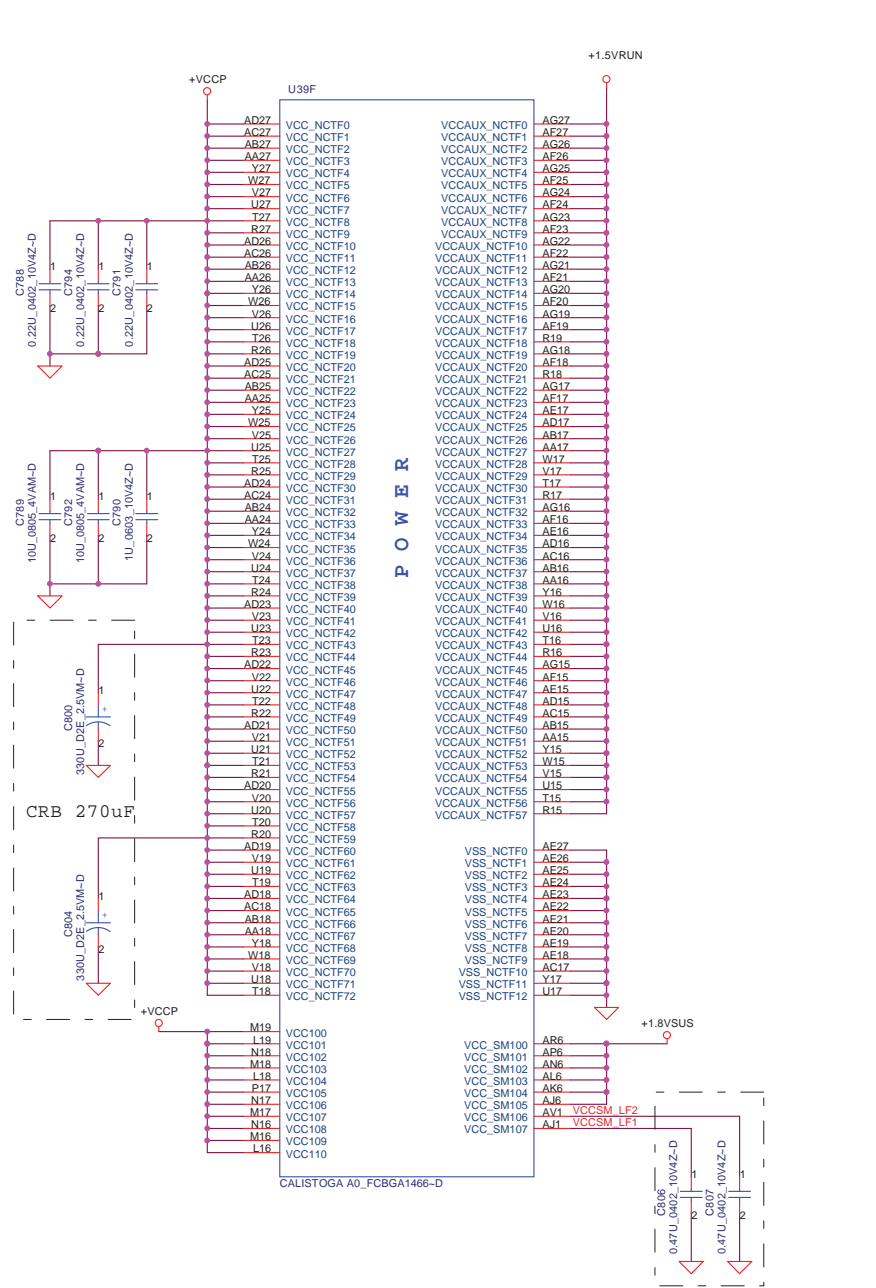
Route +2.5VRUN from GMCH pinG41 to decoupling cap (C740)<200mil to the edge.

Should be placed in cavity

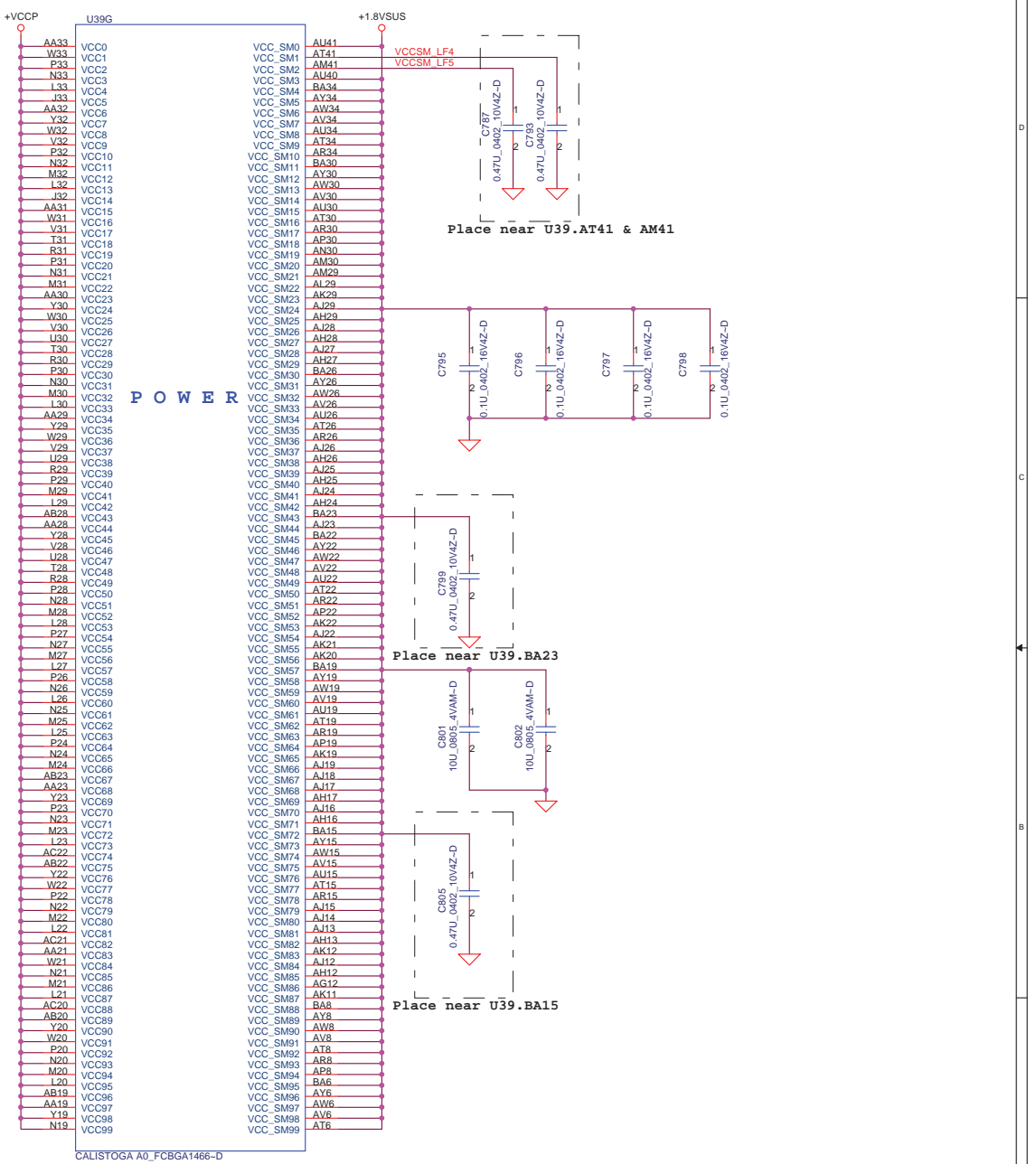
P O W E R

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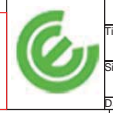
Place near U39.AV1 & AJ1



Place near U39.AT41 & AM41

Place near U39.BA23

Place near U39.BA15



U39I		AE34	
AC41	VSS0	VSS100	AE34
AA41	VSS1	VSS101	AC34
W41	VSS2	VSS102	C34
T41	VSS3	VSS103	AW33
P41	VSS4	VSS104	AV33
M41	VSS5	VSS105	AR33
J41	VSS6	VSS106	AE33
F41	VSS7	VSS107	AB33
AV40	VSS8	VSS108	Y33
AP40	VSS9	VSS109	V33
AN40	VSS10	VSS110	T33
AK40	VSS11	VSS111	R33
A40	VSS12	VSS112	M33
AH40	VSS13	VSS113	H33
AG40	VSS14	VSS114	G33
AF40	VSS15	VSS115	F33
AE40	VSS16	VSS116	D33
B40	VSS17	VSS117	B33
AY39	VSS18	VSS118	AH32
AW39	VSS19	VSS119	AG32
AV39	VSS20	VSS120	AF32
AR39	VSS21	VSS121	AE32
AN39	VSS22	VSS122	AC32
AJ39	VSS23	VSS123	AB32
AC39	VSS24	VSS124	G32
AB39	VSS25	VSS125	B32
AA39	VSS26	VSS126	AY31
Y39	VSS27	VSS127	AV31
W39	VSS28	VSS128	AN31
T39	VSS29	VSS129	AL31
R39	VSS30	VSS130	AG31
P39	VSS31	VSS131	AB31
N39	VSS32	VSS132	Y31
M39	VSS33	VSS133	AB30
L39	VSS34	VSS134	E30
J39	VSS35	VSS135	AT29
H39	VSS36	VSS136	AN29
G39	VSS37	VSS137	AF29
F39	VSS38	VSS138	T29
E39	VSS39	VSS139	N29
D39	VSS40	VSS140	K29
AT38	VSS41	VSS141	G29
AM38	VSS42	VSS142	E29
AH38	VSS43	VSS143	C29
AG38	VSS44	VSS144	B29
AF38	VSS45	VSS145	A29
AE38	VSS46	VSS146	BA28
C38	VSS47	VSS147	AW28
AK37	VSS48	VSS148	AU28
AH37	VSS49	VSS149	AP28
AB37	VSS50	VSS150	AM28
AA37	VSS51	VSS151	AD28
Y37	VSS52	VSS152	AC28
W37	VSS53	VSS153	W28
V37	VSS54	VSS154	I28
T37	VSS55	VSS155	E28
R37	VSS56	VSS156	AP27
F37	VSS57	VSS157	AM27
M37	VSS58	VSS158	AK27
L37	VSS59	VSS159	J27
J37	VSS60	VSS160	G27
H37	VSS61	VSS161	F27
G37	VSS62	VSS162	C27
F37	VSS63	VSS163	B27
D37	VSS64	VSS164	AN26
AY36	VSS65	VSS165	M26
AW36	VSS66	VSS166	K26
AV36	VSS67	VSS167	F26
AR36	VSS68	VSS168	D26
AN36	VSS69	VSS169	AK25
AH36	VSS70	VSS170	P25
AG36	VSS71	VSS171	K25
AF36	VSS72	VSS172	H25
AE36	VSS73	VSS173	E25
C36	VSS74	VSS174	D25
B36	VSS75	VSS175	A25
BA35	VSS76	VSS176	BA24
AV35	VSS77	VSS177	AU24
AR35	VSS78	VSS178	AL24
AH35	VSS79	VSS179	AP24
AB35	VSS80	VSS180	AT23
AA35	VSS81	VSS181	AN23
Y35	VSS82	VSS182	AM23
W35	VSS83	VSS183	AH23
V35	VSS84	VSS184	AC23
T35	VSS85	VSS185	W23
R35	VSS86	VSS186	K23
P35	VSS87	VSS187	J23
M35	VSS88	VSS188	F23
L35	VSS89	VSS189	C23
J35	VSS90	VSS190	AA22
H35	VSS91	VSS191	K22
G35	VSS92	VSS192	G22
F35	VSS93	VSS193	F22
D35	VSS94	VSS194	E22
AN34	VSS95	VSS195	D22
AK34	VSS96	VSS196	A22
AG34	VSS97	VSS197	BA21
AF34	VSS98	VSS198	AV21
	VSS99	VSS199	AR21

POWER

CALISTOGA A0_FCBGA1466-D

U39J		AG10	
AN21	VSS200	VSS280	AG10
AL21	VSS201	VSS281	AC10
AR21	VSS202	VSS282	W10
Y21	VSS203	VSS283	U10
P21	VSS204	VSS284	BA9
K21	VSS205	VSS285	AW9
J21	VSS206	VSS286	AR9
H21	VSS207	VSS287	AH9
C21	VSS208	VSS288	AB9
AW20	VSS209	VSS289	Y9
AR20	VSS210	VSS290	R9
AM20	VSS211	VSS291	G9
AA20	VSS212	VSS292	E9
K20	VSS213	VSS293	A9
B20	VSS214	VSS294	AG8
A20	VSS215	VSS295	AD8
AN19	VSS216	VSS296	AA8
AC19	VSS217	VSS297	U8
W19	VSS218	VSS298	K8
K19	VSS219	VSS299	C8
G19	VSS220	VSS300	BA7
C19	VSS221	VSS301	AV7
AH18	VSS222	VSS302	AP7
H18	VSS223	VSS303	AL7
D18	VSS224	VSS304	AJ7
A18	VSS225	VSS305	AH7
AY17	VSS226	VSS306	AF7
AR17	VSS227	VSS307	AC7
AP17	VSS228	VSS308	G7
AM17	VSS229	VSS309	D7
AK17	VSS230	VSS310	AG6
AV16	VSS231	VSS311	AD6
AN16	VSS232	VSS312	AB6
AL16	VSS233	VSS313	Y6
J16	VSS234	VSS314	U6
F16	VSS235	VSS315	U6
C16	VSS236	VSS316	K6
AN15	VSS238	VSS318	H6
AM15	VSS239	VSS319	B6
N15	VSS240	VSS320	AV5
M15	VSS241	VSS321	AE5
L15	VSS242	VSS322	AD5
B15	VSS243	VSS323	AY4
A15	VSS244	VSS324	AR4
BA14	VSS246	VSS326	AP4
AT14	VSS247	VSS327	AL4
AK14	VSS248	VSS328	U4
AD14	VSS249	VSS329	R4
AA14	VSS250	VSS330	J4
U14	VSS251	VSS331	F4
K14	VSS252	VSS332	C4
E14	VSS253	VSS333	AY3
AV13	VSS255	VSS335	AW3
AR13	VSS256	VSS336	AL3
AM13	VSS257	VSS337	AH3
VSS258	VSS258	VSS338	AG3
AL13	VSS259	VSS339	AF3
AG13	VSS260	VSS340	AD3
P13	VSS261	VSS341	AC3
B13	VSS262	VSS342	AA3
D13	VSS265	VSS343	G3
H13	VSS264	VSS344	AT2
AY12	VSS263	VSS345	AR2
K12	VSS267	VSS347	AP2
H12	VSS268	VSS348	AK2
E12	VSS269	VSS349	AL2
AD11	VSS270	VSS350	AB2
AA11	VSS271	VSS351	Y2
J11	VSS272	VSS352	U2
D11	VSS273	VSS353	T2
B11	VSS274	VSS354	N2
AV10	VSS276	VSS356	J2
AP10	VSS277	VSS357	H2
AL10	VSS278	VSS358	C2
AJ10	VSS279	VSS359	AL1

POWER

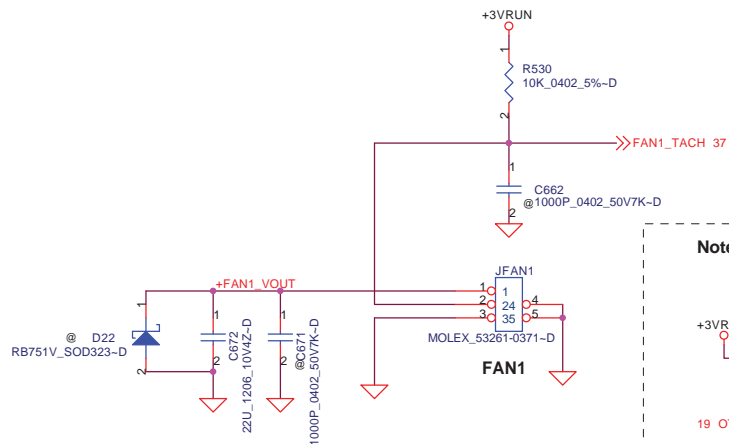
CALISTOGA A0_FCBGA1466-D

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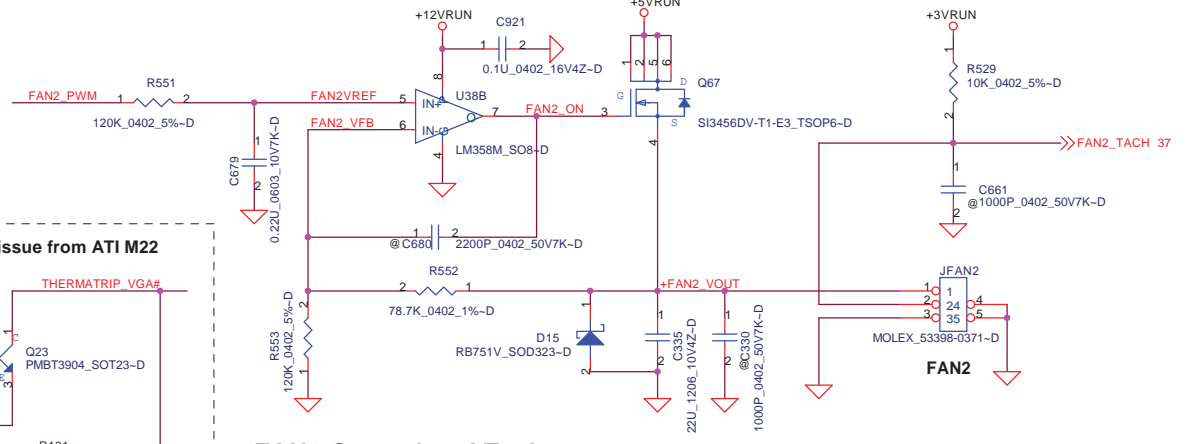
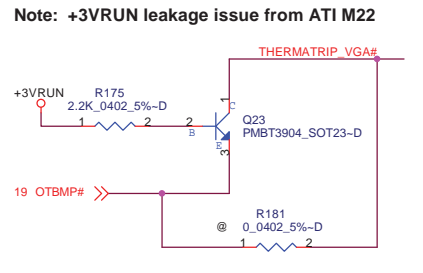


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Size	Document Number Greenland-LA2732P	Rev X03
Date	Wednesday, December 28, 2005	Sheet 15 of 63

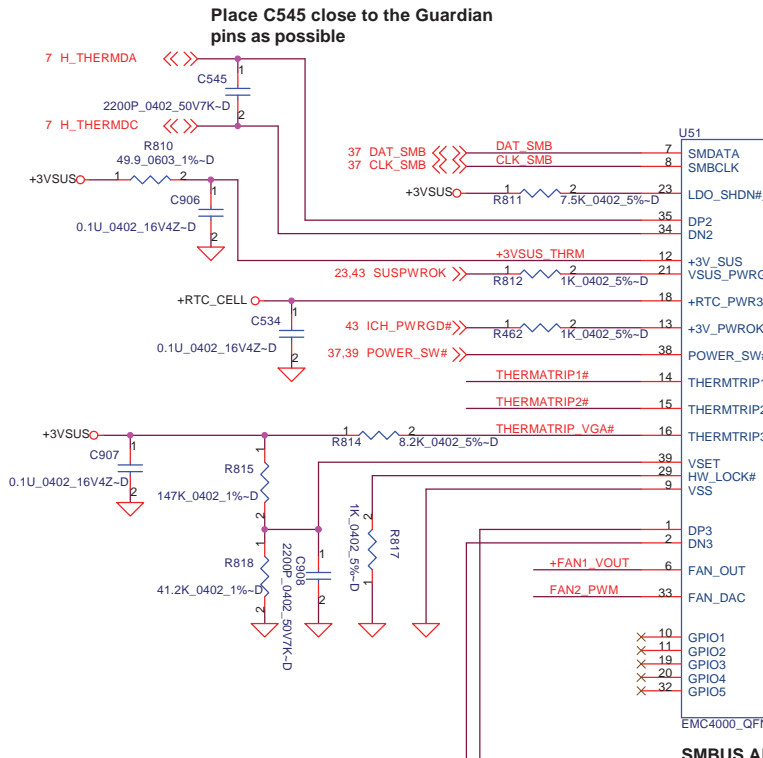
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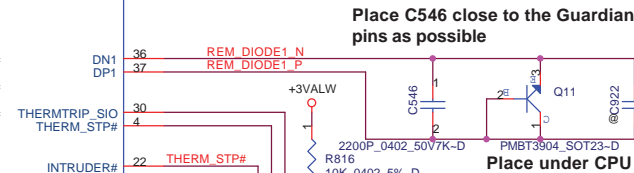
FAN1 Control and Tachometer



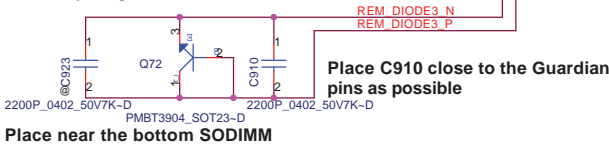
FAN2 Control and Tachometer



Voltage margining circuit for LDO output.
For Vmargin, stuff R886 and R834=30K.
R834=1K for production

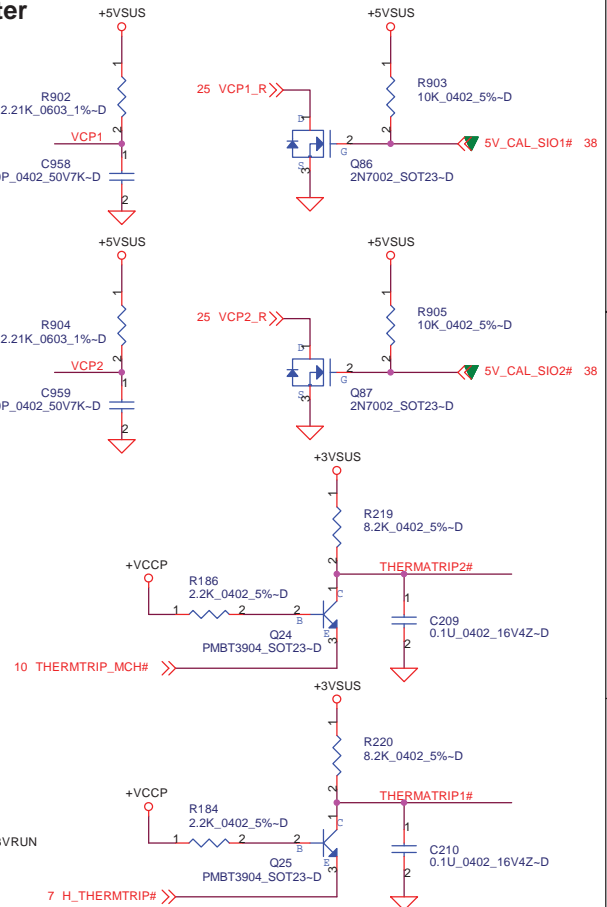


REM_DIODE3_N, REM_DIODE3_P routing together.
Trace width / Spacing = 10 / 10 mil



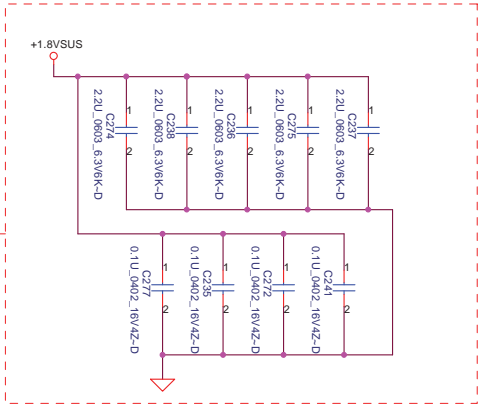
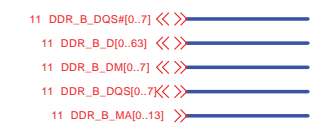
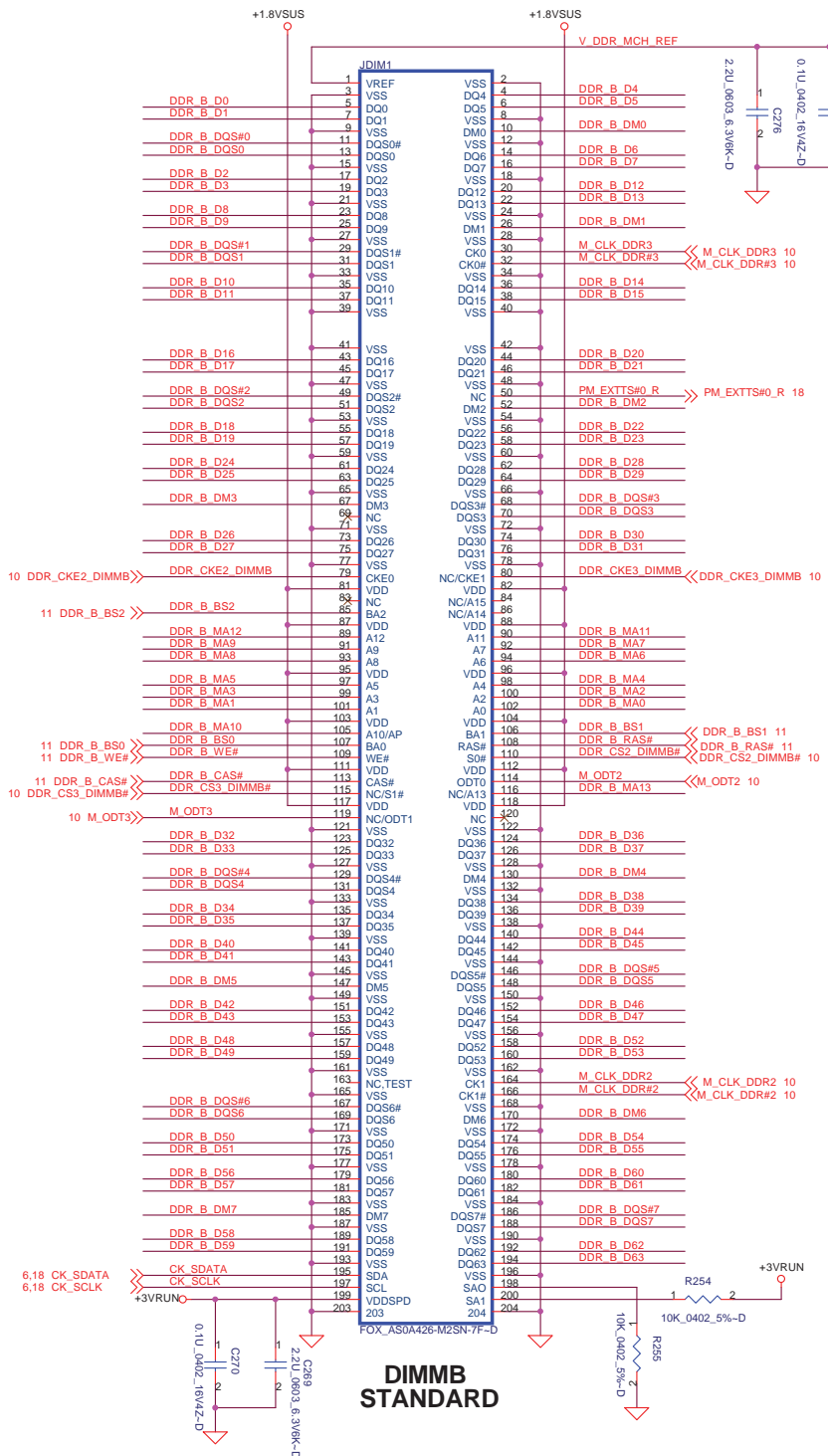
<http://hobi-elektronika.net>

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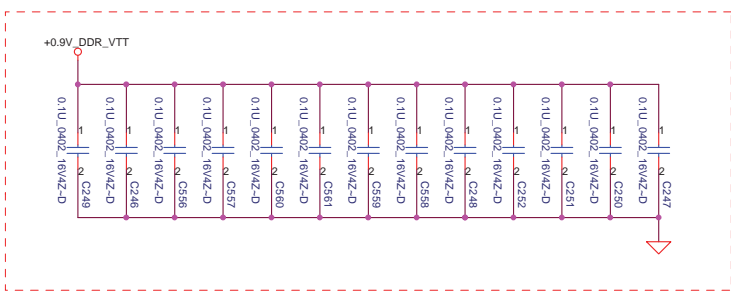


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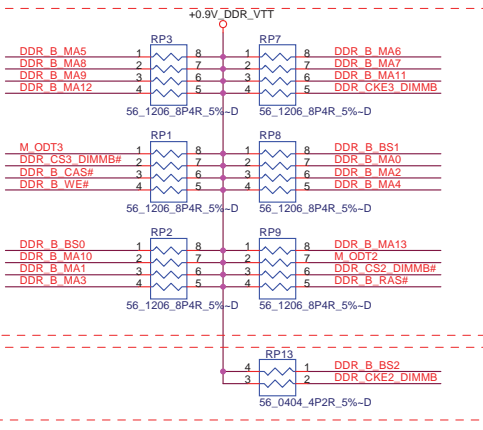
		Compal Electronics, Inc.	
		Thermal Sensor & Fan	
Size	Document Number	Greenland-LA2732P	
Custom			
Date:	Wednesday, December 28, 2005	Sheet	16 of 63



Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor closely JDIM1, all trace length < 750 mil

Layout Note:
Place these resistor closely JDIM1, all trace length Max = 1.3"

SPD Address Table

DIMM/Channel	ADDR [1:0]
A	[00]
B	[10]

DIMMB STANDARD

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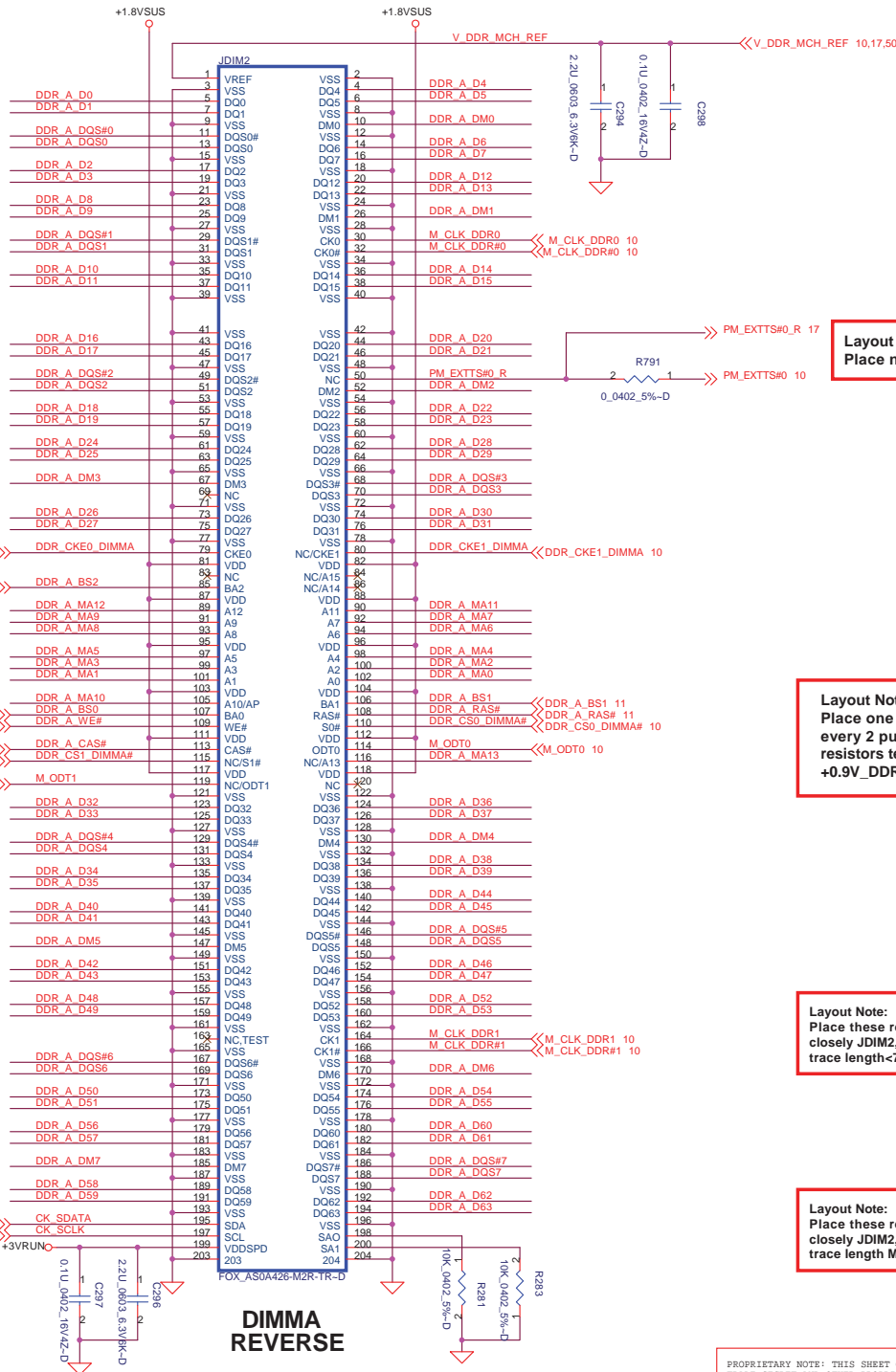
DDRII DIMM B

Greenland-LA2732P

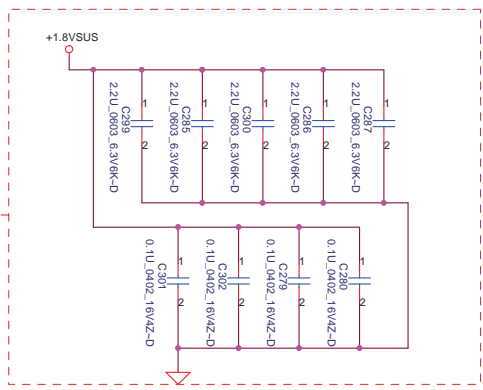
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Date: Wednesday, December 28, 2005

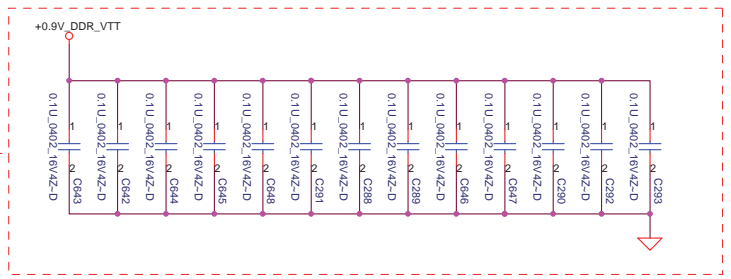
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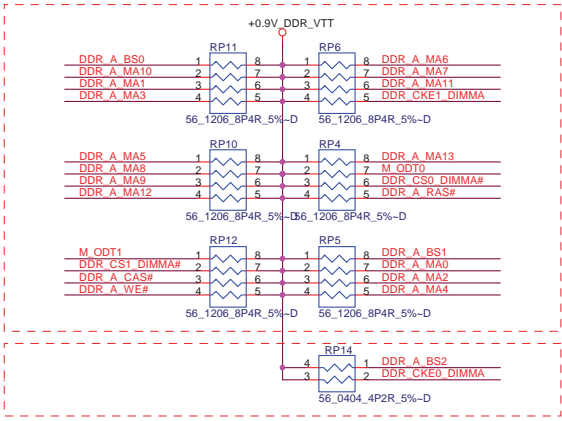
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- 11 DDR_A_D[0..63] <<<>>>
- 11 DDR_A_DM[0..7] <<<>>>
- 11 DDR_A_DQS#[0..7] <<<>>>
- 11 DDR_A_MA#[0..13] <<<>>>



Layout Note:
Place near JDIM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor closely JDIM2, all trace length < 750 mil

Layout Note:
Place these resistor closely JDIM2, all trace length Max=1.3"

DIMMA REVERSE

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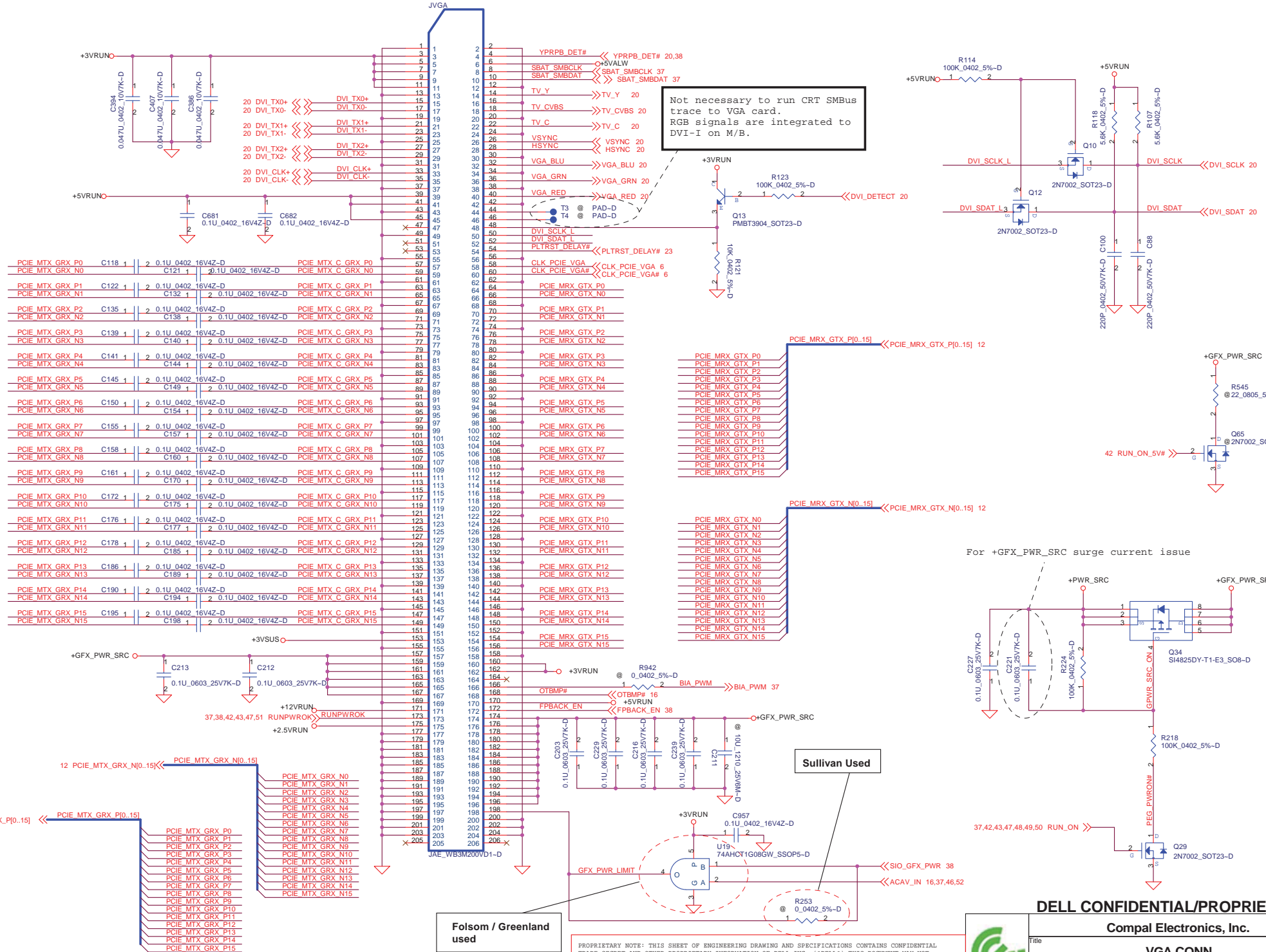
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DDRII DIMM A

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Not necessary to run CRT SMBus trace to VGA card.
RGB signals are integrated to DVI-I on M/B.

Folsom / Greenland used

Sullivan Used



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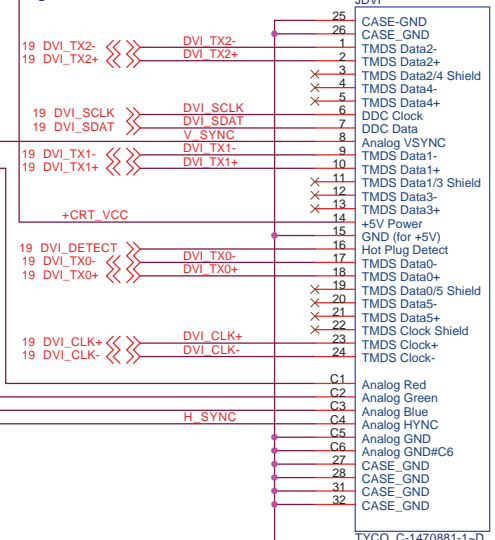
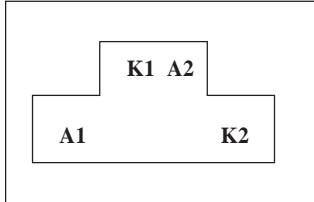
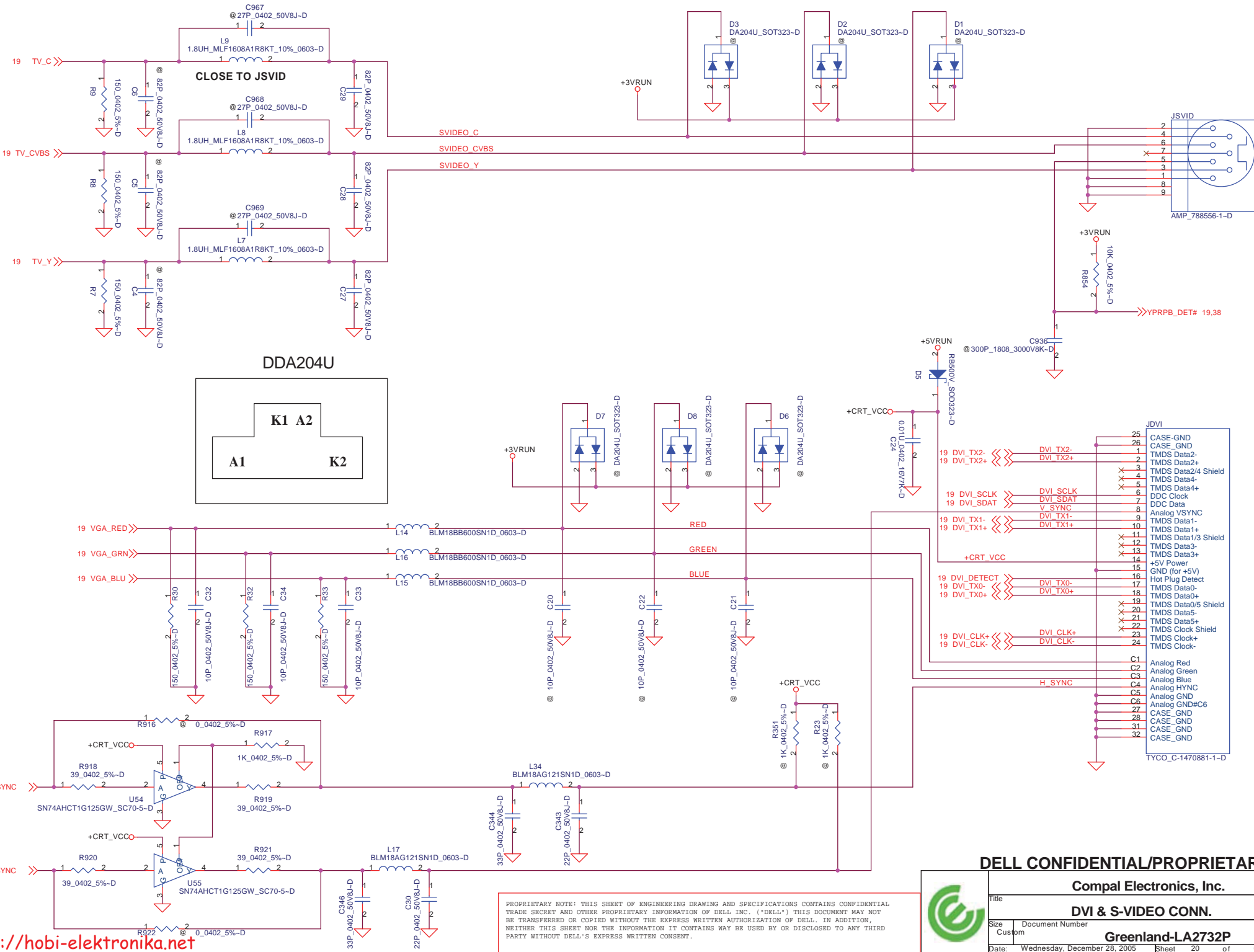
Compal Electronics, Inc.

VGA CONN.

Greenland-LA2732P

Title	VGA CONN.		
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Date:	Wednesday, December 28, 2005	Sheet	19 of 63

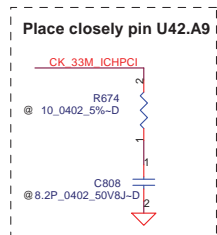
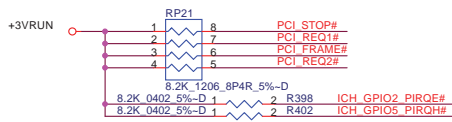
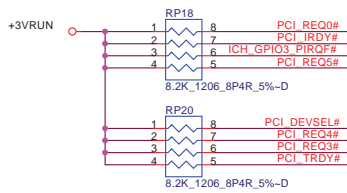
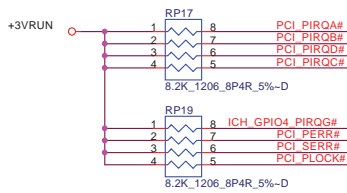
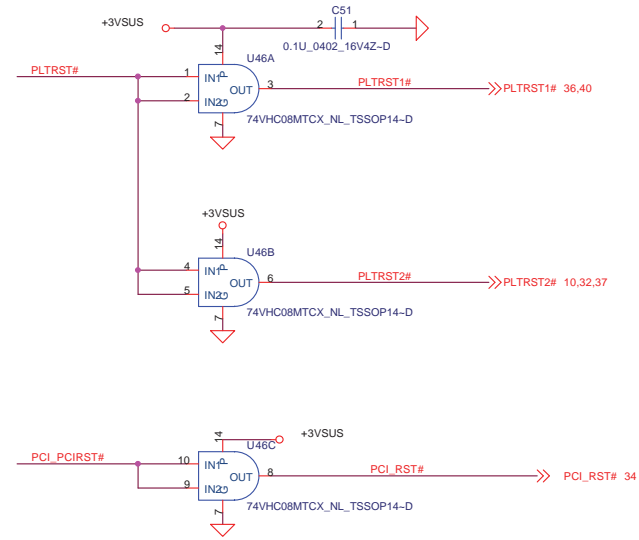
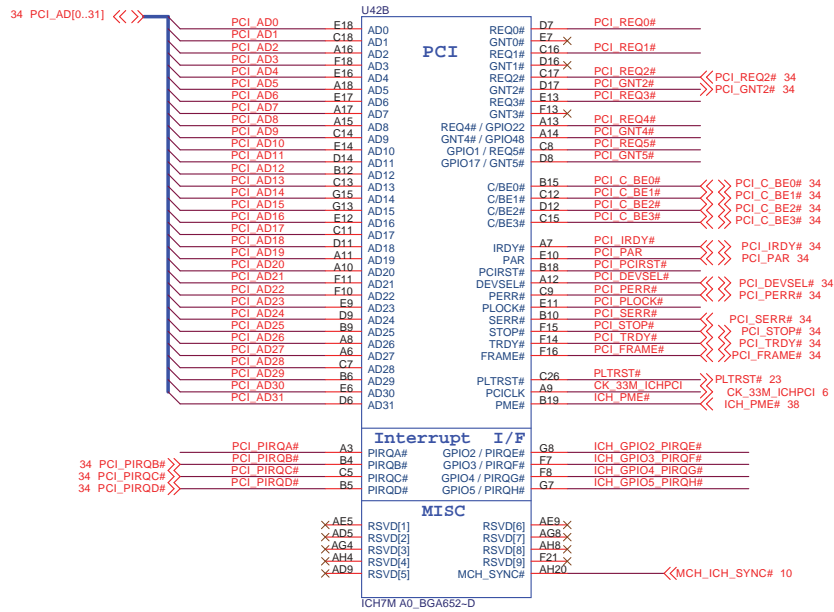
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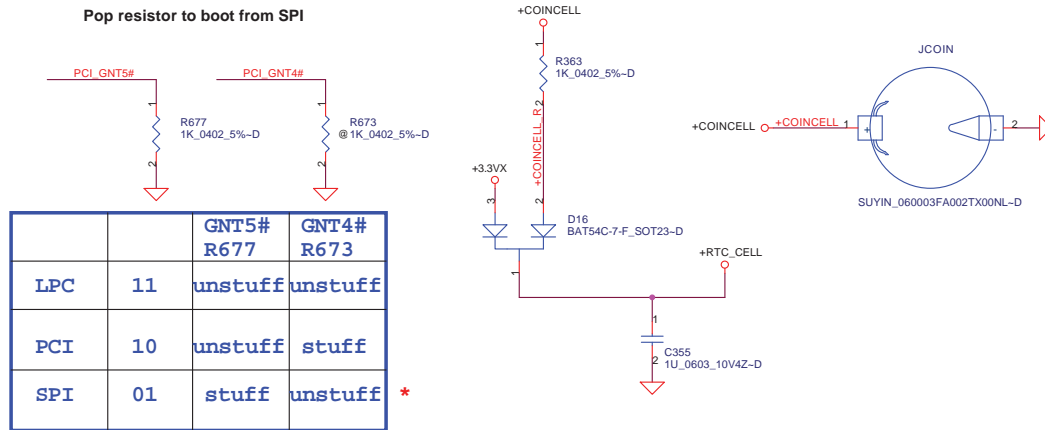
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Compal Electronics, Inc.	
DVI & S-VIDEO CONN.	
Size	Document Number
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Pop resistor to boot from SPI

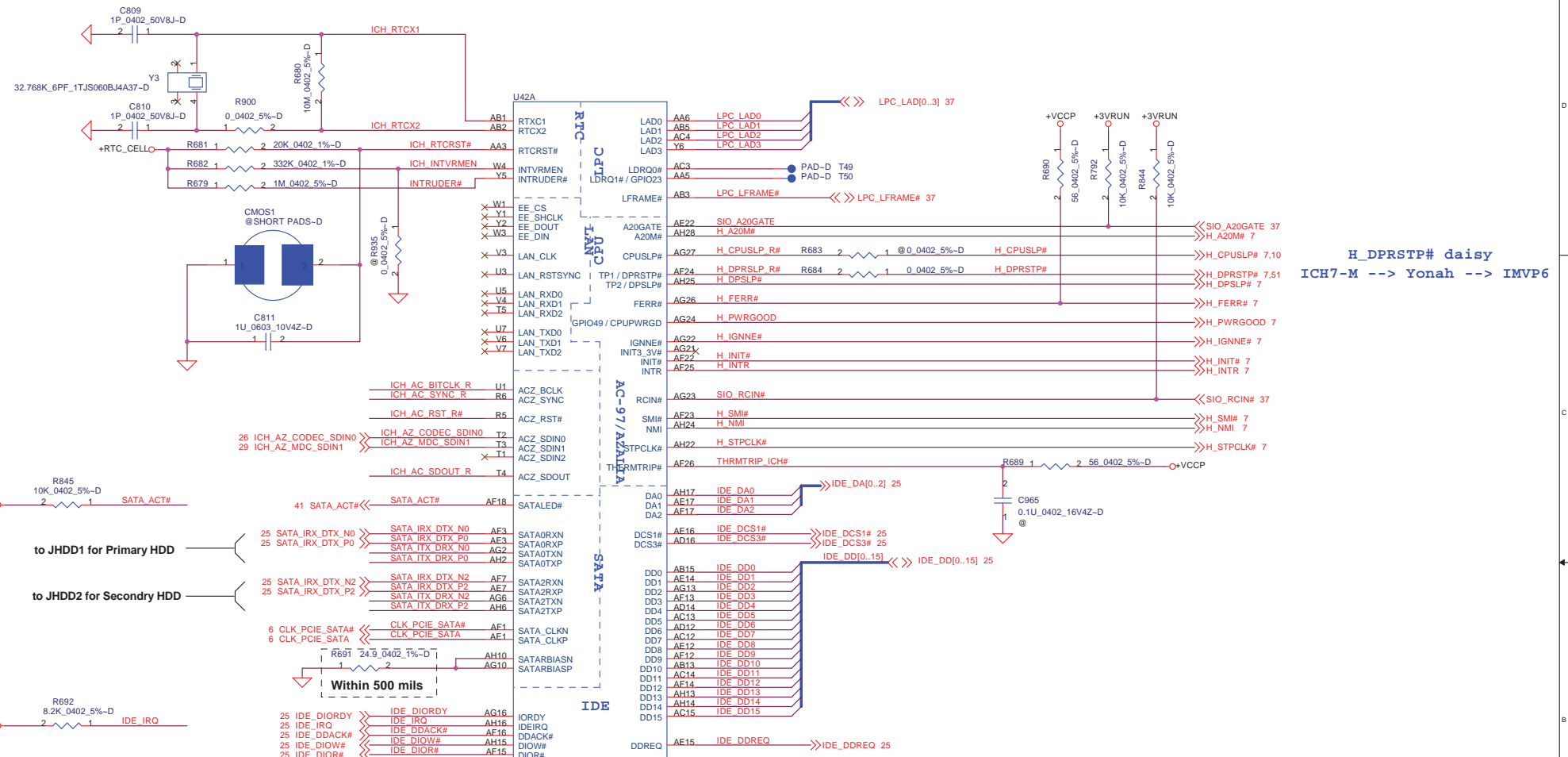


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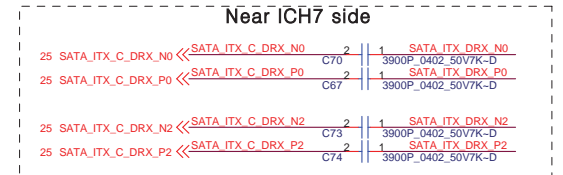
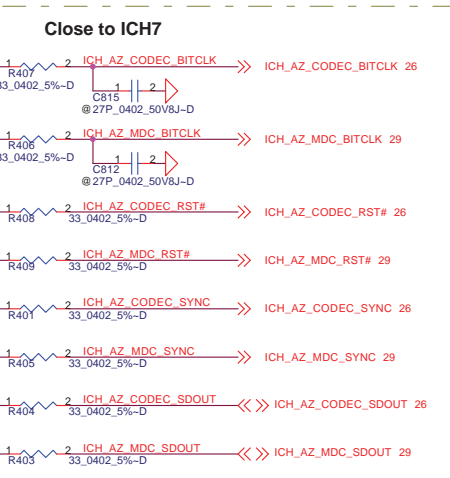


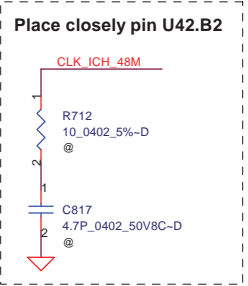
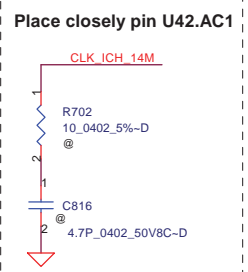
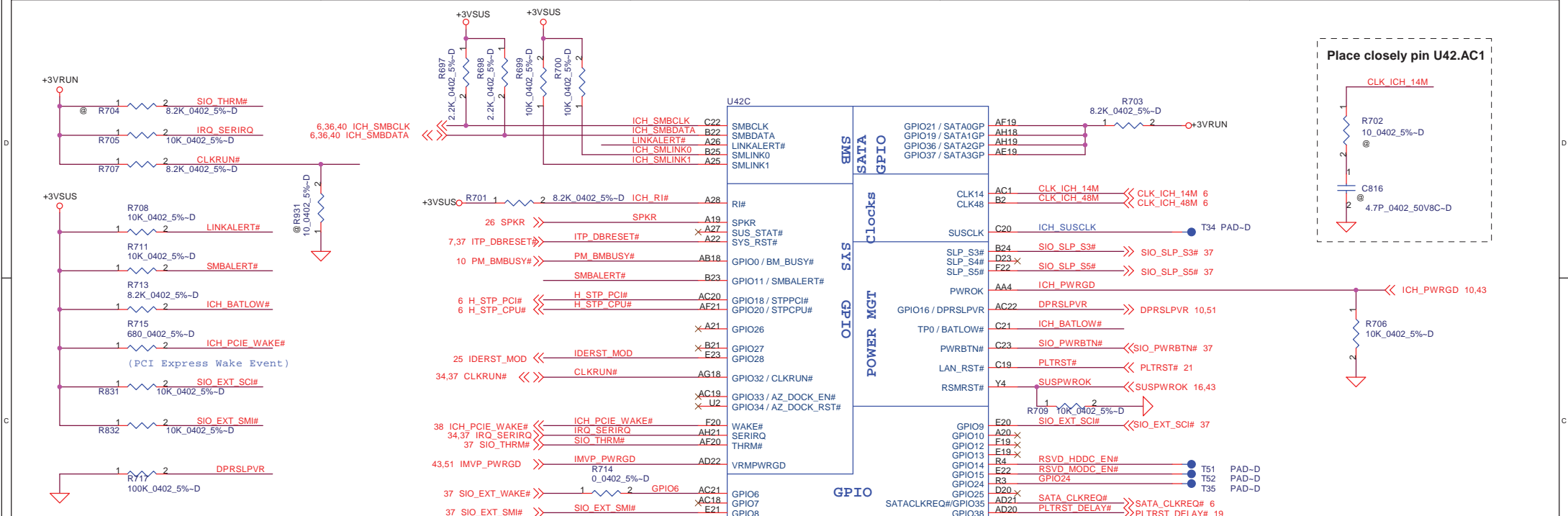
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Title	ICH7(1/4)
Size	Document Number Greenland-LA2732P
Date	Wednesday, December 28, 2005
Sheet	21 of 63

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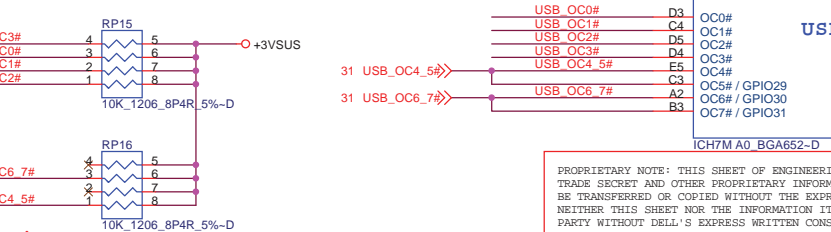
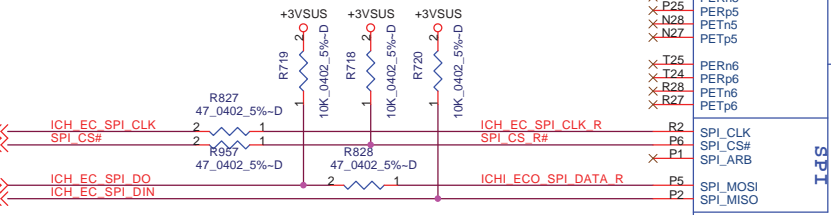
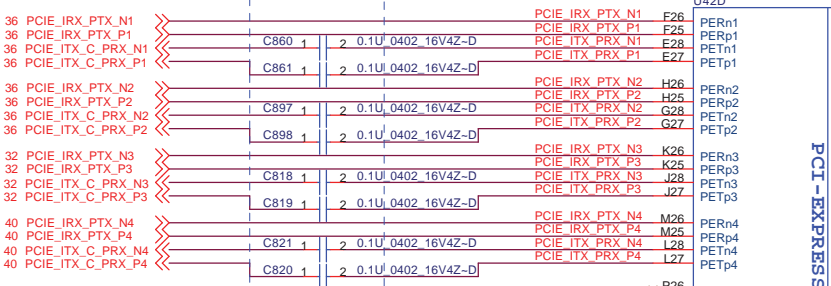


H DPRSTP# daisy
 ICH7-M --> Yonah --> IMVP6



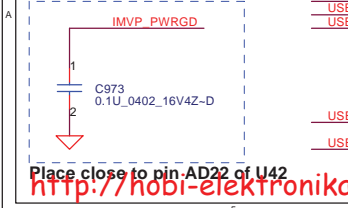


Close to ICH7M



- To Mini Card TV
- To Mini Card WLAN
- To LOM
- To Express Card

Pin P5: ICH input
Pin P2: ICH output



- USB0 => BLUETOOTH
- USB1 => USB[0] of ECE5011
- USB2 => Express Card
- USB3 => CIR
- USB4 => JUSB1(M/B)
- USB5 => JUSB2(M/B)
- USB6 => JUSB3 (USB/BD)
- USB7 => JUSB4 (USB/BD)

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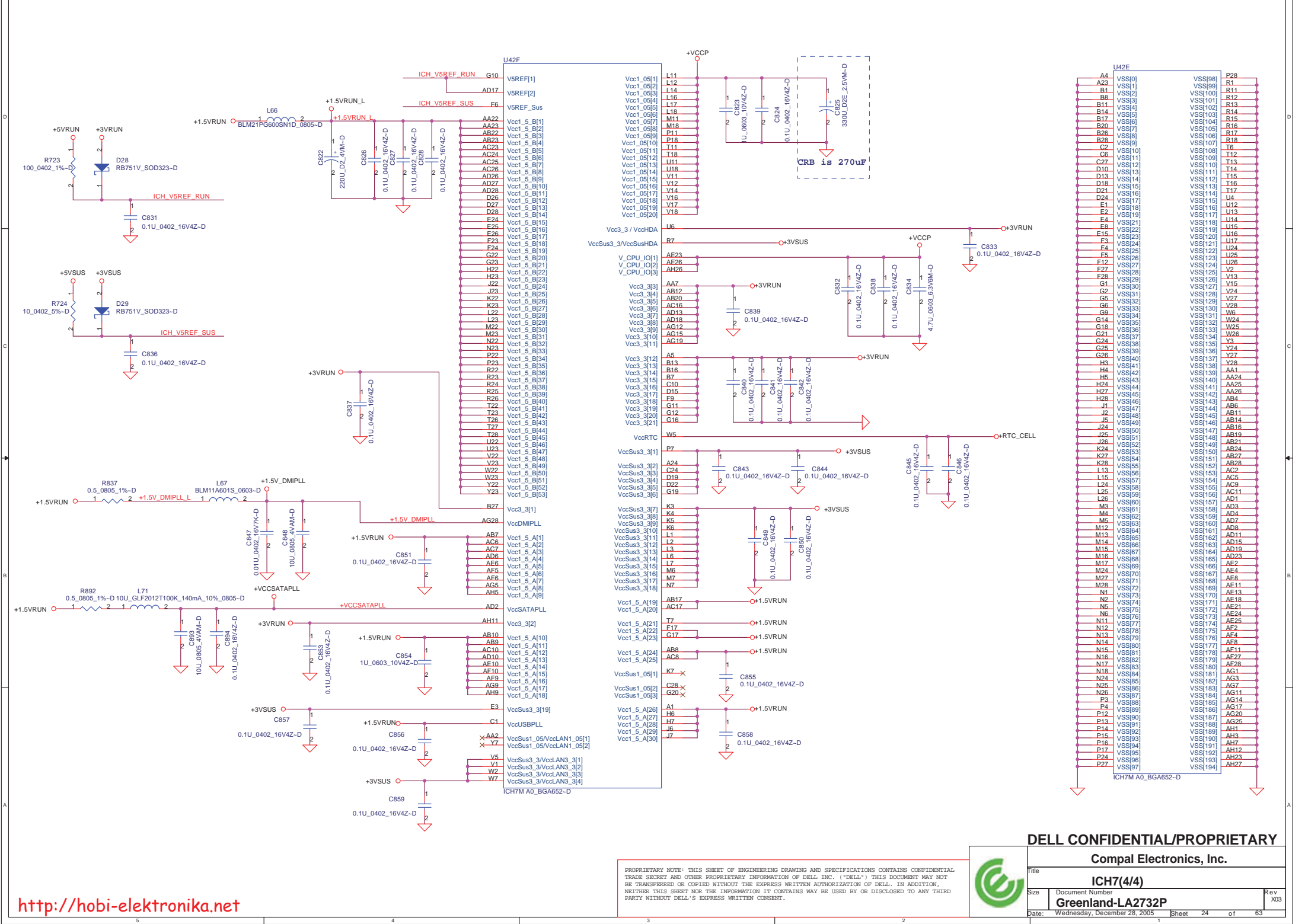


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ICH7(3/4)

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Size	Document Number	Rev X03
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U42E	VSS[0]	VSS[98]	P28
A4	VSS[0]	VSS[98]	R1
A23	VSS[1]	VSS[99]	R11
B1	VSS[2]	VSS[100]	R12
B8	VSS[3]	VSS[101]	R13
B11	VSS[4]	VSS[102]	R14
B14	VSS[5]	VSS[103]	R15
B17	VSS[6]	VSS[104]	R16
B20	VSS[7]	VSS[105]	R17
B28	VSS[8]	VSS[106]	R18
B29	VSS[9]	VSS[107]	R19
C2	VSS[10]	VSS[108]	T6
C6	VSS[11]	VSS[109]	T12
C27	VSS[12]	VSS[110]	T13
D10	VSS[13]	VSS[111]	T14
D13	VSS[14]	VSS[112]	T15
D18	VSS[15]	VSS[113]	T16
D21	VSS[16]	VSS[114]	T17
D24	VSS[17]	VSS[115]	T18
E1	VSS[18]	VSS[116]	T19
E2	VSS[19]	VSS[117]	T20
E4	VSS[20]	VSS[118]	T21
E8	VSS[21]	VSS[119]	T22
E15	VSS[22]	VSS[120]	T23
F3	VSS[23]	VSS[121]	T24
F4	VSS[24]	VSS[122]	T25
F5	VSS[25]	VSS[123]	T26
F12	VSS[26]	VSS[124]	T27
F27	VSS[27]	VSS[125]	T28
F28	VSS[28]	VSS[126]	T29
G5	VSS[29]	VSS[127]	T30
G6	VSS[30]	VSS[128]	T31
G7	VSS[31]	VSS[129]	T32
G8	VSS[32]	VSS[130]	T33
G9	VSS[33]	VSS[131]	T34
G14	VSS[34]	VSS[132]	T35
G18	VSS[35]	VSS[133]	T36
G21	VSS[36]	VSS[134]	T37
G24	VSS[37]	VSS[135]	T38
H4	VSS[38]	VSS[136]	T39
H5	VSS[39]	VSS[137]	T40
H6	VSS[40]	VSS[138]	T41
H3	VSS[41]	VSS[139]	T42
H4	VSS[42]	VSS[140]	T43
H5	VSS[43]	VSS[141]	T44
H2	VSS[44]	VSS[142]	T45
H28	VSS[45]	VSS[143]	T46
J1	VSS[46]	VSS[144]	T47
J2	VSS[47]	VSS[145]	T48
J5	VSS[48]	VSS[146]	T49
J24	VSS[49]	VSS[147]	T50
J25	VSS[50]	VSS[148]	T51
J26	VSS[51]	VSS[149]	T52
K27	VSS[52]	VSS[150]	T53
K28	VSS[53]	VSS[151]	T54
L13	VSS[54]	VSS[152]	T55
L15	VSS[55]	VSS[153]	T56
L24	VSS[56]	VSS[154]	T57
L25	VSS[57]	VSS[155]	T58
L26	VSS[58]	VSS[156]	T59
M3	VSS[59]	VSS[157]	T60
M4	VSS[60]	VSS[158]	T61
M5	VSS[61]	VSS[159]	T62
M13	VSS[62]	VSS[160]	T63
M14	VSS[63]	VSS[161]	T64
M15	VSS[64]	VSS[162]	T65
M16	VSS[65]	VSS[163]	T66
M17	VSS[66]	VSS[164]	T67
M18	VSS[67]	VSS[165]	T68
M19	VSS[68]	VSS[166]	T69
M24	VSS[69]	VSS[167]	T70
M27	VSS[70]	VSS[168]	T71
M28	VSS[71]	VSS[169]	T72
N1	VSS[72]	VSS[170]	T73
N2	VSS[73]	VSS[171]	T74
N5	VSS[74]	VSS[172]	T75
N6	VSS[75]	VSS[173]	T76
N11	VSS[76]	VSS[174]	T77
N12	VSS[77]	VSS[175]	T78
N13	VSS[78]	VSS[176]	T79
N14	VSS[79]	VSS[177]	T80
N15	VSS[80]	VSS[178]	T81
N16	VSS[81]	VSS[179]	T82
N17	VSS[82]	VSS[180]	T83
N18	VSS[83]	VSS[181]	T84
N24	VSS[84]	VSS[182]	T85
N25	VSS[85]	VSS[183]	T86
N26	VSS[86]	VSS[184]	T87
P3	VSS[87]	VSS[185]	T88
P4	VSS[88]	VSS[186]	T89
P13	VSS[89]	VSS[187]	T90
P12	VSS[90]	VSS[188]	T91
P14	VSS[91]	VSS[189]	T92
P15	VSS[92]	VSS[190]	T93
P16	VSS[93]	VSS[191]	T94
P17	VSS[94]	VSS[192]	T95
P24	VSS[95]	VSS[193]	T96
P27	VSS[96]	VSS[194]	T97
P27	VSS[97]	VSS[194]	T97

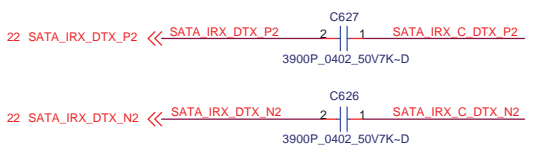
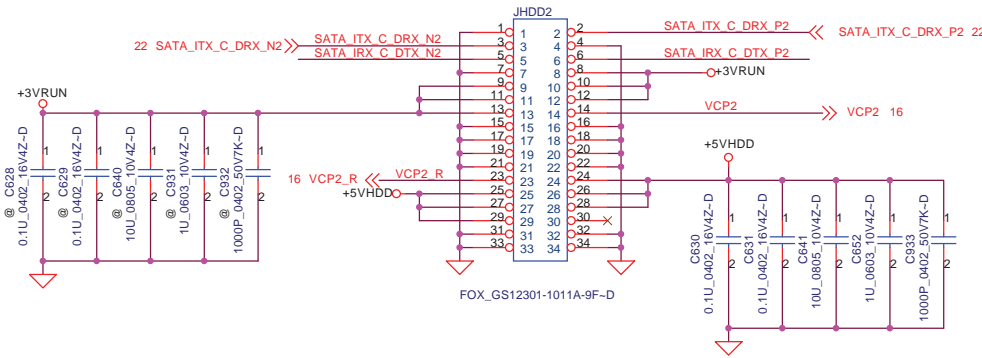
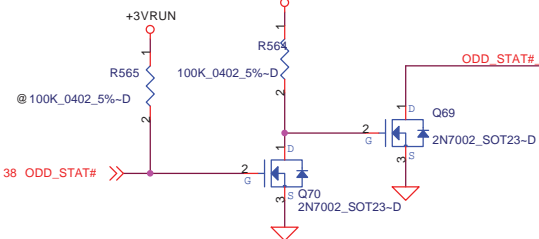
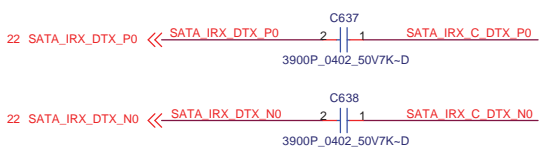
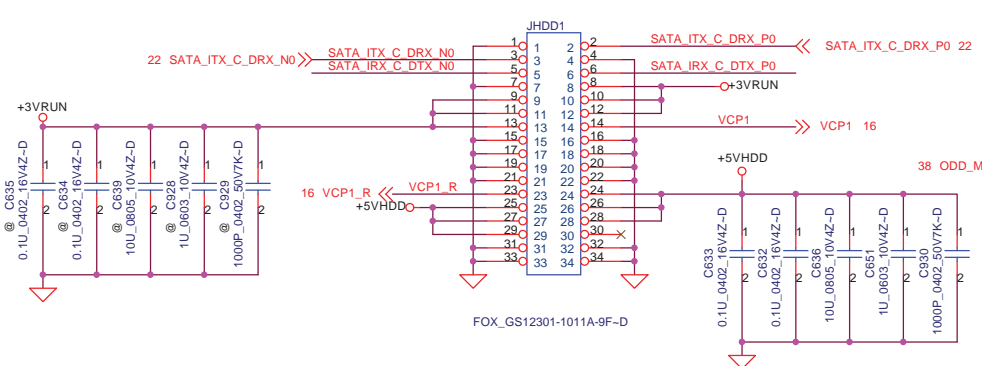
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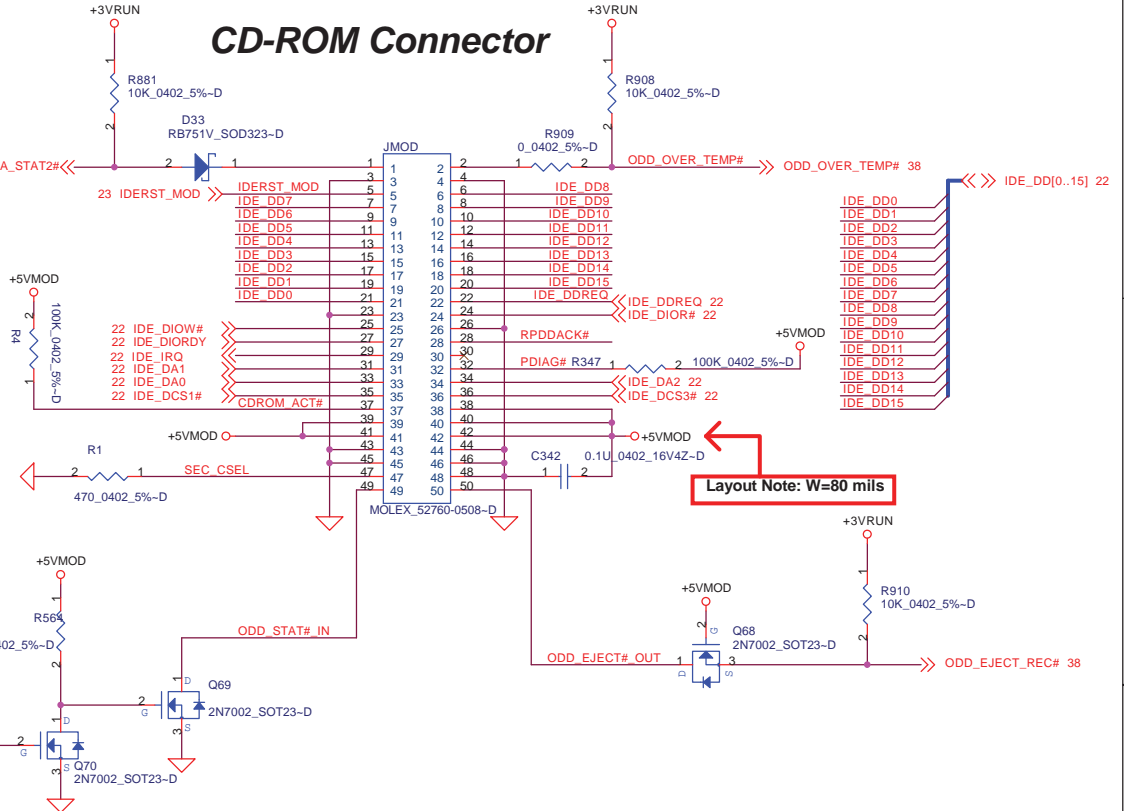


Title			ICH7(4/4)		
Size	Document Number		Rev		X03
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Date:	Wednesday, December 28, 2005	Sheet	24	of	63

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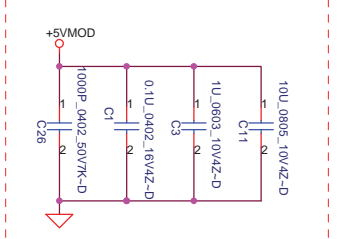


CD-ROM Connector



Layout Note: W=80 mils

Layout Note: Place close to CD-ROM CONN.



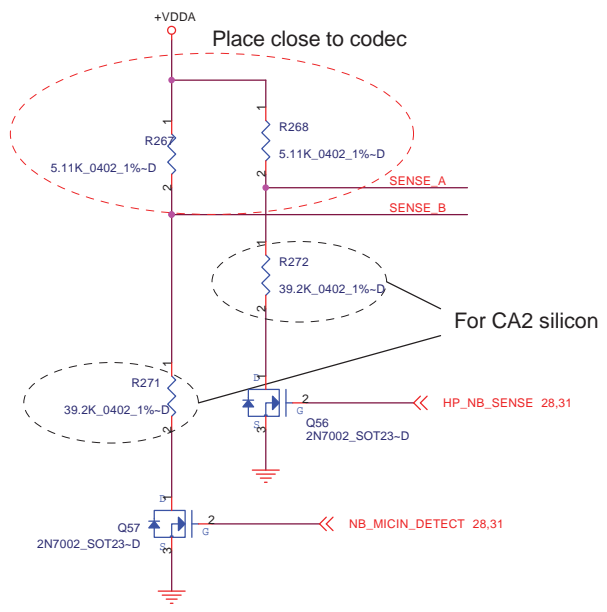
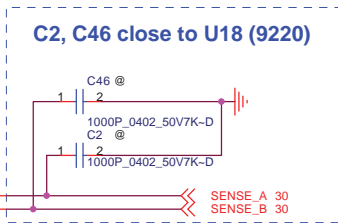
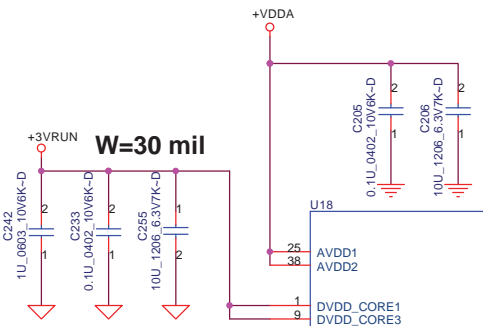
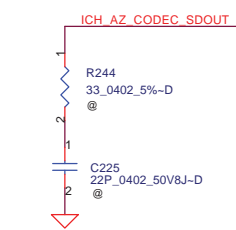
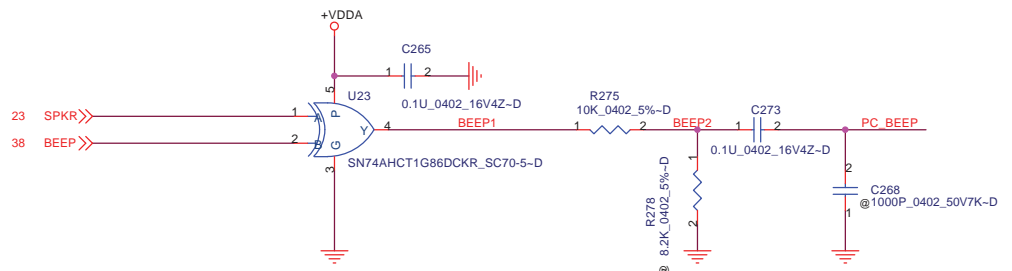
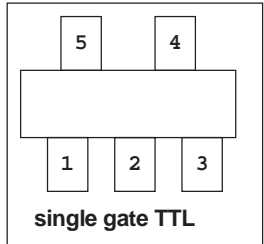
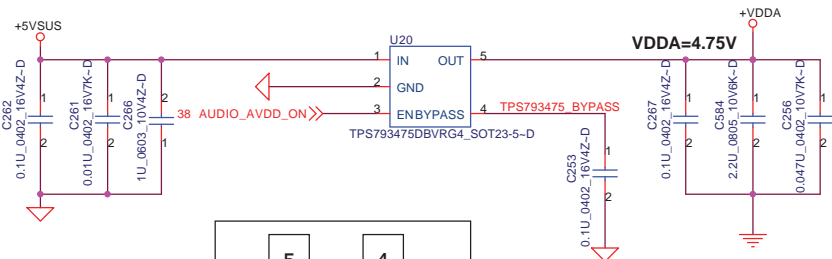
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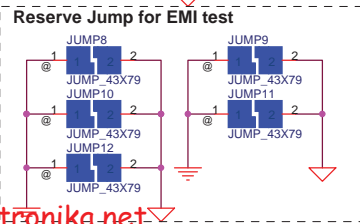
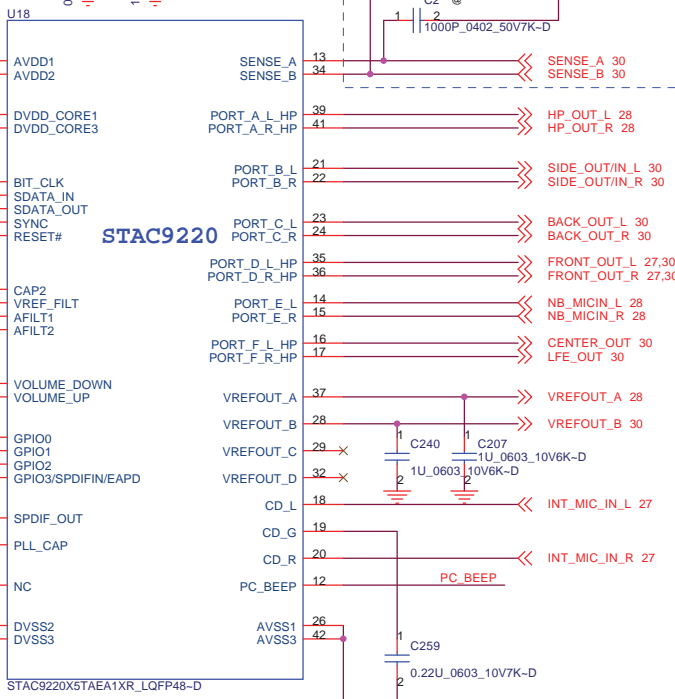
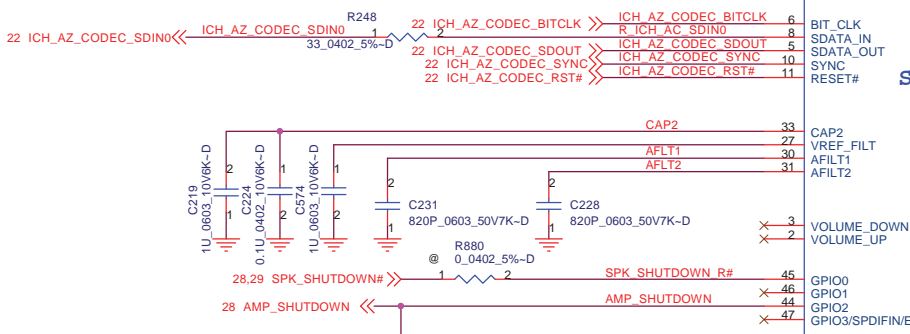


Title SATA & CD-ROM		
Size Custom	Document Number Greenland-LA2732P	Rev X03
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	R271	R272	
For CA1 silicon	5.11K	5.11K	bring-up
For CA2 silicon	39.2K	39.2K	SST



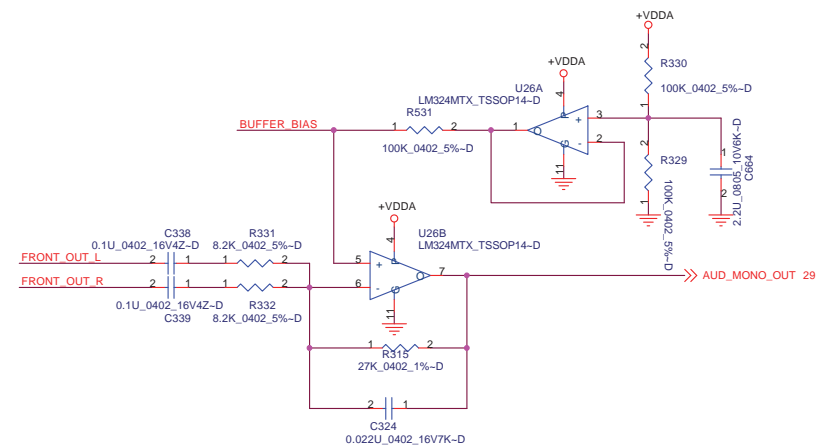
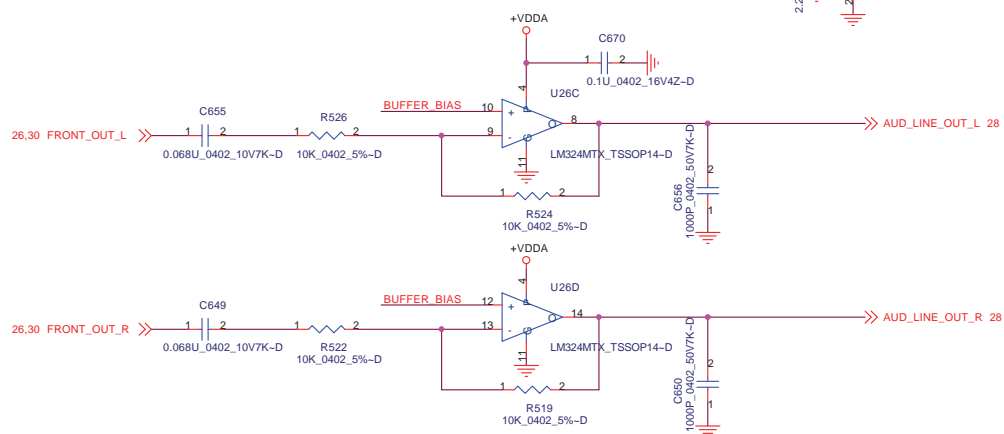
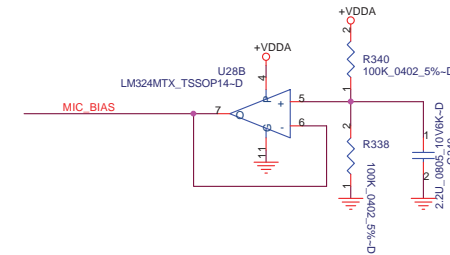
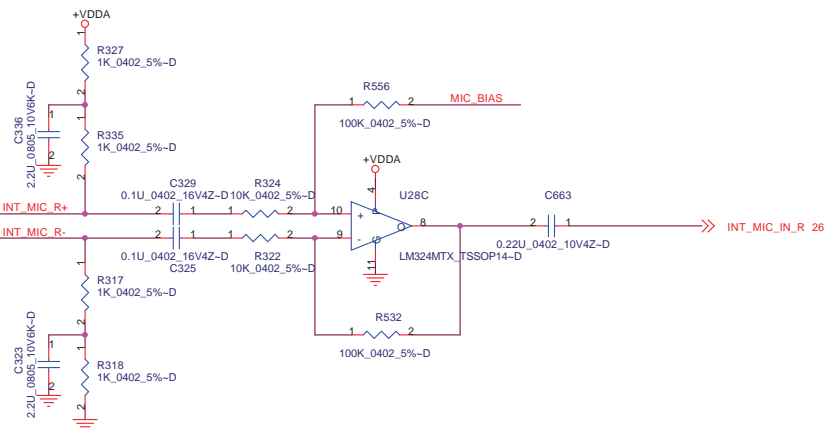
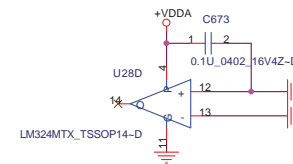
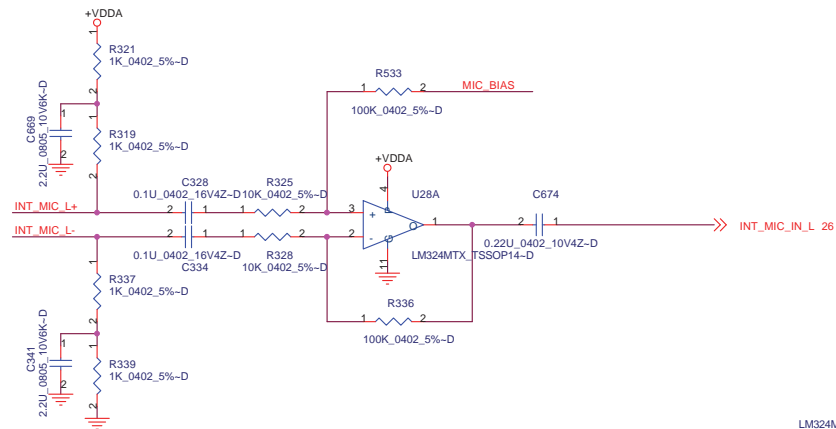
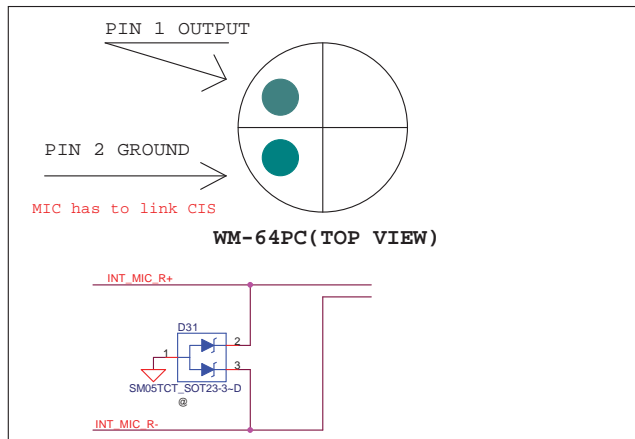
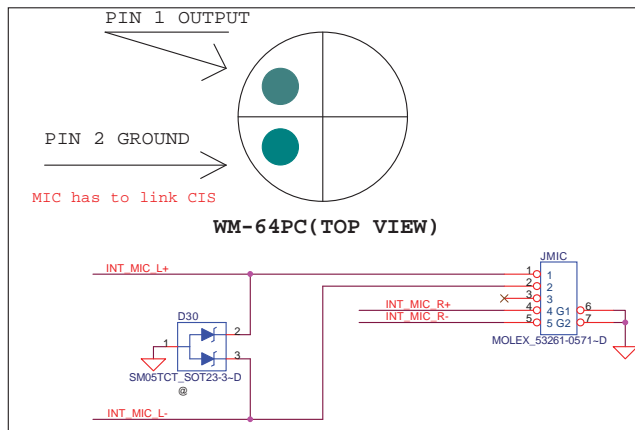
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Title: **AC97 CODEC**

Size: Document Number
Greenland-LA2732P

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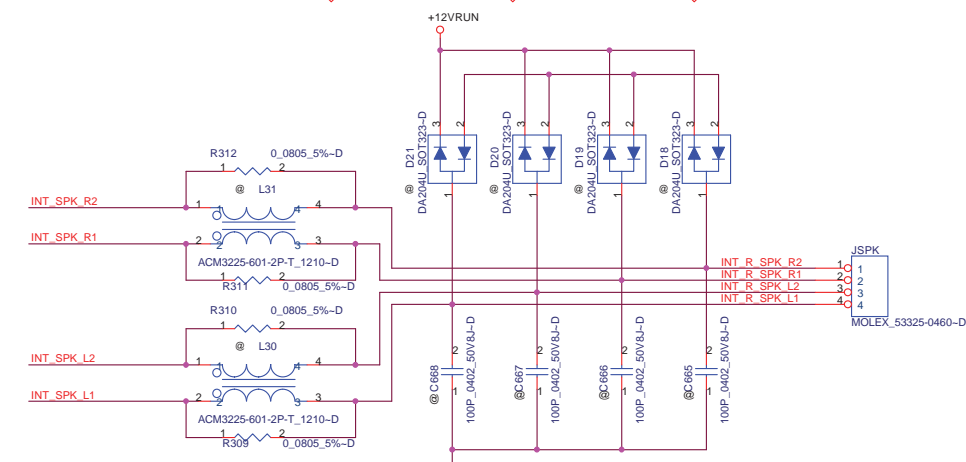
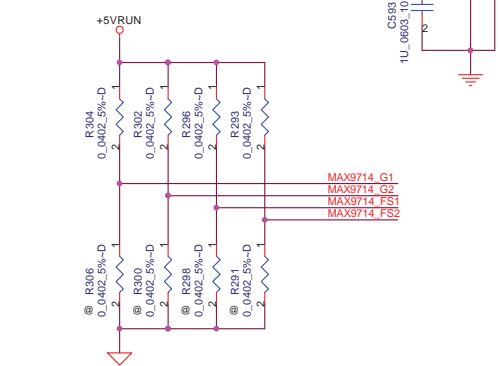
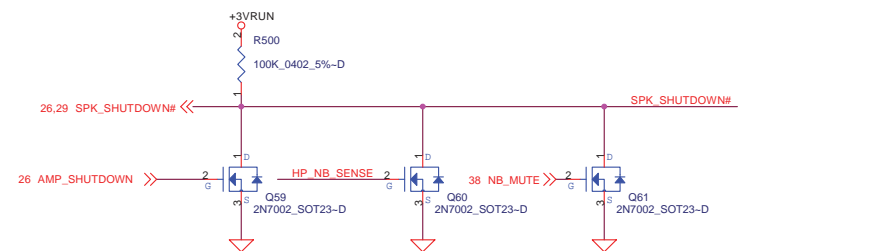
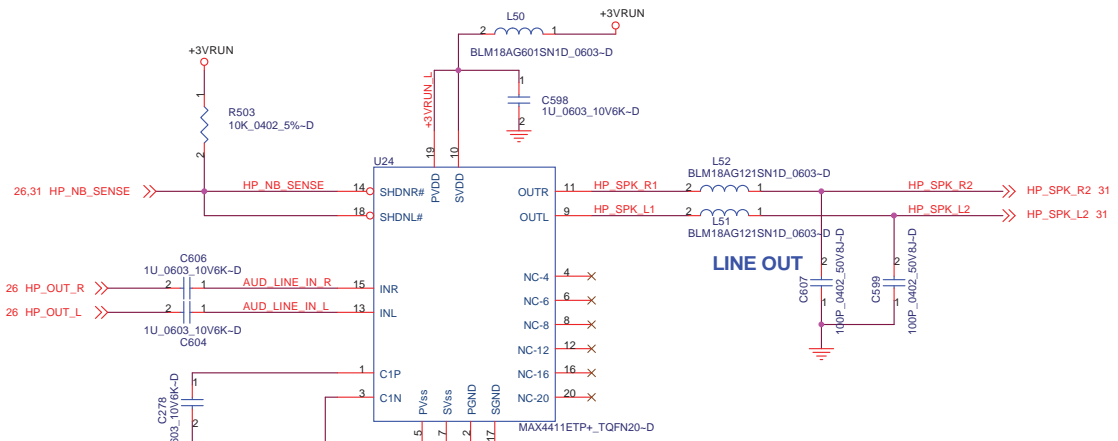
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Internal MIC

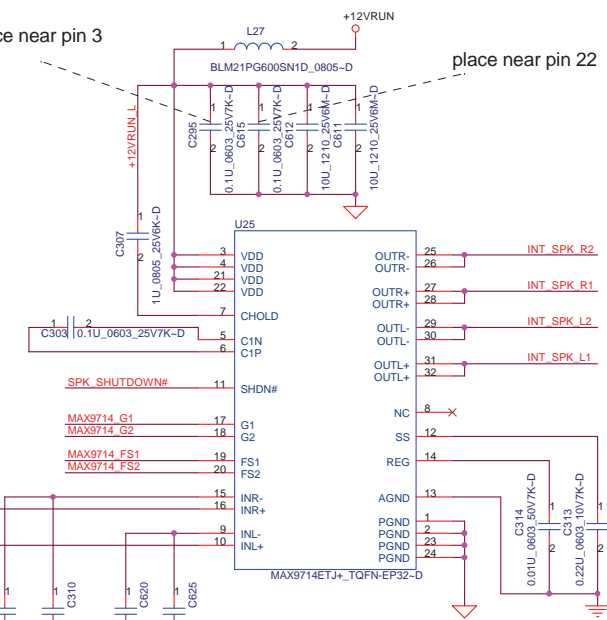
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Size	Document Number	Greenland-LA2732P	
Custom		Date:	Wednesday, December 28, 2015
		Sheet	27 of 63

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place near pin 3

place near pin 22

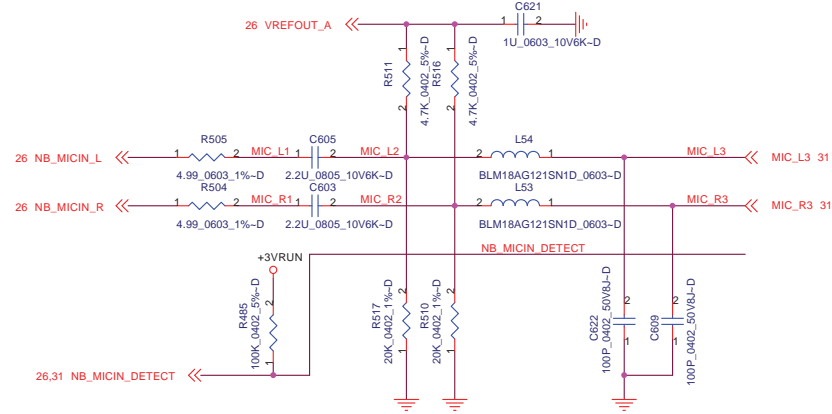
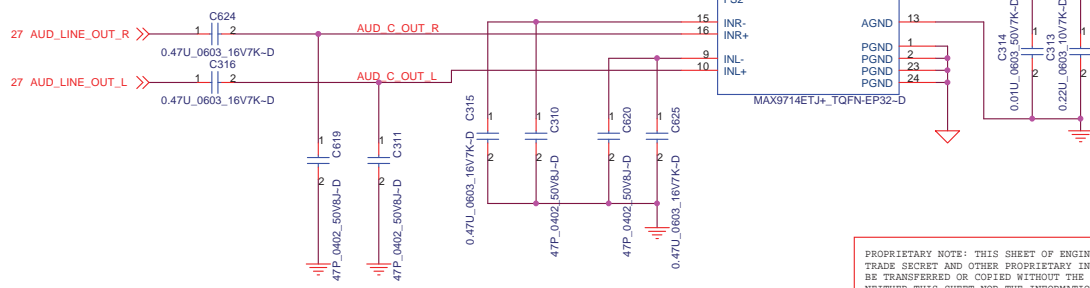


Voltage Gain selection

G1	G2	Av dB(TYP)
L	L	22.1
L	H	19.1
H	L	13
H	H	16

Oscillator frequency selection

FS1	FS2	Freq KHz
L	L	335
L	H	460
H	L	236
H	H	335 +/- 7%

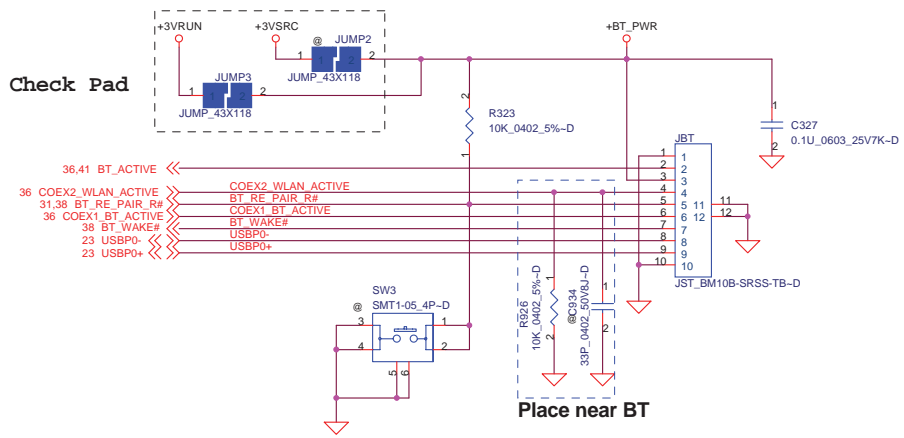


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		Compal Electronics, Inc.	
		Amplifier and Phone Jack	
Title	Document Number	Greenland-LA2732P	
Size	Date: Wednesday, December 28, 2015	Sheet 28	of 63

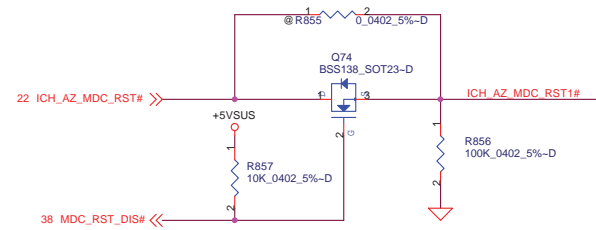
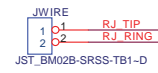
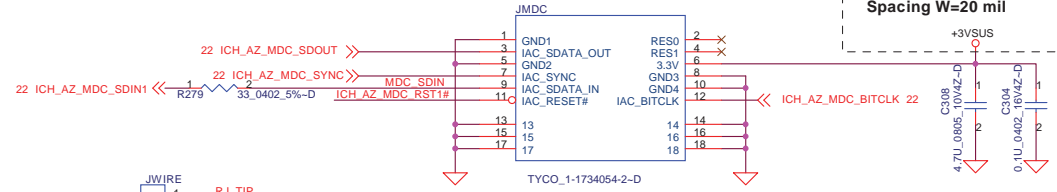
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Check Pad



Place near BT

Power/GND Minimum Spacing W=20 mil



Voltage Gain selection

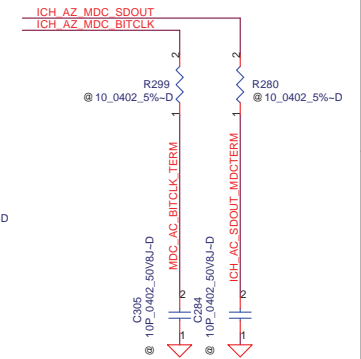
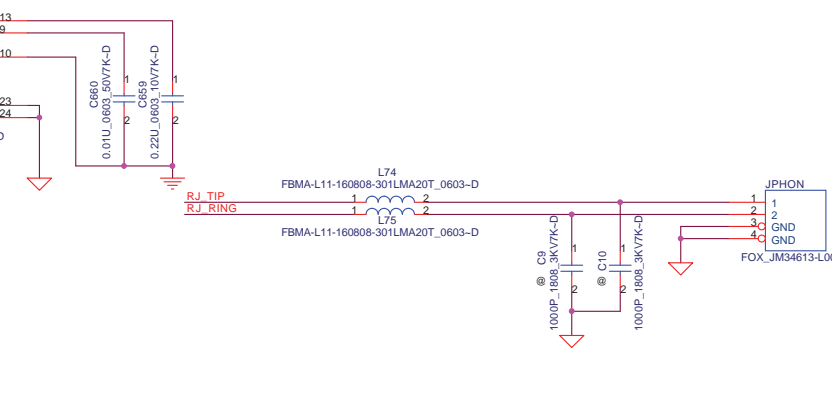
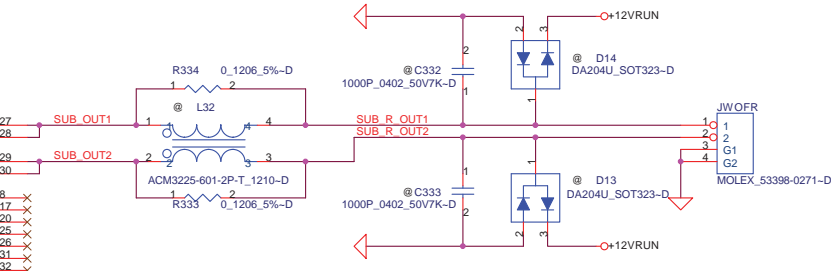
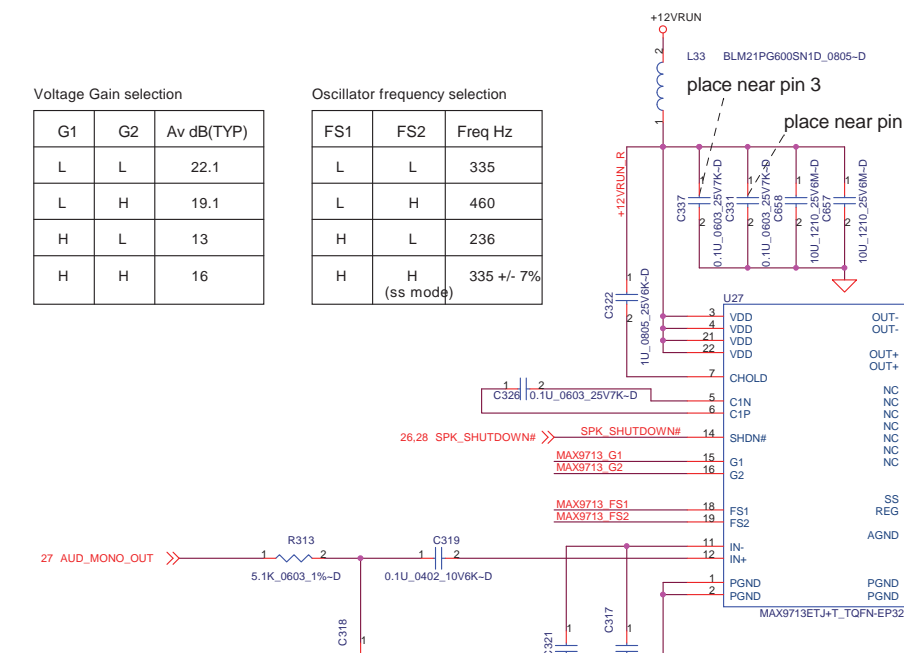
G1	G2	Av dB(TYP)
L	L	22.1
L	H	19.1
H	L	13
H	H	16

Oscillator frequency selection

FS1	FS2	Freq Hz
L	L	335
L	H	460
H	L	236
H	H	335 +/- 7% (ss mode)

place near pin 3

place near pin 22



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SUBWOOFER & BT & MDC

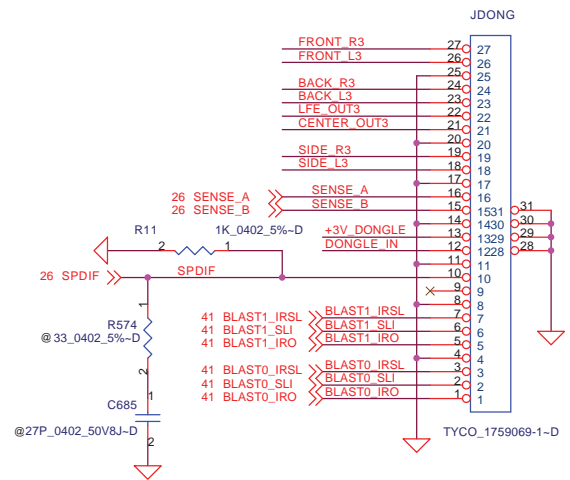
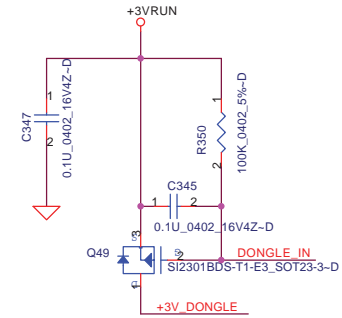
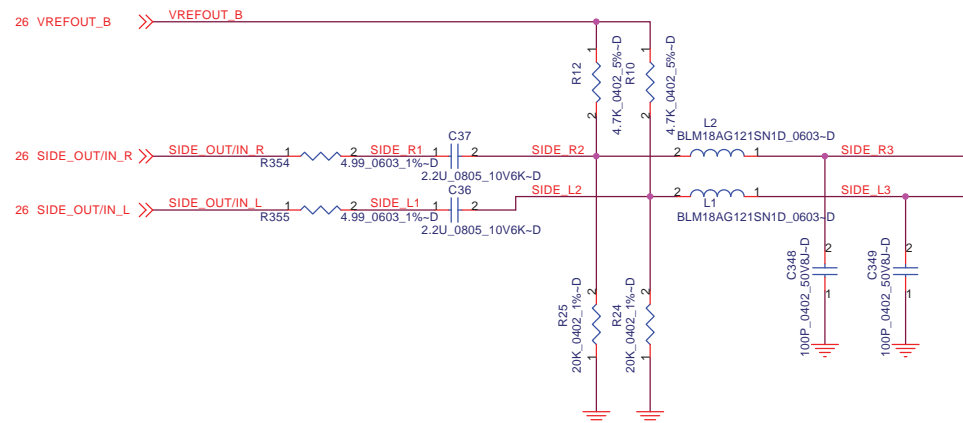
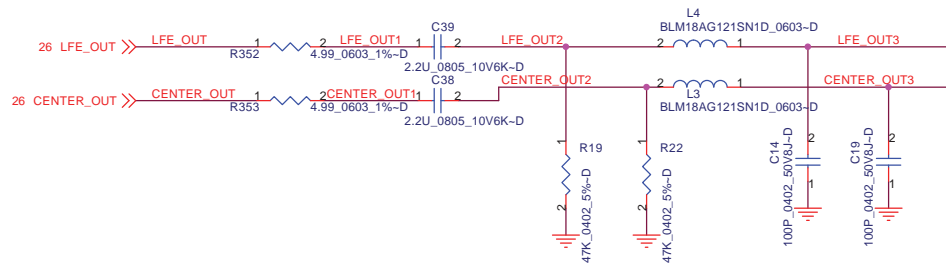
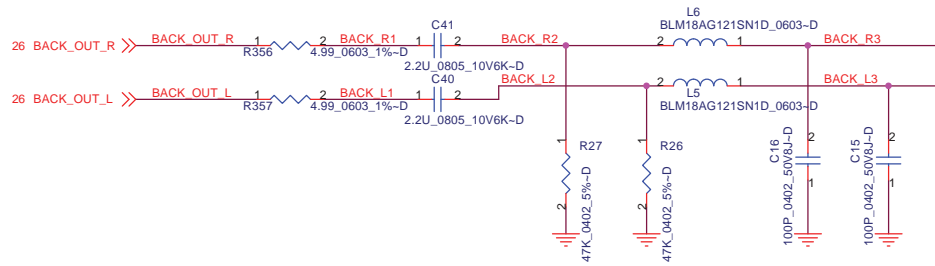
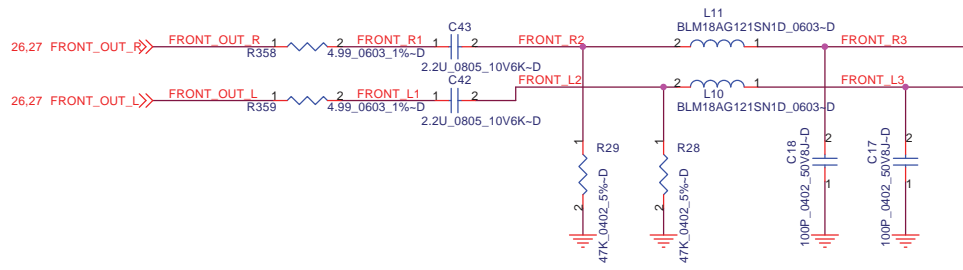
Greenland-LA2732P



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Title	SUBWOOFER & BT & MDC	
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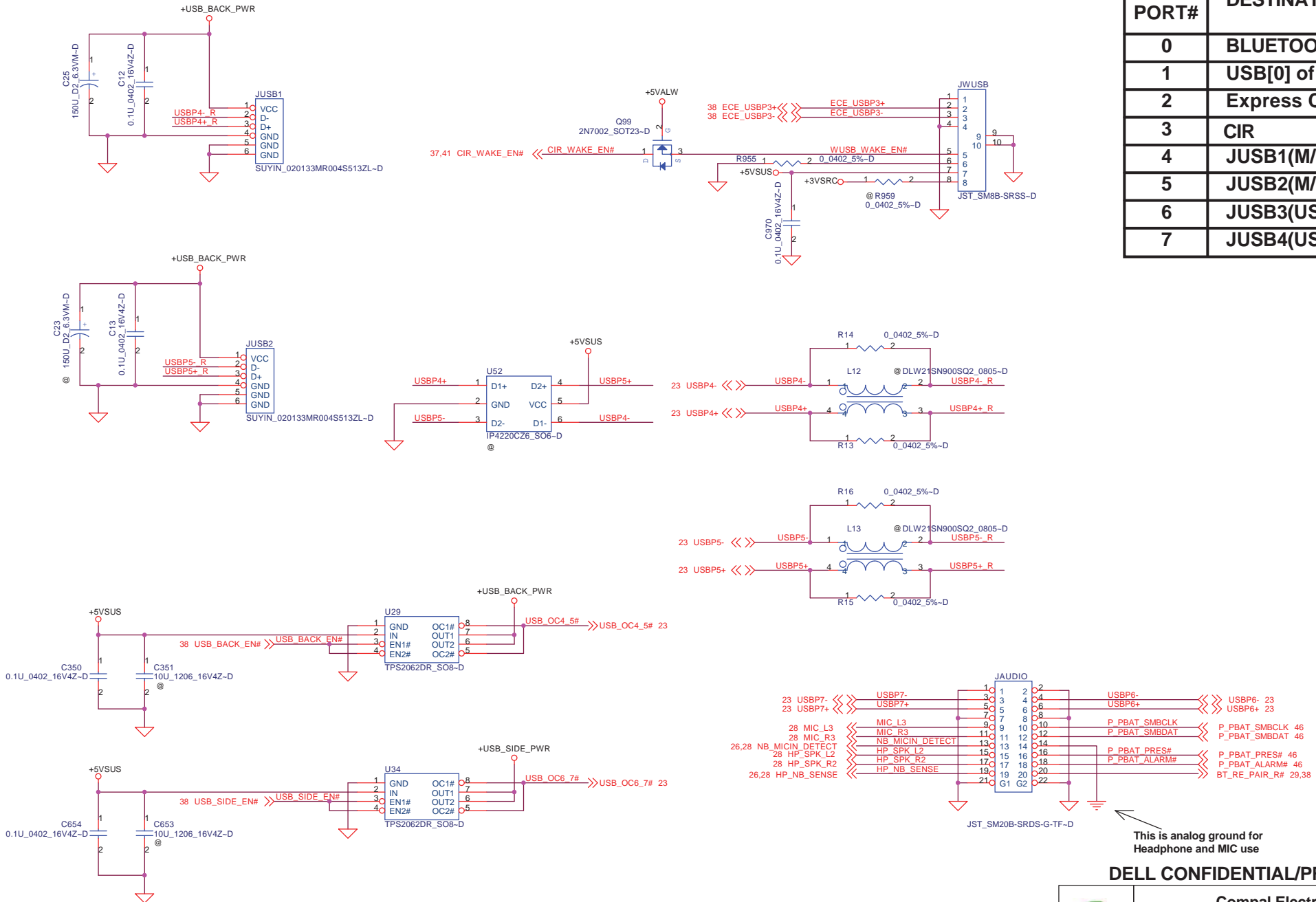


Title		Audio DONGLE	
Size	Document Number	Greenland-LA2732P	
Date:	Wednesday, December 28, 2005	Sheet	30 of 63
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USB TABLE

USB PORT#	DESTINATION
0	BLUETOOTH
1	USB[0] of ECE5011
2	Express Card
3	CIR
4	JUSB1(M/B)
5	JUSB2(M/B)
6	JUSB3(USB/BD)
7	JUSB4(USB/BD)



This is analog ground for Headphone and MIC use

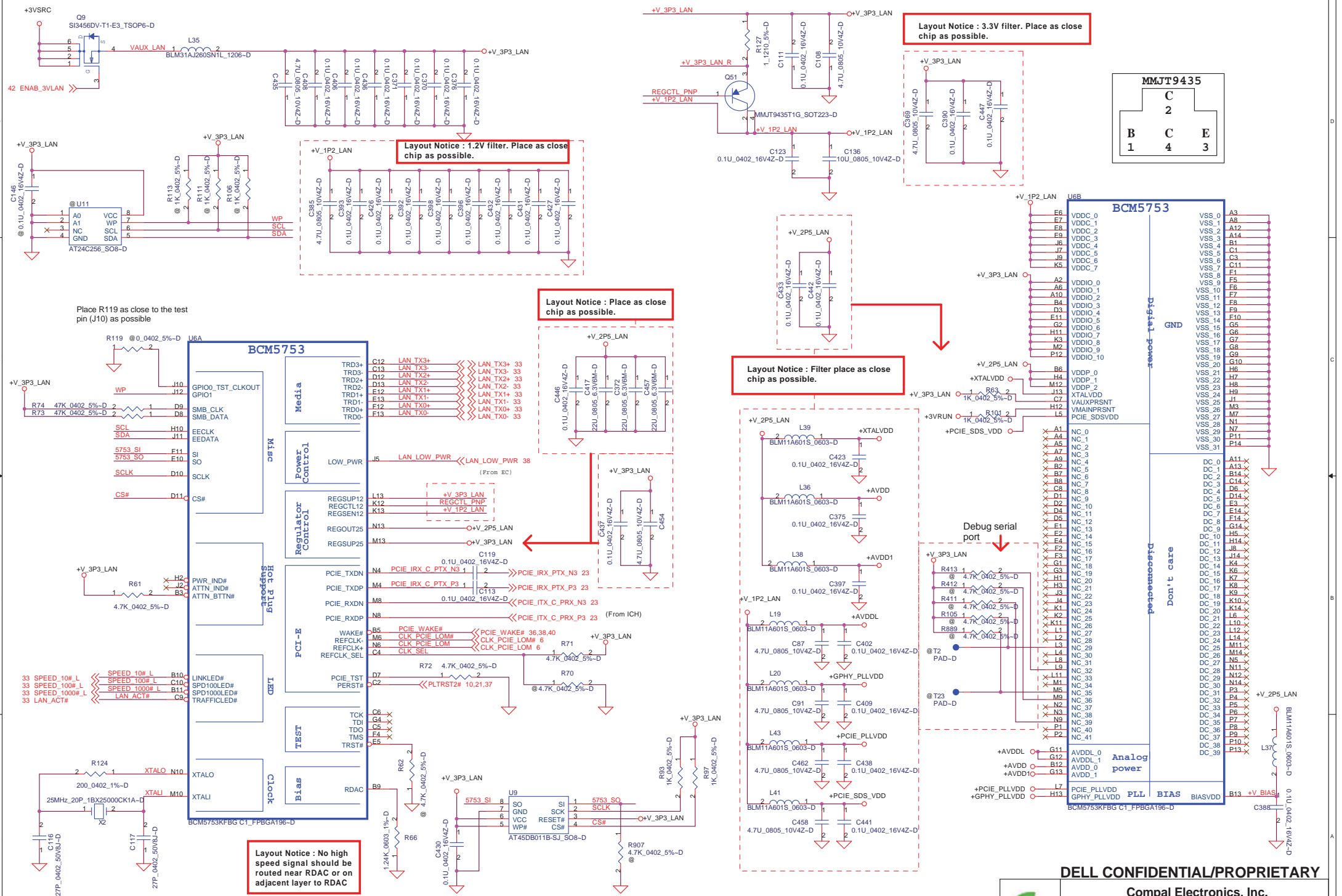
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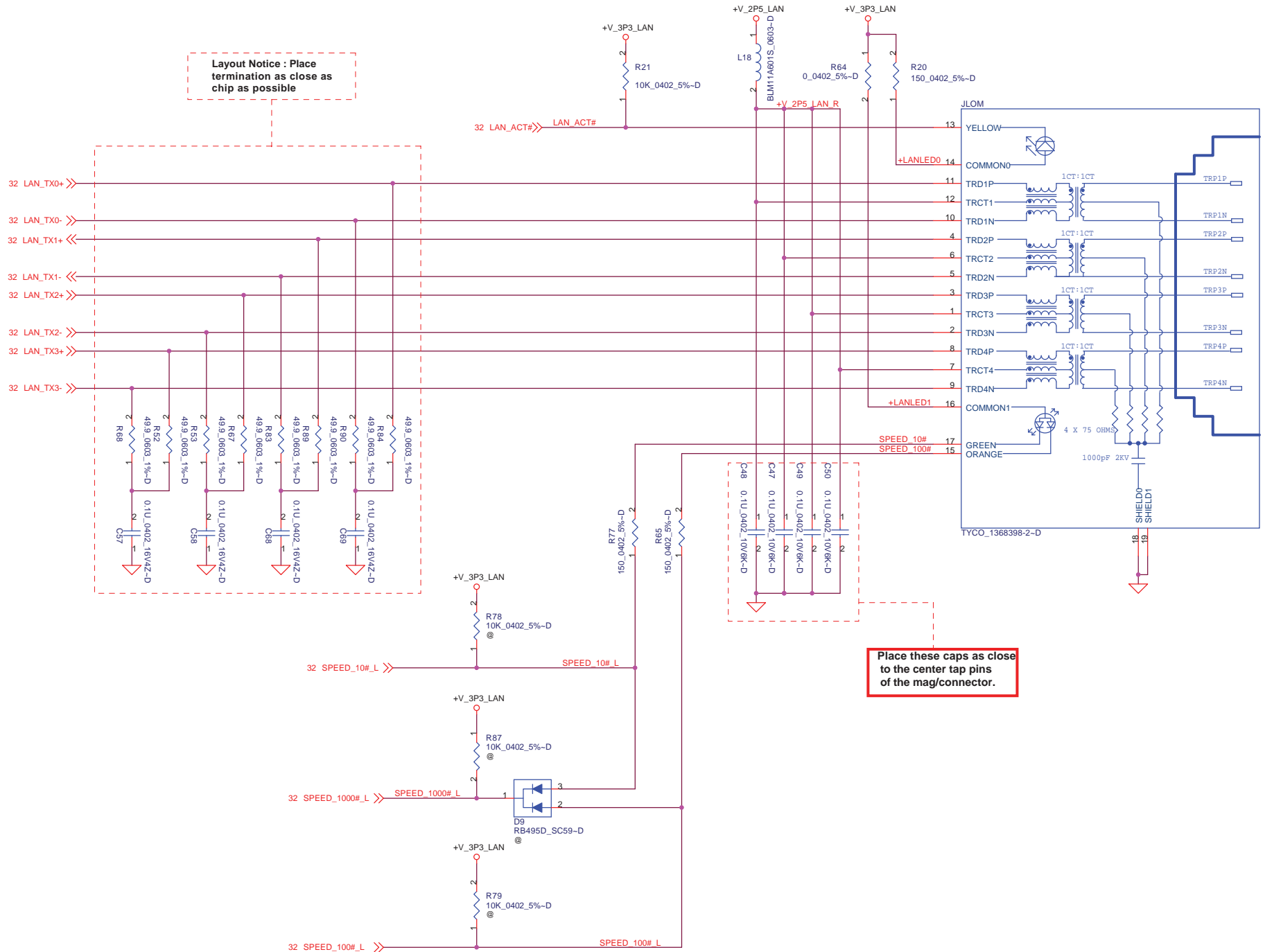
Title		USB 2.0 PORT	
Size	Document Number	Greenland-LA2732P	
Date:	Wednesday, December 28, 2005	Sheet	31 of 63
Rev	X03		

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Layout Notice : Place termination as close as chip as possible



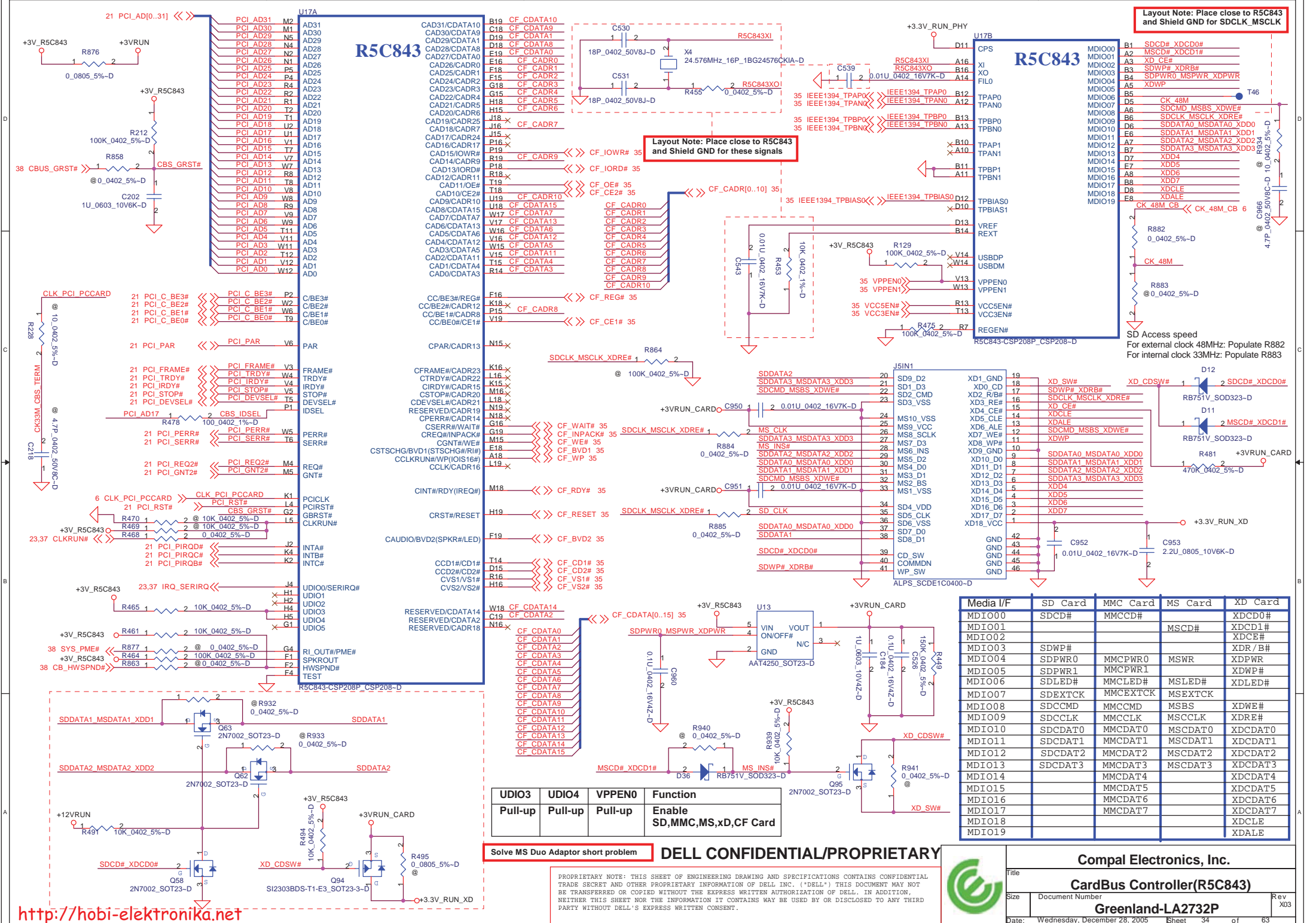
Place these caps as close to the center tap pins of the mag/connector.

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Title		
LAN Transfomer and RJ45		
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		X03
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Layout Note: Place close to R5C843 and Shield GND for SDCLK_MSCLK

Layout Note: Place close to R5C843 and Shield GND for these signals

SD Access speed
For external clock 48MHz: Populate R882
For internal clock 33MHz: Populate R883

Media I/F	SD Card	MMC Card	MS Card	XD Card
MDIO00	SDCD#	MMCCD#	MSWB#	XDCD0#
MDIO01	SDCD1#	MMCCD1#	MSWB1#	XDCD1#
MDIO02	SDCE#	MMCE#	MSWB#	XDCE#
MDIO03	SDWP#	MMCPWR0	MSWR	XDPWR
MDIO04	SDPWR0	MMCPWR1	MSWR	XDPWR
MDIO05	SDLE#	MMCLE#	MSLE#	XDLE#
MDIO06	SDLE#	MMCLE#	MSLE#	XDLE#
MDIO07	SDEXTCK	MMCEXTCK	MSEXTCK	XDEXTCK
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14	SDCDAT4	MMCDAT4	MSCDAT4	XDCDAT4
MDIO15	SDCDAT5	MMCDAT5	MSCDAT5	XDCDAT5
MDIO16	SDCDAT6	MMCDAT6	MSCDAT6	XDCDAT6
MDIO17	SDCDAT7	MMCDAT7	MSCDAT7	XDCDAT7
MDIO18	XDCL#	MMCDAT7	MSCDAT7	XDCDAT7
MDIO19	XDAL#	MMCDAT7	MSCDAT7	XDCDAT7

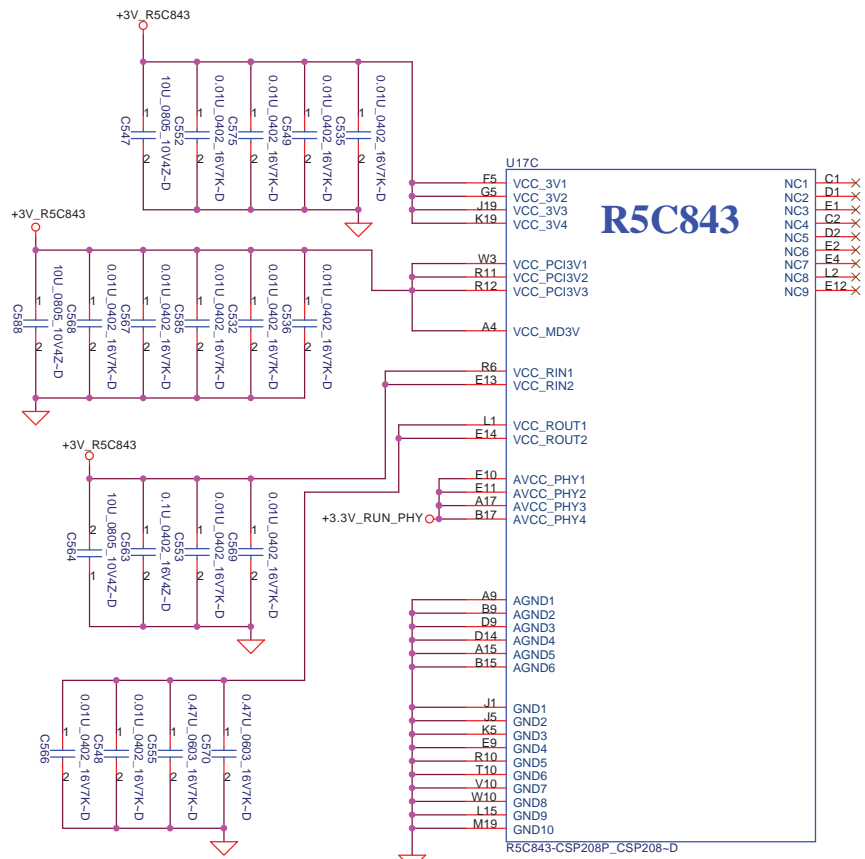
UDIO3	UDIO4	VPPEN0	Function
Pull-up	Pull-up	Pull-up	Enable SD,MMC,MS,xD,CF Card

Solve MS Duo Adaptor short problem **DELL CONFIDENTIAL/PROPRIETARY**

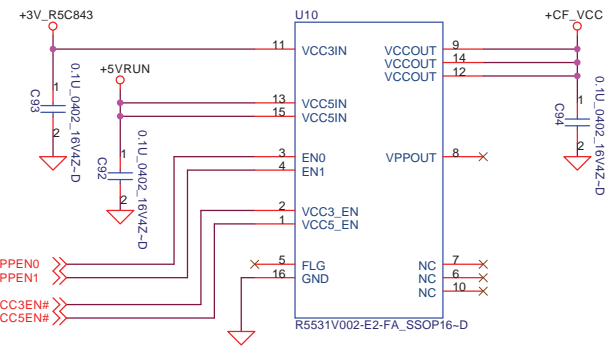
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Title		CardBus Controller(R5C843)	
Size	Document Number	Greenland-LA2732P	
Date:	Wednesday, December 28, 2005	Sheet	34 of 63
			Rev X03

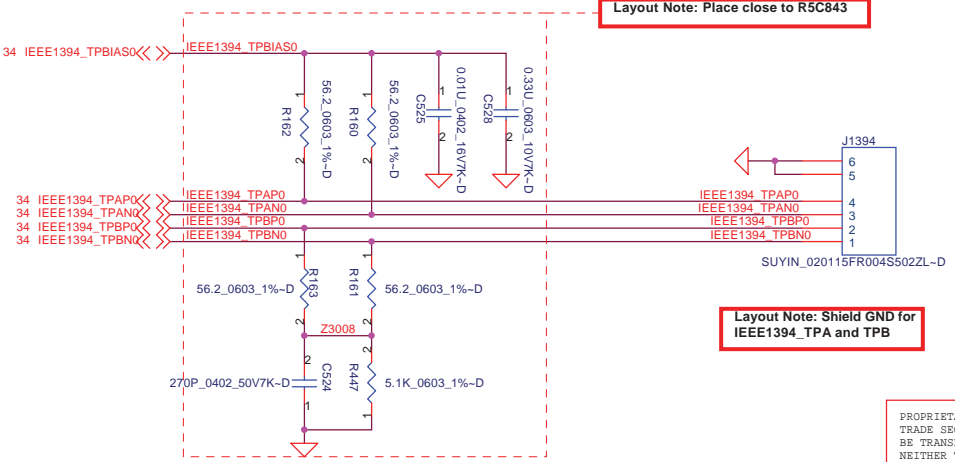
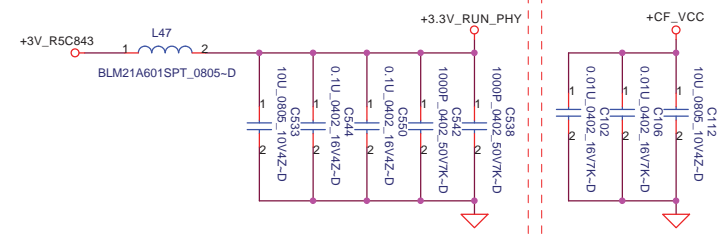


R5C843



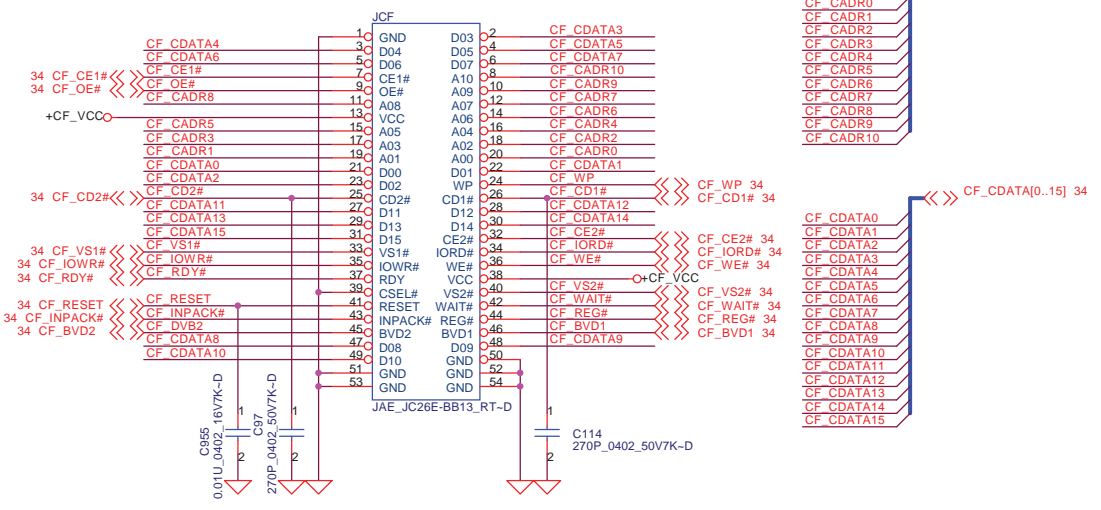
Layout Note: Place close to R5C843

Place close to JCF



Layout Note: Place close to R5C843

Layout Note: Shield GND for IIEEE1394_TPA and TPB



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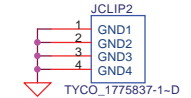
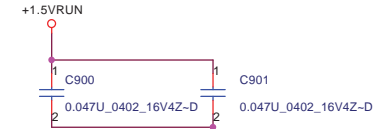
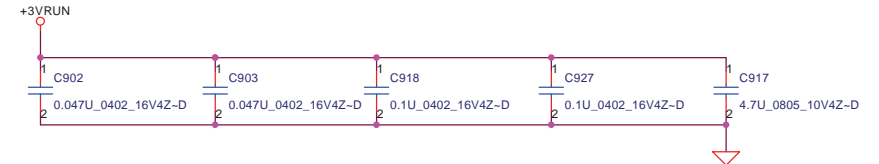
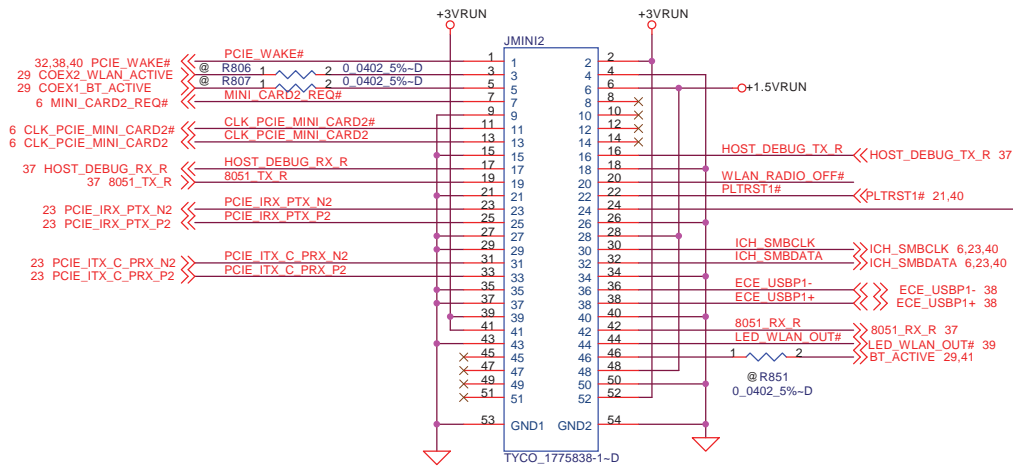


Compal Electronics, Inc.
CardBus/SD card Socket
Greenland-LA2732P

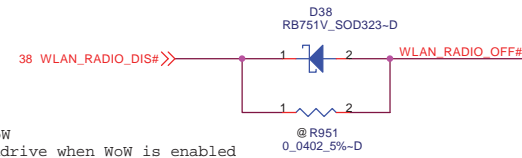
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 Size: Document Number _____ Rev X03
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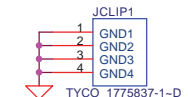
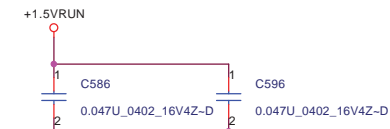
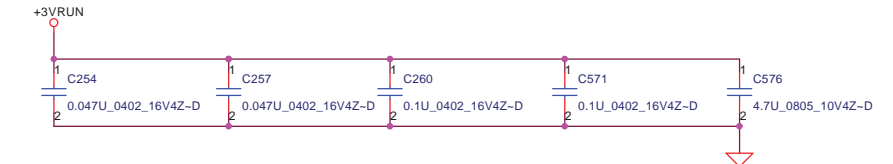
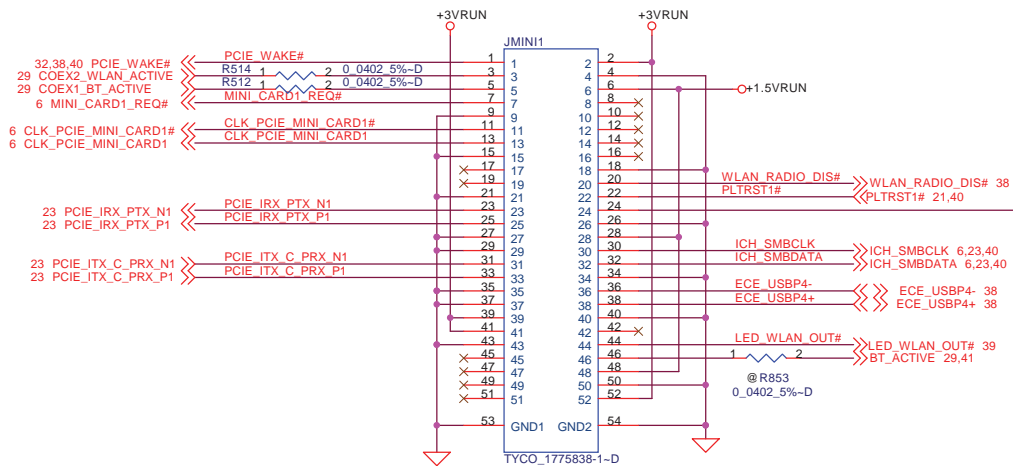
Mini-Express Card Wire less LAN



Mini-Card Latch



Mini-Express Card TV



Mini-Card Latch

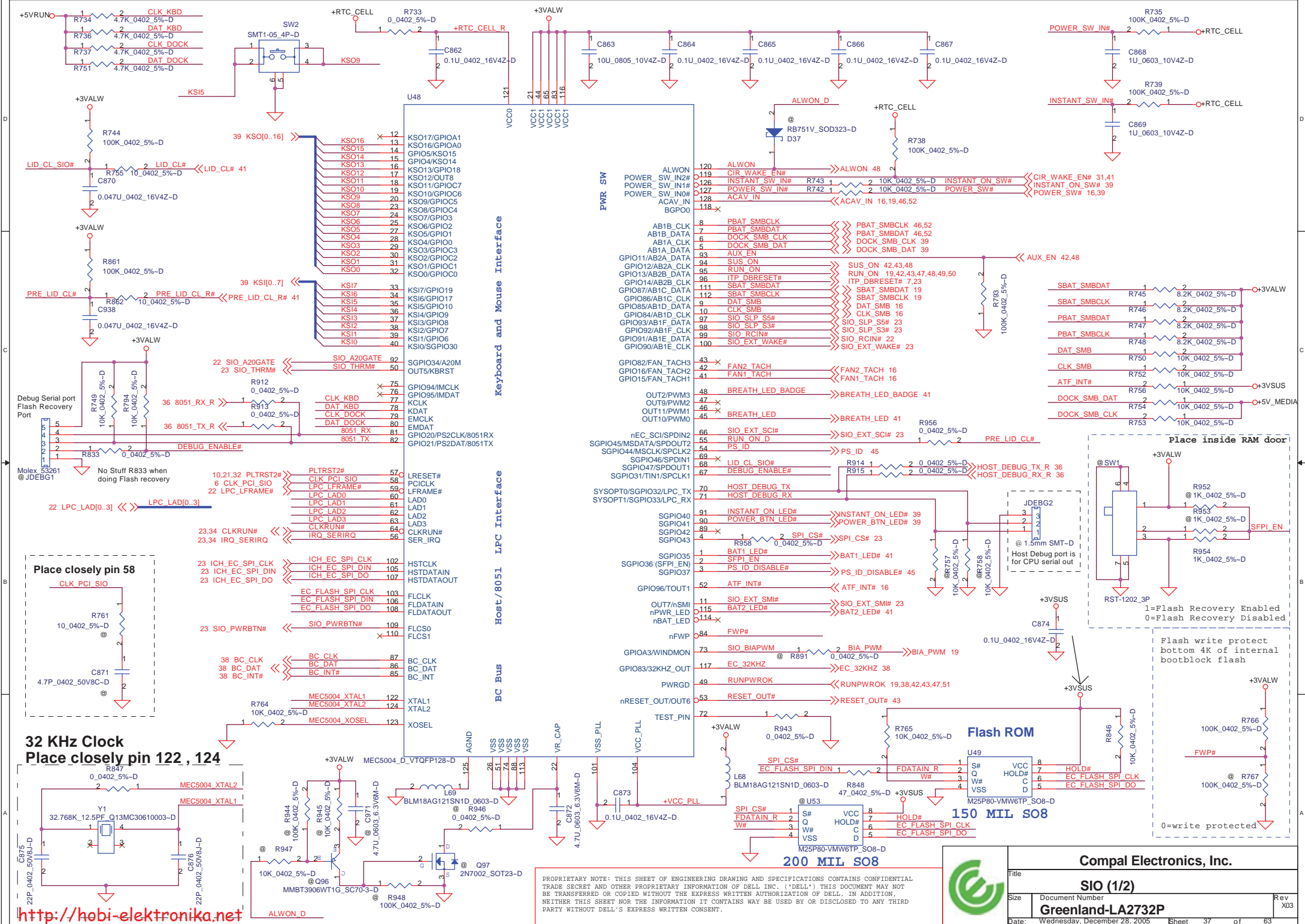
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Title		MINI-CARD WLAN/TV	
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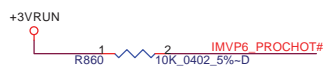
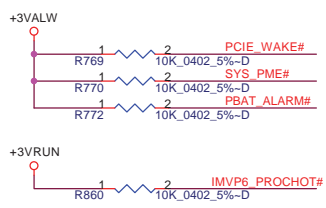
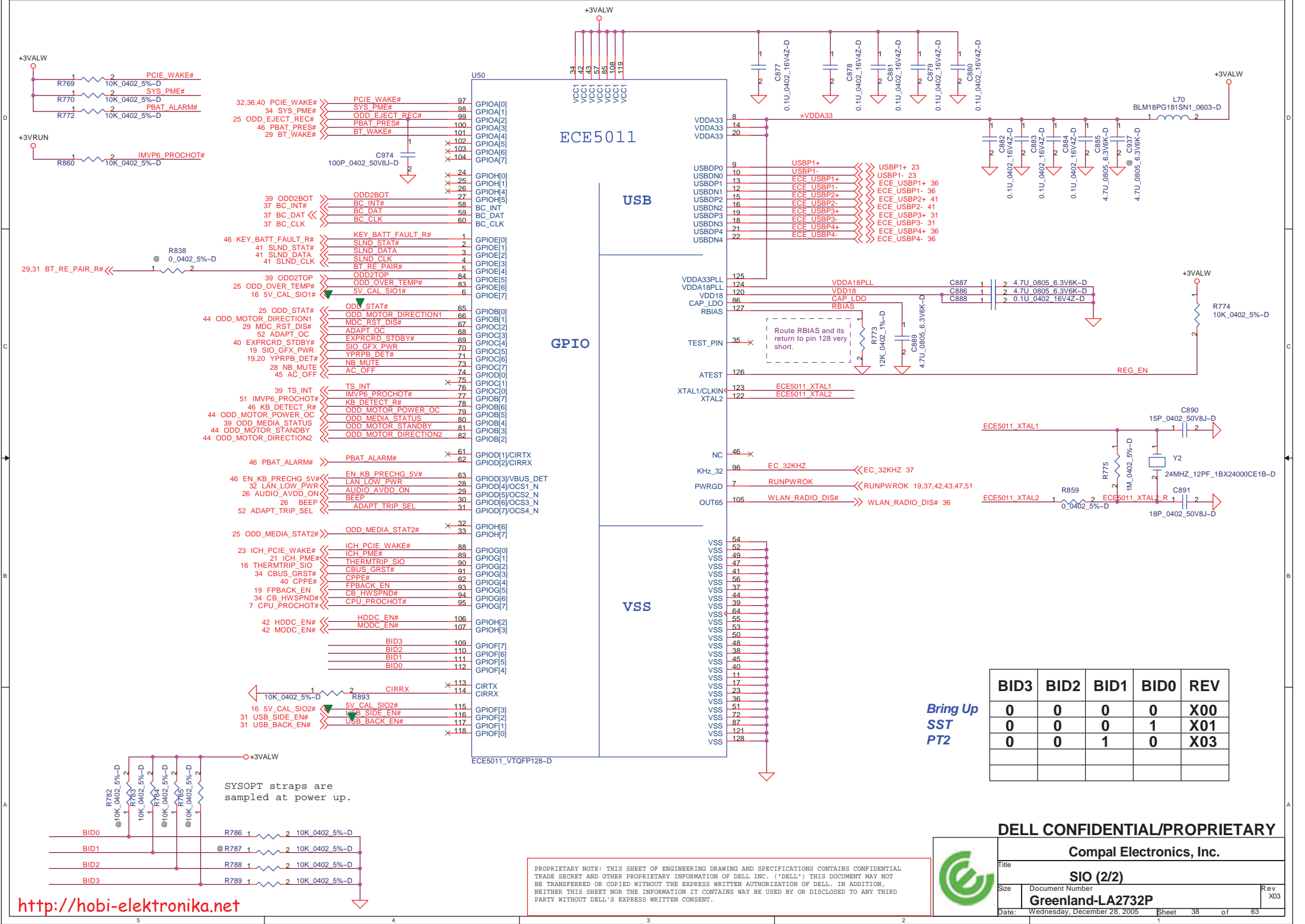


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SIO (1/2)		
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- 32,36,40 PCIE_WAKE# << PCIE_WAKE# 97
- 34 SYS_PME# << SYS_PME# 98
- 25 ODD_EJECT_REC# << ODD_EJECT_REC# 99
- 46 PBAT_ALARM# << PBAT_ALARM# 100
- 29 BT_WAKE# << BT_WAKE# 101
- 39 ODD2BOT << ODD2BOT 102
- 37 BC_INT# << BC_INT# 103
- 37 BC_DAT << BC_DAT 104
- 37 BC_CLK << BC_CLK 105
- 46 KEY_BATT_FAULT_R# << KEY_BATT_FAULT_R# 1
- 41 SLND_STAT# << SLND_STAT# 2
- 41 SLND_DATA << SLND_DATA 3
- 41 SLND_CLK << SLND_CLK 4
- 29,31 BT_RE_PAIR_R# << BT_RE_PAIR_R# 5
- 39 ODD2TOP << ODD2TOP 84
- 25 ODD_OVER_TEMP# << ODD_OVER_TEMP# 83
- 16 5V_CAL_SIO1# << 5V_CAL_SIO1# 6
- 25 ODD_STAT# << ODD_STAT# 65
- 44 ODD_MOTOR_DIRECTION1 << ODD_MOTOR_DIRECTION1 66
- 29 MDC_RST_DIS# << MDC_RST_DIS# 67
- 52 ADAPT_OC << ADAPT_OC 68
- 40 EXPRCRD_STDBY# << EXPRCRD_STDBY# 69
- 19 SIO GFX_PWR << SIO GFX_PWR 70
- 19,20 YPRPB_DET# << YPRPB_DET# 71
- 28 NB_MUTE << NB_MUTE 73
- 45 AC_OFF << AC_OFF 74
- 39 TS_INT << TS_INT 75
- 51 IMVP6_PROCHOT# << IMVP6_PROCHOT# 76
- 45 KB_DETECT_R# << KB_DETECT_R# 77
- 44 ODD_MOTOR_POWER_OC << ODD_MOTOR_POWER_OC 78
- 39 ODD_MEDIA_STATUS << ODD_MEDIA_STATUS 79
- 44 ODD_MOTOR_STANDBY << ODD_MOTOR_STANDBY 80
- 44 ODD_MOTOR_DIRECTION2 << ODD_MOTOR_DIRECTION2 81
- 46 PBAT_ALARM# << PBAT_ALARM# 61
- 46 EN_KB_PRECHG_5V# << EN_KB_PRECHG_5V# 63
- 32 LAN_LOW_PWR << LAN_LOW_PWR 28
- 26 AUDIO_AVDD_ON << AUDIO_AVDD_ON 29
- 26 BEEP << BEEP 30
- 52 ADAPT_TRIP_SEL << ADAPT_TRIP_SEL 31
- 25 ODD_MEDIA_STAT2# << ODD_MEDIA_STAT2# 32
- 23 ICH_PCIE_WAKE# << ICH_PCIE_WAKE# 88
- 21 ICH_PME# << ICH_PME# 89
- 16 THERMTRIP_SIO << THERMTRIP_SIO 90
- 34 CBUS_GRST# << CBUS_GRST# 91
- 40 CPPE# << CPPE# 92
- 19 FPBACK_EN << FPBACK_EN 93
- 34 CB_HWSPND# << CB_HWSPND# 94
- 7 CPU_PROCHOT# << CPU_PROCHOT# 95
- 42 HDDC_EN# << HDDC_EN# 106
- 42 MODC_EN# << MODC_EN# 107
- 113 CIRR# << CIRR# 113
- 114 CIRR# << CIRR# 114
- 16 5V_CAL_SIO2# << 5V_CAL_SIO2# 115
- 31 USB_SIDE_EN# << USB_SIDE_EN# 116
- 31 USB_BACK_EN# << USB_BACK_EN# 117
- 118 CIRR# << CIRR# 118

ECE5011

USB

GPIO

VSS

BID3	BID2	BID1	BID0	REV
0	0	0	0	X00
0	0	0	1	X01
0	0	1	0	X03

Bring Up
SST
PT2

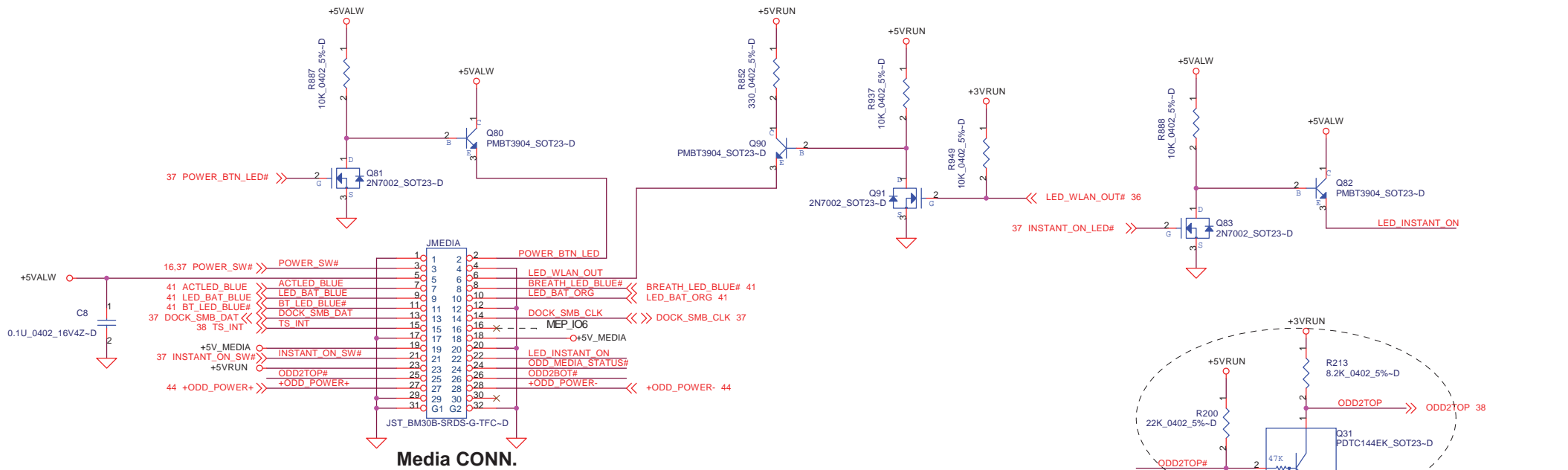
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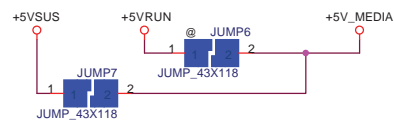
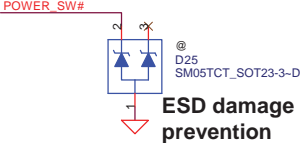
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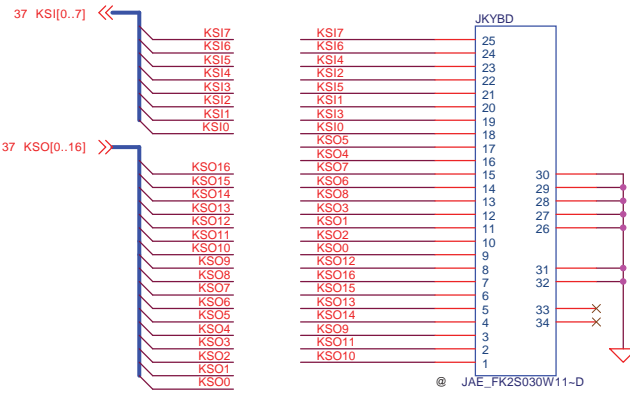
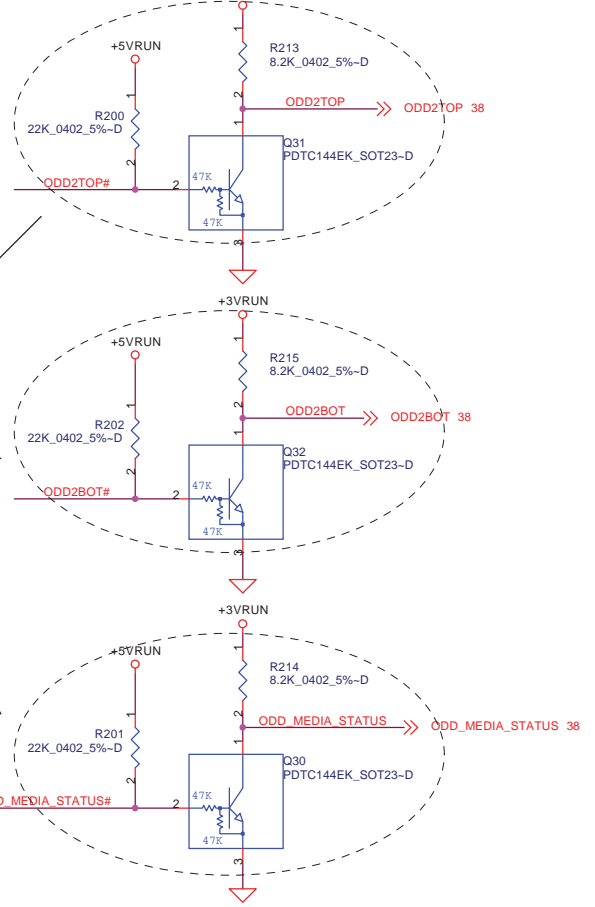
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Media CONN.



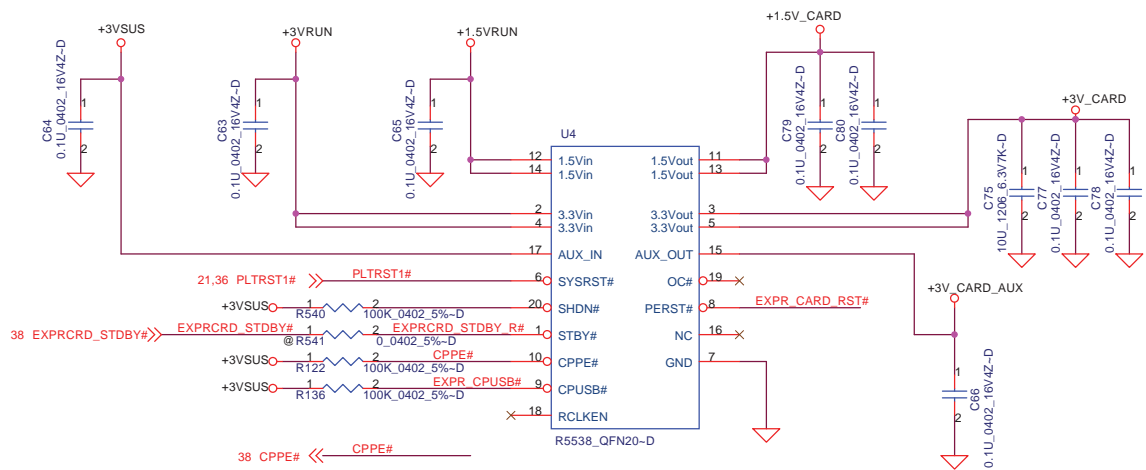
Level shift for EC



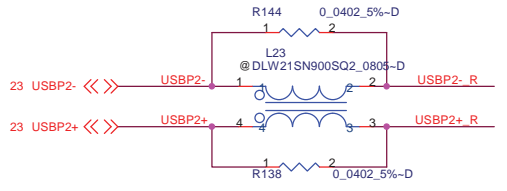
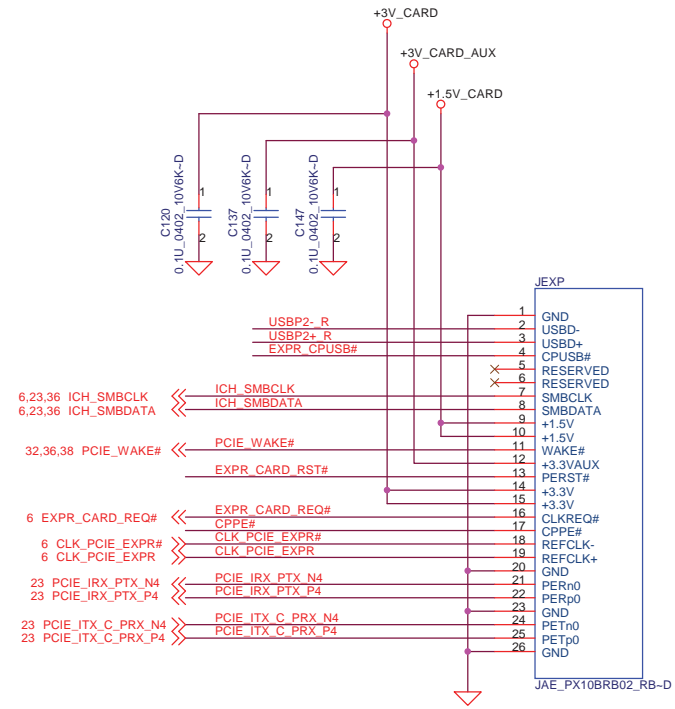
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		INT KB & Media Conn.	
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+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA



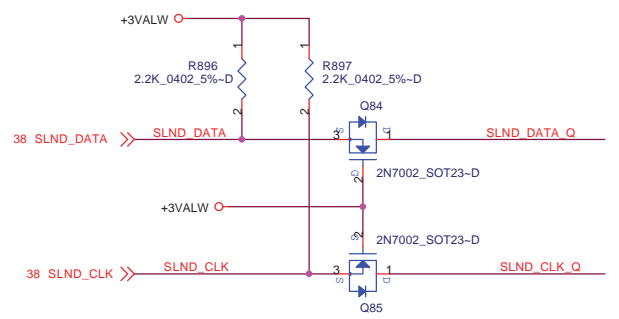
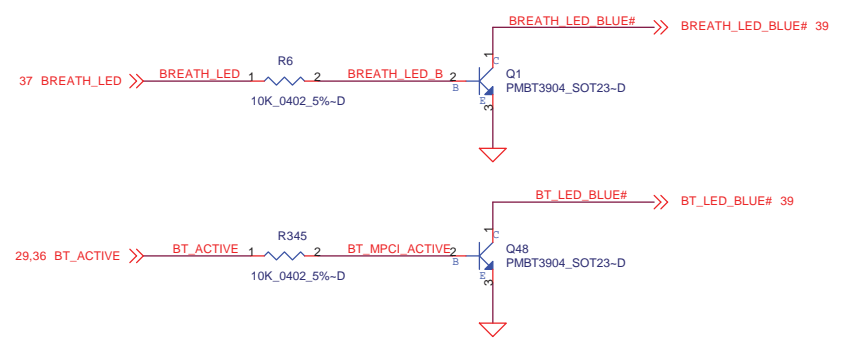
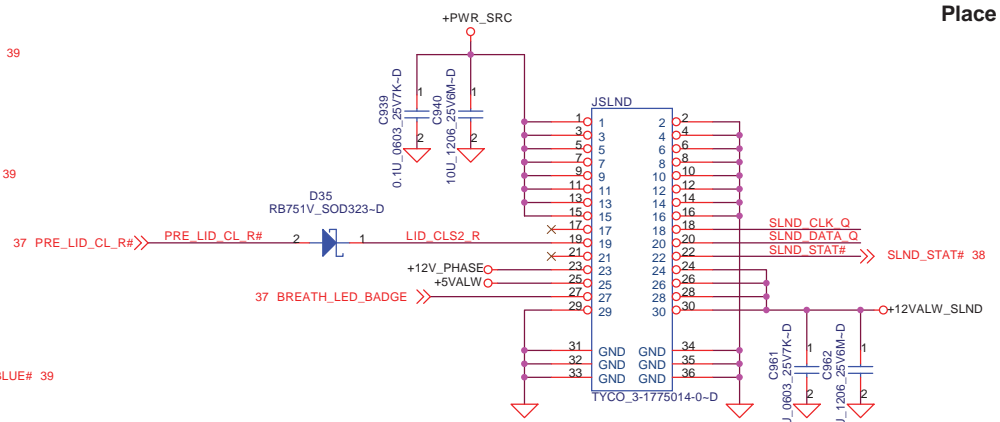
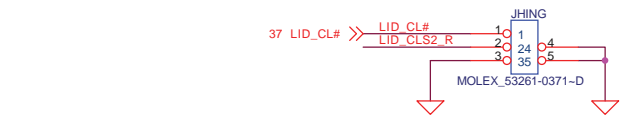
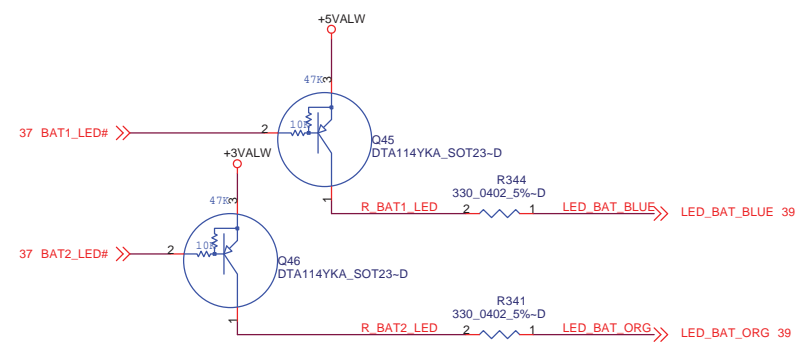
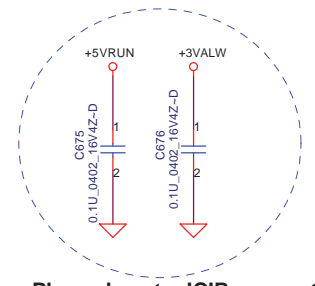
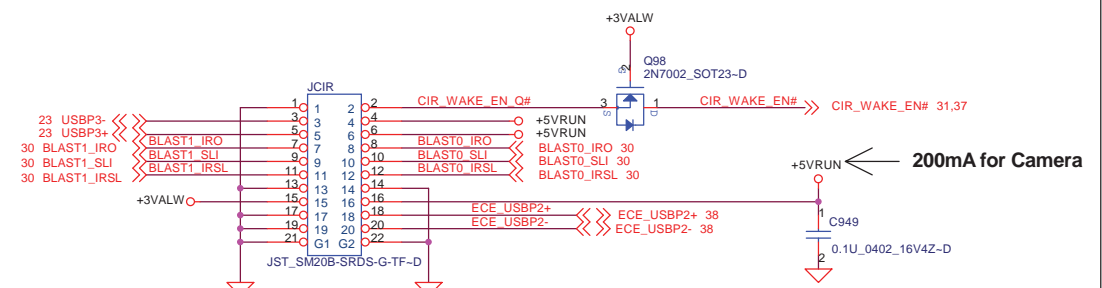
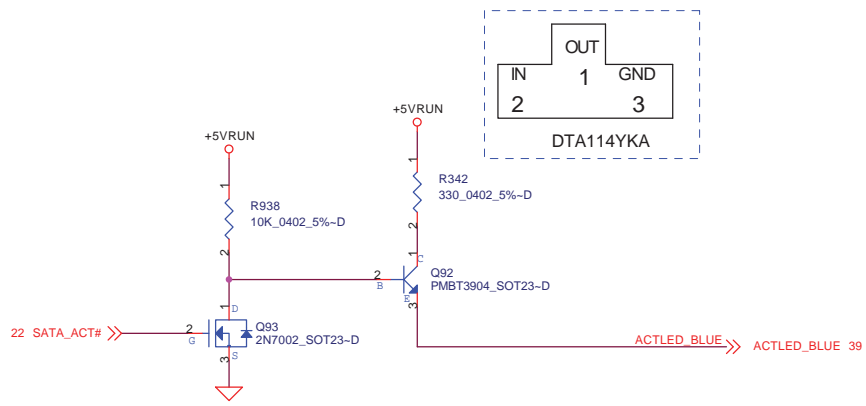
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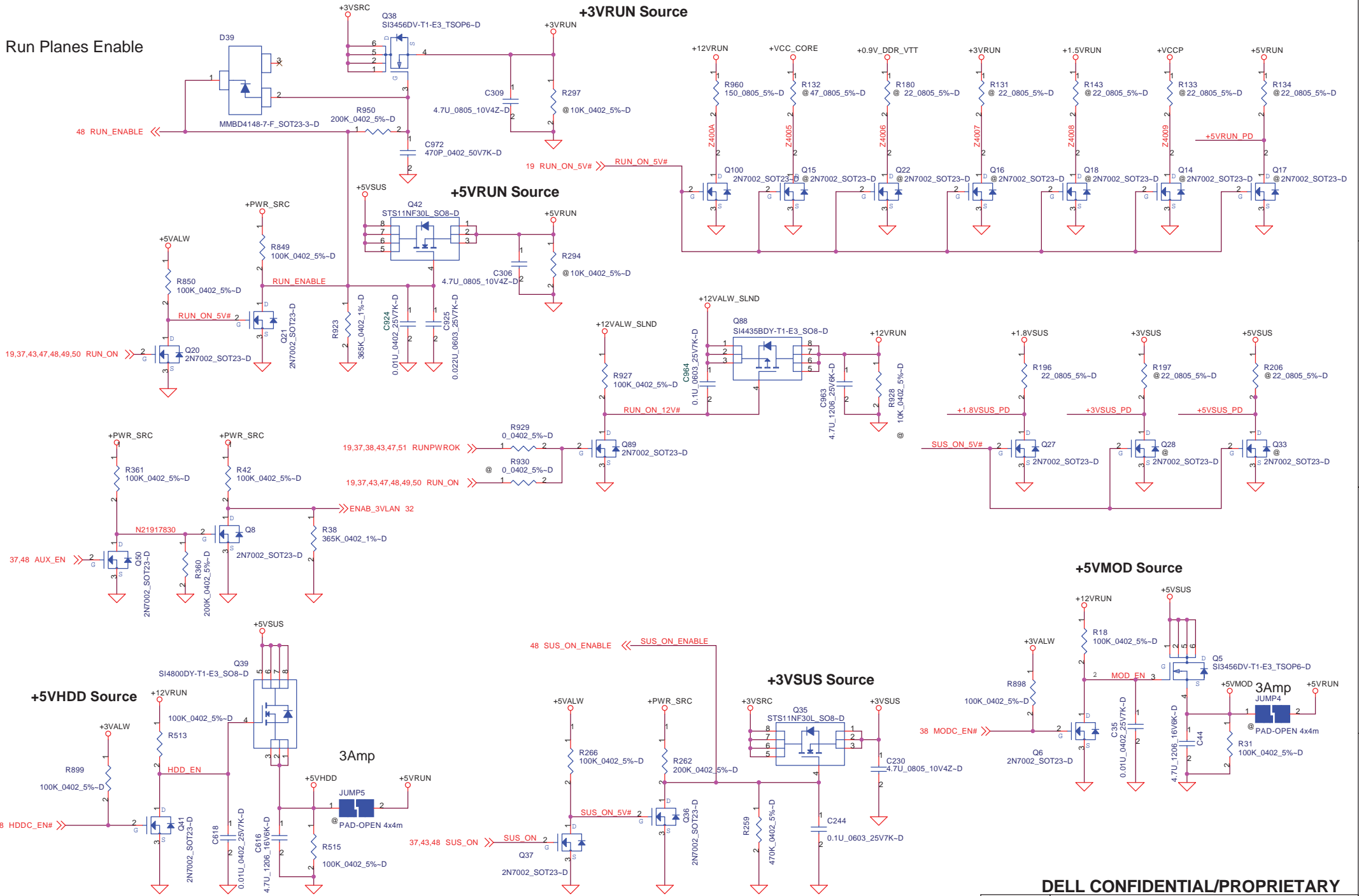


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LED & CIR & SOLENOID		
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Run Planes Enable



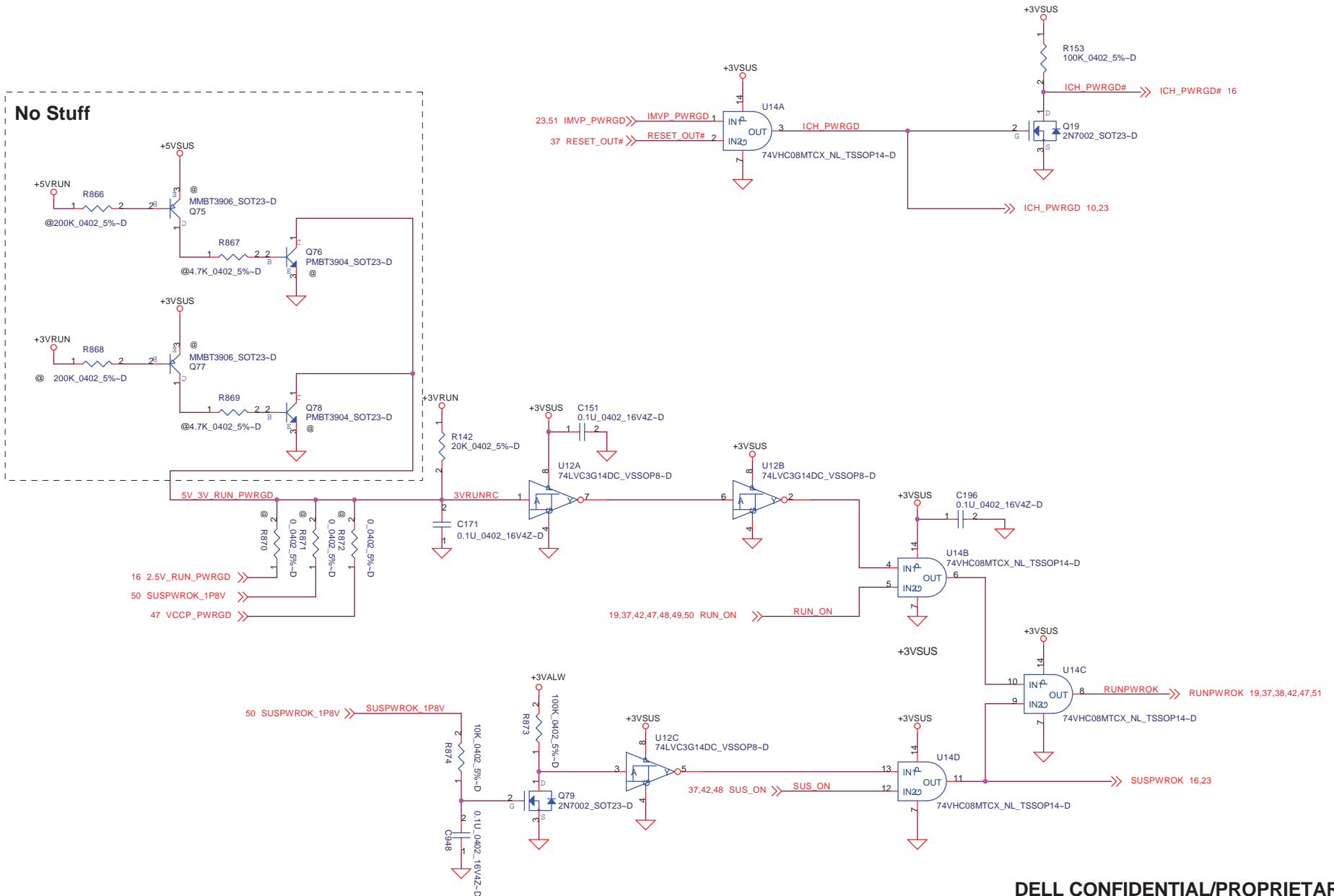
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		Power Control	
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No Stuff



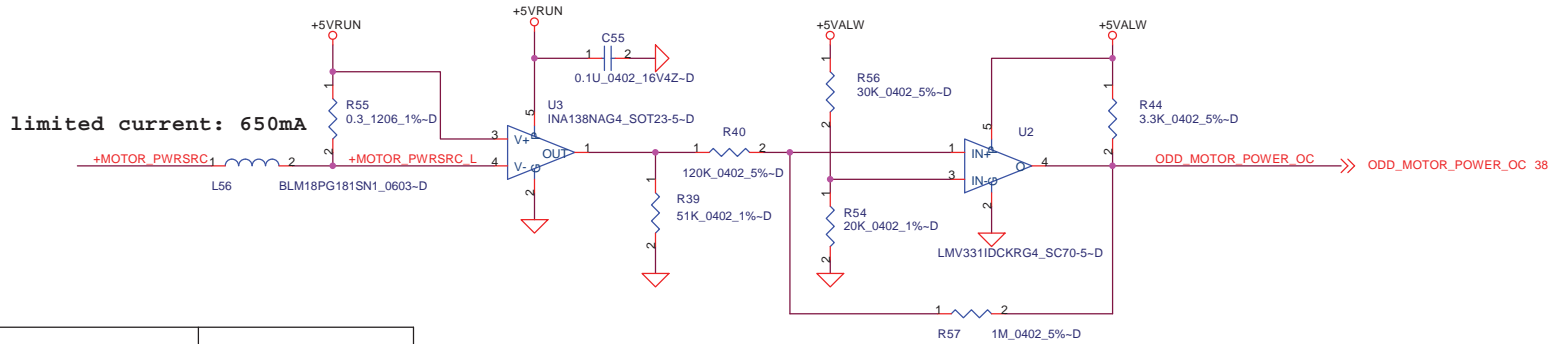
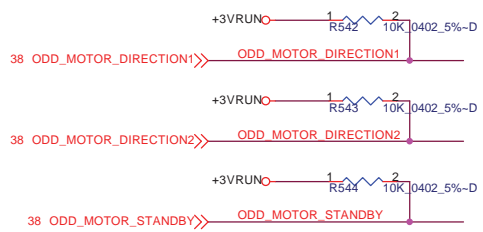
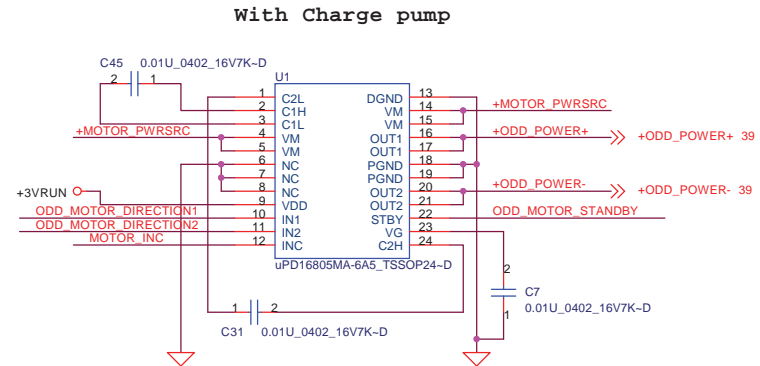
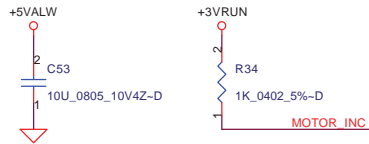
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Power sequence

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limited current: 650mA

Input Signal				Function
MOTOR_IN1	MOTOR_IN2	MOTOR_INC	MOTOR_STBY#	
H	H	H	H	Brake Mode
H	L	H	H	Forward Mode
L	H	H	H	Reverse Mode
L	L	H	H	Stop Mode
X	X	L	H	Stop Mode
X	X	X	L	Standby Mode

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Title: **CD ROM Motor**

Size: Document Number

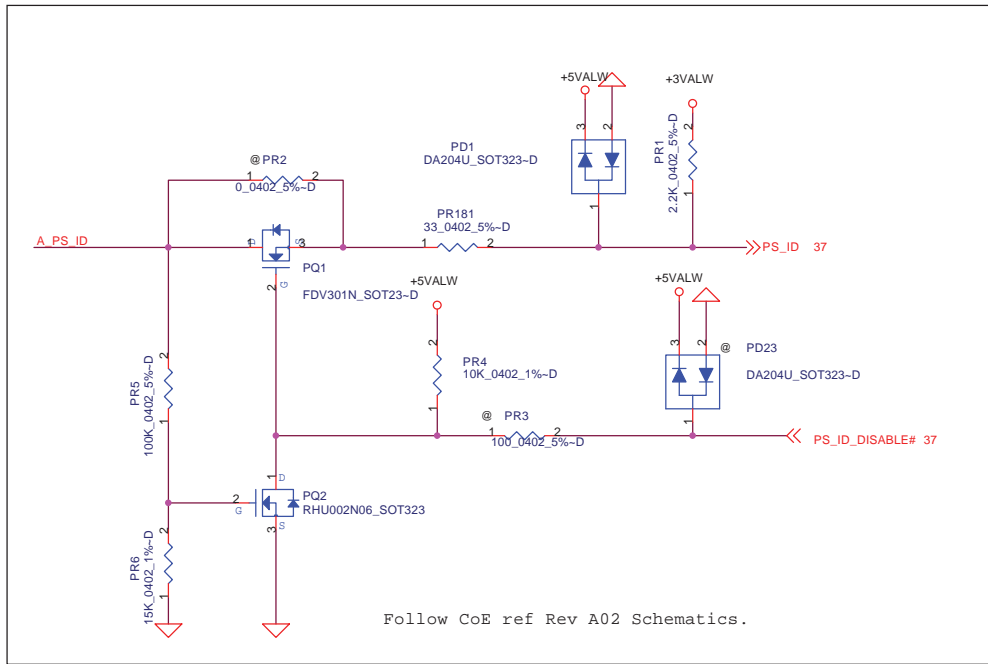
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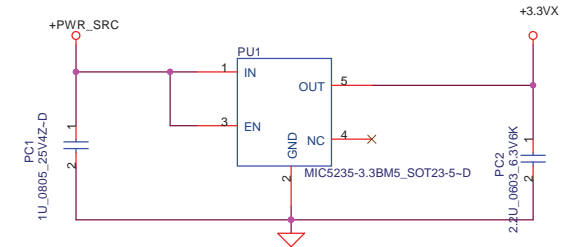
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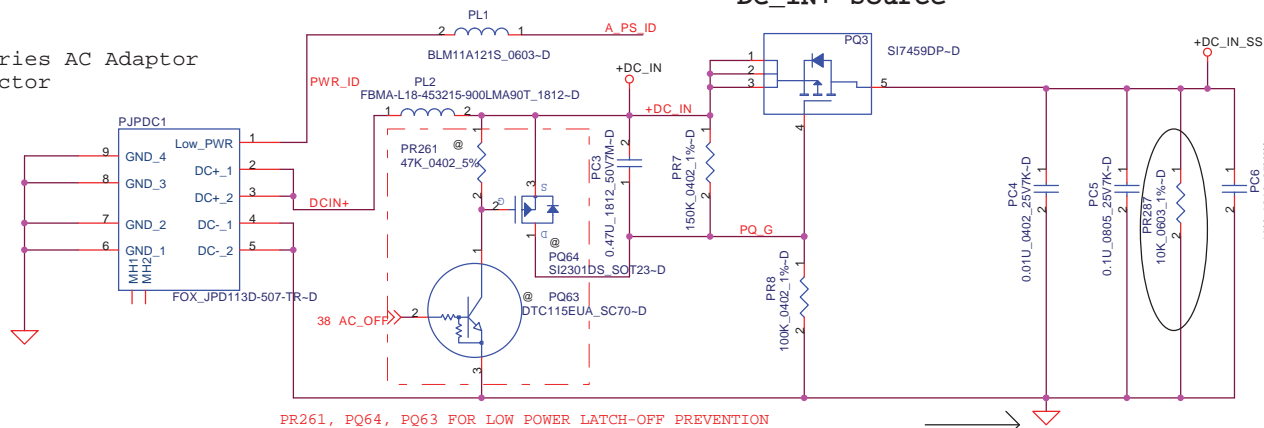


+3.3VRTC Source



DC_IN+ Source

Z-series AC Adaptor Connector



THE POINT
NOTE: *THE POINT LOCATED AT PS MODULE

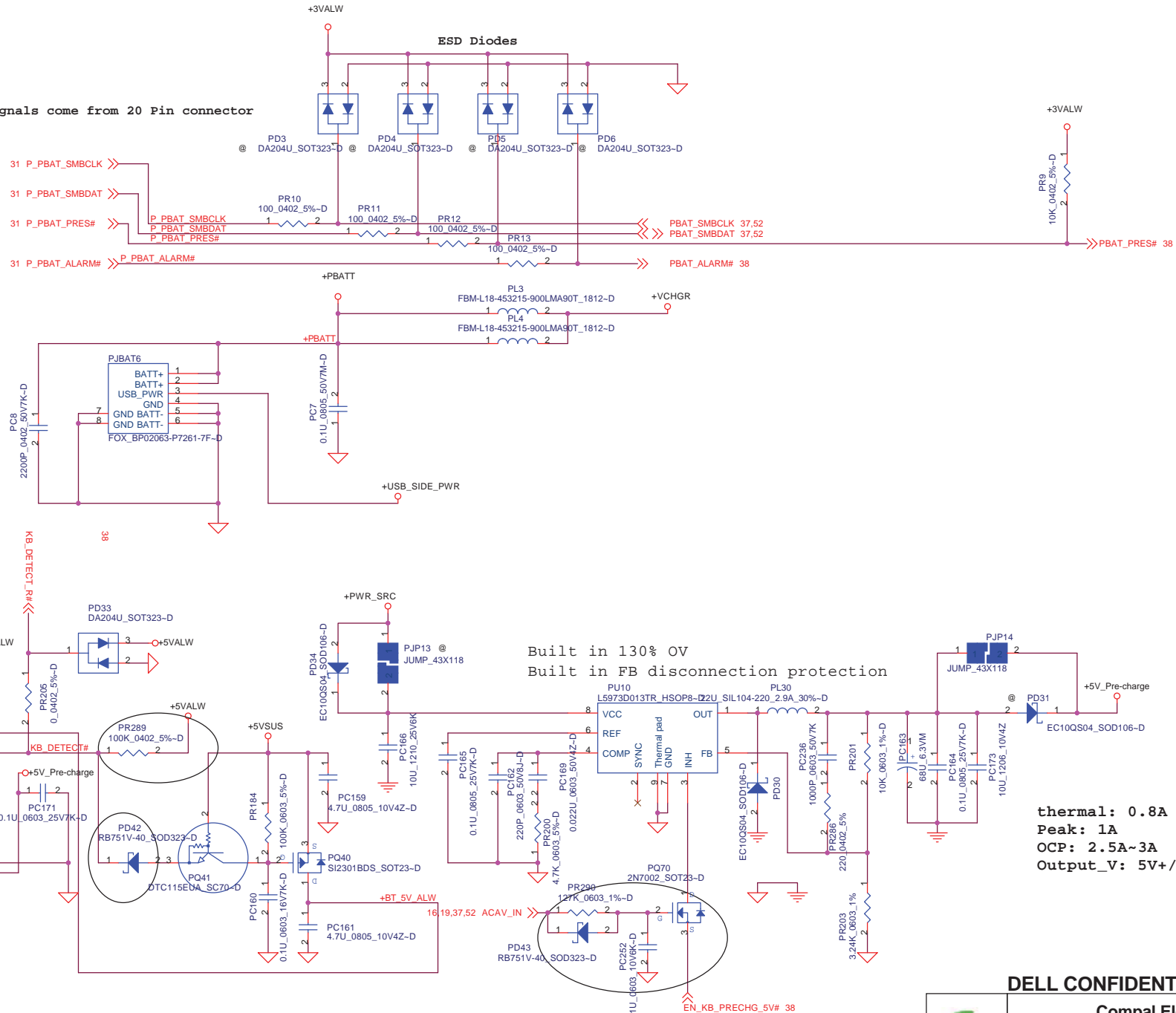
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Battery signals come from 20 Pin connector



thermal: 0.8A
 Peak: 1A
 OCP: 2.5A~3A
 Output_V: 5V+/-5%

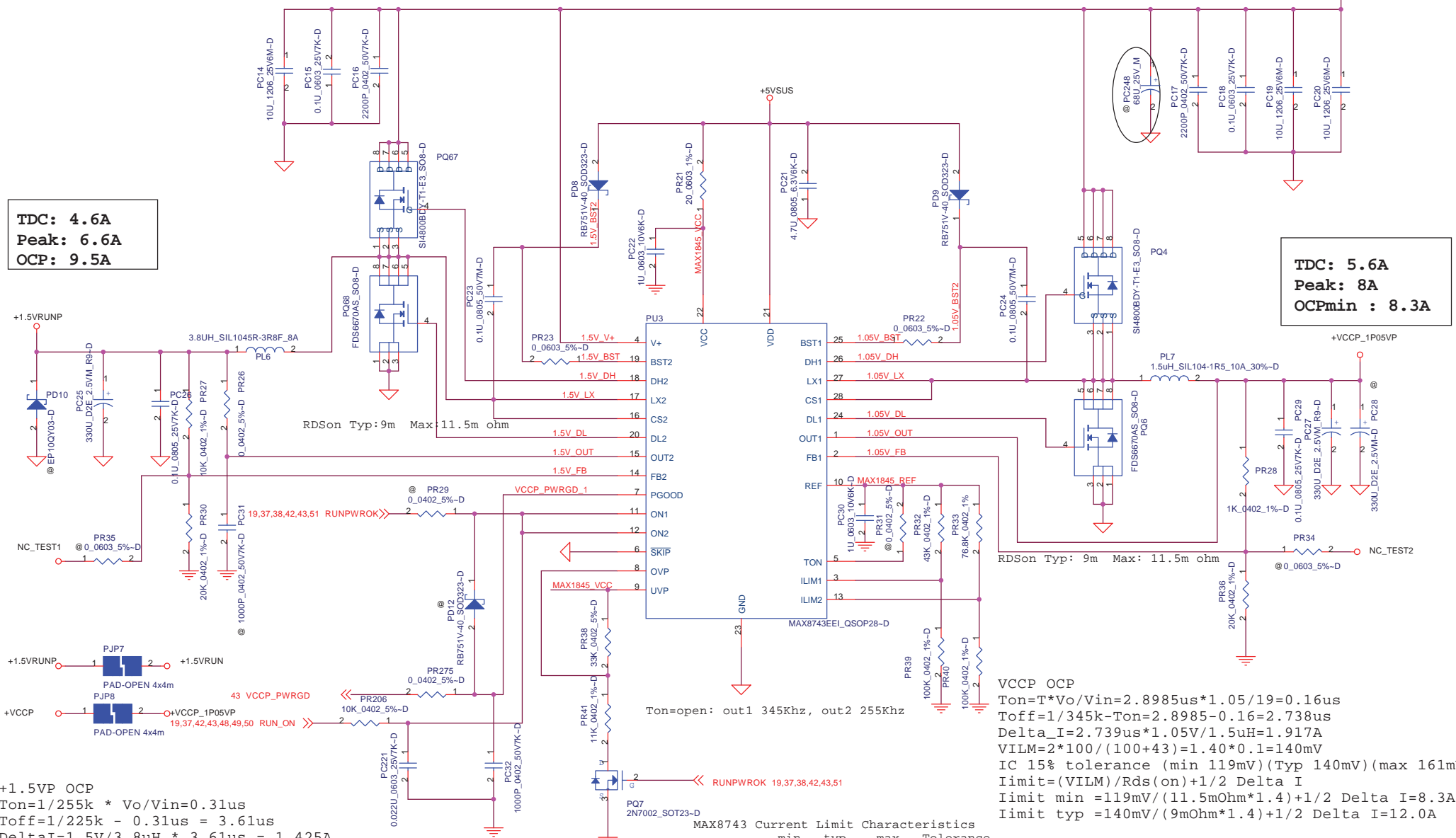
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Title Battery Conn/Kybrd_CHG		
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+1.5VRUNP / +VCCP_1P05VP



TDC: 4.6A
Peak: 6.6A
OCP: 9.5A

TDC: 5.6A
Peak: 8A
OCPmin : 8.3A

+1.5VP OCP
 $Ton = 1/255k * Vo/Vin = 0.31\mu s$
 $Toff = 1/225k - 0.31\mu s = 3.61\mu s$
 $\Delta I = 1.5V/3.8\mu H * 3.61\mu s = 1.425A$
 $I_{limit} = (VILM * 0.1) / Rds(on) + 1/2 \Delta I$
 $VILM = 2 * 100 / (100 + 76.8) = 1.13V * 0.1 = 113mV$
 IC 15% tolerance (min 96mV)(Typ 113mV)(max 130mV)
 $I_{limit} = (VILM) / Rds(on) + 1/2 \Delta I$
 $I_{limit} Min = 96mV / (11.5m\Omega * 1.4) + 1/2 \Delta I = 6.7A$
 $I_{limit} Typ = 113mV / (9m\Omega * 1.4) + 1/2 \Delta I = 9.5A$

$Ton = open: out1 345kHz, out2 255kHz$

VCCP OCP
 $Ton = T * Vo / Vin = 2.8985\mu s * 1.05 / 19 = 0.16\mu s$
 $Toff = 1/345k - Ton = 2.8985 - 0.16 = 2.738\mu s$
 $\Delta I = 2.739\mu s * 1.05V / 1.5\mu H = 1.917A$
 $VILM = 2 * 100 / (100 + 43) = 1.40 * 0.1 = 140mV$
 IC 15% tolerance (min 119mV)(Typ 140mV)(max 161mV)
 $I_{limit} = (VILM) / Rds(on) + 1/2 \Delta I$
 $I_{limit} min = 119mV / (11.5m\Omega * 1.4) + 1/2 \Delta I = 8.3A$
 $I_{limit} typ = 140mV / (9m\Omega * 1.4) + 1/2 \Delta I = 12.0A$

MAX8743 Current Limit Characteristics

	min	typ	max	Tolerance
ILIM=0.5V	40mV	50mV	60mV	20%
ILIM=1.0V	85mV	100mV	115mV	15%

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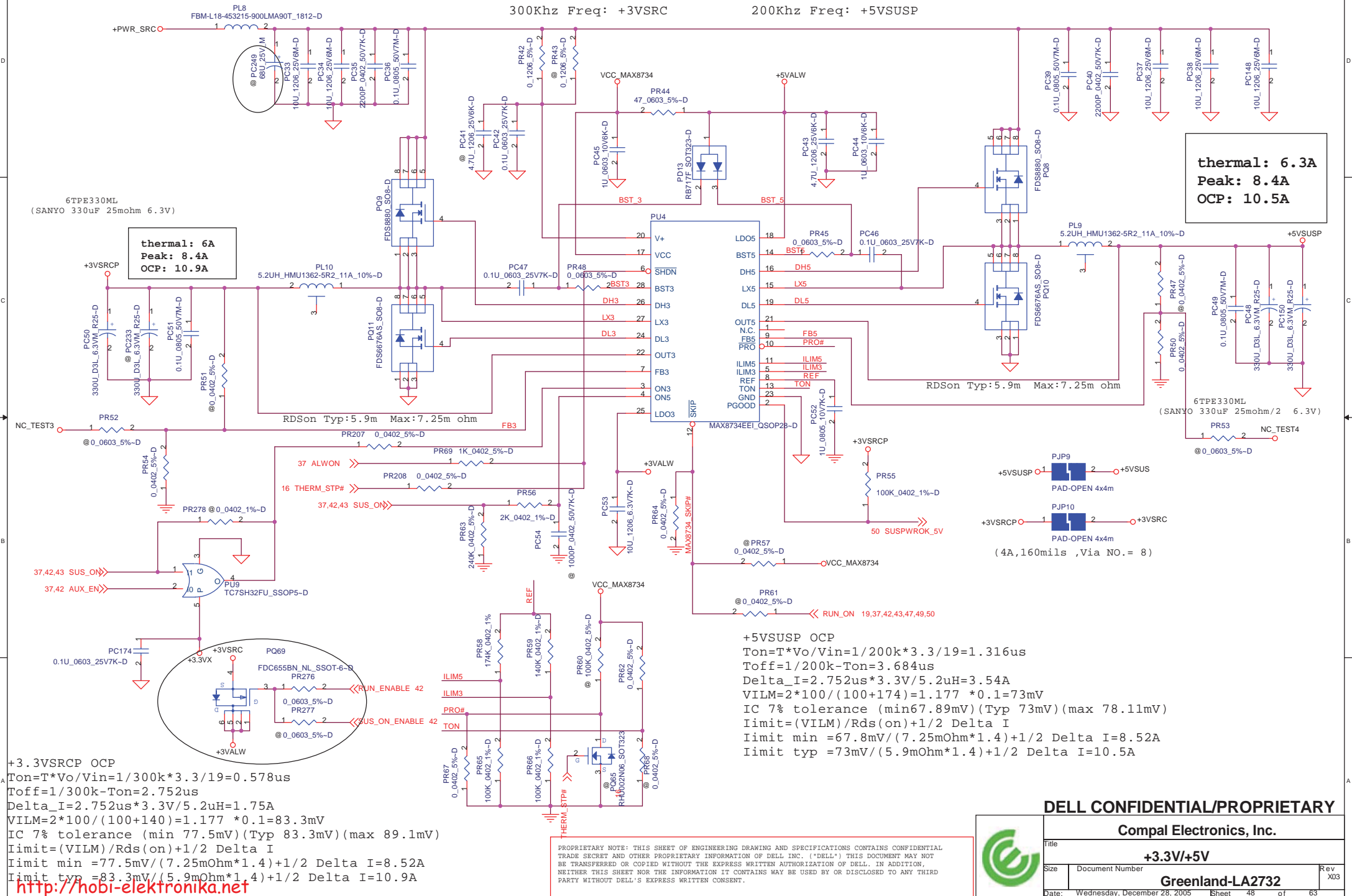
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		Compal Electronics, Inc.	
		+1.5VRUNP /+VCCP_1P05VP	
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MAX8734 Current Limit Characteristics
 min typ max Tolerance
 VLIM=0.5V 40mV 50mV 60mV 20%
 VLIM=1.0V 93mV 100m 107mV 7%

DC/DC +3V/ +5V

Follow CoE ref Rev A04 Schematics.



<http://hobi-elektronika.net>

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Title: **+3.3V/+5V**

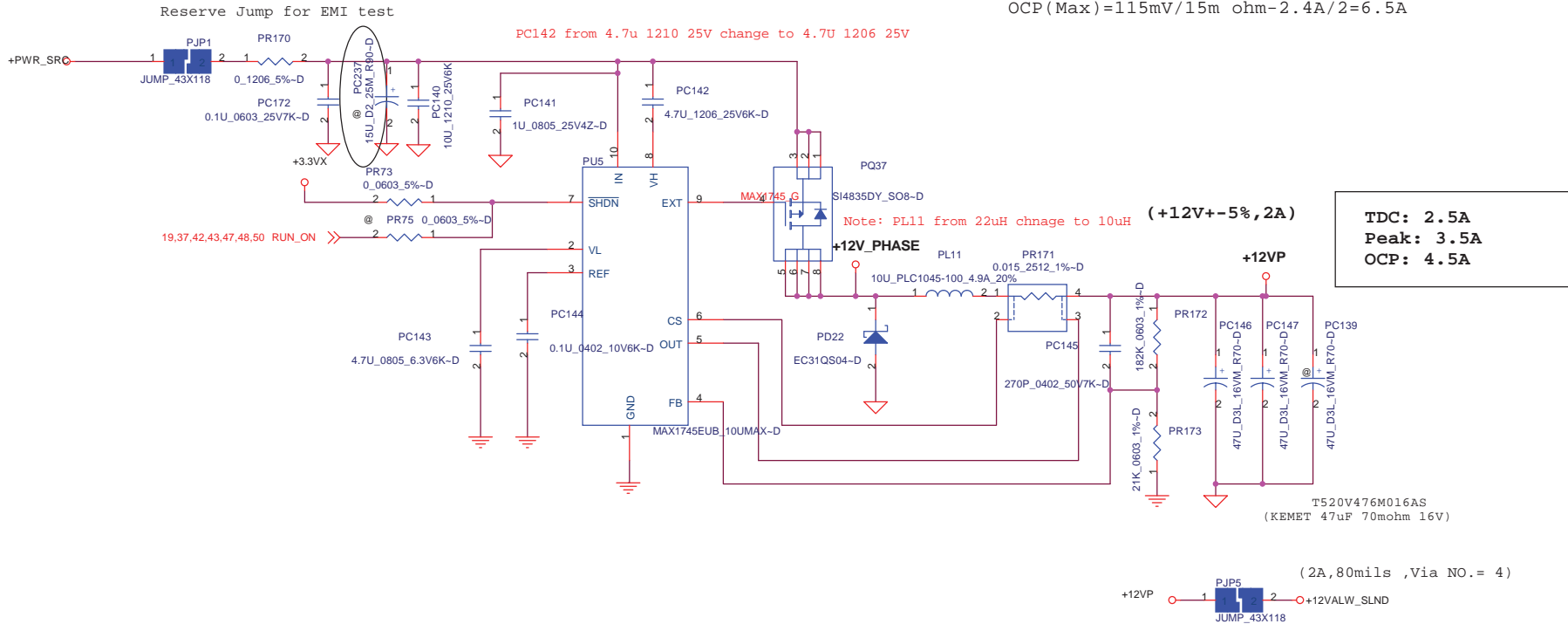
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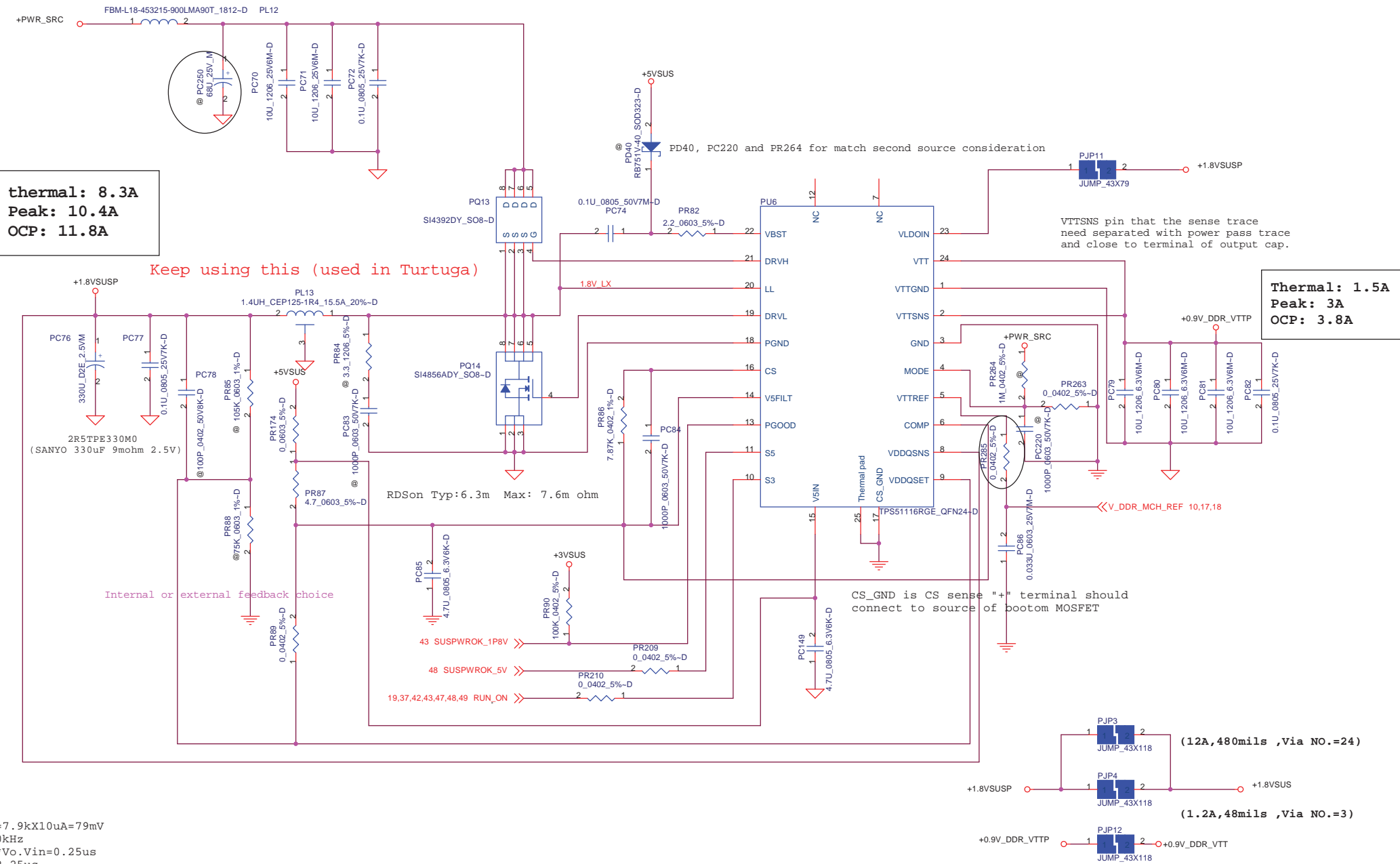
Rev X03

Greenland-LA2732

$f_z = 550k * (1-D) = 500 * (1-12/19) = 184Khz$
 $T_{off} = (1-12/19) / 184Khz = 2us$
 $\Delta I = 12V * 2us / 10uH = 2.4A$
 $OCP(min) = 85mV / 15m \text{ ohm} - 2.4A / 2 = 4.5A$
 $OCP(tyo) = 100mV / 15m \text{ ohm} - 2.4A / 2 = 5.5A$
 $OCP(Max) = 115mV / 15m \text{ ohm} - 2.4A / 2 = 6.5A$



Reserve Jump for EMI test



thermal: 8.3A
Peak: 10.4A
OCP: 11.8A

Keep using this (used in Turtuga)

Thermal: 1.5A
Peak: 3A
OCP: 3.8A

Internal or external feedback choice

RDSon Typ: 6.3m Max: 7.6m ohm

CS_GND is CS sense "+" terminal should connect to source of bottom MOSFET

VTTSNS pin that the sense trace need separated with power pass trace and close to terminal of output cap.

Vtrip=7.9kX10uA=79mV
 fs=400kHz
 Ton=T*Vo.Vin=0.25us
 Toff=2.25us
 delta I=2.25*1.8/1.4=2.9A
 IC 10% TOL: 70mV
 RDS(on)max=7.6moHm
 Iocp=Vtrip/RDS+1/2 delta I=11.8A (temperature factor has been compensated inside IC)

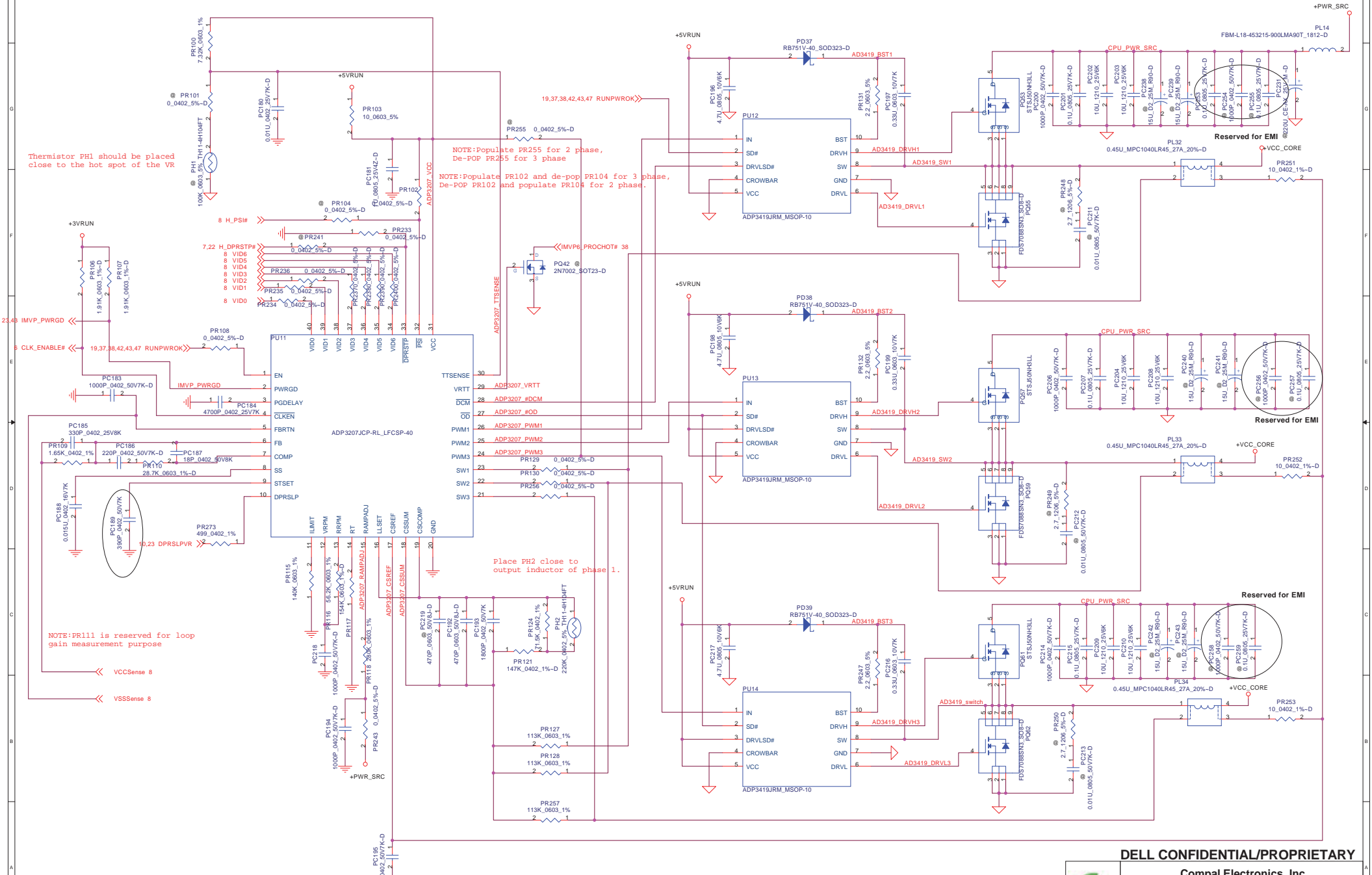
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Thermistor PH1 should be placed close to the hot spot of the VR

NOTE:Populate PR255 for 2 phase, De-POP PR255 for 3 phase
NOTE:Populate PR102 and de-pop PR104 for 3 phase, De-POP PR102 and populate PR104 for 2 phase.

Place PH2 close to output inductor of phase 1.

NOTE:PR111 is reserved for loop gain measurement purpose

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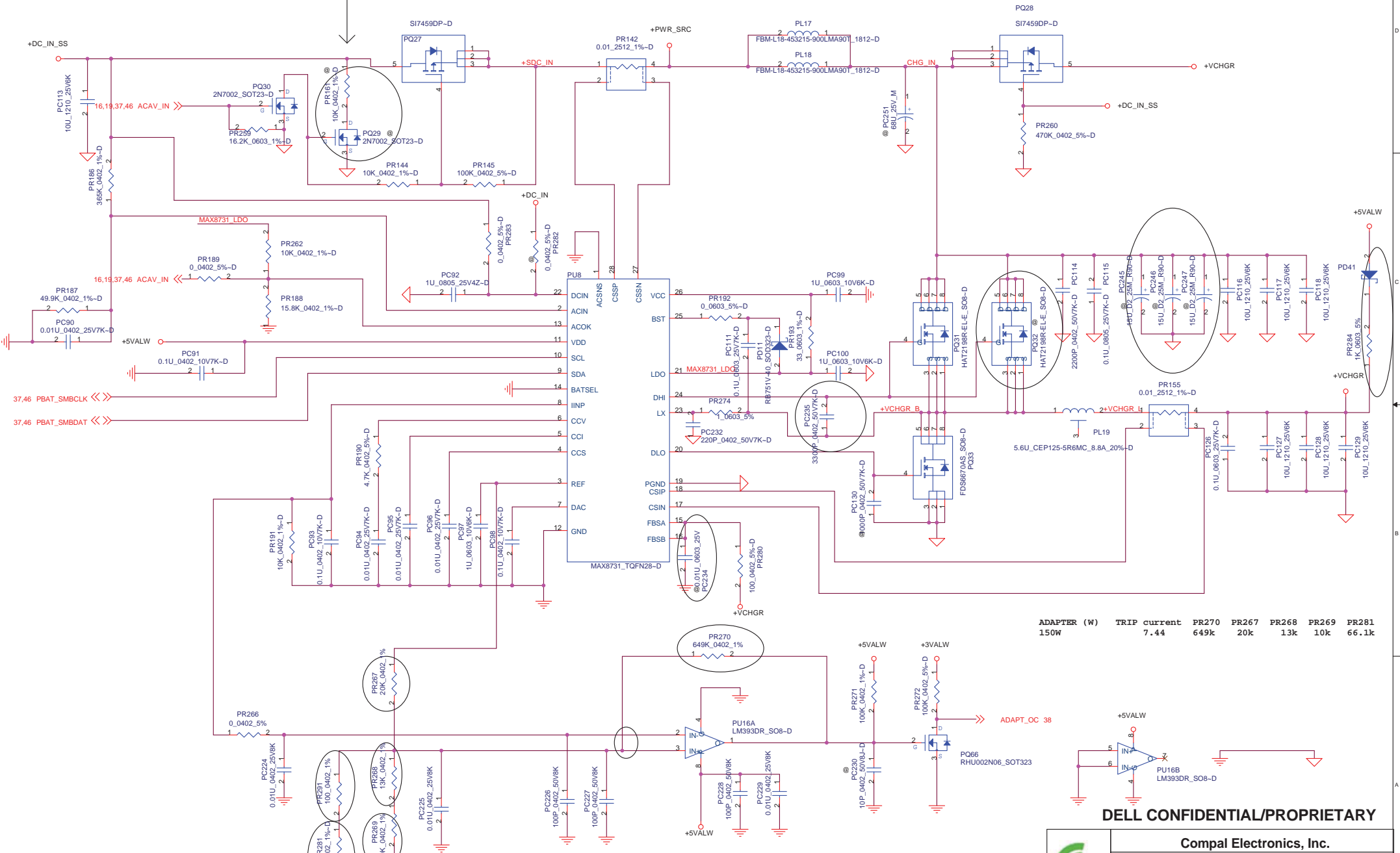
+VCCORE

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+DC_IN discharge path

Smart Charger



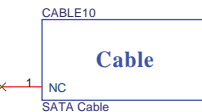
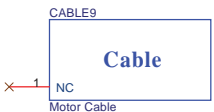
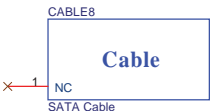
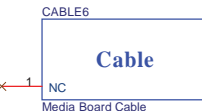
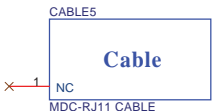
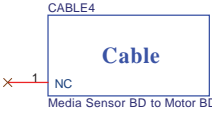
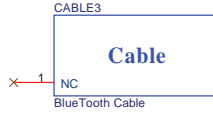
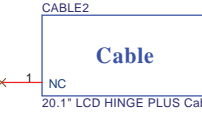
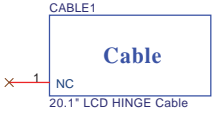
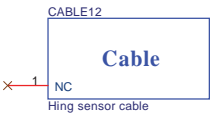
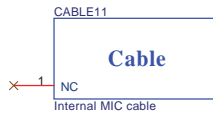
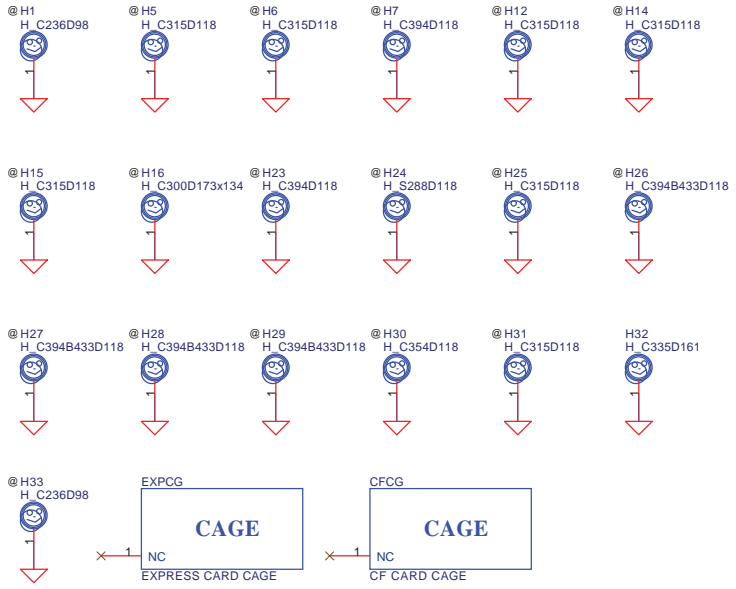
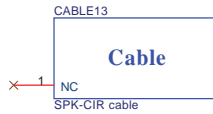
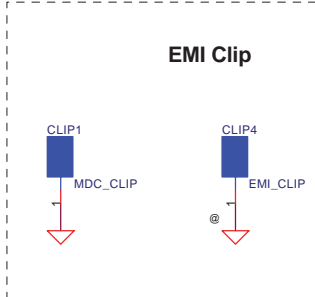
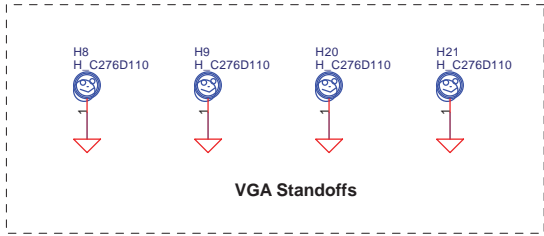
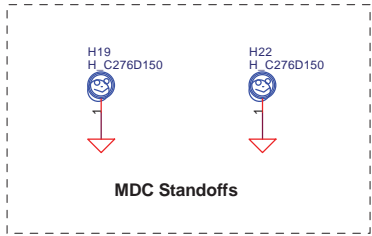
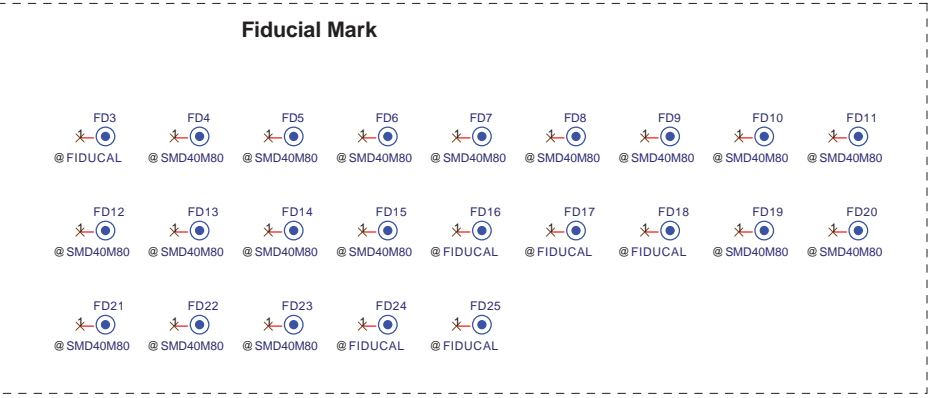
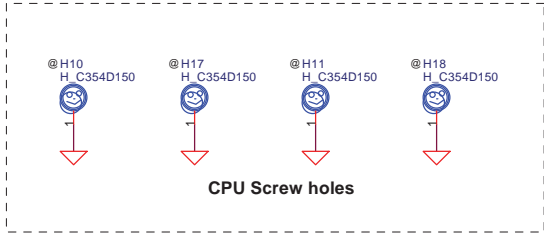
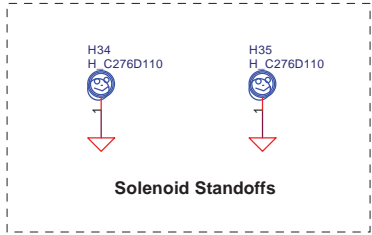
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Charger

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Version Change List (P. I. R. List) for EE Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	CoE update	2005/08/22	Dell CoE	M07-MDC-A03 CoE update: This change is due to circuit issues seen by the Travis platform regarding the varying Vgs threshold of different 2N7002 FETs.	change Q74 to BSS138 from 2n7002. The BSS138 FET has a Vgs threshold of 1.3V (typical) and 1.6V (max). This should ensure proper operation of the circuit. This change is only required by platforms using the disable circuit.	X01A
2	38	5011 Library correct	2005/08/22	Compal Willis	5011 USB port 1,3 +/- pin mistake on early version datasheet, we correct it.	U50: 5011 pin 13: USBDP1, pin 12: USBDN1 pin 19: USBDP3, pin 18: USBDN3	X01A
3	29	JWIRE Conn. Change	2005/08/23	Dell/Compal	Change JWIRE connector from 5pins include GND pin to 2 pins connetcor.	Change JWIRE connector to JST_BM02B-SRSS-TB1~D from JST_BM03(5-2.3)B-SRSSTB1LFSN-D	X01B
4	37	CoE update	2005/08/23	Dell CoE	M07-EC-Inspiron-A04 CoE update: Enable SPI ROM Boot Block are write enable on developer phase, disable it on when production.	pop R766 100Kohm, depop R767	X01B
5	10	CoE update	2005/08/23	Dell CoE	M07-945pm_gm_m07_a02 Update Delete reserved pull down resistor on M_OCDCOMP0, M_OCDCOMP1. Intel DG1.0 no require.	Delete R611, R612, Add Test point T33, T36 only	X01B
6	10	CoE update	2005/08/23	Dell CoE	M07-945pm_gm_m07_a02 Update Add 0.1uF on V_DDR_MCH_REF (total 2pcs)	Add C738 (0.1uF) but depop it now.	X01B
7	42	CoE update	2005/08/23	Dell CoE	M07-system power sequence a02 Update Add +5VRUN, +5VSUS, +3VSUS clamp ckt	1. Delete R263(100K 0402), R197 (@100K 0402), Q28 (@2N7002) 2. Change R266/1 to +5VALW from +PWR_SRC 3. Change Q27/2 to SUS_ON_5V# 4. Add Q17 (@2N7002), Q28 (@2N7002), Q33(@2N7002), R134 (@22 0805), R197 (@22 0805), R206 (@22 0805), depop them.	X01B
8	37, 41	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 33	Change net name from LID_CL# to LID_CL_SIO#. Change net name from LID_CL_R# to LID_CL#	X01C
9	6, 37	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 34	Change net name from CK_33M_SIOPCI to CLK_PCI_SIO.	X01C
10	23, 37	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 35	Change net name from ICHO_ECL_SPI_DATA to ICH_EC_SPI_DIN Change net name from ICHI_ECO_SPI_DATA to ICH_EC_SPI_DO	X01C
11	37	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 36	Change net name from FCLK to EC_FLASH_SPI_CLK Change net name from FDATAIN to EC_FLASH_SPI_DIN Change net name from FDATAOUT to EC_FLASH_SPI_DO	X01C
12	37, 42	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 37	Change net name from VAUX_EN to AUX_EN	X01C
13	38, 40	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 38	Change net name from EXPR_CPPE# to CPPE#	X01C
14	38	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 39	Change net name from IRRX to CIRRX	X01C
15	22, 26	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 68, 78, 80, 82, 84	Rename ICH_AC_SDIN0 to ICH_AZ_CODEC_SDIN0 Rename AUDIO_AC_BITCLK to ICH_AZ_CODEC_BITCLK Rename ICH_RST_AUDIO# to ICH_AZ_CODEC_RST# Rename ICH_SYNC_AUDIO to ICH_AZ_CODEC_SYNC Rename ICH_SDOUT_AUDIO to ICH_AZ_CODEC_SDOUT	X01C
16	22, 29	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 69, 79, 81, 83, 85	Rename ICH_AC_SDIN1 to ICH_AZ_MDC_SDIN1 Rename MDC_AC_BITCLK to ICH_AZ_MDC_BITCLK Rename ICH_RST_MDC# to ICH_AZ_MDC_RST# Rename ICH_SYNC_MDC to ICH_AZ_MDC_SYNC Rename ICH_SDOUT_MDC to ICH_AZ_MDC_SDOUT	X01C

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Title			EE-Changed-List History		
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Version Change List (P. I. R. List) for EE Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
17	23, 25	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 88	Rename IDE_RST_MOD to IDERST_MOD	X01C
18	6, 23	CoE update	2005/08/25	Dell CoE	Change net name same as CoE, GG issue list item 89, 90	Rename CK_14M_ICH to CLK_ICH_14M Rename CK_48M_ICH to CLK_ICH_48M	X01C
19	34, 35	GG Issue fixed	2005/08/25	Soo Lee	Modify pin number assignment for NC1 to NC7. Do match the Ricoh reference schematic. GG issue list item 96.	Update U17 R5C843 library	X01C
20	10, 12	GG Issue fixed	2005/08/25	Mohammed	Add MCH CFG10, 12 strapping pins reserved pull down resistors. GG issue list item 104	Add R622, R624, depop them.	X01C
21	20	GG Issue fixed	2005/08/25	Mohammed	change the ESD diodes (of D3, D2, D1) protection powerr rail to +3VRUN. GG Issue list item 105	Change D3, D2, D1 pull up to +3VRUN from +3VSUS.	X01C
22	7	CoE update	2005/08/25	Dell CoE	M07-Yonah A01 Update Add the 2200 PF cap to the H_THERMDA and _THERMDC pins next to he CPU pins	Add C746 2200pf on CPU side, depop it.	X01C
23	38	Board ID Change	2005/08/25	Compal Great	Change Board ID to X01 for SST	Pop R782 (10Kohm), Depop R786 (10Kohm)	X01C
24	26	GG Issue fixed	2005/08/26	Ty	A 1000pF capacitor to ground should be added to SENSE_A and SENSE_B. These should be placed close to the 9220.	Add C2, C46 (1000pf 0402), depop it now.	X01D
25	29	BT module support	2005/08/29	Compal Great	G06 BT module pin 5: BT_RE_PAIR#, and other BT module pin 5: BT_RADIO_DIS#, Standard BT module will disable when install on G06 machines.	change R323 from pull down to pull up +BT_PWR, R838 (0ohm) depop, C934 (33pf) depop. enable standard BT on developer phase.	X01E
26	31	WUSB connector	2005/08/29	Mohammed	Change WUSB connector pin define, follow Mohammed forward Cypress recommend @08/26/2005 mail.	Change JWUSB pin2 to +3VSRV from +3VSUS, pin3 to NC from +3VRUN Delete C683 (0.1uF) for +3VRUN capacitor	X01E
27	36, 37	Debug port	2005/08/30	Mohammed	Debug signals routed to WLAN mCard connector, follow Mohammed forward Kris recommend @08/30/2005 mail.	1. Connect U48.70 to JMINI2.16, and add serial resistor as 0 ohm (R914) 2. Connect U48.71 to JMINI2.17, and add serial resistor as 0 ohm (R915) 3. Connect U48.82 to JMINI2.19, and add serial resistor as 0 ohm (R913) 4. Connect U48.81 to JMINI2.42, and add serial resistor as 0 ohm (R912)	X01F
28	41	LID circuit	2005/10/07	Compal Great	Due to LID_CL# and PRE_LID_CL# always high on Solenoid board, correct LID circuit	1. change JHING pin1 connection from D34 pin2 to D34 pin1 for LID_CL 2. change JHING pin2 connection from D35 pin2 to D35 pin1 for PRE_LID_CL	X02A
29	10	CPU latency circuit	2005/10/11	Mohammed	Change the population option for the CPU latency circuit change per Intel's update. GG issue list item 5	Populate R841, Depop R610	X02B
30	20	CRT	2005/10/11	Mohammed	Add the HSYNC and VSYNC buffers to the VGA page, the Graphics card will not have it populated. Copy the same circuit on ZRS schemaitcs (X02) for U4 and U5. GG issue list item 6	Add R916-R922, U54 and U55. Depop R916 and R922, others pop	X02B
31	32	LOM	2005/10/11	Mohammed	LOM ASIC (U6) symbol name should specify 'C1' revision instead of 'C0'	Update U6 symbol name as C1	X02B
32	33	LOM	2005/10/11	Mohammed	De-pop R78, R79, R87 & D9. These are not required for BCM5753. Once LED circuit is verified on X00, these components can be removed, GG issue list item 9	De-pop R78, R79, R87 & D9.	X02B
33	42	VGS rating of FET	2005/10/11	Shiguo	RUN_ENABLE and SUS_ON_ENABLE voltage may be high up to 20.5V, so PQ69 has VGS voltage stress issue, by Dell derating, these FET signal should be 80% of VGS rating, so a resistor divider should be applied to nodes at RUN_ENABLE and SUS_ON_ENABLE.	Add R923 470K ohm, pop it.	X02B



Version Change List (P. I. R. List) for EE Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
34	37	EC flash circuit	2005/10/11	BIOS	For flash EC code easily	following ZRS, add SW1, R924 and R925	X02B
35	43	RUNPWROK circuit	2005/10/12	Mohammed	fix a back drive on the RUNPWROK circuit	1. Change Q75 and Q77 from DTA114YKA to MMBT3906, keep no stuff 2. Change R867 and R869 from 20K to 4.7K ohm, keep no stuff 3. Change R866 from 10K to 200K ohm, keep no stuff 4. Change R868 from 10K to 100K ohm, keep no stuff	X02C
36	41	CIR	2005/10/12	Mohammed	change the power rail to the CIR Wake microcontroller from +3VSR to +3VALW (Pin 15), GG issue list item14	Change JCIR pin15 from +3VSR to +3VALW	X02C
37	29	BT	2005/10/12	Mohammed	Missing 10K Pulldown on BT, COEX2_WLAN_ACTIVE signal. GG issue list item13	Add R926 10k ohm pull down on JBT pin4	X02C
38	42	+12VRUN	2005/10/13	Compal Great	Original +12VP is transferred to +12RUN, Due to Solenoid board need +12ALW_SLND power rail, so change +12VP to transfer to +12ALW_SLND, then add PMOS for +12ALW_SLND to +12RUN by RUNPWROK or RUN_ON control signal to turn on +12VRUN	Add Q88, Q89, R927~R930, C963 and C964. R928 and R930 no stuff, others pop it	X02D
39	41	Solenoid	2005/10/13	Compal Great	For Dual voltage solenoid board	JSLND pin24, 26, 28 and 30 connect to +12VALW_SLND	X02D
40	22	Crystal circuit	2005/10/13	Richard	R900 should be between Y3 pin 4 and R680 pin2, GG issue list item35	move R900 between Y3 pin 4 and R680 pin2	X02D
41	22	ICH7	2005/10/13	Richard	add a 0.1uF No Stuff cap to THRMTRIP_ICH# at R689 pin 1, GG issue list item36	Add C965 as 0.1uF no stuff	X02D
42	23	ICH7	2005/10/13	Richard	add a 10 ohm No Stuff pulldown to CLKRUN# at R707 pin 2, GG issue list item37	Add R931 as 10 ohm no stuff	X02D
43	23,31	USB OC circuit	2005/10/13	Richard	USB OC pins at U29 and U34 should be ganged, since the outputs are ganged. i.e. USB_OC4# and USB_OC5# can be ganged and named USB_OC4_5#, GG issue list item38	pin 5 and pin 8 are ganged on U29 and U34, and change net name to USB_OC4_5# and USB_OC6_7#	X02D
44	23	Solve MS Duo Adaptor circuit	2005/10/13	C. Massery	Q62 and Q63 need by pass resistor. As it is right now, circuit cannot be set to NoPop if the circuit is not needed, GG issue list item39	Add R932 and R933 as 0 ohm no stuff	X02D
45	34	48MHz	2005/10/13	C. Massery	Need AC termination for CK_48M clock input to R5C843, GG issue list item40	Add R934 and C966 no stuff	X02D
46	35	Power switch	2005/10/13	C. Massery	CardBus power switch input should be 5VRUN and not 5VSUS. Wake states are not supported so SUS plane is not needed. GG issue list item42	Change U10 pin 13 and 15 from +5VSUS to +5VRUN	X02D
47	7	ITP	2005/10/13	Mohammed	ITP termination need value changes: R577=51 Ohm, R581=39 Ohm, R582=27 Ohm per CoE input, GG issue list item44	1. Change R577 form 54.9 to 51 ohm 2. Change R581 from 39.2 to 39 ohm 3. Change R582 from 27.4 to 27 ohm	X02D
48	20	S-VEDIO	2005/10/13	Mohammed	Need to add the caps (No pop) across L9, L8, L7, 27PF caps ,nopop per CoE ref Schematics. GG issue list item46	Add C967~C969 as 27pF, no stuff	X02D
49	22	ICH7	2005/10/13	Mohammed	Need to add 0 Ohm resistor pulldown to GND on iCH_INVRMEN per CoE ref schematics, please make it no pop. GG issue list item48	Add R935 as 0 ohm, no stuff	X02D
50	37	Flash BIOS	2005/10/13	Mohammed	Need to add a switch that will short KSI5 and KSo9 to simulate the END Key Press for flash recovery. We need to place the switch on the bottom side by the memory. Need ot be exposed through the door. GG issue list item50	Add SW2	X02D



Version Change List (P. I. R. List) for EE Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
51	31	WUSB	2005/10/13	Mohammed	Follow Dell_Greenland_WUSB_Module_NoHub_SCH_V01.pdf by Mohammed's mail 2005/10/12 to modify JWUSB pin define	1. JWUSB pin4 connect to +5VSUS 2. JWUSB pin6 and pin7 change to NC 3. JWUSB pin8 connect to ECE_USBP3- 4. JWUSB pin8 connect to ECE_USBP3+	X02D
52	31,29	BT	2005/10/13	Mohammed	For the BT_RE_PAIR# signal We need to add a switch on the bottom side of the board, near the memory to short the signal to. GND. Please make sure to have a series zero Ohm resistor between the BT_RE_PAIR# signal and the GPIO on the EC. We can have the zero Ohm depoped. Also for PT2 we will have an external switch for repairing the BT module. We will need to send the signal BT_RE_PAIR# JAUDIO (maybe pin 20 has to change from GND to BT_RE_PAIR#). We need to discuss the details.	1. Add R936 as 0 ohm, no stuff 2. Add SW1 for the BT_RE_PAIR# signal	X02D
53	31	SATA LED	2005/10/13	Great	Blue LED issue	1. DEL Q44 2. Add Q92, Q93 and R938	X02D
54	39	Power BTN LED Instant On LED WLAN LED	2005/10/13	Great	Blue LED issue	1. Q81 and Q83 change from 2N3904 to 2N7002 2. R887 and R888 pin1 change from +3VALW to +5VALW 3. DEL Q73 4. Add Q90, Q91 and R937	X02D
55	35	1394 chock	2005/10/13	C. Massery	Check impedance of 1394 choke. Impedance should be 110ohm. Reference schematic recommended part is DLW21HN121SQ2	1. DEL L29 2. follow ZRS, Add L76 and L77 as DLW21SN121SQ2L	X02D
56	35	MS DUO adapter	2005/10/13	C. Massery	Follow COE to modify MS Duo Short counter measure circuit	1. DEL Q55 and Q54 2. Add Q94, Q95, D36, R939-R941 3. Change net name of J4IN1 pin 18 from XDCD# to XD_SW# 4. Change net name of J4IN1 pin 28 from MSCD#_XD1# to MS_INS#	X02D
57	20	CRT	2005/10/14	Mohammed	Follow COE, GG issue list item45	Change D5 from RB751 to RB500V-40	X02E
58	7	CPU	2005/10/14	Mohammed	Follow COE yonah_m07_a02	Change R901 from 51 to 1K ohm, no stuff	X02E
59	34	4 IN one card	2005/10/14	Mohammed	ME change 4in1 card connector to 5in1 connector	Del J4IN1, and add J5IN1	X02E
60	20	TV, CRT	2005/10/15	Mohammed	Follow COE	Change R7-9, R30, R32 and R33 from 75 to 150 ohm, pop it	X02F
61	19	VGA	2005/10/15	Mohammed	Follow ZRS	Add R942 as 0 ohm, no stuff	X02F
62	42	Power sequence	2005/10/15	Mohammed	GG issue list item21	R38, R259 and R923 change to 365K ohm	X02F
63	20	CRT	2005/10/15	Mohammed	GG issue list item65	R921 and R919 change to 365K ohm	X02F
64	37	MEC5004	2005/10/15	Mohammed	Modify by Mohammed's mail 10/15/2005, mail title is Greenland issues list updates	Add R943 as 0 ohm, pop it	X02F
65	37	MEC5004	2005/10/15	Mohammed	Modify by Mohammed's mail 10/15/2005, mail title is Greenland issues list updates	1. C872 change from 4.7u to 22uF 2. Add Q96(2N7002), Q97(2N3906), R945 and R947 as 10K, R944 and R946 as 100K, C971 as 4.7uF, D37 as RB751, pop it 3. R946 as 22 ohm, pop it	X02F



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66	39	Wireless LED	2005/11/28	Willis	LED_WLAN_OUT# signal will be NC when JMIN1 and 2 have been not installed any mini card. Then Wireless LED can not work normally.	Add Pull up resistor (R949 = 10K) to +3VRUN	X03A
67	22	SATA LED	2005/11/28	Willis	SATALED# of pin AF18 of U42 need pull up to +3VRUN. Please refer to Intel ICH7M, doc no. 17837	Change R845 from de-pop to stuff it	X03A
68	28	Audio caps	2005/11/28	Mohammed	total recommendations to move to X5R caps for improved audio performance on ALL M07 designs, follow Mohammed's mail on 11/17	1. Change C598, C207, C240, C219 and C574 form 1uF Y5V to X5R 2. Change C206 from 10uF Y5V to X7R 3. C205 and C233 from 0.1uF Y5V to X5R 4. Change C606, C604, C278 and C593 from 1U_0805_25V_6K to 1U_0603_10V_6K	X03A
69	41	CIR	2005/11/28	Willis	Due to CIR_WAKE_EN# will be pull low to 0.6V by U7 of CIR board when system in S5 state of battery mode only.This will cause ALWON active then turn on +5VALW and +3VALW.	Add Q98 to isolate U48 pin119 of M/B to U7 pin2 of CIR board in S5 state of battery mode only	X03A
70	09	CPU caps	2005/11/28	Dell	total recommendations to move to X5R caps for improved audio performance on ALL M07 designs, follow Mohammed's mail on 11/17	Change C689--C720 form 22uF X5R to X6S	X03A
71	41	BADGE LED	2005/11/28	Willis	Badge LED need +5VALW power plane	Change JCIR pin16 from +3VRUN to +5VALW, the rating current of this connector is 1A per pin.	X03A
72	29, 31, 38	BT	2005/12/01	Willis	Original connection sequence for BT_RE_PAIR#, that BT re-pair function of software and hardware can not be separated by R838.	1. Change connection sequence from U51 --> SW3 pin 1&2 and R936 pin2 --> R838 --> JBT pin5 to U51 --> R838 --> SW3 pin 1&2 and AUDIO pin20 -->JBT pin5 2. Del R936 Note. BT_RE_PAIR_R# will short to GND when use Rev. 0.3 AUDIO & USB BD	X03A
73	43	Power sequence	2005/12/01	SS	Following M07 System Power Sequence rev. A06	1. Change R868 from 100K to 200K ohm, to minimize the leakage current 2. Add R950=200K ohm and C972=470pF for delay +3VRUN, to fix IMVP_PWRGD glitch issue	X03A
74	36	Mini card	2005/12/01	B. McFarland	Following M07 Minicard rev. A07, to Add Intel WoWLAN Support Circuit	Add pop components D38, and un-pop componet R951.	X03A
75	42	HDD and ODD power	2005/12/01	R. Tony	Following M07 ICH7 rev. A07	1. Change R898 and R899 from 10K to 100K, and pop it.	X03A
76	37	EC	2005/12/01	Dell	Following M07 EC Inspiron Rev.A06	Change R946 from 22 to 0 ohm	X03A
77	37	Flash recovery circuit	2005/12/01	Willis	Simplify flash recovery circuit	1. remove R760, R763, R924 and R925 2. Add R952, R953 and R954 = 1K ohm, depop R952 and R953, pop R954	X03A
78	41	LID SW	2005/12/04	Willis	Reduce component	Remove D34 and JHING pin1 direct connect to LID_CL# signal	X03B
79	41	USB Camera	2005/12/04	Willis	USB Camera use +5VRUN power plane	Change JCIR pin16 from +3VRUN to +5VRUN, the rating current of this connector is 1A per pin.	X03B
80	41	BADGE LED	2005/12/04	Willis	Change Badge LED circuit connection from CIR BD to Solenoid BD	1. Change JCIR pin19 from BREATH_LED_BADGE signal to NC 2. Change JSLND pin25 from NC to +5VALW pin27 from NC to BREATH_LED_BADGE signal pin29 from NC to GND	X03B

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81	5, 37	SMBUS of Media BTN	2005/12/04	Compal	The Media BTN BD use +5VRUN power source, but its SMBUS has pull up to +5VALW. This will cause back drive issue in AC mode.	Change R754 and R753 pin 1 from +5VALW to +5VRUN	X03B
82	42	+3VRUN power	2005/12/04	SS	Following M07 System Power Sequence rev. A06	Add D39 between R950 pin1 and Q38 pin3	X03B
83	9	CPU Caps	2005/12/08	Shiguo	use Dell recommended cost reduction CAP combination for CPU decoupling: 4 Bulk CAPs (6mohm at 330uF)+ 32 10uF CerCAPs	1. Change C689~C720 form 22uF/X6S to 10uF/X6S 2. Change C721~C726 form 330uF/7m ohm to 330uF/6m ohm 3. Depop C721 and C725	X03B
84	23	ICH	2005/12/08	DELL	Added 0.1uF cap as a short-term solution for IMVP_PWRGD glitch issue. Follow ZRS.	Added C973	X03B
85	36	Mini card	2005/12/08	Mohammed	Follow item 15 of GGG list by Mohammed's mail on 12/08/2005	depop R807 and R806.	X03B
86	29	Subwoofer	2005/12/13	Mohammed	Greenland Filter circuit for Sub amp change by Mohammed's mail on 12/09/2005	1. Remove C320 2. Change U27 pin12 input circuit	X03B
87	31,35	USB, 1394	2005/12/13	DELL	Removing the common mode chocks for the USB ports 6,7 and 1394 port, item 3 of GG list	Remove EMI component of USB port6 & 7 and 1394 1. USB port6 & 7 --- L55, L28, R521, R520, R295 and R292 2. 1394 --- L29, R303, R305, R307 and R308	X03B
88	23,38, 42	HDD,MOD enable circuit	2005/12/14	Mohammed	This is to address a problem with the drives spinning up during a SNIFFER functionality, as well as a power glitch during a system warm boot. The ICH and SIO schematics will be updated and released tomorrow on CEC. Please refer to the attachment for the time being. follow Mohammed's mail on 12/9	1. Move HDDC_EN# to ECE5011 pin 106 2. Move MODC_EN# to ECE5011 pin 107 3. Rename ICH pin R4 to RSVD_HDDC_EN#. This pin should be No Connected. 4. Rename ICH pin E22 to RSVD_MODC_EN#. This pin should be No Connected. 5. R898 and R899 change from 100k to 10k	X03B
89	37,39	Media BTN	2005/12/14	Mohammed	Change Media BTN power source from +5VRUN to +5VSUS for remove Media BTN self test when system from S3 to S0 state	1. JMEDIA pin 18 and 19 change from +5VRUN to +5VSUS 2. R753 and R754 change pull up from +5VRUN to +5VSUS	X03B
90	41,49	Solenoid	2005/12/14	Compal	Fix +12V only have 8ms pulse width issue when use Solenoid DV BD(LS-273EP)	Add +12V_PHASE to connect JSLND pin23 and PL11 pin1	X03B
91	31	Wireless USB	2005/12/14	Mohammed	Change JWUSB from 10 pin to 8 pin, item2 of GG list	1. Change JWUSB from 10 pin to 8 pin 2. Add Q99 and R955 3. Remove C684	X03B
92	39	POWER SW	2005/12/14	Mohammed	Depop D25, because it have leakage issue	Depop D25	X03B
93	6,22, 34,38	Crystal	2005/12/14	Compal	Change Crystal circuit base on EA result	1. Change C890 form 22p to 15pF , C891 from 22p to 18pF 2. Change C809 and C810 from 12p to 1pF 3. Change R209 from 0 to 390 ohm 4. Change C530 and C531 from 12p to 18pF	X03B
94	43	Power Sequence	2005/12/14	Mohammed	Change Q79 to a 2N7002 FET per M07 design guide recommendation	Change Q79 from 2N3904 to 2N7002	X03B
95	16	FAN	2005/12/15	Mohammed	Follow M07_GUARDIANII_X05_081205, for fix noise issue	R551 and R553 change 120K, R552 change to 78.7K, and C679 change to .22uF	X03C
96	17	DDR	2005/12/15	Cody	Follow M07_Memory_X03_072105	Remove R911	X03C



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97	37	MEC5004	2005/12/15	Mohammed	Please move the PRE_LID_CL# signal from GPIO46 to GPIO45 pin 55 (currently it is RUN_ON_D). Issue with the boot block. Item 38 of GG list	Move the PRE_LID_CL# signal from GPIO46 to GPIO45 pin 55 and add R957 to cascade them	X03C
98	44	Motor	2005/12/15	Compal	Change motor current limit from 300mA to 650mA, base on motor spec	Change R55 from 0.68 ohm/2512 size to 0.4 ohm/1206 size	X03C
99	38	BID	2005/12/15	Compal	Change board ID to 0010 for PT2	Change R786 and R783 from non-pop to pop, R782 and R787 change pop to non-pop	X03C
100	39,41	All LED	2005/12/16	Compal	For fix the light of LED is too bright issue	1. Change R5, R343 and R853 from 150 to 330 ohm 2. Change R342 from 100 to 330 ohm	X03D
101	41	HDD,MOD enable circuit	2005/12/19	Mohammed	Change pull up from +3VRUN to +3VALW, item 36 of GG list	1. Change pull up of R898 and R899 pin1 from +3VRUN to +3VALW. 2. Change Q6 and Q41 from PDMC144 to 2N7002 3. Change R898 and R899 from 10K to 100K	X03E
102	39	Media BTN	2005/12/19	Mohammed	Add an option to Jumper either +5VRUN or +5VSUS rails to the Media BTN for wake from ODD buttons press.	1. Add JUMP6 and JUMP7 for power source option 2. Change pull up of R753 and R754 from +5VSUS to +5V_MEDIA	X03E
103	26-30	Audio	2005/12/19	Mohammed	Add analog ground	Add AGND symbol for connect to analog ground	X03E
104	23	SPI_CS#	2005/12/19	Mohammed	Add 47 ohm Series resistor to SPI_CS# as ICH pin P6 (close to ICH). Populate the resistor. Item 39 og GG list	Add R957 as 47 ohm on SPI_CS#	X03E
105	37	SPI_CS#	2005/12/19	Mohammed	add 0 ohm series resistor to SPI_CS# at SIO pin 4. Populate the resistor. Item 40 of GG list	Add R958 as 0 ohm on SPI_CS#	X03E
106	31	WUSB	2005/12/19	Mohammed	Change +5VRUN to +5VSUS. JWUSB pin 8 connect to +3VSRC for WUSB wake up function	1. Change JWUSB pin 7 from +5VRUN to +5VSUS 2. Change JWUSB pin 8 from Gnd to +3VSRC	X03E
107	39	Power/Instant LED	2005/12/19	Compal	remove serial resistor on MB side, since POWER BTN BD already has it.	Remove R5 and R343	X03E
108	26	Audio	2005/12/19	Compal	Add Jumper to short AGND and GND for EMI requierment	Add JUMP8-12	X03E
109	28	SPK	2005/12/19	Compal	Due to CIR BD has Speaker connector, remove ESD and Caps on MB side, add them on CIR BD	Remove D18-D21and C665-C668	X03E
110	28	SPK	2005/12/20	Compal	1. Due to CIR BD has no +12VRUN power rail to use for ESD diode, so keep ESD and EMI circuit on MB 2. Change JSPK to 2A/pin, currently is 1A/pin	1. Add D18-D21and C665-C668 2. Change JSPK from MOLEX_87438-0443_4P to MOLEX_53325-0460	X03F
111	38	ODD	2005/12/21	Compal	Please add a 100PF cap from ODD_EJECT_REC# to GND due of a glitch on the signal found during EA. Item 41 of GG list	Add C974	X03F
112	38,22	Crystal	2005/12/21	Compal	Change Crystal circuit base on EA result	1. Change Y2 from 24MHz/20pf to 24MHz/12pf 2. Change Y3 from 32.768kHz/12.5pf to 32.768kHz/6pf	X03F
113	42	Power sequence	2005/12/21	Compal	+1.8VSUS and +12VRUN discharge too slowly issue base on EA result	1. Pop R196 and Q27, follow ZRS 2. Add R960 and Q100 for +12VRUN discharge	X03F
114	37	MEC5004	2005/12/23	Compal	Depop SMSC work around proposed on EMC5004 revision D chip	1. Depop R944~R948, C971, Q96, Q97 and D37 2. Change C872 from 22uF to 4.7uF	X03G
115	20	Headphone/MIC	2005/12/23	Compal	Separate audio ground from power ground on AUDIO&USB board (LS-2736P) for fix headphone noise in battery mode only	Change net name of JAUDIO pin14 from GND to AGND	X03G
116	All	Subsystem ID	2005/12/29	DELL	Add subsystem ID	Add subsystem ID	X03G



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1	P45 P46 P47 P48 P49 P50 P51 P52	+DCIN Battery Conn/KB_CHG +1.5VSUSP /+VCCP_1P05VP +3.3V/ +5V 12V +1.8VSUSP/ +0.9V_DDR +VCORE Charger_new	0715/2005	Dell	Power source rename.	Power source rename to +PWR_SRC from PWR_SRC.	X00
2	P51	+VCORE	0727/2005	Dell	Reserve AL- Caps on CPU PWR_SRC for buzzing noise.	Add PC231 220U_25V	X00
3	P51	+VCORE	0729/2005	Dell	Dell request to add 499ohm 1% series resistor at the CPU VR ADP3207.	Add PR273 499_0402_1%	X00
4	P51	+VCORE	0729/2005	Dell	The Original High side MOSFETs are error.	The manufacture PN of PQ53,PQ57,PQ61 change to FDS6294 from FDS6982.	X00
5	P51	+VCORE	0802/2005	Compal	For support three or two phases options.	Rename PU11 PIN 24 from ADP3207_VCC change to ADP3207_PWM3.	X00
6	P48	+3.3V/5V	0826/2005	Dell	Increased +3.3VSRV rating current	1. PQ9 change to FDS8880 2. PR59 change to 66.5K. 3. PL10 change to 5.2uH_HMU1362_5R2_11A	X01
7	P47	+1.5VRUN	0826/2005	Dell	Increased +1.5VRUN rating current	1. PQ68 change to FDS6670A 2. PL6 change to 3.8uH_SIL1045R-3R8F8A 3. PR33 change to 76.8K 4. PC25 change to 330uF@9m ohm_2.5V 5. PR40 change to 100K	X01
8	P47	+1.05V	0826/2005	Dell	Reduced +1.05V rating current	1. PQ6 change to FDS6670A 2. PL7 change to SIL104-1R5PF 3. PR32 change to 80.6K 4. PC27 change to 330uF@9mohm_2.5V 5. De-pop PC28 6. PQ4 change to SI4800	X01
9	P48	+3.3V/5V	0826/2005	Dell	Redesign 5VSRS OCP setting	1. PR58 change to 158K 2. Net name rename to AUX_EN from VAUX_EN	X01
10	P48	+3.3V/5V	0831/2005	Dell	Redesign 3.3VSUS OCP setting	1. PQ11 change to PD6676AS 2. PR59 change to 140k 3. Add PC233 a 330uF_6.3V_25mohm CAP paralleled at PC50	
12	P48	+3.3V/5V	0831/2005	Dell	Redesign 5VSUS OCP setting	PR58 change to 174K	
13	P46	Battery Conn/KB_CHG	0929/2005	Compal	Support JKBDK Pin 2 current rating 1A	JKBDK Pin 7 change to +5V_Pre-charge from GND for support current rating 1A	
14	P48	+3.3V/5V	1004/2005	Dell	Improve +3VALW droop issue	Add an an external FET PQ69.	
15	P48	+3.3V/5V	1007/2005	Compal	Reserve optional path of PQ69 Pin gate which connect to SUS_ON ENABLE.	Add PR276 and Nopop PR277	
16	P51	+VCORE	1011/2005	Dell	Redesign load line adjustment.	Change PR127 PR128 PR257 from 93.1K ohm to 113K ohm.	
17	P51	+VCORE	1011/2005	Dell	Redesign input noise filter.	Move PC231 from PL14's pin 2 end to pin 1 end.	
18	P48	+3.3V/5V	1011/2005	Dell	Delate a filter	Unpopulate PR43 and PC41.	
19	P48	+3.3V/5V	1011/2005	Dell	Redesign for Pin_Pro# should be kept at Low voltage to enable OVP/UVF and discharge function.	Unpop PR60.	

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20	P48	+3.3V/5V	1011/2005	Dell	Follow CoE schematics.	Reserve a path and unpop PR278 0 ohm resistor between PU9 pin4 and SUS_ON.	X02
21	P51	+VCORE	1011/2005	Dell	Follow Napa Platform.	Unpop PR241 and pop PR233.	X02
22	P51	+VCORE	1011/2005	Dell	Delete unuseful function.	Unpop PQ42 PR101 PH1.	X02
23	P47 P48 P49 P50 P51	+1.5VSUSP /+VCCP_1P05VP +3.3V/ +5V 12V +1.8VSUSP/ +0.9V_DDR +VCORE	1011/2005	Dell	Follow CoE grounded form.	Follow CoE grounded symbol.	X02
24	P47	+1.05V	1011/2005	Dell	Redesign OCP setting.	Change PR32 from 80.6K to 43K.	X02
25	P47 P48 P50	+1.5VSUSP /+VCCP_1P05VP +3.3/ +5V +1.8VSUSP/ +0.9_DDR	1011/2005	Dell	Redesign EMI filter rating current.	Change PL5 PL8 to rating current 9A. Change jump BJP2 to PL12(rating current 9A).	X02
26	P51	+VCORE	1013/2005	Dell	Redesign L/S Vgs miller CAP voltage.	Change PR131 PR132 PR247 to 2.2 ohm.	X02
27	P51	+VCORE	1013/2005	Dell	Remove un-needed device.	Del PD41	X02
28	P52	Charger	1013/2005	Dell	Remove un-needed device.	Del PR146 PR147 PR160 PR242.	X02
29	P52	Charger	1013/2005	Dell	Follow CoE ref schematics.	Add PR279 100 ohm ,PC234 0.01U, PC235 0.01U.	X02
30	P52	Charger	1013/2005	Dell	Rename net name.	Change PQ28 gate connect to +DC_IN_SS.	X02
31	P52	Charger	1013/2005	Dell	Follow CoE ref Schematics.	Add PU16 PQ66 PC224 PC225 PC226 PC227 PC228 PC229 PR266 PR267 PR268 PR269 PR281 PR271 PR272.	X02
32	P52	Charger	1015/2005	Dell	Follow CoE ref Rev A06 Schematics. * PT build MEMO need add item 32.*	1. Add PR283 0 ohm ,between +DC_IN_SS with PU8 DCIN_Pin. 2. Del PC235, PR279. 3. Pop PR280 100 ohm 0402 4. Short PU8 FBASA_Pin with PBSB_Pin 5. Change DC_IN net name to +DC_IN 6. Add PR280 0 ohm ,btween +VCHGR with PU8 Pin 15.	X02
33	P52	Charger	1121/2005	Dell	Follow CoE ref Rev A09 Schematics.	1. Move and unpop PC234 to connect with PU8 FBASA and FBSB pins. 2. Add PC235 between PQ31 gate and switching node. 3. Change PR268 from 11.8K to 13K ohm. 4. Change PR269 from 12.1K to 10K ohm. 5. Change PR281 from 154K to 66.5K ohm. 6. Change PR270 from unpopulated to populated. 7. Correct PR270 pin 1 connect with PU16 pin3.	X03
34	P45 P46 P47 P48 P50 P51 P52	+DCIN Battery Conn/KB_CHG +1.5VSUSP /+VCCP_1P05VP +3.3V/ +5V +1.8VSUSP/ +0.9V_DDR +VCORE Charger_new	1121/2005	Compal	Take the daul layout to enter second source of bead.	Change PL2, PL3, PL4, PL5, PL8, PL12, PL14, PL17, PL18 PCB Footpoint from L_1812 to L_1812-S.	X03
35	P45, P46 P49, P51 P52	MITSUBISHI Cap 10u 25V X7R EOL	1129/2005	Compal	MITSUBISHI Cap 10u 25V X7R EOL	Change PC113, PC116, PC117, PC118, PC127, PC128, PC129, PC140, PC166, PC202, PC203, PC204, PC208, PC209, PC210, PC6 to SAMSUNG 10u 25V M X5R 1210 H2.5	X03

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36	P52	Charger	1201/2005	Dell	Follow CoE ref Rev A10 Schematics.	Add PD41, PR284	X03
37	P46	+5V_Pre-charge	1206/2005	Dell	to improve control loop stability	Add PC236, PR286. Corrected PC169 to 0.022uf	X03
38	P50	+1.8V	1206/2005	Dell	Add a PR285 0ohm resistor between the pin 5 and the outpu for 2nd SC480 application	Add PR285	X03
39	P49 P51 P52	+12V Vcore Charger	1207/2005	Dell	Proposed solutions to accoustic noise issues: add dual pads for all input caps (ceramics and POSCAPS) on PWR_SRC.	Add Vcore POSCAP on input (Unpop) :PC238, PC239, PC240, PC241, PC242, PC243. Add Charger POSCAP on input (Unpop): PC245, PC246, PC247 Add +12VP POSCAP on input (Unpop) : PC237	X03
40	P51	Vcore	1207/2005	Dell	to improve Vcore VR slew rate	PC189 from 680pf to 390pf	X03
41	P46	+5V_Pre-charge	1207/2005	Compal	to improve +5V+Pre-charger leakage when battery only.	Add PQ70 2N7002.	X03
42	P45	+DCIN	1215/2005	Dell	Dell require	Add PR287 10K_0603 at P03 pin5 to GND	X03
43	P46	+5V_Pre-charge	1215/2005	Dell	Improve +5V_Pre-charge	1.Add PR288 100K , PR289 100K, PR290 127K. 2.Add PD42 PD43 3.Add PQ70 4.Add PC252	X03
44	P52	Charger	1219/2005	Dell	Dell require	1.Change PR281 from 66.5K to 68K 2.Add PR291 100 ohm	X03
45	P51	Vcore	1227/2005	Dell	Dell EMI require.	Add PC253 and reserve PC254 PC255 PC256 PC257 PC258 PC259 .	X03

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Power-Changed-List History
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