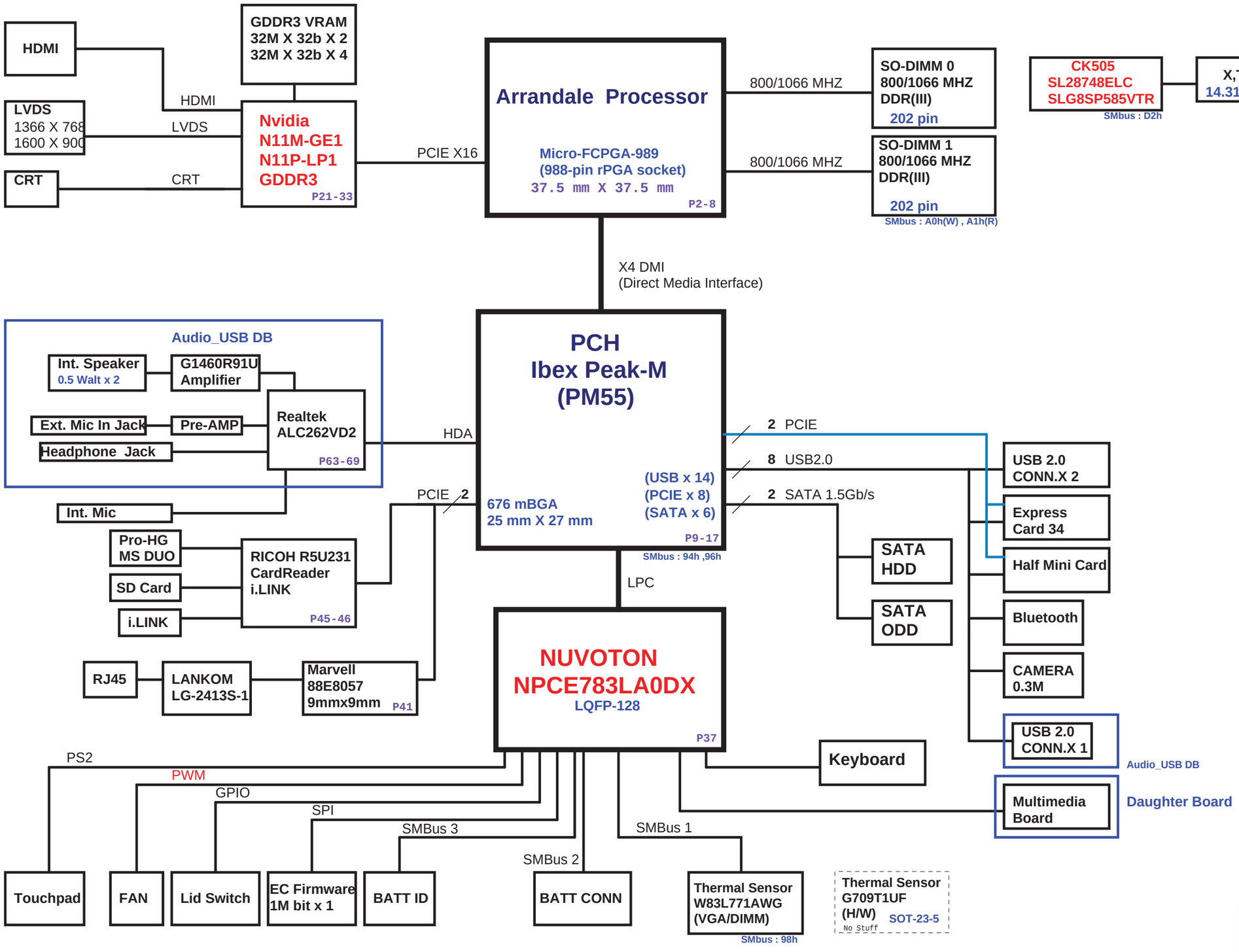
M-9A0 (Calpella + N11P/M Discrete Graphic)



TI CHARGER BQ24753 P.54	
	OUTPUTS
DC_IN	BT+ DCBATOUT

SYSTEM DC/DC MAX17020ETJ+ P.55	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +12V

SYSTEM DC/DC SC412 P.56	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN

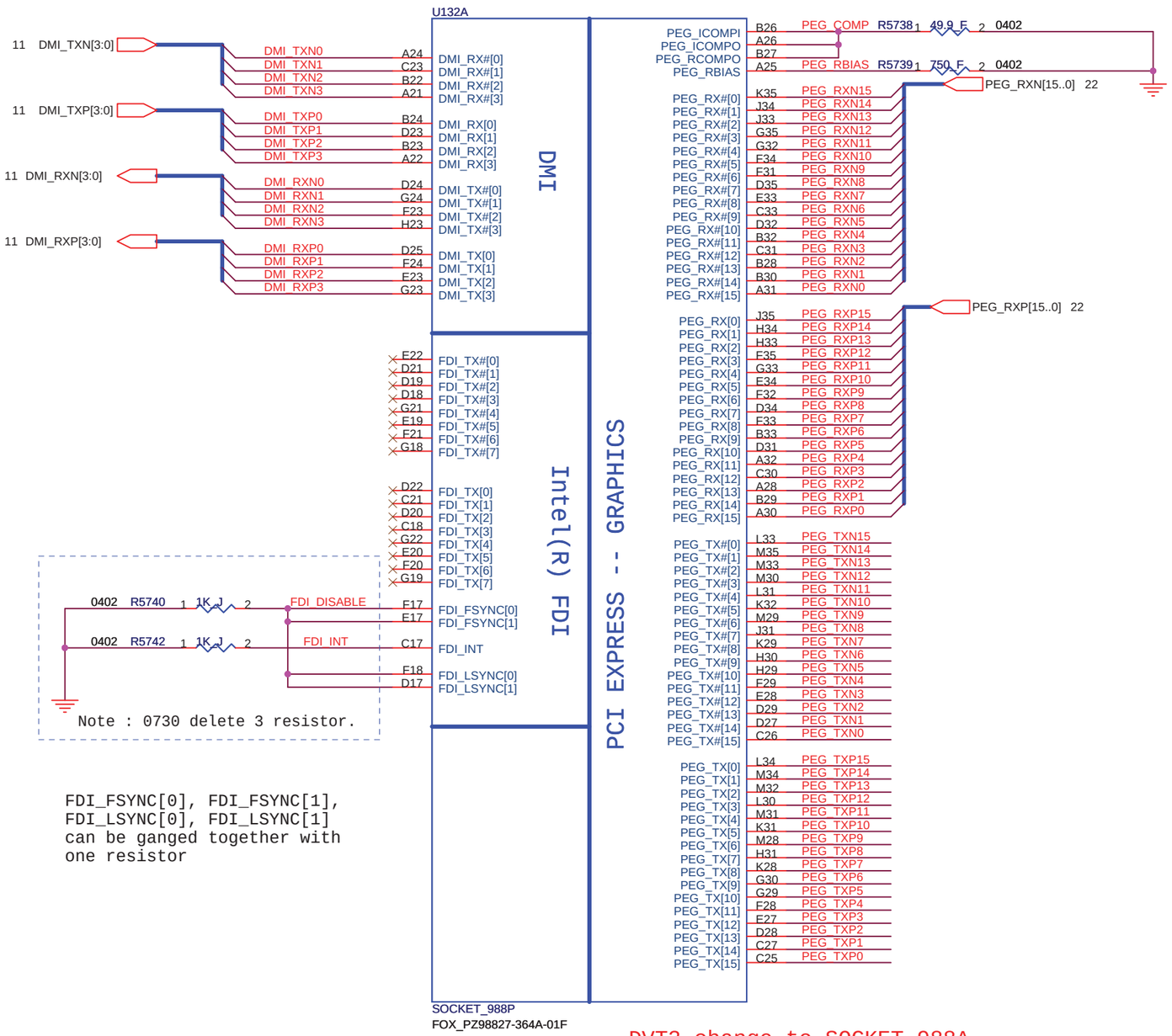
SYSTEM DC/DC SC412+G2998 P.57	
INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS
+1_8VSUS	+0_9VRUN

CPU DC/DC ISL6266A P.58	
INPUTS	OUTPUTS
DCBATOUT	VHCORE

SYSTEM DC/DC SC411+APL5913 P.61	
INPUTS	OUTPUTS
DCBATOUT	NV_VDD
+1_5VRUN	PEX_VDD

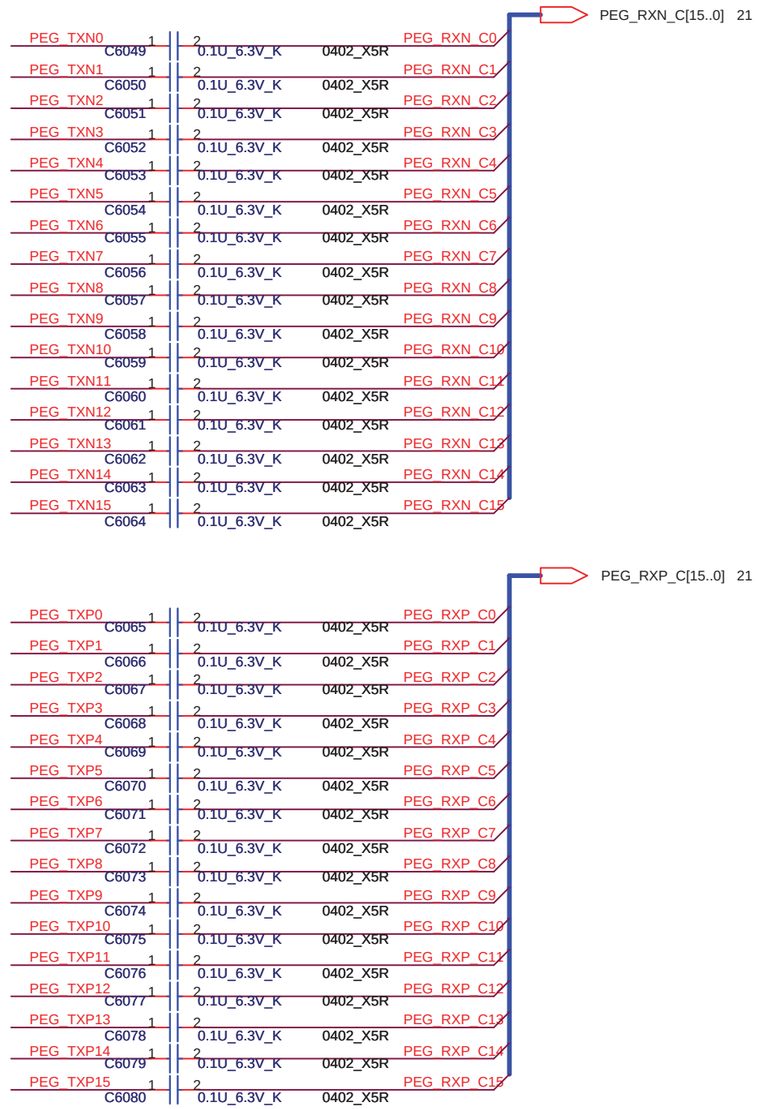
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Block Diagram	
Size Custom	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 1 of 73	



FDI_FSYNC[0], FDI_FSYNC[1],
FDI_LSYNC[0], FDI_LSYNC[1]
can be ganged together with
one resistor

DVT2 change to SOCKET_988A



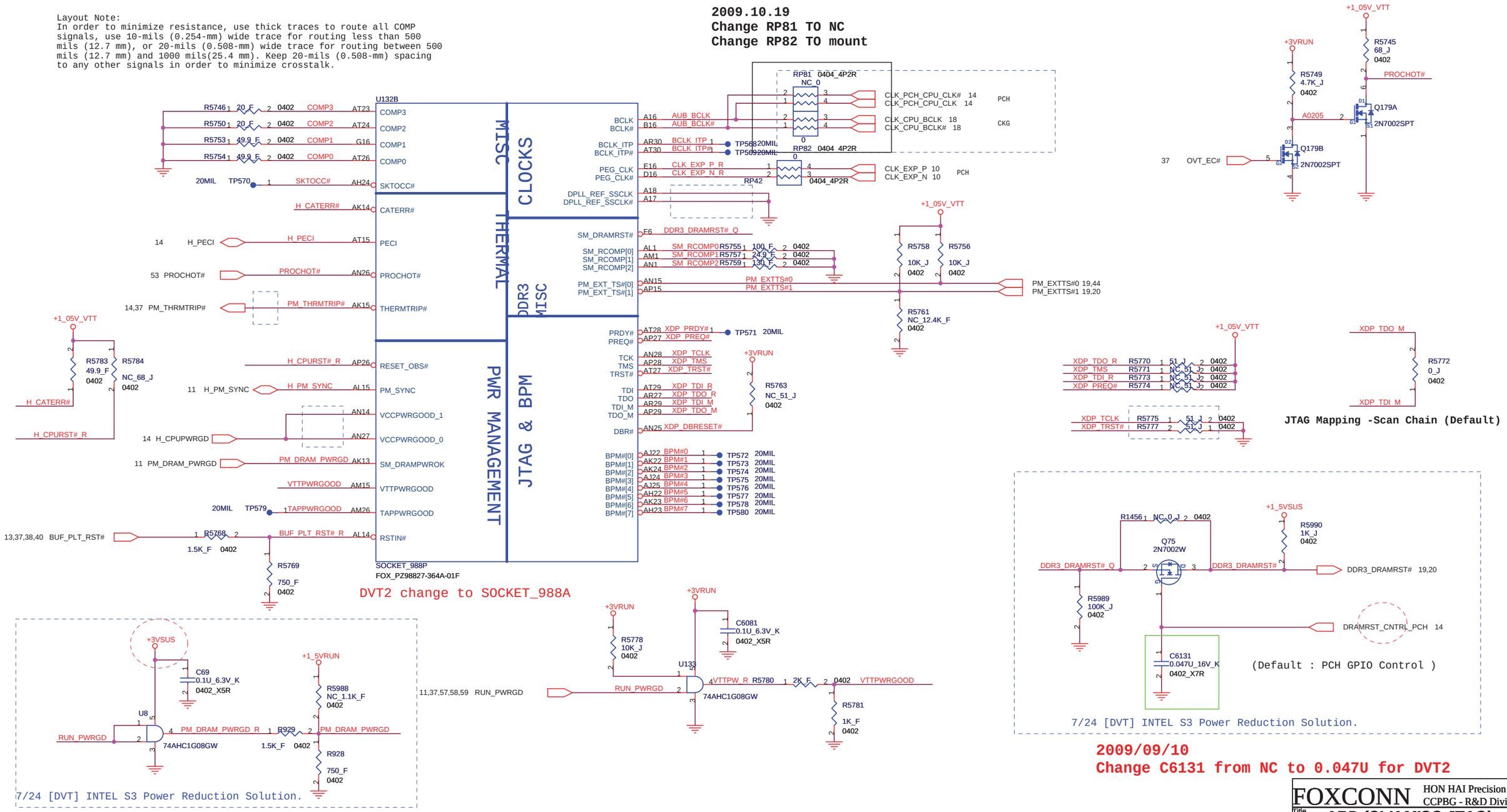
For Disable Arrandale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (DMI,PEG,FDI)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, November 19, 2009	Sheet 2 of 73	

For Disable Arrandale Graphic
DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on
Arrandale directly if motherboard only supports discrete graphics.

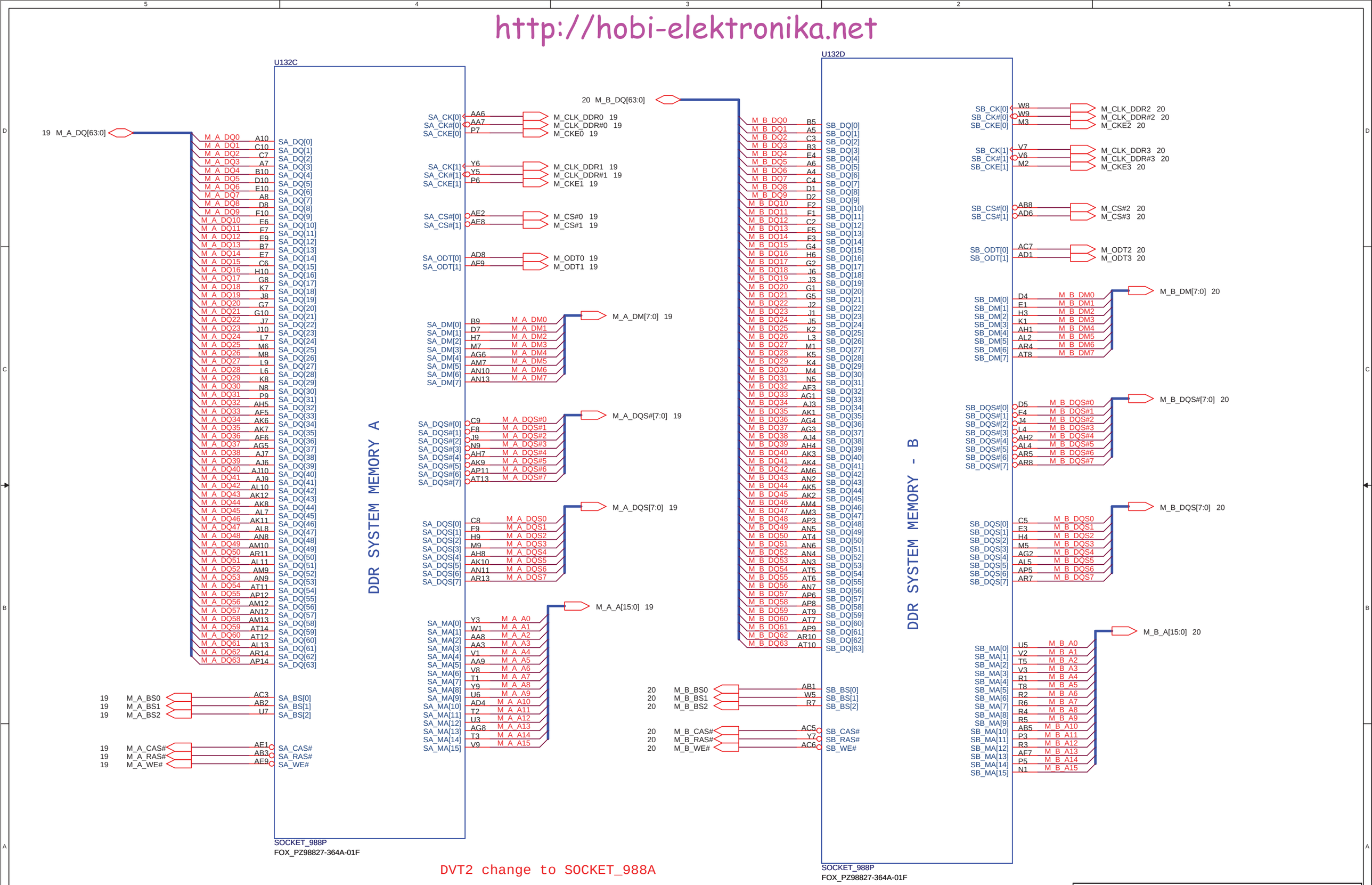
Layout Note:
In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils (0.254-mm) wide trace for routing less than 500 mils (12.7 mm), or 20-mils (0.508-mm) wide trace for routing between 500 mils (12.7 mm) and 1000 mils(25.4 mm). Keep 20-mils (0.508-mm) spacing to any other signals in order to minimize crosstalk.

2009.10.19
Change RP81 TO NC
Change RP82 TO mount



2009/09/10
Change C6131 from NC to 0.047U for DVT2

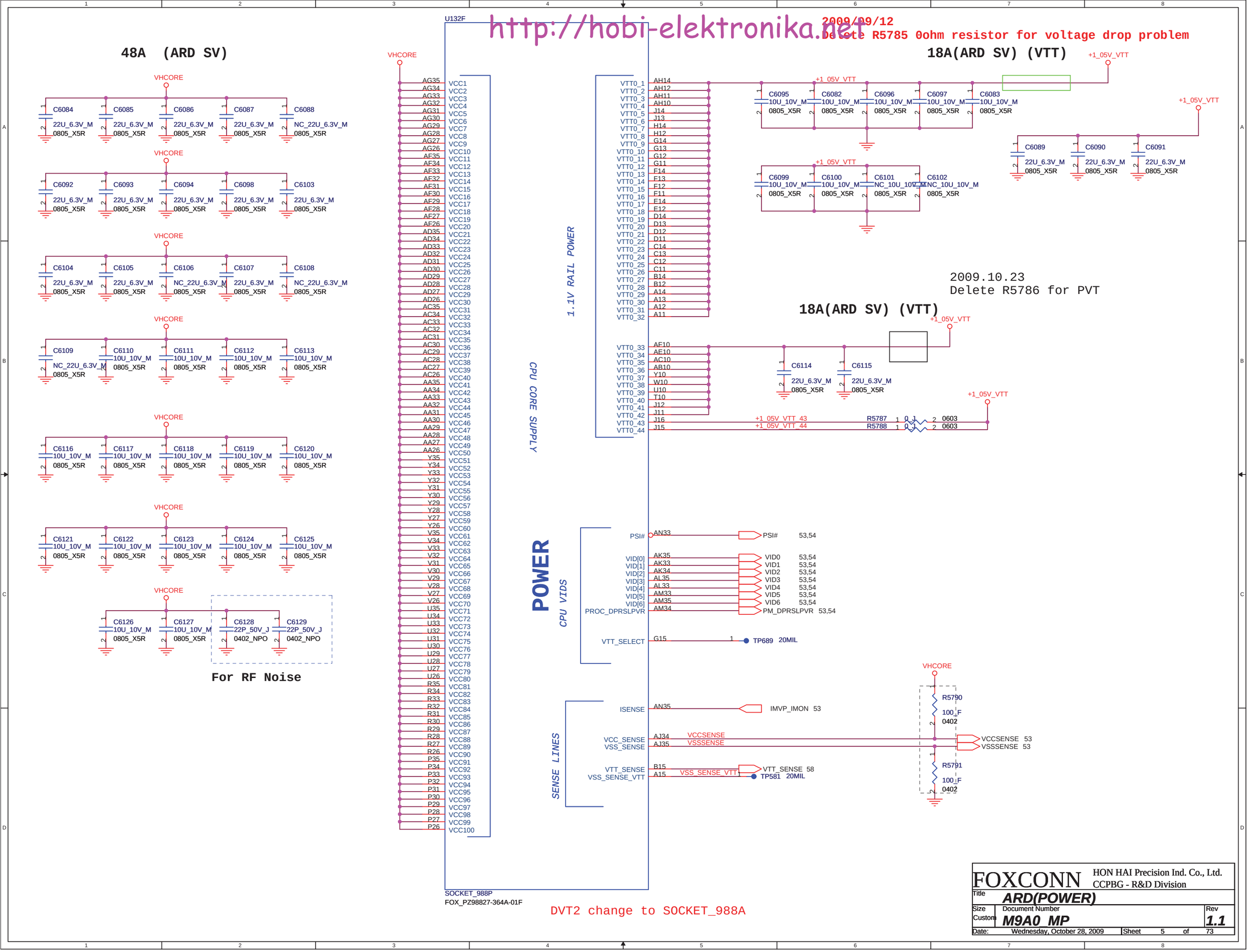
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	ARD (CLK,MISC,JTAG)		
Size Custom	Document Number M9A0_MP		Rev 1.1
Date: Thursday, November 19, 2009	Sheet 3 of 73		



DVT2 change to SOCKET_988A

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (DDR3)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, November 19, 2009	Sheet 4 of 73	

2009/09/12
Delete R5785 0ohm resistor for voltage drop problem

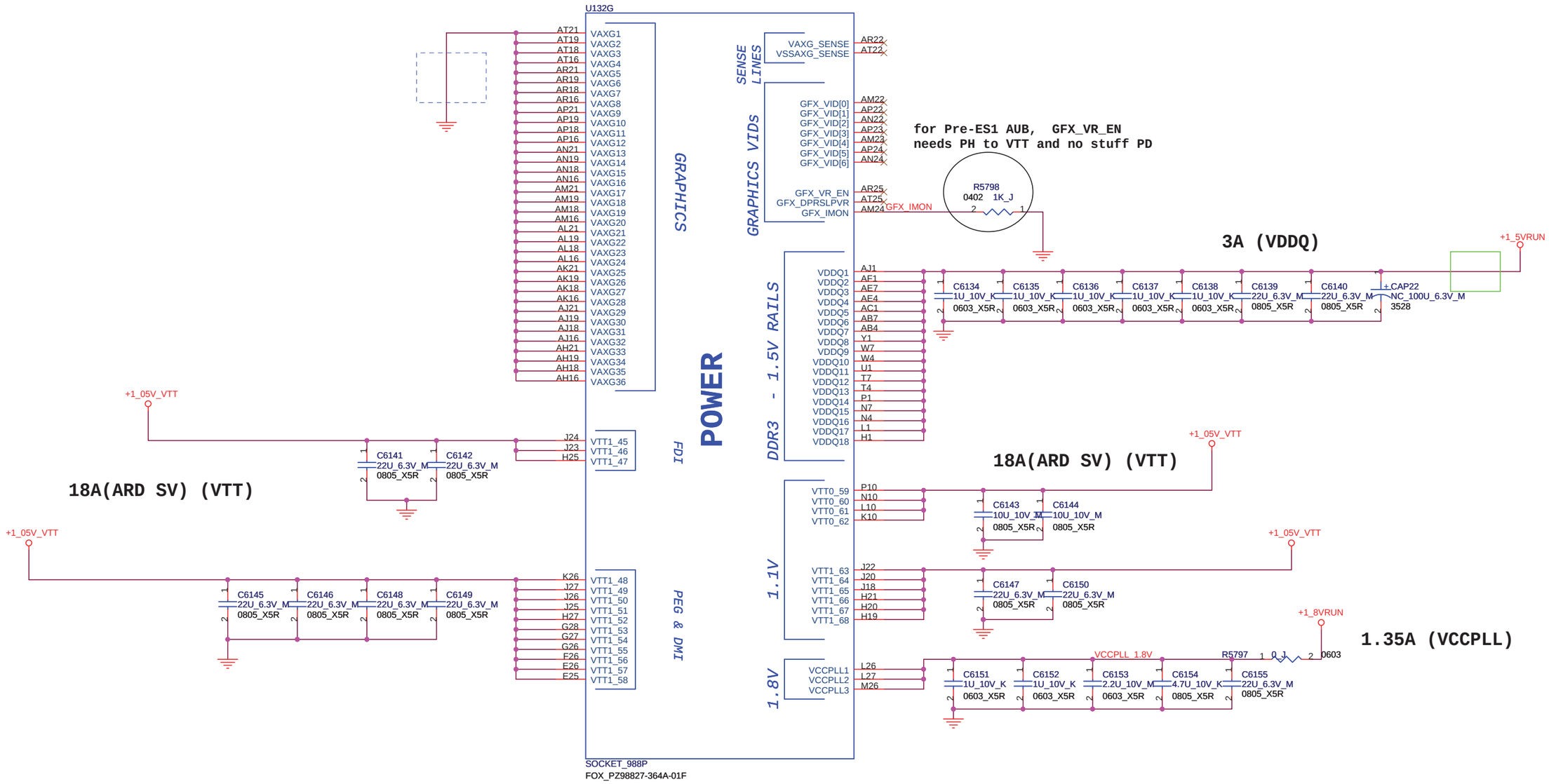


DVT2 change to SOCKET_988A

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD(POWER)	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Wednesday, October 28, 2009	Sheet 5 of 73	

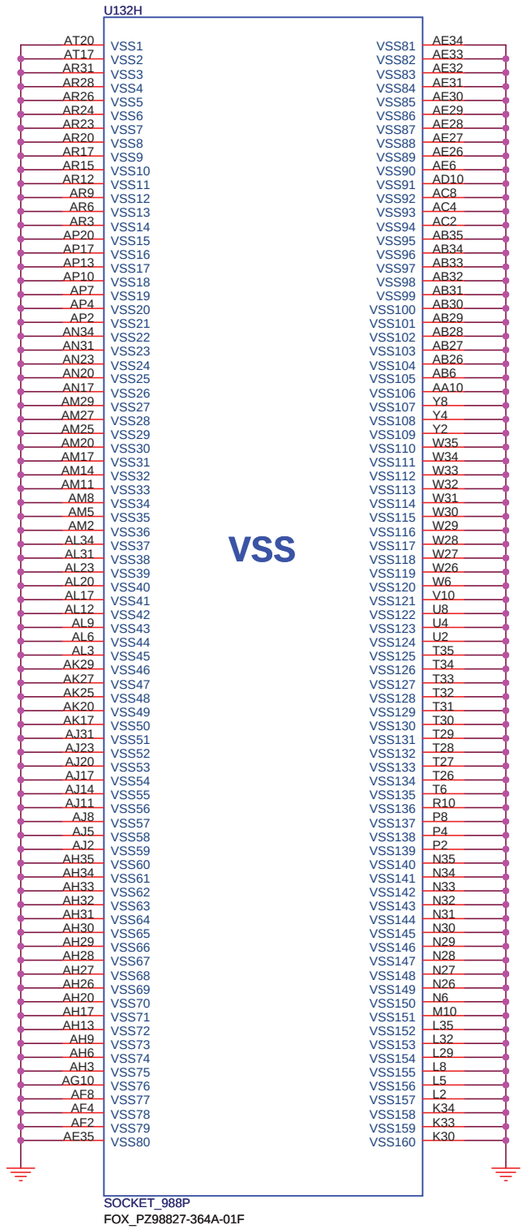
For Disable Arrandale Graphic
VAXG should be connected to GND when disable iGPU.

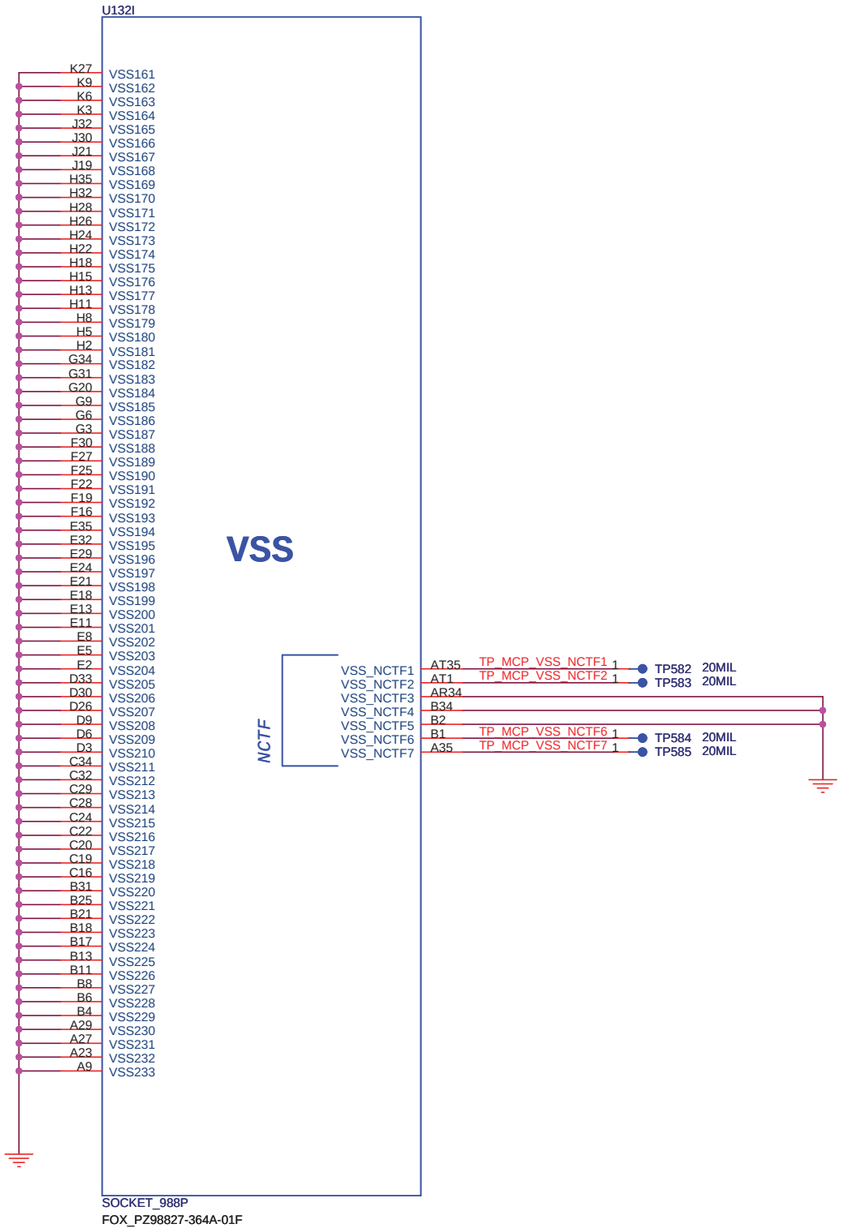
For Disable Arrandale Graphic
VAXG_SENSE and VSSAXG_SENSE on Arrandale can be left as no connect.



DVT2 change to SOCKET_988A

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (GRAPHICS POWER)	
Size Custom	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, September 23, 2009	Sheet 6 of 73	





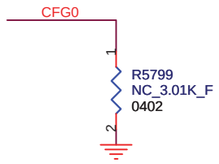
DVT2 change to SOCKET_988A

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	ARD (GND)		
Size	Document Number		Rev
Custom	M9A0_MP		1.1
Date:	Wednesday, September 23, 2009	Sheet 7 of 73	

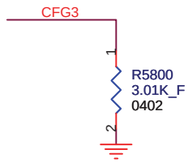
PCI Express Configuration Select
CFG0 1 : Single PEG * default
0 : Bifurcation enable

3393727 The VIL Voltage DC Specification for CFG[0] Pin is in Violation of the EDS Value by a Large Amount
The Clarksfield EDS Vol1 documents the CFG[1:0] pins for PCI Express Port Bifurcation, the straps may not work correctly when using a pull down resistor of value other than 250 Ohms to drive a value of zero on the CFG[0] pin. When left floating a value of one is sensed and there is no impact in this case.

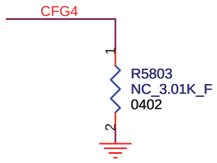
CFG pin is latch on the rising edge of CPU powergood.

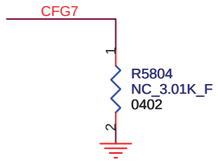


CFG3 PCI Express Static Lane Reversal
CFG3 1 : Normal
0 : Lane Numbers Reversed *
15 ->0 , 14-> 1 , ...



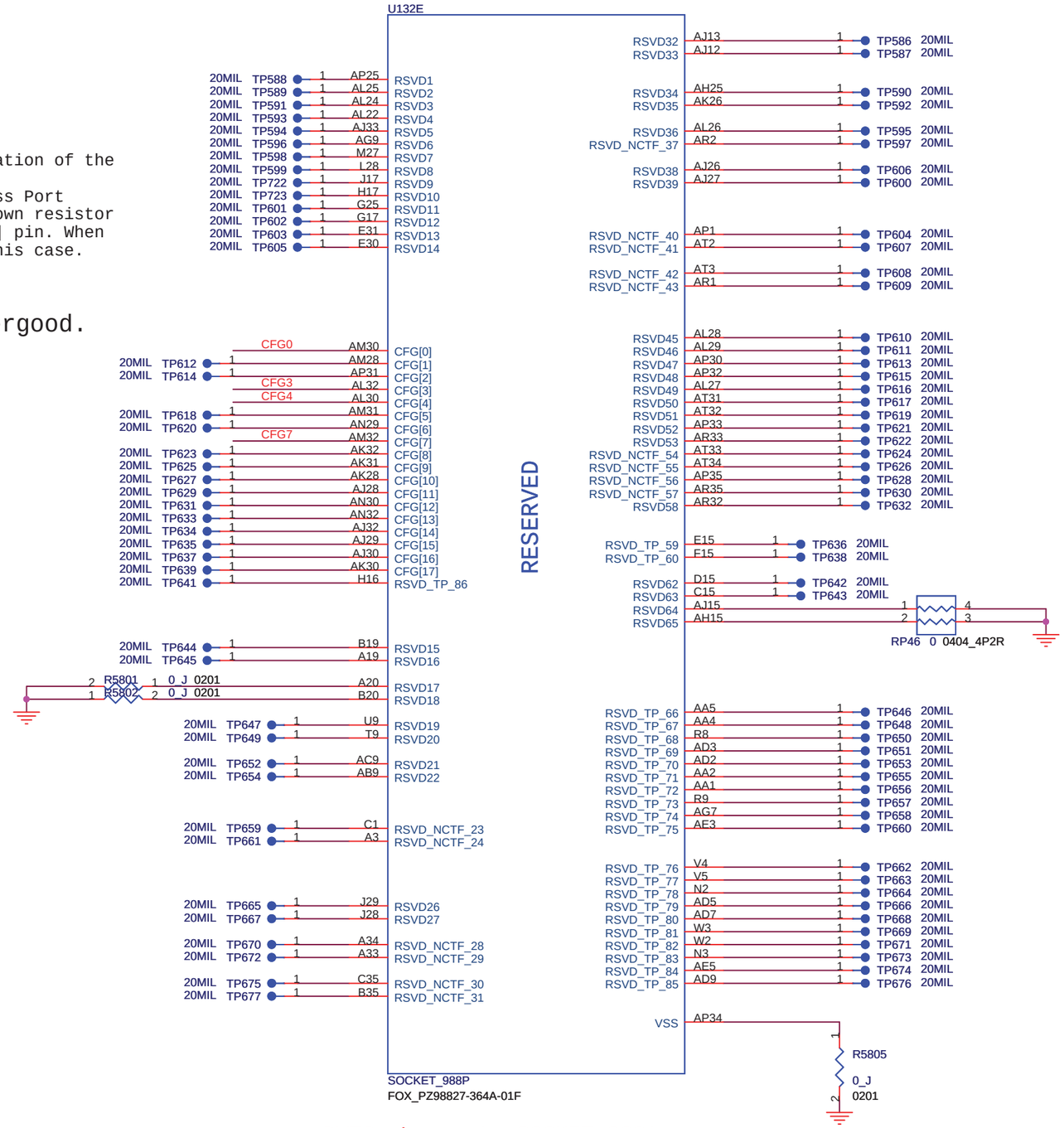
CFG4 Display Port Presence
CFG4 1 : Disabled ; No Physical Display Port attached to Embedded Display Port
0 : Enable ; An external Display Port device is connected to the Embedded Display Port





2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down).
Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.



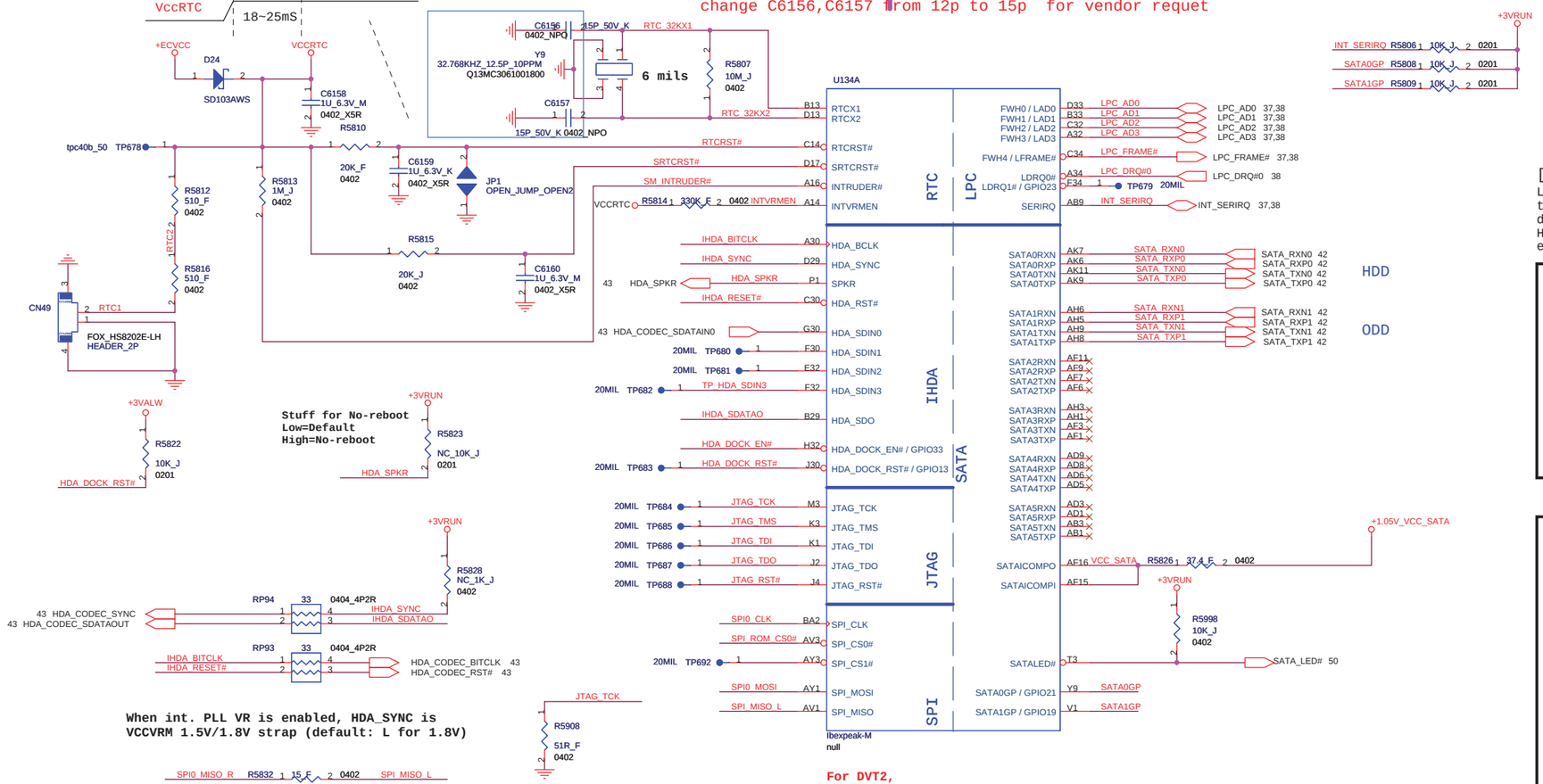
DVT2 change to SOCKET_988A

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	ARD (RESERVED)		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Wednesday, September 23, 2009	Sheet 8 of 73		

RTCRST#
VccRTC
18~25mS

The traces inside this block should be wider.

2009.0925
change C6156,C6157 from 12p to 15p for vendor requet



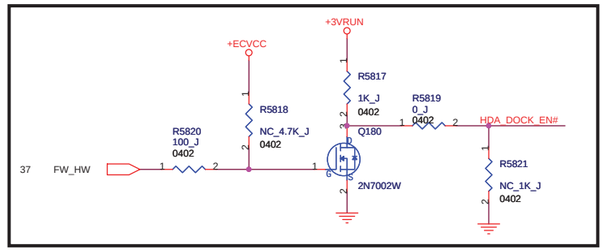
When int. PLL VR is enabled, HDA_SYNC is VCCVRM 1.5V/1.8V strap (default: L for 1.8V)

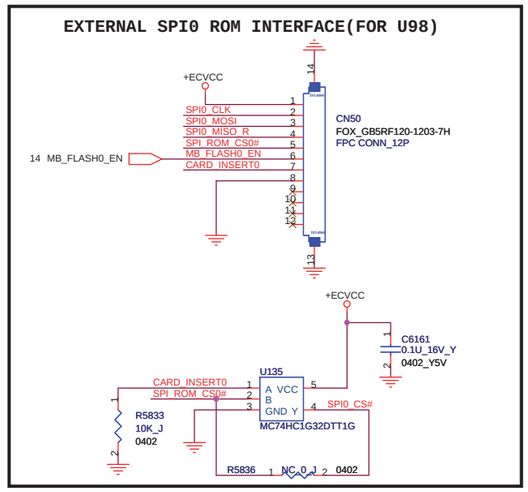
For DVT2,
ARD(QS)+PM55(MP)+4M SPI ROM

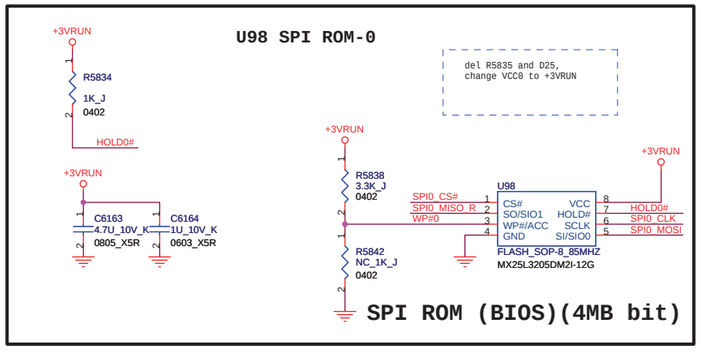
HDD

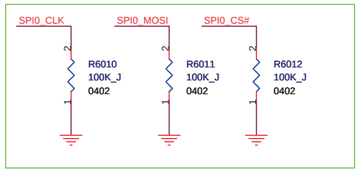
ODD

[HDA_DOCK_EN#/GPIO33]
Low (0) – Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.
High (1) – Security measure defined in the Flash Descriptor will be enabled







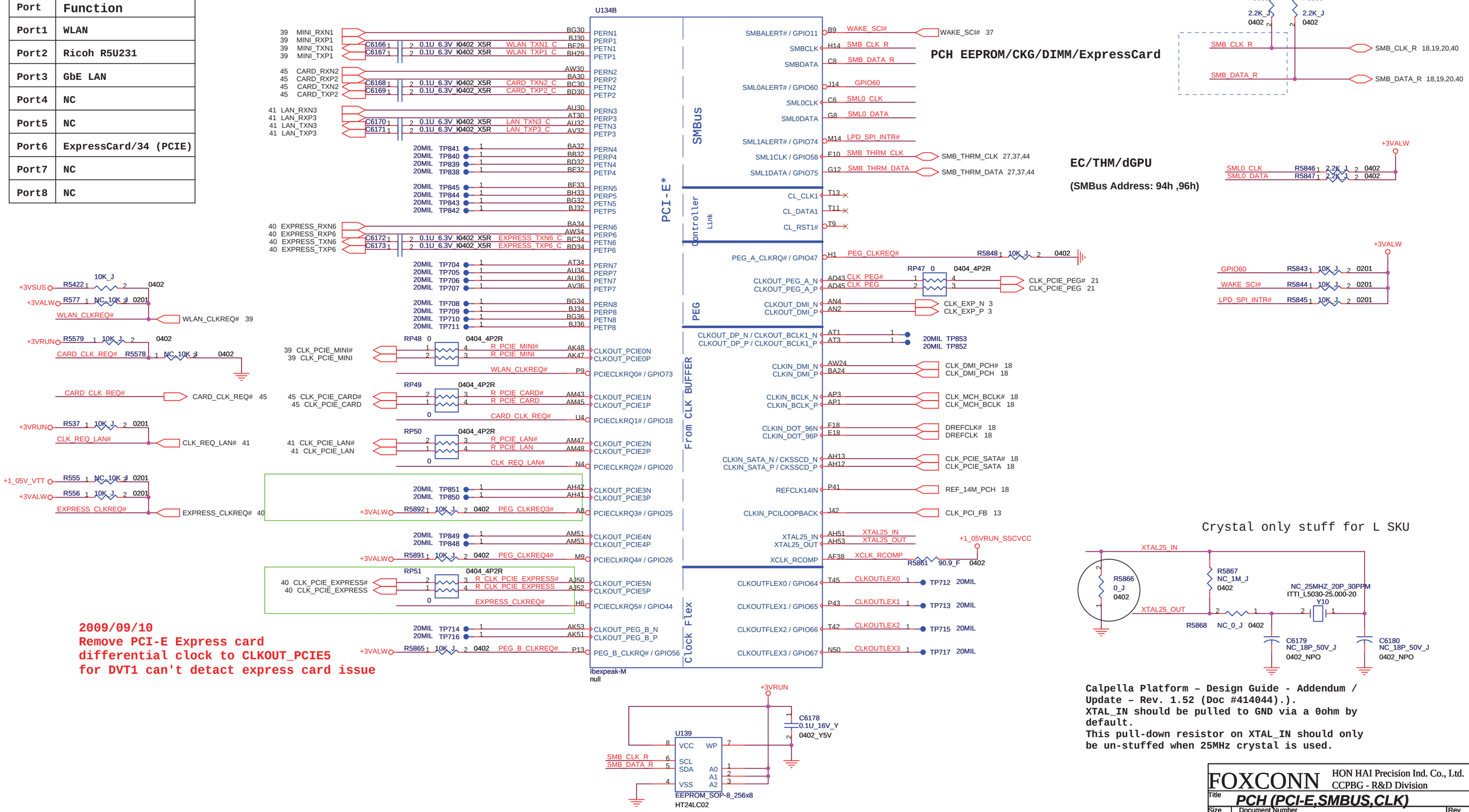


add follow EDS

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (HDA,JTAG,SAT)	
Size: Custom	Document Number: M9A0 MP	Rev: 1.1
Date: Friday, October 23, 2009	Sheet 9 of 73	

PCI-E Port Table

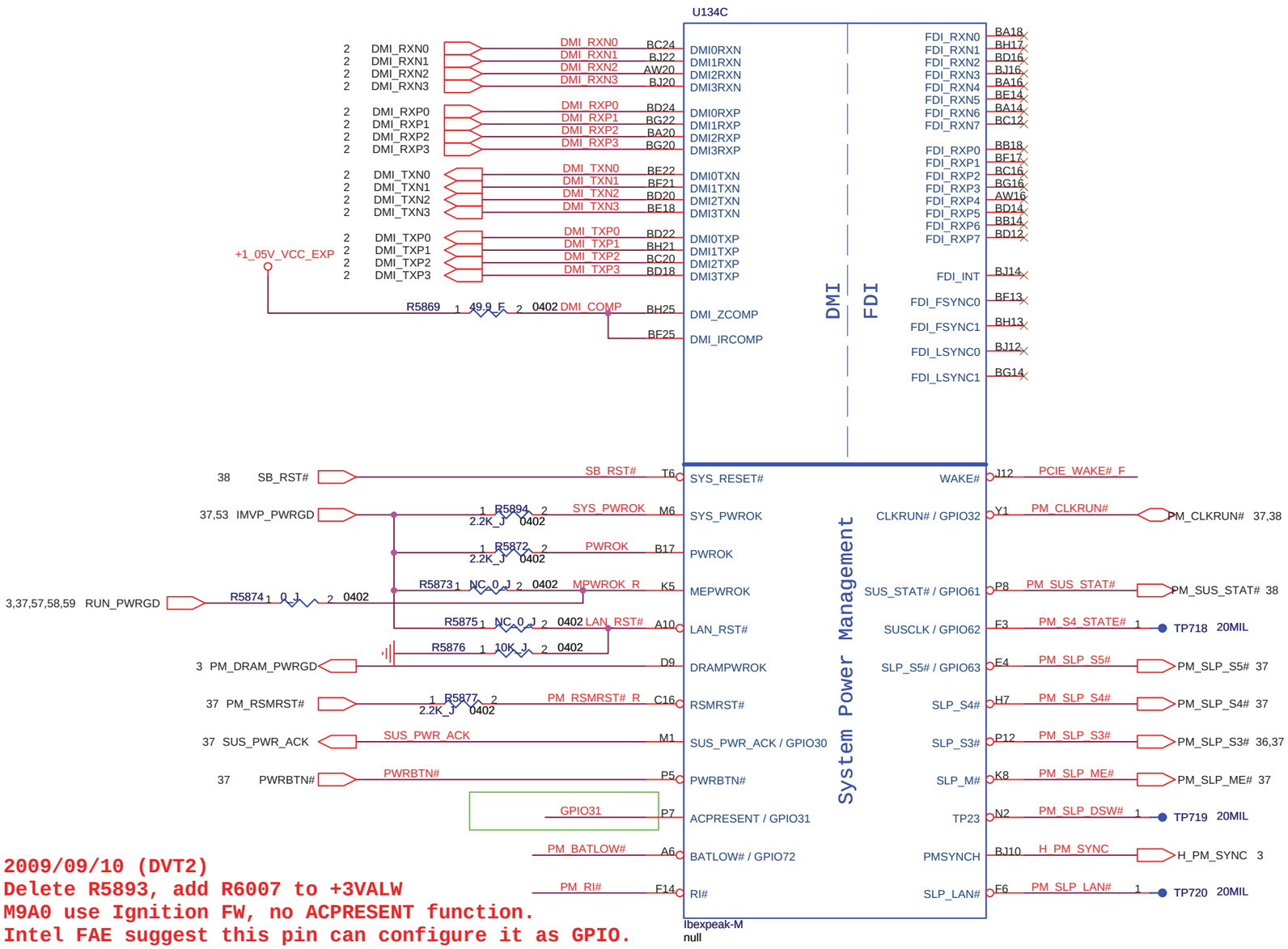
Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	NC
Port5	NC
Port6	ExpressCard/34 (PCIE)
Port7	NC
Port8	NC



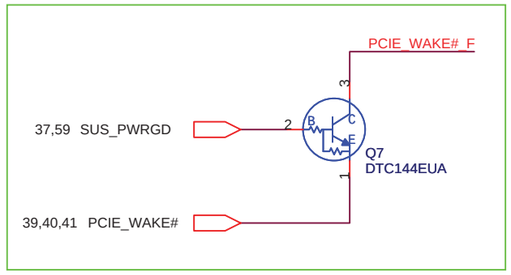
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

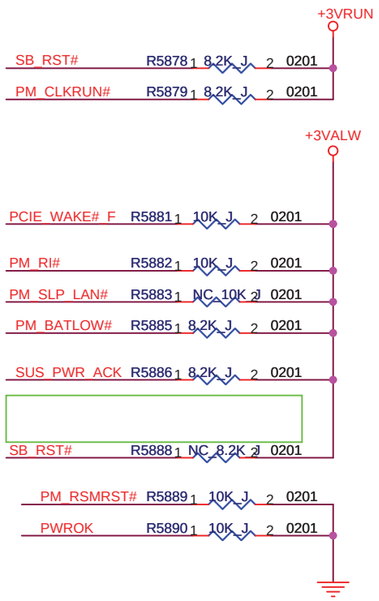
Title	PCH (PCI-E,SMBUS,CLK)		
Size: Custom	Document Number: M9A0_MP		Rev: 1.1
Date: Friday, October 23, 2009	Sheet 10 of 73		

For Disable Auburndale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The
GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

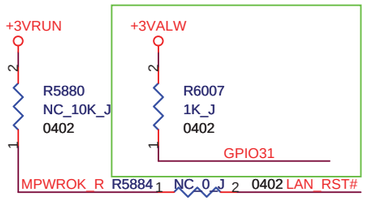


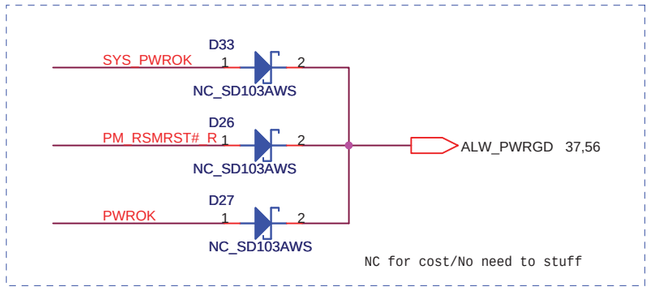
2009.0928
Add the Q7 as MOR request.





2009/09/10 (DVT2)
Delete R5893, add R6007 to +3VALW
M9A0 use Ignition FW, no ACPRESENT function.
Intel FAE suggest this pin can configure it as GPIO.

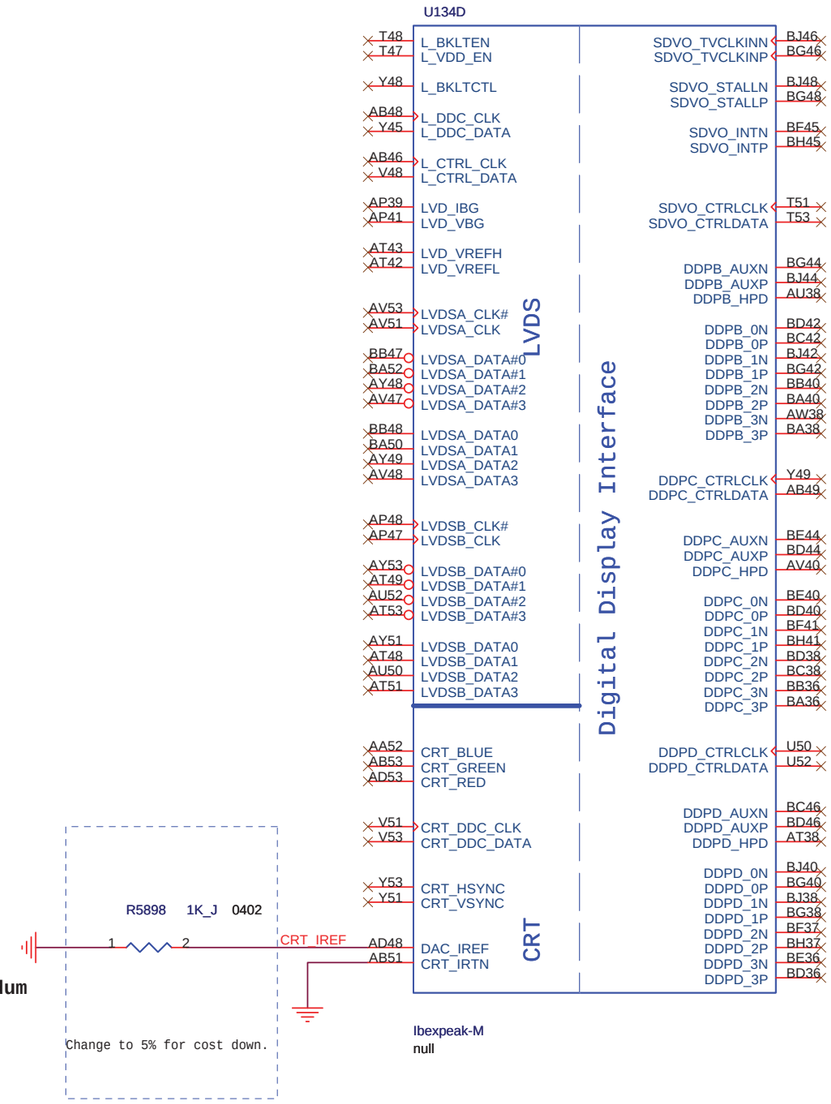




PM_SLP_ME# 1 TP721 20MIL

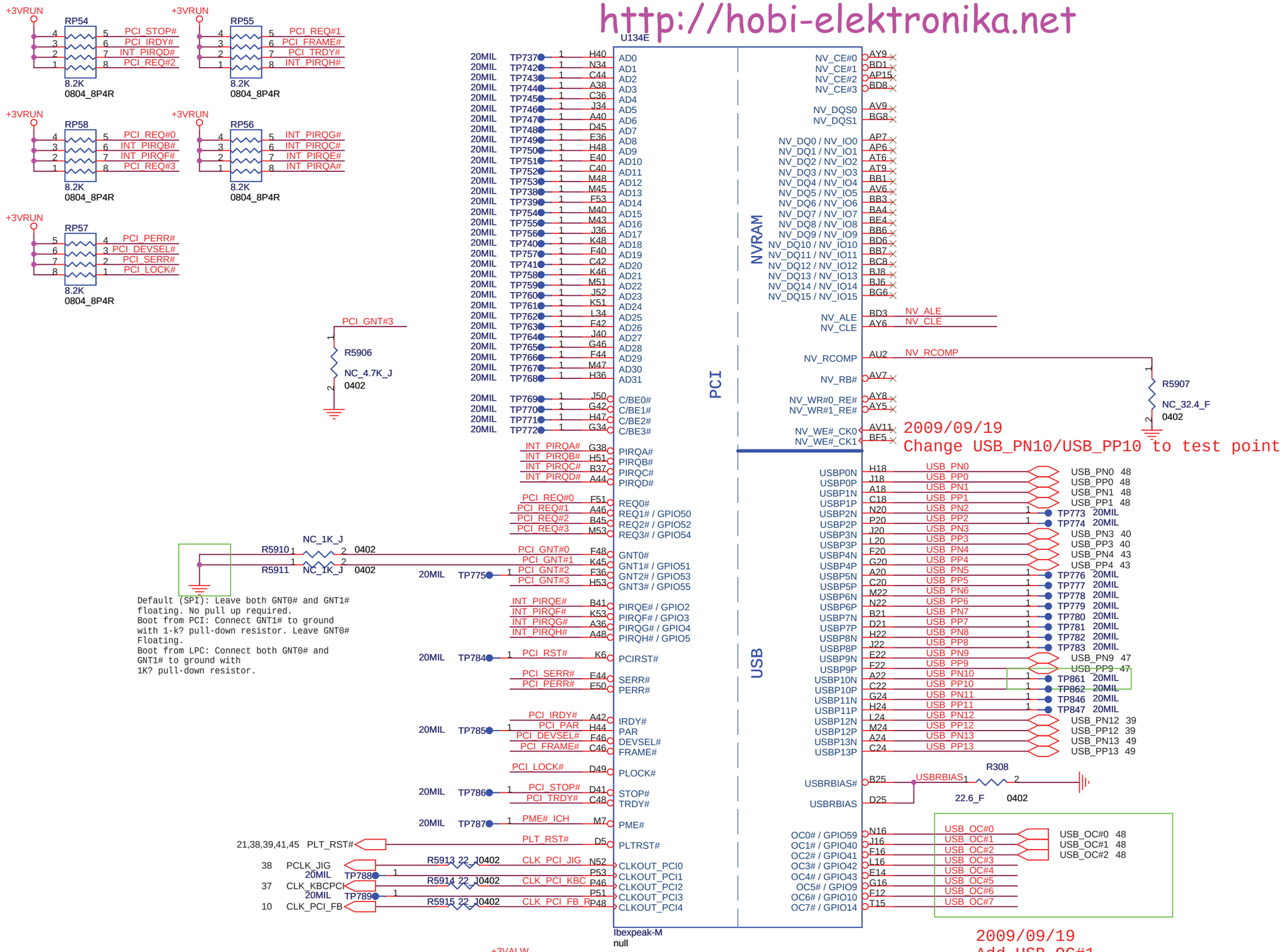
2009/09/10 (DVT2)
Delete R5887 and Net name AC_Present
M9A0 use Ignition FW, no ACPRESENT function.
Intel FAE suggest this pin can configure it as GPIO.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (DMI,FDI,GPIO)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 11 of 73	



Calpella Platform – Design Guide - Addendum / Update – Rev. 1.52 (Doc #414044).).

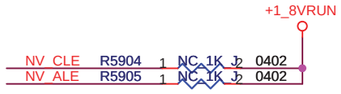
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (LVDS,DDI)	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Wednesday, September 23, 2009	Sheet 12 of 73	



2009/09/19
Change USB_PN10/USB_PP10 to test point

2009/09/19
Add USB_OC#1

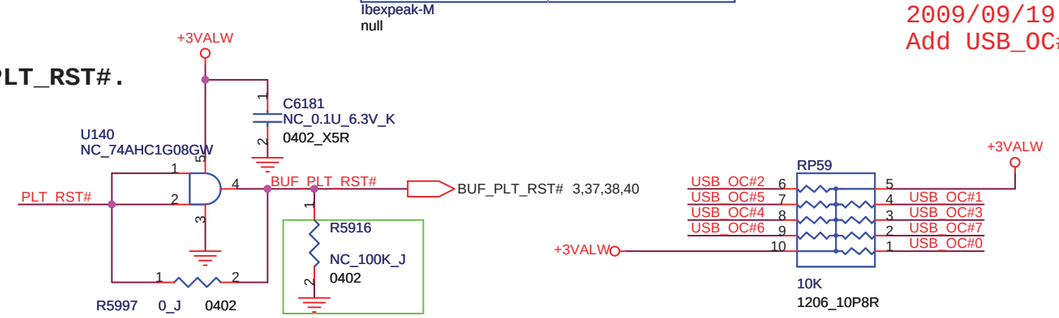
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



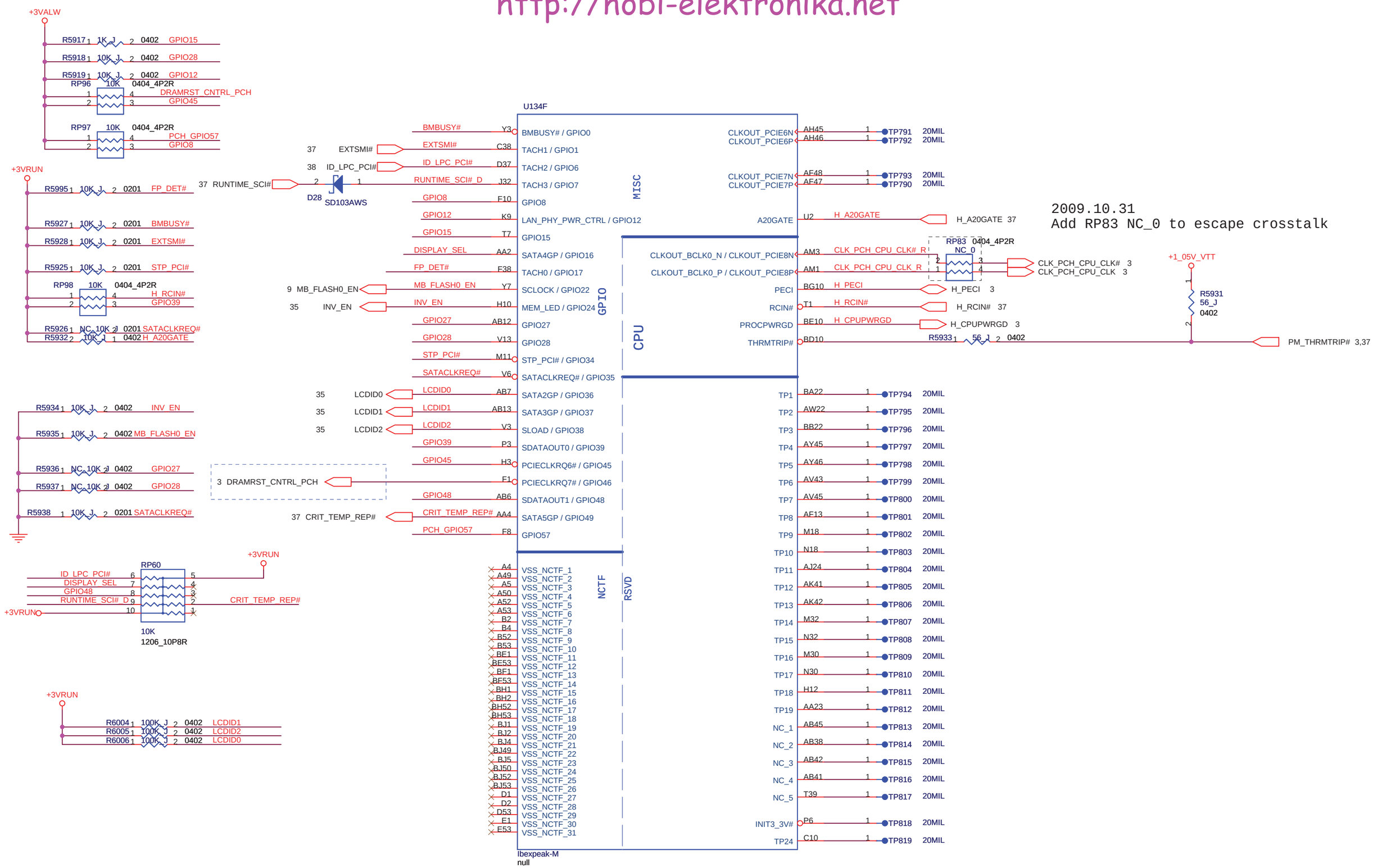
Intel Anti-Theft Technology
Disabled when Low , NC R1616
Enabled when High ,Stuff R1616

USB PORT	Function
PORT-0	External Port-0
PORT-1	External Port-1
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port-2
PORT-5	
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	No finger print
PORT-11	
PORT-12	Wireless LAN (WiMAX)
PORT-13	Bluetooth

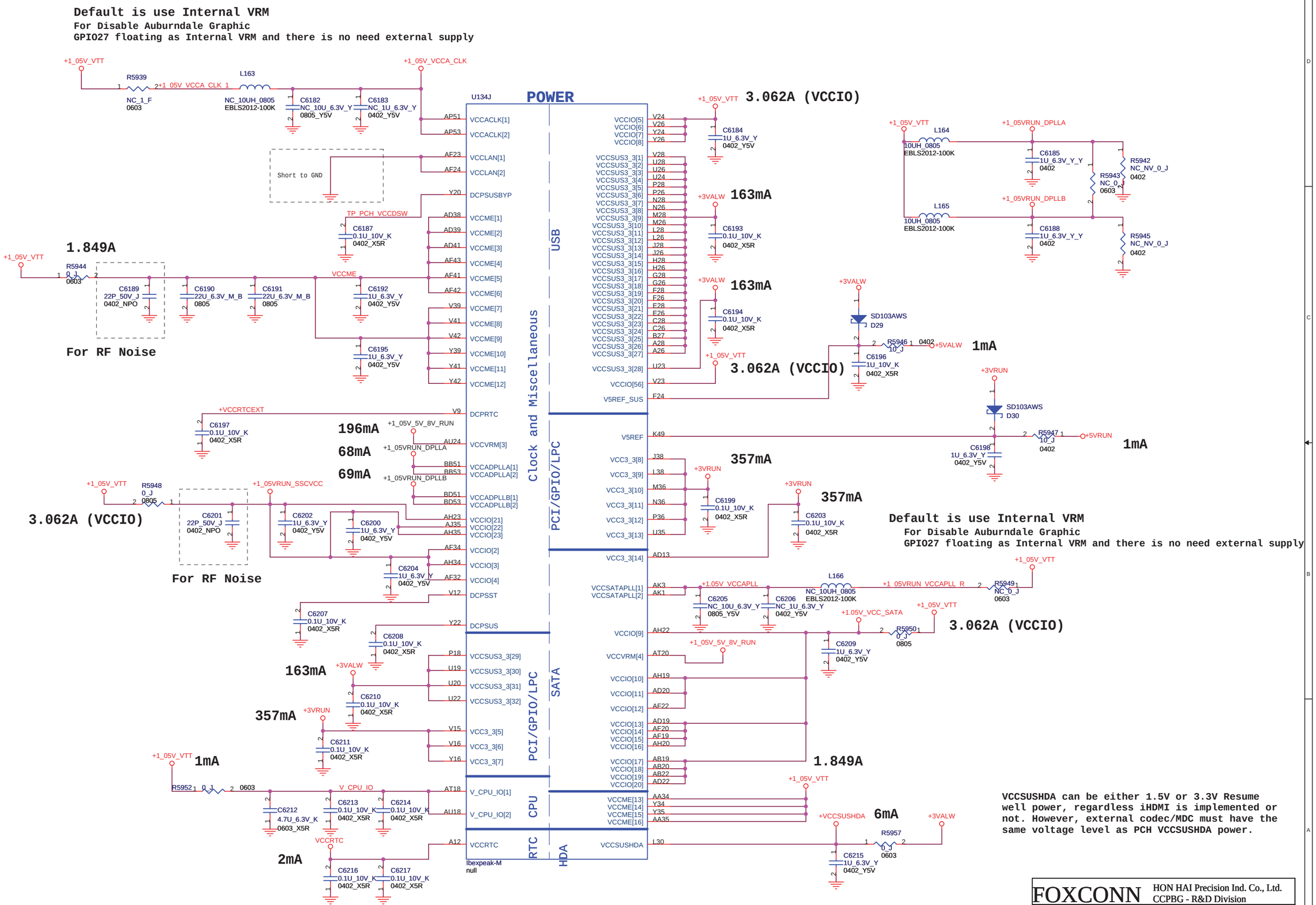
Buffer to reduce loading on PLT_RST#.



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (PCI,USB,NVRAM)		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Friday, October 23, 2009	Sheet 13 of 73		



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (GPIO,VSS_NCTF,RSVD)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Saturday, October 31, 2009	Sheet 14 of 73	

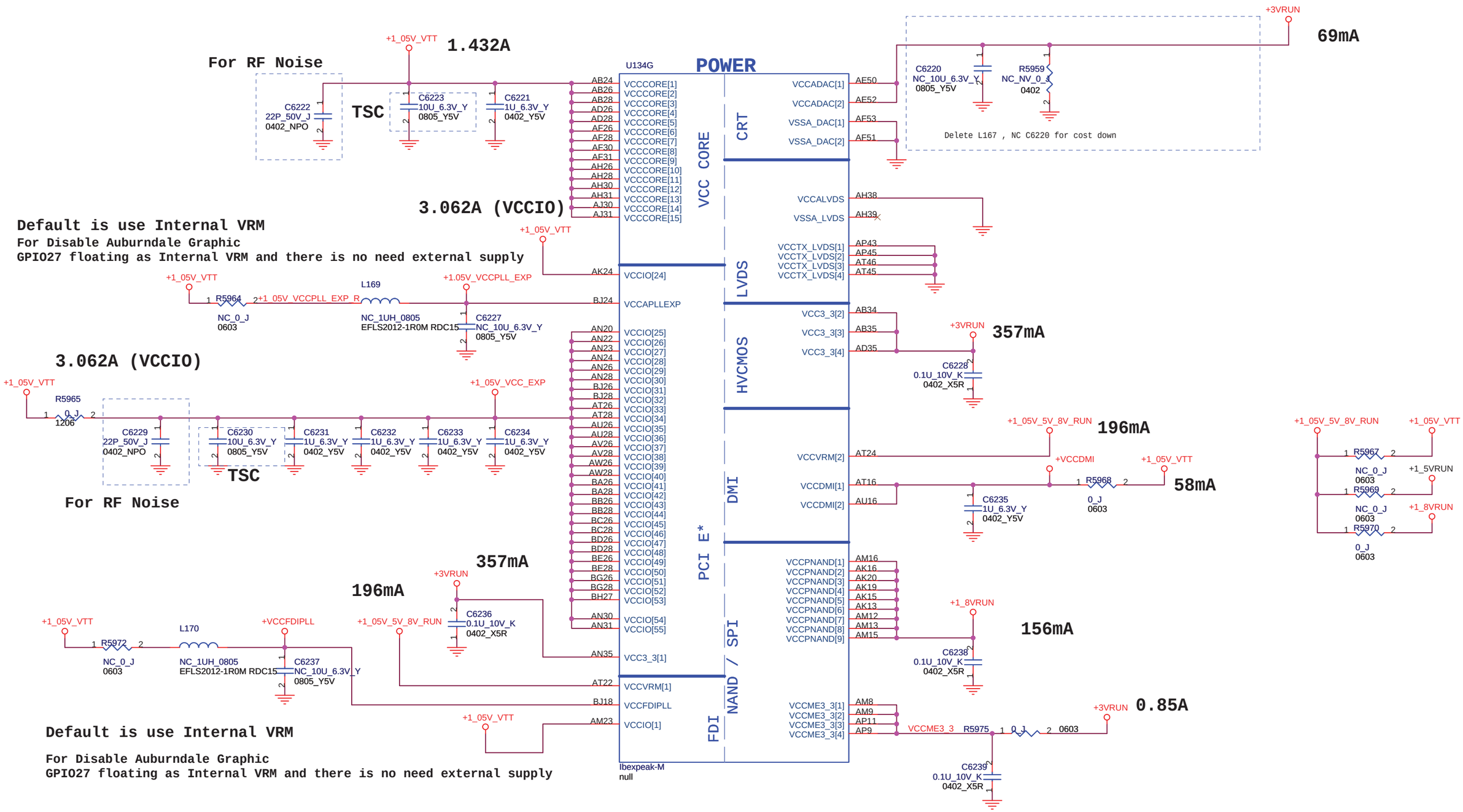


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

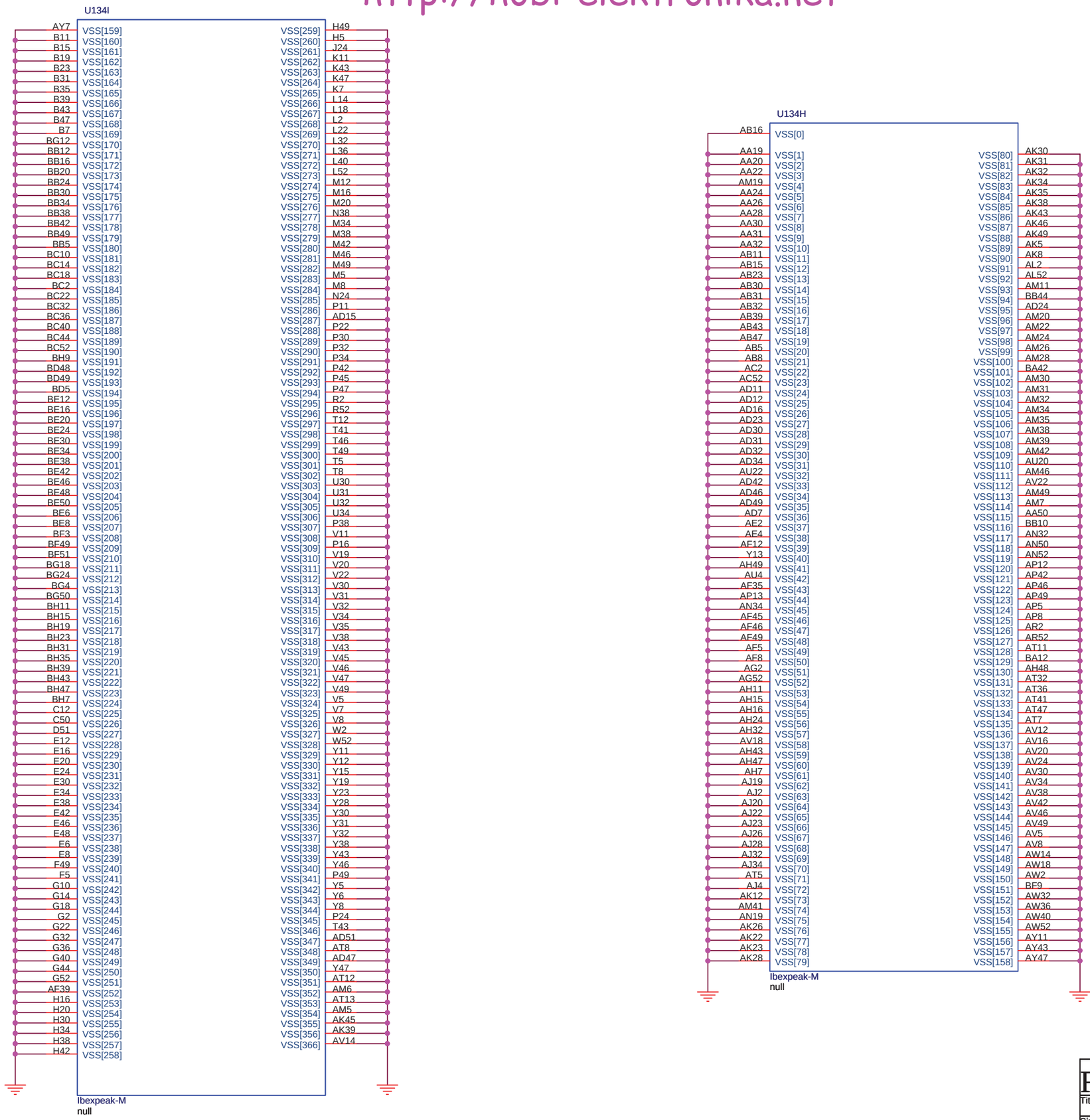
Title: PCH (POWER) 1/2

Size: Custom | Document Number: M9A0_MP | Rev: 1.1

Date: Friday, September 25, 2009 | Sheet 15 of 73



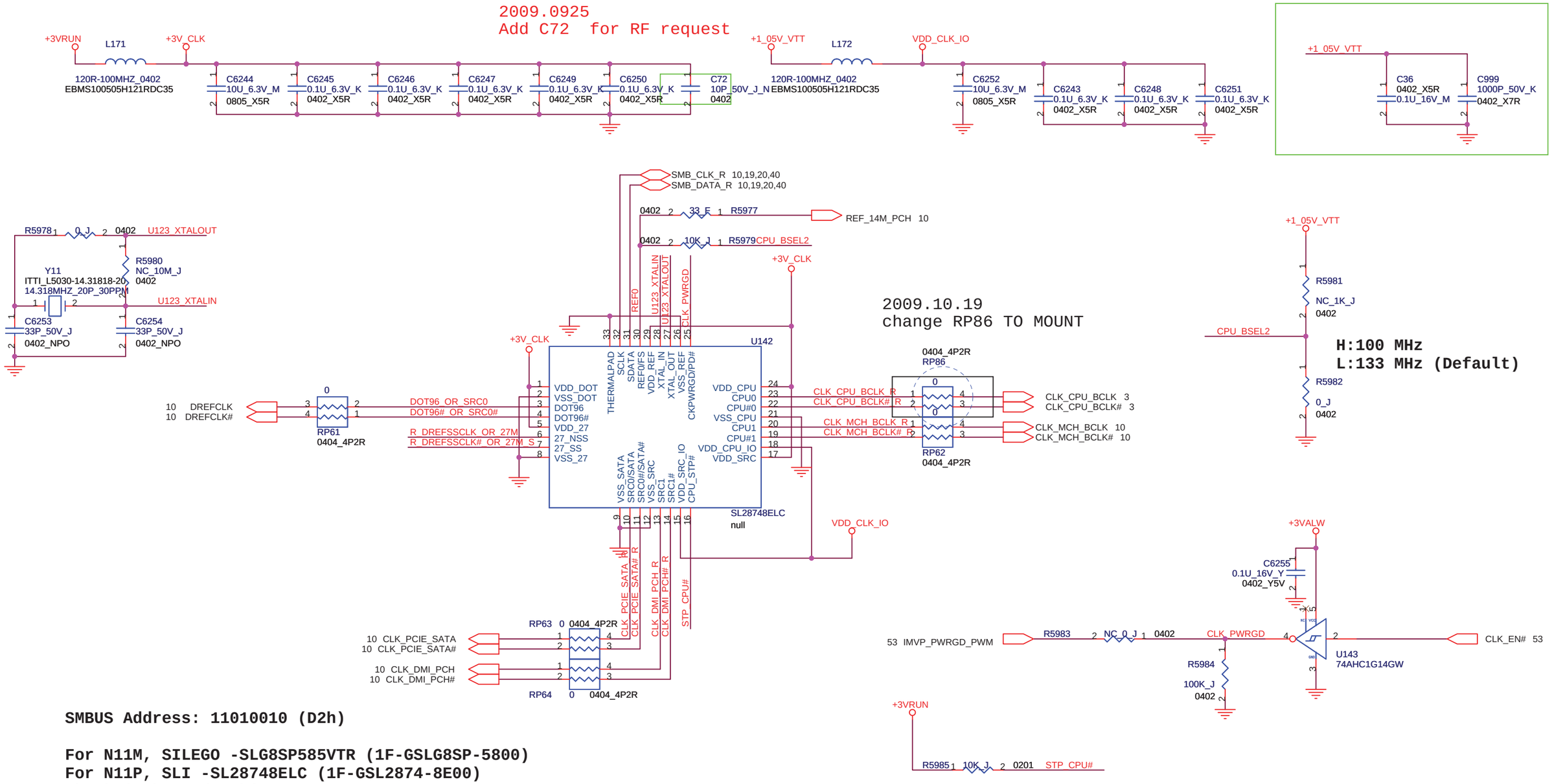
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (POWER) 2/2	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, September 23, 2009	Sheet 16 of 73	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**PCH (VSS)**	
Size A3	Document Number **M9A0_MP**	Rev 1.1
Date: Wednesday, September 23, 2009	Sheet 17 of 73	

2009.0925
ADD for EMI request

2009.0925
Add C72 for RF request



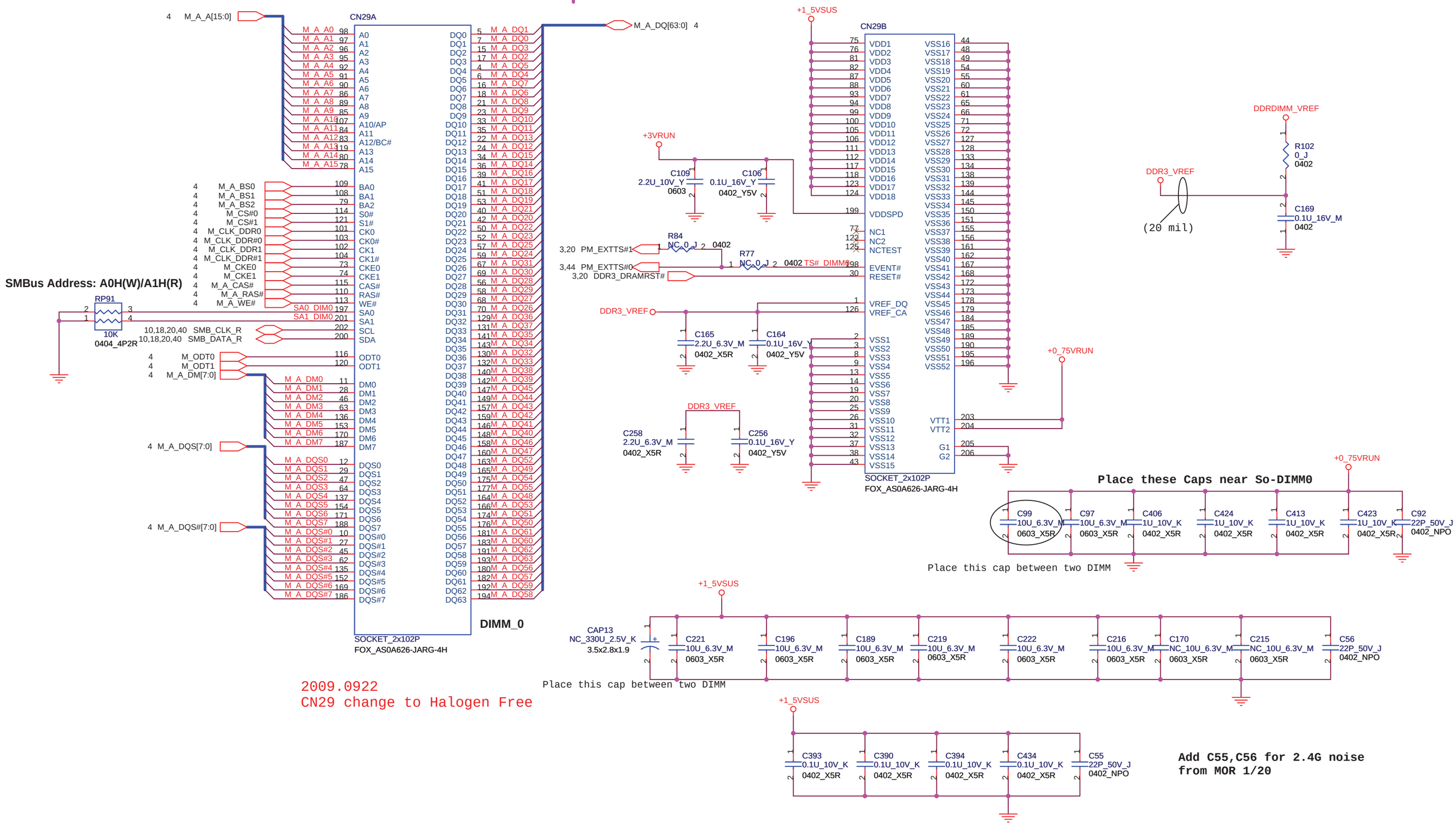
SMBUS Address: 11010010 (D2h)

For N11M, SILEGO -SLG8SP585VTR (1F-GSLG8SP-5800)
For N11P, SLI -SL28748ELC (1F-GSL2874-8E00)
Check it by Model bit0

Frequency Select Pin (FS)

FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	CLOCK GEN
Size A3	Document Number M9A0_MP
Rev	1.1
Date: Friday, October 23, 2009	Sheet 18 of 73



2009.0922
CN29 change to Halogen Free

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR(III)SO-DIMM_0	
Size A3	Document Number M9A0_MP	Rev 1.1
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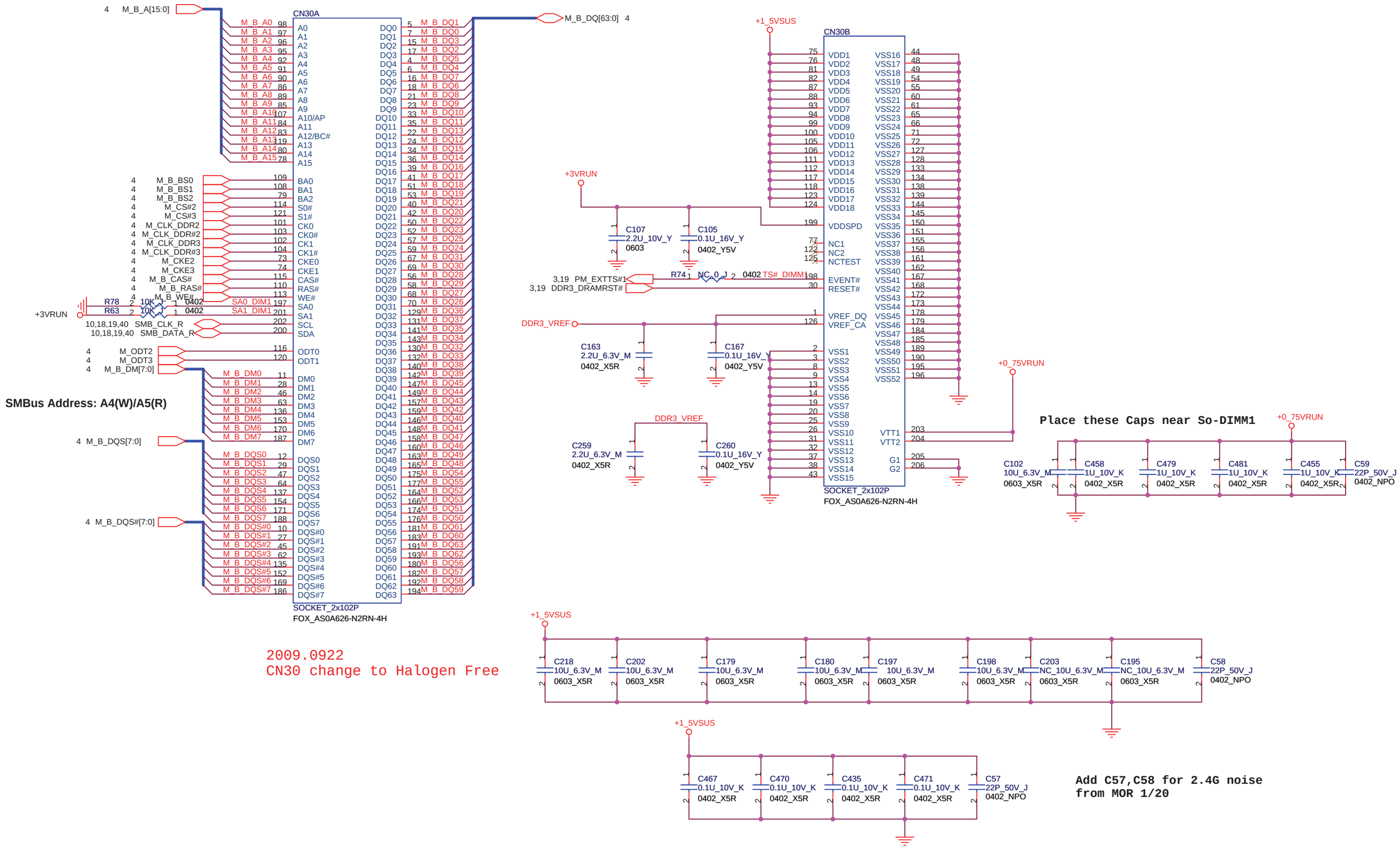

2009.0922
CN30 change to Halogen Free

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR(III)SO-DIMM_1	
Size A3	Document Number M9A0_MP	Rev 1.1
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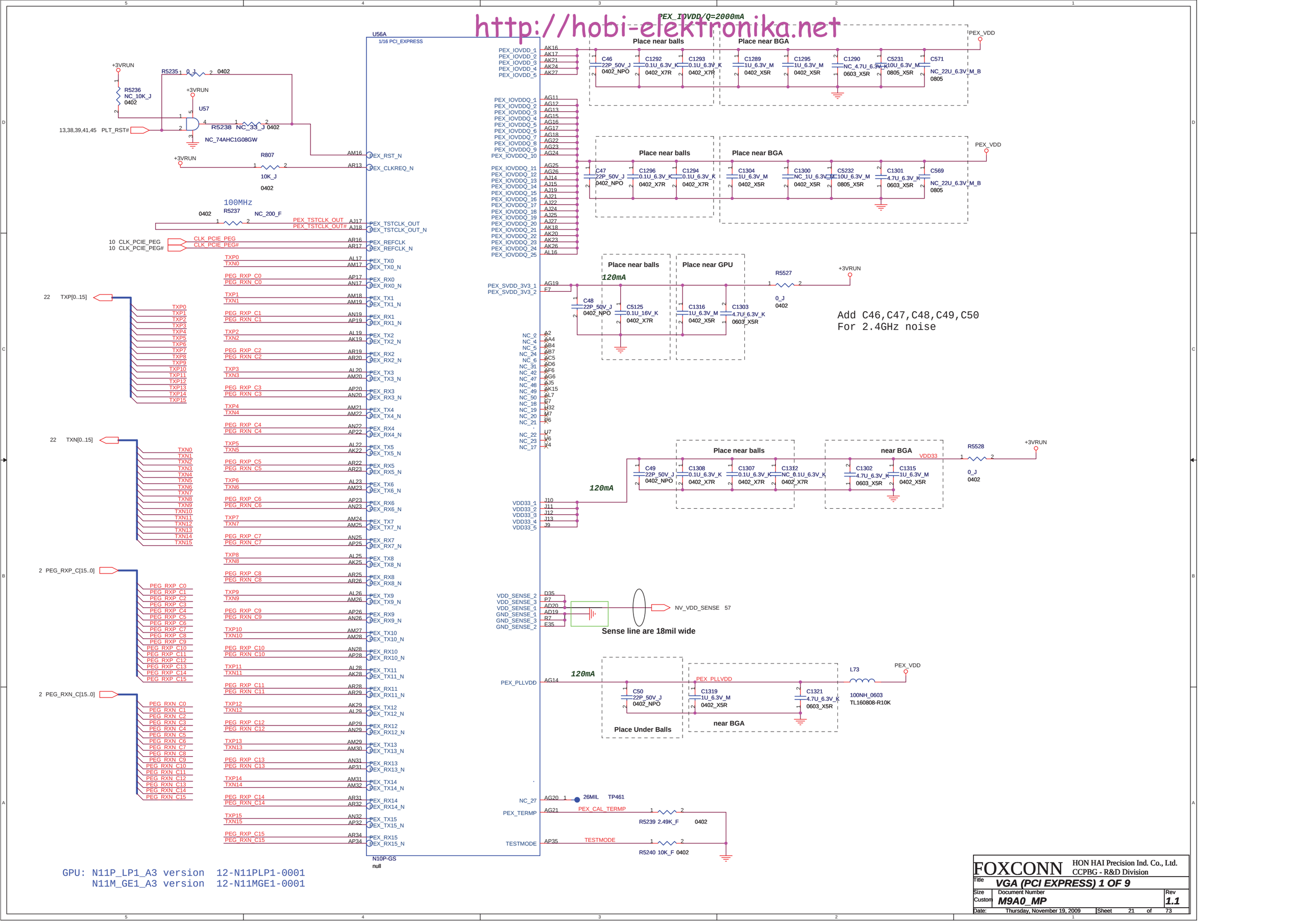

GPU: N11P_LP1_A3 version 12-N11PLP1-0001
N11M_GE1_A3 version 12-N11MGE1-0001

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title	VGA (PCI EXPRESS) 1 OF 9	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
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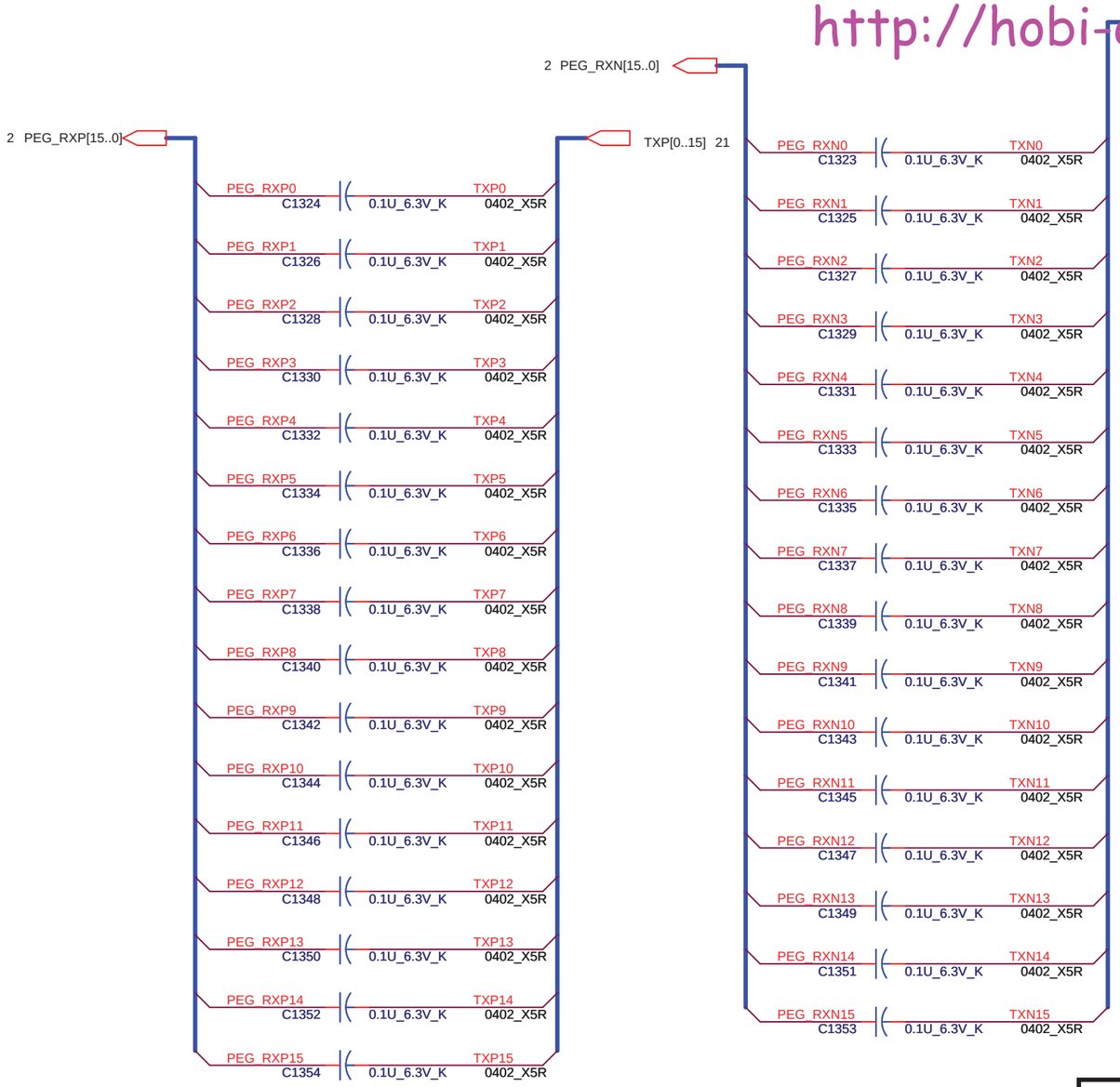


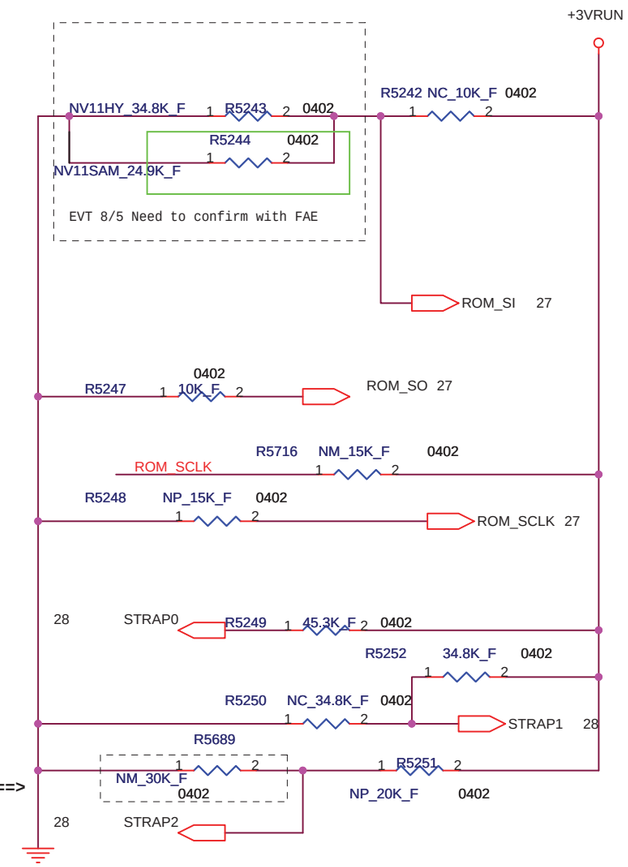
XCLK_417 0 (27M Hz) 1 (Reserved) FB_0_BAR_SIZE 0 256MB 1 (Reserved) SMB_ALT_ADDR 0 0x9E 1 0x9C(multi-GPU usage) VGA_DEVICE 0 3D device(class code 302h) 1 VGA device(class code 300h)	ROM_SO 0001
SUB_VENDOR 0 (No vedio BIOS ROM) 1 (BIOS ROM is present) SLOT_CLK_CFG 0 (GPU and MCH not share a common reference clk) 1 (GPU and MCH share a common reference clk) PEX_PLL_EN_TERM 0 (Disable) 1 (Enable)	ROM_SCLK N11P-LP1 0010 N11M-GE1 1010
USER[3:0] 1111	STRAP0 (1111)
N10x/N11x 3GIO_PADCFG[3:0] 1110	STRAP1 (1110)
N11X PCI_DEVID[3:0] N11P-LP1 1011b N11M-GE1 0101b PCI DEVICE IDs N11P-LP1 (0x0A2B) N11M-GE1 (0x0A75)	Strap2 N11P-LP1 1011 N11M-GE1 0101

0000 64-bit Reserved
1110 32Mx32 GDDR3 - 136 ball 64-bit Hynix - 35K pul Low.
0100 32Mx32 GDDR3 - 136 ball 64-bit Samsung- 25K pull Low
ROM_SI

8/3 [DVT] Revise the
Strap Pin value as FAE
provided for DVT Sample.

- N11M-GE1 x0A75
- N11P-LP1 0x0A2B

2009/9/10
N11P-LP1+SANSUNG(H2) SKU and
N11M-GE1 +SANSUANG(M2 SKU)need change BOM
R5244 change from 1R-0004532-F200(45.3K) to
1R-0002492-F200(24.9K) for nVIDIA FAE suggest



===>

Logical Strap bit Mapping

Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

Refer to <GB1 Family Design Guide DG-04642-001_v01_secured>

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Title: VGA (PCI-EXPRESS/STRAP) 2 OF 9

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M9A0 FBVDDQ current N11P_LP1 is 6.5A . N11M_GE1 is 3.3A

U56B
2/16 FBA

30 FBAD[0:63]

FBAD0	L32	FBA_D00
FBAD1	N33	FBA_D01
FBAD2	L33	FBA_D02
FBAD3	N34	FBA_D03
FBAD4	N35	FBA_D04
FBAD5	P35	FBA_D05
FBAD6	P33	FBA_D06
FBAD7	P34	FBA_D07
FBAD8	K35	FBA_D08
FBAD9	K33	FBA_D09
FBAD10	K34	FBA_D10
FBAD11	H33	FBA_D11
FBAD12	G34	FBA_D12
FBAD13	G33	FBA_D13
FBAD14	E34	FBA_D14
FBAD15	E33	FBA_D15
FBAD16	G31	FBA_D16
FBAD17	F30	FBA_D17
FBAD18	G30	FBA_D18
FBAD19	G32	FBA_D19
FBAD20	K30	FBA_D20
FBAD21	K32	FBA_D21
FBAD22	H30	FBA_D22
FBAD23	K31	FBA_D23
FBAD24	L31	FBA_D24
FBAD25	L30	FBA_D25
FBAD26	M32	FBA_D26
FBAD27	N30	FBA_D27
FBAD28	M30	FBA_D28
FBAD29	P31	FBA_D29
FBAD30	R32	FBA_D30
FBAD31	R30	FBA_D31
FBAD32	AG30	FBA_D32
FBAD33	AG32	FBA_D33
FBAD34	AH31	FBA_D34
FBAD35	AF31	FBA_D35
FBAD36	AF30	FBA_D36
FBAD37	AE30	FBA_D37
FBAD38	AC32	FBA_D38
FBAD39	AD30	FBA_D39
FBAD40	AN33	FBA_D40
FBAD41	AL31	FBA_D41
FBAD42	AM33	FBA_D42
FBAD43	AL33	FBA_D43
FBAD44	AK30	FBA_D44
FBAD45	AK32	FBA_D45
FBAD46	AJ30	FBA_D46
FBAD47	AH30	FBA_D47
FBAD48	AH33	FBA_D48
FBAD49	AH35	FBA_D49
FBAD50	AH34	FBA_D50
FBAD51	AH32	FBA_D51
FBAD52	AJ33	FBA_D52
FBAD53	AL35	FBA_D53
FBAD54	AM34	FBA_D54
FBAD55	AM35	FBA_D55
FBAD56	AF33	FBA_D56
FBAD57	AF32	FBA_D57
FBAD58	AF34	FBA_D58
FBAD59	AE35	FBA_D59
FBAD60	AE34	FBA_D60
FBAD61	AE33	FBA_D61
FBAD62	AB32	FBA_D62
FBAD63	AC35	FBA_D63

30 FBADQM[7..0]

FBADQM0	P32	FBA_DQM0
FBADQM1	H34	FBA_DQM1
FBADQM2	J30	FBA_DQM2
FBADQM3	P30	FBA_DQM3
FBADQM4	AF32	FBA_DQM4
FBADQM5	AL32	FBA_DQM5
FBADQM6	AL34	FBA_DQM6
FBADQM7	AF35	FBA_DQM7

30 FBAWDQS[7..0]

FBAWDQS0	L34	FBA_DQS_WP0
FBAWDQS1	H35	FBA_DQS_WP1
FBAWDQS2	J32	FBA_DQS_WP2
FBAWDQS3	N31	FBA_DQS_WP3
FBAWDQS4	AE31	FBA_DQS_WP4
FBAWDQS5	AJ32	FBA_DQS_WP5
FBAWDQS6	AJ34	FBA_DQS_WP6
FBAWDQS7	AC33	FBA_DQS_WP7

30 FBARDQS[7..0]

FBARDQS0	L35	FBA_DQS_RN0
FBARDQS1	G35	FBA_DQS_RN1
FBARDQS2	H31	FBA_DQS_RN2
FBARDQS3	N32	FBA_DQS_RN3
FBARDQS4	AD32	FBA_DQS_RN4
FBARDQS5	AJ31	FBA_DQS_RN5
FBARDQS6	AJ35	FBA_DQS_RN6
FBARDQS7	AC34	FBA_DQS_RN7

P29	NC_45
R29	NC_46
L29	NC_43
M29	NC_44
AG29	NC_28
AH29	NC_29
AD29	NC_25
AE29	NC_26

TP492 26MIL 1 J27 FB_VREF

N10P-GS
null

FBVDDQ_25	J23	
FBVDDQ_26	J24	
FBVDDQ_27	J29	
FBVDDQ_1	AA27	
FBVDDQ_2	AA29	
FBVDDQ_3	AA31	
FBVDDQ_4	AB27	
FBVDDQ_5	AB29	
FBVDDQ_6	AC27	
FBVDDQ_7	AD27	
FBVDDQ_8	AE27	
FBVDDQ_9	AJ28	
FBVDDQ_10	B18	
FBVDDQ_11	F21	
FBVDDQ_12	G17	
FBVDDQ_13	G18	
FBVDDQ_14	G22	
FBVDDQ_15	G8	
FBVDDQ_16	G9	
FBVDDQ_17	H29	
FBVDDQ_18	J14	
FBVDDQ_19	J15	
FBVDDQ_20	J16	
FBVDDQ_21	J17	
FBVDDQ_22	J20	
FBVDDQ_23	J21	
FBVDDQ_24	J22	

Place near IGA

+1_8VRUN

C35 10P_50V_J 0402_NPO
C874 NC_0.1U_6.3V_K 0402_X7R
C875 0.1U_6.3V_K 0402_X7R
C876 NP_0.1U_6.3V_K 0402_X7R
C877 0.047U_10V_K 0402_X7R
C880 0.047U_10V_K 0402_X7R

08/12/26 Add C33 follow RF propose.

C6018 NP_0.047U_10V_K 0402_X7R
C6014 0.01U_10V_K 0402_X7R
C6015 0.01U_10V_K 0402_X7R
C6016 NP_0.01U_10V_K 0402_X7R
C6017 NP_0.01U_10V_K 0402_X7R

Place near the chip

C2 22P_50V_J 0402_NPO
C6020 4.7U_6.3V_K 0603_X5R
C6019 NP_4.7U_6.3V_K 0603_X5R

08/12/25 Add C2(22P) against 2.4GHz noise.

C876,C6018,C6016,C6017,C6019 only for N11P

FBA_CMD0	V32	FBA_A4	
FBA_CMD1	W31	FBA_RAS#	FBA_RAS# 30
FBA_CMD2	U31	FBA_A5	
FBA_CMD3	Y32	FBA_BA1	FBA_BA1 30
FBA_CMD4	AB35	FBB_A2	
FBA_CMD5	AB34	FBB_A4	
FBA_CMD6	W35	FBB_A3	
FBA_CMD7	W33		FBB_CKE 30
FBA_CMD8	W30		FBB_CS0# 30
FBA_CMD9	T34	FBA_A11	
FBA_CMD10	T35	FBA_CAS#	FBA_CAS# 30
FBA_CMD11	AB31	FBA_WE#	FBA_WE# 30
FBA_CMD12	Y30	FBA_BA0	FBA_BA0 30
FBA_CMD13	Y34	FBB_A5	
FBA_CMD14	W32	FBA_A12	
FBA_CMD15	AA30	FBA_RESET	FBA_RESET 30
FBA_CMD16	AA32	FBA_A7	
FBA_CMD17	Y33	FBA_A10	
FBA_CMD18	U32	FBA_CKE	FBA_CKE 30
FBA_CMD19	Y31	FBA_A0	
FBA_CMD20	U34	FBA_A9	
FBA_CMD21	Y35	FBA_A6	
FBA_CMD22	W34	FBA_A2	
FBA_CMD23	V30	FBA_A8	
FBA_CMD24	U35	FBA_A3	
FBA_CMD25	U30	FBA_A1	
FBA_CMD26	U33	FBA_A13	1 26MIL TP419
FBA_CMD27	AB30	FBA_BA2	FBA_BA2 30
FBA_CMD28	AB33	FBA_RFU0	1 26MIL TP420
FBA_CMD29	T33	FBA_CS0#	FBA_CS0# 30
FBA_CMD30	W29	FBA_CMD30	1 26MIL TP463

FBA_CLK0	T32	FBA_CLK0	FBA_CLK0 30
FBA_CLK0_N	T31	FBA_CLK0#	FBA_CLK0# 30
FBA_CLK1	AC31	FBA_CLK1	FBA_CLK1 30
FBA_CLK1_N	AC30	FBA_CLK1#	FBA_CLK1# 30

FBA_DEBUG T30 FBB_CAS# FBB_CAS# 30

FBA_A[0..12] 30
FBA_A4
FBA_A5
FBA_A11
FBA_A12
FBA_A7
FBA_A10
FBA_A0
FBA_A9
FBA_A6
FBA_A2
FBA_A8
FBA_A3
FBA_A1

FBB_A[2..5] 30
FBB_A2
FBB_A4
FBB_A3
FBB_A5

FB_DLLAVDD0	AG27	
FB_PLLAVDD0	AF27	

200mA

C6042 22P_50V_J 0402_NPO
FB_PLLAVDD
C1371 1U_6.3V_M 0402_X5R
C5162 4.7U_6.3V_K 0603_X5R
L74 300R-100MHZ_0603 TB160808U301N001
PEX_VDD

Near GPU

Title	VGA(GDDR)# 3/9	
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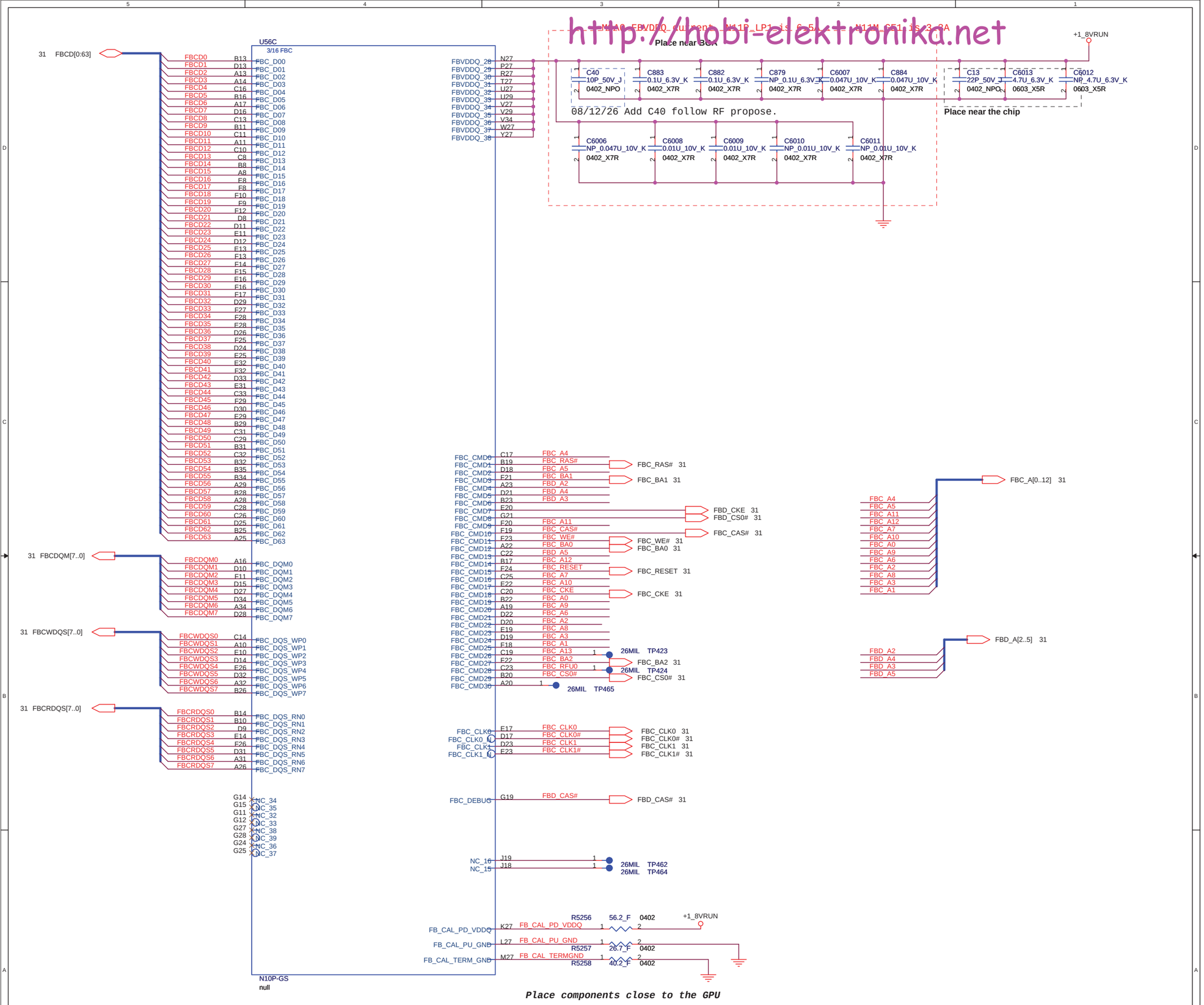

Place components close to the GPU

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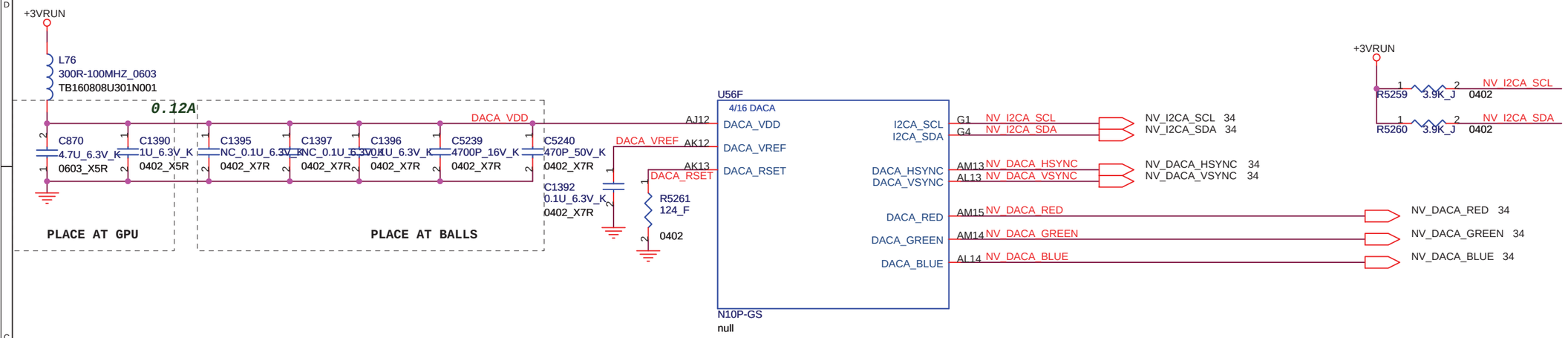
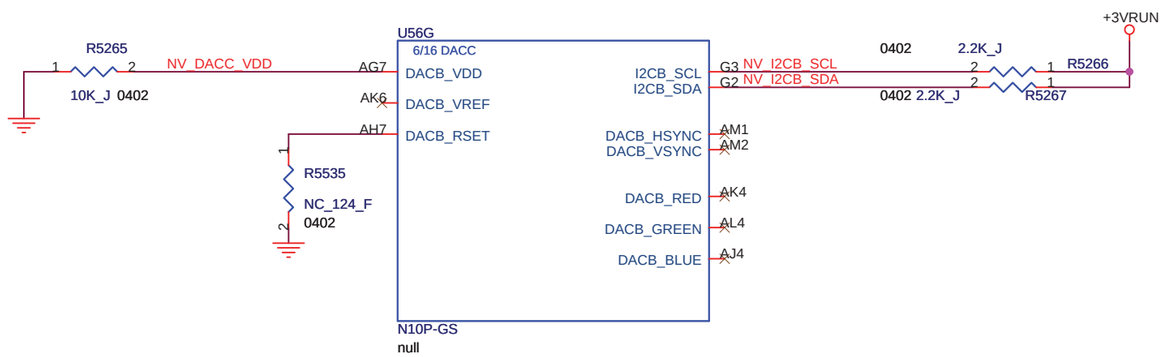
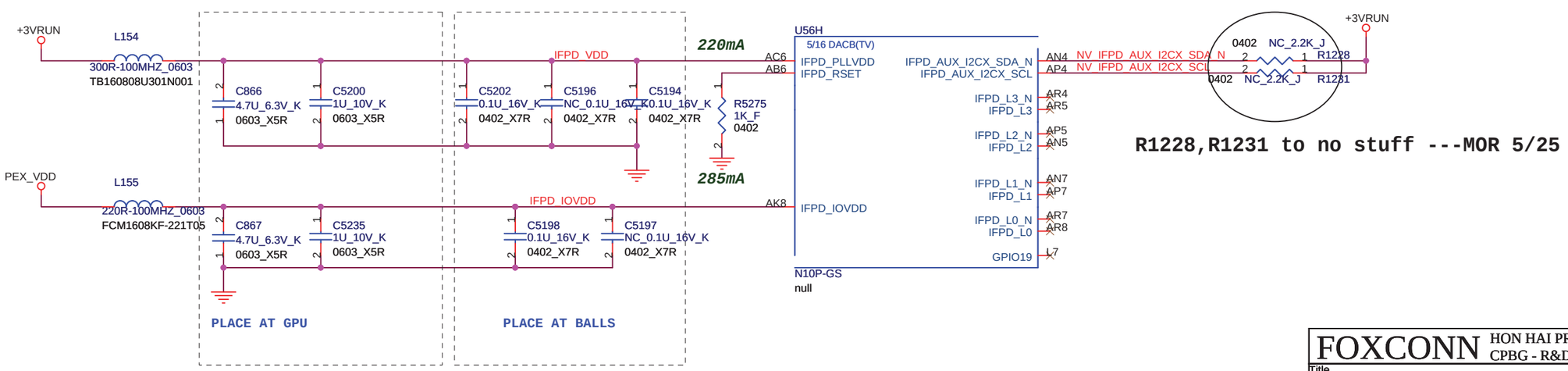




DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (CRT)5/9

Size: A3 | Document Number: M9A0_MP | Rev: 1.1

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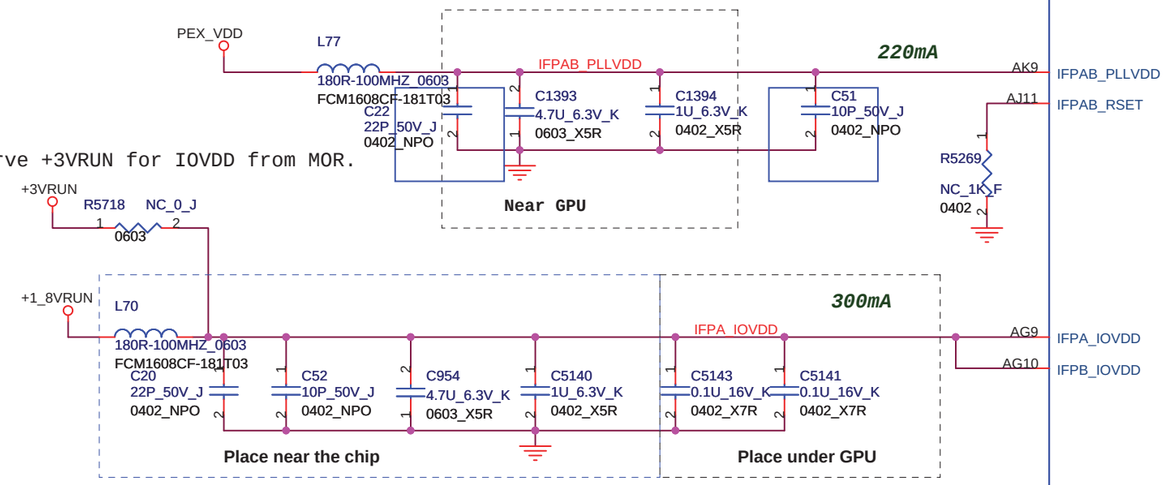
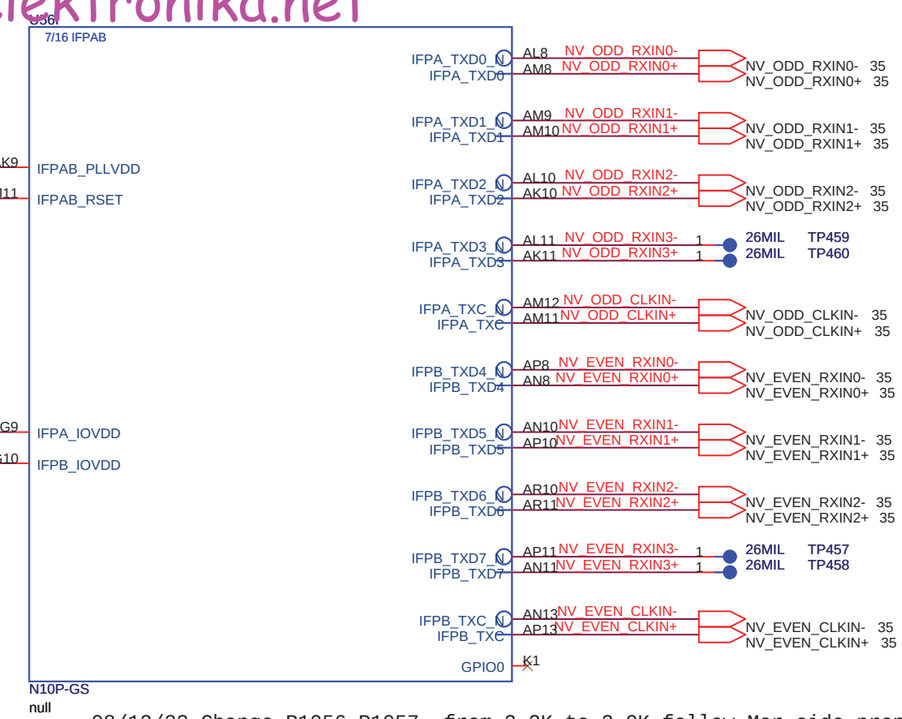
08/12/26 Add C51,C52 10p follow RF propose.

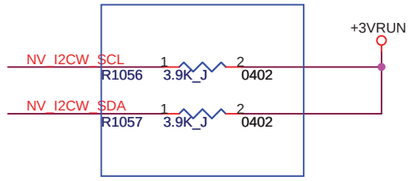
09/02/05 Reserve +3VRUN for IOVDD from MOR.

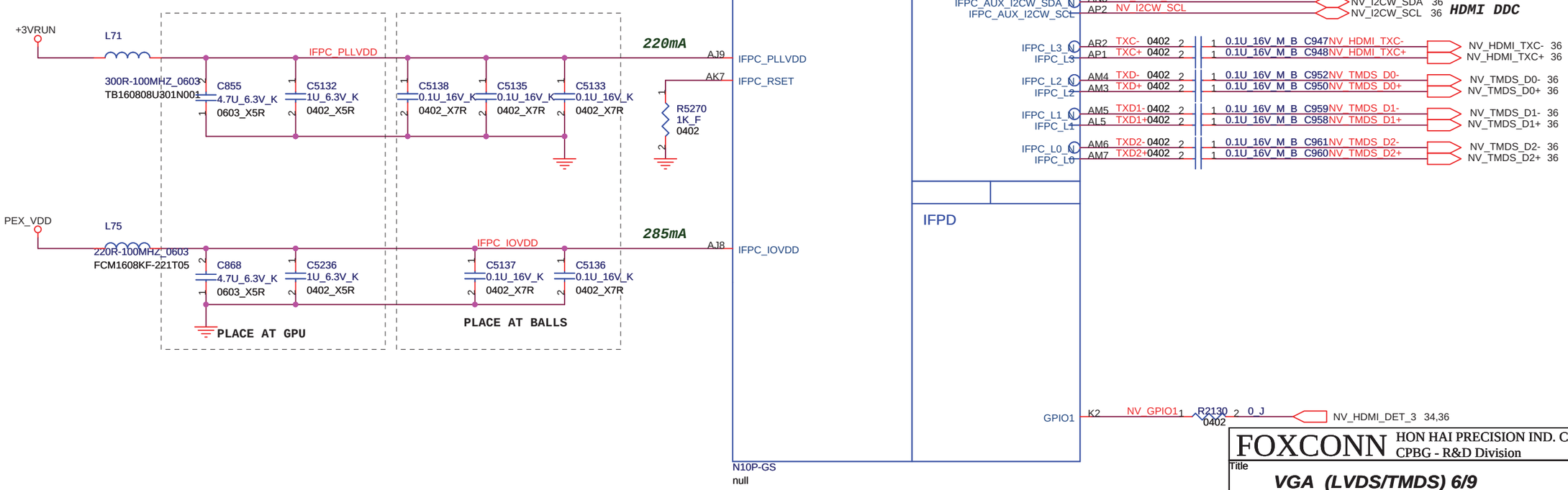
08/12/25 Add C20,C22 against 2.4GHz noise.





08/12/22 Change R1056,R1057 from 2.2K to 3.9K follow Mor-side propose.





FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA (LVDS/TMDS) 6/9	
Size A3	Document Number M9A0_MP	Rev 1.1
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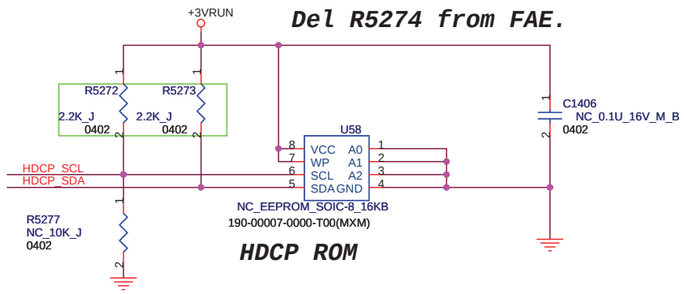
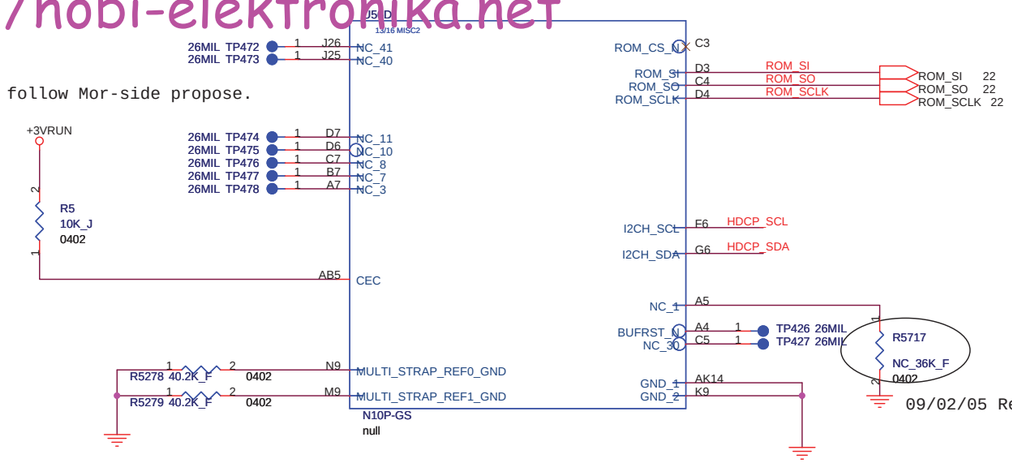
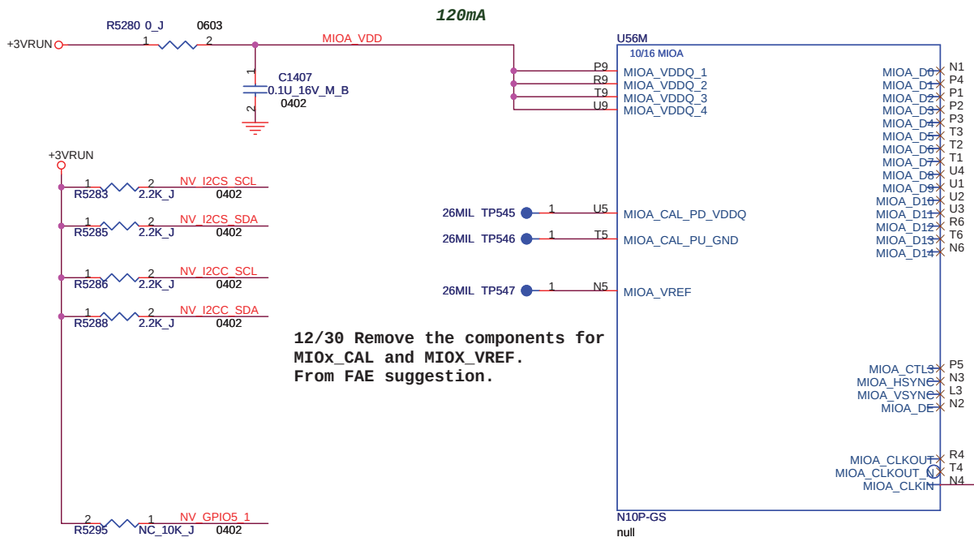


2009.0921
change R5272,R5273from NC to mount

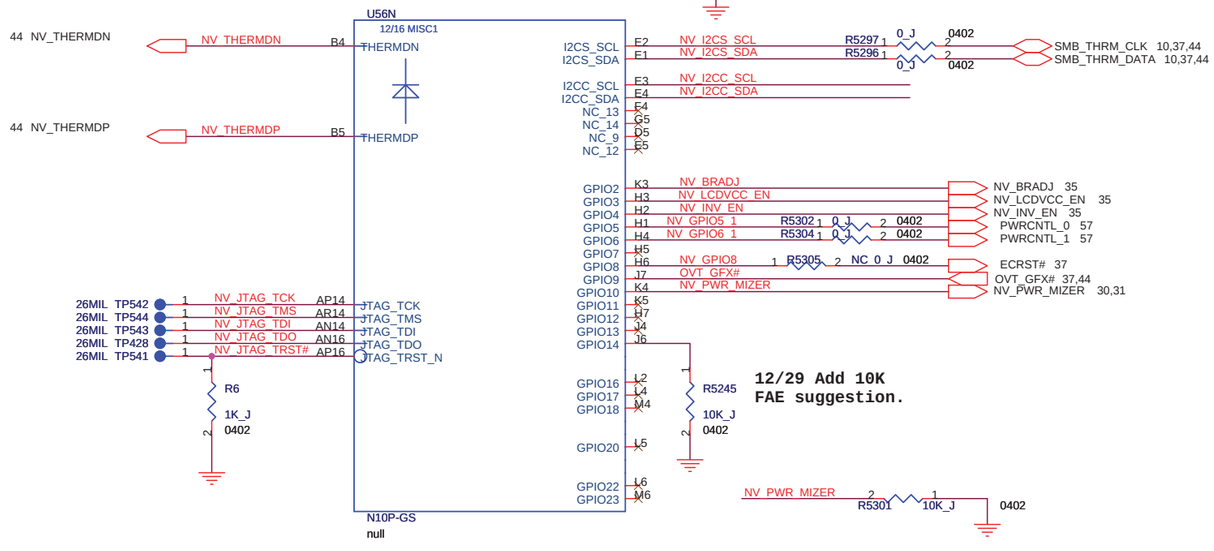
08/12/26 Add R5 follow Mor-side propose.



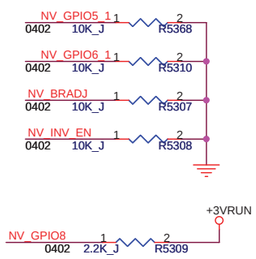
09/02/05 Reserve R5717 follow Mor-side propose.



12/30 Remove the components for
MIOx_CAL and MIOX_VREF.
From FAE suggestion.



12/29 Add R5310 10K
FAE suggestion.



12/29 Add 10K
FAE suggestion.

GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	YES		
GPIO1	I	Yes	HDMI Hot Plug Detect 0(HPD0)	**Active High**
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	**Active High**
GPIO3	O	No	Panel Power(LCD0_VDD)	**Active High**
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	**Active High**
GPIO5	O	Yes	FOR Power Control NVDD	
GPIO6	O	No	FOR Power Control NVDD	
GPIO8	O	No	reserve for reset EC	
GPIO9	I	No	System Power Limit Alert Input	**Active Low**

SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CS_SCL I2CS_SDA	I/O	For VGA thermial I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (XTAL/GPIO) 7/9

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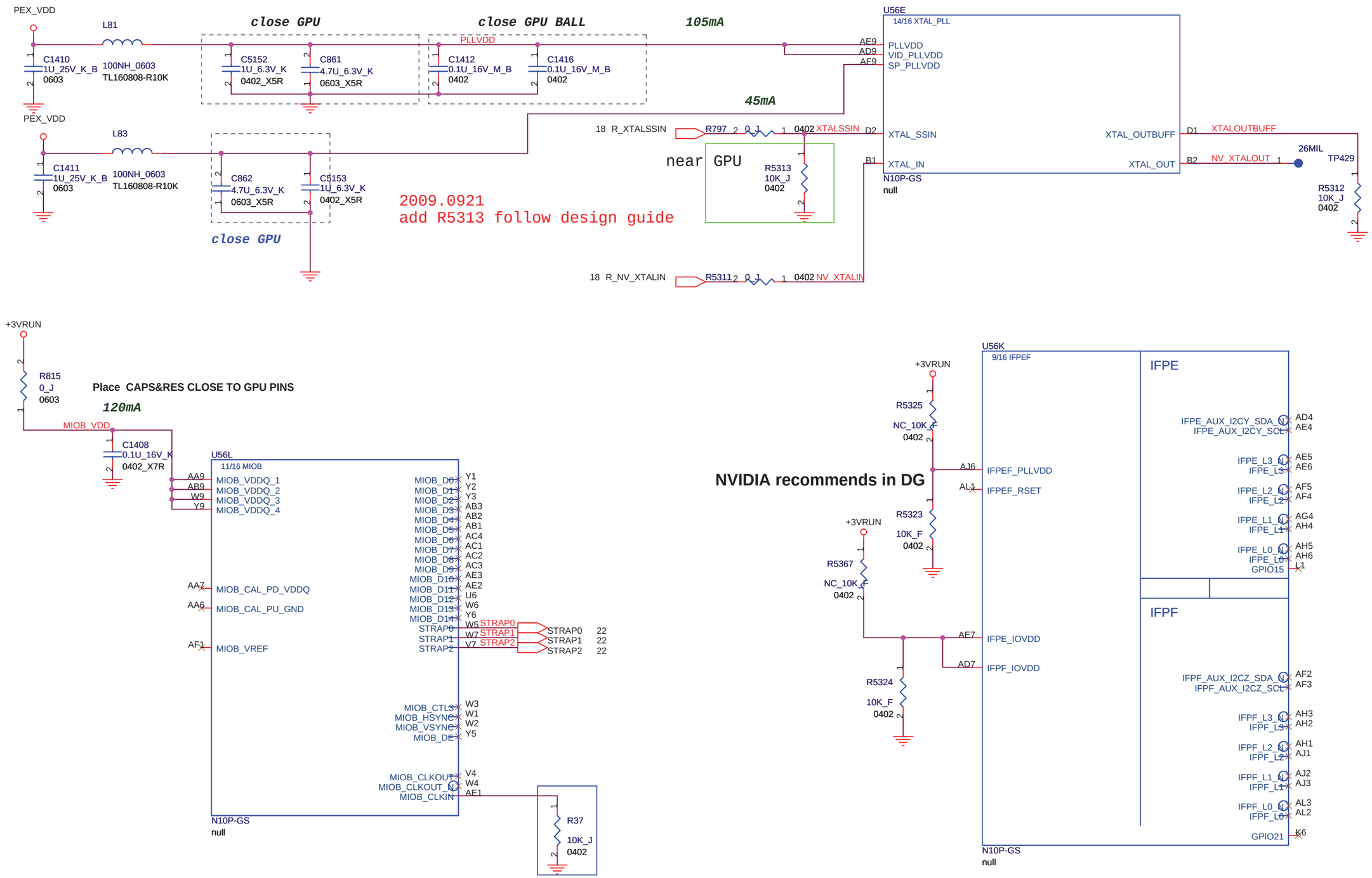

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA (INTER DISPLAY) 8/9	
Size A3	Document Number M9A0_MP	Rev 1.1
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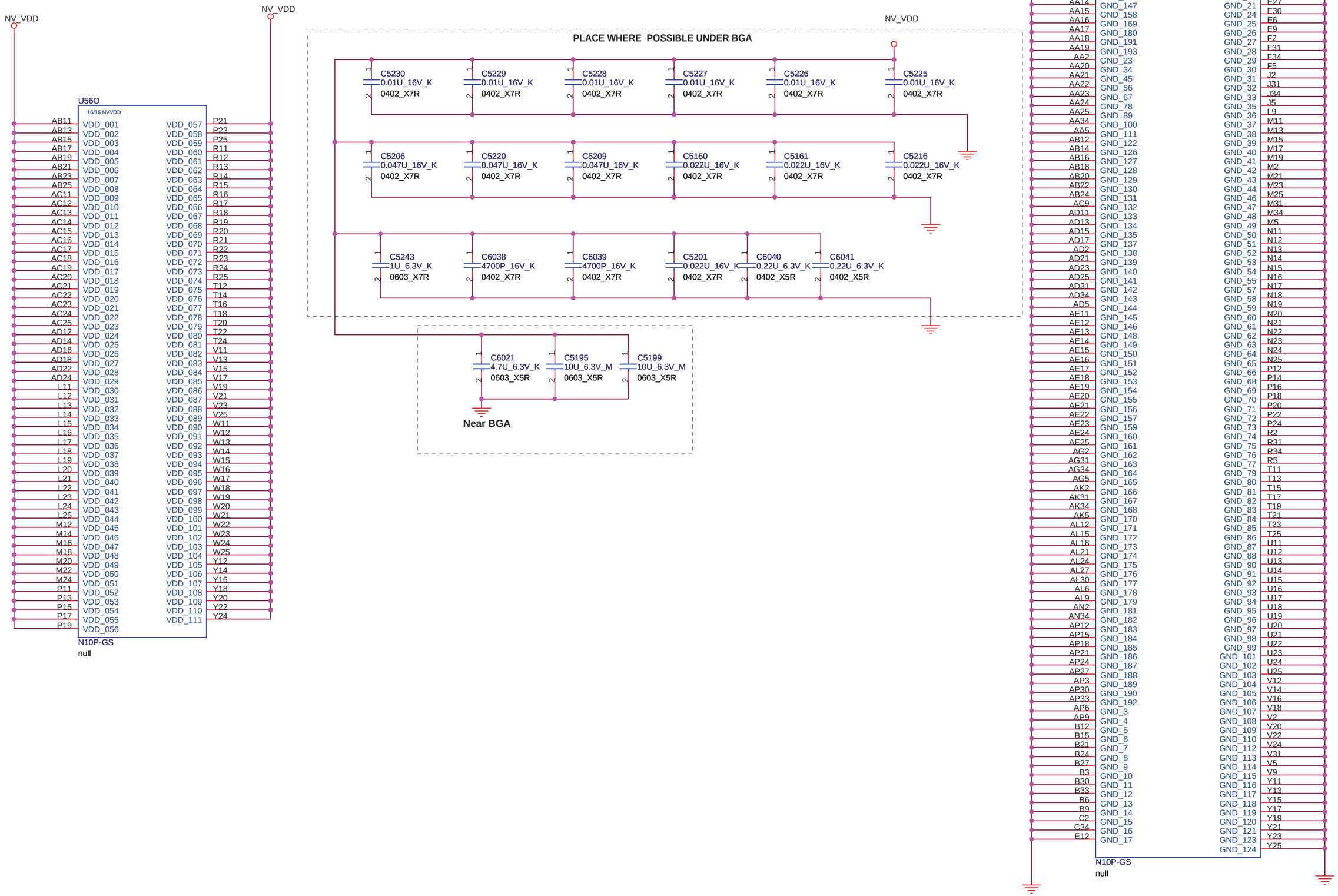
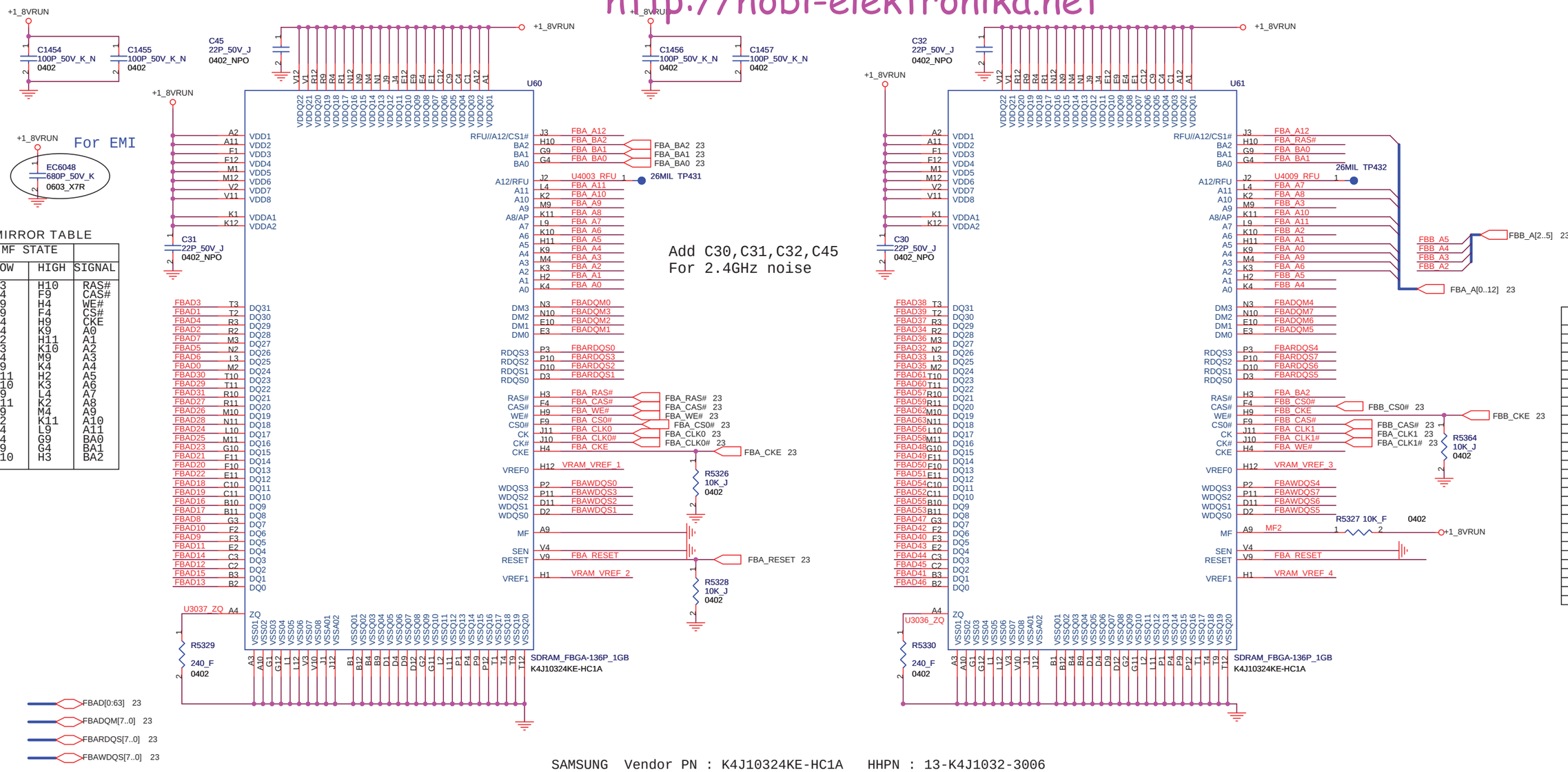
M9A0 NVVDD current N11P_LP1 is 21.94A N11M_GE1 is 16.29A



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA(POWER/GROUND) 9/9	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Tuesday, November 03, 2009	Sheet 29 of 73	



Add C30,C31,C32,C45
For 2.4GHz noise

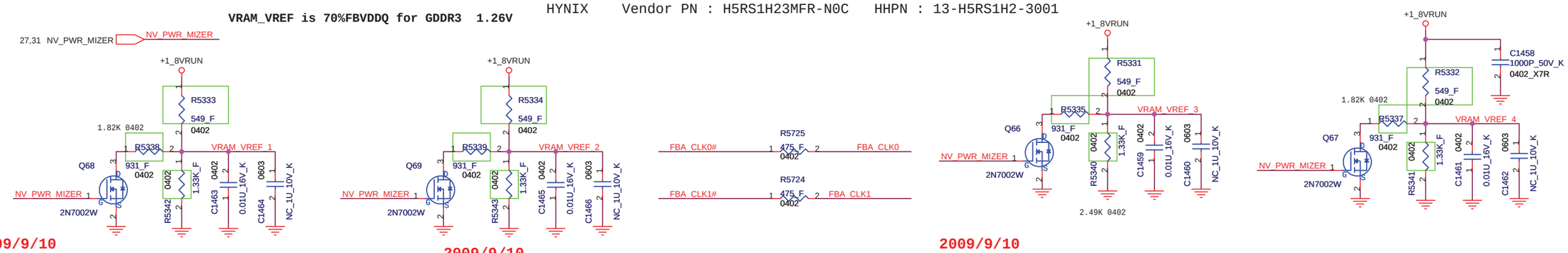
MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2

SAMSUNG Vendor PN : K4J10324KE-HC1A HHPN : 13-K4J1032-3006
HYNIX Vendor PN : H5RS1H23MFR-N0C HHPN : 13-H5RS1H2-3001

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V



2009/9/10
N11P-LP1+SAMSUNG(H2 SKU)
Change R5340,R5341,R5342,R5343 from
1R-0001331-F200(1.33K) to 1R-0000222-J200(2.2K)
for nVIDIA FAE suggest.

2009/9/10
N11P-LP1+SAMSUNG(H2 SKU)
Change R5331,R5332,R5333,R5334 from
1R-0005490-F200(549ohm) to 1R-0009310-F200(931ohm)
for nVIDIA FAE suggest.

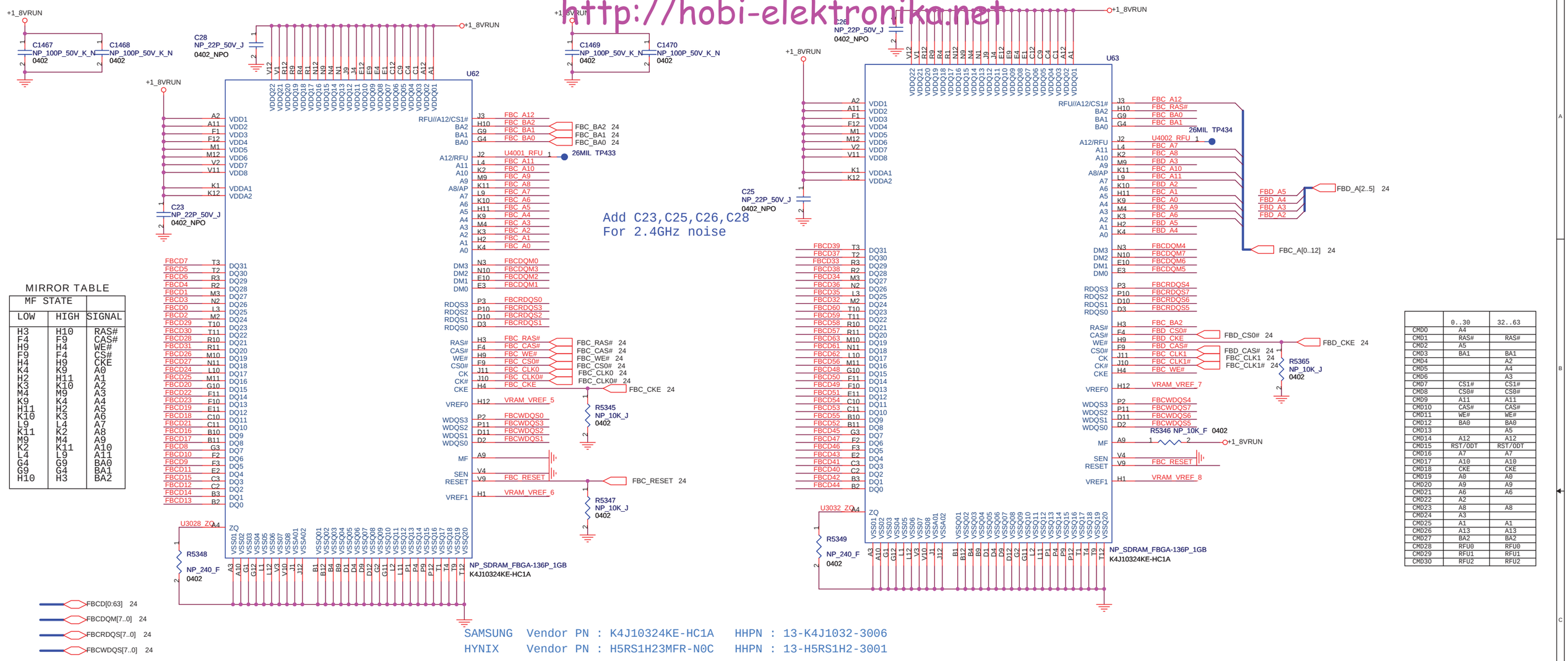
2009/9/10
N11P-LP1+SANSUNG(H2 SKU)
Change R5335,R5337,R5338,R5339 from
1R-0009310-F200(931ohm) to 1R-0000122-F200(1.2K)
for nVIDIA FAE suggest.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VRAM(GDDR)# 1/2

Size: Custom | Document Number: M9A0_MP | Rev: 1.1

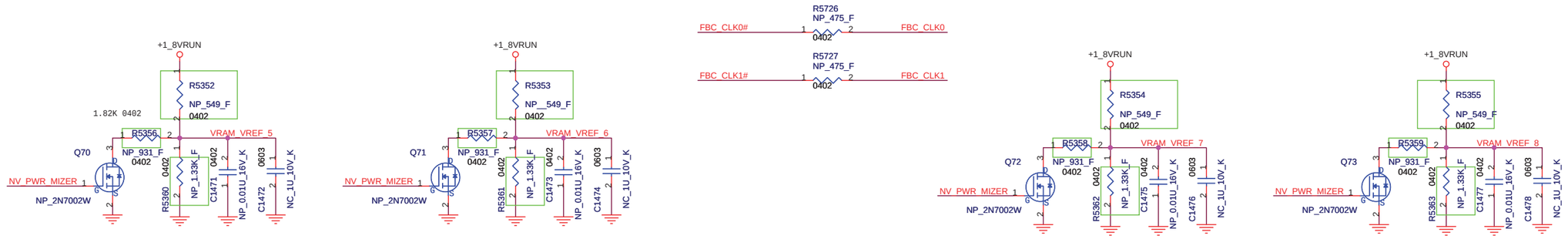
Date: Thursday, November 19, 2009 | Sheet 30 of 73



MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2



2009/9/10
N11P-LP1+SAMSUNG(H2 SKU)
Change R5356,R5357,R5358,R5359 from
1R-0009310-F200(931ohm) to 1R-0000122-F200(1.2K)
for nVIDIA FAE suggest.

2009/9/10
N11P-LP1+SAMSUNG(H2 SKU)
Change R5352,R5353,R5354,R5355 from
1R-0005490-F200(549ohm) to 1R-0009310-F200(931ohm)
for nVIDIA FAE suggest.

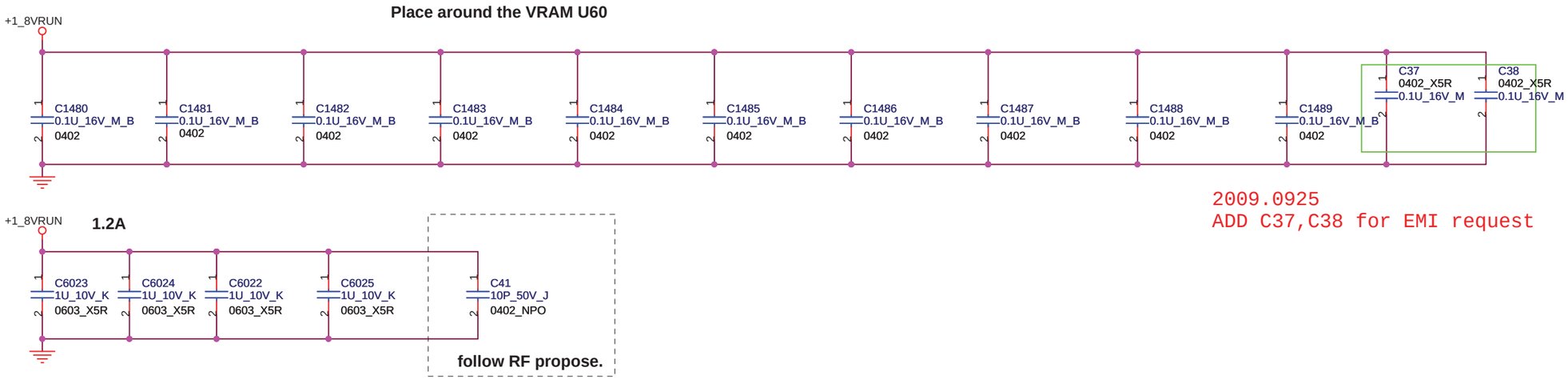
2009/9/10
N11P-LP1+SAMSUNG(H2 SKU)
Change R5360,R5361,R5362,R5363 from
1R-0001331-F200(1.33K) to 1R-0000222-J200(2.2K)
for nVIDIA FAE suggest.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

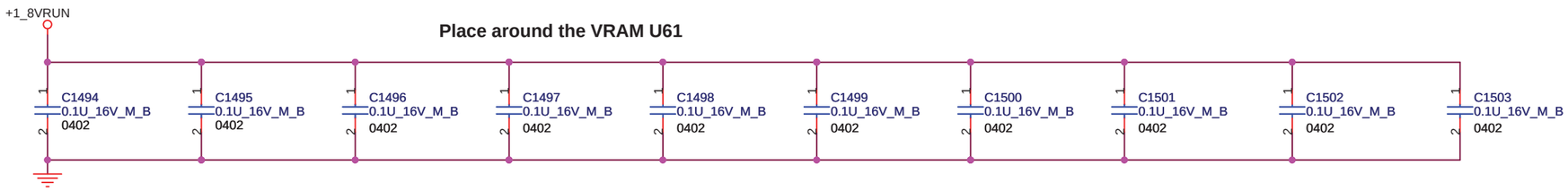
Title: VRAM(GDDR)# 2/2

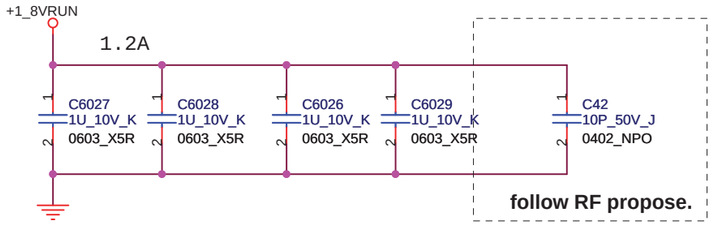
Size: Custom | Document Number: M9A0_MP | Rev: 1.1

Date: Thursday, November 19, 2009 | Sheet 31 of 73

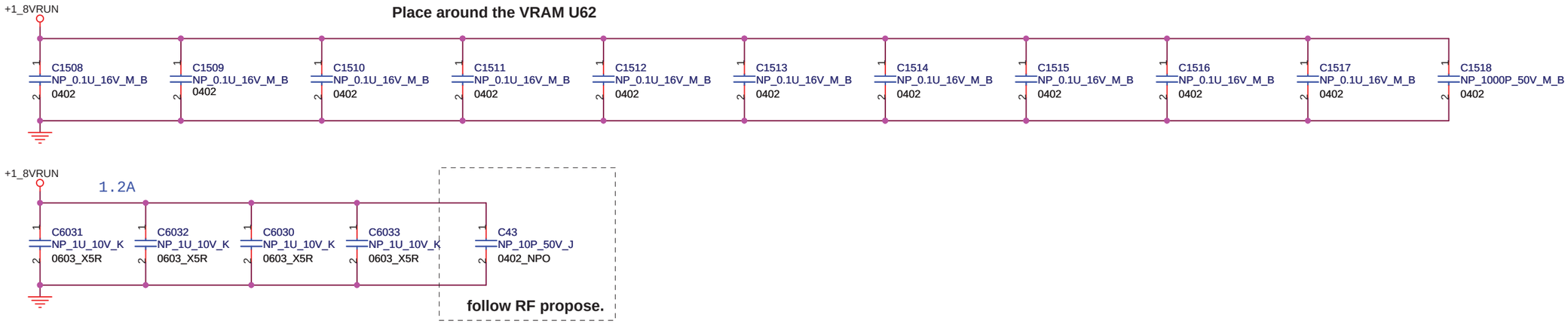


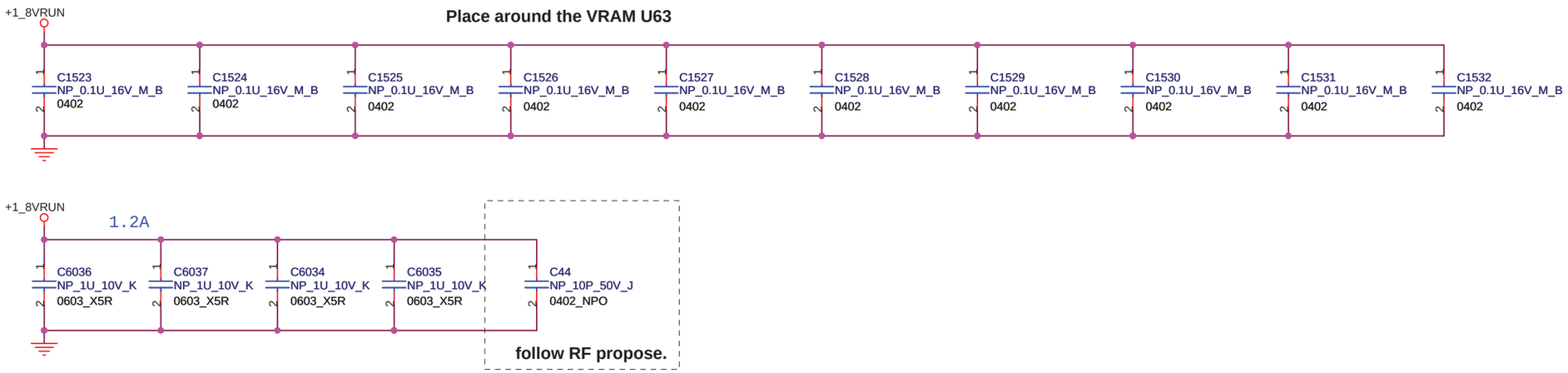
2009.0925
ADD C37,C38 for EMI request



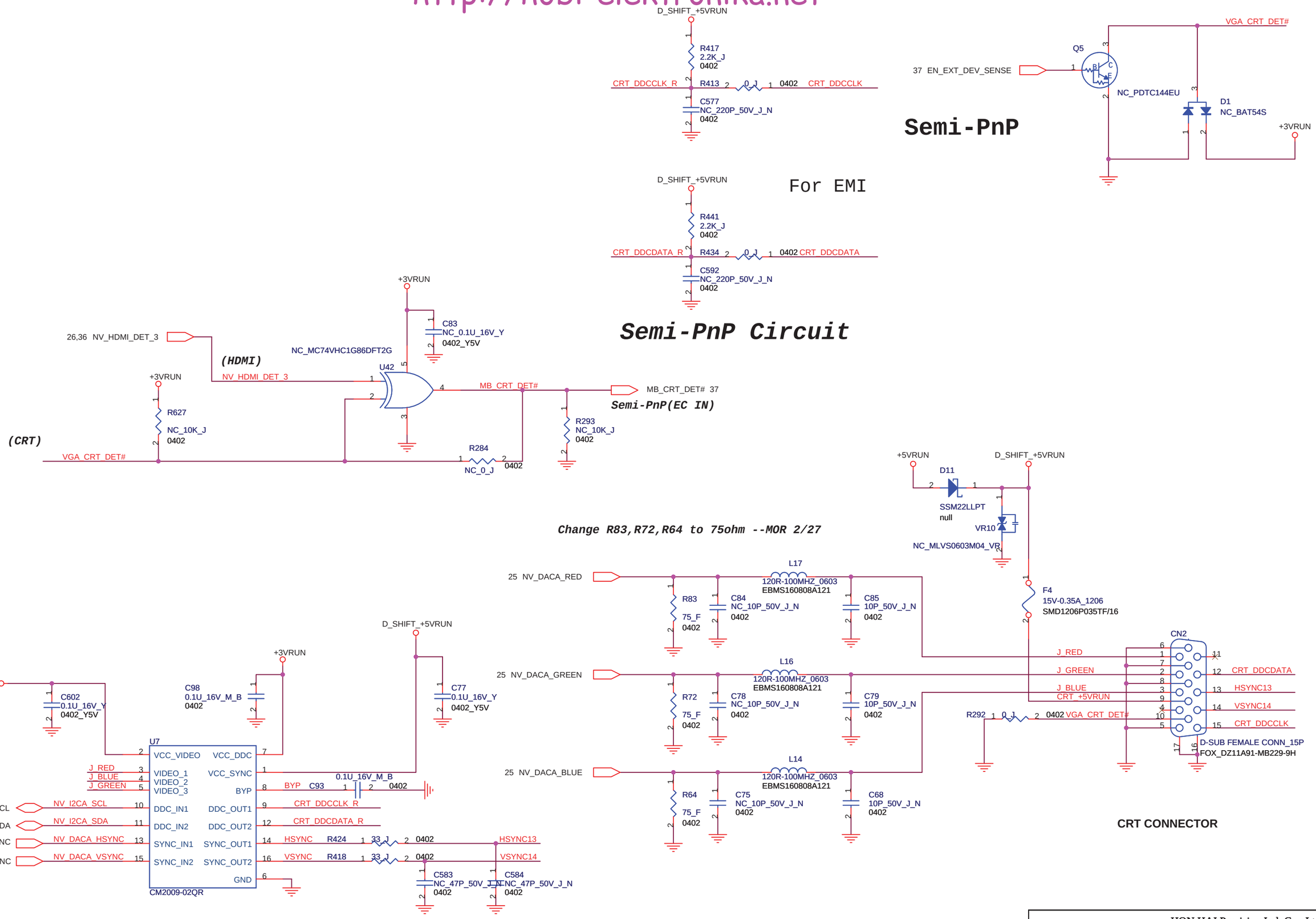


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM (POWERBYPASS) 1 OF 2	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Saturday, September 26, 2009	Sheet 32 of 73	





FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM (POWERBYPASS) 2 OF 2	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, November 20, 2009	Sheet 33 of 73	

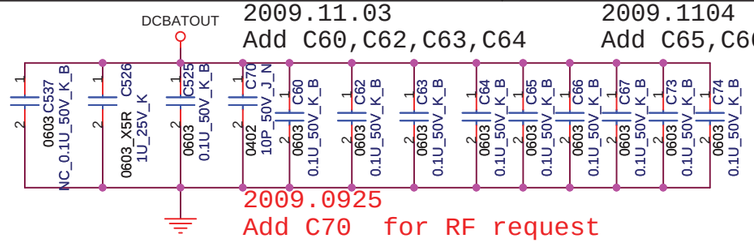


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CRT	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, October 29, 2009	Sheet 34 of 73	

LVDS CONNECTOR

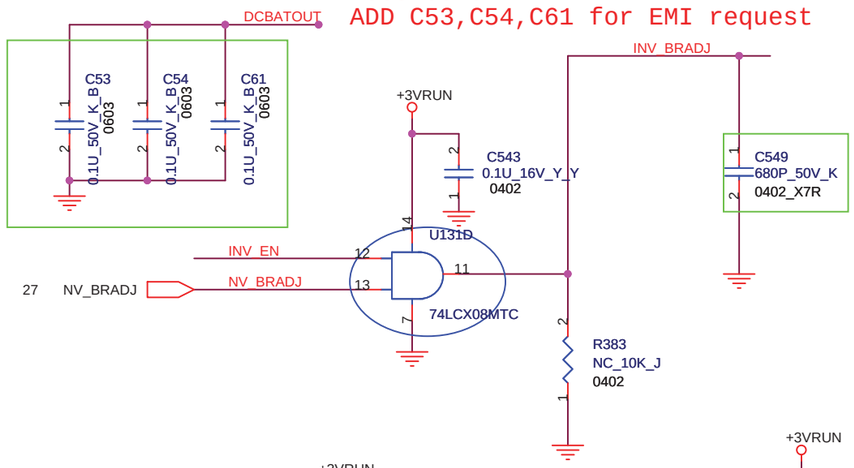
2009.11.03
Add C60,C62,C63,C64

2009.1104
Add C65,C66,C67,C73,C74 for FAN issue



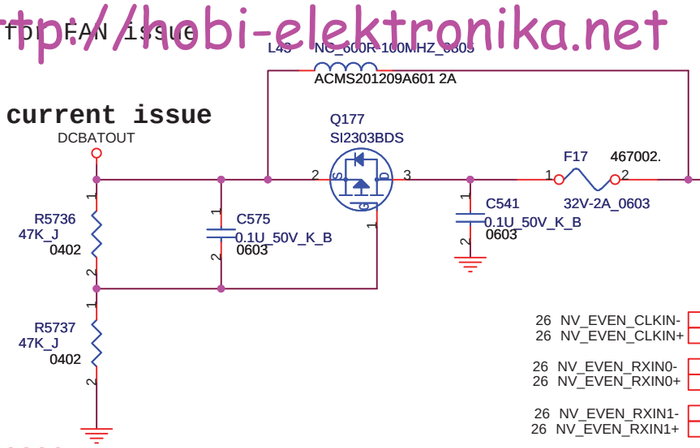
2009.0925
Add C70 for RF request

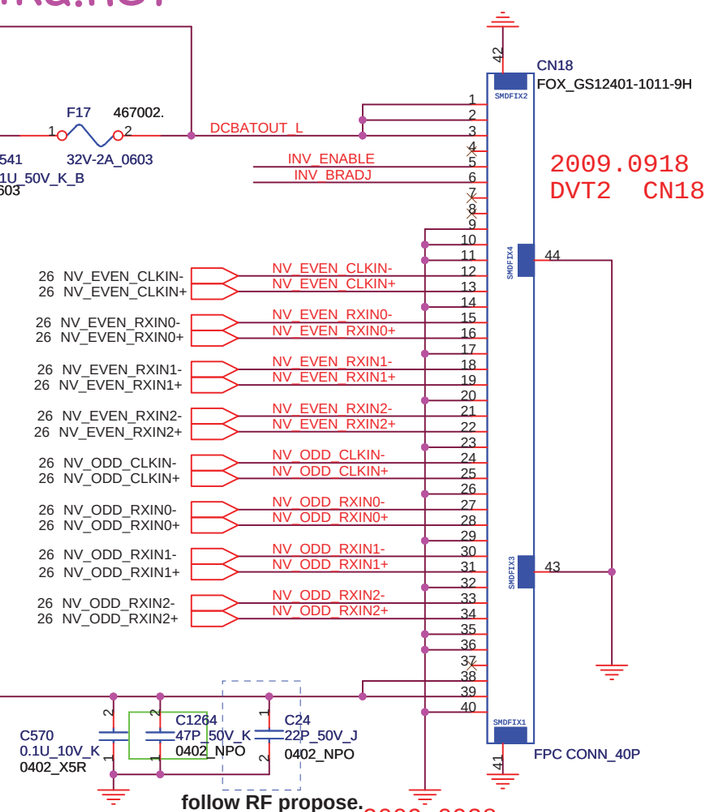
2009.0925
ADD C53,C54,C61 for EMI request



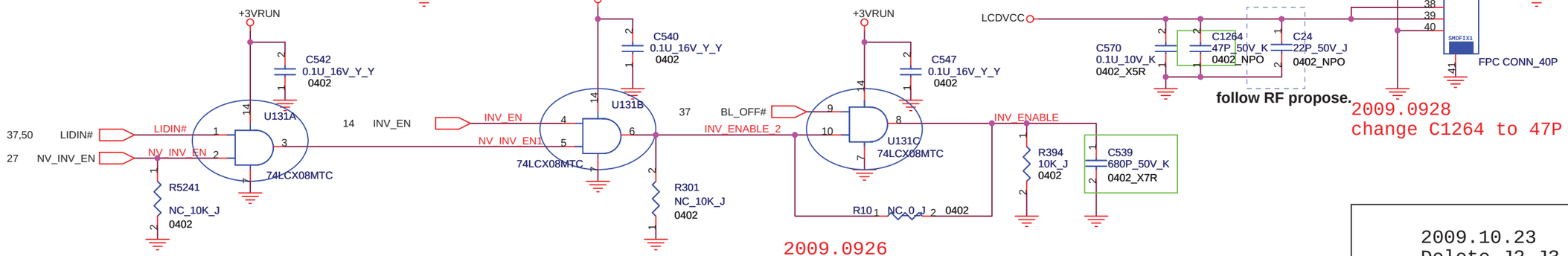
2009.0926
ADD C549 680P for EMI request
place it near LVDS connector

For rush current issue





2009.0918
DVT2 CN18 change to Halogen Free



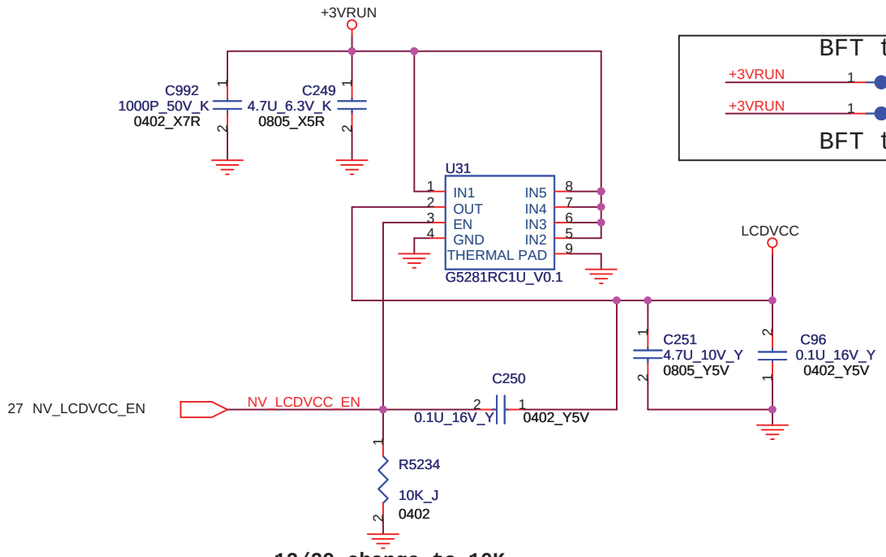
follow RF propose.

2009.0928
change C1264 to 47P for RF request

2009.0926
Change C539 TO 680P for EMI request

2009.10.23
Delete J2,J3

Current limit is from 1.1A to 2.1A.



12/29 change to 10K
FAE suggestion.

BFT test TOP

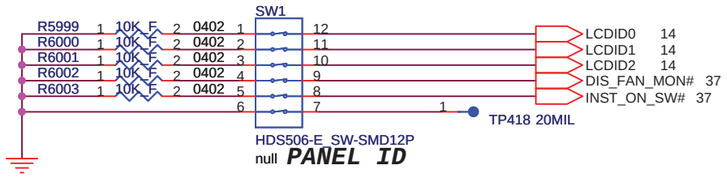
+3VRUN 1	TP900	tpc40b_75
+3VRUN 1	TP901	tpc40b_75

BFT test BOT

LCDID0 1	TP897	tpc40b_75
LCDID1 1	TP898	tpc40b_75
LCDID2 1	TP899	tpc40b_75

BFT test BOT

2009.10.23
Add test point TP897,TP898,TP899 ,
TP900,TP901 for PVT



PANEL ID

	DIS_FAN_MON#	LCDID2	LCDID1	LCDID0
	0	0	0	0
AUO B140XW02 V1	0	0	0	1
LGD LP140WH2-TLN1	0	0	1	0
SAMSUNG LTN140AT08	0	0	1	1
AUO B140RW02 V0	0	1	0	0
DISABLE FAN LOCK FUNCTION	0	X	X	X

ON:0 , OFF:1

LCDID0 1	TP892	tpc40b_75
LCDID1 1	TP893	tpc40b_75
LCDID2 1	TP894	tpc40b_75
DIS_FAN_MON# 1	TP895	tpc40b_75
INST_ON_SW# 1	TP896	tpc40b_75

BFT Test TOP

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: LVDS
Size: A3
Document Number: M9A0_MP
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Date: Wednesday, November 04, 2009
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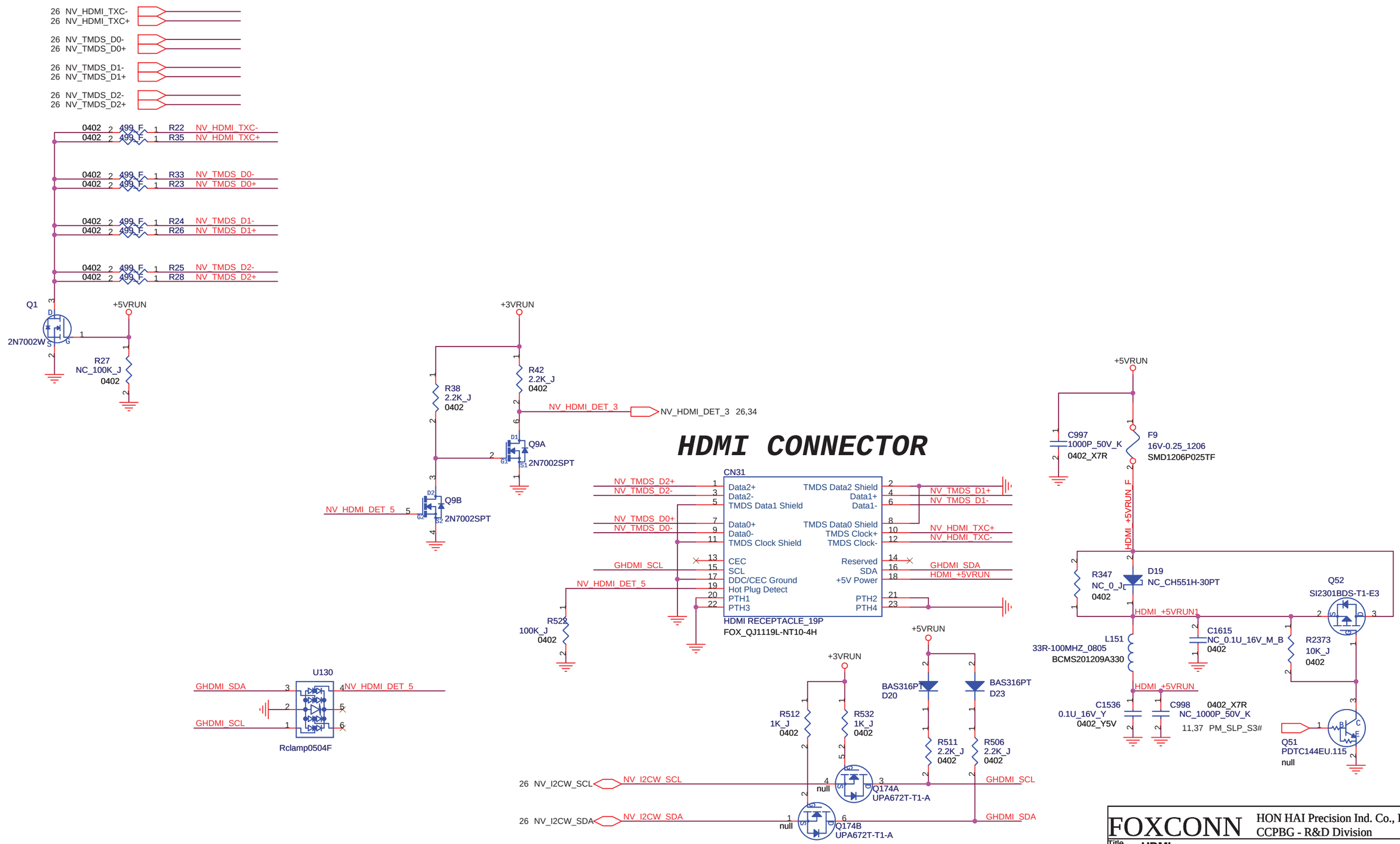
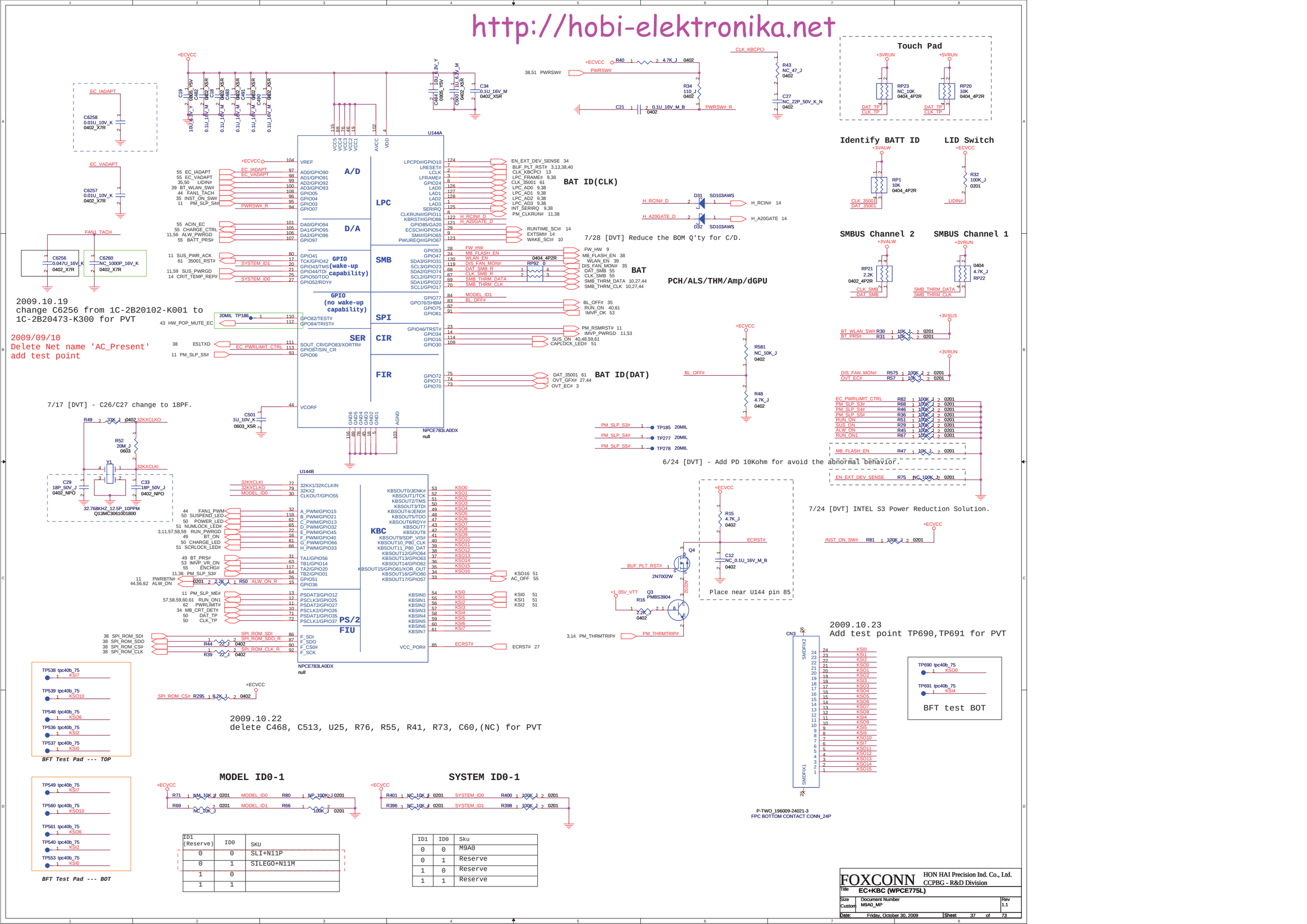
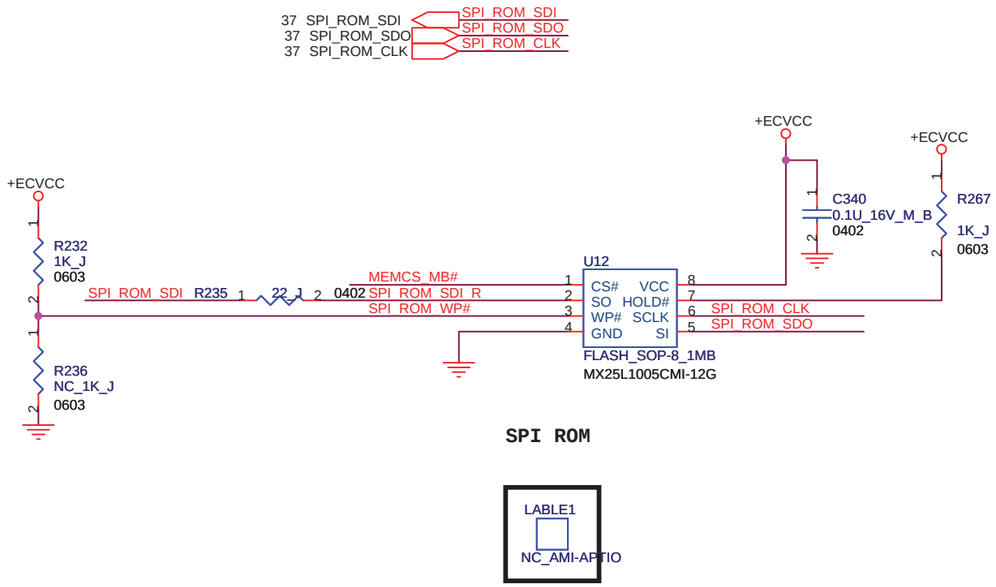
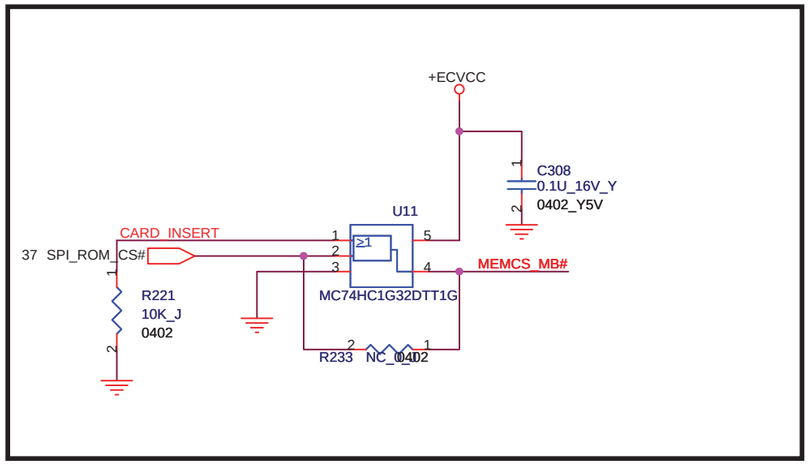


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HDMI	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 30, 2009	Sheet 36 of 73	

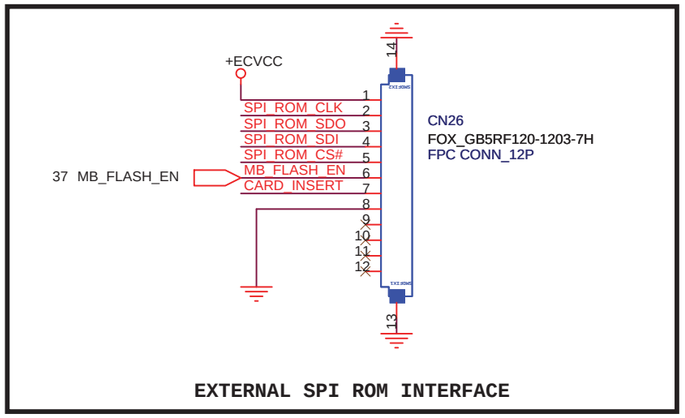




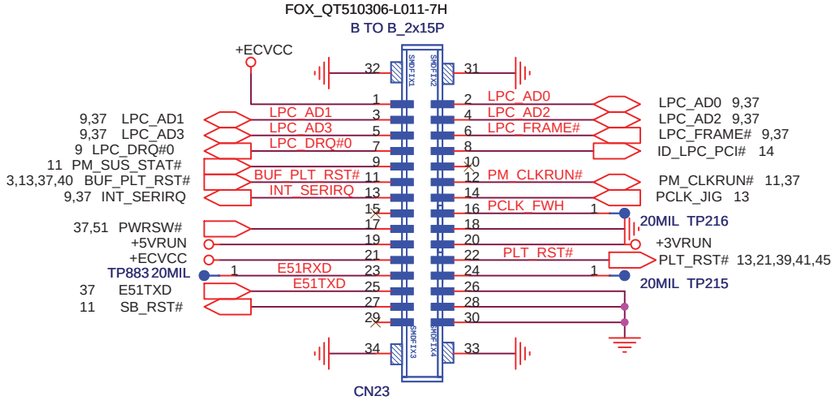
SPI ROM



2009.10.23
Delete TP531,TP530,TP532,TP533,TP529,TP520,519,TP518



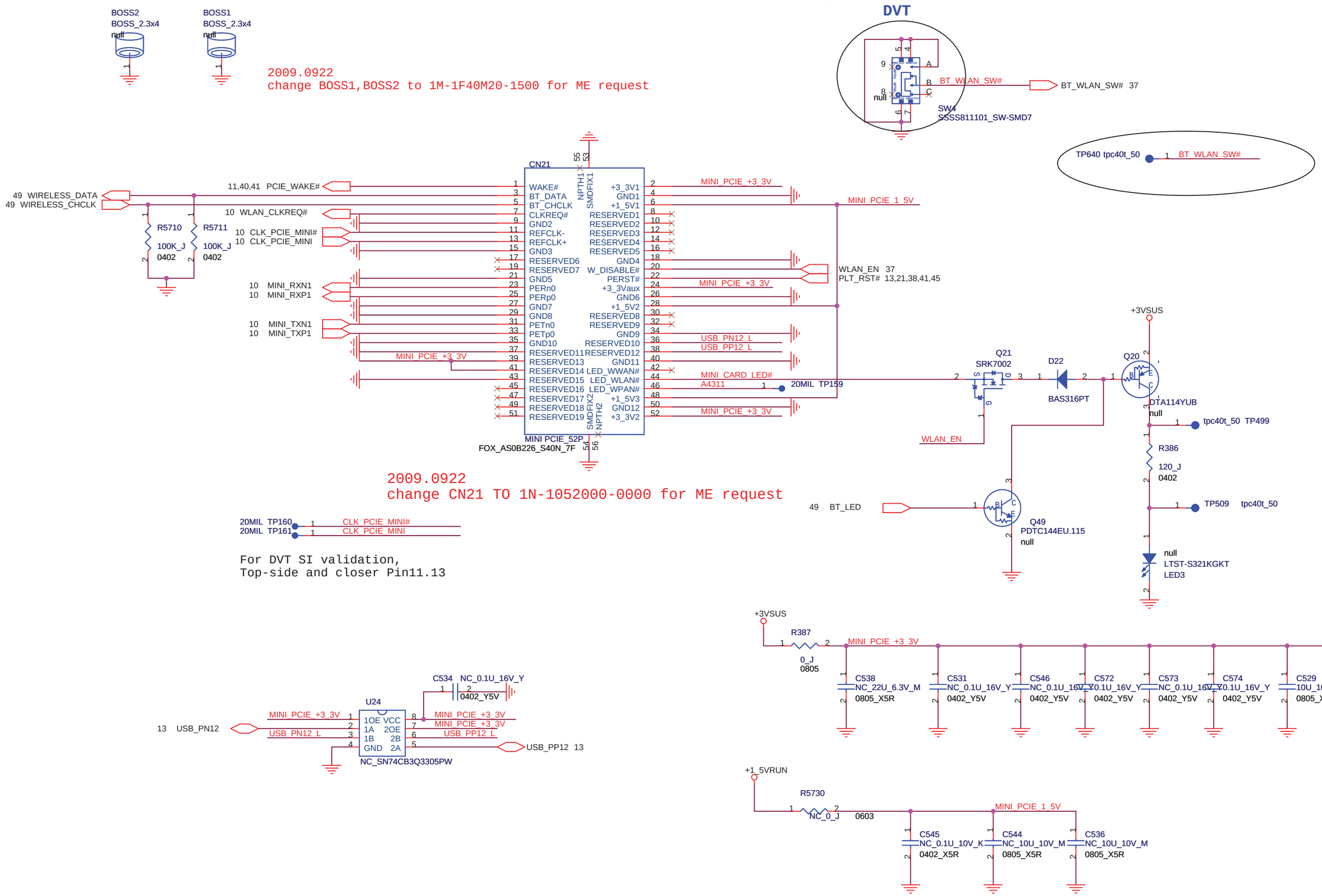
EXTERNAL SPI ROM INTERFACE



JIG-120

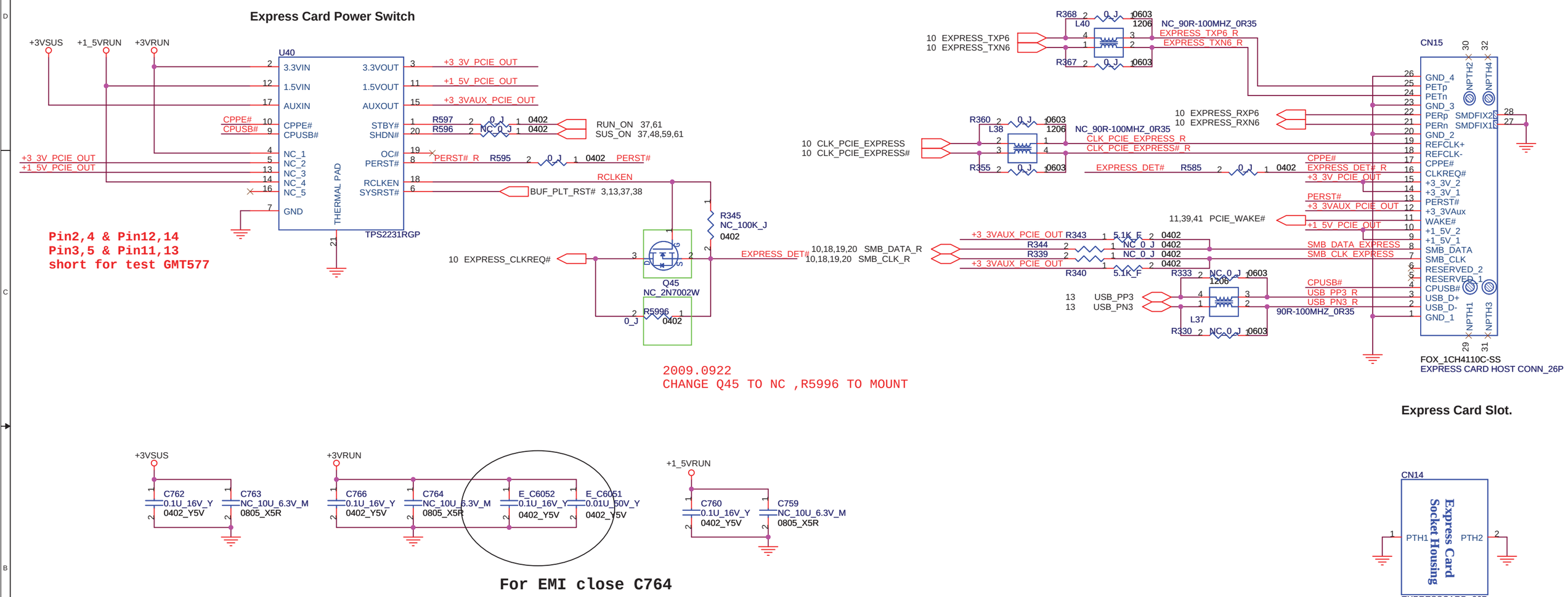
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Flash ROM/SPI	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 38 of 73	

SW4.C pin delete and SW4.A connect to GND.



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

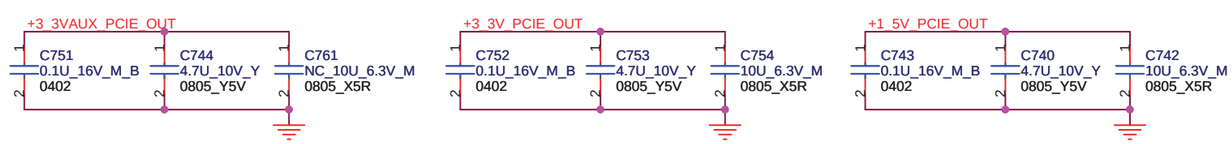
Title	Half Mini Card	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 39 of 73	

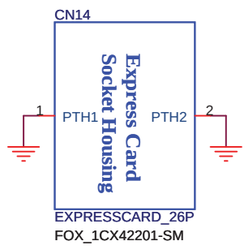


2009.0922
CHANGE Q45 TO NC ,R5996 TO MOUNT

Express Card Slot.

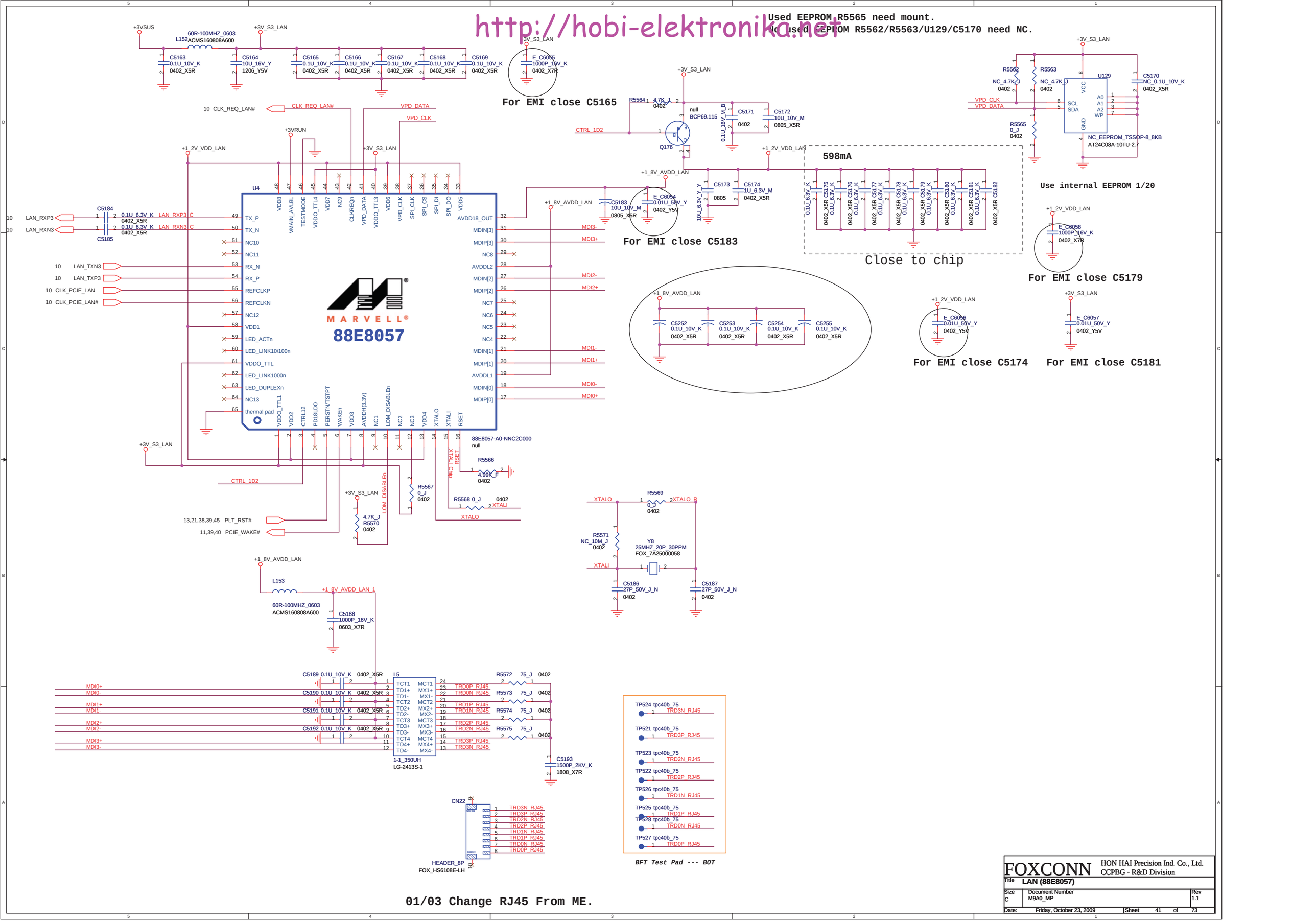
For EMI close C764





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	EXPRESS CARD	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 40 of 73	

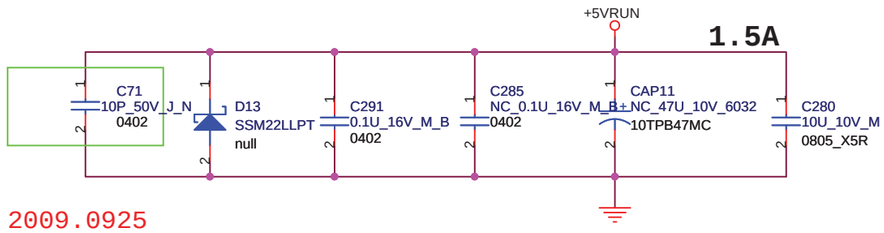
Used EEPROM R5565 need mount.
No used EEPROM R5562/R5563/U129/C5170 need NC.



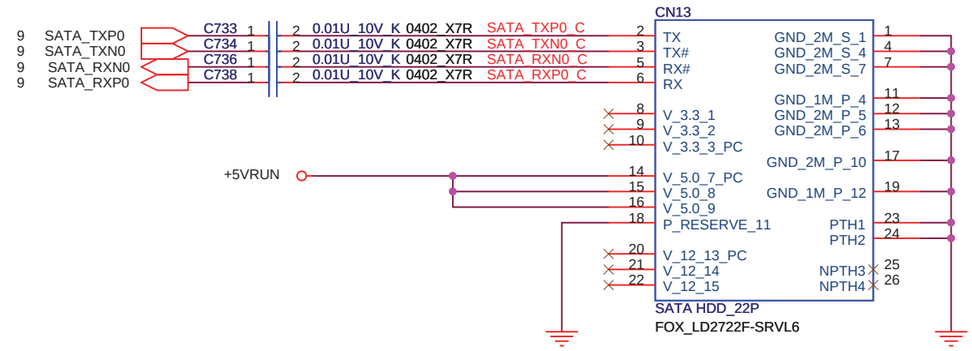
01/03 Change RJ45 From ME.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	LAN (88E8057)
Size C	Document Number M9A0_MP
Rev	1.1
Date: Friday, October 23, 2009	Sheet 41 of 73

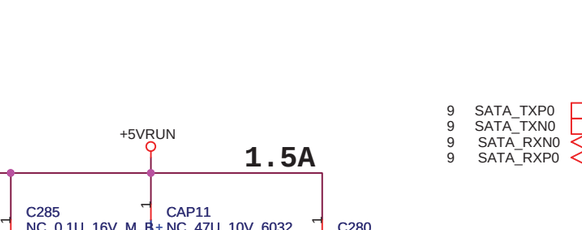
SATA HDD CONN



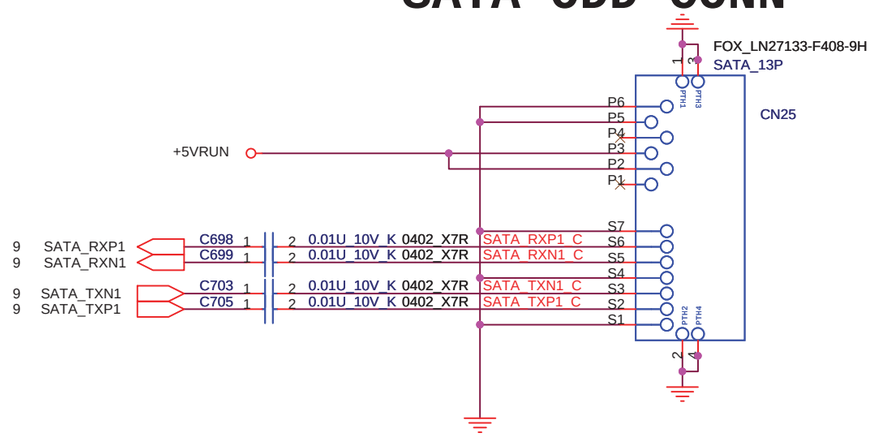
2009.0925
Add C71 for RF request



SATA ODD CONN

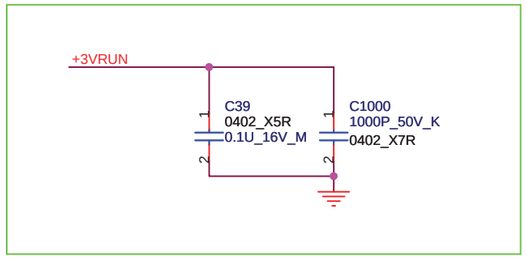


Co-layout

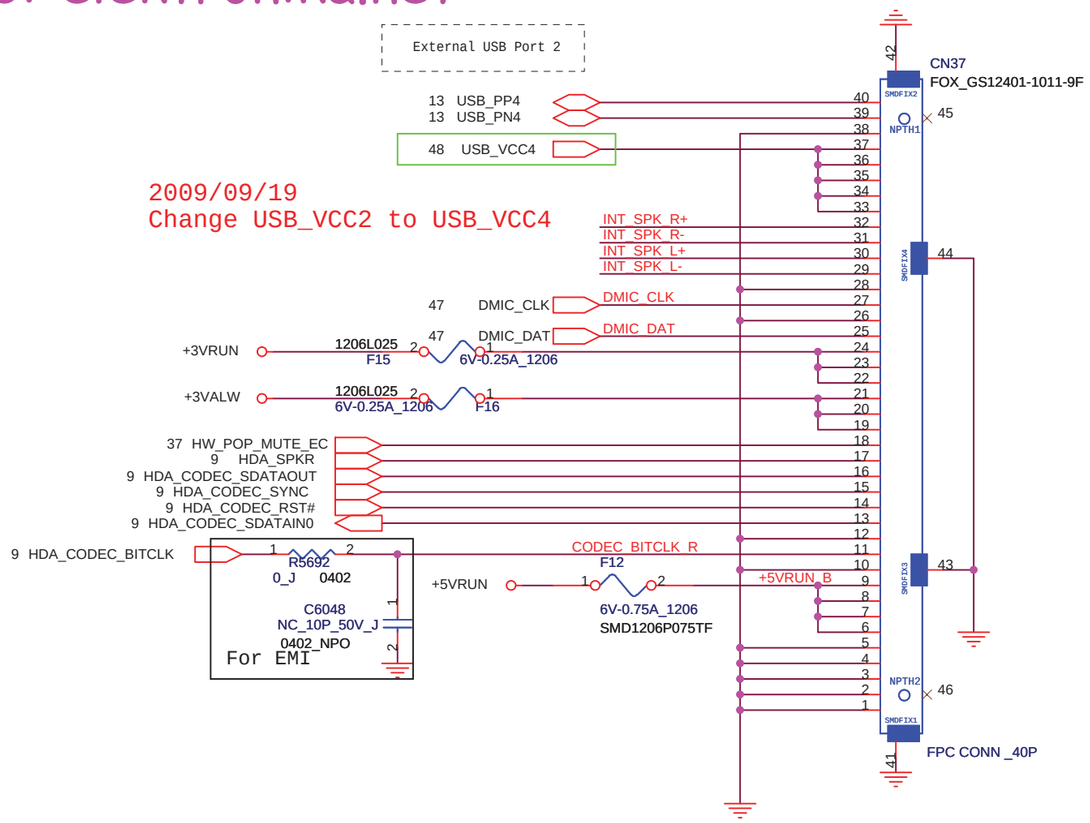


2009.0922
CN25 change to Halogen Free

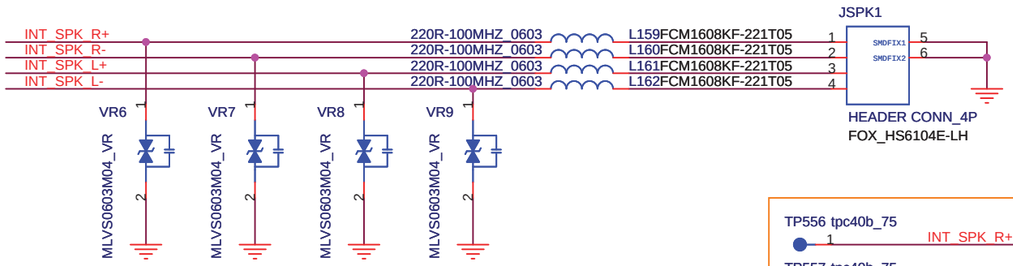
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SATA HDD/ODD	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, October 28, 2009	Sheet 42 of 73	

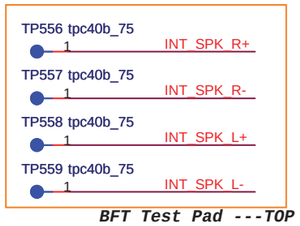


2009.0925
ADD for EMI request



INTERNAL SPEAKER

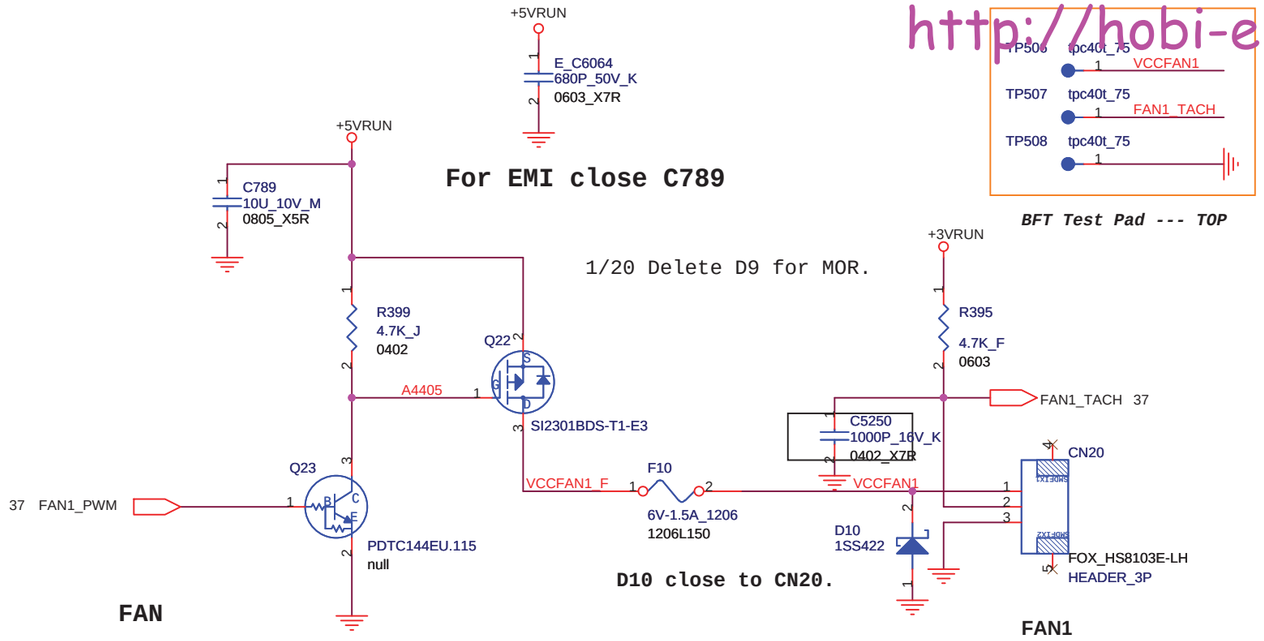




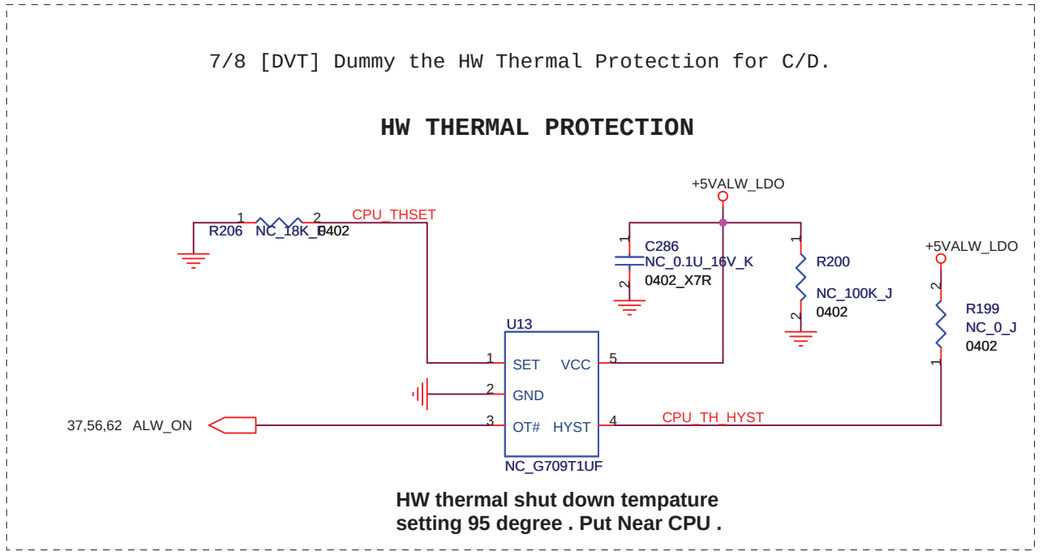
BFT Test Pad ---TOP

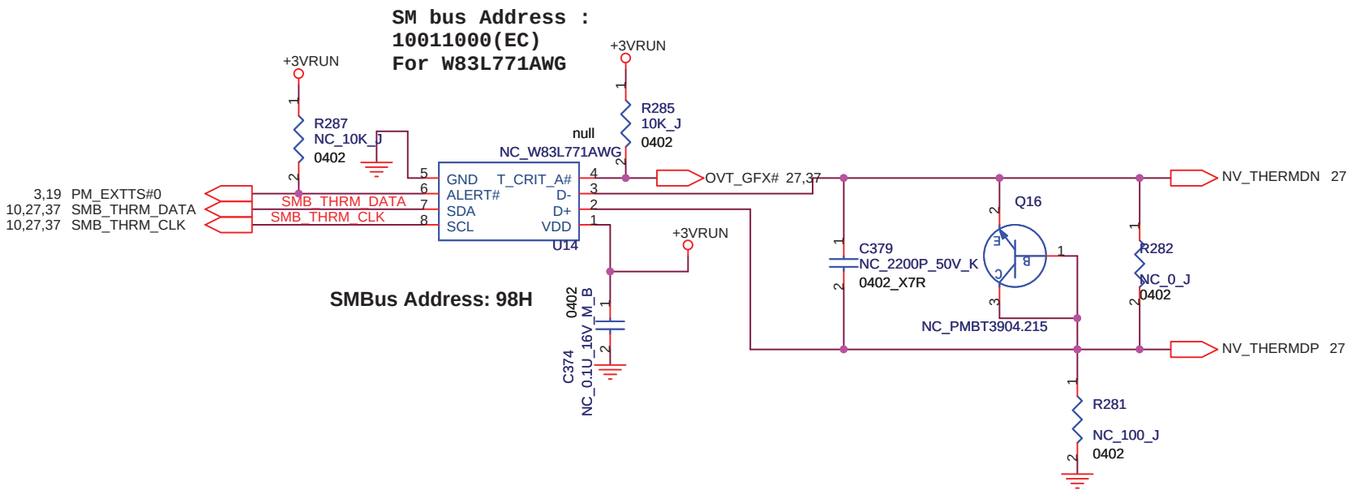
Audio & USB WTB CONN.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	**BTB CONN**	
Size A3	Document Number **M9A0_MP**	Rev **1.1**
Date: Wednesday, November 04, 2009	Sheet 43 of 73	



2009.10.19
change C5250 from 1C-2B20473-K300 to
1C-2B20102-K001 for PVT





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	FAN/Thermal	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 44 of 73	

01/20 Add pin headers and resistors for PCIe protocol measurement for R5U231.

Delete parts for R5U231 protocol measurement.

C496 22P_50V_J 0402_NPO
C497 27P_50V_J_N 0402
Y3 24.576MHZ_16P_30PPM ITTI_L5030-24.576-16
XIN XOUT_R XOUT
R605 0_J 0402
R604 NC_10M_J 0402

MFIO14 R5691 0_J 0402 MS_CLK

U21 R5U231 null

Close to U21

Change CN35 From ME request.

Close to U21

CN35 SOCKET_14P YAMAICHI_JES014-2000-1

2009.0921
ADD R5991 follow design guide
change C476 TO NC_12P

2009.10.19
change R5703 from 68ohm to 75ohm for PVT

2009/09/10
Add test point for for L6 TE request

TP512 tpc40b_75 TPB-
TP513 tpc40b_75 TPB+
TP514 tpc40b_75 TPA-
TP515 tpc40b_75 TPA+

BFT TEST PAD _BOT

CN11 IEEE 1394 AV CONN_4P FOX_UV31413-WU82P-7H

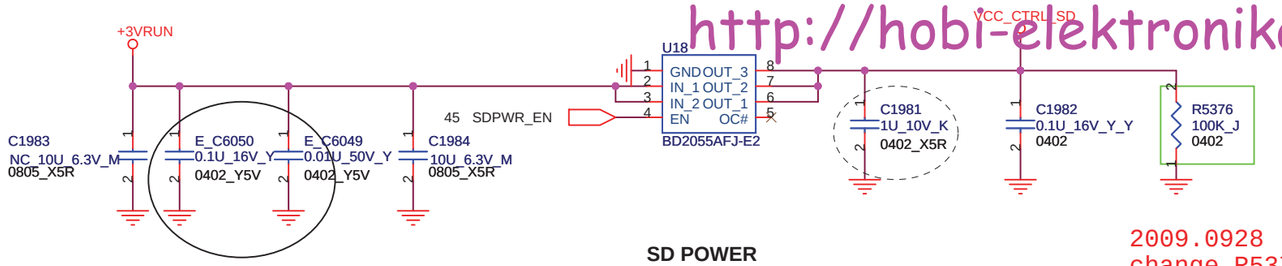
2009.0918
DVT2 CN11 change to Halogen Free

U20 EEPROM_SOP-8_256x8 HT24LC02

SROM: UDIO1
Pull-Hi: Disable
Pull-Lo: Enable (Default)

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title	PCIE (PCIE BUS) 1/2		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Thursday, October 29, 2009	Sheet 45 of 73		



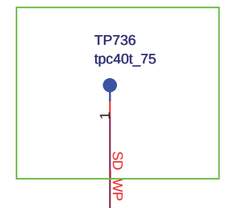
For EMI close C1983

SD POWER

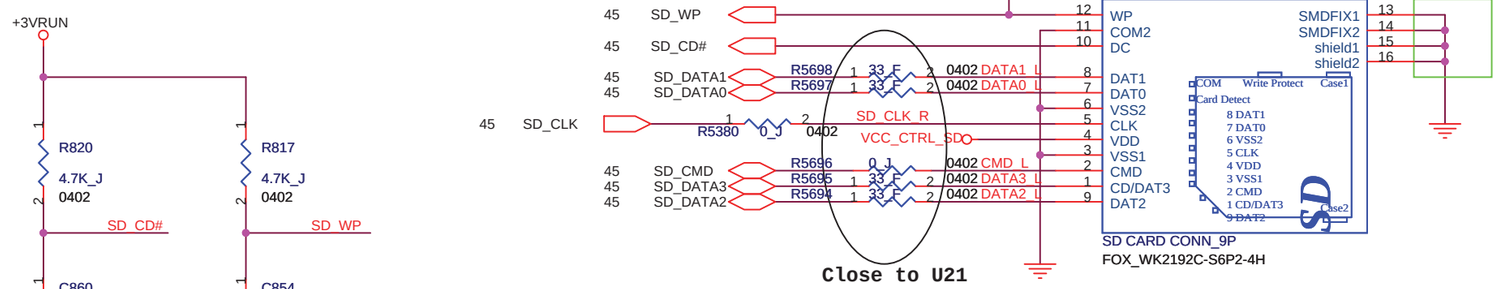
2009.0928
change R5376 to 100K follow design guide

2009/09/10
Add test point for L6 TE request

BFT TEST PAD_ TOP



2009.10.23
change net SD_WP# to SD_WP



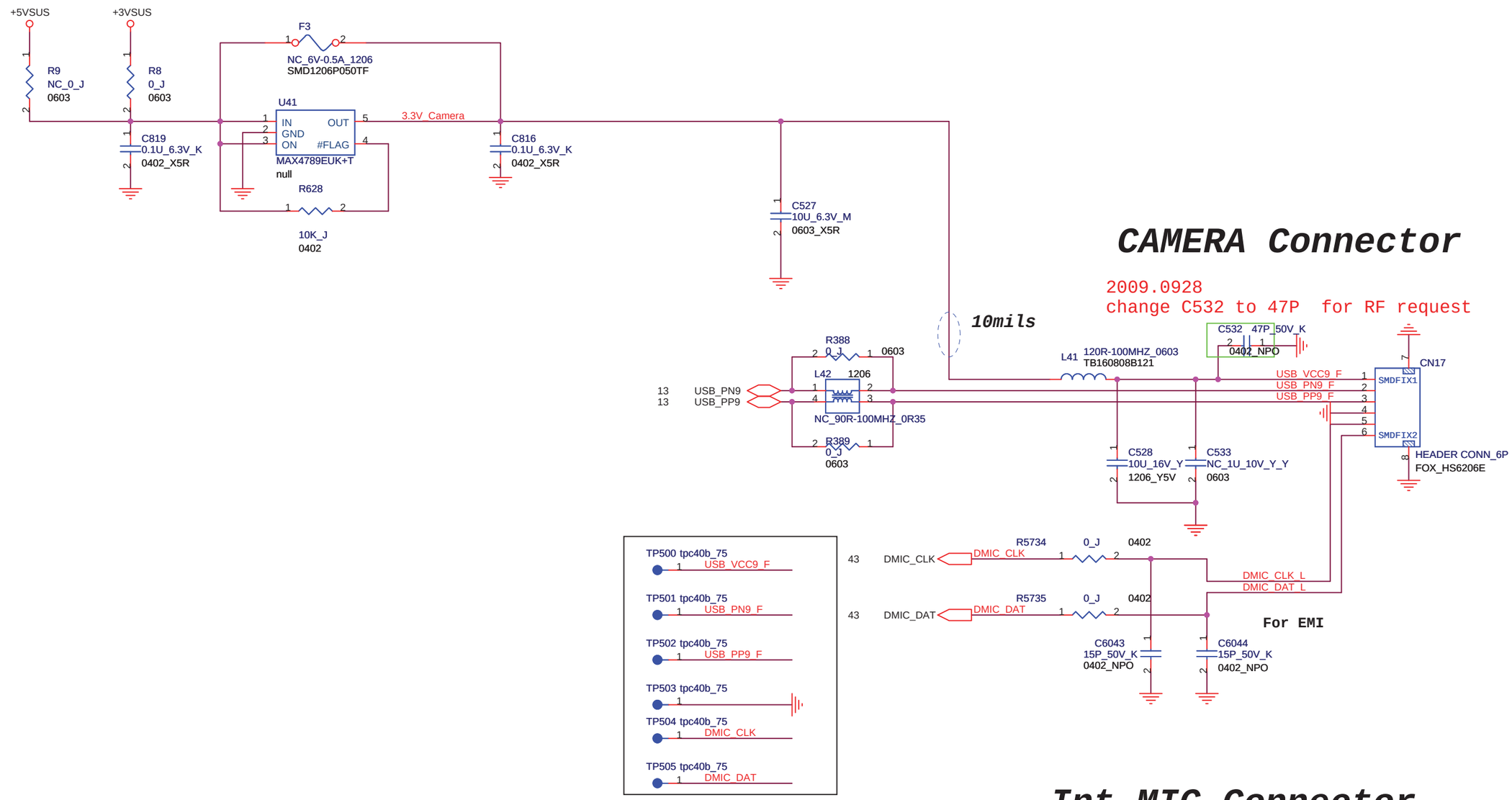
Close to U21

SD CONN.

For EMI

2009.0921
change C1986 to 12p

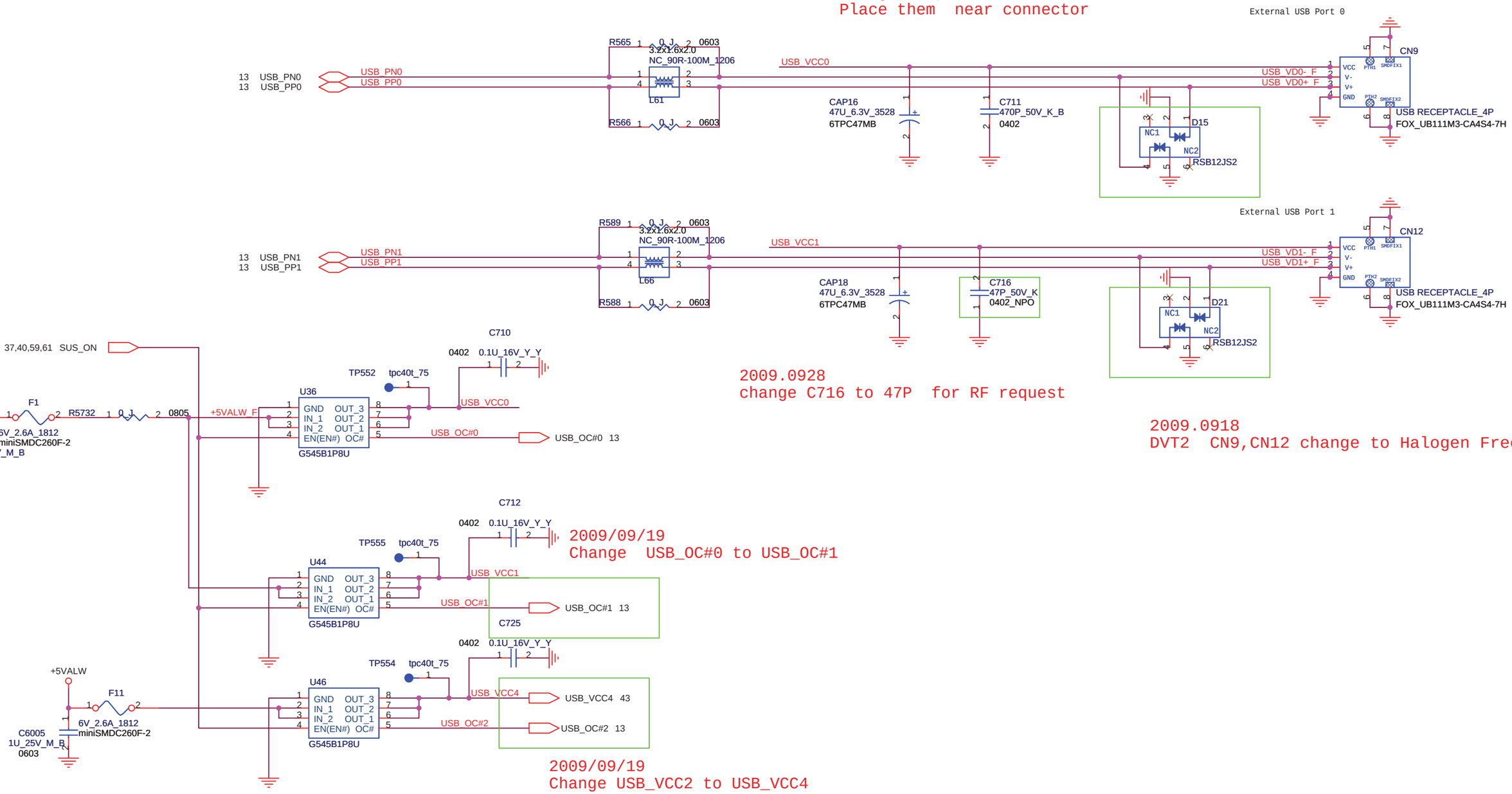
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCIE (MS/SD) 2/2	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 46 of 73	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CAMERA/Int MIC.	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 47 of 73	

http://hobi-elektronika.net

2009.0921
change D15,D21from NC to mount
Place them near connector

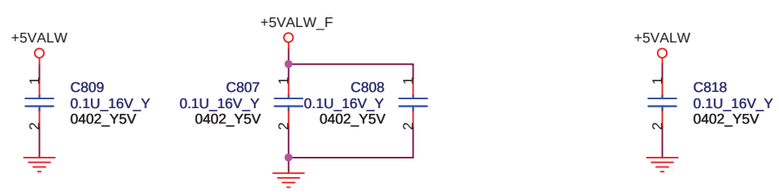


2009.0928
change C716 to 47P for RF request

2009.0918
DVT2 CN9,CN12 change to Halogen Free

2009/09/19
Change USB_OC#0 to USB_OC#1

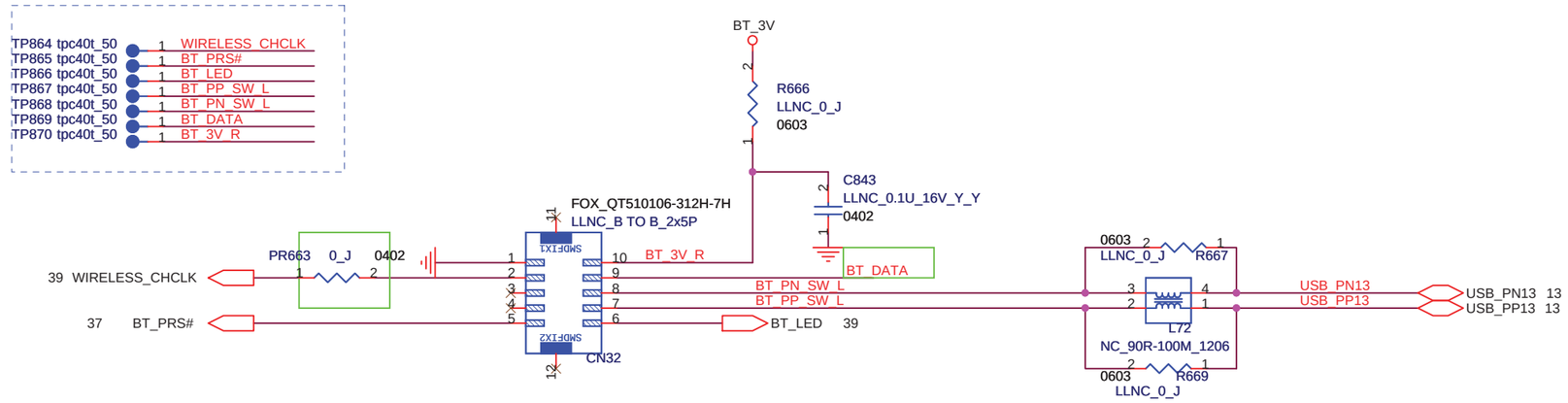
2009/09/19
Change USB_VCC2 to USB_VCC4



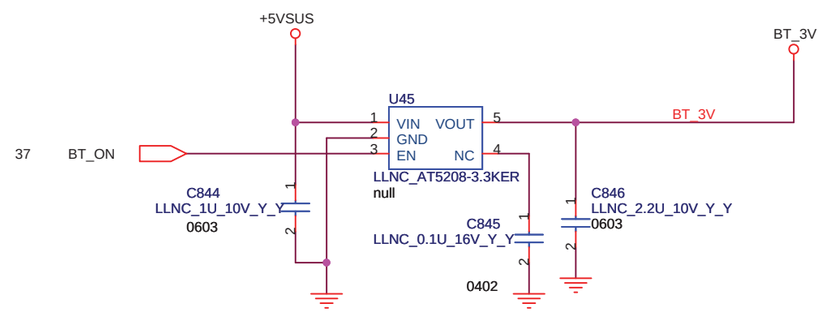
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	USB2.0	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, October 29, 2009	Sheet 48 of 73	

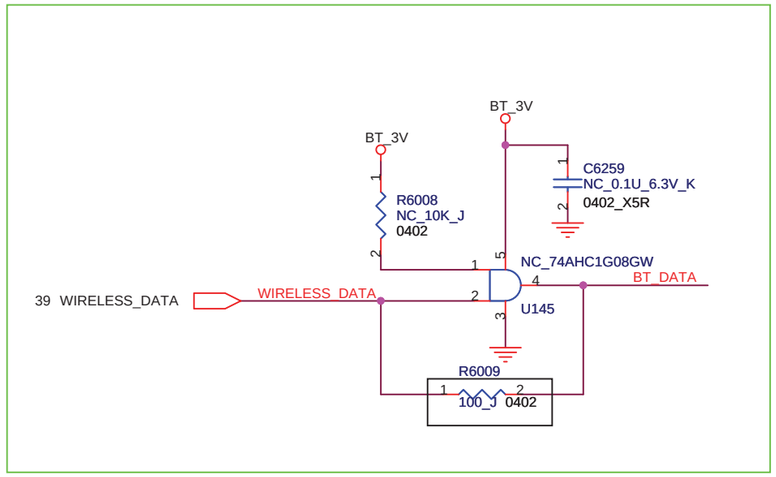
Bluetooth connector

BOT Side PVT

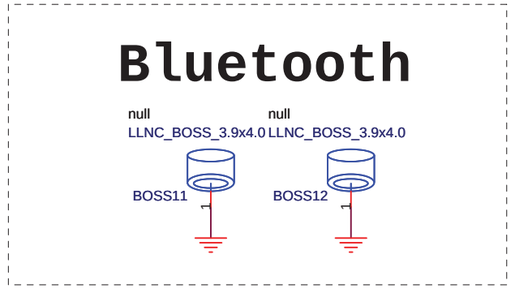


2009.0921
WIRELESS_DATA/WIRELESS_CHCLK follow M930

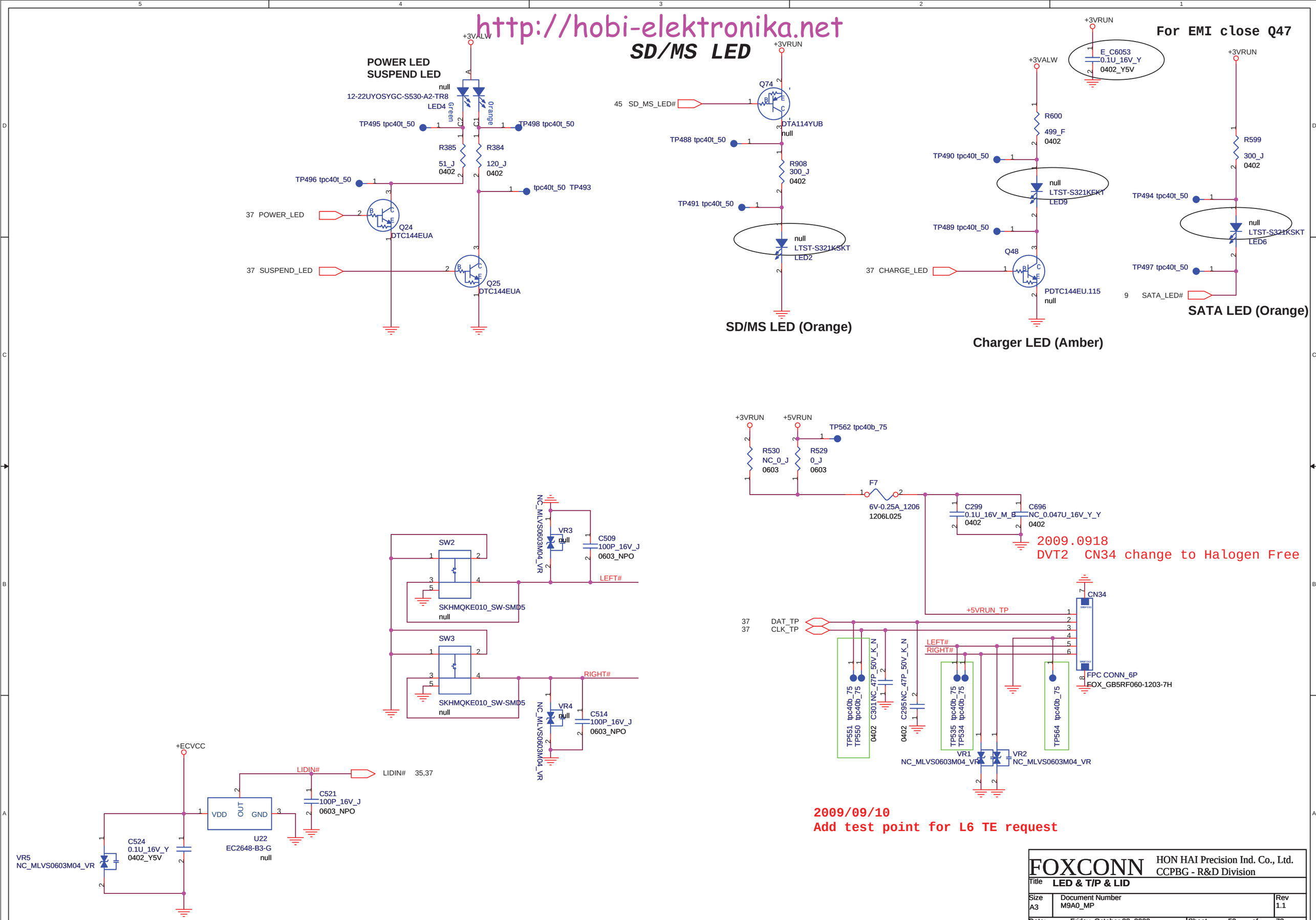




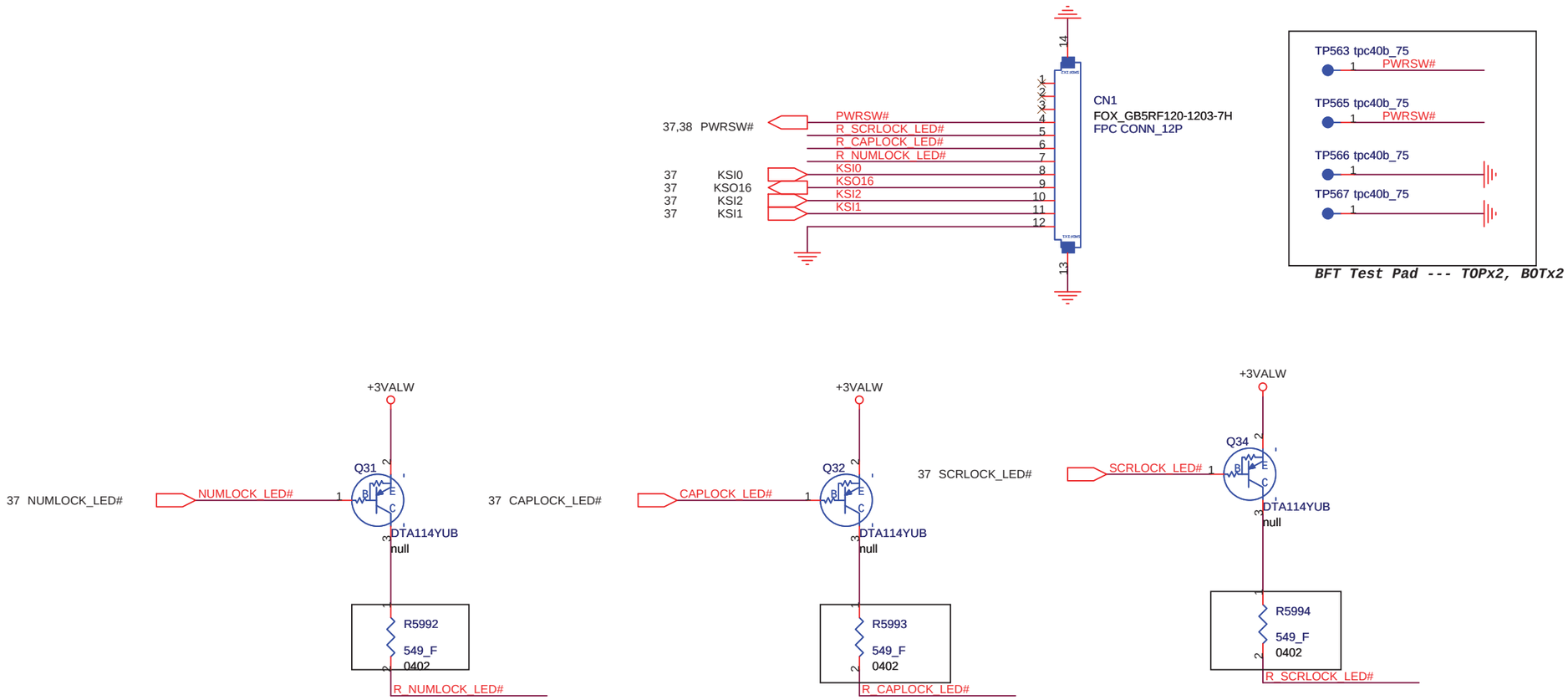
2009.11.19
Change R6009 from 1R-0000000-J200 to 1R-0000101-J200 for RF request



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	**Bluetooth**	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, November 19, 2009	Sheet 49 of 73	

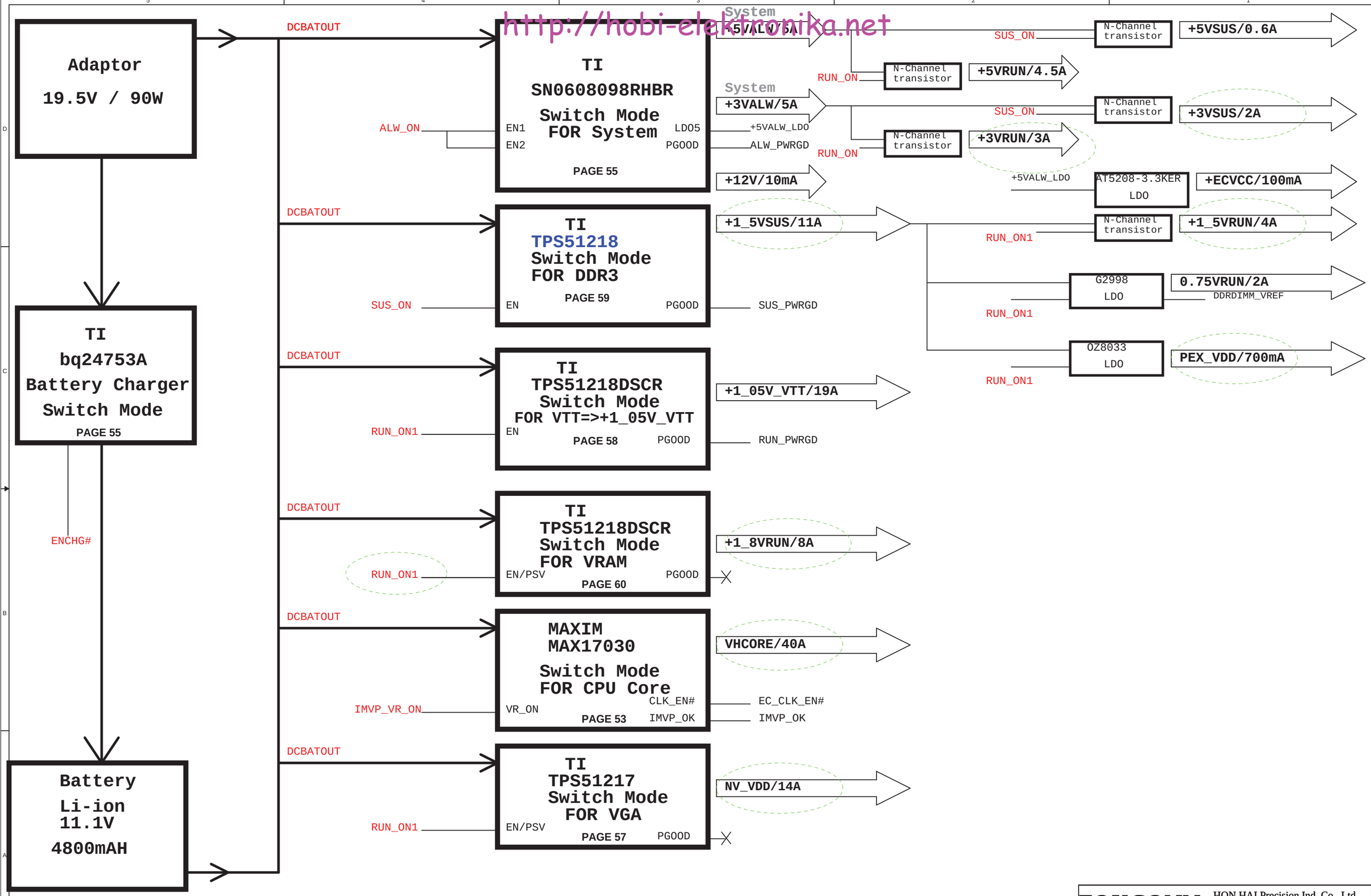


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LED & T/P & LID	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 50 of 73	

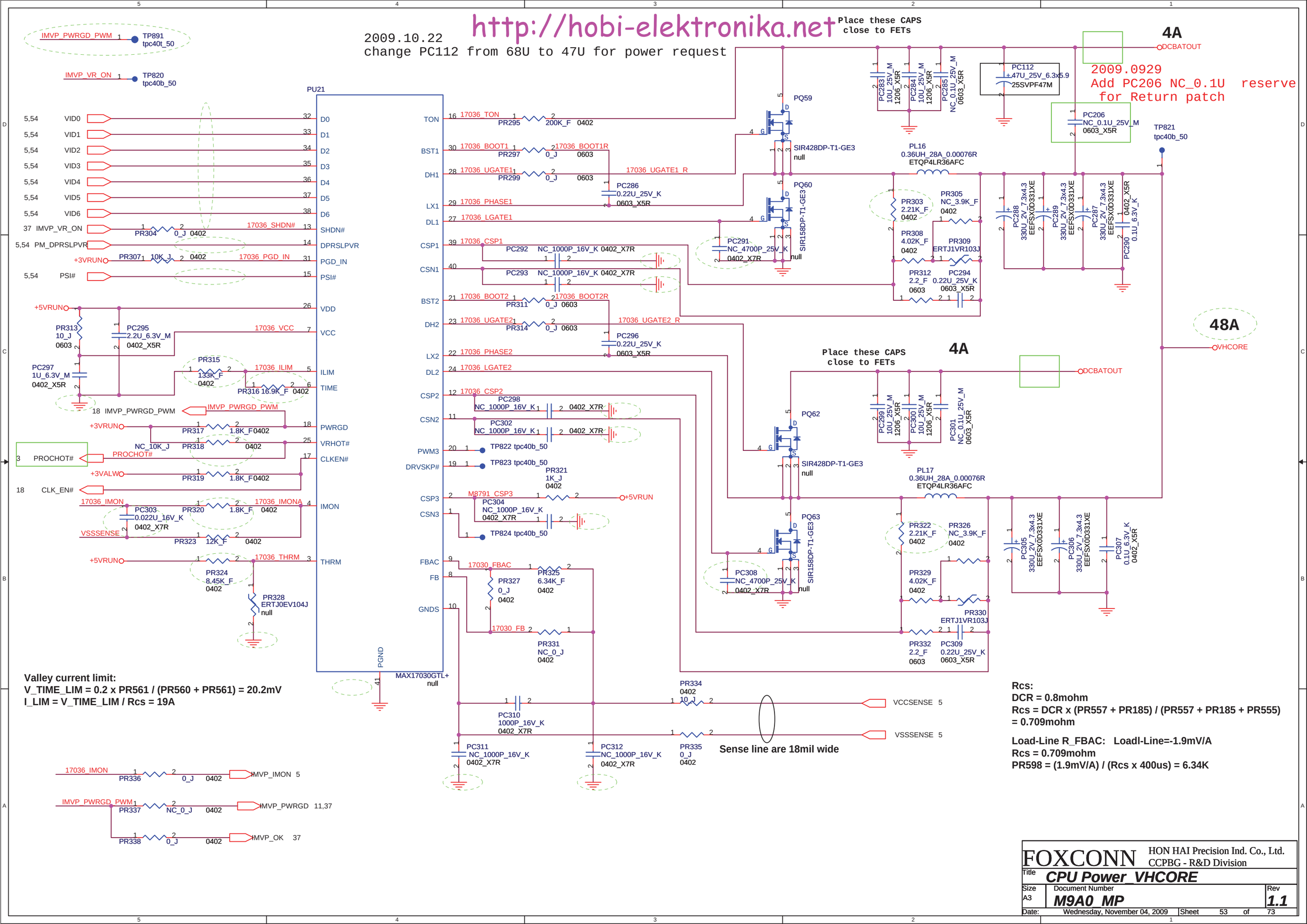


2009.10.30
change R5992,R5993,R5994 from 120ohm to 549ohm follow M870

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Power Board MB CONN	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 51 of 73	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Power Design Diagram		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Wednesday, September 23, 2009	Sheet 52 of 73		



Valley current limit:
V_TIME_LIM = 0.2 x PR561 / (PR560 + PR561) = 20.2mV
I_LIM = V_TIME_LIM / Rcs = 19A

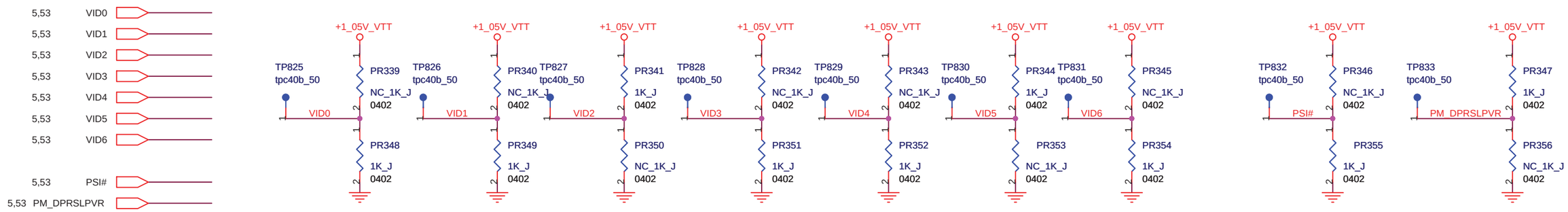
Rcs:
DCR = 0.8mohm
Rcs = DCR x (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.709mohm

Load-Line R_FBAC: LoadI-Line=-1.9mV/A
Rcs = 0.709mohm
PR598 = (1.9mV/A) / (Rcs x 400us) = 6.34K

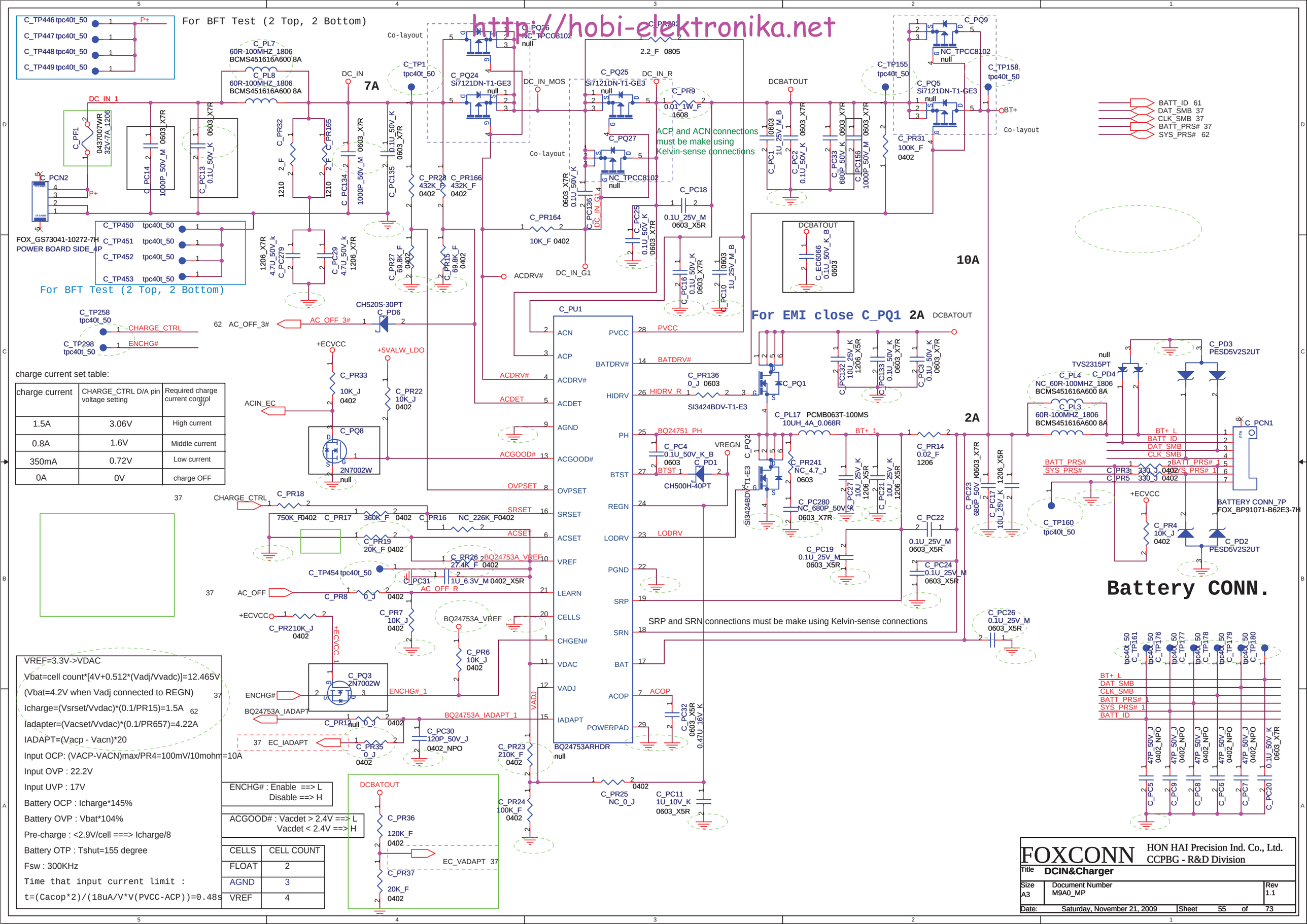
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CPU Power_VHCORE	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 53 of 73	

Default value of VID [6:0] = [0100100] , PSI = 0 , PROC_DPRSLPVR = 1

Market Segment Selection MSID[2:0] = [100] (SV)
- 416056_416056_Ard_EDS_Rev.1.1 - 403779_Clarksfield_MPG_Rev1.5



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	CPU Power_VID		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Tuesday, November 03, 2009	Sheet 54 of 73		



charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREF=3.3V->VDAC
Vbat=cell count*[4V+0.512*(Vadj/Vvadc)]=12.465V
(Vbat=4.2V when Vadj connected to REGN)
Icharge=(Vsrset/Vvdac)*(0.1/PR15)=1.5A
Iadapter=(Vacset/Vvdac)*(0.1/PR657)=4.22A
IADAPT=(Vacp - Vacn)*20
Input OCP: (VACP-VACN)max/PR4=100mV/10mohm=10A
Input OVP : 22.2V
Input UVP : 17V
Battery OCP : Icharge*145%
Battery OVP : Vbat*104%
Pre-charge : <2.9V/cell ===> Icharge/8
Battery OTP : Tshut=155 degree
Fsw : 300KHz
Time that input current limit :
t=(Cacop*2)/(18uA/V*V(PVCC-ACP))=0.48s

ENCHG# : Enable ==> L
Disable ==> H

ACGOOD# : Vacdet > 2.4V ==> L
Vacdet < 2.4V ==> H

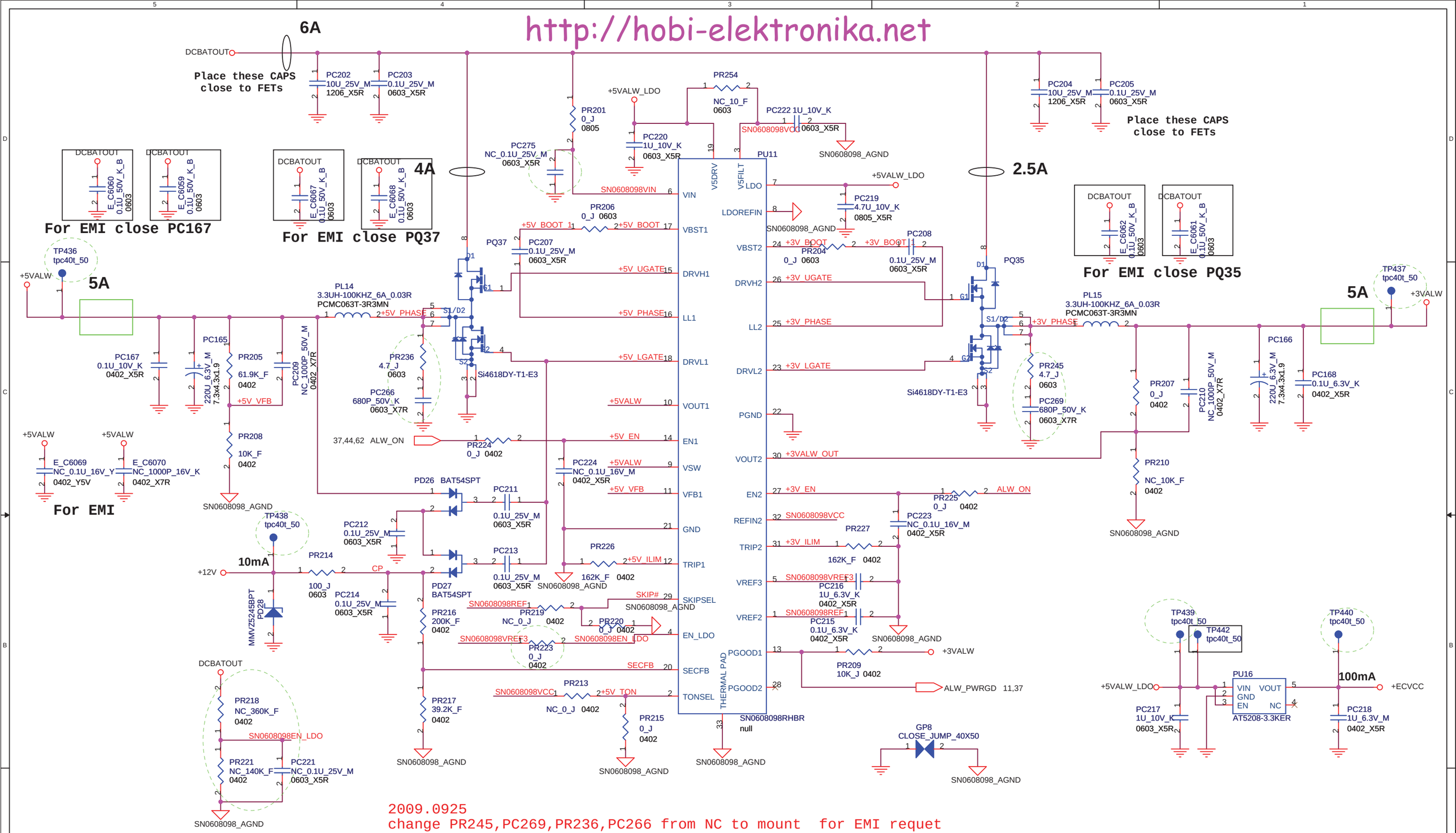
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: DCIN&Charger

Size: A3 | Document Number: M9A0_MP | Rev: 1.1

Date: Saturday, November 21, 2009 | Sheet 55 of 73



2009.0925
change PR245,PC269,PR236,PC266 from NC to mount for EMI requet

TON	Operating Frequence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
Rocp=(Iocp-Iripple/2)*(10*Rds(on))/5u
+5VALW=((PR205/PR208)+1)*VFB1

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

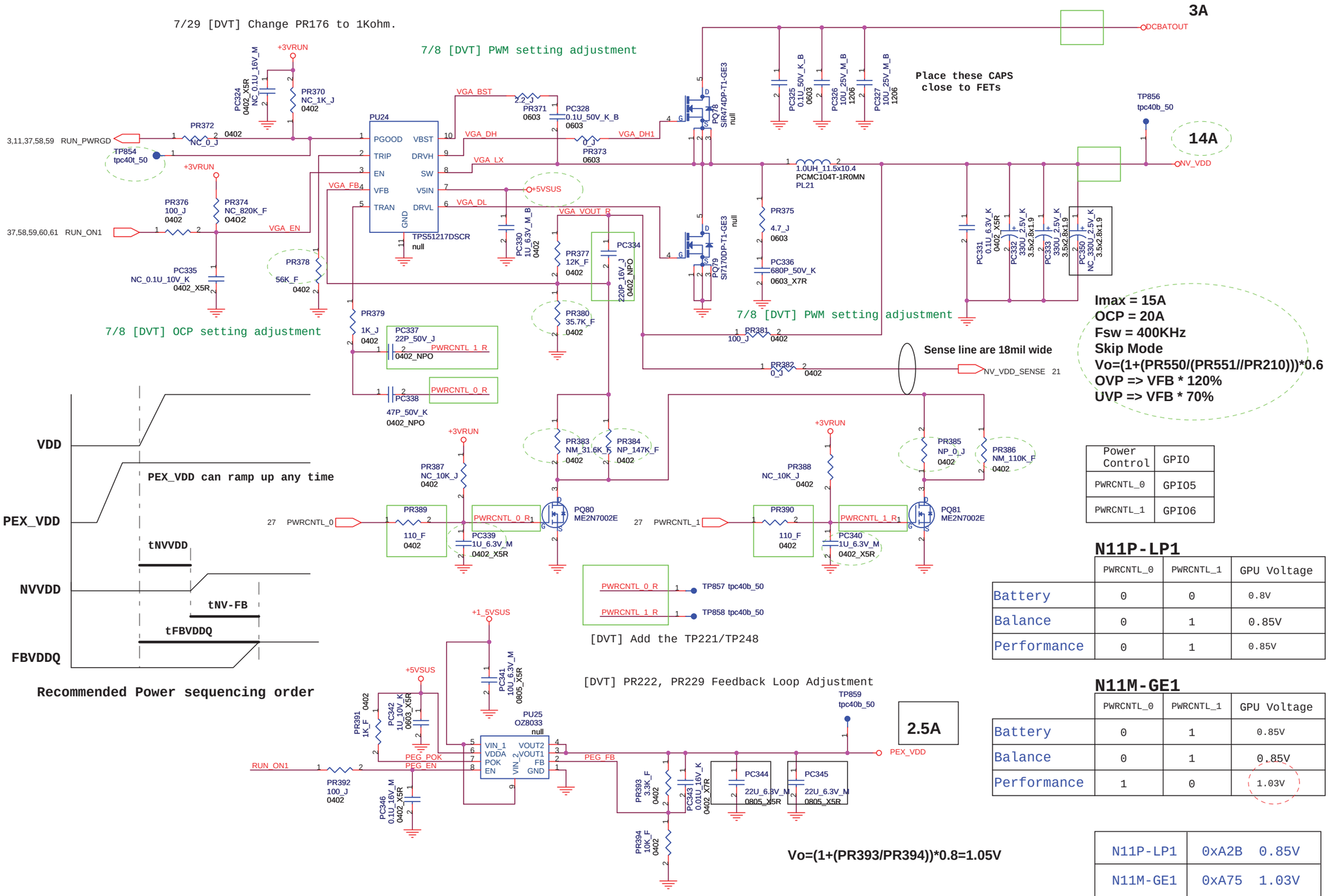
Title: SYS Power (+3_3V/+5V)

Size: A3 | Document Number: M9A0_MP | Rev: 1.1

Date: Wednesday, November 04, 2009 | Sheet 56 of 73

7/29 [DVT] Change PR176 to 1Kohm.

7/8 [DVT] PWM setting adjustment



Power Control	GPIO
PWRCNTL_0	GPIO5
PWRCNTL_1	GPIO6

N11P-LP1

	PWRCNTL_0	PWRCNTL_1	GPU Voltage
Battery	0	0	0.8V
Balance	0	1	0.85V
Performance	0	1	0.85V

N11M-GE1

	PWRCNTL_0	PWRCNTL_1	GPU Voltage
Battery	0	1	0.85V
Balance	0	1	0.85V
Performance	1	0	1.03V

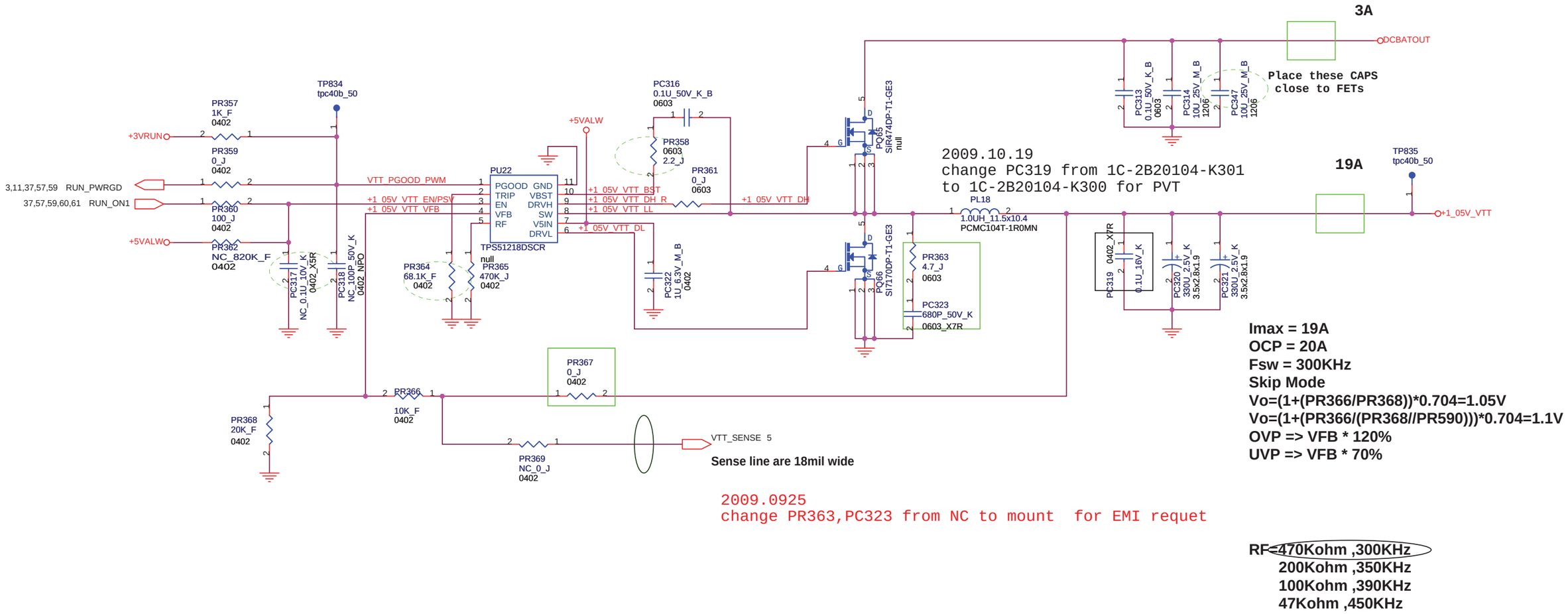
N11P-LP1	0xA2B	0.85V
N11M-GE1	0xA75	1.03V
P8 P12	0.85 V 0.8 V	

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: SYS Power(+1_5V/+1_05V)

Size: Custom | Document Number: M9A0_MP | Rev: 1.1

Date: Wednesday, November 04, 2009 | Sheet 57 of 73



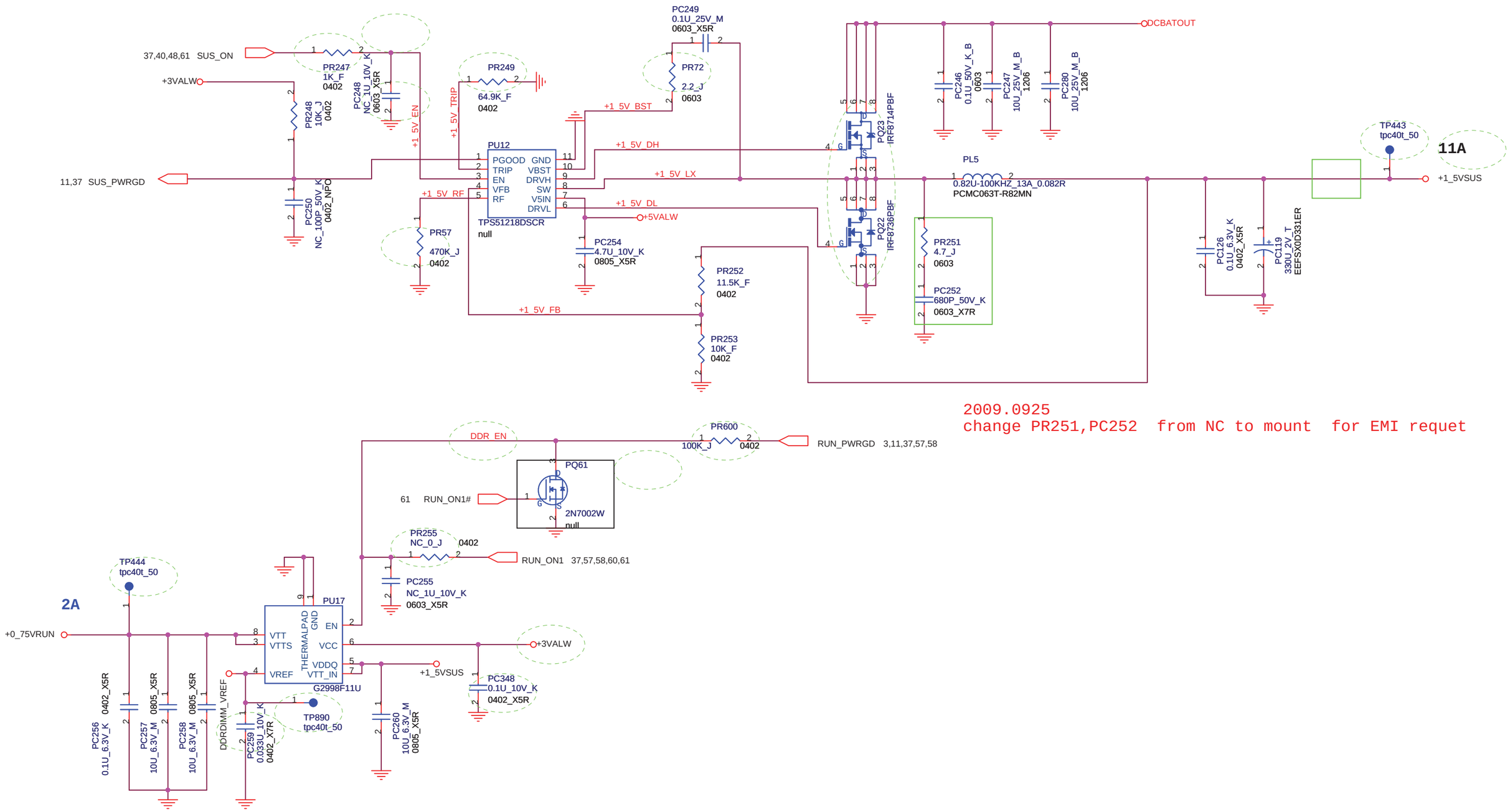
2009.10.19
change PC319 from 1C-2B20104-K301
to 1C-2B20104-K300 for PVT

Imax = 19A
OCP = 20A
Fsw = 300KHz
Skip Mode
Vo=(1+(PR366/PR368))*0.704=1.05V
Vo=(1+(PR366/(PR368//PR590)))*0.704=1.1V
OVP => VFB * 120%
UVP => VFB * 70%

2009.0925
change PR363,PC323 from NC to mount for EMI requet

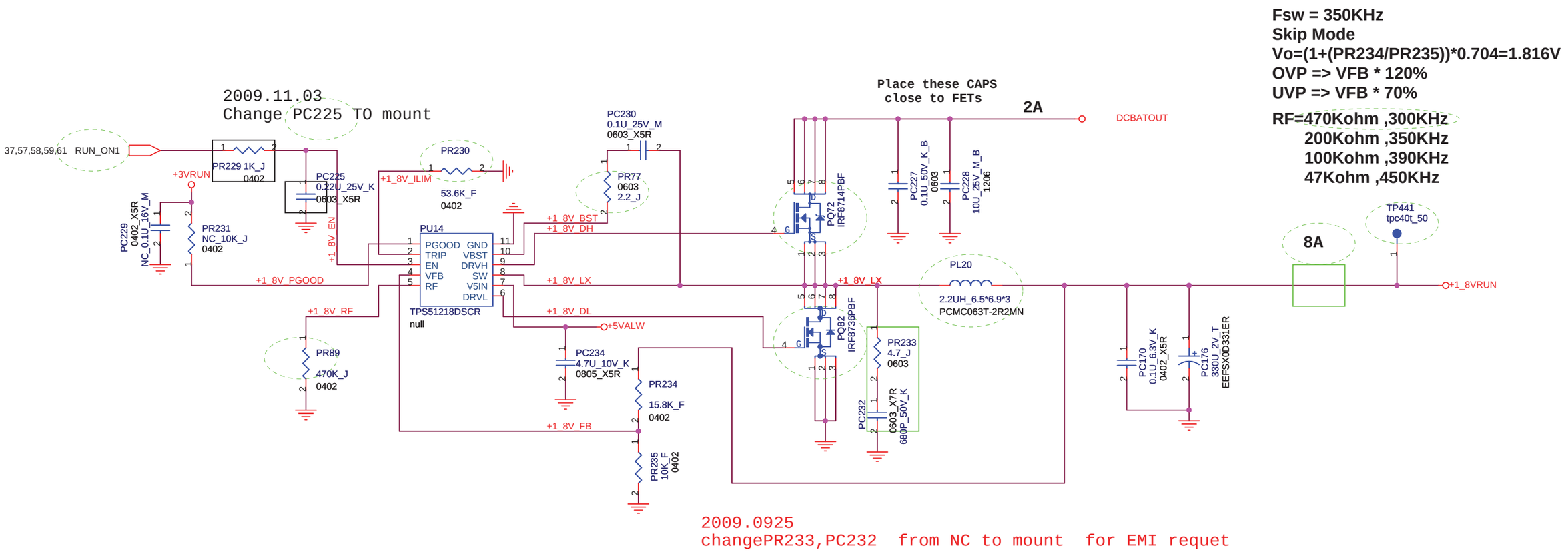
RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	***DDR3 Power(+1_5V/+0_75V)***	
Size Custom	Document Number ***M9A0_MP***	Rev ***1.1***
Date: Wednesday, November 04, 2009	Sheet 58 of 73	



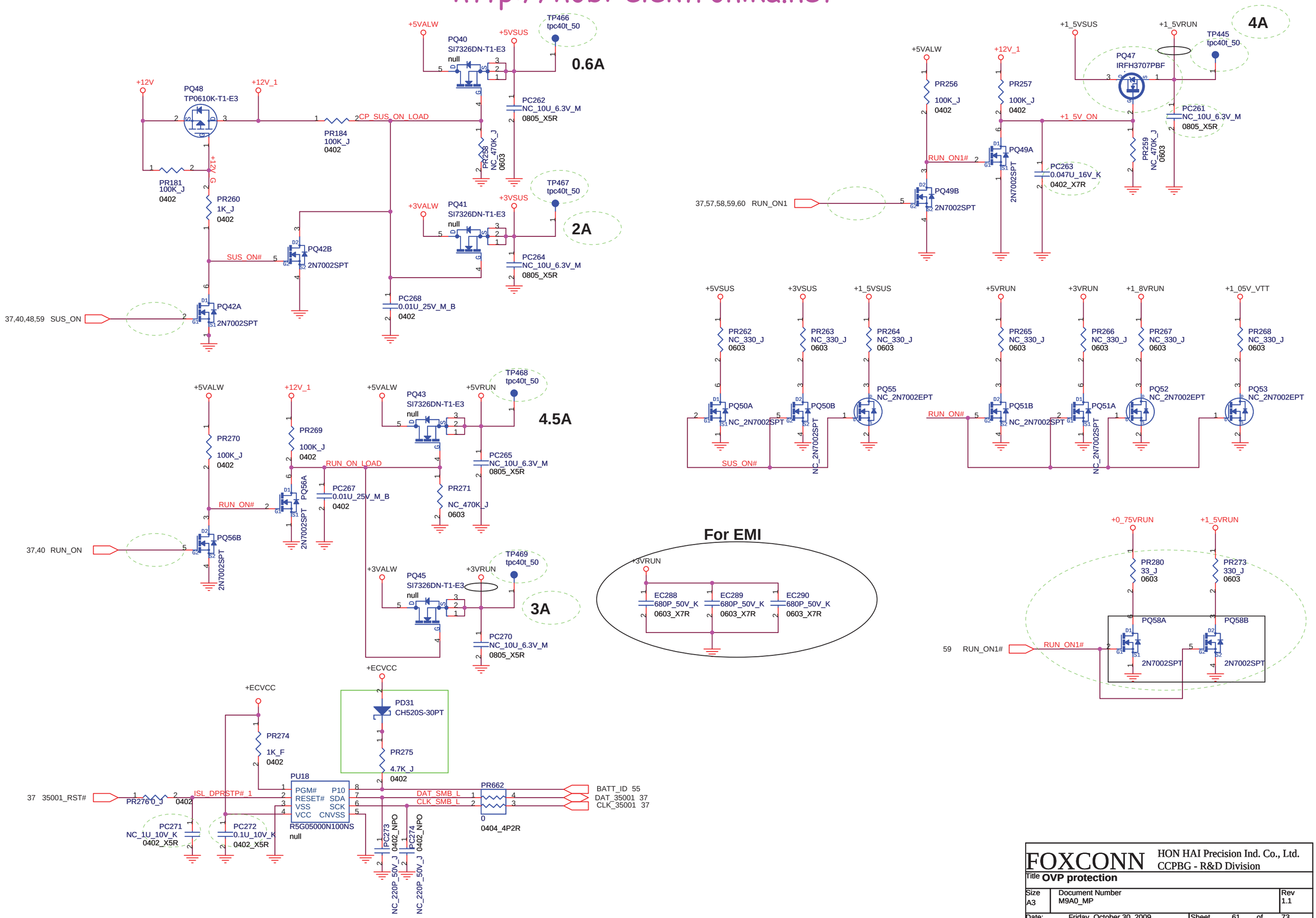
2009.0925
change PR251,PC252 from NC to mount for EMI requet

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_8V)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 59 of 73	

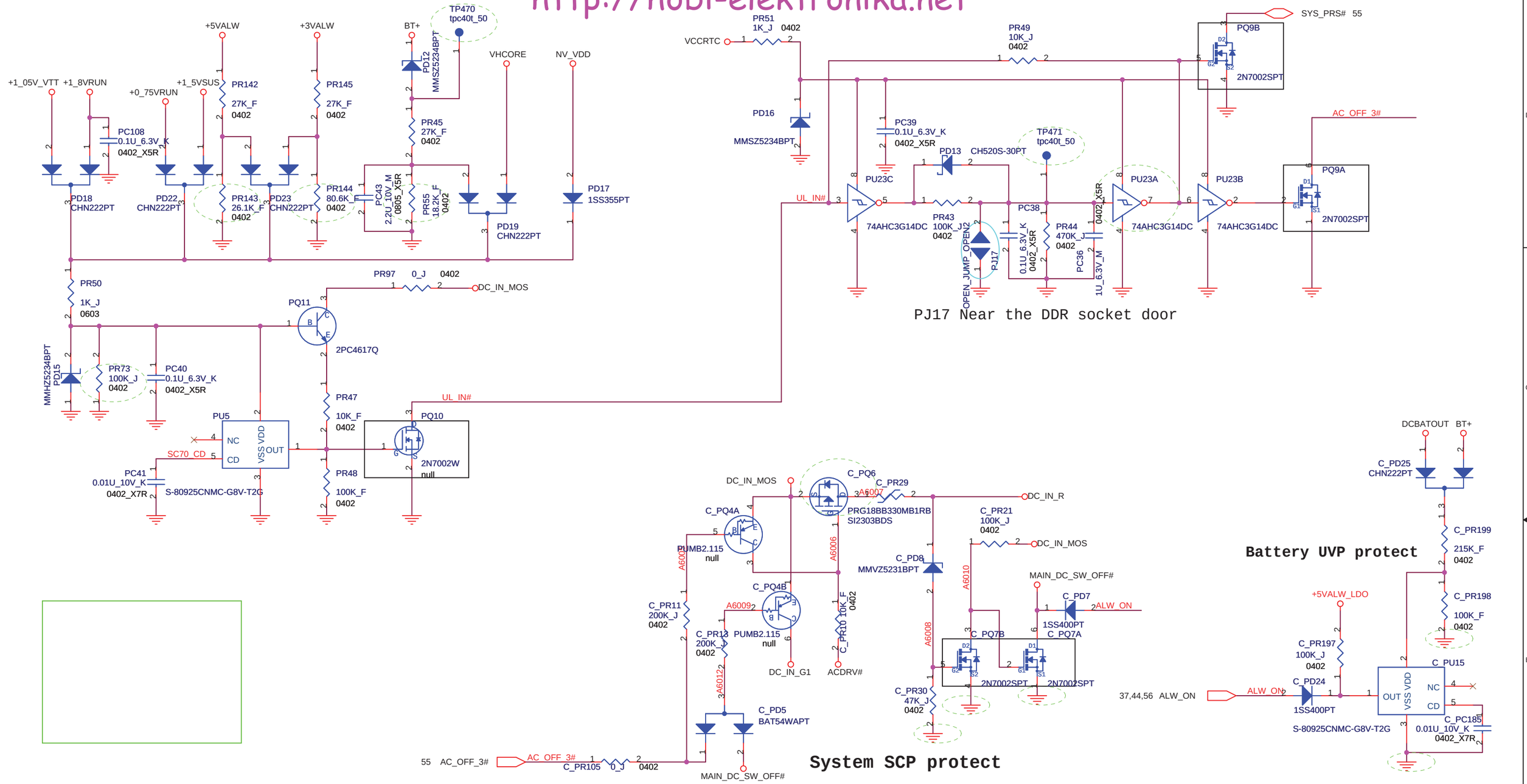


2009.0925
changePR233,PC232 from NC to mount for EMI requet

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Others power plan	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 60 of 73	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title OVP protection		
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 30, 2009	Sheet 61 of 73	

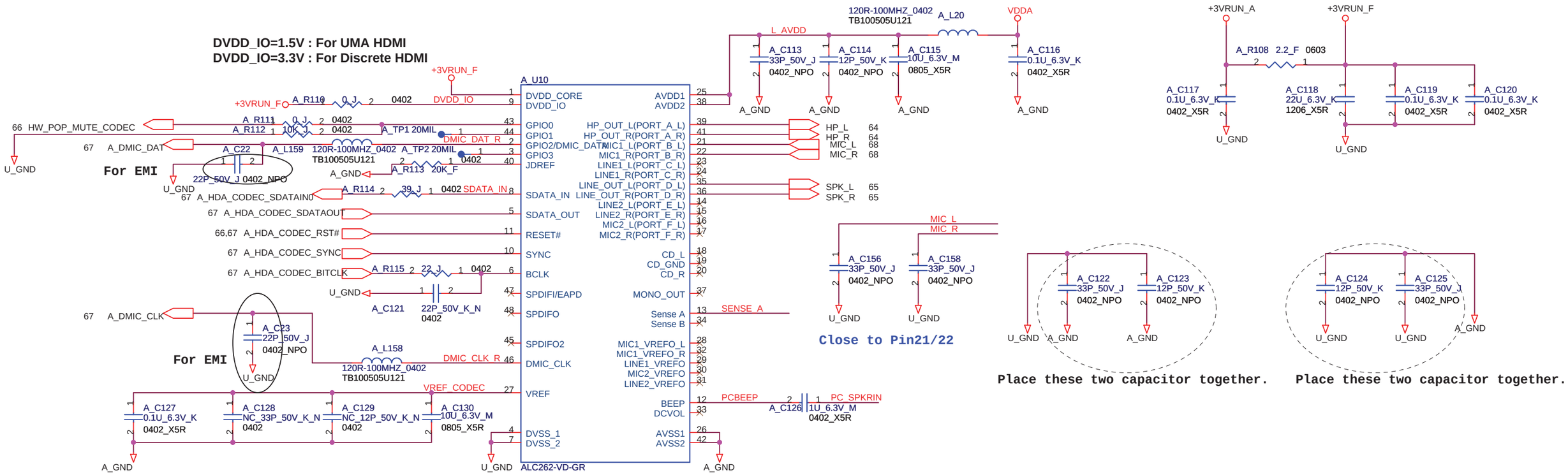


VIINP	90W adaptor
PWRLIMIT	1.3V/85W

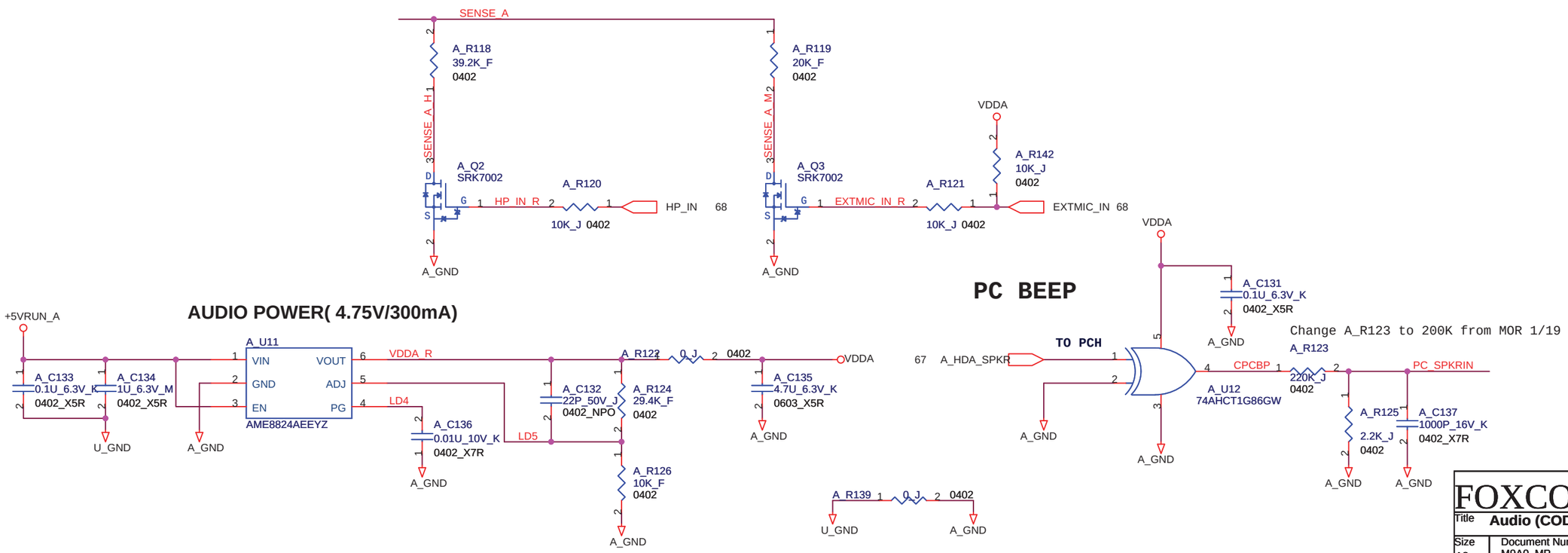
adapter max load : 5.7A/3000ms
adapter OCP : 7.5Amax

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	VGA Power(Fix +1_1V)		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Thursday, November 19, 2009	Sheet 62 of 73		

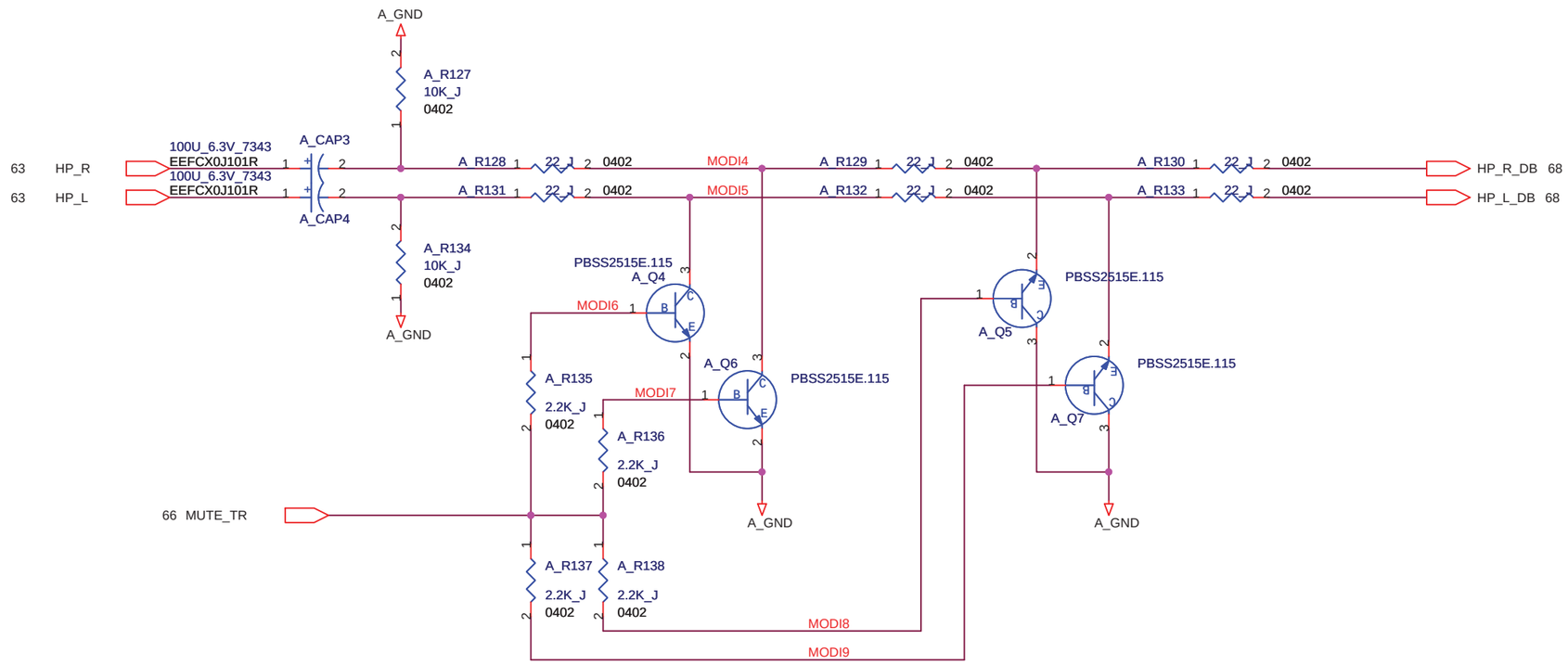


2009.11.03
change A_C23,A_C22 from 15PF to 22PF for EMI request



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Audio (CODEC & POWER)		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Tuesday, November 03, 2009	Sheet 63 of 73		



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Audio (HP)**	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 64 of 73	

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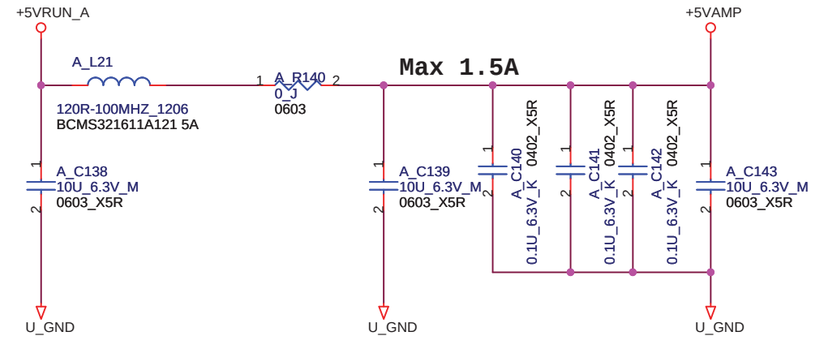
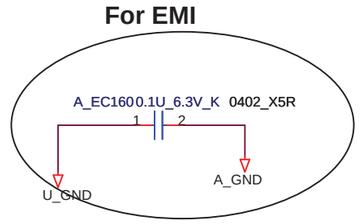
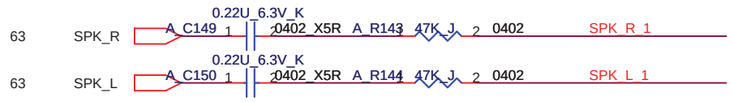
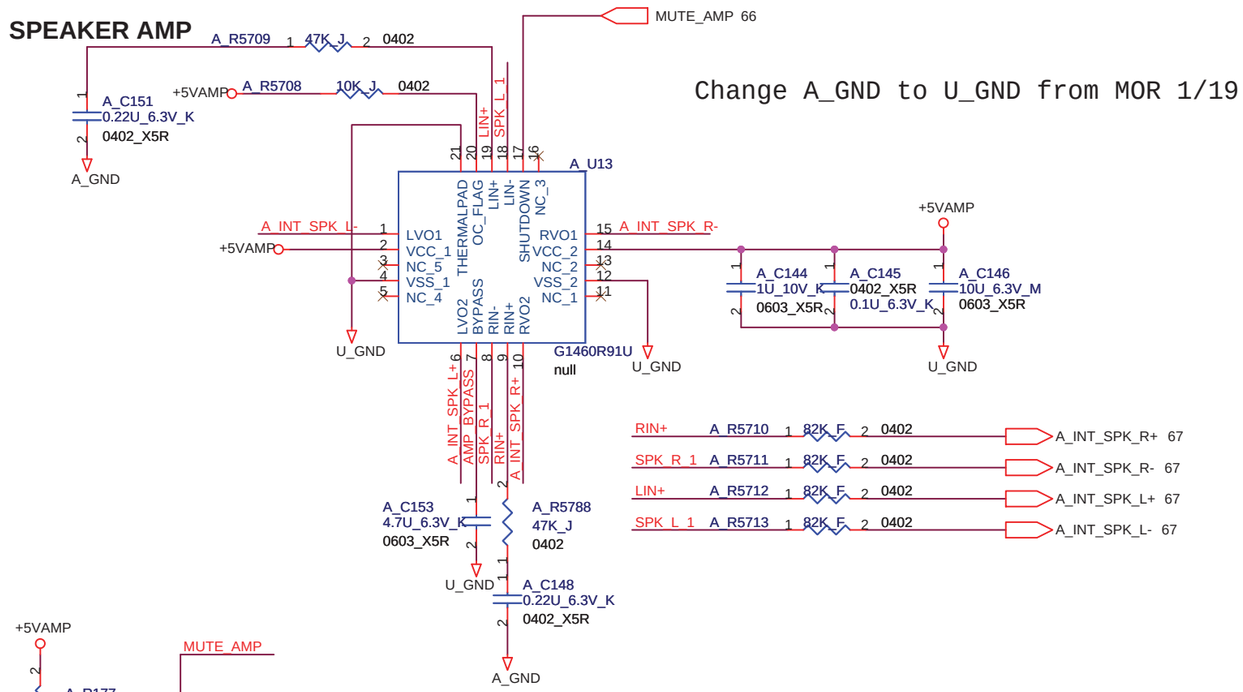
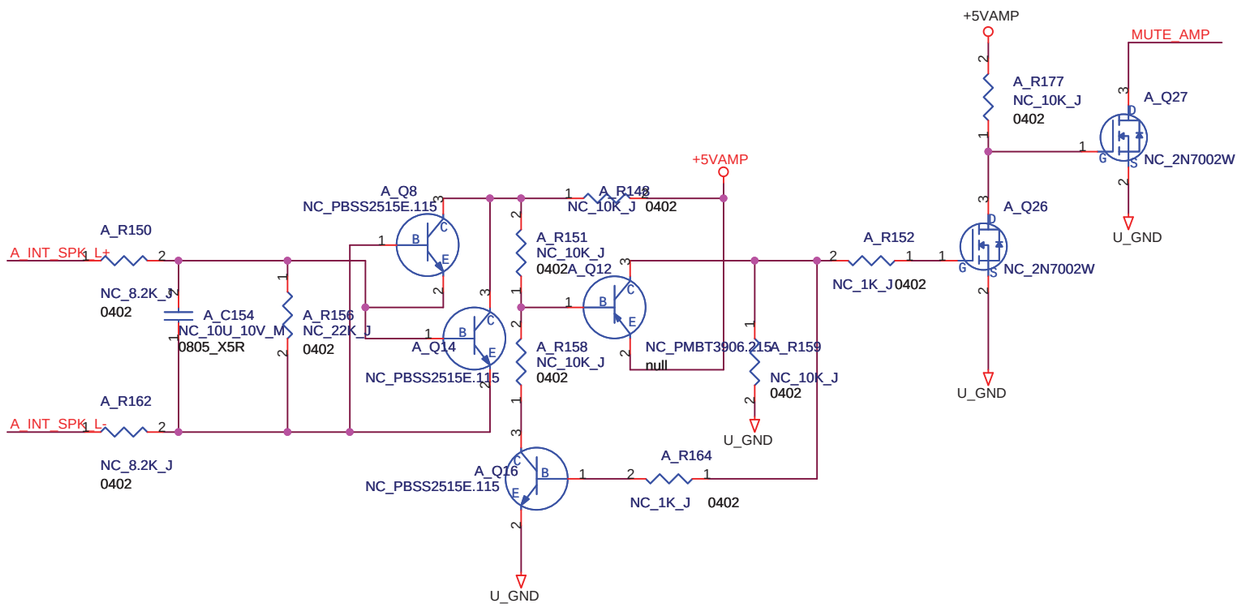


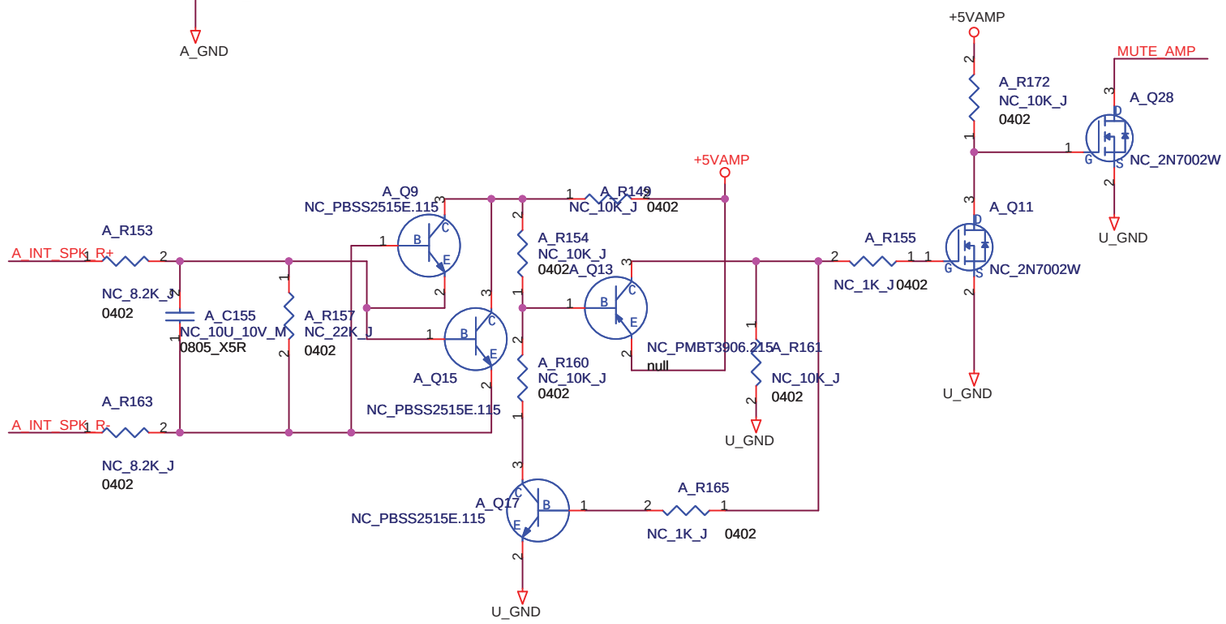






Change A_GND to U_GND from MOR 1/19





For Mor request,add the speaker cable short protection circuit

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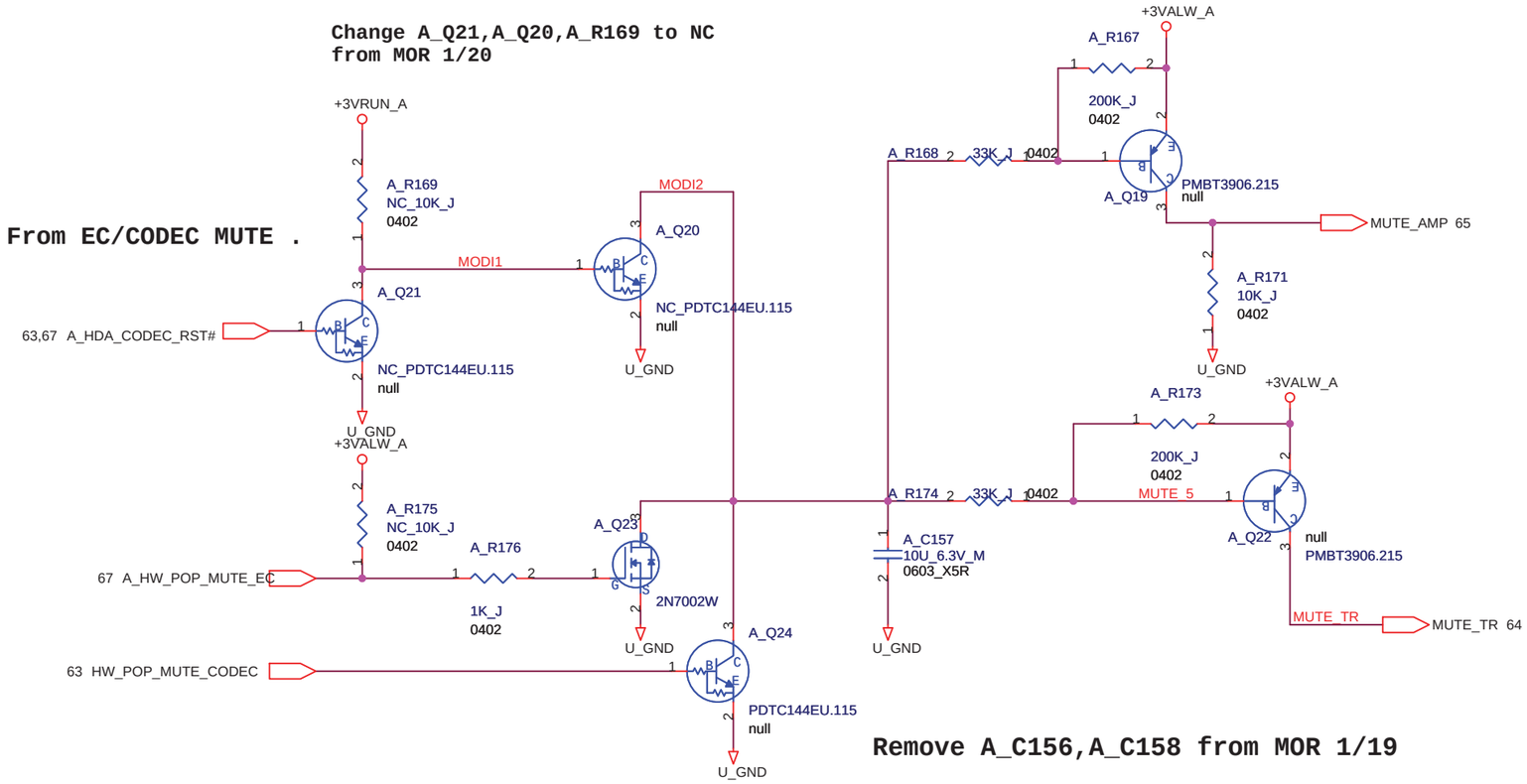

Delete A_R177+A_R178, change A_Q24
to DTC144EUA from MOR 1/20.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
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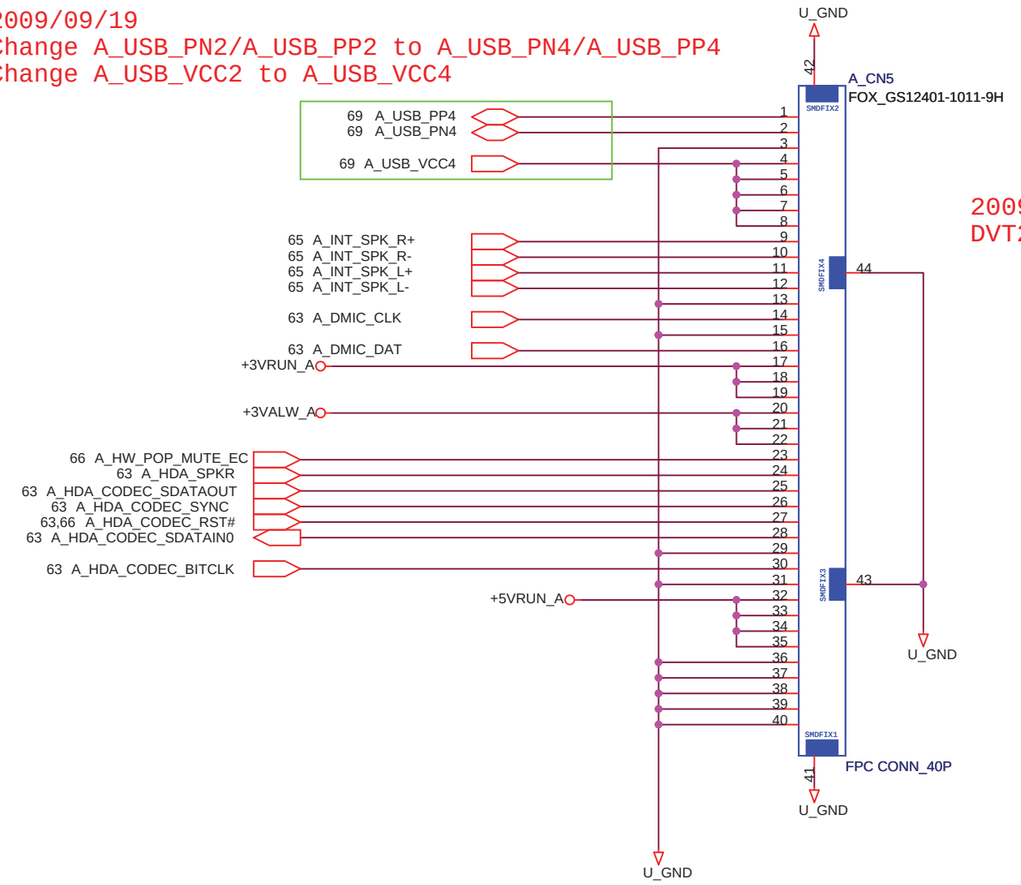
2009/09/19
Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4
Change A_USB_VCC2 to A_USB_VCC4



2009.0918
DVT2 A_CN5 change to Halogen Free

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
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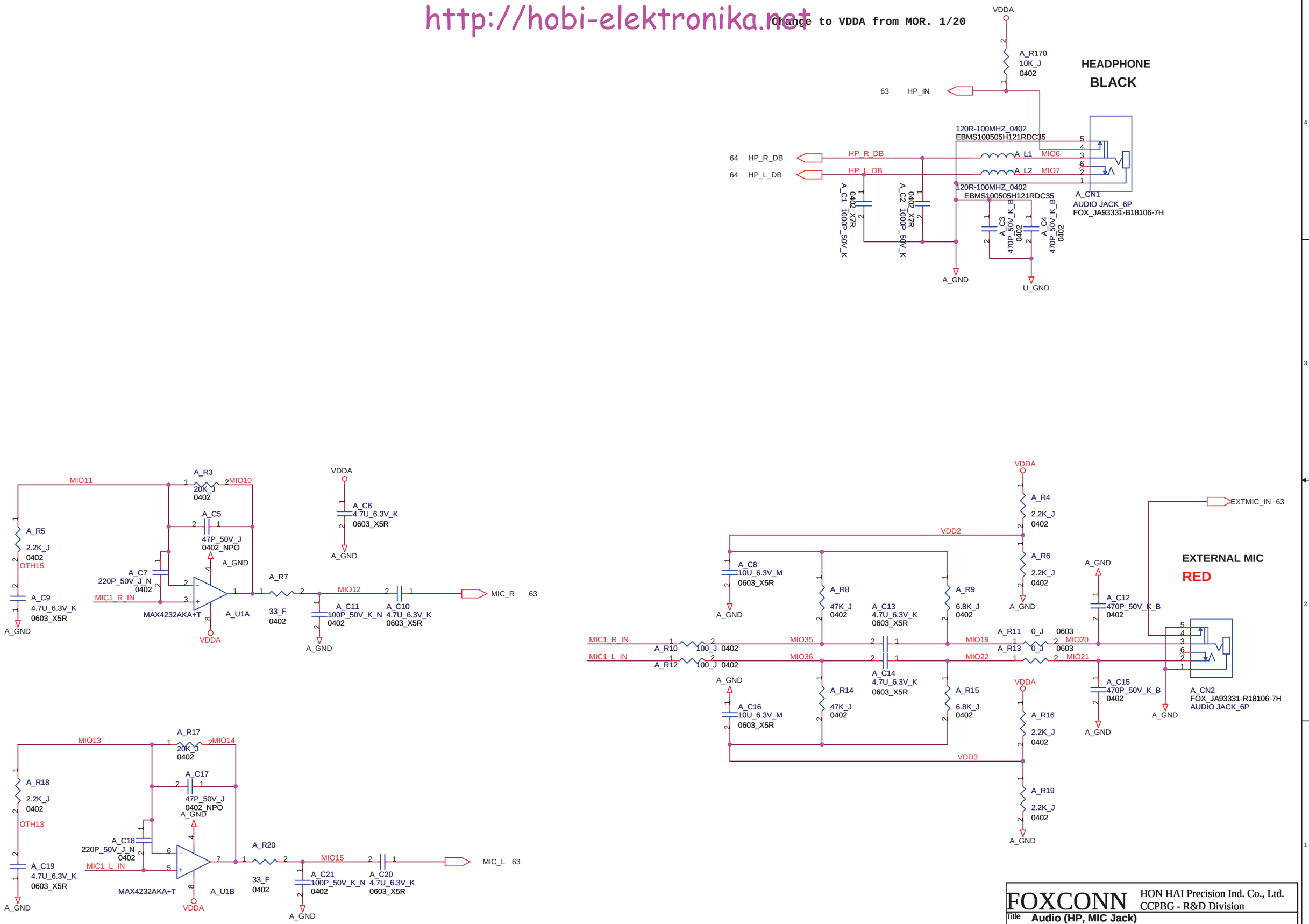
Change to VDDA from MOR. 1/20



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

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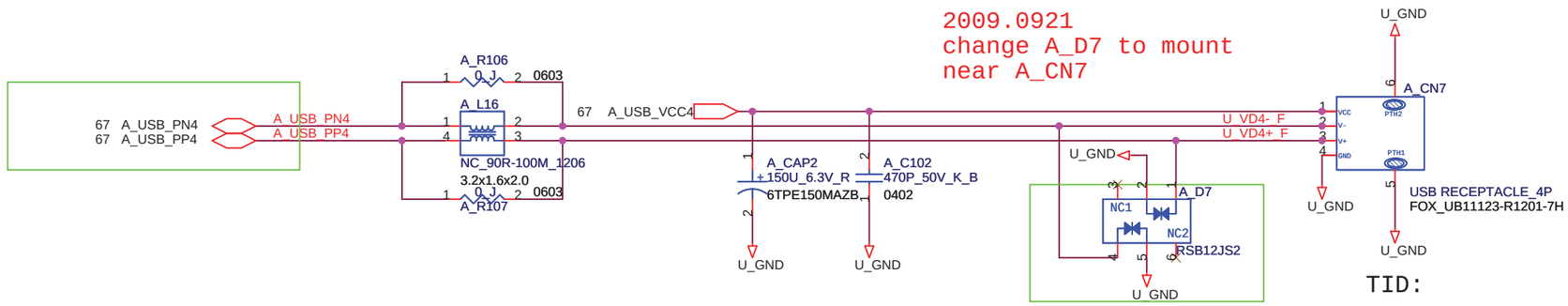

2009.0921
change A_D7 to mount
near A_CN7

TID:

2009.0918
DVT2 A_CN7 change to Halogen Free

2009/09/19
Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4
Change A_USB_VCC2 to A_USB_VCC4
Change U_VD2+_F/U_VD2-_F to U_VD4+_F/U_VD4-_F

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	USB2.0	
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VespaCP no fingerprint function, so this page reserve

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	FINGER PRINT	
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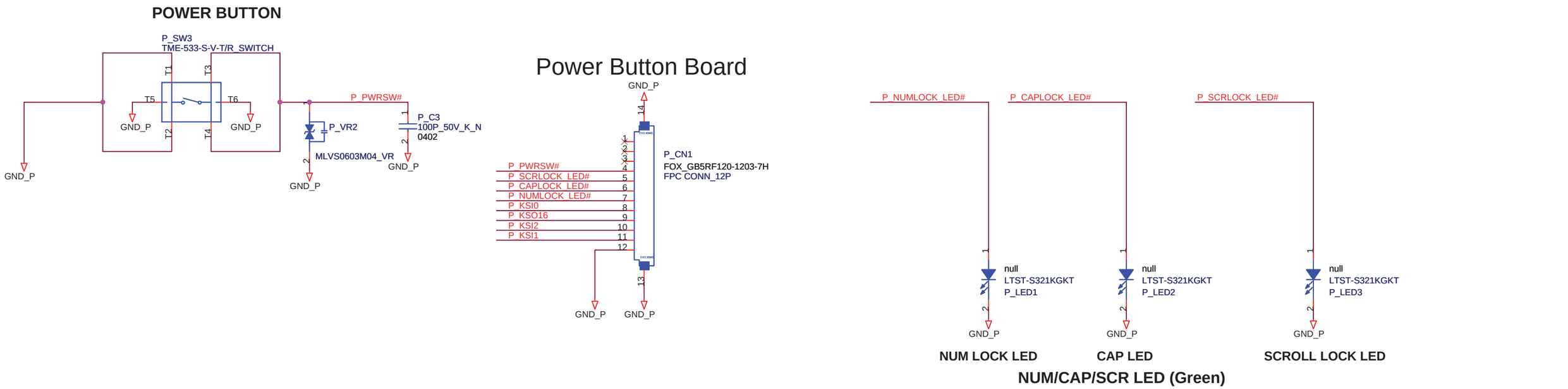

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CONN & BUTTONS	
Size A3	Document Number M9A0_MP	Rev 1.1
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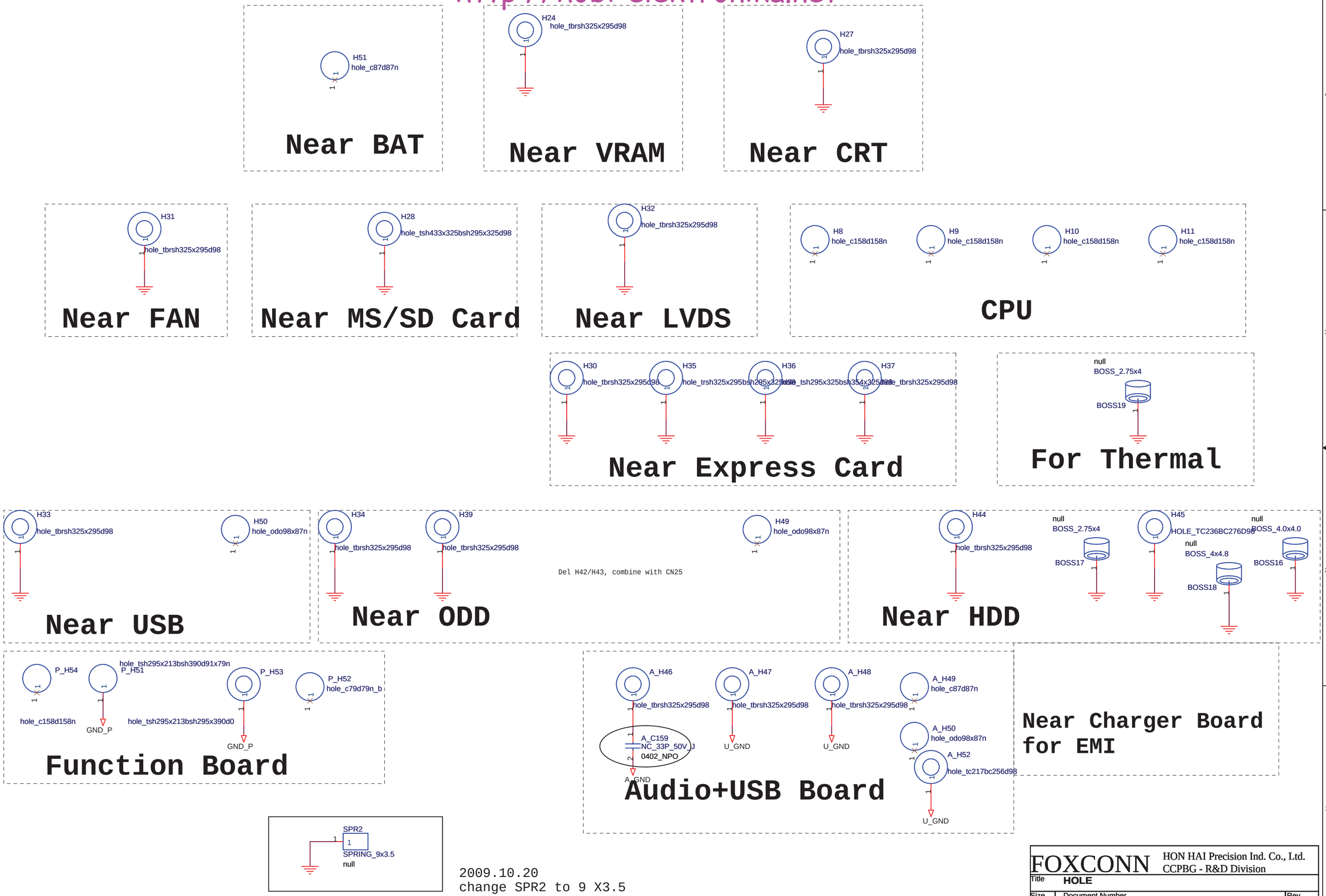

2009.10.20
change SPR2 to 9 X3.5

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HOLE	
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2009/0910

1. Add S/D CARD test point for L6 TE request
 TP736

2. Add MS CARD test point for L6 TE request
TP690, TP691, TP693, TP694, TP695, TP696, TP697
TP702, TP724, TP698, TP699, TP700, TP701, TP703

delete

3. Add I_LINK test point for L6 TE request
TP512, TP513, TP514,TP515

4. Add TOUCHPAD test point for L6 TE request
TP551, TP550, TP535, TP534 ,TP562, TP564

5.Delete R5893, R5887 and trace AC PRESENT,
add R6007 to +3VALW in page 11, delete trace AC PRESENT,
add test point TP186 in page 37. VespaCP use Ignition FW,
no ACPRESENT function.
Intel FAE suggest this pin can configure as GPIO.

6.change C6131 from NC_470P_16V_K to 0.047U_16V_K follow Intel suggest

7. Change trace（CLK-PCIE-EXPRESS#,CLK-PCIE-EXPRESS,EXPRESS-CLKREQ#) from
U134(AH42,AH41,A8) to (AJ50,AJ52,H6) for DVT1 express card can't detect issue.

8. Change page 70 from finger print to reserve, VespaCP no this function.

2009/0912

9. Delete R5785 0ohm resistor for voltage drop problem

10. Change RP82 from NC to mount for SI test
Change RP81 from mount to NC for SI test
Change RP86 from NC to mount for SI test

2009/0914

11.delete finger print

12.delete TP417,link to gnd

13.CN16 PIN 15 LINK TO GND
14.CN35: change 0ohm to 33ohm

15.PCH: GNT0# and GNT1# change from pull high to +3vsus to pull low to gnd

16.DC_IN: DELETE C_PQ9 ,C_PR34
change C_PR36,C_PR37 from NC to mount
C_PF1 change to 0437007.WR

17.+1.05V: change PC319 from Y5V to X5R

18. VHCORE: change OVT_EC# to PROCHOT#

20.other: add PD31
change PR275 from 10K to 4.7K

21.OVP: DELETE PR78 ,PQ17
change PC35, PU2, PC37, PR240, PR108,PR39,
PR36 from mount to NC

22.N11P-LP1+SANSUNG(H2) SKU and
N11M-GE1 +SANSUANG(M2 SKU)need change BOM
R5244 change from 1R-0004532-F200(45.3K) to
1R-0002492-F200(24.9K) for nVIDIA FAE suggest

2009.0918
23. CN11, CN18, CN34, CN9, CN12, A_CN7, A_CN5 change to Halogen Free

2009/09/19
1.Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4
Change A_USB_VCC2 to A_USB_VCC4 in page 67

2. Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4
Change A_USB_VCC2 to A_USB_VCC4
Change U_VD2+_F/U_VD2-_F to U_VD4+_F/U_VD4-_F in page 69

3.Change USB_VCC2 to USB_VCC4
Change USB_OC#0 to USB_OC#1 in page 48

4.Add USB_OC#1
Change USB_PN10/USB_PP10 to test point in page 13

5.Change USB_VCC2 to USB_VCC4 in page 43

2009.0921
Page 50
1.R531 Delete,then pull CN34 pin4 to GND.
2.Remove the Test point TP562 to +5VRUN.

2009.0922
1.change R5727,R5273 from NC to mount
2.add R5313 for 10K_J
3.change R5916 TO NC
4.change D15,D21,A_D7 TO mount and place them near connector
5.WIRELESS_DATA/WIRELESS_CHCLK change，please refere to page 49
6.ADD R5991 for 100K_J
7.change C476 TO NC_12P
8.change C1986 TO 12P
9.ADD R6010,R6011,R6012 to pull-down SPI0_CLK,SPI0_MOSI,SPI0_CS# in page 09
10.change CN25,CN29,CN30 TO Halogen Free
11.change D13,D11 TO 16-SSM22LL_PT00
12.change R5910,R5911 to NC_1K
13.DELETE TP498,TP491,TP490,TP495,TP494,TP509
14.CHANGE Q45 TO NC ,R5996 TO MOUNT
15.change CN21 TO 1N-1052000-0000 for ME request
16.change BOSS1,BOSS2 to 1M-1F40M20-1500 for ME request
17.page 57:change net PWRCNTL_0_R TO PWRCNTL_1_R
change net PWRCNTL_1_R TO PWRCNTL_0_R
change PR389,PR380 TO 110 ohm
change PC334 to 220P_16V_J 0402
change PC337 to 220P_50V_J 0402
delete PJ23,PJ24,PJ25,PJ26

18.page 53:delete PJ18,PJ19
19.page 56:delete PJ1,PJ2
20.page 58:delete PJ20,PJ21,PJ22
ADD PR367/0 ohm
21.page 59:delete PJ5
22.page 60:delete PJ3
23.page 06:delete PJ43

2009.0923
ADD test point TP490,TP491,TP494,TP495,TP498,TP509

2009.0925
ADD C6260 NC_1000P_16V_K

2009.0925
For EMI request
1.Add Cap.C36 0.1U,C999 1000PF on net +1_05V_VTT
2.Add Cap.C37,C38 0.1U on net +1_8VRUN
3.Add Cap. C39 0.1U,C1000 1000PF on net +3VRUN
4.Add Cap.C53,C54,C61 0.1U on net DCBATOUT
5.Add SPR2

2009.0925
ADD C70,C71,C72 10P for RF request

2009.0925
change C6156,C6157 from 12p to 15p for vendor request

2009.0925
change PR245,PC269,PR236,PC266,PR363,PC323,PR251,
PC252,PR233,PC232 from NC to mount for EMI request

2009.0926
For EMI request
1.Add PC62 0.1U on net +1_8V_LX ,place it near PQ72
2.change C539 from NC to 680P
3.Add C549 680P on net INV_BRADJ,place it near LVDS connector

2009.0928
For RF request
change C1264,C716,C532 to 47P

2009.0928
change R5376 to 100K follow design guide

2009.0928
change PC337 to 22P

2009.0928
Add Q7 for MOR request

2009.0929
Add PC206 NC_0.1U reserve for Return patch

2009.0929
change RP86 ,RP82 TO NC
change RP81 TO mount

2009.10.19
1.Change PC319 from 1C-2B20104-K301 To 1C-2B20104-K300.
2.change R5703 from 68ohm to 75 ohm
3 NC RP81 for 1R-1010000-JP00
4. MOUNT RP82, RP86 for 1R-1010000-JP00
5. change C5250 from 1C-2B20473-K300 to 1C-2B20102-K001
6. change C6256 from 1C-2B20102-K001 to 1C-2B20473-K300

2009.10.20
change SPR2 from 4x3 to 7x2.5

2009.10.22
PAGE37:delete C468, C513, U25, R76, R55, R41, R73, C60（NC), TP871,
TP872,TP873,TP876,TP878,TP880,TP874.TP875,TP877,TP879,TP881,
TP882 for PVT
PAGE53:change PC112 from 68U to 47U for power request

2009.10.23
Page 35：deleteJ2,J3
Page 38：delete TP531,TP530,TP532,TP533,TP529,TP520,519,TP518
Page 05：delete R5786
Page 37：add TP690, TP690
PAGE 45,46:change net SD_WP# to SD_WP
Page 35：Add test point TP897,TP898,TP899 for PVT

page 35：add TP900,TP901 for +3VRUN

2009.10.28
page 57: Change PC344 to 1C-2B70226-M100.
Add PC345 1C-2B70226-M100.
Change PEX_VDD to 2.5A.

2009.10.30

page 55: Change C_PQ3,C_PQ8 to 17-2N7002W-0000.

page 59: Change PQ61 to 17-2N7002W-0000.

page 61: Change PQ58 to 17-2N7002S-PT00.

page 62: Change C_PQ7 to 17-2N7002S-PT00.
Change PQ10 to 17-2N7002W-0000.
Change PQ9 to 17-2N7002S-PT00.

Page 51:change R5992,R5993,R5994 from 120ohm to 549ohm follow M870

Page 36:change Q9 to 17-2N7002S-PT00.
Page 03:change Q179 to 17-2N7002S-PT00

Page 72 :change SPR2 to 9 X3.5

2009.10.31

page 57: Add PC350 1C-33U0337-KX00 NC_330U_2.5V_K.

Page 14 ：add RP83 NC_0 to escape crosstalk

2009.11.3
Page60：Change PC225 TO mount
page 60: Delete PC62.

page 60: Change PR229 to 1K_J.
Change PC225 to 0.22U_25V_K.

2009.11.03
Page 35:add C60,C62,C63,C64

For EMI request
1:Page 55 change C_PC14 to 4700pf
change C_PC13 to 0.1U
2: Page 55 change C_PC156 to 2200pf
3.Page 63 change A_C23,A_C22 from 15PF to 22PF

2009.11.4
Page 35:add C65,C66,C67,C73,C74 for FAN issue

page 55: Change C_EC6066 to 1C-2B30104-K000.

page 56: Add TP442.

page 56: Change E_C6060 to 1C-2B30104-K000.
Change E_C6059 to 1C-2B30104-K000.
Change E_C6067 to 1C-2B30104-K000.
Change E_C6068 to 1C-2B30104-K000.
Change E_C6062 to 1C-2B30104-K000.
Change E_C6061 to 1C-2B30104-K000.

2009.11.16
change C_PC14, C_PC156 to 1000P for EMI request

2009.11.19
Page49: Change R6009 from 1R-0000000-J200 to 1R-0000101-J200 for RF request

2009.11.19
Page 55: Add C_PQ26,C_PQ27,C_PQ9 NC_TPCC8102 for 2nd source.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
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