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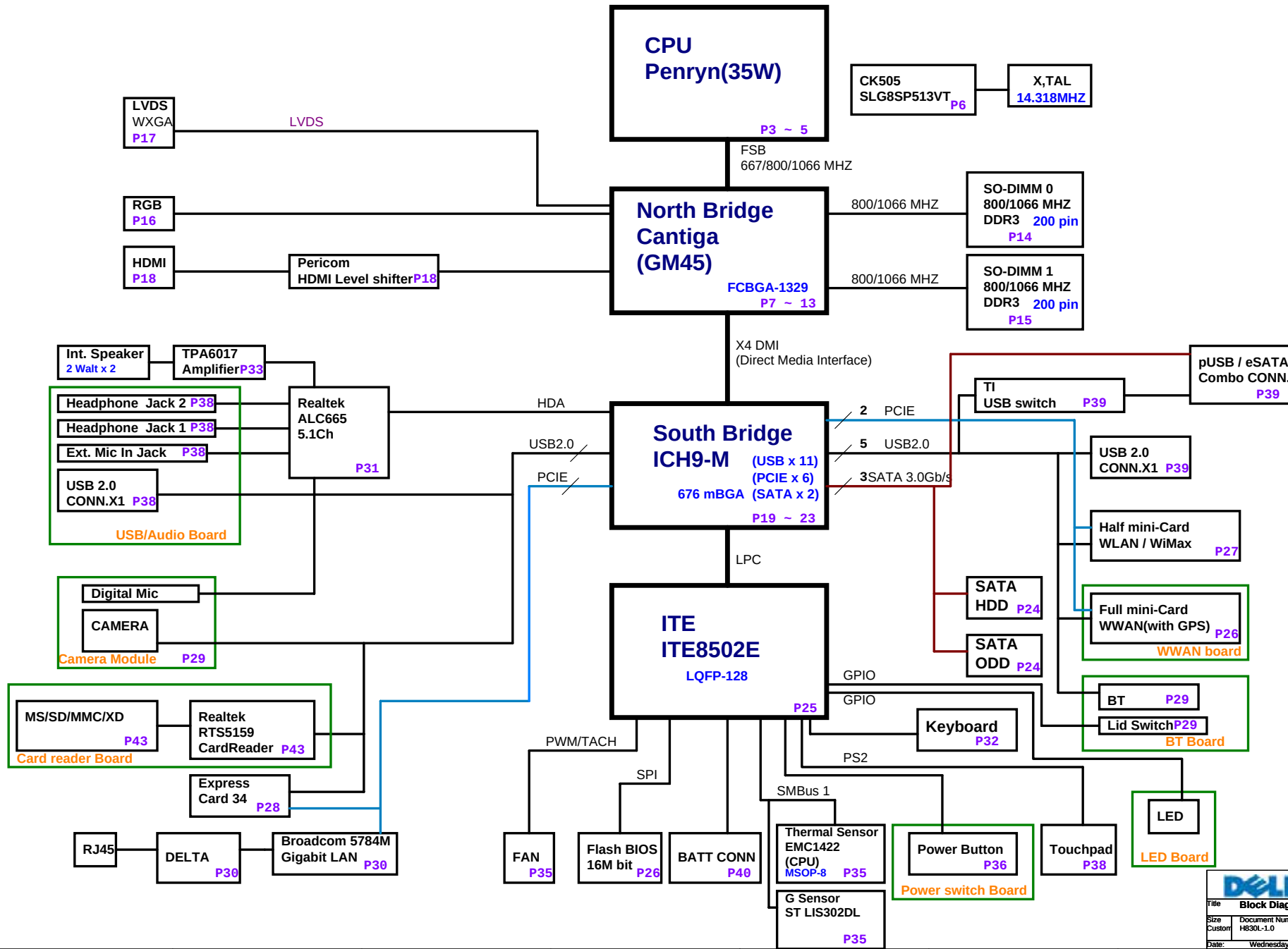
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11	Cantiga (POWER,VCC) 5/7	1.0	09'0410	46	Others power plane	1.0	09'0410
12	Cantiga (VCC CORE) 6/7	1.0	09'0410	47	HOLE	1.0	09'0410
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Project Code & Schematics Subject: H830-L Main Board 6L

PCB P/N:	1P-0093200-6010 (NANYA) 1P-0093J00-6010 (IRIS) 1P-0093500-6010 (HANNSTAR)
BT DB P/N:	1P-1093200-6010 (NANYA) 1P-1093J03-6010 (IRIS) 1P-1093503-6010 (HANNSTAR)
LED DB P/N:	1P-1093201-6010 (NANYA) 1P-1093J01-6010 (IRIS) 1P-1093502-6010 (HANNSTAR)
P/B DB P/N:	1P-1093202-6010 (NANYA) 1P-1093J00-6010 (IRIS) 1P-1093501-6010 (HANNSTAR)

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H830(Montevina UMA)



7 H_A#[3..35]

7 H_ADSTB#0
7 H_REQ#[4..0]

7 H_ADSTB#1

20 H_A20M#
20 H_FERR#
20 H_IGNNE#

20 H_STPCLK#
20 H_INTR#
20 H_NMI#
20 H_SMI#

TP22 tpc20	1	TP CPU RSVD01	M4
TP25 tpc20	1	TP CPU RSVD02	N5
TP13 tpc20	1	TP CPU RSVD03	T2
TP18 tpc20	1	TP CPU RSVD04	V3
TP5 tpc20	1	TP CPU RSVD05	B2
TP21 tpc20	1	CPU TEST7	C3
TP12 tpc20	1	TP CPU RSVD07	D2
TP31 tpc20	1	TP CPU RSVD08	D22
TP17 tpc20	1	TP CPU RSVD09	D3
TP26 tpc20	1	TP CPU RSVD10	F6

H_A#3	J4	A[3]#
H_A#4	L5	A[4]#
H_A#5	L4	A[5]#
H_A#6	K5	A[6]#
H_A#7	M3	A[7]#
H_A#8	N2	A[8]#
H_A#9	J1	A[9]#
H_A#10	N3	A[10]#
H_A#11	P5	A[11]#
H_A#12	P2	A[12]#
H_A#13	L2	A[13]#
H_A#14	P4	A[14]#
H_A#15	P1	A[15]#
H_A#16	R1	A[16]#

H_REQ#0	K3	REQ[0]#
H_REQ#1	H2	REQ[1]#
H_REQ#2	K2	REQ[2]#
H_REQ#3	J3	REQ[3]#
H_REQ#4	L1	REQ[4]#

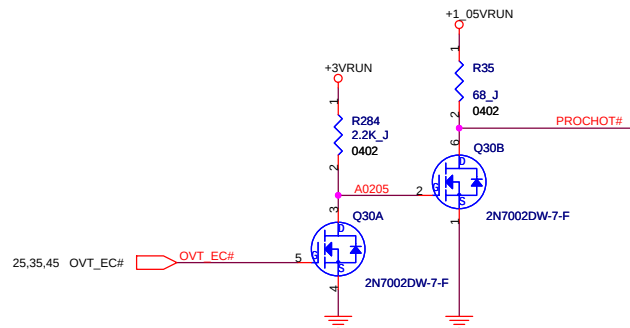
H_A#17	Y2	A[17]#
H_A#18	U5	A[18]#
H_A#19	R3	A[19]#
H_A#20	W6	A[20]#
H_A#21	U4	A[21]#
H_A#22	Y5	A[22]#
H_A#23	U1	A[23]#
H_A#24	R4	A[24]#
H_A#25	T5	A[25]#
H_A#26	T3	A[26]#
H_A#27	W2	A[27]#
H_A#28	W5	A[28]#
H_A#29	Y4	A[29]#
H_A#30	U2	A[30]#
H_A#31	V4	A[31]#
H_A#32	W3	A[32]#
H_A#33	AA4	A[33]#
H_A#34	AB2	A[34]#
H_A#35	AA3	A[35]#

ADSTB#0	M1	ADSTB[0]#
ADSTB#1	V1	ADSTB[1]#

A20M#	A6	A20M#
FERR#	A5	FERR#
IGNNE#	C4	IGNNE#

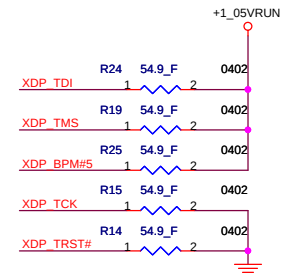
H_STPCLK#	D5	H_STPCLK#
LINT0	C6	LINT0
LINT1	B4	LINT1
SMI#	A3	SMI#

CPU SOCKET_478P
FOX_P24782A-274M-01



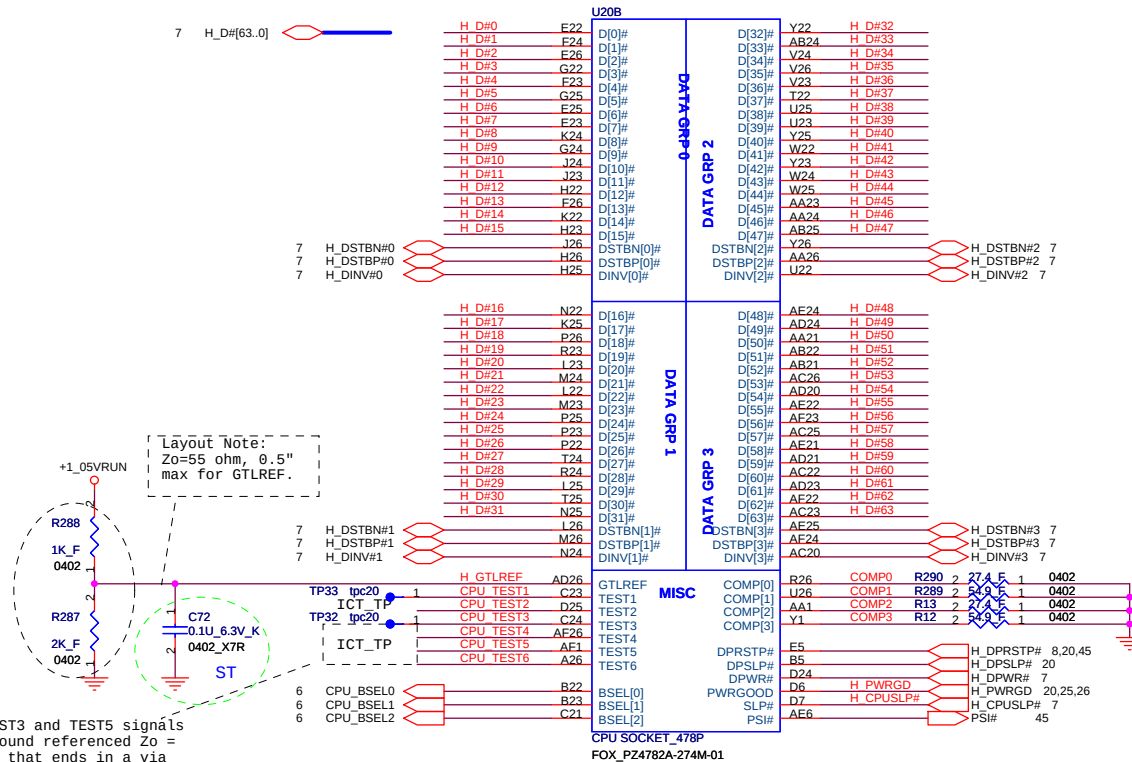
ADDR GROUP 0
ADDR GROUP 1
XDP/TP SIGNALS
THERMAL
H CLK
RESERVED

ADS#	H1	H_ADS#	7
BNR#	E2	H_BNR#	7
BPR#	G5	H_BPR#	7
DEFER#	H5	H_DEFER#	7
DRDY#	F21	H_DRDY#	7
DBSY#	E1	H_DBSY#	7
BR0#	F1	H_BREQ#0	7
IERR#	D20	H_IERR#	7
INIT#	B3	H_INIT#	20
LOCK#	H4	H_LOCK#	7
RESET#	C1	H_CPURST#	7,26
RS[0]#	E3	H_RS#0	7
RS[1]#	F4	H_RS#1	7
RS[2]#	G3	H_RS#2	7
TRDY#	G2	H_TRDY#	7
HIT#	G6	H_HIT#	7
HITM#	F4	H_HITM#	7
BPM[0]#	AD4	XDP_BPM#0	1
BPM[1]#	AD3	XDP_BPM#1	1
BPM[2]#	AD1	XDP_BPM#2	1
BPM[3]#	AC4	XDP_BPM#3	1
PRDY#	AC2	XDP_BPM#4	1
PREQ#	AC1	XDP_BPM#5	1
TCK	AA6	XDP_TCK	1
TDI	AB3	XDP_TDI	1
TDO	AB5	XDP_TDO	1
TMS	AB6	XDP_TMS	1
TRST#	AB6	XDP_TRST#	1
DBR#	C20	XDP_DBR#	1
PROCHOT#	D21	PROCHOT#	35
H_THERMDA	A24	H_THERMDA	35
H_THERMDC	B25	H_THERMDC	35
PM_THRMTRIP#	C7	PM_THRMTRIP#	8,20,25
CLK_CPU_BCLK	A22	CLK_CPU_BCLK	6
CLK_CPU_BCLK	A21	CLK_CPU_BCLK	6

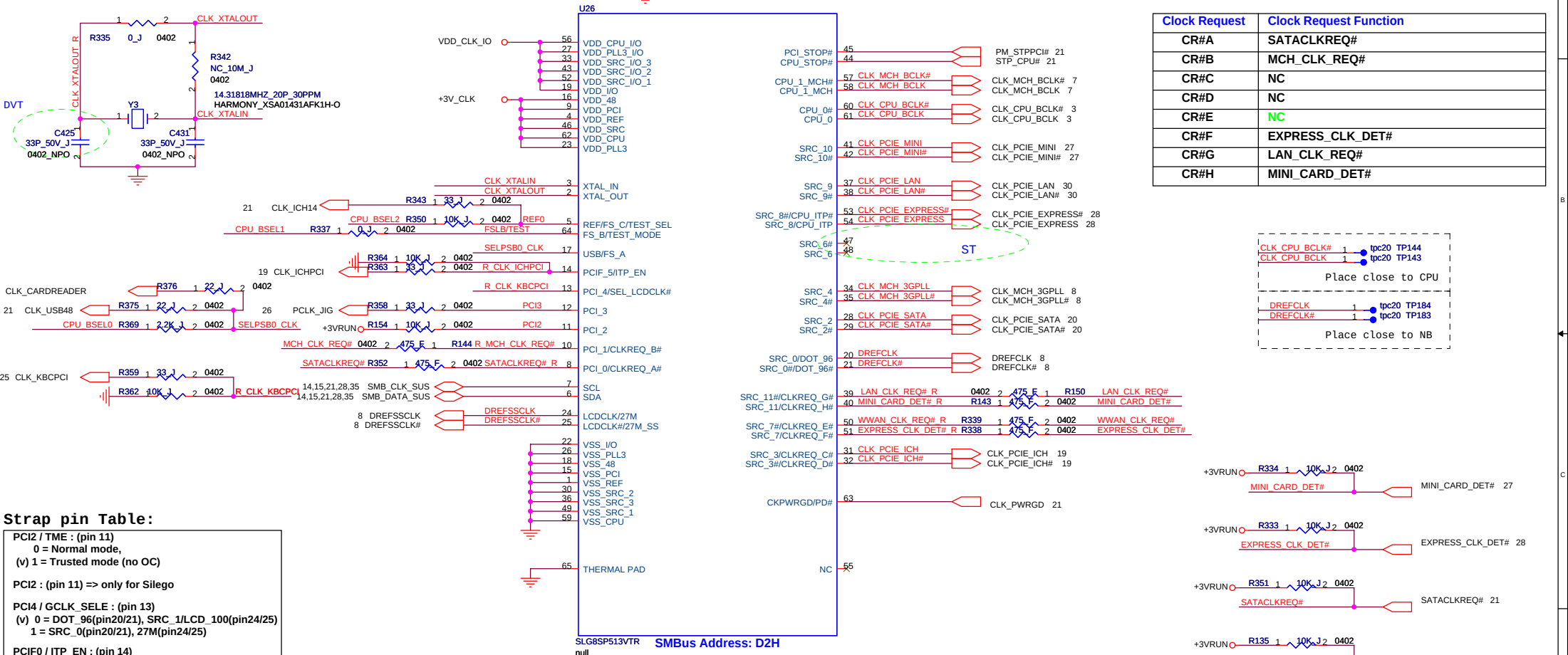
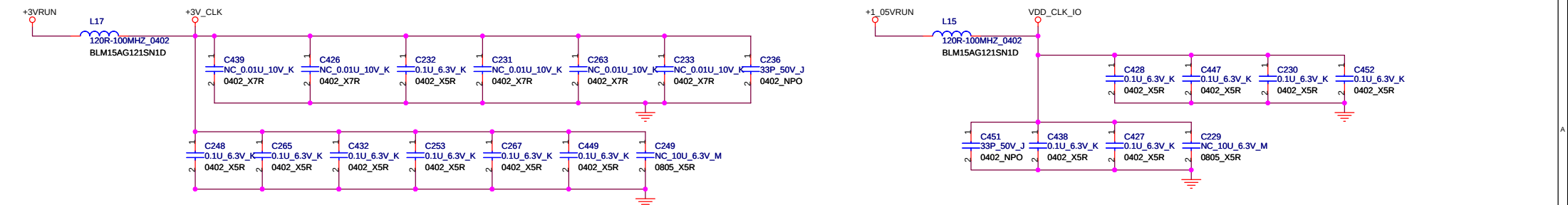


Place close to CPU

Route the TEST3 and TEST5 signals through a ground referenced $Z_o = 55\text{-ohm}$ trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.



Layout Note:
Comp0,2 connect with $Z_o = 27.4\text{ ohm}$, make trace length shorter then $0.5''$. Width=18mil(MS)
Comp1,3 connect with $Z_o = 55\text{ ohm}$, make trace length shorter then $0.5''$. Width=5mil(MS)



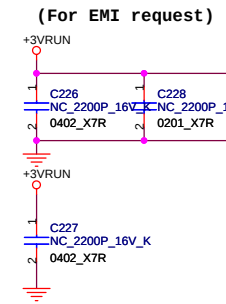
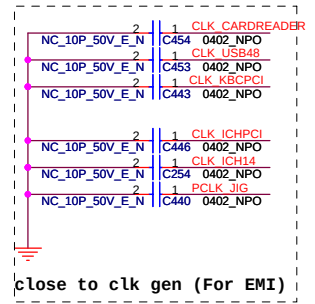
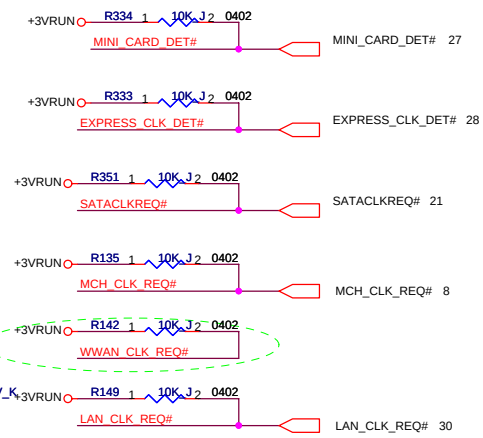
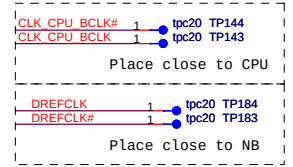
Strap pin Table:

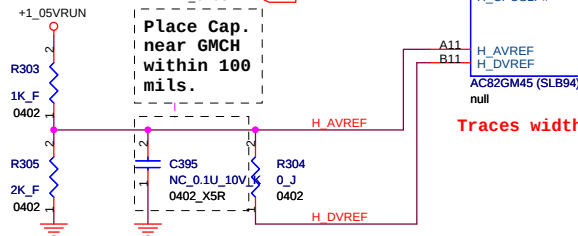
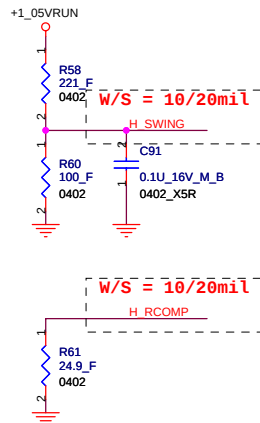
PCI2 / TME : (pin 11)
0 = Normal mode,
(v) 1 = Trusted mode (no OC)
PCI2 : (pin 11) => only for Silego
PCI4 / GCLK_SELE : (pin 13)
(v) 0 = DOT_96(pin20/21), SRC_1/LCD_100(pin24/25)
1 = SRC_0(pin20/21), 27M(pin24/25)
PCI_F0 / ITP_EN : (pin 14)
(v) 0 = SRC_8
1 = CPU2_ITP

FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

Clock Request	Clock Request Function
CR#A	SATACLKREQ#
CR#B	MCH_CLK_REQ#
CR#C	NC
CR#D	NC
CR#E	NC
CR#F	EXPRESS_CLK_DET#
CR#G	LAN_CLK_REQ#
CR#H	MINI_CARD_DET#





H_D#0	F2	H_D#_0
H_D#1	G8	H_D#_1
H_D#2	F8	H_D#_2
H_D#3	E5	H_D#_3
H_D#4	G2	H_D#_4
H_D#5	H6	H_D#_5
H_D#6	H2	H_D#_6
H_D#7	F6	H_D#_7
H_D#8	D4	H_D#_8
H_D#9	H3	H_D#_9
H_D#10	M9	H_D#_10
H_D#11	M11	H_D#_11
H_D#12	J1	H_D#_12
H_D#13	J2	H_D#_13
H_D#14	N12	H_D#_14
H_D#15	J6	H_D#_15
H_D#16	P2	H_D#_16
H_D#17	L2	H_D#_17
H_D#18	R2	H_D#_18
H_D#19	N9	H_D#_19
H_D#20	L6	H_D#_20
H_D#21	M5	H_D#_21
H_D#22	J3	H_D#_22
H_D#23	N2	H_D#_23
H_D#24	R1	H_D#_24
H_D#25	N5	H_D#_25
H_D#26	N6	H_D#_26
H_D#27	P13	H_D#_27
H_D#28	N8	H_D#_28
H_D#29	L7	H_D#_29
H_D#30	N10	H_D#_30
H_D#31	M3	H_D#_31
H_D#32	Y3	H_D#_32
H_D#33	AD14	H_D#_33
H_D#34	Y6	H_D#_34
H_D#35	Y10	H_D#_35
H_D#36	Y12	H_D#_36
H_D#37	Y14	H_D#_37
H_D#38	Y7	H_D#_38
H_D#39	W2	H_D#_39
H_D#40	AA8	H_D#_40
H_D#41	Y9	H_D#_41
H_D#42	AA13	H_D#_42
H_D#43	AA9	H_D#_43
H_D#44	AA11	H_D#_44
H_D#45	AD11	H_D#_45
H_D#46	AD10	H_D#_46
H_D#47	AD13	H_D#_47
H_D#48	AE12	H_D#_48
H_D#49	AE9	H_D#_49
H_D#50	AA2	H_D#_50
H_D#51	AD8	H_D#_51
H_D#52	AA3	H_D#_52
H_D#53	AD3	H_D#_53
H_D#54	AD7	H_D#_54
H_D#55	AE14	H_D#_55
H_D#56	AE3	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AE3	H_D#_58
H_D#59	AC3	H_D#_59
H_D#60	AE11	H_D#_60
H_D#61	AE8	H_D#_61
H_D#62	AG2	H_D#_62
H_D#63	AD6	H_D#_63

U22A

HOST

H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	F16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
H_A#_8	M16	H_A#8
H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	E17	H_A#14
H_A#_15	P17	H_A#15
H_A#_16	E17	H_A#16
H_A#_17	G20	H_A#17
H_A#_18	B19	H_A#18
H_A#_19	J16	H_A#19
H_A#_20	E20	H_A#20
H_A#_21	H16	H_A#21
H_A#_22	J20	H_A#22
H_A#_23	L17	H_A#23
H_A#_24	A17	H_A#24
H_A#_25	B17	H_A#25
H_A#_26	L16	H_A#26
H_A#_27	C21	H_A#27
H_A#_28	J17	H_A#28
H_A#_29	H20	H_A#29
H_A#_30	B18	H_A#30
H_A#_31	K17	H_A#31
H_A#_32	B20	H_A#32
H_A#_33	P21	H_A#33
H_A#_34	K21	H_A#34
H_A#_35	L20	H_A#35

H_ADS#_0	H12	H_ADS#_0
H_ADS#_1	B16	H_ADS#_1
H_ADS#_2	G17	H_ADS#_2
H_ADS#_3	A9	H_ADS#_3
H_ADS#_4	E11	H_ADS#_4
H_ADS#_5	G12	H_ADS#_5
H_ADS#_6	E9	H_ADS#_6
H_ADS#_7	B10	H_ADS#_7
H_ADS#_8	AH7	H_ADS#_8
H_ADS#_9	AH6	H_ADS#_9
H_ADS#_10	J11	H_ADS#_10
H_ADS#_11	E9	H_ADS#_11
H_ADS#_12	H9	H_ADS#_12
H_ADS#_13	E12	H_ADS#_13
H_ADS#_14	H11	H_ADS#_14
H_ADS#_15	C9	H_ADS#_15

H_DIN#_0	J8	H_DIN#_0
H_DIN#_1	L3	H_DIN#_1
H_DIN#_2	Y13	H_DIN#_2
H_DIN#_3	Y1	H_DIN#_3

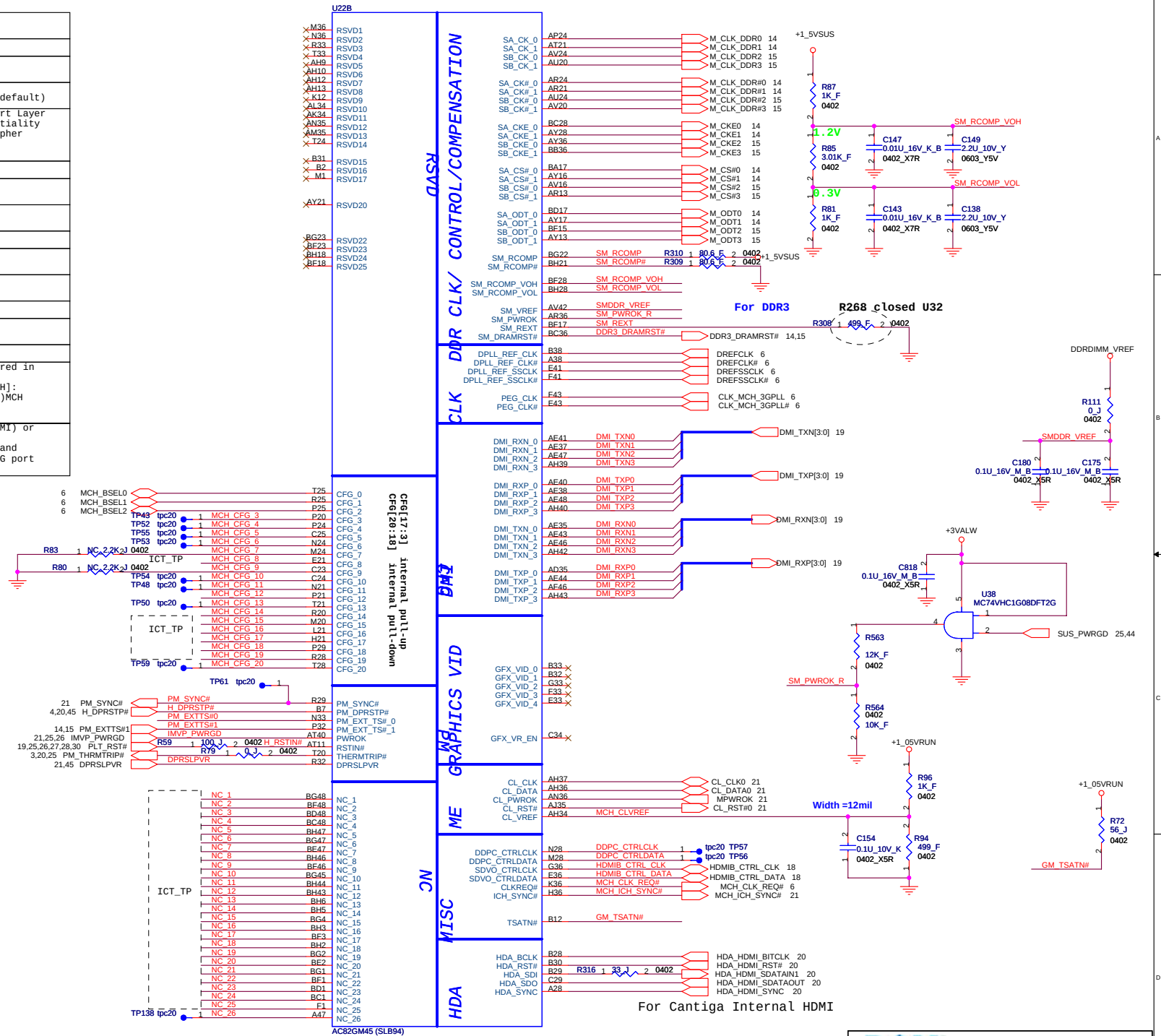
H_DSTBN#_0	L10	H_DSTBN#_0
H_DSTBN#_1	M7	H_DSTBN#_1
H_DSTBN#_2	AA5	H_DSTBN#_2
H_DSTBN#_3	AE6	H_DSTBN#_3

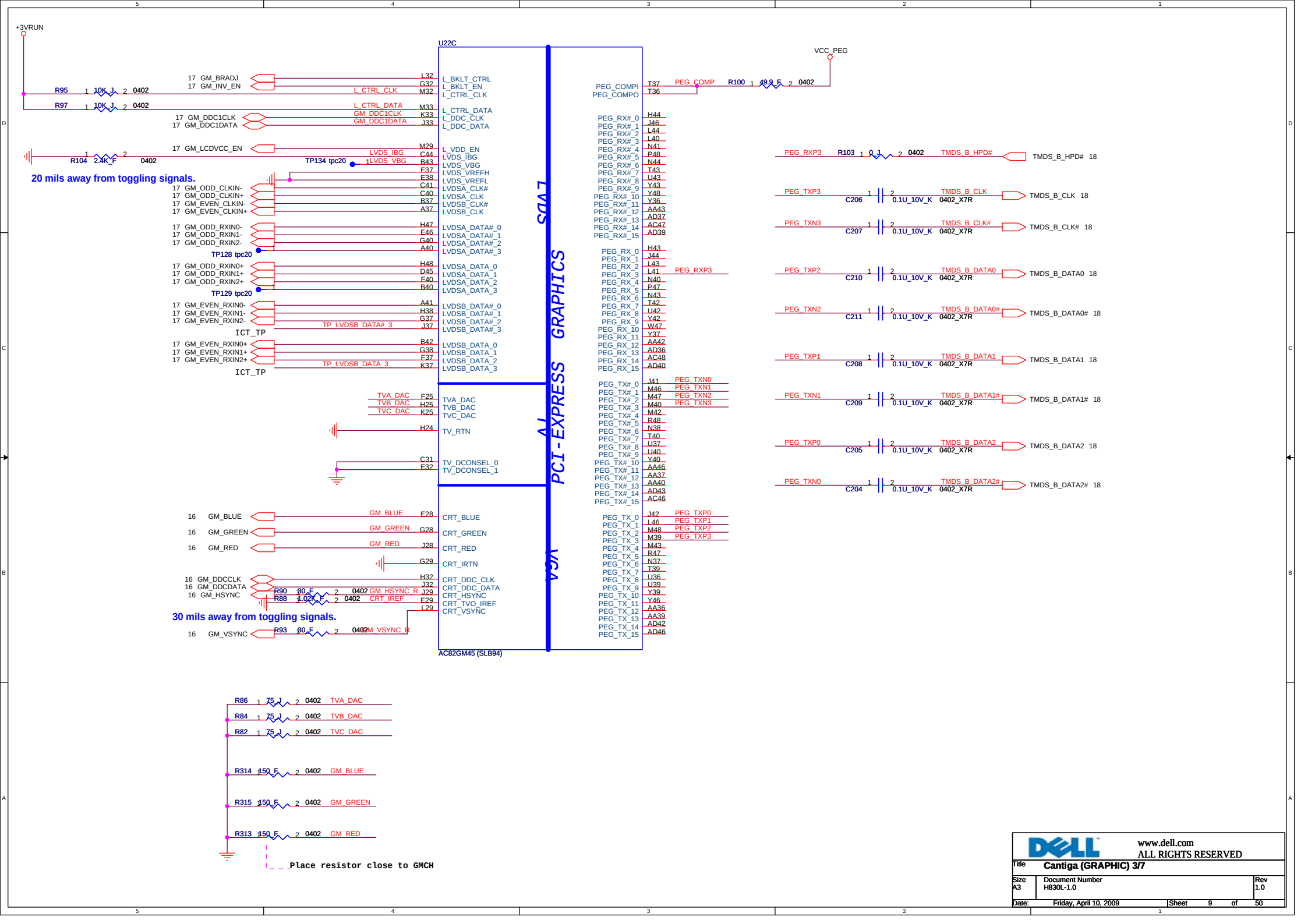
H_DSTBP#_0	L9	H_DSTBP#_0
H_DSTBP#_1	M8	H_DSTBP#_1
H_DSTBP#_2	AA6	H_DSTBP#_2
H_DSTBP#_3	AE5	H_DSTBP#_3

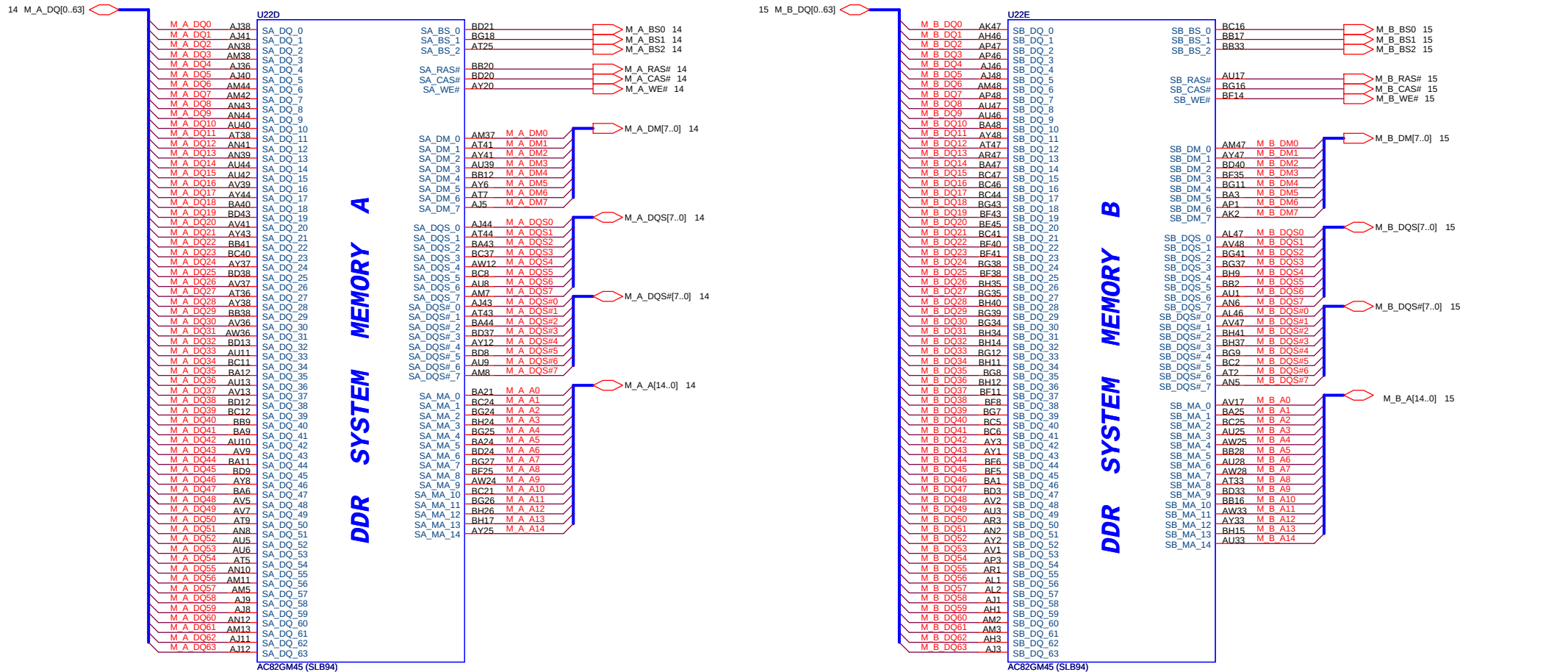
H_REQ#_0	B15	H_REQ#_0
H_REQ#_1	K13	H_REQ#_1
H_REQ#_2	E13	H_REQ#_2
H_REQ#_3	B13	H_REQ#_3
H_REQ#_4	B14	H_REQ#_4

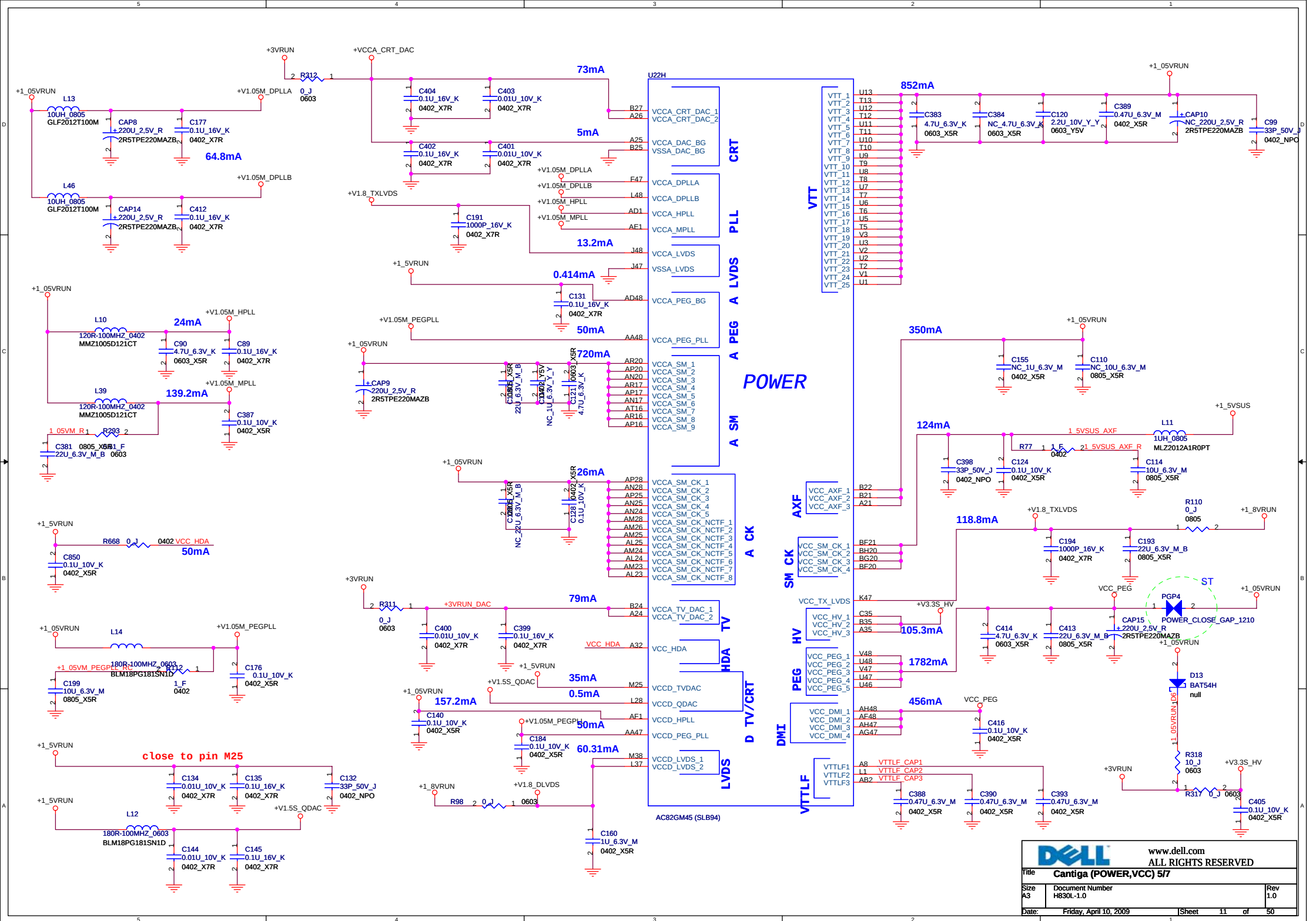
H_RS#_0	B6	H_RS#_0
H_RS#_1	E12	H_RS#_1
H_RS#_2	C8	H_RS#_2

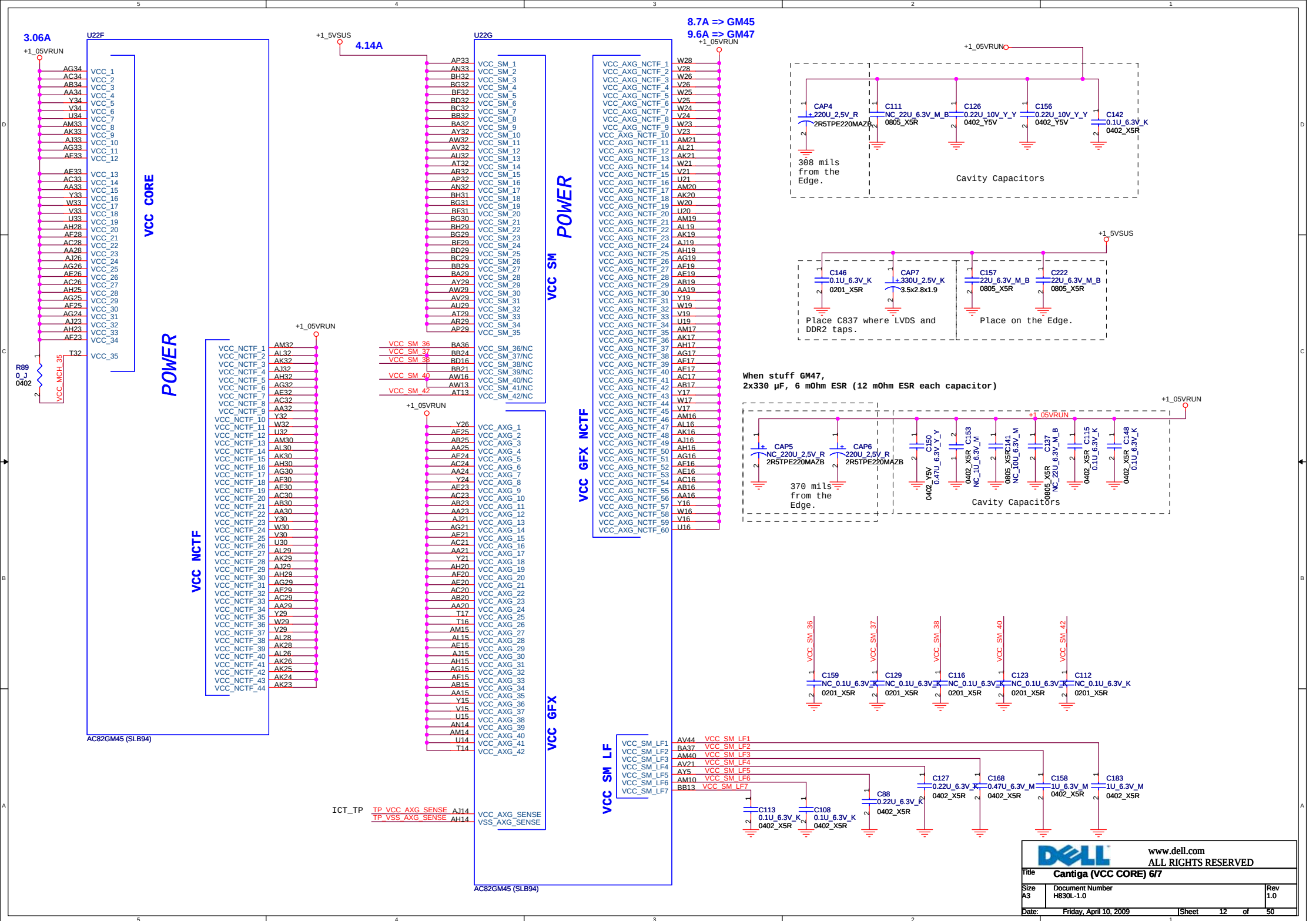
MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIe Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

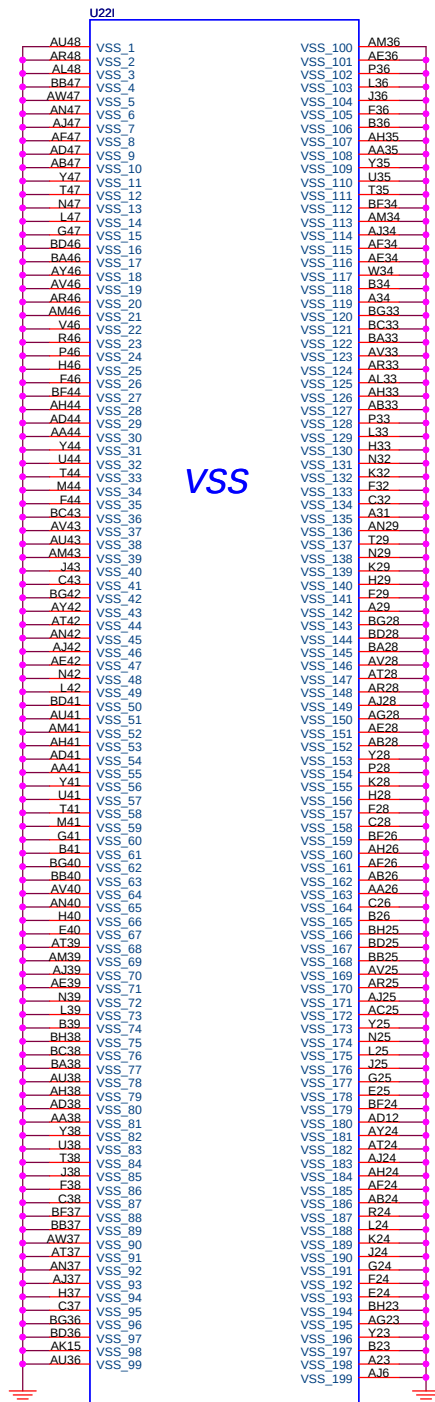




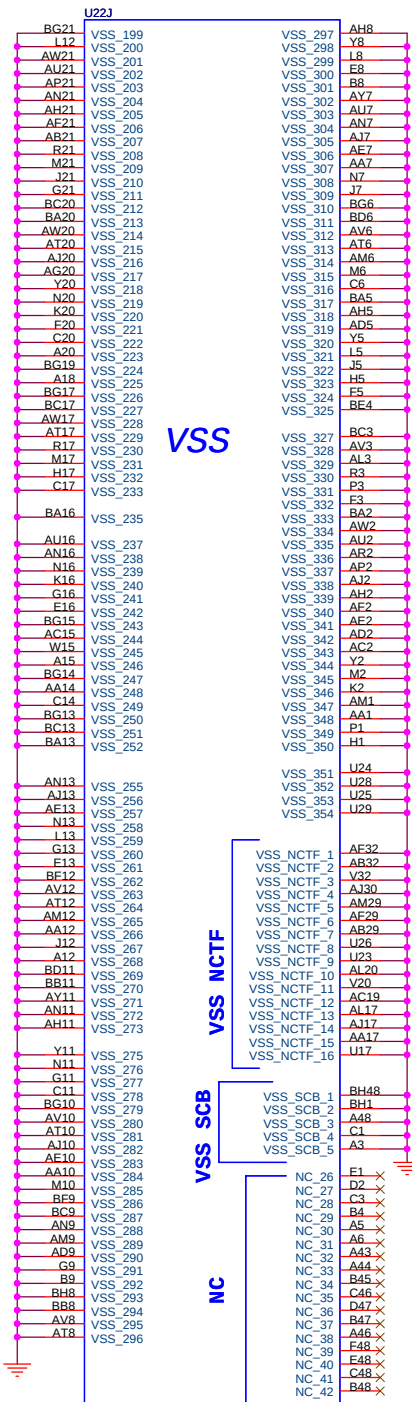




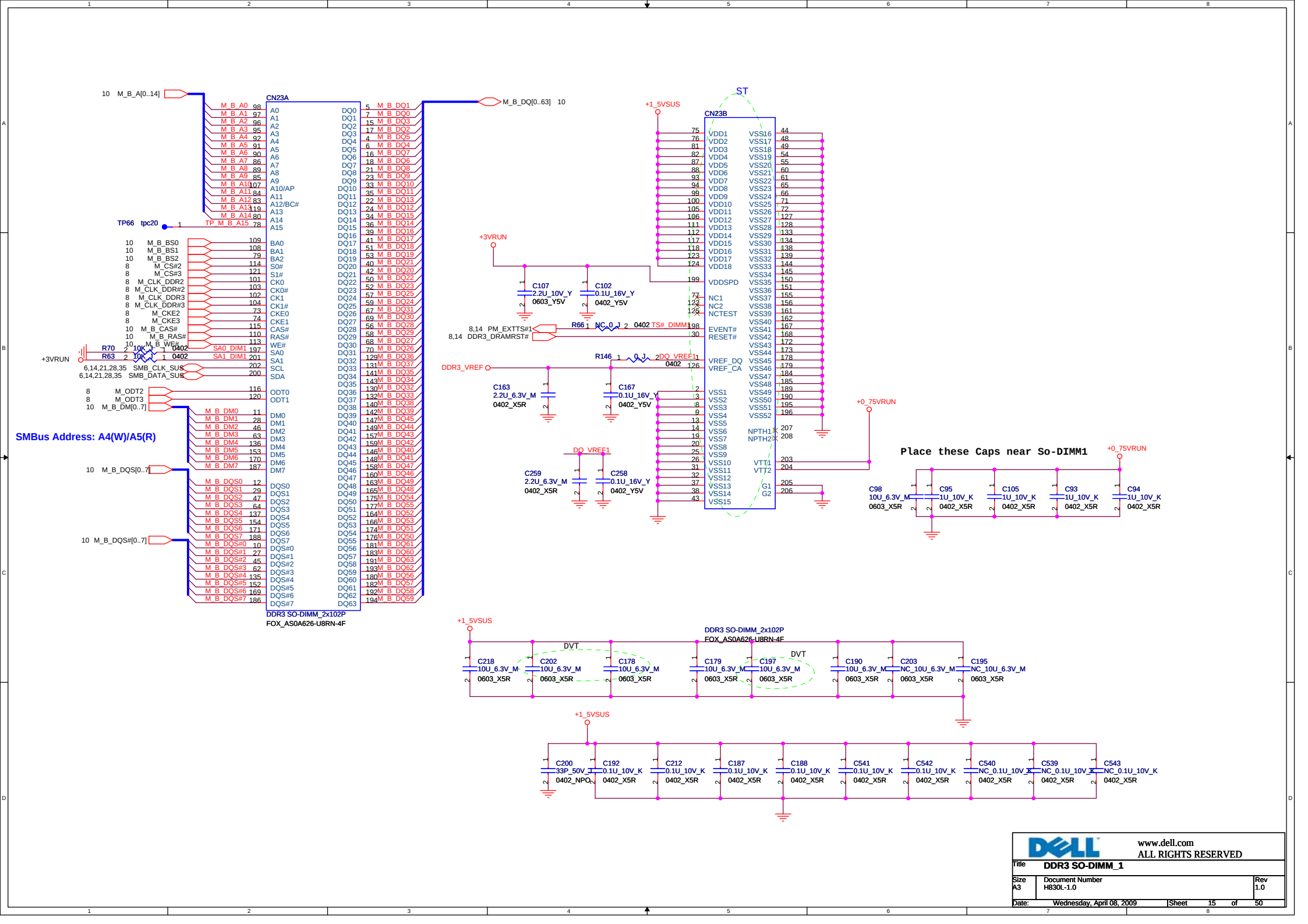


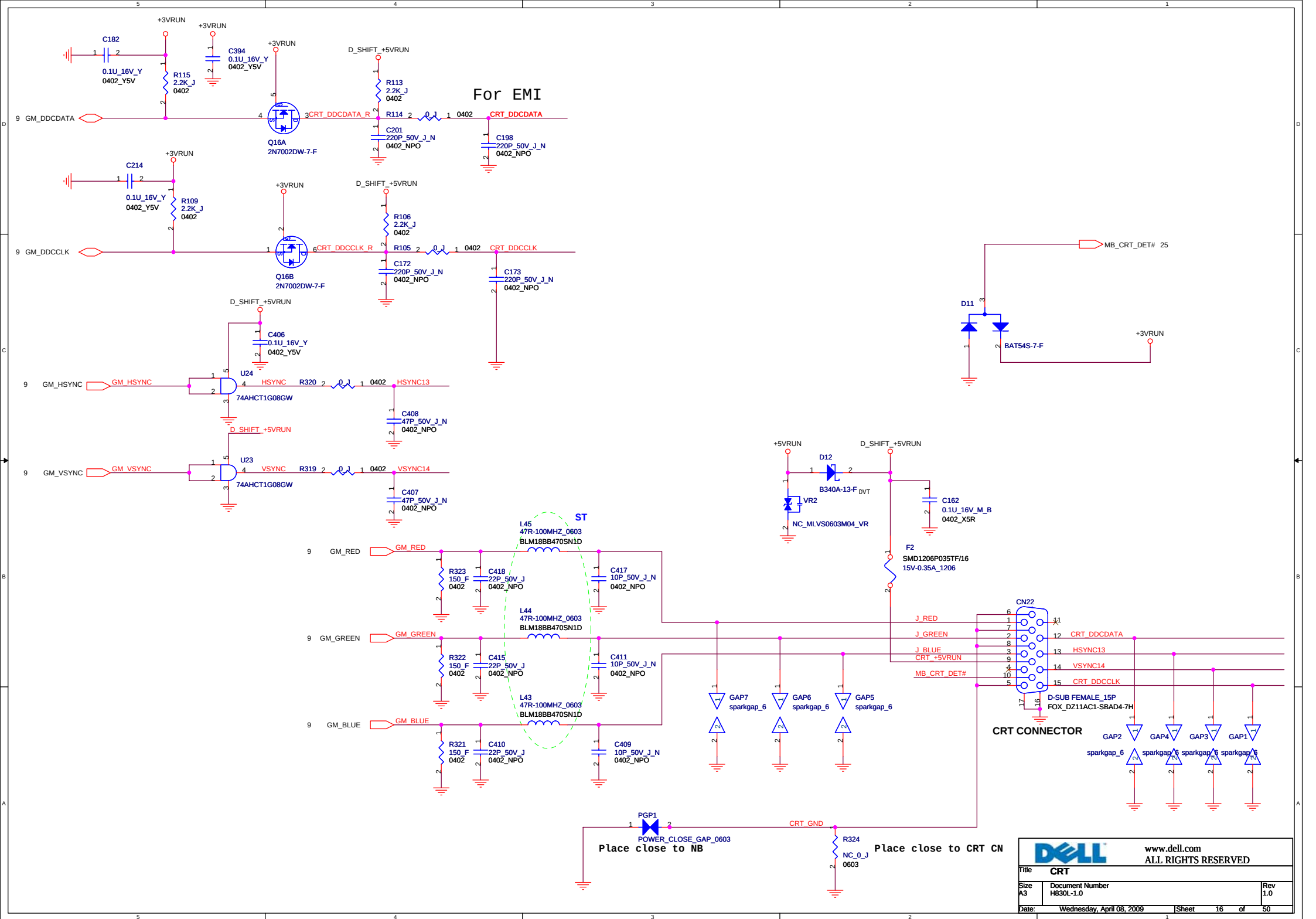


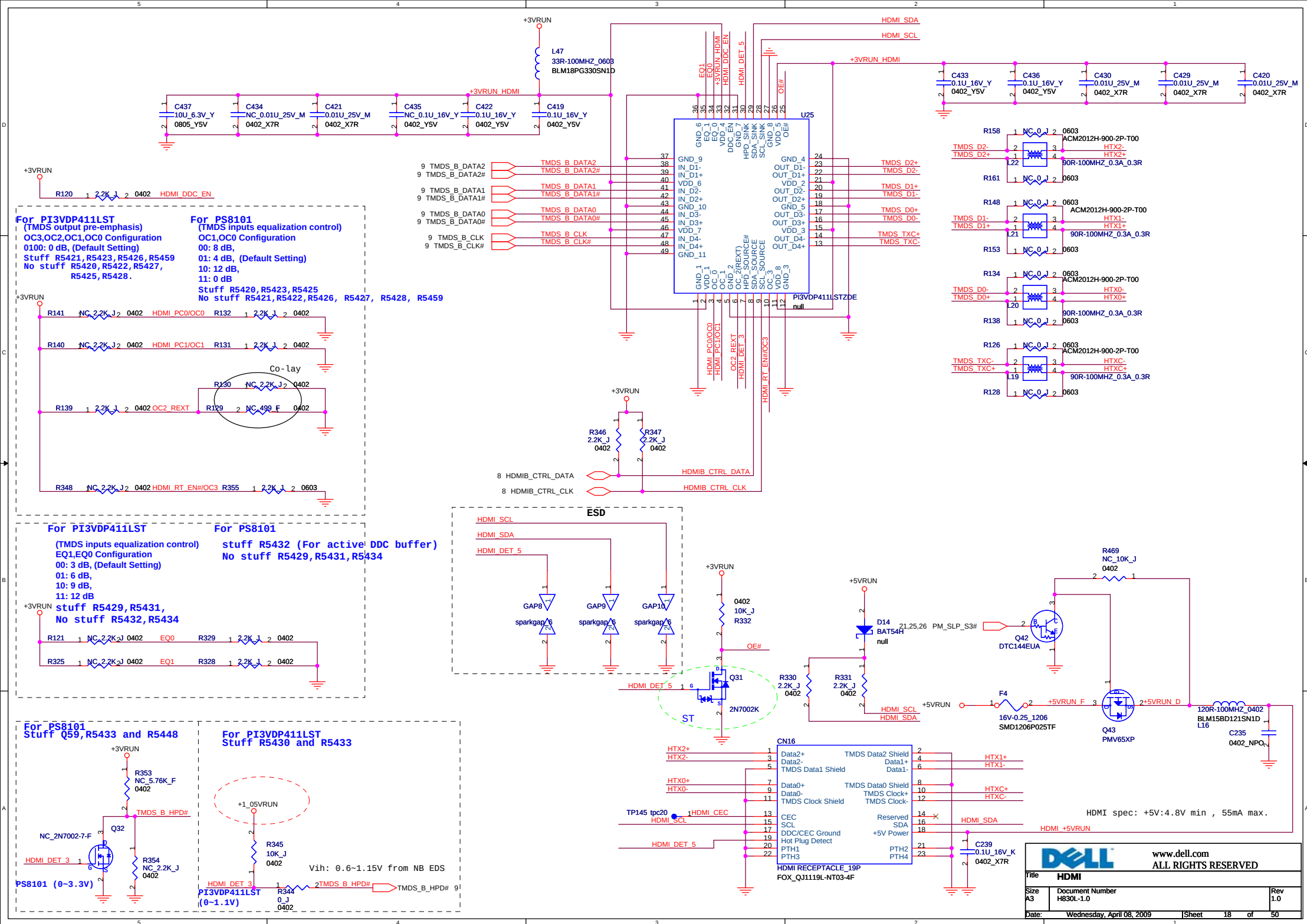
AC82GM45 (SLB94)

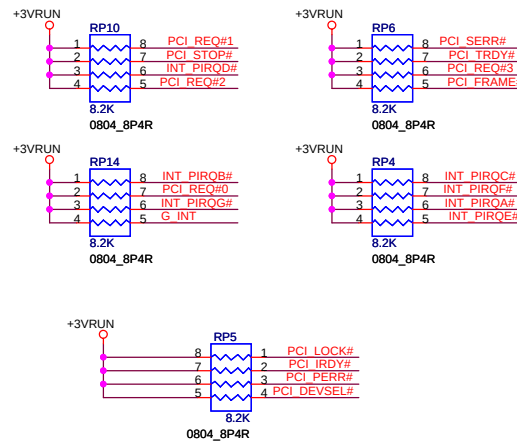


AC82GM45 (SLB94)

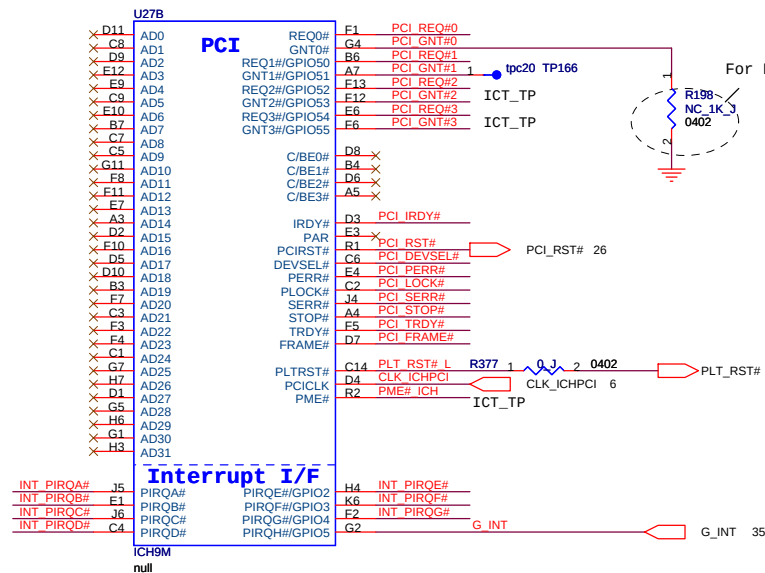








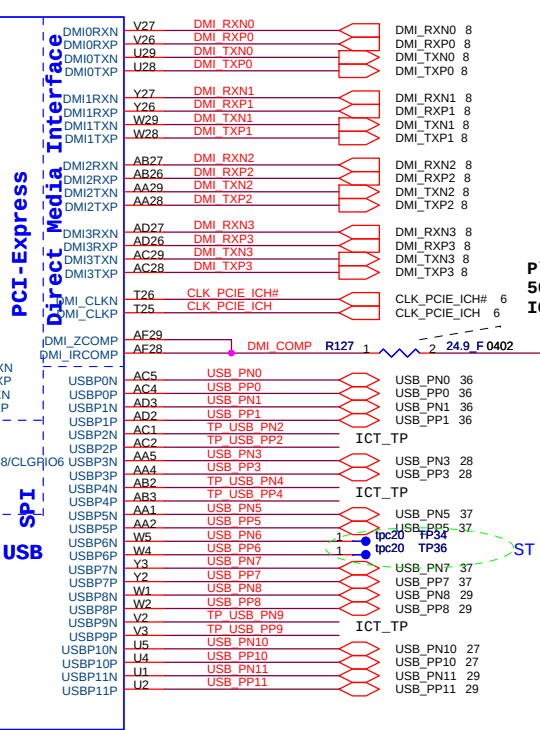
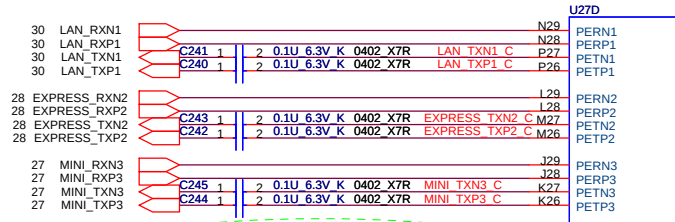
PCI Pullups



Strap for Boot-BIOS

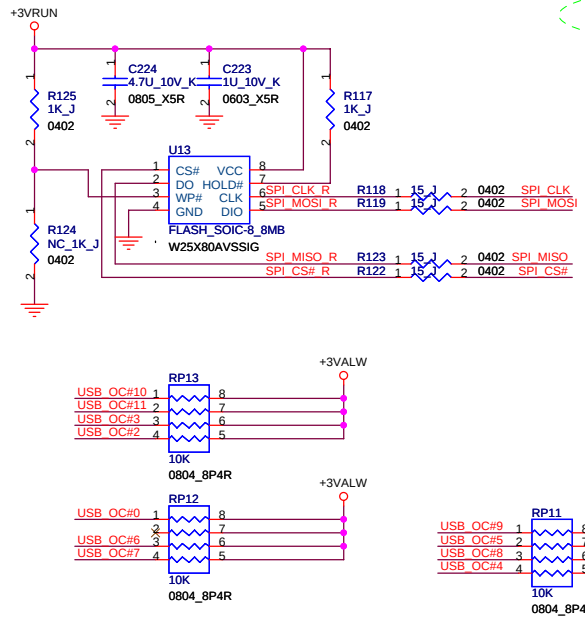
	GNT0#	SPI_CS1#
LPC(Default)	H1	H1
PCI	H1	LOW
SPI	LOW	H1

LAN
Express Card
WLAN

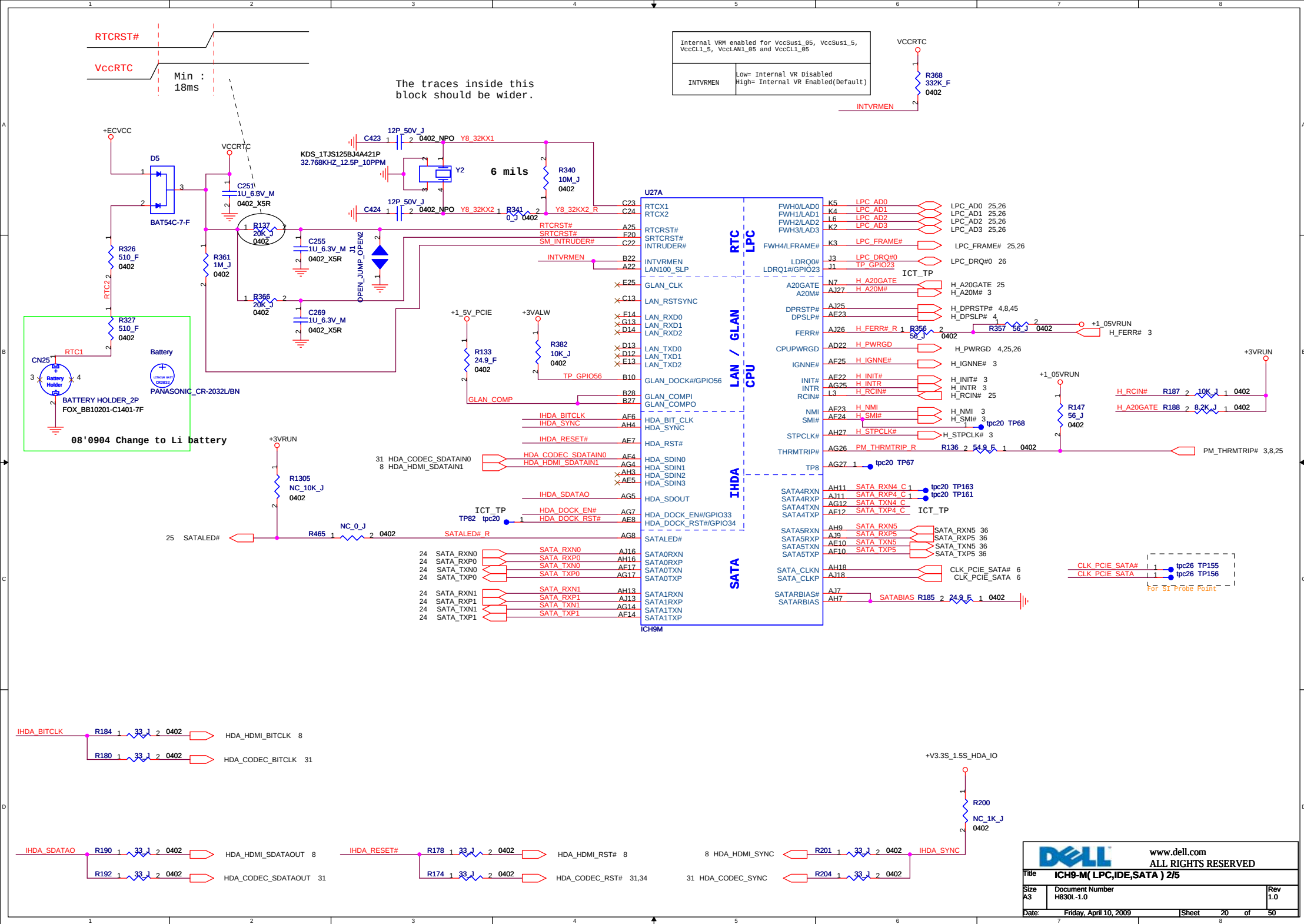


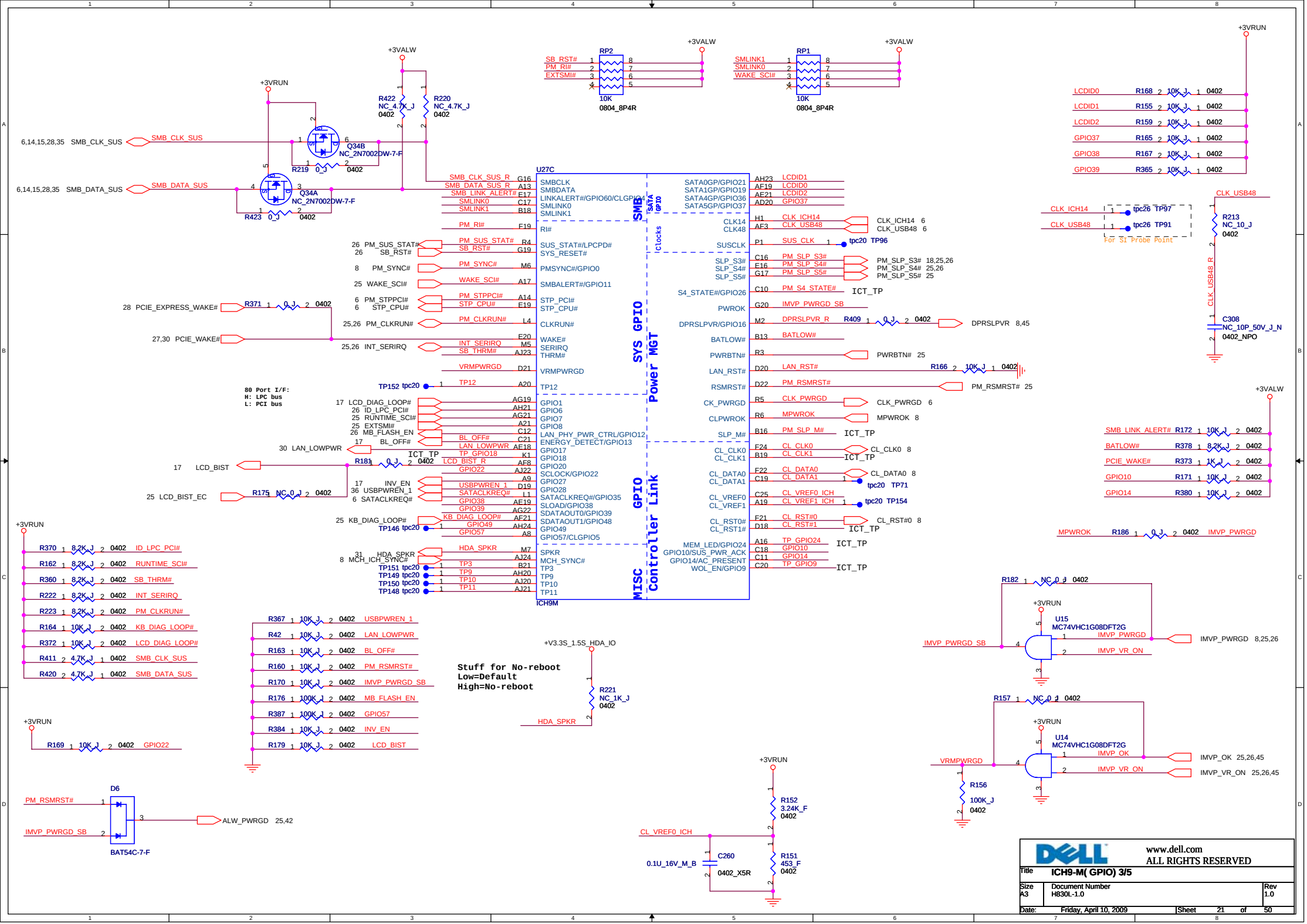
Place within 500 mils of ICH

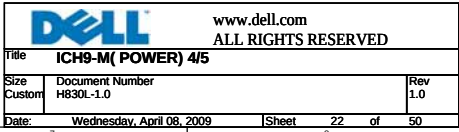
USB PORT	Function
PORT-0	Ext. Port
PORT-1	Ext. Port
PORT-2	
PORT-3	EXPRESS CARD
PORT-4	
PORT-5	Ext. Port
PORT-6	ST
PORT-7	Card reader
PORT-8	Bluetooth
PORT-9	
PORT-10	WLAN/WiMAX
PORT-11	Camera

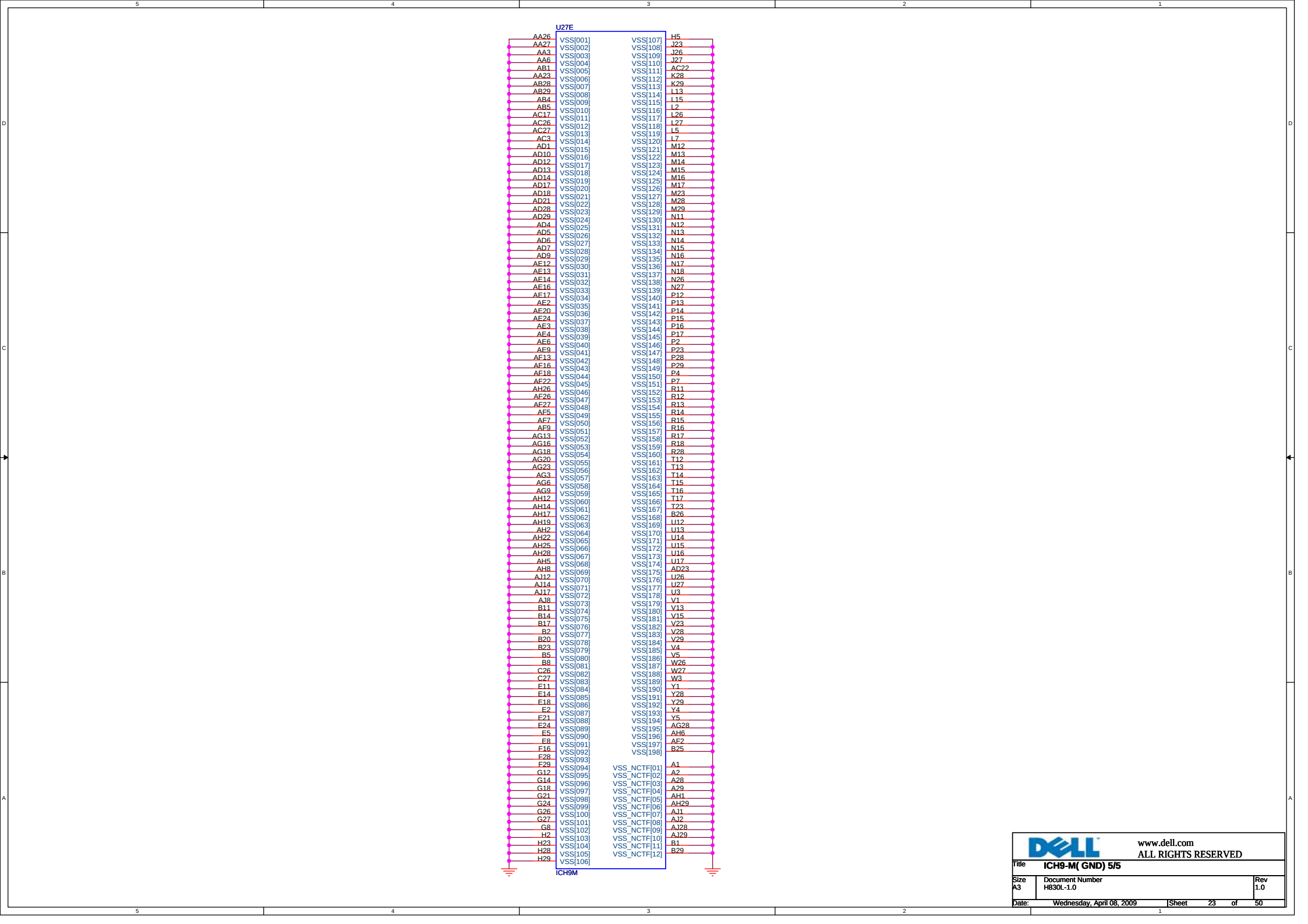


Place within 500 mils of ICH and don't routing next to high speed signals

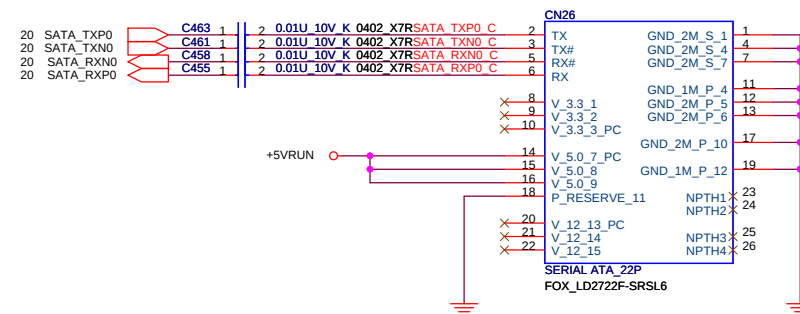
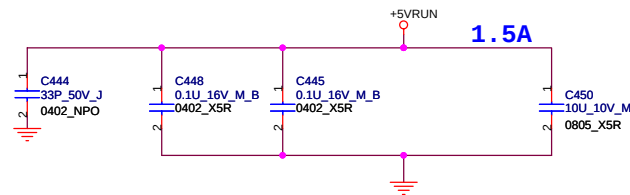




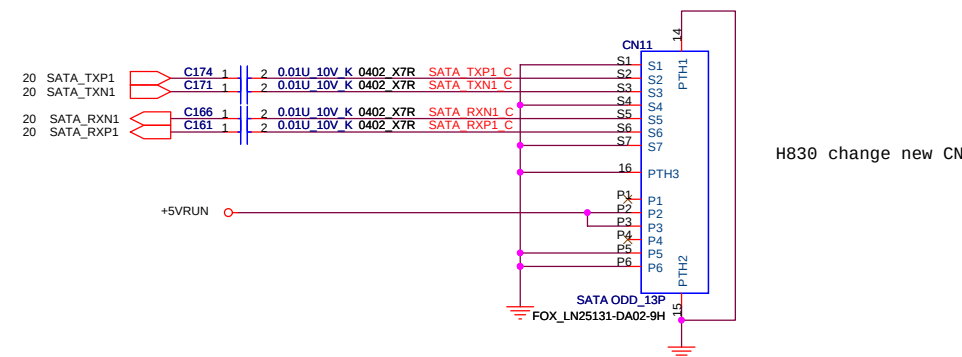
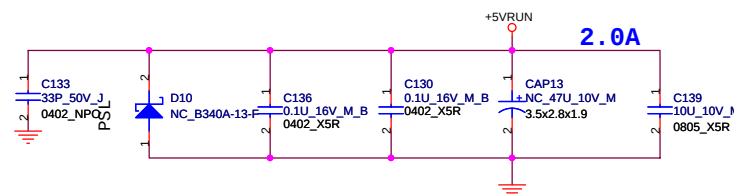




SATA HDD CONN

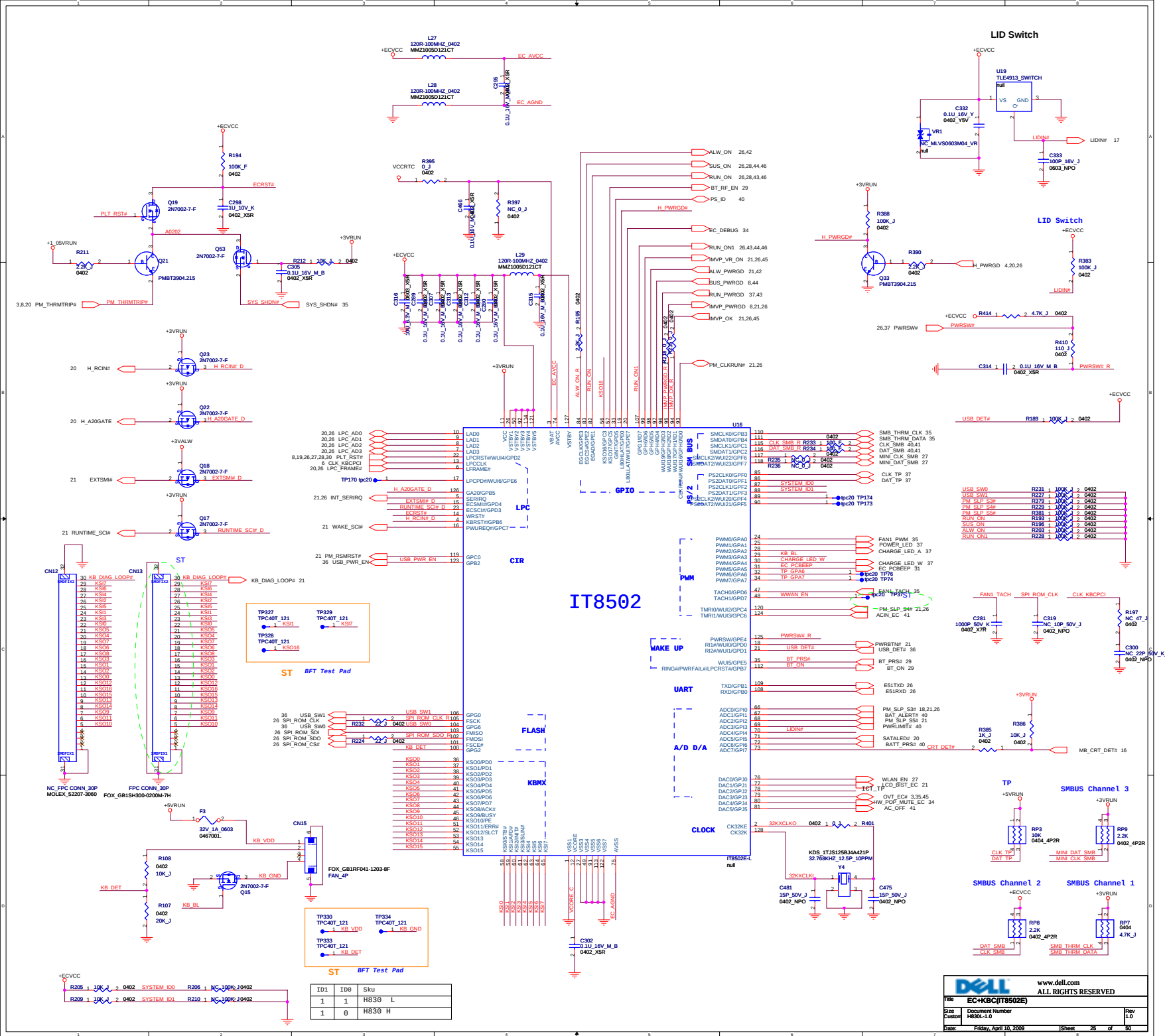


SATA ODD CONN



ODD CON ADAPTER

Add CN68 need 2N-0013009-FKG0 in BOM



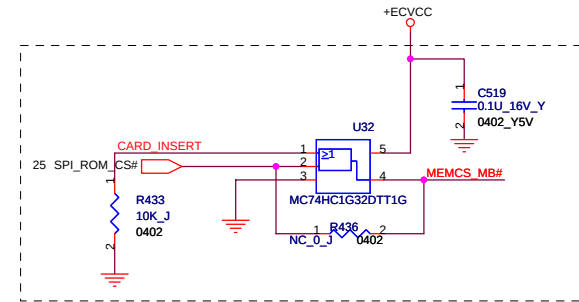
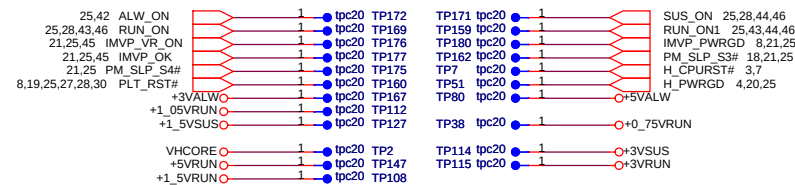
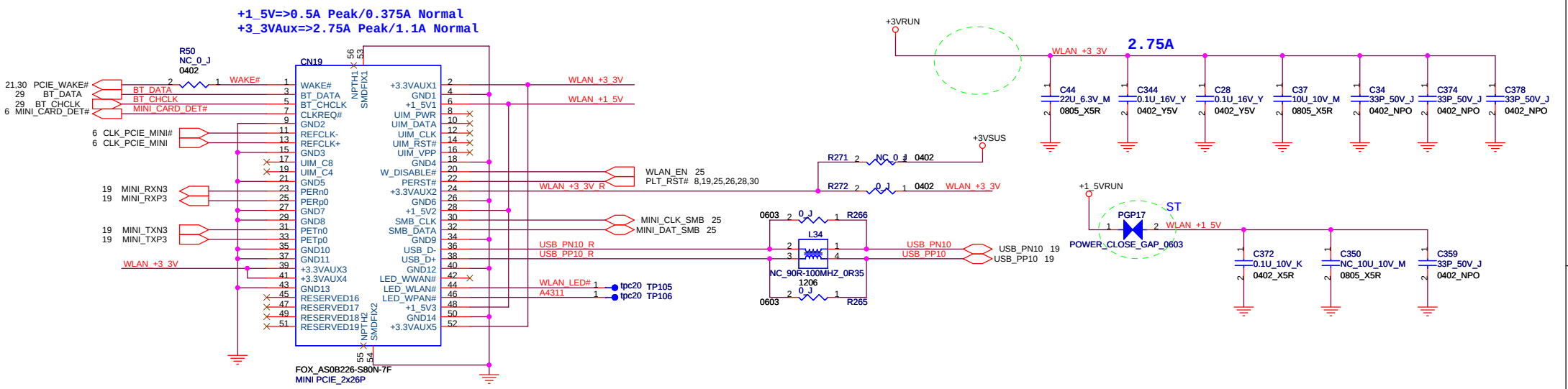
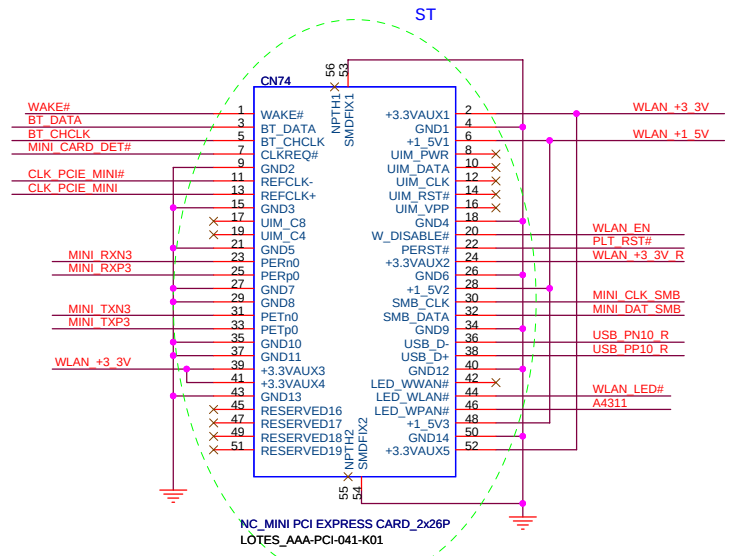


Diagram illustrating the External SPI ROM Interface. The SPI ROM is connected to the ST microcontroller via the PFC CONN_12P connector. The SPI ROM pins are: 12 (SCLK), 11 (SDO), 10 (SDI), 9 (CS#), 8 (MB_FLASH_EN), 7 (CARD_INSERT), 6 (GND), 5 (GND), 4 (GND), 3 (GND), 2 (GND), 1 (GND). The ST microcontroller pins are: 14 (VCC), 13 (GND), 12 (SCLK), 11 (SDO), 10 (SDI), 9 (CS#), 8 (MB_FLASH_EN), 7 (CARD_INSERT), 6 (GND), 5 (GND), 4 (GND), 3 (GND), 2 (GND), 1 (GND). The ST microcontroller is labeled 'ST' and 'FOX_GB5RF120-1203M-7F'. The PFC CONN_12P connector is labeled 'PFC CONN_12P'. The SPI ROM is labeled 'SPI ROM'.

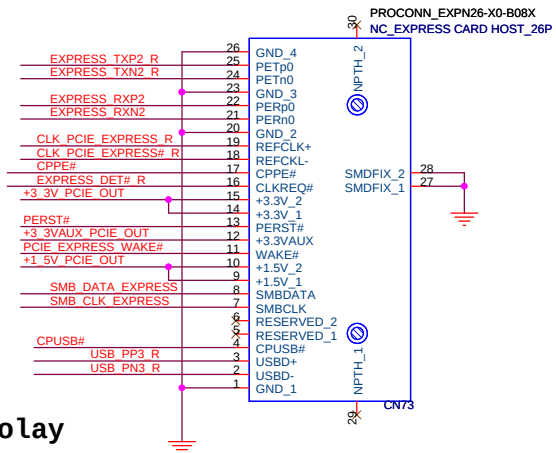




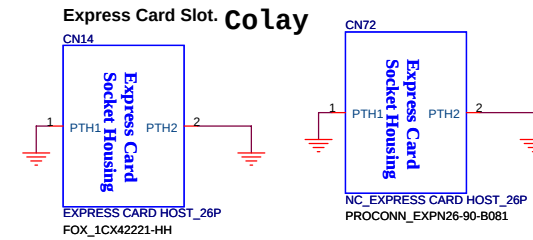
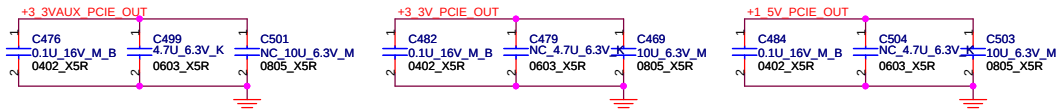
Half Mini Card for WLAN or WiMAX

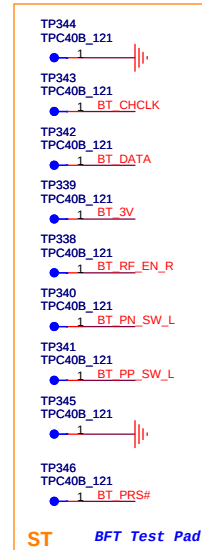
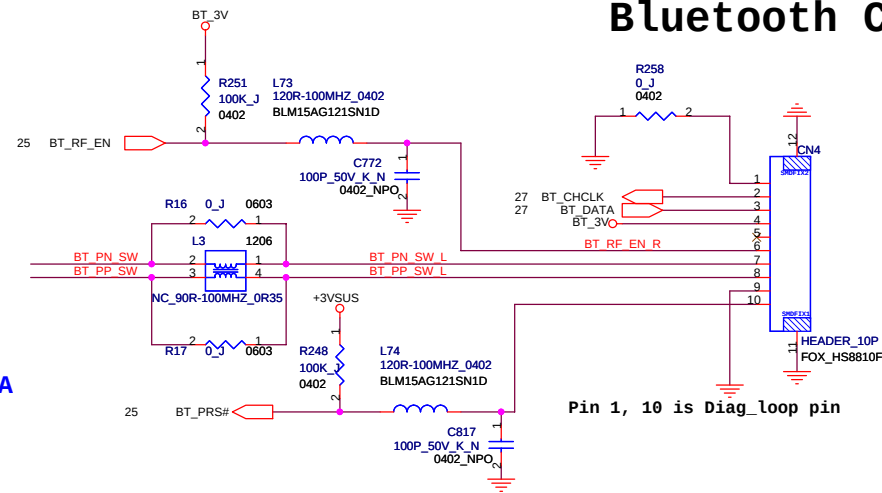
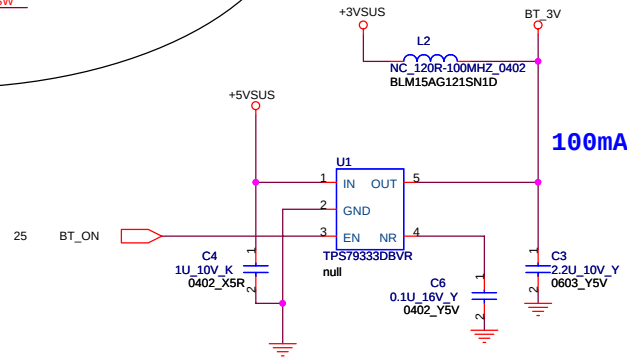
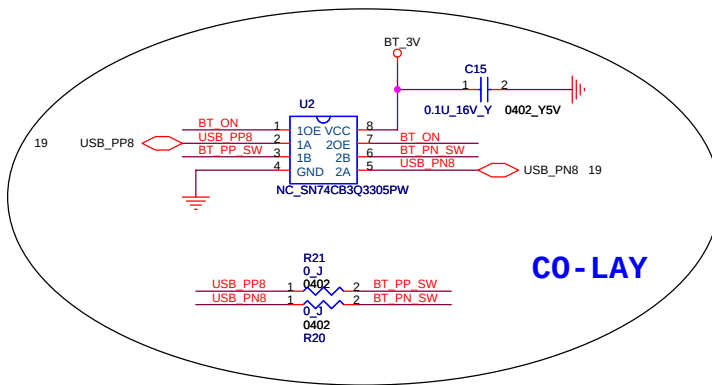


Colay: Half Mini Card CN second source



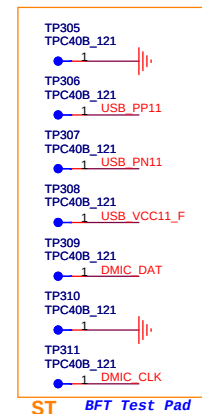
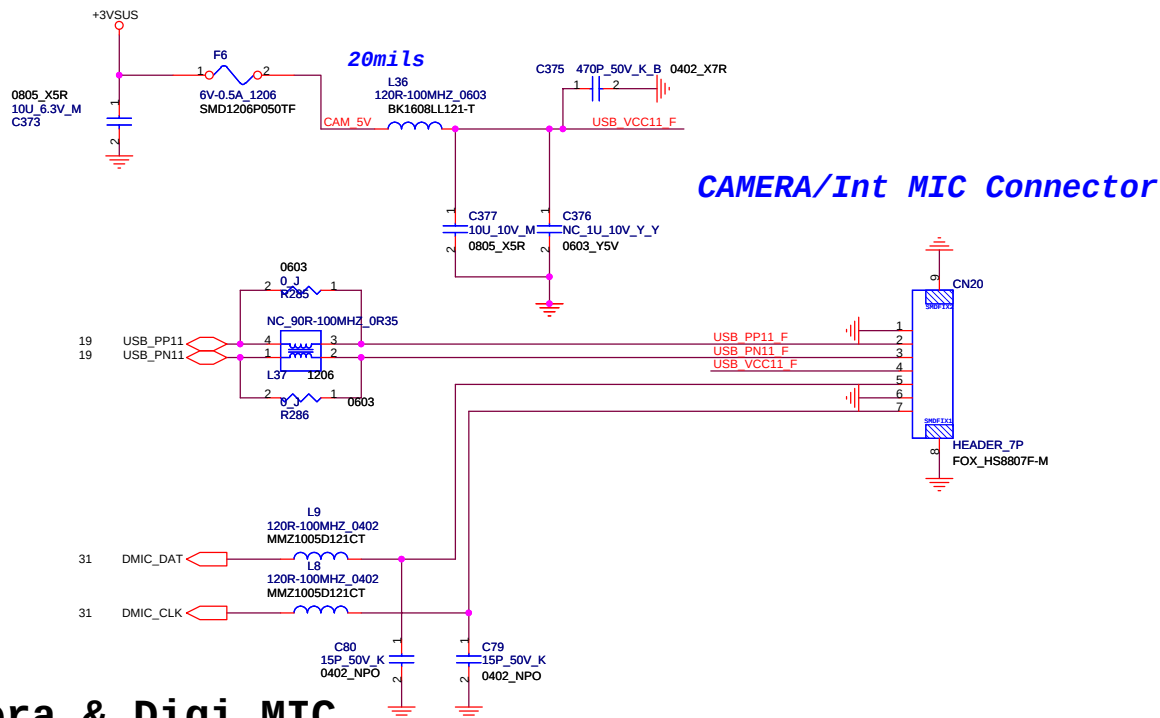
Colay



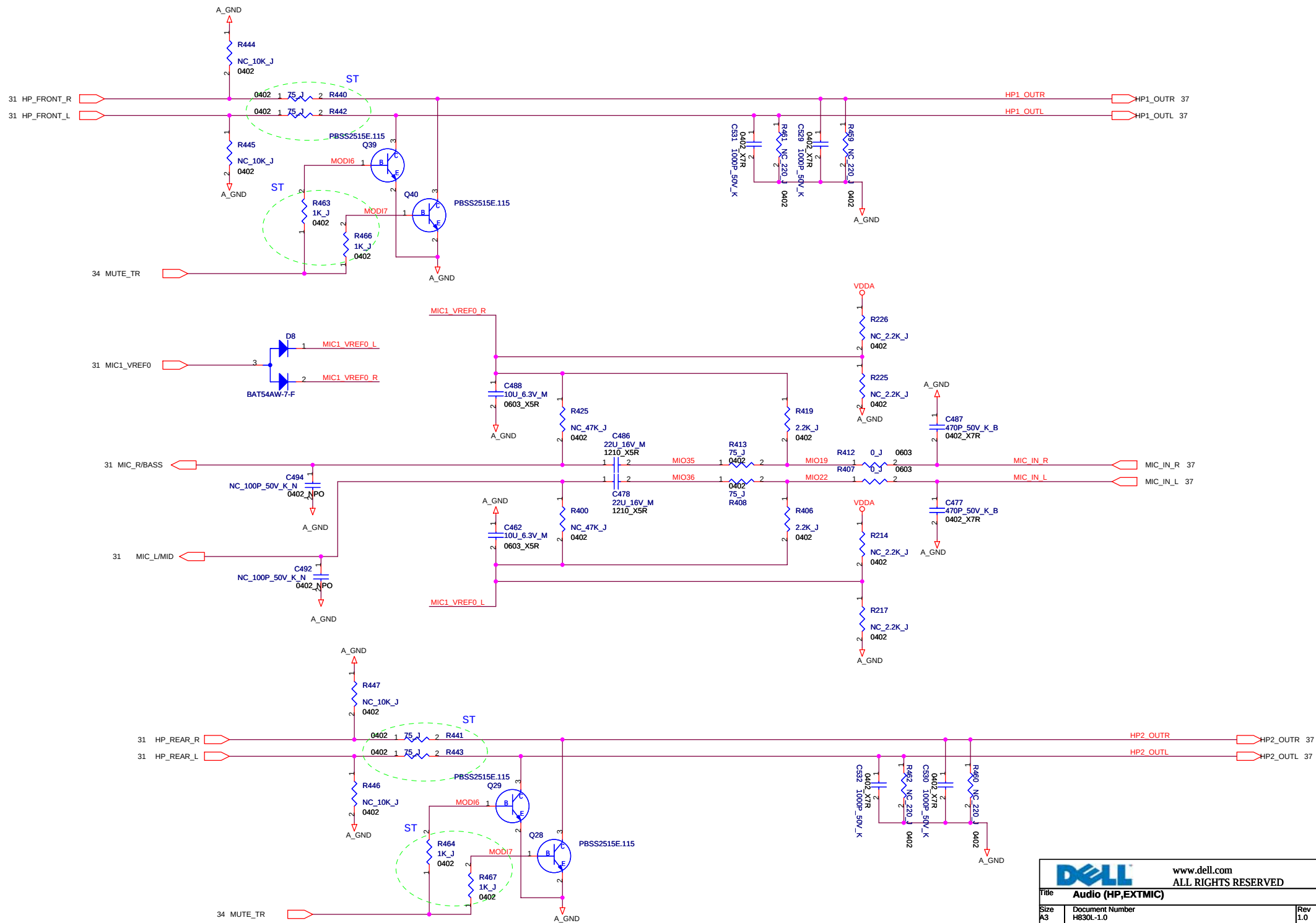


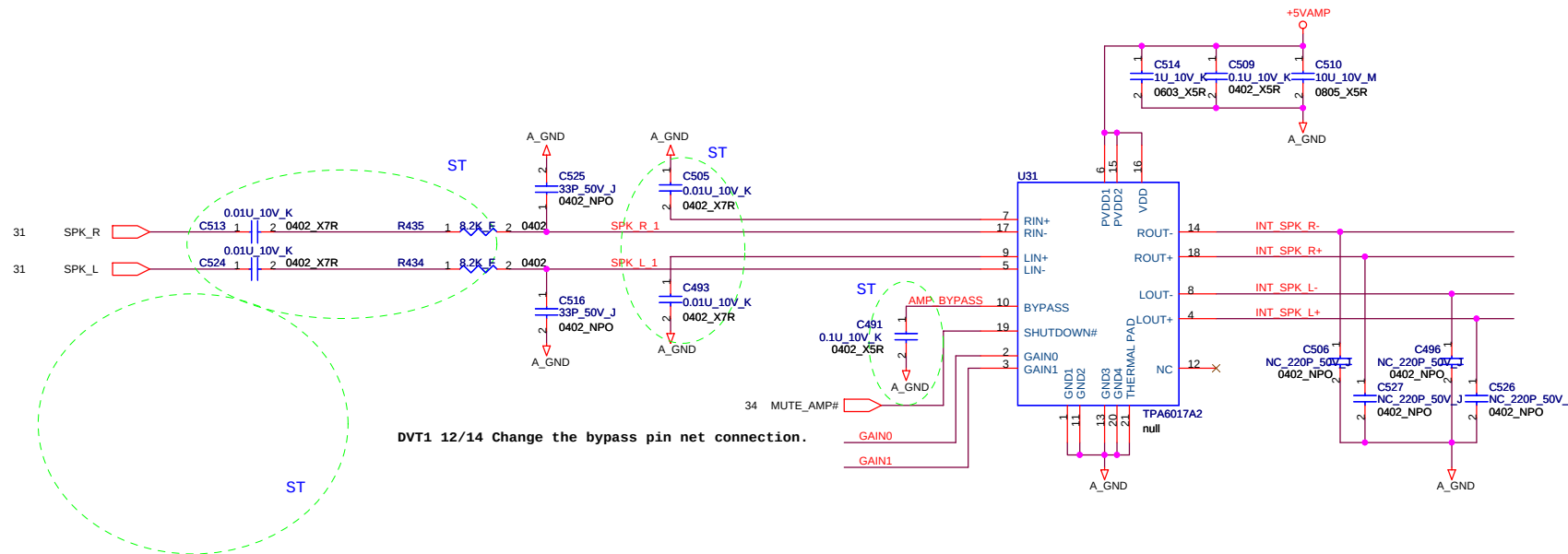
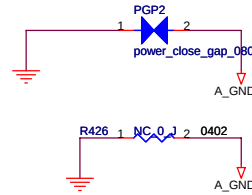
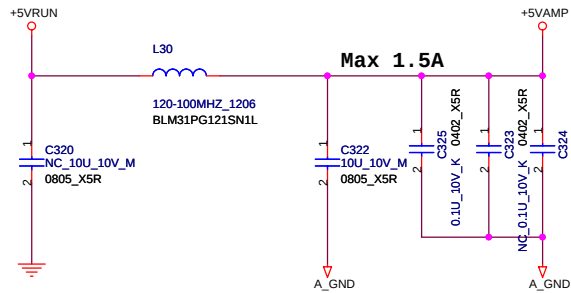
Bluetooth CONN.

Bluetooth

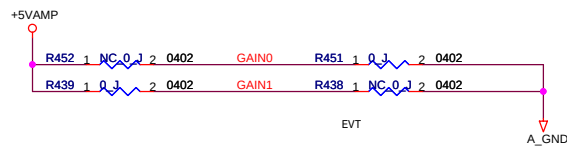


Camera & Digi MIC





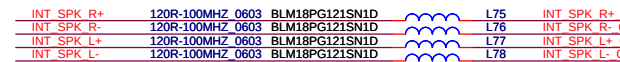
DVT1 12/14 Change the bypass pin net connection.



SPEAKER AMP

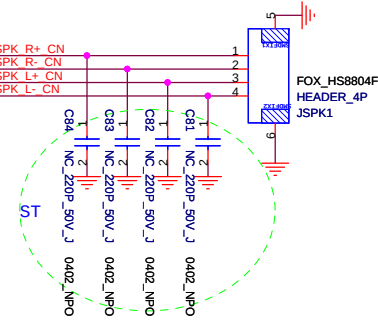
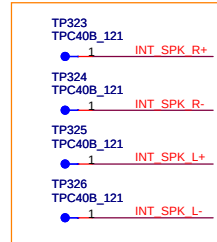
	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1

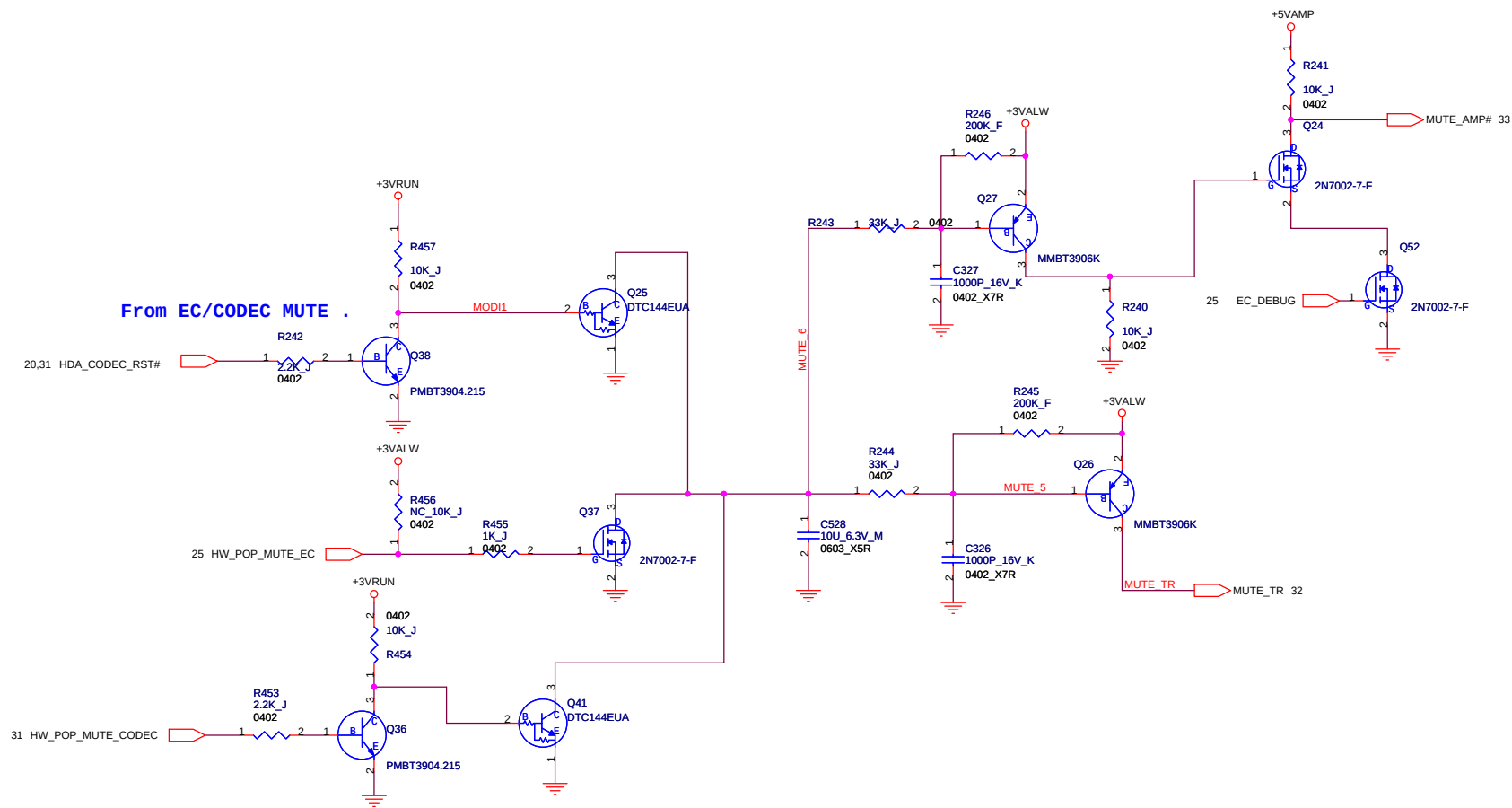
dB=20logGain
If set 10dB , gain is 3.162.
 $P_o = \{(1.2V_{rms} * 3.162)^2\} / 4 = 3.599 W$

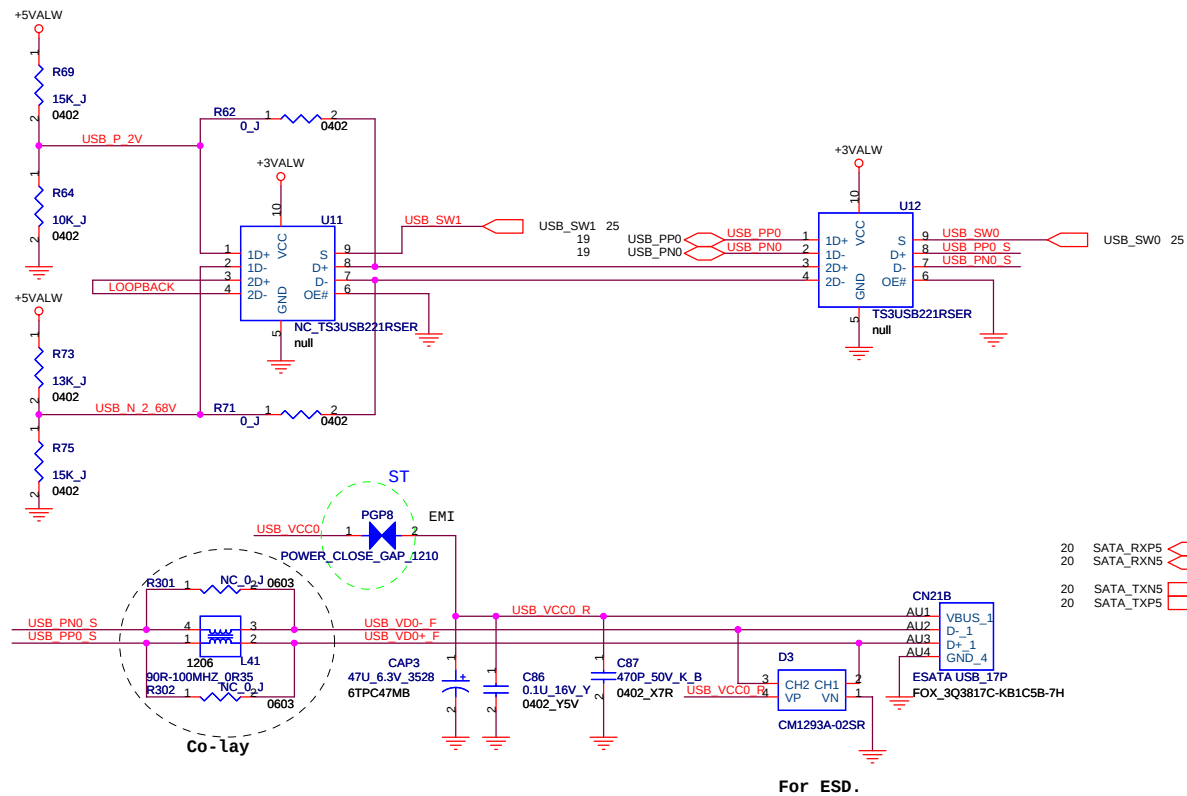


INTERNAL SPEAKER

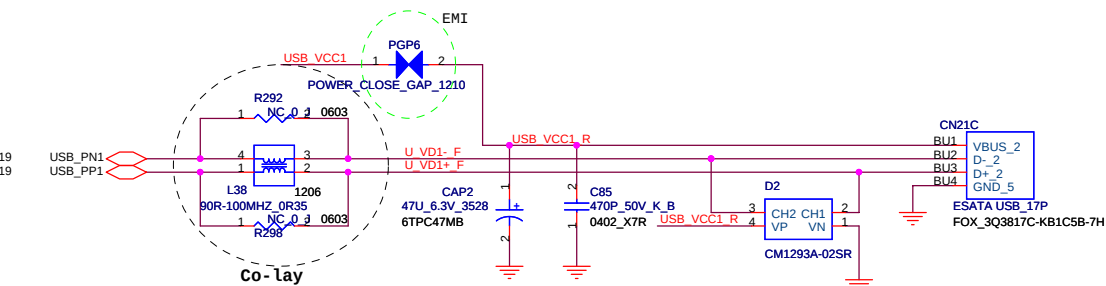
ST BFT Test Pad



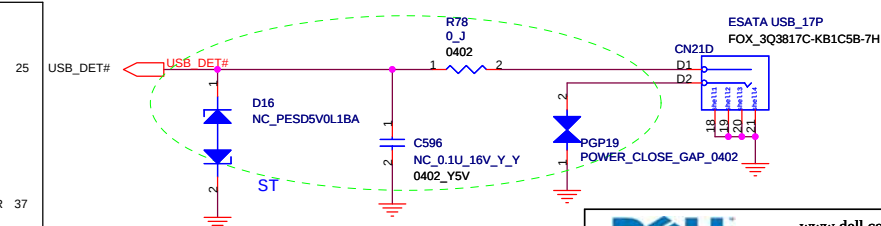
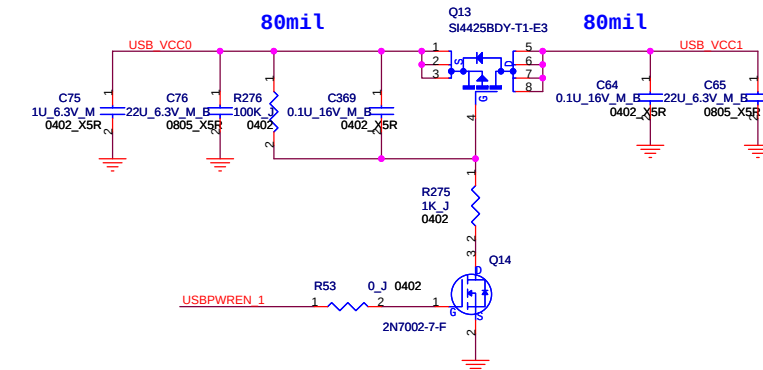
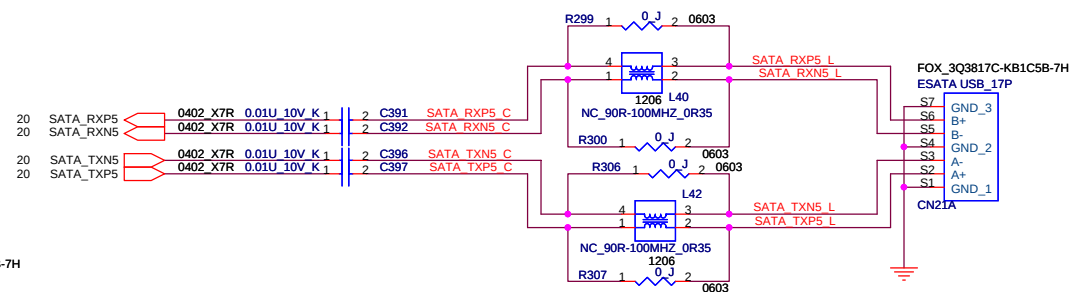
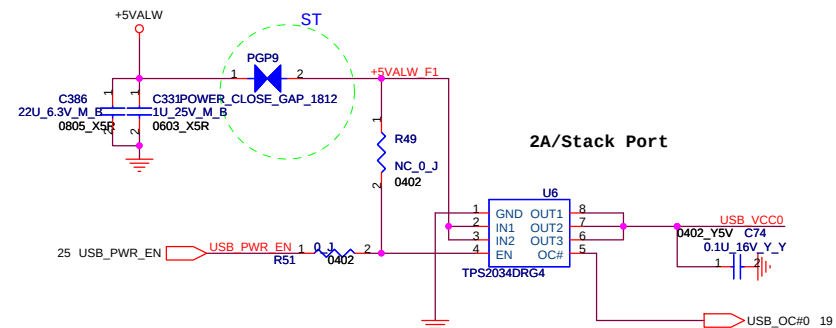




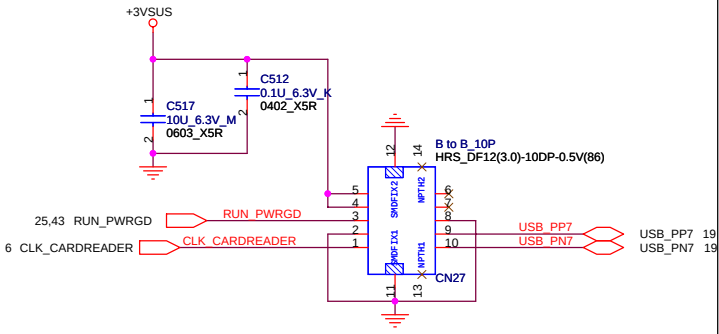
For ESD.



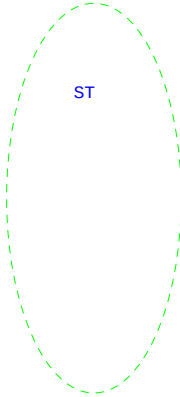
For ESD.



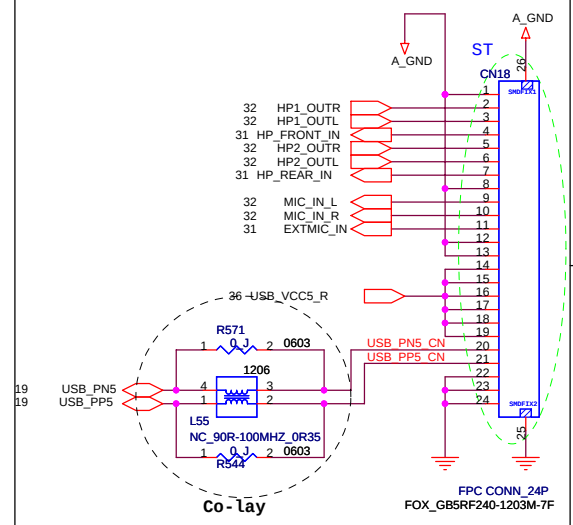
Cardreader Board



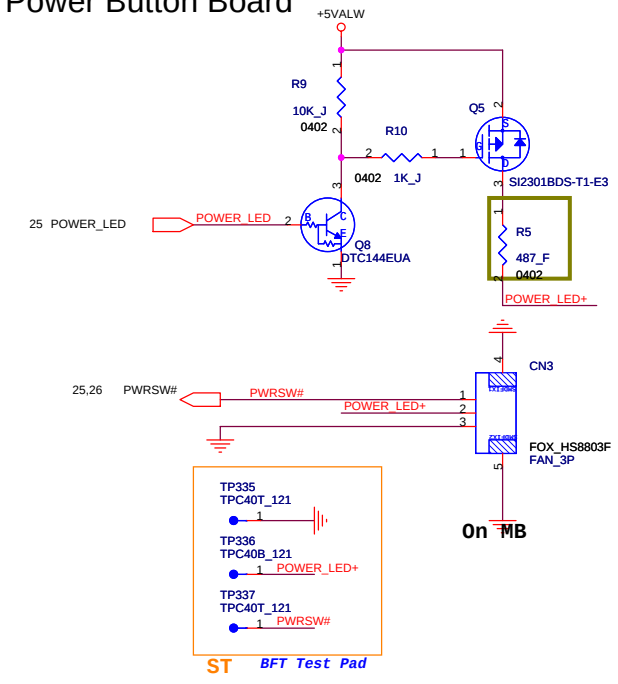
WWAN Board



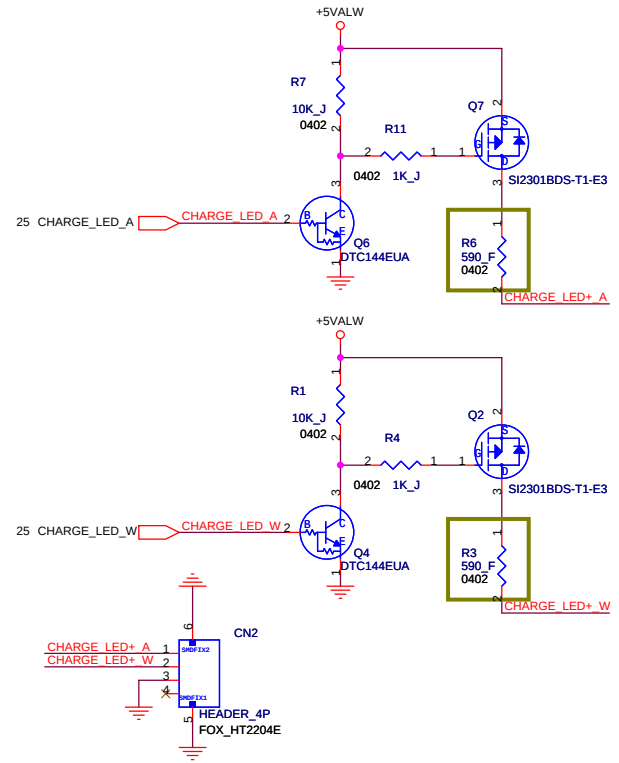
Audio_USB Board On MB



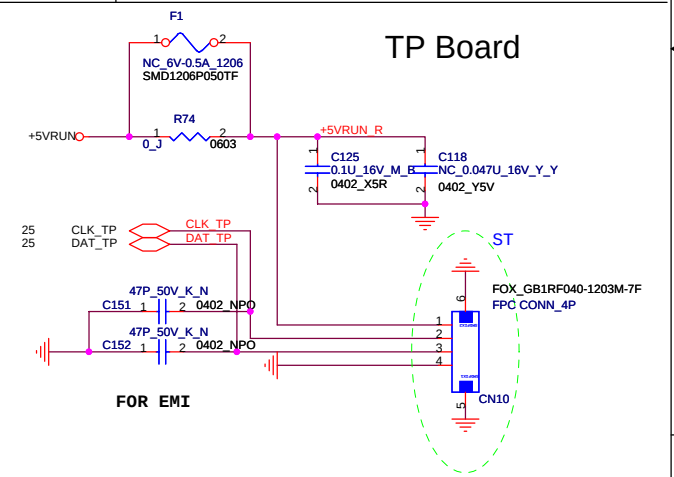
Power Button Board



LED Board



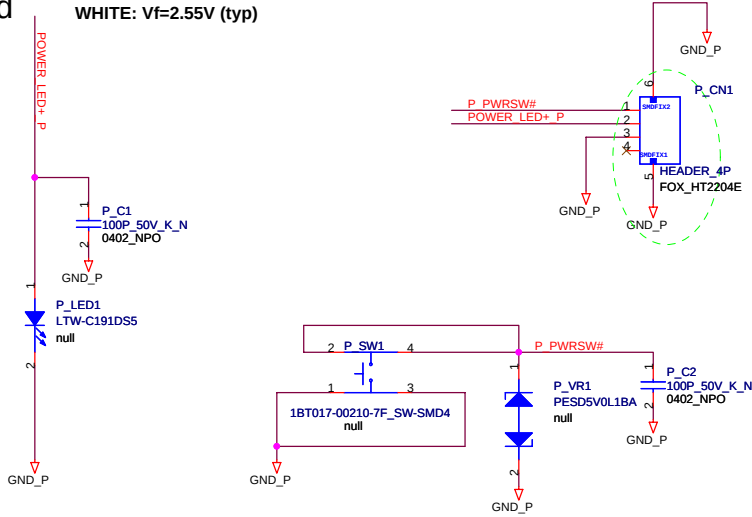
TP Board



			www.dell.com ALL RIGHTS RESERVED		
Title DB board connector (MB)					
Size A3	Document Number H830L-1.0				Rev 1.0
Date:	Wednesday, April 08, 2009		Sheet 37	of	50

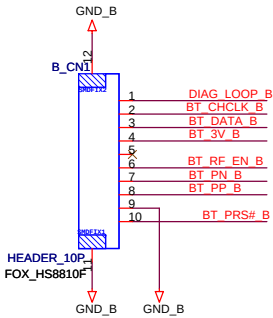
Power Button Board

WHITE: Vf=2.55V (typ)

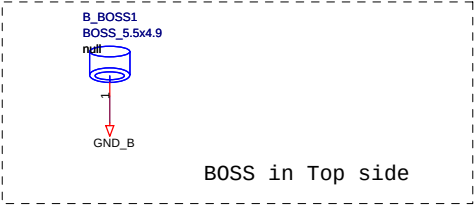
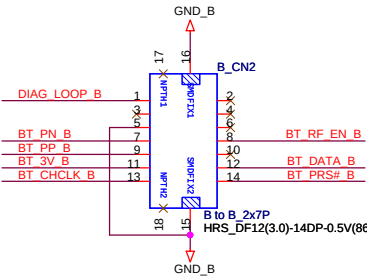


POWER BUTTON

Bluetooth Board

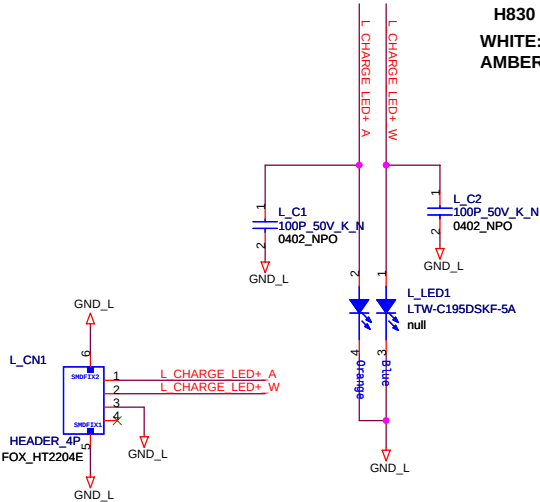


Bluetooth CONN.



LED Board

H830
WHITE: Vf=2.55V (typ)
AMBER: Vf=2.0V (typ)



ST

Adaptor
19.5V
65W

MAX 8731A
SMBus L2
Battery Charger
Switch Mode
PAGE 44

Battery Pack
56Wh
85Wh

DCBATOUT

ALW_ON

DCBATOUT

RUN_ON1

DCBATOUT

SUS_ON

RUN_ON1

DCBATOUT

IMVP_VR_ON

MAXIM
MAX17020
Switch Mode
For System Power
PAGE 45

TI
TPS51117RGYRG4
Switch Mode
For System CPUVIO
PAGE 46

MAXIM
MAX17000
Switch Mode
For DDR3
PAGE 47

INTERSIL
ISL6266A
Switch Mode
For CPU Core
PAGE 48

7.5A

+5VALW/4A

6A

+3VALW/0.2A

+5VALW_LDO

ALW_PWRGD

+5VALW_LDO

14A

RUN_PWRGD

11A

2A

DDRDIMM_VREF

SUS_PWRGD

44A

IMVP_OK

SUS_ON

N-Channel
MOSFET

+5VSUS/0.2A

SUS_ON

N-Channel
MOSFET

+3VSUS/4.2A

+5VALW_LDO

LDO
TPS79333

+ECVCC/0.012A

+3VRUN

LDO
RT9198

+1.8VRUN/0.12A

+3VRUN

+1.05VRUN/14A

RUN_ON1

+1.5VSUS/10A

RUN_ON1

N-Channel
MOSFET

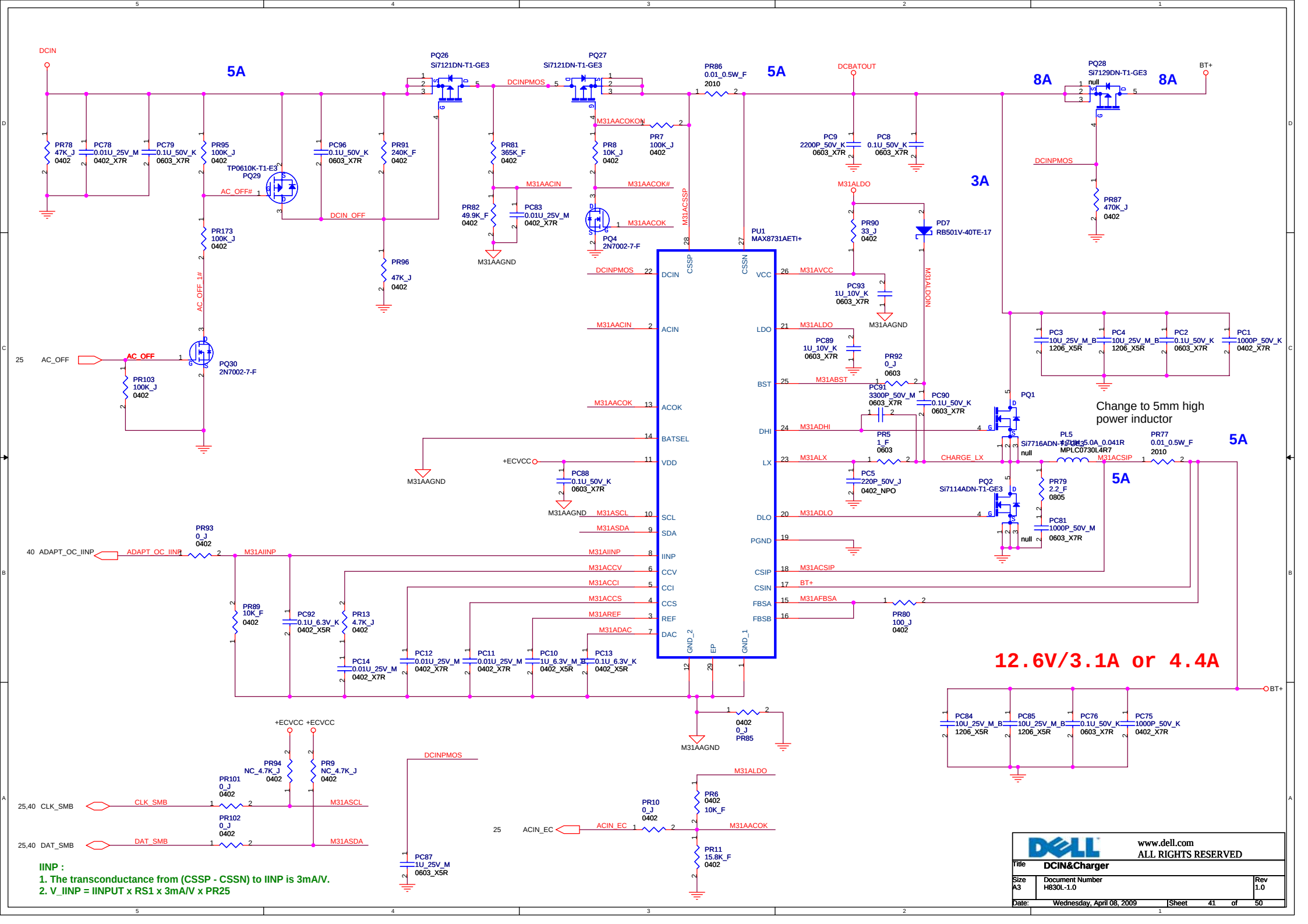
+1.5VRUN/3.3A

+0.75VRUN/2A

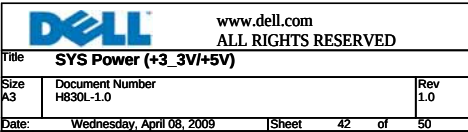
VHORE/44A

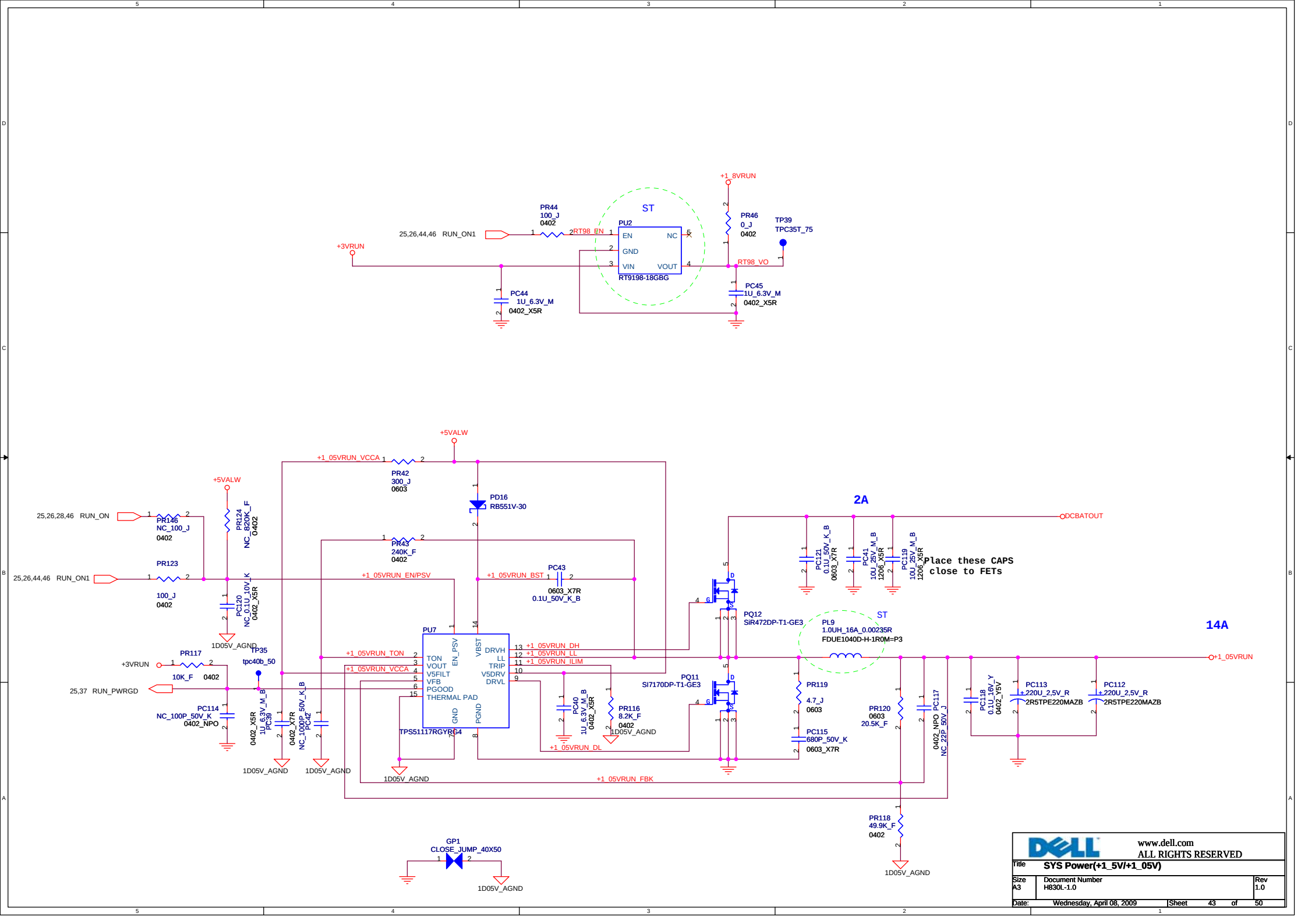
<http://www.fangyuannb.com> <http://shop63900485.taobao.com>

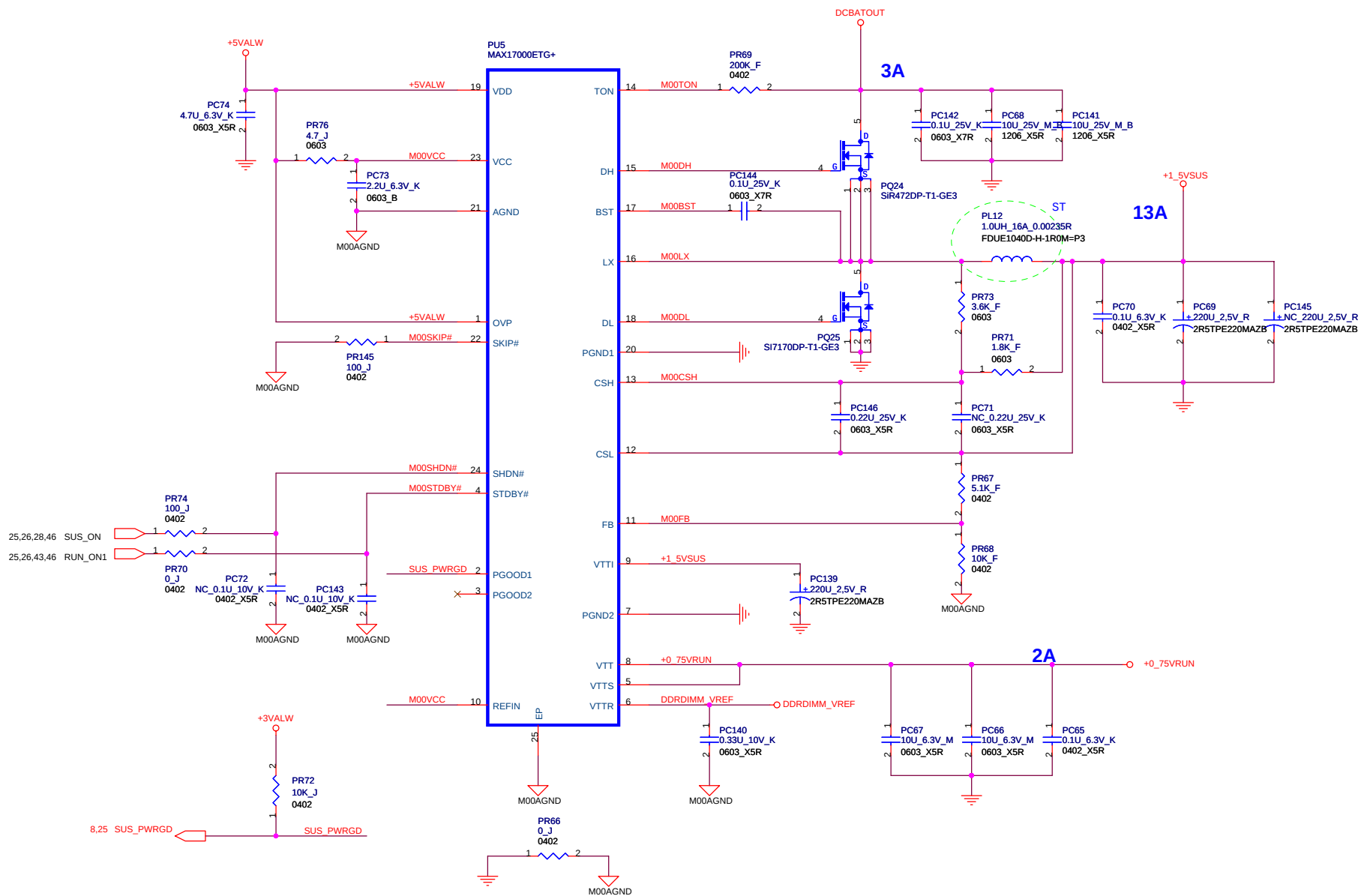


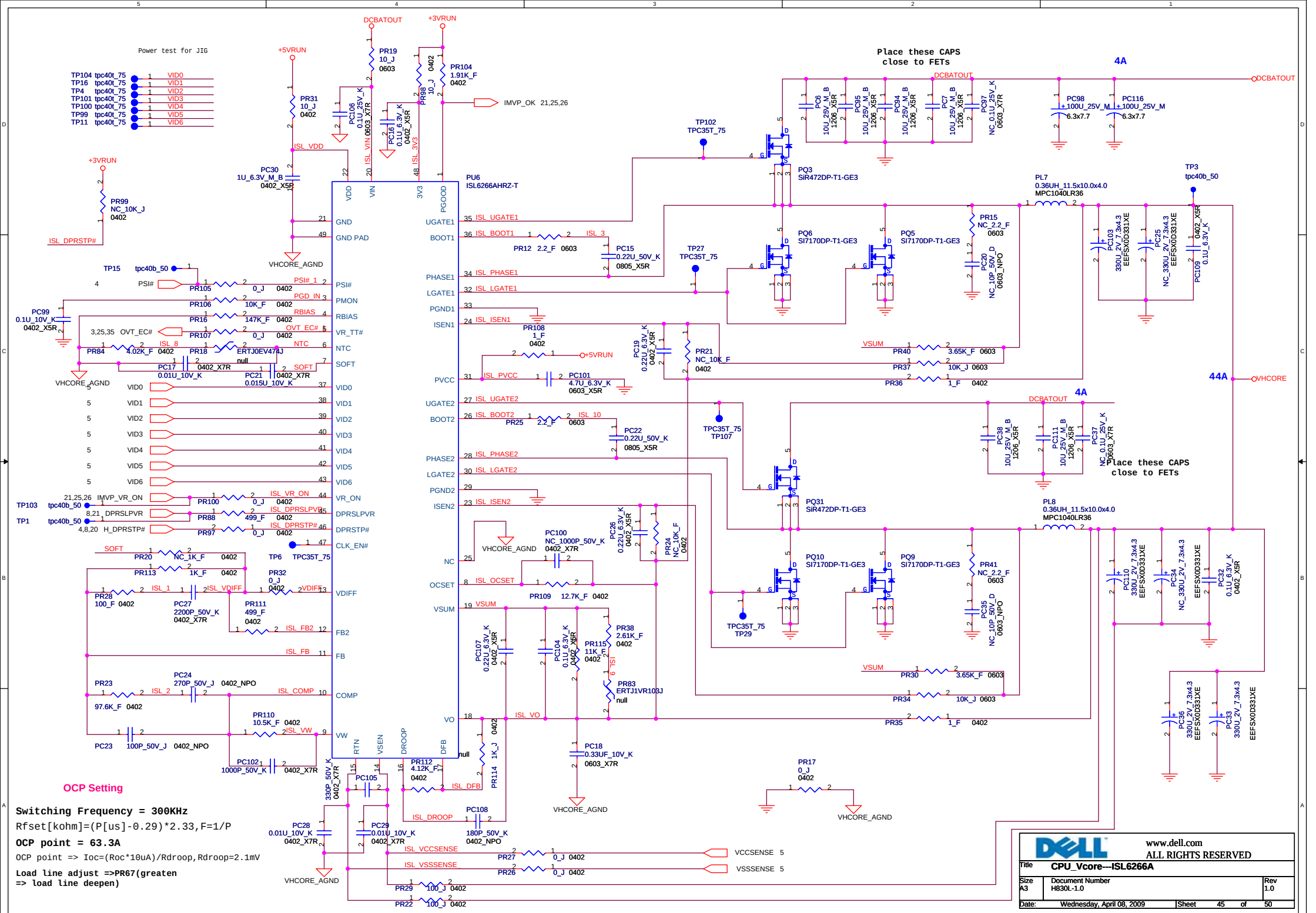


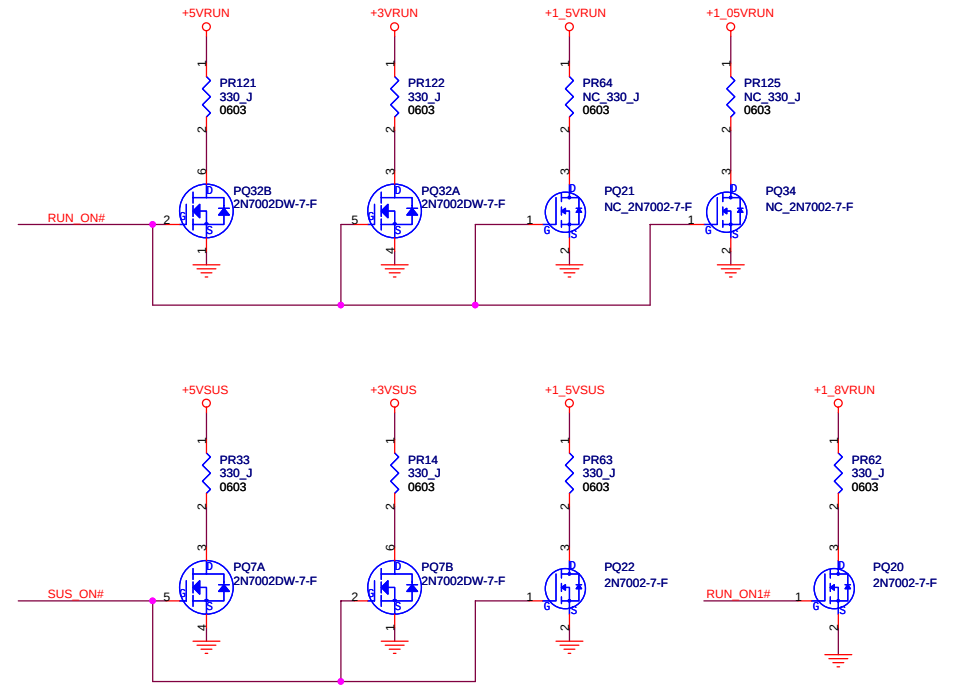
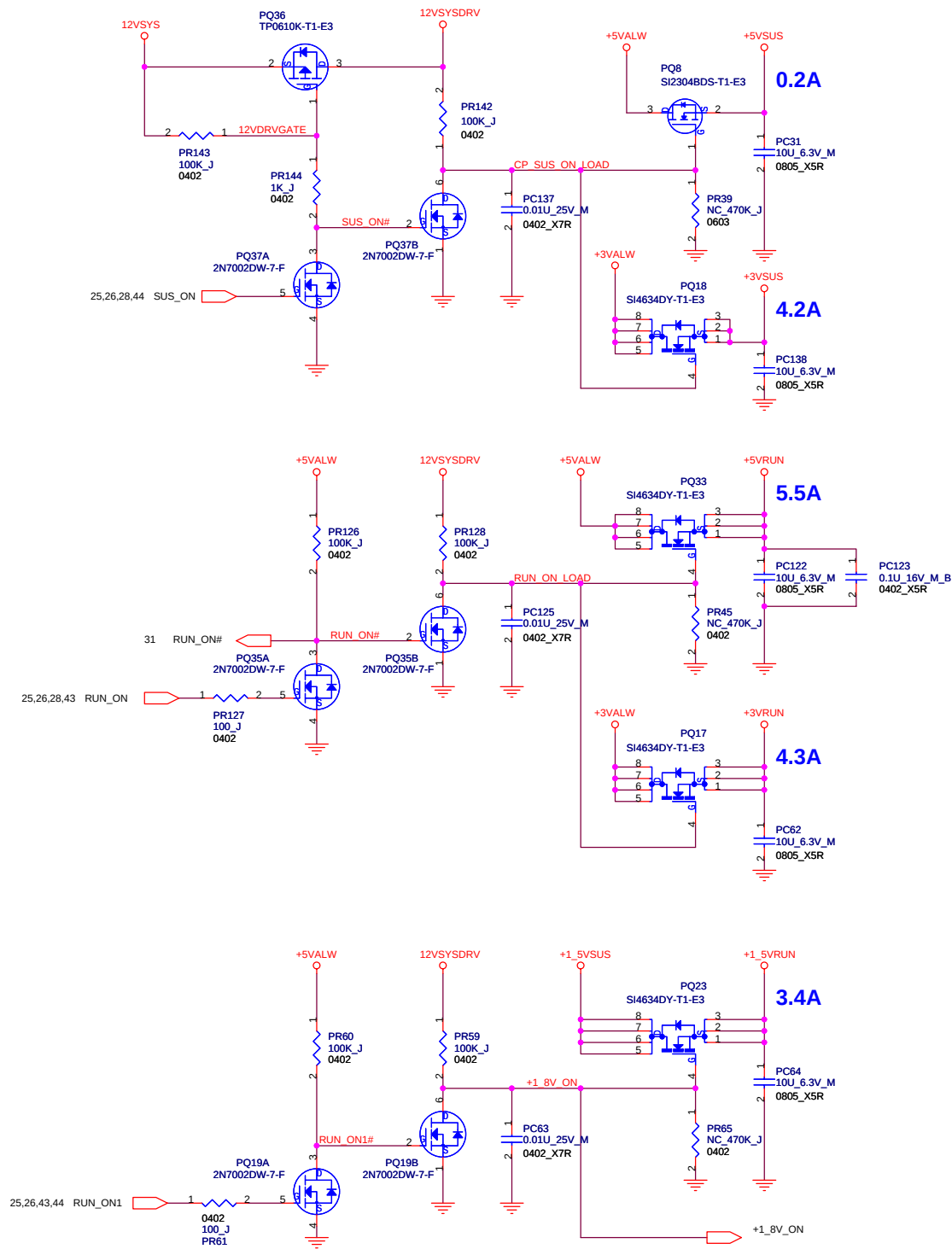
IINP :
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_{IINP} = IINP \times RS1 \times 3mA/V \times PR25$











H830-L EVT -> DVT

(2008/12/29)

P.25 Change KB CN: CN13 to Stuff; CN12 to NC for ME requirement.
P.28 Change Express Card CN: CN14, CN17 to Foxconn for ME requirement.
P.37 Change WWAN CN: CN8 to Stuff; CN7 to NC for ME requirement.
P.41 Change PR87 to 470K from 100K to fix part number error.
P.41 Change PR6 to 10K from 100K to fix part number error.
P.41 Change PR89 to 10K from 8.45K to fix part number error.
P.41 Change PR77, PR86 to CYTEC from WAL SIN for purchase requirement.
P.42 Change PR136 to 27K from 33K for fine tune voltage.
P.42 Change PR56 to NC ; PR55 to stuff to fix 3V/5V over-spec issue.
P.43 Change PQ11 to SI7170DP-T1-GE3 from SiR466DP-T1-GE3.
P.45 Change PR108, PR36, PR35 to 1ohm from 100K to fix part number error.
P.45 Change PR20 to NC for ISL6266A improved by internal circuit.

(2008/12/31)

P.25/29/30/33/35/37/40 Add test point TP300-TP337 for DVT BFT test.

(2009/01/06)

P.18 Change L47 vender to PSL vender Murata.
P.29 Add TP338-TP to solve PC_BEEP issue.
P.33 Add Q50, R468,R560,C816,C792 to solve PC_BEEP issue.
P.34 Add Q41 to solve speaker mute issue.
P.37 Change CN3 to 4pin CN from 3pin to avoid confusing with LED Brd CN.
P.38 Reverse L_SMD1 to follow cable pin definition.

(2009/01/08)

P.20 Change RTC battery part number to CR-2032L/BN from CR-2032L/BE for PUR.
P.40 Add PU PR172 for PS_ID.
P.24 Change CN26 (HDD CN) footprint for ME request.
P.24 Change CN26 (HDD CN) footprint for ME request.
P.19 Change R124 to NC for no necessary.

(2009/01/09)

P.14/15 Change C221,C196,C219,C220,C202,C178,C197 to stuff to follow H830H.
P.38 Change R299,R300,R306,R307 to Stuff; L40,L42 to NC to solve e-sata issue.
P.20 Change C423, C424 to 12pF from 15pF for crystal Y2 precision.
P.30 Change C48 to 15pF, C47 to 18pF for crystal Y1 precision.
P.25 Change C481 to 15pF, C475 to 15pF for crystal Y4 precision.
P.06 Change C425 to 27pF for crystal Y3 precision.
P.21 Change USBPWREN_1 to SB GPIO28; GPIO22 connect +3VRUN to solve USB S3 auto resume issue.
P.40 Change TP300, TP301,TP302,TP303,TP304 to TPC60B_75 for TE request.
P.41/42 Change PQ2, PQ15 to Si7114ADN-T1-GE3 for power request.
P.43 Change PQ11 to SI7170DP-T1-GE3 for power request.
P.34 Add Q52 and connect EC_DEBUG to EC to solve PC_BBEP issue.

(2009/01/09-2)

P.30 Change Y1 to X5H025000FC1H-H for vender suggest.
P.20 Change RTC Battery CN25 to BB10201-C1401-7F for ME request.

(2009/01/12)

P.36 Change U6,U34 to HF part RT9703GS for vender suggest.

(2009/01/14)

P.38 Change L_SMD1 to L_CN1 for ME request.
P.48 Del H1,H10 & H23 for ME request.
P.43 Change PU2 to RT9198-18PBG from RT9198-18GBG for PUR request.
P.36 Change U6,U34 back to LF part RT9703PS for vender lead time issue.

(2009/01/16)

P.36 Del eSATA Choke L40 and L42 for improve SI.
P.18 Change HMDI CN CN16 to DIP type for factory EE request.
P.37 Change PWR BTN CN CN3 to 3pin and LED Brd CN CN2 to 4pin for ME request.

(2009/01/19)

P.41 Add PR173 for solve PQ29 derating issue.
P.42 Move PC124 to DCIN5VALW for power request.
P.06 Change C425 to 33pF for crystal Y3 precision.

(2009/01/20)

P.43 Add PD16 for power request.
P.08 Add U38, C818, R563,R564 to solve SUS_PWRGD level drop issue.
P.05 Add C819, C820, C821 for RF request.
P.27 Del D4 and add R469, Q42 and Q43 to solve HDMI CN VCC issue.
P.42 Del PR52 and change PR51 to 0ohm;change PR53 to NC for power request.
P.47 Add PAD2-PAD12 for ME request.

(2009/01/21)

P.17 Change R269 to 62ohm and stuff R360 and Q12; add C534 to solve panel power sequence issue.
P.36 Change USB power switch U34, U6 to TPS2034DRG4 (low Rds on).
P.38 Add BC_CN4 and BC_CN3 for BT second source.
P.52 Add PR146 NC for resevering power sequence test.

(2009/02/02)

P.31 Change C518 to 2.2uF from 10uF to solve S3 pop noise issue.
P.47 Connect H30 to AGND from GND.
P.37 Increse USB_VCC5_R to 6pin from 4pin and decrease AGND, GND pin to improve voltage drop.

(2009/02/02)

P.37 Del colay connector CN6 for ME request.

(2009/02/05)

P.47 Del BOSS6 for ME request.
P.38 Add BC_TP1, BC_TP2.
P.25 Change Q21B(3904) to Q53 (2N7002) to prevent current leakage.
P. Change test point to ICT test point: TP111,TP113,TP116,TP117,TP118,TP119,TP120,TP121,TP122,TP123,TP124,TP125,TP126,TP130,TP131,TP132,TP133,TP135,TP136,P137,TP139,TP140,TP141,TP142,TP153,TP157,TP158,TP178,TP179,TP34,TP36,TP37,TP40,TP41,TP42,TP44,TP45,TP46,TP47,TP49,TP58,TP60,TP62,TP63,TP64,TP69,TP70,TP72,TP75,TP77,TP78,TP79,TP8,TP85,TP86,TP87,TP88,TP89,TP9,TP90,TP92,TP93,TP94,TP95,
P.35 Add U39,U40,R565,R568,R569,R570,R566,R567,C823 for G sensor function.

(2009/02/06)

P.47 Del BOSS6 for ME request.
P.31 Change LDO U18 to TPS73601DBVR for current limit up to 400mA.
P.31 Change R478 to 0ohm from 22ohm for SI.
P.37 Add L55, R544, R571 for EMI.
P.20 Add R465,R1305 and SATALED# for HDD LED.
P.35 Add Q54, R575, TP255, TP249 for G sensor function.
P.28 Add CN72, CN73 for expresscard CN second source.

(2009/02/07)

P.36 Change D2,D3 to PSL vender.
P.51 Change PR136 to 0 ohm and PR137 to NC to solve +3VALW level too high issue. .

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(2009/02/10)

- P.16 Change C418,C415 & C410 to 22pF for EMI requirement.
- P.29 Add L73, L74,C772 & C817 for EMI requirement.
- P.16 Change L45,L44,L43 to BLM18BB750SN1D for RGB Tr, Tf issue.
- P.33 Del R54,R55,R56,R57 and add L75,L76,L77,L78 for EMI issue.

(2009/02/11)

- P.40 Add C822 1000pF on PCN1 pin 3 for EMI requirement.
- P.42 Change PR54 to 120k for 3.3V OCP Change.
- P.43 Change PR43 to 240k for 1.05V Frequency Change.
- P.44 Change PR43 to 1.8k for 1.5V OCP Change
- P.41 Change PQ28 to Si7129DN-T1-GE3 for Id Derating Fail
- P.44 Change PC69,PC139 to 220uF, for Power IC issue,Maxim FAE instance
- P.43 Change PC112,PC113 to 220uF, for Power IC issue,TI FAE instance.
- P.44 Change PC145(NC) to 220uF, for Power IC issue,Maxim FAE instance
- P.45 Change PC143 to 0.1uF for For Vhcore loadline and transient.
- P.45 Change PR111 to 499ohm for Vhcore loadline and transient
- P.45 Change PR112 to 4.12Kohm for Vhcore loadline and transient
- P.42 Add PR147(NC) 0ohm for +3D3VALWV0 from +ECVCC,for PT energy star test.
- P.42 Add PR148(NC) 0ohm for M0200N2 from M020LD0,for PT energy star test.

(2009/02/12)

- P.30 Change R26 to 1.1K from 1.24k for LAN SI issue.

(2009/02/13)

- P.38 Add BC_BOSS1 for BT2 Brd nut.
- P.14/15 Add C535,C537,C538,C317,C538,C541,C542,C540,C539,C543 for DDR EMI issue.
- P.42 Add PC146 and NC PC71 for DDR power.
- P.30 Change R26 to 1.24K from 1.1k for LAN SI issue.
- P.40 Add PCN2 toBP03091-B82F3-9F for ME request.
- P.16 Change F2 to SMD1206P035TF/16 for fuse derating issue.
- P.36 Change F5,F7 to SMD1812P260TF for fuse derating issue.

(2009/02/17)

- P.20 Change R1035,R465 to NC to reserve for SATA LED.

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(2009/03/08)

- P.33 Change Q50,R468,C816,C792 to NC because new version Codec solved PC-Beep issue (PT implement. E-ECN)
- P.21 Change RTC battery part number to CR-2032L/BN from CR-2032L/BE for PUR request.
- P.35 Change U40 G-sensor part number to DE351DL for request.
- P.41-45 Remove Power open gap PJ1,PJ2,PJ3,PJ4,PJ5,PJ6,PJ7,PJ8,PJ9,PJ10,PJ11,PJ12,PJ13,PJ14,PJ15,PJ16,PJ17 for power request.
- P.42 Change PR135 to 16.2K ohm to solve +5VALW voltage too high issue.

(2009/03/15)

- P.42 Change PR135 to 16.2K ohm to solve +5VALW voltage too high issue.
- P.17 Change R38 to 51K and C534 to 0.015uF tol solve LCD power sequence issue.
- P.25/26/37 Change CN13,CN29,CN18,CN10 material to met tin for ME request.
- P.40 Add PR175, PR177, PQ45,PQ44,PR176, PD19,PR174, and del PD5; change C822 to NC_100pF for AD_ID(PS_ID) protection.
- P.18 Change Q31 to 2N7002K for HDMI detection pin ESD protection.
- P.36 Reserve D16 PESD5V0L1BA NC for USB port detection pin ESD.

(2009/03/16)

- P.38 Change P_SMD1 to P_CN1 for ME request.

(2009/03/16)

- P.17 Add fuse F8 for LVDS power protection.

(2009/03/17)

- P.17 Add fuse F8 for LVDS power protection.
- P.37 Change CN8 to 18pin and del C368,C498,C73,C72 for del PCIe interface of WWAN DB.

(2009/03/26)

- P.17 LVDS CN, change +3VRUN to pin 10 from pin4 to prevent DCBATOUT short to +3VRUN.
- P.47 Del H20 and modify H4,H18,H26,H9,H16,H28 for ME request.
- P.20 Del C246,C247 for del PCIe interface of WWAN DB.
- P.04 Add C72 to solve H_GTLREF Vpp over-spec issue.
- P.47 Modify P_H1 and P_PAD1 for ME request.
- P.37 Change WWAN DB CN +3VALW to 8pin from 7pin.
- P.27 Add CN74 WLAN CN second source colay with CN17 for ME request.

(2009/03/27)

- P.17 LVDS CN, change +3VRUN to pin 10 from pin4 to prevent DCBATOUT short to +3VRUN.

(2009/03/27-2)

- P.37 Modify WWAN CN8 pin define.
- P.26 LVDS CN, change +3VRUN to pin 4, pin3 to NC prevent DCBATOUT short to +3VRUN.

(2009/03/27-3)

- P.31 Change R207 to 13.3K for Realtek recommand.

(2009/03/31)

- P.18 Change R386 to NC for 27MHz XTAL.
- P.33 Change R435,R434 to 8.2K for 6ohm SPK.
- P.14/15 Change DDR CN package: CN24 to AS0A626-U4RN-4F, CN23 to AS0A626-U8RN-4F for SMT.
- P.43 Change PU2 to RT9198-18GBG (HF part)for PUR request.

(2009/04/02)

- P.33 Change C81,C82,C83 and C84 to NC for EMI request.
- P.33 Del Q50,R468,R560,C816,C792 to del reservation for PCBeep.

(2009/04/03)

- P.16 Change L43,L44,L45 to BLM18BB470SN1D to solve VGA SI issue.
- P.19/25/38 Del CN8,C78,C225,C77 add TP34,TP36,TP37 for WWAN CN PCIe interface cancelled.

(2009/04/05)

- P.40 Change BFT Testpoint TP300, TP301,TP302, TP303,TP304 to TPC60B_121 for TE request.
- P.25/35/37 Change BFT Testpoint TP327,TP328,TP329,TP330,TP333,TP334,TP312,TP313,TP314,TP335,TP337 to tpc40t_121 for TE request.
- P.29/30/33/37 Change BFT Testpoint TP305,TP306,TP307,TP308,TP310,TP338,TP339,TP340,TP341,TP342,TP343,TP344,TP345,TP346,TP309,TP311 TP315,TP316,TP317,TP318,TP319,TP320,TP321,TP322 ,TP323,TP324,TP325,TP326,TP336 to tpc40B_121 for TE request.

(2009/04/08)

- P.42 Change PL_10 to FDVE0630-H-1R5M=P3 (HF part) for power request.
- P.43 Change PL_9 to FDUE1040D-H-1R0M=P3 (HF part) for power request.
- P.44 Change PL_12 to FDUE1040D-H-1R0M=P3 (HF part) for power request.

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(2009/04/08)

- P.17 Change F8 to 467002 (32V-2A_0603) forLVDS VCC protection.
- P.38 Del BC_CN4,BC_CN3,BC_BOSS1,BC_TP1,BC_TP2 for BT2 board is not necessary.

(2009/04/09)

- P.35 Change R568,R575, Q54,R569,R570,R565,U40,C824,R566,C823,R567 to NC for cancelling support G-sensor.
- P.33 Change C513,C524,C505,C493 to 0.01uF;C491 to 0.1uF for speaker pop noise.
- P.17 Del R270 0ohm for no necessary.
- P.27 Del R39 0ohm and change R278 to close gap PGP17.
- P.11 Change R116 0ohm to close gap PGP4.
- P.36 Change R247,R47,R52 0ohm to close gap PGP5,PGP6,PGP8.
- P.36 Change F5,F7 to close gap PGP7,PGP9.

(2009/04/10)

- P.30 Change R48 0ohm to close gap PGP18.
- P.45 Add C596 NC and PGP19 for USB detection softstart.
- P.32 Change R463,R446,R464,R467 to 1K ohm to solve pop noise..