

TABLE OF CONTENTS

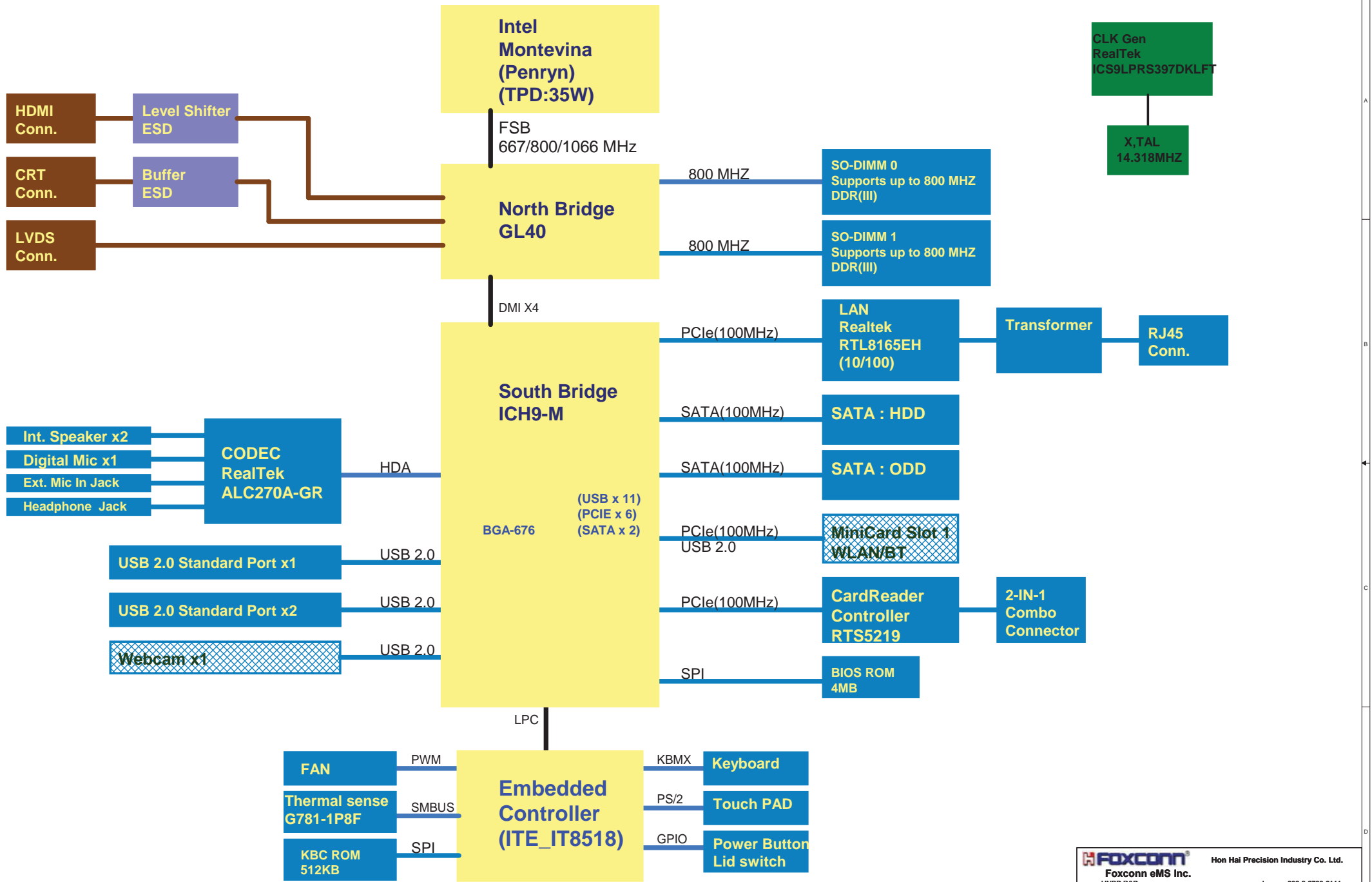
MB

P01 : COVER SHEET	P24 : Cantiga (GRAPHIC) 3/7
P02 : SYSTEM BLOCK DIAGRAM	P25 : Cantiga (DDR3) 4/7
P03 : POWER MAP	P26 : Cantiga (POWER,VCC) 5/7
P04 : POWER SEQUENY DIAGRAM	P27 : Cantiga (VCC CORE) 6/7
P05 : CLOCK MAP	P28 : Cantiga (VSS) 7/7
P06 : SMBUS&I2C MAP	P29 : ICH9-M (PCI/USB) 1/5
P07 : POWER SEQUENCE	P30 : ICH9-M(LPC, IDE, SATA) 2/5
P08 : DCIN/BATT	P31 : ICH9-M (GPIO) 3/5
P09 : PWR_CHARGE	P32 : ICH9-M (POWER) 4/5
P10 : PWR_5V/3.3V	P33 : ICH9-M (GND) 5/5
P11 : PWR_VTT	P34 : DDR3(SO-DIMM_0) 1/2
P12 : PWR_1.5V/0.75S	P35 : DDR3(SO-DIMM_1) 2/2
P13 : PWR_CPU_VCORE	P36 : CLOCK GEN
P14 : PWR_OTHER	P37 : EC+KBC (IT8518)
P15 : PWR_(Empty)	P38 : Audio(CODEC)
P16 : PWR_1.8VS	P39 : Audio(JACK/SPEAKER/MIC)
P17 : PWR_(Empty)	P40 : LAN (RTL8165EH)
P18 : POWER SEQUENY CHART	P41 : Card Reader(RTL5219)
P19 : Penryn(HOST BUS) 1/3	P42 : Mini PCIe&BT/PWRB/Control
P20 : Penryn(HOST BUS) 2/3	P43 : USBX2/USB DB/SATA CONN
P21 : Penryn(Power/Gnd) 3/3	P44 : LVDS/Webcam
P22 : Cantiga (HOST) 1/7	P45 : HDMI & CRT
P23 : Cantiga (DMI) 2/7	P46 : Thermal/Fan/Stitch Cap

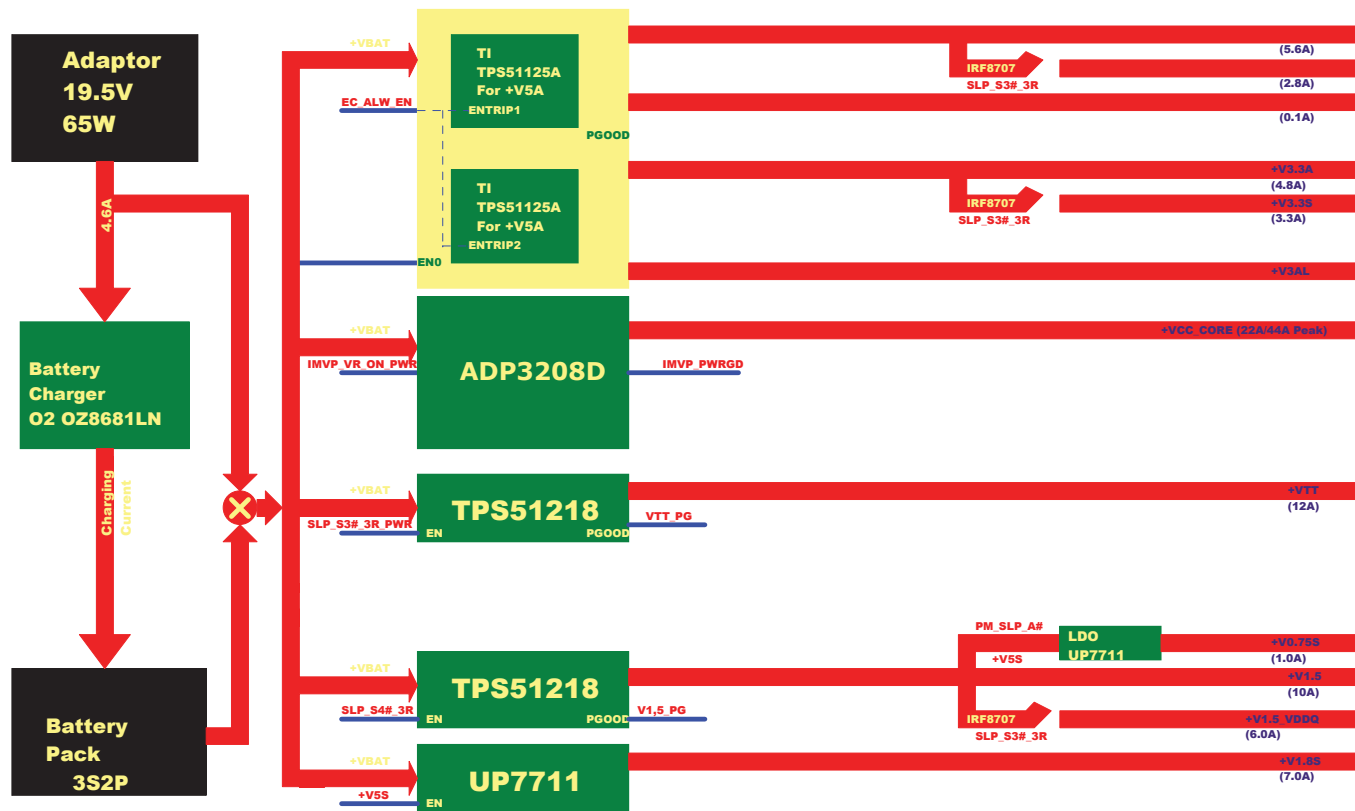
P. Leader	Check by	Design by

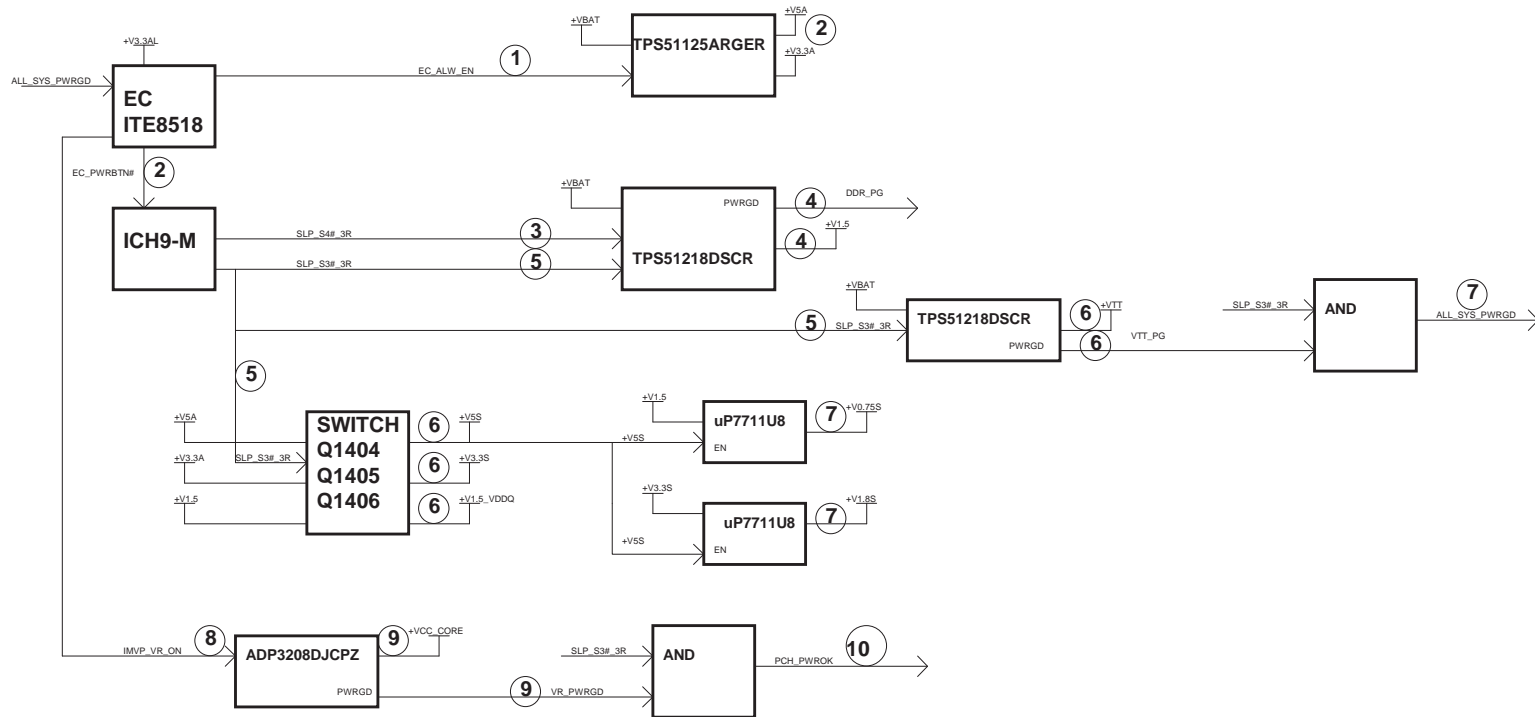

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Title		
Index Page		
Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Monte	
Page Modified: Monday, January 24, 2011 08:43:01 (UTC/GMT) Sheet 1 of 46		



POWER MAP

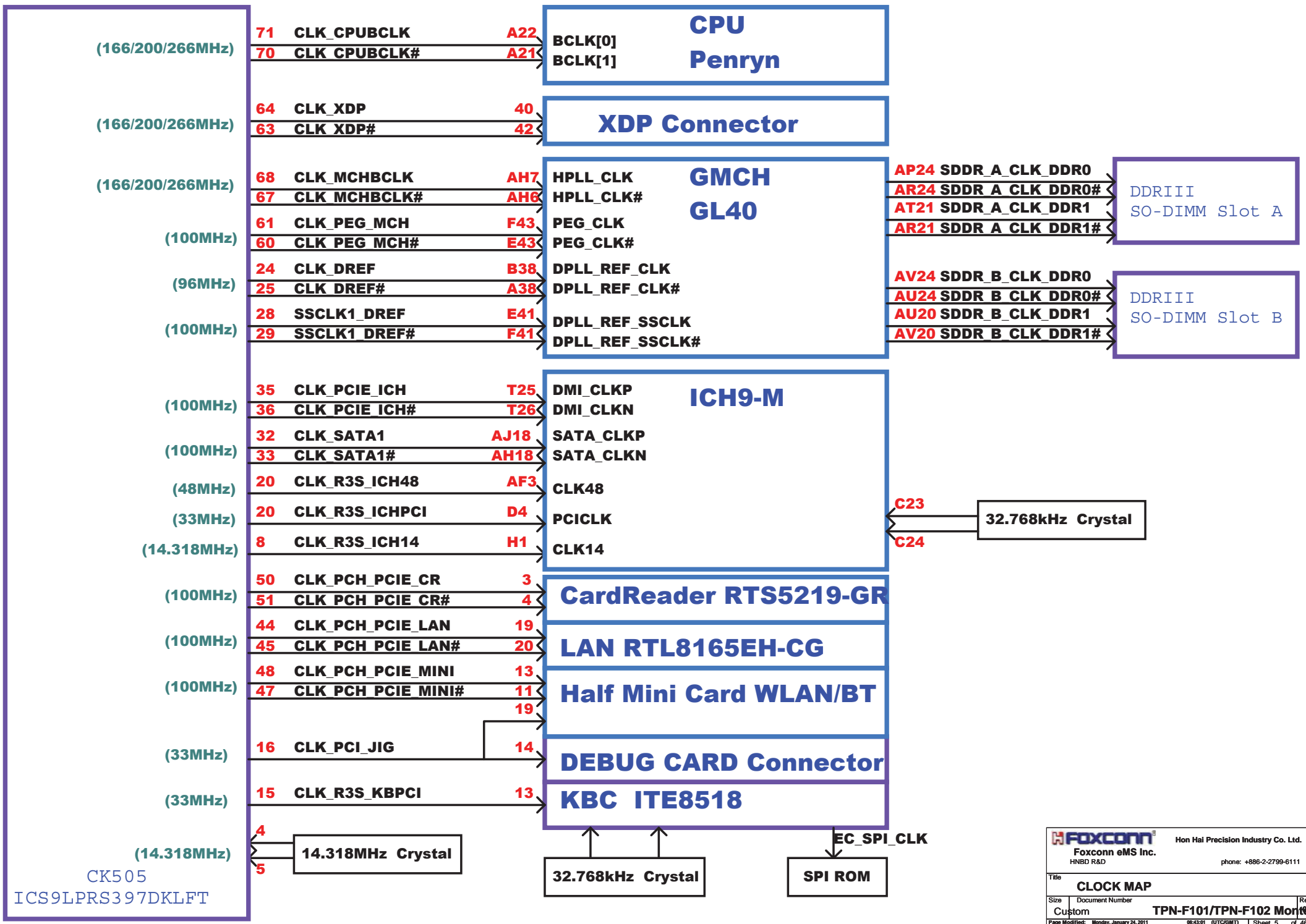




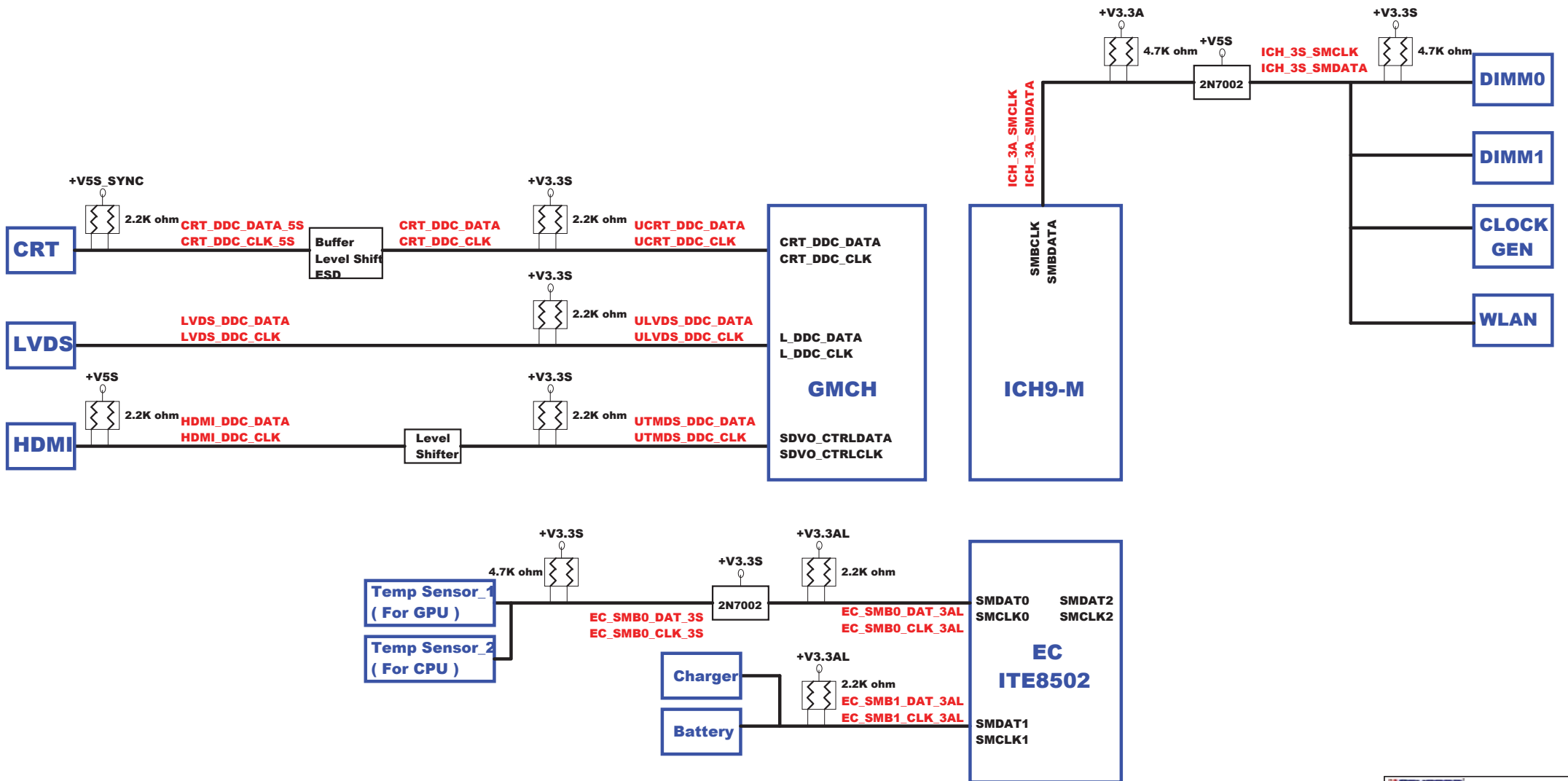
Power on Sequence required:

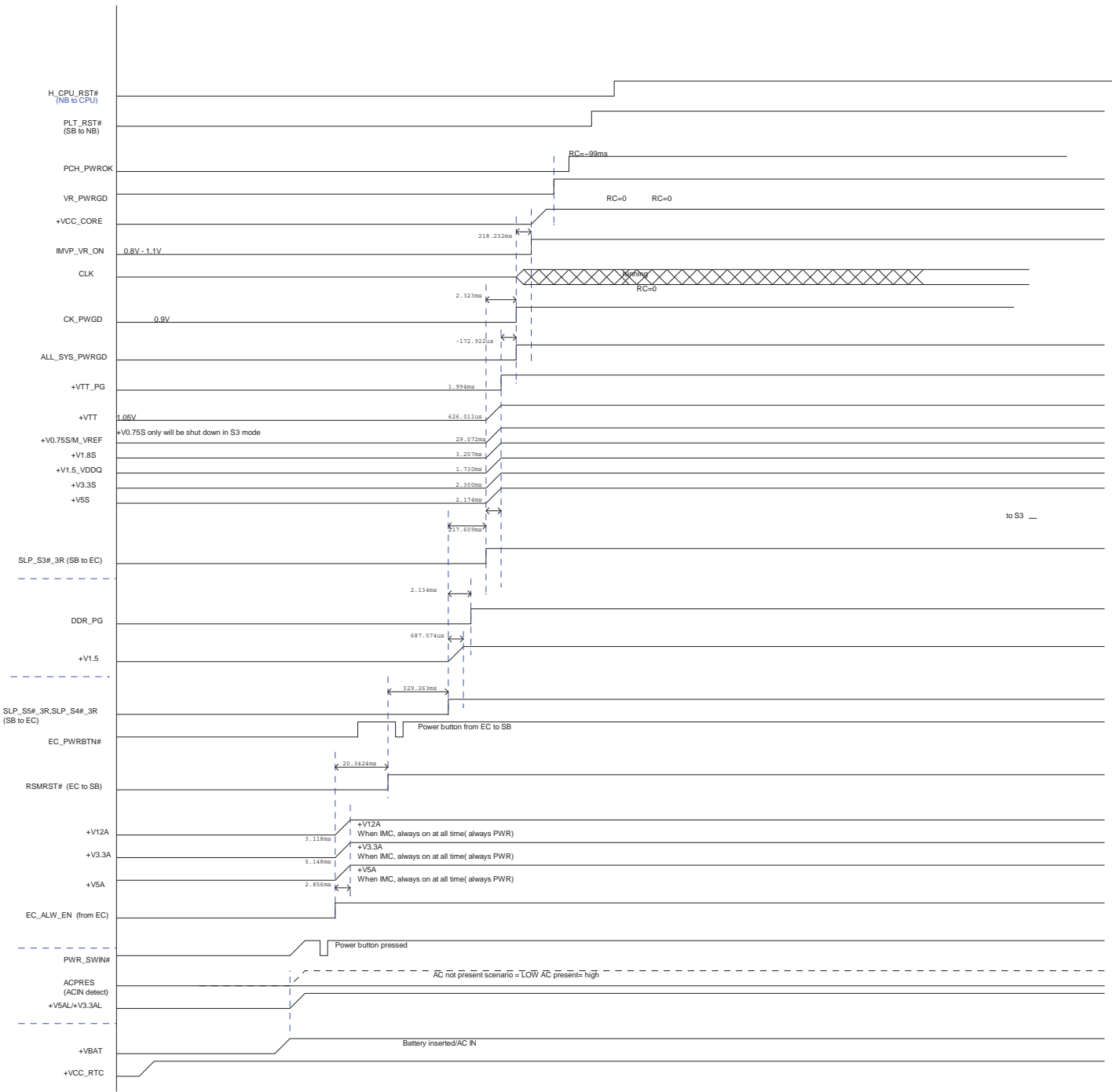
- GL40:
 1. +V3.3A ramp before +V1.1A
 2. +V3.3S ramp before +V1.8S
 3. +V1.8S ramp before +V1.1S
 4. +V3.3S ramp before +V1.1S

- ICH9-M:
 1. 0 < (+V3.3S) - (+V1.8S) < 2.1
 2. +V1.8S ramp before +V1.1S
 3. +V1.1S ramp before VCC_NB



CK505
ICS9LPRS397DKLFT





Power on Sequence required:

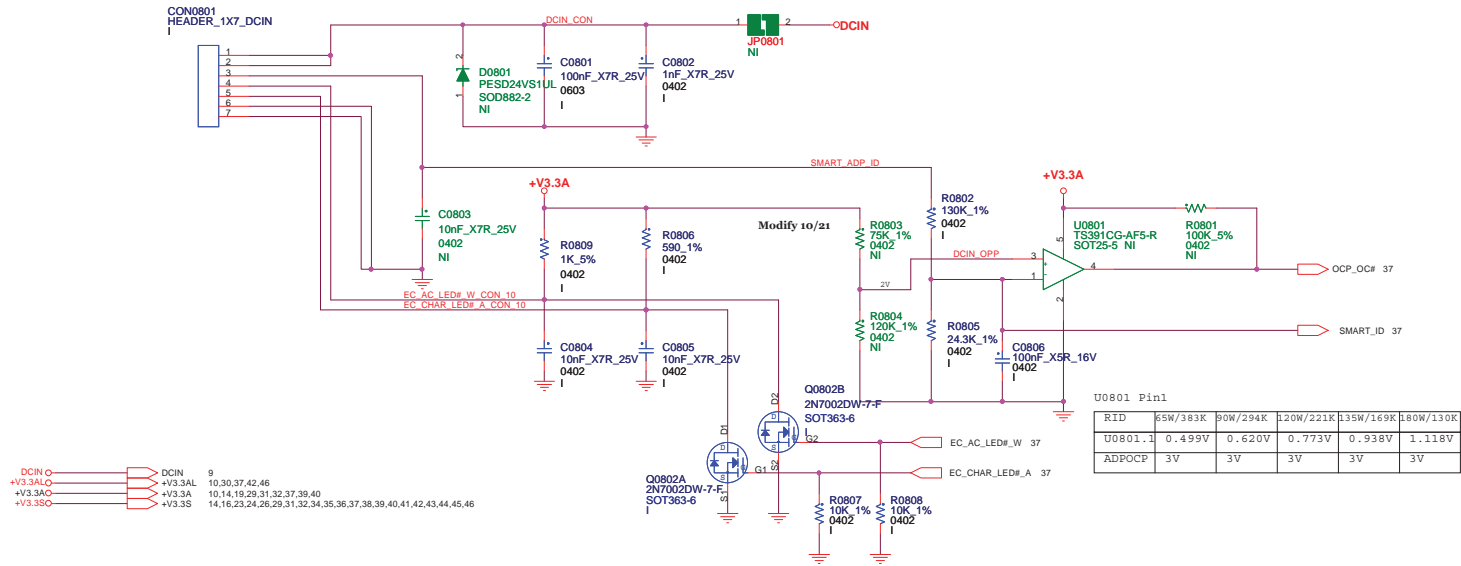
ICH9M:

- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 5, +V3.3A ramping down time > 300us
- 6, 50uS <= All power rails except +V3.3A <= 40ms
- 7, 100uS <= +V3.3A <= 40ms

GMCH:

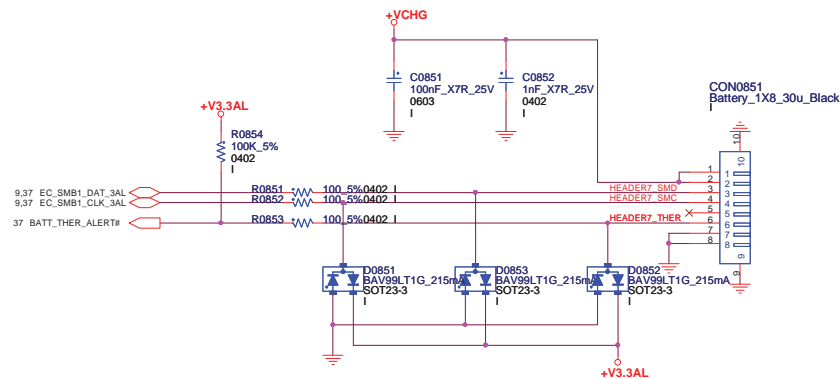
- 1, 0 < (+V3.3S) - (+V1.8S) < 2.1
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before +VCC_NB

DC_JACK WIRE to BOARD CONNECTOR

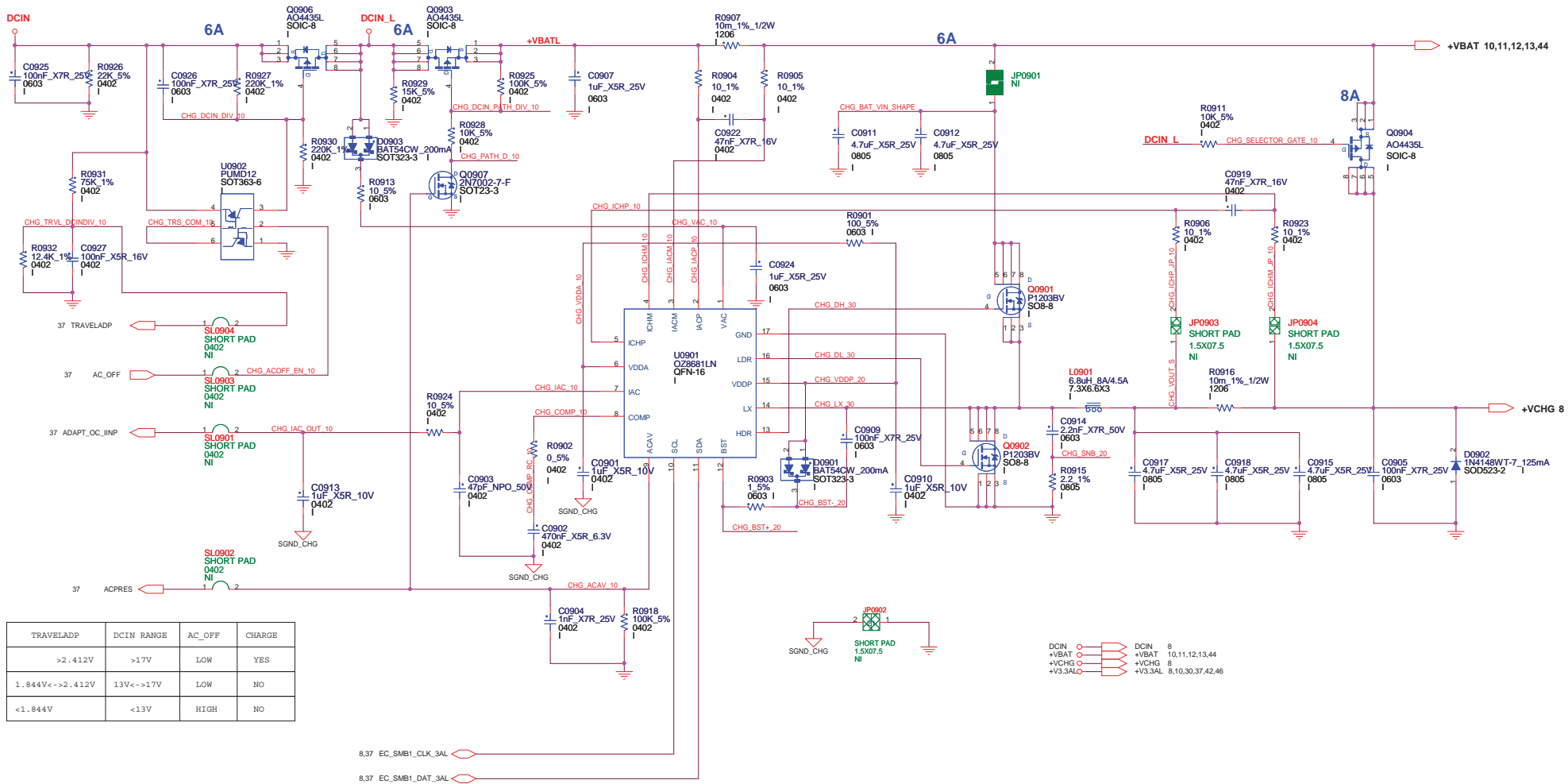


BATTERY CONNECTOR

2010.0914.0



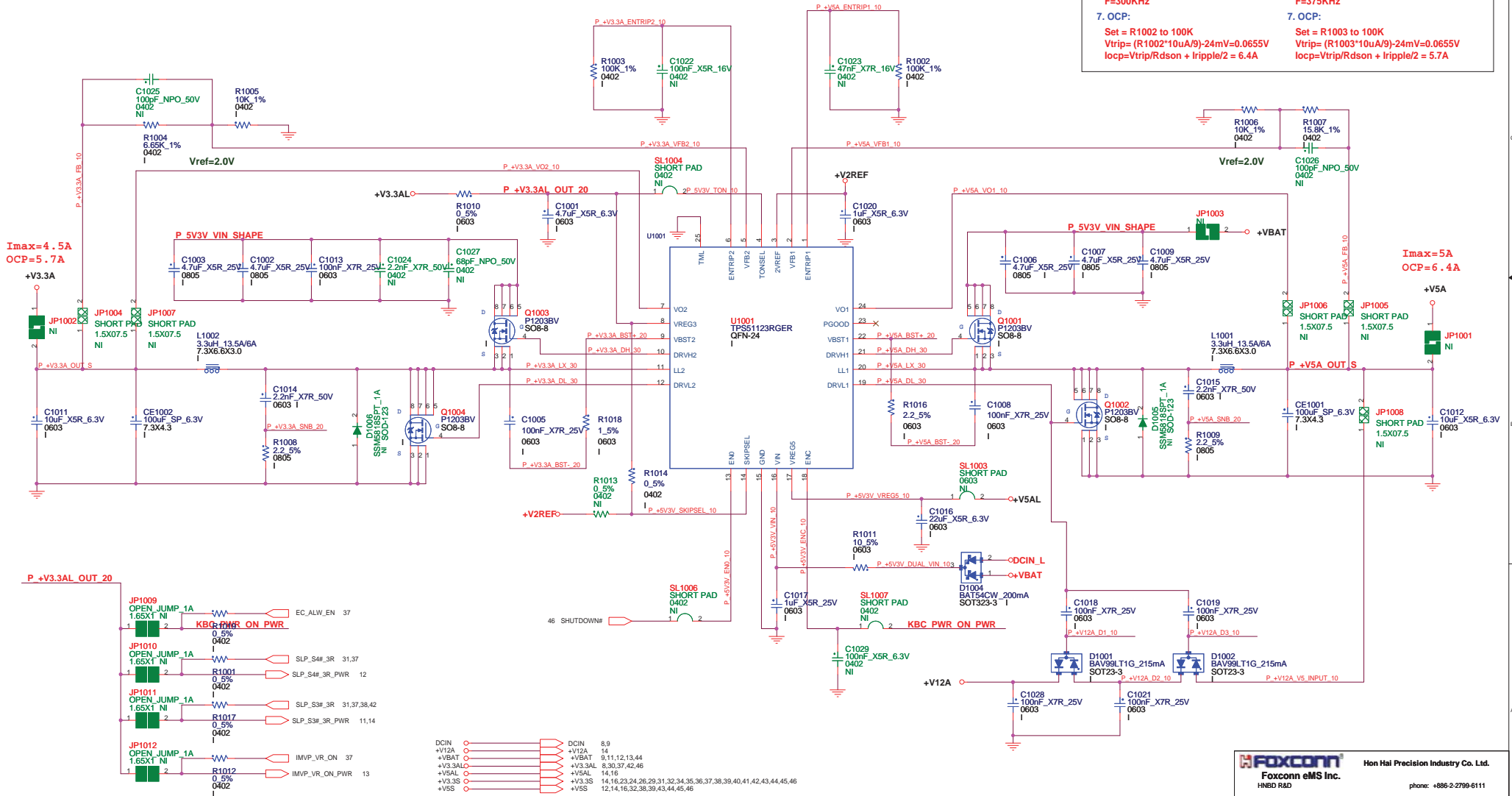
BATTERY CHARGER



+V5A / +V3.3A POWER SUPPLY

2010.1103.0

+V5A:	+V3.3A:
1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.7A$	1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.2A$
2. Ripple Current: $I_{rip} = 3.72A$	2. Ripple Current: $I_{rip} = 2.21A$
3. Ripple Voltage: ESR/1 = 15mohm $V_{rip} = 55.8mV$	3. Ripple Voltage: ESR/1 = 15mohm $V_{rip} = 33.15mV$
4. Inductor Spec: Isat = 13.5A I _{dc} = 6A DCR = 30mohm	4. Inductor Spec: Isat = 13.5A I _{dc} = 6A DCR = 30mohm
5. MOSFET Spec: H-side MOSFET: IRF8707PBF R _{ds(ON)} = 17.5mohm (V _{gs} = 4.5 V) I _{cont} = 11A (T = 25 °C) I _{peak} = 88A (Pause = 10 us)	L-side MOSFET: IRF8707PBF R _{ds(ON)} = 17.5mohm (V _{gs} = 4.5 V) I _{cont} = 11A (T = 25 °C) I _{peak} = 88A (Pause = 10 us)
6. Frequency: F = 300KHz	6. Frequency: F = 375KHz
7. OCP: Set = R1002 to 100K $V_{trip} = (R1002 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 6.4A$	7. OCP: Set = R1003 to 100K $V_{trip} = (R1003 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 5.7A$



DCIN	8,9
+V12A	14
+VBAT	8,11,12,13,44
+V3.3AL	8,30,37,42,46
+V5AL	14,16
+V3.3S	14,16,23,24,26,29,31,32,34,35,36,37,38,39,40,41,42,43,44,45,46
+V5S	12,14,16,32,38,39,43,44,45,46

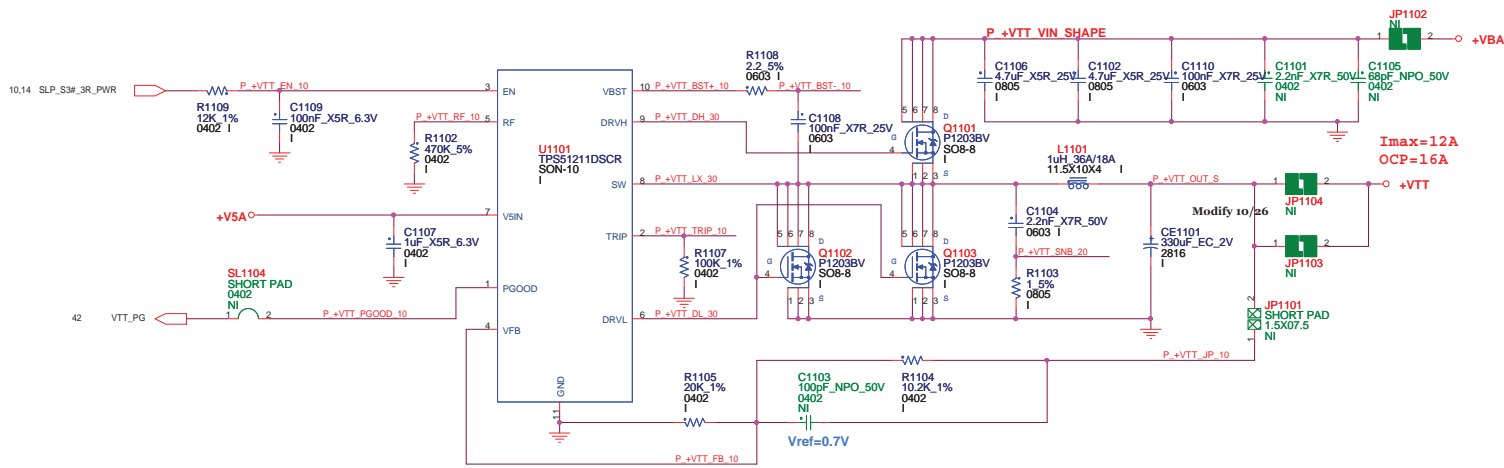
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Title: **5V/3.3V**

Size	Document Number	Rev
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Page Modified: Monday, January 24, 2011 09:08:38 (UTC+08:00) Sheet 10 of 43

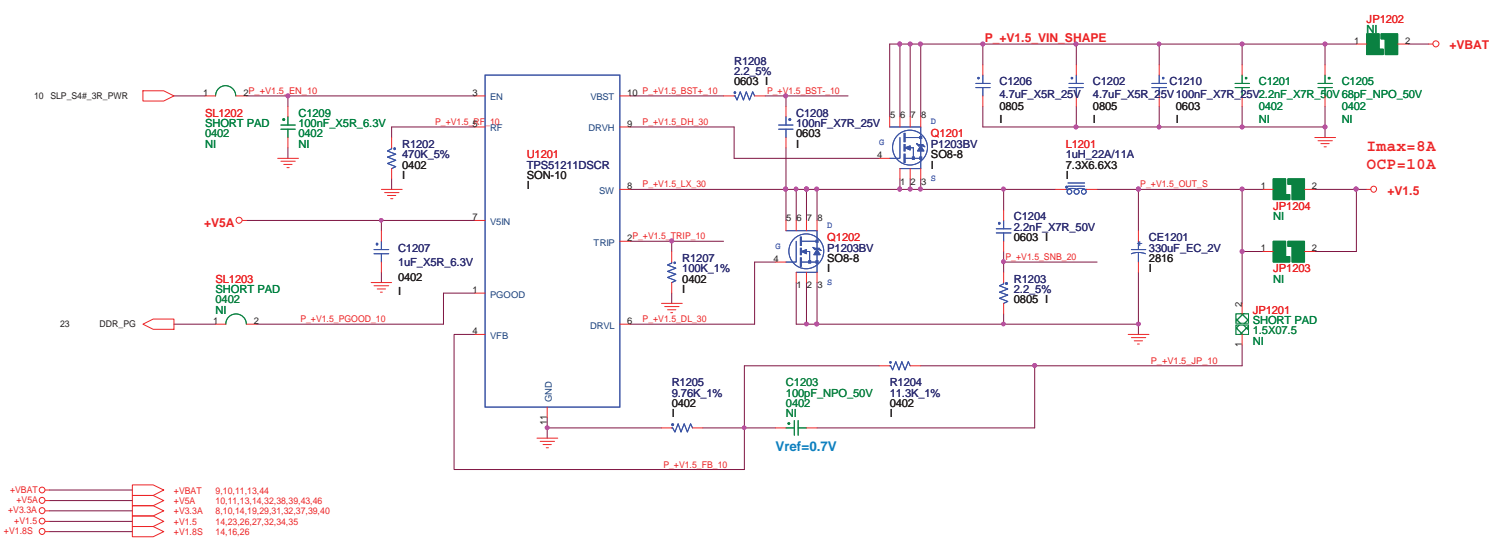
+VTT POWER SUPPLY



- +VTT:**
- I/P Current:**
 $I_{in} = V_o * I_o / (0.75 * V_{in}) = 1.86A$
 - Ripple Current:**
 $I_{rip} = 3.42A$
 - Ripple Voltage:**
 $ESR/1 = 9mohm$
 $V_{rip} = 30.78mV$
 - Inductor Spec:**
 $I_{sat} = 36A$
 $I_{dc} = 18A$
 $DCR = 3.3mohm$
 - MOSFET Spec:**
H-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 17.5mohm$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause = 10 us)
L-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 17.5mohm$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause = 10 us)
 - Frequency:**
 $F = 290KHz$ ($R_{0802} = 470K$)
 - OCp:**
 $Set = R_{0807}$ to 100K
 $V_{trips} = R_{0807} * I_o = 1V$
 $I_{ocp} = (V_{trips} / 8 * R_{dson}) + I_{ripple} / 2 = 16A$

+V3.3S	+V3.3S	14,16,23,24,26,29,31,32,34,35,36,37,38,39,40,41,42,43,44,45,46
+VSS	+VSS	12,14,16,32,38,39,43,44,45,46
+VBAT	+VBAT	9,10,12,13,44
+VTT	+VTT	13,14,19,20,21,22,23,24,26,27,30,32,36,46

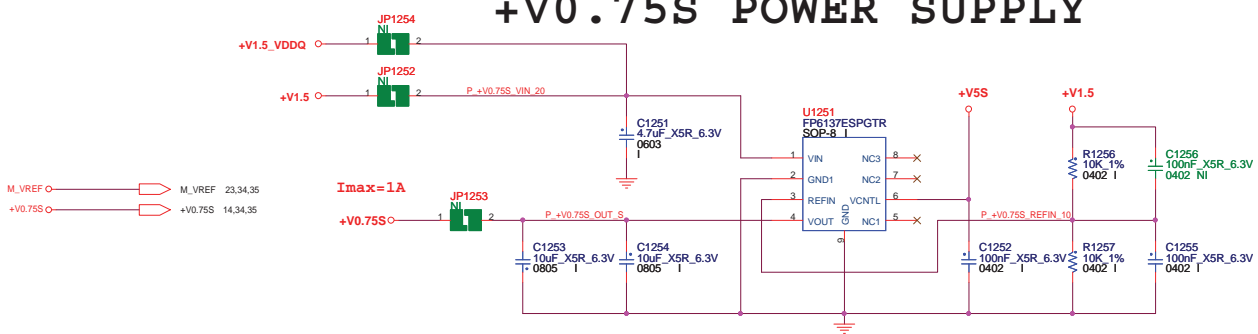
+V1.5 POWER SUPPLY



- +V1.5:**
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.78A$
 - Ripple Current:**
 $I_{rip} = 3.34A$
 - Ripple Voltage:**
 $ESR/1 = 9m\Omega$
 $V_{rip} = 30.6mV$
 - Inductor Spec:**
 $I_{sat} = 36A$
 $I_{dc} = 18A$
 $DCR = 3.3m\Omega$
 $I_{max} = 8A$
 $OCP = 1.0A$
 - MOSFET Spec:**
H-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause = 10 us)
L-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause = 10 us)
 - Frequency:**
 $F = 290KHz$ ($R_{0902} = 470K$)
 - OCP:**
 Set = R0907 to 100K
 $V_{trip} = R_{0907} \cdot I_o = 1V$
 $I_{ocp} = (V_{trip} / 8 \cdot R_{dson}) + I_{ripple} / 2 = 9.5A$

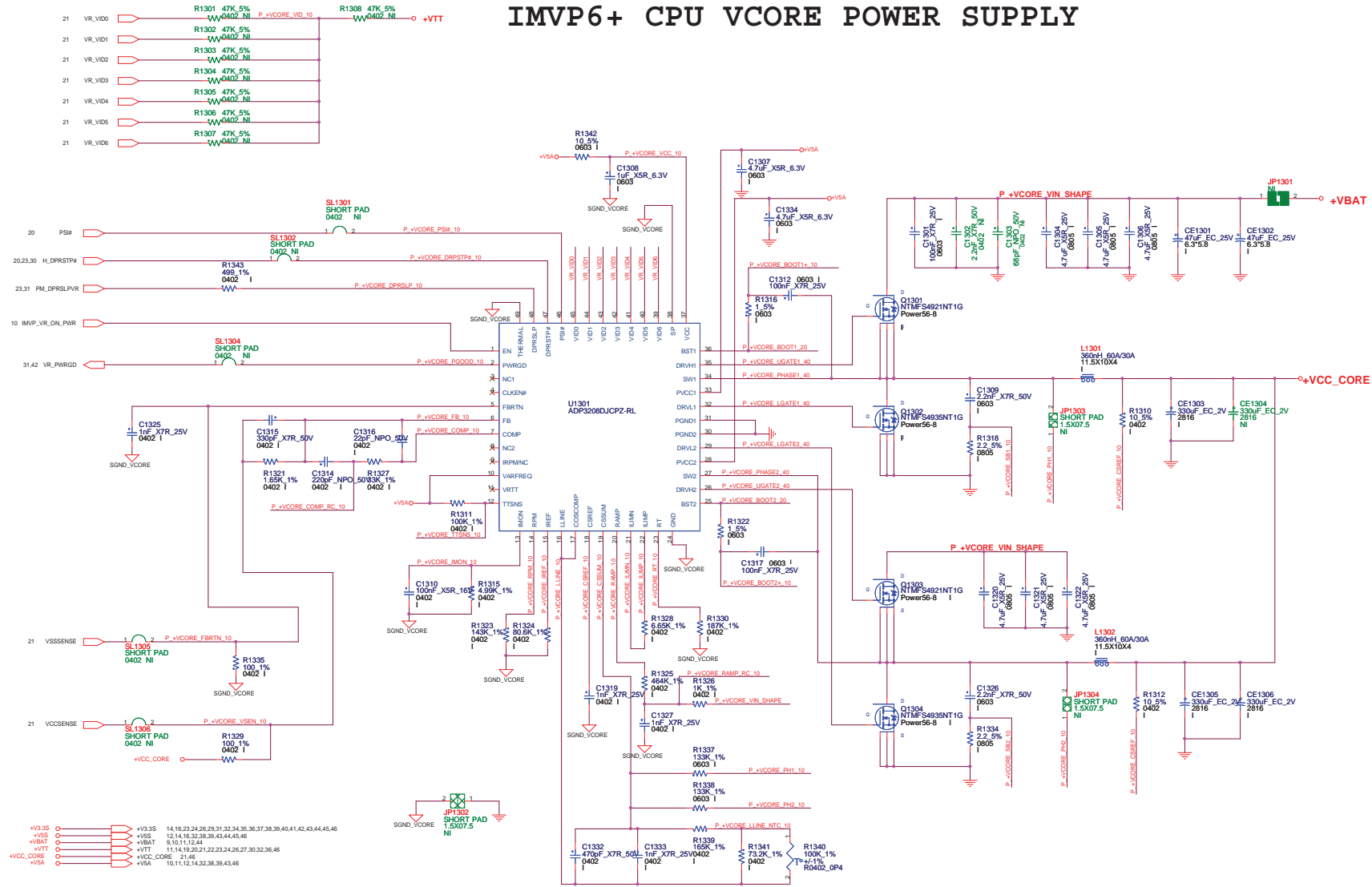
+VBATO	+VBAT	9,10,11,13,44
+V5AO	+V5A	10,11,13,14,32,38,39,43,46
+V3.3AO	+V3.3A	8,10,14,16,28,31,32,37,39,40
+V1.5AO	+V1.5	14,23,26,27,32,34,35
+V1.8S	+V1.8S	14,16,26

+V0.75S POWER SUPPLY



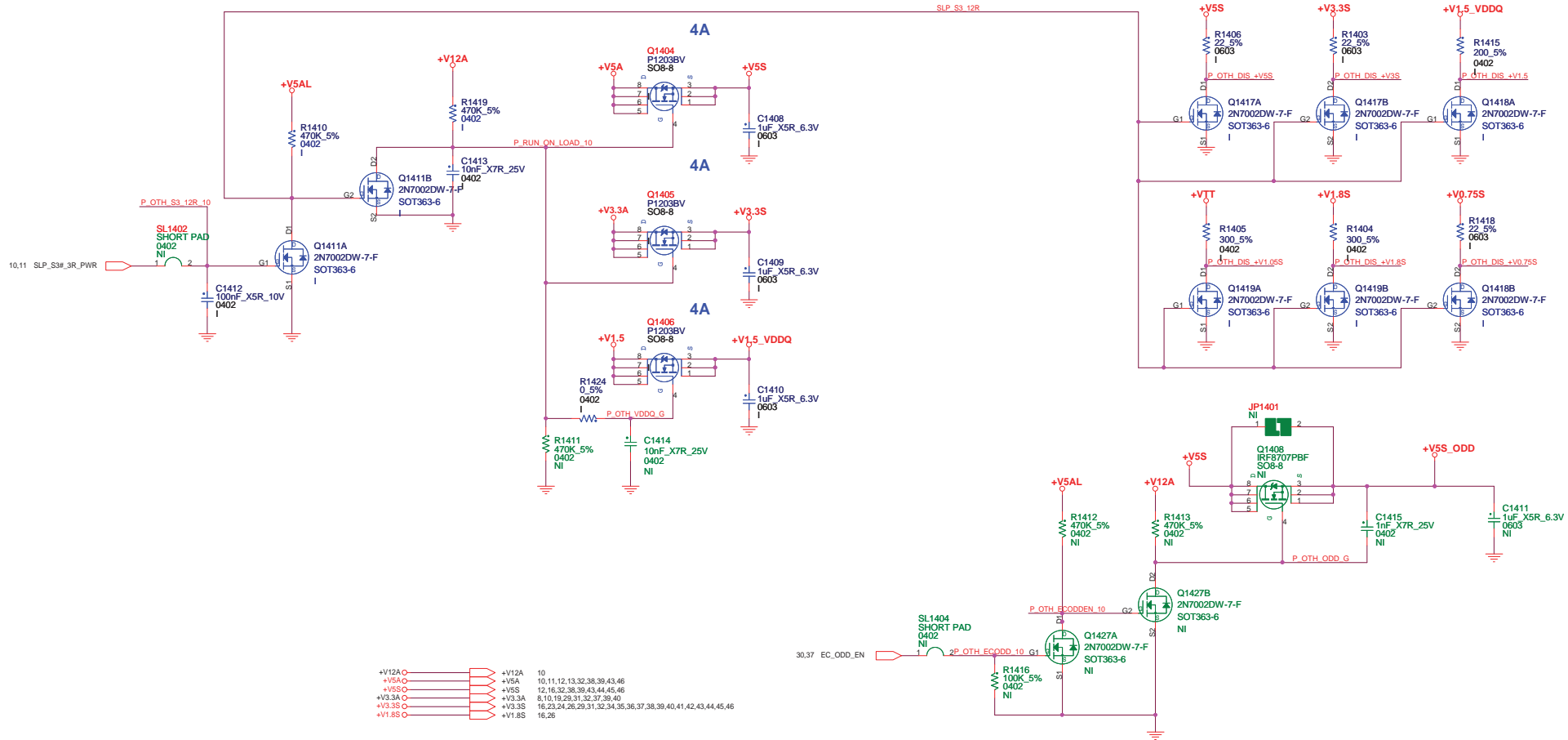
M_VREF	M_VREF	23,34,35
+V0.75S	+V0.75S	14,34,35

IMVP6+ CPU VCORE POWER SUPPLY



+V3S	14,16,23,24,26,29,31,32,34,35,36,37,38,39,40,41,42,43,44,45,46
+V5	12,14,16,32,38,39,43,44,45,46
+V8T	9,10,11,12,44
+VTT	11,14,19,20,21,22,23,24,26,27,30,32,36,46
+VCC_CORE	21,46
+VISA	10,11,12,14,32,38,39,43,46

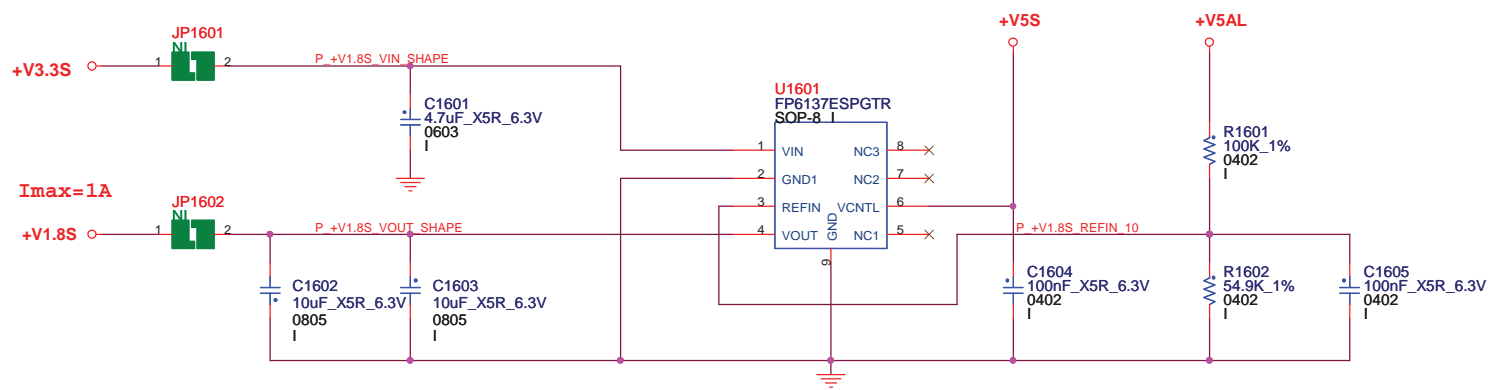
OTHER POWER / DISCHARGE CIRCUITS





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Size	Document Number	Rev	
Cust	FW-F101/TPN-F102 Montevina platform	0.1	
Page Number	Monday, January 24, 2011	64852 (P175287)	Sheet 15 of 46

+V1.8S POWER SUPPLY

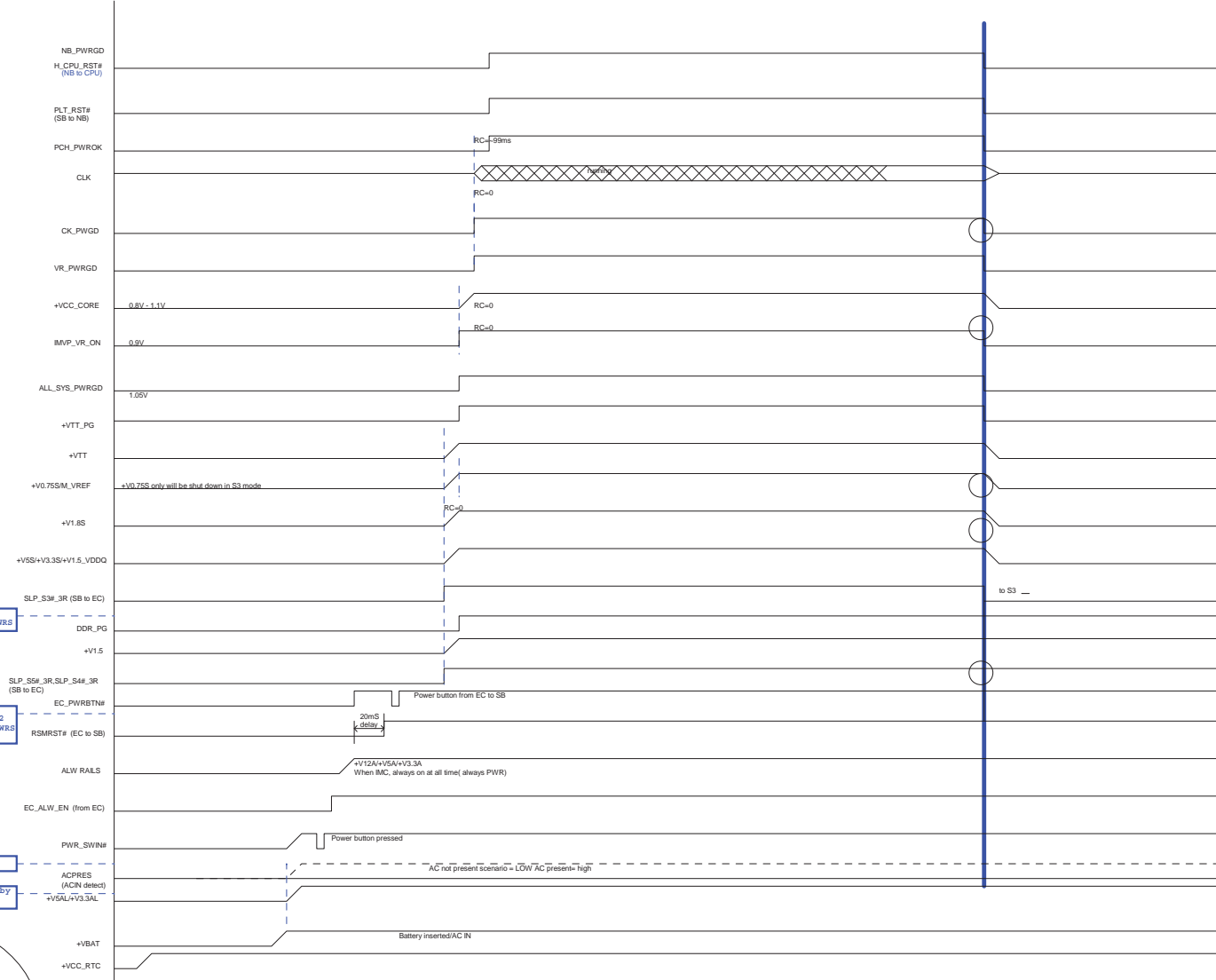


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Customer	CHICAGO		0.1
Page Modified: Monday, January 24, 2011		08:43:02 (UTC/GMT)	Sheet 16 of 46



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Title: <Title>			
Size:	Document Number:	Rev:	
Cust: TPN-F101/TPN-F102 Montevina platform		0.1	
Page Number: Monday, 24 Oct 2011		Sheet 12 of 46	

Signals	Test Point
LDT_RST#	CX61
LDT_PG	RX23
CPU_CLKP/N	CX72 ; CX73
NB_PWRGD	RX30
SB_PWRGD	DS63
+VCC_NB	PJ212
+VLDT	PJP15/2
+V1.1S	PJP15/1
VRM_PWRGD	DB72
+VDDR_CPU	PJ16/1
+VCC_CORE	PCE12
+VDDNB_CPU	PJ17/2
VDDA_PWRGD	PR211
+VDDA_CPU	PJ22/2
+V1.5S	PJ28/1
V1.8S_PWRGD	DS71
+V1.8S	PJ21
+V3.3S	PC170
+V5S	PC175
+V12S	PQ41/D
SLP_S3M_3R	RS60
+V0.75S	PJ8/2
M_VREF	PC182
+V1.5	RS76
SLP_S5M_3R	DB/2
EC_PWRBTN#	DB/2
RSMRST#	RS61
+V1.1A	PJ23/2
+V3.3A	PC109
+V5A	PJ25
+V12A	PC169
EC_ALW_EN	PQ27/G
PWR_SWIN#	HEADER2/B
ACPRES	RS51
+V5A/L	PC164
+V3.3A/L	PJ24
MS1ALDO	PC61
+VBAT	PJ19/2
+VCC_RTC	CS48



CPU MEM CTL & DDR3 SODIMM PWRB

CPU TMM/SB/SB_SCL1/2 SB_KB/SPI/LPC ROM PWRB

KBC is ready

KBC is powered by +V3.3A/L

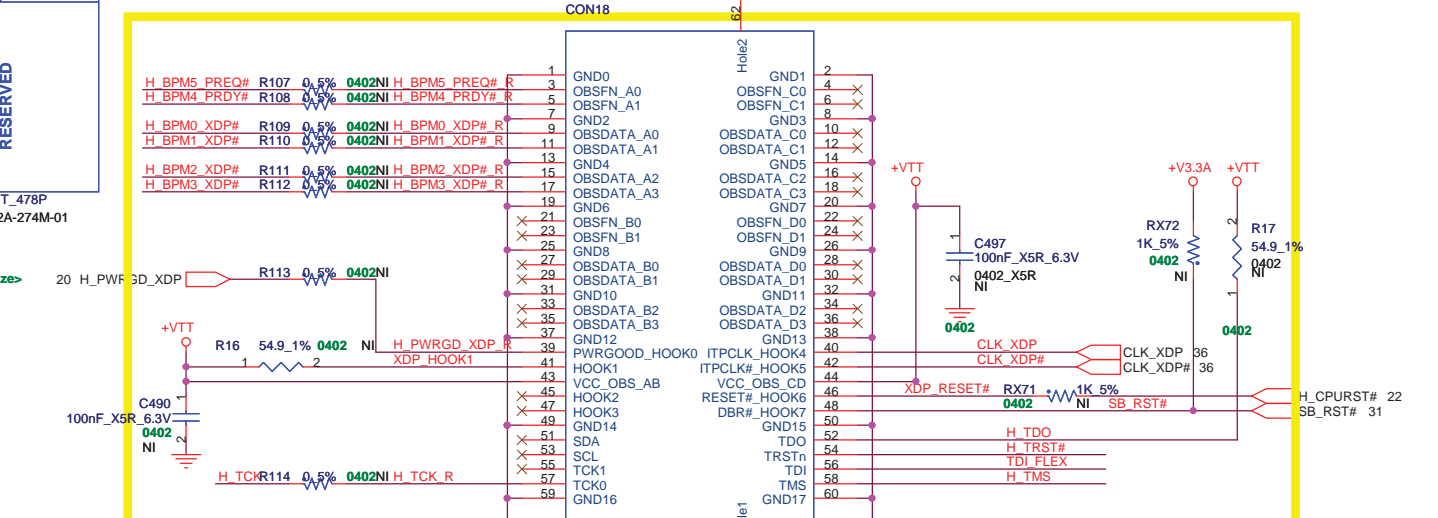
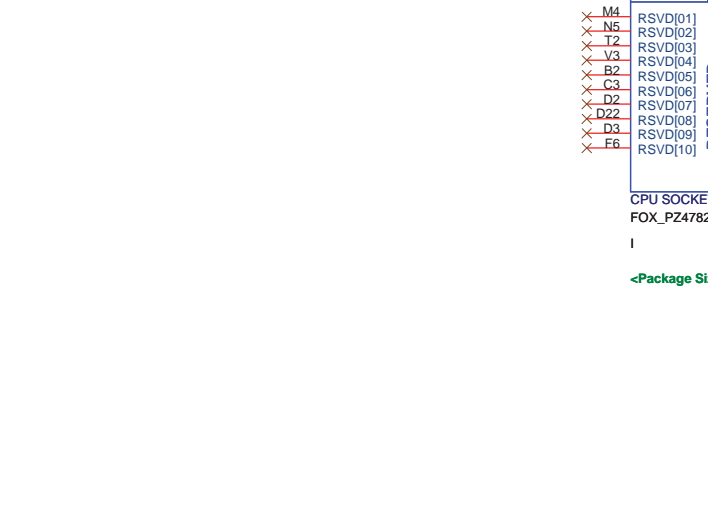
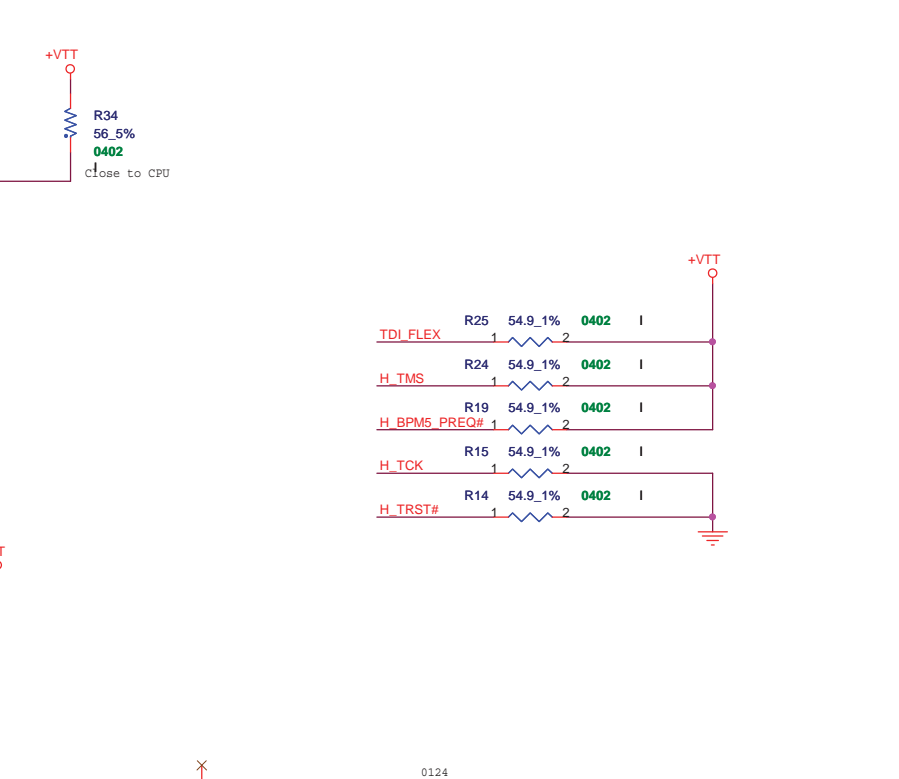
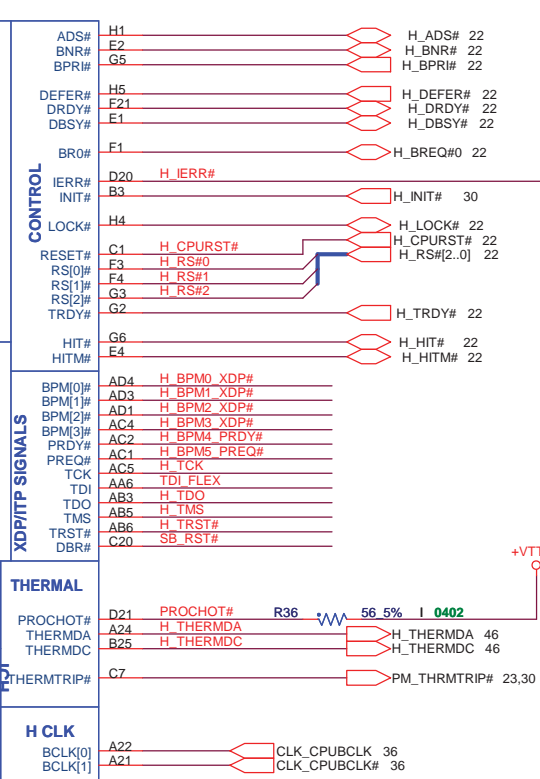
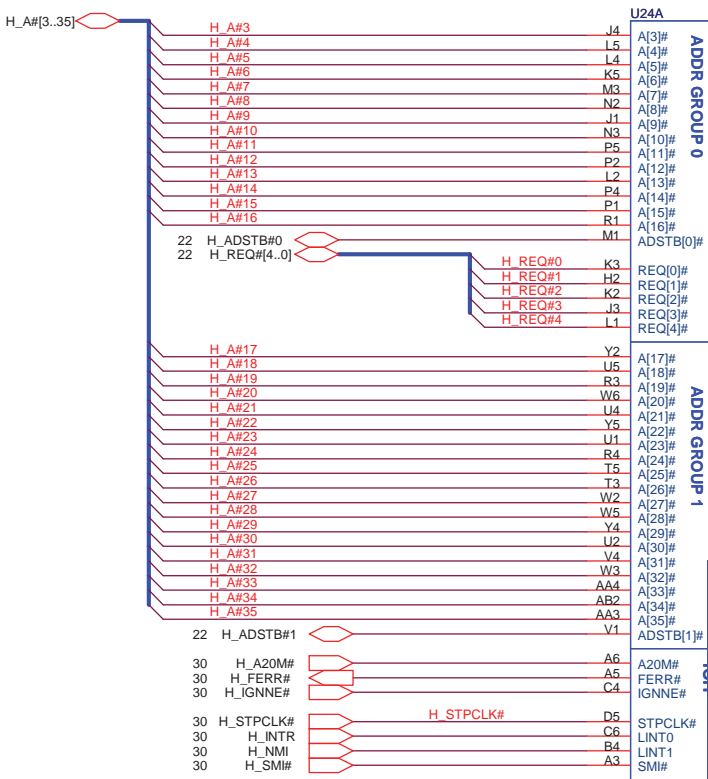
Power on Sequence required:

ICHM:

- +V3.3A ramp before +V1.1A
- +V3.3S ramp before +V1.8S
- +V1.8S ramp before +V1.1S
- +V3.3A ramping down time > 300us
- +V3.3A ramping down time > 300us
- 50us <= All power rails except +V3.3A <= 40mS
- 100us <= +V3.3A <= 40mS

GMCH:

- 0 <= (+V3.3S) - (+V1.8S) < 2.1
- +V1.8S ramp before +V1.1S
- +V1.1S ramp before +VCC_NB

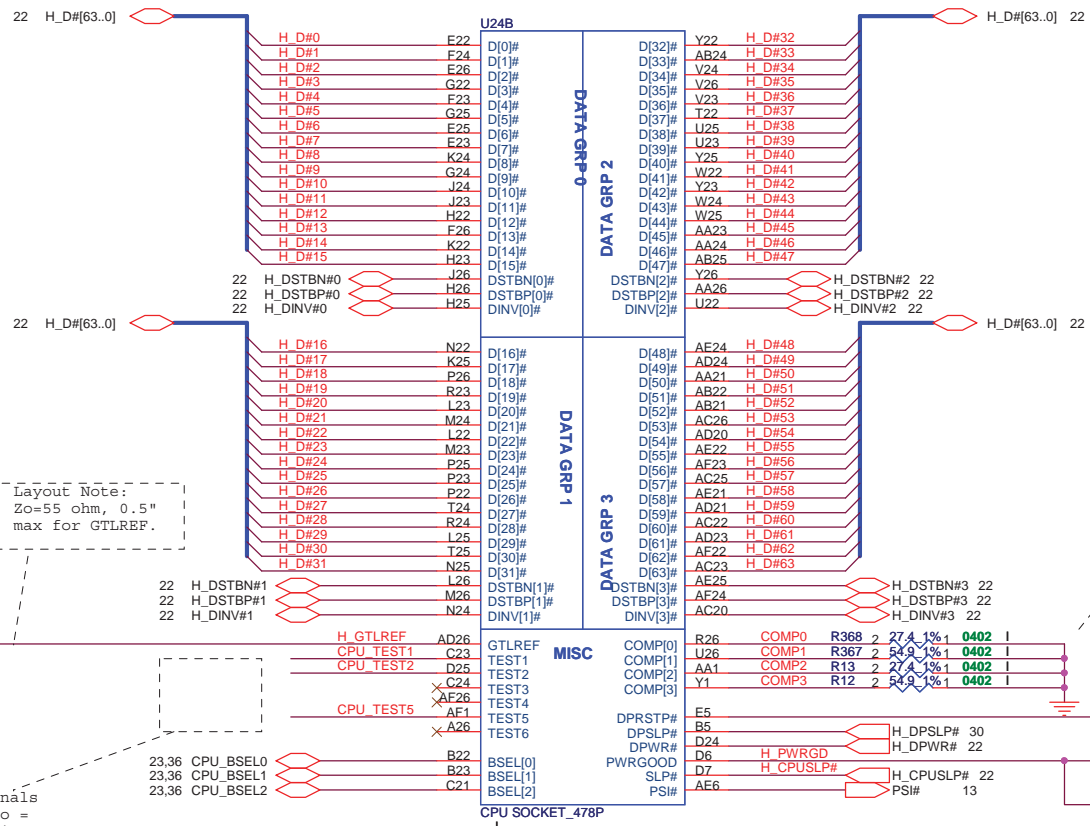


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Title		
Penryn (HOST BUS) 1/3		
Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina	
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)		Sheet 19 of 46

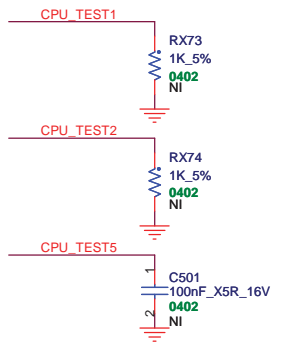


Layout Note:
 Zo=55 ohm, 0.5"
 max for GTLREF.

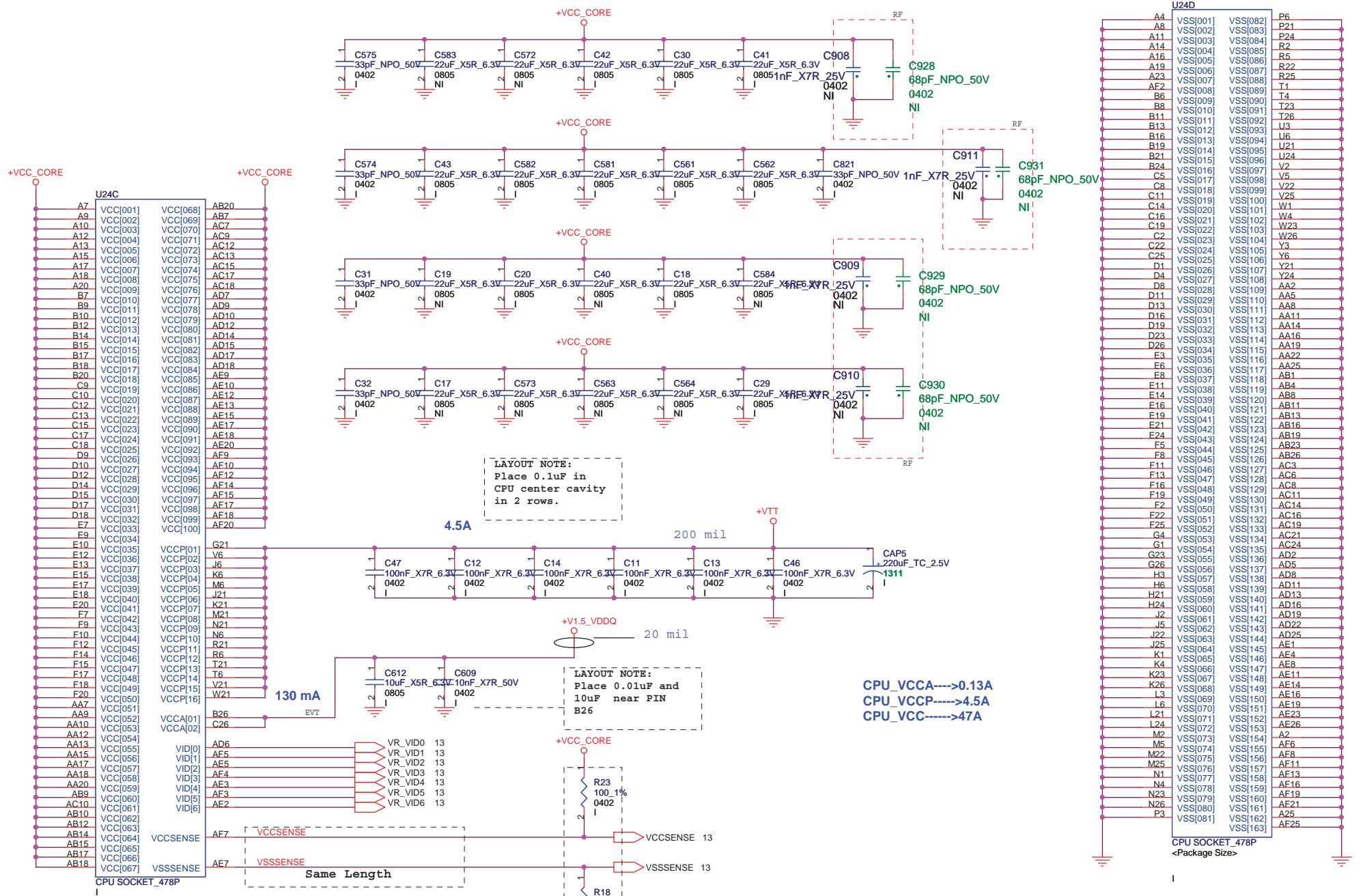
Layout Note:
 Comp0,2 connect with Zo=27.4 ohm, make trace
 length shorter then 0.5". Width=18mil(MS)
 Comp1,3 connect with Zo=55 ohm, make trace
 length shorter then 0.5". Width=5mil(MS)

Place close to CPU

Route the TEST3 and TEST5 signals
 through a ground referenced Zo =
 55-ohm trace that ends in a via
 that is near a GND via and is
 accessible through an oscilloscope
 connection. TEST4 and TEST6 and
 TEST7 pins can be left NC.



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Title Penryn (HOST BUS) 2/3			
Size Custom	Document Number TPN-F101/TPN-F102 Montevina	Rev 1	
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)		Sheet 20 of 46	



Outer width=18 mil spacing=7 mil
 Inner width=14 mil spacing=7 mil
 Length match < 25 mil

Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 1 inch of CPU.

PU & PD avoid to route with stub

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Title					
Penryn (POWER/GROUND) 3/3					
Size	Document Number				Rev
Custom		TPN-F101/TPN-F102 Montevina			
Page Modified: Monday, January 24, 2011			09:05:39 (UTC/GMT)		Sheet 21 of 46

20 H_D#[63..0] H_D#[63..0]

U27A

- H_D#0 E2 H_D#_0
- H_D#1 G8 H_D#_1
- H_D#2 F8 H_D#_2
- H_D#3 E6 H_D#_3
- H_D#4 G2 H_D#_4
- H_D#5 H6 H_D#_5
- H_D#6 H2 H_D#_6
- H_D#7 F6 H_D#_7
- H_D#8 D4 H_D#_8
- H_D#9 H3 H_D#_9
- H_D#10 M9 H_D#_10
- H_D#11 M11 H_D#_11
- H_D#12 J1 H_D#_12
- H_D#13 J2 H_D#_13
- H_D#14 N12 H_D#_14
- H_D#15 J6 H_D#_15
- H_D#16 P2 H_D#_16
- H_D#17 L2 H_D#_17
- H_D#18 R2 H_D#_18
- H_D#19 N9 H_D#_19
- H_D#20 L6 H_D#_20
- H_D#21 M5 H_D#_21
- H_D#22 J3 H_D#_22
- H_D#23 N2 H_D#_23
- H_D#24 R1 H_D#_24
- H_D#25 N5 H_D#_25
- H_D#26 N6 H_D#_26
- H_D#27 P13 H_D#_27
- H_D#28 N8 H_D#_28
- H_D#29 L7 H_D#_29
- H_D#30 N10 H_D#_30
- H_D#31 M3 H_D#_31
- H_D#32 Y3 H_D#_32
- H_D#33 AD14 H_D#_33
- H_D#34 Y6 H_D#_34
- H_D#35 Y10 H_D#_35
- H_D#36 Y12 H_D#_36
- H_D#37 Y14 H_D#_37
- H_D#38 Y7 H_D#_38
- H_D#39 W2 H_D#_39
- H_D#40 AA8 H_D#_40
- H_D#41 Y9 H_D#_41
- H_D#42 AA13 H_D#_42
- H_D#43 AA9 H_D#_43
- H_D#44 AA11 H_D#_44
- H_D#45 AD11 H_D#_45
- H_D#46 AD10 H_D#_46
- H_D#47 AD13 H_D#_47
- H_D#48 AE12 H_D#_48
- H_D#49 AE9 H_D#_49
- H_D#50 AA2 H_D#_50
- H_D#51 AD8 H_D#_51
- H_D#52 AA3 H_D#_52
- H_D#53 AD3 H_D#_53
- H_D#54 AD7 H_D#_54
- H_D#55 AE14 H_D#_55
- H_D#56 AE3 H_D#_56
- H_D#57 AC1 H_D#_57
- H_D#58 AE3 H_D#_58
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- H_D#61 AE8 H_D#_61
- H_D#62 AG2 H_D#_62
- H_D#63 AD6 H_D#_63

- H_A#_3 A14 H_A#3
- H_A#_4 C15 H_A#4
- H_A#_5 F16 H_A#5
- H_A#_6 H13 H_A#6
- H_A#_7 C18 H_A#7
- H_A#_8 M16 H_A#8
- H_A#_9 J13 H_A#9
- H_A#_10 P16 H_A#10
- H_A#_11 R16 H_A#11
- H_A#_12 N17 H_A#12
- H_A#_13 M13 H_A#13
- H_A#_14 P17 H_A#14
- H_A#_15 F17 H_A#15
- H_A#_16 G20 H_A#16
- H_A#_17 B19 H_A#17
- H_A#_18 J16 H_A#18
- H_A#_19 E20 H_A#19
- H_A#_20 H16 H_A#20
- H_A#_21 J20 H_A#21
- H_A#_22 L17 H_A#22
- H_A#_23 A17 H_A#23
- H_A#_24 B17 H_A#24
- H_A#_25 L16 H_A#25
- H_A#_26 C21 H_A#26
- H_A#_27 J17 H_A#27
- H_A#_28 H20 H_A#28
- H_A#_29 B18 H_A#29
- H_A#_30 K17 H_A#30
- H_A#_31 B20 H_A#31
- H_A#_32 F21 H_A#32
- H_A#_33 K21 H_A#33
- H_A#_34 L20 H_A#34
- H_A#_35

H_A#[3..35] 19

- H_ADS# H12 H_ADS# 19
- H_ADSTB#_0 B16 H_ADSTB#0 19
- H_ADSTB#_1 G17 H_ADSTB#1 19
- H_BNR# A9 H_BNR# 19
- H_BPR# F11 H_BPR# 19
- H_BREQ# G12 H_BREQ# 19
- H_BREQ#_0 E9 H_BREQ#0 19
- H_DEFER# B10 H_DEFER# 19
- H_DBSY# AH7 H_DBSY# 19
- HPLL_CLK AH6 CLK_MCHBCLK 36
- H_DPWR# J11 H_DPWR# 20
- H_DRDY# F9 H_DRDY# 19
- H_HIT# H9 H_HIT# 19
- H_HITM# E12 H_HITM# 19
- H_LOCK# H11 H_LOCK# 19
- H_TRDY# C9 H_TRDY# 19

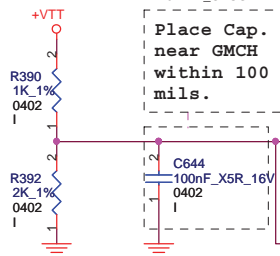
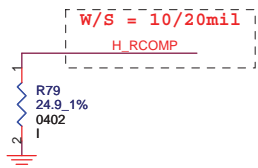
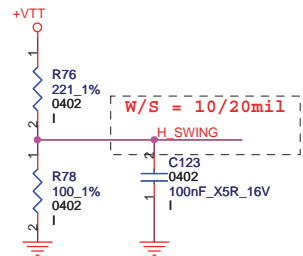
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- H_DIN#_0 J8 H_DIN#0 20
- H_DIN#_1 L3 H_DIN#1 20
- H_DIN#_2 Y13 H_DIN#2 20
- H_DIN#_3 Y1 H_DIN#3 20
- H_DSTB#_0 L10 H_DSTB#0 20
- H_DSTB#_1 M7 H_DSTB#1 20
- H_DSTB#_2 AA5 H_DSTB#2 20
- H_DSTB#_3 AE6 H_DSTB#3 20
- H_DSTBP#_0 L9 H_DSTBP#0 20
- H_DSTBP#_1 M8 H_DSTBP#1 20
- H_DSTBP#_2 AA6 H_DSTBP#2 20
- H_DSTBP#_3 AE5 H_DSTBP#3 20
- H_REQ#_0 B15 H_REQ#0 19
- H_REQ#_1 K13 H_REQ#1 19
- H_REQ#_2 F13 H_REQ#2 19
- H_REQ#_3 B13 H_REQ#3 19
- H_REQ#_4 B14 H_REQ#4 19
- H_RS#_0 B6 H_RS#0 19
- H_RS#_1 F12 H_RS#1 19
- H_RS#_2 C8 H_RS#2 19

H_SWING C5 H_SWING
H_RCOMP E3 H_RCOMP

H_CPURST# C12 H_CPURST#
H_CPUSLP# E11 H_CPUSLP#

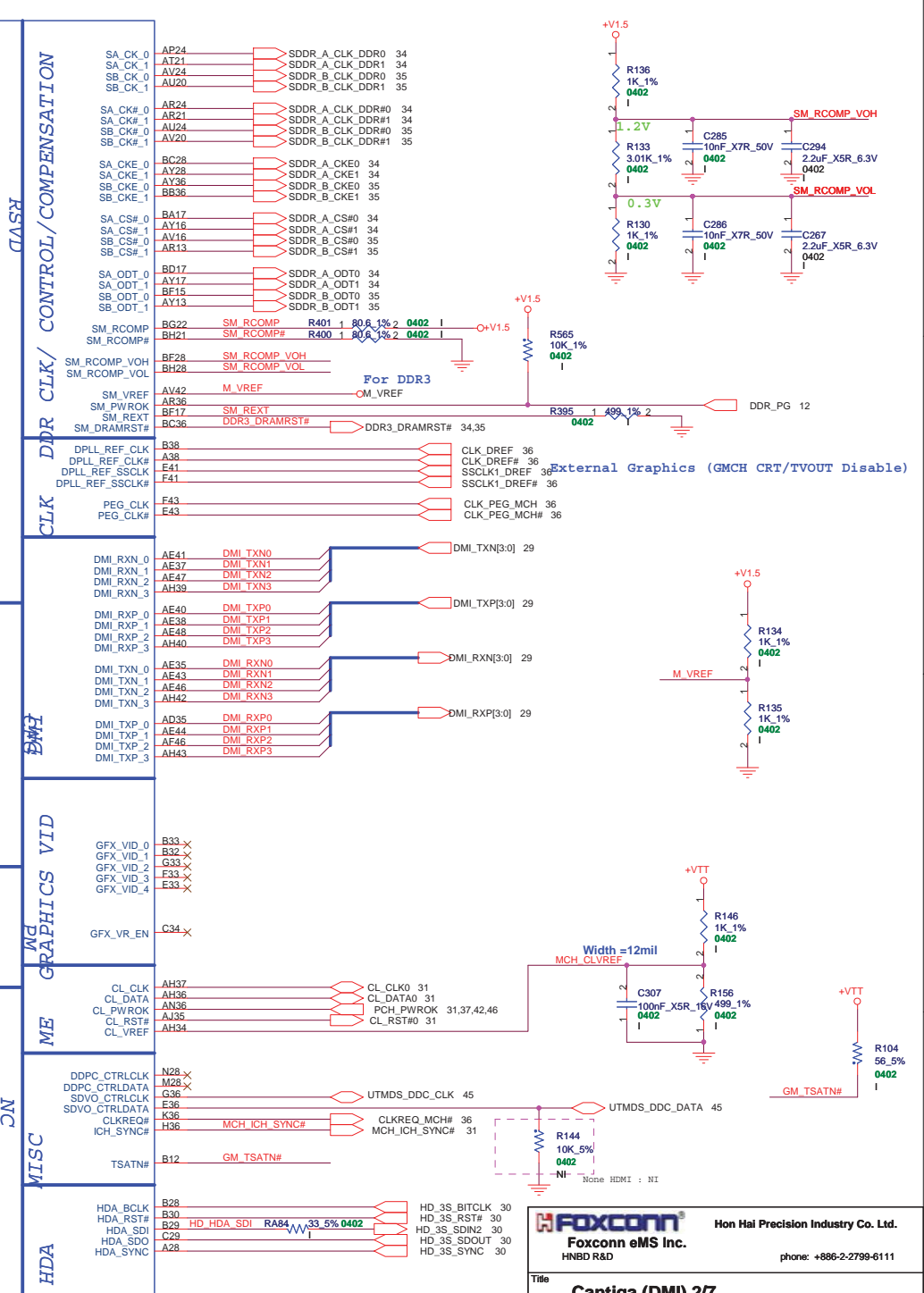
H_AVREF A11 H_AVREF
H_DVREF B11 H_DVREF
GL40



Traces width 10 mils.

MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low = The ITPM Host Interface is enabled High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Transport Layer Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIe Loopback enable	Low = Enabled High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode ([G]MCH->ICH): (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode ([G]MCH ->ICH): (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) and Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

- X M36
- X N36
- X R33
- X T33
- X AH9
- X AH10
- X AH12
- X AH13
- X K12
- X AL34
- X AK34
- X AN35
- X AM35
- X T24
- X B31
- X B2
- X M1
- X AY21
- X BG23
- X BF21
- X BH18
- X BF18
- X P23
- X P24
- X C25
- X P20
- X P21
- X P22
- X P27
- X P28
- X P29
- X P30
- X P31
- X P32
- X P33
- X P34
- X P35
- X P36
- X P37
- X P38
- X P39
- X P40
- X P41
- X P42
- X P43
- X P44
- X P45
- X P46
- X P47
- X P48
- X P49
- X P50
- X P51
- X P52
- X P53
- X P54
- X P55
- X P56
- X P57
- X P58
- X P59
- X P60
- X P61
- X P62
- X P63
- X P64
- X P65
- X P66
- X P67
- X P68
- X P69
- X P70
- X P71
- X P72
- X P73
- X P74
- X P75
- X P76
- X P77
- X P78
- X P79
- X P80
- X P81
- X P82
- X P83
- X P84
- X P85
- X P86
- X P87
- X P88
- X P89
- X P90
- X P91
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- X P95
- X P96
- X P97
- X P98
- X P99
- X P100

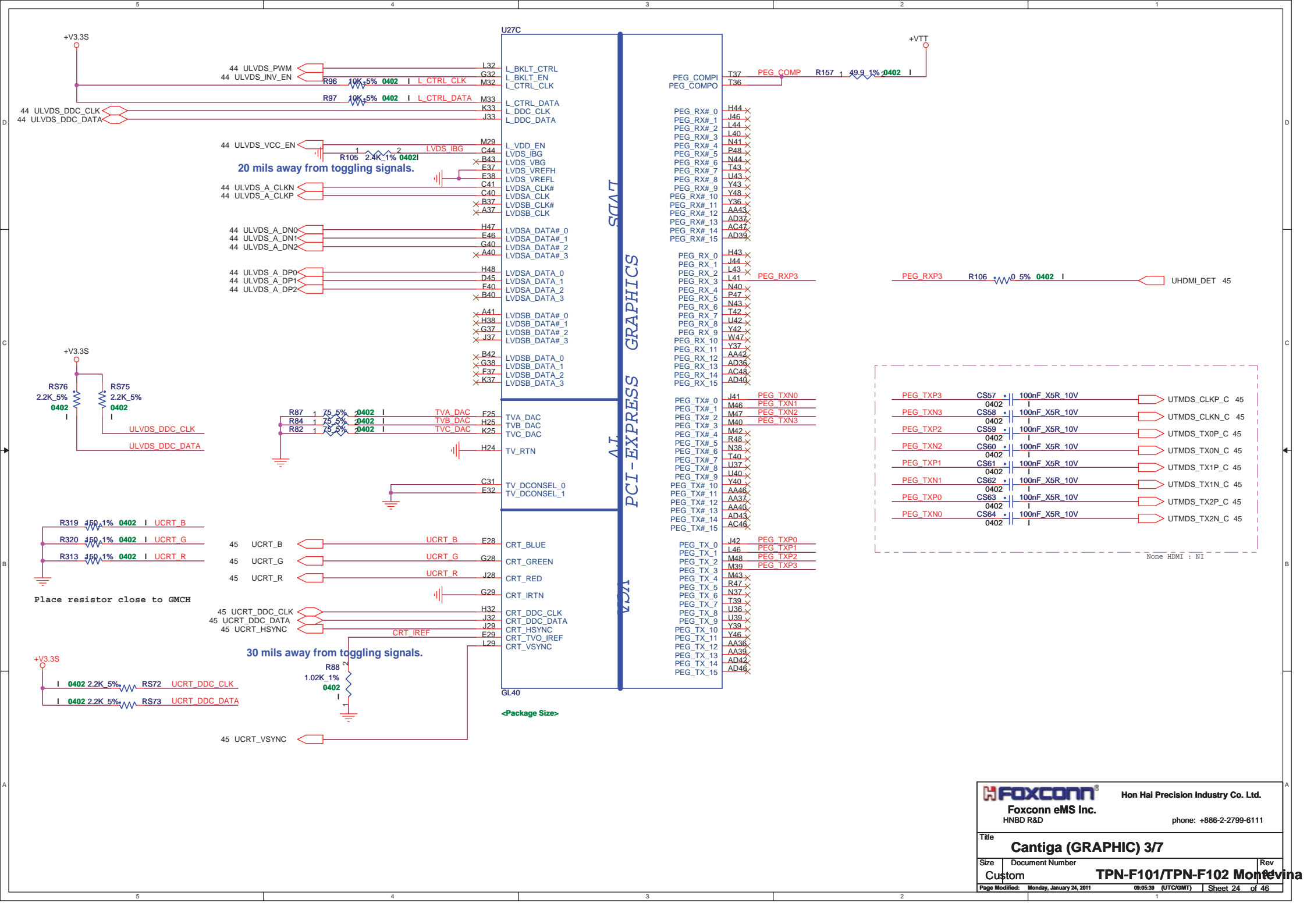


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Title: **Cantiga (DMI) 2/7**

Size: Document Number
Custom **TPN-F101/TPN-F102 Montevina pl** Rev

Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT) Sheet 23 of 46



20 mils away from toggling signals.

30 mils away from toggling signals.

Place resistor close to GMCH

PEG TXP3	CS57	100nF X5R 10V	UTMDS_CLKP_C 45
PEG TXN3	CS58	100nF X5R 10V	UTMDS_CLKN_C 45
PEG TXP2	CS59	100nF X5R 10V	UTMDS_TX0P_C 45
PEG TXN2	CS60	100nF X5R 10V	UTMDS_TX0N_C 45
PEG TXP1	CS61	100nF X5R 10V	UTMDS_TX1P_C 45
PEG TXN1	CS62	100nF X5R 10V	UTMDS_TX1N_C 45
PEG TXP0	CS63	100nF X5R 10V	UTMDS_TX2P_C 45
PEG TXN0	CS64	100nF X5R 10V	UTMDS_TX2N_C 45

None HDMI : NI

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Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina	
Page Modified: Monday, January 24, 2011 09:05:39 (UTC/GMT)		Sheet 24 of 46

34 SDDR_A_DQ[63..0]

- SDDR A DQ0 AJ38
- SDDR A DQ1 AJ41
- SDDR A DQ2 AN38
- SDDR A DQ3 AM38
- SDDR A DQ4 AJ36
- SDDR A DQ5 AJ40
- SDDR A DQ6 AM44
- SDDR A DQ7 AM42
- SDDR A DQ8 AN43
- SDDR A DQ9 AN44
- SDDR A DQ10 AU40
- SDDR A DQ11 AT38
- SDDR A DQ12 AN41
- SDDR A DQ13 AN39
- SDDR A DQ14 AU44
- SDDR A DQ15 AU42
- SDDR A DQ16 AV39
- SDDR A DQ17 AV39
- SDDR A DQ18 BA40
- SDDR A DQ19 BD43
- SDDR A DQ20 AV41
- SDDR A DQ21 AY43
- SDDR A DQ22 BB41
- SDDR A DQ23 BC40
- SDDR A DQ24 AY37
- SDDR A DQ25 BD38
- SDDR A DQ26 AV37
- SDDR A DQ27 AT36
- SDDR A DQ28 AY38
- SDDR A DQ29 BB38
- SDDR A DQ30 AV36
- SDDR A DQ31 AW36
- SDDR A DQ32 BD13
- SDDR A DQ33 AU11
- SDDR A DQ34 BC11
- SDDR A DQ35 BA12
- SDDR A DQ36 AU13
- SDDR A DQ37 AV13
- SDDR A DQ38 BD12
- SDDR A DQ39 BC12
- SDDR A DQ40 BB9
- SDDR A DQ41 BA9
- SDDR A DQ42 AU10
- SDDR A DQ43 AV9
- SDDR A DQ44 BA11
- SDDR A DQ45 BD9
- SDDR A DQ46 AY8
- SDDR A DQ47 BA6
- SDDR A DQ48 AV5
- SDDR A DQ49 AV7
- SDDR A DQ50 AT9
- SDDR A DQ51 AN8
- SDDR A DQ52 AU5
- SDDR A DQ53 AU6
- SDDR A DQ54 AT5
- SDDR A DQ55 AN10
- SDDR A DQ56 AM11
- SDDR A DQ57 AM5
- SDDR A DQ58 AJ9
- SDDR A DQ59 AJ8
- SDDR A DQ60 AN12
- SDDR A DQ61 AM13
- SDDR A DQ62 AJ11
- SDDR A DQ63 AJ12

DDR SYSTEM MEMORY A

U27D

- SA_DS_0
- SA_DS_1
- SA_DS_2
- SA_DS_3
- SA_DS_4
- SA_DS_5
- SA_DS_6
- SA_DS_7
- SA_DS_8
- SA_DS_9
- SA_DS_10
- SA_DS_11
- SA_DS_12
- SA_DS_13
- SA_DS_14
- SA_DS_15
- SA_DS_16
- SA_DS_17
- SA_DS_18
- SA_DS_19
- SA_DS_20
- SA_DS_21
- SA_DS_22
- SA_DS_23
- SA_DS_24
- SA_DS_25
- SA_DS_26
- SA_DS_27
- SA_DS_28
- SA_DS_29
- SA_DS_30
- SA_DS_31
- SA_DS_32
- SA_DS_33
- SA_DS_34
- SA_DS_35
- SA_DS_36
- SA_DS_37
- SA_DS_38
- SA_DS_39
- SA_DS_40
- SA_DS_41
- SA_DS_42
- SA_DS_43
- SA_DS_44
- SA_DS_45
- SA_DS_46
- SA_DS_47
- SA_DS_48
- SA_DS_49
- SA_DS_50
- SA_DS_51
- SA_DS_52
- SA_DS_53
- SA_DS_54
- SA_DS_55
- SA_DS_56
- SA_DS_57
- SA_DS_58
- SA_DS_59
- SA_DS_60
- SA_DS_61
- SA_DS_62
- SA_DS_63

GL40

35 SDDR_B_DQ[63..0]

- SDDR B DQ0 AK47
- SDDR B DQ1 AH46
- SDDR B DQ2 AP47
- SDDR B DQ3 AP46
- SDDR B DQ4 AJ46
- SDDR B DQ5 AJ48
- SDDR B DQ6 AM48
- SDDR B DQ7 AP48
- SDDR B DQ8 AU47
- SDDR B DQ9 AU46
- SDDR B DQ10 BA48
- SDDR B DQ11 AY48
- SDDR B DQ12 AT47
- SDDR B DQ13 AR47
- SDDR B DQ14 BA47
- SDDR B DQ15 BC47
- SDDR B DQ16 BC46
- SDDR B DQ17 BC44
- SDDR B DQ18 BC43
- SDDR B DQ19 BF43
- SDDR B DQ20 BE45
- SDDR B DQ21 BC41
- SDDR B DQ22 BF40
- SDDR B DQ23 BF41
- SDDR B DQ24 BG38
- SDDR B DQ25 BF38
- SDDR B DQ26 BH35
- SDDR B DQ27 BG35
- SDDR B DQ28 BH40
- SDDR B DQ29 BC39
- SDDR B DQ30 BC34
- SDDR B DQ31 BH34
- SDDR B DQ32 BH14
- SDDR B DQ33 BG12
- SDDR B DQ34 BH11
- SDDR B DQ35 BG8
- SDDR B DQ36 BH12
- SDDR B DQ37 BF11
- SDDR B DQ38 BF8
- SDDR B DQ39 BG7
- SDDR B DQ40 BC5
- SDDR B DQ41 BC6
- SDDR B DQ42 AY3
- SDDR B DQ43 AY1
- SDDR B DQ44 BF6
- SDDR B DQ45 BF5
- SDDR B DQ46 BA1
- SDDR B DQ47 BD3
- SDDR B DQ48 AV2
- SDDR B DQ49 AU3
- SDDR B DQ50 AR3
- SDDR B DQ51 AN2
- SDDR B DQ52 AY2
- SDDR B DQ53 AV1
- SDDR B DQ54 AP3
- SDDR B DQ55 AR1
- SDDR B DQ56 AL1
- SDDR B DQ57 AL2
- SDDR B DQ58 AJ1
- SDDR B DQ59 AH1
- SDDR B DQ60 AM2
- SDDR B DQ61 AM3
- SDDR B DQ62 AH3
- SDDR B DQ63 AJ3

U27E

GL40

DDR SYSTEM MEMORY B

- SB_DS_0
- SB_DS_1
- SB_DS_2
- SB_DS_3
- SB_DS_4
- SB_DS_5
- SB_DS_6
- SB_DS_7
- SB_DS_8
- SB_DS_9
- SB_DS_10
- SB_DS_11
- SB_DS_12
- SB_DS_13
- SB_DS_14
- SB_DS_15
- SB_DS_16
- SB_DS_17
- SB_DS_18
- SB_DS_19
- SB_DS_20
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- SB_DS_25
- SB_DS_26
- SB_DS_27
- SB_DS_28
- SB_DS_29
- SB_DS_30
- SB_DS_31
- SB_DS_32
- SB_DS_33
- SB_DS_34
- SB_DS_35
- SB_DS_36
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- SB_DS_41
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- SB_DS_63

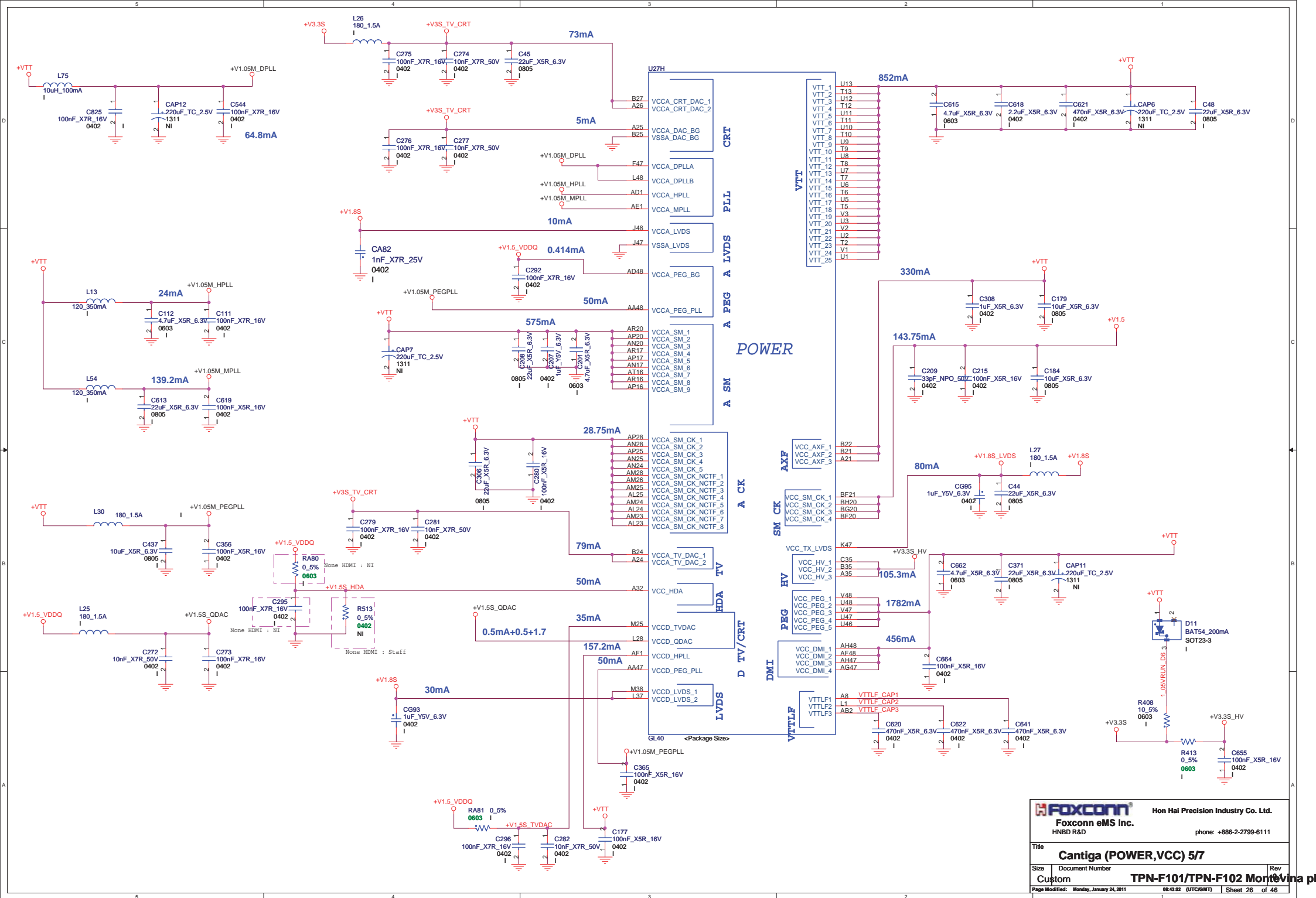
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- SA_WE#
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- SA_DM_2
- SA_DM_3
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- SA_DM_6
- SA_DM_7
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- SA_DQS_1
- SA_DQS_2
- SA_DQS_3
- SA_DQS_4
- SA_DQS_5
- SA_DQS_6
- SA_DQS_7
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- SA_MA_8
- SA_MA_9
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- SA_MA_11
- SA_MA_12
- SA_MA_13
- SA_MA_14

- BC16
- BB17
- BB33
- AU17
- BG16
- BF14
- AM47
- AY47
- BD40
- BF35
- BG11
- BA3
- AP1
- AK2
- AL47
- AV48
- BG41
- BG37
- BH9
- BB2
- AU1
- AN6
- AL46
- AV47
- BH41
- BH37
- BG9
- BC2
- AT2
- AN5
- AV17
- BA25
- BC25
- AU25
- AW25
- BB28
- AU28
- AW28
- AT33
- BD33
- BB16
- AW33
- AY33
- BH15
- AU33
- SDDR_B_BS0 35
- SDDR_B_BS1 35
- SDDR_B_BS2 35
- SDDR_B_RAS# 35
- SDDR_B_CAS# 35
- SDDR_B_WE# 35
- SDDR_B_DM[7..0] 35
- SDDR_B_DQS[7..0] 35
- SDDR_B_DQS#[7..0] 35
- SDDR_B_A[14..0] 35

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Size	Document Number	Rev
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Page Modified: Monday, January 24, 2011 09:05:39 (UTC/GMT)		Sheet 25 of 46

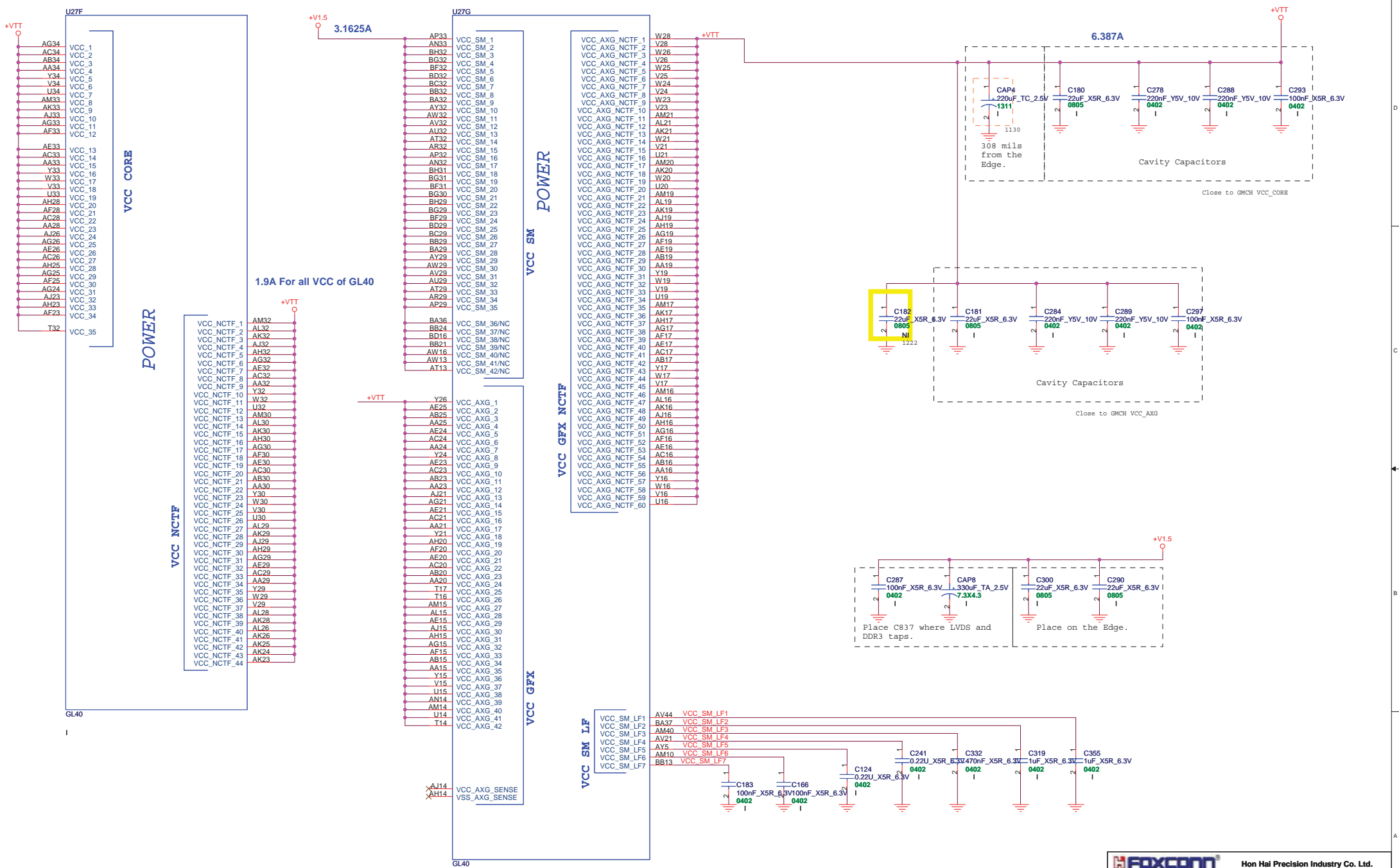


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Page Modified: Monday, January 24, 2011 08:43:32 (UTC/GMT) Sheet 26 of 46



U271		VSS	
AU48	VSS_1	VSS_100	AM36
AR48	VSS_2	VSS_101	F36
AL48	VSS_3	VSS_102	L36
BB47	VSS_4	VSS_103	AU21
AW47	VSS_5	VSS_104	J36
AN47	VSS_6	VSS_105	F36
AJ47	VSS_7	VSS_106	AF21
AF47	VSS_8	VSS_107	AH35
AD47	VSS_9	VSS_108	AA35
AB47	VSS_10	VSS_109	Y35
Y47	VSS_11	VSS_110	U35
T47	VSS_12	VSS_111	G21
N47	VSS_13	VSS_112	BF34
L47	VSS_14	VSS_113	AM34
G47	VSS_15	VSS_114	AF34
BD46	VSS_16	VSS_115	AE34
BA46	VSS_17	VSS_116	W34
AY46	VSS_18	VSS_117	B34
AV46	VSS_19	VSS_118	B34
AR46	VSS_20	VSS_119	K20
AM46	VSS_21	VSS_120	BC33
V46	VSS_22	VSS_121	K20
R46	VSS_23	VSS_122	BA33
P46	VSS_24	VSS_123	AV33
H46	VSS_25	VSS_124	AR33
F46	VSS_26	VSS_125	AL33
BF44	VSS_27	VSS_126	AH33
AH44	VSS_28	VSS_127	AB33
AD44	VSS_29	VSS_128	P33
AA44	VSS_30	VSS_129	L33
Y44	VSS_31	VSS_130	H33
U44	VSS_32	VSS_131	N32
T44	VSS_33	VSS_132	K32
M44	VSS_34	VSS_133	F32
F44	VSS_35	VSS_134	C32
BC43	VSS_36	VSS_135	A31
AV43	VSS_37	VSS_136	AN29
AU43	VSS_38	VSS_137	T29
AM43	VSS_39	VSS_138	N29
J43	VSS_40	VSS_139	K29
C43	VSS_41	VSS_140	H29
BG42	VSS_42	VSS_141	F29
AY42	VSS_43	VSS_142	E16
AT42	VSS_44	VSS_143	BG28
AN42	VSS_45	VSS_144	BD28
AJ42	VSS_46	VSS_145	BA28
AE42	VSS_47	VSS_146	AV28
N42	VSS_48	VSS_147	AT28
L42	VSS_49	VSS_148	AR28
RD41	VSS_50	VSS_149	AJ28
AU41	VSS_51	VSS_150	BG13
AM41	VSS_52	VSS_151	AE28
AH41	VSS_53	VSS_152	AB28
AD41	VSS_54	VSS_153	Y28
AA41	VSS_55	VSS_154	P28
Y41	VSS_56	VSS_155	K28
U41	VSS_57	VSS_156	H28
T41	VSS_58	VSS_157	F28
M41	VSS_59	VSS_158	C28
G41	VSS_60	VSS_159	BF26
B41	VSS_61	VSS_160	AH26
RG40	VSS_62	VSS_161	AF26
BB40	VSS_63	VSS_162	AB26
AV40	VSS_64	VSS_163	AA26
AN40	VSS_65	VSS_164	C26
H40	VSS_66	VSS_165	B26
E40	VSS_67	VSS_166	BH25
AT39	VSS_68	VSS_167	BD25
AM39	VSS_69	VSS_168	BB25
AJ39	VSS_70	VSS_169	AV25
AE39	VSS_71	VSS_170	AR25
N39	VSS_72	VSS_171	AJ25
L39	VSS_73	VSS_172	AC25
B39	VSS_74	VSS_173	Y25
BH38	VSS_75	VSS_174	N25
BC38	VSS_76	VSS_175	L25
BA38	VSS_77	VSS_176	J25
AU38	VSS_78	VSS_177	G11
AH38	VSS_79	VSS_178	E25
AD38	VSS_80	VSS_179	BF24
AA38	VSS_81	VSS_180	AD12
Y38	VSS_82	VSS_181	AY24
U38	VSS_83	VSS_182	AT24
T38	VSS_84	VSS_183	AJ24
J38	VSS_85	VSS_184	AH24
F38	VSS_86	VSS_185	AF24
C38	VSS_87	VSS_186	AB24
BF37	VSS_88	VSS_187	R24
BB37	VSS_89	VSS_188	L24
AW37	VSS_90	VSS_189	K24
AT37	VSS_91	VSS_190	J24
AN37	VSS_92	VSS_191	G24
AJ37	VSS_93	VSS_192	F24
H37	VSS_94	VSS_193	E24
C37	VSS_95	VSS_194	BH23
PG36	VSS_96	VSS_195	AV23
BD36	VSS_97	VSS_196	Y23
AK15	VSS_98	VSS_197	B23
AU36	VSS_99	VSS_198	A23
		VSS_199	AJ6

GL40

U27J		VSS	
BG21	VSS_199	VSS_297	AH8
L12	VSS_200	VSS_298	Y8
AW21	VSS_201	VSS_299	L8
F36	VSS_202	VSS_300	E8
AP21	VSS_203	VSS_301	B8
AN21	VSS_204	VSS_302	AY7
AH21	VSS_205	VSS_303	AU7
B36	VSS_206	VSS_304	AN7
AB21	VSS_207	VSS_305	AJ7
R21	VSS_208	VSS_306	AE7
M21	VSS_209	VSS_307	AA7
J21	VSS_210	VSS_308	N7
T36	VSS_211	VSS_309	U7
BC20	VSS_212	VSS_310	BG6
BA20	VSS_213	VSS_311	BD6
AW20	VSS_214	VSS_312	AV6
AJ20	VSS_215	VSS_313	AT6
AG20	VSS_216	VSS_314	AM6
B34	VSS_217	VSS_315	M6
Y20	VSS_218	VSS_316	C6
A34	VSS_219	VSS_317	BA5
N20	VSS_220	VSS_318	AH5
K20	VSS_221	VSS_319	AD5
F20	VSS_222	VSS_320	Y5
C20	VSS_223	VSS_321	L5
A20	VSS_224	VSS_322	J5
AR33	VSS_225	VSS_323	H5
A18	VSS_226	VSS_324	F5
BG17	VSS_227	VSS_325	BE4
BC17	VSS_228		
AW17	VSS_229	VSS_327	BC3
AT17	VSS_230	VSS_328	AV3
R17	VSS_231	VSS_329	AL3
M17	VSS_232	VSS_330	R3
H17	VSS_233	VSS_331	P3
C17	VSS_235	VSS_332	F3
		VSS_333	BA2
BA16	VSS_237	VSS_334	AW2
		VSS_335	U2
AL16	VSS_238	VSS_336	AR2
AN16	VSS_239	VSS_337	AP2
N16	VSS_240	VSS_338	AJ2
H29	VSS_241	VSS_339	AH2
K16	VSS_242	VSS_340	AE2
G16	VSS_243	VSS_341	AD2
E16	VSS_244	VSS_342	AC2
BG15	VSS_245	VSS_343	Y2
AC15	VSS_246	VSS_344	M2
W15	VSS_247	VSS_345	K2
AV28	VSS_248	VSS_346	AM1
BG14	VSS_249	VSS_347	AA1
AA14	VSS_250	VSS_348	P1
C14	VSS_251	VSS_349	H1
AG28	VSS_252	VSS_350	
BC13	VSS_255	VSS_351	U24
BA13	VSS_258	VSS_352	U28
		VSS_353	U25
AN13	VSS_259	VSS_354	U29
K28	VSS_260		
H28	VSS_261	VSS_NCTF_1	AF32
F28	VSS_262	VSS_NCTF_2	AB32
C28	VSS_263	VSS_NCTF_3	V32
BF26	VSS_264	VSS_NCTF_4	AJ30
G13	VSS_265	VSS_NCTF_5	AM29
E13	VSS_266	VSS_NCTF_6	AF29
BF12	VSS_267	VSS_NCTF_7	AB29
AV12	VSS_268	VSS_NCTF_8	U26
C26	VSS_269	VSS_NCTF_9	U23
AM12	VSS_270	VSS_NCTF_10	AL20
AA12	VSS_271	VSS_NCTF_11	V20
J12	VSS_272	VSS_NCTF_12	AC19
BB25	VSS_273	VSS_NCTF_13	AL17
BD11	VSS_275	VSS_NCTF_14	AJ17
BB11	VSS_276	VSS_NCTF_15	AA17
AV25	VSS_277	VSS_NCTF_16	U17
AR25	VSS_278		
AJ25	VSS_279	VSS_SCB_1	BH48
AC25	VSS_280	VSS_SCB_2	BH1
Y25	VSS_281	VSS_SCB_3	A48
N25	VSS_282	VSS_SCB_4	C1
L25	VSS_283	VSS_SCB_5	A3
J25	VSS_284		
G11	VSS_285	NC_26	E1 X
E25	VSS_286	NC_27	D2 X
BF24	VSS_287	NC_28	C3 X
AD12	VSS_288	NC_29	B4 X
AY24	VSS_289	NC_30	A5 X
AT24	VSS_290	NC_31	A6 X
AJ24	VSS_291	NC_32	A4 X
AH24	VSS_292	NC_33	A4 X
AF24	VSS_293	NC_34	B4 X
AB24	VSS_294	NC_35	C4 X
R24	VSS_295	NC_36	D4 X
L24	VSS_296	NC_37	A4 X
K24		NC_38	A4 X
J24		NC_39	F48 X
G24		NC_40	E48 X
F24		NC_41	C48 X
E24		NC_42	B48 X
BH23			
AV23			
Y23			
B23			
A23			
AJ6			

GL40

VSS

VSS_NCTF

VSS_SCB

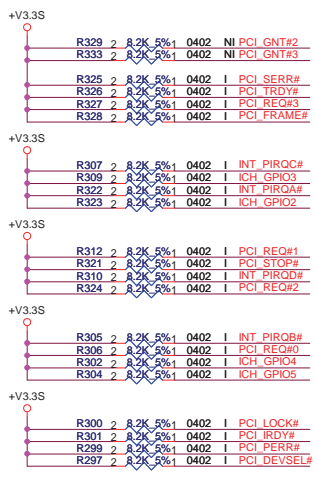
NC

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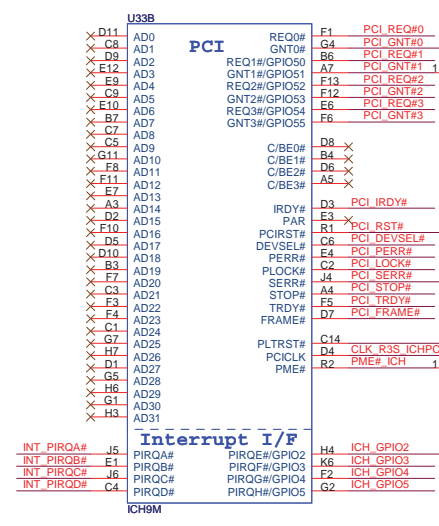
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Size: Document Number Rev
 Custom **TPN-F101/TPN-F102 Montevina pl**

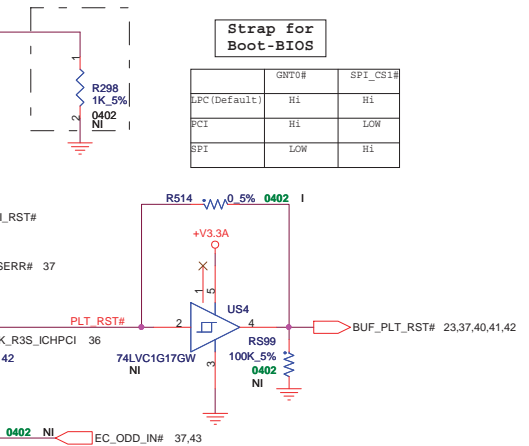
Page Modified: Monday, January 24, 2011 08:43:33 (UTC/GMT) Sheet 28 of 46



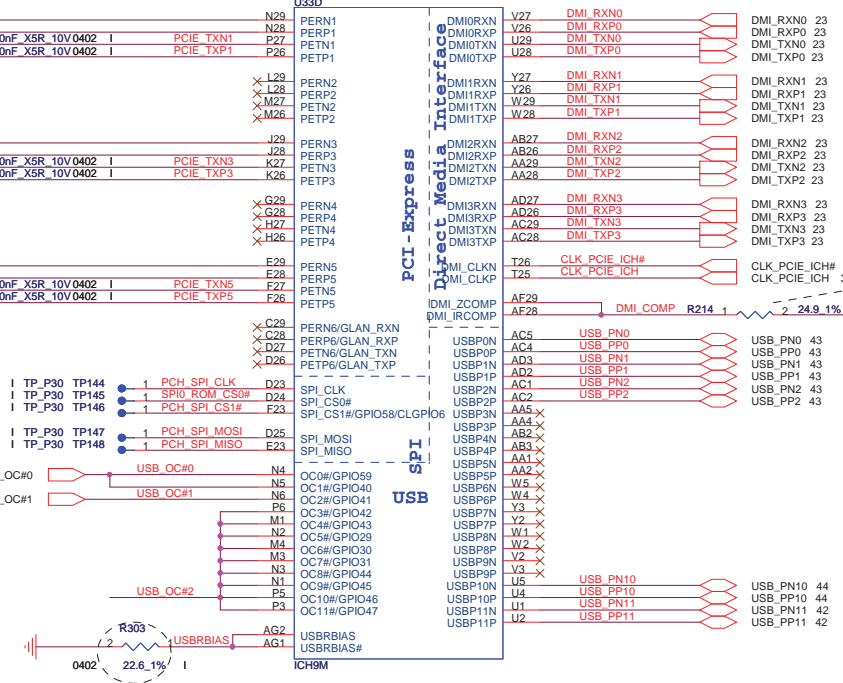
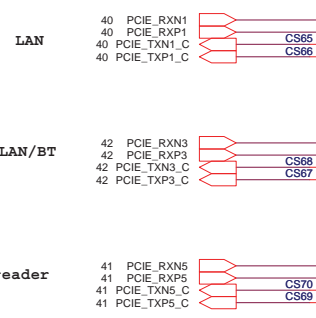
PCI Pullups



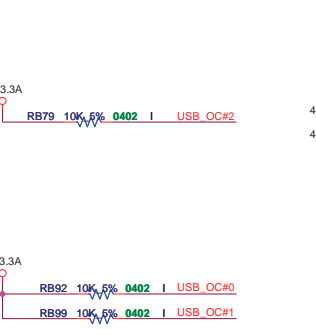
For Boot BIOS Selection.



GPIO#	INT#	SPI_CS1#
LPC (Default)	HI	HI
PCI	HI	LOW
SPI	LOW	HI

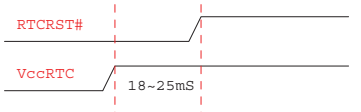


Place within 500 mils of ICH



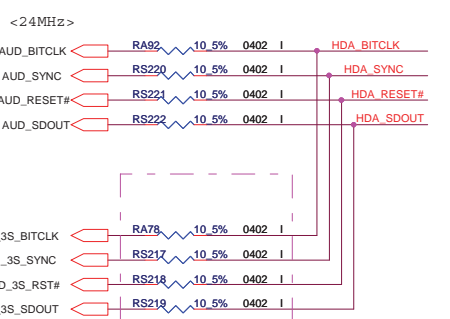
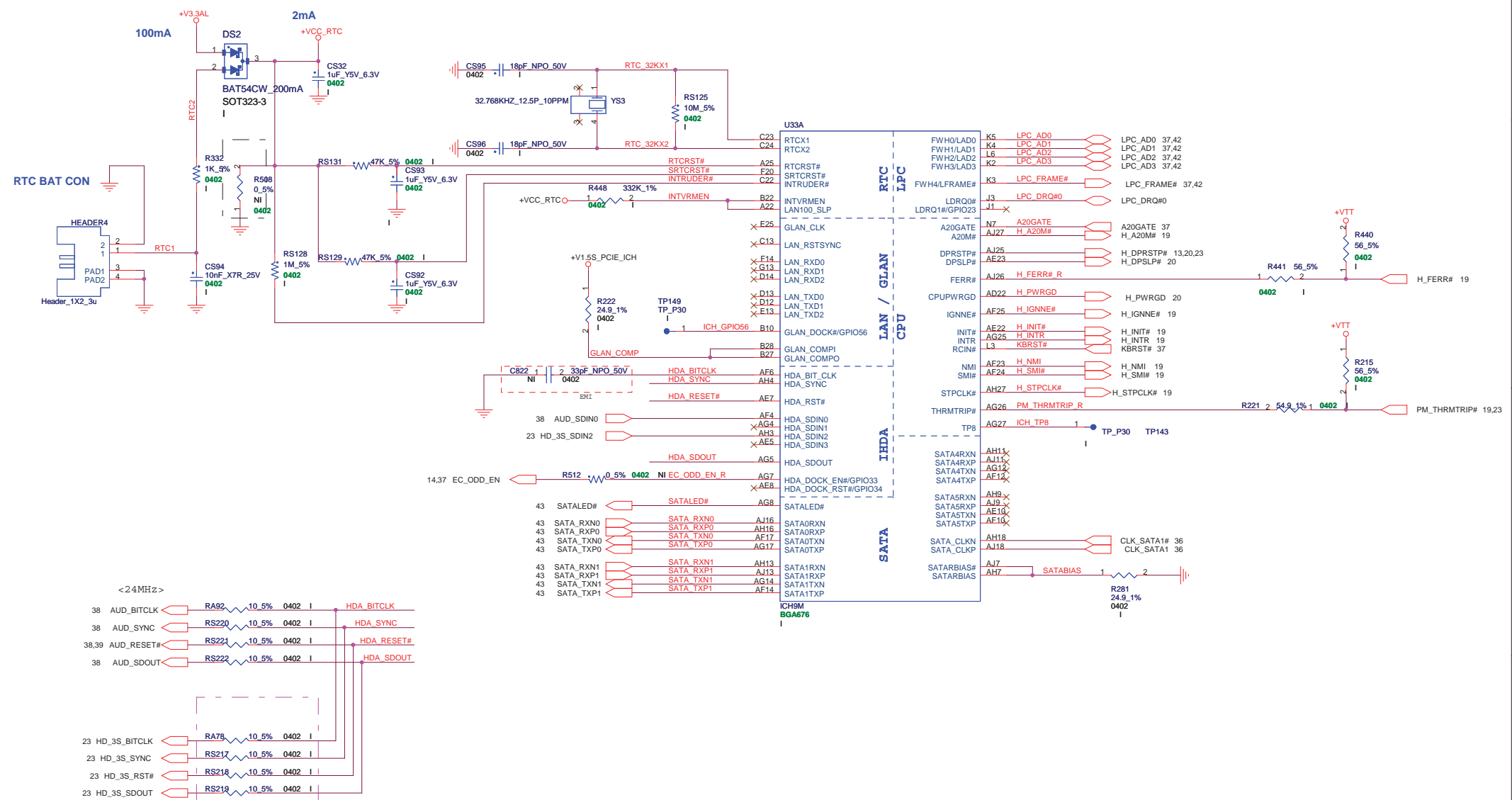
Place within 500 mils of ICH and don't routing next to high speed signals

USB PORT	Function	OC pin
PORT-0	Ext. USB 0	
PORT-1	Ext. USB 1	
PORT-2	Ext. USB 2	
PORT-3		
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8		
PORT-9		
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12		
PORT-13		



Internal VRM enabled for VccSui1_05, VccSui1_5, VccCl1_5, VccLAI1_05 and VccCl1_05

INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)
----------	---



None HDMI : don't staff

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Title: **ICH9-M(LPC,IDE,SATA) 2/5**

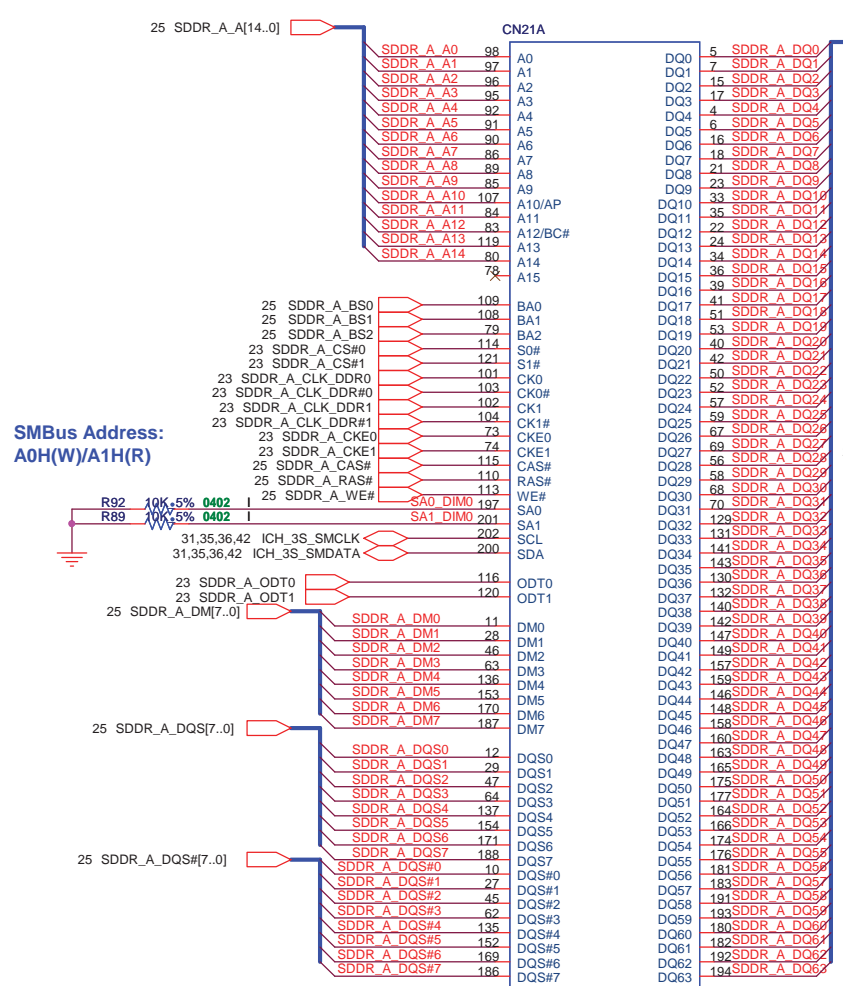
Size: Document Number
 Custom **TPN-F101/TPN-F102 Montevina pl** Rev

Page Modified: Monday, January 24, 2011 09:05:39 (UTC/GMT) Sheet 30 of 46

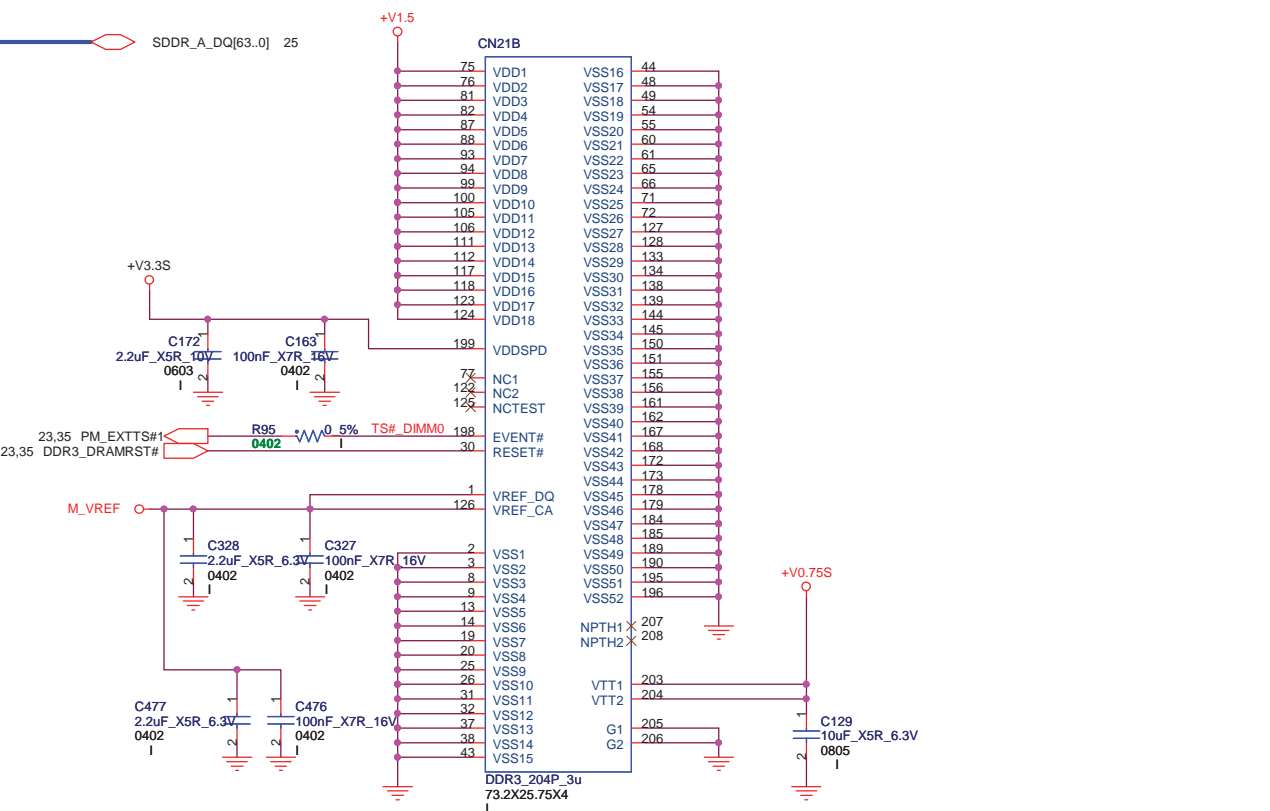
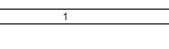
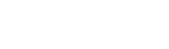
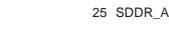
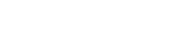
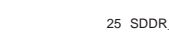
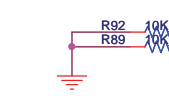
U33E		H5	
AA26	VSS[001]	VSS[107]	J23
AA27	VSS[002]	VSS[108]	J26
AA3	VSS[003]	VSS[109]	J27
AA6	VSS[004]	VSS[110]	AC22
AB1	VSS[005]	VSS[111]	K28
AA23	VSS[006]	VSS[112]	K29
AB28	VSS[007]	VSS[113]	L13
AB29	VSS[008]	VSS[114]	L15
AB4	VSS[009]	VSS[115]	L2
AB5	VSS[010]	VSS[116]	L26
AC17	VSS[011]	VSS[117]	L27
AC26	VSS[012]	VSS[118]	L5
AC27	VSS[013]	VSS[119]	L7
AC3	VSS[014]	VSS[120]	M12
AD1	VSS[015]	VSS[121]	M13
AD10	VSS[016]	VSS[122]	M14
AD12	VSS[017]	VSS[123]	M15
AD13	VSS[018]	VSS[124]	M16
AD14	VSS[019]	VSS[125]	M17
AD17	VSS[020]	VSS[126]	M23
AD18	VSS[021]	VSS[127]	M28
AD21	VSS[022]	VSS[128]	M29
AD28	VSS[023]	VSS[129]	N11
AD29	VSS[024]	VSS[130]	N12
AD4	VSS[025]	VSS[131]	N13
AD6	VSS[026]	VSS[132]	N14
AD6	VSS[027]	VSS[133]	N15
AD7	VSS[028]	VSS[134]	N16
AD9	VSS[029]	VSS[135]	N17
AE12	VSS[030]	VSS[136]	N18
AE13	VSS[031]	VSS[137]	N26
AE14	VSS[032]	VSS[138]	N27
AE16	VSS[033]	VSS[139]	P12
AE17	VSS[034]	VSS[140]	P13
AE2	VSS[035]	VSS[141]	P14
AE20	VSS[036]	VSS[142]	P15
AE24	VSS[037]	VSS[143]	P16
AE3	VSS[038]	VSS[144]	P17
AE4	VSS[039]	VSS[145]	P2
AE6	VSS[040]	VSS[146]	P23
AE9	VSS[041]	VSS[147]	P28
AF13	VSS[042]	VSS[148]	P29
AF16	VSS[043]	VSS[149]	P4
AF18	VSS[044]	VSS[150]	P7
AF22	VSS[045]	VSS[151]	R11
AH26	VSS[046]	VSS[152]	R12
AF27	VSS[047]	VSS[153]	R13
AF5	VSS[048]	VSS[154]	R14
AF7	VSS[049]	VSS[155]	R15
AF9	VSS[050]	VSS[156]	R16
AG13	VSS[051]	VSS[157]	R17
AG16	VSS[052]	VSS[158]	R18
AG18	VSS[053]	VSS[159]	R28
AG19	VSS[054]	VSS[160]	T12
AG20	VSS[055]	VSS[161]	T13
AG23	VSS[056]	VSS[162]	T14
AG3	VSS[057]	VSS[163]	T15
AG6	VSS[058]	VSS[164]	T16
AG9	VSS[059]	VSS[165]	T17
AH14	VSS[060]	VSS[166]	T23
AH17	VSS[061]	VSS[167]	B26
AH19	VSS[062]	VSS[168]	U12
AH2	VSS[063]	VSS[169]	U13
AH22	VSS[064]	VSS[170]	U14
AH25	VSS[065]	VSS[171]	U15
AH28	VSS[066]	VSS[172]	U16
AH5	VSS[067]	VSS[173]	U17
AH5	VSS[068]	VSS[174]	AD23
AH8	VSS[069]	VSS[175]	U26
AJ12	VSS[070]	VSS[176]	U27
AJ14	VSS[071]	VSS[177]	U3
AJ17	VSS[072]	VSS[178]	V1
AJ8	VSS[073]	VSS[179]	V13
B11	VSS[074]	VSS[180]	V15
B14	VSS[075]	VSS[181]	V23
B17	VSS[076]	VSS[182]	V28
B2	VSS[077]	VSS[183]	V29
B20	VSS[078]	VSS[184]	V4
B5	VSS[079]	VSS[185]	V5
B8	VSS[080]	VSS[186]	W26
B8	VSS[081]	VSS[187]	W27
C26	VSS[082]	VSS[188]	W3
C27	VSS[083]	VSS[189]	Y1
E11	VSS[084]	VSS[190]	Y28
E14	VSS[085]	VSS[191]	Y29
E18	VSS[086]	VSS[192]	Y4
E2	VSS[087]	VSS[193]	Y5
E21	VSS[088]	VSS[194]	AG28
E24	VSS[089]	VSS[195]	AH6
E5	VSS[090]	VSS[196]	AF2
E8	VSS[091]	VSS[197]	B25
F16	VSS[092]	VSS[198]	A1
F28	VSS[093]		A2
F29	VSS[094]	VSS_NCTF[01]	A28
G12	VSS[095]	VSS_NCTF[02]	A29
G14	VSS[096]	VSS_NCTF[03]	AH1
G18	VSS[097]	VSS_NCTF[04]	AH29
G21	VSS[098]	VSS_NCTF[05]	AJ1
G24	VSS[099]	VSS_NCTF[06]	AJ2
G26	VSS[100]	VSS_NCTF[07]	AJ28
G27	VSS[101]	VSS_NCTF[08]	AJ29
G8	VSS[102]	VSS_NCTF[09]	B1
H2	VSS[103]	VSS_NCTF[10]	B29
H23	VSS[104]	VSS_NCTF[11]	
H28	VSS[105]	VSS_NCTF[12]	
H29	VSS[106]		

ICH9M

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Title: ICH9-M (GND) 5/5			
Size	Document Number	Rev	
Custom	TPN-F101/TPN-F102	Montevina pl	
Page Modified: Monday, January 24, 2011 08:43:32 (UTC/GMT) Sheet 33 of 46			

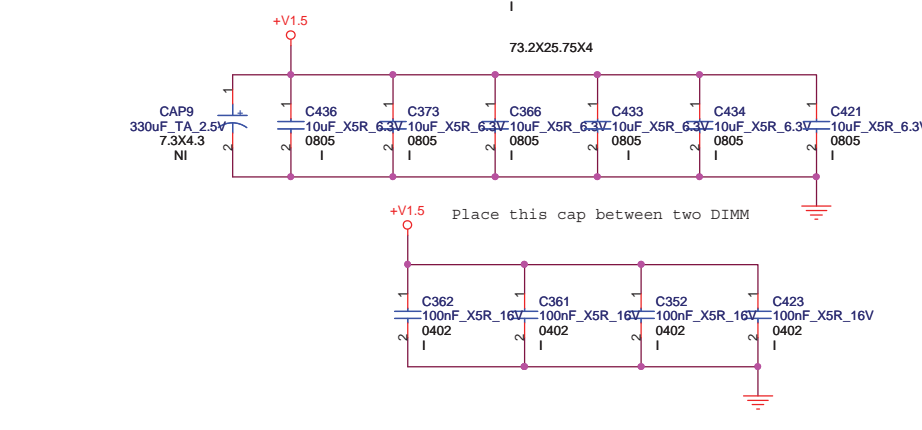


SMBus Address:
A0H(W)/A1H(R)



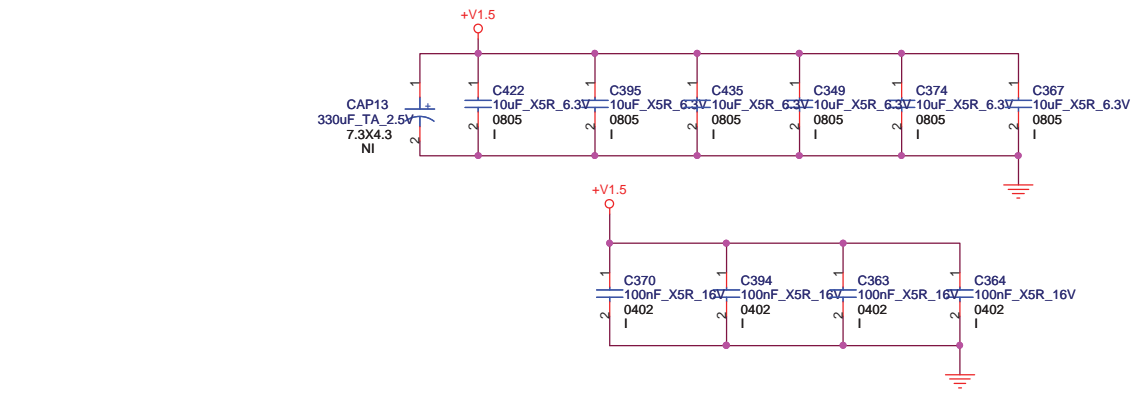
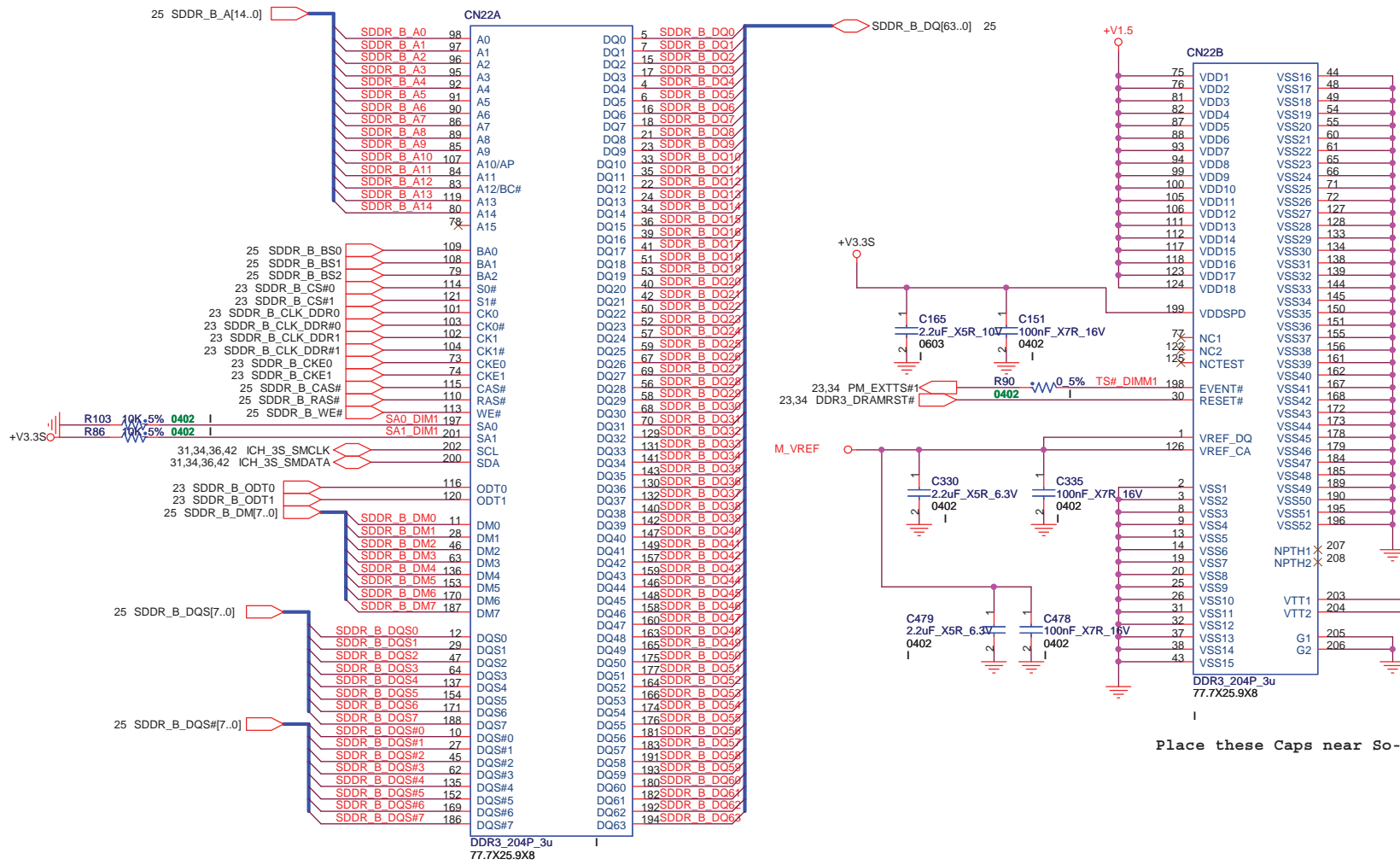
Place these Caps near So-DIMM0

Place this cap between two DIMM



Place this cap between two DIMM

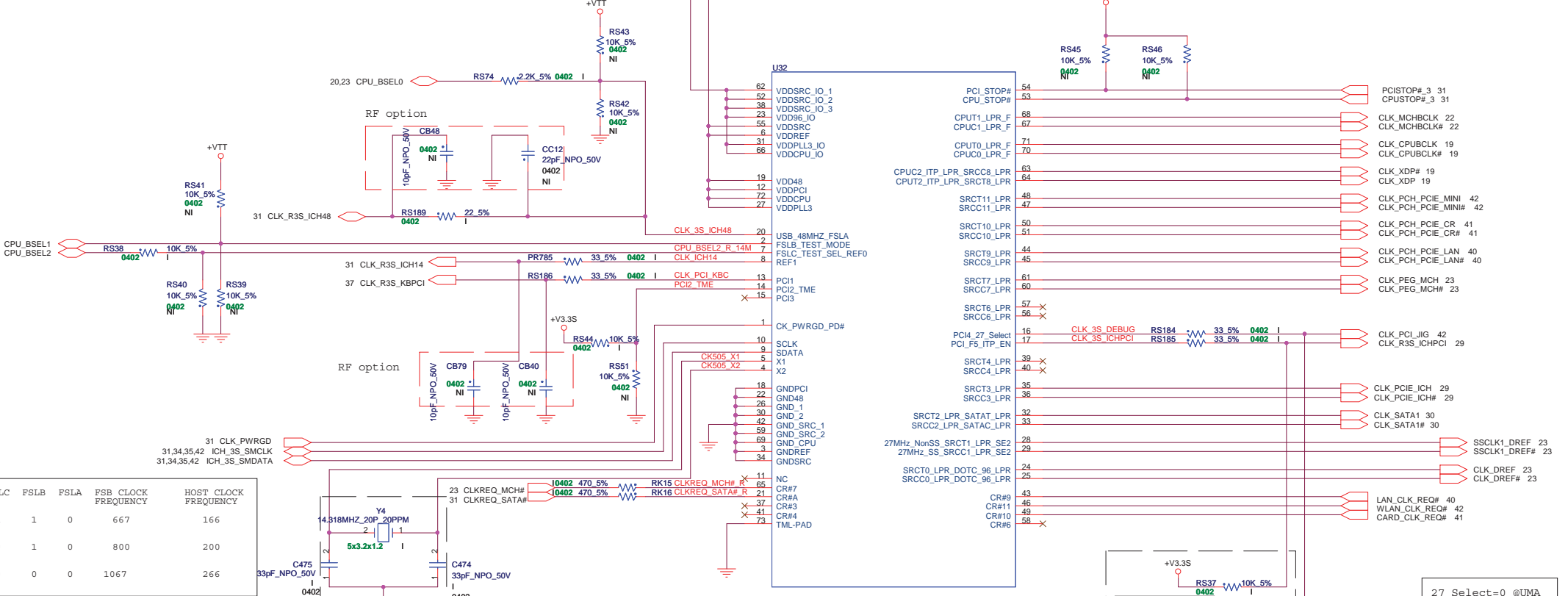
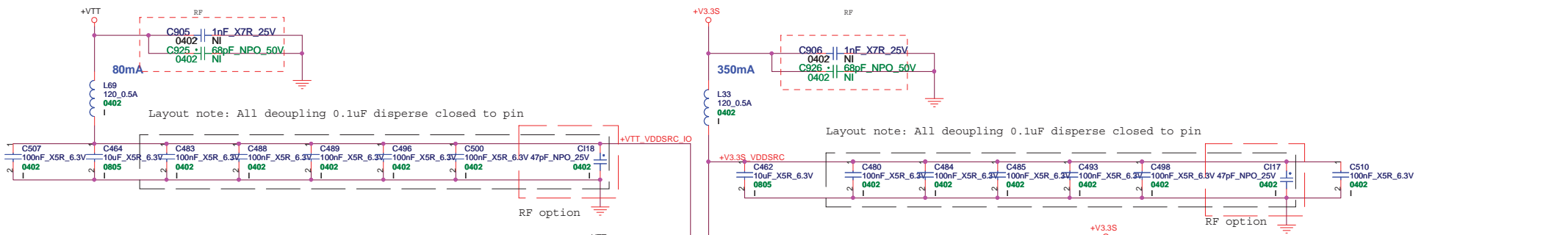
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Size	Document Number			Rev
Custom		TPN-F101/TPN-F102 Montevina		Rev
Page Modified: Monday, January 24, 2011		09:05:38 (UTC/GMT)		Sheet 34 of 46



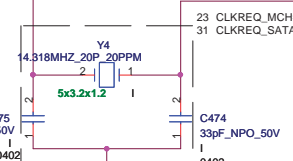
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Title: **DDR3 SO-DIMM_1**

Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina	
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)		Sheet 35 of 46



FSLC	FSLB	FSLA	FSB	CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	667	166
0	1	0	800	800	200
0	0	0	1067	1067	266

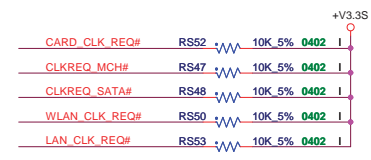


Please place close to CLKGEN within 500mils

*CLKREQ# pin controls SRC Table.

CR#_A	Byte5:bit7=0, disable CR#_A; 1 enable CR#_A	CR#_3	Byte5:bit5=0 (PWD), disable CR#3; 1, enable CR#_3
	Byte5:bit6=0 (PWD)		Byte5:bit6=1
	SRC0		SRC2
	SRC4		SRC6

CR#_7	Byte5:bit2=0 (PWD), disable CR#7; 1, enable CR#7
SRC7	
CR#_9	Byte5:bit1=0 (PWD), disable CR#9; 1, enable CR#9
SRC9	
CR#_10	Byte5:bit0=0 (PWD), disable CR#10; 1, enable CR#10
SRC10	
CR#_11	Byte6:bit7=0 (PWD), disable CR#11; 1, enable CR#11
SRC11	



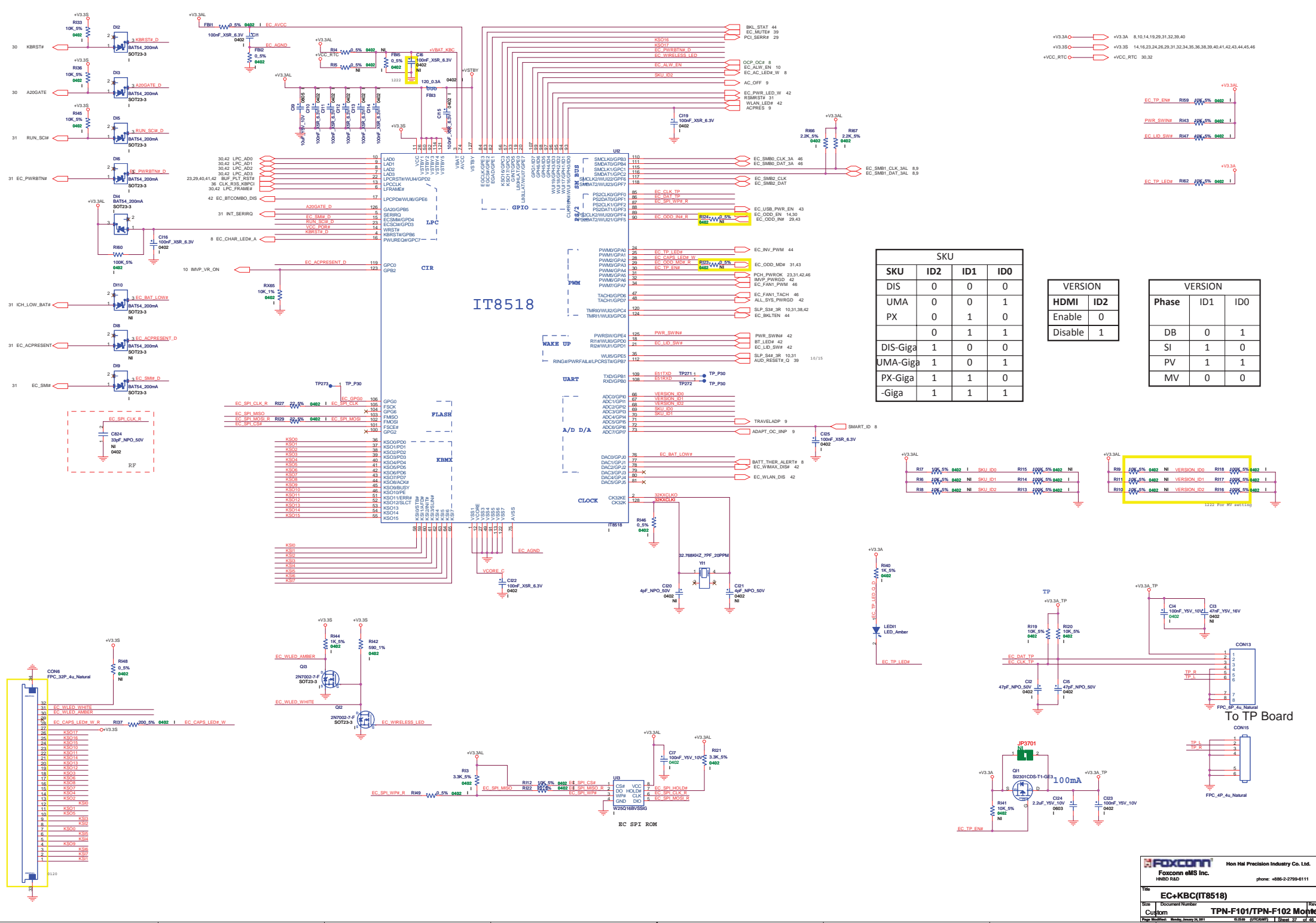
27_Select=0 @UMA
LCD_SST 100MHz
27_Select=1 @DIS
27MHz non-spread clock

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Title: **CLOCK GEN**

Size: Document Number: **TPN-F101/TPN-F102** Rev: **Montevina p**

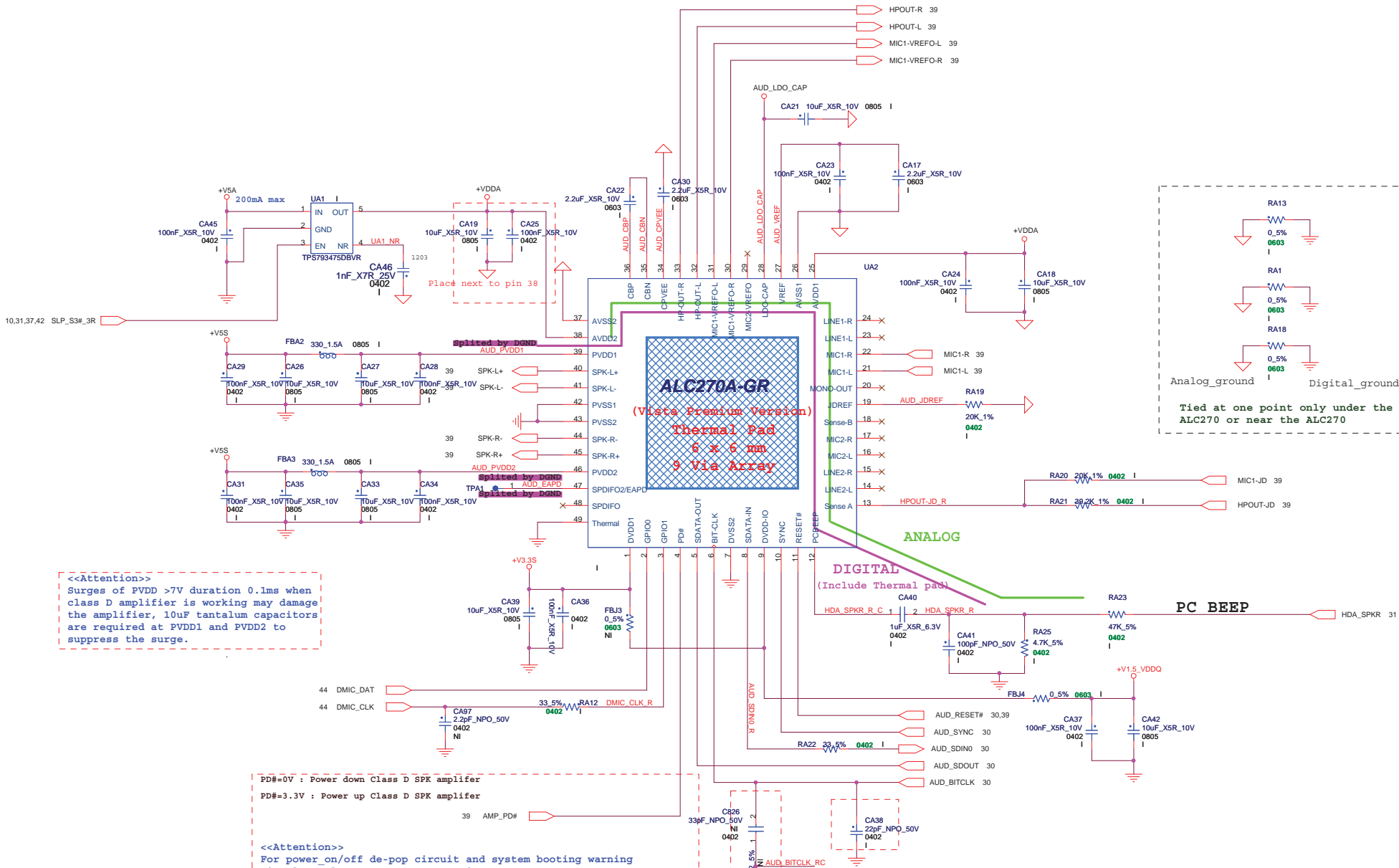
Page Modified: Monday, January 24, 2011 09:05:39 (UTC/GMT) Sheet 36 of 46



SKU			
SKU	ID2	ID1	ID0
DIS	0	0	0
UMA	0	0	1
PX	0	1	0
	0	1	1
DIS-Giga	1	0	0
UMA-Giga	1	0	1
PX-Giga	1	1	0
-Giga	1	1	1

VERSION		
HDMI	ID2	
Enable	0	
Disable	1	

VERSION		
Phase	ID1	ID0
DB	0	1
SI	1	0
PV	1	1
MV	0	0

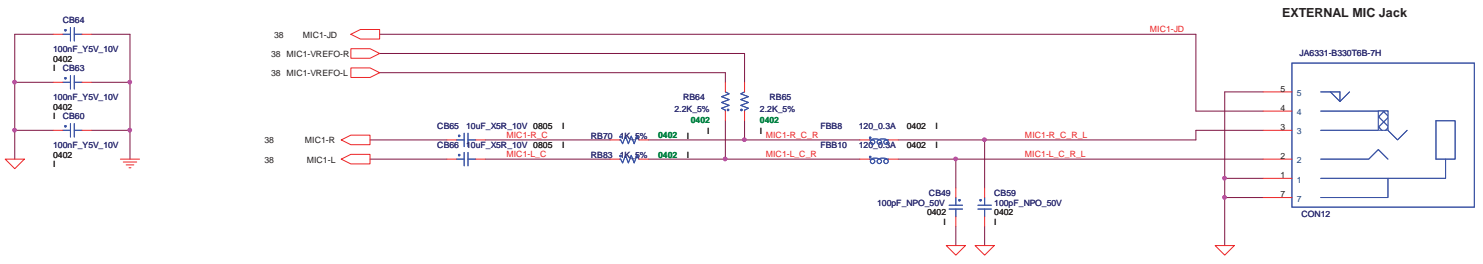
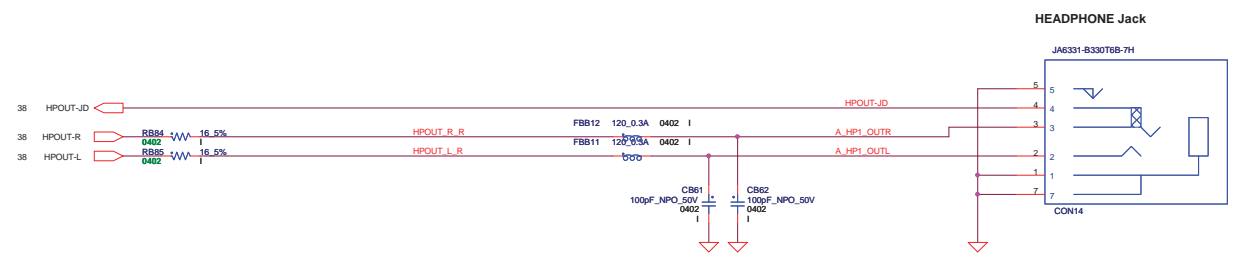
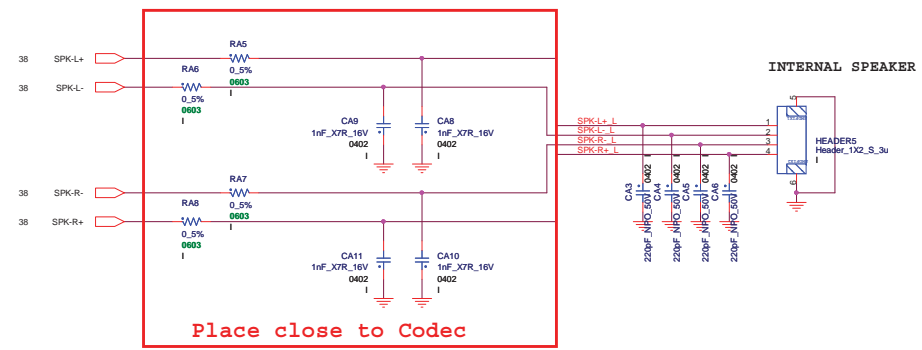
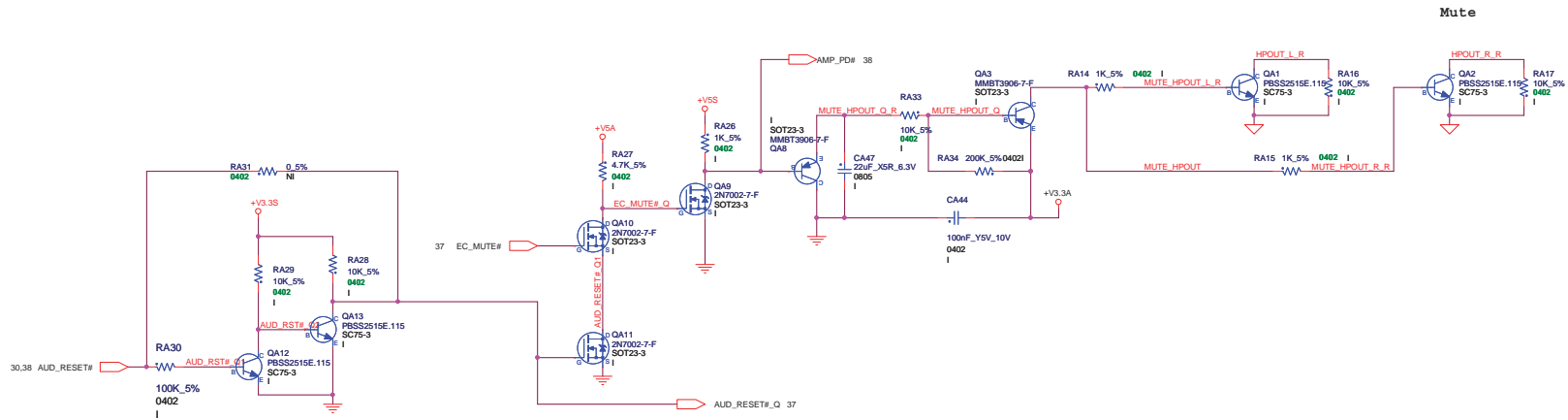


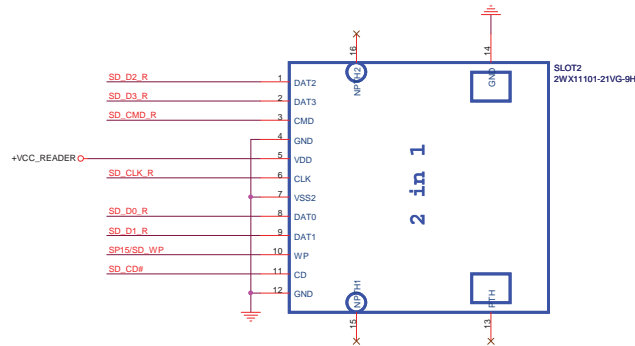
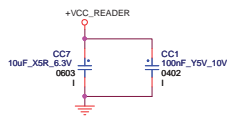
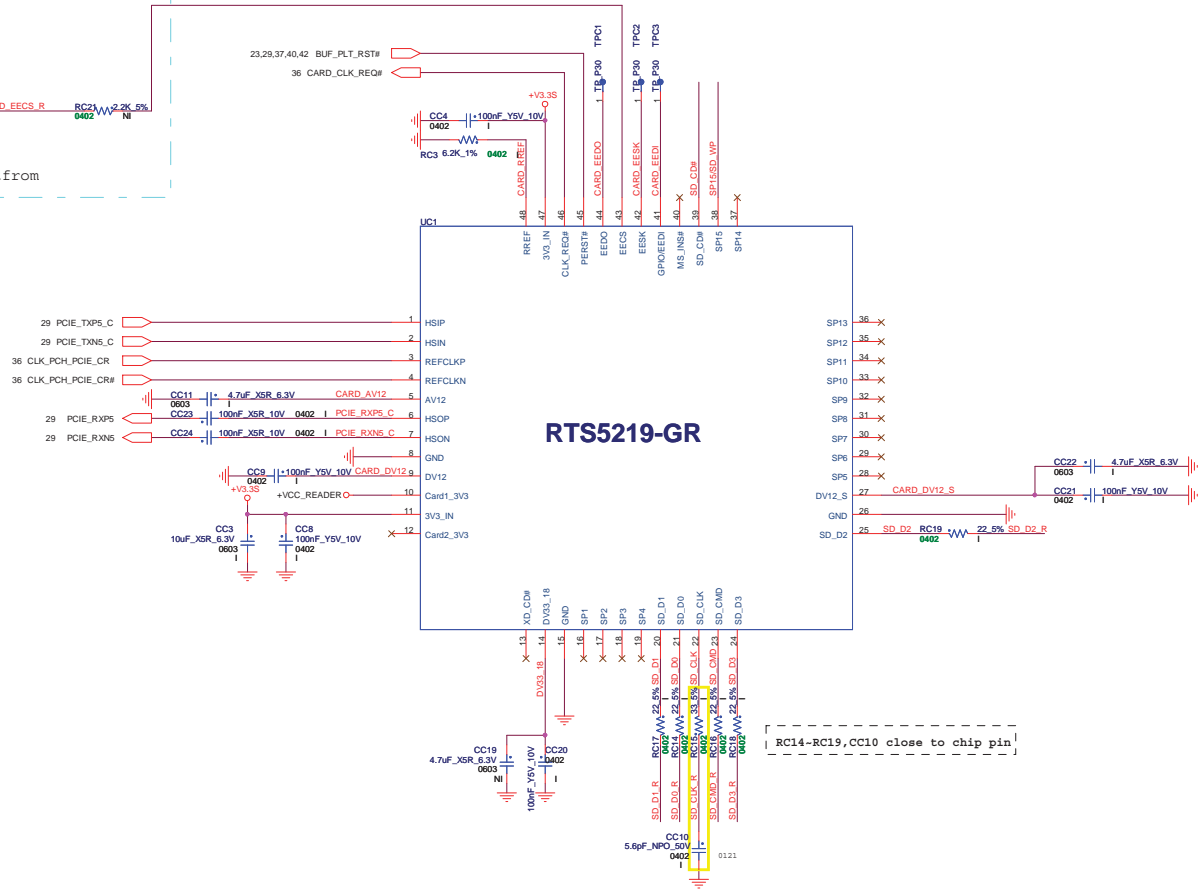
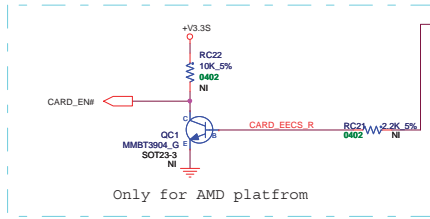
<<Attention>>
 Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

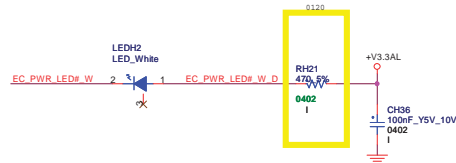
PD#=0V : Power down Class D SPK amplifier
 PD#=3.3V : Power up Class D SPK amplifier

39 AMP_PD#

<<Attention>>
 For power on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
 1. If you want the system make warning signal after power on , please let EC MUTE# High first.
 2. When you want to exit your Bios Programming Code, please let the EC_MUTE# Low. (The programming is different from before .)

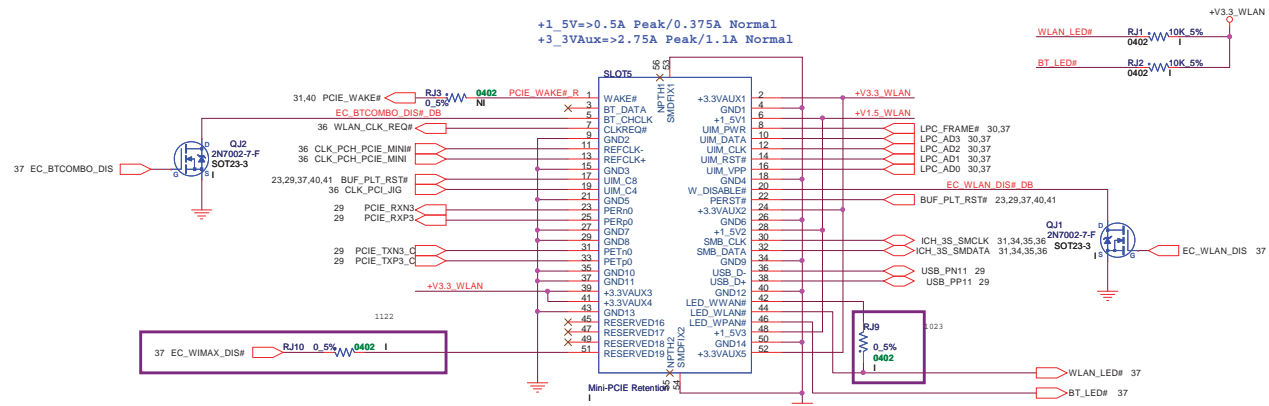
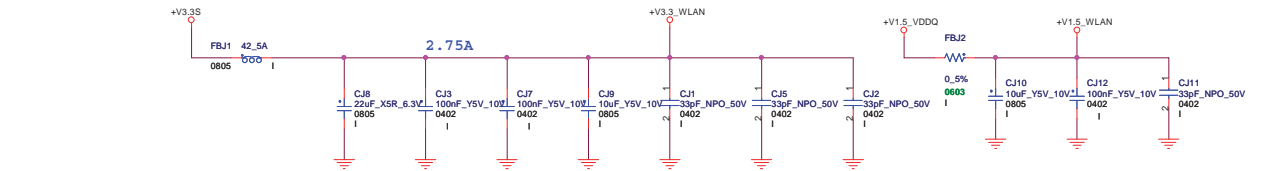
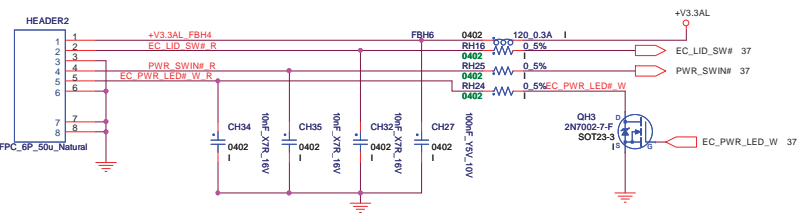




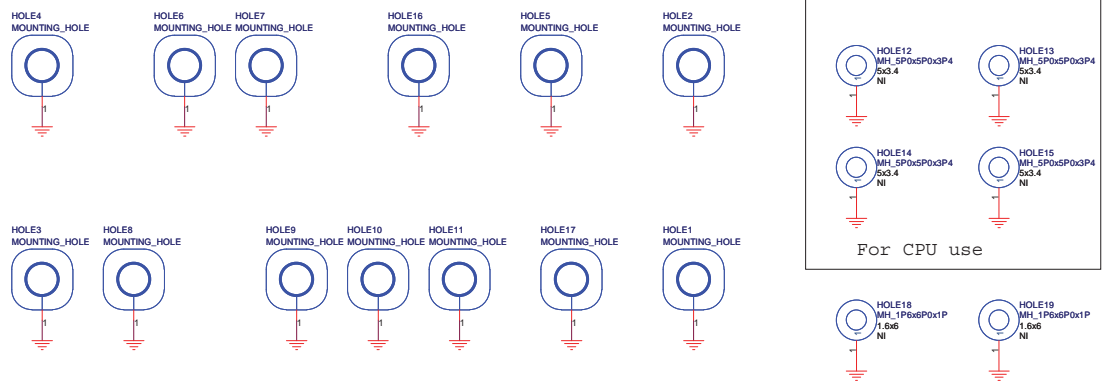


PWR LED

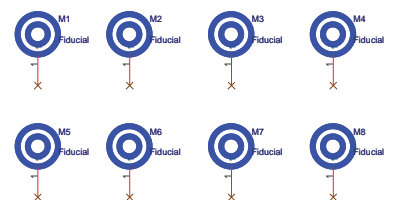
PWR Board CONN.



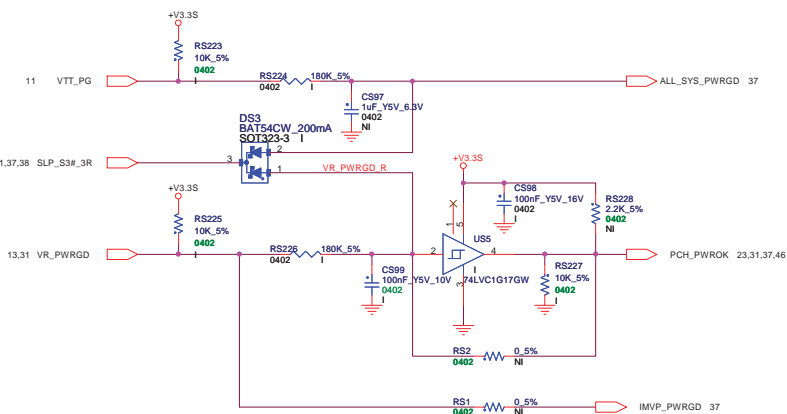
Half Mini Card for WLAN



Mounting HOLE



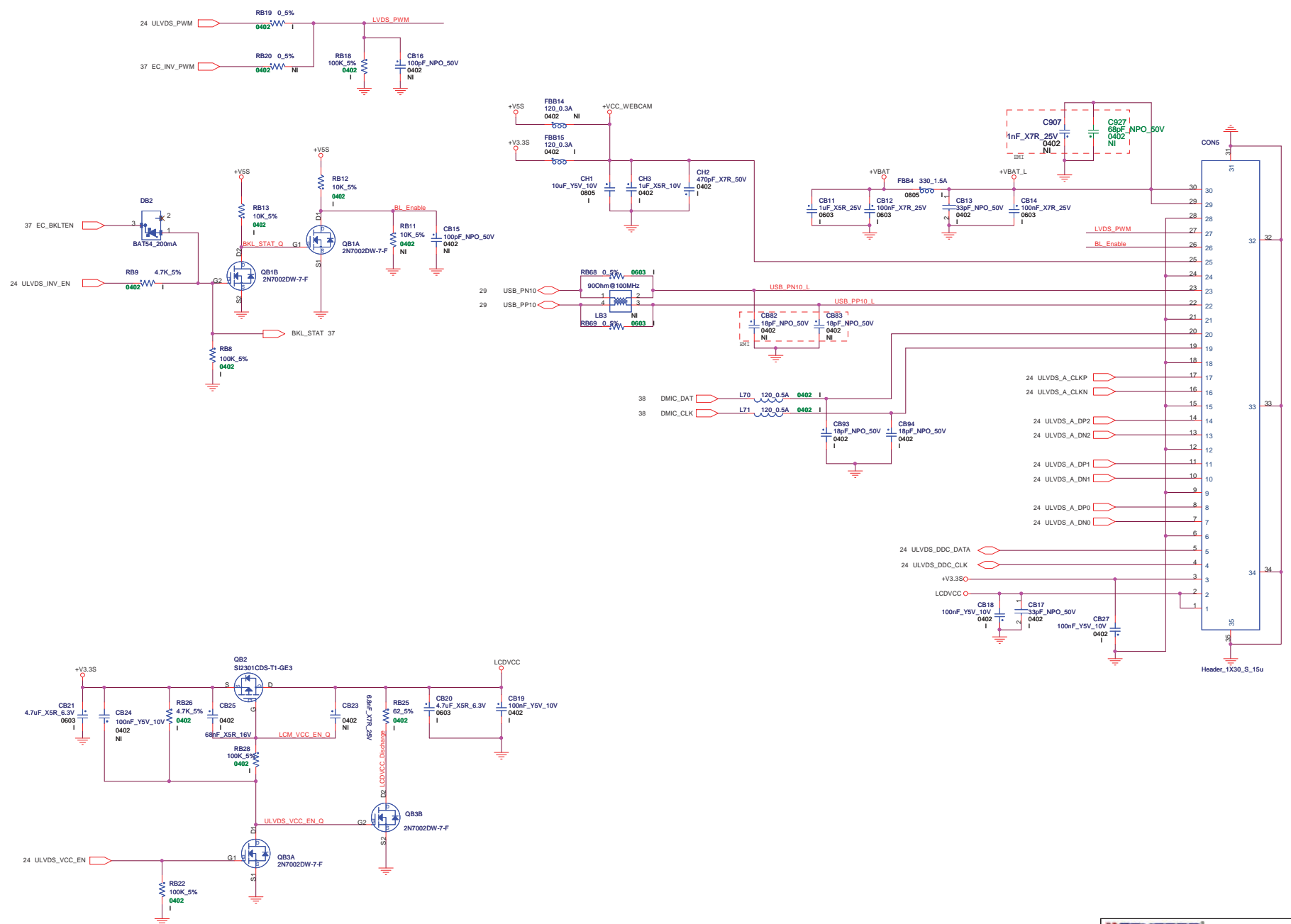
Fiducial Mark



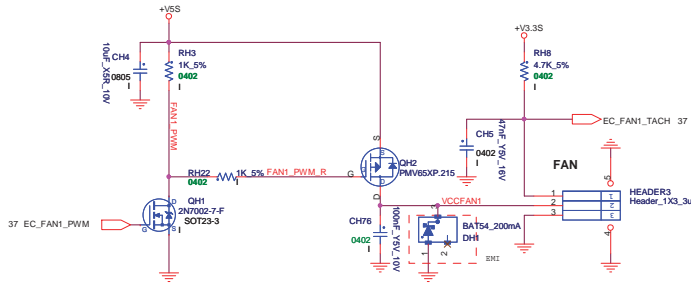
SEQUENCE CIRCUIT

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 H98D-R&D fax: (261) 868-1515

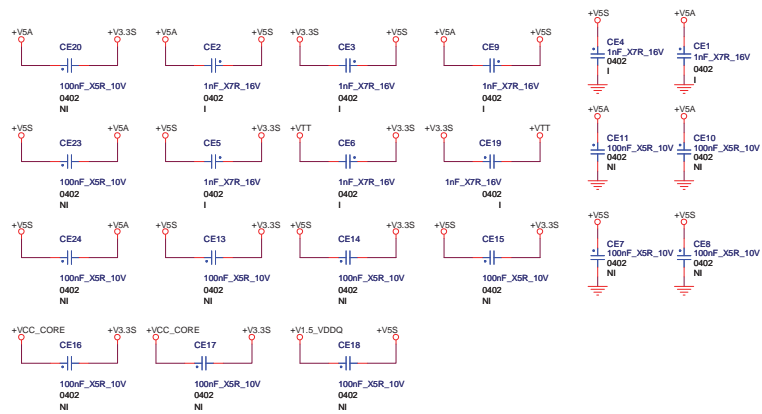
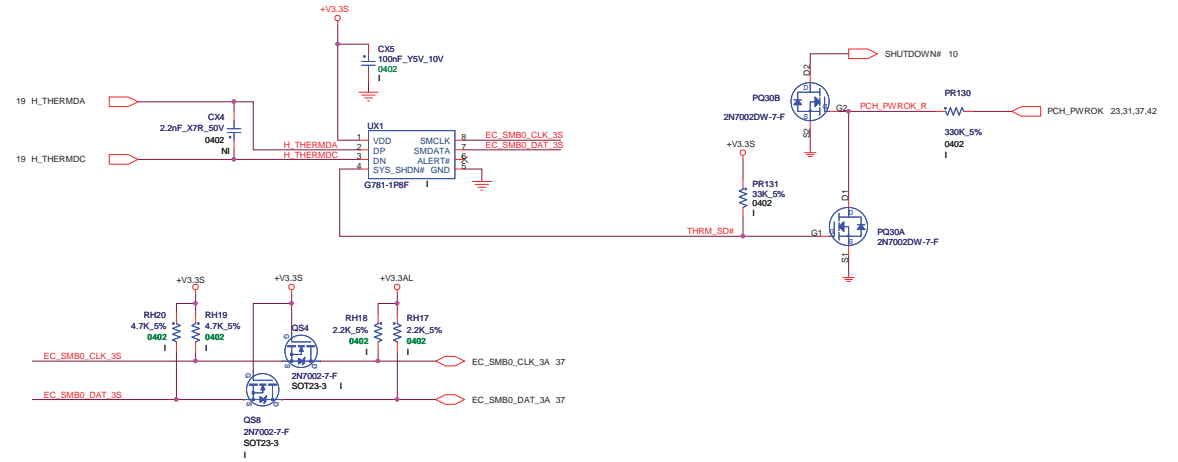
Title	Mini PCIe&BT
Size	Document Number
Customer	TPN-F101/TPN-F102 Montevina platform
Page Modified	Monday, January 24, 2011 09:28 (UTC GMT) Sheet 42 of 46



FAN



THERMAL SENSOR



stitch cap

RF Solution