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40	ICH8-M(GPIO) 3/5	1.0	2007/8/24	80		1.0	2007/8/24

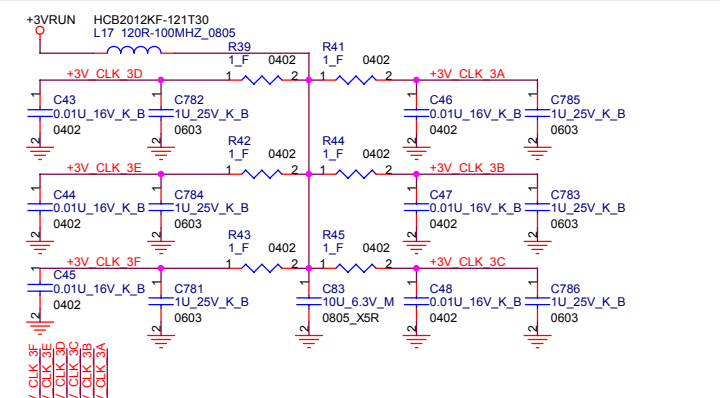
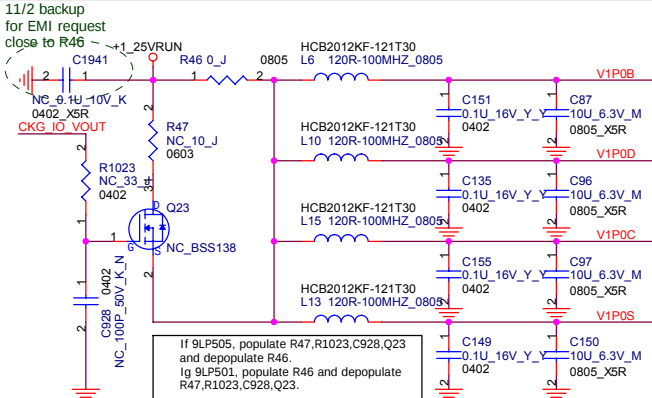
Project Code & Schematics Subject: M612 PVT Main Board

PCB P/N: 黃田
翰宇博德

P. Leader		Check by	Design by
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division			
Title Index Page			
Size A3	Document Number (M612-1-01)MainBoard (MBX-176) 2007.8.24		Rev 1.0
Date: Friday, August 31, 2007		Sheet 1 of 81	

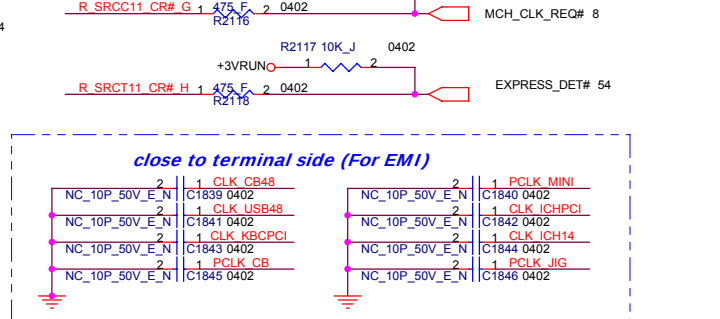
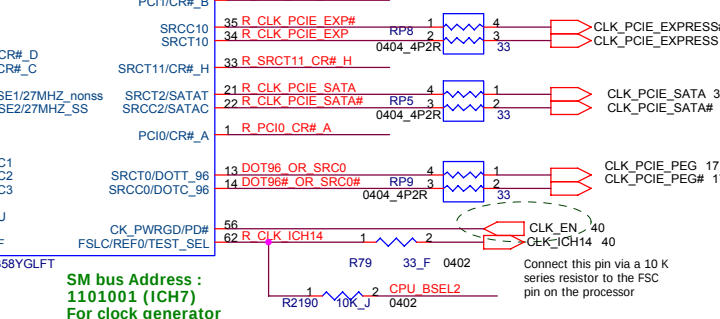
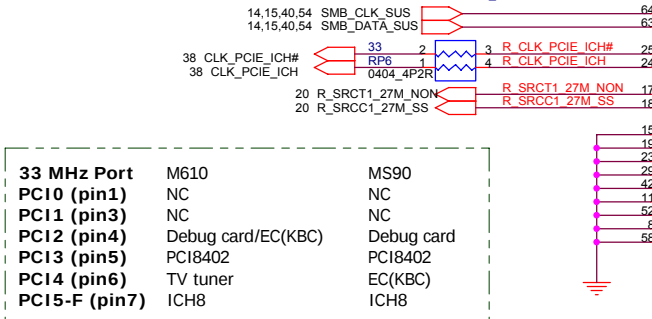
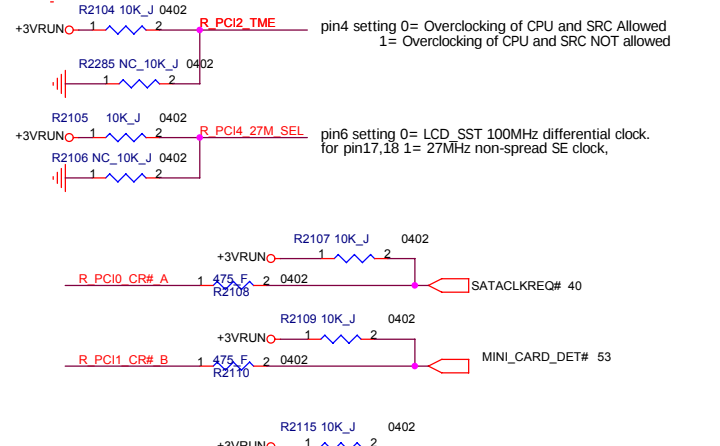
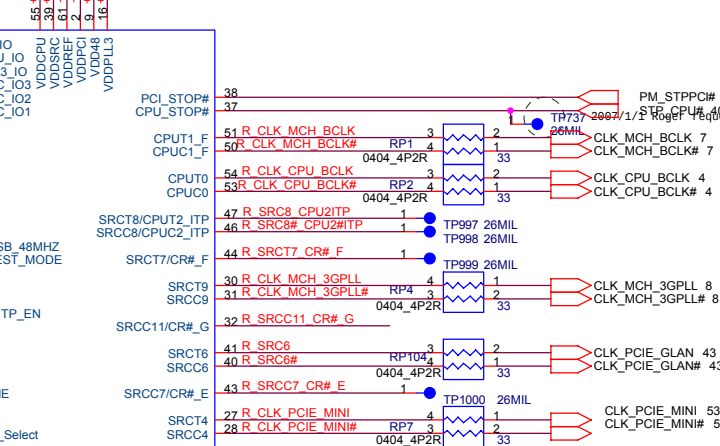
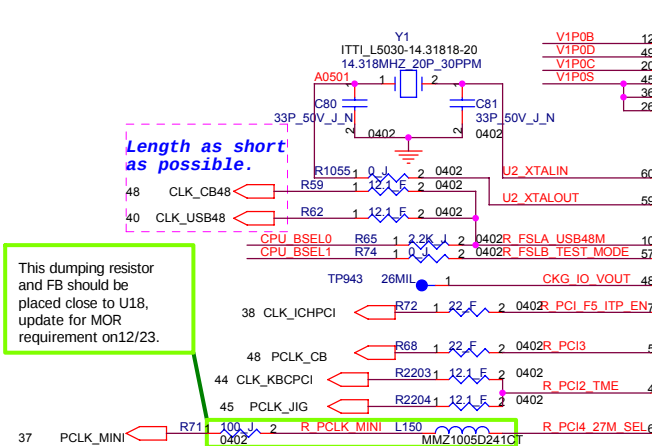
Red texts:
New modified





FSB Frequency Table:

FSLC	FSLB	FSLA	CPU SRC[7:0]	PCI	FSB
1	0	1	100	100	33 /
0	0	1	133	100	33 /
0	1	1	166	100	33 667
0	1	0	200	100	33 800
0	0	0	266	100	33 /
1	0	0	333	100	33 /
1	1	0	400	100	33 /
1	1	1	(Reserved)		

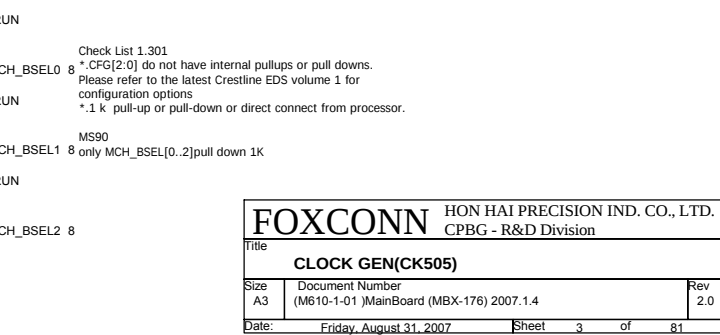


33 MHz Port

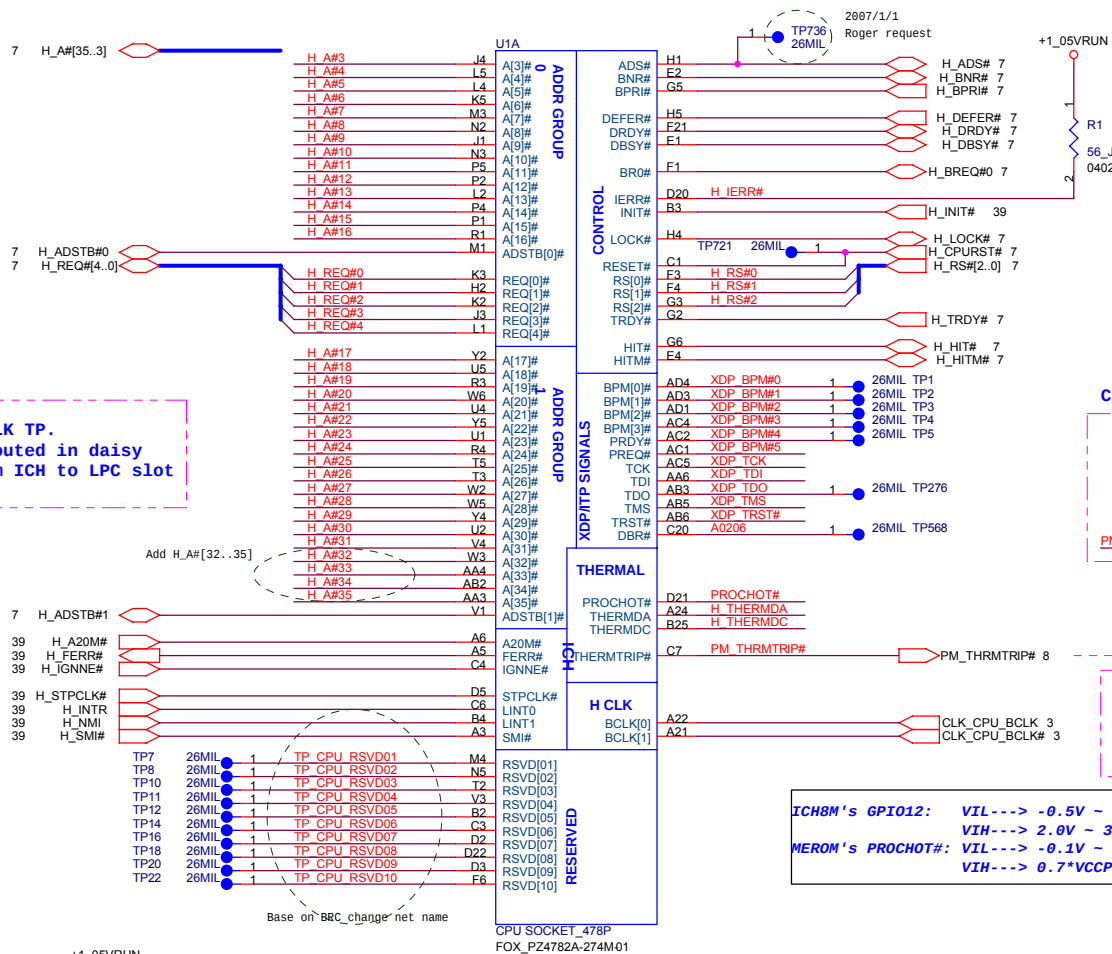
Port	M610	MS90
PCI0 (pin1)	NC	NC
PCI1 (pin3)	NC	NC
PCI2 (pin4)	Debug card/EC(KBC)	Debug card
PCI3 (pin5)	PCI8402	PCI8402
PCI4 (pin6)	TV tuner	EC(KBC)
PCI5-F (pin7)	ICH8	ICH8

100 MHz Port

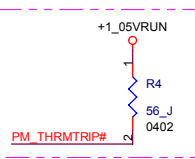
Port	M610 setting configuration	S/W Setting this pin type (B2b0=0) for use SRC0	S/W Setting CLKREQ for this pin
SRC0 (pin13,14)	GFX PCIE_PEG		
SRC1 (pin17,18)	(SRC0 / SRC1 only either one)		
SRC2 (pin21,22)	PCIE SATA		
SRC3 (pin24,25)	PCIE ICH8		
SRC4 (pin27,28)	PCIE MINI		
SRC6 (pin40,41)	PCIE G-LAN		
SRC7 (pin43,44)	NC		
SRC8 (pin46,47)	NC		
SRC9 (pin30,31)	MCH 3GPLL		
SRC10 (pin34,35)	PCIE EXPRESS		
SRC11 (pin32,33)	CR#G(MCH)/CR#H(EXPRESS)		



Layout note:
no stub on H_STPCLK TP.
H_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.

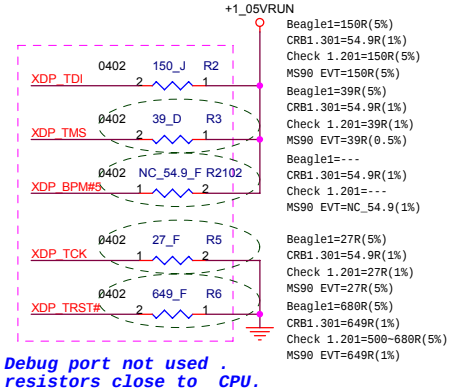


Close to CPU side



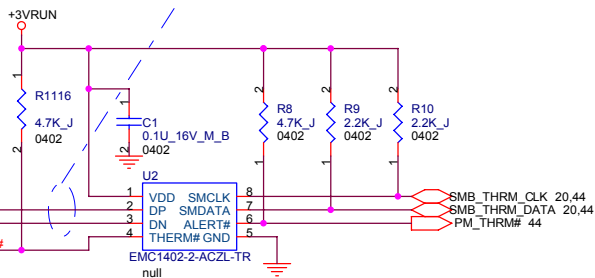
PM_THRMTRIP# should connect to ICH7-M and GMCH without T-ing (No stub)

ICH8M's GPIO12: VIL---> -0.5V ~ 0.8V
VIH---> 2.0V ~ 3.3+0.5V
MEROM's PROCHOT#: VIL---> -0.1V ~ 0.3*VCCP
VIH---> 0.7*VCCP ~ VCCP+0.1



Debug port not used . resistors close to CPU.

W/S:10/10 (microstrip)

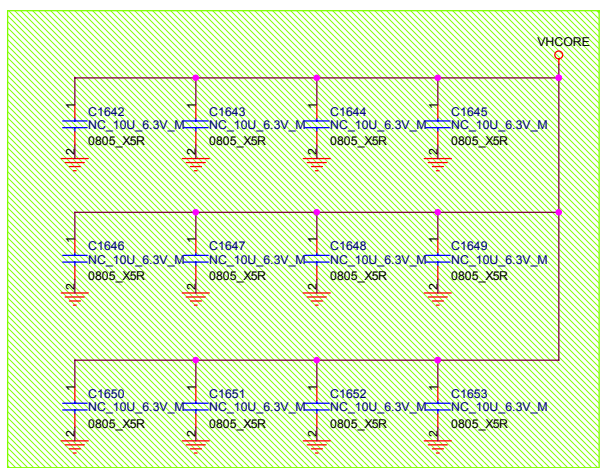
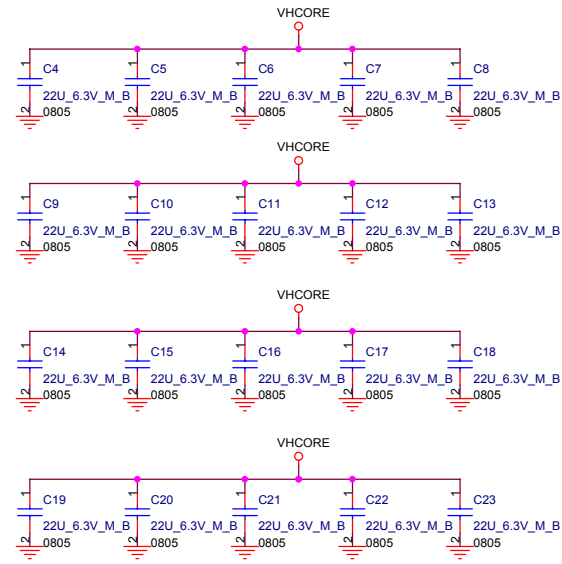


SM bus Address : 1001101 = 9A
For F75384M Place Thermal-Sensor near CPU & GMCH.

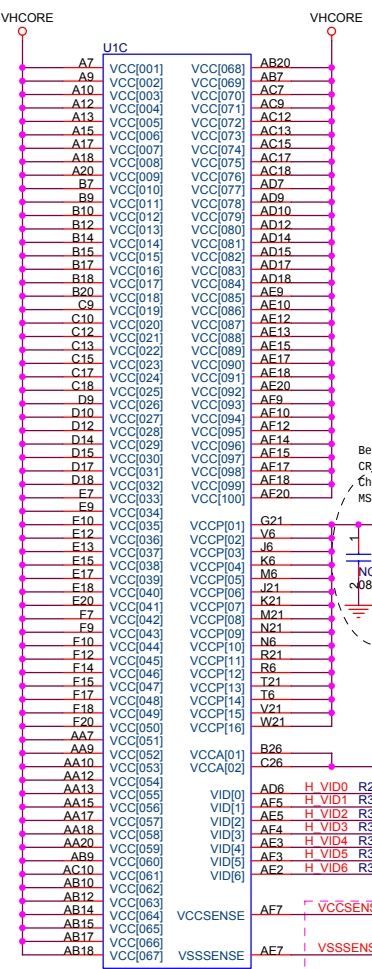
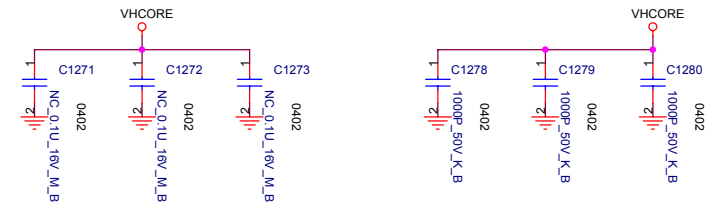
11/16 change part from F75384M (15-F75384M-0000) to G781-1P8I (15-G7811P8-0000)

CPU_VCCA----->130mA
CPU_VCCP----->4.5A
CPU_VCC----->44A

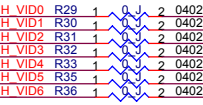
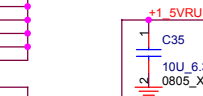
MS90 check



Backup 10uF capacitors for 22uF shortage.

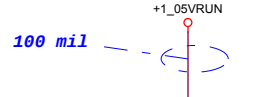


Beagle1=18U
CRB1_301=N0
Check 1_201=N0
MS90 EVI=N0

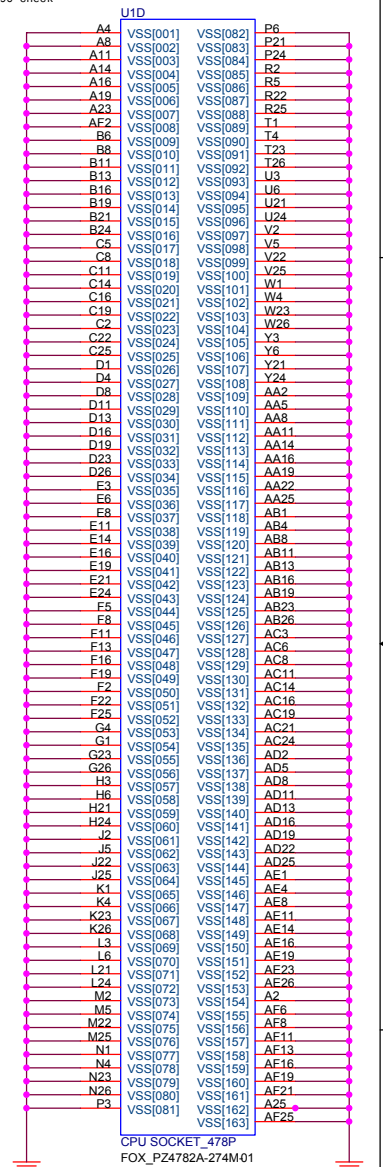


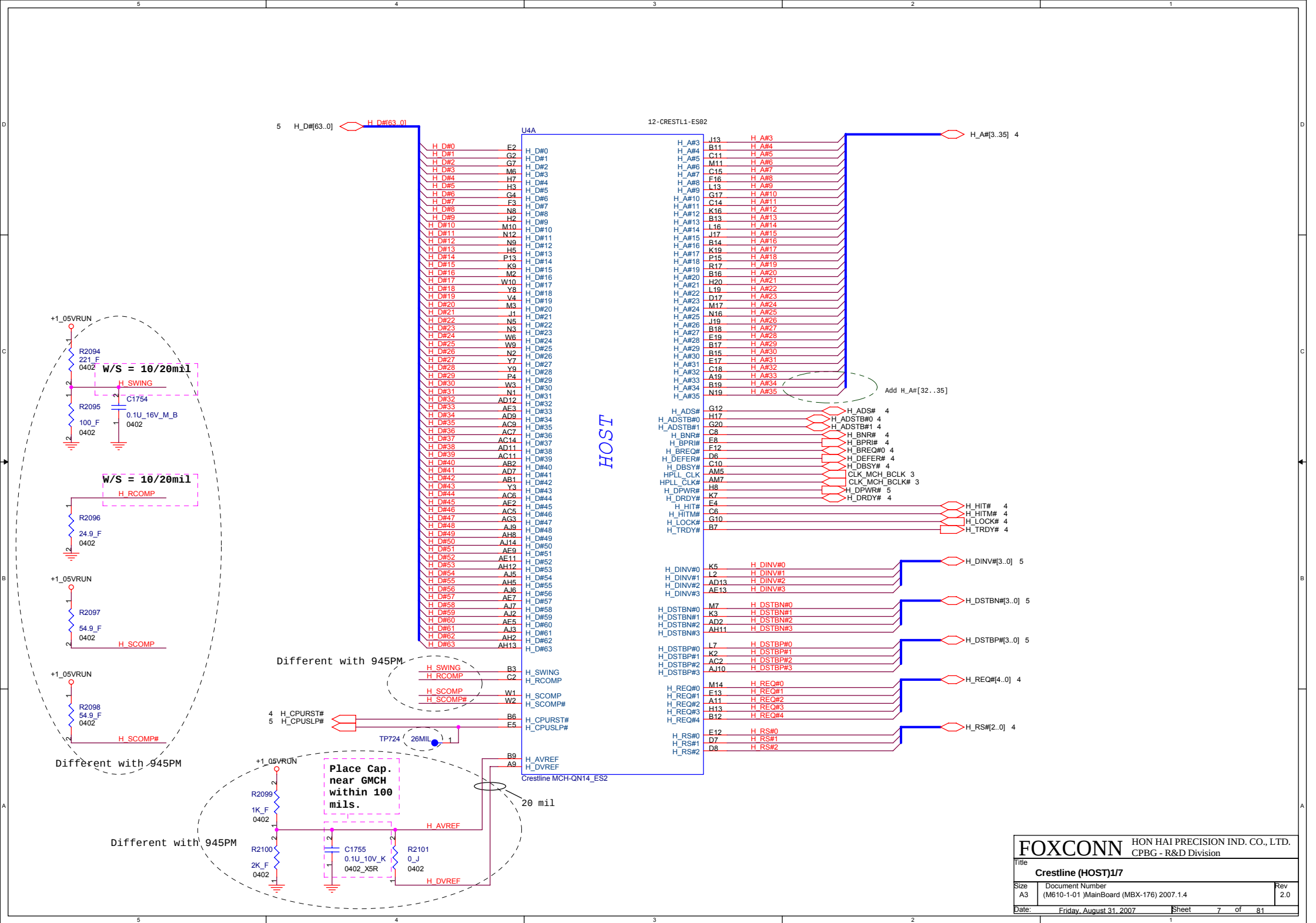
Layout Note: Route
VCCSENSE traces at 27.4
Ohms with 50 mil spacing.
Place PU and PD within 1
inch of cpu.
width=18 mil
spacing=7 mil

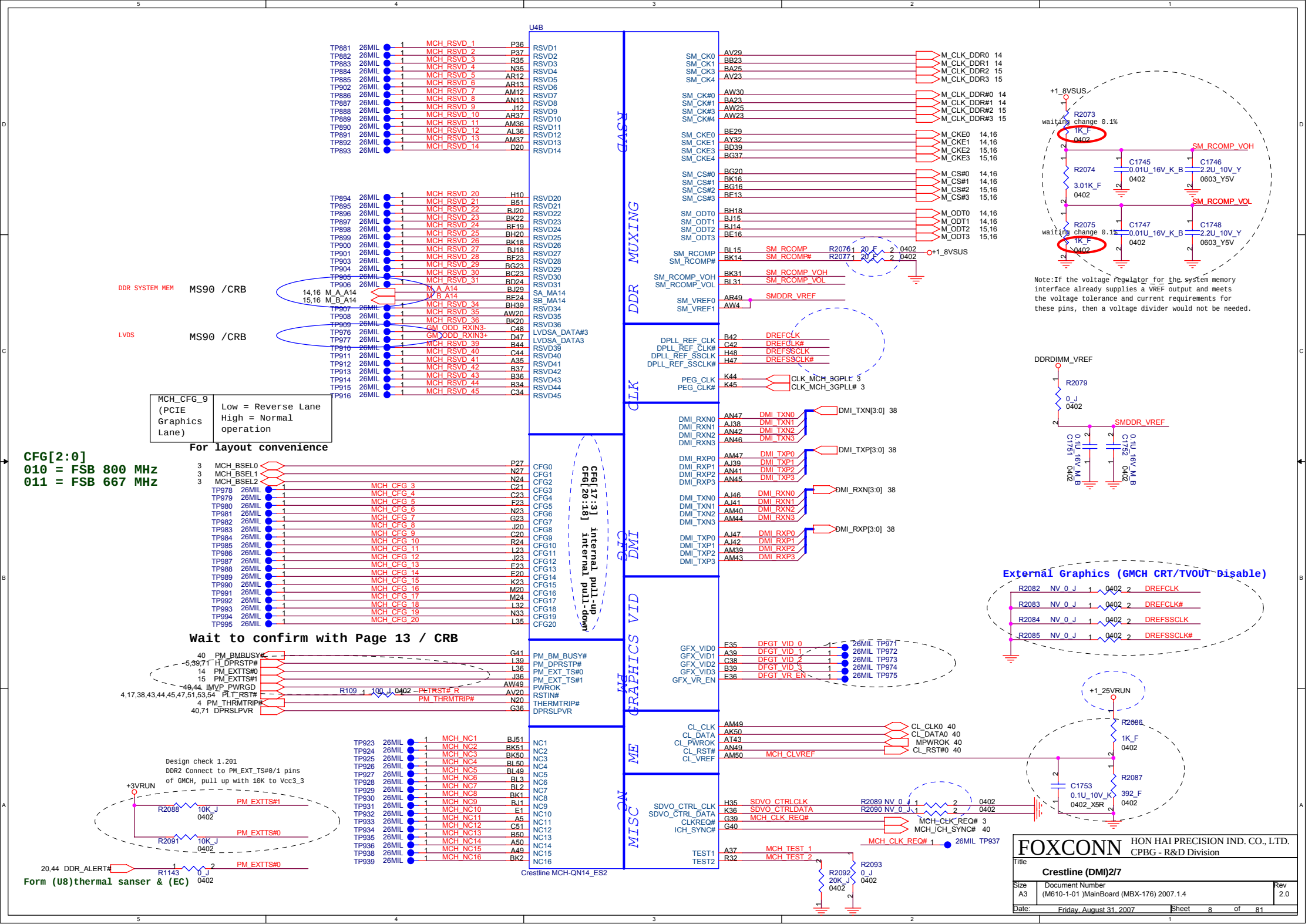
(Design check 1.301) 2006.9.3
No Stuff 27.4 ± 1% pull-down to GND
near Intel MVP 6 controller for testing purposes.

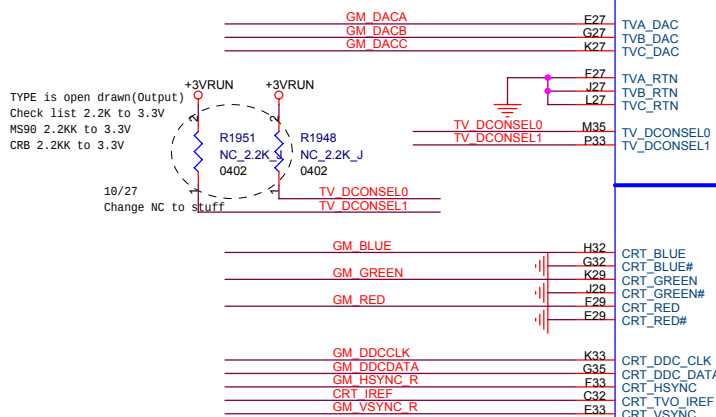
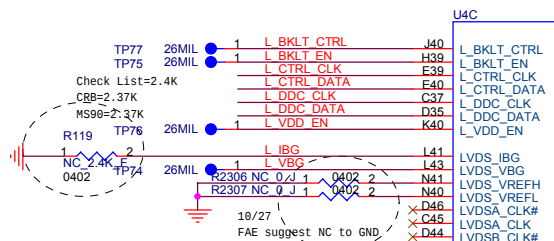


LAYOUT NOTE:
Place 0.01uF
near PIN B26

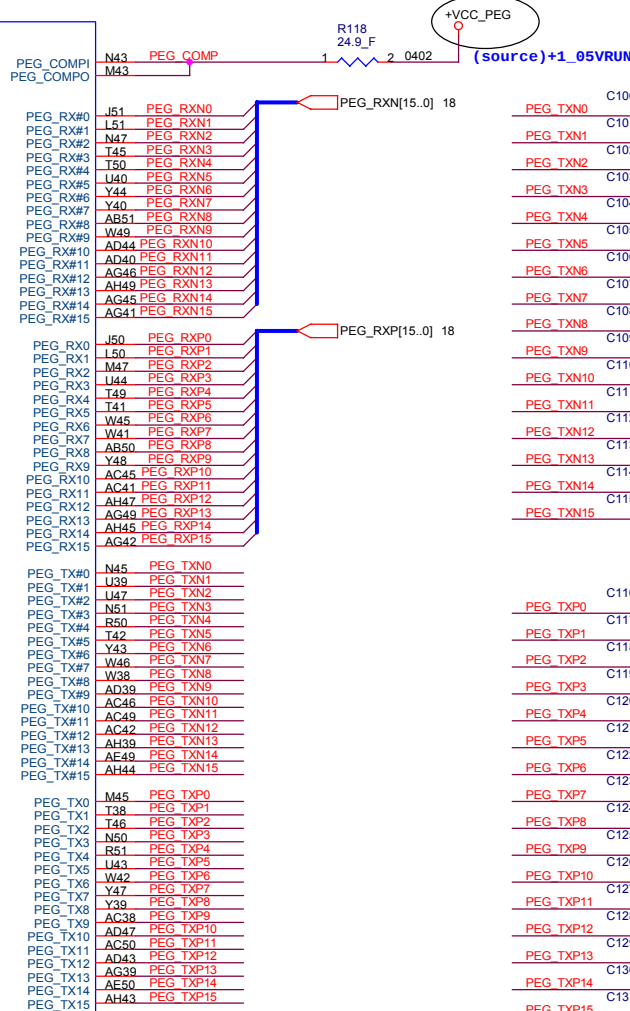
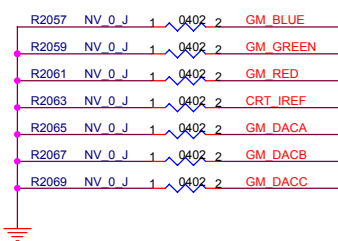




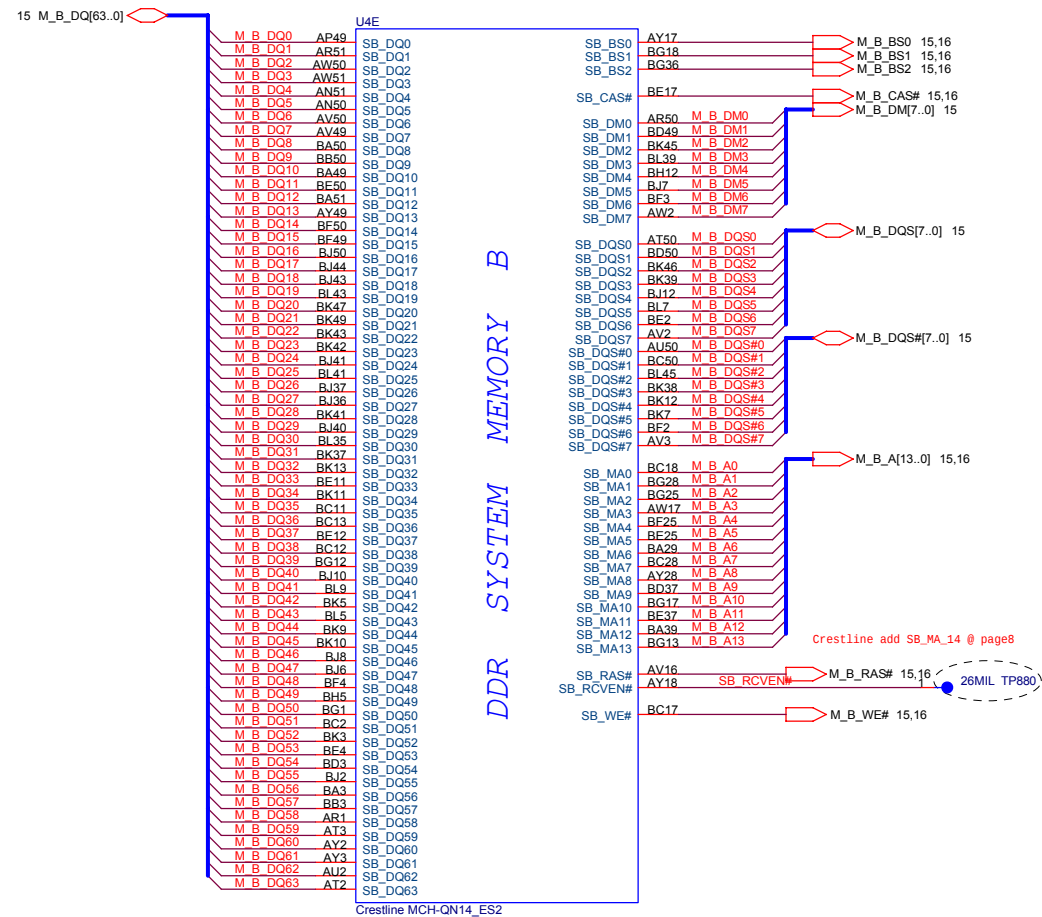
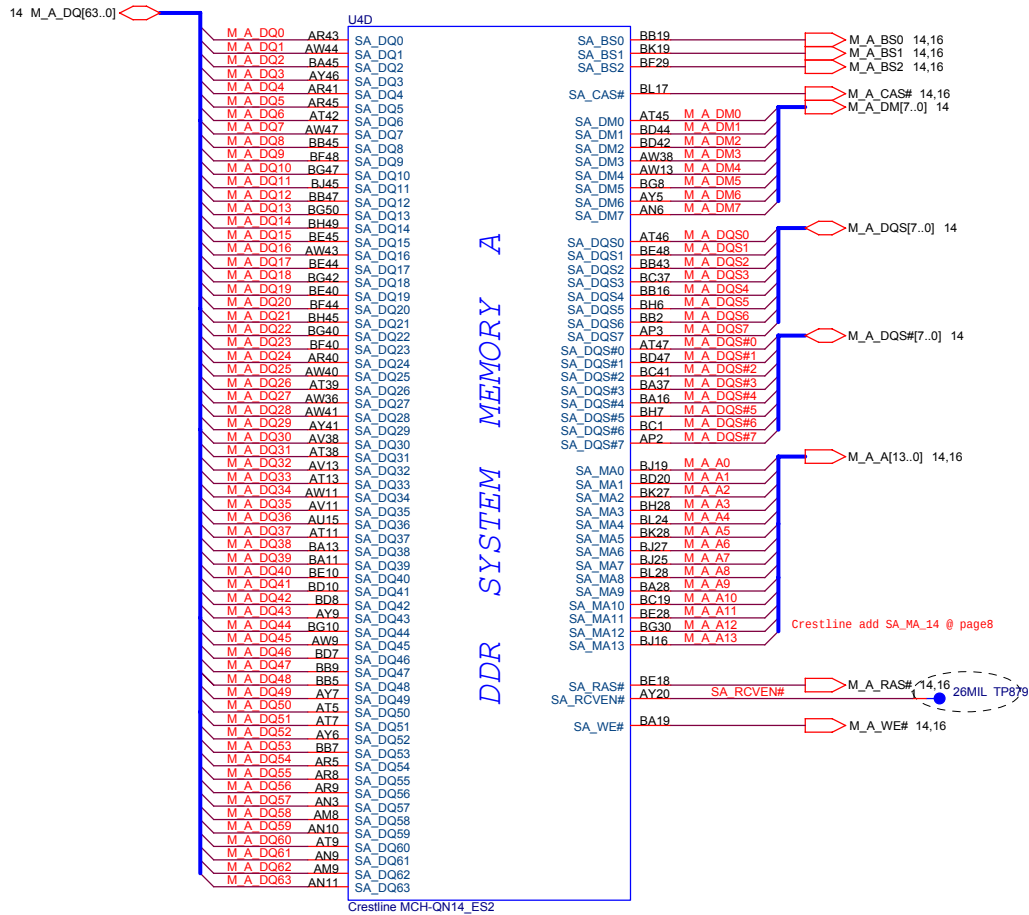


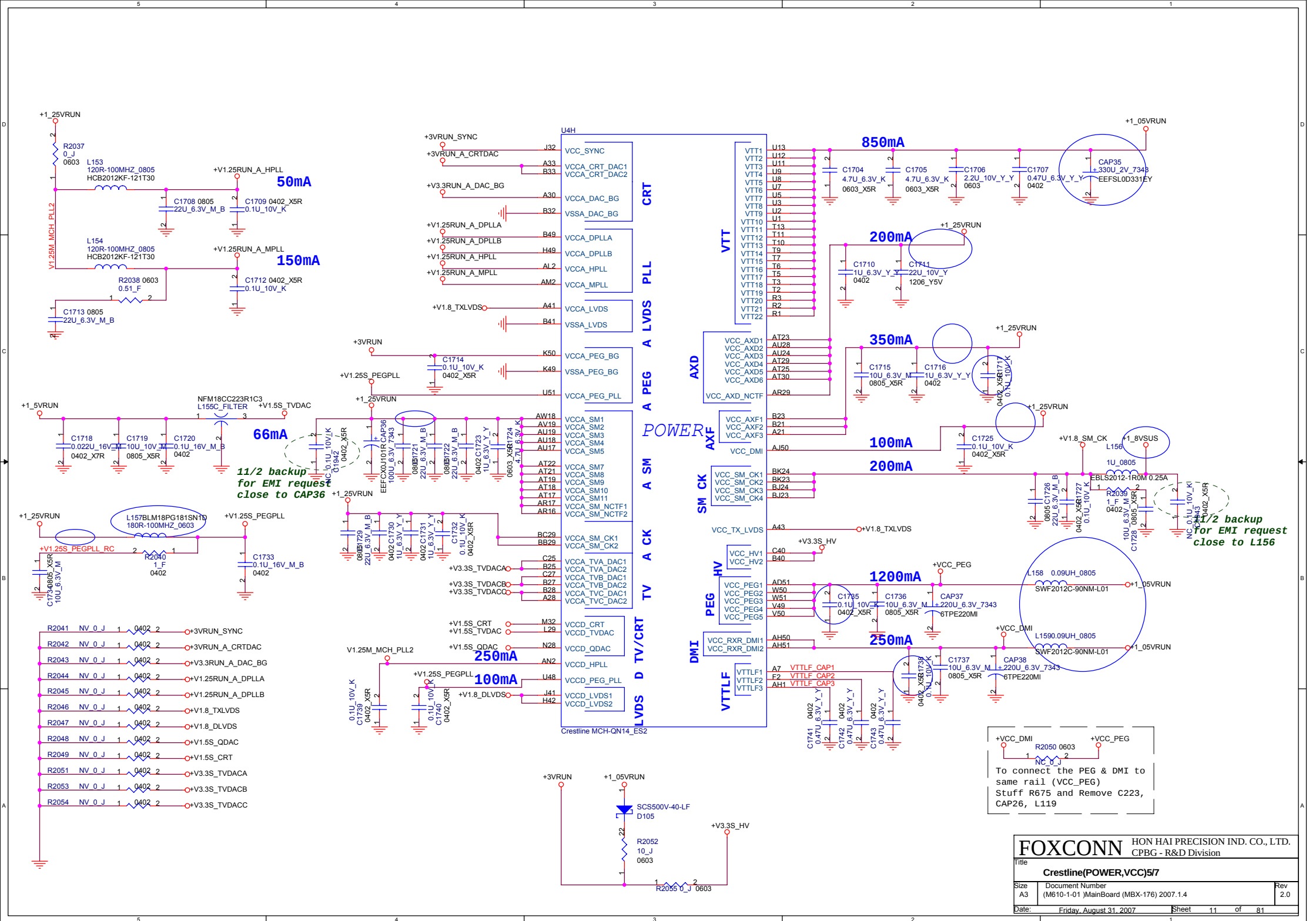


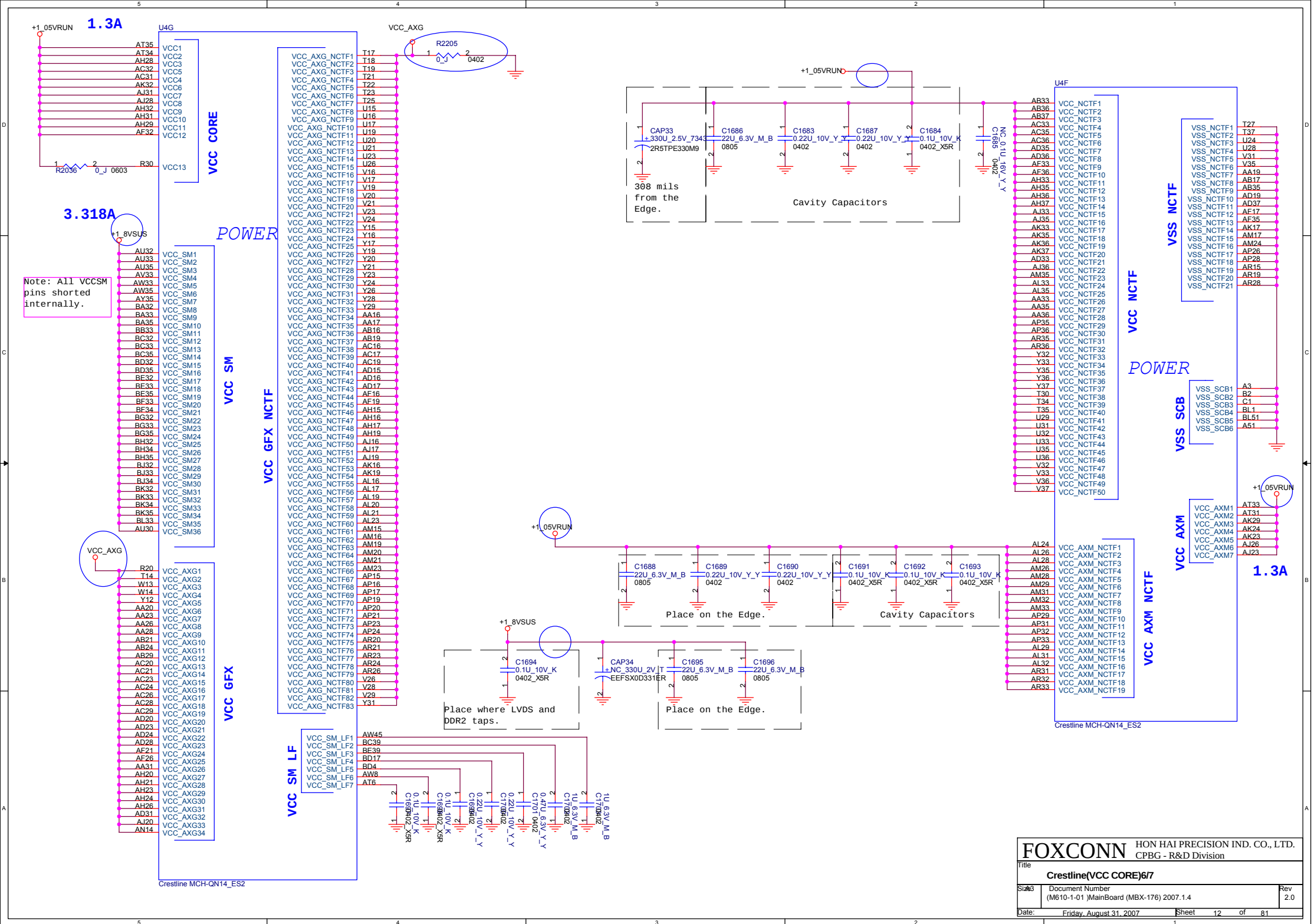
External Graphics (GMCH CRT/TVOUT Disable)

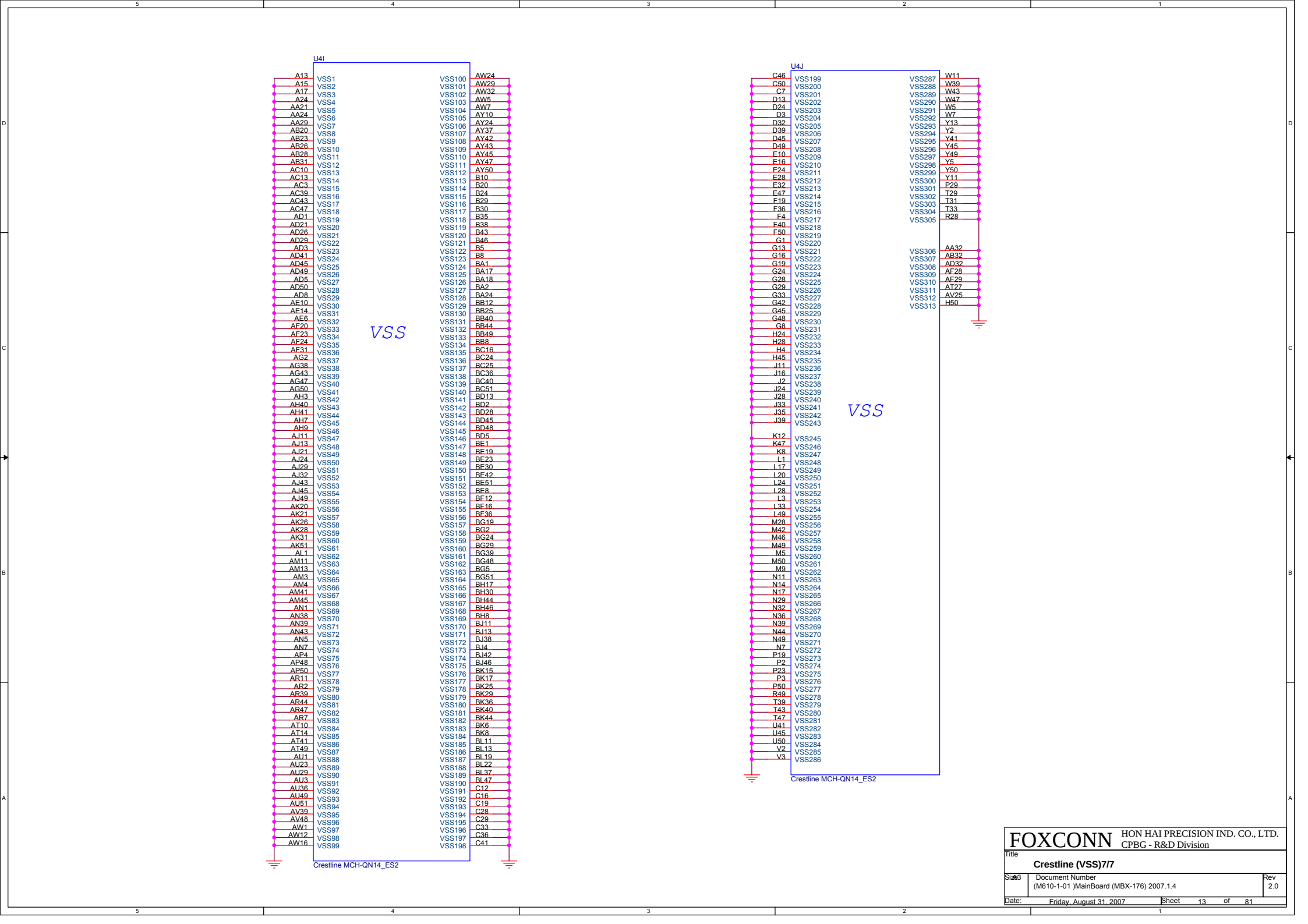


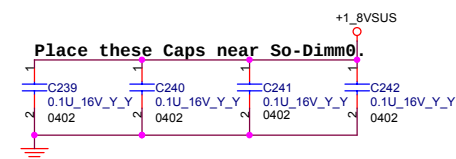
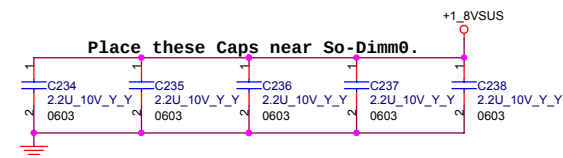
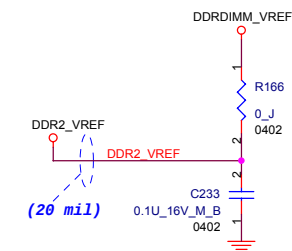
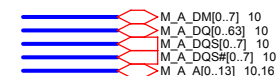
Base on below document:
Mobile Merom Processor and Crestline Chipset
- Santa Rosa Platform Design Guide-21112,1.0
.pvd.pdf (May 2006/ Rev 1.0)page 193
Table 82. External Graphics (GMCH Integrated Graphics Disable)
Connect these signals to GND

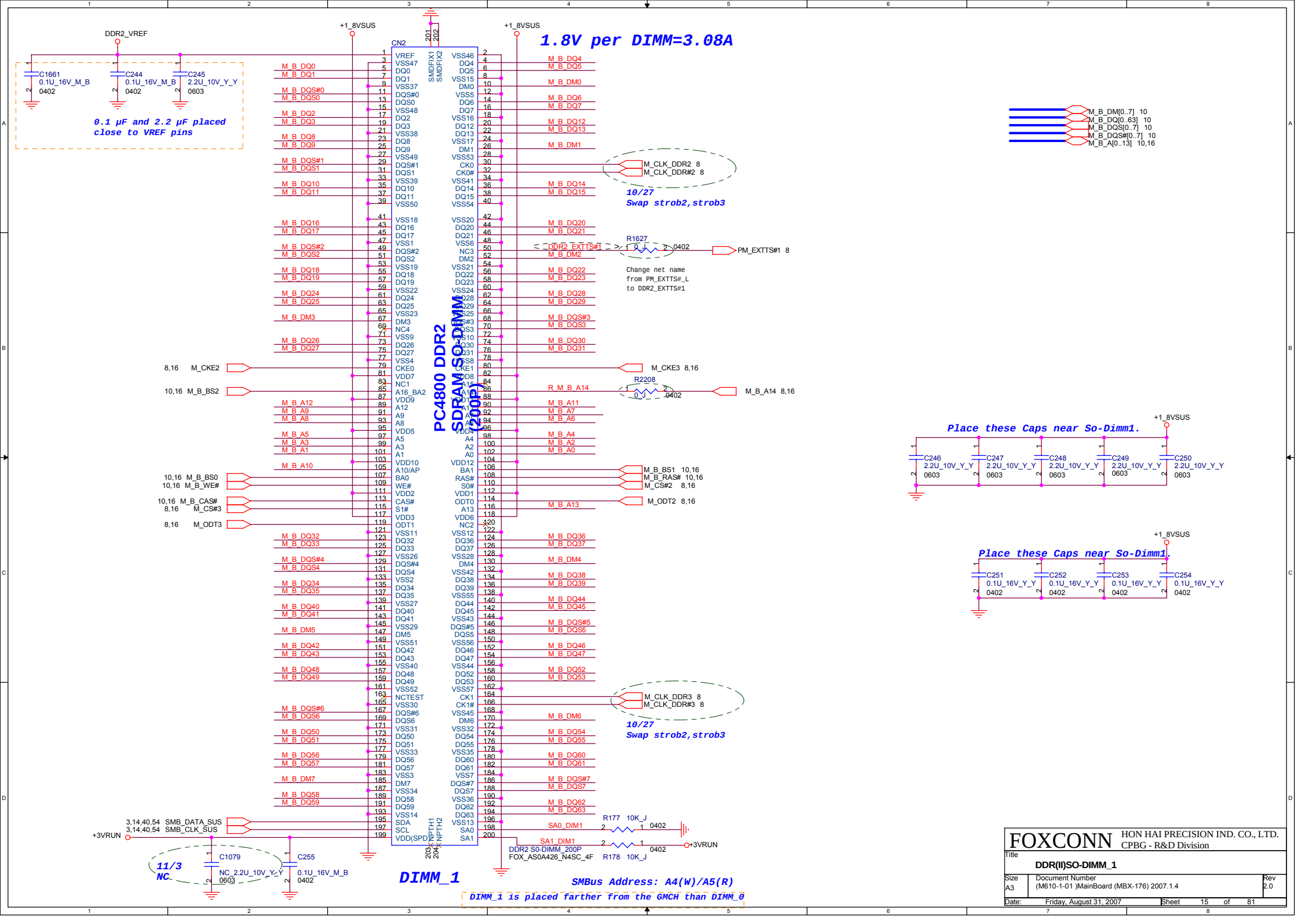


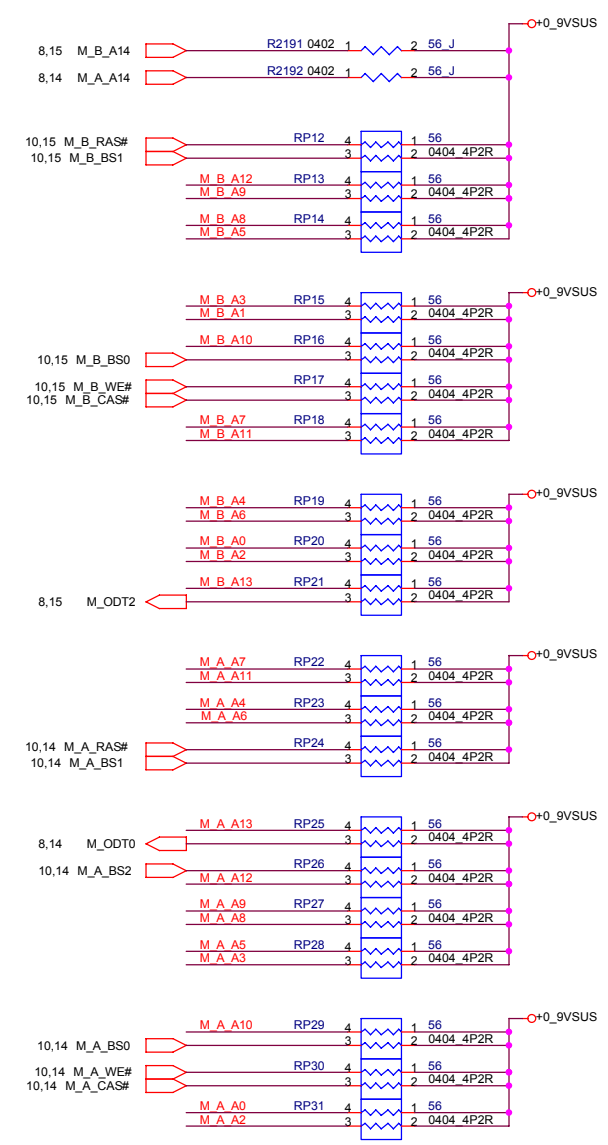
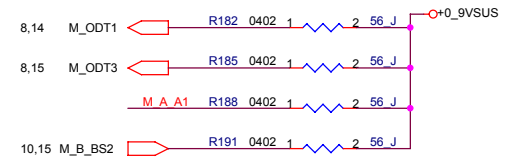
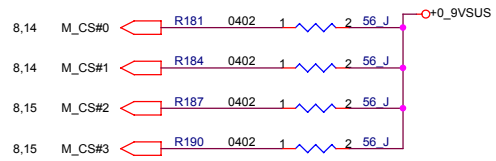
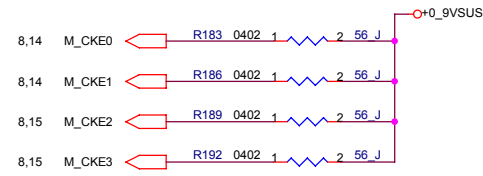
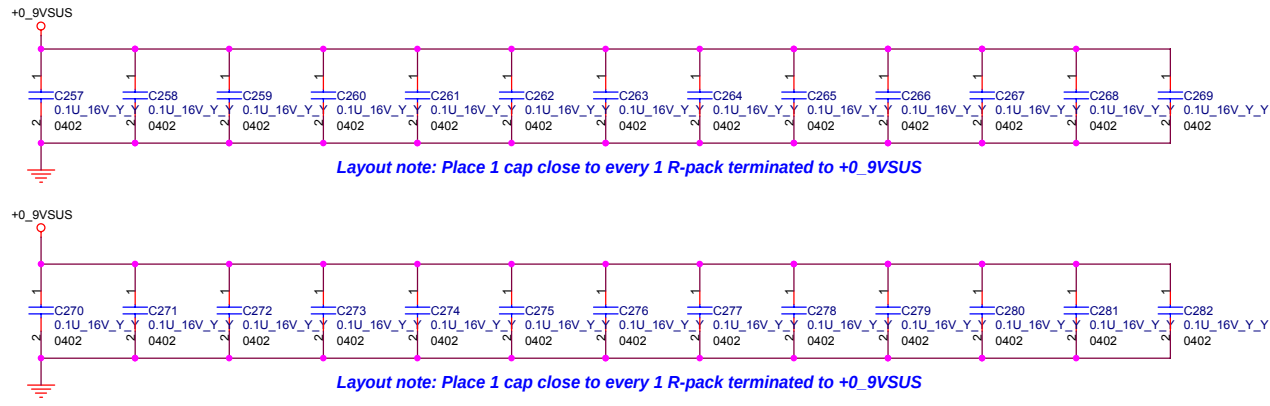


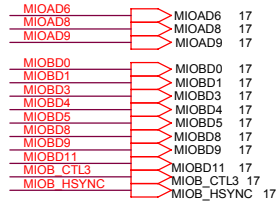
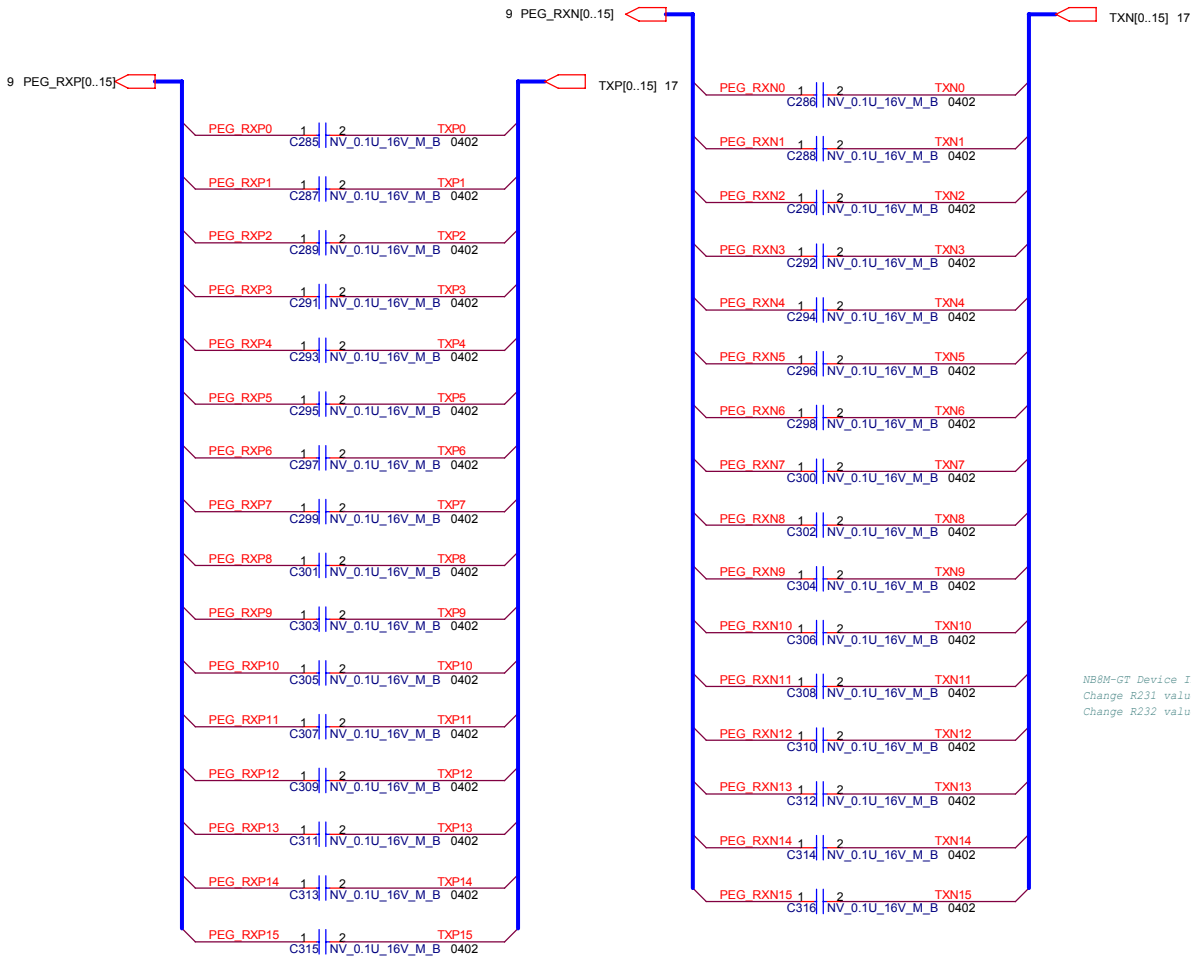












NB8X Strap for GDDR3-136ball RAM_CFG0
0001 16Mx32Infineon
0010 16Mx32Hynix
0011 16Mx32Samsung
0101 8Mx32Infineon
0110 8Mx32Hynix
0111 8Mx32Samsung

SUB_VENDOR
0 (USE SYSTEM BIOS)
1 (USE EXTERNAL ROM)

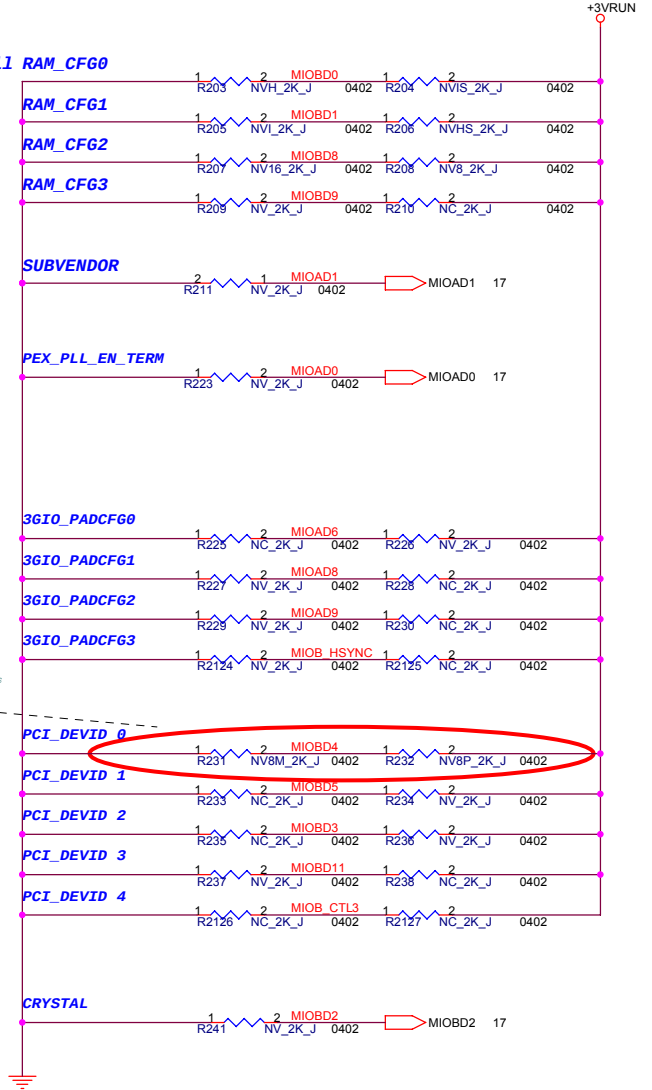
MIOAD0 is used to set the PCI Express PLL termination enable.
DEFAULT "0"

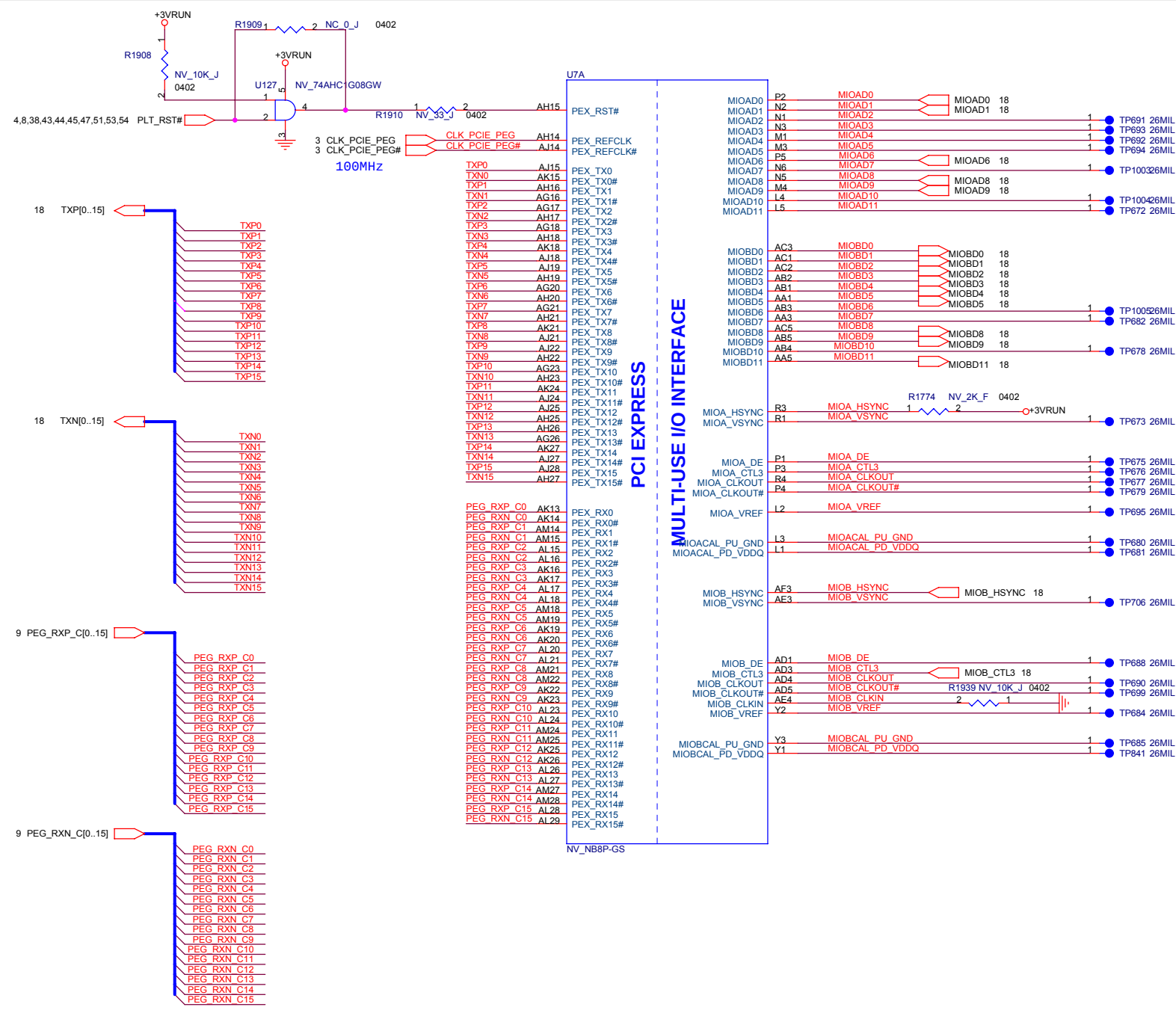
NB8X 3GIO_PADCFG[3:0]
0001

NB8M-GT Device ID setting mismatch between VBIOS and H/W Straps
Change R231 value from NC_ to NV8M_
Change R232 value from NV_ to NV8P_

NB8X PCI_DEVID[4:0]
NB8P-GS X0111 "X7"
NB8M-GT X0110 "X6"

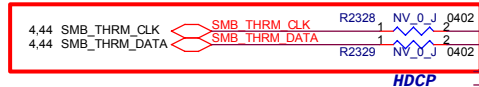
CRYSTAL (NB8X)
0 (27M Hz)
1 (Reserved)





[MIOA_HSYNC : SLOT_CLOCK_CF6]
0 GPU and MCH share a common reference clock
1 GPU and MCH do not share a common reference clock

Use GPU internal thermal sensor
Change R2328,R2329 form NC to mount

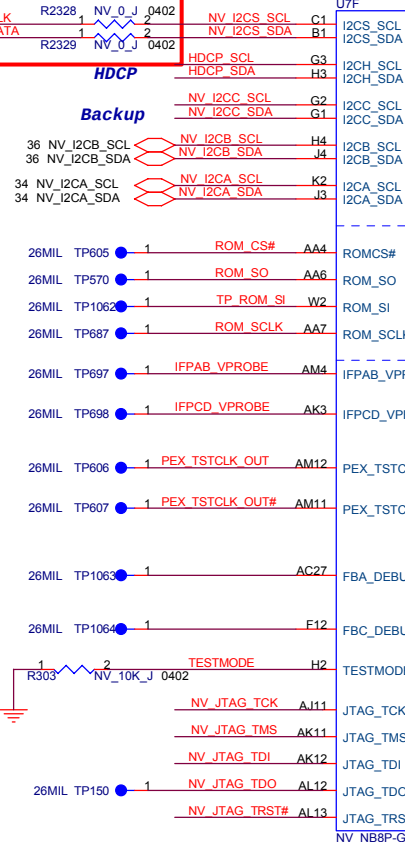
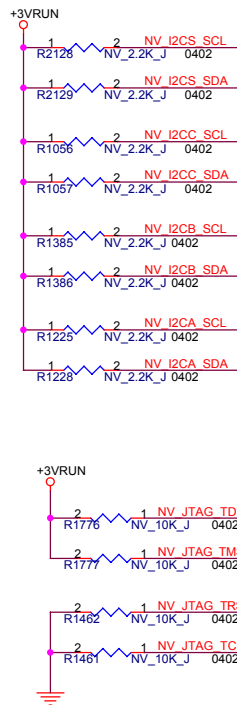


HDCP

Backup

HDMI DDC

CRT DDC

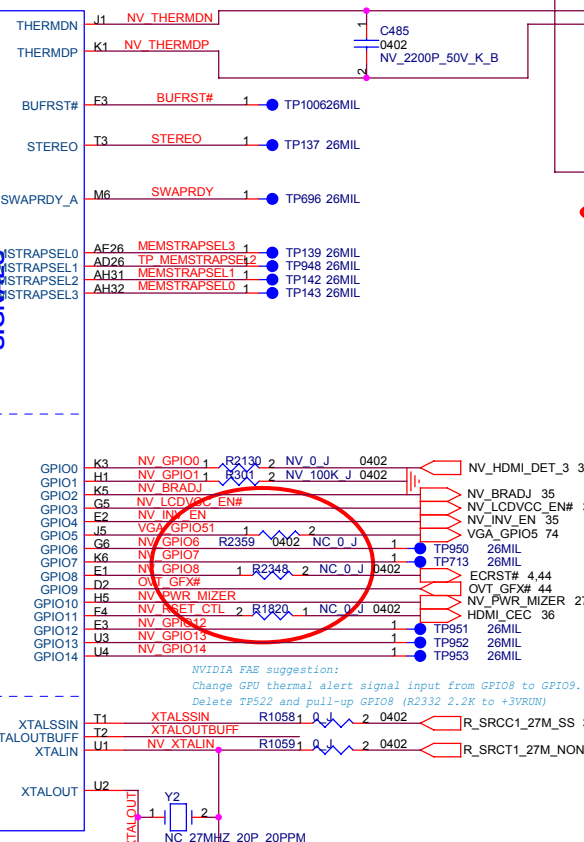


ROM

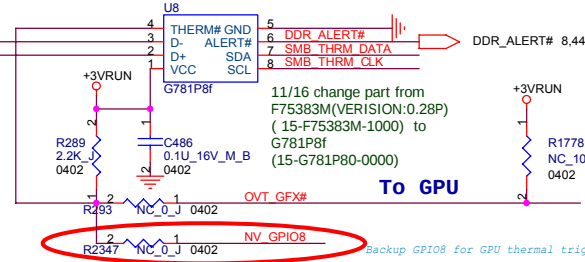
GENERAL SIGNAL

TEST SIGNAL

CRYSTAL



SM bus Address :
1001100(EC)
For F75383M



11/16 change part from F75383M(VERSION:0.28P) (15-F75383M-1000) to G781P8 (15-G781P80-0000)

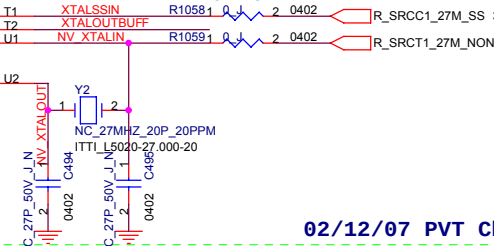
Backup GPIO8 for GPU thermal trigger signal
Change R293 from mount to NC for using internal thermal sensor

From EC

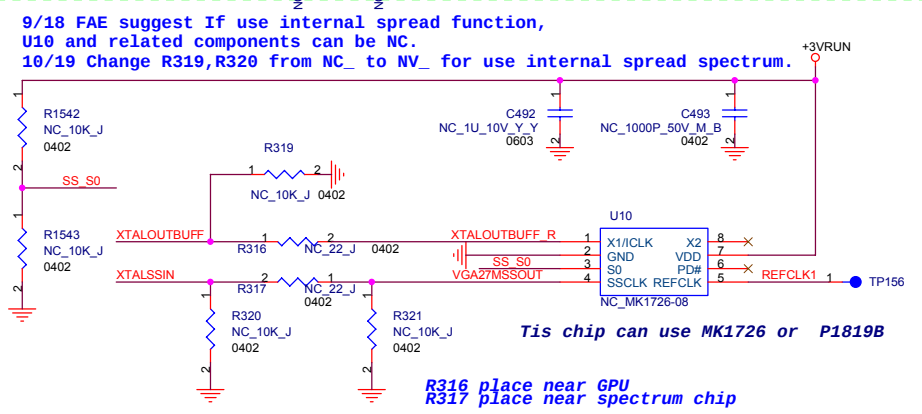
2007/1/4 Update

GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	Yes	HDMI Hot Plug Detect 0 (HPD0)	Active High
GPIO1	I	Yes	DVI Hot Plug Detect 1 (HPD1)	Active High
GPIO2	O	Yes	LCD BL Brightness (LCD0_BL_PWM)	Active High
GPIO3	O	No	Panel Power (LCD0_VDD)	Active Low
GPIO4	O	Yes	LCD Backlight enable (LCD0_BL_EN)	Active High
GPIO5	O	Yes	GPU Power Downgrade for NV_VDD	Active Low
GPIO8	O	No	Thermal Alert Output (>125 Degree)	Active Low
GPIO9	I	No	System Power Limit Alert Input	Active Low
GPIO10	O	No	Memory Vref switch (MEM_VREF)	Active High
GPIO11	I/O	No	HDMI CEC Function Backup	

NVIDIA FAE suggestion:
Change GPU thermal alert signal input from GPIO8 to GPIO9.
Delete TP522 and pull-up GPIO8 (R2332 2.2K to +3VRUN)



02/12/07 PVT Change



9/18 FAE suggest If use internal spread function, U10 and related components can be NC.
10/19 Change R319,R320 from NC_ to NV_ for use internal spread spectrum.
Tis chip can use MK1726 or P1819B
R316 place near GPU
R317 place near spectrum chip



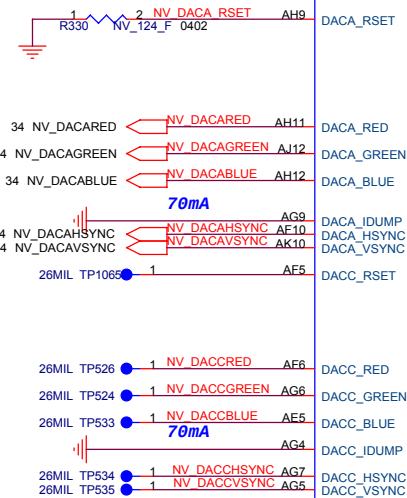
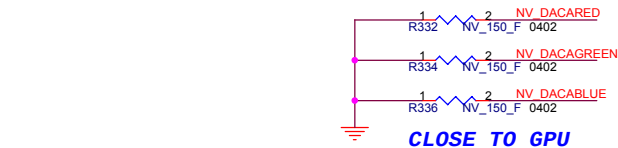
Change R2333 from NC to mount for using internal thermal sensor

SP	SPREAD	Spread
0	DOWN	-1.8
1	DOWN	-6.6
2	DOWN	-2.5

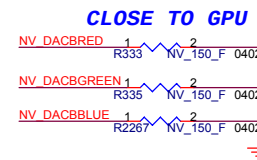
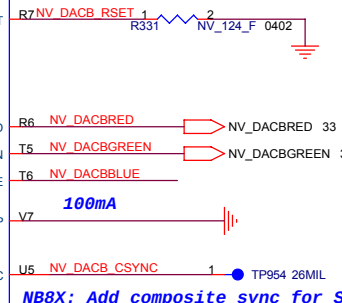
0 = connect to GND
M = unconnected
1 = connect directly to VDD

SRS	SPREAD	Spread
0	DOWN	-1.25
1	DOWN	-1.75

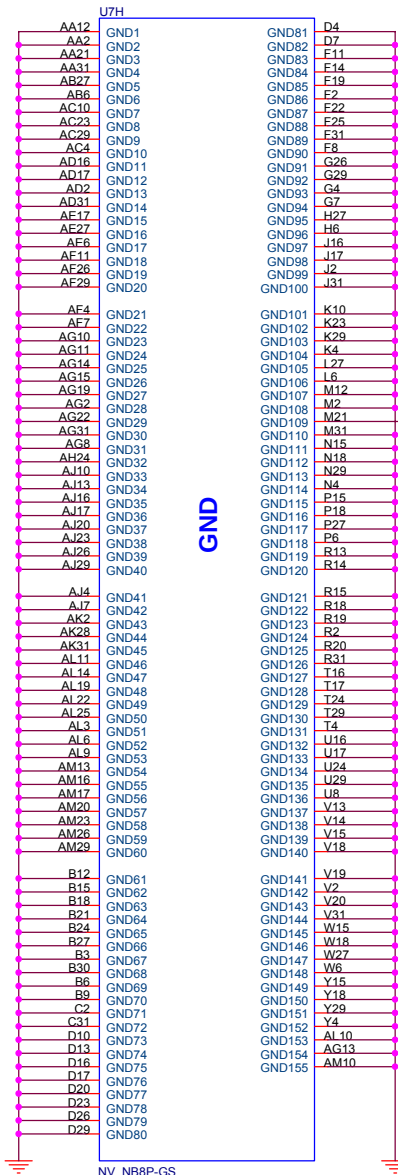
nVidia support Down -1.25%



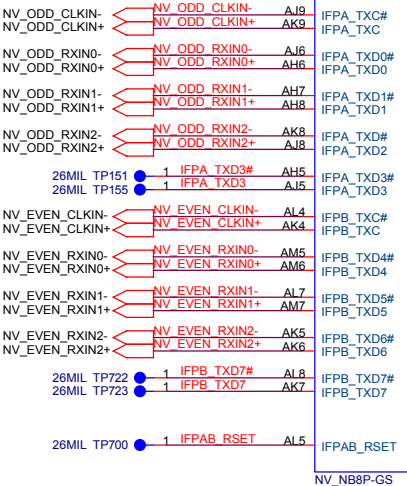
VIDEO DAC



NB8X: Add composite sync for SCART support



GND SENSE



LVDS

TMDS

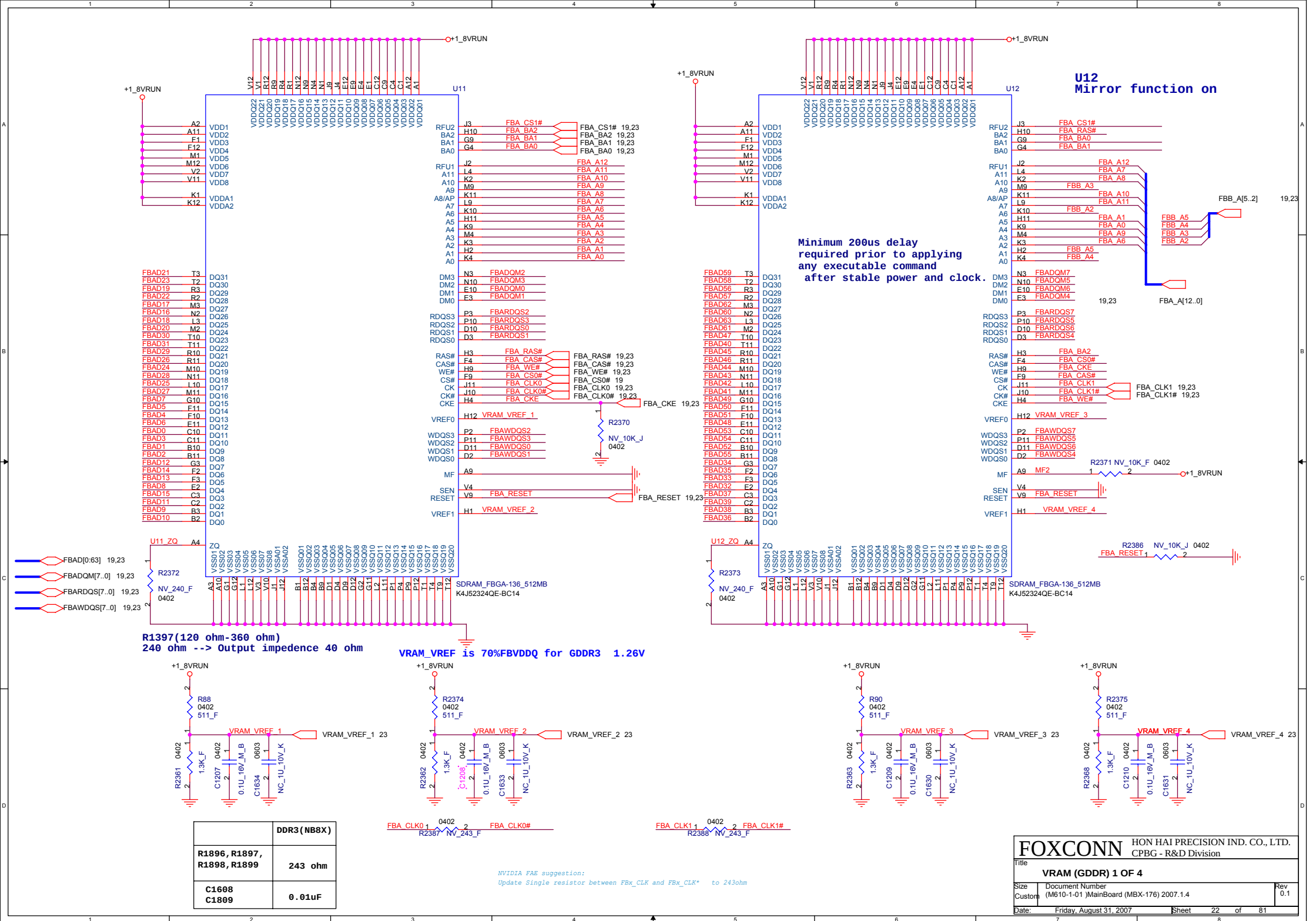
TMDS CLK 154MHz

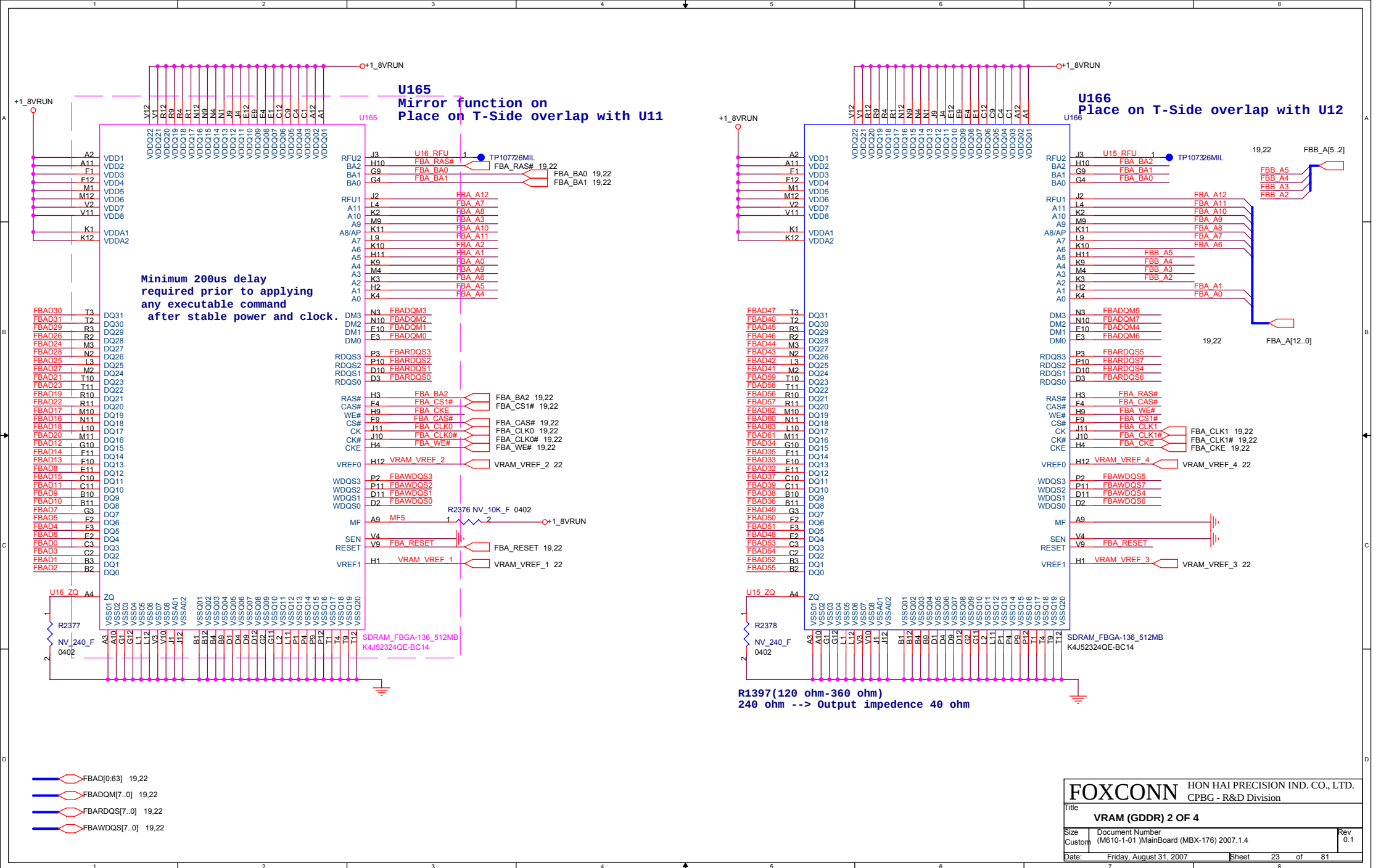
10/6 Add test point for TMDS channel 2 cause by DVI on docking been cancelled

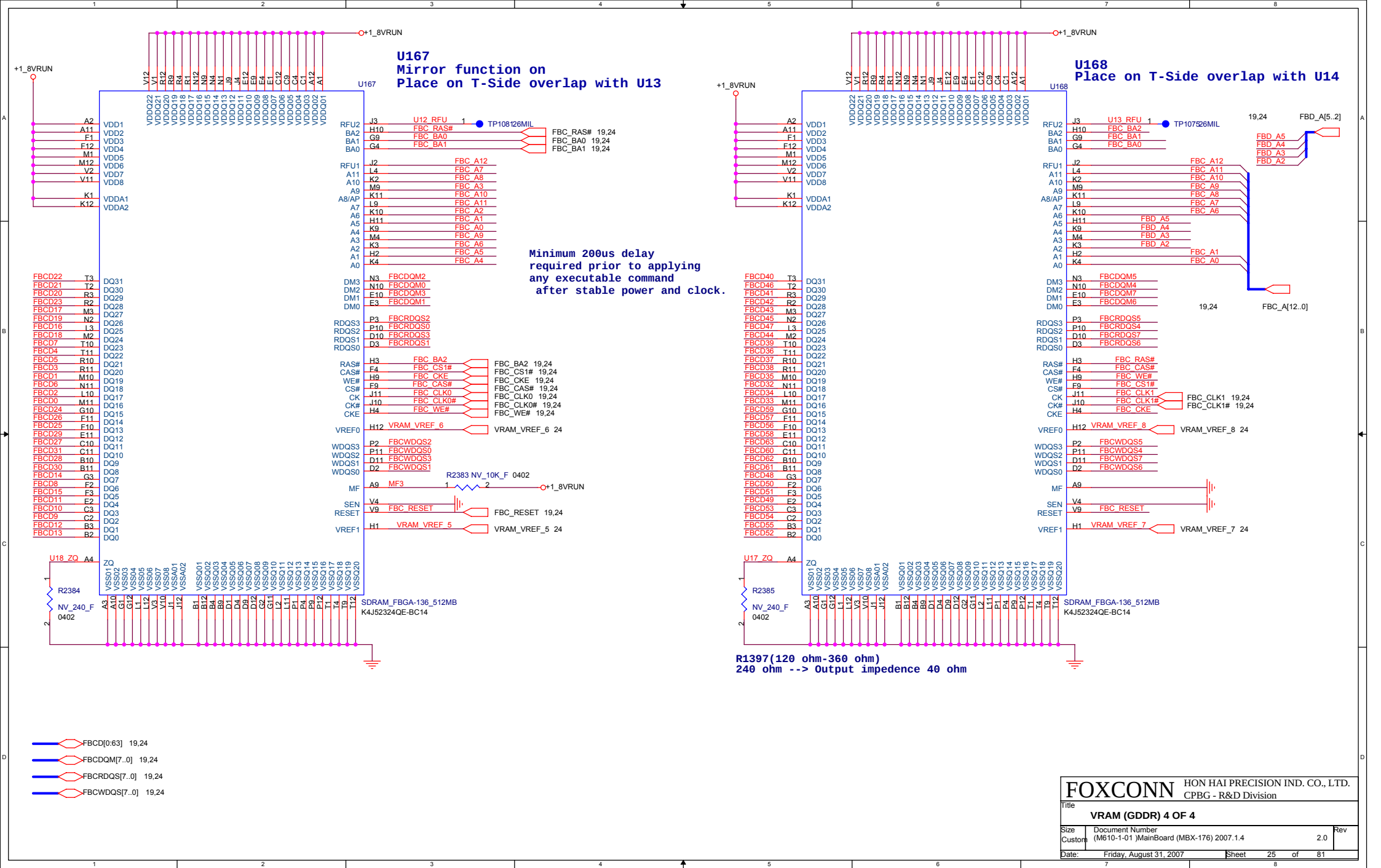
DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DCLK	SCL
	VGA-D0DATA	SDA

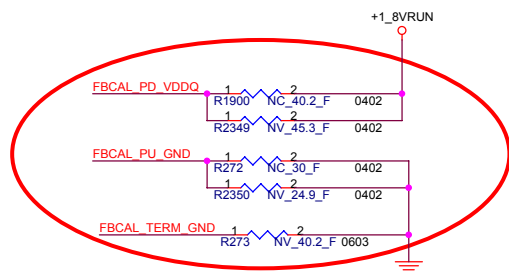
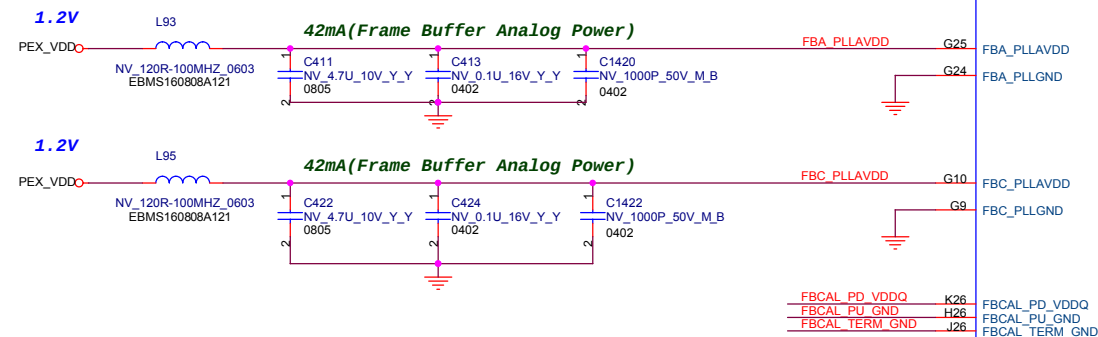
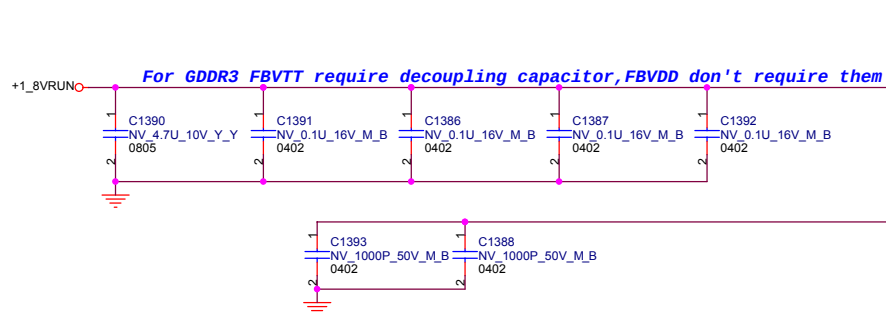
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y			
DACB-BLUE		COMPOSITE#B		
			LINE1	
			LINE2	SCL
			LINE3	SDA

DACC	DVI-I	I2CB
DACC-RED	R	
DACC-GREEN	G	
DACC-BLUE	B	
DACC-HSYNC	HSYNC	
DACC-VSYNC	VSYNC	
	DVI-DCLK	SCL
	DVI-D0DATA	SDA









NVIDIA update NB8M VRAM termination value

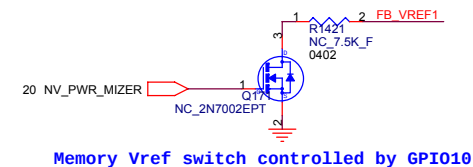
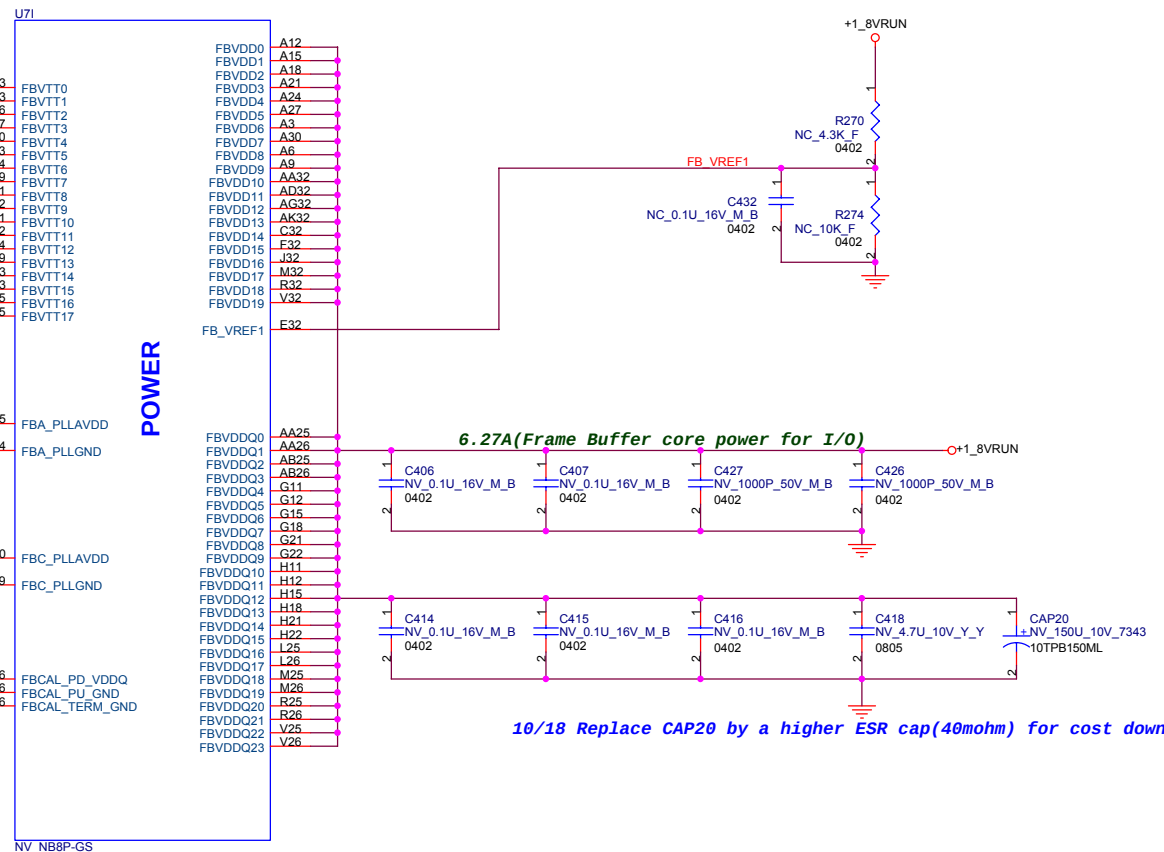
FBCAL_PD_VDDQ 45.3 Ω

FBCAL_PU_GND 24.9 Ω

FBCAL_TERM_GND 40.2 Ω

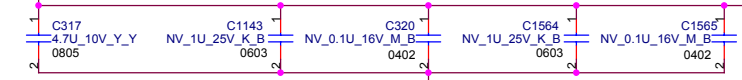
NVIDIA 07/1/5 update

	DDR3(NB8M-GT)	DDR3(NB8P-GS)
FBCAL_PD_VDDQ	45.3 ohm	45.3 ohm
FBCAL_PU_GND	24.9 ohm	24.9 ohm
FBCAL_TERM_GND	40.2 ohm	40.2 ohm



1.2V

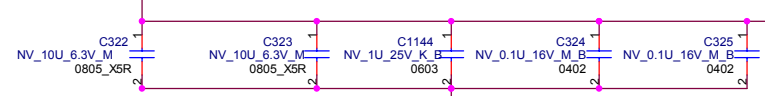
PEX_VDD



1.2V

PEX_VDD

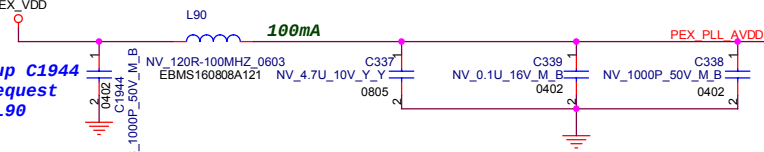
VDD/VDDQ:1500mA (I/O Power)



1.2V

PEX_VDD

11/2 backup C1944 for EMI request close to L90



1.2V

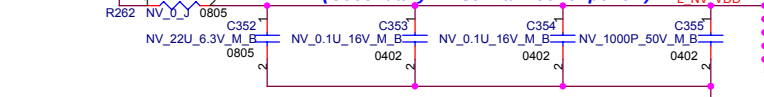
PEX_VDD



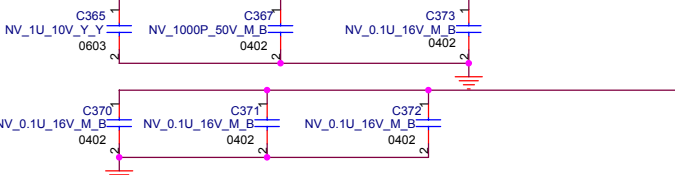
1.2V

NV_VDD

(Secondary internal core power)

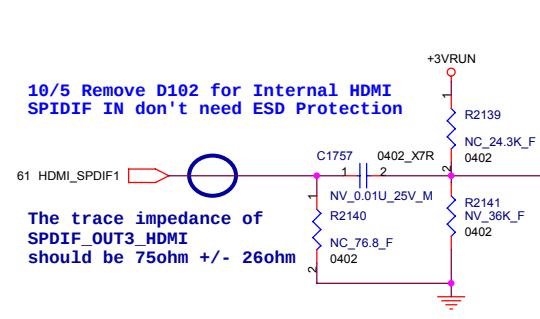


110mA(3.3V Power rail GPIO,I2C,GPU DIGITAL LOGIC)



10/5 Remove D102 for Internal HDMI SPIDIF IN don't need ESD Protection

The trace impedance of SPDIF_OUT3 HDMI should be 75ohm +/- 26ohm



26MIL TP1067	1	AG12	NC1
26MIL TP624	1	AD13	NC2
26MIL TP626	1	AD14	NC3
26MIL TP628	1	AD15	NC4
26MIL TP629	1	AD16	NC5
26MIL TP1068	1	AD17	NC6
26MIL TP635	1	AD18	NC7
26MIL TP634	1	AD19	NC8
26MIL TP636	1	AD20	NC9
26MIL TP637	1	AD21	NC10
		AD22	NC11
		AD23	NC12

	NB8X	0.5V Swing	NB8X	3.3V Swing
C1688		10nF		10nF
R2140		76.8 ohm		No Stuff
R2141		No Stuff		No Stuff
R2139		No Stuff		No Stuff

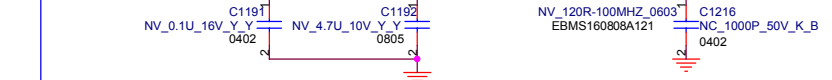
U7B

- AD23 PEX_IOVDD0
- AE24 PEX_IOVDD1
- AE23 PEX_IOVDD2
- AG24 PEX_IOVDD3
- AG25 PEX_IOVDD4
- AG25 PEX_IOVDD5
- AC16 PEX_IOVDDQ0
- AC17 PEX_IOVDDQ1
- AC21 PEX_IOVDDQ2
- AC22 PEX_IOVDDQ3
- AE18 PEX_IOVDDQ4
- AE22 PEX_IOVDDQ5
- AE12 PEX_IOVDDQ6
- AE18 PEX_IOVDDQ7
- AE21 PEX_IOVDDQ8
- AE22 PEX_IOVDDQ9
- AE22 PEX_IOVDDQ10

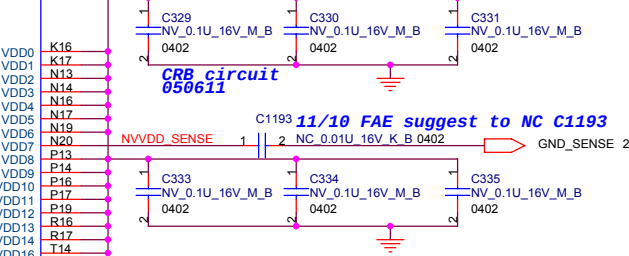
POWER

NV_PLAVDD

45mA(Frame Buffer Analog Power)



19.81A(Internal logic core power)



VDD0

VDD1

VDD2

VDD3

VDD4

VDD5

VDD6

VDD7

VDD8

VDD9

VDD10

VDD11

VDD12

VDD13

VDD14

VDD15

VDD16

VDD17

VDD18

VDD19

VDD20

VDD21

VDD22

VDD23

VDD24

VDD25

VDD26

VDD27

VDD28

VDD29

VDD30

VDD31

VDD32

VDD33

VDD34

VDD35

VDD36

VDD37

NC13

NC14

NC15

NC16

NC17

NC18

NC19

NC20

NC21

NC22

NC23

NC24

NC25

NC26

NC27

NC28

NC29

NC30

NC31

NC32

M5

V4

D31

D1

W4

W5

V5

Y6

F6

G8

G23

A28

F1

A26

W3

NC28

NC29

TP618

TP617

TP620

TP623

TP625

TP627

TP631

TP630

TP633

TP586

TP587

TP590

TP955

TP956

TP955

TP956

TP955

TP956

TP955

NB8X: 9/18 change power rail from PEX_VDD to NV_VDD

Place close to L102

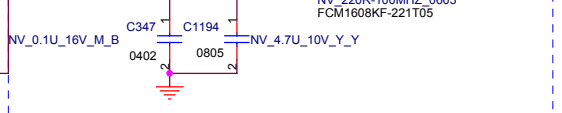
NB8X 1.2V

CRB circuit 050611

11/10 FAE suggest to NC C1193

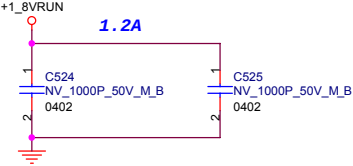
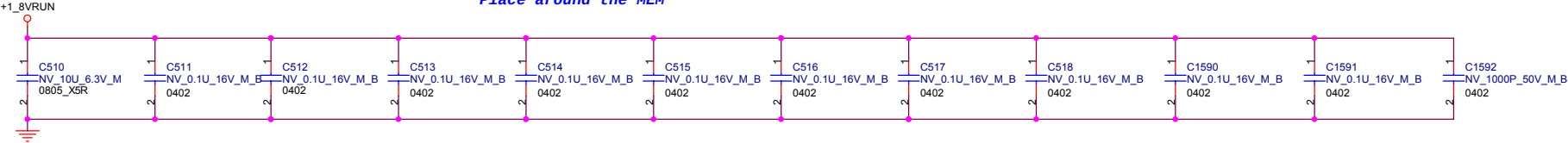
H_PLLVDD is new power rail for NB8M

15mA(Power rail)



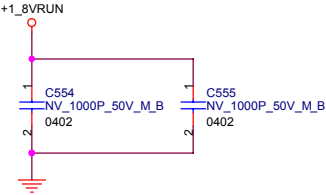
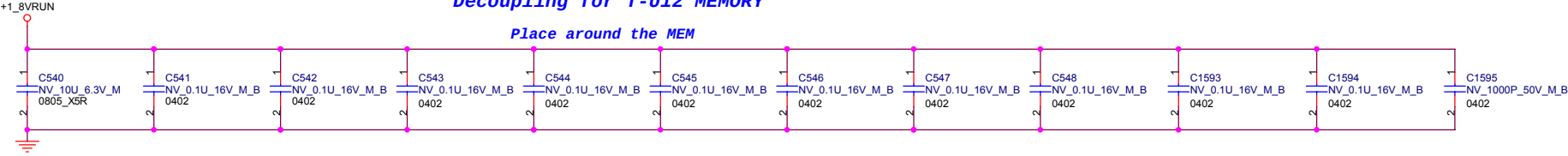
Decoupling for T-U11 MEMORY

Place around the MEM



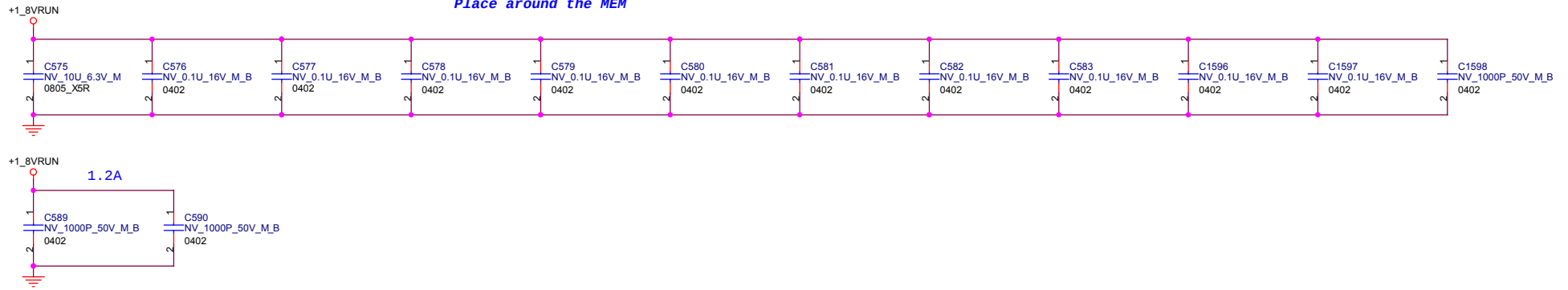
Decoupling for T-U12 MEMORY

Place around the MEM



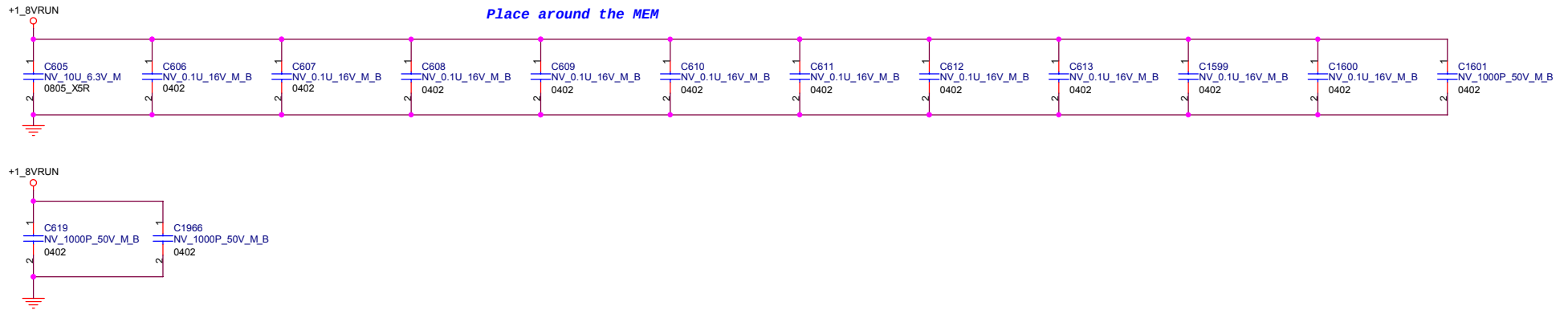
Decoupling for T-U13 MEMORY

Place around the MEM



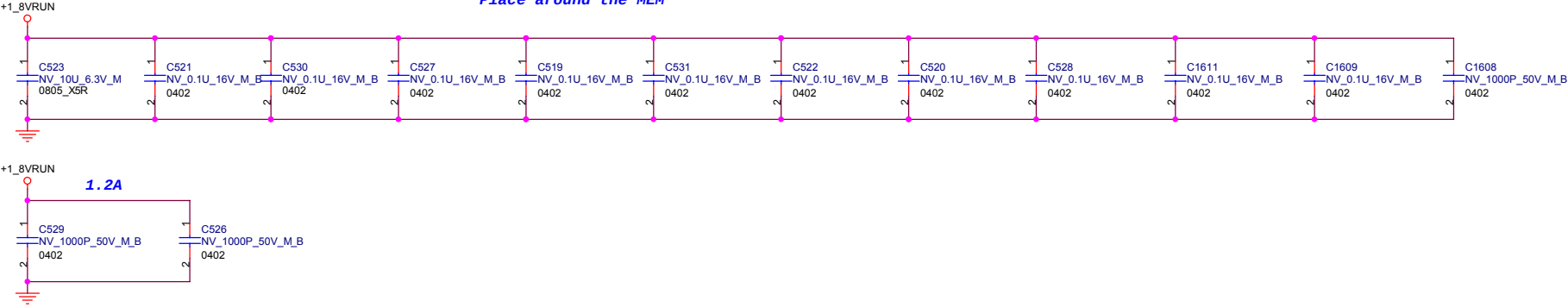
Decoupling for T-U14 MEMORY

Place around the MEM



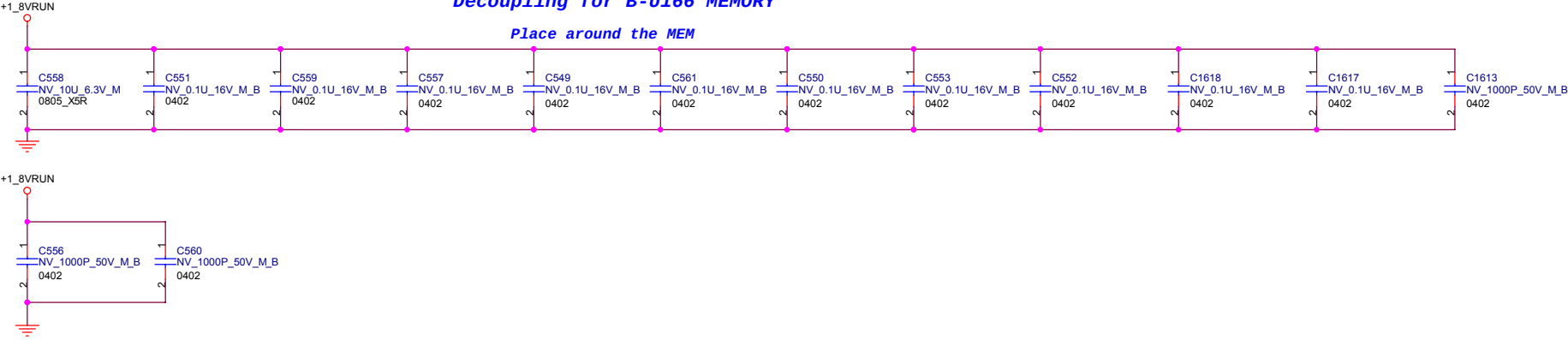
Decoupling for B-U165 MEMORY

Place around the MEM



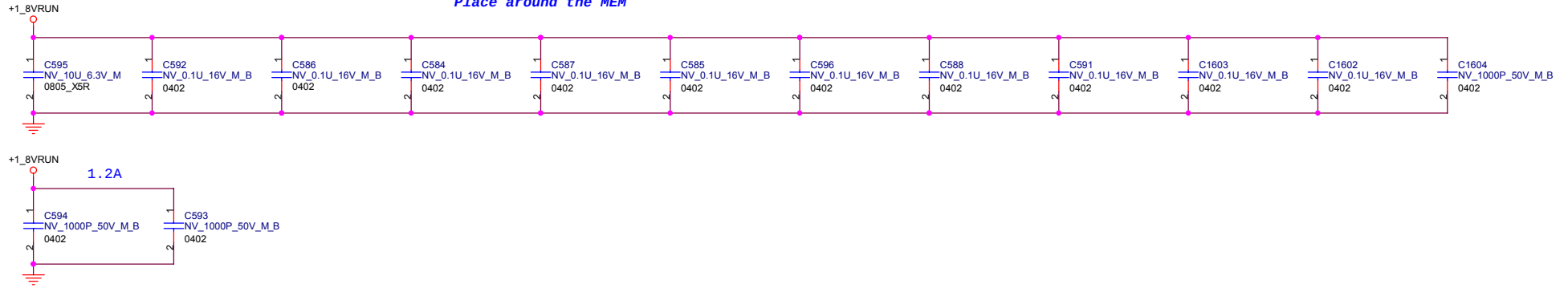
Decoupling for B-U166 MEMORY

Place around the MEM



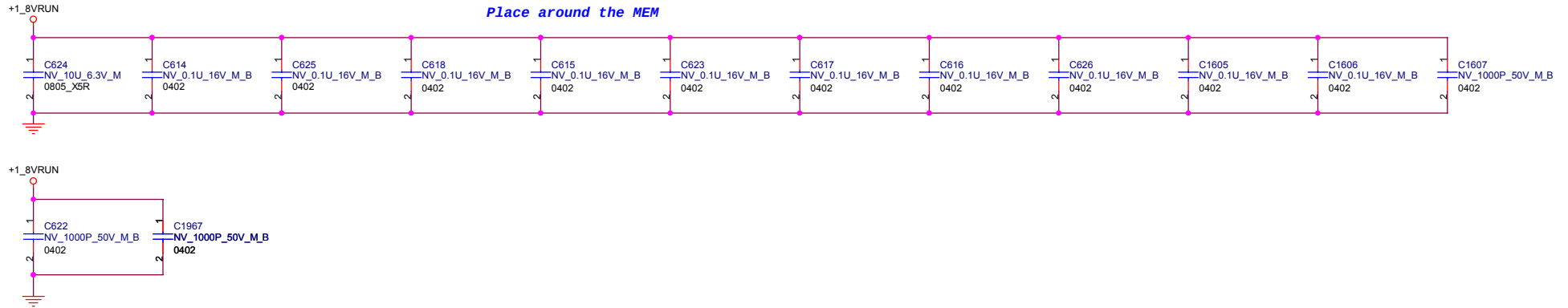
Decoupling for B-U167 MEMORY

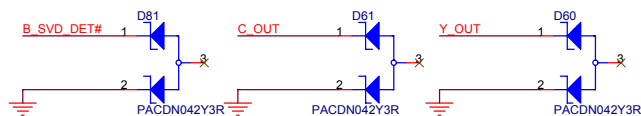
Place around the MEM



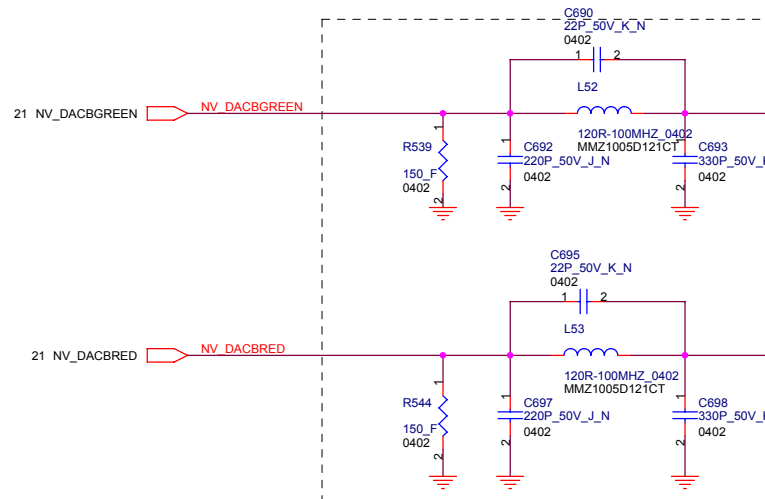
Decoupling for B-U168 MEMORY

Place around the MEM

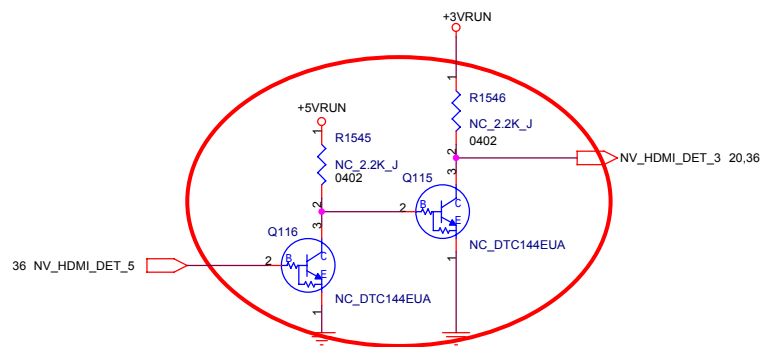
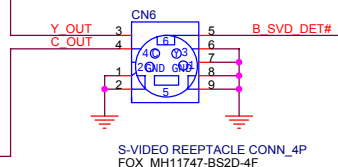




These compoent close to S-Video connector within 700 mil

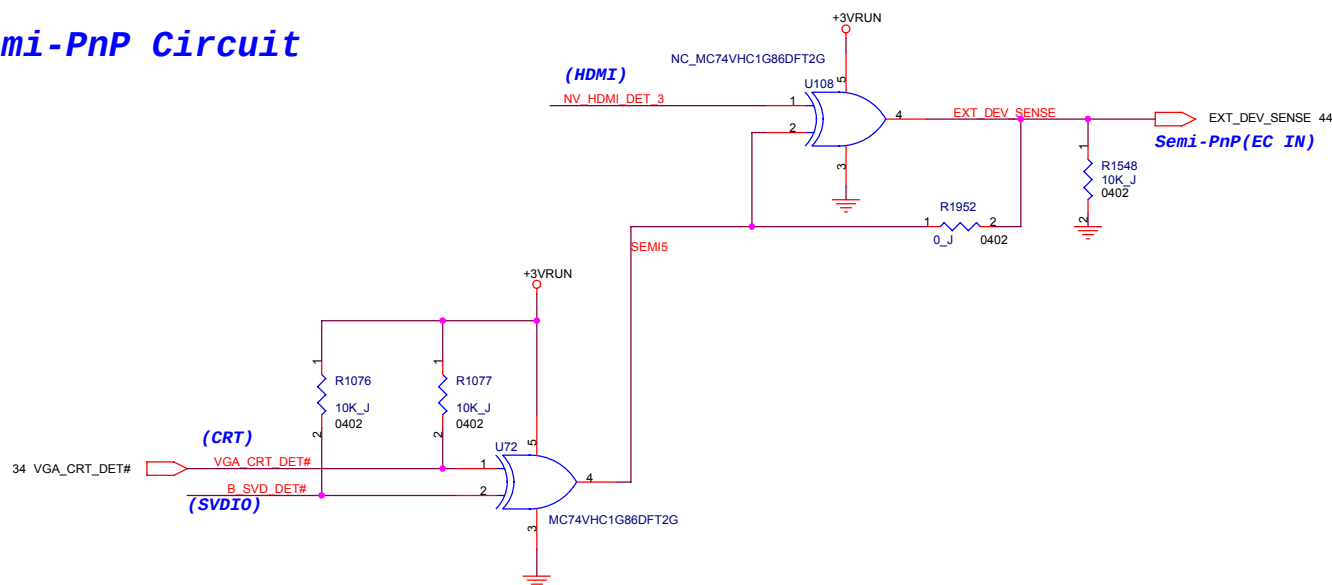


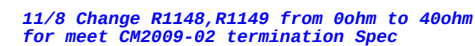
S-VIDEO CONNECTOR



PS101 HPD has level shift function, so backup this circuit
Change Q115,Q116,R1545,R1546 to NC

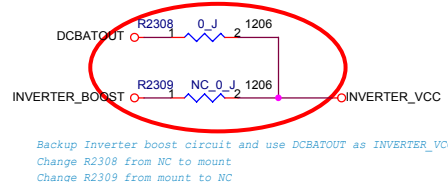
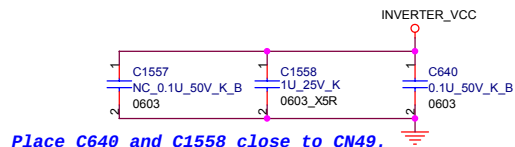
Semi-PnP Circuit



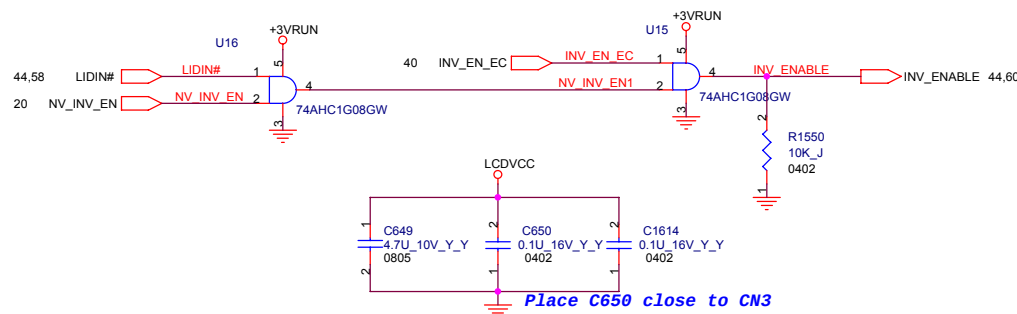


LVDS CONNECTOR

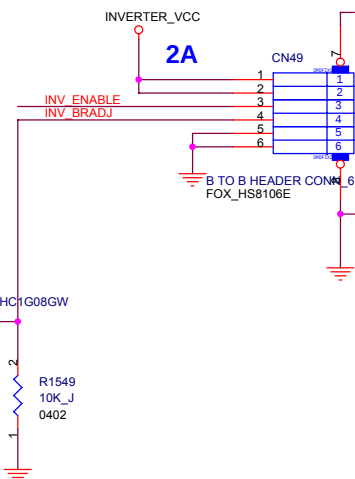
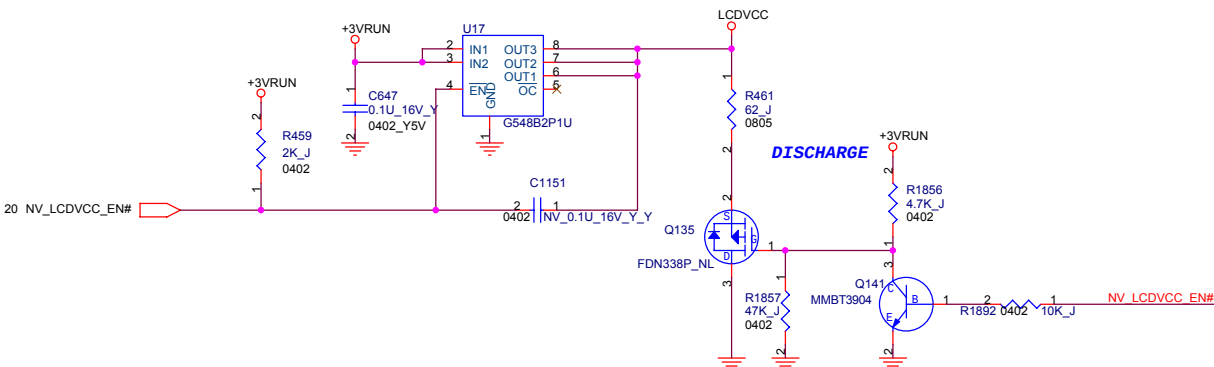
INVERTER CONNECTOR



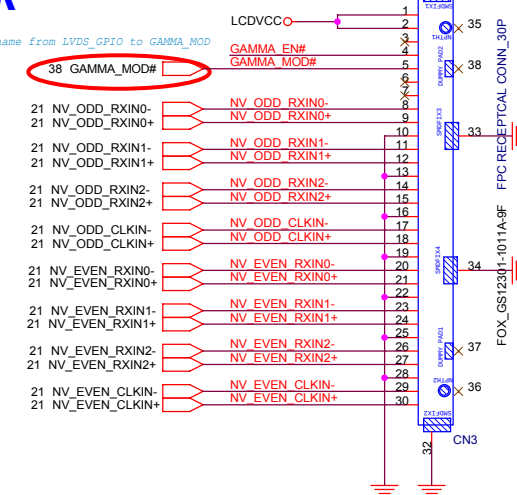
U106, U15, U16 can use ON (MC74VHC1G08DFT2G)
H.H. PN:14-MC74VHC-1G04



Current limit is from 1.1A to 2.1A.



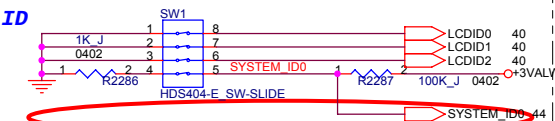
Change net name from LVDS_GPIO to GAMMA_MOD



Use H/W selection to enable GAMMA function.
Change R1937, R1938 from 4.7K to 0ohm

H: GAMMA Disable
L: GAMMA Enable

PANEL ID



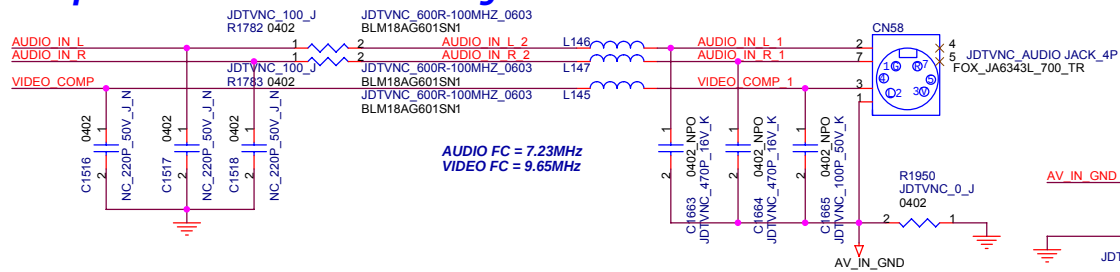
Add R2286, R2287 for Instant On function been used again

Type	WXGA+	WXGA+	WUXGA	WUXGA
Size	17" wide	17" wide	17" wide	17" wide
Vender	LG.PHILIPS	LG.PHILIPS	SHARP	SHARP
Device Name	LP171WP74-TLA1	LP171WP7-TLA1	LQ170M11LA4G	LQ170M11LA4B
Panel ID Check[2..0]	010	001	100	101

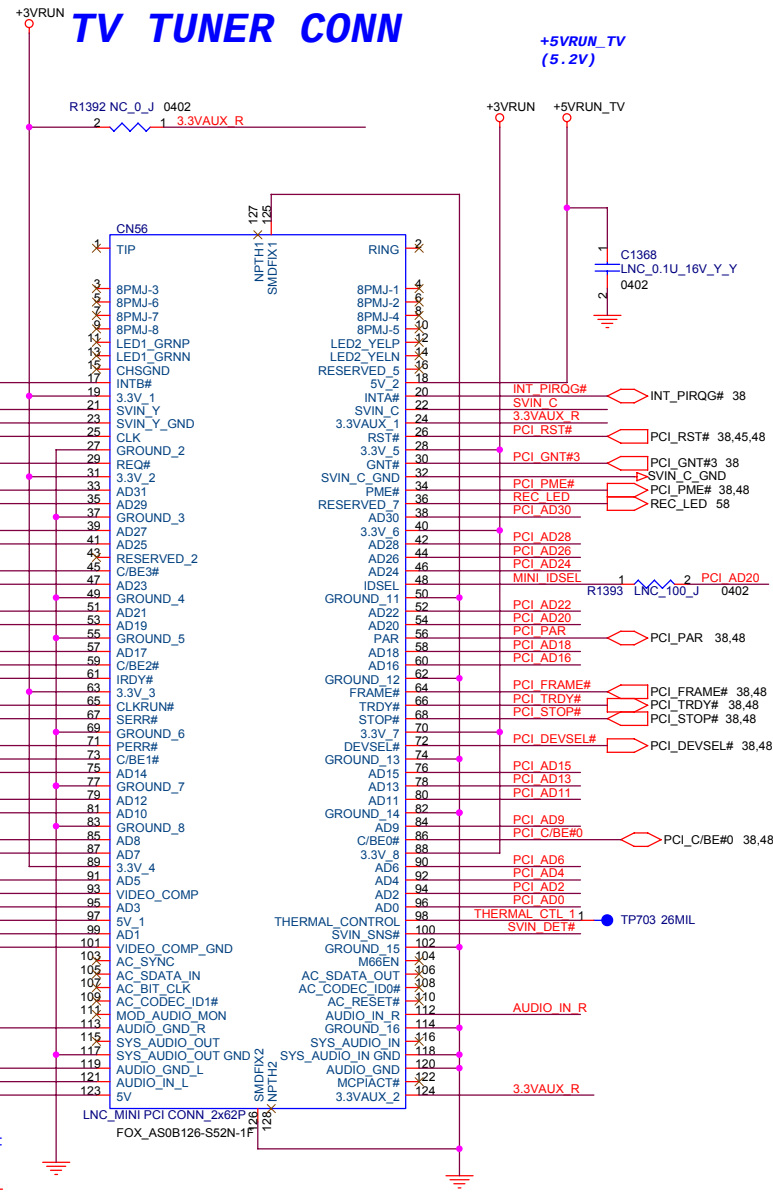
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title	LVDS
Size	Document Number
A3	(M610-1-01) MainBoard (MBX-176) 2007.1.4
Date:	Friday, August 31, 2007
Sheet	35 of 81

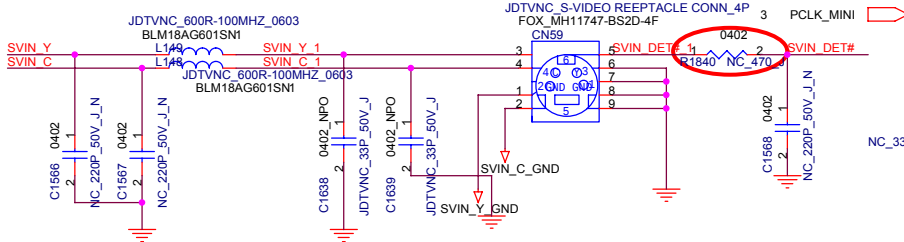
Special mini stereo jack



TV TUNER CONN

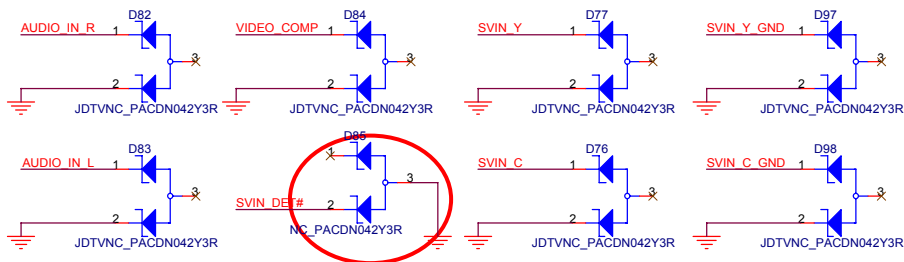


S-VIDEO IN



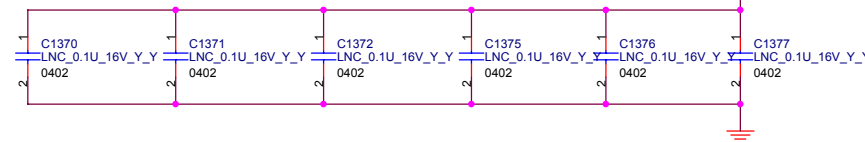
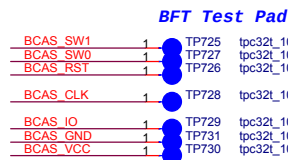
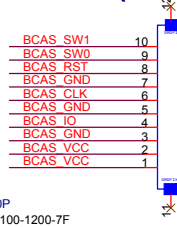
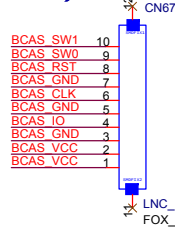
TV-TUNER not support CLKRUN

TV tuner "SVIN_DET#" signal no use.
Change R1840,D85 to NC



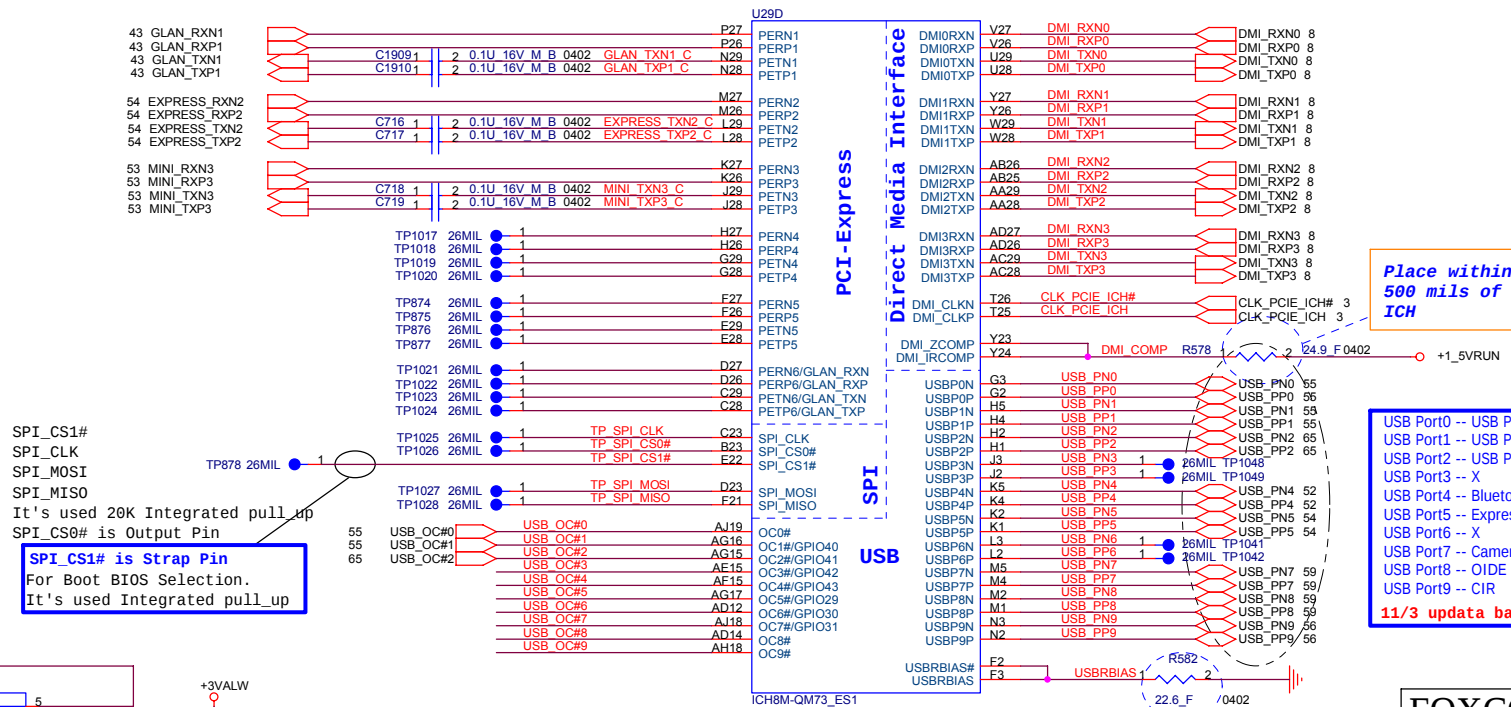
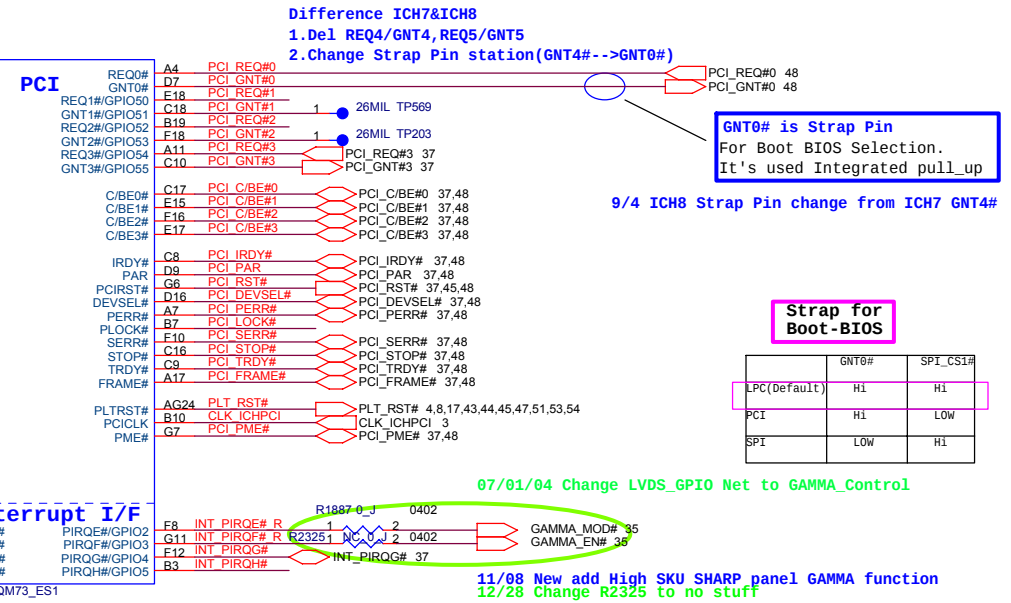
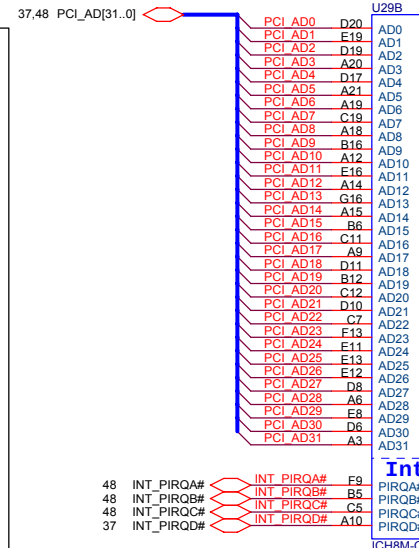
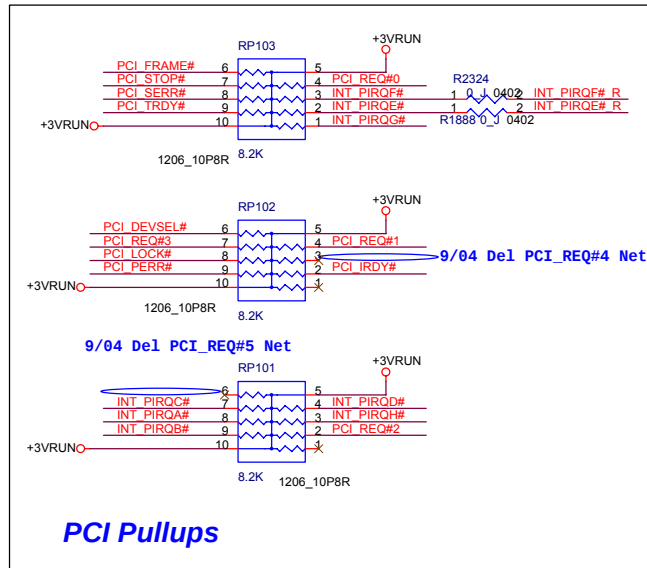
B-CAS connector (Close to TV Tuner)

FFC CONNECT TO TV TUNER BOARD (FOR JP DIAGITAL)



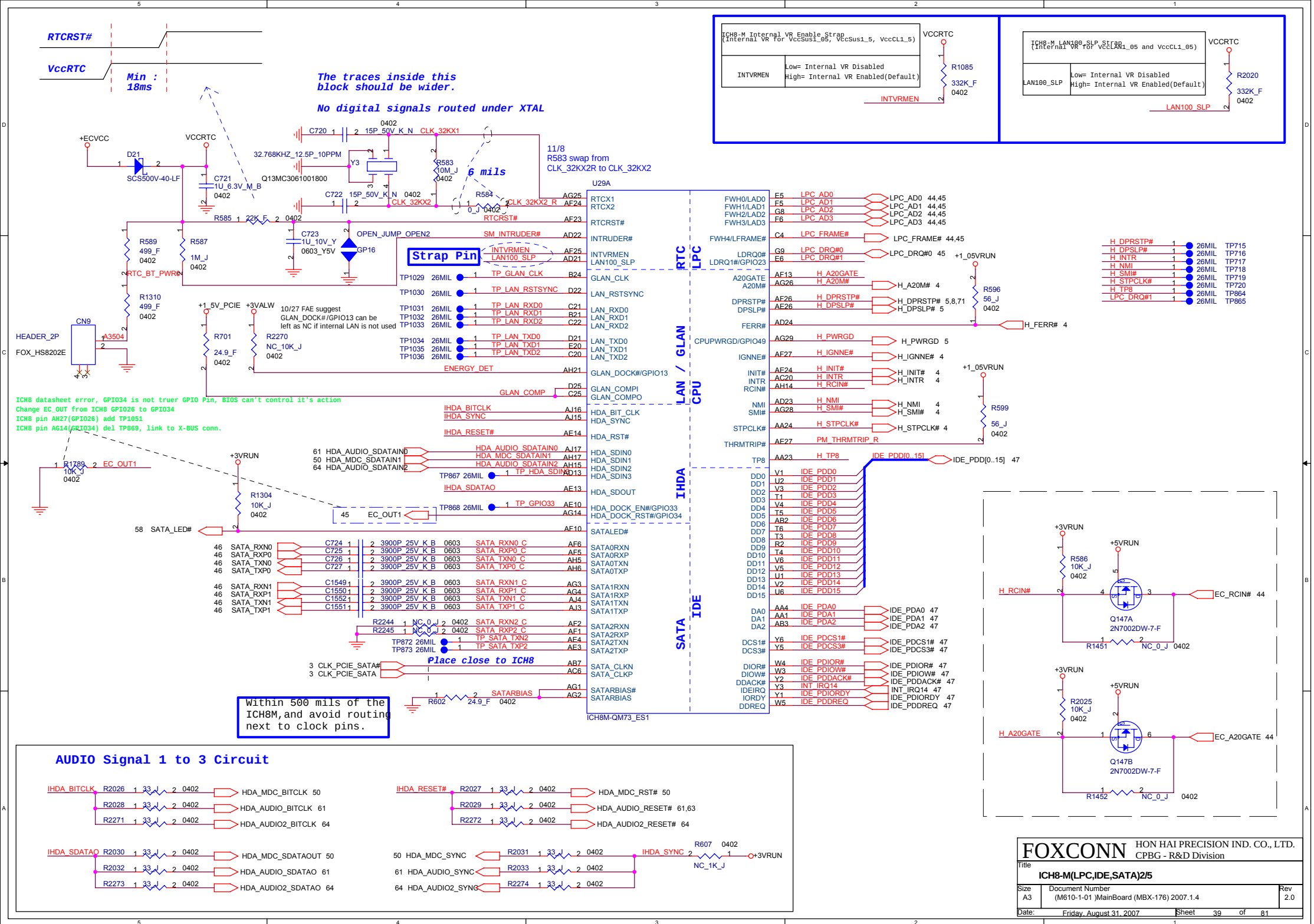
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

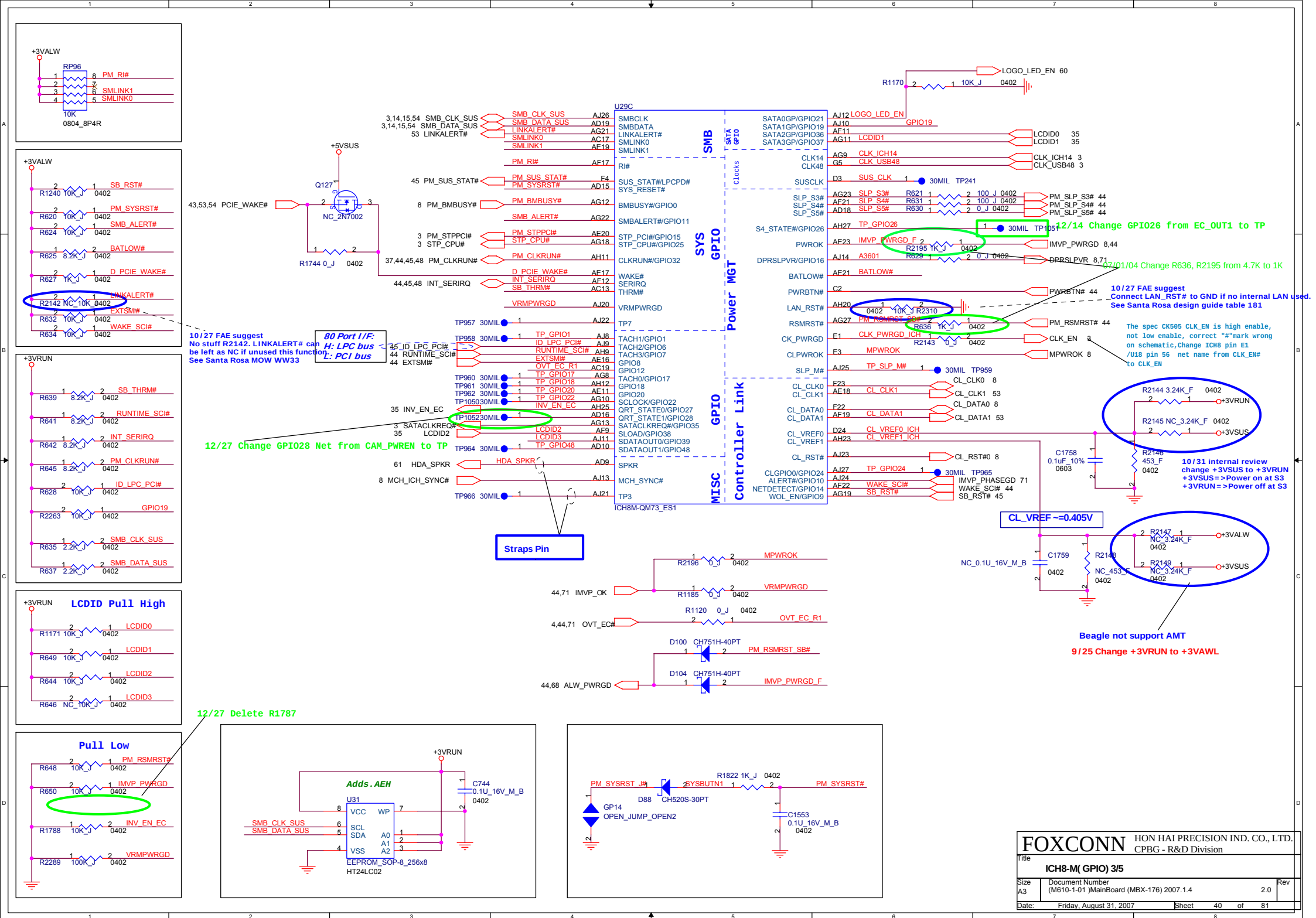
Title		
MINI-PCI CONN.		
Size	Document Number	Rev
A3	(M610-1-01) MainBoard (MBX-176) 2007.1.4	2.0
Date:	Friday, August 31, 2007	Sheet 37 of 81

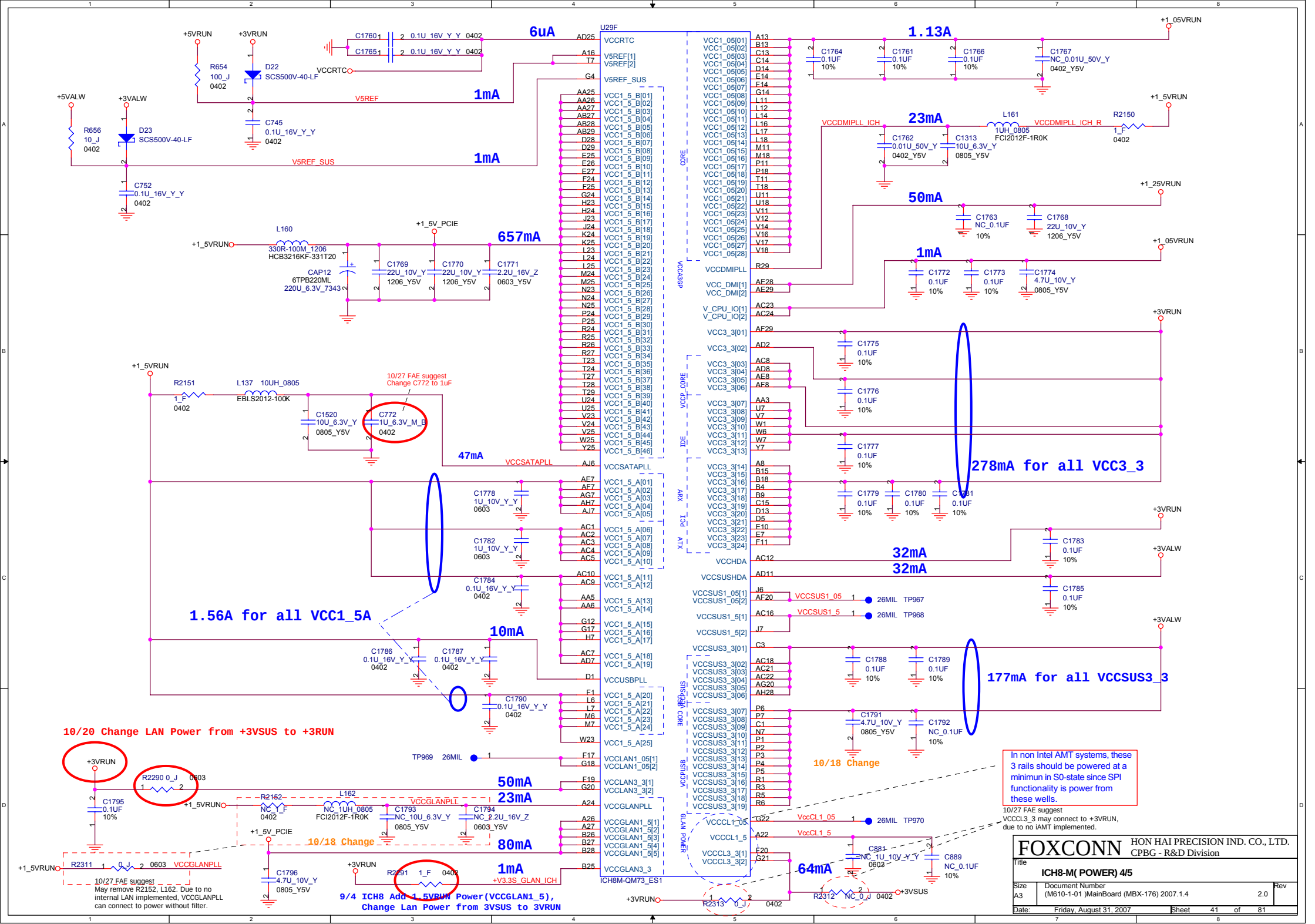


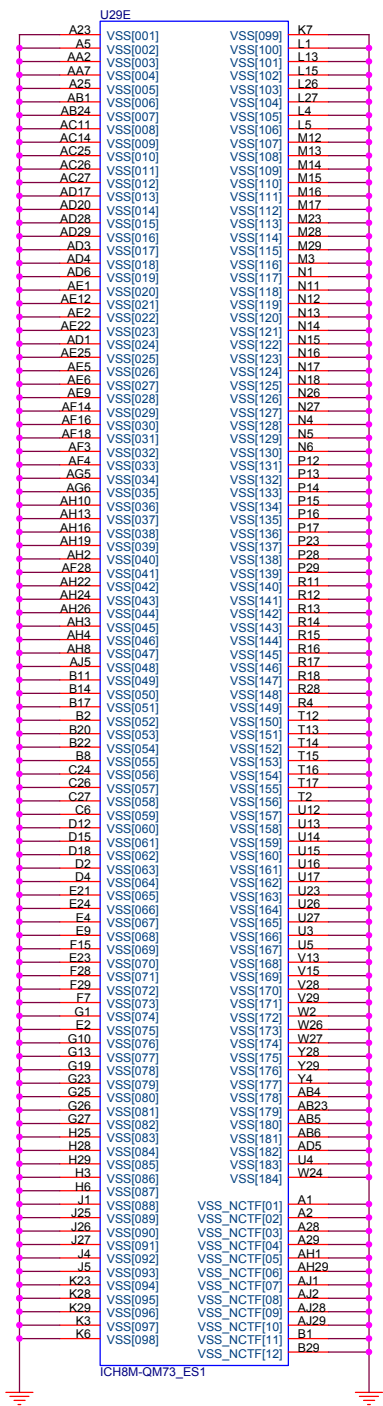
USB Port0 -- USB Port0
USB Port1 -- USB Port1
USB Port2 -- USB Port2(Audio Board)
USB Port3 -- X
USB Port4 -- Bluetooth
USB Port5 -- Express Card
USB Port6 -- X
USB Port7 -- Camera (10/26 modify)
USB Port8 -- OIDE
USB Port9 -- CIR

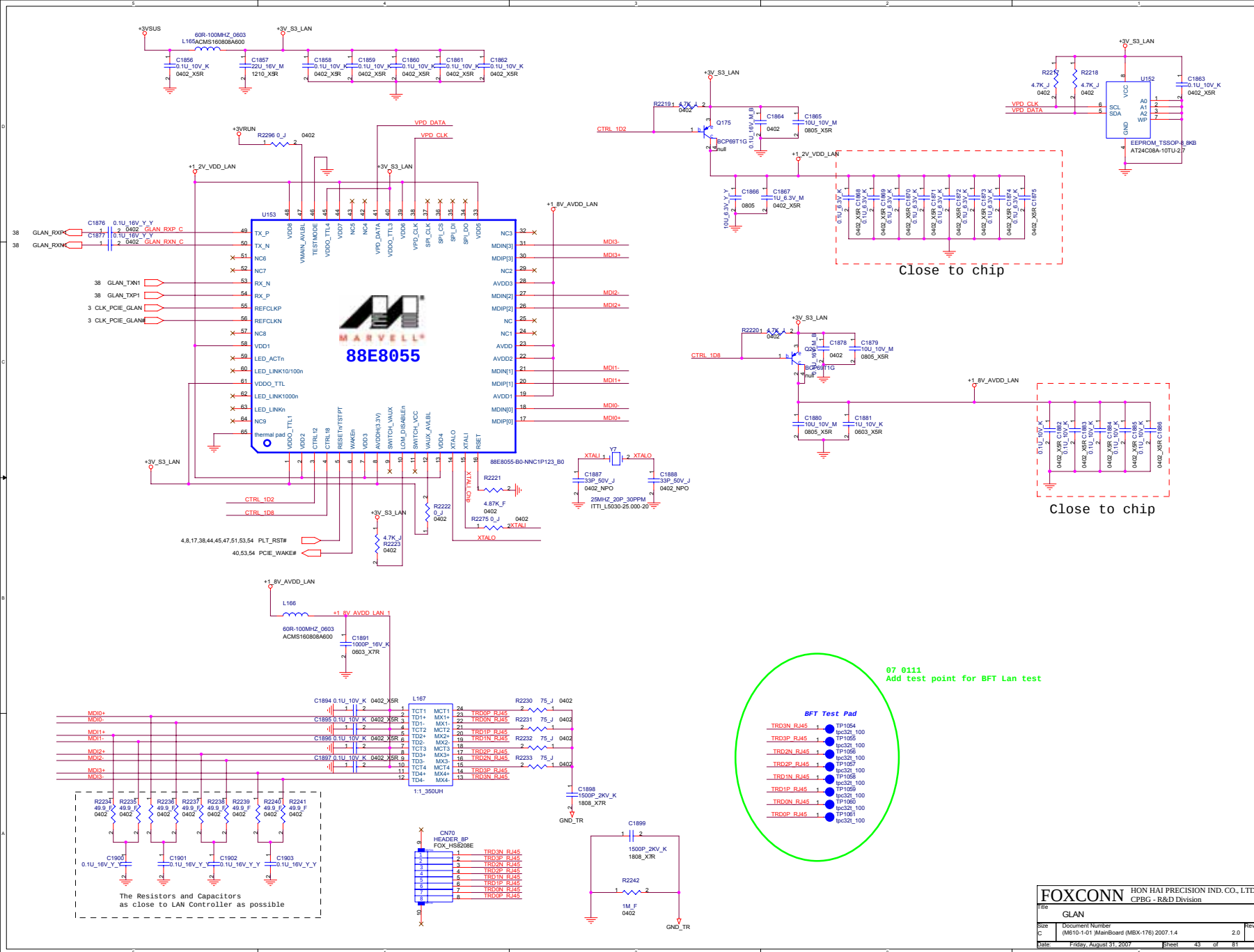
11/3 updata base on MOR side suggest

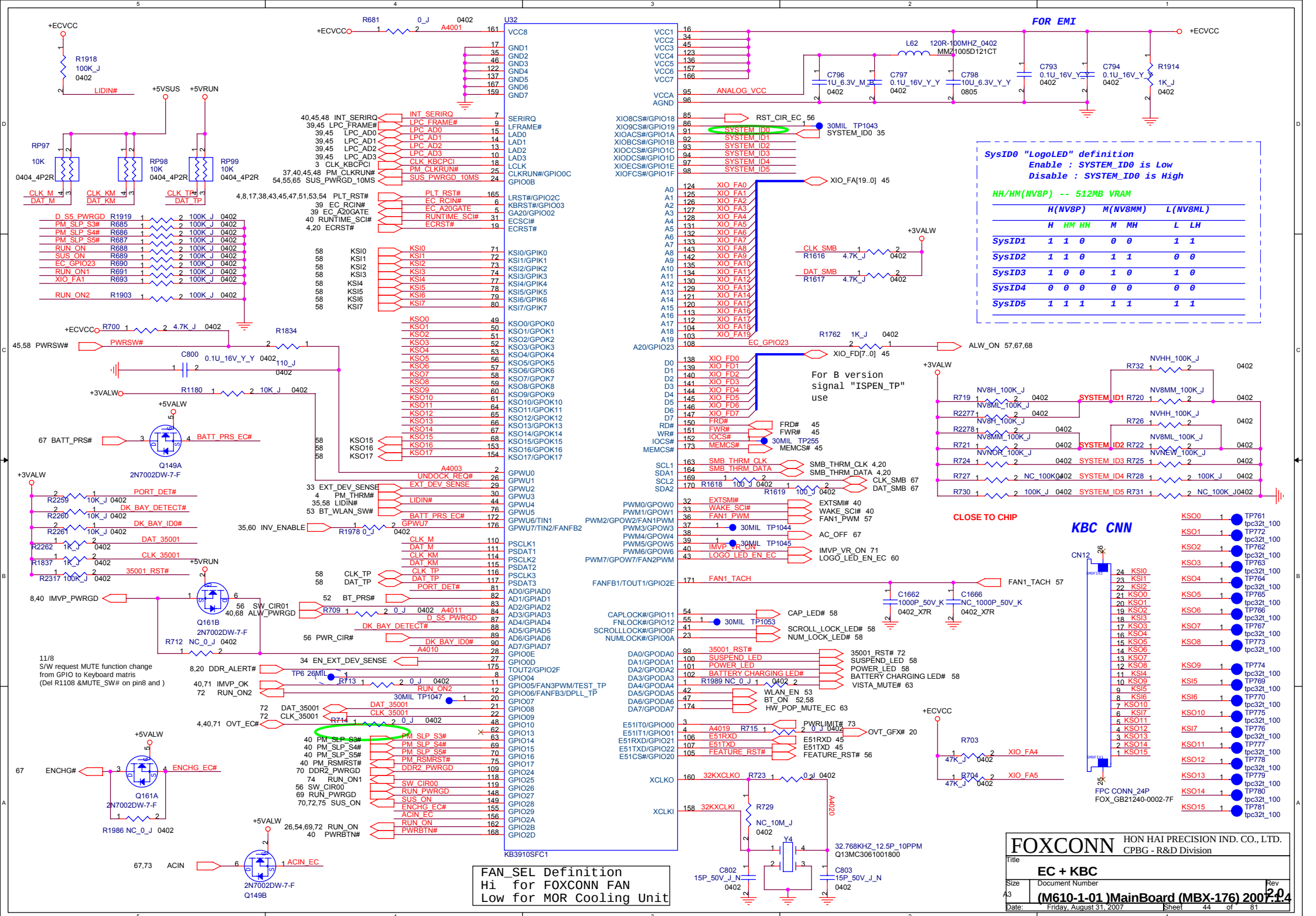












SysID0 "LogoLED" definition
Enable : SYSTEM_ID0 is Low
Disable : SYSTEM_ID0 is High

HH/HM(NV8P) -- 512MB VRAM

	H(NV8P)		M(NV8MM)		L(NV8ML)	
	H	HM	H	HM	L	LH
SysID1	1	1	0	0	0	1
SysID2	1	1	0	1	1	0
SysID3	1	0	0	1	0	1
SysID4	0	0	0	0	0	0
SysID5	1	1	1	1	1	1

CLOSE TO CHIP

KBC CNN

FAN_SEL Definition
Hi for FOXCONN FAN
Low for MOR Cooling Unit

FOXCONN

HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title

EC + KBC

Size

Document Number

A3

(M610-1-01) MainBoard (MBX-176) 2007.2.4

Date:

Friday, August 31, 2007

Rev

2.0

Sheet

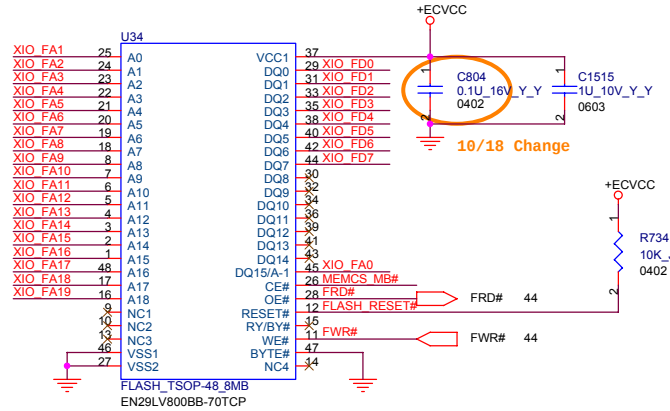
44

of

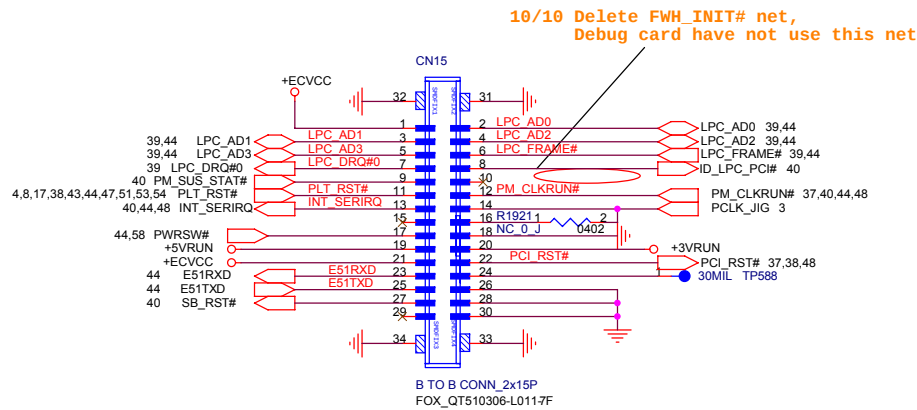
81

FLASH BIOS

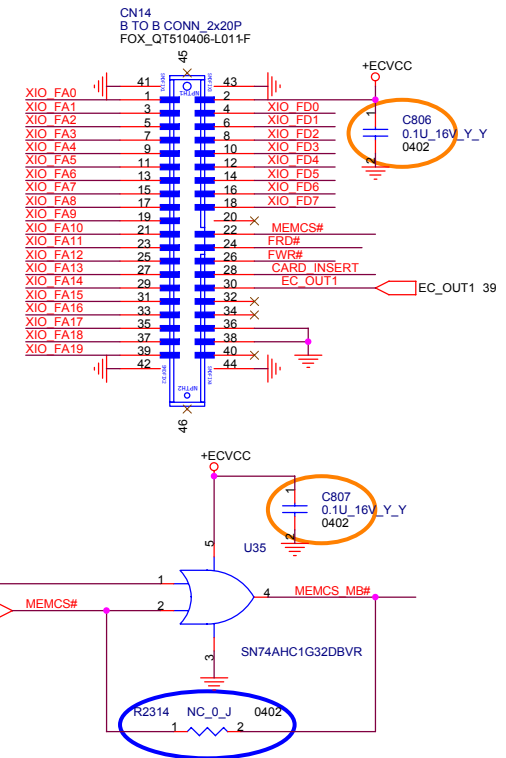
44 XIO_FA[19..0]
44 XIO_FD[7..0]

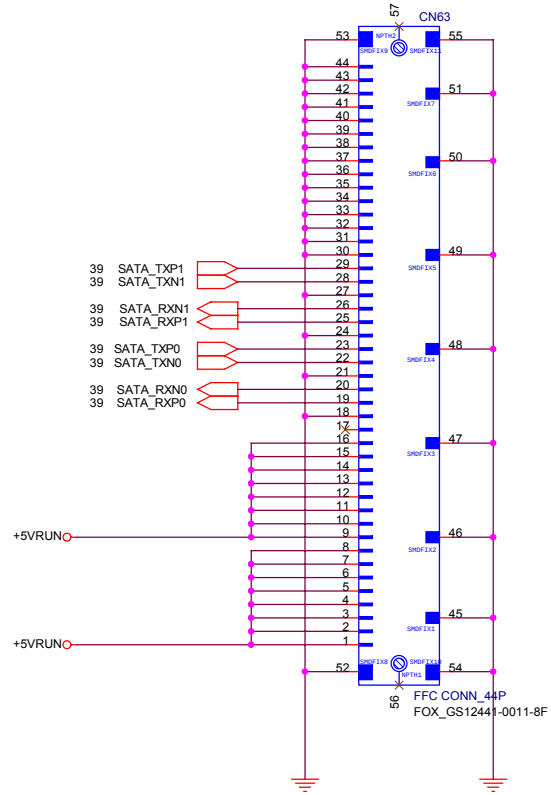
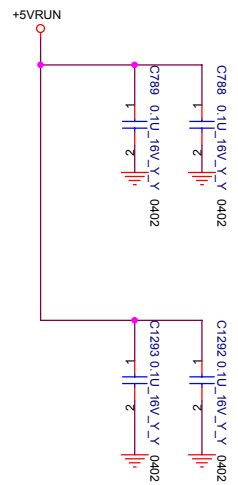


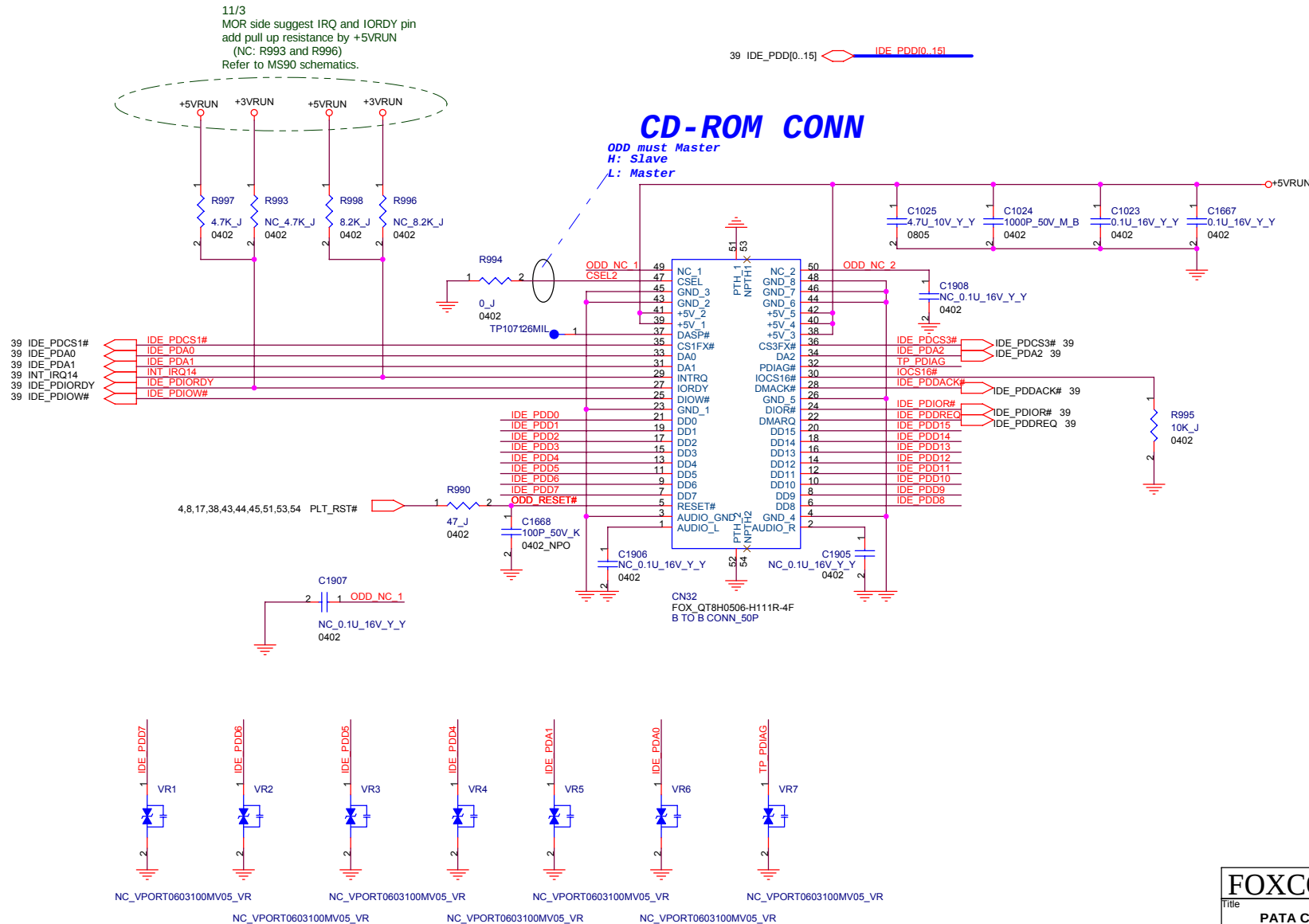
JIG-120

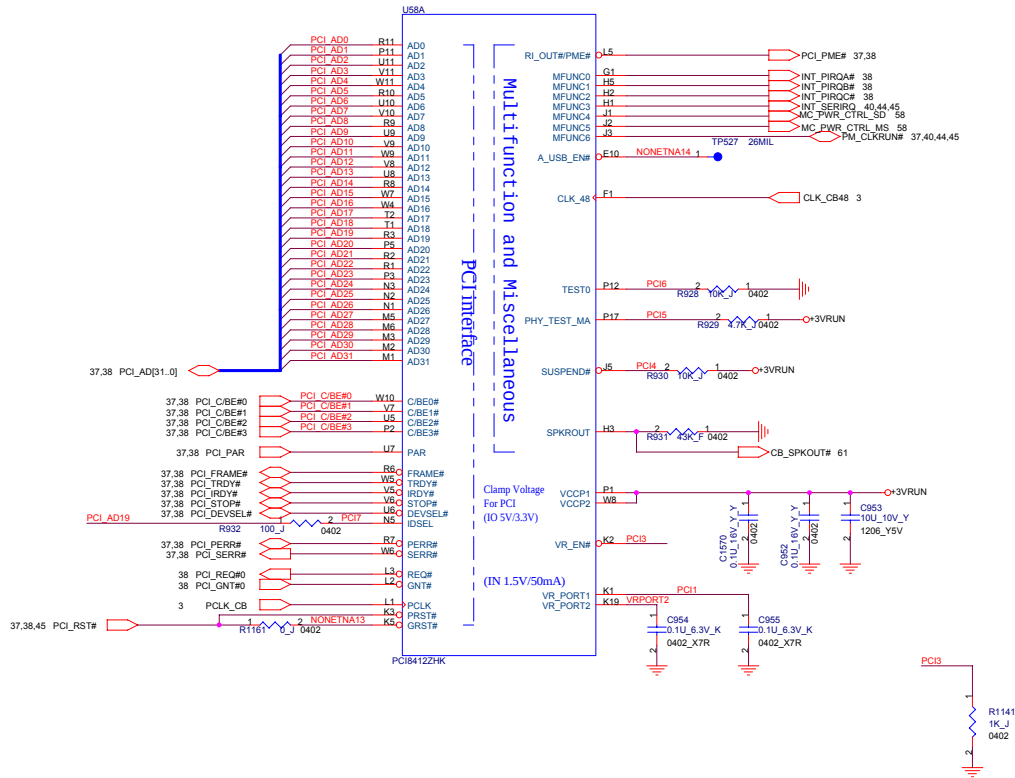


X-BUS







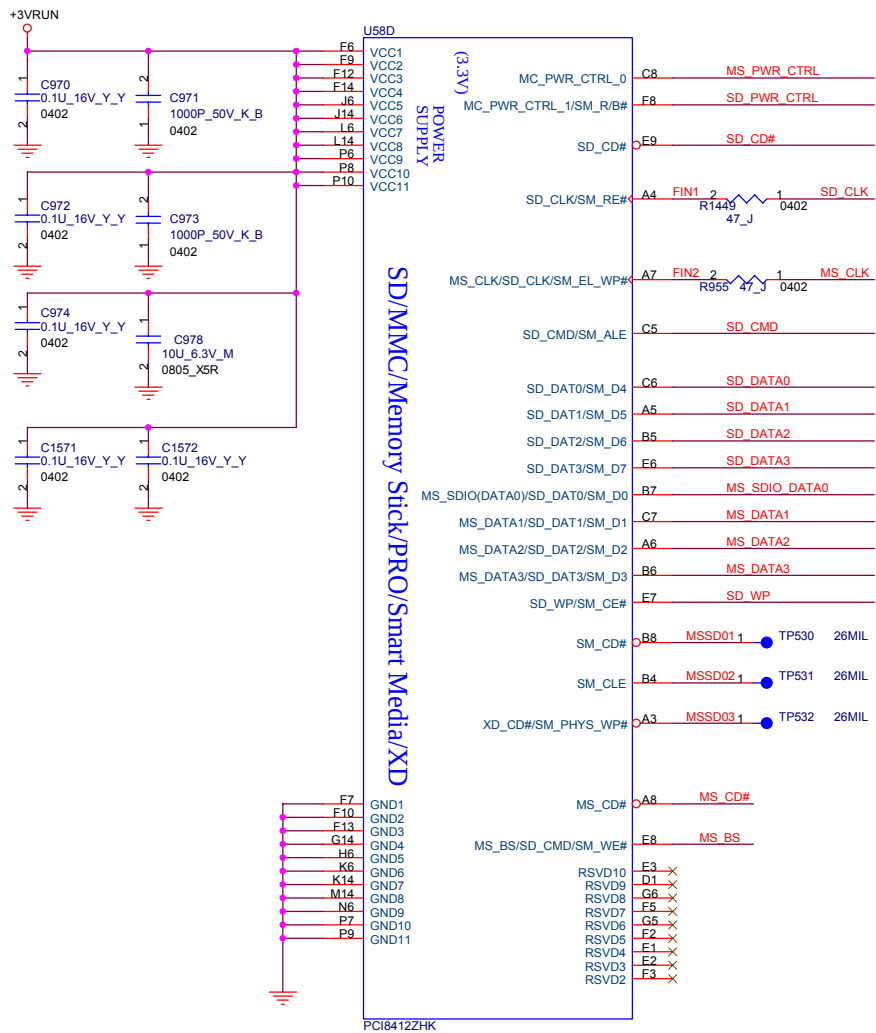


FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title			
PCI (PCI BUS)			
Size	Document Number		Rev
Custom	(MS10-1-01) MainBoard (MBX-176) 2007.1.4	2.0	
Date:	Friday, August 31, 2007	Sheet	48 of 61

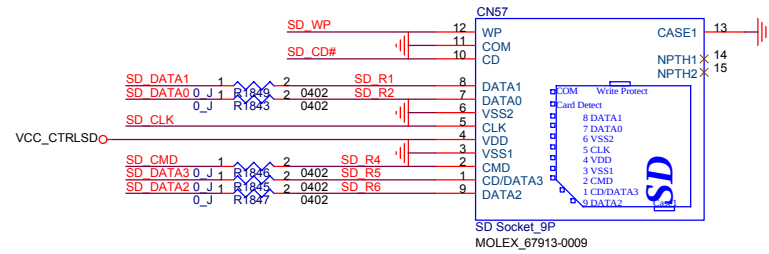


Place near PCI7412.

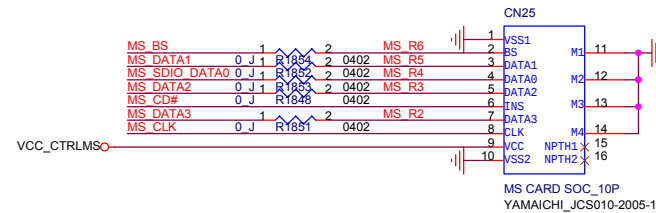
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title PCI (ILINK)			
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.14		Rev 2.0
Date:	Friday, August 31, 2007	Sheet 49 of 81	



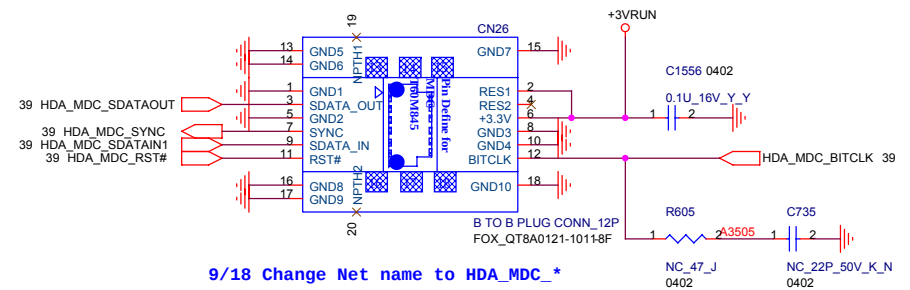
SD CONN.



MS STD/DUO CONN.

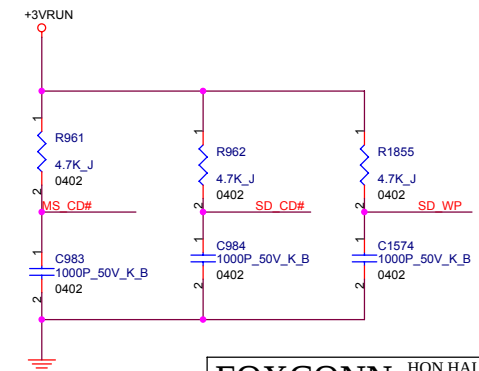
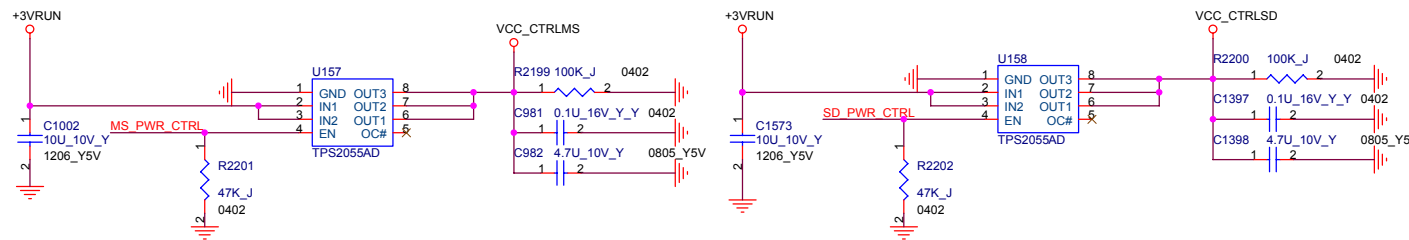


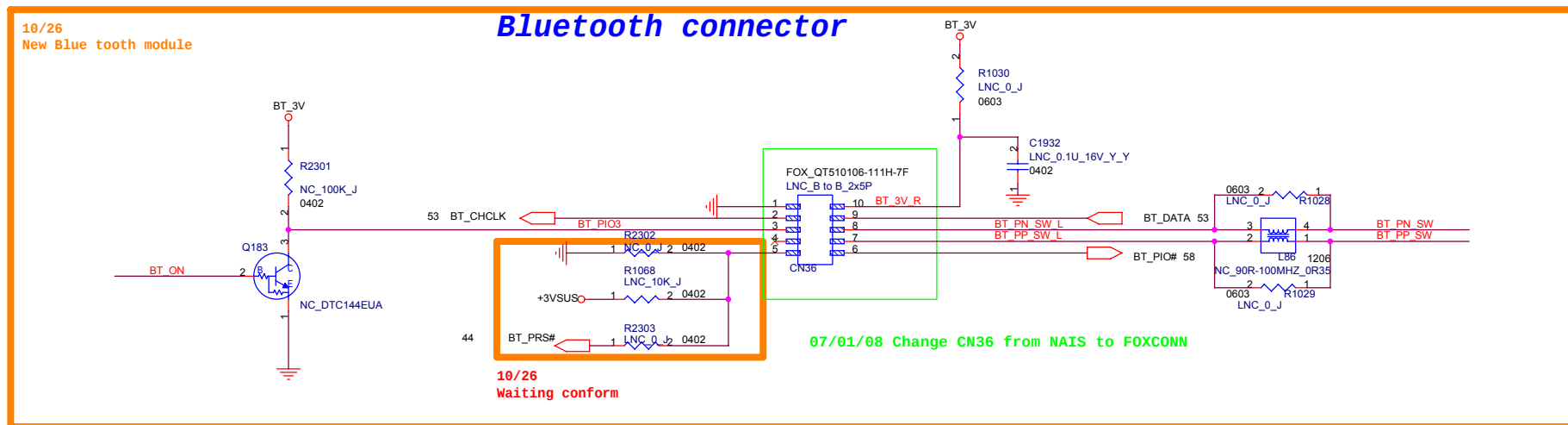
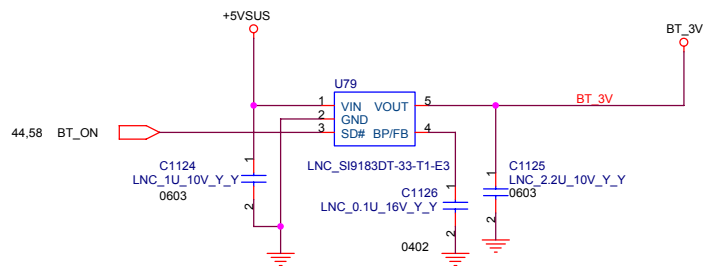
MDC CONN.



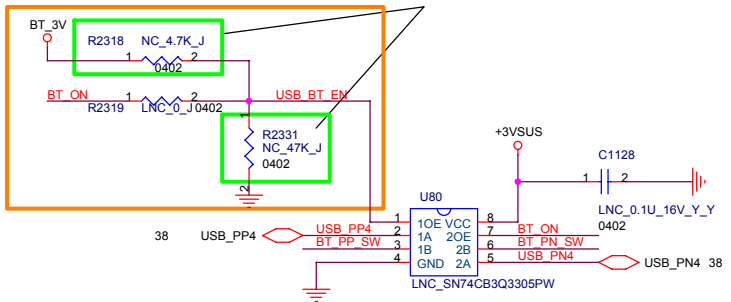
9/18 Change Net name to HDA_MDC_*

02/12/07 PVT Change MS Power switch to TPS2055

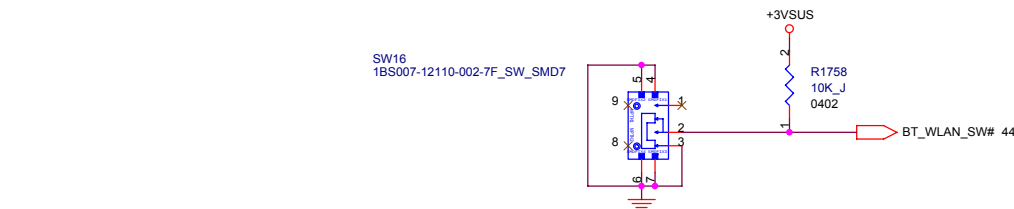




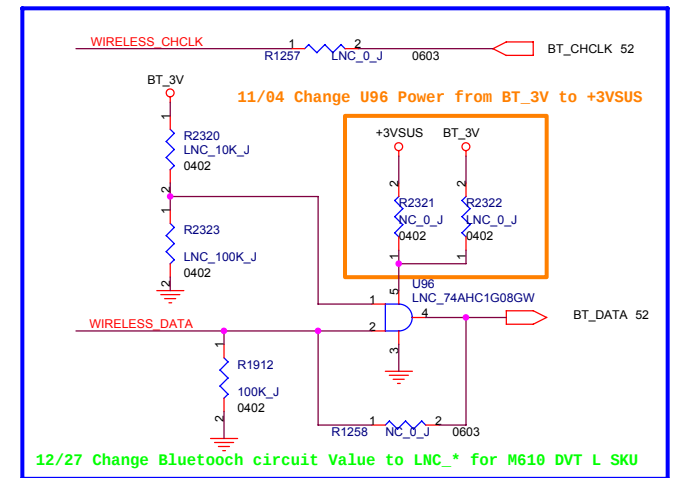
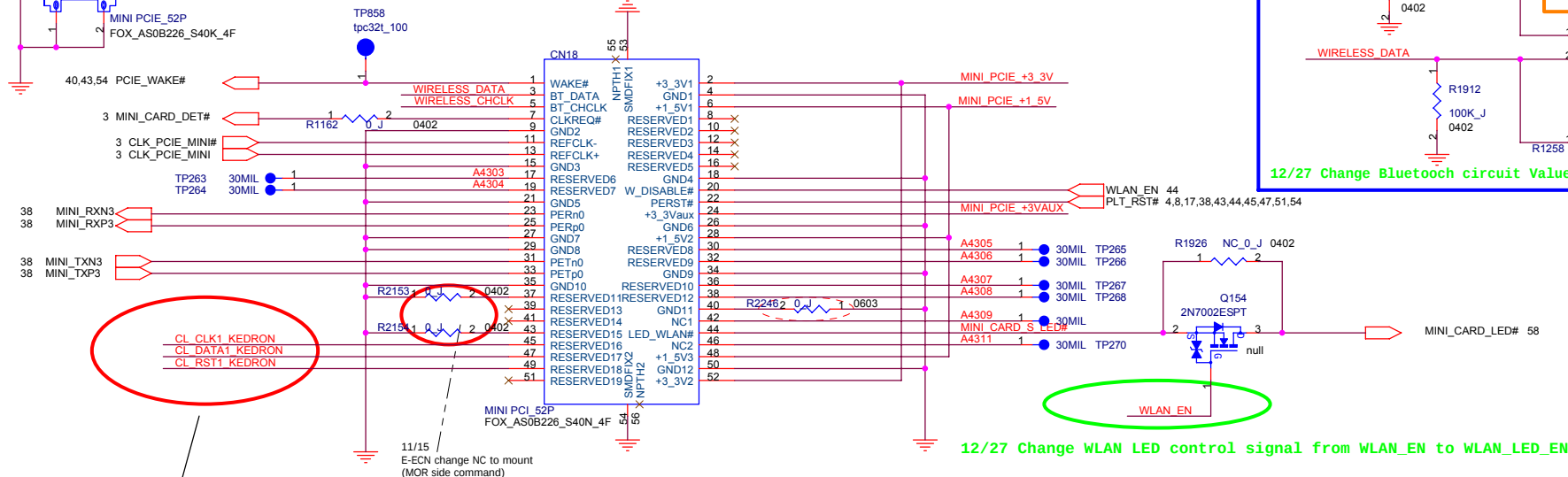
- 11/04 Change U80 Enable from BT_ON to BT_3V
- U79 LDO Ton Max is 1000us
- U80 BUS Switch Ton Max is 5ns
- 12/27 Change Bluetooth circuit Value to LNC_* for M610 DVT L SKU
- 12/14 Change R2318 from 1K to 4.7K, Add one 47K pull up resistance



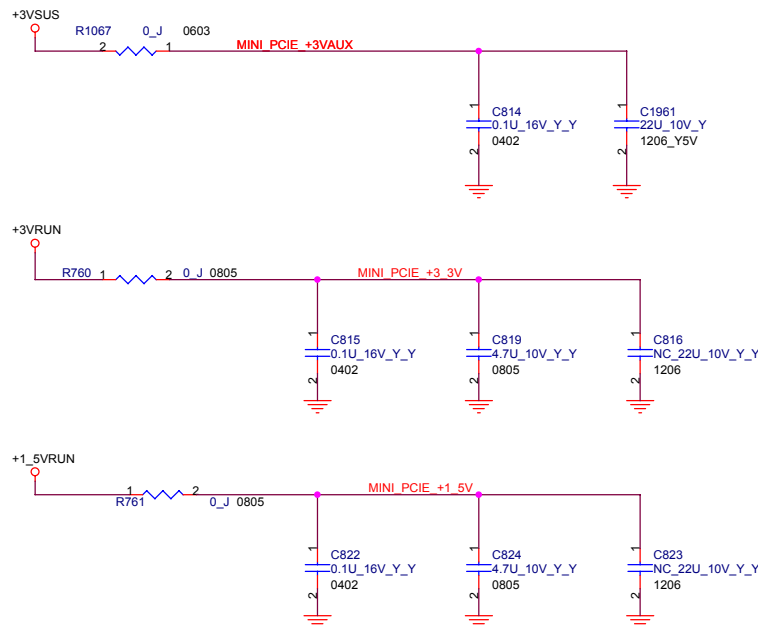
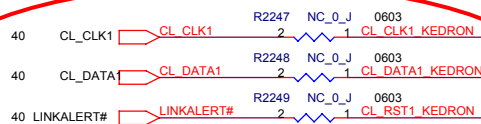
To solve U80 enable pin (net name USB_BT_EN) floating during U79 (BT_3V from LDO) BT_ON disable, Add Pull low 47K(R2331) at net USB_BT_EN, Change R2318 from 10K to 1K.



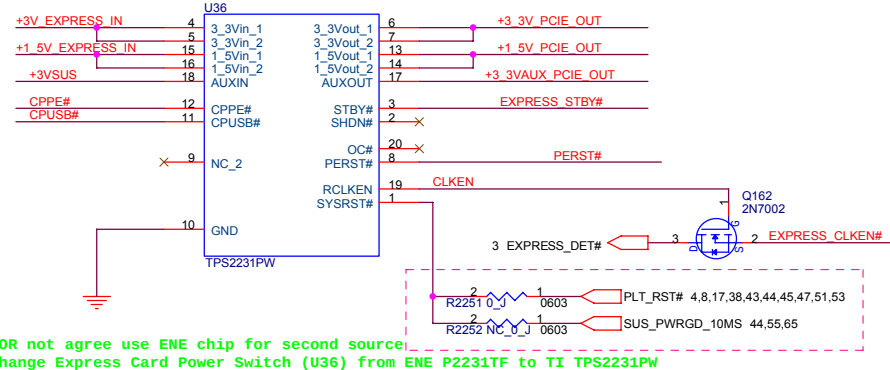
Mini-PCIE Card connector



10/27 FAE suggest
CL_CLK1/CL_DATA1/CL_VREF1 can be left as NC if unused iAMT. Don't need to connect to WLAN card.

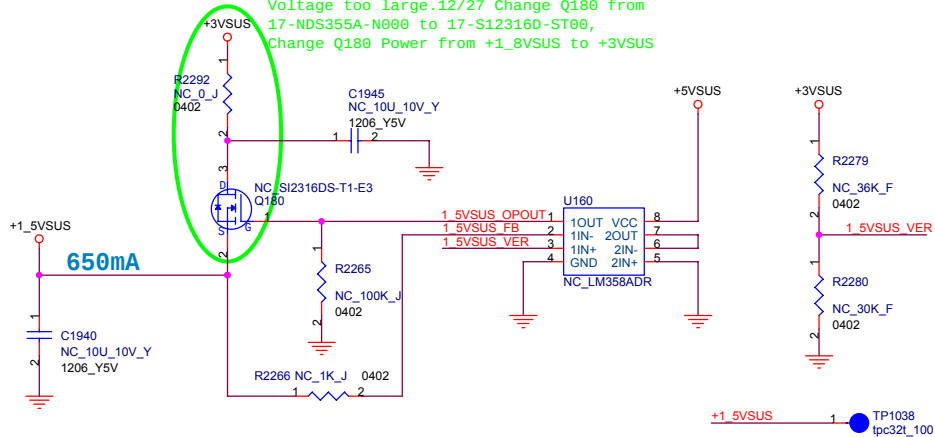


VOLTAGE INPUTS ⁽¹⁾			LOGIC INPUTS			VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

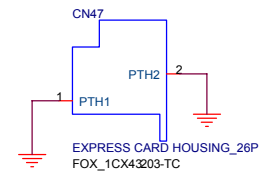
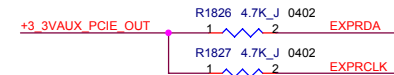
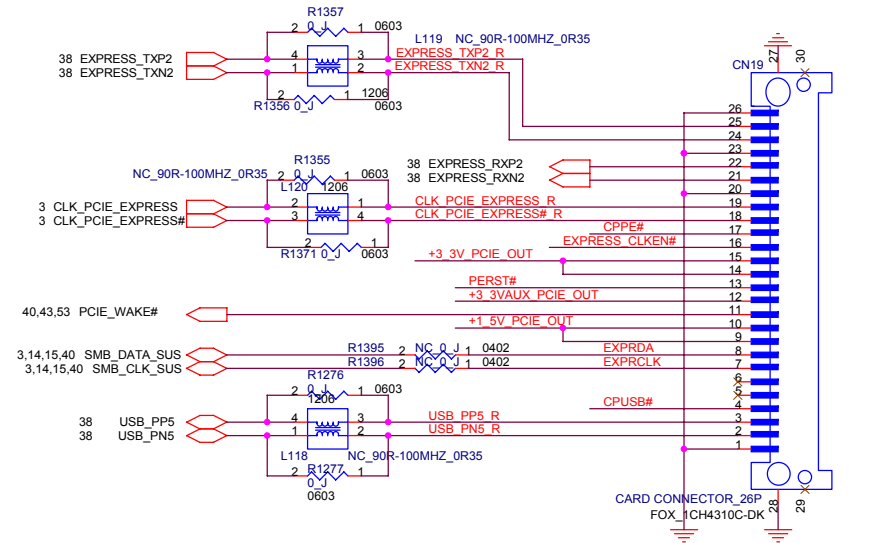


Constant-voltage +1_5VSUS

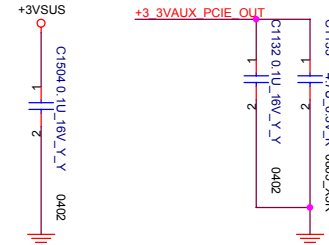
12/29 Load current test fial, 1.8V transfer 1.5V drop
Voltage too large.12/27 Change Q180 from
17-NDS355A-N000 to 17-S12316D-ST00,
Change Q180 Power from +1_8VSUS to +3VSUS



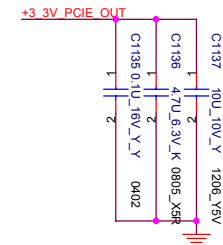
EXPRESS Card



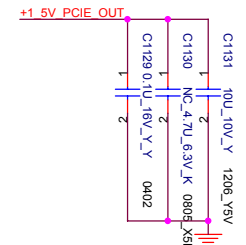
Supply Max 275mA



Supply Max 1300mA

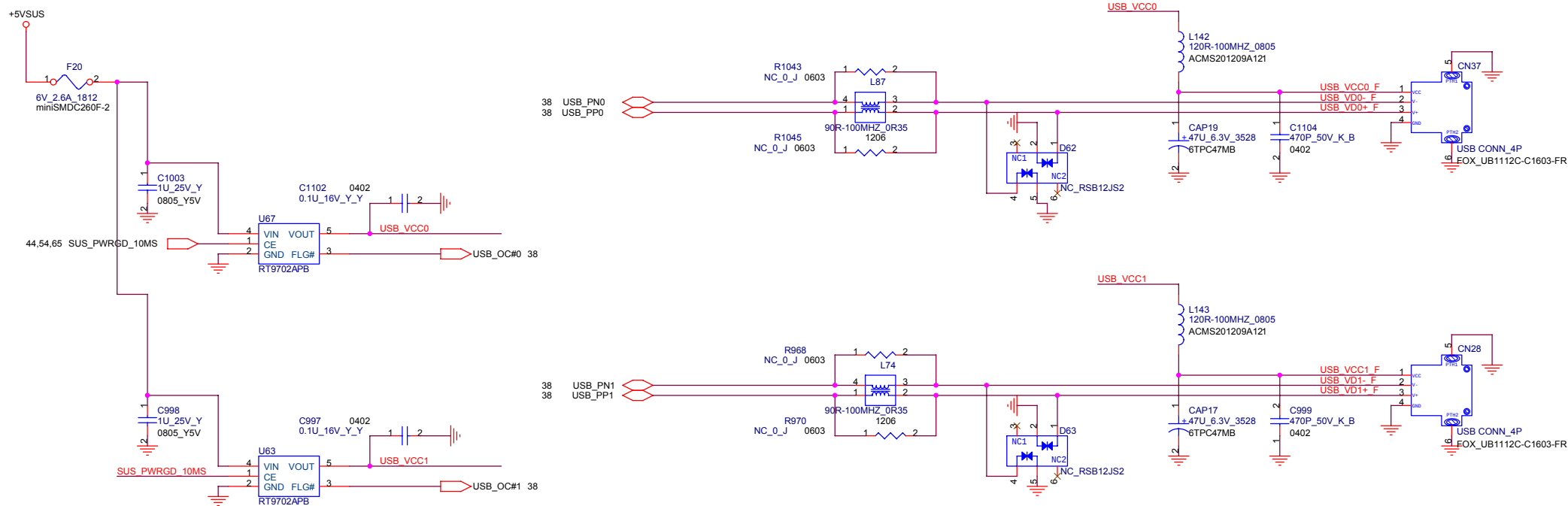


Supply Max 650mA

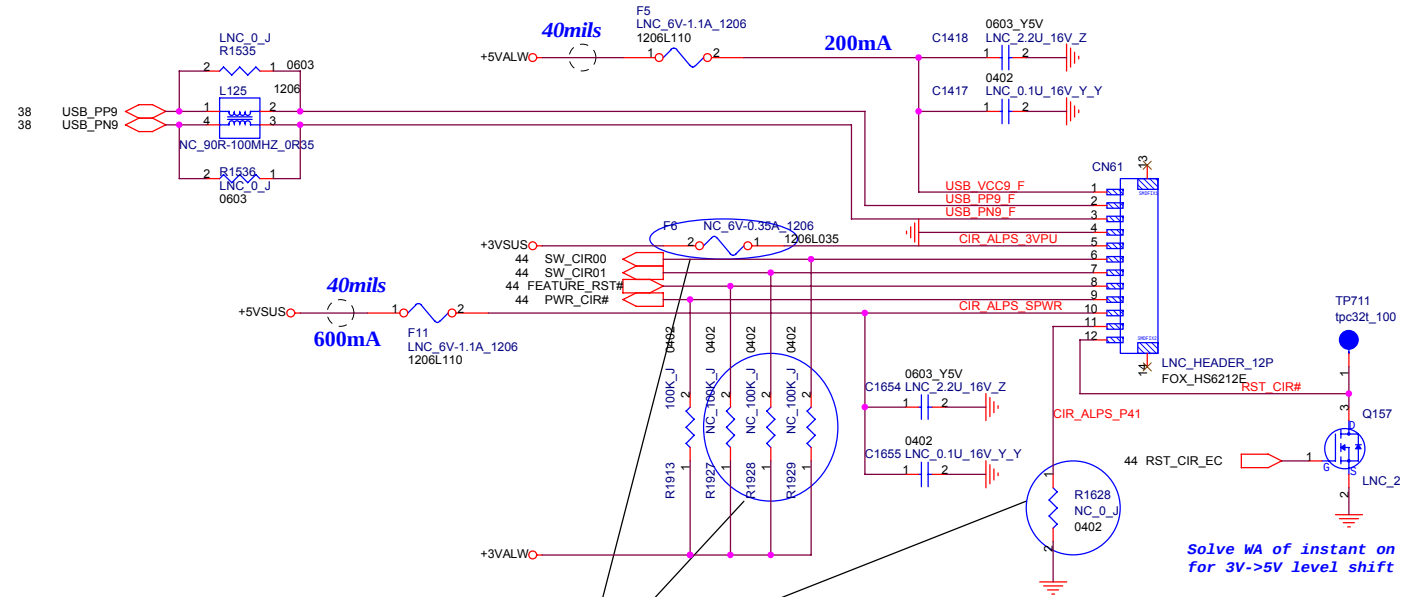


FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
EXPRESS CARD			
Size	Document Number		Rev
A3	(M610-1-01) MainBoard (MBX-176) 2007.1.4	2.0	
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USB connector *2



IR Rreceiver connector



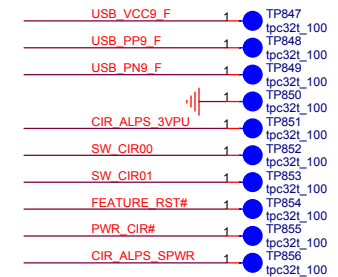
Button		SW1	SW0
VAIO button	Kick Instant On	L	L
Green button	Kick Windows	L	H
Shortcut button	Kick Windows	H	L
Standby button	Kick Windows	H	H

Num	Signal Name	I/O	Comment	Difference from ALPS.
1	+5VALW	VCC		<-
2	USB+	I/O		<-
3	USB-	I/O		<-
4	GND	GND		<-
5	+3VSUS	-	Not for use. Because SMK's IC use internal pull up resistor for D-.	ALPS's IC use this signal as a pull up plane of D- for low speed detection.
6	SW0	O	Use for detecting of the remote button. 3.3V CMOS output.	3.3V open drain output.
7	SW1	O	Use for detecting of the remote button. 3.3V CMOS output.	3.3V open drain output.
8	Feature_RST#	I	Software reset signal. (3.3V internal pull up resistor.)	Use for detecting of the remote button. 3.3V open drain output.
9	PWR#	O	Power on request signal. Open drain output.	<-
10	SPWR	I	Power OK signal. 5V input.	<-
11	EN	-	Not for use.	Low: Disable instant on feature Open or High: Enable instant on feature (3.3V internal pull up resistor.)
12	Hard_RST#	I	Hardware reset.	<-

9/26 FOR NEW SMK IR module compatiy
1.Change stuff to NC:F6,R1927,R1928,R1929,
2.EC Page GPIO20(105),GPIOAD2(83) pin swape

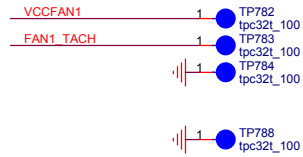
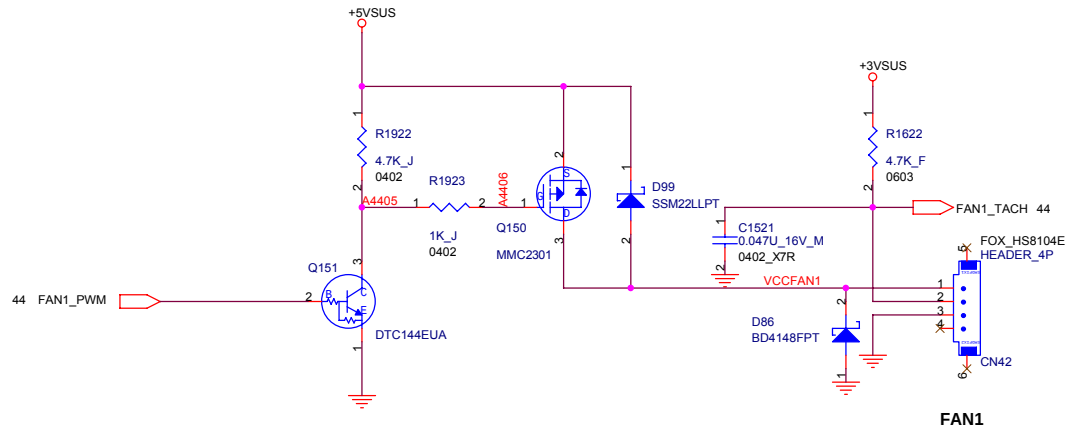
12/27 Change CIR circuit Value to LNC_* for M610 DVT L SKU

At Only USB Internal CIR, it's USB Power



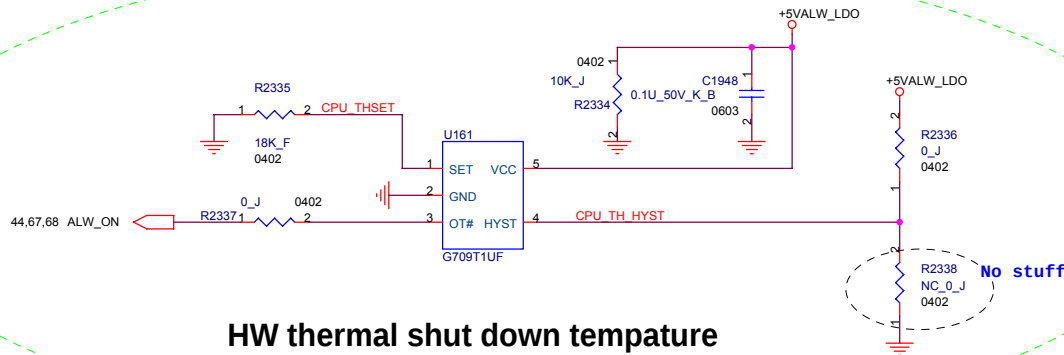
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
LED/LID SW#/Touch PAD			
Size	Document Number	Rev	
A3	(M610-1-01) MainBoard (MBX-176) 2007.1.4	2.0	
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FAN circuit



HW THERMAL PROTECTION

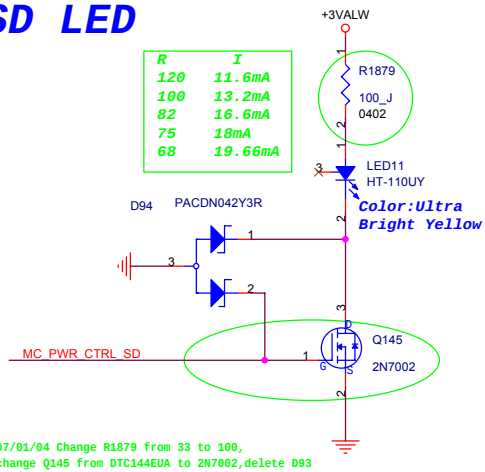
07/01/09 Change HW THERMAL PROTECTION circuit to stuff



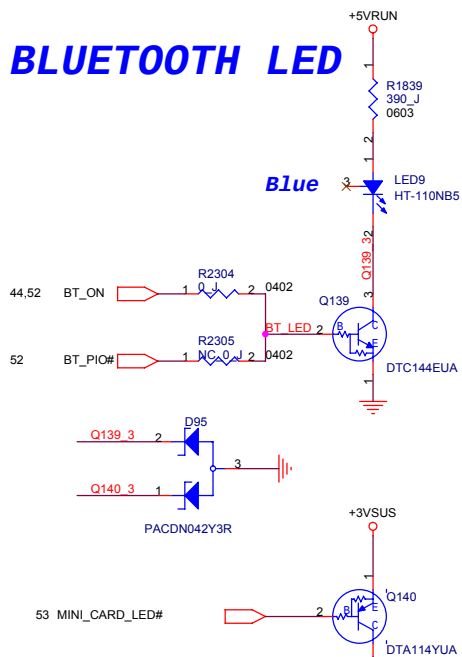
HW thermal shut down tempature setting 95 degree . Put Near CPU .

Base on MOR side request to add HW thermal protection circuit

SD LED



BLUETOOTH LED

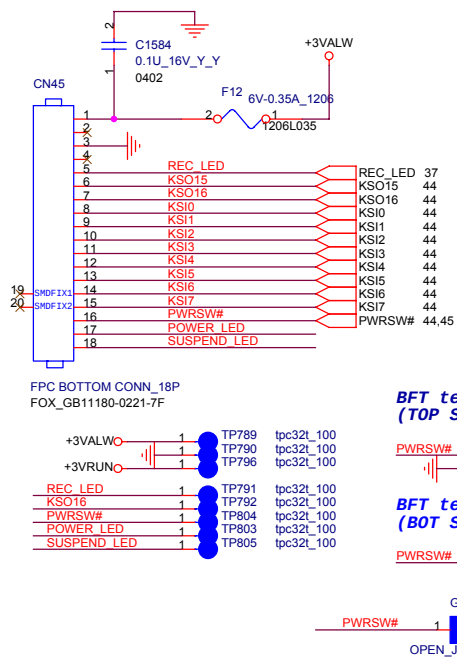


WLAN LED

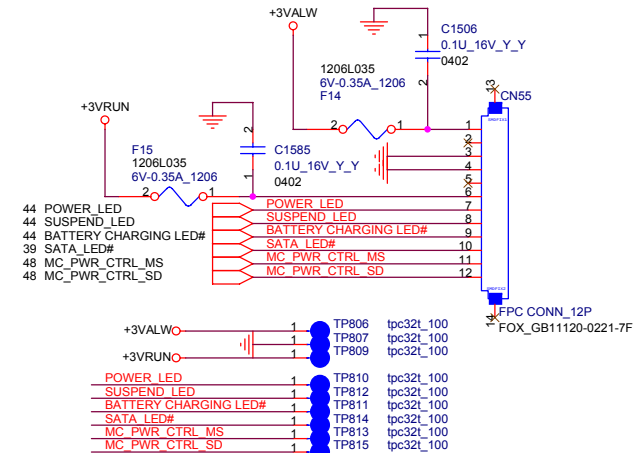
LED IF SPEC:

20mA(TYP), 30mA(MAX)

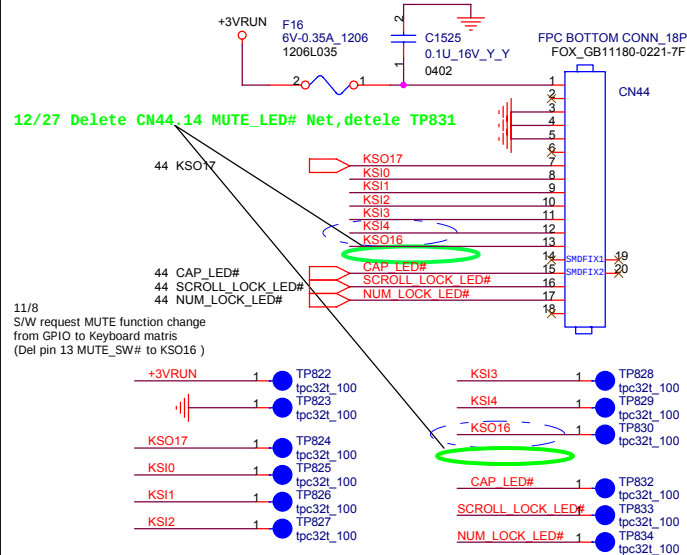
To Power Button Board Connector



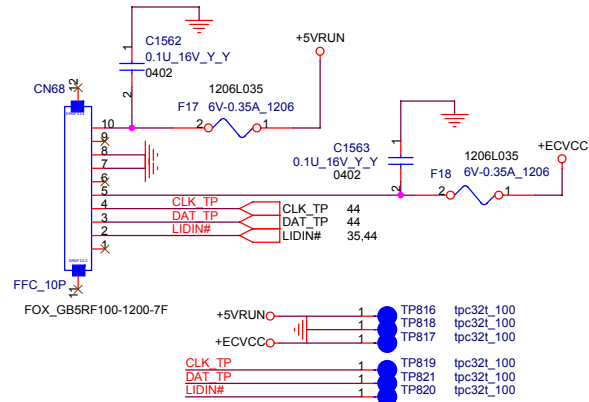
To LED Board Connector



To AV Function Board Connector



To Touch Pad Board Connector



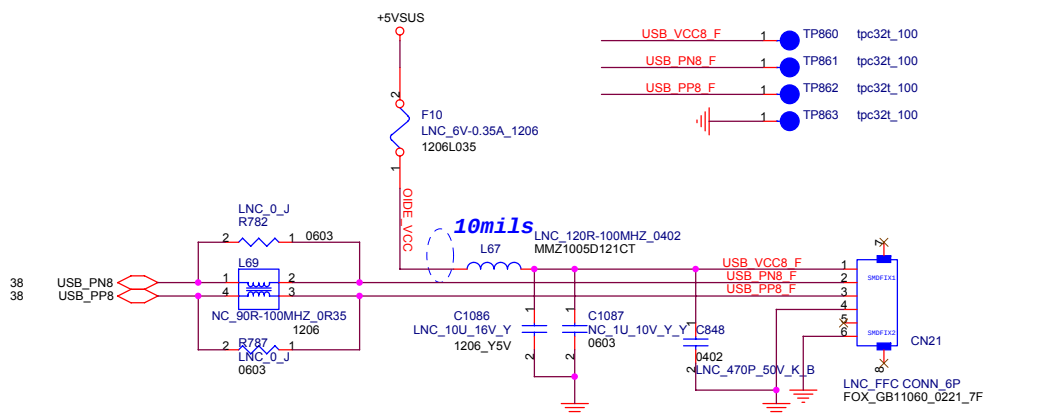
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

POWER BD + HOT KEY BD + T/P&LED BD + LOGO LED

Size A3 Document Number (M610-1-01) MainBoard (MBX-176) 2007.2.4

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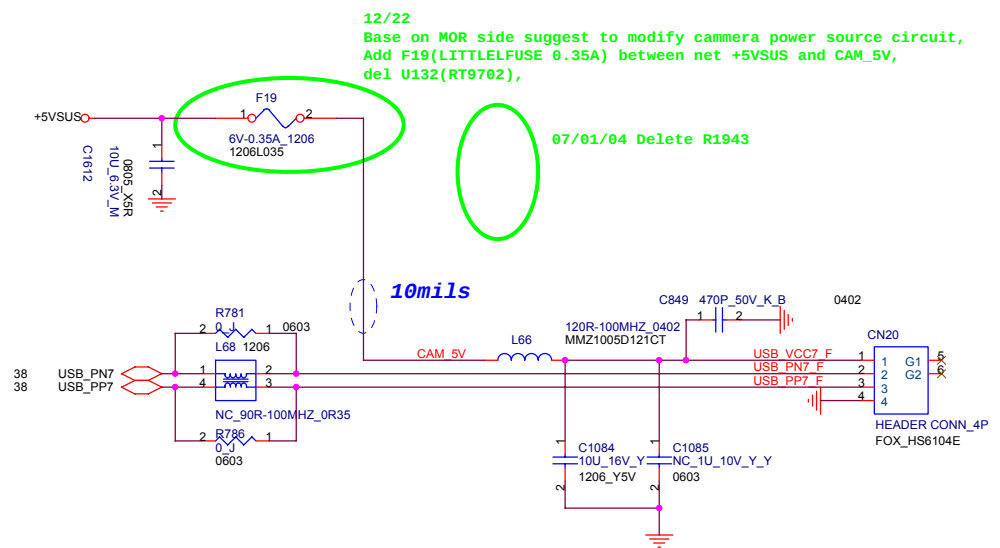
OIDE Connector



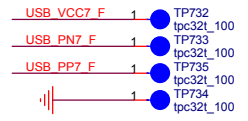
2006.1.4pin swape for ME request

12/27 Change Felica circuit Value to LNC_* for M610 DVT L SKU

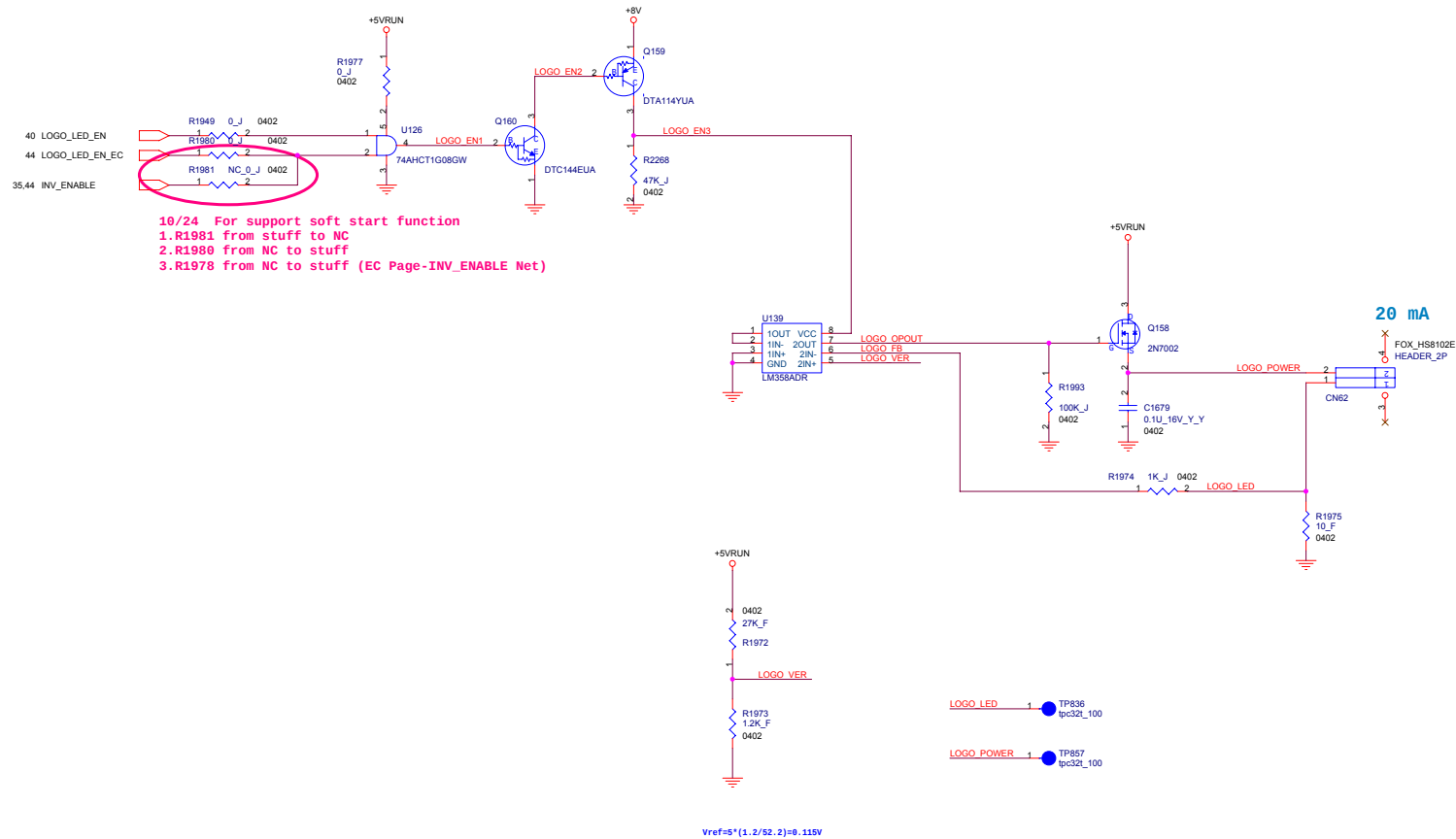
CAMERA Connector



12/21 BFT Test Pad

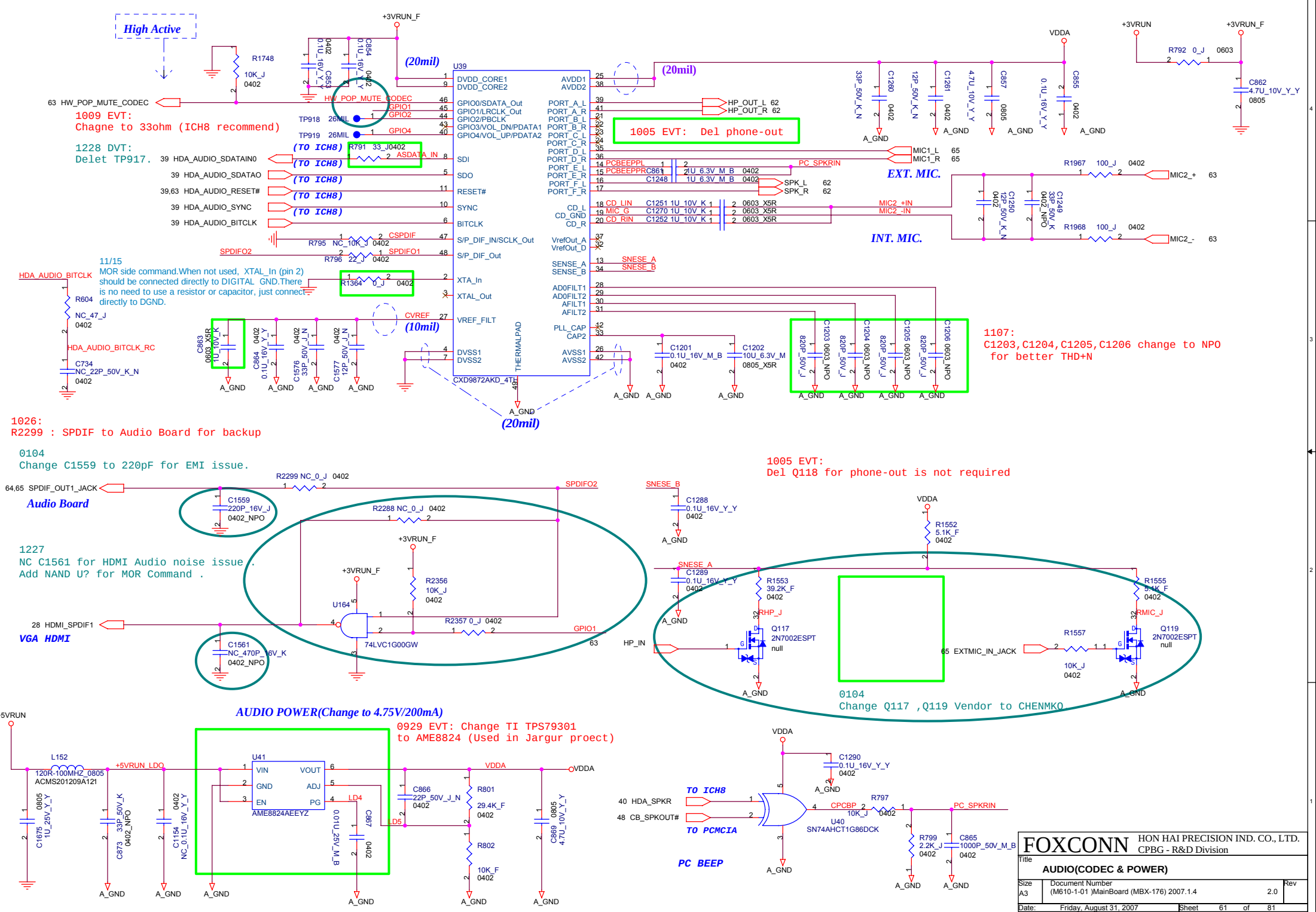


Constant-Current SONY LOGO LED



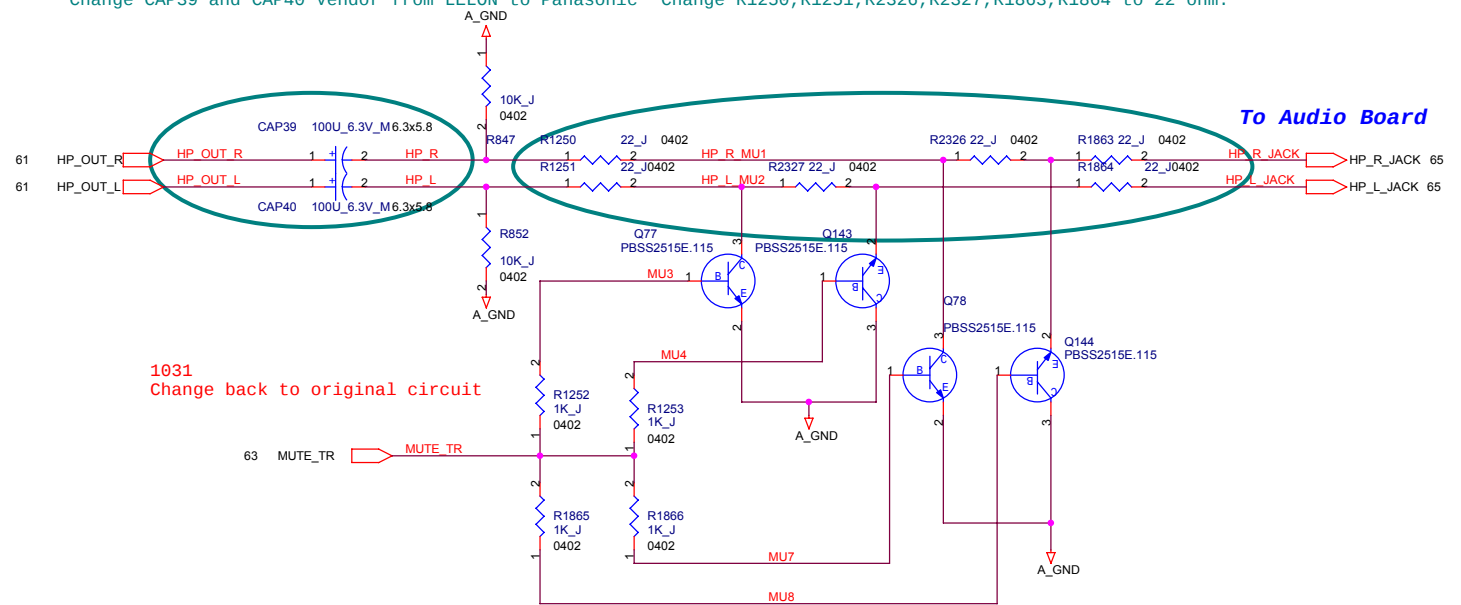
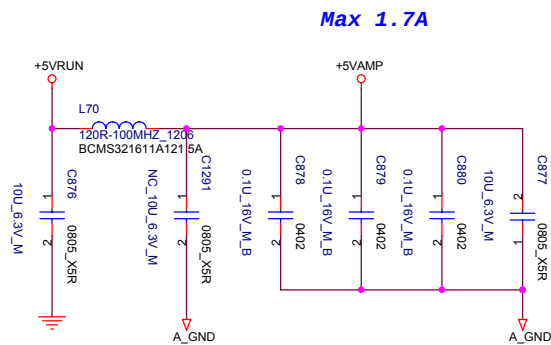
FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title Logo LED / +1_5VSUS			
Size	Document Number		Rev
Custom	(MS10-1-01) MainBoard (MBX-176) 2007.1.4	2.0	
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High Active



0920
Add 2PCS CAP39,CAP40 100_6.3V_M
Delet CAP24,CAP25
1103
Change CAP39 and CAP40 Vendor from NIPPON CHEMI-CON to LELON

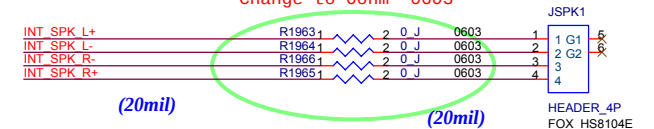
1228
Change CAP39 and CAP40 Vendor from LELON to Panasonic
1229
Change R1250,R1251,R2326,R2327,R1863,R1864 to 22 ohm.



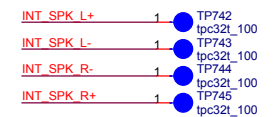
1031
Change back to original circuit

INTERNAL SPEAKER

0920
Change to 0ohm 0603



BFT Test Pad



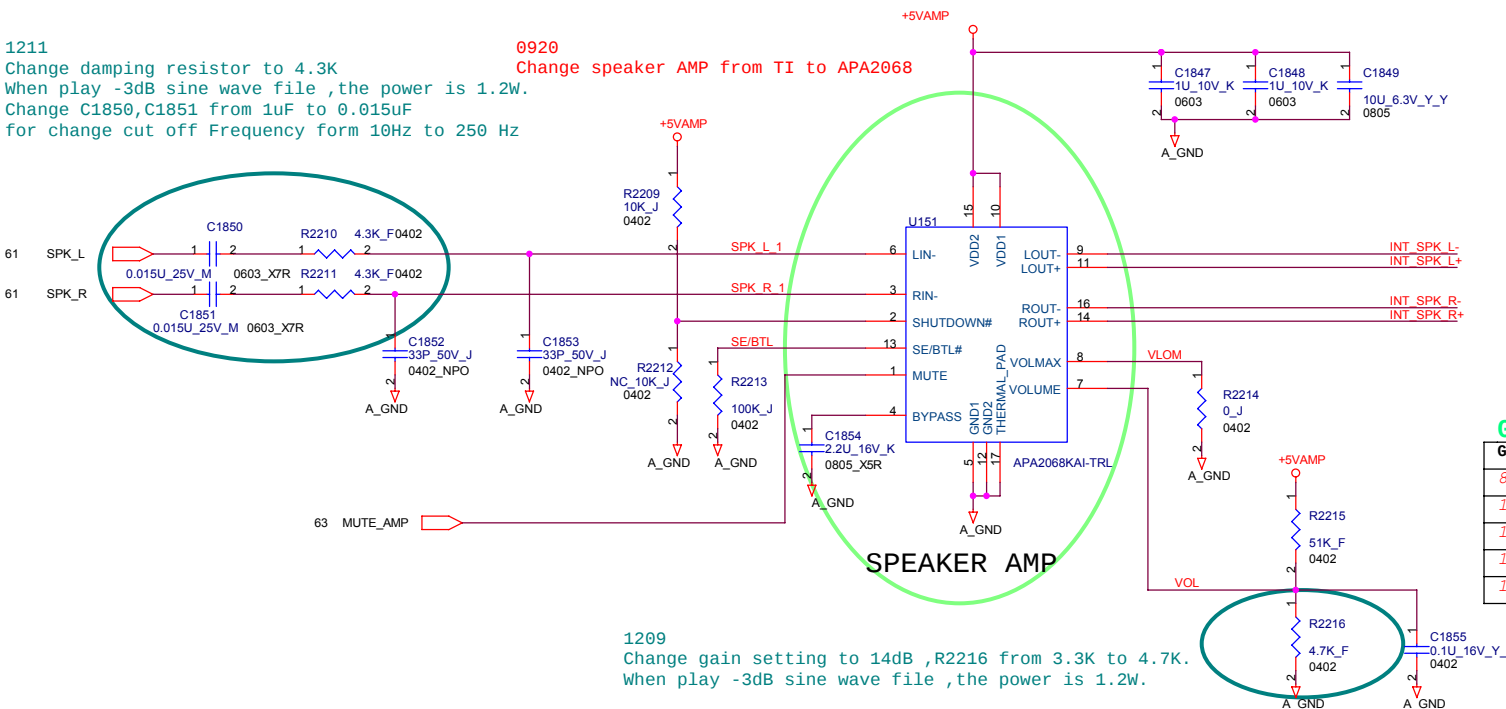
Gain setting table

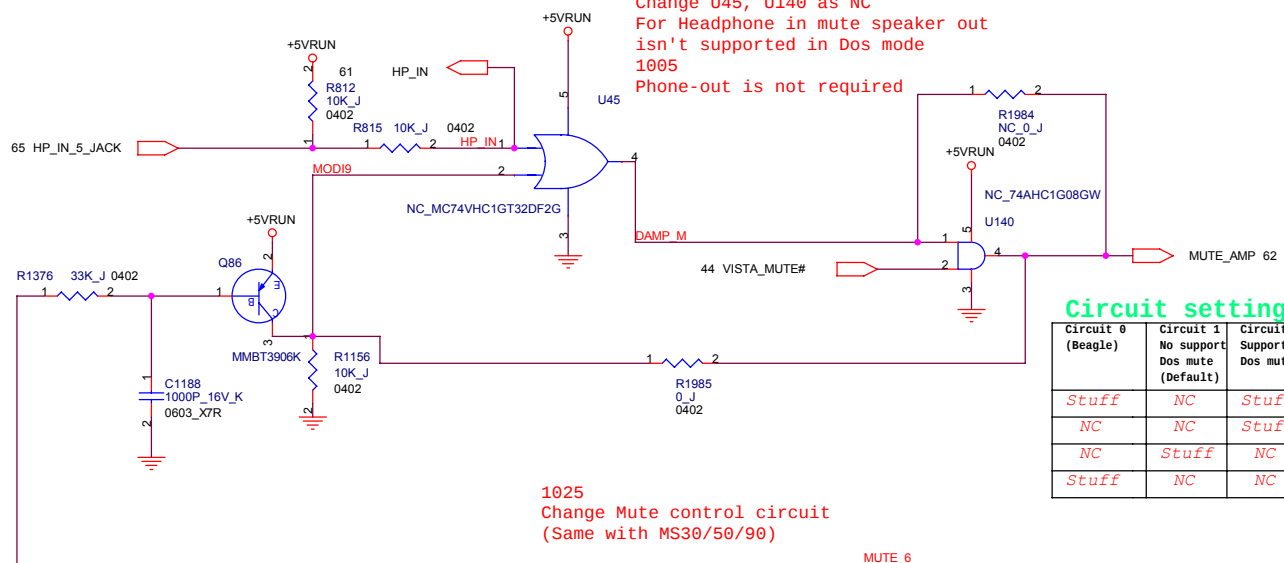
Gain	R2216	Voltage
8dB	9.1K	0.77V
10dB	7.68K	0.65V
12dB	6.2K	0.54V
14dB	4.7K	0.43V
16dB	3.3K	0.31V

SPEAKER AMP

1209
Change gain setting to 14dB ,R2216 from 3.3K to 4.7K.
When play -3dB sine wave file ,the power is 1.2W.

1211
Change damping resistor to 4.3K
When play -3dB sine wave file ,the power is 1.2W.
Change C1850,C1851 from 1uF to 0.015uF
for change cut off Frequency form 10Hz to 250 Hz

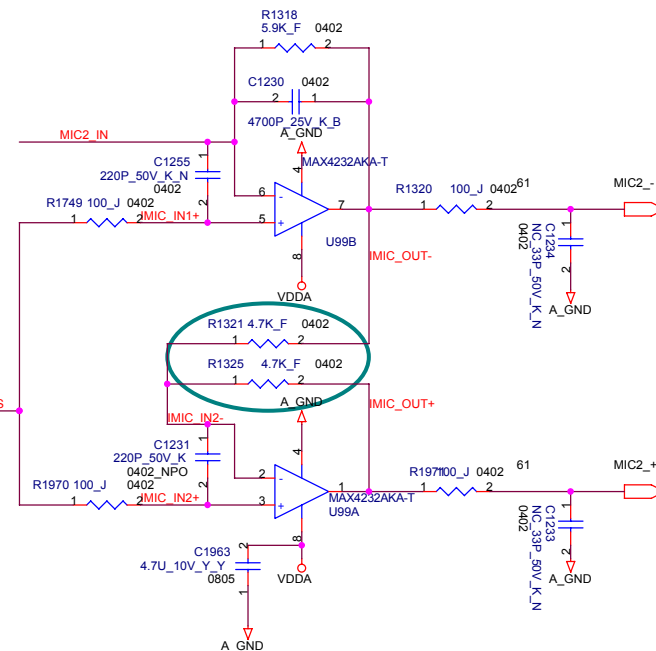




1025
Change Mute control circuit
(Same with MS30/50/90)

Circuit setting table

Circuit 0 (Beagle)	Circuit 1 No support Dos mute (Default)	Circuit 2 Support Dos mute	component
Stuff	NC	Stuff	U45
NC	NC	Stuff	U140
NC	Stuff	NC	R1985
Stuff	NC	NC	R1984



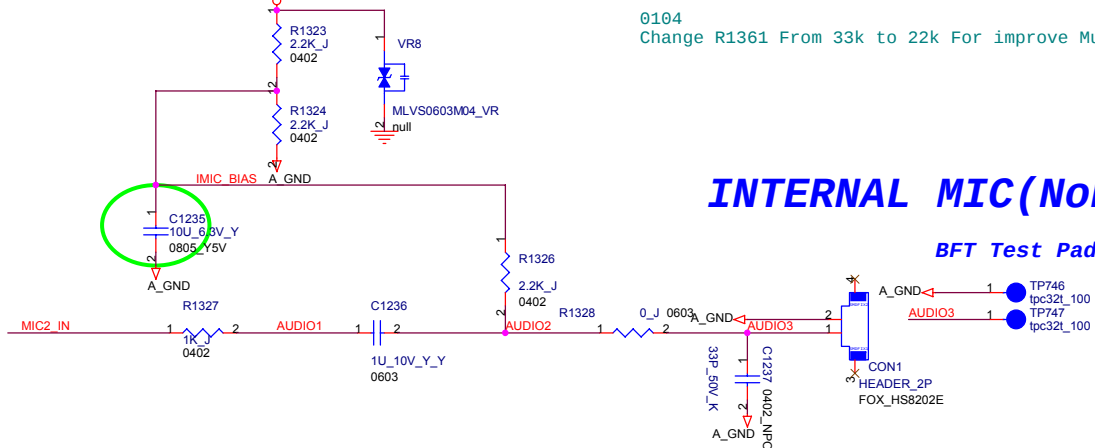
1227
Change R1321 and R1325 from 4.7k_J to 4.7K_F
for MOR Side Command.

1005
Del phone-out mute circuit
for phone-out is not required

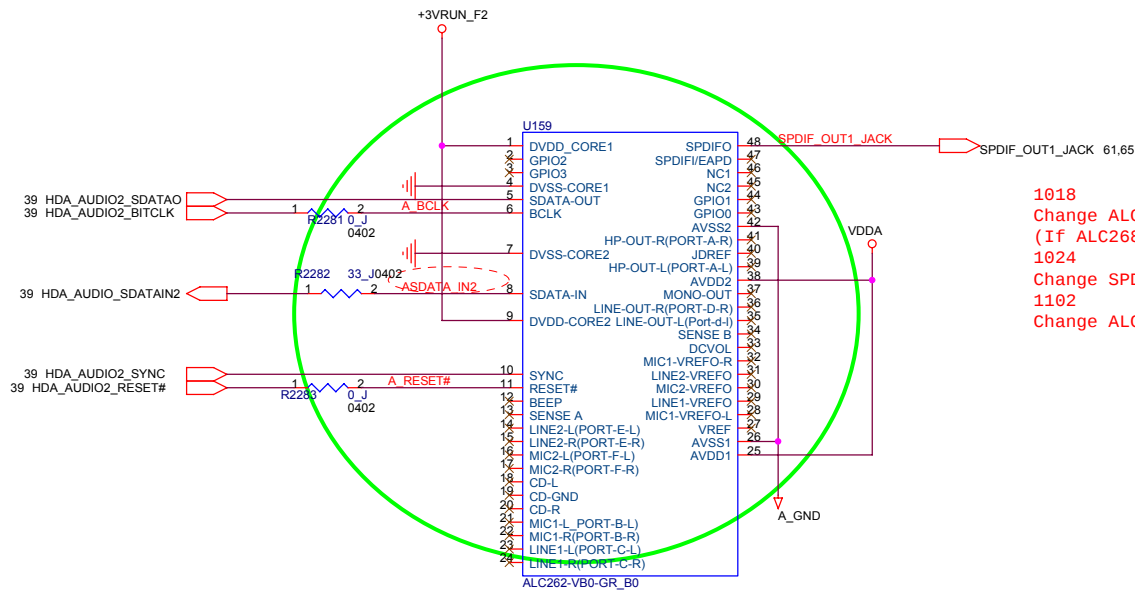
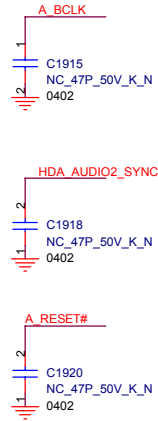
0104
Change R1361 From 33k to 22k For improve Mute_TR signal quality well.

INTERNAL MIC(Non)

BFT Test Pad

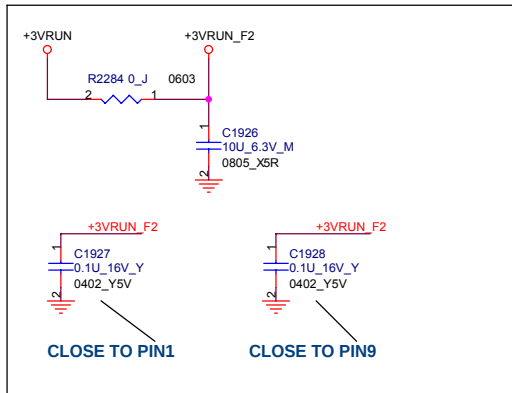


Anti-Glitch

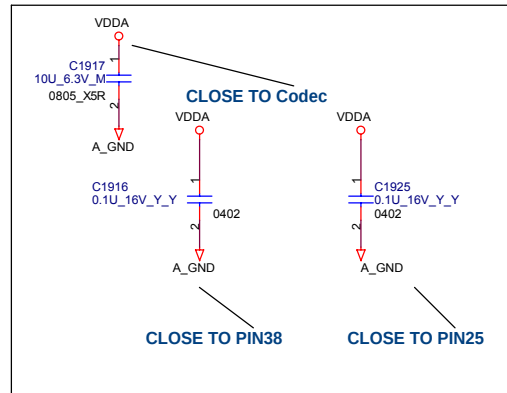


1018
Change ALC262 to ALC268.
(If ALC268 sample schdule delay, change to ALC262)
1024
Change SPDIF of Second codec to MB optical out
1102
Change ALC268 to ACL262

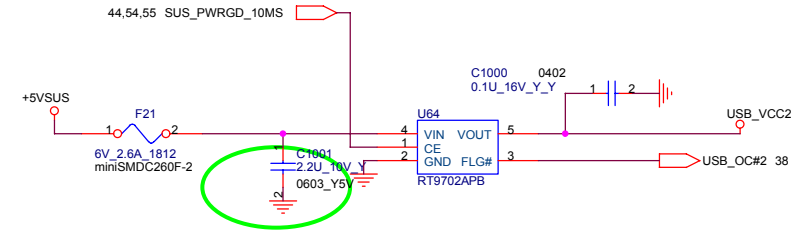
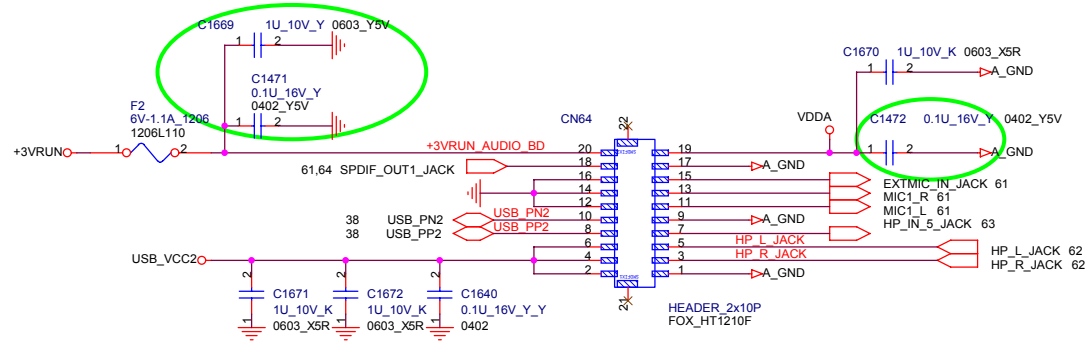
Decoupling Caps, place close to power pin.



Decoupling Caps, place close to power pin.

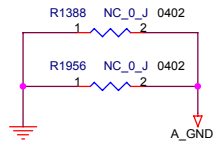


Audio Board connector

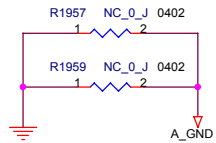


Backup two jumper resistors for bridge between GND and A_GND

Close screw hole H3

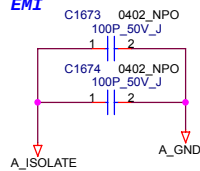


Close screw hole H5

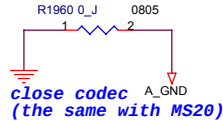
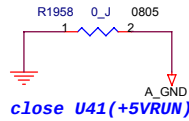
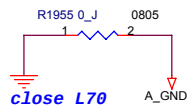


Isolate screw hole H4, and add EMI/ESD solution

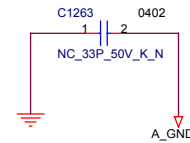
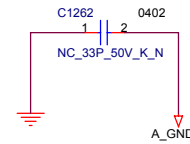
EMI



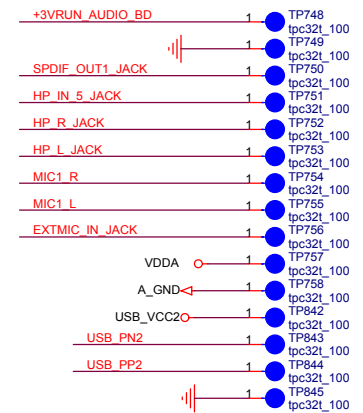
Add jumper resistor for Return patch



Original EMI back up solution to continue with MS20(bridge between GND and A_GND)



BFT Test Pad

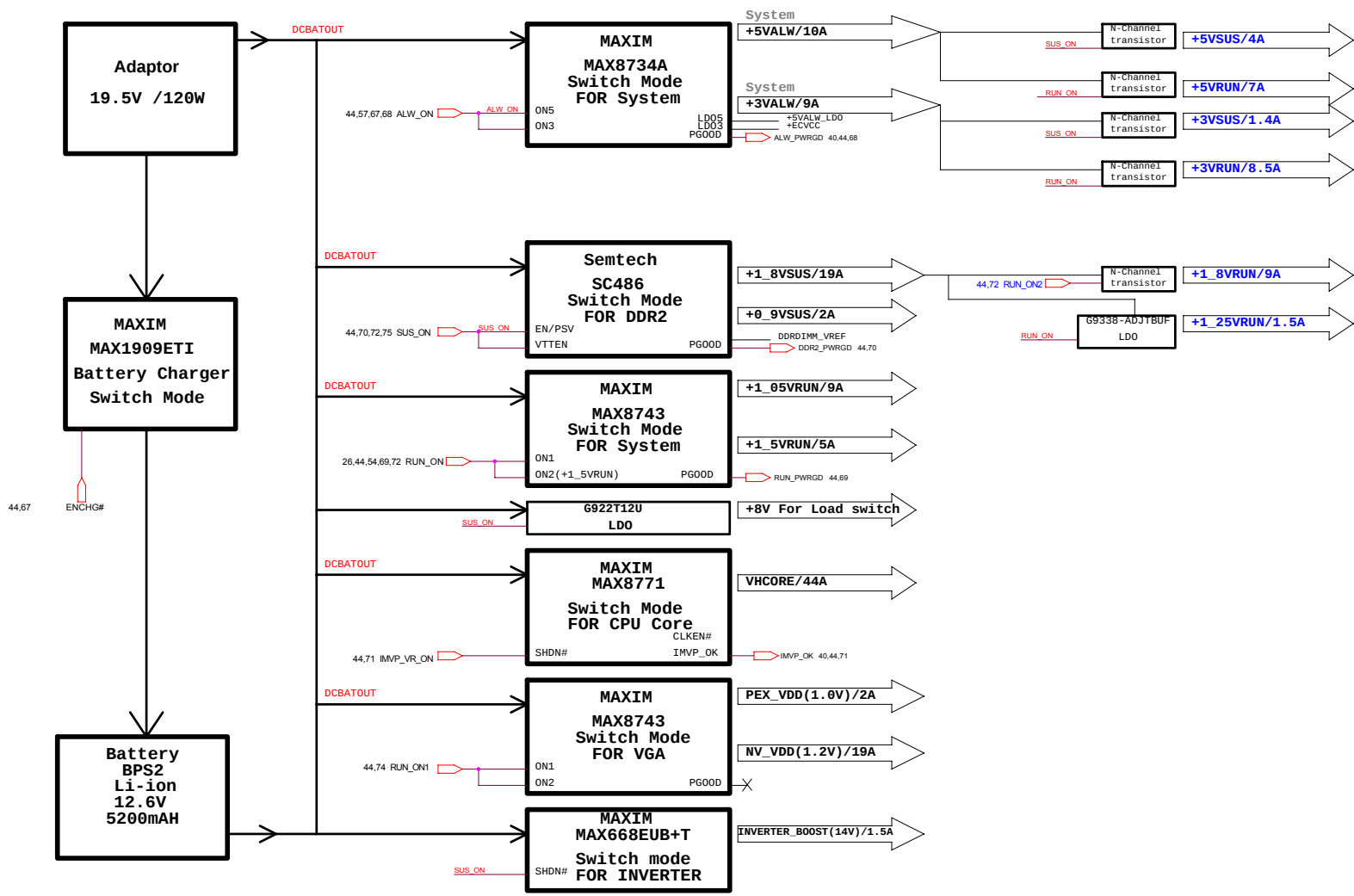


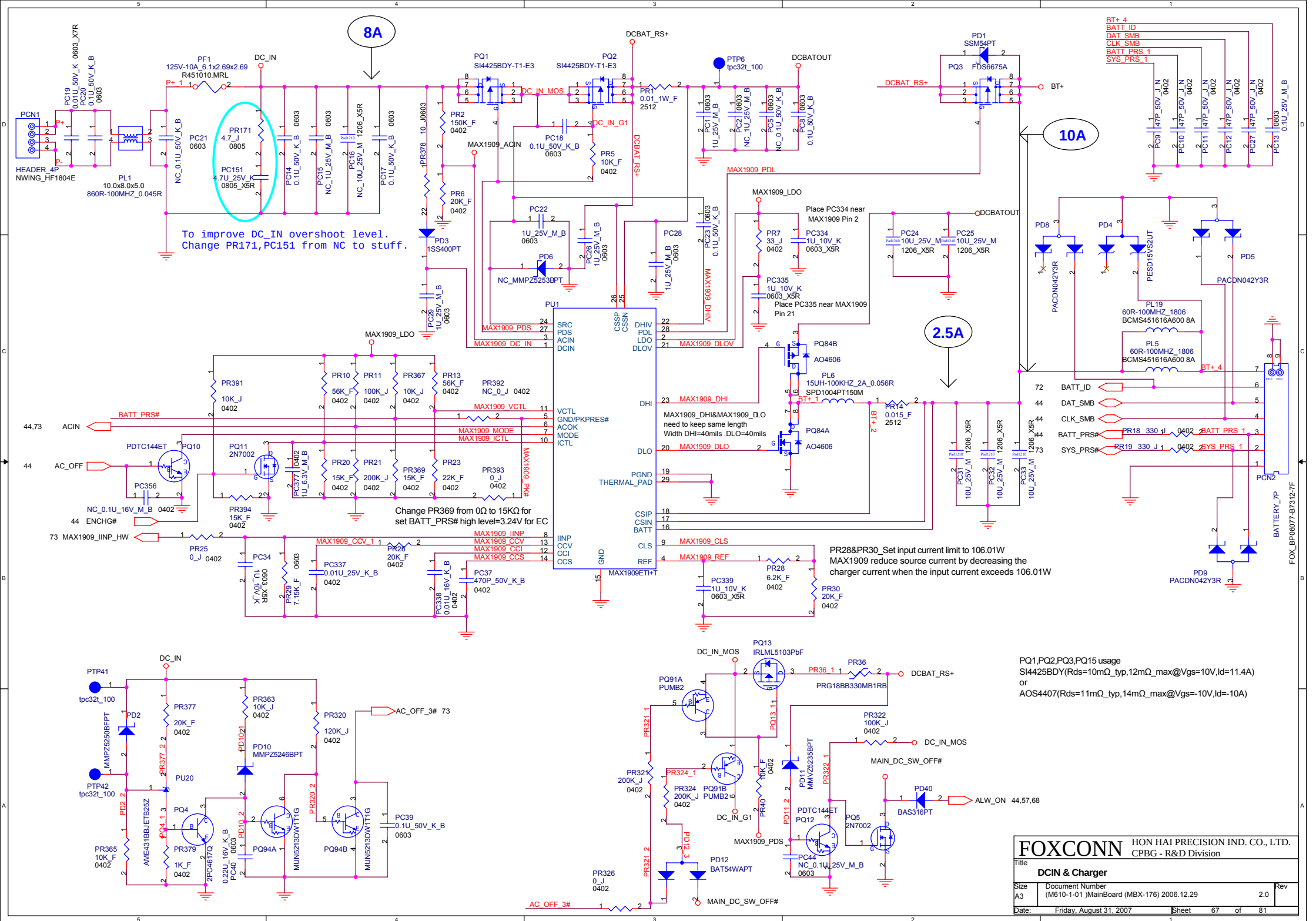
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

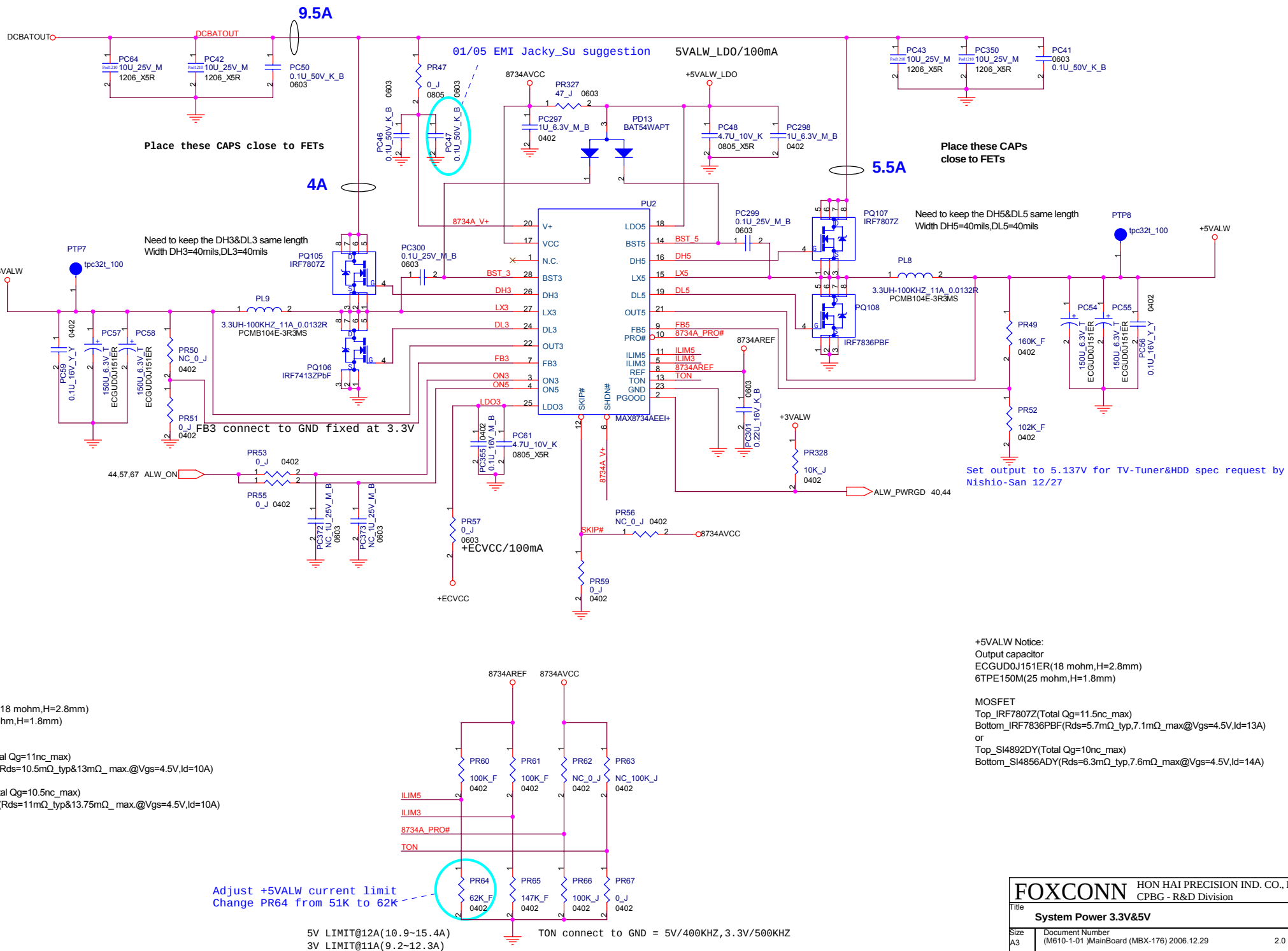
Title: **Audio Board conn**

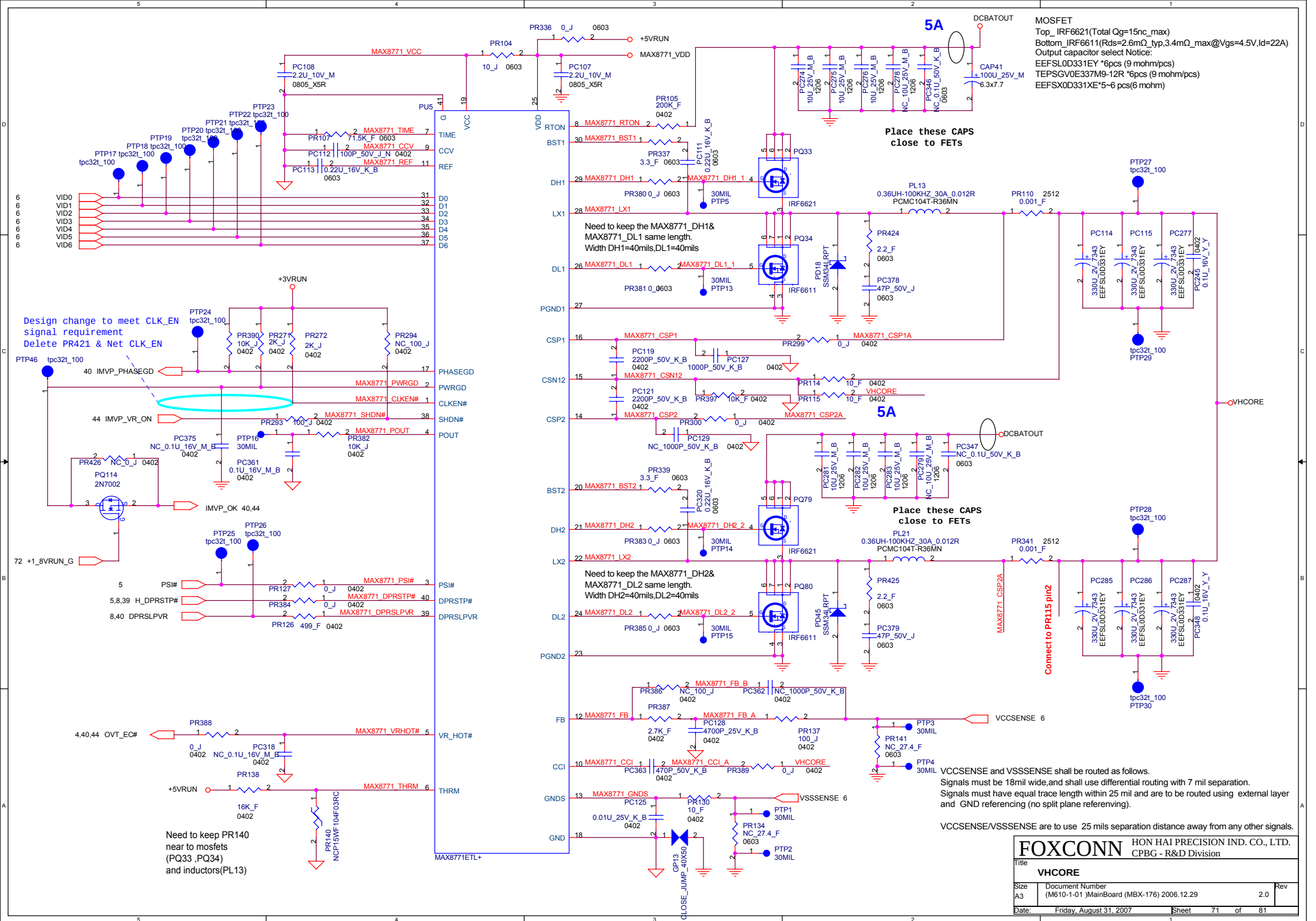
Size: A3 Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 2.0 Rev

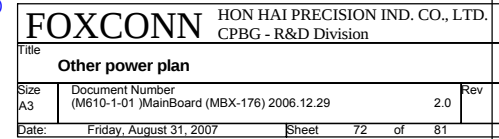
Date: Friday, August 31, 2007 Sheet 65 of 81

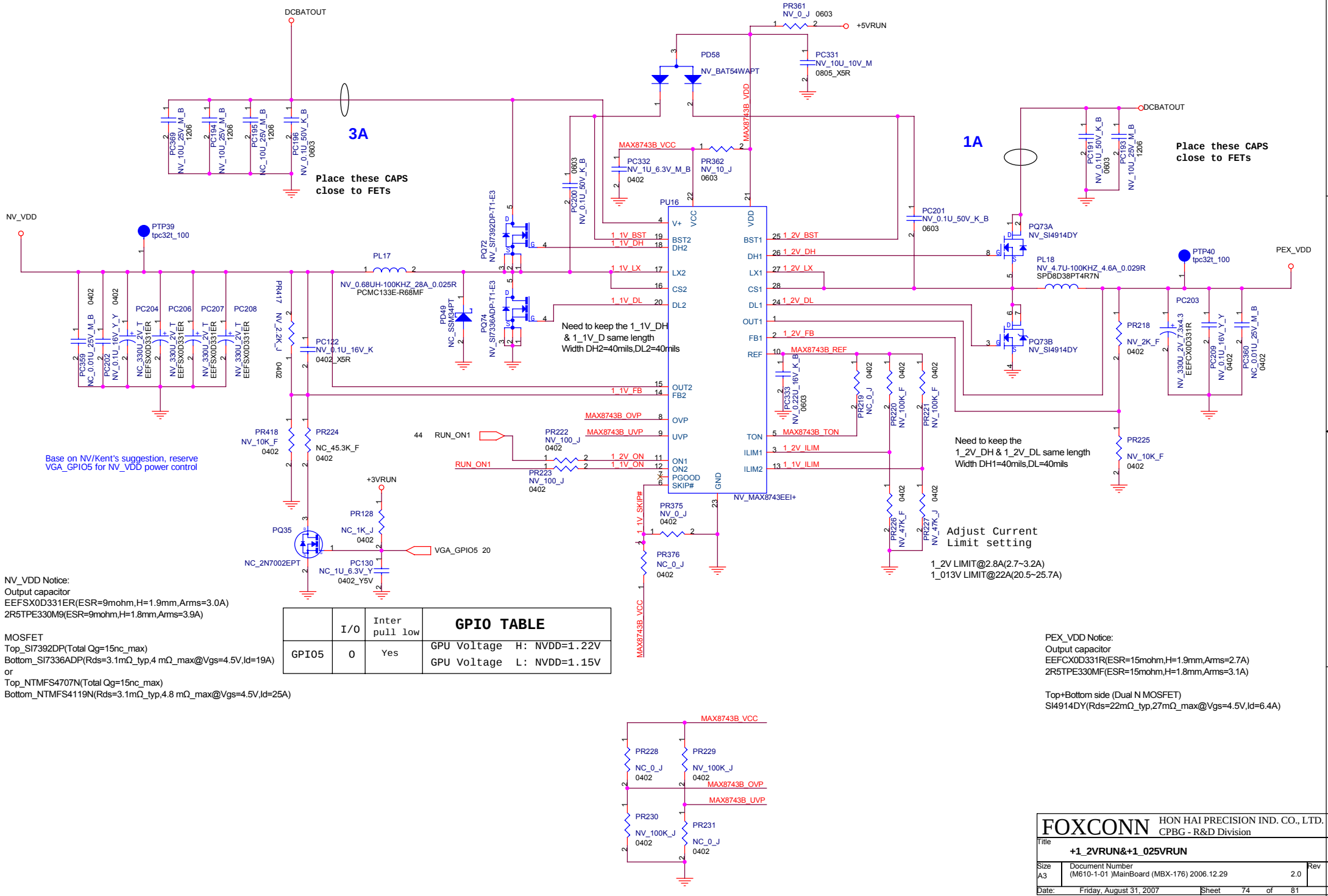












NV_VDD Notice:
Output capacitor
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

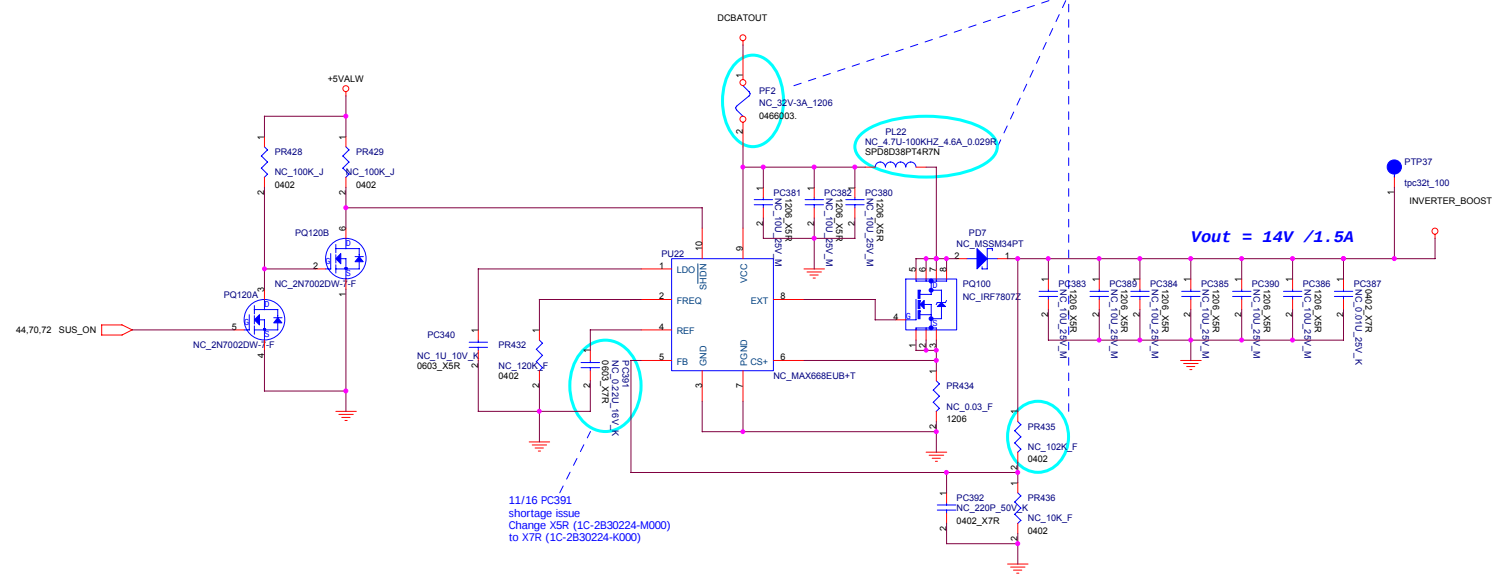
MOSFET
Top_Si7392DP(Total Qg=15nc_max)
Bottom_Si7336ADP(Rds=3.1mΩ_typ,4 mΩ_max@Vgs=4.5V,Id=19A)
or
Top_NTMFS4707N(Total Qg=15nc_max)
Bottom_NTMFS4119N(Rds=3.1mΩ_typ,4.8 mΩ_max@Vgs=4.5V,Id=25A)

GPIO TABLE			
GPIO5	I/O	Inter pull low	GPU Voltage H: NVDD=1.22V
			GPU Voltage L: NVDD=1.15V
0		Yes	

PEX_VDD Notice:
Output capacitor
EEFCX0D331R(ESR=15mohm,H=1.9mm,Arms=2.7A)
2R5TPE330MF(ESR=15mohm,H=1.8mm,Arms=3.1A)

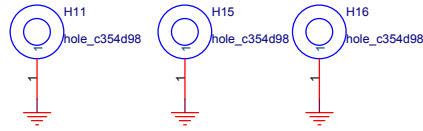
Top+Bottom side (Dual N MOSFET)
SI4914DY(Rds=22mΩ_typ,27mΩ_max@Vgs=4.5V,Id=6.4A)

Boost circuit design change.
Add PF2 (32V-3A 1206) fuse for boost circuit,
Change PL22 from 8UH-100KHZ_2.5A_0.07R to 4.7U-100KHZ_4.6A_0.029R.
Change PR435 from 95.3K to 102K



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Title		CPBG - R&D Division	
STEP_UP			
Size Custom	Document Number (M610-1-01)MainBoard (MBX-176) 2006.12.29	2.0	Rev
Date:	Friday, August 31, 2007	Sheet	75 of 81

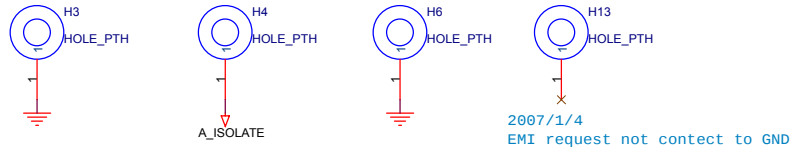
HOLE Type 1



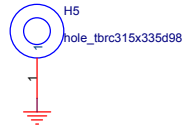
Type 2

Type 3

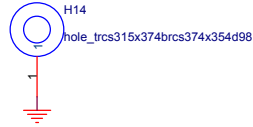
Type 4



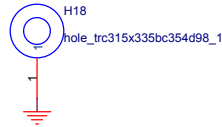
Type 5



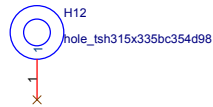
Type 6



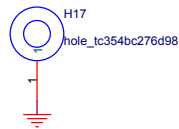
Type 7



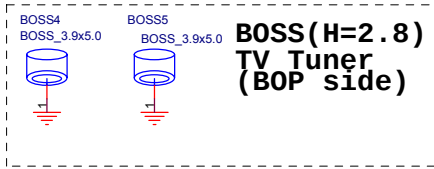
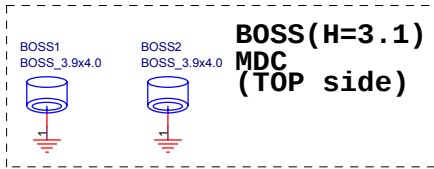
Type 8



Type 9



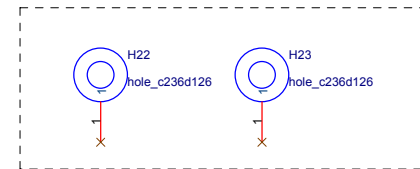
Type CPU



Type NPTH Guide (spherical)HOLD



Type NPTH Guide (oval-shaped)HOLD



VRAM Thermal Solution

M612 DVT2 Change Circuit

- 1.(Page 17~32) 07/08/17 Modify Page from 17 to 32 for 8pcs Vram.(512MB:16MBx32bx8pcs)
- 2. (Page 4) 07/08/29 For support Penryn-CPU, change U2-CPU Thermal Sensor from GMT to SMSC.
- 3. (Page 44) 07/08/29 Change System ID to M612 Type
- 4. (Page 76) 07/08/29 Add H22,H23 for VRAM thermal solution