ZB3

CPU CORE
MAX8736
Page:31
VCC_CORE
+1.5V_RUN

+1.2V (SC1470) VCCP_+1.05V (MAX1992)
Page:32
+1.2V
VCCP_+1.05V

+1.8VSUS +0.9V_VTER (NCP5214)
Page:33
+1.8VSUS
+1.8V
+0.9V_VTER

+3VPCU/+5VPCU +3V_S5 +3V/+5V +3VSUS/+5VSUS 15V
MAX1999
Page:34
+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5VSUS
+5V
15V

BATTERY CHARGER
MAX8724
Page:35
BATTERY

X'TAL 14.31818MHz

Clock generator
ICS951413CGLFT
Page:5

Yonah/Yonah Celeron-M
INTEL Mobile_479 CPU SOCKET_M
Page:3, 4

HOST BUS 533/667MHZ

VGA option

+1.0V/+1.2V VGA Power
MAX1993
Page:30

VGA_CORE

VGA Memory 128MB/256MB (Channel-B)
Page:19

NB ATi RC410ME 533MHz/667MHz
707-Pins FCBGA Package
Page: 6 , 7, 8, 9

PCI-E 16X

VGA ATi M52-P(M54-P)
Page: 15, 16, 17, 18, 19

RGB
CRT Page: 20

LVDS
LVDS Page: 20

UMA(option)

DDR-II SODIMM1 Page: 10
DDR-II SODIMM2 Page: 10
DDR-II 533/667MHz

2X PCIE

MINI-Card Wireless LAN
Page: 22
USB7

Manufacturing Option

SATA HDD Page: 21
PATA HDD Page: 21
IDE-ODD Page: 21
SATA
ATA 66/100

SB
ATi SB460
549-Pins BGA Package
Page: 11, 12, 13, 14

RTC Page: 11

2X PCIE

MARVEL 88E8038
64QFN-Pins Package
Page: 23

BOTHHAND TRANSFORMER NS0013 Page: 23

RJ45 Page: 23

PCI BUS 33MHZ

TI PCI7412 Cardbus controller
AD17
REQ3# / GNT3#
INTE#, INTH#,
INTG#(share)
Page: 24,25

PCMCIA SLOT Page: 24

5 IN1 CARD READER Page: 25

USB 2.0

MINI-PCI Wireless LAN
AD20
REQ2# / GNT2#
INTF#,
INTG#(share)
Page: 22

Bluetooth USB interface Page:22
USB6

SYSTEM USB PORT*3 Page: 22
USB0,2,4

X'TAL 32.768KHz

LPC 33MHZ

KBC NS PC97551
176-Pins Package
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Touchpad Page: 26
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Audio DJ Page: 27
FAN Page: 29

Azalia

MIC-IN Page: 26
LINE-IN Page: 26

AUDIO CODEC
REALTEK- ALC883
48-pins Package
Page: 26

Audio AMP MAX9755 Page: 27
SPEAKER Page: 27

MODEM Page: 26
RJ11 Page: 23

Power State Table

Power Name	Control Signal	Power State
VCC_CORE	VRON	S0
VCCP_+1.05V	MAINON	S0
+3VPCU +3V_S5 +3VSUS +3V	N/A S5_ON SUSD MAIND	ALWAYS S0-S5 S0-S3 S0
+5VPCU +5VSUS +5V	N/A SUSD MAIND	ALWAYS S0-S3 S0
15V	N/A	S0
+1.2V	MAINON	S0
VGA_CORE	VGA_MAINON	S0
+2.5V	MAINON (Delay 1ms)	S0
+0.9V_VTER	MAINON	S0
+1.8V_S5 +1.8VSUS +1.8V	S5_ON SUSON MAIND	S0-S5 S0-S3 S0
+1.5V_RUN	MAINON	S0

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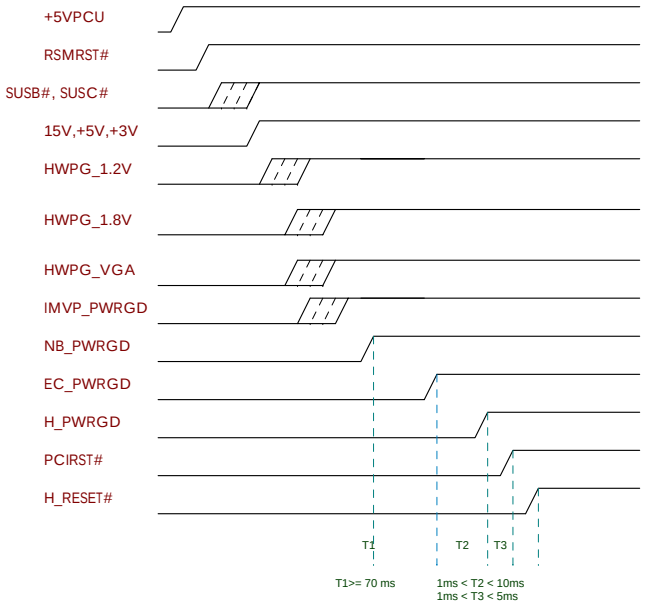
TABLE OF CONTENTS

	POWER	VOLTAGE	ACTIVE SCOPE	PAGE
SYSTEM	15V	15V	S0	33
	+5V	+5V	S0	33
	+3V	+3.3V	S0	33
	+5VPCU	+5V	ALWAYS	33
	+3VPCU	+3.3V	ALWAYS	33
	+5VSUS	+5V	S0-S3	33
	+3VSUS	+3.3V	S0-S3	33
	+3V_S5	+3.3V	S0-S5	33
CPU	VCC_CORE	VID[0..6]	S0	31
	VCCP_+1.05V	+1.05V	S0	31
	+1.5V_RUN	+1.5V	S0	31
RC410ME NB	VCCP_+1.05V	+1.05V	S0	31
	+1.8V	+1.8V	S0	33
	+1.8VSUS	+1.8V	S0-S3	33
	+1.2V	+1.2V	S0	32
	+3V	+3.3V	S0	33
	+1.2V_PCIE	+1.2V	S0	9
	+1.2V_CORE	+1.2V	S0	9
	VDD18	+1.8V	S0	9
	VDDA18	+1.8V	S0	9
	NB_VDDR	+3.3V	S0	8
	AVDD_NB	+3.3V	S0	8
	AVDDQ	+1.8V	S0	8
	PLVDD	+1.8V	S0	8
	NB_LPVDD	+1.8V	S0	8
	NB_LVDDR18A	+1.8V	S0	8
SB460 SB	+3V	+3.3V	S0	33
	+1.8V	+1.8V	S0	33
	+3V_S5	+3.3V	S0-S5	33
	+1.8V_S5	+1.8V	S0-S5	30
	VCCP_+1.05V	+1.05V	S0	31
	+1.8VUSB_PHY	+1.8V	S0-S5	13
	V5_REF	+5V	S0	13
	+1.8V_ATA	+1.8V	Reserve	13
	PLLVDD_ATA	+1.8V	Reserve	13
	XTLVDD_ATA	+1.8V	Reserve	13
	PCIE_PVDD	+1.8V	S0	11
	PCIE_VDDR	+1.8V	S0	11
	AVDD_USB	+3VSUS	S0-S3	12
	+3.3V_AVDDC	+3.3V	S0-S3	12
	VCCRTC	+3.0V	--	11
	VDDQ_3V	+3.3V	S0	13
	VDD_1.8V	+1.8V	S0	13
	SB_S5_3V	+3.3V	S0-S5	13
	SB_S5_1.8V	+1.8V	S0-S5	13
	AVDD_CK_1.8V	+1.8V	S0	13
DDR2	+1.8V	+1.8V	S0	33
	+1.8VSUS	+1.8V	S0-S3	10
	+0.9V_VTER	+0.9V	S0	10

POWER UP SEQUENCE



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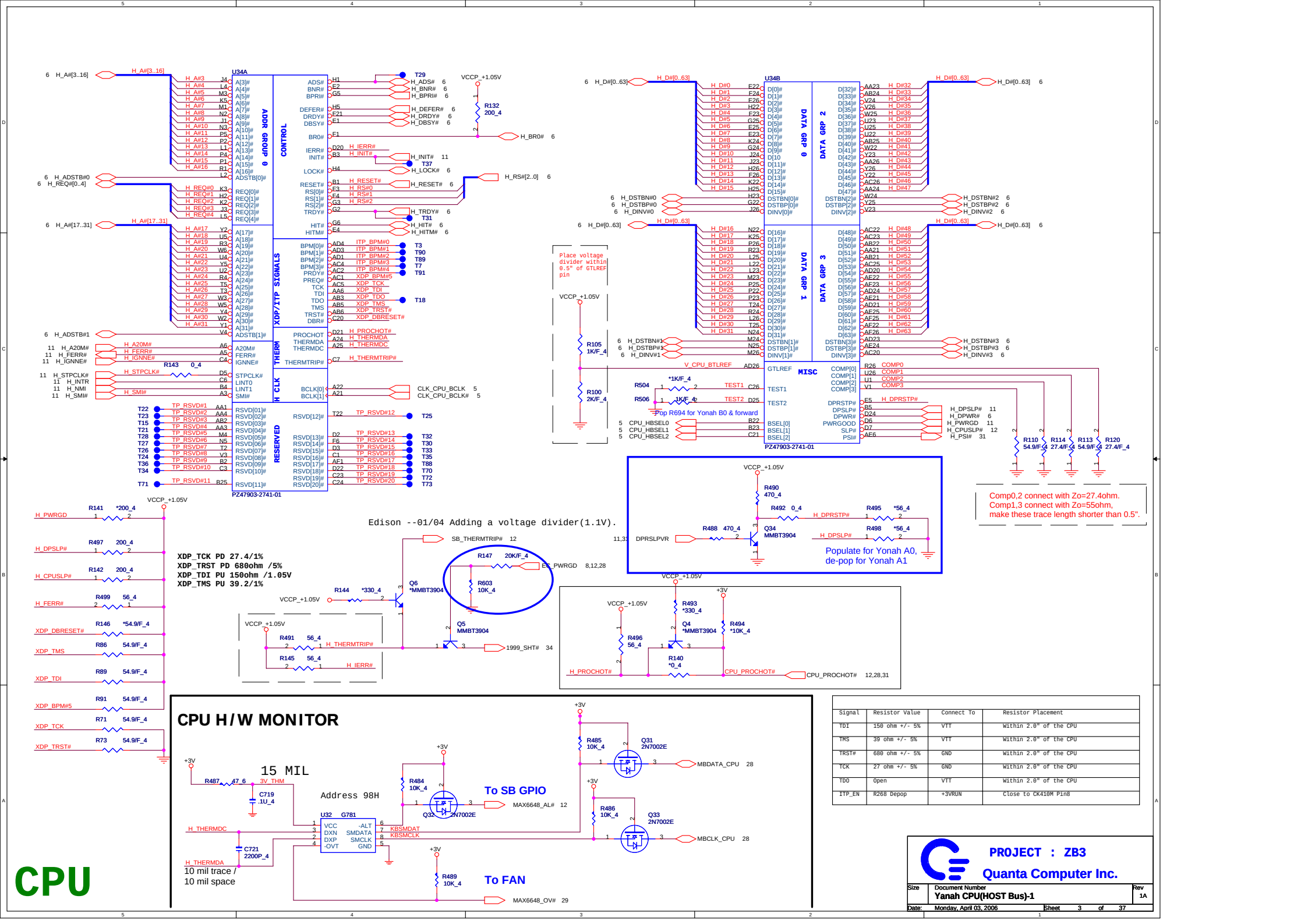

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VTT	Within 2.0" of the CPU
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

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Size	Document Number	Rev
	Yanah CPU(HOST Bus)-1	1A
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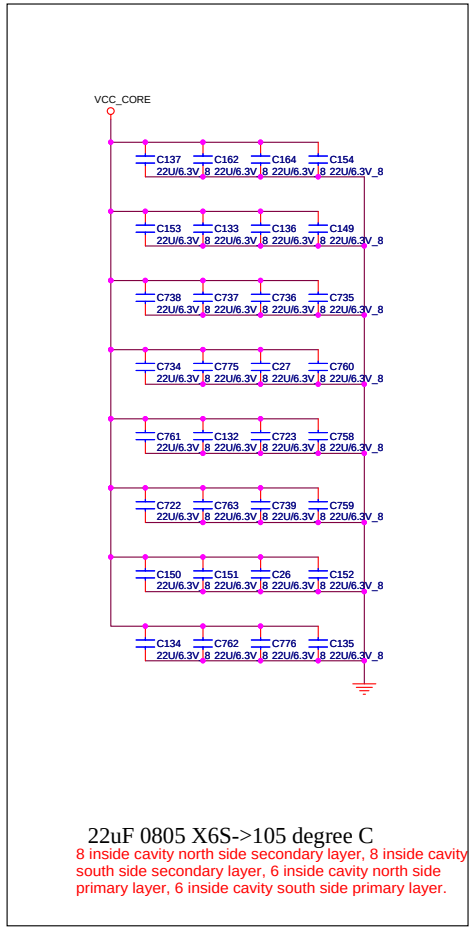

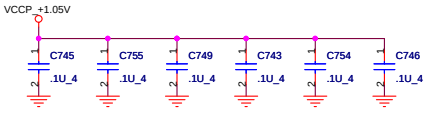

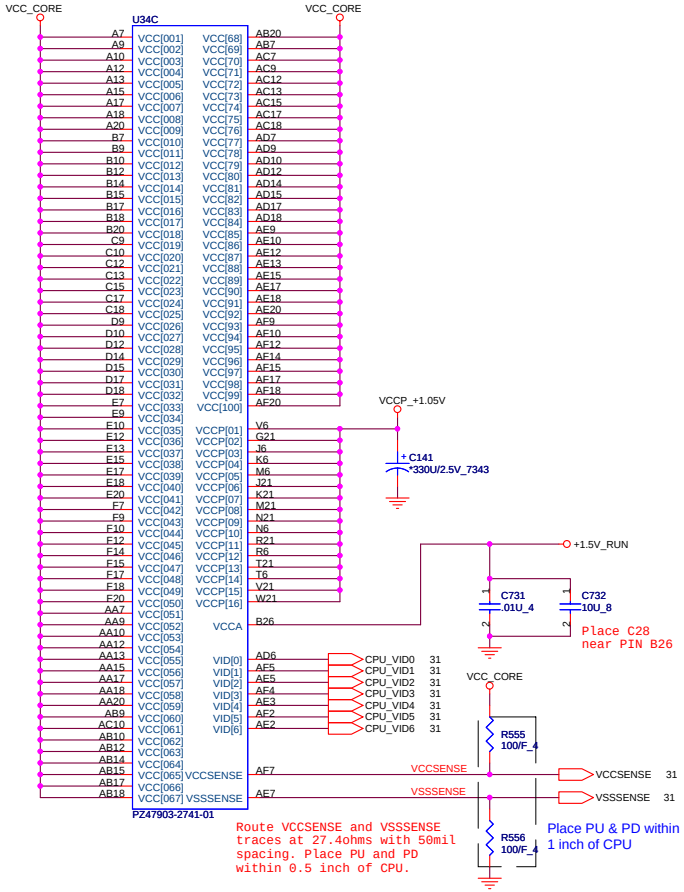

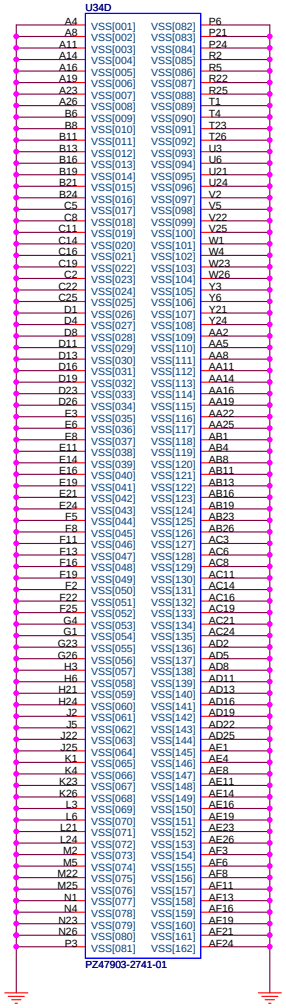

CPU

PROJECT : ZB3		
Quanta Computer Inc.		
Size	Document Number: Yanah CPU(Power/NC)-2	Rev: 1A
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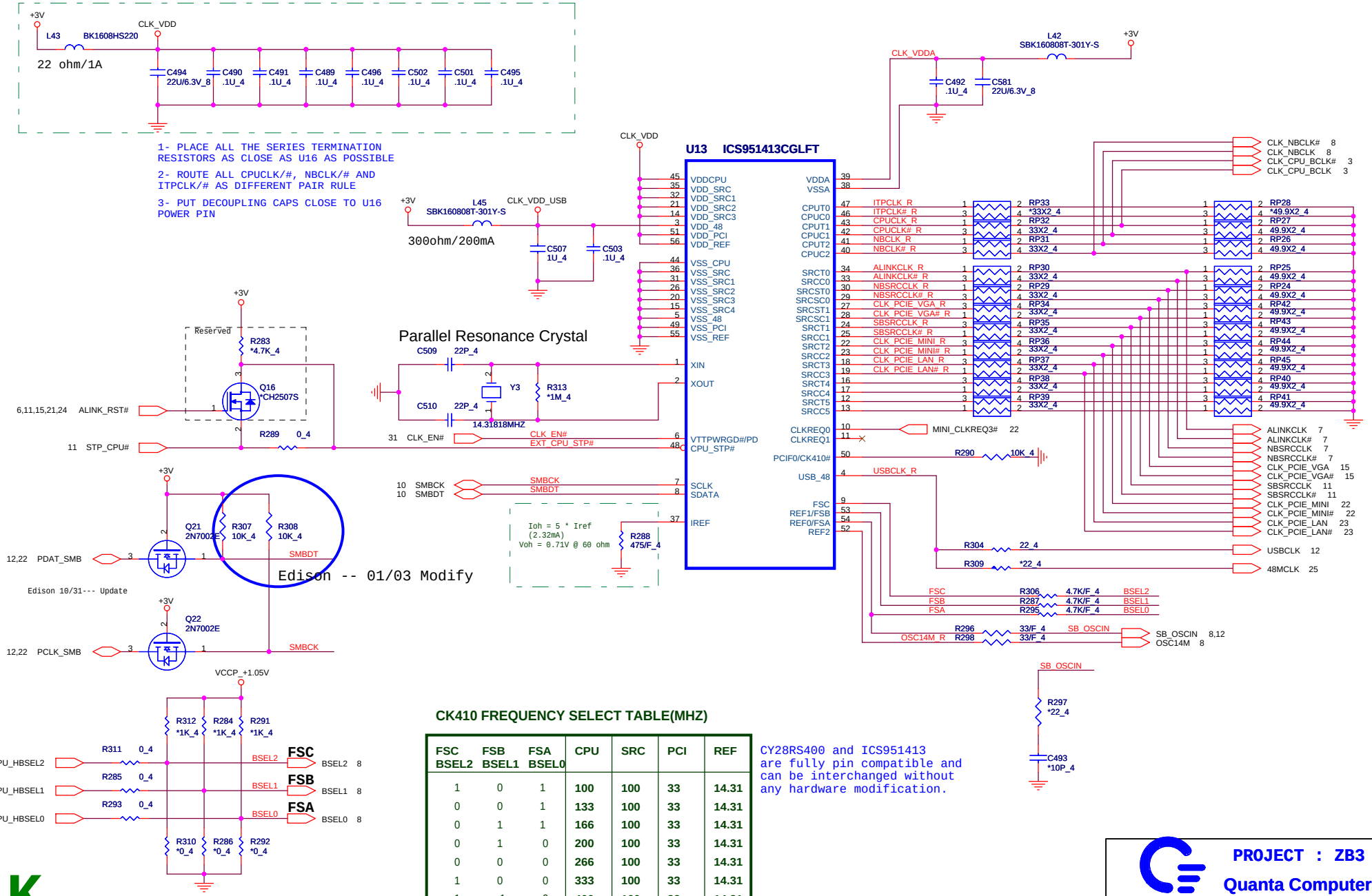

CLK

CK410 FREQUENCY SELECT TABLE(MHZ)

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

CY28RS400 and ICS951413 are fully pin compatible and can be interchanged without any hardware modification.

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Size	Document Number	Rev
	CLOCK GENERATOR	1A
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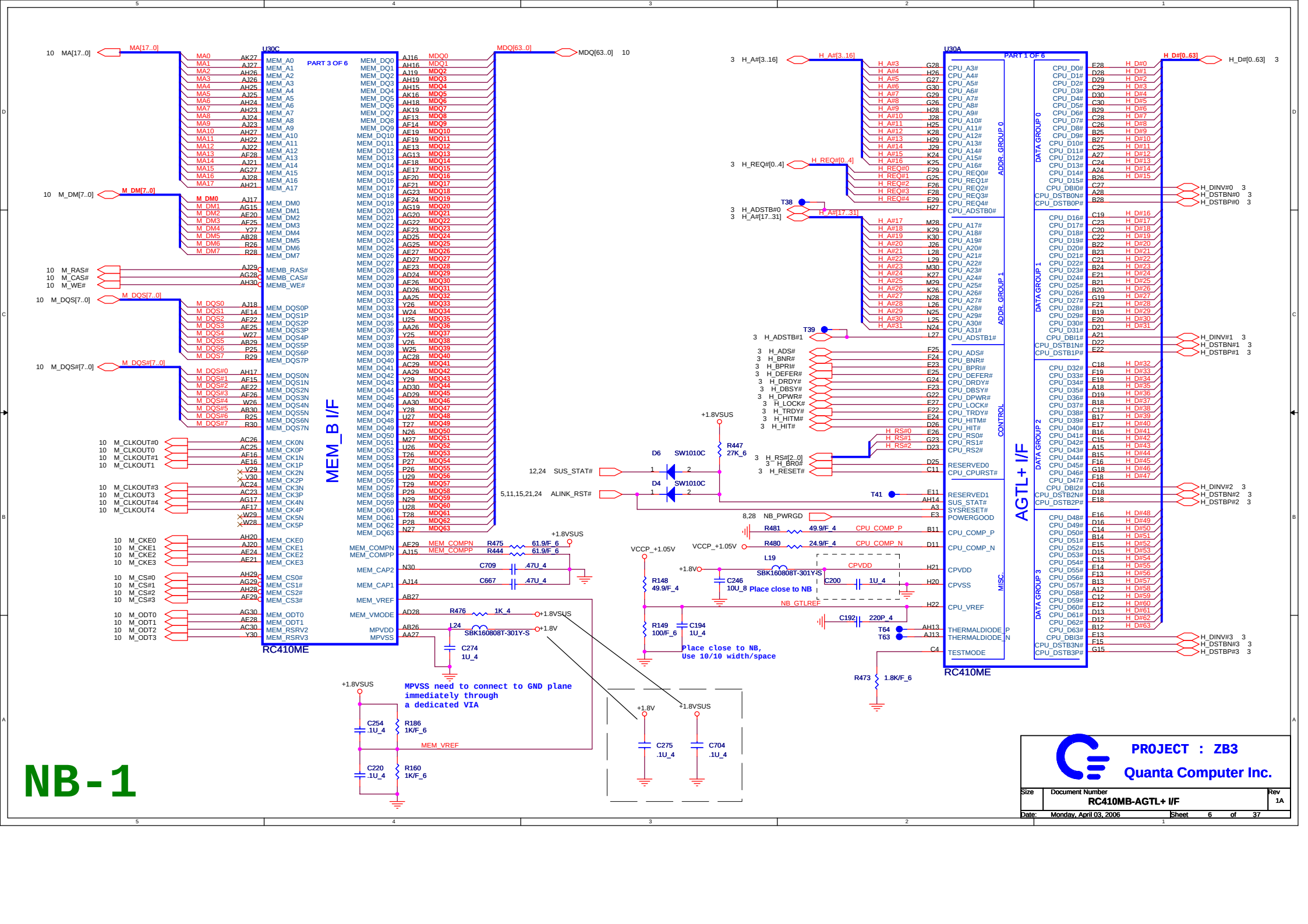
U30C
PART 3 OF 6
MEM_B I/F
RC410ME
U30A
PART 1 OF 6
AGTL+ I/F
RC410ME
NB-1
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Quanta Computer Inc.
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RC410MB-AGTL+ I/F
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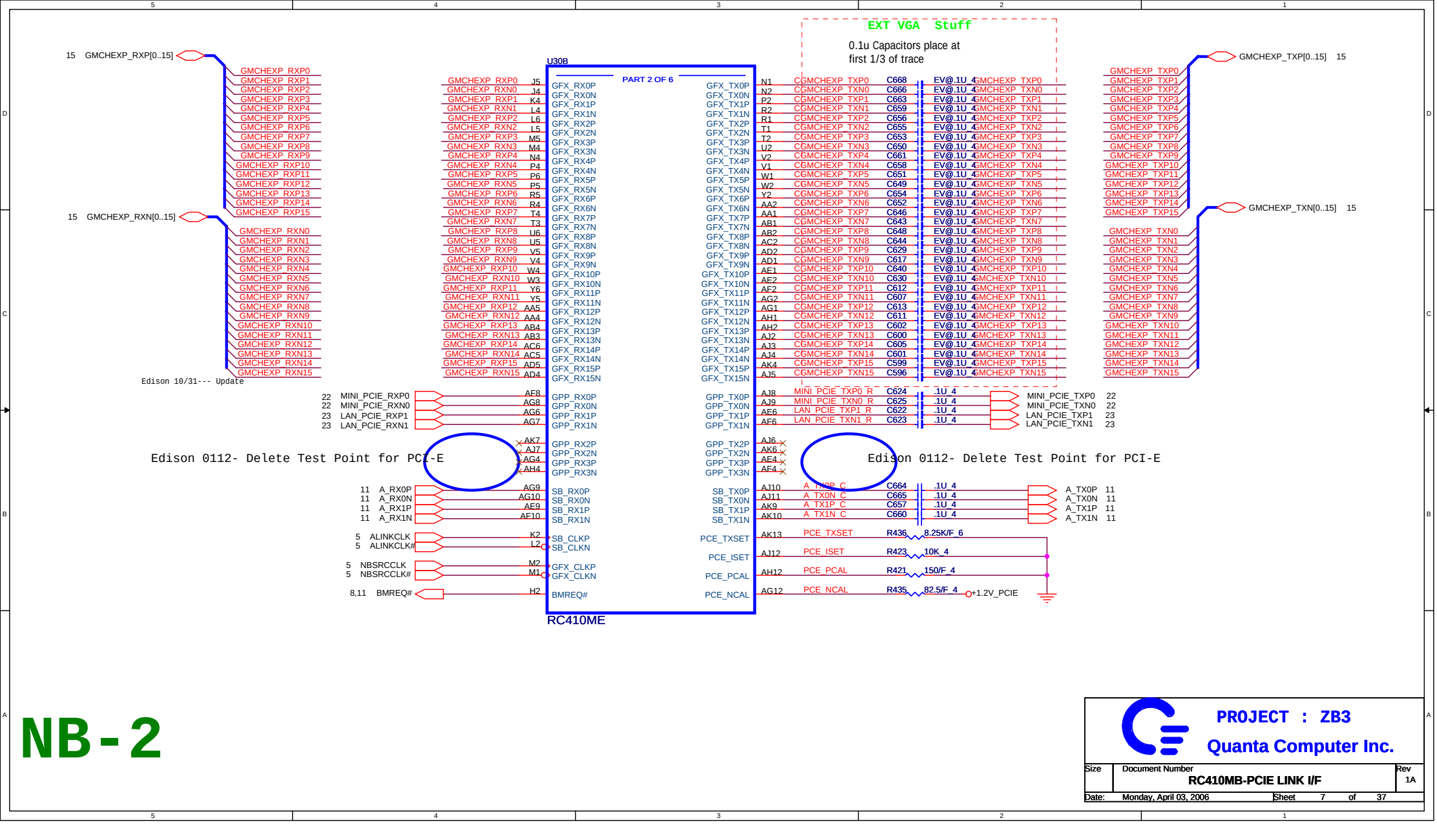
MPVSS need to connect to GND plane immediately through a dedicated VIA
Place close to NB
Use 10/10 width/space
Place close to NB



NB-2

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Quanta Computer Inc.

Size	Document Number	Rev
	RC410MB-PCIE LINK I/F	1A
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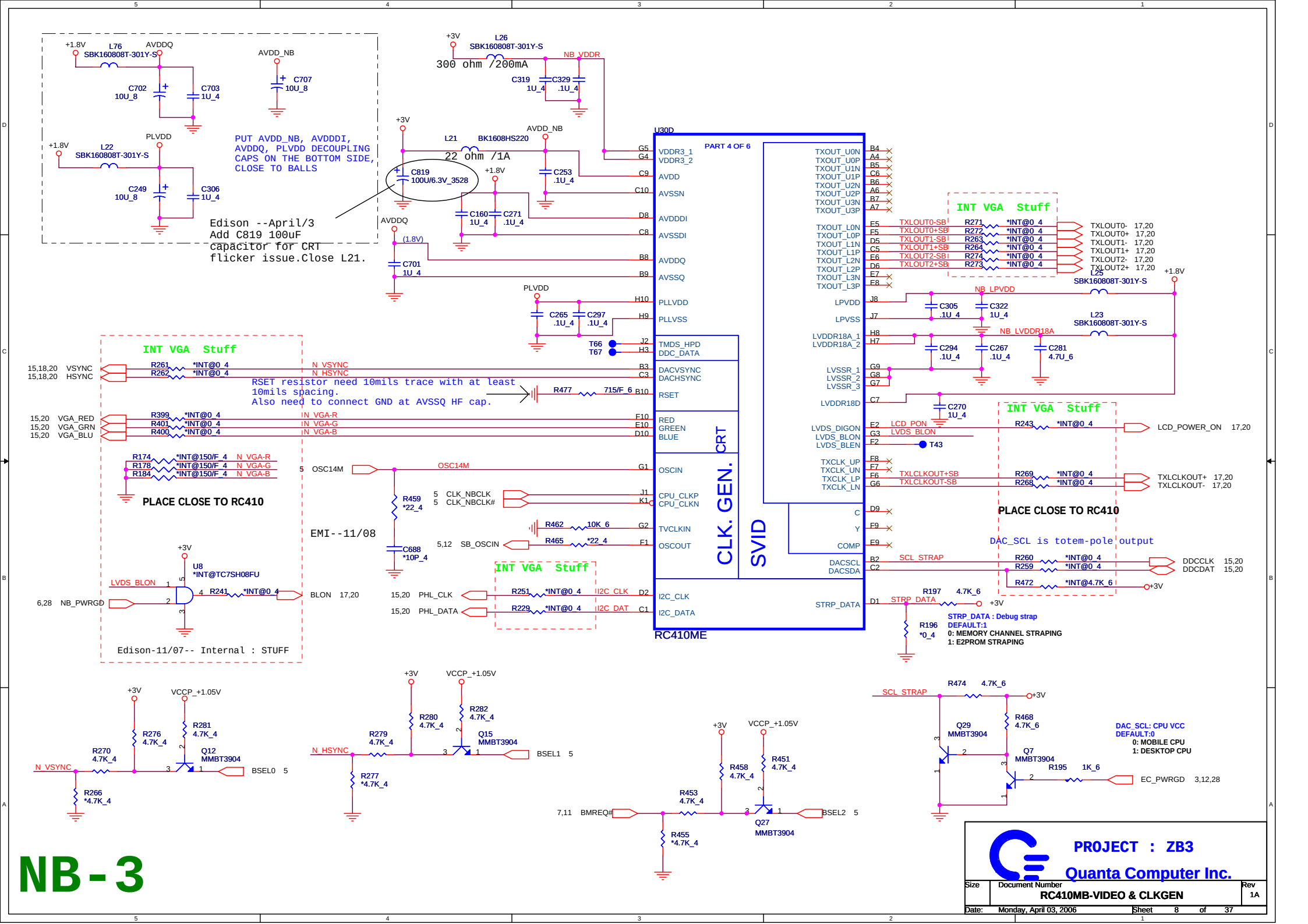
+1.8V
L76
SBK160808T-301Y-S
AVDDQ
C702
10U_8
C703
1U_4
AVDD_NB
C707
10U_8
PLVDD
L22
SBK160808T-301Y-S
C249
10U_8
C306
1U_4
PUT AVDD_NB, AVDDDI, AVDDQ, PLVDD DECOUPLING CAPS ON THE BOTTOM SIDE, CLOSE TO BALLS
Edison --April/3
Add C819 100uF
capacitor for CRT
flicker issue.Close L21.
+3V
L26
SBK160808T-301Y-S
300 ohm /200mA
NB_VDDR
C319
1U_4
C329
.1U_4
L21
BK1608HS220
22 ohm /1A
C819
100U/6.3V_3528
C253
.1U_4
C160
1U_4
C271
.1U_4
C701
1U_4
C265
.1U_4
C297
.1U_4
T66
T67
U30D
PART 4 OF 6
VDDR3_1
VDDR3_2
AVDD
AVSSN
AVDDDI
AVSSDI
AVDDQ
AVSSQ
PLLVDD
PLLVSS
TMDS_HPD
DDC_DATA
DACVSYNC
DACHSYNC
RSET
RED
GREEN
BLUE
OSCIN
CPU_CLKP
CPU_CLKN
TVCLKIN
OSCOUT
I2C_CLK
I2C_DATA
CLK. GEN.
CRT
SVID
C
Y
COMP
DACSCL
DACSDA
STRP_DATA
TXOUT_U0N
TXOUT_U0P
TXOUT_U1N
TXOUT_U1P
TXOUT_U2N
TXOUT_U2P
TXOUT_U3N
TXOUT_U3P
TXOUT_L0N
TXOUT_L0P
TXOUT_L1N
TXOUT_L1P
TXOUT_L2N
TXOUT_L2P
TXOUT_L3N
TXOUT_L3P
LPVDD
LPVSS
LVDDR18A_1
LVDDR18A_2
LVSSR_1
LVSSR_2
LVSSR_3
LVDDR18D
LVDS_DIGON
LVDS_BLON
LVDS_BLEN
TXCLK_UP
TXCLK_UN
TXCLK_LP
TXCLK_LN
RC410ME
INT VGA Stuff
R271
R272
R263
R264
R274
R273
*INT@0_4
TXLOUT0- 17,20
TXLOUT0+ 17,20
TXLOUT1- 17,20
TXLOUT1+ 17,20
TXLOUT2- 17,20
TXLOUT2+ 17,20
L25
SBK160808T-301Y-S
NB_LPVDD
C305
.1U_4
C322
1U_4
L23
SBK160808T-301Y-S
NB_LVDDR18A
C294
.1U_4
C267
.1U_4
C281
4.7U_6
C270
1U_4
INT VGA Stuff
R243
LCD_POWER_ON 17,20
LCD_PON
LVDS_BLON
T43
R269
R268
TXLCLKOUT+ 17,20
TXLCLKOUT- 17,20
PLACE CLOSE TO RC410
DAC_SCL is totem-pole output
SCL_STRAP
R260
R259
R472
DDCCLK 15,20
DDCDAT 15,20
R197 4.7K_6
STRP_DATA
R196
*0_4
STRP_DATA : Debug strap
DEFAULT:1
0: MEMORY CHANNEL STRAPING
1: E2PROM STRAPING
INT VGA Stuff
15,18,20 VSYNC
15,18,20 HSYNC
R261
R262
N_VSYNC
N_HSYNC
RSET resistor need 10mils trace with at least 10mils spacing.
Also need to connect GND at AVSSQ HF cap.
R477
715/F_6
15,20 VGA_RED
15,20 VGA_GRN
15,20 VGA_BLU
R399
R401
R400
N_VGA-R
N_VGA-G
N_VGA-B
R174
R178
R184
*INT@150/F_4
PLACE CLOSE TO RC410
5 OSC14M
OSC14M
R459
*22_4
5 CLK_NBCLK
5 CLK_NBCLK#
EMI--11/08
R462
10K_6
R465
*22_4
5,12 SB_OSCIN
C688
*10P_4
U8
*INT@TC7SH08FU
LVDS_BLON
6,28 NB_PWRGD
R241
BLON 17,20
INT VGA Stuff
15,20 PHL_CLK
15,20 PHL_DATA
R251
R229
I2C_CLK
I2C_DAT
Edison-11/07-- Internal : STUFF
+3V
VCCP_+1.05V
R276
4.7K_4
R281
4.7K_4
R270
4.7K_4
Q12
MMBT3904
N_VSYNC
BSEL0 5
R266
*4.7K_4
R280
4.7K_4
R282
4.7K_4
R279
4.7K_4
Q15
MMBT3904
N_HSYNC
BSEL1 5
R277
*4.7K_4
R458
4.7K_4
R451
4.7K_4
R453
4.7K_4
7,11 BMREQ#
BSEL2 5
R455
*4.7K_4
Q27
MMBT3904
R474 4.7K_6
SCL_STRAP
R468
4.7K_6
Q29
MMBT3904
Q7
MMBT3904
R195 1K_6
EC_PWRGD 3,12,28
DAC_SCL: CPU VCC
DEFAULT:0
0: MOBILE CPU
1: DESKTOP CPU
NB-3
PROJECT : ZB3
Quanta Computer Inc.
Size
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RC410MB-VIDEO & CLKGEN
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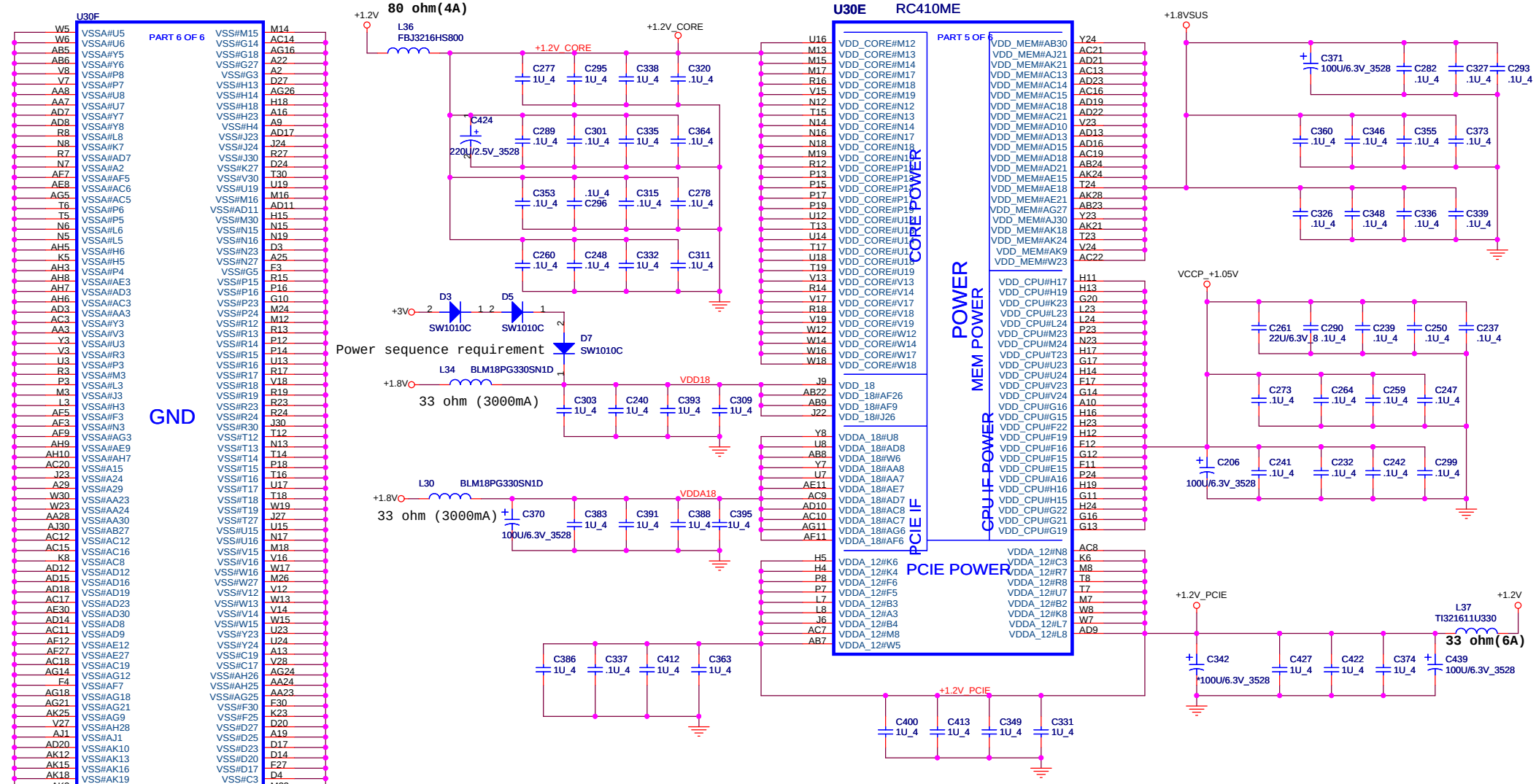

NB-4

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Quanta Computer Inc.

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	RC410MB-POWER	1A

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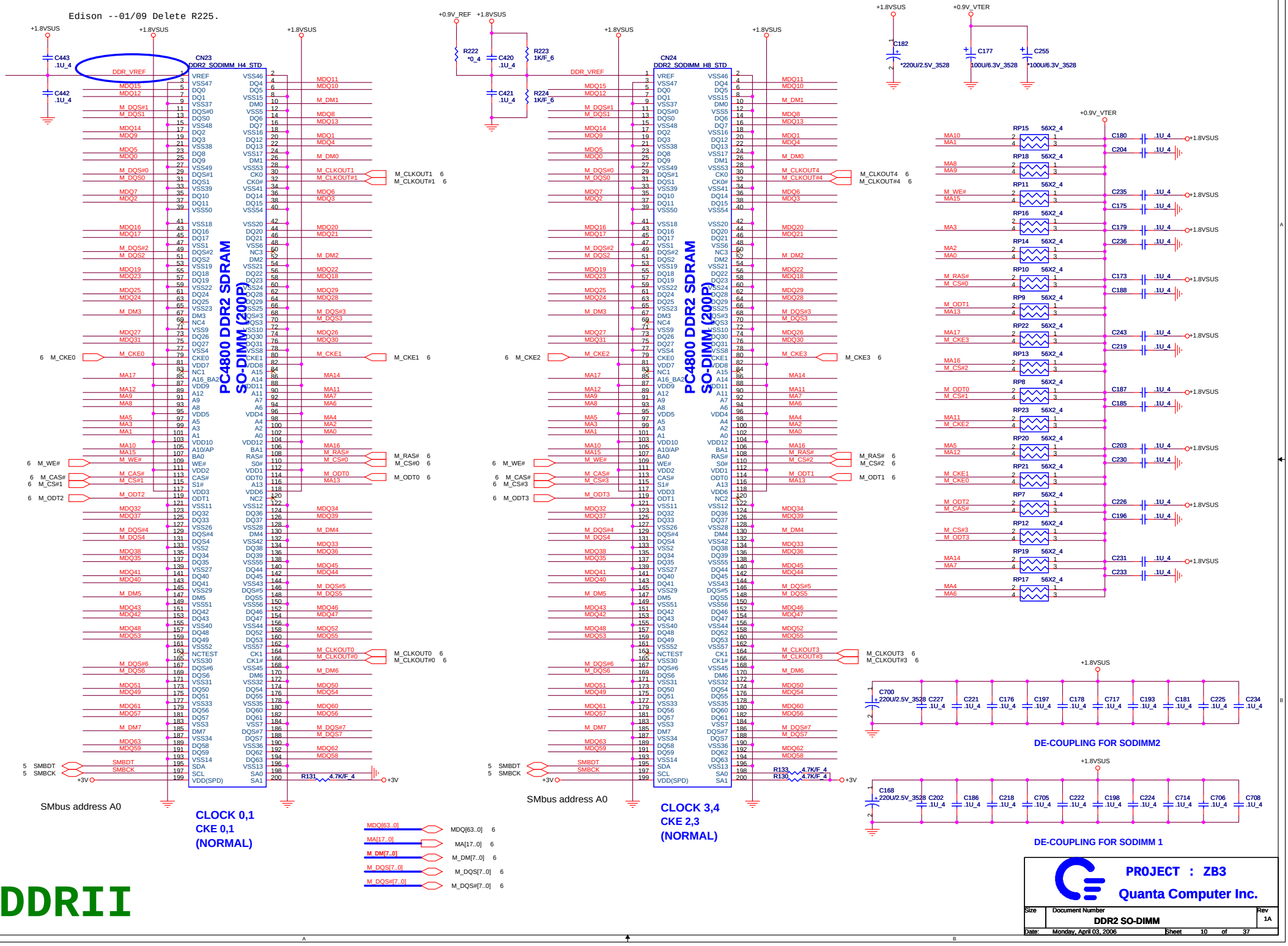
Edison --01/09 Delete R225.



DDRII

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	DDR2 SO-DIMM	1A
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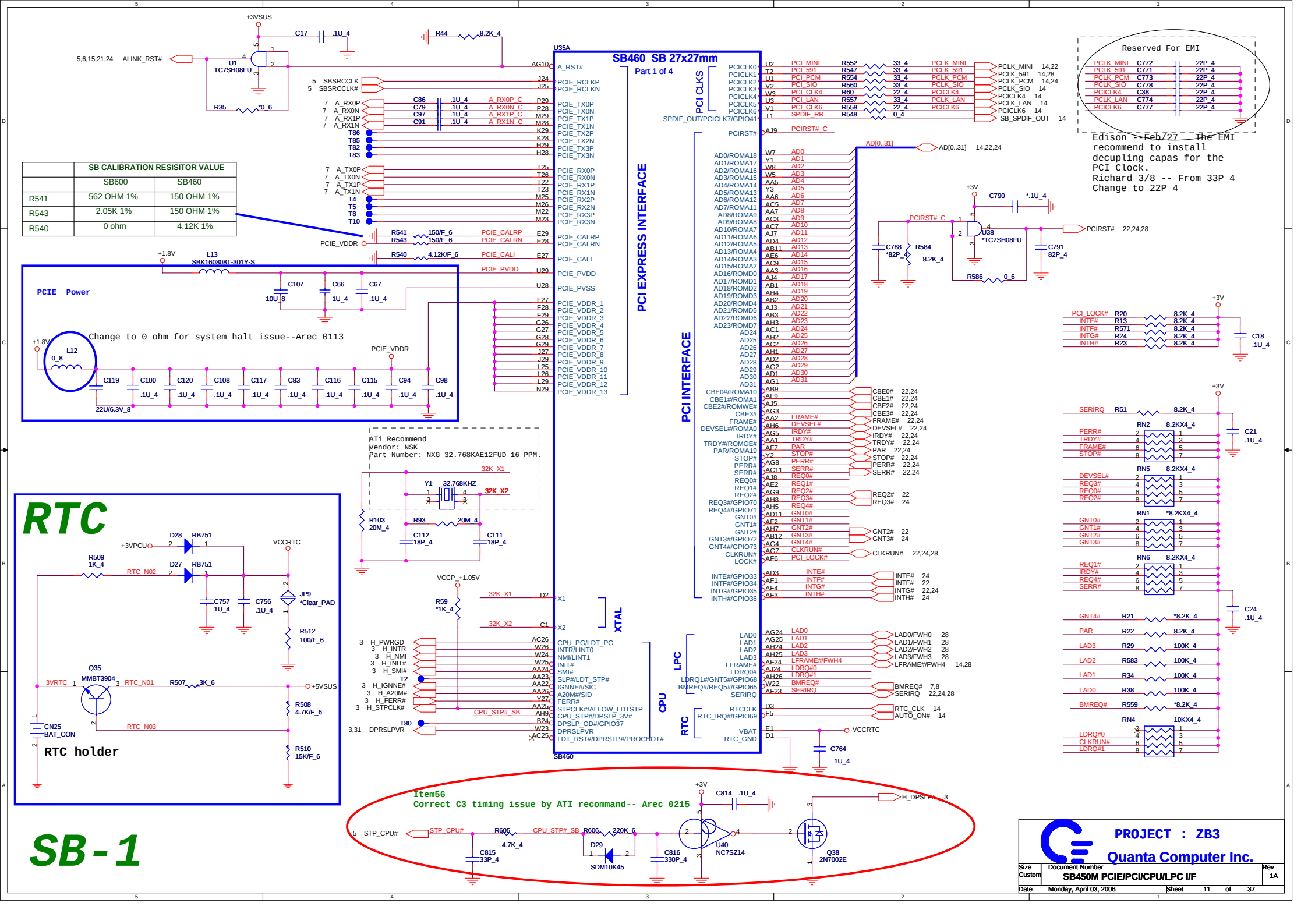
SB460 SB 27x27mm
Part 1 of 4
U35A
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
LPC
CPU
RTC
XTAL
SB460
SB CALIBRATION RESISITOR VALUE
SB600
SB460
R541 562 OHM 1% 150 OHM 1%
R543 2.05K 1% 150 OHM 1%
R540 0 ohm 4.12K 1%
PCIE Power
Change to 0 ohm for system halt issue--Arec 0113
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM
RTC
RTC holder
Item56
Correct C3 timing issue by ATI recommand-- Arec 0215
Reserved For EMI
Edison --Feb/27 -- The EMI recommend to install decupling capas for the PCI Clock.
Richard 3/8 -- From 33P_4 Change to 22P_4
SB-1
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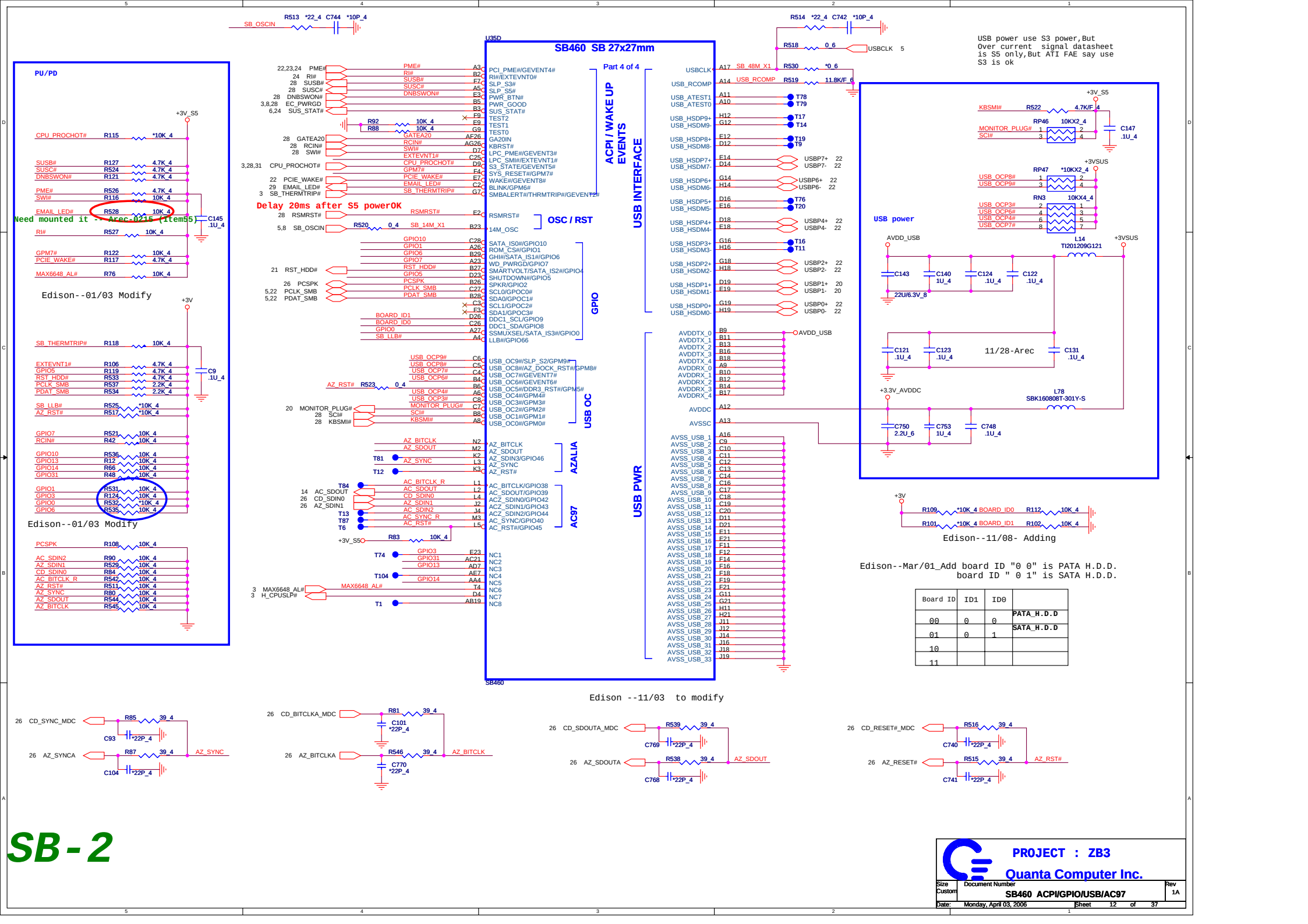
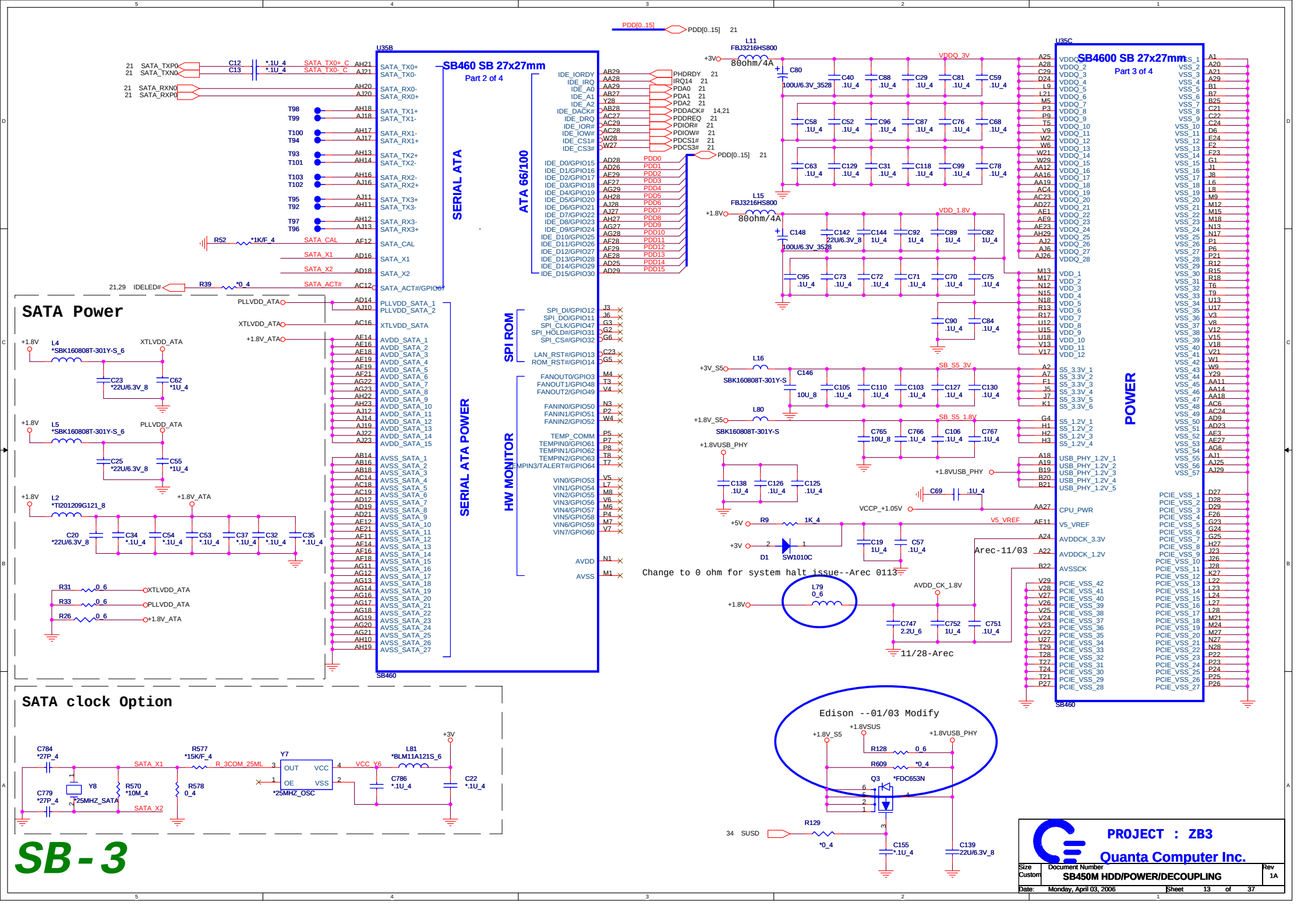
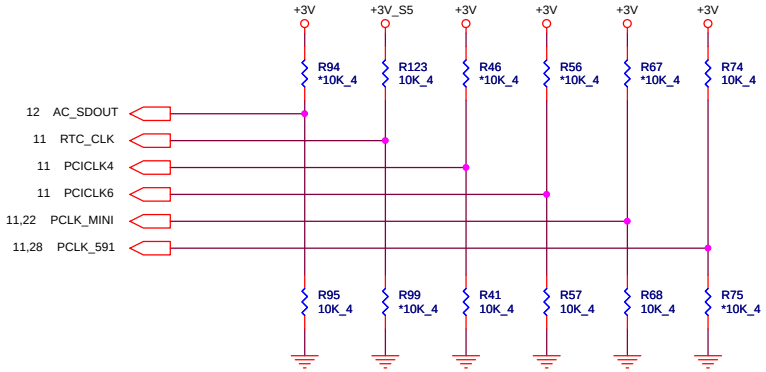
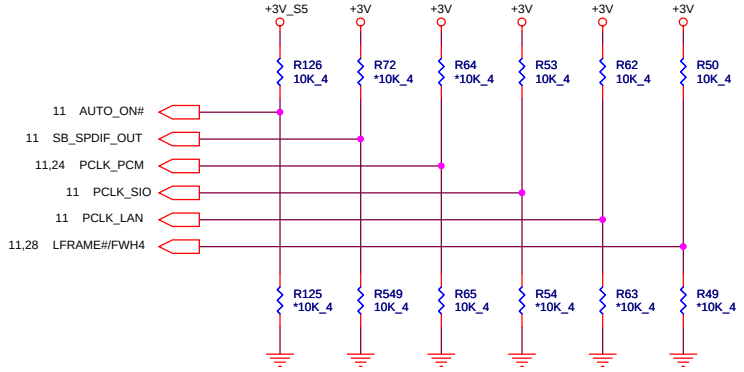
Quanta Computer Inc.
SB450M PCIE/PCI/CPU/LPC I/F
Monday, April 03, 2006


PU/PD
+3V_S5
CPU_PROCHOT# R115 *10K_4
SUSB# R127 4.7K_4
SUSC# R524 4.7K_4
DNBSWON# R121 4.7K_4
PME# R526 4.7K_4
SWI# R116 10K_4
EMAIL_LED# R528 10K_4
C145 .1U_4
Need mounted it -- Arec-0215 (item55)
R#
R527 10K_4
GPM7# R122 10K_4
PCIE_WAKE# R117 4.7K_4
MAX6648_AL# R76 10K_4
Edison--01/03 Modify
+3V
SB_THERMTRIP# R118 10K_4
EXTEVNT1# R106 4.7K_4
GPIO5 R119 4.7K_4
RST_HDD# R533 4.7K_4
PCLK_SMB R537 2.2K_4
PDAT_SMB R534 2.2K_4
C9 .1U_4
SB_LLB# R525 *10K_4
AZ_RST# R517 *10K_4
GPIO7 R521 10K_4
RCIN# R42 10K_4
GPIO10 R536 10K_4
GPIO13 R12 10K_4
GPIO14 R66 10K_4
GPIO31 R48 10K_4
GPIO1 R531 10K_4
GPIO3 R124 10K_4
GPIO0 R532 *10K_4
GPIO6 R535 10K_4
Edison--01/03 Modify
PCSPK R108 10K_4
AC_SDIN2 R90 10K_4
AZ_SDIN1 R529 10K_4
CD_SDIN0 R84 10K_4
AC_BITCLK_R R542 10K_4
AZ_RST# R511 10K_4
AZ_SYNC R80 10K_4
AZ_SDOUT R544 10K_4
AZ_BITCLK R545 10K_4
SB_OSCIN
R513 *22_4 C744 *10P_4
U35D
SB460 SB 27x27mm
Part 4 of 4
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN
KBRST#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
ACPI / WAKE UP EVENTS
22,23,24 PME#
24 RI#
28 SUSB#
28 SUSC#
28 DNBSWON#
3,8,28 EC_PWRGD
6,24 SUS_STAT#
R92 10K_4
R88 10K_4
28 GATEA20
28 RCIN#
28 SWI#
3,28,31 CPU_PROCHOT#
22 PCIE_WAKE#
29 EMAIL_LED#
3 SB_THERMTRIP#
Delay 20ms after S5 powerOK
RSMRST#
28 RSMRST#
OSC / RST
5,8 SB_OSCIN
R520 0_4 SB_14M_X1
14M_OSC
USB INTERFACE
GPIO
SATA_IS0#/GPIO10
ROM_CS#/GPIO1
GHI#/SATA_IS1#/GPIO6
WD_PWRGD/GPIO7
SMARTVOLT/SATA_IS2#/GPIO4
SHUTDOWN#/GPIO5
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
SSMUXSEL/SATA_IS3#/GPIO0
LLB#/GPIO66
21 RST_HDD#
26 PCSPK
5,22 PCLK_SMB
5,22 PDAT_SMB
BOARD_ID1
BOARD_ID0
GPIO0
SB_LLB#
USB OC
USB_OC9#/SLP_S2/GPM9#
USB_OC8#/AZ_DOCK_RST#/GPM8#
USB_OC7#/GEVENT7#
USB_OC6#/GEVENT6#
USB_OC5#/DDR3_RST#/GPM5#
USB_OC4#/GPM4#
USB_OC3#/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_RST# R523 0_4
20 MONITOR_PLUG#
28 SCI#
28 KBSMI#
AZALIA
AZ_BITCLK
AZ_SDOUT
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
T81
T12
AC97
AC_BITCLK_R
AC_SDOUT
CD_SDIN0
AZ_SDIN1
AC_SDIN2
AC_SYNC_R
AC_RST#
AC_BITCLK/GPIO38
AC_SDOUT/GPIO39
ACZ_SDIN0/GPIO42
ACZ_SDIN1/GPIO43
ACZ_SDIN2/GPIO44
AC_SYNC/GPIO40
AC_RST#/GPIO45
T84
T13
T87
T6
14 AC_SDOUT
26 CD_SDIN0
26 AZ_SDIN1
+3V_S5
R83 10K_4
T74
T104
T1
GPIO3
GPIO31
GPIO13
GPIO14
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
3 MAX6648_AL#
3 H_CPUSLP#
MAX6648_AL#
SB460
USB PWR
USBCLK
USB_RCOMP
USB_ATEST1
USB_ATEST0
USB_HSDP9+
USB_HSDM9-
USB_HSDP8+
USB_HSDM8-
USB_HSDP7+
USB_HSDM7-
USB_HSDP6+
USB_HSDM6-
USB_HSDP5+
USB_HSDM5-
USB_HSDP4+
USB_HSDM4-
USB_HSDP3+
USB_HSDM3-
USB_HSDP2+
USB_HSDM2-
USB_HSDP1+
USB_HSDM1-
USB_HSDP0+
USB_HSDM0-
AVDDTX_0
AVDDTX_1
AVDDTX_2
AVDDTX_3
AVDDTX_4
AVDDRX_0
AVDDRX_1
AVDDRX_2
AVDDRX_3
AVDDRX_4
AVDDC
AVSSC
AVSS_USB_1
AVSS_USB_2
AVSS_USB_3
AVSS_USB_4
AVSS_USB_5
AVSS_USB_6
AVSS_USB_7
AVSS_USB_8
AVSS_USB_9
AVSS_USB_10
AVSS_USB_11
AVSS_USB_12
AVSS_USB_13
AVSS_USB_14
AVSS_USB_15
AVSS_USB_16
AVSS_USB_17
AVSS_USB_18
AVSS_USB_19
AVSS_USB_20
AVSS_USB_21
AVSS_USB_22
AVSS_USB_23
AVSS_USB_24
AVSS_USB_25
AVSS_USB_26
AVSS_USB_27
AVSS_USB_28
AVSS_USB_29
AVSS_USB_30
AVSS_USB_31
AVSS_USB_32
AVSS_USB_33
R514 *22_4 C742 *10P_4
R518 0_6 USBCLK 5
A17 SB_48M_X1
R530 *0_6
A14 USB_RCOMP
R519 11.8K/F_6
T78
T79
T17
T14
T19
T9
T76
T20
T16
T11
T18
T10
USBP7+ 22
USBP7- 22
USBP6+ 22
USBP6- 22
USBP4+ 22
USBP4- 22
USBP2+ 22
USBP2- 22
USBP1+ 20
USBP1- 20
USBP0+ 22
USBP0- 22
AVDD_USB
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok
USB power
+3V_S5
KBSMI# R522 4.7K/F_4
RP46 10KX2_4
MONITOR_PLUG#
SCI#
C147 .1U_4
+3VSUS
RP47 *10KX2_4
USB_OCP8#
USB_OCP9#
RN3 10KX4_4
USB_OCP3#
USB_OCP6#
USB_OCP4#
USB_OCP7#
AVDD_USB
L14 TI201209G121
+3VSUS
C143
C140 1U_4
C124 .1U_4
C122 .1U_4
22U/6.3V_8
C121 .1U_4
C123 .1U_4
11/28-Arec
C131 .1U_4
+3.3V_AVDDC
L78 SBK160808T-301Y-S
C750 2.2U_6
C753 1U_4
C748 .1U_4
+3V
R109 *10K_4 BOARD_ID0
R112 10K_4
R101 *10K_4 BOARD_ID1
R102 10K_4
Edison--11/08- Adding
Edison--Mar/01_Add board ID "0 0" is PATA H.D.D.
board ID " 0 1" is SATA H.D.D.
Board ID | ID1 | ID0
00 | 0 | 0 | PATA_H.D.D
01 | 0 | 1 | SATA_H.D.D
10
11
Edison --11/03 to modify
26 CD_SYNC_MDC
R85 39_4
C93 *22P_4
26 AZ_SYNCA
R87 39_4
C104 *22P_4
AZ_SYNC
26 CD_BITCLKA_MDC
R81 39_4
C101 *22P_4
26 AZ_BITCLKA
R546 39_4
C770 *22P_4
AZ_BITCLK
26 CD_SDOUTA_MDC
R539 39_4
C769 *22P_4
26 AZ_SDOUTA
R538 39_4
C768 *22P_4
AZ_SDOUT
26 CD_RESET#_MDC
R516 39_4
C740 *22P_4
26 AZ_RESET#
R515 39_4
C741 *22P_4
AZ_RST#
SB-2
PROJECT : ZB3
Quanta Computer Inc.
Size Custom
Document Number
SB460 ACPI/GPIO/USB/AC97
Rev 1A
Date: Monday, April 03, 2006
Sheet 12 of 37


SB460 SB 27x27mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SATA Power
SATA clock Option
SB460 SB 27x27mm
Part 3 of 4
POWER
Change to 0 ohm for system halt issue--Arec 0113
Arec-11/03
11/28-Arec
Edison --01/03 Modify
PROJECT : ZB3
Quanta Computer Inc.
SB450M HDD/POWER/DECOUPLING
Monday, April 03, 2006
SB-3



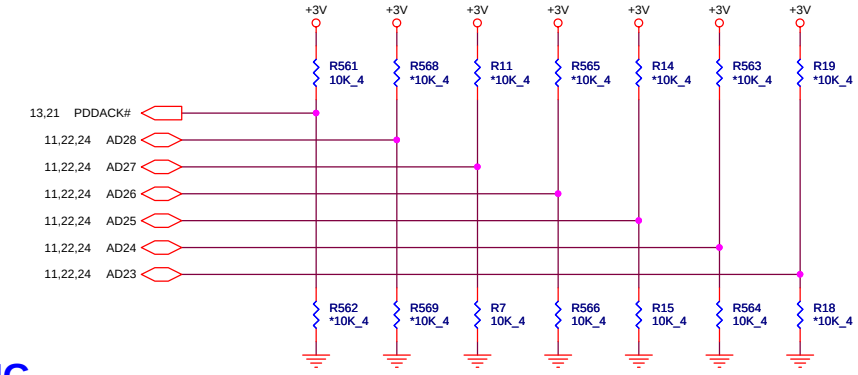


REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591
					PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]

	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

Edison-11/07-- Modify



DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

SB-4

PROJECT : ZB3

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB450M STRAPS	1A
Date: Monday, April 03, 2006	Sheet 14 of 37	

NOTE: some of the PCIE testpoints will be available trought via on traces.

MEMORY CLOCK SPREAD SPECTRUM

S0: H = -2.5%
S0: X = -0.6% (Default)
S0: L = -1.8%

PUT THEM CLOSE TO X'TAL

VGA H/W MONITOR

15 MIL

10 mil trace / 10 mil space

Close to pin ASIC

SLAVE ADDRESS: 9A

Edison -0111--
Detele resistor
R267,R278

POWERPLAY

HI: LOW CORE VOLTAGE FOR BATTERY MODE
LO: HIGH CORE VOLTAGE FOR PERFORMANCE MODE

VRAM TYPE STRAP PINS

PLACE CLOSE TO ASIC

PROJECT :	ZB3
Quanta Computer Inc.	
Size	Document Number: M52-P_MAIN_PCIE (1 of 4) Rev: 00
Date:	Thursday, April 06, 2006 Sheet 15 of 37

RV410 MEMORY CHANNELS A and B

Channel B

19 MDA[0..63]

Z= 50 ohm

U29D

Part 4 of 7

MEMORY INTERFACE B

EV@M52(M54)

MAA[0..15] 19

MAIN TRUNK: Z= 35 ohm
BRACHES: Z= 55 ohm

-DQMA[0..7] 19

Z= 50 ohm

RDQSA[0..7] 19

Z= 50 ohm

WDQSA[0..7] 19

Z= 50 ohm

Z= 100 ohm

Z= 55 ohm

+1.8V

R482 EV@100/F_4

VRAM_REF0

R483 EV@100/F_4

C715 EV@.1U_4

+1.8V

R162 EV@100/F_4

VRAM_REF1

R176 EV@100/F_4

C223 EV@.1U_4

TEST_MCLK

TEST_YCLK

R208 EV@4.7K_4

R449 EV@4.7K_4

R205 EV@243/F_4

Channel A

U29C

Part 3 of 7

MEMORY INTERFACE A

EV@M52(M54)

U29F

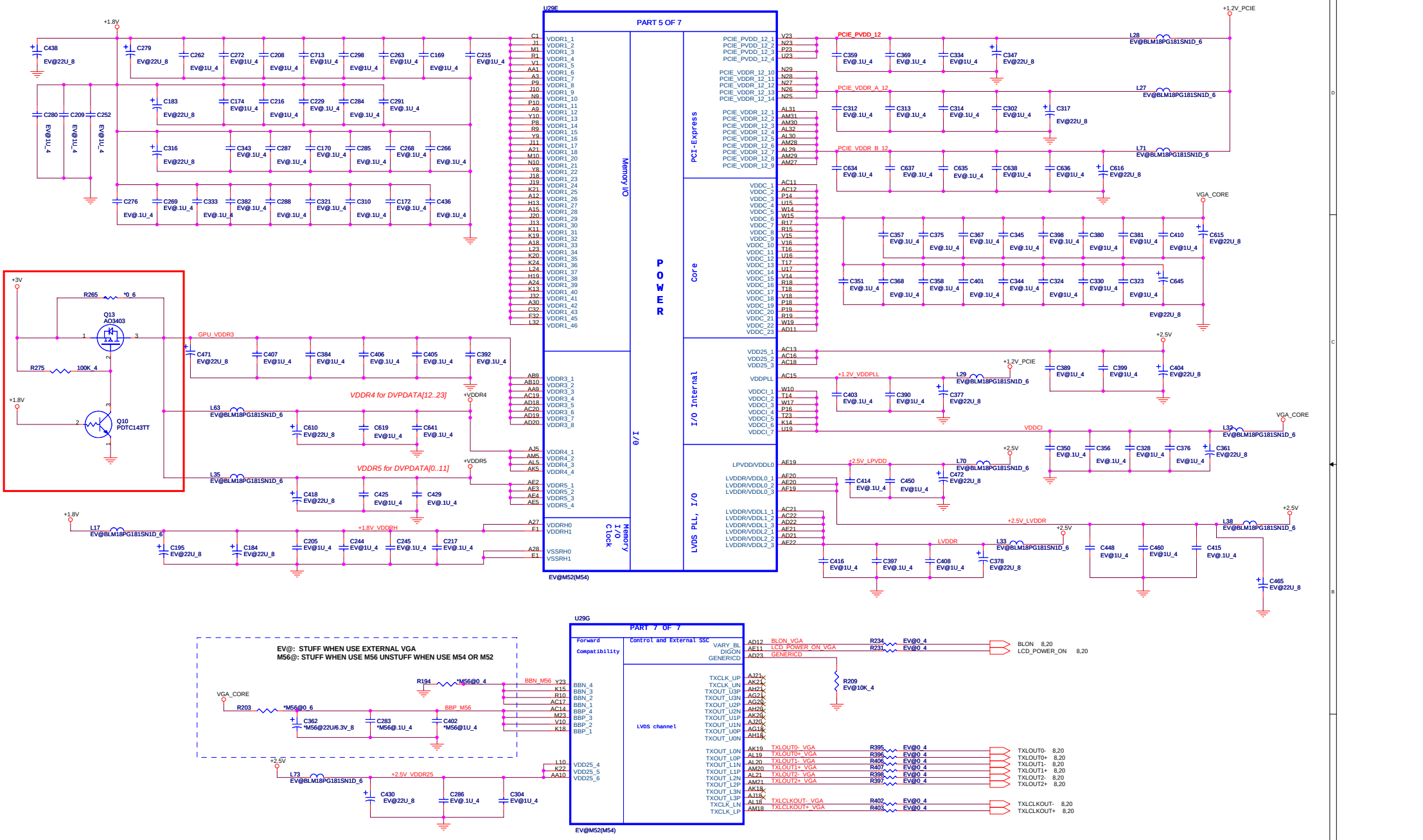
Part 6 of 7

PCI-Express GND

EV@BLM18PG181SN1D_6

L31

CORE GND



PROJECT : ZB3			
Quanta Computer Inc.			
Size	Document Number		Rev
	M52-P_Power_LVDS(3 of 4)		00
Date: Monday, April 03, 2006	Sheet 17 of 37		

OPTION STRAPS

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground ↓ High logic voltage

Signal

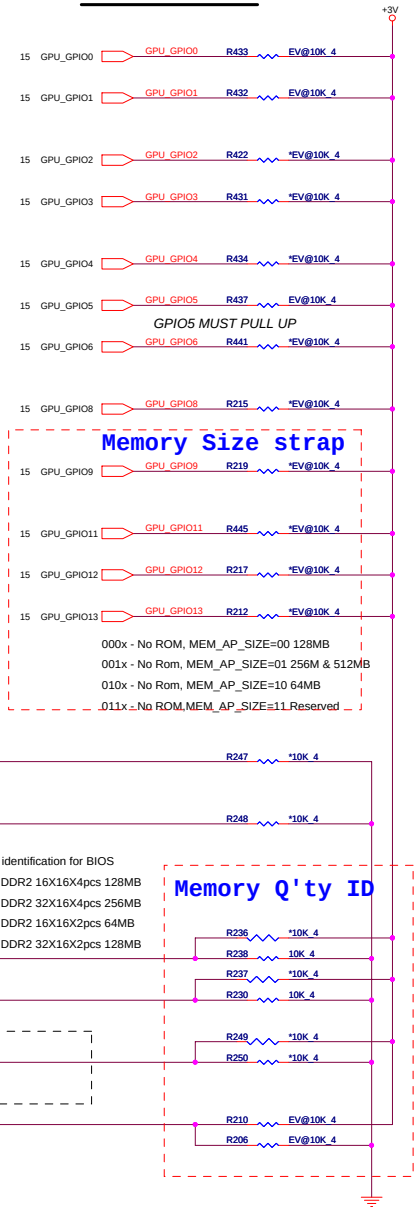
Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.

Vendor P/N	QCI P/N	Size	GPU_GPIO13	GPU_GPIO12	MEMTYP_1	MEMTYP_0
HYB18T256161AFL25	AKD5JG-T^00	**16M*16 *4pcs (128MB)**	0	0	0	0
HY5PS561621AFP-25	AKD5JG-TW12					
K4N56163QG-ZC25	AKD5JG-T514					
HYB18T512161BF-25	AKD5FG-T^00	32M*16 *2pcs (128MB)	0	0	1	1
HY5PS121621BFP-25	AKD5FG-TW14	**32M*16 *4pcs (256MB)**	0	1	0	1
K4N51163QC-ZC25	AKD5FGBT501					

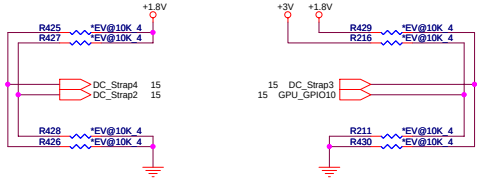
(Default setting)

```
Memory Aperture Size Select
When no ROM is attached, GPIO_9 is set to 0
GPIO_[13:12] is used to select the memory aperture size.
GPIO_[13:12] = 00: 128M memory aperture, same as ROM strap 00
GPIO_[13:12] = 01: 256M memory aperture, same as ROM strap 01
GPIO_[13:12] = 10: 64M memory aperture, same as ROM strap 10
GPIO_[13:12] = 11: reserved, same as ROM strap 11

Default: 128M memory aperture.
GPIO_[13:12] = 01 (256M memory aperture) recommended
for designs with 256MB or 512MB of physical memory.
```



ATI FAE: ALL N/A



M56-P Strap

STRAPS	PIN	DESCRIPTION	Board DEFAULT
TX_PWRS_ENB	GPIO0 (Internal pull-down)	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	1
TX_DEEMPH_EN	GPIO1 (Internal pull-down)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	1
	GPIO(3:2) (Internal pull-down)	RSVD	
DEBUG_ACCESS	GPIO4 (Internal pull-down)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5 (Internal pull-down)	RSVD	
	GPIO6 (Internal pull-down)	RSVD	
Force_ Compliance	GPIO8 (Internal pull-down)	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13,12,11) (Internal pull-down)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128M 001x - No Rom, MEM_AP_SIZE=01 256M 010x - No Rom, MEM_AP_SIZE=10 64M 011x - No ROM,MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	000
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYNC, V2SYNC, GENERICC	RSVD	
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

00

Board Straps

REV: 0.3

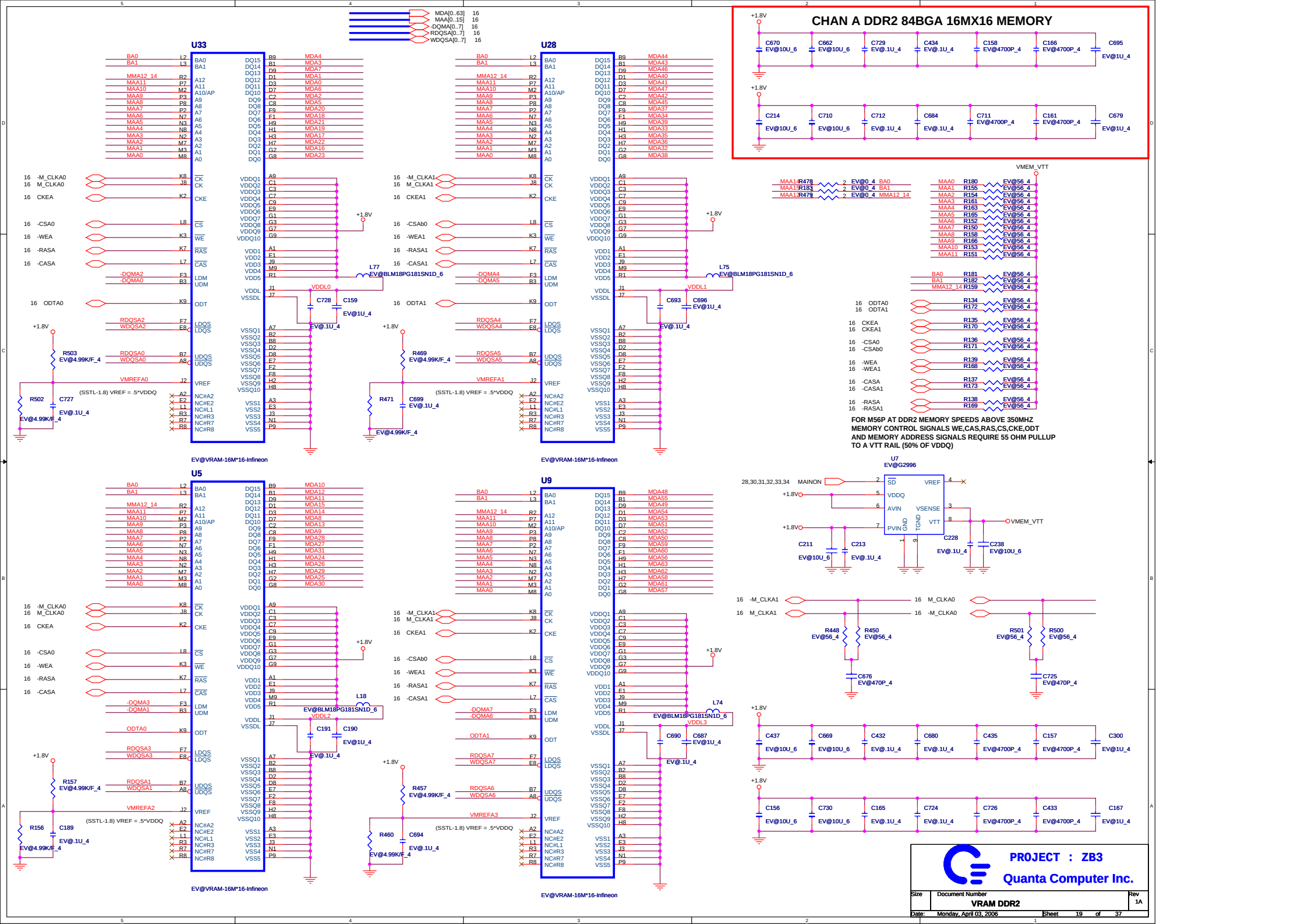
STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	DVPDATA(1:0)	Memory identification for BIOS 00 - DDR2 16X16X4pcs 128MB 01 - DDR2 32X16X4pcs 256MB 10 - DDR2 16X16X2pcs 64MB 11 - DDR2 32X16X2pcs 128MB	
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	DVPDATA13	Video Capture Enabled **0 - Disabled** 1 - Not detected	0
DC_Strap3	DVPDATA14	HDTV out detect **0 - Detected** 1 - Enabled	1
DC_Strap4, DEMUX_SEL	DVPDATA15	Video capture enable 00 - DAC2 Off **01 - DAC2 On as CRT** 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

PROJECT : ZB3

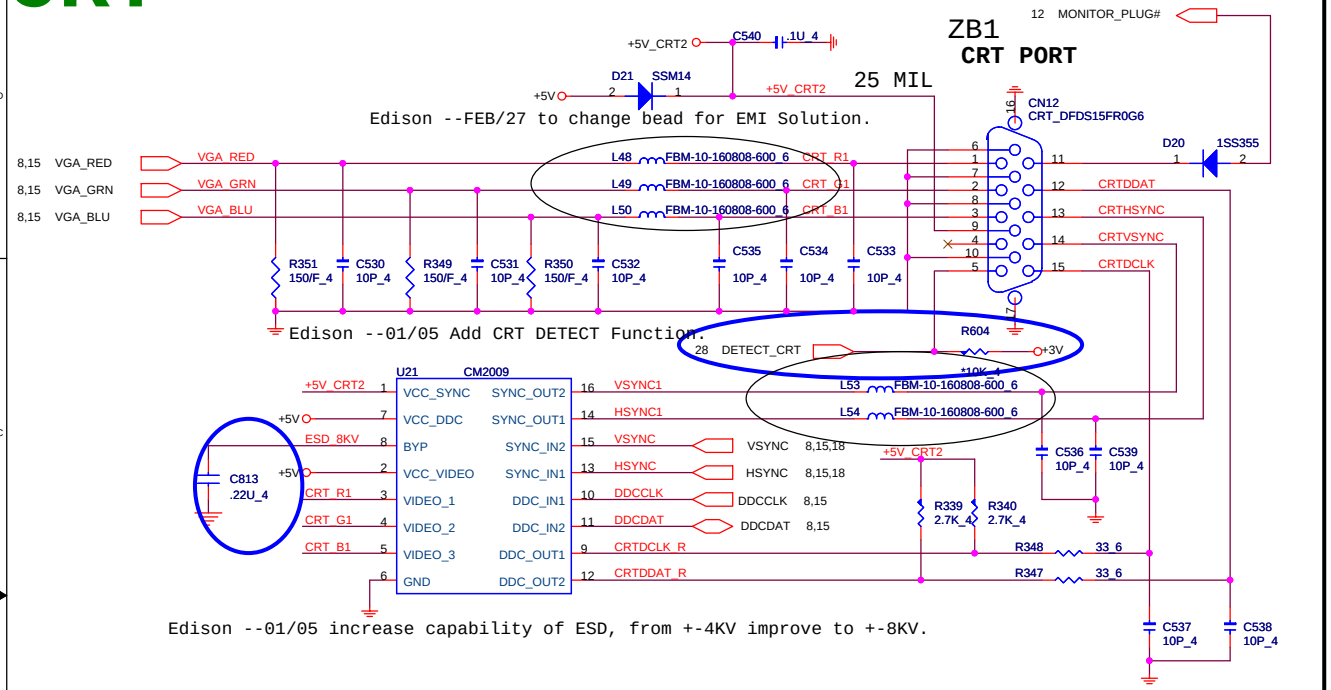
Quanta Computer Inc.

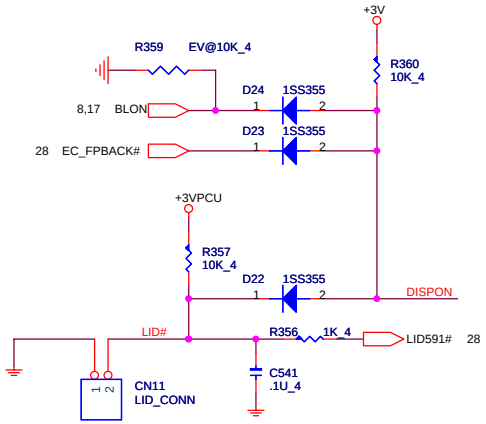
Size	Document Number	Rev
	M52-P_Straps (4 of 4)	00

Date: Monday, April 03, 2006 Sheet 18 of 37

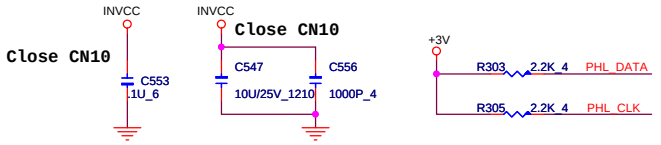

MDA[0..63] 16
MAA[0..15] 16
-DQMA[0..7] 16
RDQSA[0..7] 16
WDQSA[0..7] 16
CHAN A DDR2 84BGA 16MX16 MEMORY
U33
U28
U5
U9
EV@VRAM-16M*16-Infineon
VMEM_VTT
FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ
MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT
AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP
TO A VTT RAIL (50% OF VDDQ)
U7
EV@G2996
PROJECT : ZB3
Quanta Computer Inc.
Size
Document Number
VRAM DDR2
Rev
1A
Date: Monday, April 03, 2006
Sheet 19 of 37

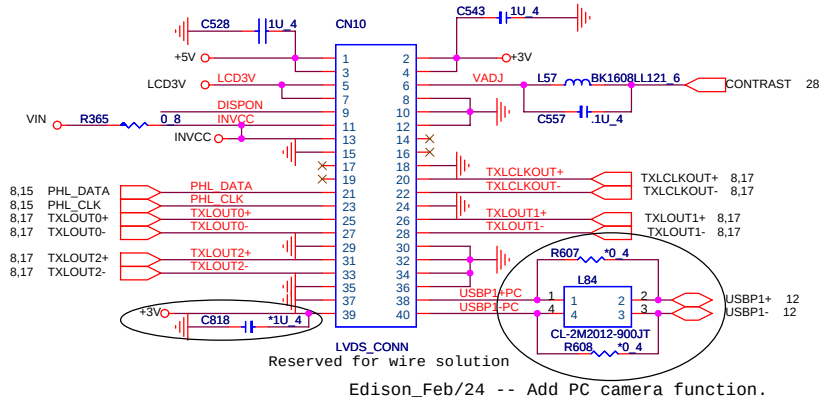
CRT

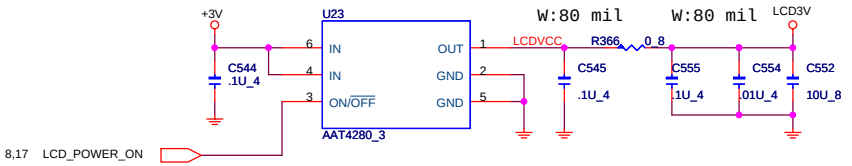




LVDS







DSC Pinout : pin1 -- VCC(+3V)
pin2 -- USB-
pin3 -- USB+
pin4 -- GND
pin5 -- Shielding
the connector is JST SM05B-SSR-H-TB

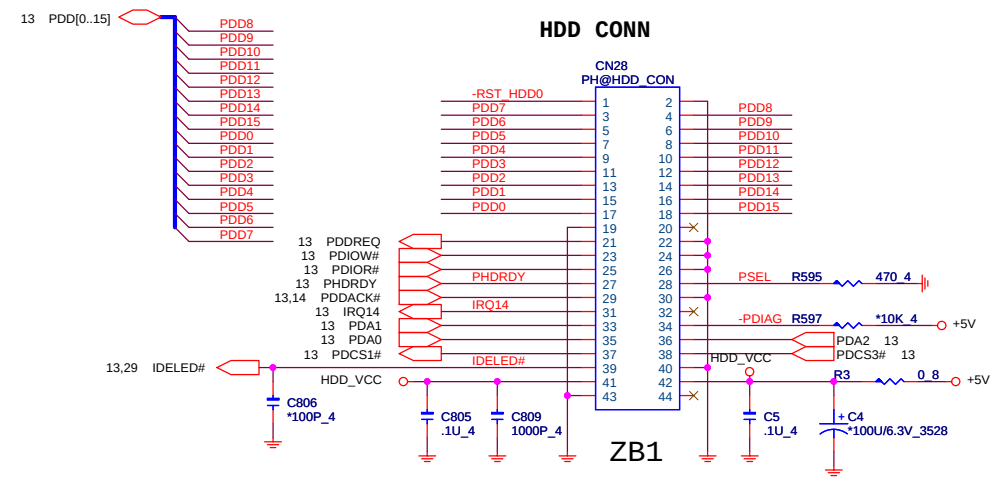
PROJECT : ZB3

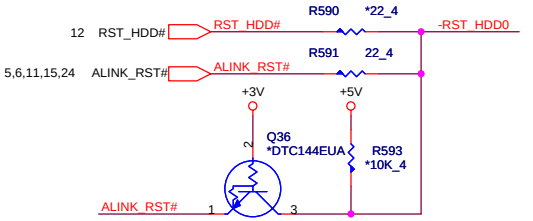
Quanta Computer Inc.

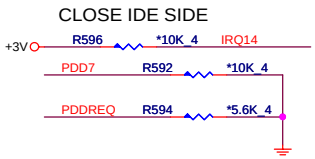
Size	Document Number	Rev
	VGA Ports, LID, & HOLES	1A
Date: Monday, April 03, 2006	Sheet 20 of 37	

IDE

HDD CONN

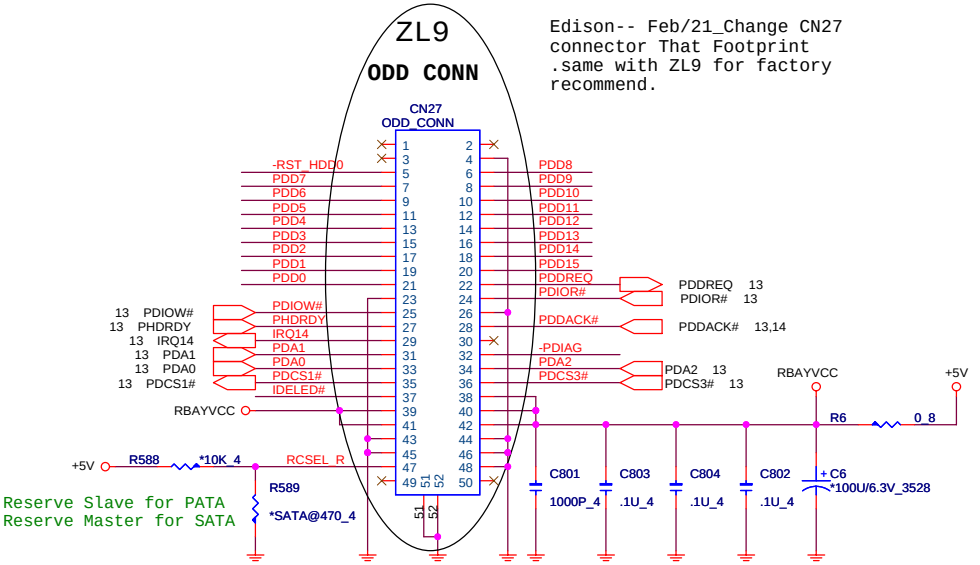


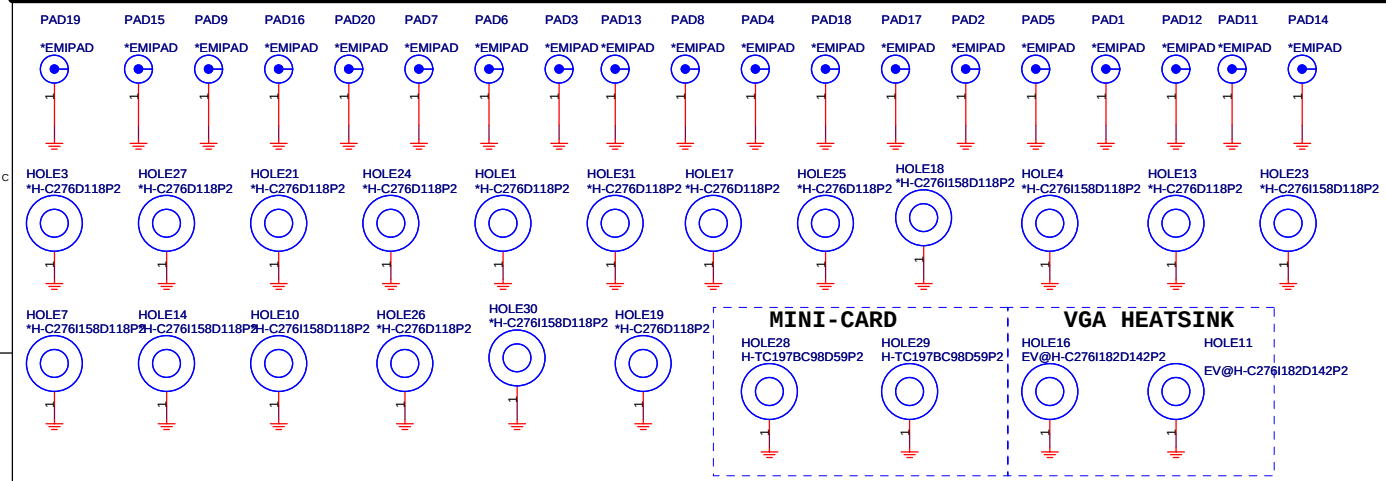




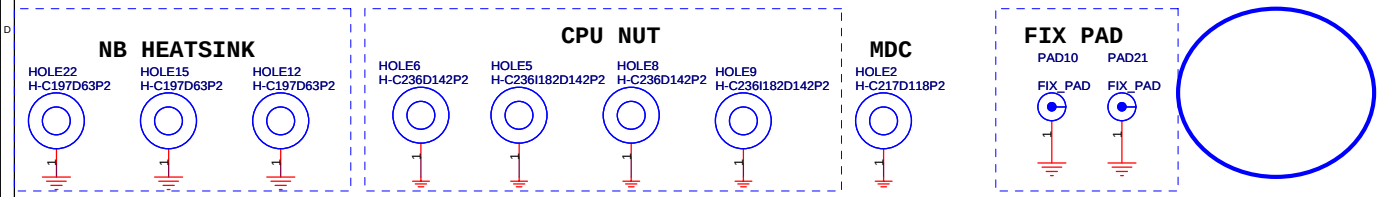
ZL9 ODD CONN

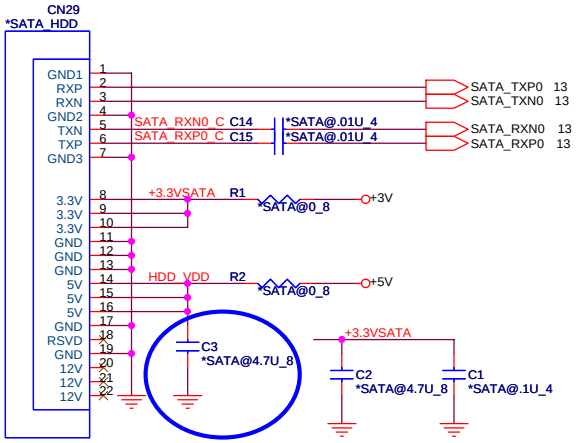
Edison-- Feb/21_Change CN27 connector That Footprint .same with ZL9 for factory recommend.

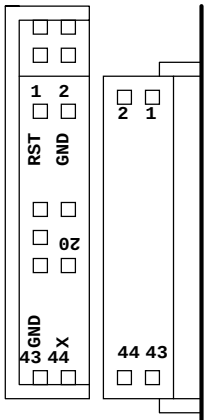




Edison 0106 - Delete PAD22 ~ PAD24.







Edison 0112 - To modify the C3 connect to HDD_VDD.

PROJECT : ZB3

Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM , HOLES	1A
Date: Monday, April 03, 2006	Sheet 21 of 37	

ID Select : AD20
Interrupt Pin : INTF# , INTG#
Request Indicate : REQ2#
Grant Indicate : GNT2#

MINI-PCI

CN18 MINIPCI

Edison ---Feb/22_ Delete the C673, C674 capacitor for PCI-E of Minicard.

Edison -0104-- Modify

Edison -0111-- Delete Resistor R439,R440,R438

Close Minicard connector

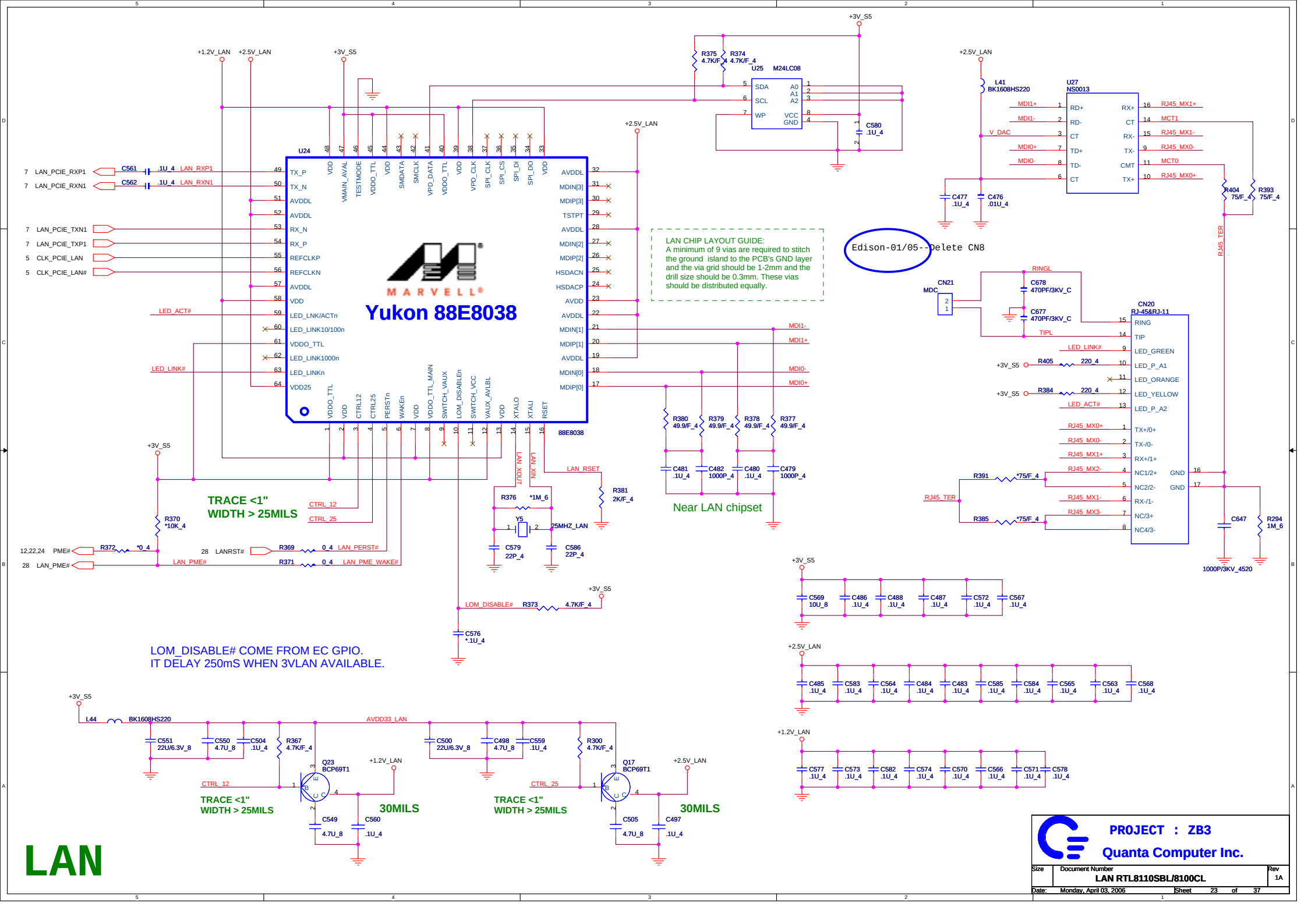
Edison--Mar/02__Add EMI solution install L52, and also delete R354,R355.

Edison--Mar/22__Add EMI solution install L51/L56, and also delete R352,R353,R362,R363.

MPC

USB

PROJECT : ZB3			
Quanta Computer Inc.			
Size	Document Number		Rev
	MINI PCI&PCI-E,USB PORT		1A
Date: Monday, April 03, 2006		Sheet 22 of 37	


Yukon 88E8038
MARVELL
U24
88E8038
U25 M24LC08
U27 NS0013
CN20 RJ-45&RJ-11
CN21
L41 BK1608HS220
L44 BK1608HS220
Q23 BCP69T1
Q17 BCP69T1
Y5 25MHZ_LAN
+1.2V_LAN
+2.5V_LAN
+3V_S5
LAN_RXP1
LAN_RXN1
LAN_PCIE_TXN1
LAN_PCIE_TXP1
CLK_PCIE_LAN
CLK_PCIE_LAN#
LED_ACT#
LED_LINK#
LAN_RSET
CTRL_12
CTRL_25
LAN_PME#
LAN_PERST#
LAN_PME_WAKE#
LOM_DISABLE#
AVDD33_LAN
MDI1-
MDI1+
MDI0-
MDI0+
RJ45_TER
RJ45_MX1+
RJ45_MX1-
RJ45_MX0-
RJ45_MX0+
MCT1
MCT0
V_DAC
RINGL
TIPL
LED_GREEN
LED_P_A1
LED_ORANGE
LED_YELLOW
LED_P_A2
TRACE <1"
WIDTH > 25MILS
30MILS
LAN CHIP LAYOUT GUIDE:
A minimum of 9 vias are required to stitch the ground island to the PCB's GND layer and the via grid should be 1-2mm and the drill size should be 0.3mm. These vias should be distributed equally.
Edison-01/05--Delete CN8
Near LAN chipset
LOM_DISABLE# COME FROM EC GPIO.
IT DELAY 250mS WHEN 3VLAN AVAILABLE.
LAN
PROJECT : ZB3
Quanta Computer Inc.
LAN RTL8110SBL/8100CL
Size
Document Number
Rev
1A
Date: Monday, April 03, 2006
Sheet 23 of 37

ID Select : AD17
Interrupt Pin : INTE#/INTG#(share)/INTH#
Request Indicate : REQ3#
Grant Indicate : GNT3#

CARDBUS SLOT
ZB1

Near Slot

CN19

U10A PCI7412

U10B PCI7412

PCI Interface

1394 Interface

Miscellaneous

CardBus Interface

UPPER PIN

LOWER PIN

CARD_BUS

Near Chipset

+3V Plane

Near Chipset

U10D PCI7412

Power/GND

Cardbus EEPROM

U6 24LC02BT 2K bit

Cardbus power switch

U11 TPS2220APWP

Near TPS2210A

Near TPS2210A

Near TPS2210A

Near TPS2210A

CARD Bus

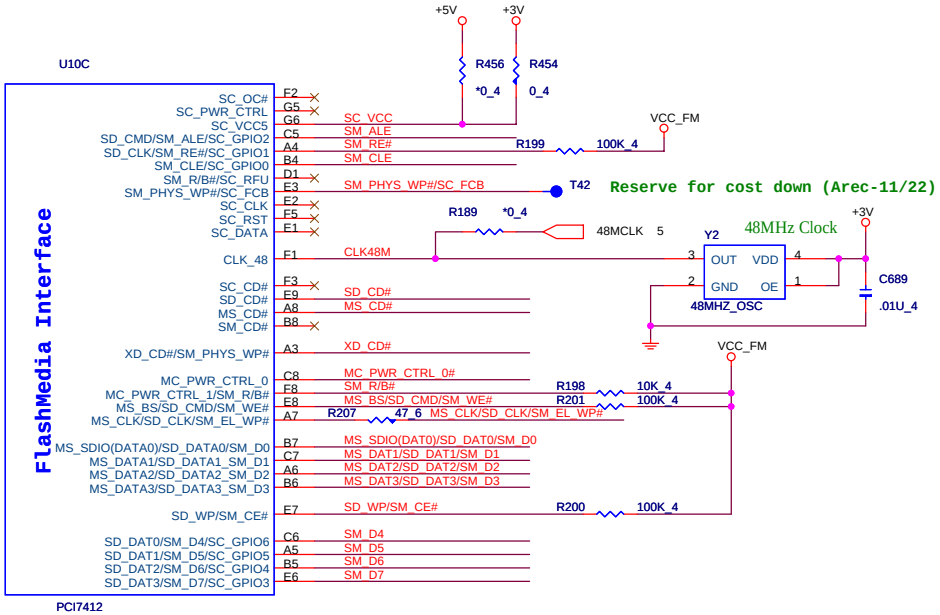
PROJECT : ZB3

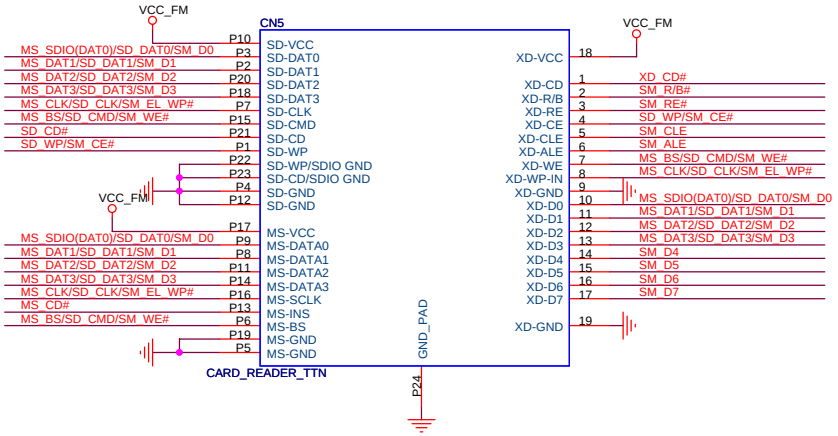
Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412-PCMCIA CONTROLLE	1A
Date: Monday, April 03, 2006	Sheet 24 of 37	

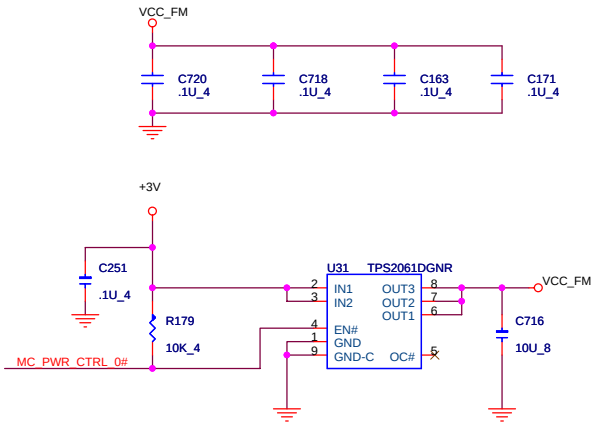
Reserve for XD identification (Arec-11/23)

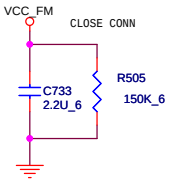
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

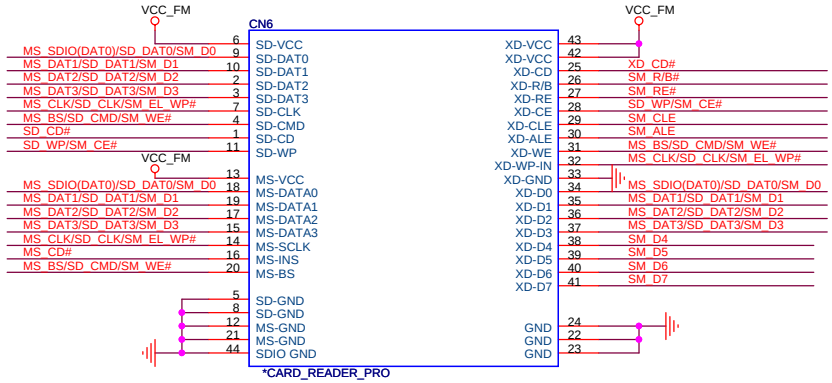




5 IN1 CARD READER





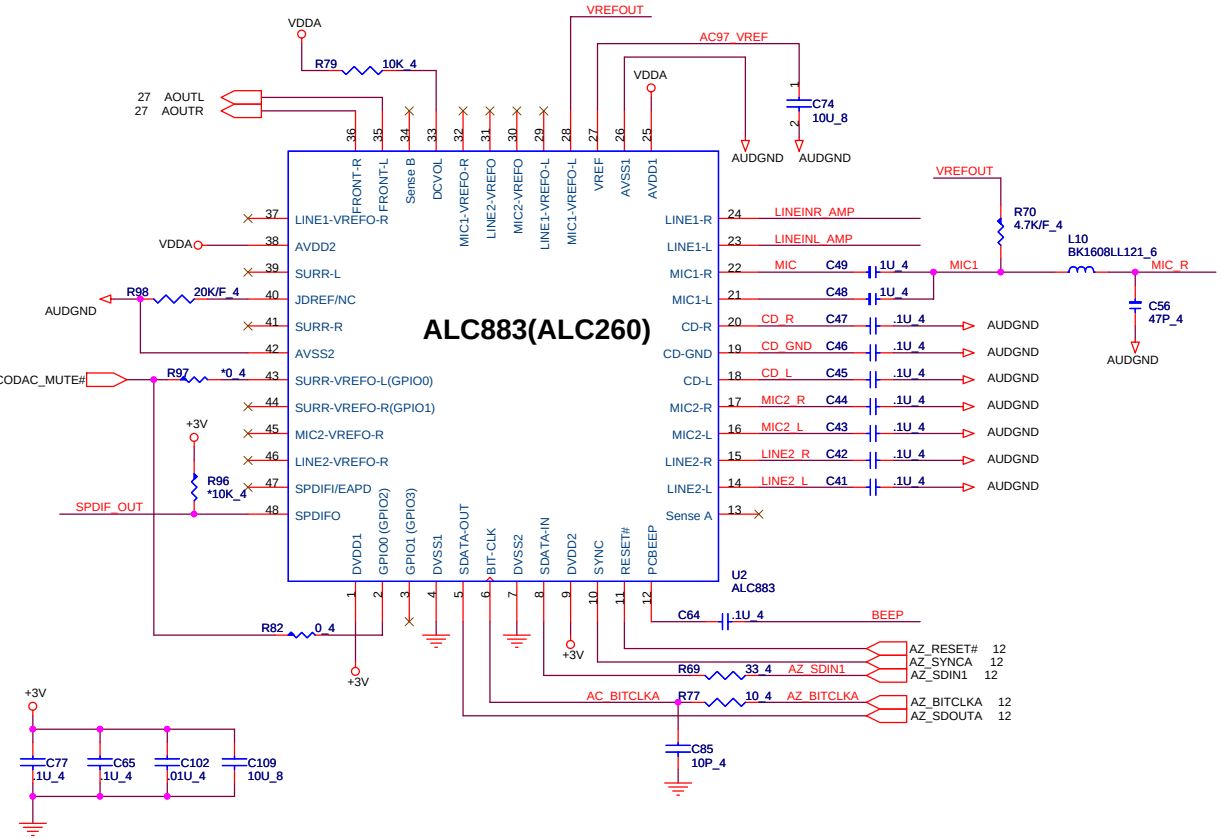


PROJECT : ZB2

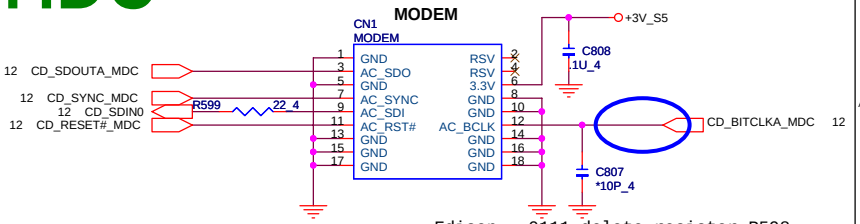
Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412-CARD READER	00
Date: Monday, April 03, 2006	Sheet 25 of 37	

ADO

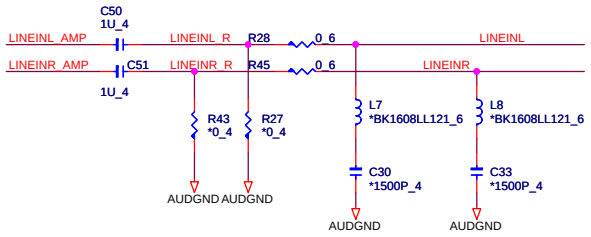


MDC



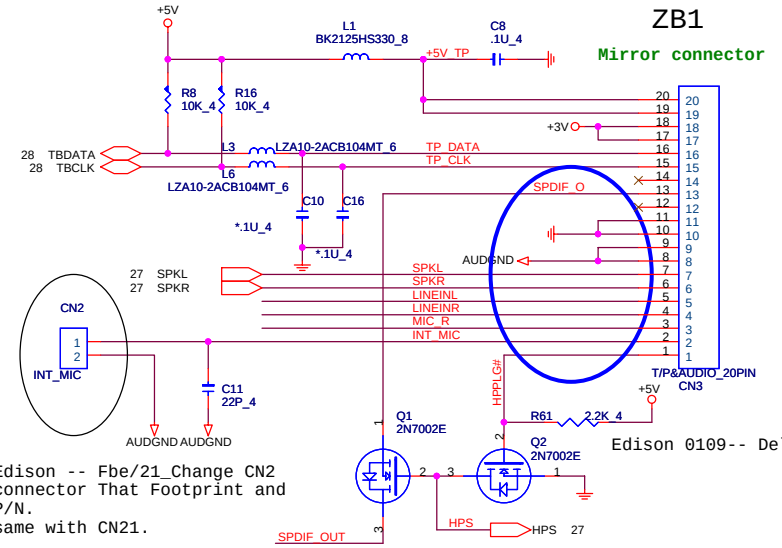
Edison --0111 delete resistor R598

LINE IN



ZB1

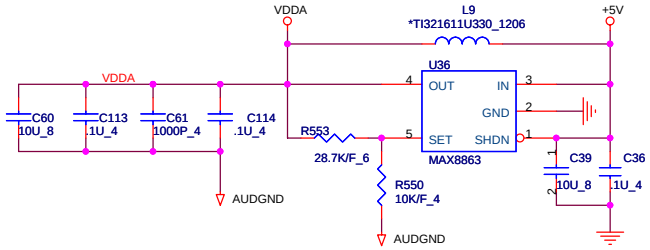
Mirror connector



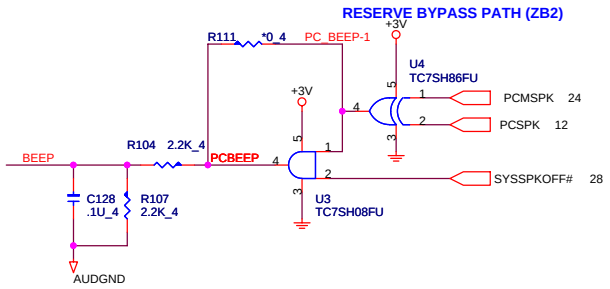
Edison 0109-- Delete

Edison -- Fbe/21_Change CN2 connector That Footprint and P/N.
same with CN21.

Audio Power



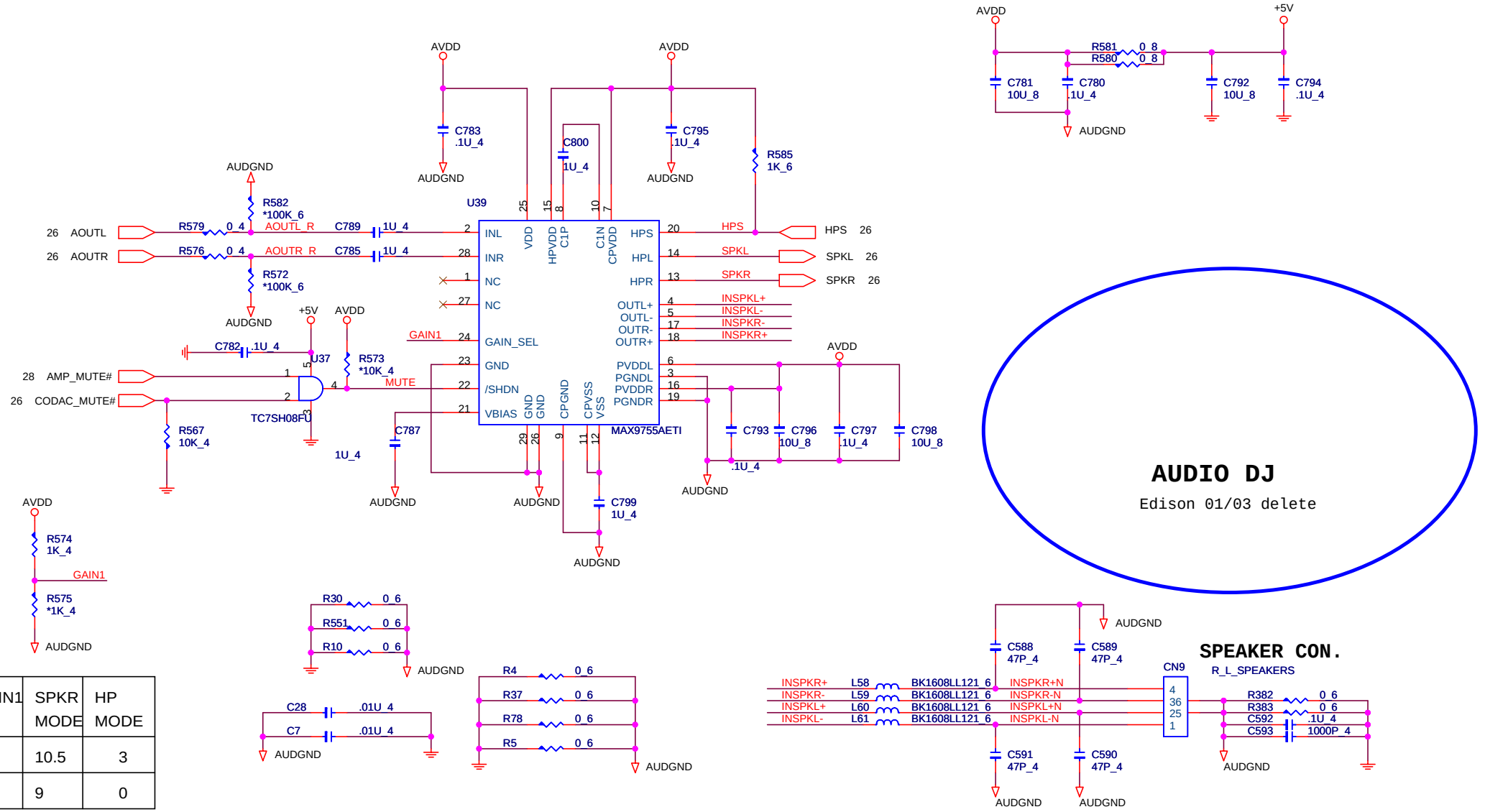
BEEP



PROJECT : ZB3

Quanta Computer Inc.

Size	Document Number	Rev
	CODEC & LINE IN & MIC	1A
Date: Monday, April 03, 2006	Sheet 26 of 37	



AUDIO DJ

Edison 01/03 delete

SPEAKER CON.

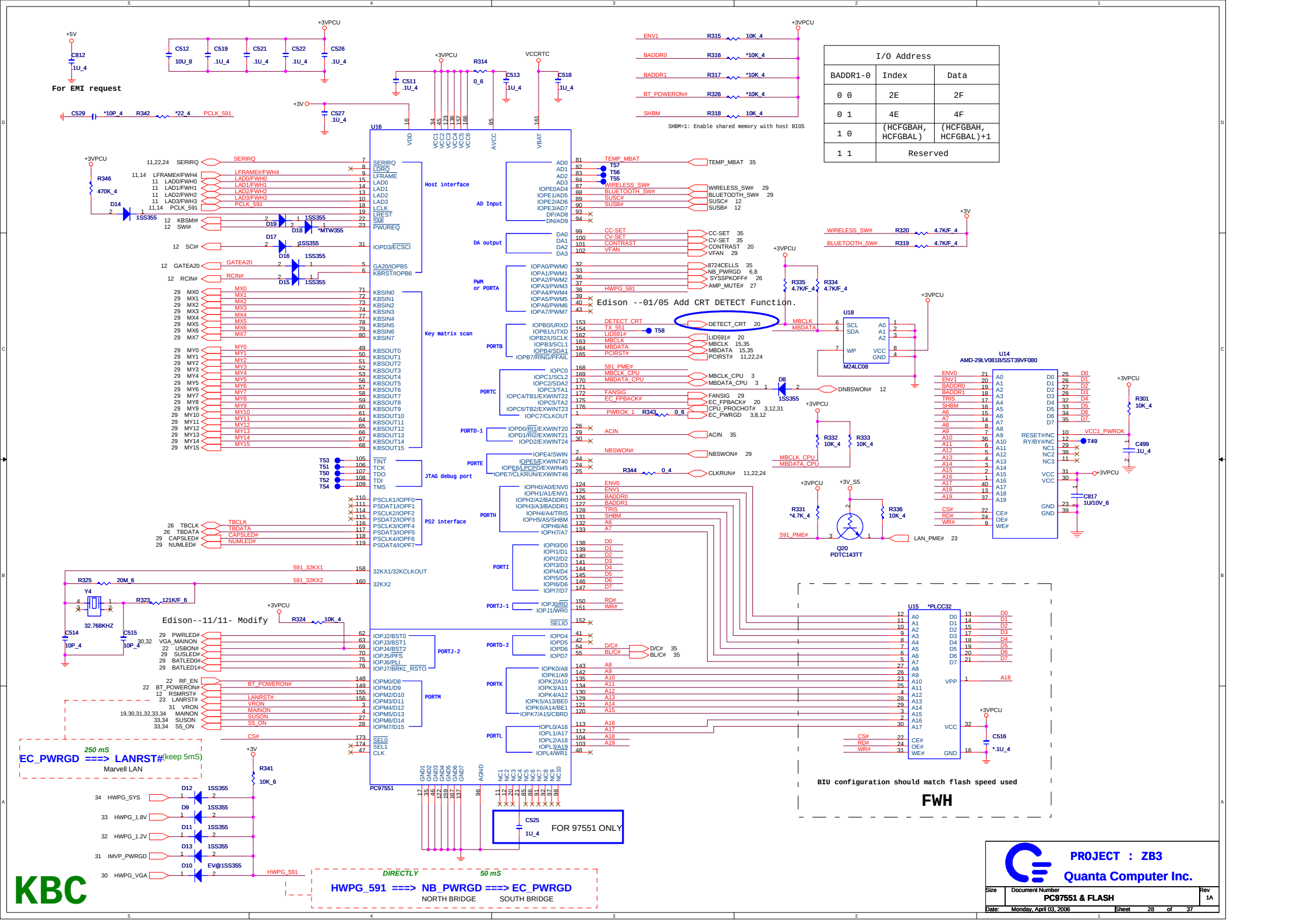
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

AMP

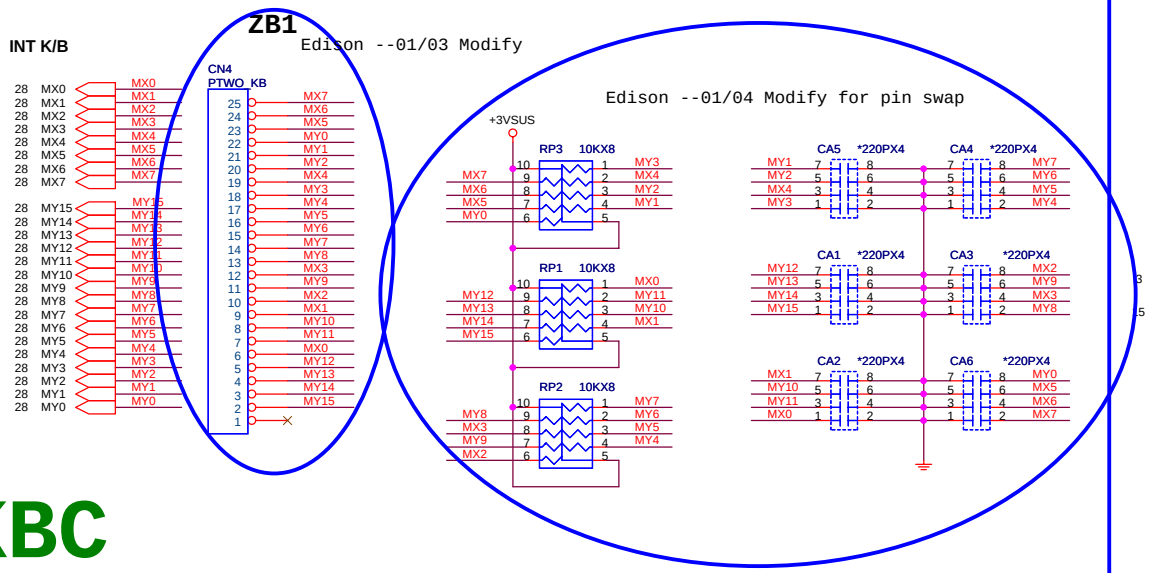
PROJECT : ZB3

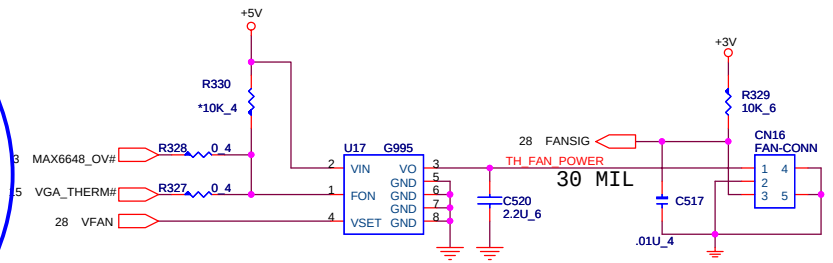
Quanta Computer Inc.

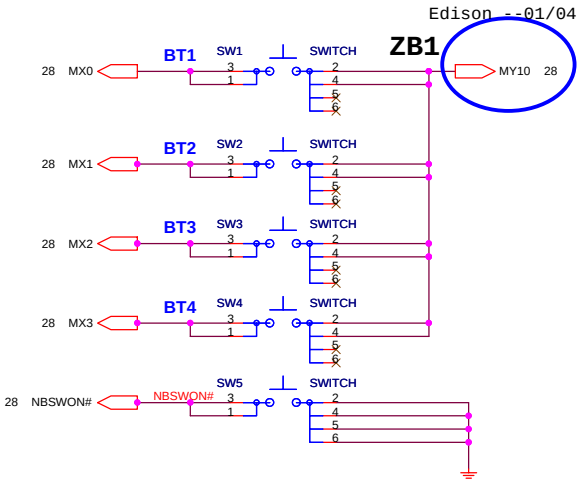
Size	Document Number	Rev
	AUDIO AMP	1A
Date: Monday, April 03, 2006	Sheet 27 of 37	

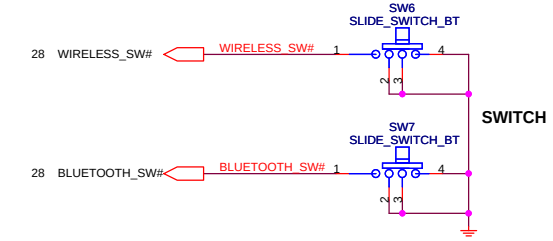


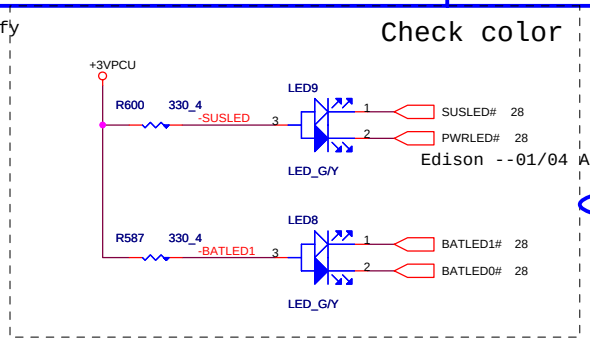
I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

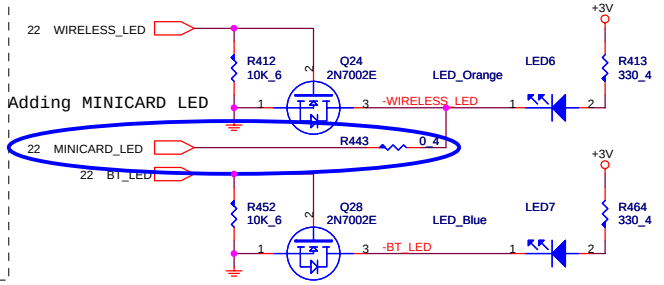


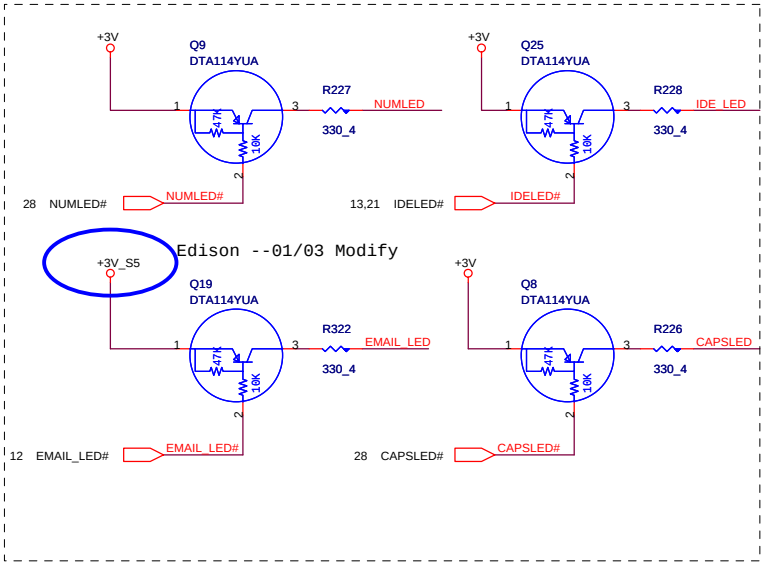


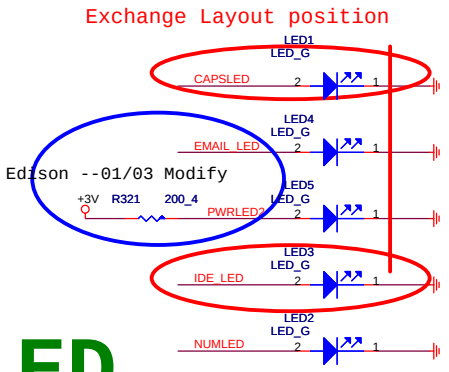








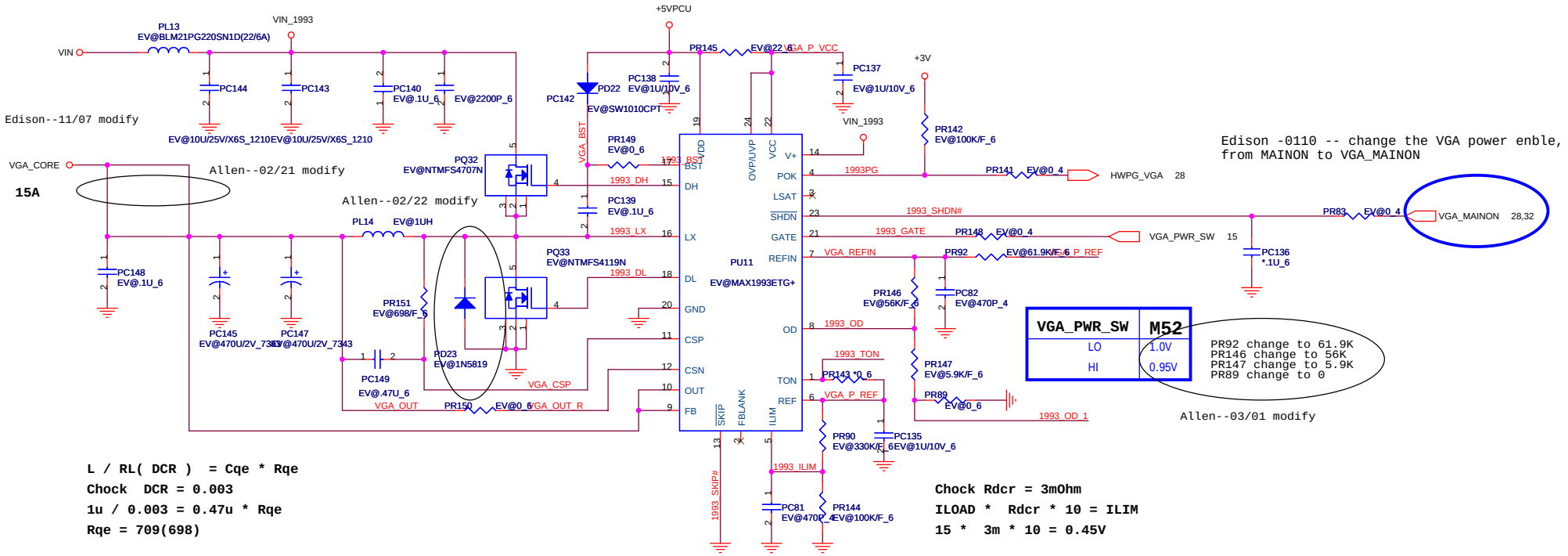


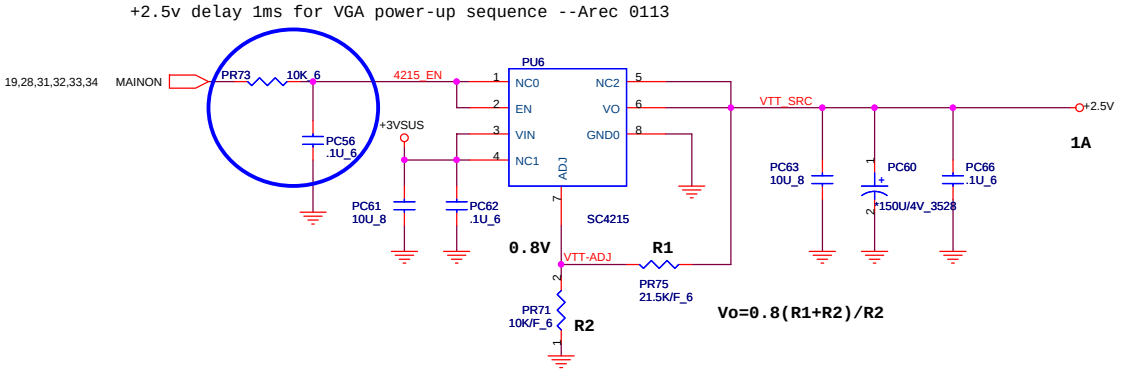


PROJECT : ZB3

Quanta Computer Inc.

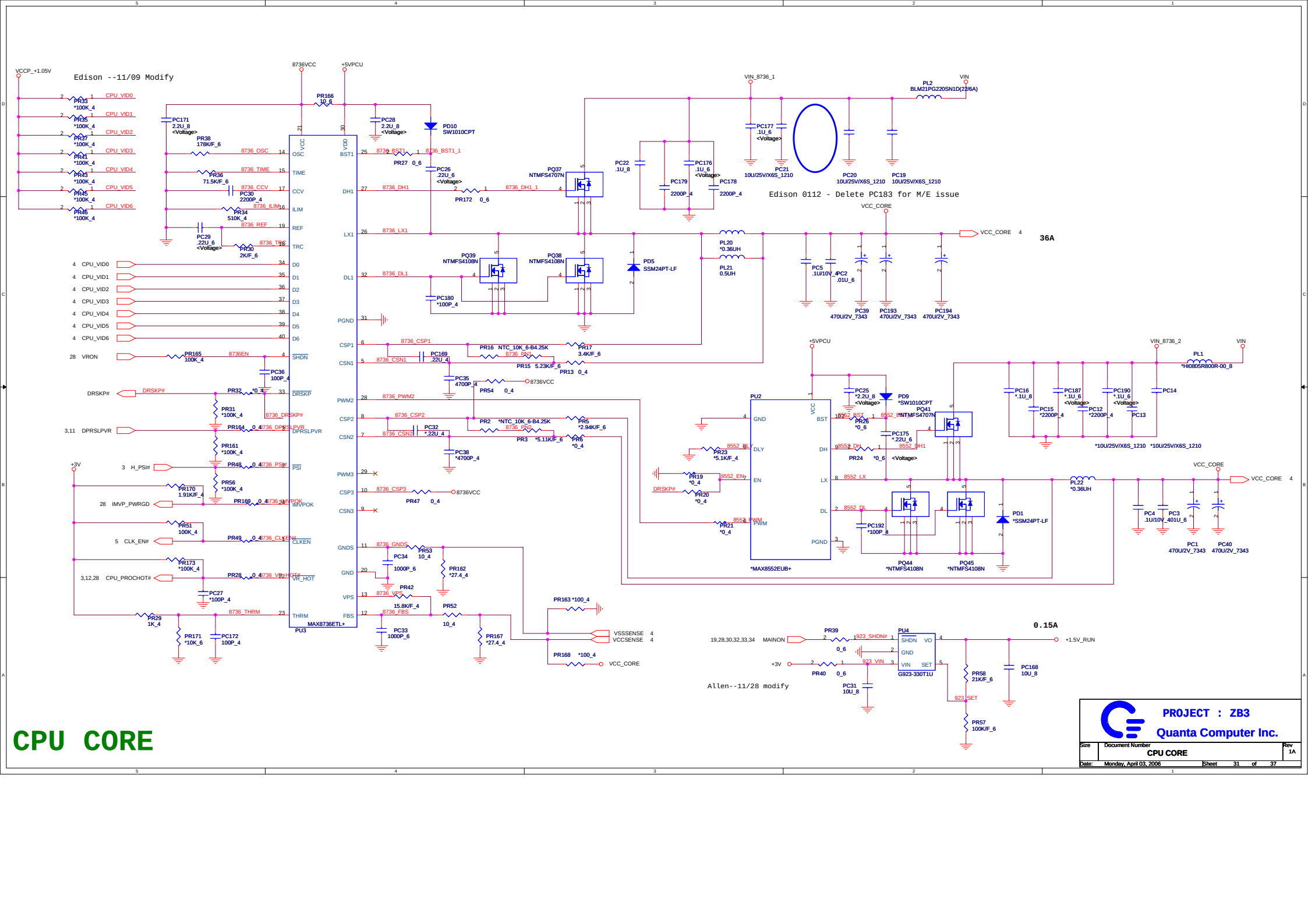
Size	Document Number	Rev
	T/P,FAN,SWITCH,LED,K/B	1A
Date: Monday, April 03, 2006	Sheet 29 of 37	

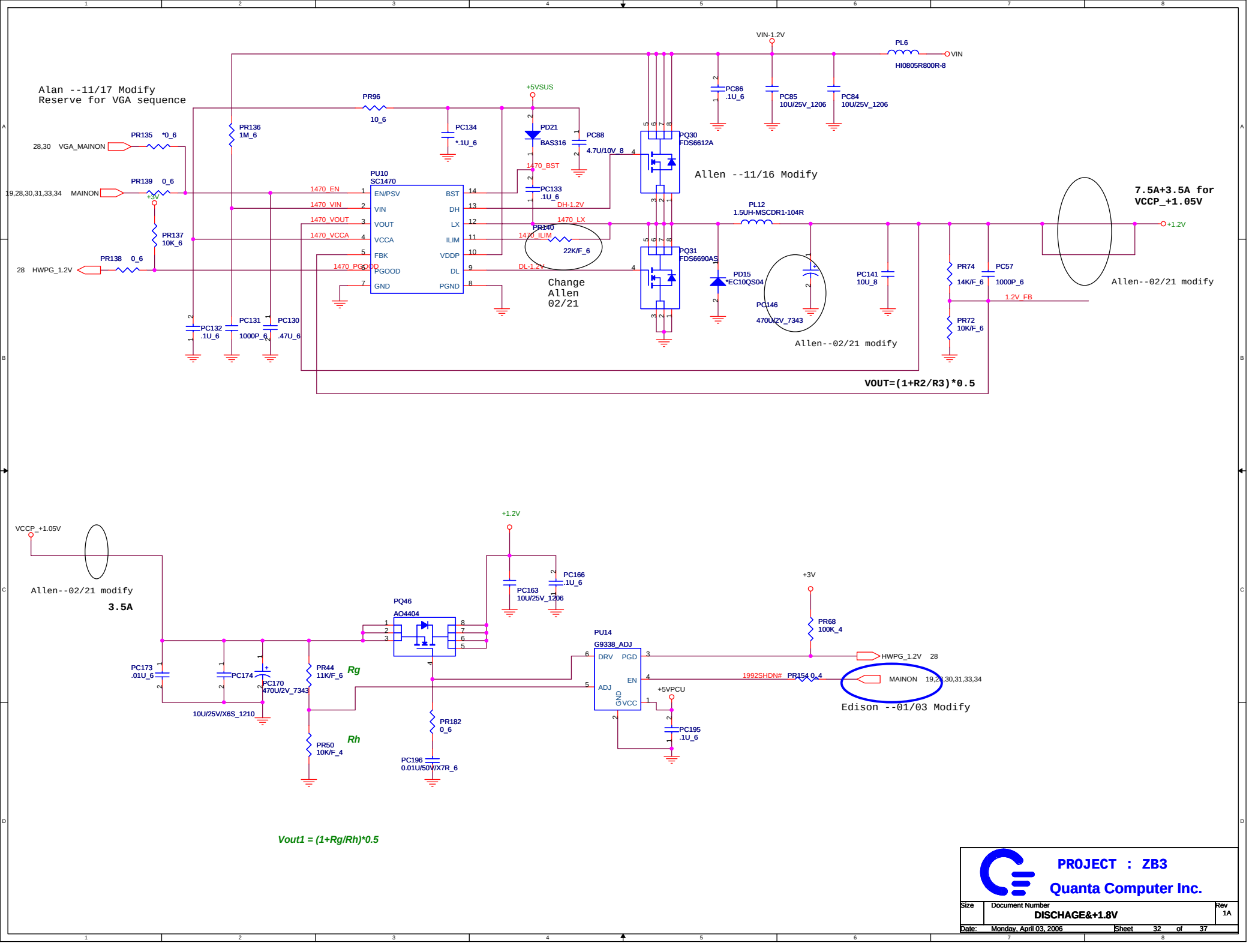




VGA CORE

PROJECT : ZB3	
Quanta Computer Inc.	
Size	Document Number: VGA CORE — Rev: 1A
Date: Monday, April 03, 2006	Sheet 30 of 37


Edison --11/09 Modify
Edison 0112 - Delete PC183 for M/E issue
Allen--11/28 modify
36A
0.15A
MAX8736ETL+
*MAX8552EUB+
CPU CORE
PROJECT : ZB3
Quanta Computer Inc.
CPU CORE
Monday, April 03, 2006
Sheet 31 of 37



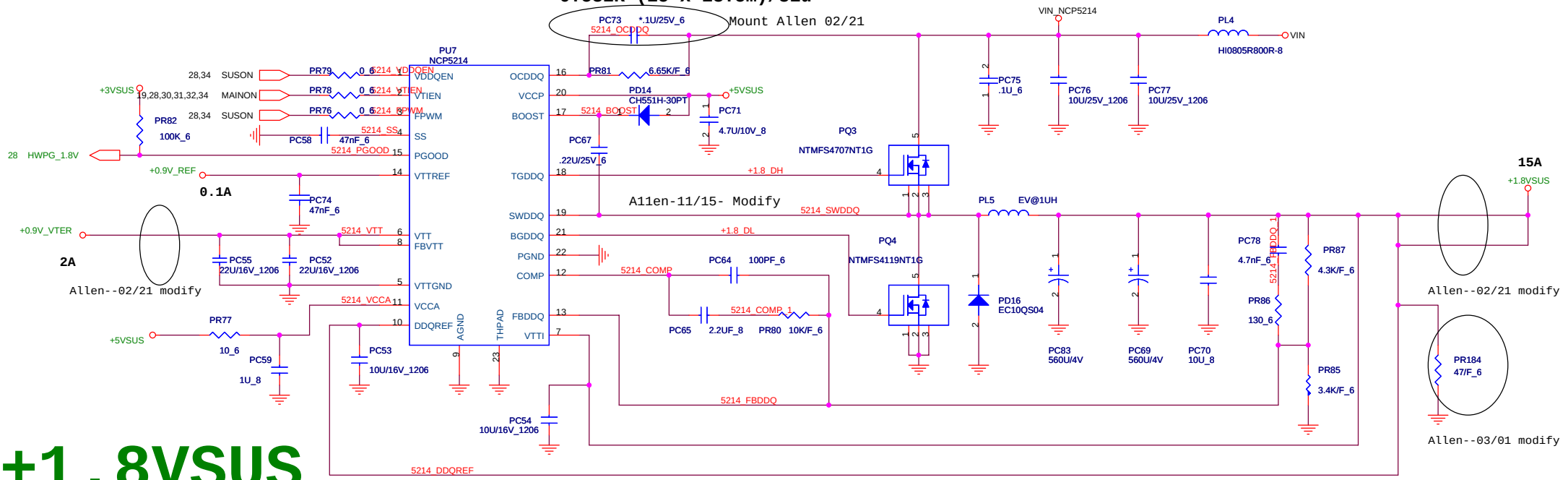
PROJECT : ZB3

Quanta Computer Inc.

Size	Document Number	Rev
	DISCHAGE&+1.8V	1A
Date: Monday, April 03, 2006	Sheet 32 of 37	

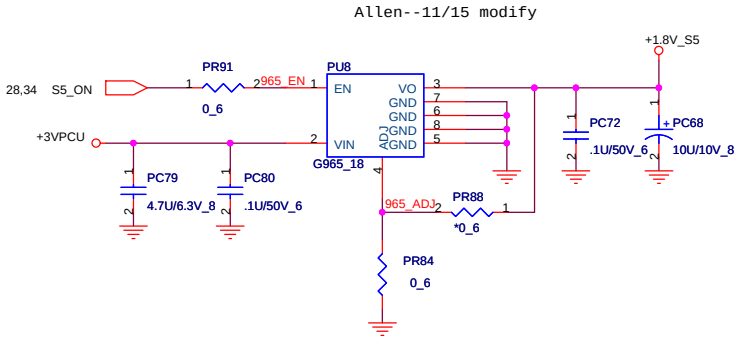
RL1=(Ilim x Rdson-h)/IOC(31uA)

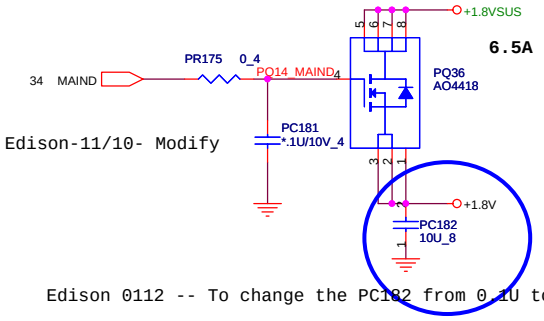
6.532K=(15 x 13.5m)/31u



+1.8VSUS

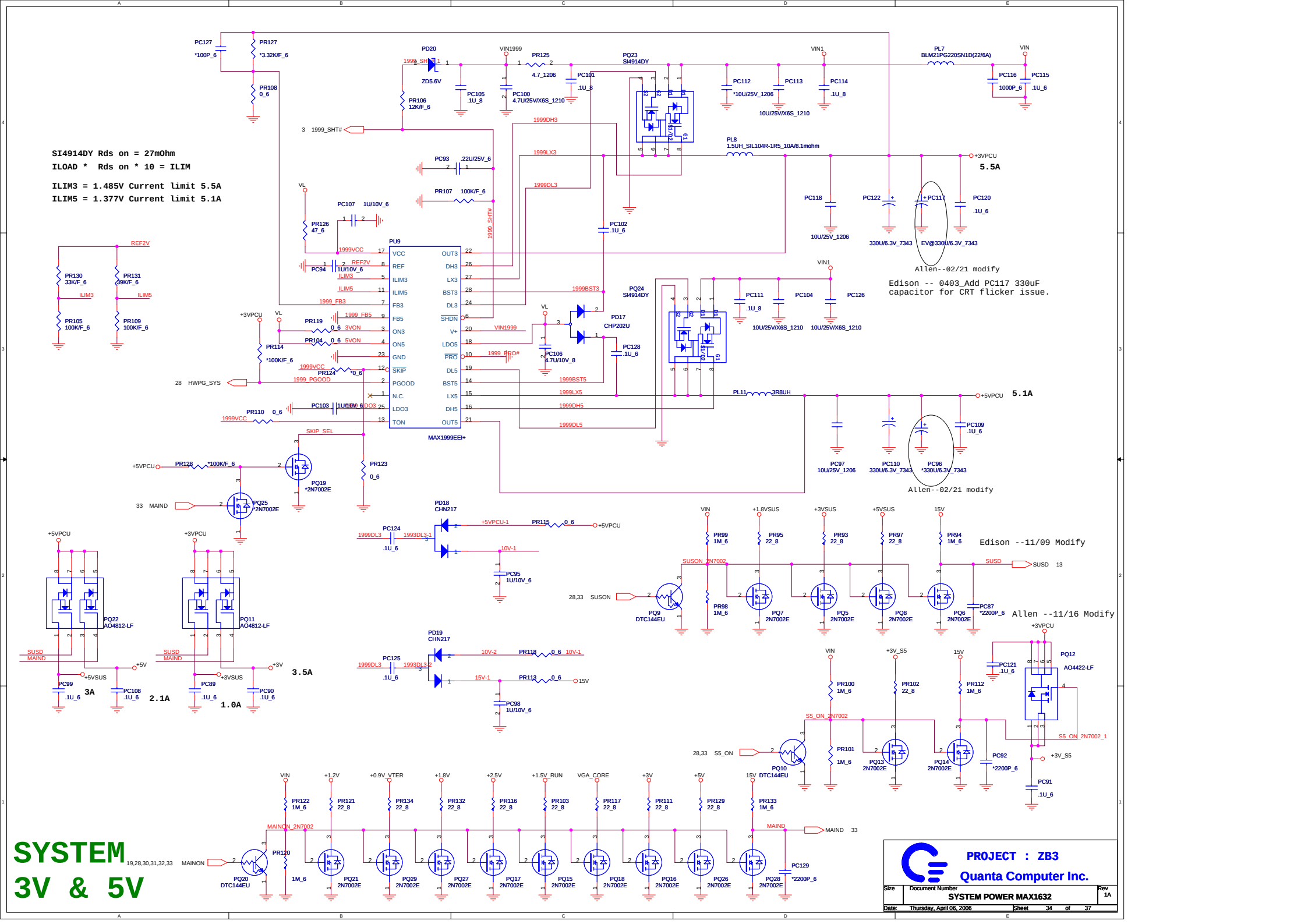
DDR Power & NB Power

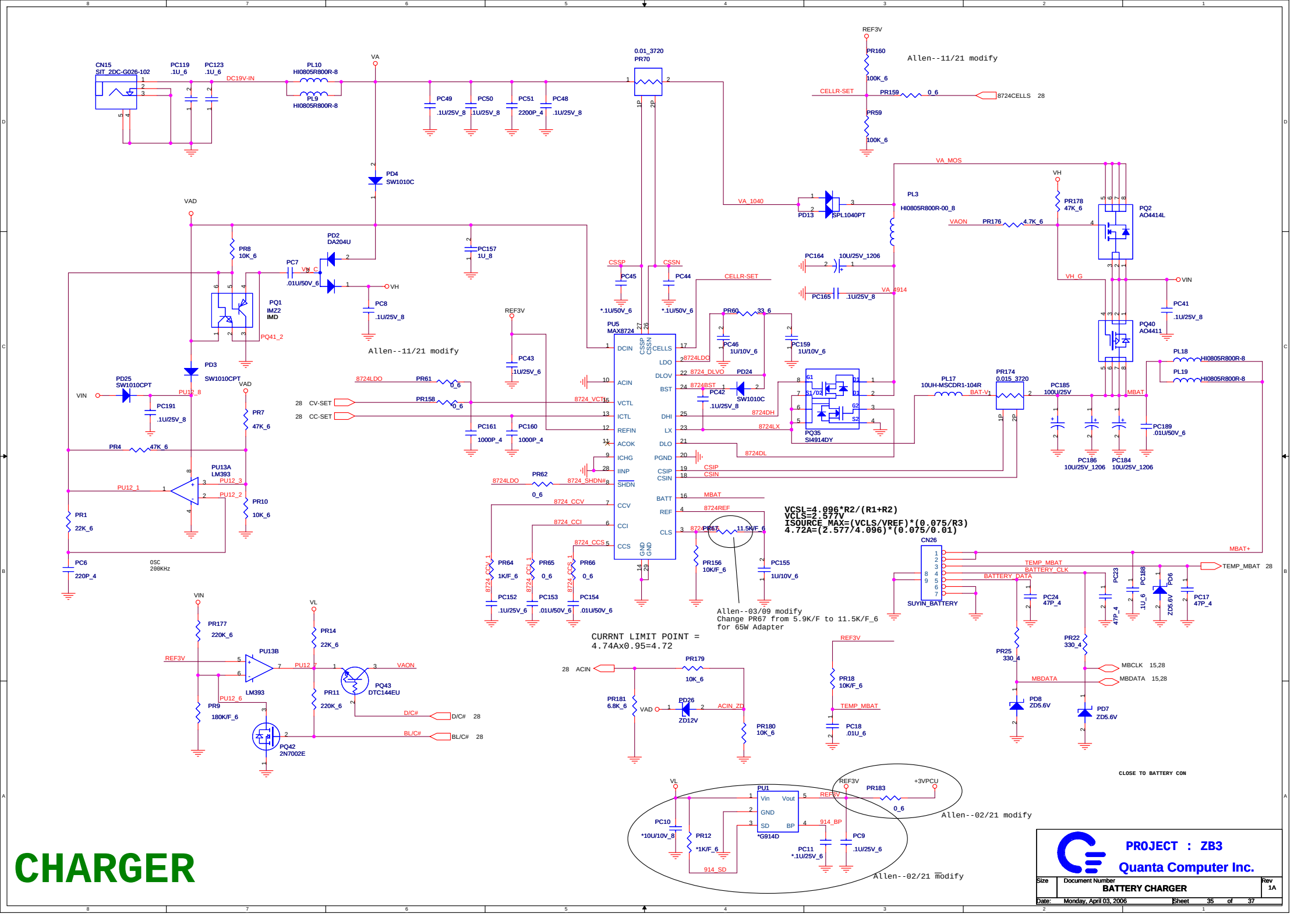




Edison 0112 -- To change the PC182 from 0.1U to 10uF_0805

PROJECT : ZB3		
Quanta Computer Inc.		
Size	Document Number: SMDDR_VTERM&+1.2V&+1.8VSUS	Rev: 1A
Date: Monday, April 03, 2006	Sheet 33 of 37	


SI4914DY Rds on = 27mOhm
ILOAD * Rds on * 10 = ILIM
ILIM3 = 1.485V Current limit 5.5A
ILIM5 = 1.377V Current limit 5.1A
MAX1999EEI+
5.5A
5.1A
3.5A
2.1A
1.0A
Allen--02/21 modify
Edison -- 0403_Add PC117 330uF capacitor for CRT flicker issue.
Edison --11/09 Modify
Allen --11/16 Modify
SYSTEM
3V & 5V
PROJECT : ZB3
Quanta Computer Inc.
SYSTEM POWER MAX1632
Thursday, April 06, 2006


CHARGER
Allen--11/21 modify
Allen--11/21 modify
VCSL=4.096*R2/(R1+R2)
VCLS=2.577V
ISOURCE_MAX=(VCLS/VREF)*(0.075/R3)
4.72A=(2.577/4.096)*(0.075/0.01)
Allen--03/09 modify
Change PR67 from 5.9K/F to 11.5K/F_6
for 65W Adapter
CURRNT LIMIT POINT =
4.74Ax0.95=4.72
Allen--02/21 modify
Allen--02/21 modify
CLOSE TO BATTERY CON
PROJECT : ZB3
Quanta Computer Inc.
BATTERY CHARGER
Monday, April 03, 2006
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