QL5(15.6W) BLOCK DIAGRAM

PCB STACK UP
8L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : SGND1
- LAYER 5 : SVCC
- LAYER 6 : IN2
- LAYER 7 : SGND2
- LAYER 8 : BOT

- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 35
- SYSTEM POWER ISL6237IRZ-T PAGE 36
- VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 37
- CPU CORE ISL6266A PAGE 38
- VGACORE(1.025V)Oz8118 PAGE 39
- DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 40

CPU Penryn
478P (uPGA)/35W
PAGE 3,4

CPU THERMAL SENSOR
PAGE 5

FSB 667/800/1066

CLK_CPU_BCLK,CLK_CPU_BCLK#
CLK_MCH_BCLK,CLK_MCH_BCLK#
DREFCLK,DREFCLK#
DREFSSCLK,DREFSSCLK#

CLOCK GEN
ALPRS355B MLF64PIN
PAGE 2
14.318MHz

PS8101
PAGE 20

27MHz

NORTH BRIDGE
Cantiga
PAGE 5~9

DDRII-SODIMM1
PAGE 10
DDRII 667/800 MHz

DDRII-SODIMM2
PAGE 10
DDRII 667/800 MHz

PCI-Express 16X

NVIDIA N10M-GE1 64bit or N10P-GE1 128bit
969p
PAGE 12~18

Dual Link

HDMI CON
PAGE 20

CRT
PAGE 20

LCD CONN
PAGE 19

Mini PCI-E(WLAN) 10
Mini PCI-E(WWAN) 11
Express Card x1 7
E-SATA x1 0

DMI LINK

32.768KHz

NBSRCCLK, NBSRCCLK#

SOUTH BRIDGE
ICH9-M
PAGE 21~24

SATA - HDD (SATA0)
PAGE 30
SATA0 150MB

SATA - ODD(SATA1)
PAGE 30
SATA1 150MB

E-SATA(SATA5)
PAGE 31
SATA5 150MB

USB2.0

1,2 USB2.0 Ports X2 PAGE 26

8 BlueTooth PAGE 26

9 Webcam PAGE 19

6 RTS5159 PAGE 25
12MHz

PCI-E

Azalia

X2 Mini PCI-E Card (Wireless LAN/WWAN) PAGE 33

X1 LAN Realtek PCIE-LAN RTL8111/8103E (10/100/GagaLAN) PAGE 28,29
25MHz

X1 Express Card (NEW CARD) PAGE 30

Analog
Azalia ALC272
PAGE 26

SPI
PAGE 22

LPC

32.768KHz

ENE KBC
KB3926 C0
PAGE 32

Keyboard
Touch Pad PAGE 32

MDC CONN
PAGE 27

AUDIO Amplifier TPA6017A2
PAGE 27

RJ45
PAGE 28

Microphone
PAGE 19

Audio Jacks (Phone/ MIC)
PAGE 26

Jack to Speaker
PAGE 27

G995 FAN
PAGE 34

SPI
PAGE 32

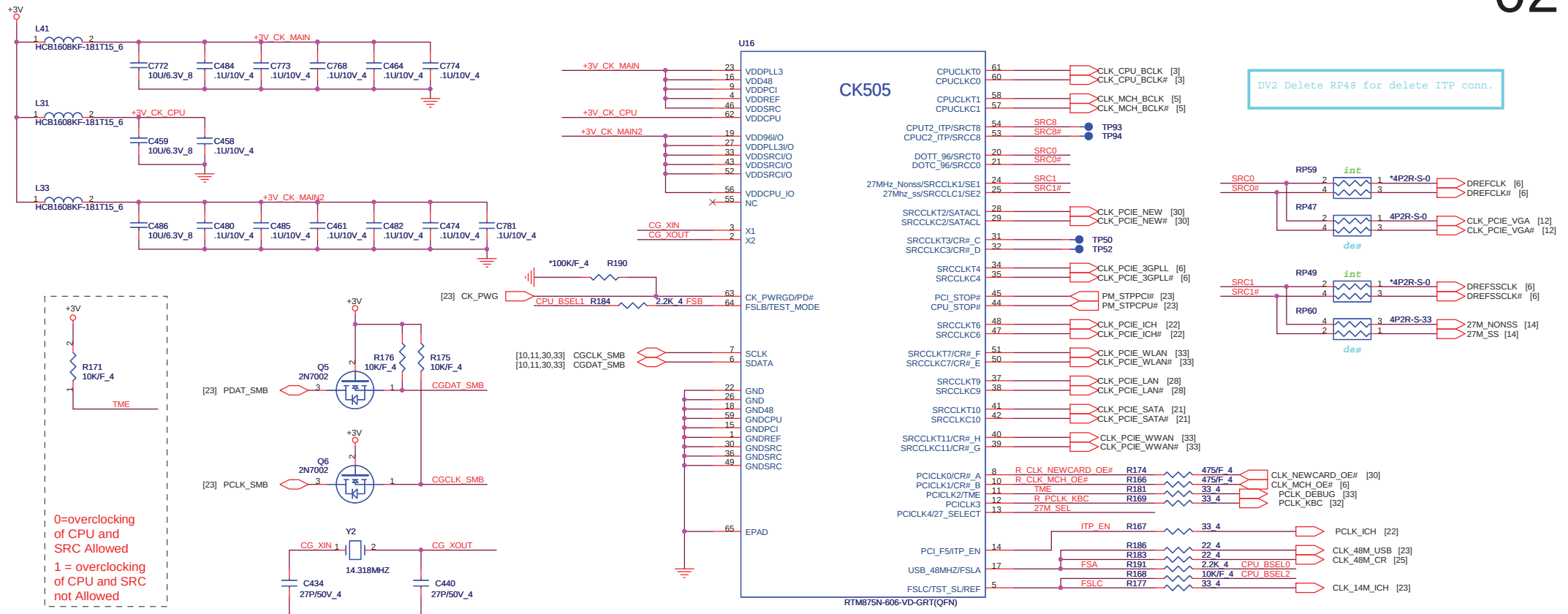
DV2
DV3

NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Tuesday, March 17, 2009 | Sheet 1 of 41

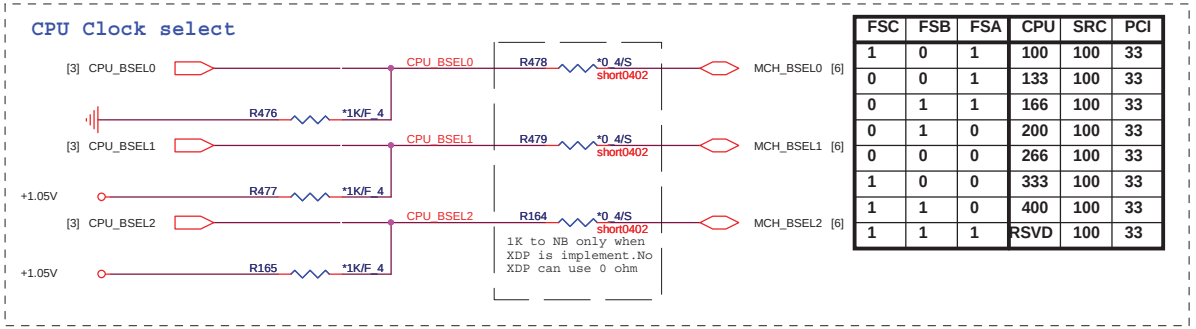


http://hobi-elektronika.net/

CK505 QFN64

ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GRT	AL000875000

27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	1A

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[2,4,5,6,8,9,21,24,31,37,38] +1.05V

U25A

[5] H_A#[35:3]

H_A#3 J4
H_A#4 L5
H_A#5 L4
H_A#6 K5
H_A#7 M3
H_A#8 N2
H_A#9 J1
H_A#10 N3
H_A#11 P5
H_A#12 P2
H_A#13 L2
H_A#14 P4
H_A#15 P1
H_A#16 R1

A[3]#
A[4]#
A[5]#
A[6]#
A[7]#
A[8]#
A[9]#
A[10]#
A[11]#
A[12]#
A[13]#
A[14]#
A[15]#
A[16]#
ADSTB[0]#

ADDR GROUP 0

[5] H_ADSTB#0
[5] H_REQ#[4:0]

H_REQ#0 K3
H_REQ#1 H2
H_REQ#2 K2
H_REQ#3 J3
H_REQ#4 L1

REQ[0]#
REQ[1]#
REQ[2]#
REQ[3]#
REQ[4]#

H_A#[35:3]

H_A#17 Y2
H_A#18 U5
H_A#19 R3
H_A#20 W6
H_A#21 U4
H_A#22 Y5
H_A#23 U1
H_A#24 R4
H_A#25 T5
H_A#26 T3
H_A#27 W2
H_A#28 W5
H_A#29 Y4
H_A#30 U2
H_A#31 V4
H_A#32 W1
H_A#33 AA4
H_A#34 AB2
H_A#35 AA3

A[17]#
A[18]#
A[19]#
A[20]#
A[21]#
A[22]#
A[23]#
A[24]#
A[25]#
A[26]#
A[27]#
A[28]#
A[29]#
A[30]#
A[31]#
A[32]#
A[33]#
A[34]#
A[35]#
ADSTB[1]#

ADDR GROUP 1

[5] H_ADSTB#1

[21] H_A20M#
[21] H_FERR#
[21] H_IGNNE#

A6
A5
C4

A20M#
FERR#
IGNNE#

[21] H_STPCLK#
[21] H_INTR
[21] H_NMI
[21] H_SMI#

D5
C6
B4
A3

STPCLK#
LINT0
LINT1
SMI#

PV Del R83

F6
D3

TDI_1/RSV
TDO_2/RSV

PV R544 Change to ShortPad

R544 *0_4S short0402

TP6

DV2 Add R544 for Intel request

TP4
TP3
TP1

N5
M4
B2
AE8
D8
F8
D22
T2
V3
AA8
AC8
AA7

BMP_1#[0]/RSV
BMP_1#[1]/RSV
BMP_1#[2]/RSV
BMP_1#[3]/VSS
DCLKPH_1/VSS
ACLKPH_1/VSS
GTLREF_2/RSV
THRMDA_1/RSV
THRMDC_1/RSV
HFPLL_1/VSS
SPARE_1[4]/VSS
BR1#/VCC

Penryn Ball-out Rev 1a

ADS# H1
BNR# E2
BPRI# G5

H_ADS# [5]
H_BNR# [5]
H_BPRI# [5]

DEFER# H5
DRDY# F21
DBSY# E1

H_DEFER# [5]
H_DRDY# [5]
H_DBSY# [5]

BR0# F1

HBREQ#0 [5]

IERR# D20
INIT# B3

H_IERR# R43 49.9/F_4 +1.05V
H_INIT# [21]

LOCK# H4

H_LOCK# [5]
H_CPURST# [5]

RESET# C1
RS[0]# F3
RS[1]# F4
RS[2]# G3
TRDY# G2

H_RS#0
H_RS#1
H_RS#2

H_RS#[2:0] [5]
H_TRDY# [5]

HIT# G6
HITM# E4

H_HIT# [5]
H_HITM# [5]

CONTROL

BPM[0]# AD4
BPM[1]# AD3
BPM[2]# AD1
BPM[3]# AC4
PRDY# AC2
PREQ# AC1
TCK AC5
TDI AA6
TDO AB3
TMS AB5
TRST# AB6
DBR# C20

ITP_BPM#0
ITP_BPM#1
ITP_BPM#2
ITP_BPM#3
ITP_BPM#4
ITP_BPM#5
ITP_TCK
ITP_TDI
ITP_TDO
ITP_TMS
ITP_TRST#

TP95
TP96
TP97
TP98
TP99
TP100

SYS_RST# [23]

ITP/BPM SIGNALS

THERMAL

PROCHOT# D21
THERMDA A24
THERMDC B25

R49 *0_4 H_PROCHOT# [38] +1.05V
R46 68_4 +1.05V
H_THERMDA [4]
H_THERMDC [4]

THERMTRIP# C7

PM_THRMTRIP# [6,21]

TDI

H CLK

BCLK[0] A22
BCLK[1] A21

CLK_CPU_BCLK [2]
CLK_CPU_BCLK# [2]

Quard Core Only

RSVD[06] D2

CPU_TEST2 R52 *1K/F_4
CPU_TEST1 R82 *1K/F_4

U25B

[5] H_D#[63:0]

H_D#0 E22
H_D#1 F24
H_D#2 E26
H_D#3 G22
H_D#4 F23
H_D#5 G25
H_D#6 E25
H_D#7 F23
H_D#8 K24
H_D#9 G24
H_D#10 J24
H_D#11 J23
H_D#12 H22
H_D#13 F26
H_D#14 K22
H_D#15 H23

D[0]#
D[1]#
D[2]#
D[3]#
D[4]#
D[5]#
D[6]#
D[7]#
D[8]#
D[9]#
D[10]#
D[11]#
D[12]#
D[13]#
D[14]#
D[15]#

DATA GRP 0

[5] H_DSTBN#0 J26
[5] H_DSTBP#0 H26
[5] H_DINV#0 H25

DSTBN[0]#
DSTBP[0]#
DINV[0]#

H_D#[63:0]

H_D#16 N22
H_D#17 K25
H_D#18 P26
H_D#19 R23
H_D#20 L23
H_D#21 M24
H_D#22 L22
H_D#23 M23
H_D#24 P25
H_D#25 P23
H_D#26 P22
H_D#27 T24
H_D#28 R24
H_D#29 L25
H_D#30 T25
H_D#31 N25

D[16]#
D[17]#
D[18]#
D[19]#
D[20]#
D[21]#
D[22]#
D[23]#
D[24]#
D[25]#
D[26]#
D[27]#
D[28]#
D[29]#
D[30]#
D[31]#

DATA GRP 1

[5] H_DSTBN#1 L26
[5] H_DSTBP#1 M26
[5] H_DINV#1 N24

DSTBN[1]#
DSTBP[1]#
DINV[1]#

R346 1K/F_4 +1.05V
R345 2K/F_4

H_GTLREF AD26

CPU_TEST1 C23
CPU_TEST2 D25
CPU_TEST3 C24
CPU_TEST4 AF26
CPU_TEST5 AE1
CPU_TEST6 A26
CPU_TEST7 C3

TP5
TP2
TP73
TP74
TP8

[2] CPU_BSEL0 B22
[2] CPU_BSEL1 B23
[2] CPU_BSEL2 C21

GTLREF
TEST1
TEST2
TEST3
TEST4
TEST5
TEST6
TEST7
BSEL[0]
BSEL[1]
BSEL[2]

MISC

COMP[0]
COMP[1]
COMP[2]
COMP[3]

R26 COMP0 R349 27.4/F_4
U26 COMP1 R348 54.9/F_4
AA1 COMP2 R16 27.4/F_4
Y1 COMP3 R36 54.9/F_4

DPRSTP# E5
DPSLP# B5
DPWR# D24
PWRGOOD D6
SLP# D7
PSI# AE6

H_DPRSTP# [6,21,38]
H_DPSLP# [21]
H_DPWR# [5]
H_PWRGD [21]
H_CPUSLP# [5]
PM_PSI# [38]

DATA GRP 2

Y22 H_D#32
AB24 H_D#33
V24 H_D#34
V26 H_D#35
V23 H_D#36
T22 H_D#37
U25 H_D#38
U23 H_D#39
Y25 H_D#40
W22 H_D#41
V23 H_D#42
W24 H_D#43
W25 H_D#44
AA23 H_D#45
AA24 H_D#46
AB25 H_D#47

D[32]#
D[33]#
D[34]#
D[35]#
D[36]#
D[37]#
D[38]#
D[39]#
D[40]#
D[41]#
D[42]#
D[43]#
D[44]#
D[45]#
D[46]#
D[47]#

H_D#[63:0]

DSTBN[2]# Y26 H_DSTBN#2 [5]
DSTBP[2]# AA26 H_DSTBP#2 [5]
DINV[2]# U22 H_DINV#2 [5]

DATA GRP 3

H_D#[63:0]

AE24 H_D#48
AD24 H_D#49
AA21 H_D#50
AB22 H_D#51
AB21 H_D#52
AC26 H_D#53
AD20 H_D#54
AE22 H_D#55
AF23 H_D#56
AC25 H_D#57
AE21 H_D#58
AD21 H_D#59
AC22 H_D#60
AD23 H_D#61
AF22 H_D#62
AC23 H_D#63

D[48]#
D[49]#
D[50]#
D[51]#
D[52]#
D[53]#
D[54]#
D[55]#
D[56]#
D[57]#
D[58]#
D[59]#
D[60]#
D[61]#
D[62]#
D[63]#

DATA GRP 3

DSTBN[3]# AE25 H_DSTBN#3 [5]
DSTBP[3]# AF24 H_DSTBP#3 [5]
DINV[3]# AC20 H_DINV#3 [5]

Penryn Ball-out Rev 1a

Populate ITP700Flex for bringup

R335 54.9/F_4 ITP_TCK
R333 54.9/F_4 ITP_TRST#

DV2 Del JITP1,R337,R336,R85,C609,C610,C154

ITP_TDO R334 *54.9/F_4 +1.05V
ITP_TMS R332 54.9/F_4
ITP_TDI R331 54.9/F_4

NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn 1/2	1A

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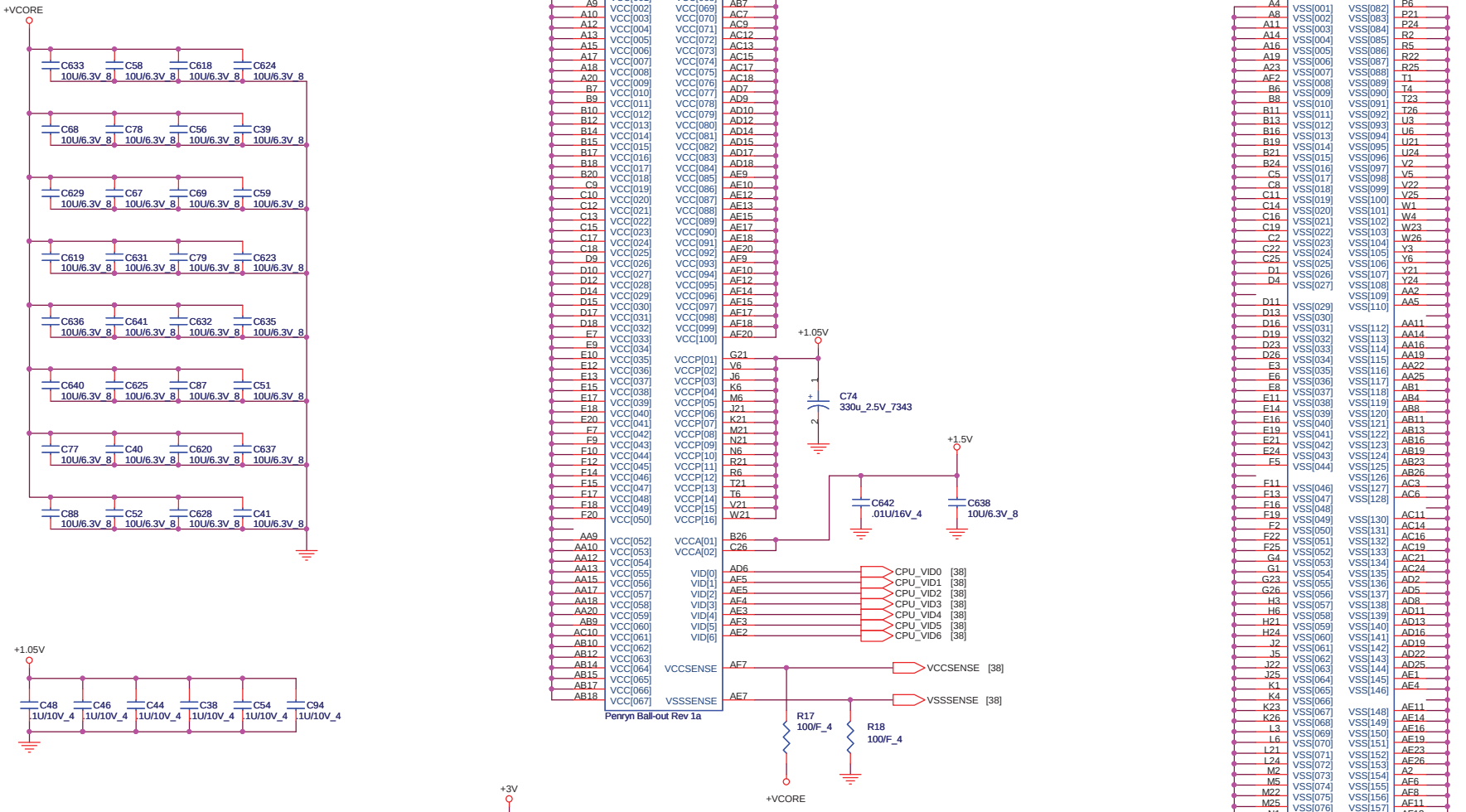
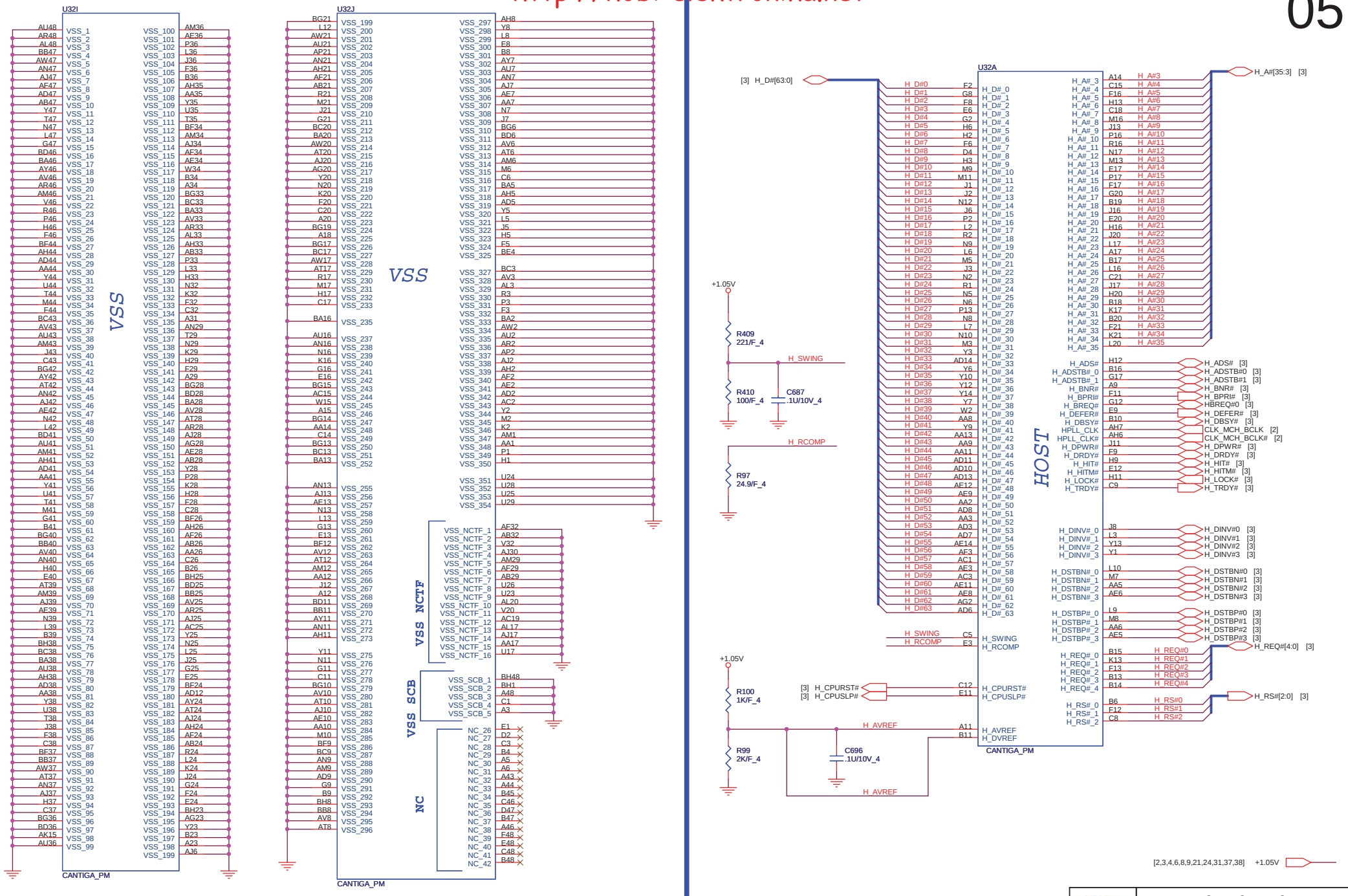


NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn & TH Monitor 2/2	1A

Date: Tuesday, March 17, 2009 Sheet 4 of 41



PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga Host & VSS 1/5	1A

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NB5

MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reserved

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

U32B

RSVD
CLK / DDR CLK / CONTROL/COMPENSATION
ME JTAG
CFG
DMI
GRAPHICS VID
PM
ME
MISC
HDA
NC

CANTIGA_PM

U32C

LVDS
TV
VGA
PCI-EXPRESS GRAPHICS

CANTIGA_PM

Change to 75 ohm to GND

Change to 0 ohm to GND

DV2-FOR ITPM

FOR TEST

C341 10P/50V_4 CLOSE U32 EMI

For UMA HDMI Function

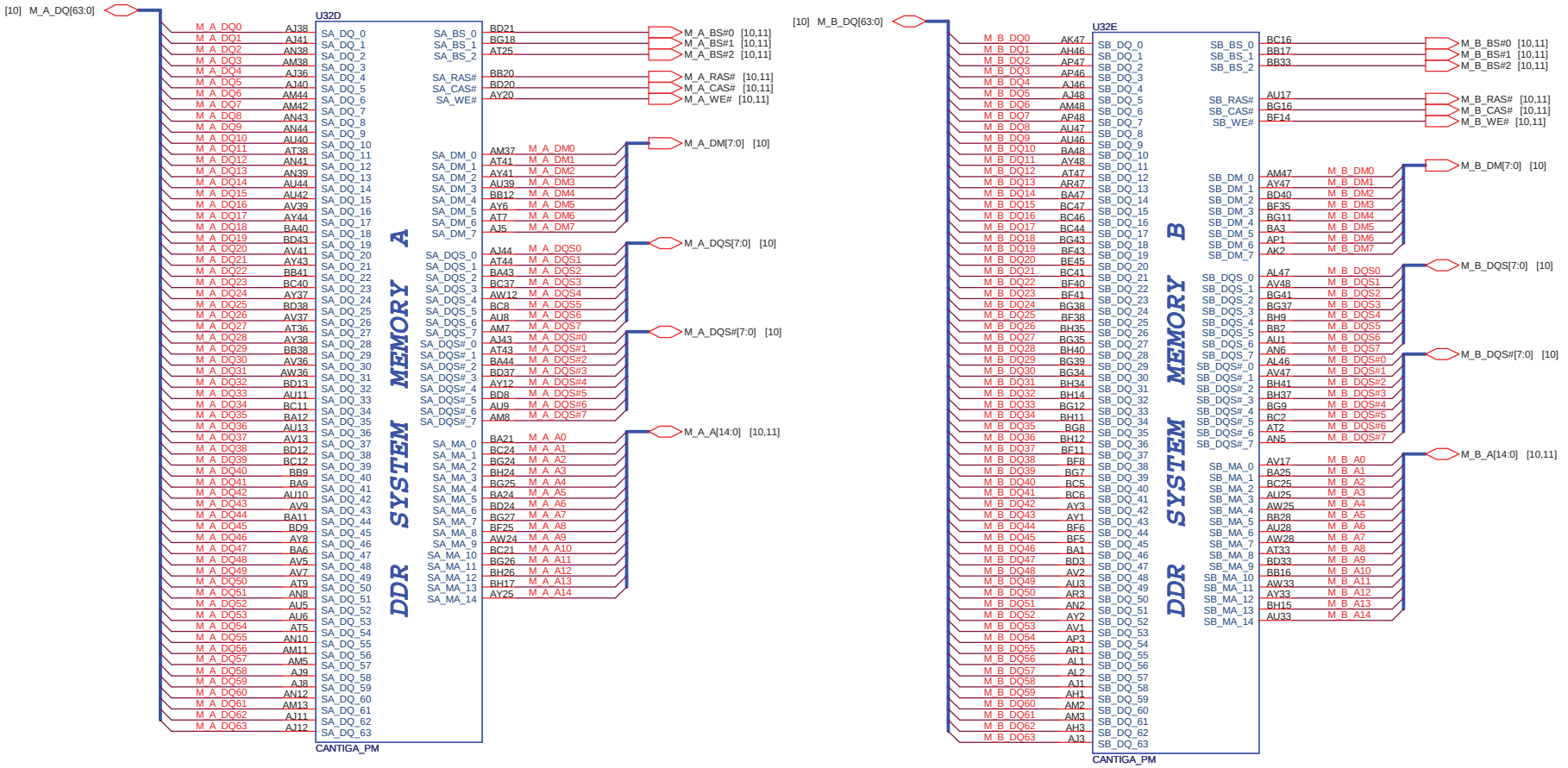
C364,C369,C383,C375
C367,C365,C374,C370
Need to install for GM

HPD# Inverting Level Shifting Circuit

PROJECT : QL5
Quanta Computer Inc.

NB5

Size: Custom | Document Number: Cantiga DMI/DISP 2/5 | Rev: 1A
Date: Tuesday, March 17, 2009 | Sheet 6 of 41



NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga DDR2 3/5	1A

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U32G

+1.8VSUS

2600mA

VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desgins.

VCC SM POWER

VCC_SM_1 … VCC_SM_35 (AP33, AN33, BH32, BG32, BF32, BD32, BC32, BB32, BA32, AY32, AW32, AV32, AU32, AT32, AR32, AP32, AN32, BH31, BG31, BF31, BG30, BH29, BG29, BF29, BD29, BC29, BB29, BA29, AY29, AW29, AV29, AU29, AT29, AR29, AP29)

VCC_SM_36/NC (BA36), VCC_SM_37/NC (BB24), VCC_SM_38/NC (BD16), VCC_SM_39/NC (BB21), VCC_SM_40/NC (AW16), VCC_SM_41/NC (AW13), VCC_SM_42/NC (AT13)

+1.05V

VCC GFX

VCC_AXG_1 … VCC_AXG_42 (Y26, AE25, AB25, AA25, AE24, AC24, AA24, Y24, AE23, AC23, AB23, AA23, AJ21, AG21, AE21, AC21, AA21, Y21, AH20, AF20, AE20, AC20, AB20, AA20, T17, T16, AM15, AL15, AE15, AJ15, AH15, AG15, AF15, AB15, AA15, Y15, V15, U15, AN14, AM14, U14, T14)

VCC_AXG_SENSE (AJ14), VSS_AXG_SENSE (AH14)

R104 10_4

R103 10_4

VCC GFX NCTF

VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60 (W28, V28, W26, V26, W25, V25, W24, V24, W23, V23, AM21, AL21, AK21, W21, V21, U21, AM20, AK20, W20, U20, AM19, AL19, AK19, AJ19, AH19, AG19, AF19, AE19, AB19, AA19, Y19, W19, V19, U19, AM17, AK17, AH17, AG17, AF17, AE17, AC17, AB17, Y17, W17, V17, AM16, AL16, AK16, AJ16, AH16, AG16, AF16, AE16, AC16, AB16, AA16, Y16, W16, V16, U16)

VCC SM LF

VCC_SM_LF1 … VCC_SM_LF7 (AV44, BA37, AM40, AV21, AY5, AM10, BB13)

+VCCSM_LF1 … +VCCSM_LF7

C258 .1U/10V_4, C249 .1U/10V_4, C223 .33U/6.3V_4, C303 .33U/6.3V_4, C358 .47U/6.3V_4, C357 1U/6.3V_4, C359 1U/6.3V_4

CANTIGA_PM

Ivcc=1930.4+508.12=2438.52mA

Ivcc_axg=6326.84mA

+1.05V

C681 *330u_2.5V_7343, C224 10U/6.3V_8, C400 10U/6.3V_8, C260 .33U/6.3V_4, C282 .33U/6.3V_4, C283 .1U/10V_4

+1.8VSUS

C690 .1U/10V_4, C700 10U/6.3V_8, C730 10U/6.3V_8, C714 10U/6.3V_8, C709 10U/6.3V_8

EMI

+1.8VSUS: C719 1000P/50V_4, C688 1000P/50V_4

+1.05V: C373 1000P/50V_4, C309 1000P/50V_4, C299 1000P/50V_4, C445 1000P/50V_4, C769 1000P/50V_4, C310 1000P/50V_4

+1.05V

C298 .47U/6.3V_4, C257 1U/6.3V_4, C204 10U/6.3V_8, C186 10U/6.3V_8, C399 10U/6.3V_8, C284 1U/10V_4, C275 .1U/10V_4

C697 390U/2.5V_6X5.8ESR10

Modify 0831

U32F

VCC CORE POWER

AG34, AC34, AB34, AA34, Y34, V34, U34, AM33, AK33, AJ33, AG33, AF33, AE33, AC33, AA33, Y33, W33, V33, U33, AH28, AF28, AC28, AA28, AJ26, AG26, AE26, AC26, AH25, AG25, AF25, AG24, AJ23, AH23, AF23, T32

VCC_1 … VCC_35

CANTIGA_PM

VCC NCTF

+1.05V

VCC_NCTF_1 … VCC_NCTF_44 (AM32, AL32, AK32, AJ32, AH32, AG32, AE32, AC32, AA32, Y32, W32, U32, AM30, AL30, AK30, AH30, AG30, AF30, AE30, AC30, AB30, AA30, Y30, W30, V30, U30, AL29, AK29, AJ29, AH29, AG29, AF29, AC29, AA29, Y29, W29, V29, AL28, AK28, AL26, AK26, AK25, AK24, AK23)

[6,9,10,31,37,40] +1.8VSUS
[2,3,4,5,6,9,21,24,31,37,38] +1.05V

NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga Vcc 4/5	1A

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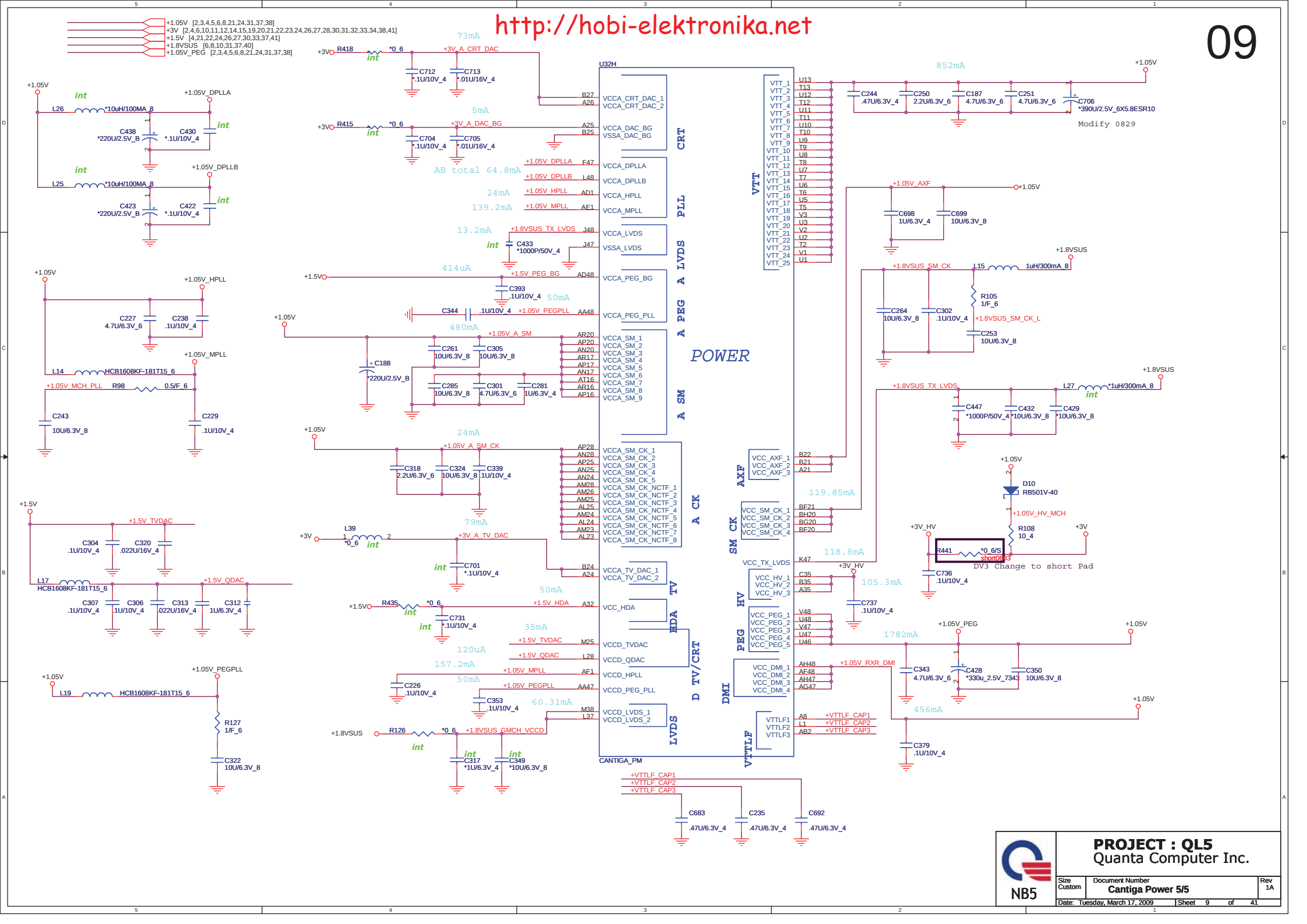

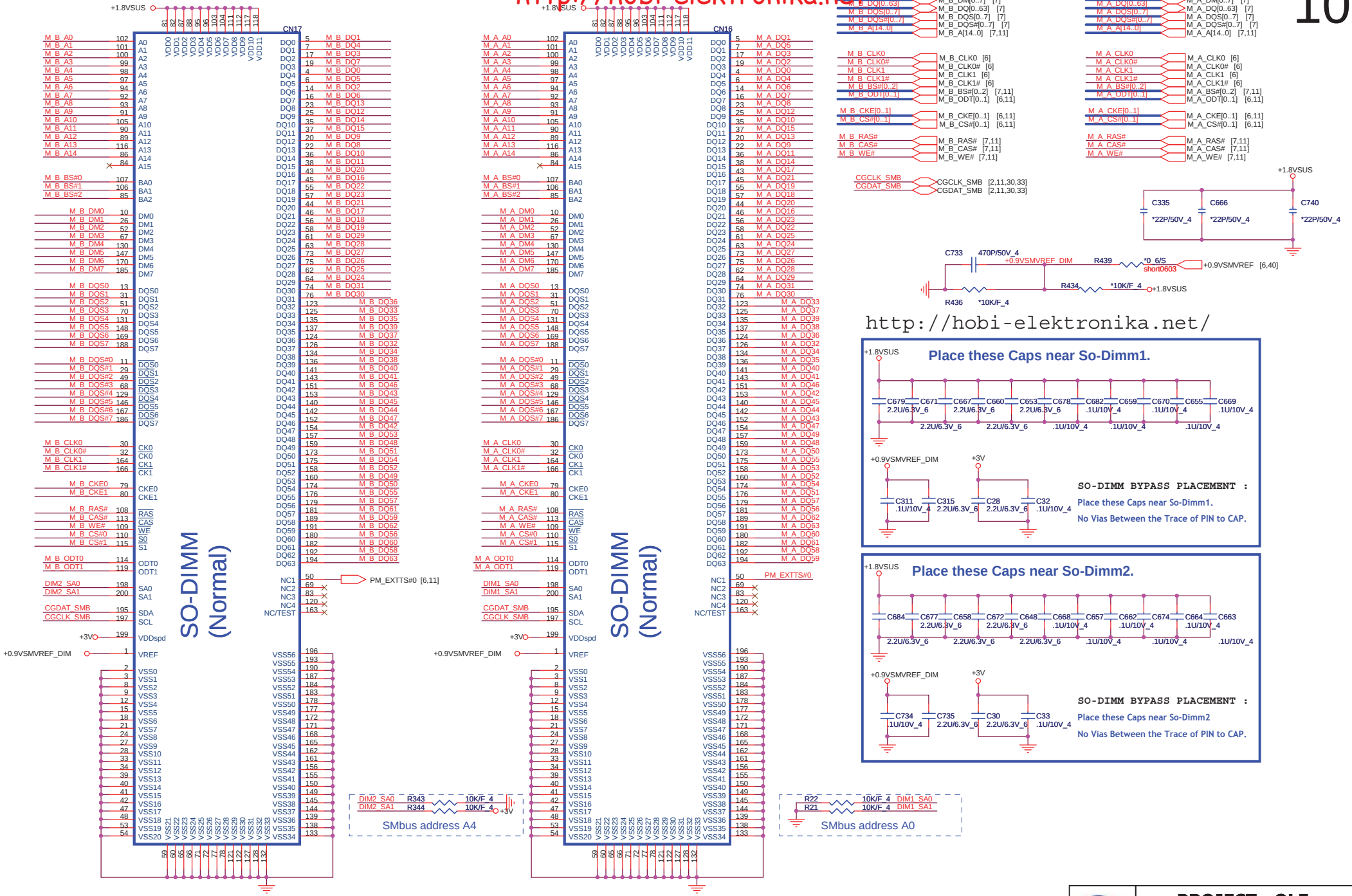

NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 DIMM	1A

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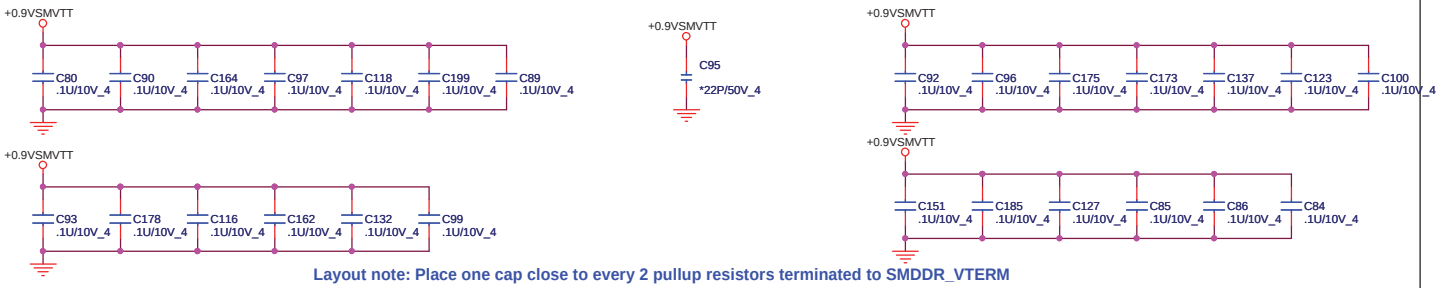
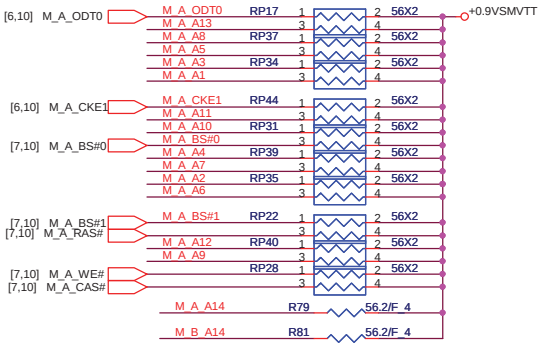
DDRII DUAL CHANNEL A,B.

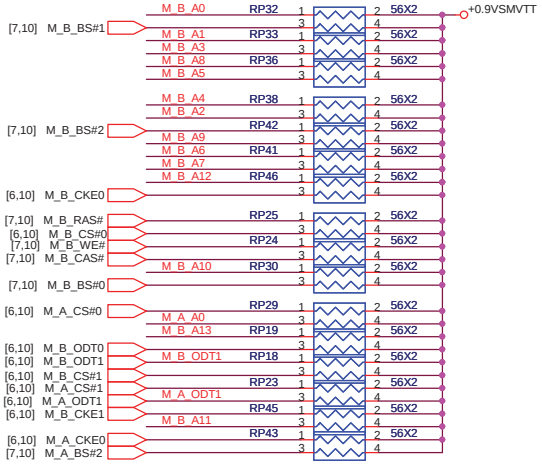
DDRII A CHANNEL

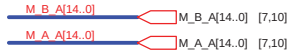
DDRII B CHANNEL

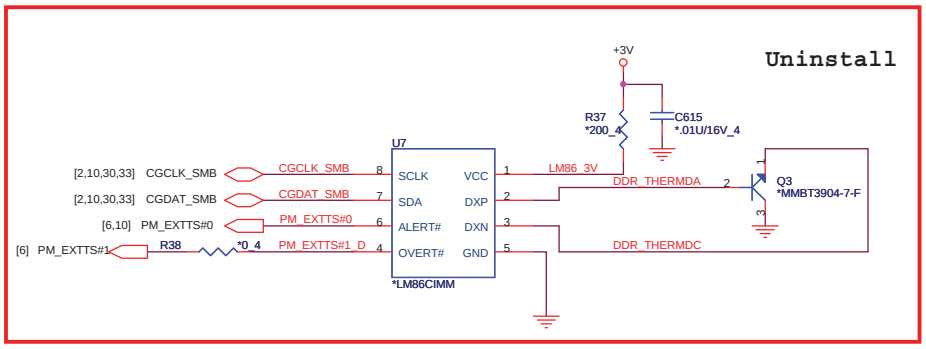


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM









+0.9VSMVTT [40]

+3V [2,4,6,9,10,12,14,15,19,20,21,22,23,24,26,27,28,30,31,32,33,34,38,41]

NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 termination	1A

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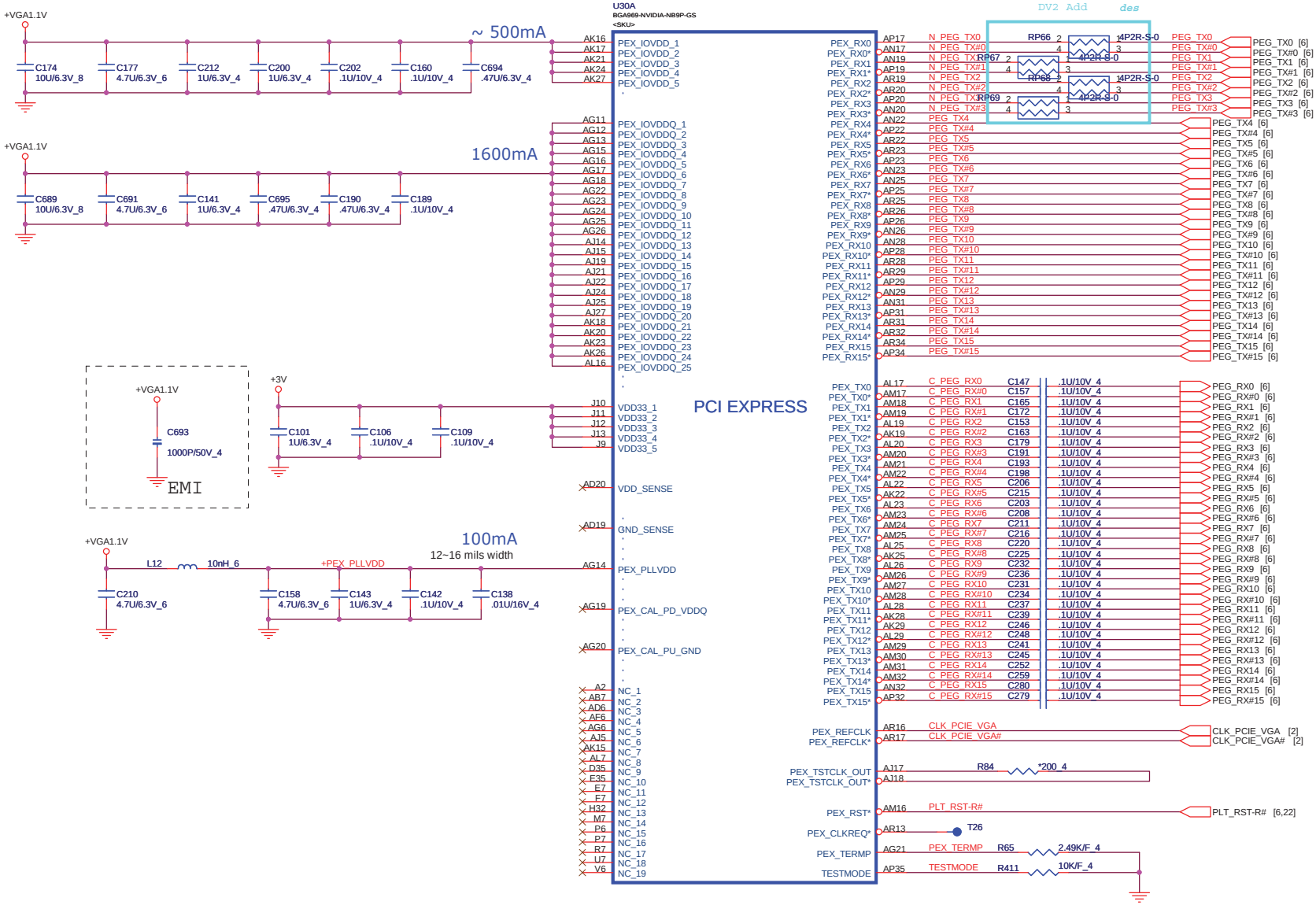

MEMORY I/F A

U30B
BGA969-NVIDIA-NB9P-GS
<SKU>

[17] VMA_MA3 [17] VMA_MA0 [17] VMA_MA2 [17] VMA_MA1 [17] VMA_MA3H [17] VMA_MA4H [17] VMA_MA5H
[17] VMA_CS0# [17] VMA_WE# [17] VMA_BA0 [17] VMA_CKE [17] VMA_ODT [17] VMA_MA2H [17] VMA_MA12 [17] VMA_RAS# [17] VMA_MA11 [17] VMA_MA10 [17] VMA_BA1 [17] VMA_MA8 [17] VMA_MA9 [17] VMA_MA6 [17] VMA_MA5 [17] VMA_MA7 [17] VMA_MA4 [17] VMA_CAS#
[17] VMA_BA2
Add for 64x16 vram

FBA_CMD0 FBA_CMD1 FBA_CMD2 FBA_CMD3 FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15 FBA_CMD16 FBA_CMD17 FBA_CMD18 FBA_CMD19 FBA_CMD20 FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26 FBA_CMD27 FBA_CMD28 FBA_CMD29 FBA_CMD30

VMA_DM0 VMA_DM1 VMA_DM2 VMA_DM3 VMA_DM4 VMA_DM5 VMA_DM6 VMA_DM7
FBA_DQM0 FBA_DQM1 FBA_DQM2 FBA_DQM3 FBA_DQM4 FBA_DQM5 FBA_DQM6 FBA_DQM7

VMA_WDQS0 VMA_WDQS1 VMA_WDQS2 VMA_WDQS3 VMA_WDQS4 VMA_WDQS5 VMA_WDQS6 VMA_WDQS7
FBA_DQS_WP0 FBA_DQS_WP1 FBA_DQS_WP2 FBA_DQS_WP3 FBA_DQS_WP4 FBA_DQS_WP5 FBA_DQS_WP6 FBA_DQS_WP7

VMA_RDQS0 VMA_RDQS1 VMA_RDQS2 VMA_RDQS3 VMA_RDQS4 VMA_RDQS5 VMA_RDQS6 VMA_RDQS7
FBA_DQS_RN0 FBA_DQS_RN1 FBA_DQS_RN2 FBA_DQS_RN3 FBA_DQS_RN4 FBA_DQS_RN5 FBA_DQS_RN6 FBA_DQS_RN7

FBA_WDS0 FBA_WDS0* FBA_WDS1 FBA_WDS1* FBA_WDS2 FBA_WDS2* FBA_WDS3 FBA_WDS3*

+1.8V
FBVDDQ_1 FBVDDQ_2 FBVDDQ_3 FBVDDQ_4 FBVDDQ_5 FBVDDQ_6 FBVDDQ_7 FBVDDQ_8 FBVDDQ_9 FBVDDQ_10 FBVDDQ_11 FBVDDQ_12 FBVDDQ_13 FBVDDQ_14 FBVDDQ_15 FBVDDQ_16 FBVDDQ_17 FBVDDQ_18 FBVDDQ_19 FBVDDQ_20 FBVDDQ_21 FBVDDQ_22 FBVDDQ_23 FBVDDQ_24 FBVDDQ_25 FBVDDQ_26 FBVDDQ_27

FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63

VMA_DQ0 VMA_DQ1 VMA_DQ2 VMA_DQ3 VMA_DQ4 VMA_DQ5 VMA_DQ6 VMA_DQ7 VMA_DQ8 VMA_DQ9 VMA_DQ10 VMA_DQ11 VMA_DQ12 VMA_DQ13 VMA_DQ14 VMA_DQ15 VMA_DQ16 VMA_DQ17 VMA_DQ18 VMA_DQ19 VMA_DQ20 VMA_DQ21 VMA_DQ22 VMA_DQ23 VMA_DQ24 VMA_DQ25 VMA_DQ26 VMA_DQ27 VMA_DQ28 VMA_DQ29 VMA_DQ30 VMA_DQ31 VMA_DQ32 VMA_DQ33 VMA_DQ34 VMA_DQ35 VMA_DQ36 VMA_DQ37 VMA_DQ38 VMA_DQ39 VMA_DQ40 VMA_DQ41 VMA_DQ42 VMA_DQ43 VMA_DQ44 VMA_DQ45 VMA_DQ46 VMA_DQ47 VMA_DQ48 VMA_DQ49 VMA_DQ50 VMA_DQ51 VMA_DQ52 VMA_DQ53 VMA_DQ54 VMA_DQ55 VMA_DQ56 VMA_DQ57 VMA_DQ58 VMA_DQ59 VMA_DQ60 VMA_DQ61 VMA_DQ62 VMA_DQ63

FBA_CLK0 FBA_CLK0* FBA_CLK1 FBA_CLK1*
T32 VMA_CLK0 T31 VMA_CLK0# AC31 VMA_CLK1 AC30 VMA_CLK1#
VMA_CLK0 [17] VMA_CLK0# [17] VMA_CLK1 [17] VMA_CLK1# [17]

FB_VREF
J27 +FB_VREF1
+1.8V
R92 *1K/F_4
R93 *1K/F_4
15mils width
C207 .1U/10V_4

For Debug only
FBA_DEBUG
T30 FBA_DEBUG *60.4/F_4 R94 +1.8V

FB_DLLAVDD0 FB_PLLAVDD0
AG27 AF27 +FB_PLLAVDD
15mils width
L13 HCB1608KF-181T15_6
+VGA1.1V
C176 .1U/10V_4
C159 .1U/10V_4
C228 1U/6.3V_4

[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]
[18] VMC_DQ[63..0]
[18] VMC_DM[7..0]
[18] VMC_WDQS[7..0]
[18] VMC_RDQS[7..0]

R95 10K/F_4 VMA_ODT
R96 10K/F_4 VMA_CKE
R412 10K/F_4 VMC_ODT
R88 10K/F_4 VMC_CKE

for DDR2 need use CMD11(CKE) and CMD12(ODT)

use internal Vref, ext divider no stuff

MEMORY I/F B

U30C
BGA969-NVIDIA-NB9P-GS
<SKU>

[18] VMC_MA3 [18] VMC_MA0 [18] VMC_MA2 [18] VMC_MA1 [18] VMC_MA3H [18] VMC_MA4H [18] VMC_MA5H
[18] VMC_CS0# [18] VMC_WE# [18] VMC_BA0 [18] VMC_CKE [18] VMC_ODT [18] VMC_MA2H [18] VMC_MA12 [18] VMC_RAS# [18] VMC_MA11 [18] VMC_MA10 [18] VMC_BA1 [18] VMC_MA8 [18] VMC_MA9 [18] VMC_MA6 [18] VMC_MA5 [18] VMC_MA7 [18] VMC_MA4 [18] VMC_CAS#
[18] VMC_BA2
Add for 64x16 vram

FBC_CMD0 FBC_CMD1 FBC_CMD2 FBC_CMD3 FBC_CMD4 FBC_CMD5 FBC_CMD6 FBC_CMD7 FBC_CMD8 FBC_CMD9 FBC_CMD10 FBC_CMD11 FBC_CMD12 FBC_CMD13 FBC_CMD14 FBC_CMD15 FBC_CMD16 FBC_CMD17 FBC_CMD18 FBC_CMD19 FBC_CMD20 FBC_CMD21 FBC_CMD22 FBC_CMD23 FBC_CMD24 FBC_CMD25 FBC_CMD26 FBC_CMD27 FBC_CMD28 FBC_CMD29 FBC_CMD30

VMC_DM0 VMC_DM1 VMC_DM2 VMC_DM3 VMC_DM4 VMC_DM5 VMC_DM6 VMC_DM7
FBC_DQM0 FBC_DQM1 FBC_DQM2 FBC_DQM3 FBC_DQM4 FBC_DQM5 FBC_DQM6 FBC_DQM7

VMC_WDQS0 VMC_WDQS1 VMC_WDQS2 VMC_WDQS3 VMC_WDQS4 VMC_WDQS5 VMC_WDQS6 VMC_WDQS7
FBC_DQS_WP0 FBC_DQS_WP1 FBC_DQS_WP2 FBC_DQS_WP3 FBC_DQS_WP4 FBC_DQS_WP5 FBC_DQS_WP6 FBC_DQS_WP7

VMC_RDQS0 VMC_RDQS1 VMC_RDQS2 VMC_RDQS3 VMC_RDQS4 VMC_RDQS5 VMC_RDQS6 VMC_RDQS7
FBC_DQS_RN0 FBC_DQS_RN1 FBC_DQS_RN2 FBC_DQS_RN3 FBC_DQS_RN4 FBC_DQS_RN5 FBC_DQS_RN6 FBC_DQS_RN7

FBC_WDS0 FBC_WDS0* FBC_WDS1 FBC_WDS1* FBC_WDS2 FBC_WDS2* FBC_WDS3 FBC_WDS3*

+1.8V
FBVDDQ_28 FBVDDQ_29 FBVDDQ_30 FBVDDQ_31 FBVDDQ_32 FBVDDQ_33 FBVDDQ_34 FBVDDQ_35 FBVDDQ_36 FBVDDQ_37 FBVDDQ_38

FBC_D0 FBC_D1 FBC_D2 FBC_D3 FBC_D4 FBC_D5 FBC_D6 FBC_D7 FBC_D8 FBC_D9 FBC_D10 FBC_D11 FBC_D12 FBC_D13 FBC_D14 FBC_D15 FBC_D16 FBC_D17 FBC_D18 FBC_D19 FBC_D20 FBC_D21 FBC_D22 FBC_D23 FBC_D24 FBC_D25 FBC_D26 FBC_D27 FBC_D28 FBC_D29 FBC_D30 FBC_D31 FBC_D32 FBC_D33 FBC_D34 FBC_D35 FBC_D36 FBC_D37 FBC_D38 FBC_D39 FBC_D40 FBC_D41 FBC_D42 FBC_D43 FBC_D44 FBC_D45 FBC_D46 FBC_D47 FBC_D48 FBC_D49 FBC_D50 FBC_D51 FBC_D52 FBC_D53 FBC_D54 FBC_D55 FBC_D56 FBC_D57 FBC_D58 FBC_D59 FBC_D60 FBC_D61 FBC_D62 FBC_D63

VMC_DQ0 VMC_DQ1 VMC_DQ2 VMC_DQ3 VMC_DQ4 VMC_DQ5 VMC_DQ6 VMC_DQ7 VMC_DQ8 VMC_DQ9 VMC_DQ10 VMC_DQ11 VMC_DQ12 VMC_DQ13 VMC_DQ14 VMC_DQ15 VMC_DQ16 VMC_DQ17 VMC_DQ18 VMC_DQ19 VMC_DQ20 VMC_DQ21 VMC_DQ22 VMC_DQ23 VMC_DQ24 VMC_DQ25 VMC_DQ26 VMC_DQ27 VMC_DQ28 VMC_DQ29 VMC_DQ30 VMC_DQ31 VMC_DQ32 VMC_DQ33 VMC_DQ34 VMC_DQ35 VMC_DQ36 VMC_DQ37 VMC_DQ38 VMC_DQ39 VMC_DQ40 VMC_DQ41 VMC_DQ42 VMC_DQ43 VMC_DQ44 VMC_DQ45 VMC_DQ46 VMC_DQ47 VMC_DQ48 VMC_DQ49 VMC_DQ50 VMC_DQ51 VMC_DQ52 VMC_DQ53 VMC_DQ54 VMC_DQ55 VMC_DQ56 VMC_DQ57 VMC_DQ58 VMC_DQ59 VMC_DQ60 VMC_DQ61 VMC_DQ62 VMC_DQ63

FBC_CLK0 FBC_CLK0* FBC_CLK1 FBC_CLK1*
E17 VMC_CLK0 D17 VMC_CLK0# D23 VMC_CLK1 E23 VMC_CLK1#
VMC_CLK0 [18] VMC_CLK0# [18] VMC_CLK1 [18] VMC_CLK1# [18]

FB_CAL_PD_VDDQ
K27 FB_CAL_PD_VDDQ R89 30.1/F_4 +1.8V

FB_CAL_PU_GND
L27 FB_CAL_PU_GND R90 36.5/F_4

FB_CAL_TERM_GND
M27 FB_CAL_TERM_GND R91 *30.1/F_4
R91 Install for DDR3

FBC_DEBUG
G19 FBC_DEBUG R86 *60.4/F_4 +1.8V
R86 no stuff

G96 only
FB_DLLAVDD1 FB_PLLAVDD1
J19 J18 +FB_PLLAVDD
C166 .1U/10V_4
C217 .1U/10V_4

+1.8V
C748 *22P/50V_4
C327 *22P/50V_4
C746 22P/50V_4

+1.8V
C336 4.7U/6.3V_6
C333 .47U/6.3V_4
C676 .47U/6.3V_4
C745 .1U/10V_4
C673 4.7U/6.3V_6
C201 .47U/6.3V_4
C230 .47U/6.3V_4
C222 .1U/10V_4
C720 .1U/10V_4
C218 .1U/10V_4
C219 .1U/10V_4
C140 .1U/10V_4
C718 .1U/10V_4
C221 .1U/10V_4

+1.8V
C680 4.7U/6.3V_6
C334 .47U/6.3V_4
C240 .47U/6.3V_4
C192 .1U/10V_4
C149 4.7U/6.3V_6
C130 .47U/6.3V_4
C145 .47U/6.3V_4
C150 .1U/10V_4
C148 .1U/10V_4
C213 .1U/10V_4
C214 .1U/10V_4
C205 .1U/10V_4
C209 .1U/10V_4
C120 .1U/10V_4

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Quanta Computer Inc.

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Custom	NV10X (MEMORY I/F) 2/5	1A
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U30D

BGA969-NVIDIA-N89P-GS
<SKU>

IFPAB(LVDS)

IFPCD

IFPC

IFPD

TMDS channel two

IFPEF

Display port output

DACA(CRT)

DACC(CRT2)

DACB(TV)

SI Build

XTAL_PLL

STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

Close to GPU

DV2 Add for HDMI port

Pix Ball out and Pin Name

SPREAD SPECTRUM

U8 *ICS91730AMLF-T

I2C ADDRESS: 0xD4H

Install it when not connected to Spread spectrum device

PROJECT :	QL5
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: NV10X (DISPLAY) 3/5
Rev: 1A	
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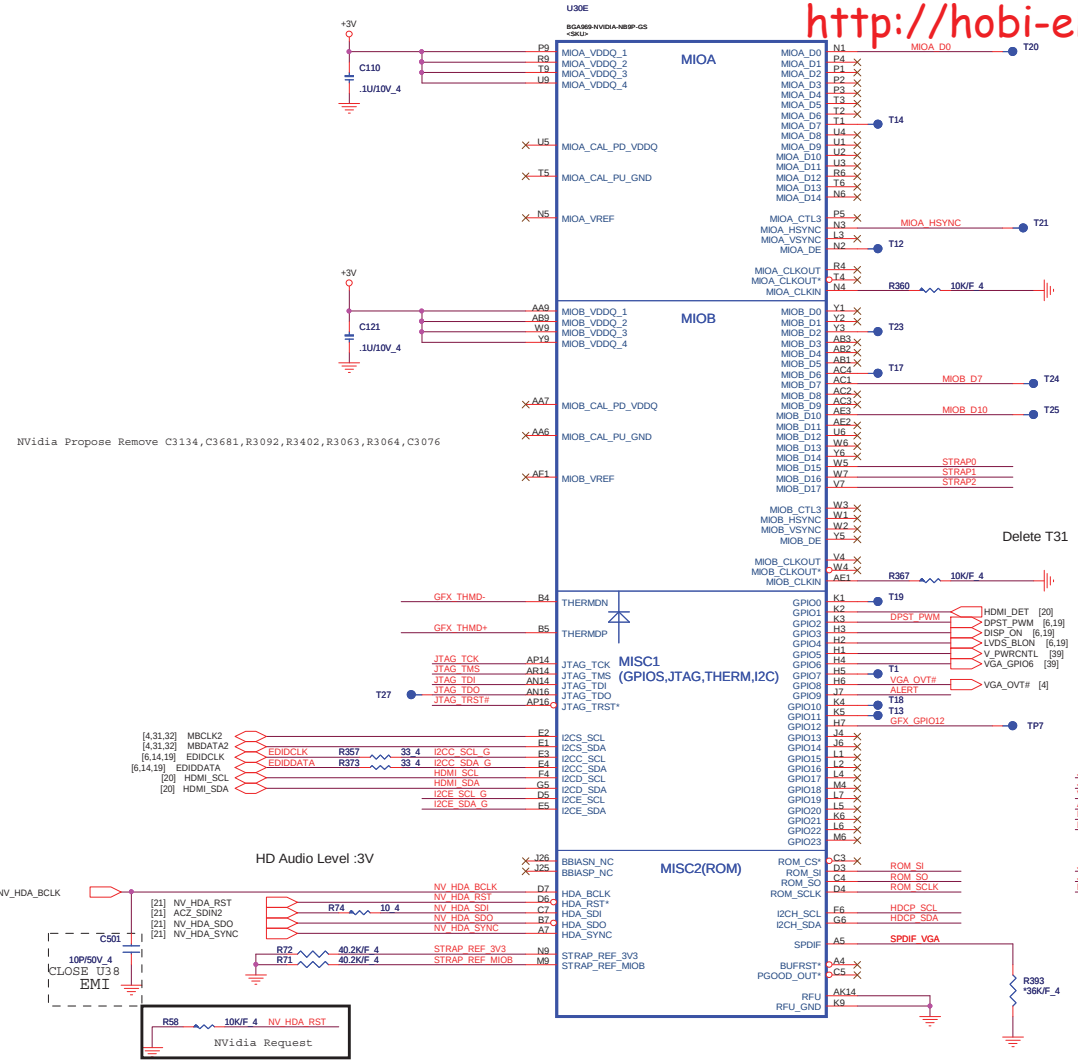
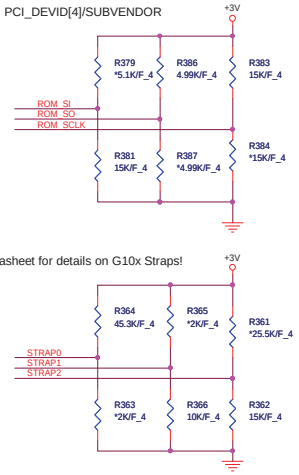


N10P-GE1 (G96) Straps
N10M-GE1 (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



PV	Hynix	Samsung	Qimonda
R381	CS25102FB02 5K	CS31002FB26 10K	CS31502FB24 15K

N10M-GE1	N10P-GE1
R361 25K	R362 15K
R384 15K	R383 15K

Logical Strap Bit Mapping

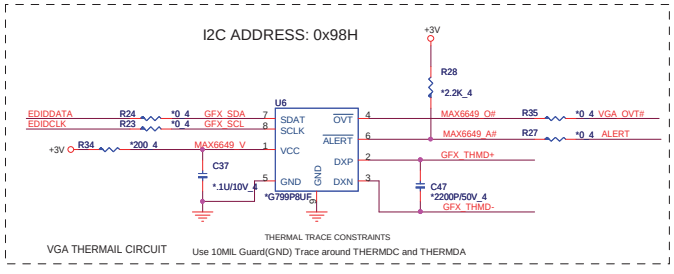
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

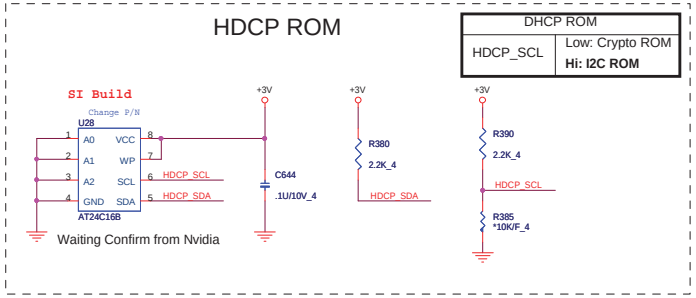
N10M-GE1

RAM_CFG[3:0]	Config	Definitions
	64Mx16 DDR2	Hynix
	64Mx16 DDR2	Samsung
	64Mx16 DDR2	Qimonda

N10P-GE1

RAM_CFG[3:0]	Config	Definitions
0000	64Mx16 DDR2	Hynix
0001	64Mx16 DDR2	Samsung
0010	64Mx16 DDR2	Qimonda





DHCP ROM	
HDCP_SCL	Low: Crypto ROM **Hi: I2C ROM**

PROJECT : QL5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
C	NV10X (GPIO & STRRAPS) 4/5	1A

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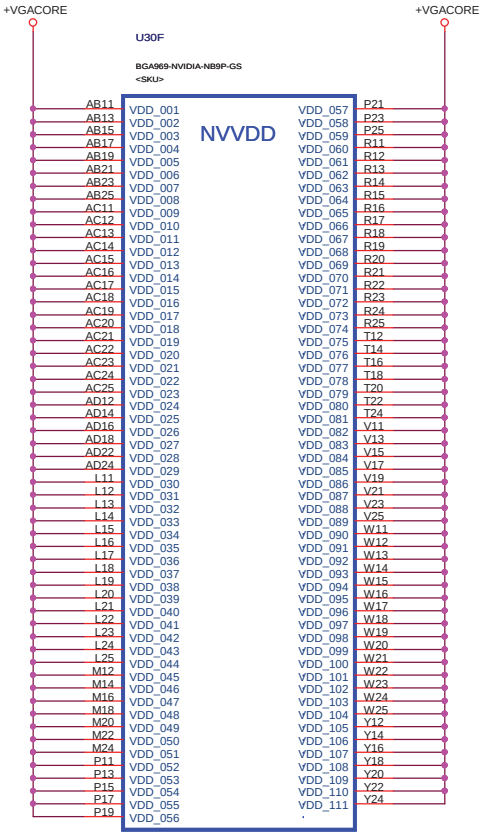
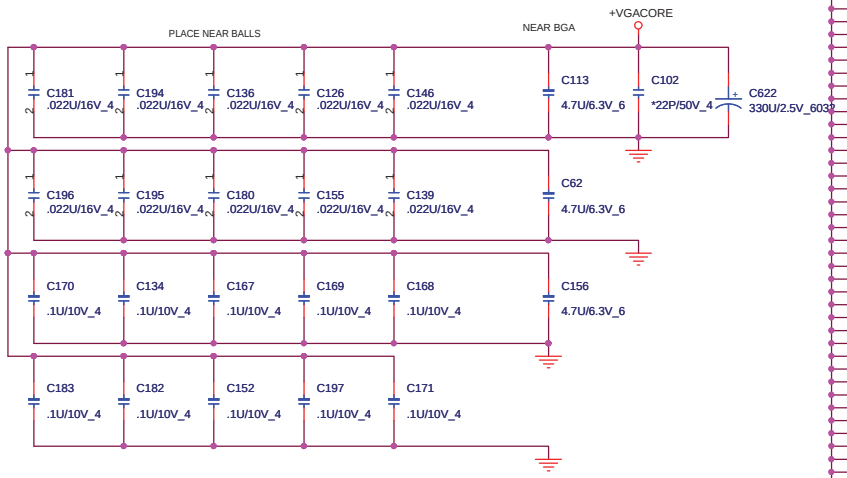
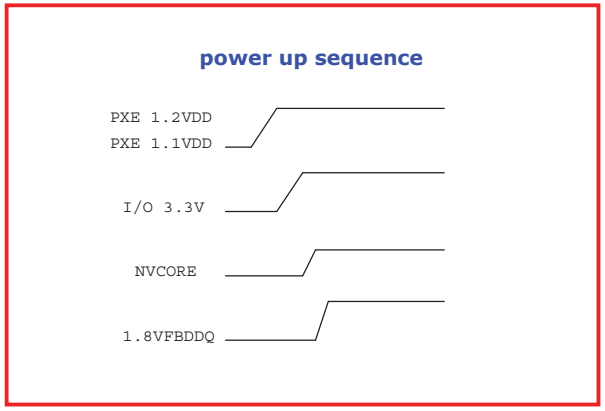
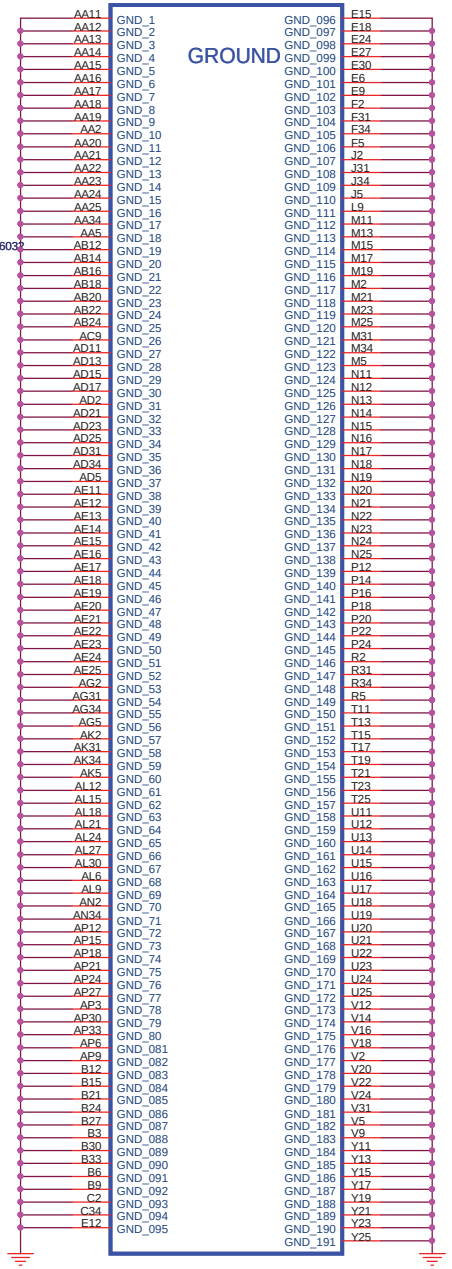
NVVDD Decoupling





Follow Design Guide DG-03276-001 4.7uFx3 and 0.22x10 uF instead of 0.1uF x10





PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV10X (POWER & GND) 5/5	1A
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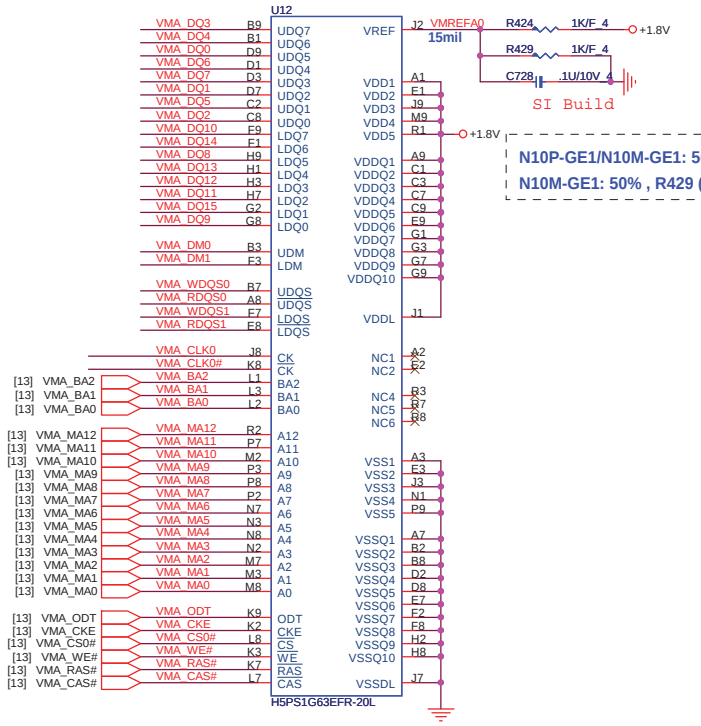
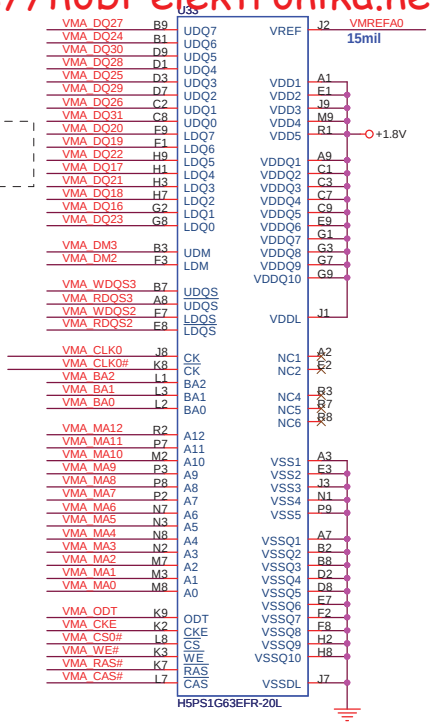
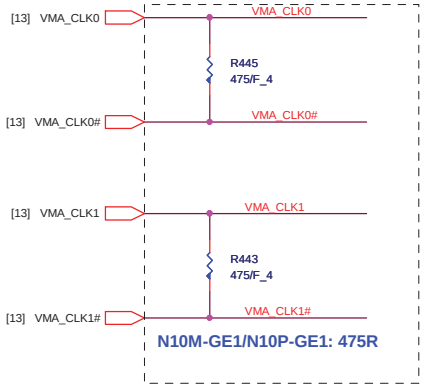
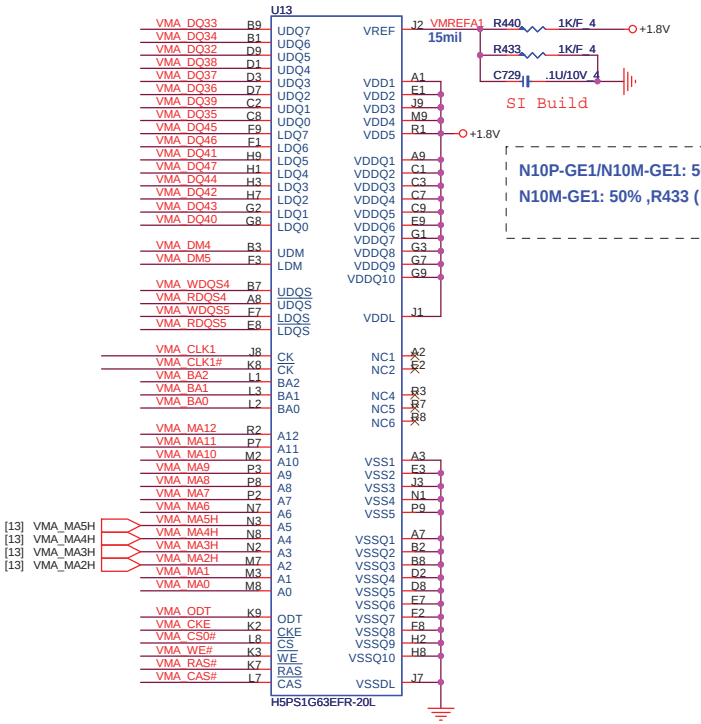
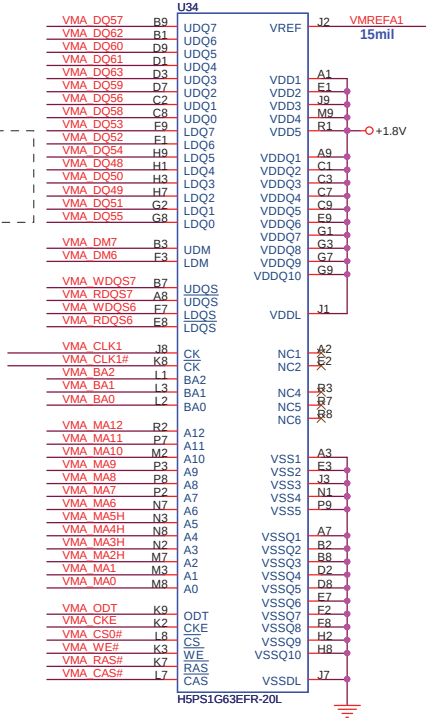




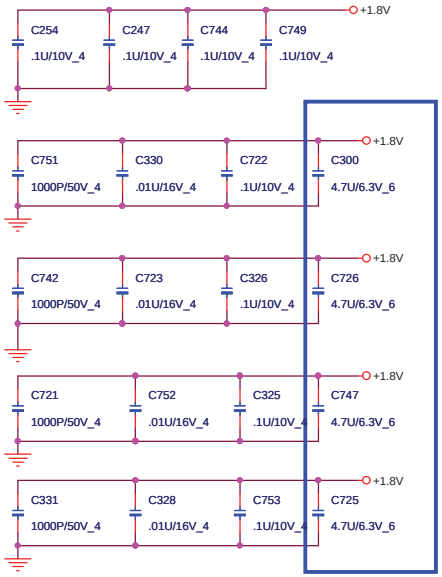


CS14752FB11 RES CHIP 475 1/16W +-1%(0402)





(By pass capacitor)



[13] VMA_DQ[63..0]
[13] VMA_DM[7..0]
[13] VMA_WDQS[7..0]
[13] VMA_RDQS[7..0]

For DB:
N10P/N10M : AKD5LG-T500(Samsung,64M*16)
AKD5LG-T^02(Qimonda 64M*16)
AKD5LG-TW01(Hynix,64M*16)

PROJECT : QL5
Quanta Computer Inc.

NB5

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Custom	NV10X VRAM-1(GDDR2 BGA84)	1A

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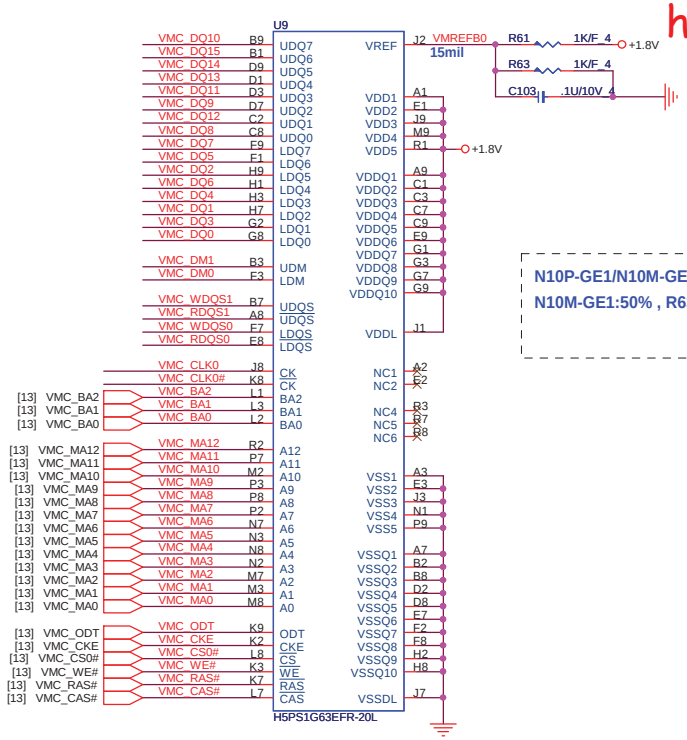
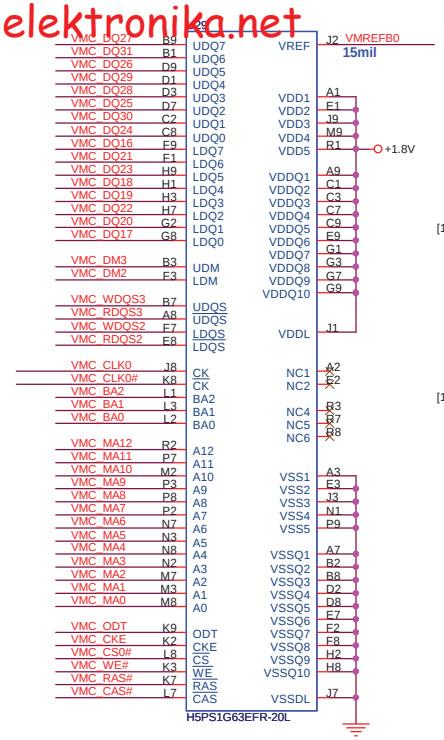
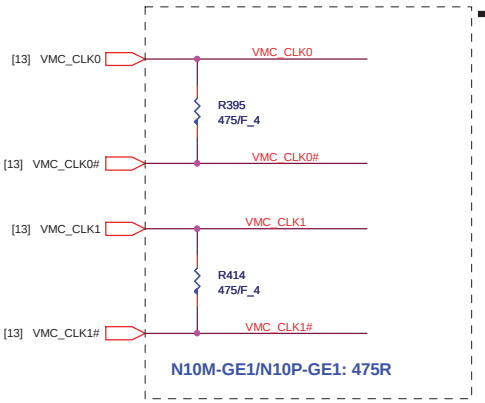
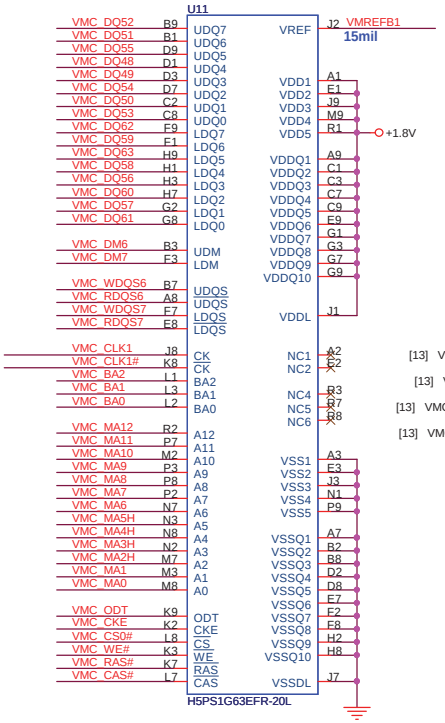
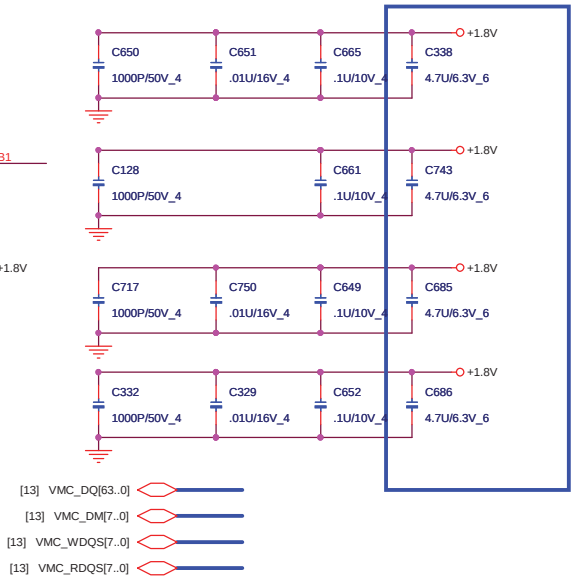






CS14752FB11 RES CHIP 475 1/16W +-1%(0402)





For DB:
N10P/N10M : AKD5LG-T500(Samsung,64M*16)
AKD5LG-T^02(Qimonda 64M*16)
AKD5LG-TW01(Hynix,64M*16)

PROJECT : QL5
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NB5

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1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA

[6] LA_CLK	RP10	*4P2R-S-0	TXLCLKOUT+	
[6] LA_CLK#			TXLCLKOUT-	
[6] LA_DATAP0	RP6	*4P2R-S-0	TXLOUT0+	
[6] LA_DATAN0			TXLOUT0-	
[6] LA_DATAP1	RP8	*4P2R-S-0	TXLOUT1+	
[6] LA_DATAN1			TXLOUT1-	
[6] LA_DATAP2	RP12	*4P2R-S-0	TXLOUT2+	
[6] LA_DATAN2			TXLOUT2-	
[6] LB_CLK#	RP27	*4P2R-S-0	TXUCLKOUT-	
[6] LB_CLK			TXUCLKOUT+	
[6] LB_DATAP0	RP14	*4P2R-S-0	TXUOUT0+	
[6] LB_DATAN0			TXUOUT0-	
[6] LB_DATAP1	RP16	*4P2R-S-0	TXUOUT1+	
[6] LB_DATAN1			TXUOUT1-	
[6] LB_DATAP2	RP21	*4P2R-S-0	TXUOUT2+	
[6] LB_DATAN2			TXUOUT2-	

OPTION SIGNAL FROM Nvidia to VGA

[14] EXT_TXLCLKOUT+	RP9	4P2R-S-0	TXLCLKOUT+	
[14] EXT_TXLCLKOUT-			TXLCLKOUT-	
[14] EXT_TXLOUT0-	RP5	4P2R-S-0	TXLOUT0-	
[14] EXT_TXLOUT0+			TXLOUT0+	
[14] EXT_TXLOUT1+	RP7	4P2R-S-0	TXLOUT1+	
[14] EXT_TXLOUT1-			TXLOUT1-	
[14] EXT_TXLOUT2+	RP11	4P2R-S-0	TXLOUT2+	
[14] EXT_TXLOUT2-			TXLOUT2-	
[14] EXT_TXUCLKOUT+	RP26	4P2R-S-0	TXUCLKOUT+	
[14] EXT_TXUCLKOUT-			TXUCLKOUT-	
[14] EXT_TXUOUT0+	RP13	4P2R-S-0	TXUOUT0+	
[14] EXT_TXUOUT0-			TXUOUT0-	
[14] EXT_TXUOUT1-	RP15	4P2R-S-0	TXUOUT1-	
[14] EXT_TXUOUT1+			TXUOUT1+	
[14] EXT_TXUOUT2+	RP20	4P2R-S-0	TXUOUT2+	
[14] EXT_TXUOUT2-			TXUOUT2-	

[2,4,6,9,10,11,12,14,15,20,21,22,23,24,26,27,28,30,31,32,33,34,38,41] +3V
[1,42,43,44] +5V
[35,36,37,38,39,40,41] +VIN
[21,27,31,32,35,36,39,41] +3VPCU
[36,41] +15VALW

+3V R1 2.2K_4 EDIDCLK
R2 2.2K_4 EDIDDATA

+3.6V_CAM C17 *4.7U/6.3V_6 C18 .01U/16V_4
DIGITAL_D1 DIGITAL_CLK C15 33P/50V_4 C14 33P/50V_4 EMI

+3VLCD_CON
+3V
[6,14,15] EDIDCLK
[6,14,15] EDIDDATA
C4 1000P/50V_4

CN2
TXLOUT0- TXLOUT0+
TXLOUT1- TXLOUT1+
TXLOUT2- TXLOUT2+
TXLCLKOUT- TXLCLKOUT+
TXUOUT0- TXUOUT0+
TXUOUT1- TXUOUT1+
TXUOUT2- TXUOUT2+
TXUCLKOUT- TXUCLKOUT+
VADJ1
BLON_CON
FOX-GS12401-1011

MIC
[26] DIGITAL_D1
[26] DIGITAL_CLK
[22] USBP9-
[22] USBP9+
L3 SBK160808T-301Y-N
L4 SBK160808T-301Y-N
L5 *WCM2012-90
+3.6V_CAM
CAMERA
CN3
USB CAMERA CONN
87213-0600-6P-L

DV3 change to Short Pad
[6,15] DPST_PWM R4 *0_4/S short0402
[32] PWM_VADJ R3 *0_4
DV2 Modify
VADJ1
C5 *4.7U/6.3V_6 C7 .1U/10V_4

+VIN_BLIGHT
+VIN L2 FBM2125 HM330-T
C6 .1U/50V_6
C9 .01U/50V_4
C10 .1U/50V_6
C8 *10U/25V_12

USB CAMERA POWER
+3V +5V +3.6V_CAM
R9 *0_6 R12 *0_6
+5V U2 VIN VOUT SHDN GND SET
C19 1U/6.3V_4
R1 R10 215K/F/04
R2 R11 100K/F/04
IC(5P) G913C (SOT23-5)EP
C16 4.7U/6.3V_6

+3VPCU R6 33K_6
Close to EC
[6,15] LVDS_BLON R7 1K/F_4 D3 RB501V-40 LID_EC# [31,32]
PN_BLON D2 RB501V-40 BLON_CON
[23] LCD_BK Q1 DTC144EUA
R5 100K/F_4 C13 22P/50V_4

Vout=1.25(1+R1/R2)

+15VALW R328 330K_6
+5VSUS R330 100K/F_4
Q10 AO3404
AO3404 ID current 5.8A
C608 .1U/10V_4
+3V
+3VLCD
LCDONG
Q13 2N7002
C607 .022U/16V_4
Q12 DTC144EUA
[6,15] DISP_ON
LCDON#
Q11 2N7002
L1 PBY201209T-4A/08
R327 22_8
LCDDISCHG
+3VLCD_CON
C2 .01U/16V_4 C3 .1U/10V_4 C1 10U/6.3V_8

DISP_ON R329 100K/F_4
LVDS_BLON R8 100K/F_4

NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
B	LCD CONN/Lid function	1A
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CRT PORT

CN14
070546FR015S202CR

+5VCRT — C611 1U/10V_4 — 40 MIL

+5V — F2 40 mils — +5VCRT

FUSE1A6V_POLY SSM14 spec is 40V 1A

[6,14] CRT_R — CRT_R — L8 BLM18BA470SN1 — CRT_R1
[6,14] CRT_G — CRT_G — L7 BLM18BA470SN1 — CRT_G1
[6,14] CRT_B — CRT_B — L6 BLM18BA470SN1 — CRT_B1

R25 150/F_4 | R20 150/F_4 | R19 150/F_4
C35 6.8P/50V_4 | C29 6.8P/50V_4 | C27 6.8P/50V_4
C26 6.8P/50V_4 | C31 6.8P/50V_4 | C34 6.8P/50V_4

EMI

+5V — C24 .1U/10V_4 — U3 M74VHC1GT125DF2G — [6,14] VSYNC_COM — PR_VSYNC
U4 M74VHC1GT125DF2G — [6,14] HSYNC_COM — PR_HSYNC

R15 *0_4/S short0402 — DDCCLK3
R341 *0_4/S short0402 — CRTVSYNC
R342 *0_4/S short0402 — CRTHSYNC
R340 *0_4/S short0402 — DDCDAT3

C23 *470P/50V_4 | C613 *47P/50V_4 | C614 *47P/50V_4 | C612 *470P/50V_4

+3V — Q2 2N7002EPT — R14 2.2K_4 — [6,14] DDCCLK — DDCCLK
+3V — Q14 2N7002EPT — R339 2.2K_4 — [6,14] DDCDATA — DDCDAT2

DV2-Change footprint

+5VCRT — RB501V-40 D4 — +5V_CRT2 — R13 2.2K_4 | R338 2.2K_4

+3V
D25 *BAV99W — CRT_R
D24 *BAV99W — CRT_G
D23 *BAV99W — CRT_B
D5 *BAV99W — DDCCLK2
D21 *BAV99W — PR_VSYNC
D22 *BAV99W — PR_HSYNC
D20 *BAV99W — DDCDAT2

For UMA HDMI function

+3V — L35 *0_6 EMI — +3V_LS

PC0 R394 *0_4
PC1 R389 *0_4
REXT R382 *0_4
RT_EN# R353 *0_4
CFG1 R47 *0_4
CFG0 R53 *0_4

C82 *.1U/10V_4 | C627 *.01U/16V_4 | C647 *.01U/16V_4 | C64 *.01U/16V_4
C621 *.01U/16V_4 | C626 *.1U/10V_4

TXC_HDMI+ / TXC_HDMI- — *4P2R-S-0 — RP2 — N_TXC_HDMI+ / N_TXC_HDMI-
TX0_HDMI+ / TX0_HDMI- — *4P2R-S-0 — RP4 — N_TX0_HDMI+ / N_TX0_HDMI-
TX1_HDMI+ / TX1_HDMI- — *4P2R-S-0 — RP3 — N_TX1_HDMI+ / N_TX1_HDMI-
TX2_HDMI+ / TX2_HDMI- — *4P2R-S-0 — RP1 — N_TX2_HDMI+ / N_TX2_HDMI-

U27

POWER: VCC ×10
CONTROL: DDC_EN, PC0, PC1, DDCBUF_EN, CFG, RT_EN#, OE#, REXT
GND: GND ×16, EPAD

IN_D1+ / IN_D1- — [6] IN_CLK / IN_CLK# — OUT_D1+ / OUT_D1- — TXC_HDMI+ / TXC_HDMI-
IN_D2+ / IN_D2- — [6] IN_D0 / IN_D0# — OUT_D2+ / OUT_D2- — TX0_HDMI+ / TX0_HDMI-
IN_D3+ / IN_D3- — [6] IN_D1 / IN_D1# — OUT_D3+ / OUT_D3- — TX1_HDMI+ / TX1_HDMI-
IN_D4+ / IN_D4- — [6] IN_D2 / IN_D2# — OUT_D4+ / OUT_D4- — TX2_HDMI+ / TX2_HDMI-
SCL — [6] SDVO_CLK — SCL_SINK — HDMI_SCL
SDA — [6] SDVO_DATA — SDA_SINK — HDMI_SDA
HPD — [6] HDMI_HPD_CON — HPD_SINK — HDMI_DET

R355 *2K/F_4 — SDVO_DATA
R354 *2K/F_4 — SDVO_CLK

+3V
R350 *4.7K_4 — DDC_EN
R391 *4.7K_4 — PC0
R388 *4.7K_4 — PC1
R48 *4.7K_4 — CFG1
R50 *4.7K_4 — CFG0

R378 *499/F_4 — REXT
R547 *4.7K_4 — DV3 Add

*PI3VDP411LSZDE

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CFG1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

+5V_HDMIC — D11 RB501V-40 — R112 2K/F_4 | R109 2K/F_4

[15] HDMI_SCL — R110 33_4 — HDMI_SCL_C
[15] HDMI_SDA — R111 33_4 — HDMI_SDA_C

DV3 Change to ShortPad
L16 *0_6/S short0603 — HDMISCL
L18 *0_6/S short0603 — HDMISDA

C708 *10P/50V_4 | C703 *10P/50V_4

For EXT VGA

UMA : 0R
N10M/N10P-GE1: 0.1uF

[14] N_TX2_HDMI+ — R59 *100/F_4 — N_TX2_HDMI+ — C351 .1U/10V_4 | C352 *22P/50V_4 | C354 .1U/10V_4
[14] N_TX2_HDMI- — N_TX2_HDMI-
[14] N_TX1_HDMI+ — R55 *100/F_4 — N_TX1_HDMI+ — C337 .1U/10V_4 | C323 *22P/50V_4 | C319 .1U/10V_4
[14] N_TX1_HDMI- — N_TX1_HDMI-
[14] N_TX0_HDMI+ — R57 *100/F_4 — N_TX0_HDMI+ — C342 .1U/10V_4 | C346 *22P/50V_4 | C347 .1U/10V_4
[14] N_TX0_HDMI- — N_TX0_HDMI-
[14] N_TXC_HDMI+ — R54 *100/F_4 — N_TXC_HDMI+ — C316 .1U/10V_4 | C314 *22P/50V_4 | C308 .1U/10V_4
[14] N_TXC_HDMI- — N_TXC_HDMI-

C_TX2_HDMI+ / C_TX2_HDMI-
C_TX1_HDMI+ / C_TX1_HDMI-
C_TX0_HDMI+ / C_TX0_HDMI-
C_TXC_HDMI+ / C_TXC_HDMI-

Only for NVIDIA
Q16 2N7002

R431 499/F_4 — C_TX2_HDMI+
R438 499/F_4 — C_TX2_HDMI-
R423 499/F_4 — C_TX1_HDMI+
R420 499/F_4 — C_TX1_HDMI-
R426 499/F_4 — C_TX0_HDMI+
R428 499/F_4 — C_TX0_HDMI-
R419 499/F_4 — C_TXC_HDMI+
R417 499/F_4 — C_TXC_HDMI-

CN20 HDMI CONN
SHELL1 SHELL3 SHELL4 SHELL2
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET

+5VO — F1 FUSE1A6V_POLY — +5V_HDMIC — C710 220P/50V_4

HDMI_DET_N — L40 *0_6/S_HDMI_DET_C short0603

[32] HDMI_DET1 — R204 *0_4
[15] HDMI_DET — R33 10K/F_4 — HDMI_DET_N
D6 BAV99W — R30 100K/F_4

HDMI PORT

+5V_HDMIC — C294 *.01U/16V_4 — for EMI request

NB5

PROJECT : QL5
Quanta Computer Inc.

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C	CRT/PS8101 HDMI Conn	1A

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[19,27,31,32,35,36,39,41] +3VPCU
[24] +3VRTC
[2,4,6,9,10,11,12,14,15,19,20,22,23,24,26,27,28,30,31,32,33,34,38,41] +3V
[4,9,22,24,26,27,30,33,37,41] +1.5V
[2,3,4,5,6,8,9,24,31,37,38] +1.05V
[22,23,24,30,41] +3VS5

U38A

ICH9M REV 1.0

RTC / LPC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN, LAN100_SLP, FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23

LAN / GLAN: LAN_RXD0, LAN_RXD1, LAN_RXD2, LAN_TXD0, LAN_TXD1, LAN_TXD2, GLAN_CLK, LAN_RSTSYNC, GLAN_COMPI, GLAN_COMPO, GPIO56

CPU: A20GATE, A20M#, DPRSTP#, DPSLP#, FERR#, CPUPWRGD, IGNNE#, INIT#, INTR, RCIN#, NMI, SMI#, STPCLK#, THRMTRIP#, TP12

HDA: HDA_BIT_CLK, HDA_SYNC, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDOUT, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO34, SATALED#

SATA: SATA0RXN, SATA0RXP, SATA0TXN, SATA0TXP, SATA1RXN, SATA1RXP, SATA1TXN, SATA1TXP, SATA4RXN, SATA4RXP, SATA4TXN, SATA4TXP, SATA5RXN, SATA5RXP, SATA5TXN, SATA5TXP, SATA_CLKN, SATA_CLKP, SATARBIAS#, SATARBIAS

20MIL
For CR2032(Large)
BT1 BAT_CONN
DV2 change to DFHS02FS609

Notice: GPIO33 is also a strap pin. Don't pull it to high.

HP Request

SATA HDD1

SATA ODD

E-SATA CONNECT

ALC272

MDC

North Bridge

Nvidia

Close to U45

SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

PROJECT :	QL5
Quanta Computer Inc.	
Size: Custom	Document Number: ICH9-M Host 1/4
Rev: 1A	
Date: Tuesday, March 17, 2009	Sheet 21 of 41

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[4,9,21,24,26,27,30,33,37,41] +1.5V
[2,4,6,9,10,11,12,14,15,19,20,21,23,24,26,27,28,30,31,32,33,34,38,41] +3V
[23,25,26,33,37,39,41] +3VSUS

MINI CARD PCI-E(WLAN)

EXPRESS CARD (NEW CARD)

MINI CARD PCI-E(WWAN)

PCIE-LAN

U38D

PCI-Express / Direct Media Interface

SPI

USB

ICH9M REV 1.0

E-SATA and USB Connector
USB Connector
USB Connector
Card reader
NEW CARD
BLUETOOTH
Carama USB
WLAN Min-Card
WWAN Min-Card

DV2-FOR ITPM

U15 *W25X40VSSIG

512K byte SPI ROM
For HDCP only
For GM HDCP

EMI

U38B

PCI

Interrupt I/F

ICH9M REV 1.0

RP50 RP61 RP51 RP52 10P8R-8.2K

U39 *MC74VHC1G08DFT2G

PROJECT : QL5
Quanta Computer Inc.
NB5
Size Custom
Document Number ICH9-M PCIE 2/4
Rev 1A
Date: Tuesday, March 17, 2009
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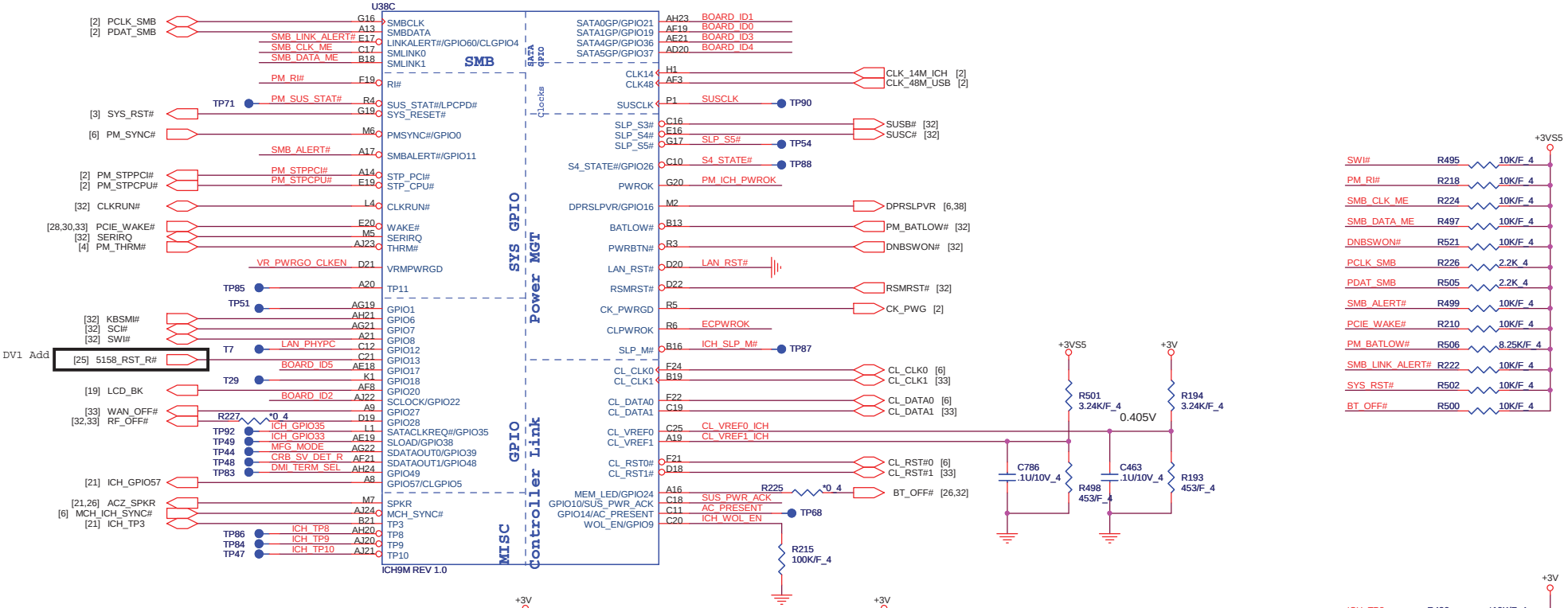
[4,9,21,22,24,26,27,30,33,37,41] +1.5V
[2,4,6,9,10,11,12,14,15,19,20,21,22,24,26,27,28,30,31,32,33,34,38,41] +3V
[21,22,24,30,41] +3VS5
[25,26,33,37,39,41] +3VSUS



System Board ID

PV change system board ID set

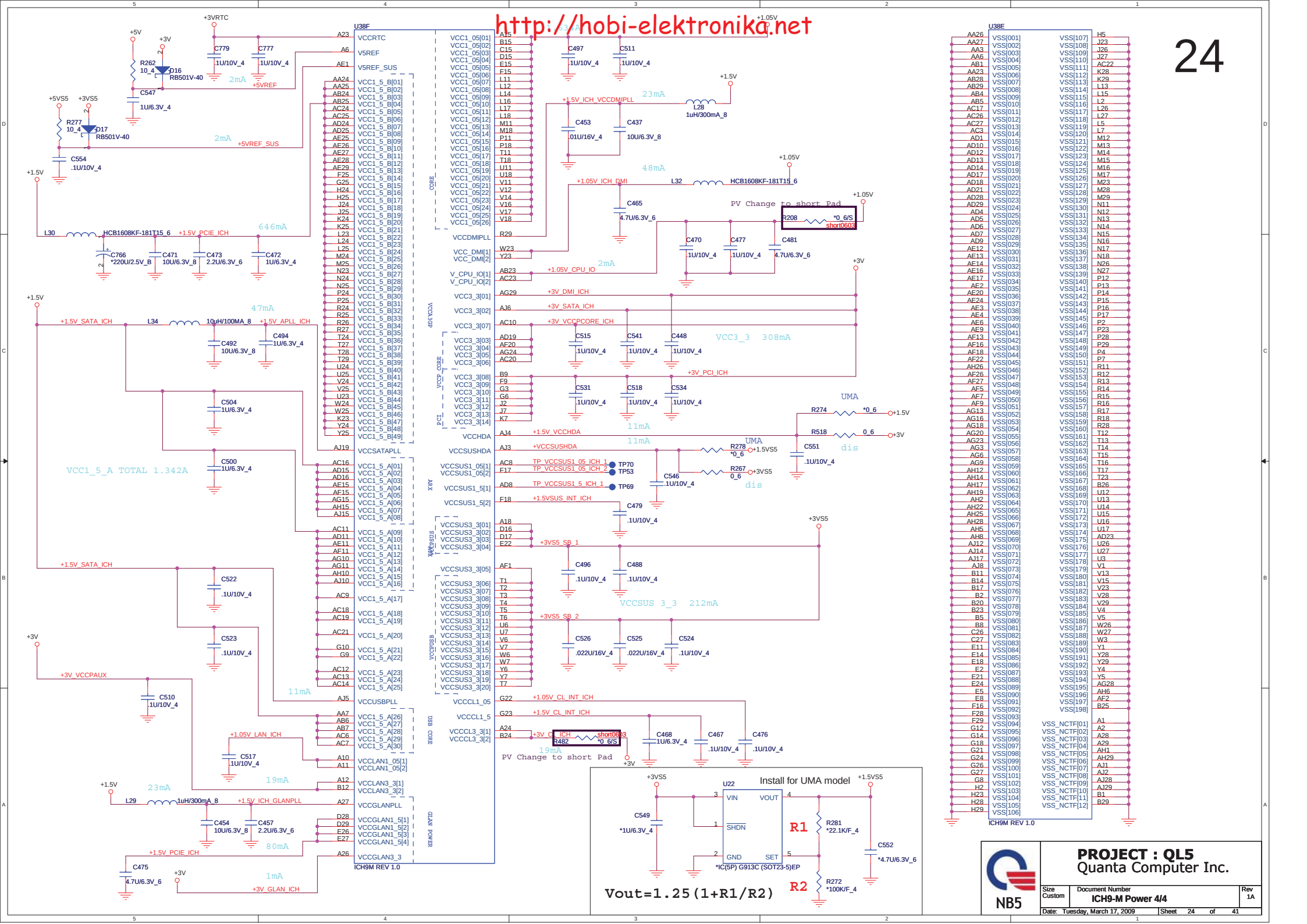
		ID 5	ID 4	ID 3	ID 2	ID 1	ID 0
QL5	GL40	1	0	1	0	0	0
QL5	GM45	1	0	1	0	0	0
QL5	N10M	1	0	1	1	0	0
QL5	N10P	1	0	1	0	0	0

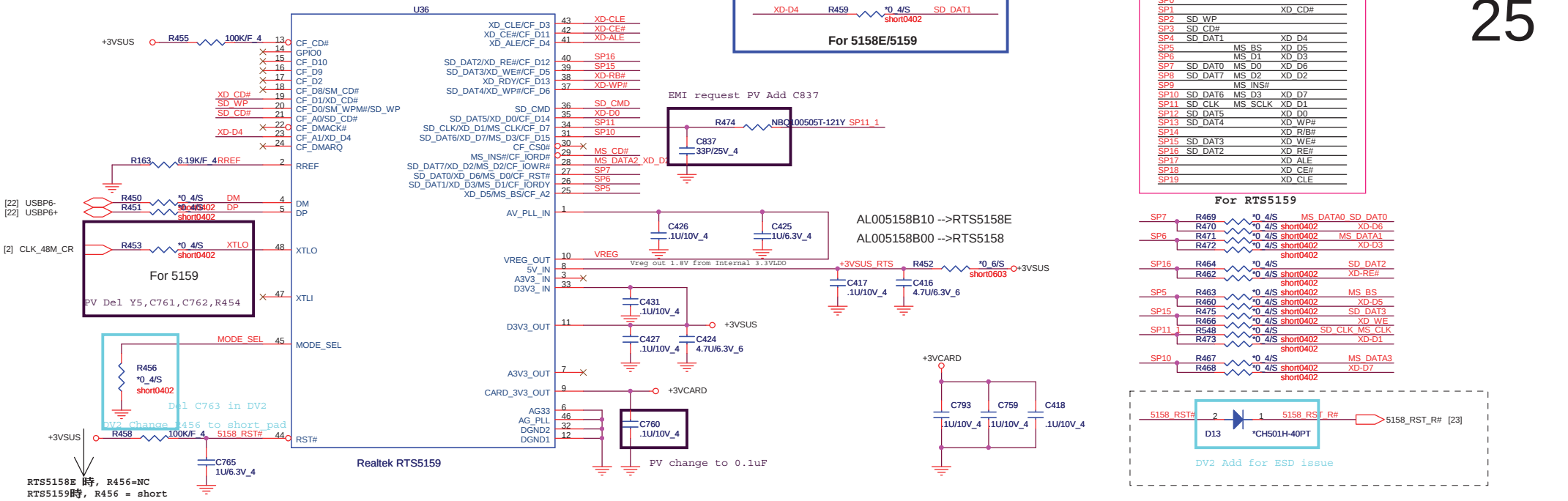
NB5

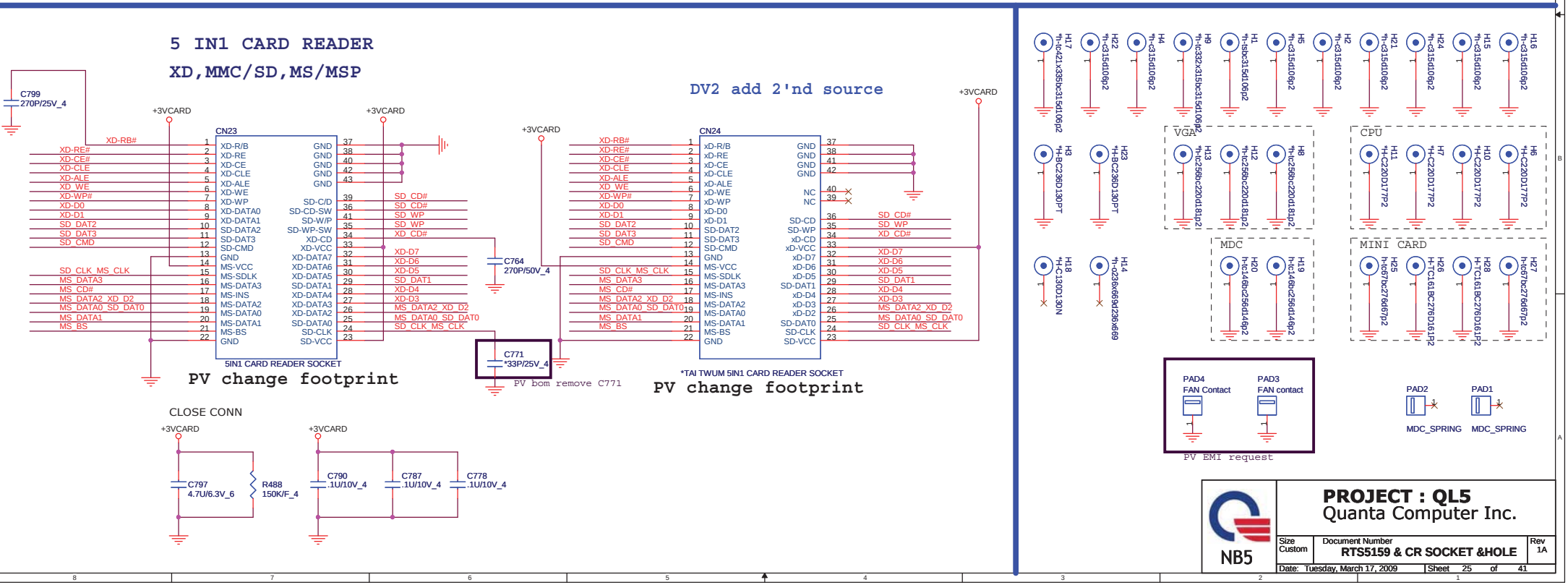
PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	1A

Date: Tuesday, March 17, 2009 | Sheet 23 of 41



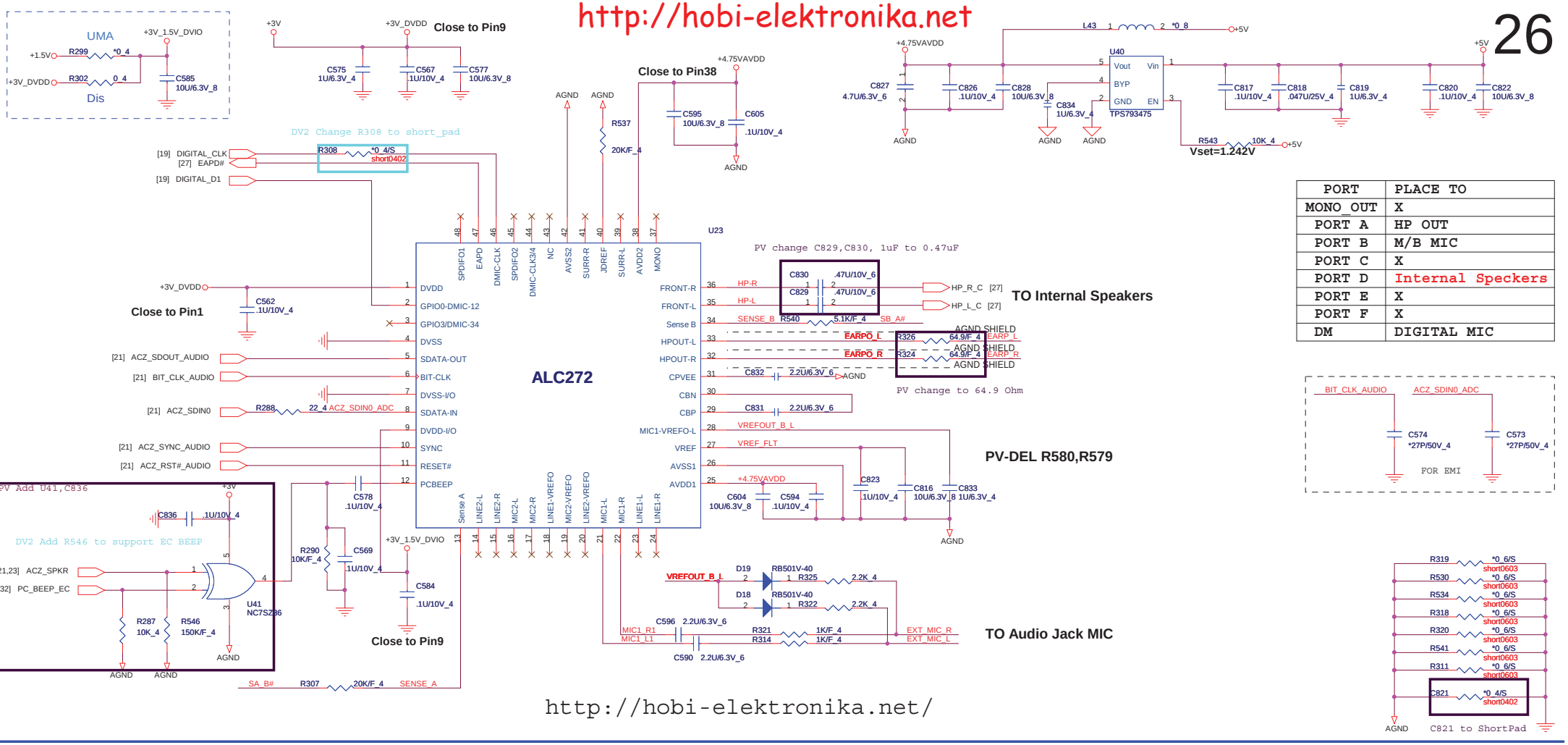




PROJECT : QL5
Quanta Computer Inc.

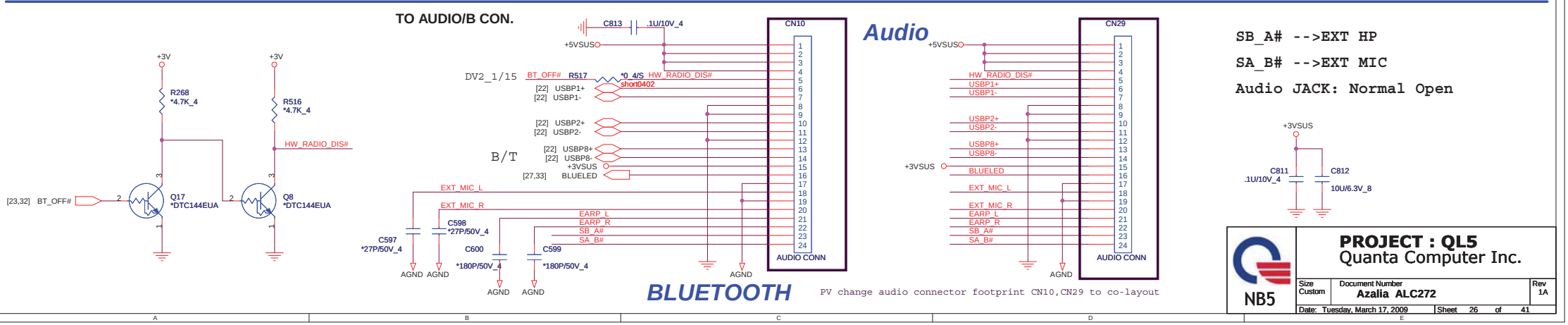
Size	Document Number	Rev
Custom	RTS5159 & CR SOCKET &HOLE	1A

Date: Tuesday, March 17, 2009 Sheet 25 of 41



PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	X
PORT F	X
DM	DIGITAL MIC

http://hobi-elektronika.net/



NB5

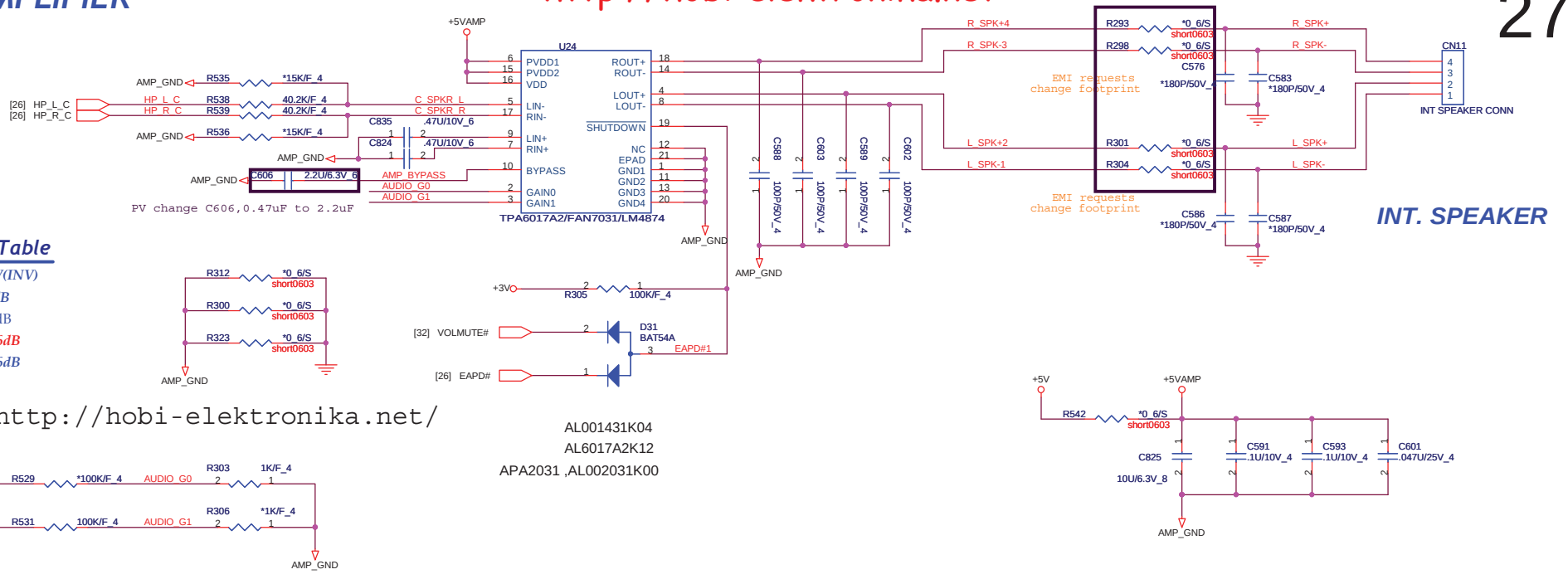
PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia ALC272	1A
Date: Tuesday, March 17, 2009	Sheet 26 of 41	

AUDIO AMPLIFIER

http://hobi-elektronika.net

27



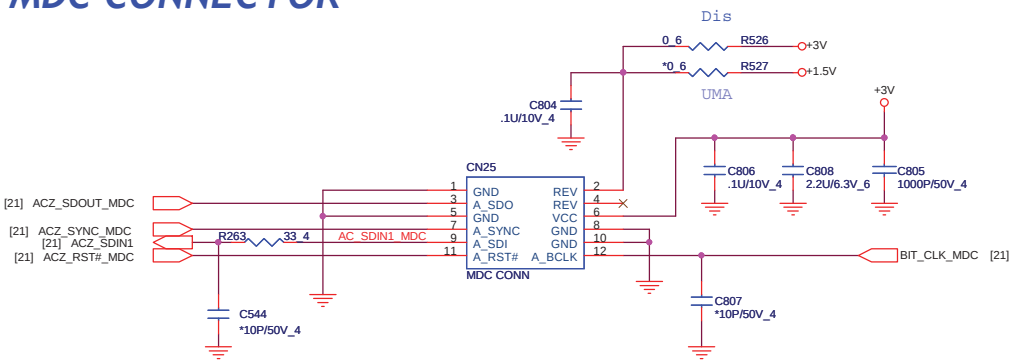
6017A2 Gain Table

GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

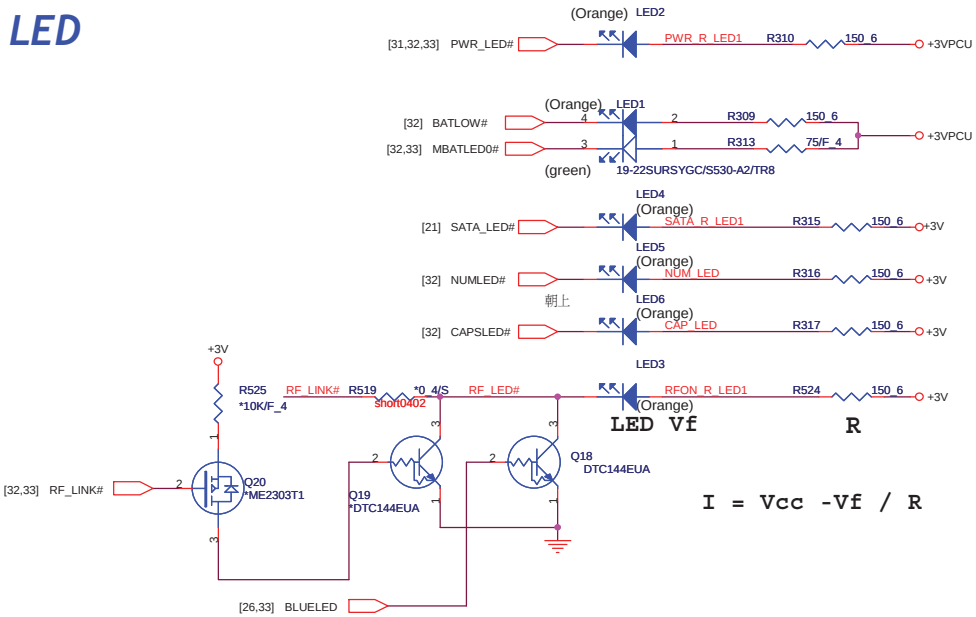
http://hobi-elektronika.net/

AL001431K04
AL6017A2K12
APA2031 ,AL002031K00

MDC CONNECTOR



LED



NB5	**PROJECT : QL5** Quanta Computer Inc.
Size: Custom	Document Number: AMP_TPA6017/Accelerometer
Rev: 1A	
Date: Tuesday, March 17, 2009	Sheet 27 of 41

T : Stuffed for RTL8111DL(10/100/1000)

E : Stuffed for 8103EL(10/100)

for RTL8111DL use

close Pin 44,45

C755 10U/6.3V_8

C754 10U/6.3V_8

C757 0.1U/10V_4

+CTRL12DVDD

+CTRL12DVDD

for RTL8111DL use

R449 0_6 +3V_LAN

R442 *0_6 +DVDD12_LAN

for RTL8103E use

Remove R3571,R3573

R3571 and R3573 are used in RTL8111DL , remove R3573 if switching regulator is enable , Remove R3571 external power is used.

Y1

25MHZ

C392 33P/50V_4

C384 33P/50V_4

DV2 change C384,C392 22p to 33p

XTAL1

XTAL2

+CTRL12DVDD

R141 2.49K/F_4 LANRSET

ENSWREG

+3V_LAN

+DVDD12_LAN

LAN_TX#

[29] +CTRL12A

+CTRL12A

+3V_LAN

U14

RTL8103EL/8111DL

AVDD33 MDIP0 MDIN0 NC/FB12 MDIP1 MDIN1 GND1 NC/MDIP2 NC/MDIN2 DVDD12/AVDD12 NC/MDIP3 NC/MDIN3

VCTRL12A/SROUT12 GND4 RSET VCTRL2V/VDDSR NCVDD33 NCENSWREG CKTAL2 CKTAL1 NCAVDD33 NCLX_LX1 LED0 VDD33B

DVDD12 GND2 HSIP HSIN REFCLK_P REFCLK_N EVDD12 HSOP HSON NC/GPO NC/GPO NCNC

DVDD12B LED1/EESK LED2/EEDI LED3/EEDO EECS GND3 DVDD12A VDD33A ISOLATEB PERSTB LANWAKEB CLKREQB

+3V_LAN +DVDD12_LAN +DVDD12_LAN

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- +DVDD12_LAN MDI3+ MDI3-

LAN_GLINK100# LAN_GLINK10# R149 3.6K_6 +3V_LAN

EECS

+DVDD12_LAN +3V_LAN

ISOLATEB

LAN_REST_R# R147 *0_4 R148 *0_4/S short0402 LAN_REST# [32]

PCIE_WAKE# PLTRST# [22,30,32,33] PCIE_WAKE# [23,30,33]

R148 DV3 Change to short -pad

for RTL8103E use

R150 *1K/F_4

+3V

R156 *1K/F_4

ISOLATEB

R157 100_4 LAN_DISABLE# [21,32]

R155 15K/F_4

*RB501V-40 D12

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

+DVDD12_LAN

LAN CABLE DETECT [32]

[22] PCIE_TXP6_LAN PCIE_TXP6_LAN

[22] PCIE_TXN6_LAN PCIE_TXN6_LAN

[2] CLK_PCIE_LAN CLK_PCIE_LAN

[2] CLK_PCIE_LAN# CLK_PCIE_LAN#

PCIE_RXN6_LAN_L C396 0.1U/10V_4 PCIE_RXN6_LAN [22]

PCIE_RXP6_LAN_L C391 0.1U/10V_4 PCIE_RXP6_LAN [22]

EVDD12

AL08111DB00 RTL8111DL-GR

AL08103EB00 RTL8103EL-GR

LAN_GLINK100# LAN_GLED#

LAN_TX# R70 *0_4/S short0402 LAN_YLED#

C144 *.01U/16V_4 C122 *.01U/16V_4

Link

U26

NS892405

TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-

MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4+ MX4-

C42 .01U/16V_4 V_DAC0

C55 .01U/16V_4 V_DAC1

C63 .01U/16V_4 V_DAC2

C75 .01U/16V_4 V_DAC3

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-

LAN_MCT0 C73 0.01U/100V_0603 R42 75/F_4

LAN_MX0+ LAN_MX0-

LAN_MCT1 C81 0.01U/100V_0603 R45 75/F_4

LAN_MX1+ LAN_MX1-

LAN_MCT2 C91 0.01U/100V_0603 R51 75/F_4

LAN_MX2+ LAN_MX2-

LAN_MCT3 C98 0.01U/100V_0603 R56 75/F_4

LAN_MX3+ LAN_MX3-

C43 1000P/3KV_1808

NS892402:GIGABIT DB0AT9LAN05

NS892405:10/100 DB0ZB1LAN04

RJ45

CN18

C100F9-110A4-L

+3V_LAN R64 330/F_4

C105,C135 FOR EMI CLOSE TO RJ45

C105 .1U/10V_4

LAN_YLED LAN_YLED# LED_YEL_P LED_YEL_N

LAN_MX0+ LAN_MX0- LAN_MX1+ LAN_MX2+ LAN_MX2- LAN_MX1- LAN_MX3+ LAN_MX3-

MX0+ MX0- MX1+ MX2+ MX2- MX1- MX3+ MX3- GND GND GND

+3V_LAN R73 330/F_4

C135 .1U/10V_4

LAN_GLED LAN_GLED# LED_GRE_P LED_GRE_N

TIP RING

CN19

RJ-11 CON

C242 470P/3KV-1808 C233 470P/3KV-1808

CHASSIS2_GND C255 .01U/16V_4 C256 .01U/16V_4

CHASSIS1_GND C50 *.01U/16V_4 C49 *.01U/16V_4

NB5

PROJECT : QL5

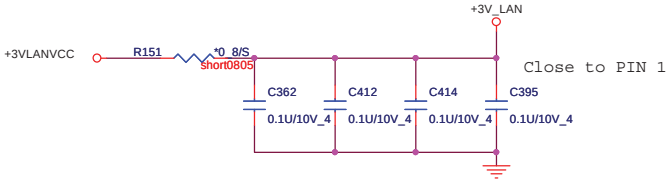
Quanta Computer Inc.

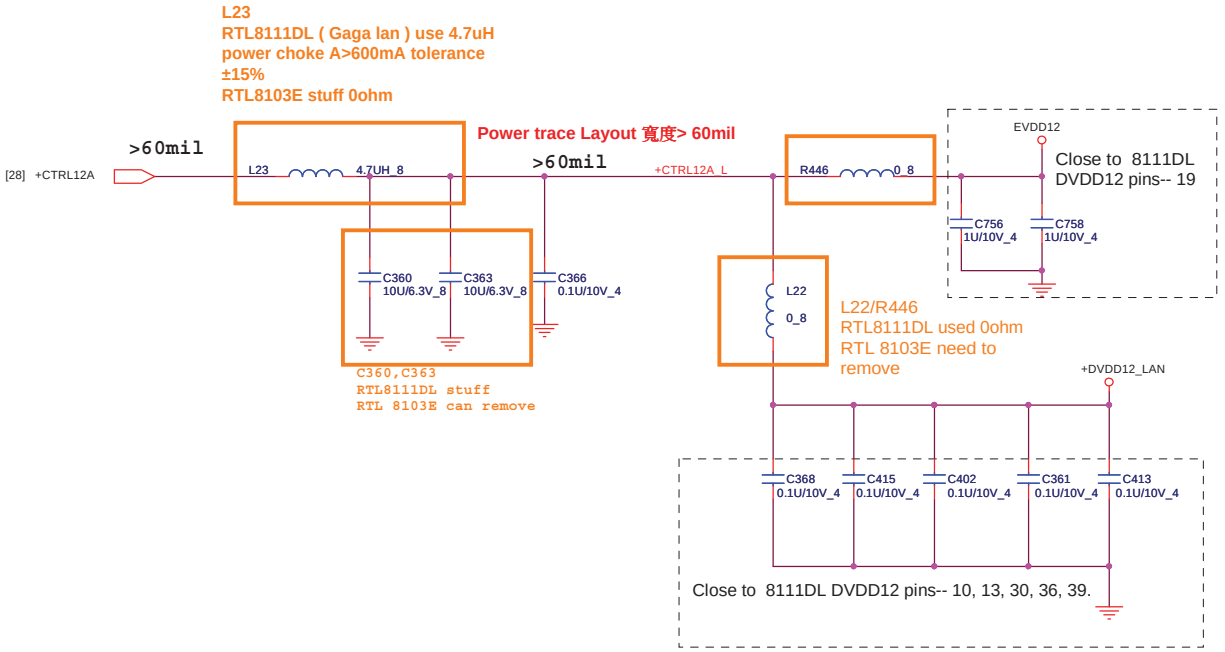
Size	Document Number	Rev
Custom	RTL8111DL/8103EL/RJ45	1A

Date: Tuesday, March 17, 2009 Sheet 28 of 41

T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8102E(10/100)





NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN Power	1A

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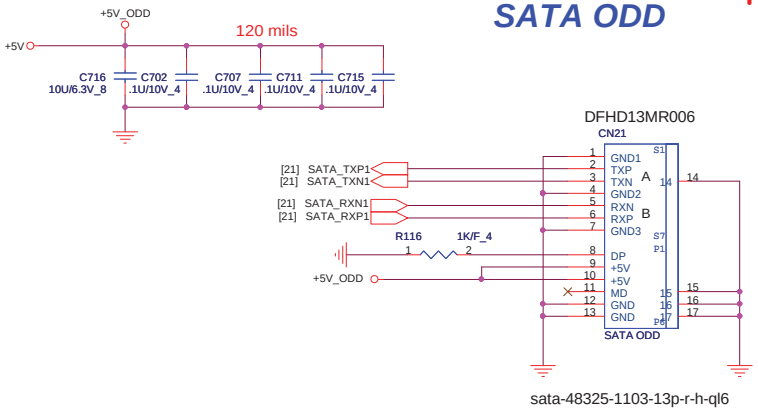
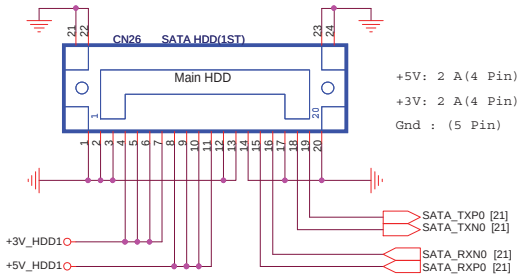
SATA ODD

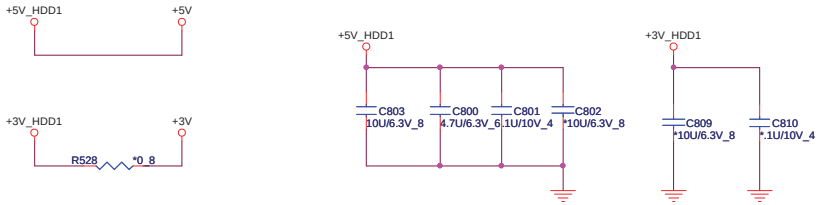


sata-48325-1103-13p-r-h-ql6

SATA_1 CONNECTOR

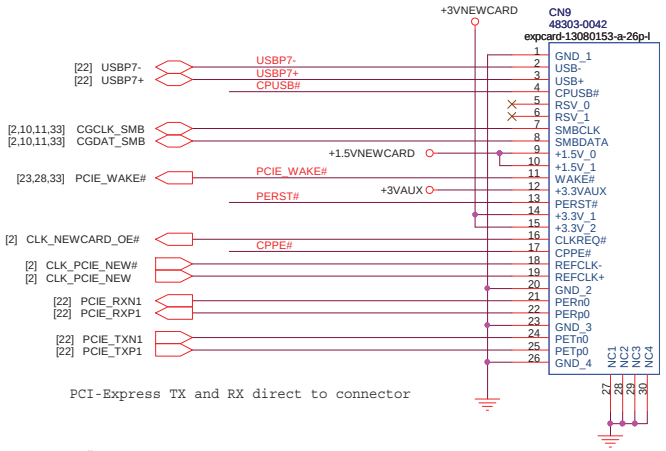
DC Current rating: 0.5 A





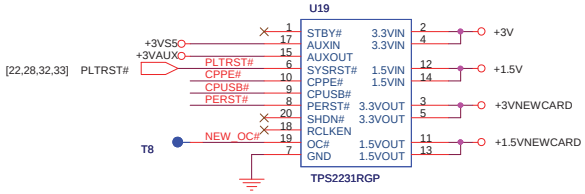
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

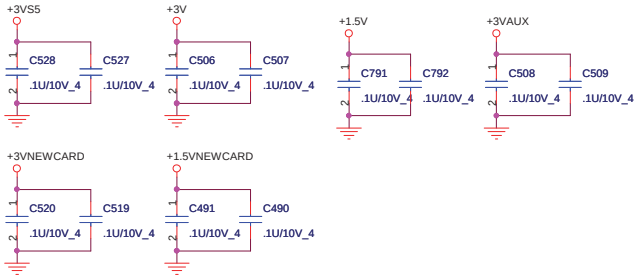


PCI-Express TX and RX direct to connector

Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-l-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



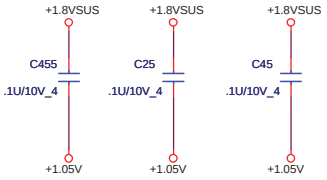
Change net name from 3V_NEWAUX to 3VAUX

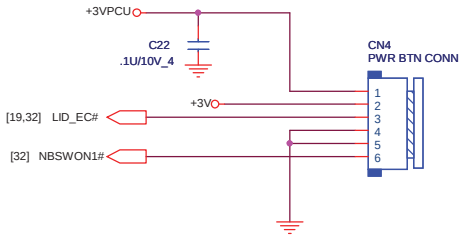


NB5

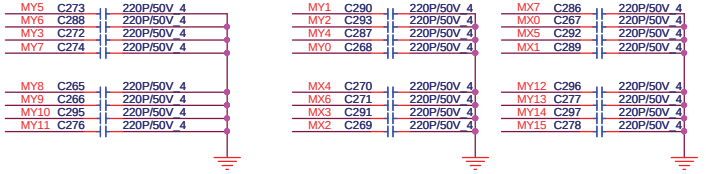
PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD	1A
Date: Tuesday, March 17, 2009	Sheet 30 of 41	

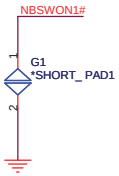




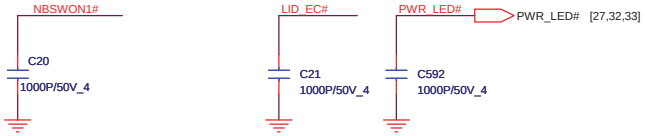
1. +3VPCU(LIDSWITCH PWR)
2. +3V
3. LIDSWITCH
4. GND
5. GND
6. POWERON#
7. NC
8. NC



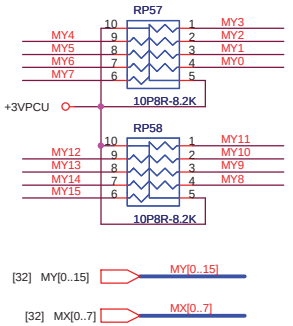
Close to U21 For EMI

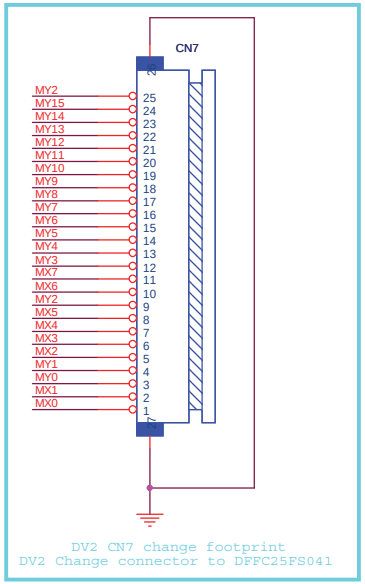


POWER BOTTON CONNECT

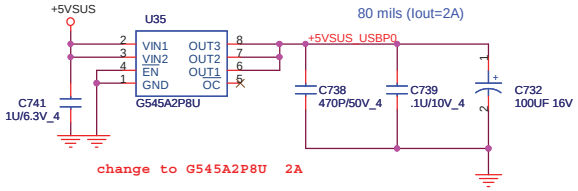


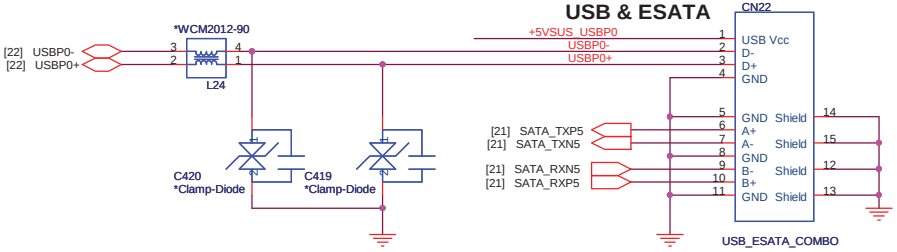
KEYBOARD PULL-UP

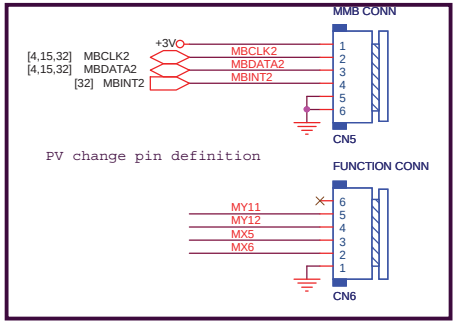




E-SATA/USB COMBO







NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/CAP/POWER CONN	1A

Date: Tuesday, March 17, 2009 | Sheet 31 of 41

TOUCH PAD CONNECTOR

U17

KB3926QF D2

PV Change U17 to 3926D2

For KB3926 B, C version

DV2 Add

DV2 modify footprint to BL121-12R-12P-L-QT6

DFFC12FR293

TOUCH PAD L/R SW1,SW2 in QL5 use, SW3,SW4 in TW9 use

DV2 Add support TW9 Touch-pad SW

close conn

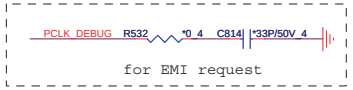
Socket: DG008000031
MXIC: AKE5GFK0Z09

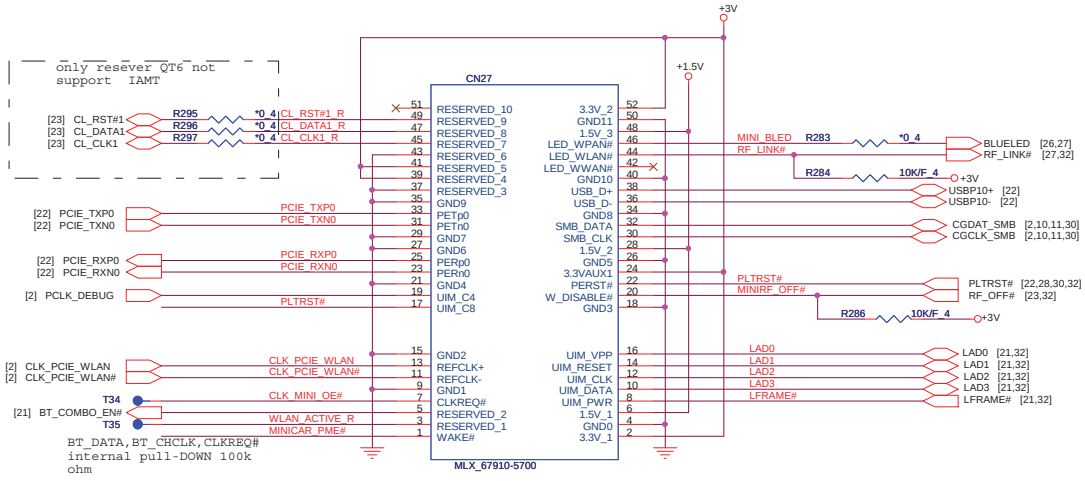
SPI ROM SOCKET
1M byte
SPI
BIOS

High:LG
Low :CB

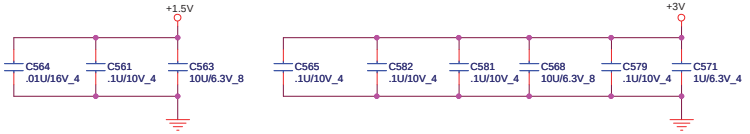
PROJECT : QL5	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: KB3926/ROM/TP; Rev: 1A
Date: Tuesday, March 17, 2009	Sheet 32 of 41

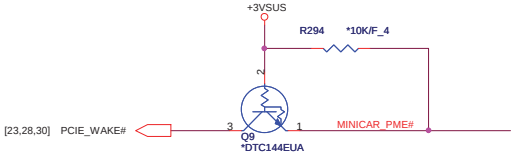
Mini PCI-E Card 1
WLAN



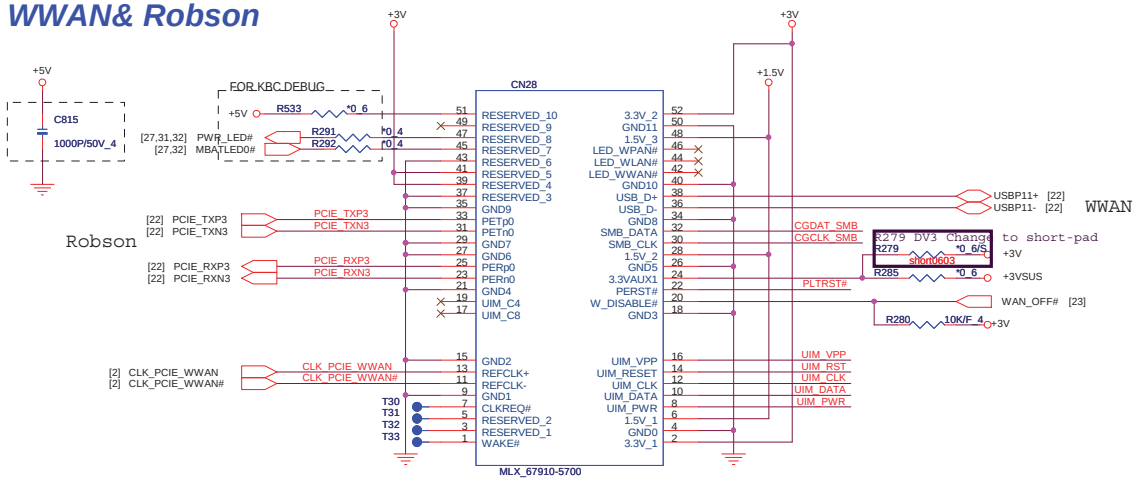


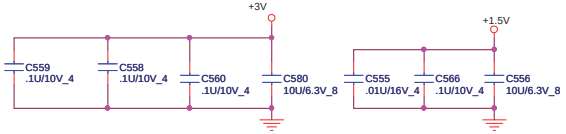
INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm

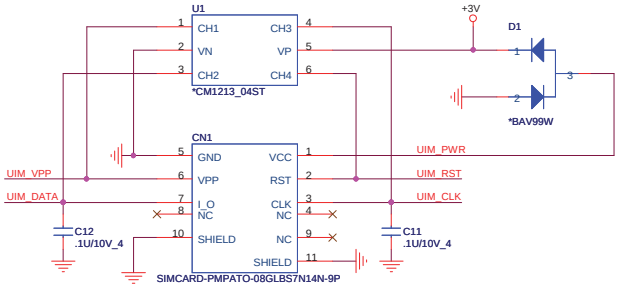




Mini PCI-E Card 2
WWAN& Robson

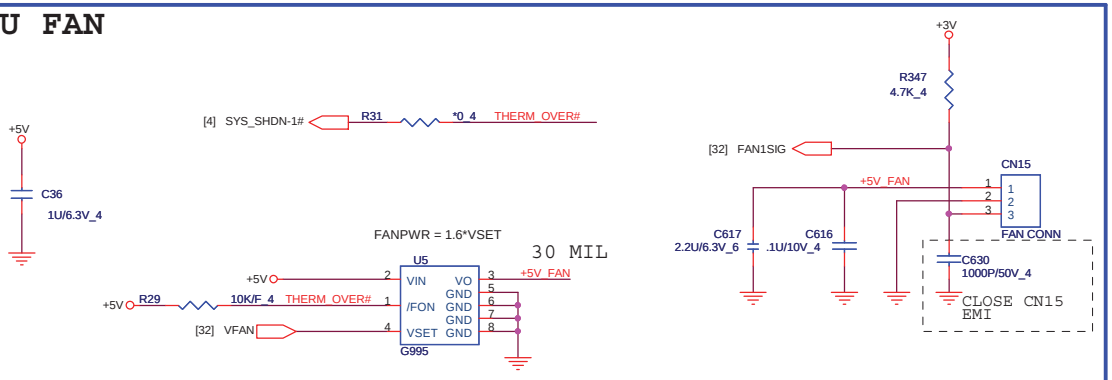






NB5	PROJECT : QL5 Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN X2	Rev: 1A
Date: Tuesday, March 17, 2009	Sheet 33 of 41	

CPU FAN



NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DOCKING/FAN	1A

Date: Tuesday, March 17, 2009 | Sheet 34 of 41

TOP DC_JACK
65W/90W

over lap prevent acoustic nosie

ADP TYPE	PR95 VALUE	P/N
65W	31.6K/F	CS33162FB14
90W	2.61K/F	CS22612FB15

CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

Charging Curret setting =
I chg = 165mV / Rsense * (Vchlim / 3.3V)

Input Current monitor
V icm = 19.9 * (Vcsip - Vcsin)

V ACLIM = VREF *
(Rl // 152K) / (Rhi // 152K + Rlow// 152K)
Input curren = 2.9A (71.5K , 10K)
(0.05/Vref * Vaclim + 0.05) / Rsense

VADJ =
VERF >> 4.2V +5%
Float >> 4.2V
GND >> 4.2 -5%

Setting the Vin min to 12V
For ACSET 1.26V

Setting the Vin min to 17V
For EN = 1.06V

PROJECT : QL5	
Quanta Computer Inc.	
Size: Custom	Document Number: Charger (ISL6251)
Rev: 1A	
Date: Tuesday, March 17, 2009	Sheet 35 of 41

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

over lap prevent acoustic nosie

over lap prevent acoustic nosie

PV Del PR158

5 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 9A

Rds(on) 20m ohm

Rds(on) 20m ohm

EMI request Add

PROJECT : QL5	Quanta Computer Inc.
NB5	Size B / Document Number +5V/+3V (ISL6237) / Rev 1A
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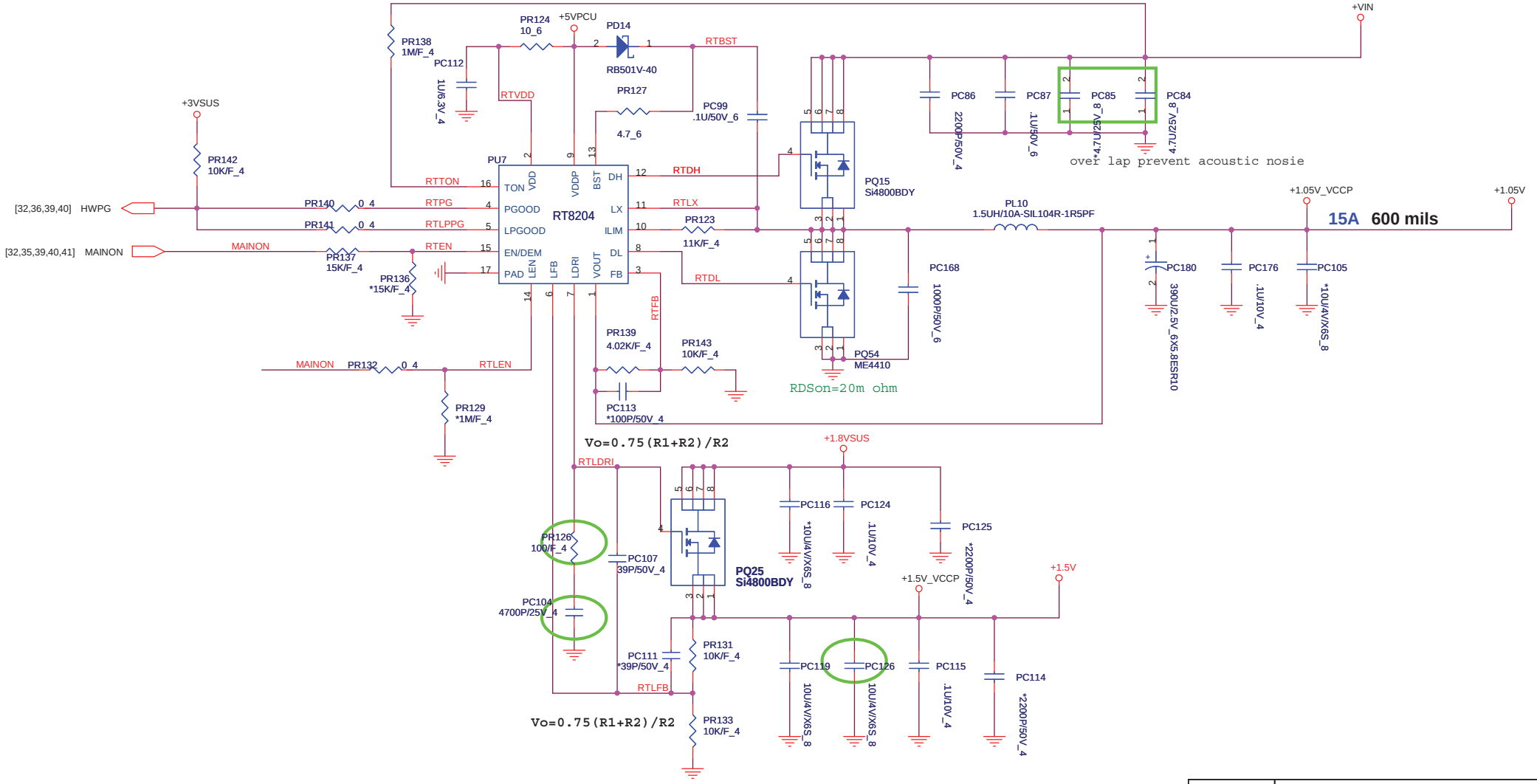
VCCP1.05V & +1.5V

+1.05Volt +/- 5%
Countinue current 6A
Peak current:8A
OCP minimum 12A



NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.05V/+1.5V (RT8204)	1A

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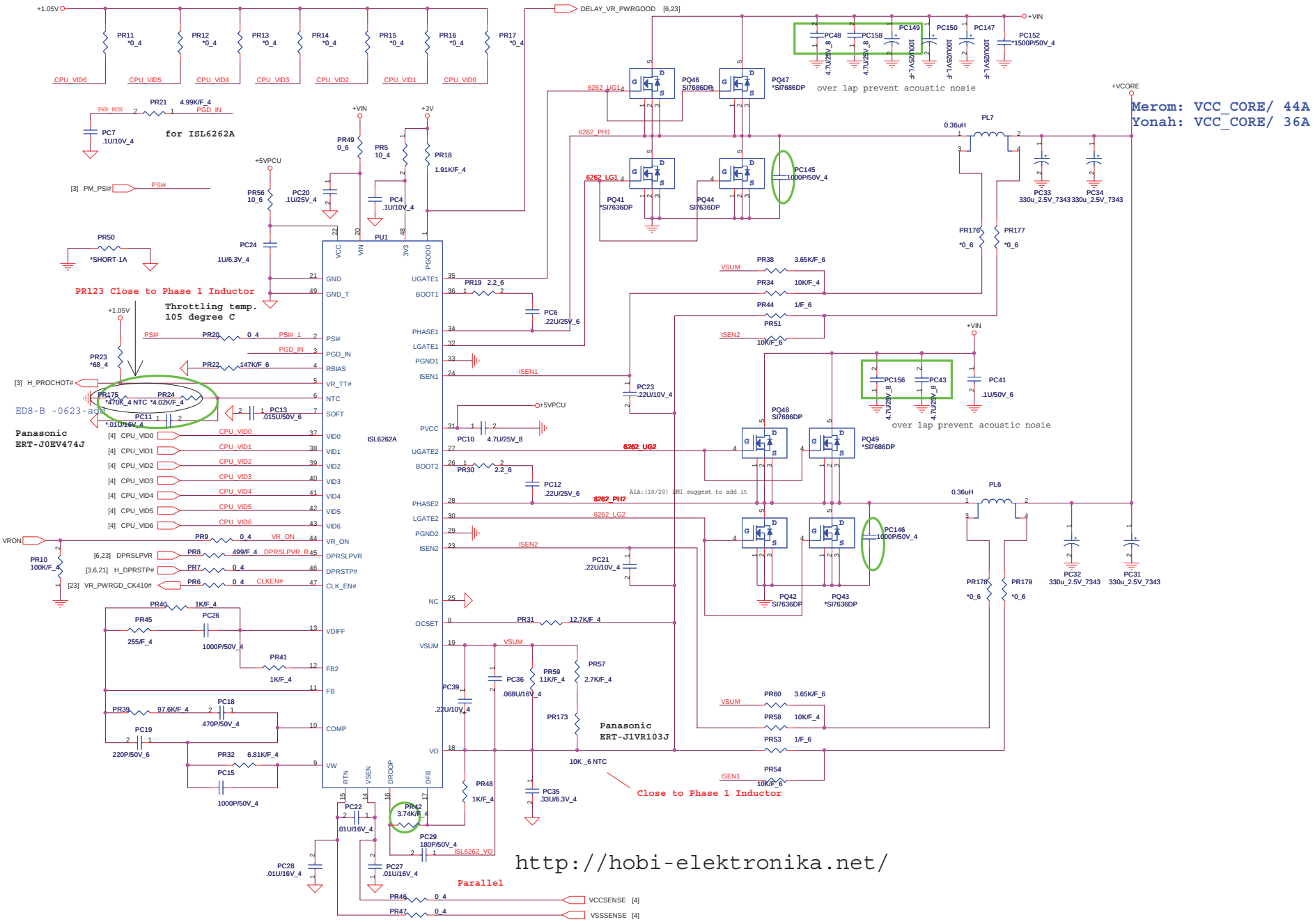

NB5	PROJECT : QL5 Quanta Computer Inc.	
Size: Custom	Document Number: CPU Core (ISL6266A)	Rev: 1A
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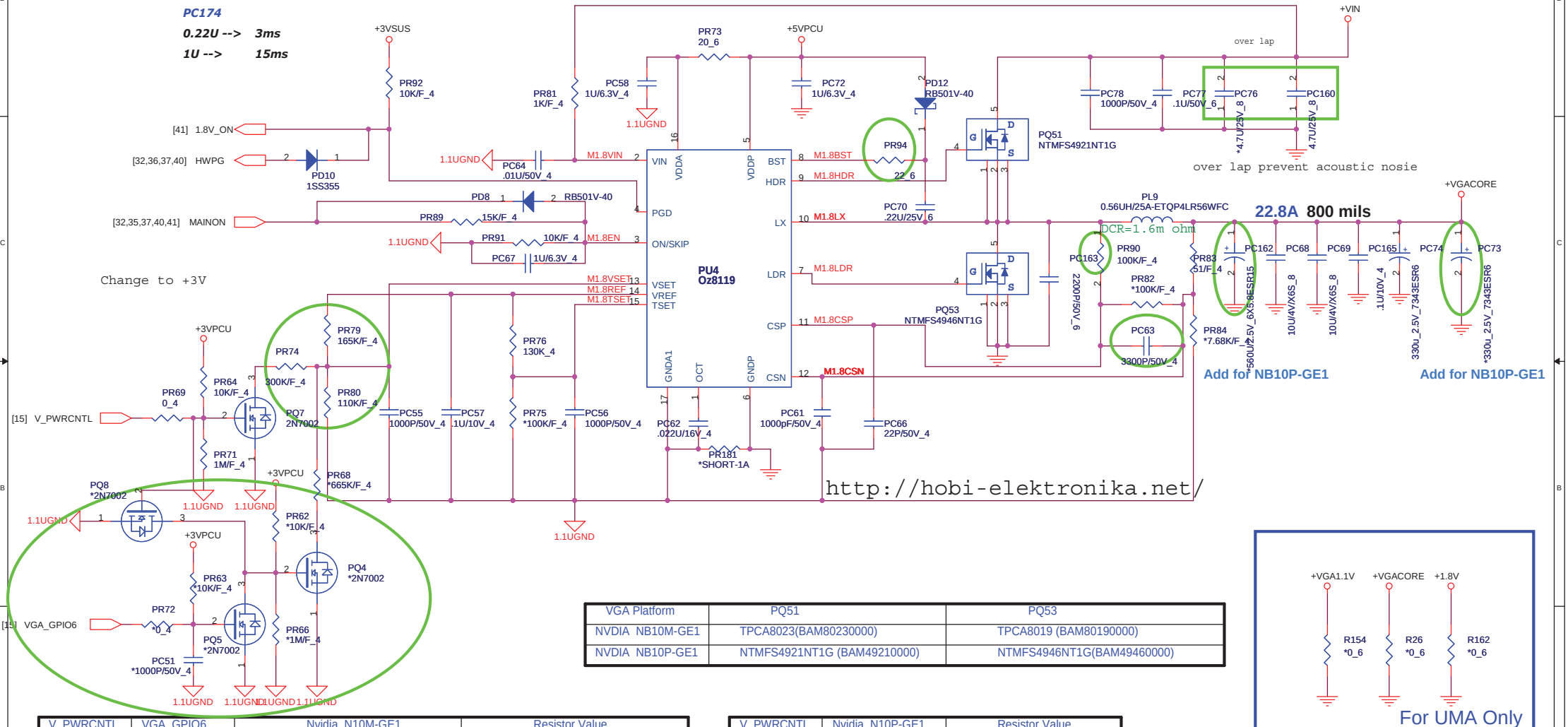
VGA Core & VCC1.1

http://hobi-elektronika.net

+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 25A



VGA Platform	PQ51	PQ53
NVDIA NB10M-GE1	TPCA8023(BAM80230000)	TPCA8019 (BAM80190000)
NVDIA NB10P-GE1	NTMFS4921NT1G (BAM49210000)	NTMFS4946NT1G(BAM49460000)

V_PWRCNTL	VGA_GPIO6	Nvidia N10M-GE1	Resistor Value
LO	LO	1.09V	PR68_665K_CS46652FB00
LO	HI	1.20V	PR79_154K_CS41542FB16
HI	LO	0.90V	PR74_200K_CS42002FB04
HI	HI	0.90V	PR80_120K_CS41202FB17

V_PWRCNTL	Nvidia N10P-GE1	Resistor Value
HI	0.9V	PR80_110K_CS41102FB13
		PR74_300K_CS43002FB15
LO	1.1V	PR79_165K_CS41652FB14

NB5

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B	VGA CORE OZ8118	1A
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(VTT/2A)

1.8 Volt +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum 13.5A

over lap prevent acoustic nosie

(3mA)

RDSon=8.5m ohm

For Discrete Only

1.1 Volt +/- 5%
Countinue current:2A
Peak current:3A

(2.24A)

for G73&G8X VGA
PLL power

VO=(0.8(R1+R2)/R2)
R2<120Kohm

NB5	PROJECT : QL5 Quanta Computer Inc.	
Size: Custom	Document Number: 1.8V/DDR_VTER/+1.8v/+1.1V	Rev: 1A
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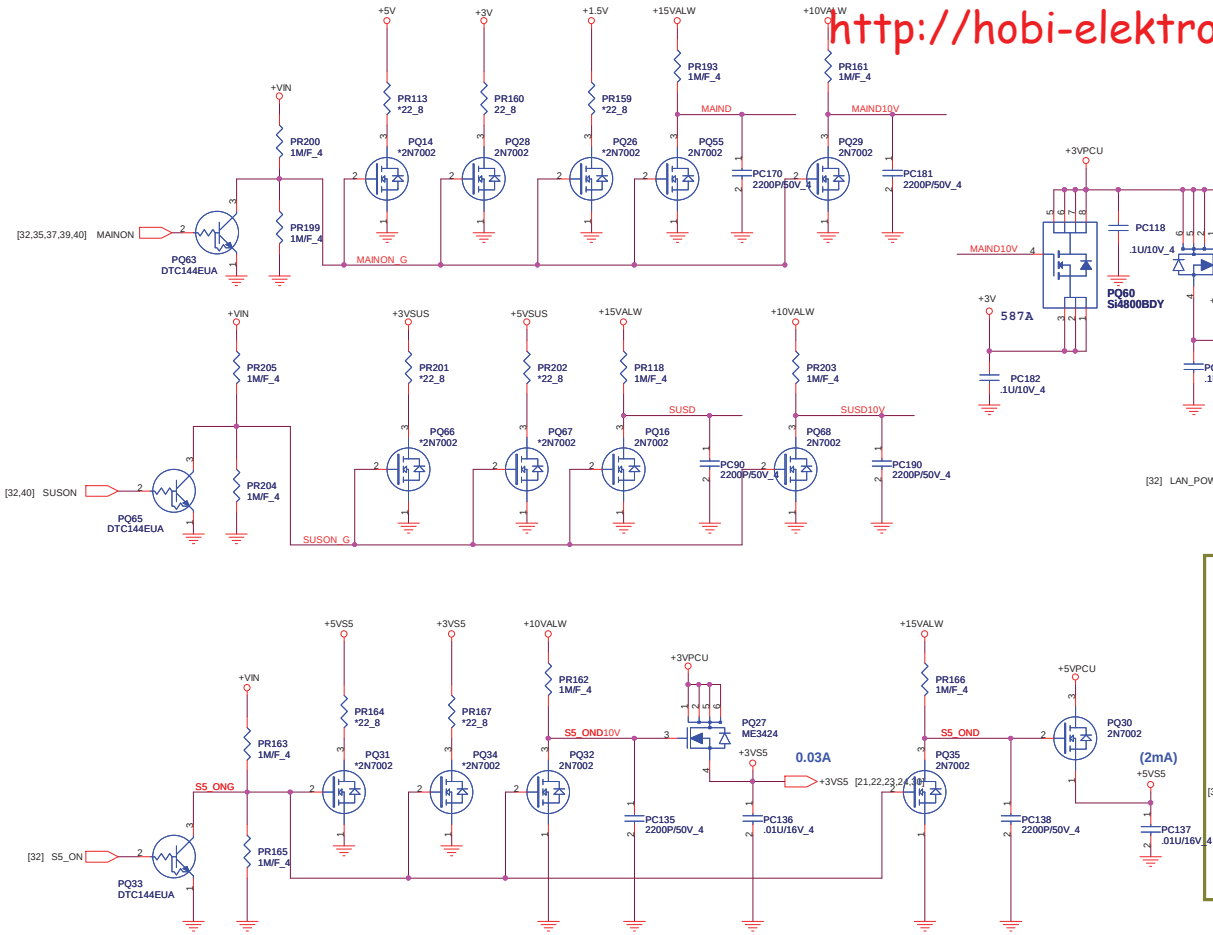
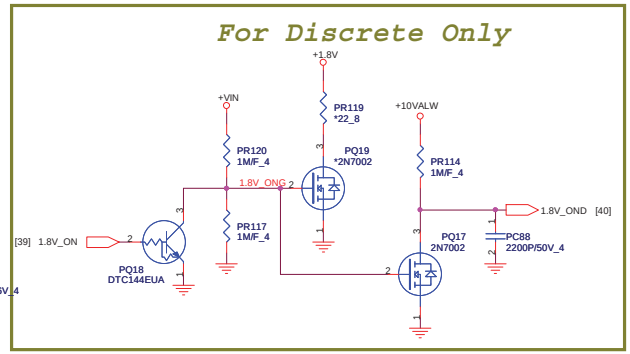


For Discrete Only



		AC MODE				DC MODE			
	Voltage level	S0	S3	S4	S5	S0	S3	S4	S5
+3VPCU	3.3V +/- 5%	V	V	V	V	V	V	V	V
+5VPCU	5V +/- 5%	V	V	V	V	V	V	V	V
+3VRTC	3.3V +/- 5%	V	V	V	V	V	V	V	V
+3VS5	3.3V +/- 5%	V	V	V	V	V	V		
+5VS5	5V +/- 5%	V	V	V	V	V	V		
+3VSUS	3.3V +/- 5%	V	V			V	V		
+5VSUS	5V +/- 5%	V	V			V	V		
+1.8VSUS	1.8V +/- 5%	V	V			V	V		
+0.9VSMVTT	0.9V +/- 5%	V	V			V	V		
+1.5V	1.5V +/- 5%	V				V			
+1.05V	1.05V +/- 5%	V				V			
+VCORE	0.9~1.15V	V				V			
+VGA_CORE	0.9~1.2V	V				V			
+VGA1.1V	1.1V +/- 5%	V				V			
+1.8V	1.8V +/- 5%	V				V			
+3VLANVCC	3.3V +/- 5%	V				V			

NB5

PROJECT : QL5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	1A

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