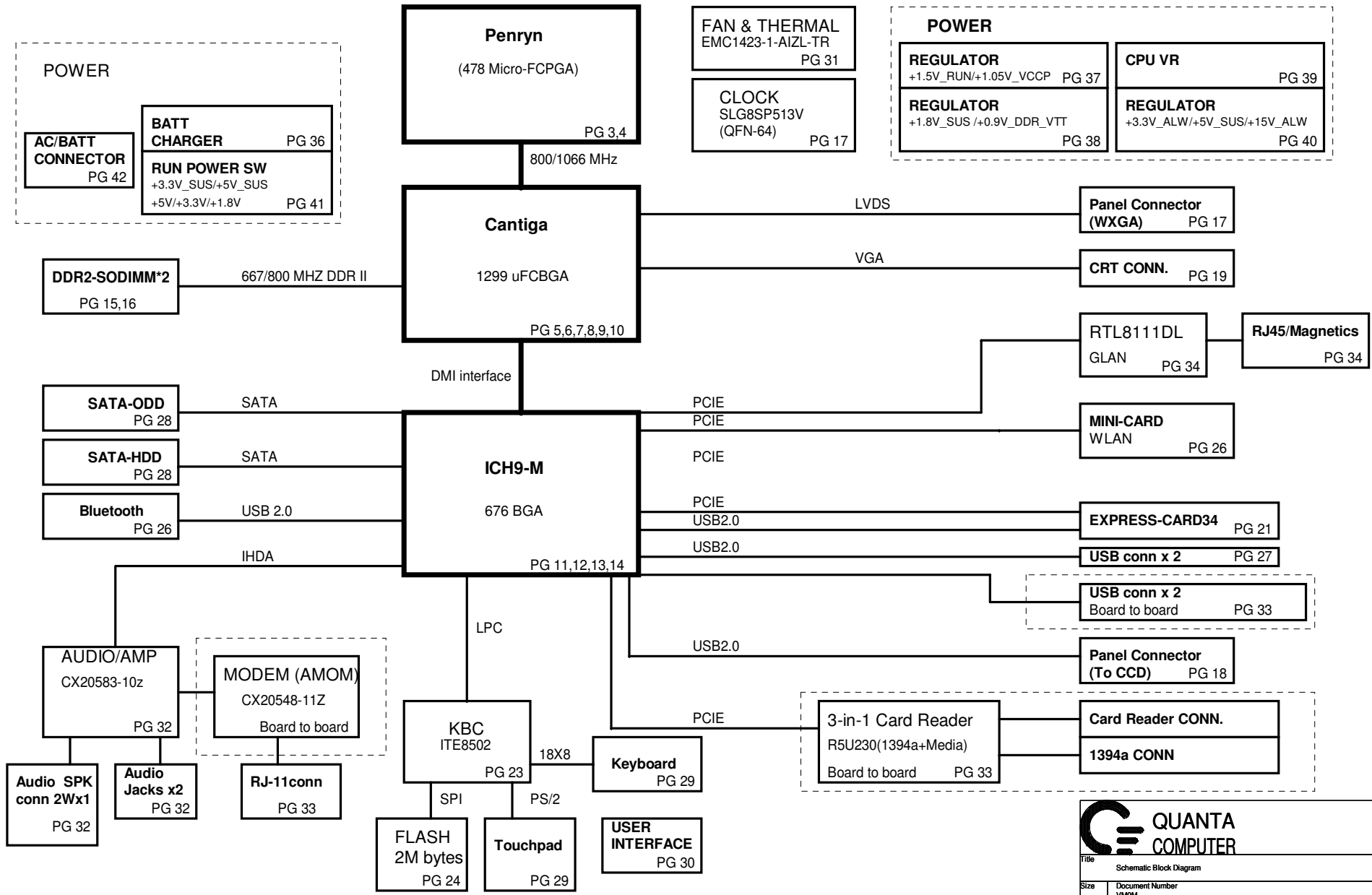


VM9M Block Diagram Intel UMA

VER : F3B




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Size: VM9M	Document Number: VM9M	Rev: 1A
Date: Monday, June 08, 2009	Sheet: 1	of 46

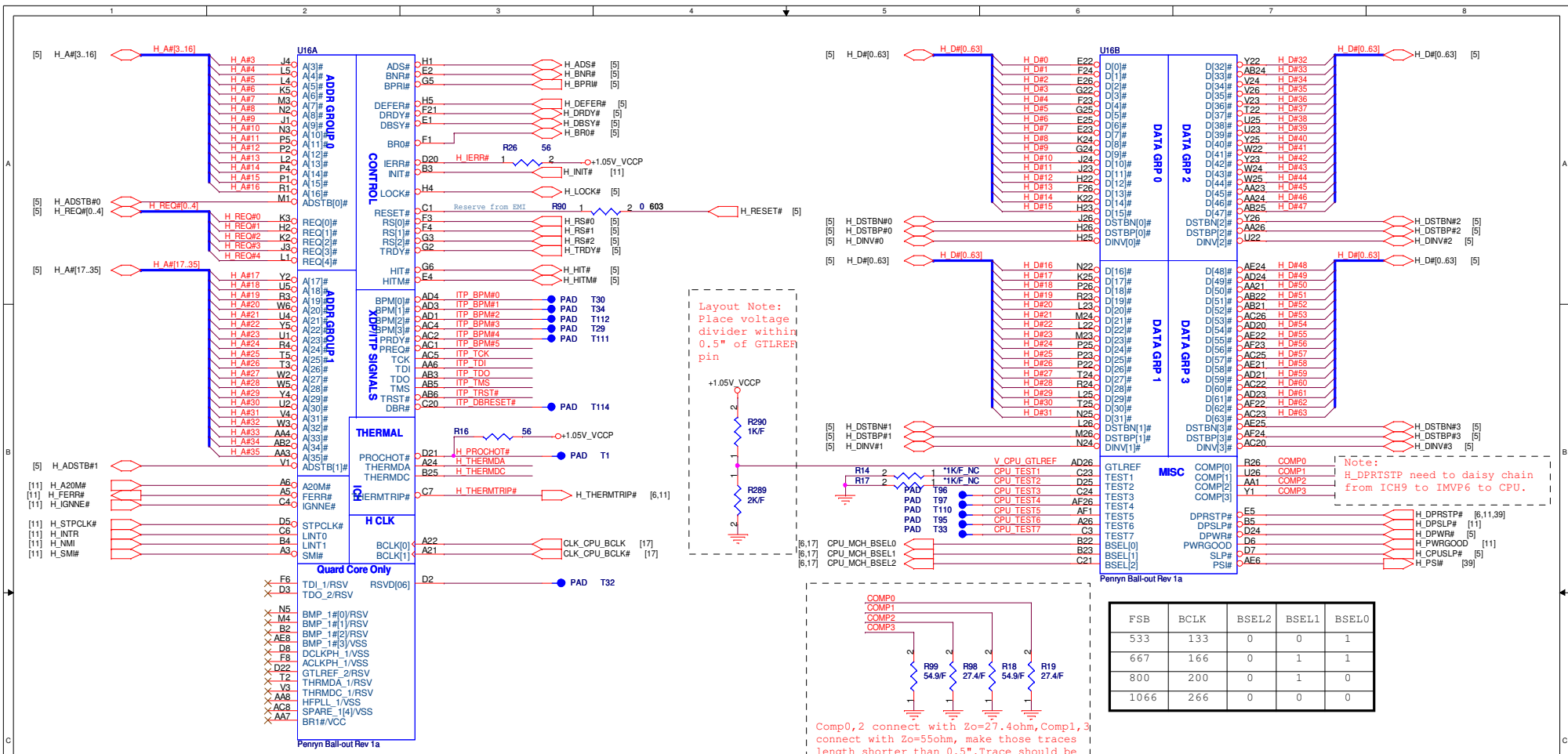
Table of Contents

PAGE	DESCRIPTION
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2	Front Page
3-4	Penryn
5-10	Cantiga
11-14	ICH9M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18	LCD Conn.
19	CRT Conn
21	Express card
23	SIO (ITE8512)
24	FLASH/RTC
25	BLANK PAGE
26	Mini Card / BT
27	USB
28	SATA Conn
29	TP / KEYBOARD
30	SWITCH /LED
31	FAN & Thermal
32	Audio CODEC/Phone Jack
33	Board To Board
34	LAN / TRANSFORM
35	BLANK PAGE
36	Battery Selector & Charger
37	1.05VCCP / 1.5VRUJN
38	DDR2_1.8VSUS, 0.9V
39	CPU_MAX17410(2phase)
40	MAX17020 (+5.5V,+3,3V)
41	RUN Power Switch
42	DCIN,Batt
43	PAD& SCREW
44	EMI CAP
45	SMBUS BLOCK
46	Power Block Dianram

Power States

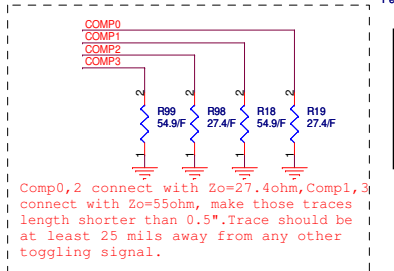
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,18,24,36,37,3,8,39,40,44	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,23,24	RTC		S0~S5
+3.3V_ALW	+3.3V	3,23,24,30,35,36,38,40,41,42,45	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,38,40,41,42	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	11,18,40,41	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	34	LAN POWER		
+5V_SUS	+5V	14,27,30,39,40,41,44	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,18,25,30,37,39,41,45	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,37,38,41	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,38,41	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,19,21,25,28,29,30,31,32,41,44	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,12,13,14,15,17,30,31,32,34,18,19,20,21,23,25,26,28,41,44,45	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,26,37,41,44	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,6,8,9,11,14,37,44	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,39	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	18	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	28	Module Power		
+5V_HDD	+5V	28	HDD Power		
+PBATT	+10V~+17V	42	MAIN BATTERY	CHG_PBATT	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



Layout Note:
Place voltage divider within 0.5" of GTLREF pin

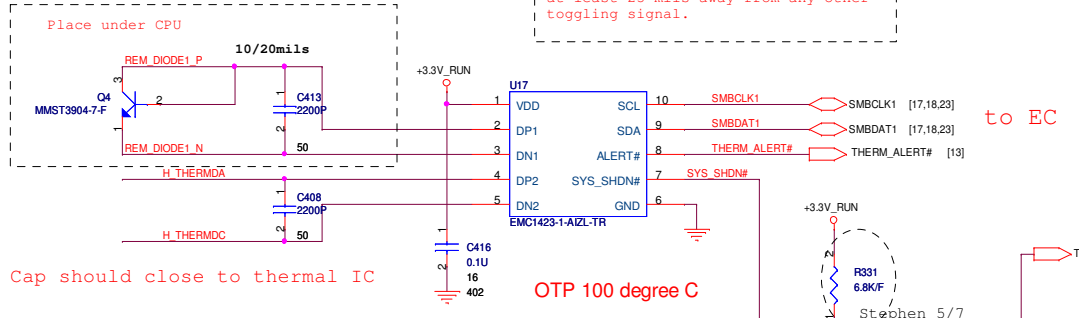
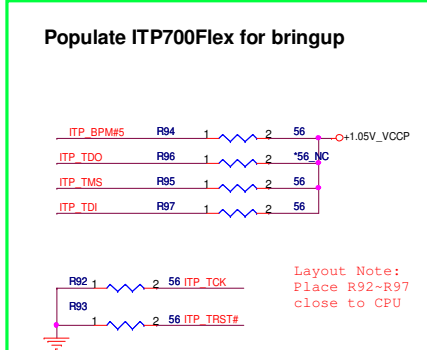
Note:
H_DPRTSTP need to daisy chain from ICH9 to INV6 to CPU.



Penryn Ball-out Rev 1a

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

Comp0,2 connect with Zo=27.4ohm, Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.



QUANTA COMPUTER

Title: Penryn Processor (HOST BUS)

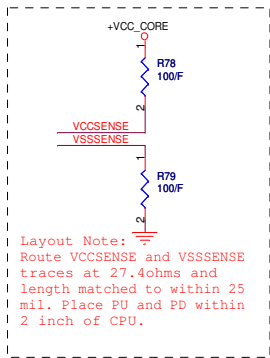
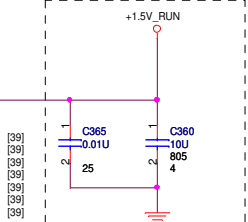
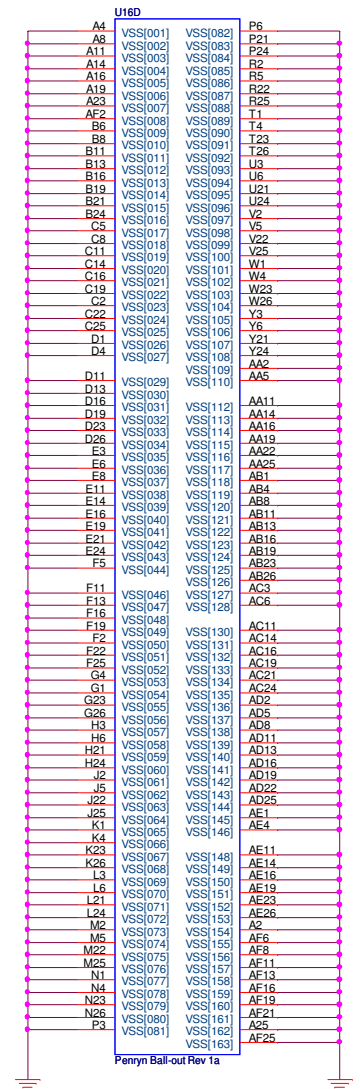
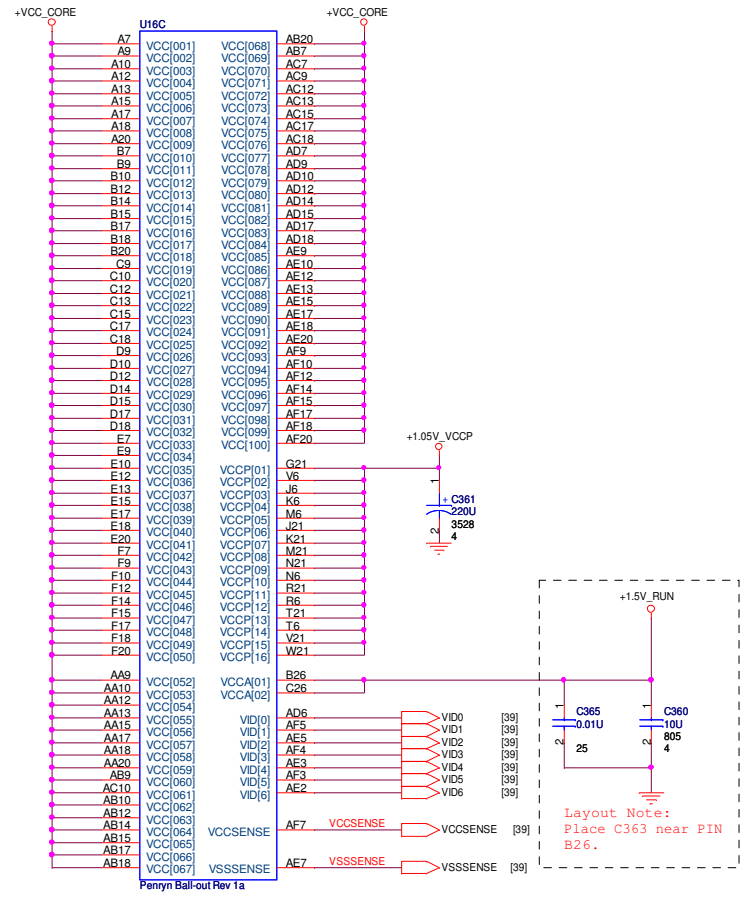
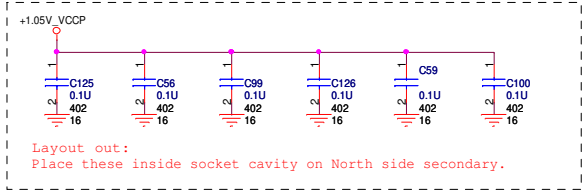
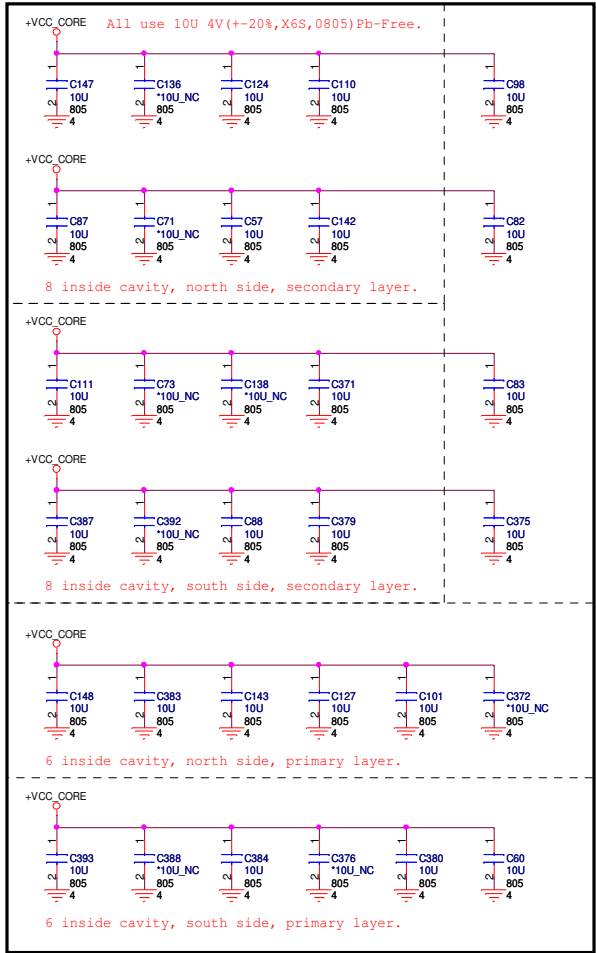
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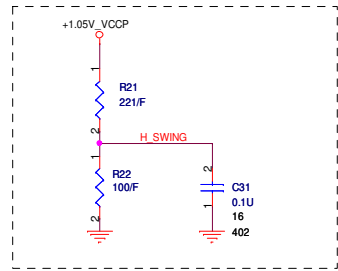
Document Number: VMSM

Rev: 1A

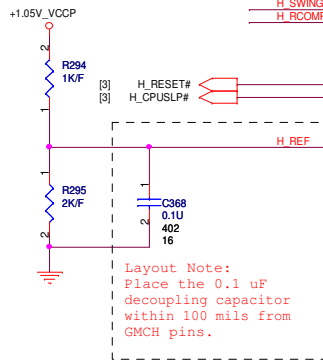
Date: Saturday, June 06, 2009

Sheet: 3 of 46

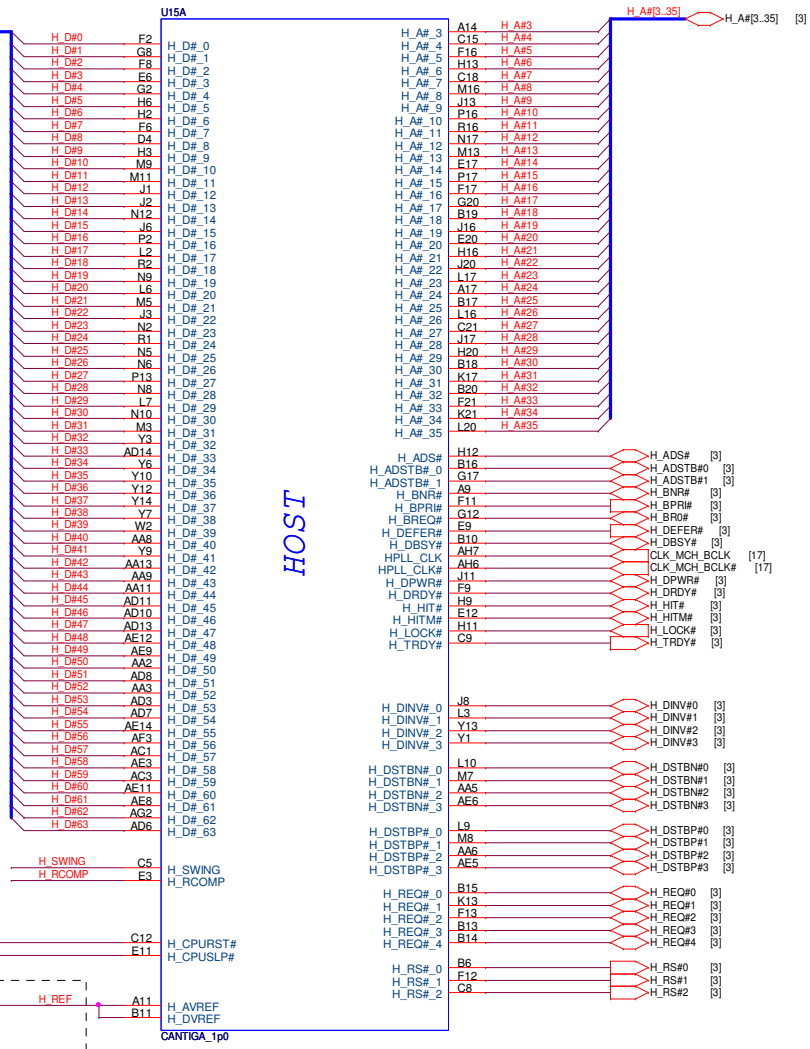




Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.



Layout Note:
Place the 0.1 uF
decoupling capacitor
within 100 mils from
GMCH pins.



HOST

For EA test use

- ET10 1 H_DSTBP#0
- ET12 1 H_D#12
- ET14 1 H_DSTB#1
- ET8 1 H_DSTBP#1
- ET13 1 H_D#29
- ET3 1 H_D#21
- ET18 1 H_D#32



Title Cantiga (HOST)		
Size	Document Number VMSM	Rev 1A
Date:	Wednesday, June 03, 2009	Sheet 5 of 46

[15] DDR_A_D0[0..63]

DDR A D0	AJ38	SA DO_0
DDR A D1	AJ41	SA DO_1
DDR A D2	AN38	SA DO_2
DDR A D3	AM38	SA DO_3
DDR A D4	AJ36	SA DO_4
DDR A D5	AJ46	SA DO_5
DDR A D6	AM44	SA DO_6
DDR A D7	AM42	SA DO_7
DDR A D8	AN43	SA DO_8
DDR A D9	AN44	SA DO_9
DDR A D10	AU40	SA DO_10
DDR A D11	AT38	SA DO_11
DDR A D12	AN41	SA DO_12
DDR A D13	AN39	SA DO_13
DDR A D14	AU44	SA DO_14
DDR A D15	AU42	SA DO_15
DDR A D16	AV39	SA DO_16
DDR A D17	AY44	SA DO_17
DDR A D18	BA40	SA DO_18
DDR A D19	BD43	SA DO_19
DDR A D20	AV41	SA DO_20
DDR A D21	AY43	SA DO_21
DDR A D22	BA41	SA DO_22
DDR A D23	BC40	SA DO_23
DDR A D24	AY37	SA DO_24
DDR A D25	BD38	SA DO_25
DDR A D26	AV37	SA DO_26
DDR A D27	AT36	SA DO_27
DDR A D28	AY39	SA DO_28
DDR A D29	BB38	SA DO_29
DDR A D30	AV36	SA DO_30
DDR A D31	AW36	SA DO_31
DDR A D32	BD13	SA DO_32
DDR A D33	AU11	SA DO_33
DDR A D34	BC11	SA DO_34
DDR A D35	BA12	SA DO_35
DDR A D36	AU13	SA DO_36
DDR A D37	AV13	SA DO_37
DDR A D38	BD12	SA DO_38
DDR A D39	BC12	SA DO_39
DDR A D40	BB9	SA DO_40
DDR A D41	BA9	SA DO_41
DDR A D42	AU10	SA DO_42
DDR A D43	AV9	SA DO_43
DDR A D44	BA11	SA DO_44
DDR A D45	BD9	SA DO_45
DDR A D46	AV8	SA DO_46
DDR A D47	BA6	SA DO_47
DDR A D48	AV5	SA DO_48
DDR A D49	AV7	SA DO_49
DDR A D50	AT9	SA DO_50
DDR A D51	AN8	SA DO_51
DDR A D52	AU5	SA DO_52
DDR A D53	AU6	SA DO_53
DDR A D54	AT5	SA DO_54
DDR A D55	AN10	SA DO_55
DDR A D56	AM11	SA DO_56
DDR A D57	AM5	SA DO_57
DDR A D58	AJ9	SA DO_58
DDR A D59	AJ8	SA DO_59
DDR A D60	AN12	SA DO_60
DDR A D61	AM13	SA DO_61
DDR A D62	AJ11	SA DO_62
DDR A D63	AJ12	SA DO_63

U150

DDR SYSTEM MEMORY A

B21	DDR A BS0	DDR A BS0	[15,16]
BG18	DDR A BS1	DDR A BS1	[15,16]
AT25	DDR A BS2	DDR A BS2	[15,16]
BR20	DDR A RAS#	DDR A_RAS#	[15,16]
BD20	DDR A CAS#	DDR A_CAS#	[15,16]
AY20	DDR A WE#	DDR A_WE#	[15,16]
AM37	DDR A DM0	DDR_A_DM[0..7]	[15]
AT41	DDR A DM1		
AY41	DDR A DM2		
AU39	DDR A DM3		
BR12	DDR A DM4		
AY6	DDR A DM5		
AT7	DDR A DM6		
AJ5	DDR A DM7		
AJ44	DDR A DQS0	DDR_A_DQS[0..7]	[15]
AT44	DDR A DQS1		
BA43	DDR A DQS2		
BC37	DDR A DQS3		
AW12	DDR A DQS4		
BC8	DDR A DQS5		
AU8	DDR A DQS6		
AM7	DDR A DQS7		
AJ43	DDR A DQS#0	DDR_A_DQS#[0..7]	[15]
AT43	DDR A DQS#1		
BA44	DDR A DQS#2		
BD37	DDR A DQS#3		
AY12	DDR A DQS#4		
BR8	DDR A DQS#5		
AU9	DDR A DQS#6		
AM8	DDR A DQS#7		
BA21	DDR A MA0	DDR_A_MA[0..14]	[15,16]
BC24	DDR A MA1		
BG24	DDR A MA2		
BH24	DDR A MA3		
BG25	DDR A MA4		
BA24	DDR A MA5		
BD24	DDR A MA6		
BG27	DDR A MA7		
BF25	DDR A MA8		
AN24	DDR A MA9		
BC21	DDR A MA10		
BG26	DDR A MA11		
BH26	DDR A MA12		
BH17	DDR A MA13		
AY25	DDR A MA14		

[15] DDR_B_D0[0..63]

DDR B D0	AK47	SB DO_0
DDR B D1	AH46	SB DO_1
DDR B D2	AP47	SB DO_2
DDR B D3	AP46	SB DO_3
DDR B D4	AP47	SB DO_4
DDR B D5	AJ48	SB DO_5
DDR B D6	AM48	SB DO_6
DDR B D7	AP48	SB DO_7
DDR B D8	AU47	SB DO_8
DDR B D9	AJ46	SB DO_9
DDR B D10	BA48	SB DO_10
DDR B D11	AY48	SB DO_11
DDR B D12	AT47	SB DO_12
DDR B D13	AP47	SB DO_13
DDR B D14	BA47	SB DO_14
DDR B D15	BC47	SB DO_15
DDR B D16	BC46	SB DO_16
DDR B D17	BC44	SB DO_17
DDR B D18	BC43	SB DO_18
DDR B D19	BF43	SB DO_19
DDR B D20	BE45	SB DO_20
DDR B D21	BC41	SB DO_21
DDR B D22	BF40	SB DO_22
DDR B D23	BF41	SB DO_23
DDR B D24	BG38	SB DO_24
DDR B D25	BF38	SB DO_25
DDR B D26	BH35	SB DO_26
DDR B D27	BG35	SB DO_27
DDR B D28	BH40	SB DO_28
DDR B D29	BG39	SB DO_29
DDR B D30	BG34	SB DO_30
DDR B D31	BH34	SB DO_31
DDR B D32	BH14	SB DO_32
DDR B D33	BG12	SB DO_33
DDR B D34	BH11	SB DO_34
DDR B D35	BG8	SB DO_35
DDR B D36	BH12	SB DO_36
DDR B D37	BF11	SB DO_37
DDR B D38	BF8	SB DO_38
DDR B D39	BG7	SB DO_39
DDR B D40	BC5	SB DO_40
DDR B D41	BC6	SB DO_41
DDR B D42	AV3	SB DO_42
DDR B D43	AY1	SB DO_43
DDR B D44	BF6	SB DO_44
DDR B D45	BF5	SB DO_45
DDR B D46	BA1	SB DO_46
DDR B D47	BD3	SB DO_47
DDR B D48	AV2	SB DO_48
DDR B D49	AJ3	SB DO_49
DDR B D50	AR3	SB DO_50
DDR B D51	AV2	SB DO_51
DDR B D52	AY2	SB DO_52
DDR B D53	AV1	SB DO_53
DDR B D54	AP3	SB DO_54
DDR B D55	AL1	SB DO_55
DDR B D56	AL1	SB DO_56
DDR B D57	AL2	SB DO_57
DDR B D58	AJ1	SB DO_58
DDR B D59	AH1	SB DO_59
DDR B D60	AM2	SB DO_60
DDR B D61	AM3	SB DO_61
DDR B D62	AJ3	SB DO_62
DDR B D63	AJ3	SB DO_63

U15E

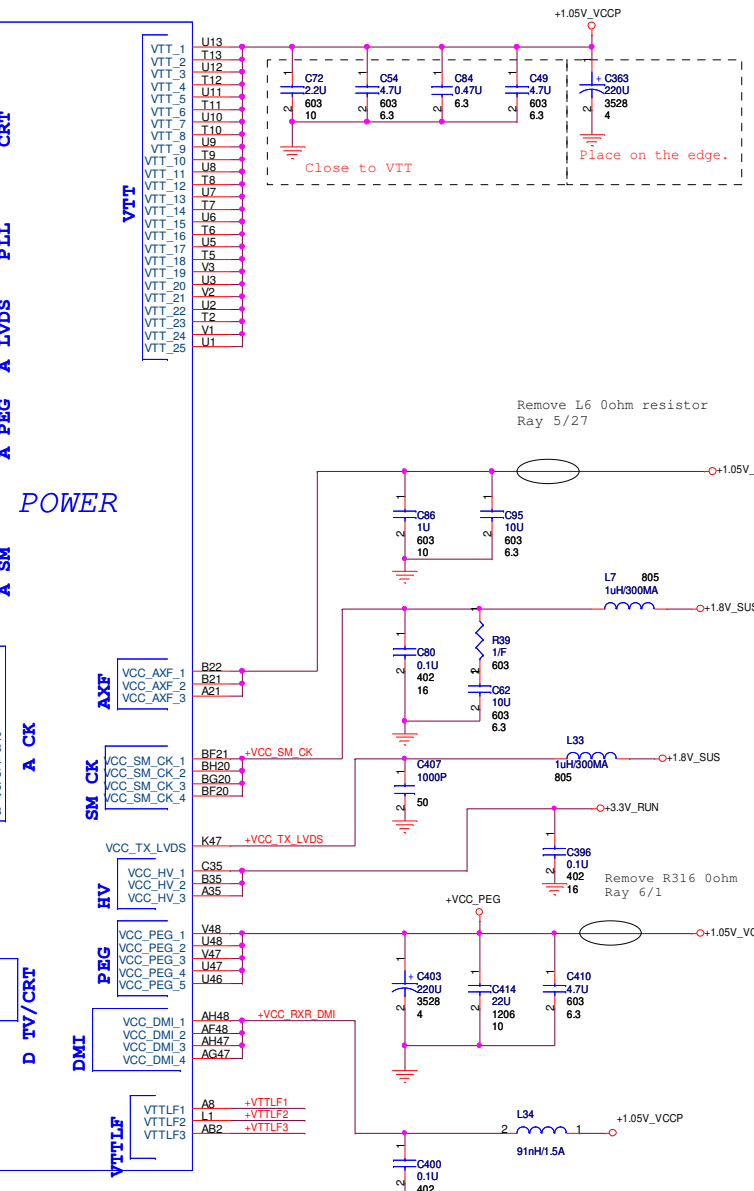
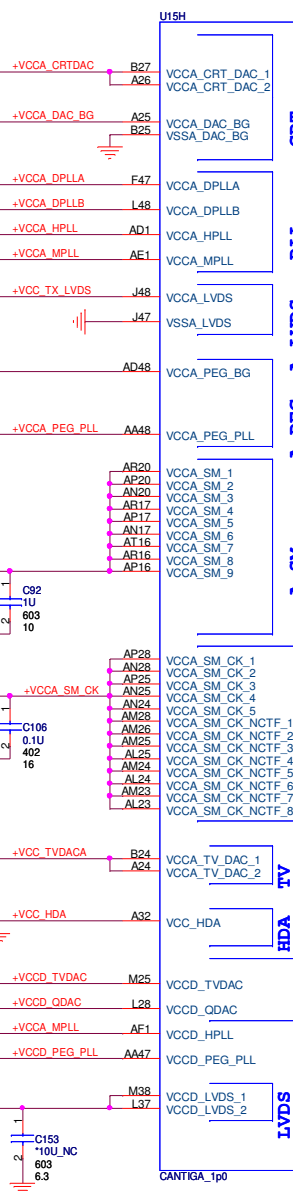
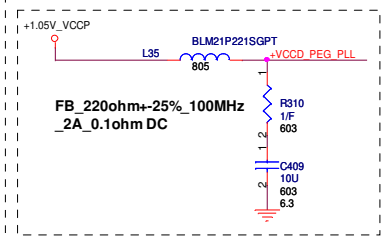
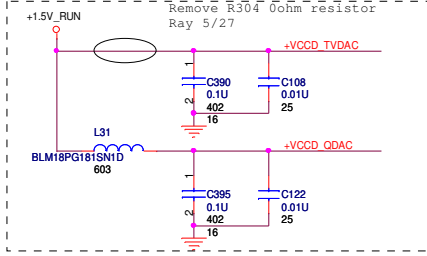
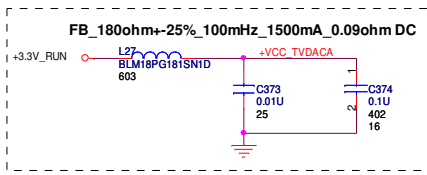
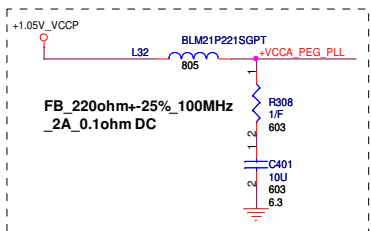
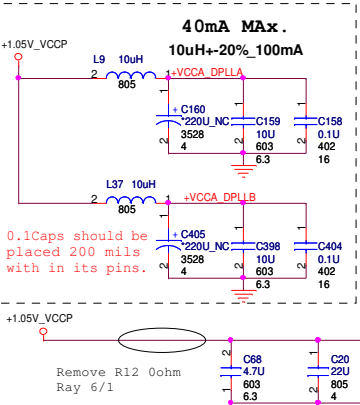
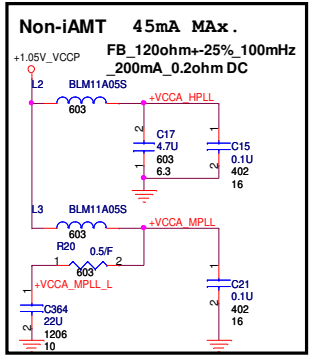
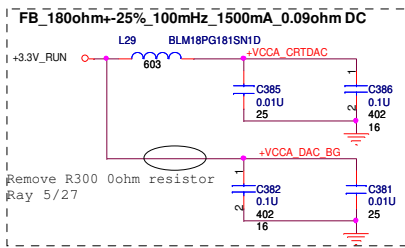
DDR SYSTEM MEMORY B

BC16	DDR B BS0	DDR B BS0	[15,16]
BB17	DDR B BS1	DDR B BS1	[15,16]
BB33	DDR B BS2	DDR B BS2	[15,16]
AU17	DDR B RAS#	DDR B_RAS#	[15,16]
BG16	DDR B CAS#	DDR B_CAS#	[15,16]
BF14	DDR B WE#	DDR B_WE#	[15,16]
AM47	DDR B DM0	DDR_B_DM[0..7]	[15]
AY47	DDR B DM1		
BD40	DDR B DM2		
BF35	DDR B DM3		
BG11	DDR B DM4		
BA3	DDR B DM5		
AP1	DDR B DM6		
AK2	DDR B DM7		
AL47	DDR B DQS0	DDR_B_DQS[0..7]	[15]
AV48	DDR B DQS1		
BC41	DDR B DQS2		
BG37	DDR B DQS3		
BH9	DDR B DQS4		
BB2	DDR B DQS5		
AU1	DDR B DQS6		
AN6	DDR B DQS7		
AL46	DDR B DQS#0	DDR_B_DQS#[0..7]	[15]
AV47	DDR B DQS#1		
BH41	DDR B DQS#2		
BH37	DDR B DQS#3		
BG9	DDR B DQS#4		
BC2	DDR B DQS#5		
AT2	DDR B DQS#6		
AN5	DDR B DQS#7		
AV17	DDR B MA0	DDR_B_MA[0..14]	[15,16]
BA25	DDR B MA1		
BC25	DDR B MA2		
AU25	DDR B MA3		
AV25	DDR B MA4		
BB28	DDR B MA5		
AU28	DDR B MA6		
AT33	DDR B MA8		
BD33	DDR B MA9		
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AW33	DDR B MA11		
AY33	DDR B MA12		
BH15	DDR B MA13		
AJ33	DDR B MA14		

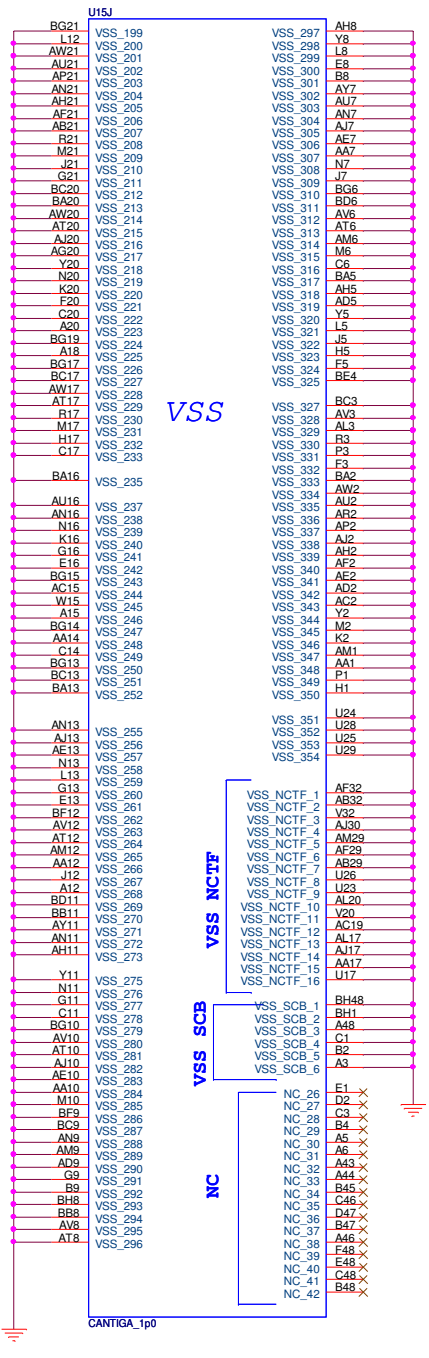
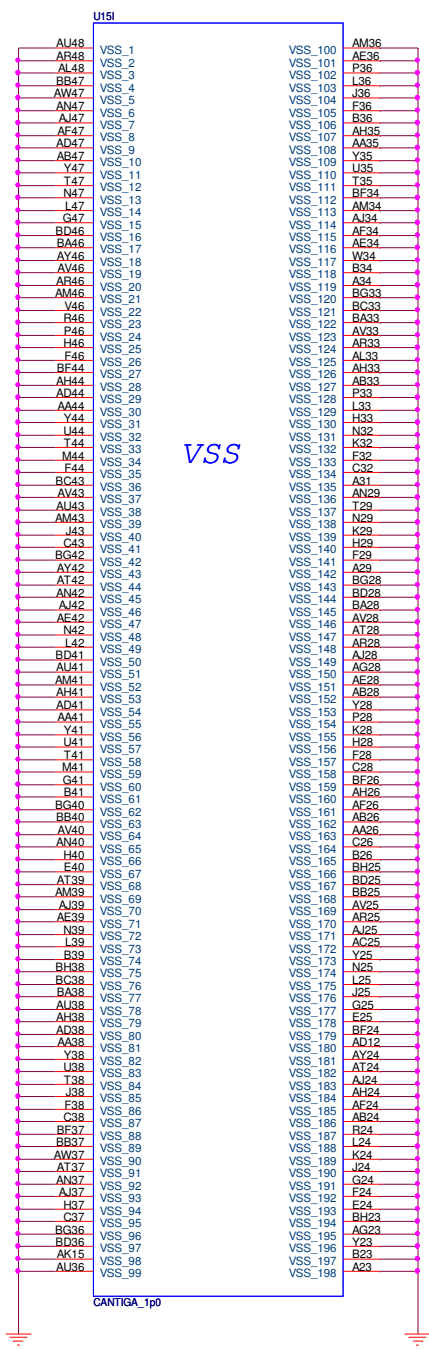
CANTIGA_Tp0



Title		
Cantiga (DDR2)		
Size	Document Number	Rev
	VMSM	1A
Date:	Saturday, June 06, 2009	Sheet 7 of 46



Title: Cantiga (POWER)		
Size: VMSM	Document Number:	Rev: 1A
Date: Saturday, June 06, 2009	Sheet: 9	of 46

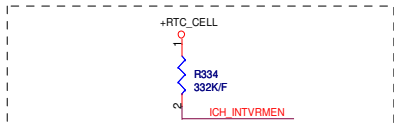
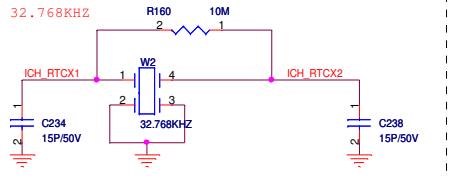


QUANTA
COMPUTER

Title: Cantiga (VSS)

Size	Document Number VMSM	Rev 1A
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Date: Wednesday, June 03, 2009 Sheet 10 of 46

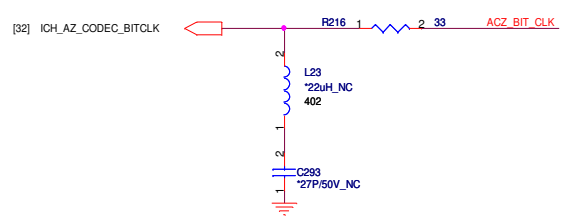
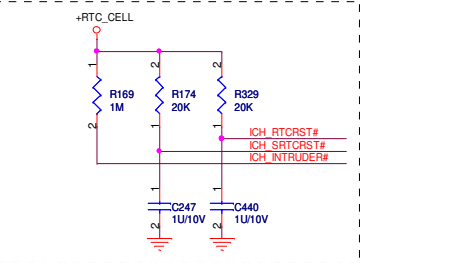


ICH9M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

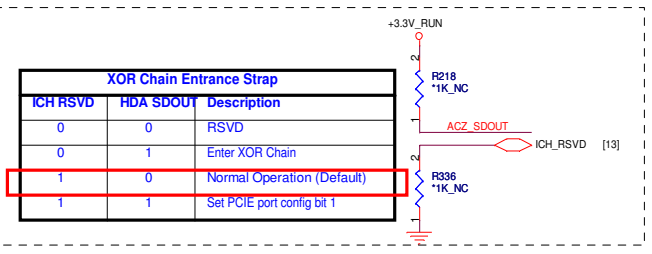
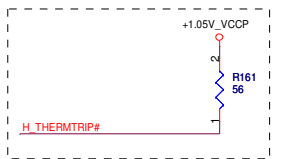
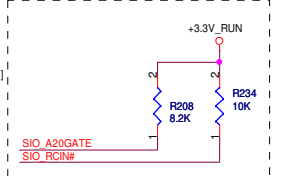
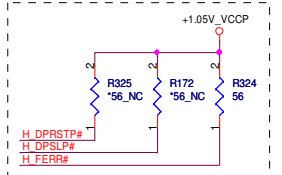
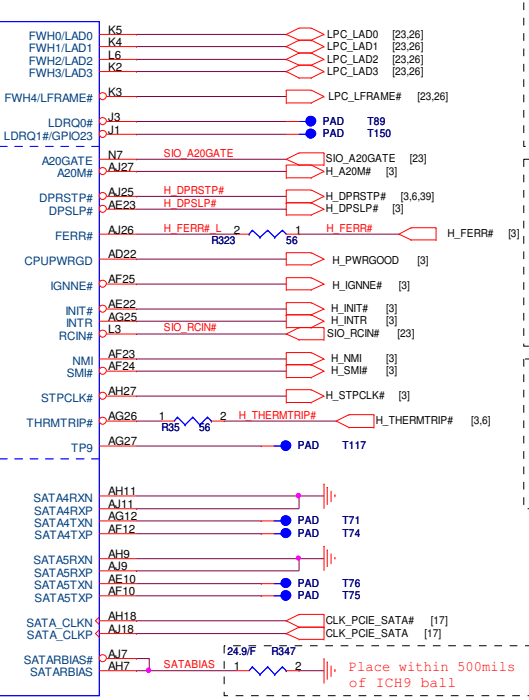
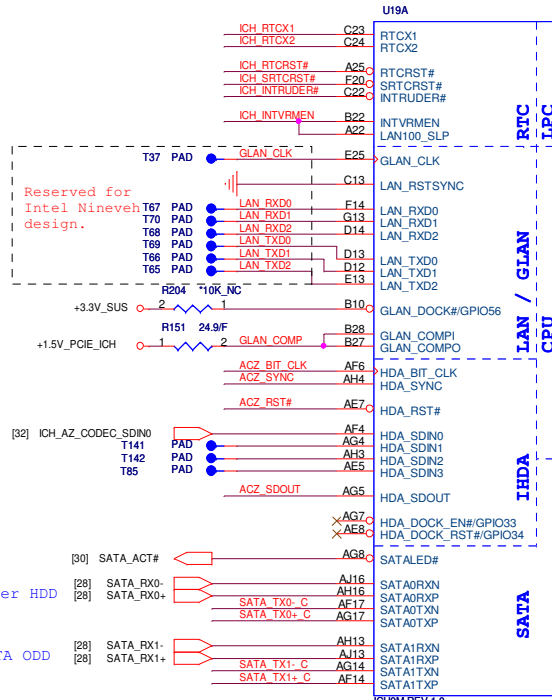
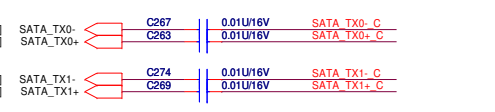
Low = Internal VR Disabled
High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

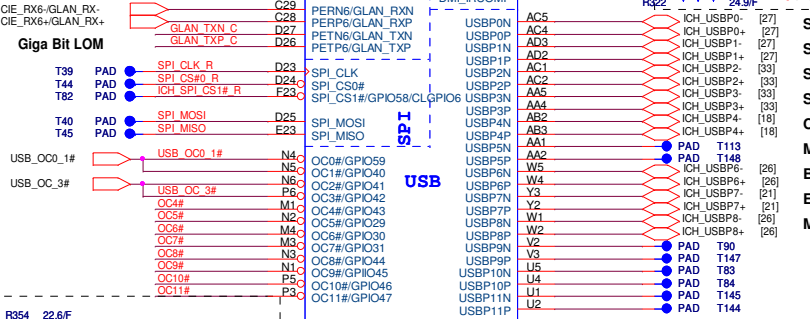
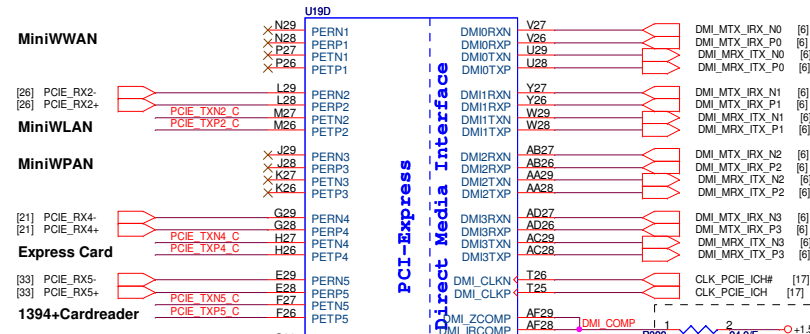
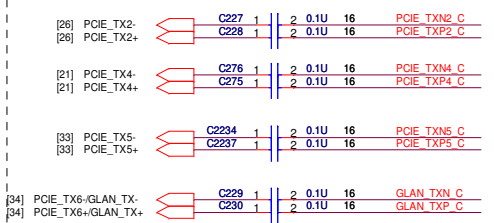
Low = Internal VR Disabled
High = Internal VR Enabled(Default)



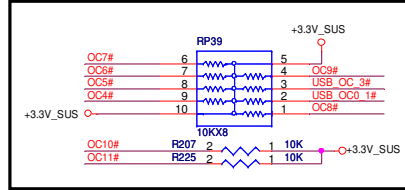
Place all series terms close to ICH9 except for SDIN input lines, which should be close to source.



Place TX DC blocking caps close ICH9.

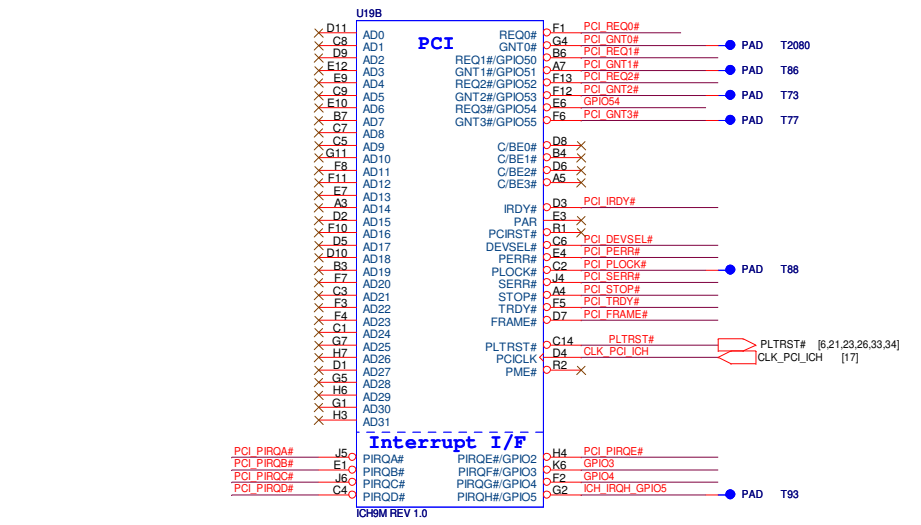
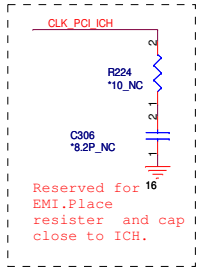
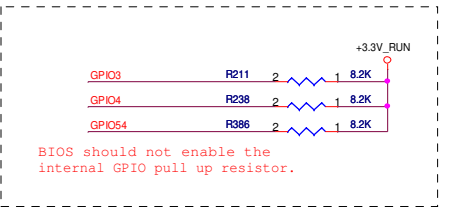
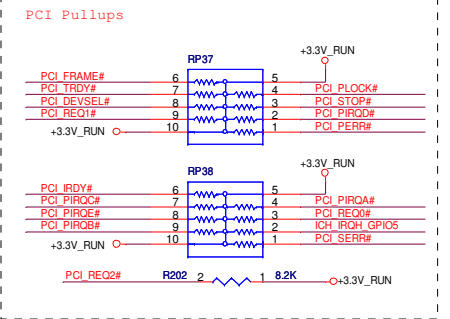


Boot BIOS Strap			
	GNT0#	SPI_CS1#	
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff



Place within 500mils of ICH9

- Side Pair Left
- Side Pair Left
- Side Pair Right
- Side Pair Right
- Camera
- Mini Card (WWAN)
- Bluetooth
- Express Card
- Mini Card (WLAN)

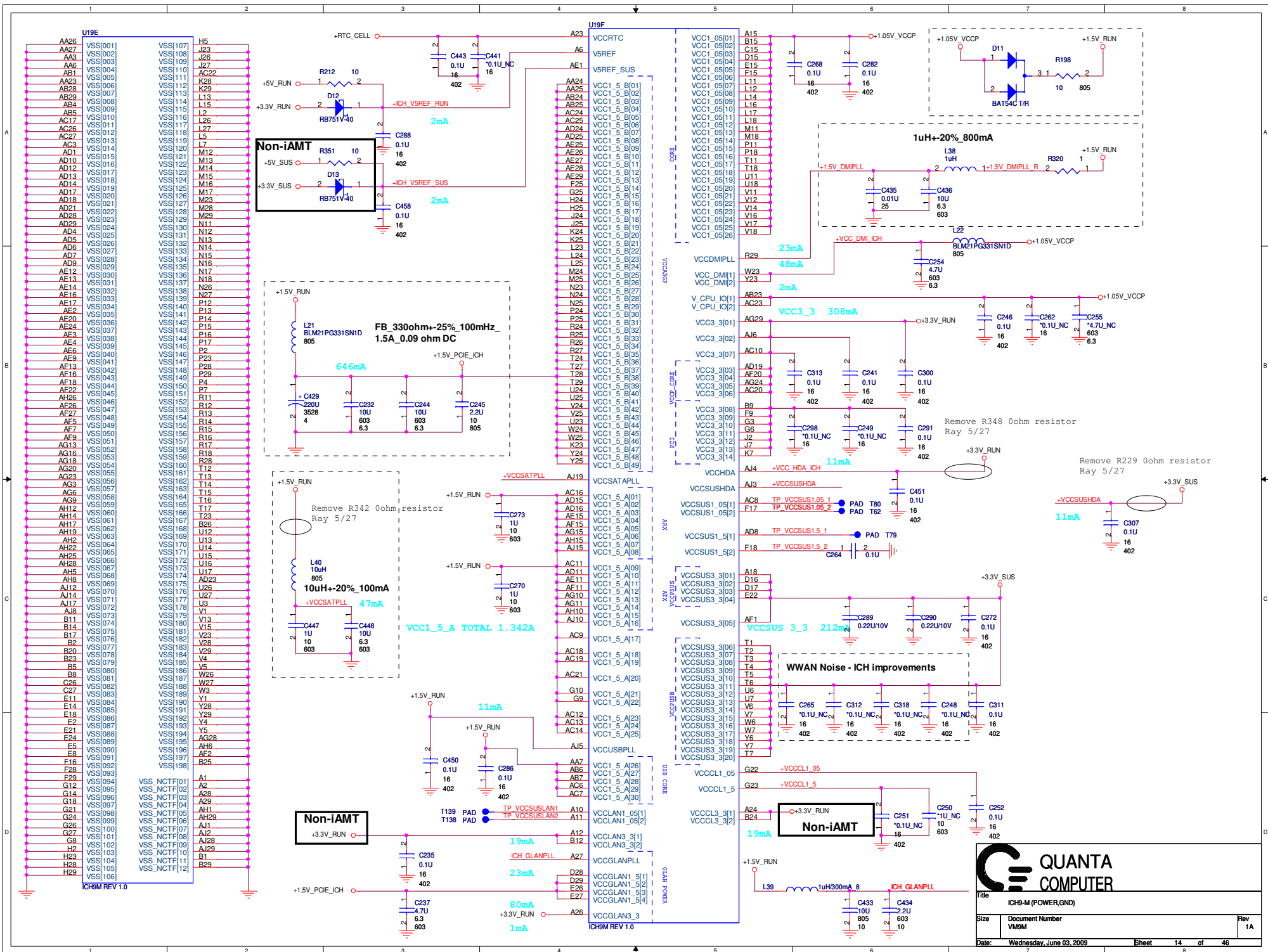


QUANTA COMPUTER

Title: ICH9-M (USB,DM,PCI,PCI)

Size: Document Number VMSM Rev 1A

Date: Saturday, June 06, 2009 Sheet 12 of 46

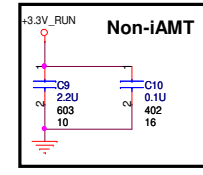
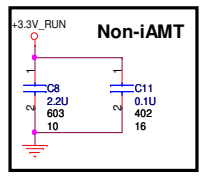
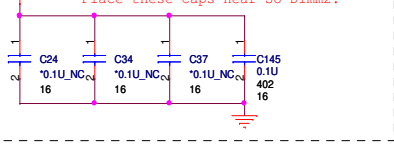
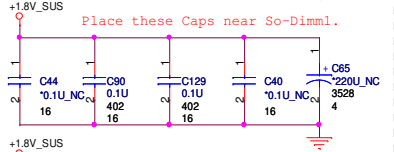
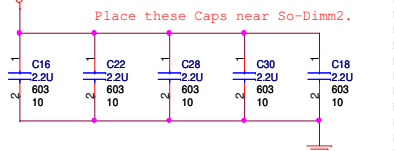
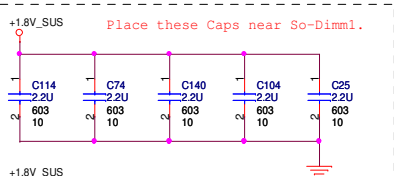
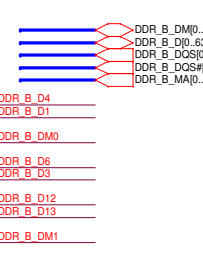
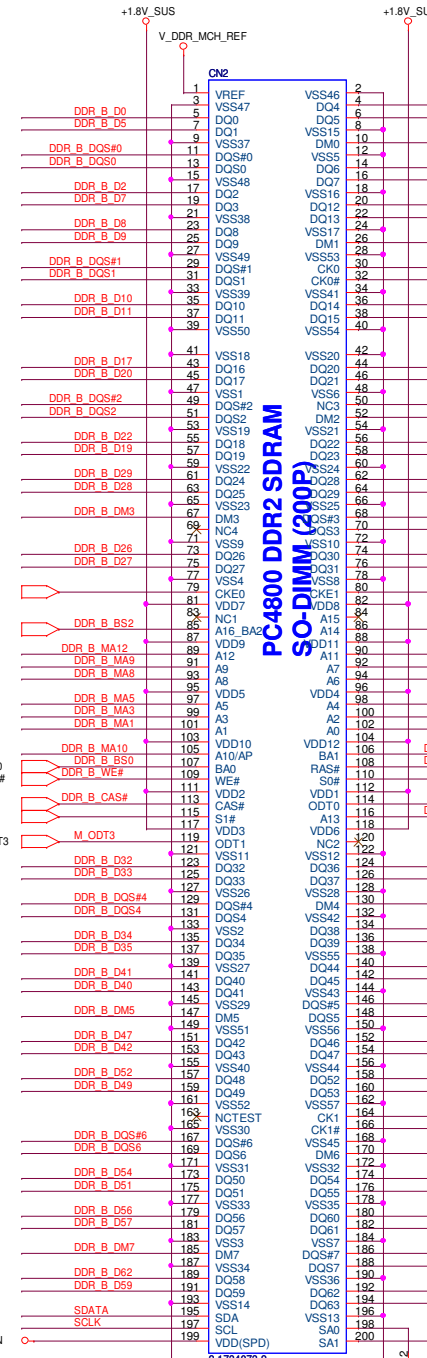
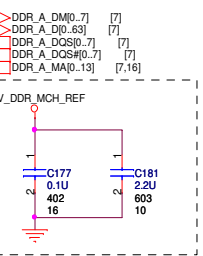
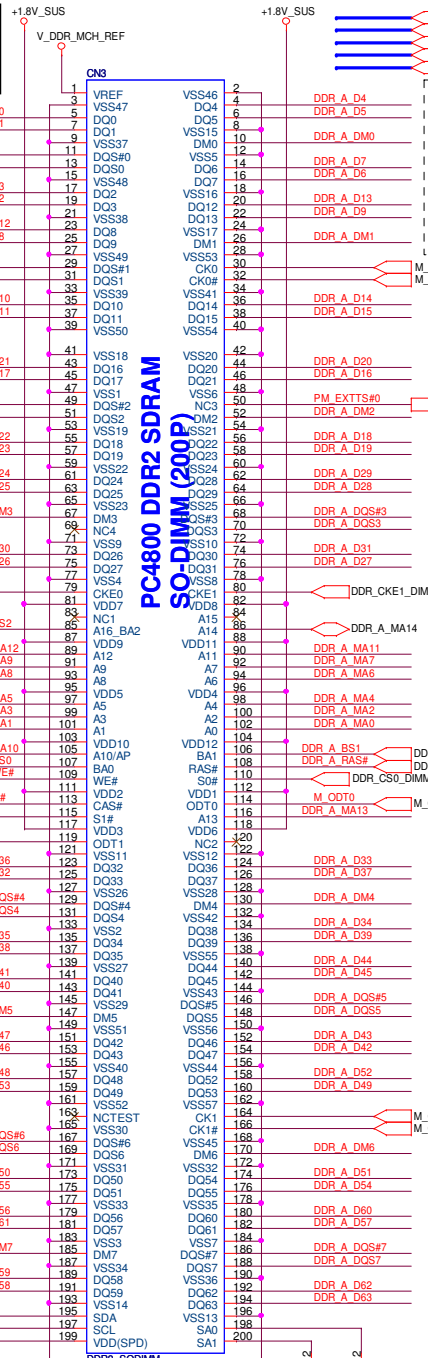


U19E

AA26	VSS1001	VSS107	H5
AA27	VSS1002	VSS108	J23
AA3	VSS1003	VSS109	J26
AA6	VSS1004	VSS110	J27
AA3	VSS1005	VSS111	AC22
AB1	VSS1006	VSS112	K28
AB28	VSS1007	VSS113	L13
AB29	VSS1008	VSS114	L15
AB4	VSS1009	VSS115	L2
AB5	VSS1010	VSS116	L26
AC17	VSS1011	VSS117	L27
AC26	VSS1012	VSS118	L5
AC27	VSS1013	VSS119	L7
AC3	VSS1014	VSS120	L12
AD1	VSS1015	VSS121	M12
AD10	VSS1016	VSS122	M13
AD12	VSS1017	VSS123	M14
AD13	VSS1018	VSS124	M15
AD14	VSS1019	VSS125	M16
AD17	VSS1020	VSS126	M17
AD18	VSS1021	VSS127	M28
AD21	VSS1022	VSS128	M29
AD28	VSS1023	VSS129	M29
AD29	VSS1024	VSS130	N11
AD4	VSS1025	VSS131	N13
AD5	VSS1026	VSS132	N14
AD6	VSS1027	VSS133	N14
AD7	VSS1028	VSS134	N15
AD9	VSS1029	VSS135	N17
AE12	VSS1030	VSS136	N18
AE13	VSS1031	VSS137	N26
AE14	VSS1032	VSS138	N27
AE16	VSS1033	VSS139	N27
AE17	VSS1034	VSS140	P12
AE2	VSS1035	VSS141	P13
AE20	VSS1036	VSS142	P14
AE24	VSS1037	VSS143	P15
AE3	VSS1038	VSS144	P16
AE4	VSS1039	VSS145	P17
AE6	VSS1040	VSS146	P2
AE9	VSS1041	VSS147	P23
AF13	VSS1042	VSS148	P28
AF18	VSS1043	VSS149	P4
AF22	VSS1044	VSS150	P7
AF3	VSS1045	VSS151	R11
AH26	VSS1046	VSS152	R12
AF26	VSS1047	VSS153	R13
AF7	VSS1048	VSS154	R14
AF5	VSS1049	VSS155	R15
AF9	VSS1050	VSS156	R16
AG13	VSS1051	VSS157	R17
AG16	VSS1052	VSS158	R18
AG18	VSS1053	VSS159	R28
AG20	VSS1054	VSS160	T12
AG23	VSS1055	VSS161	T13
AG3	VSS1056	VSS162	T14
AG6	VSS1057	VSS163	T15
AG9	VSS1058	VSS164	T16
AGH9	VSS1059	VSS165	T17
AH12	VSS1060	VSS166	T22
AH14	VSS1061	VSS167	T23
AH17	VSS1062	VSS168	U12
AH19	VSS1063	VSS169	U13
AH2	VSS1064	VSS170	U14
AH22	VSS1065	VSS171	U15
AH25	VSS1066	VSS172	U16
AH28	VSS1067	VSS173	U17
AH5	VSS1068	VSS174	U27
AH8	VSS1069	VSS175	AD23
AJ12	VSS1070	VSS176	U26
AJ14	VSS1071	VSS177	U27
AJ17	VSS1072	VSS178	U3
B11	VSS1073	VSS179	V1
B14	VSS1074	VSS180	V13
B17	VSS1075	VSS181	V15
B2	VSS1076	VSS182	V23
B20	VSS1077	VSS183	V29
B23	VSS1078	VSS184	V4
B5	VSS1080	VSS186	V5
B8	VSS1081	VSS187	W27
C26	VSS1082	VSS188	W3
C27	VSS1083	VSS189	Y1
E11	VSS1084	VSS190	Y2
E18	VSS1085	VSS191	Y4
E2	VSS1086	VSS192	Y5
E21	VSS1087	VSS193	AG28
E24	VSS1088	VSS194	AH6
E5	VSS1089	VSS195	AE2
FR	VSS1090	VSS196	B25
F16	VSS1091	VSS197	B25
F28	VSS1092	VSS198	B25
F29	VSS1093	VSS199	B25
G12	VSS1094	VSS_NCTF[0]	A1
G14	VSS1095	VSS_NCTF[02]	A28
G18	VSS1096	VSS_NCTF[03]	A28
G21	VSS1097	VSS_NCTF[04]	A29
G24	VSS1098	VSS_NCTF[05]	A29
G26	VSS1099	VSS_NCTF[06]	AH1
G27	VSS1100	VSS_NCTF[07]	AH2
G8	VSS1101	VSS_NCTF[08]	AJ28
H2	VSS1102	VSS_NCTF[09]	AJ29
H23	VSS1103	VSS_NCTF[10]	B29
H28	VSS1104	VSS_NCTF[11]	B29
H29	VSS1105	VSS_NCTF[12]	B29
H29	VSS1106	VSS_NCTF[12]	B29



A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.



Non-iAMT SMbus address A0

CLOCK 0,1 CKE 0,1

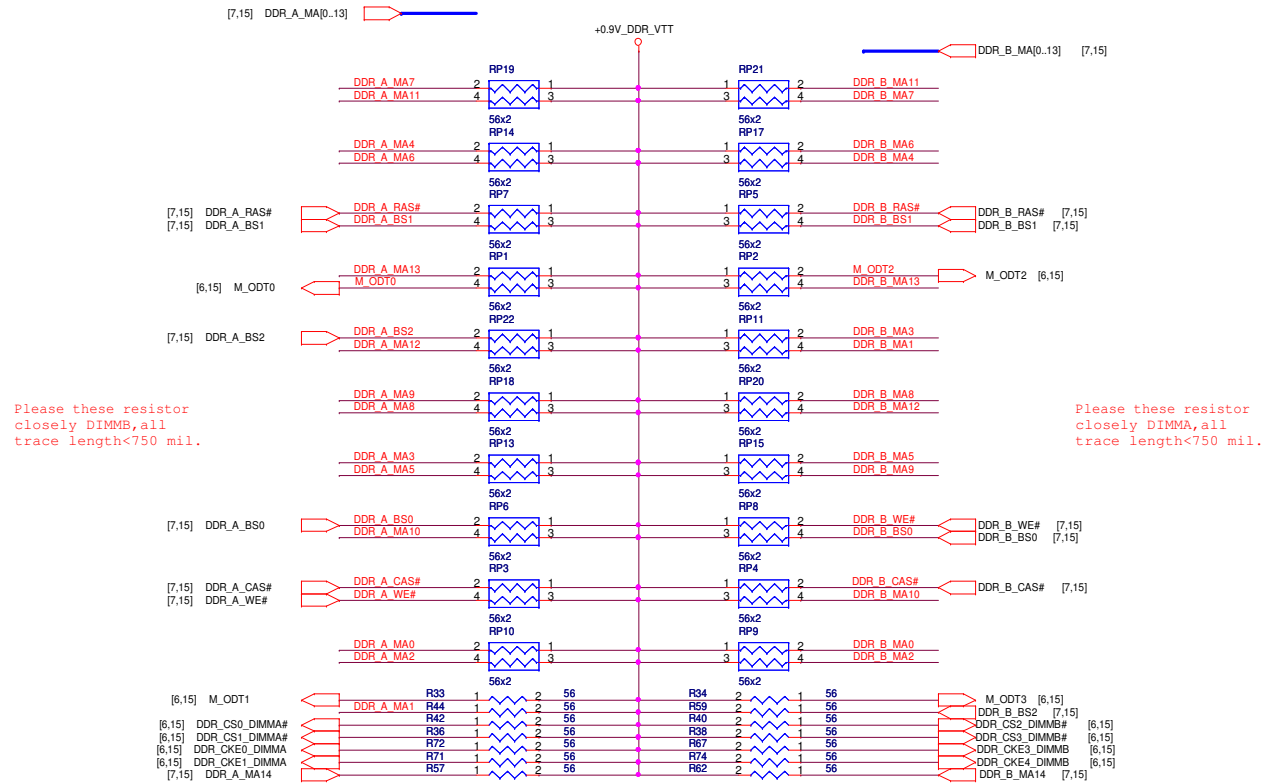
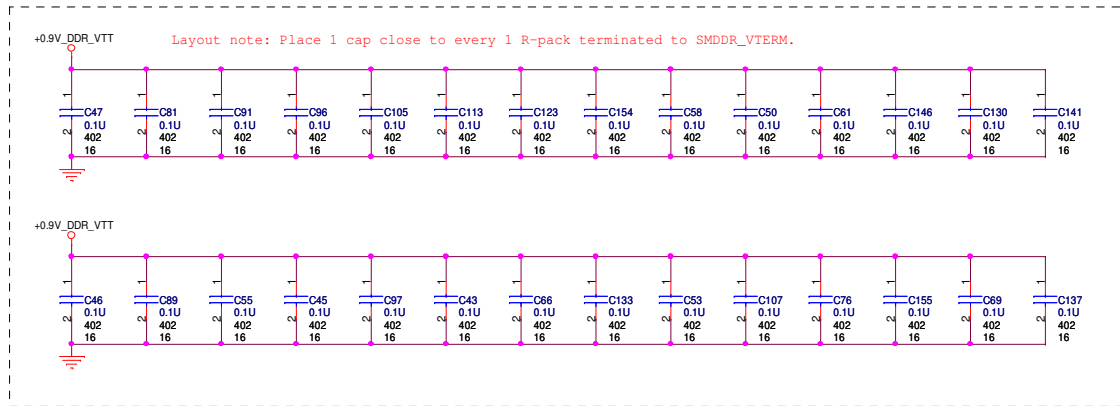
Non-iAMT SMbus address A4

CLOCK 2,3 CKE 2,3

Non-iAMT



Title			DDR2 SDRAM (200P) X 2		
Size	Document Number	VMSM		Rev	1A
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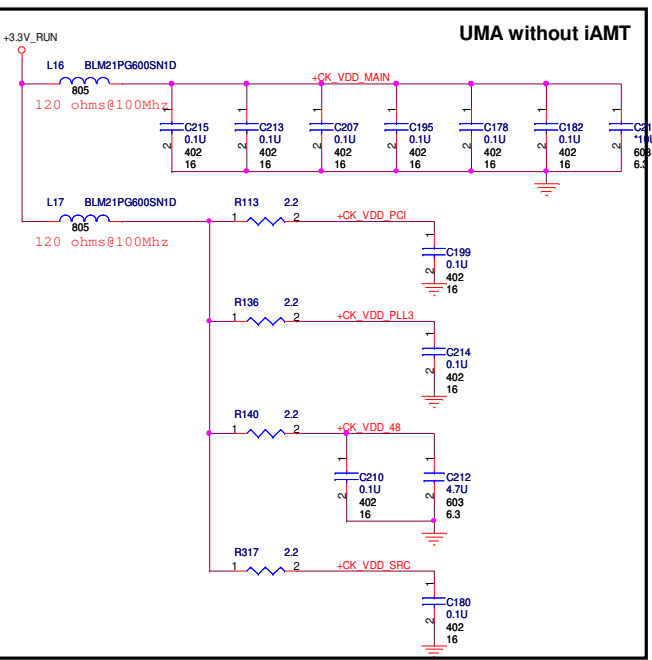
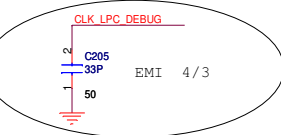
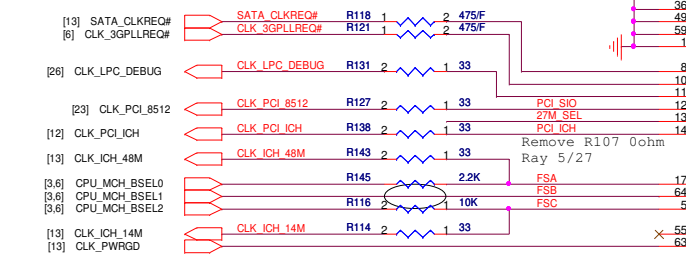
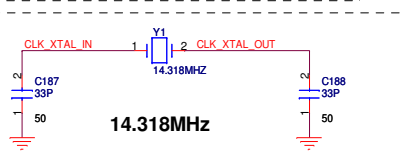
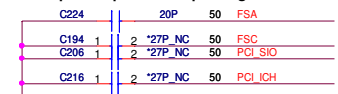
QUANTA COMPUTER

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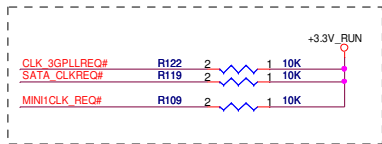
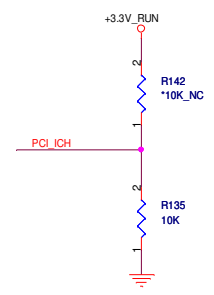
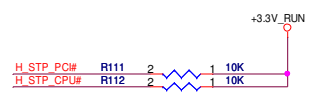
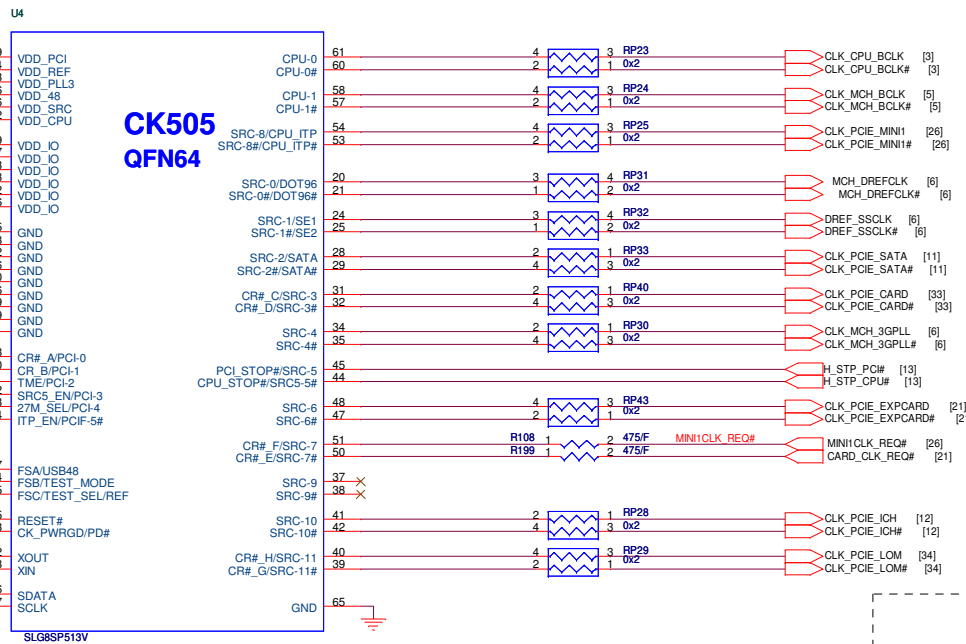
Size	Document Number VMSM	Rev 1A
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Add capacitor pads for improving WWAN.



CK505 QFN64

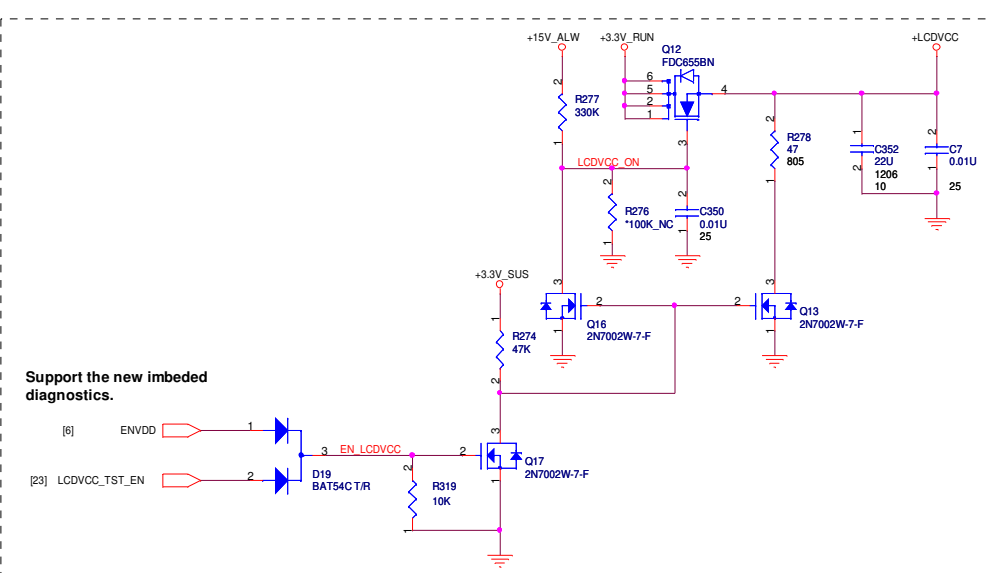


FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	0	0	200	100	33
0	1	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

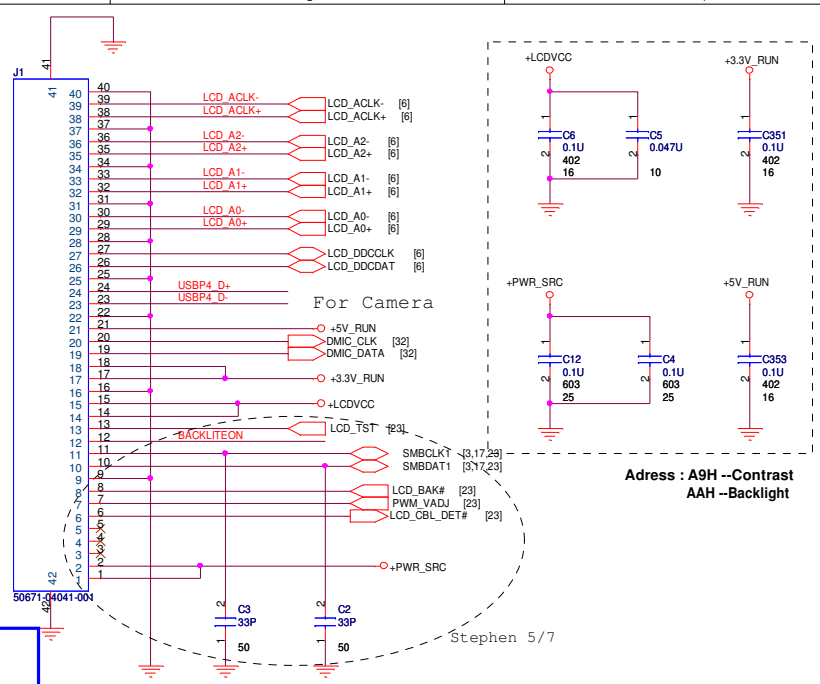
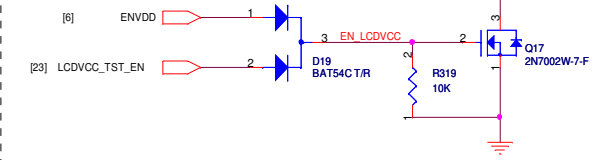
27M_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



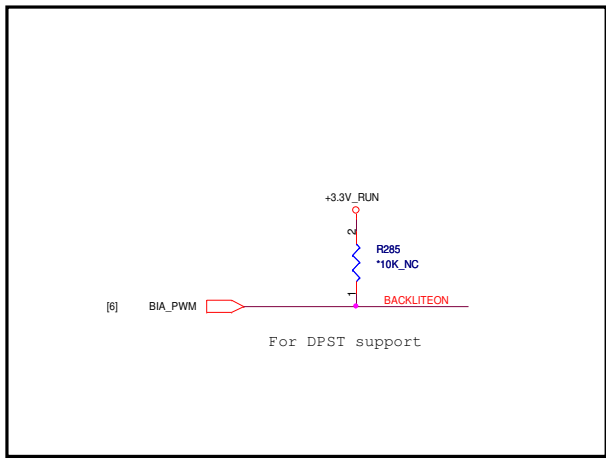


Support the new imbedded diagnostics.

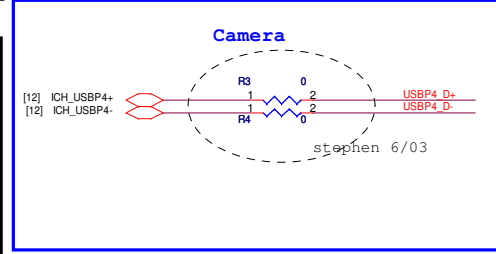


Address : A9H --Contrast
AAH --Backlight

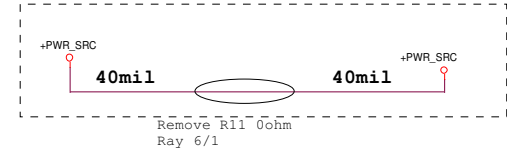
Stephen 5/7



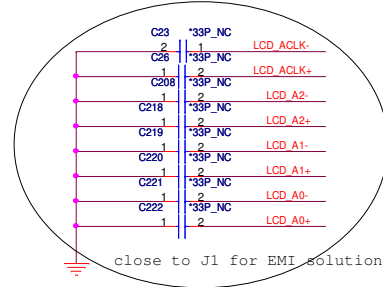
For DPST support



stephen 6/03

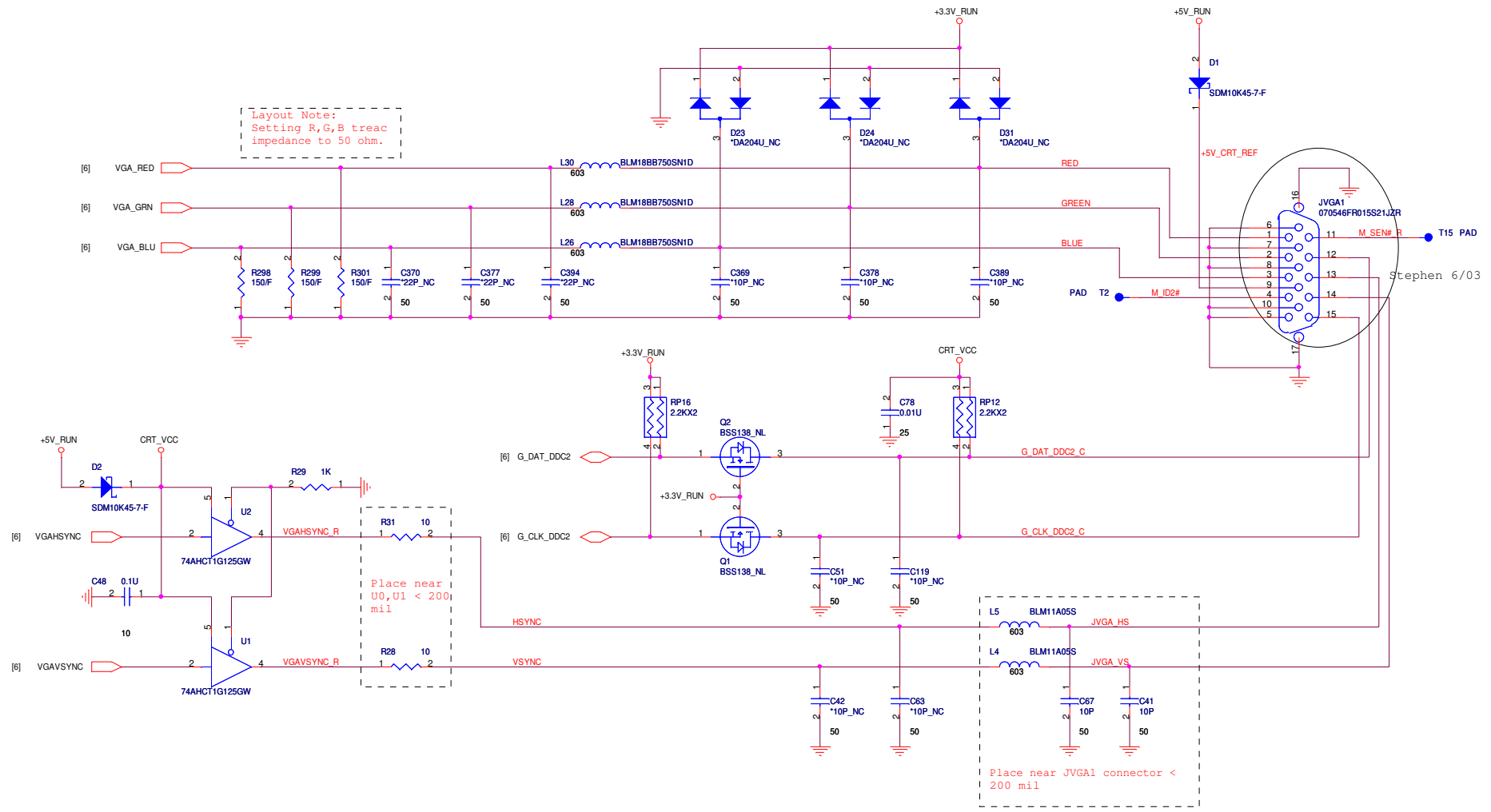


Remove R11 0ohm
Ray 6/1



close to J1 for EMI solution

Layout Note:
Setting R,G,B treac
impedance to 50 ohm.



Place near
U0,U1 < 200
mil

Place near JVGA1 connector <
200 mil

Stephen 6/03



Title CRT&TV CONN		
Size VMSM	Document Number VMSM	Rev 1A
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A

B

C

D

E

1

1

2


2

3

3

4

4

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Title	Card Reader-RTS5158E	
Size	Document Number VM9M	Rev 1A
Date:	Wednesday, June 03, 2009	Sheet 20 of 46

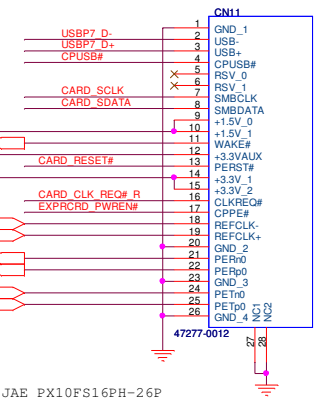
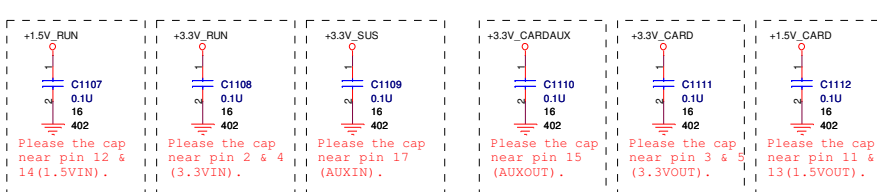
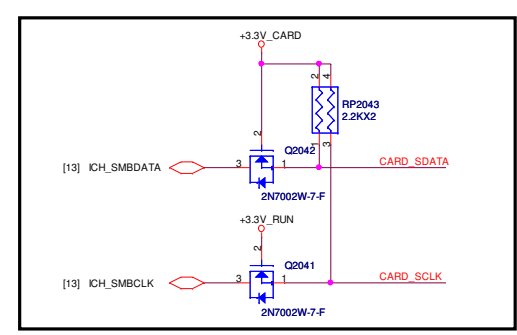
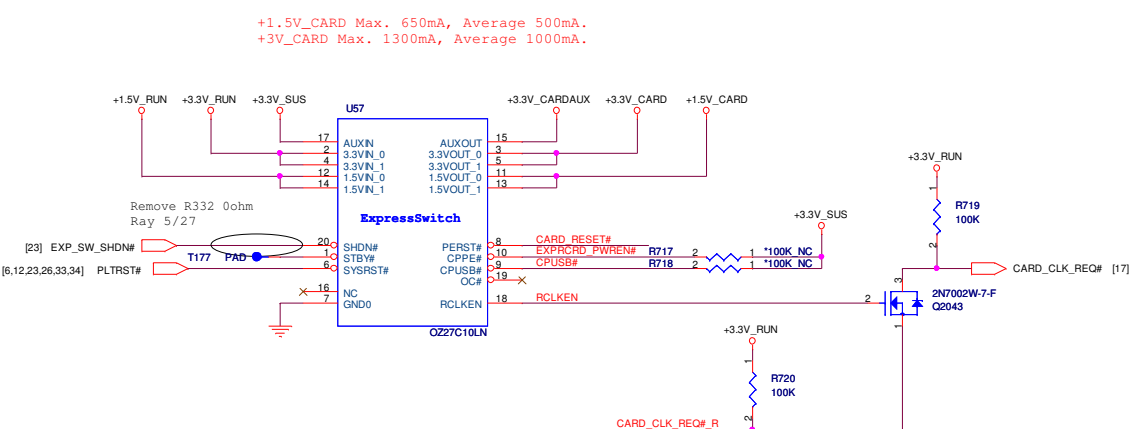
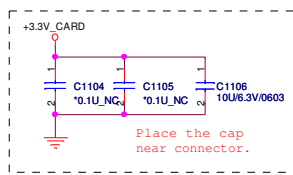
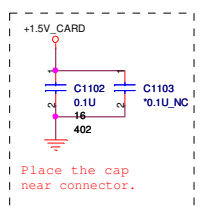
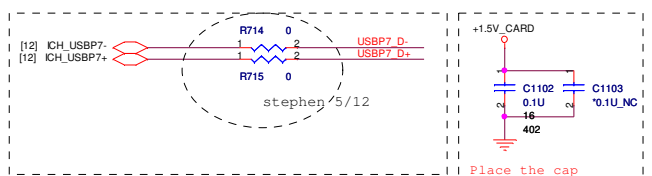
A

B

C

D

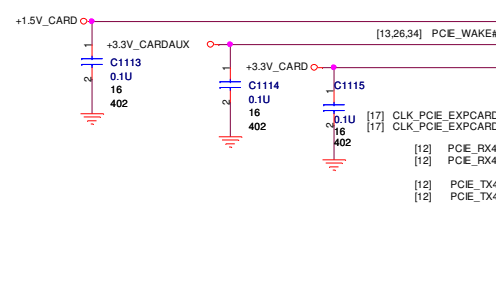
E



Express Card

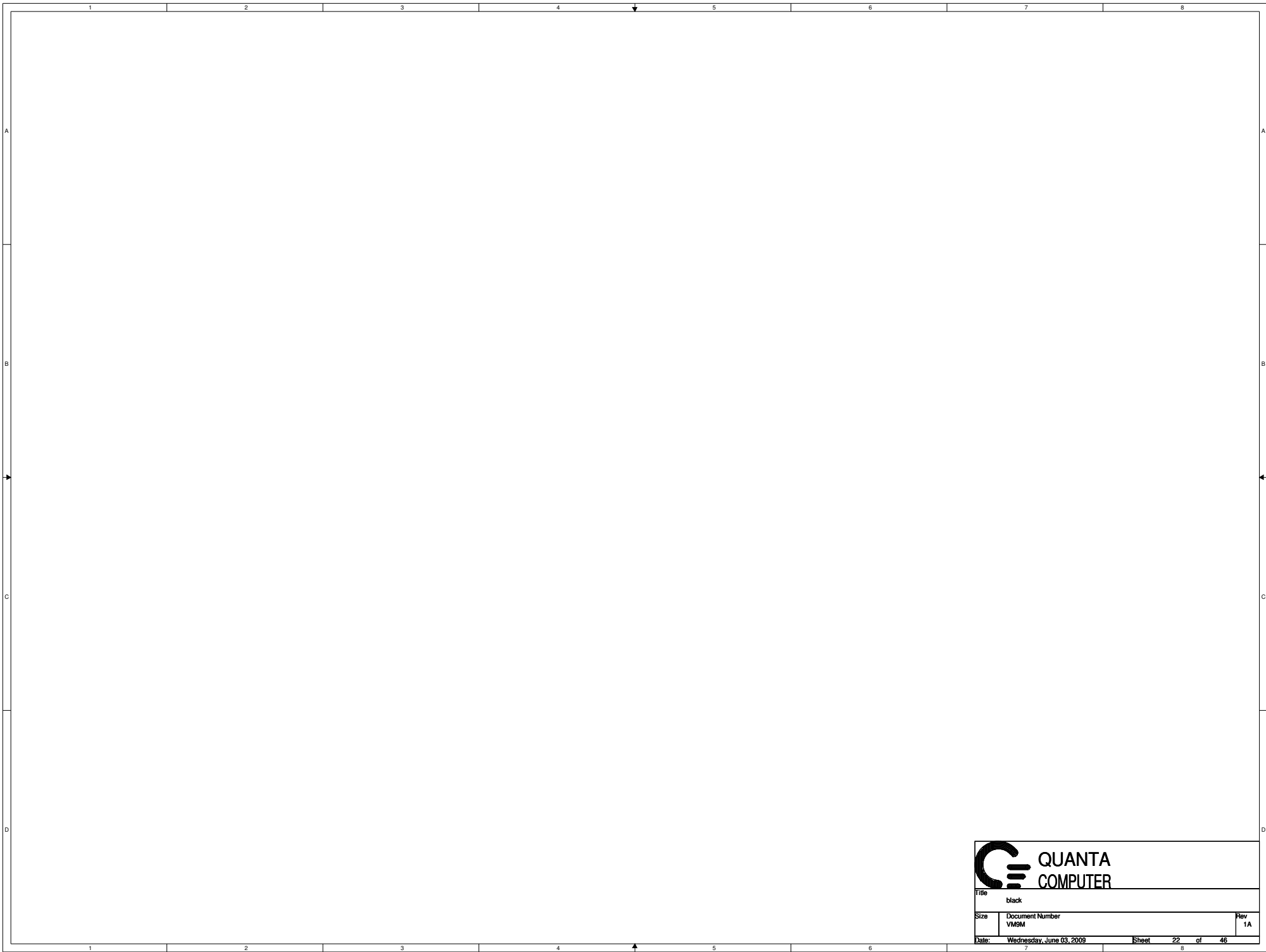


Express Card cage



JAE PX10FS16PH-26P

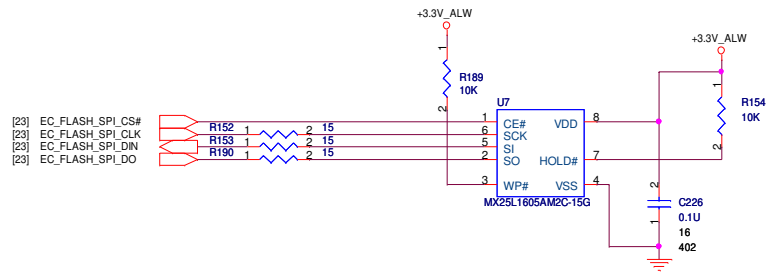
		Title	
		Express Card	
Size	Document Number	Rev	
	VMM8	1A	
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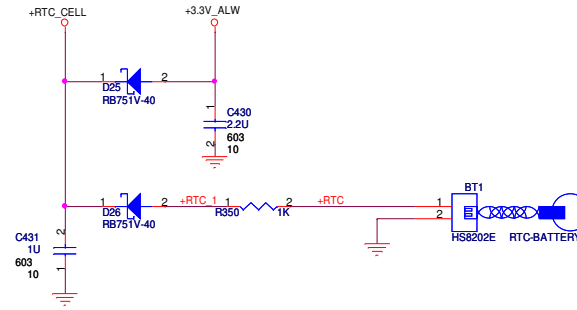
QUANTA
COMPUTER

Title black		
Size	Document Number VMSM	Rev 1A
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16Mbit (2M Byte), SPI



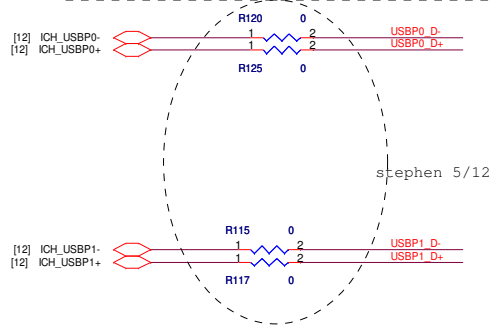
RTC BATTERY



	1	2	3	4	5	6	7	8
A								
B								
C								
D								
	1	2	3	4	5	6	7	8

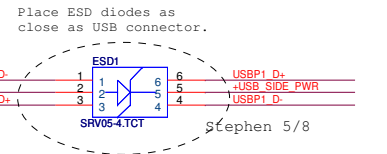
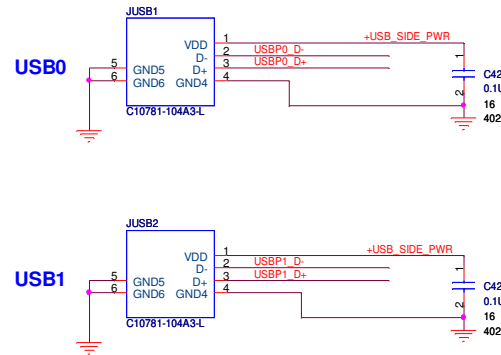
 QUANTA COMPUTER		
Title: Black		
Size: VMSM	Document Number:	Rev: 1A
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External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

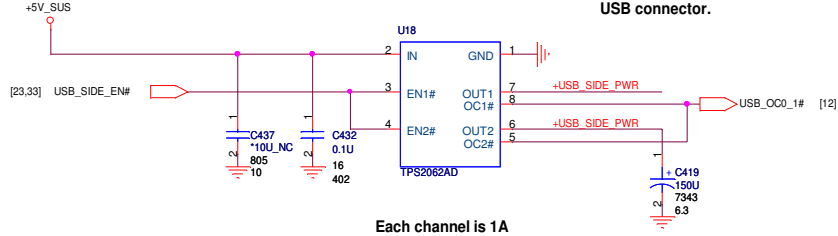


stephen 5/12

Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.




stephen 5/8



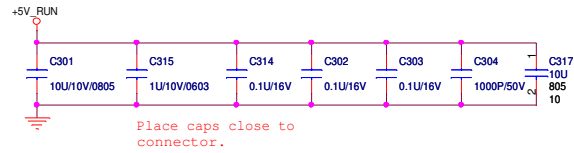
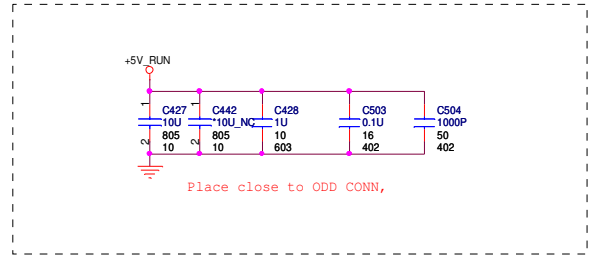
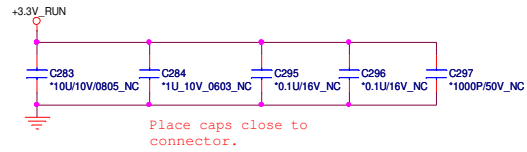
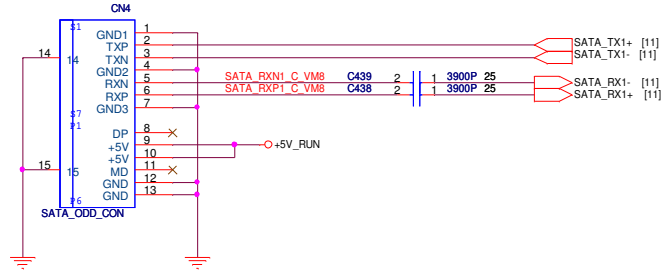
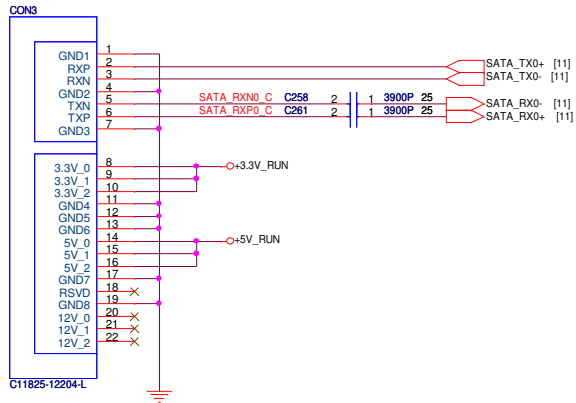
Place one 150uF cap by each USB connector.

Each channel is 1A

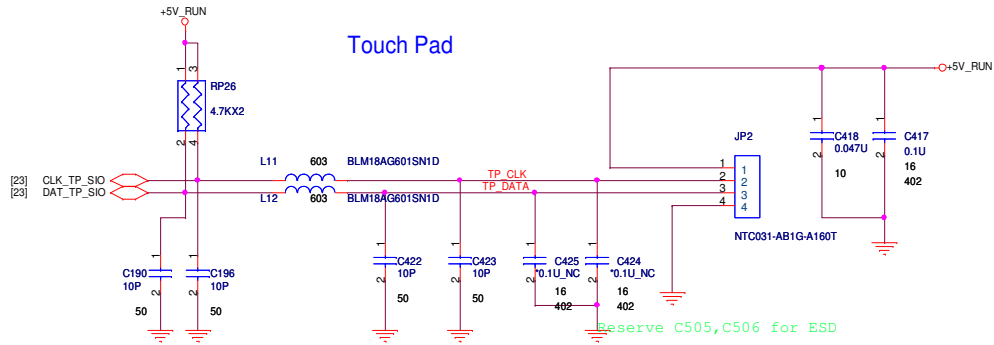
 QUANTA COMPUTER		
Title SERIAL PORT & USB		
Size	Document Number VM9M	Rev 1A
Date: Wednesday, June 03, 2009 Sheet 27 of 46		

SATA HDD Connector.

SATA ODD Connector.

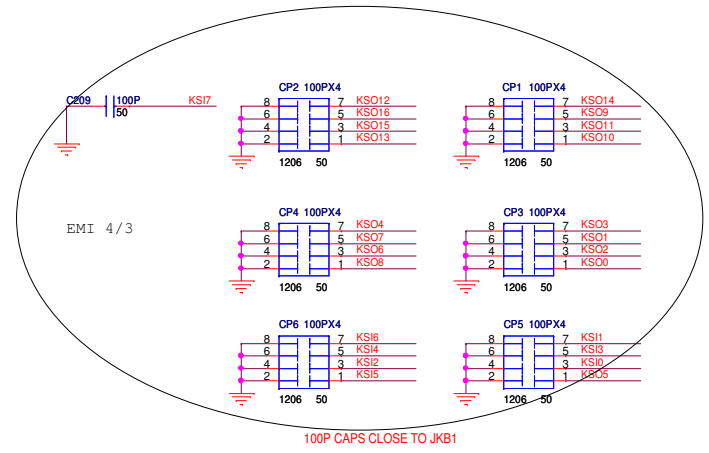
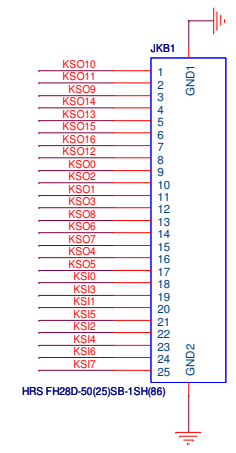


Touch Pad



KEYBOARD CONNECTOR

[23] KSO[0..16]
 [23] KSI[0..7]



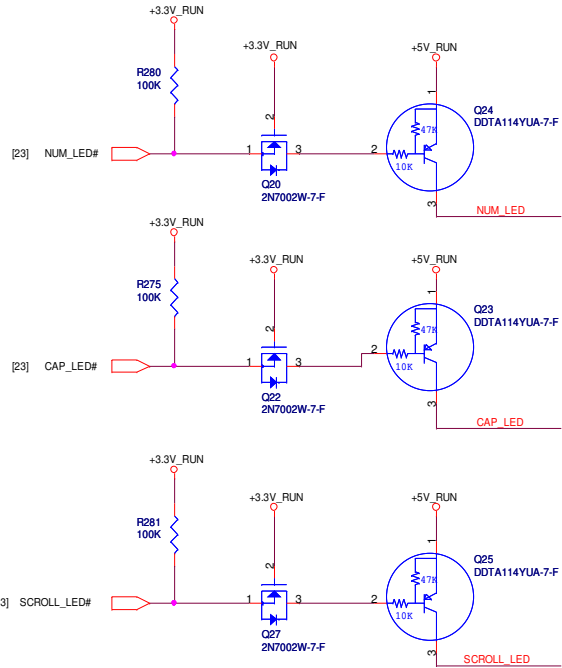
QUANTA COMPUTER

Title: TOUCH PAD, BULE TOOTH & FIR

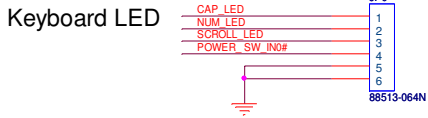
Size	Document Number VMSM	Rev 1A
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Date: Wednesday, June 03, 2009 Sheet 29 of 46

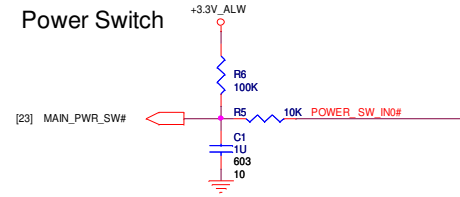
Keyboard LED



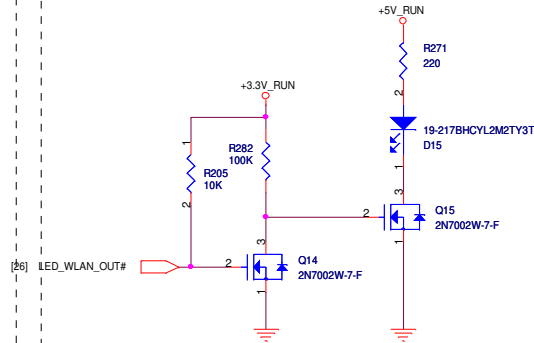
Dash board connector



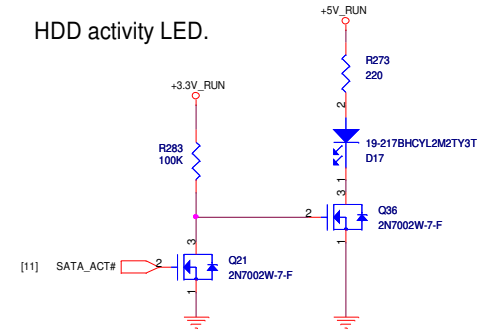
Power Switch



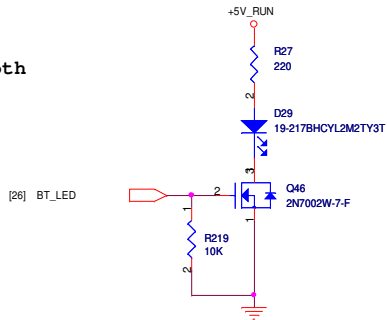
WLAN



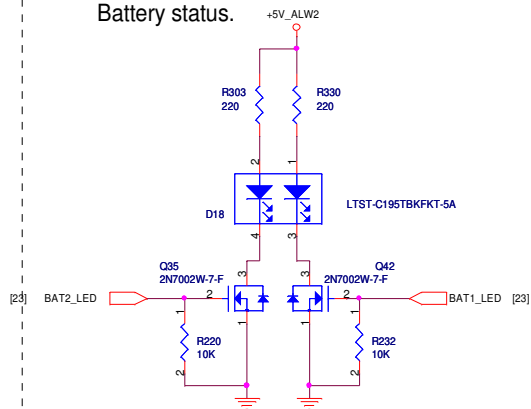
HDD activity LED.



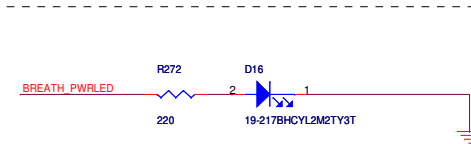
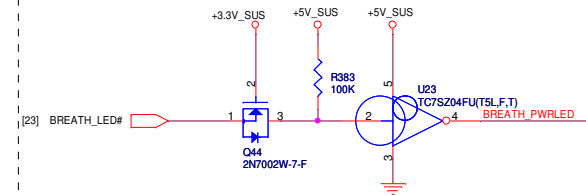
Bluetooth

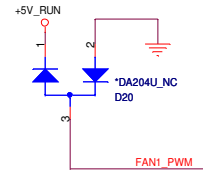
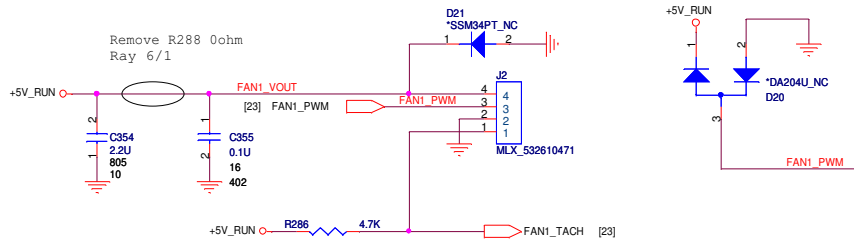



Battery status.

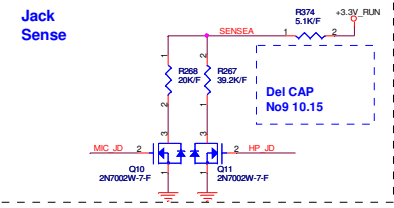
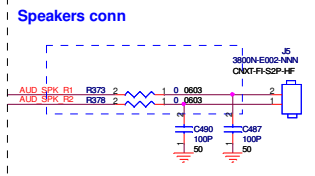
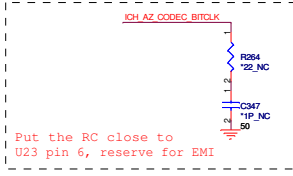


Power & Suspend.



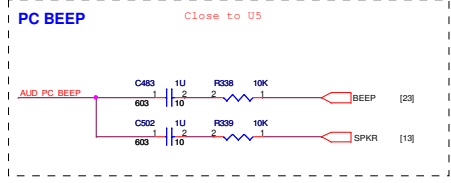
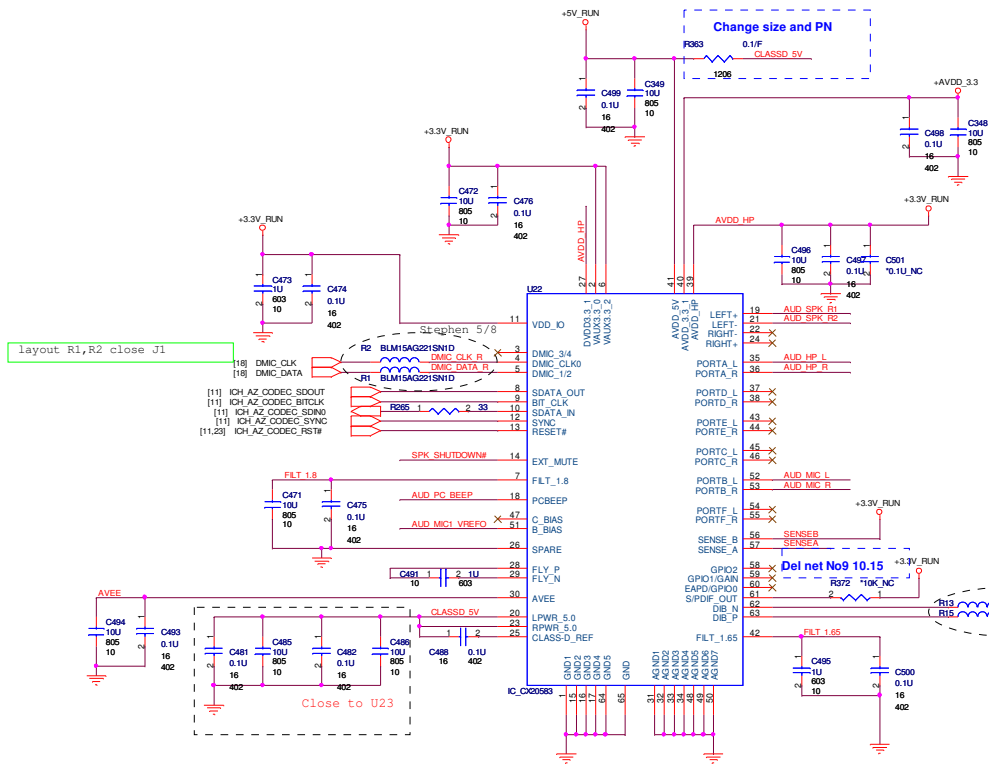


 QUANTA COMPUTER		
Title: FAN & THERMAL		
Size: VMSM	Document Number: VMSM	Rev: 1A
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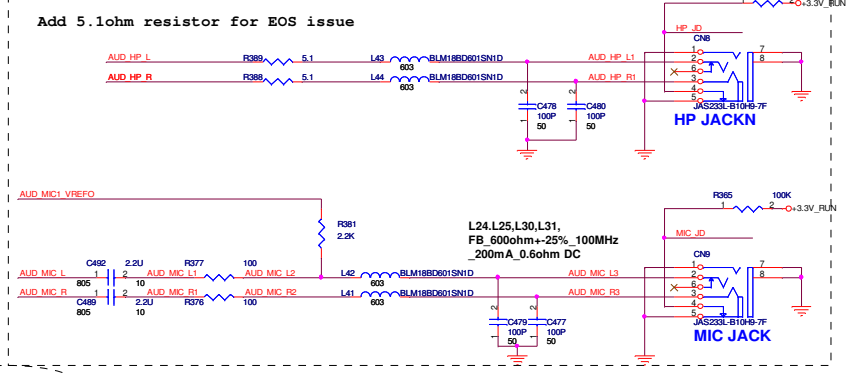


Add PC beep for system error circuit No9 10.14
Del PC beep No9 10.15

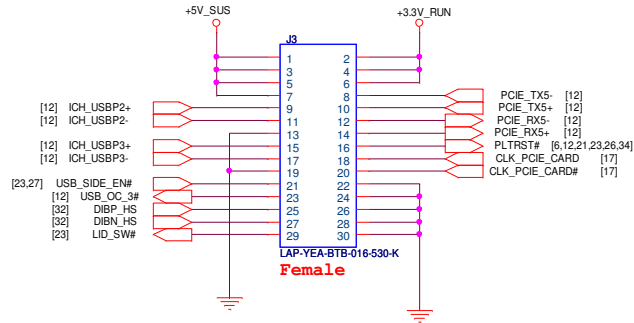
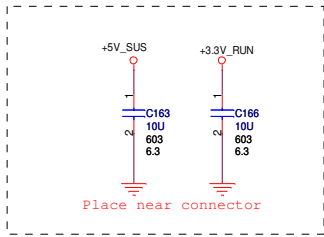
AUDIO CODEC



Audio Jacks

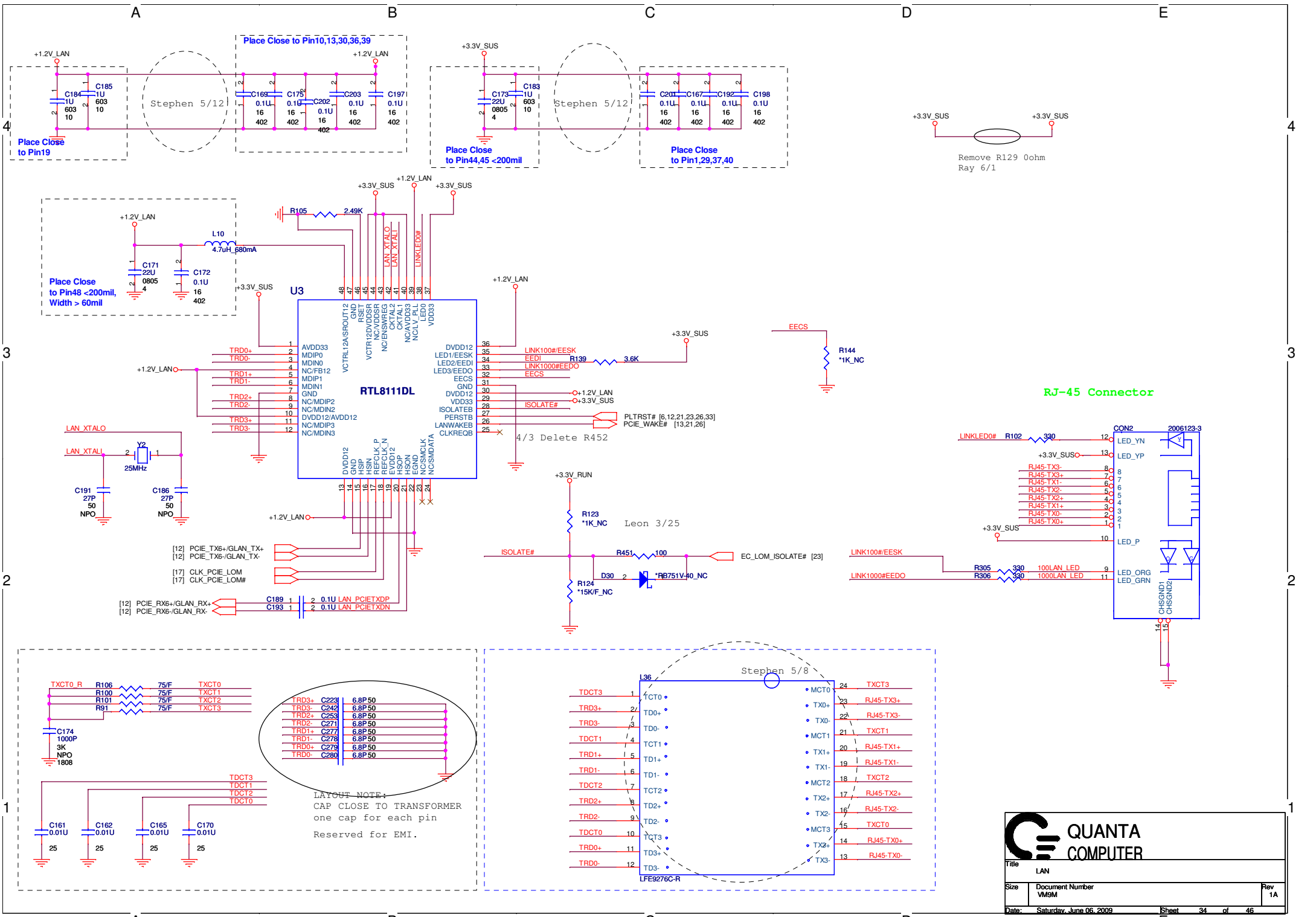


Title		
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Board to board connector (Modem Card + Cardreader+1394a+ 2 USB Port)

QUANTA COMPUTER		
Title		
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QUANTA COMPUTER

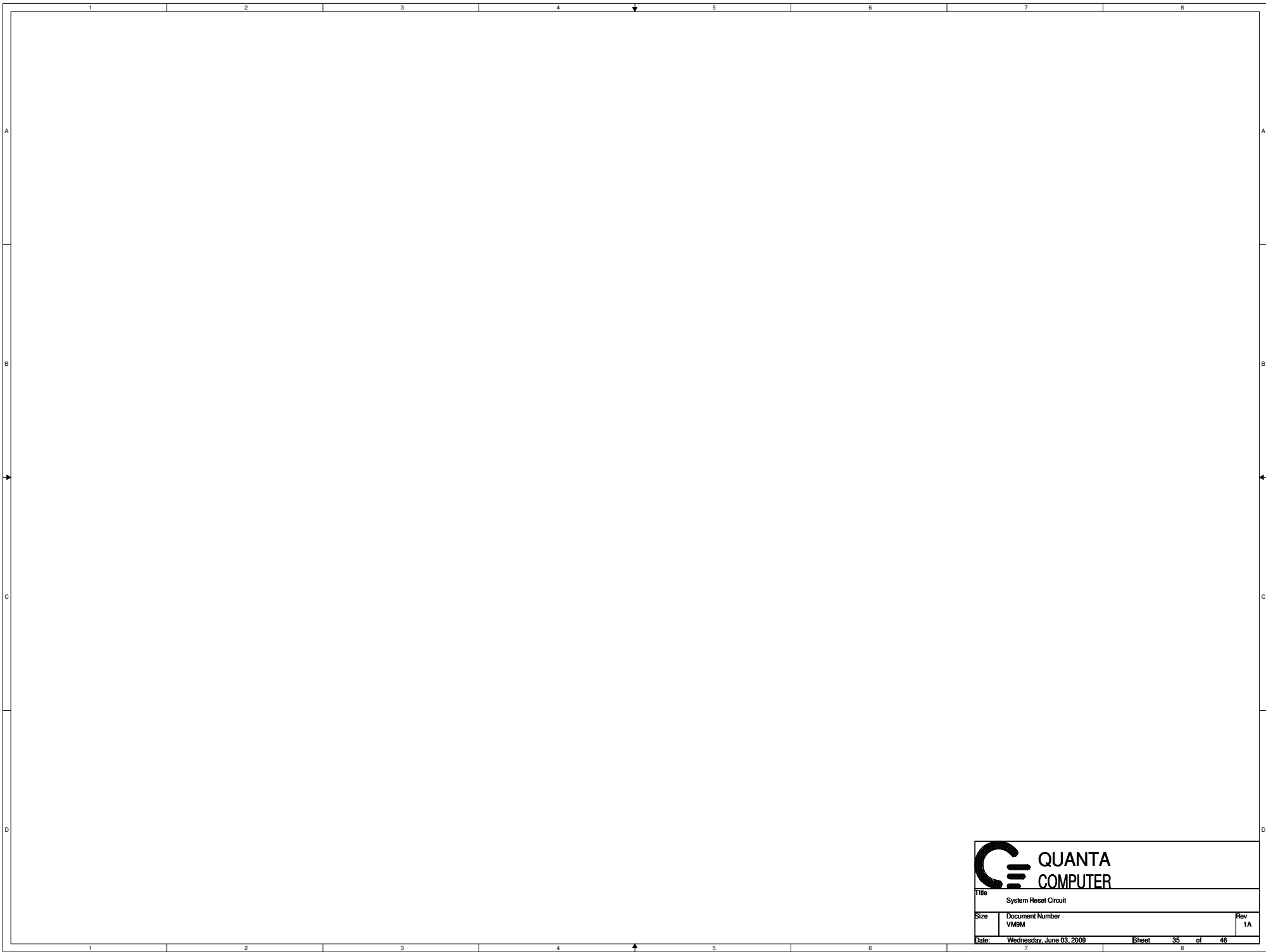
Title: LAN


Size: Document Number VM9M

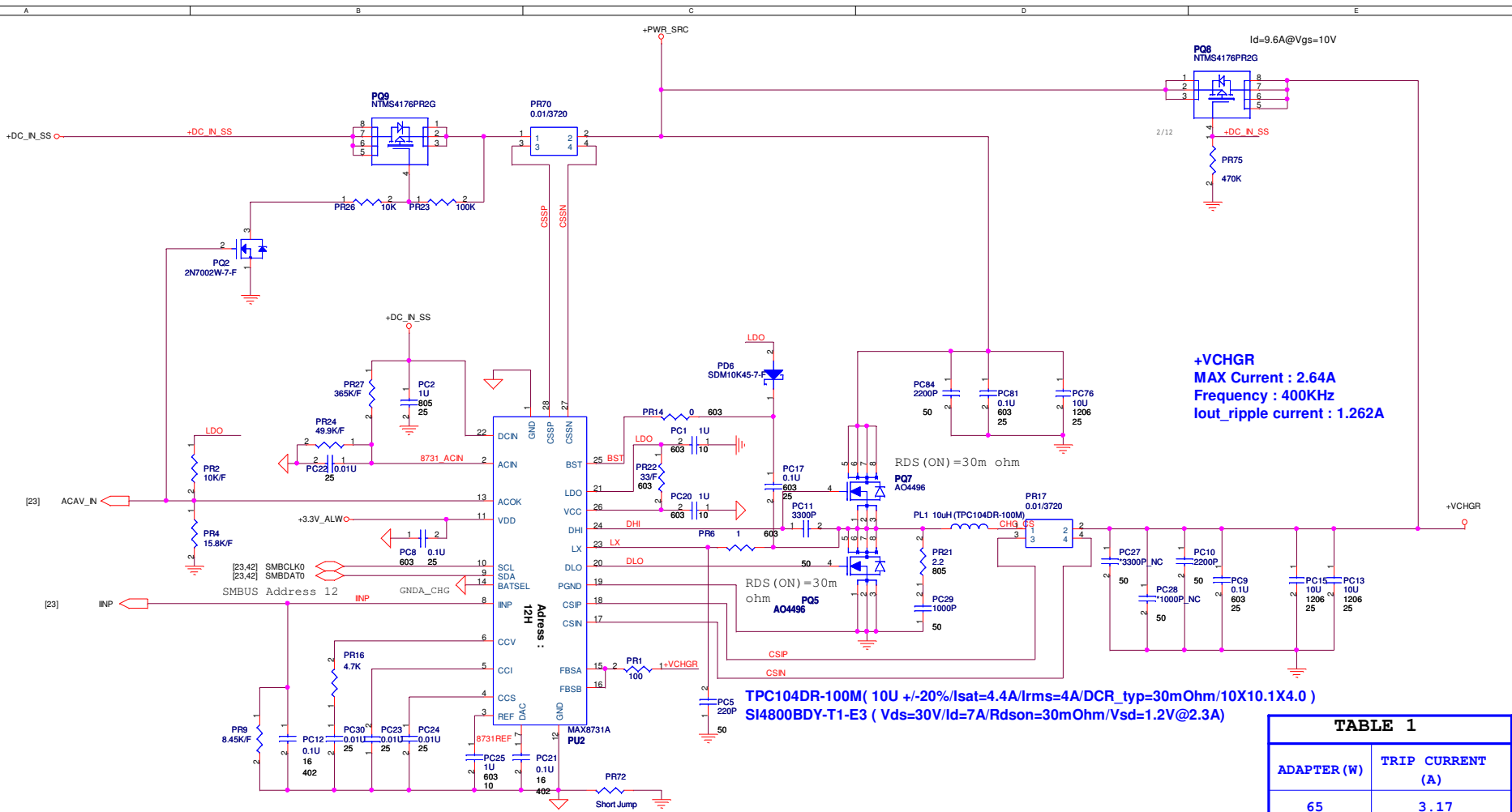
Date: Saturday, June 06, 2009

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 QUANTA COMPUTER		
Title: System Reset Circuit		
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+VCHGR
MAX Current : 2.64A
Frequency : 400KHz
Iout_ripple current : 1.262A

TPC104DR-100M (10U +/-20%/Isat=4.4A/Irms=4A/DCR_typ=30mOhm/10X10.1X4.0)
SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm/Vsd=1.2V@2.3A)

ADAPTER (W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.28

QUANTA COMPUTER

Title: Charger (MAX8731A)

Size: Document Number VM9M Rev: 1A

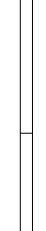
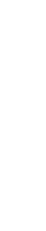
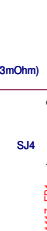
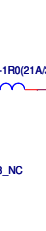
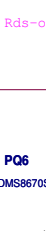
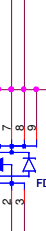
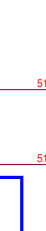
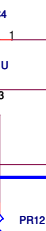
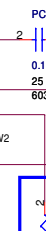
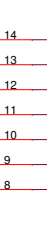
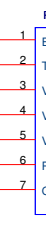
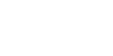
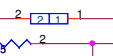
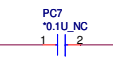
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Remove PR3 0ohm
Ray 6/3

[23.38.41] RUN_ON

[23.38] HWPG

Remove PR18 0ohm
Ray 6/3



Current Limiting Setting :
 $R_{trip}(Kohm) = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$

+1.05V_VCCP
TDC : 14.947A
OCP: 21.354A
Frequency : 300KHz
I_{out_ripple} current : 3.3207A

$V_{OUT} = (1 + R1/R2) * 0.75$
 The recommended R2 value is 10 K to 100 K.

APXE2R5ARA561ME61G (560UF/2.5V/ESR16)
 MPO104-1R0 (1.00 +/- 20% Isat=30A/DCR_max=3m Ohm/11.5X10X4)

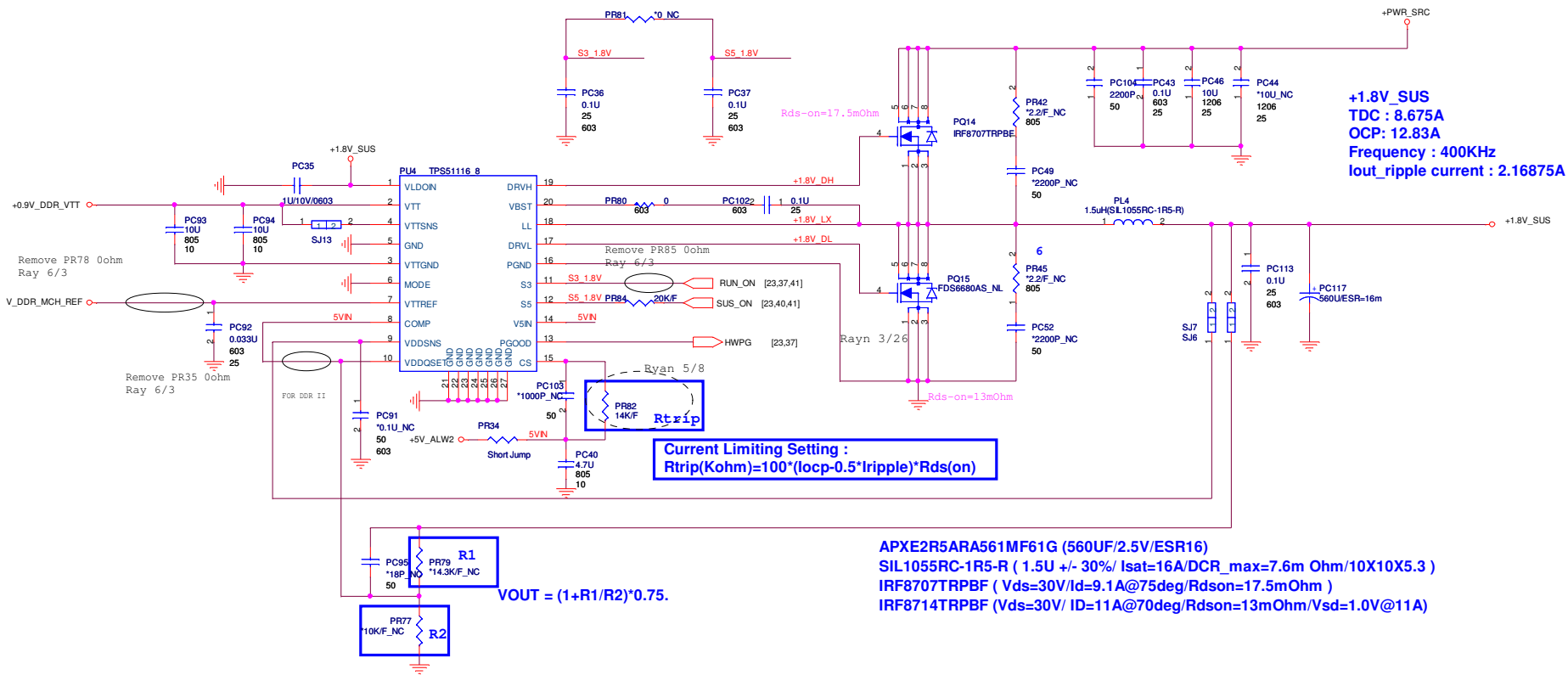
NTMFS4921NT1G (V_{ds}=30V/I_d=10.2A@85deg/R_{ds(on)}=10.5mOhm)
 NTMFS4946NT1G (V_{ds}=30V/ I_D=14.6A@85deg/R_{ds(on)}=5.1mOhm/V_{sd}=1.0V@30A)

Max current (TDC) -> 1.505A

$V_{out} = 0.8 (1 + R1/R2)$
 $= 1.5V$



Title 1.05_VCCP & 1.5V_RUN(TPS51117)		
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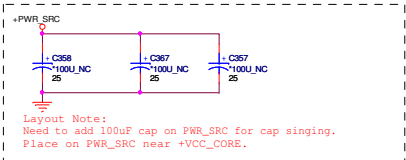


+1.8V_SUS
TDC : 8.675A
OCP: 12.83A
Frequency : 400KHz
lout_ripple current : 2.16875A

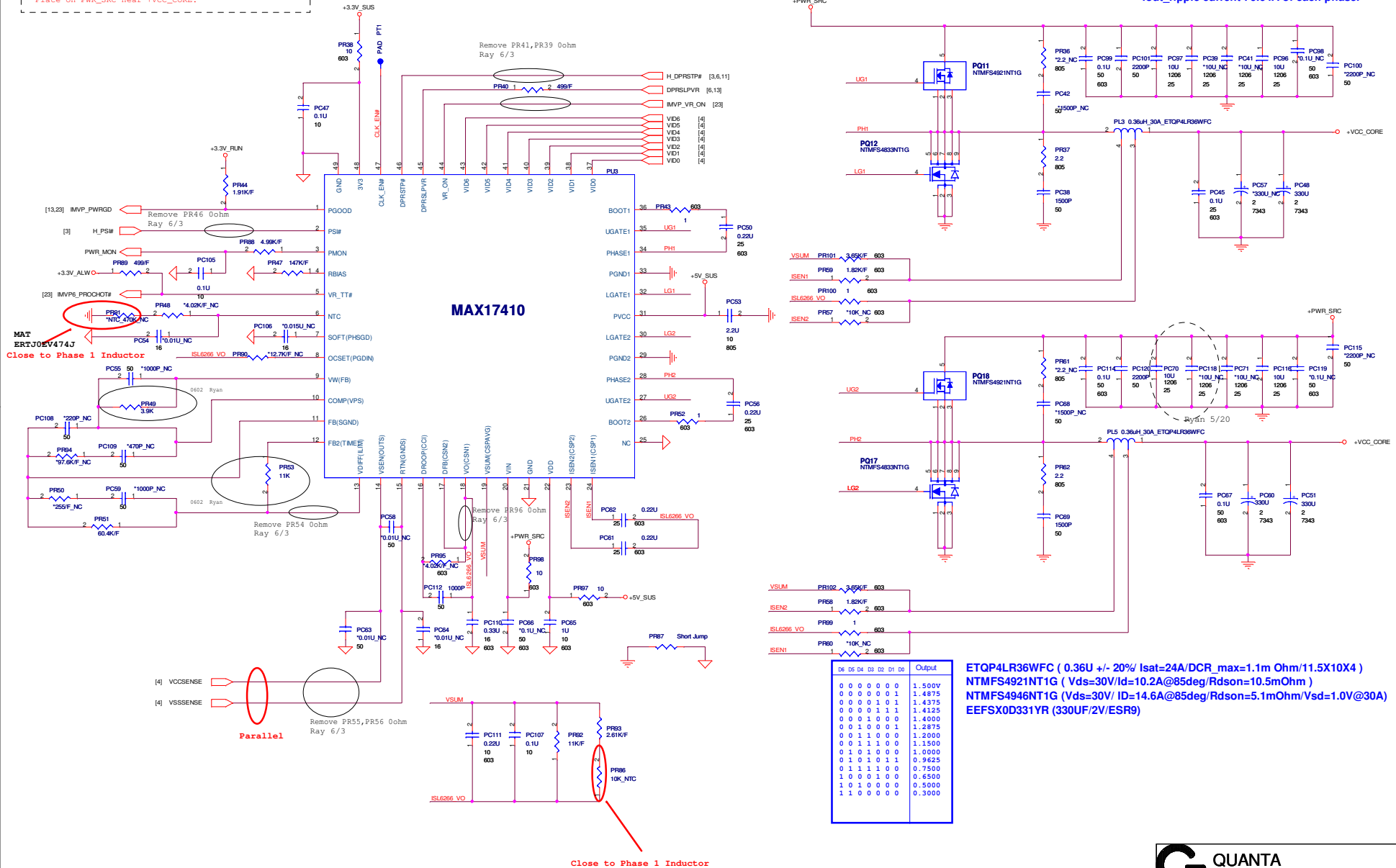
Current Limiting Setting :
 $R_{trip}(Kohm)=100*(I_{ocp}-0.5*I_{ripple})*R_{ds(on)}$

$V_{OUT} = (1+R1/R2)*0.75.$

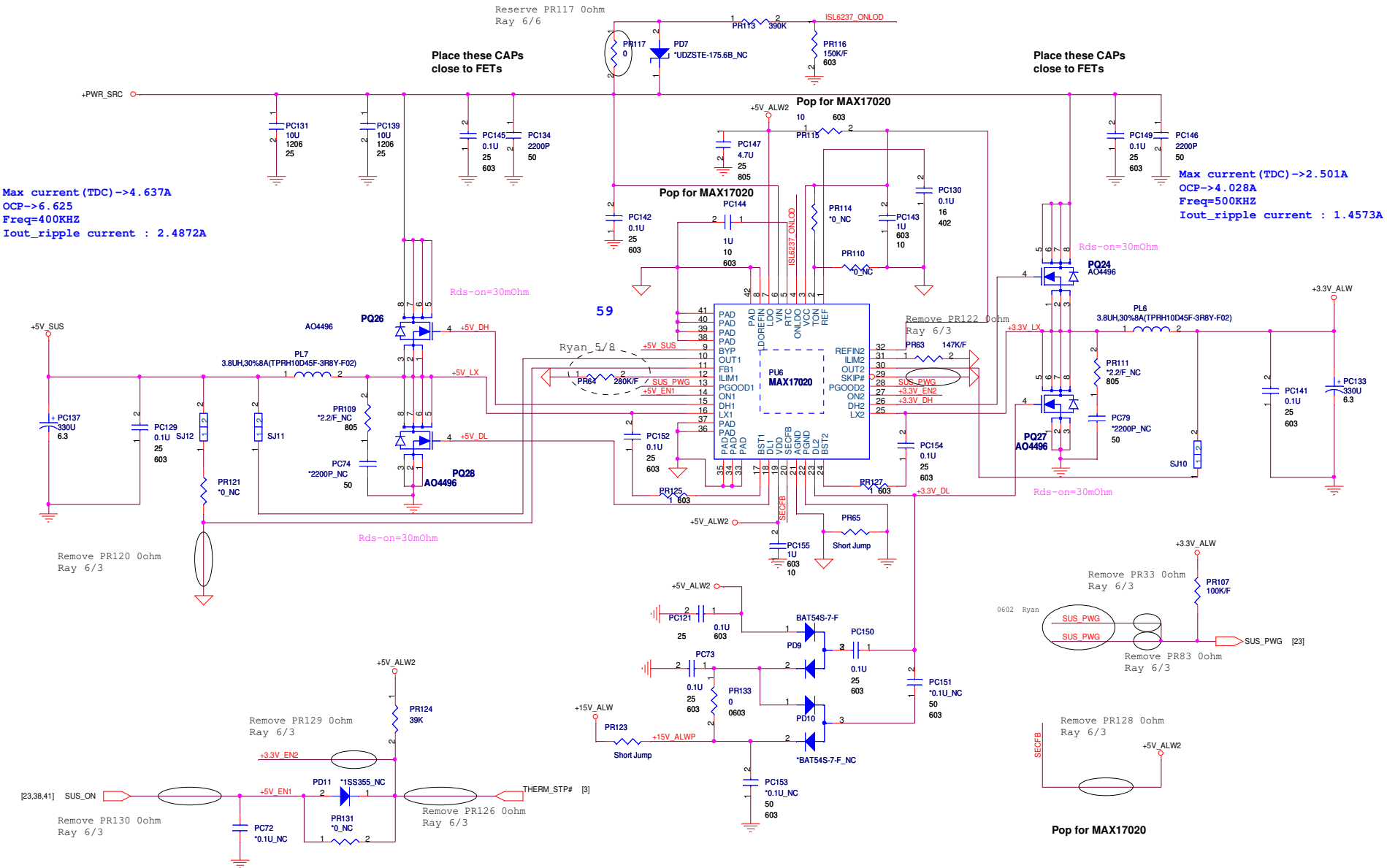
APXE2R5ARA561MF61G (560UF/2.5V/ESR16)
 SIL1055RC-1R5-R (1.5U +/- 30%/ Isat=16A/DCR_max=7.6m Ohm/10X10X5.3)
 IRF8707TRPBF (Vds=30V/Id=9.1A@75deg/Rdson=17.5mOhm)
 IRF8714TRPBF (Vds=30V/ ID=11A@70deg/Rdson=13mOhm/Vsd=1.0V@11A)



+VCC_CORE
TDC : 35A
MAX:47A
Frequency : 300KHz
Iout_ripple current : 9.64A of each phase.



DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW



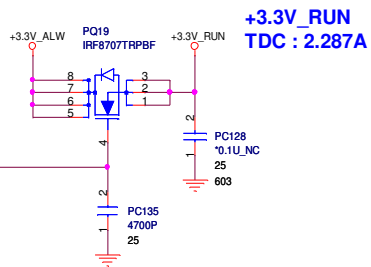
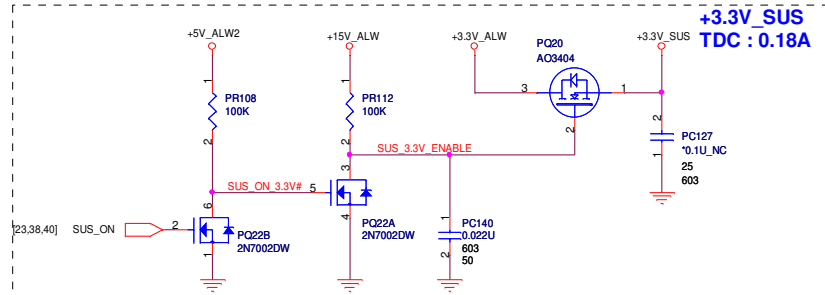
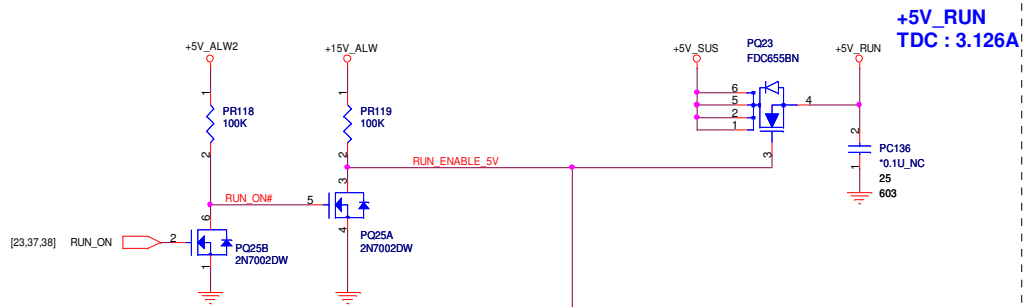
APX6R3ARA331MF61G (330UF/6.3V/ESR17)
TPC104DR-3R8Y(3.8U +/- 30%/ Isat=6A/DCR_max=12m Ohm/10X10X4)
SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm/Vsd=1.2V@2.3A)

QUANTA COMPUTER

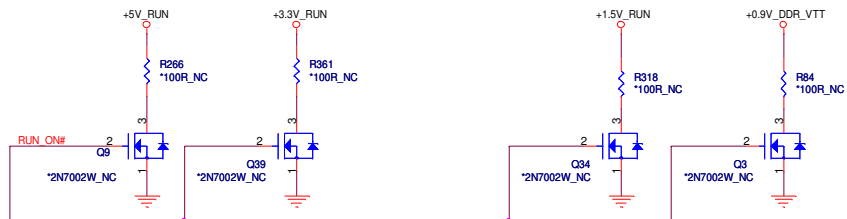
Title: 3VALW,5V,3V,(MAX17020)

Size: Document Number VMSM Rev 1A

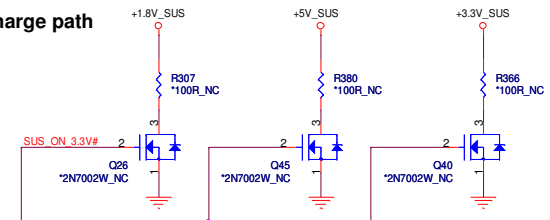
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Reserve discharge path

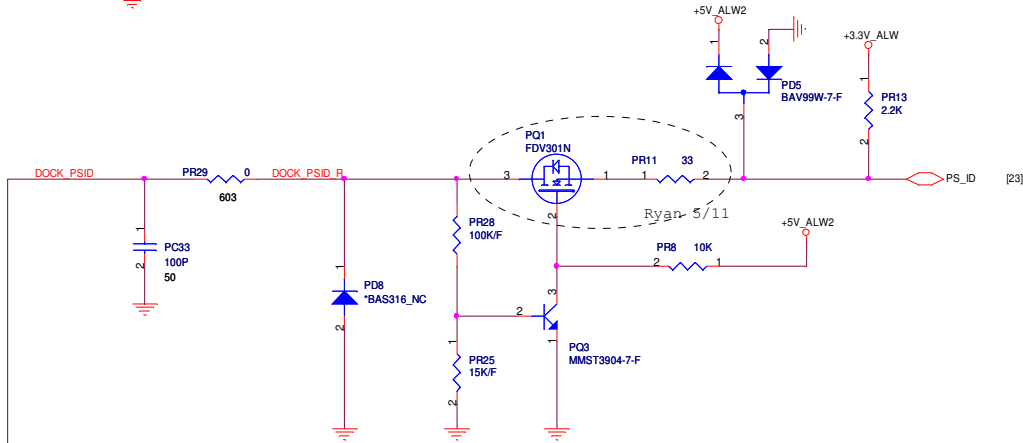
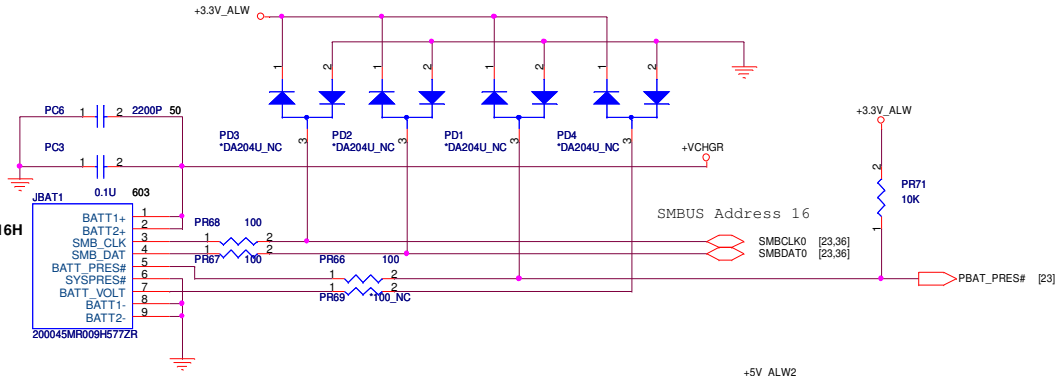


Reserve discharge path

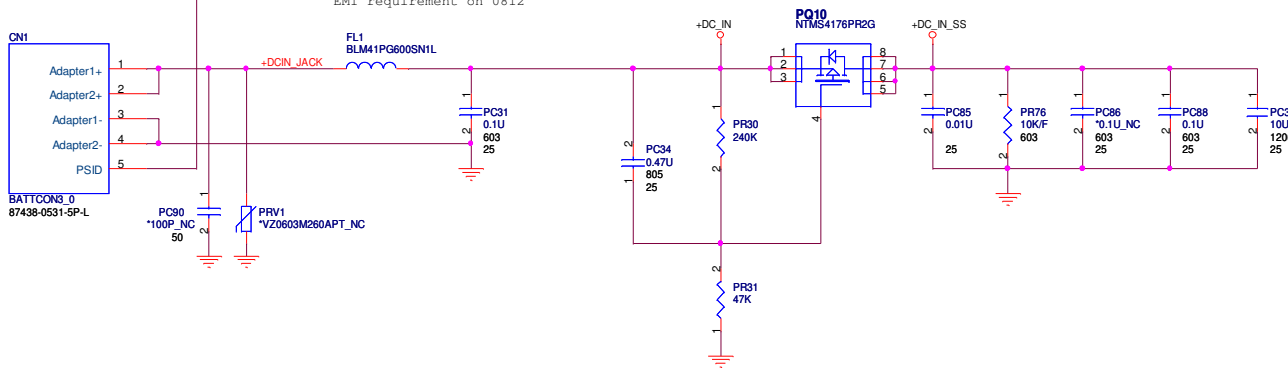


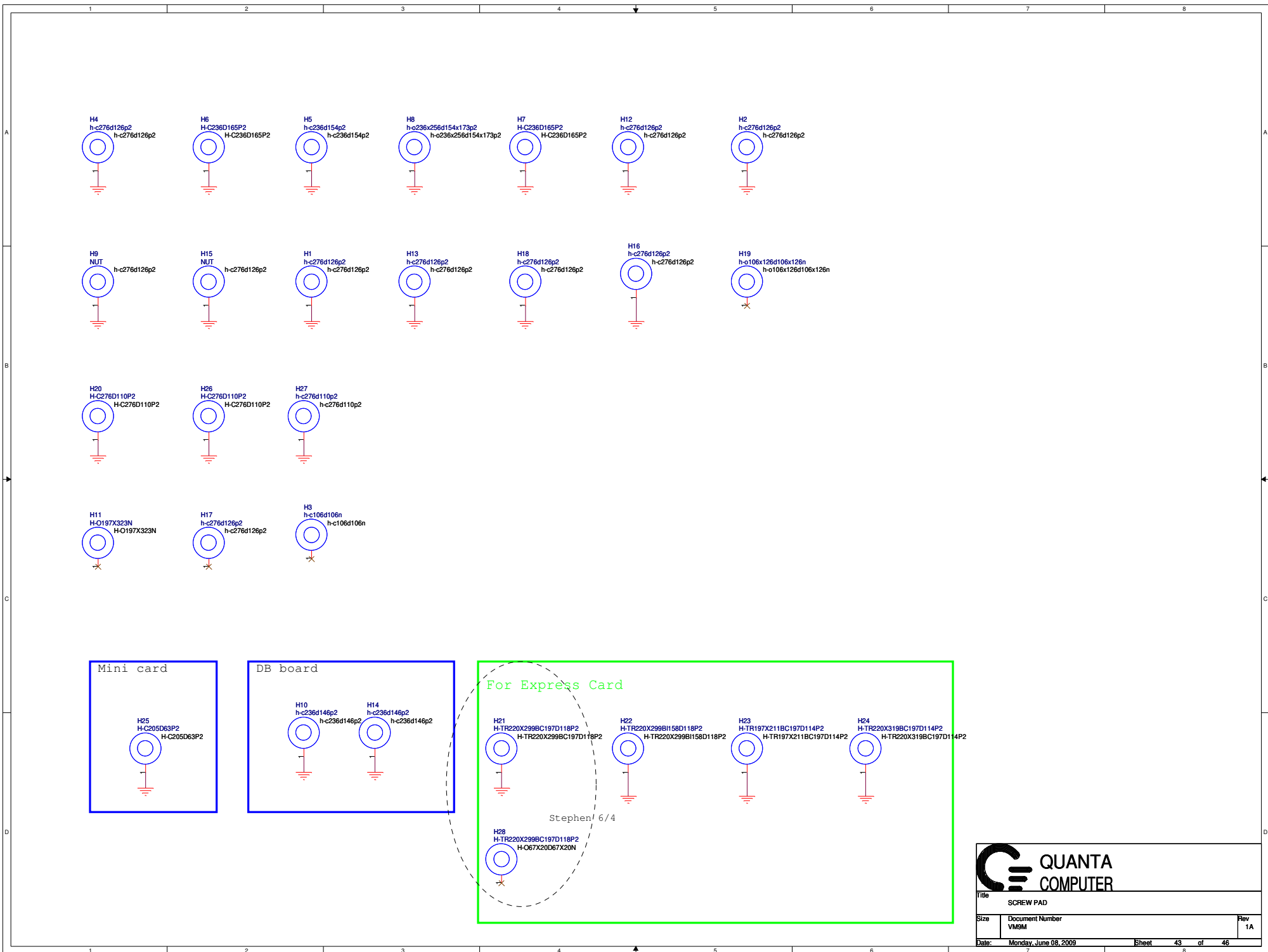
Title RUN POWER SW		
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Adress : 16H



Change Value per GG updated
EMI requirement on 0812





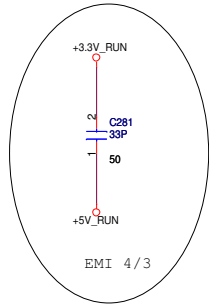
QUANTA COMPUTER


Title: SCREW PAD

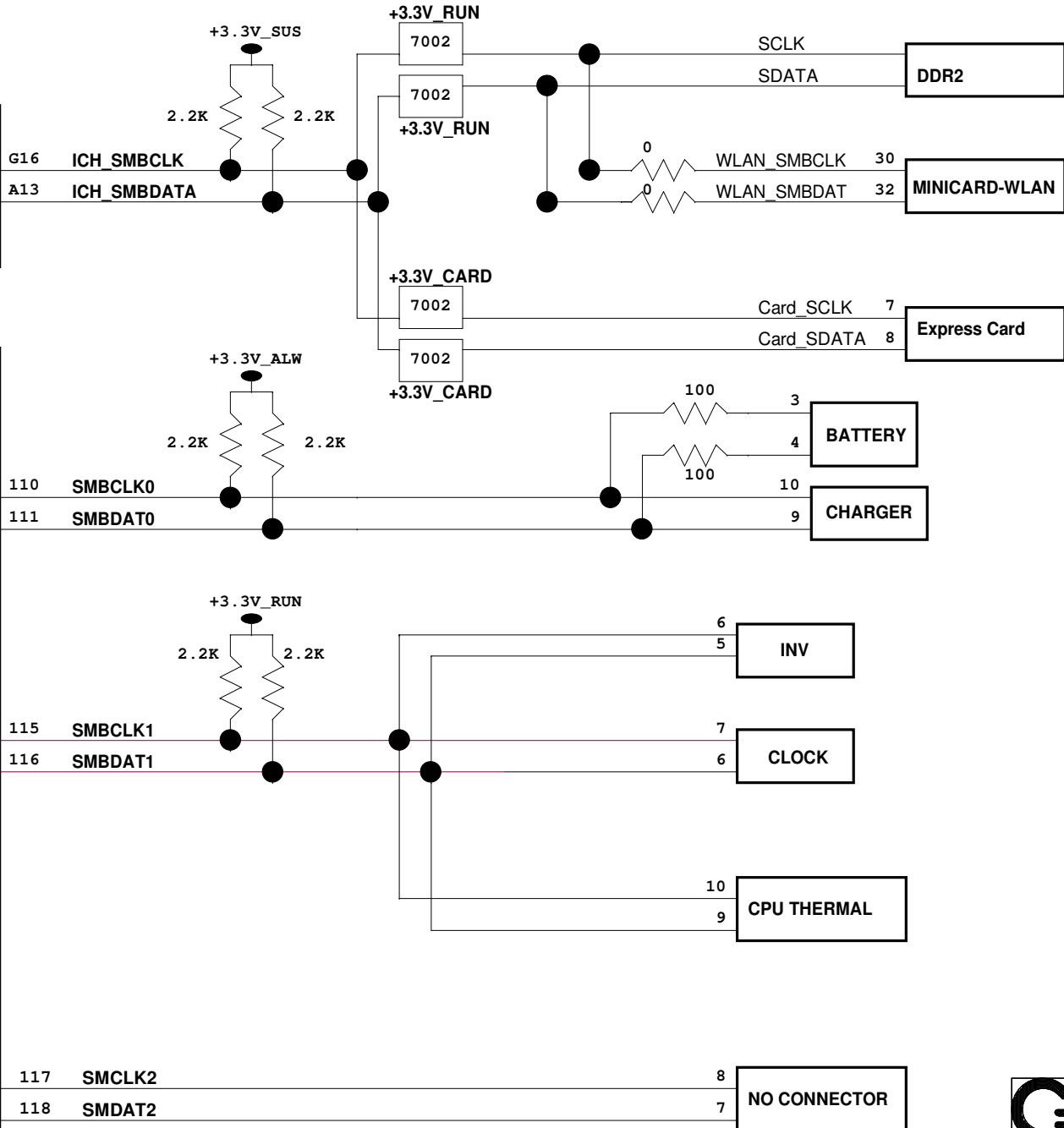
Size: VMSM	Document Number: VMSM	Rev: 1A
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Reserved for EMI.



 QUANTA COMPUTER		
Title: EMI CAP		
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Title: SMBUS BLOCK		
Size: VMSM	Document Number: VMSM	Rev: 1A
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