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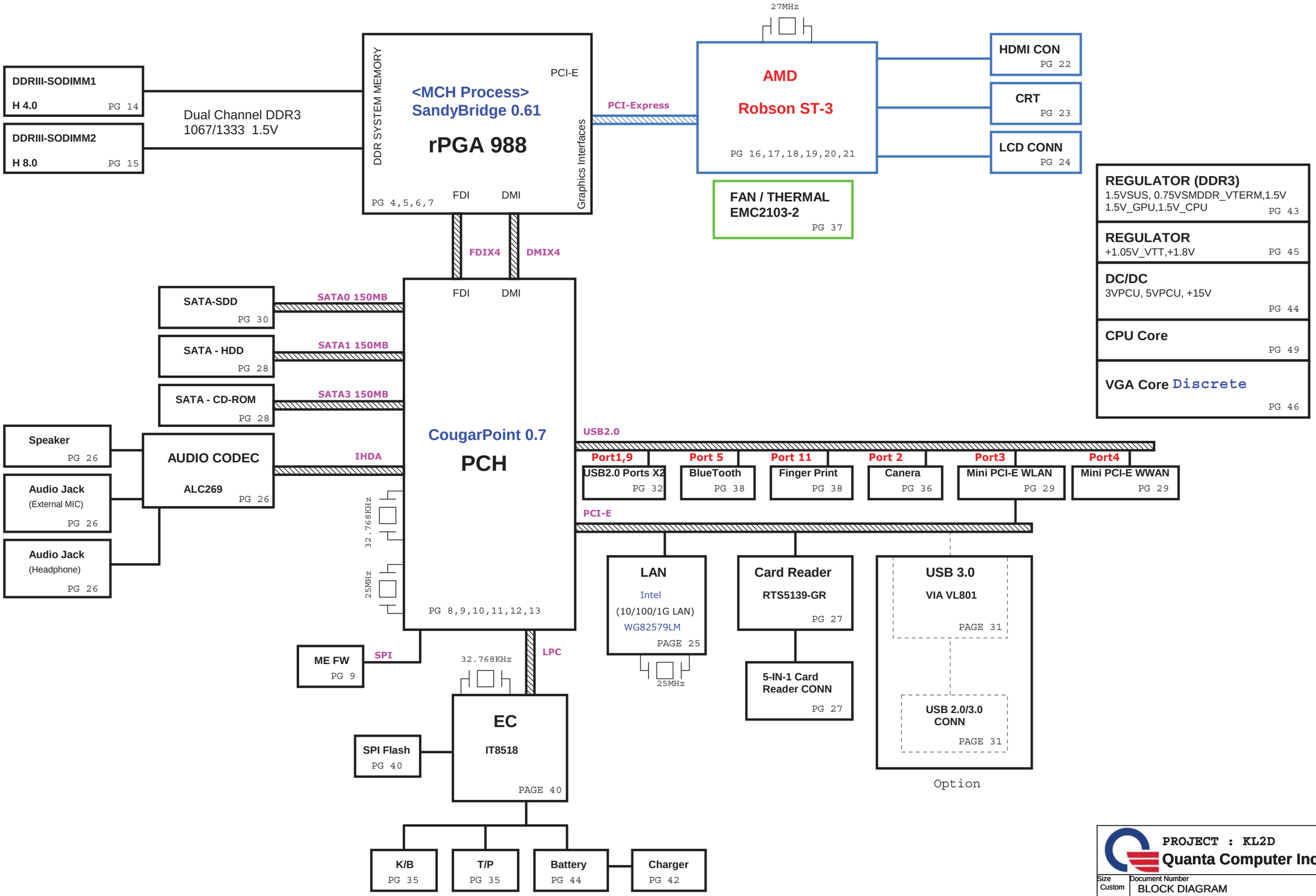
KL9A Intel Huron River Platform with AMD Discrete GFX



PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Wednesday, January 05, 2011 Sheet 1 of 52

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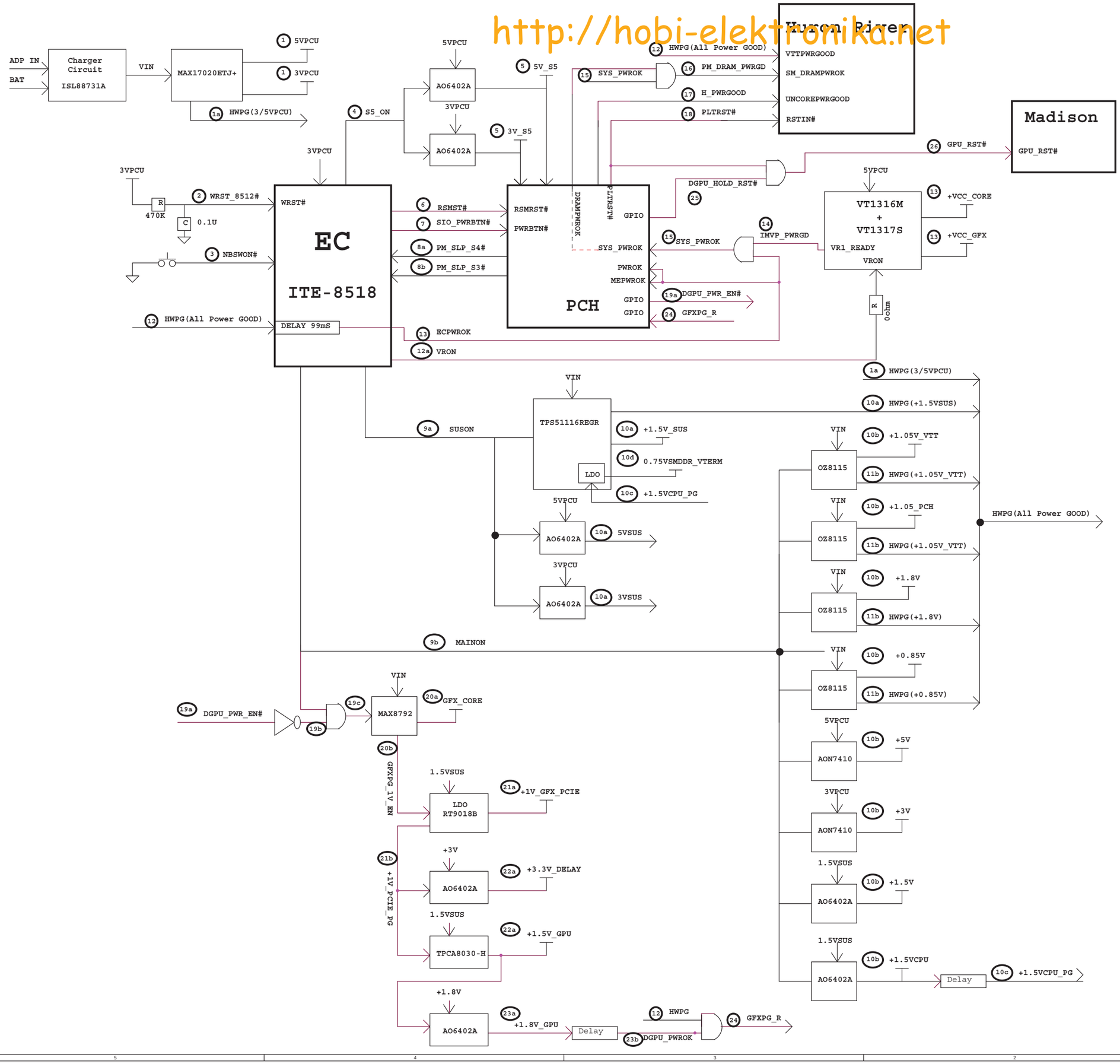

PROJECT : KL2D

Quanta Computer Inc. <Project Name>

Size	Document Number	Rev
	POWER SEQUENCE DIAGRAM	1A

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CLK Gen(CLK)

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02/20 DEL for Pre-ES1

CPU_CLK select(CLK)

02/20 DEL for Pre-ES1

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
	Clock Generator	1A

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Sandy Bridge Processor (DMI,PEG,FDI)

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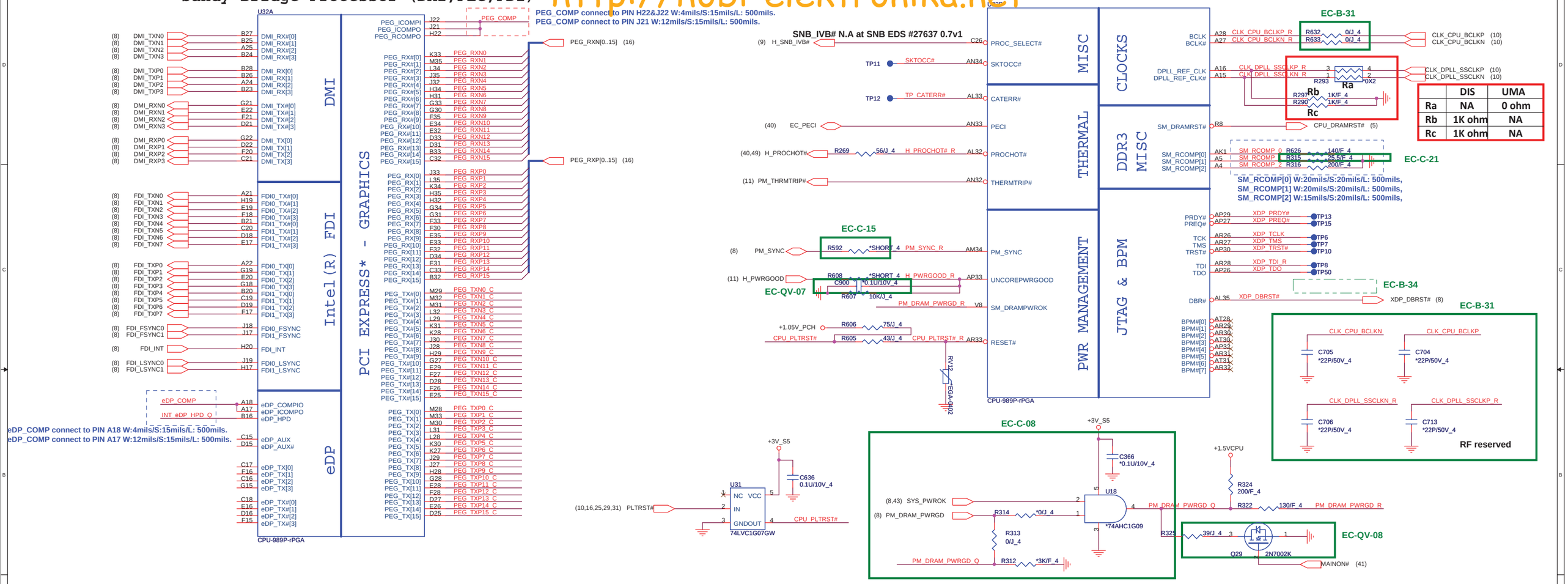
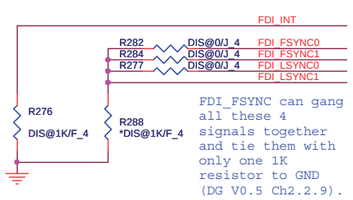
Sandy Bridge Processor (CLK,MISC,JTAG)

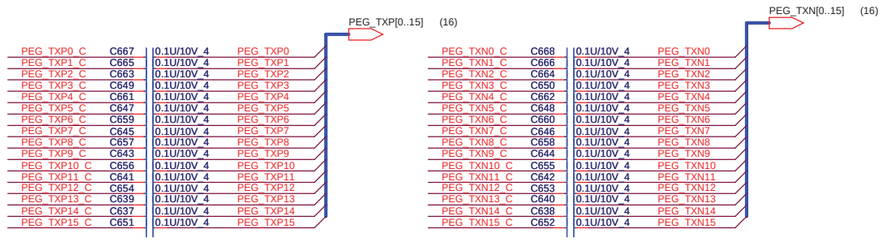


	DIS	UMA
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

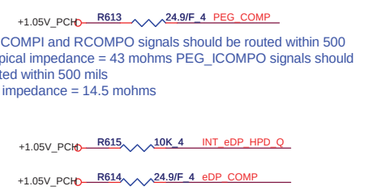
FDI Enable



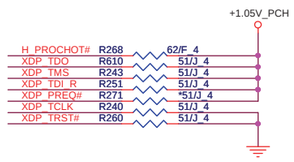
PEG x16 (UMA Non-stuff)



DP & PEG Compensation



Processor pull-up(CPU)



PROJECT : KL2D

Quanta Computer Inc.

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	Sandy Bridge 1/4	1A

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Sandy Bridge Processor (DDR3)

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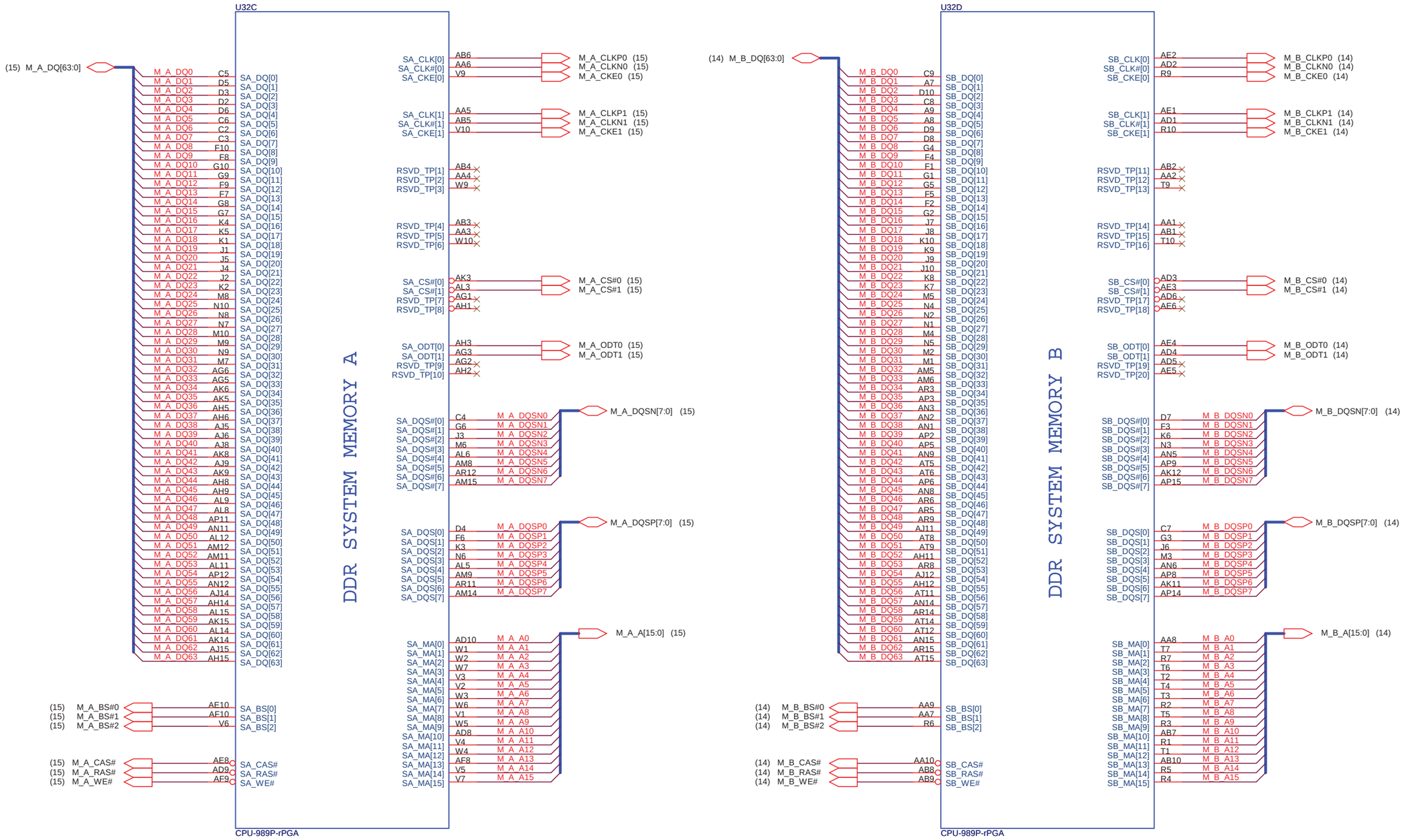

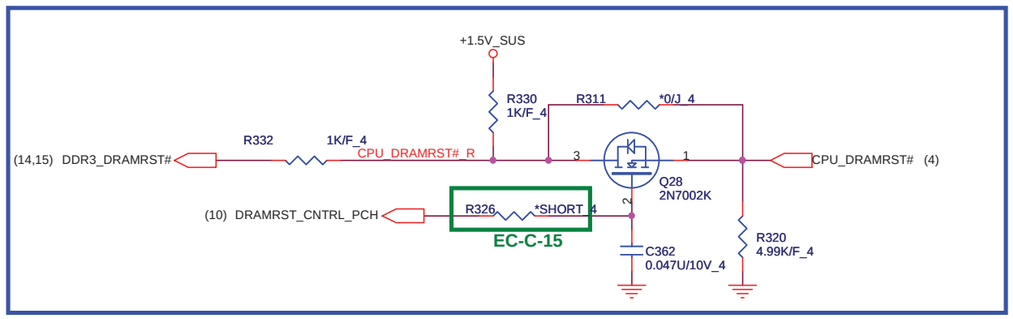

PROJECT : KL2D

Quanta Computer Inc.

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	Sandy Bridge 2/4	1A

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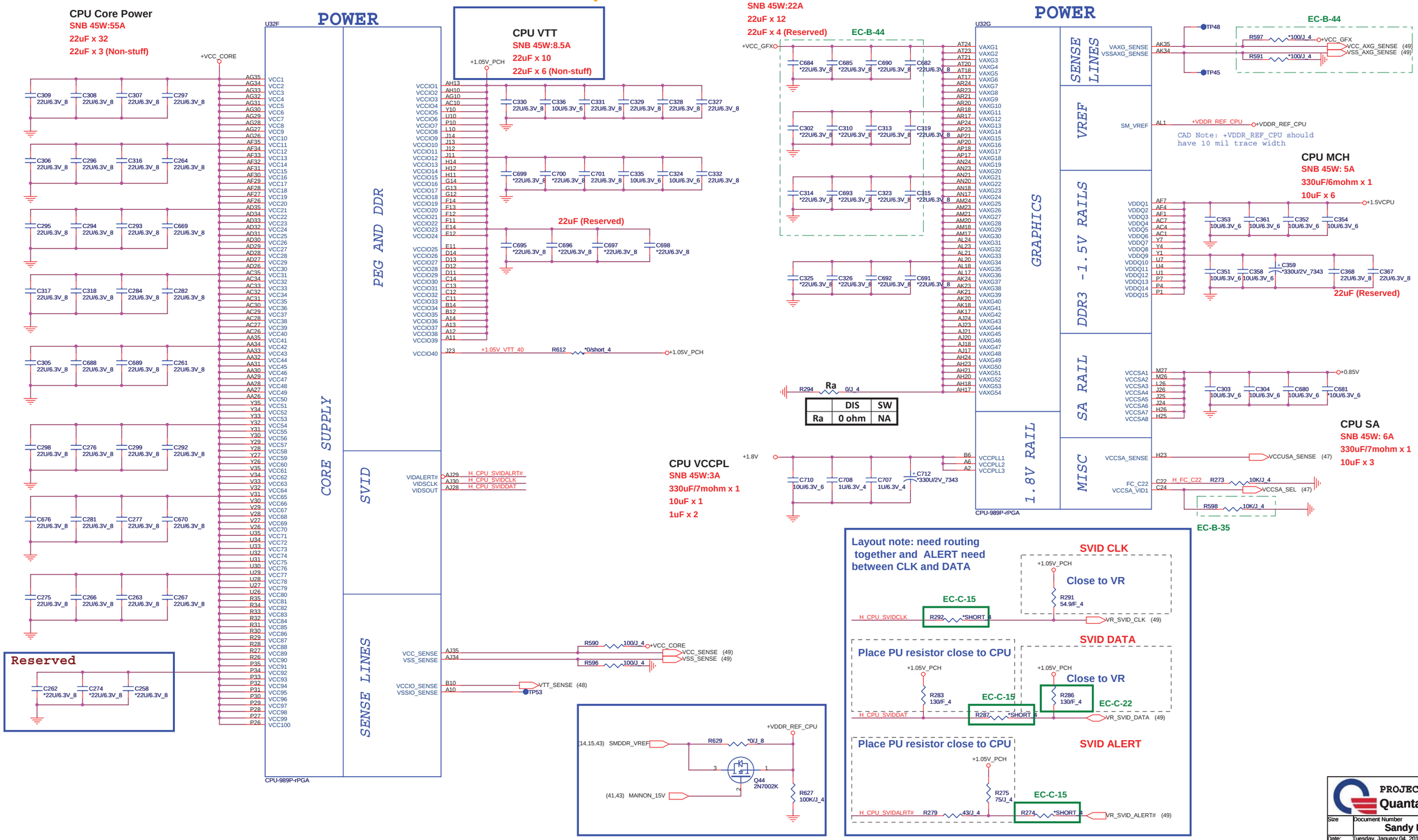

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Quanta Computer Inc.	
Size	
Document Number	Sandy Bridge 3/4
Rev	1A
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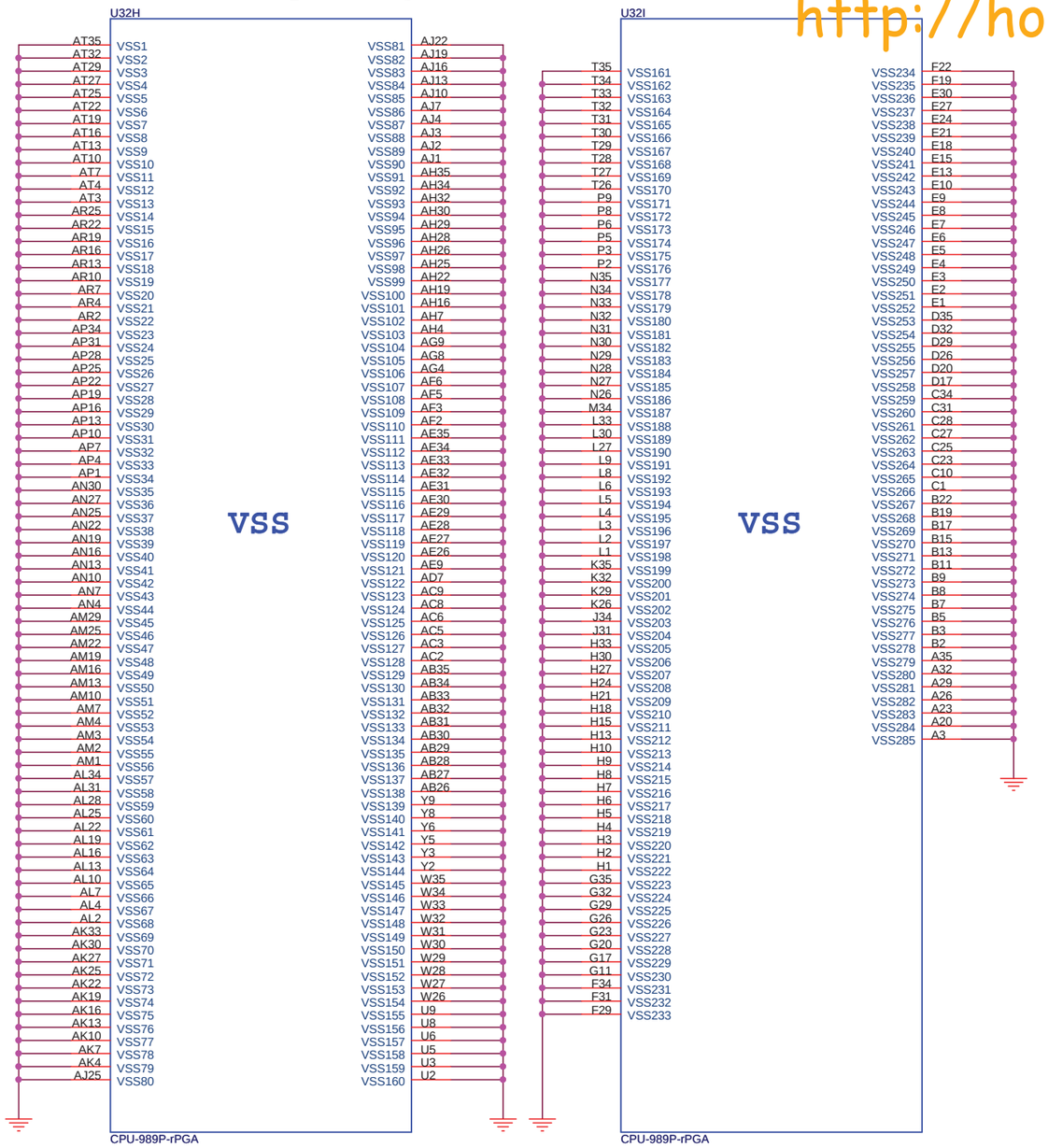
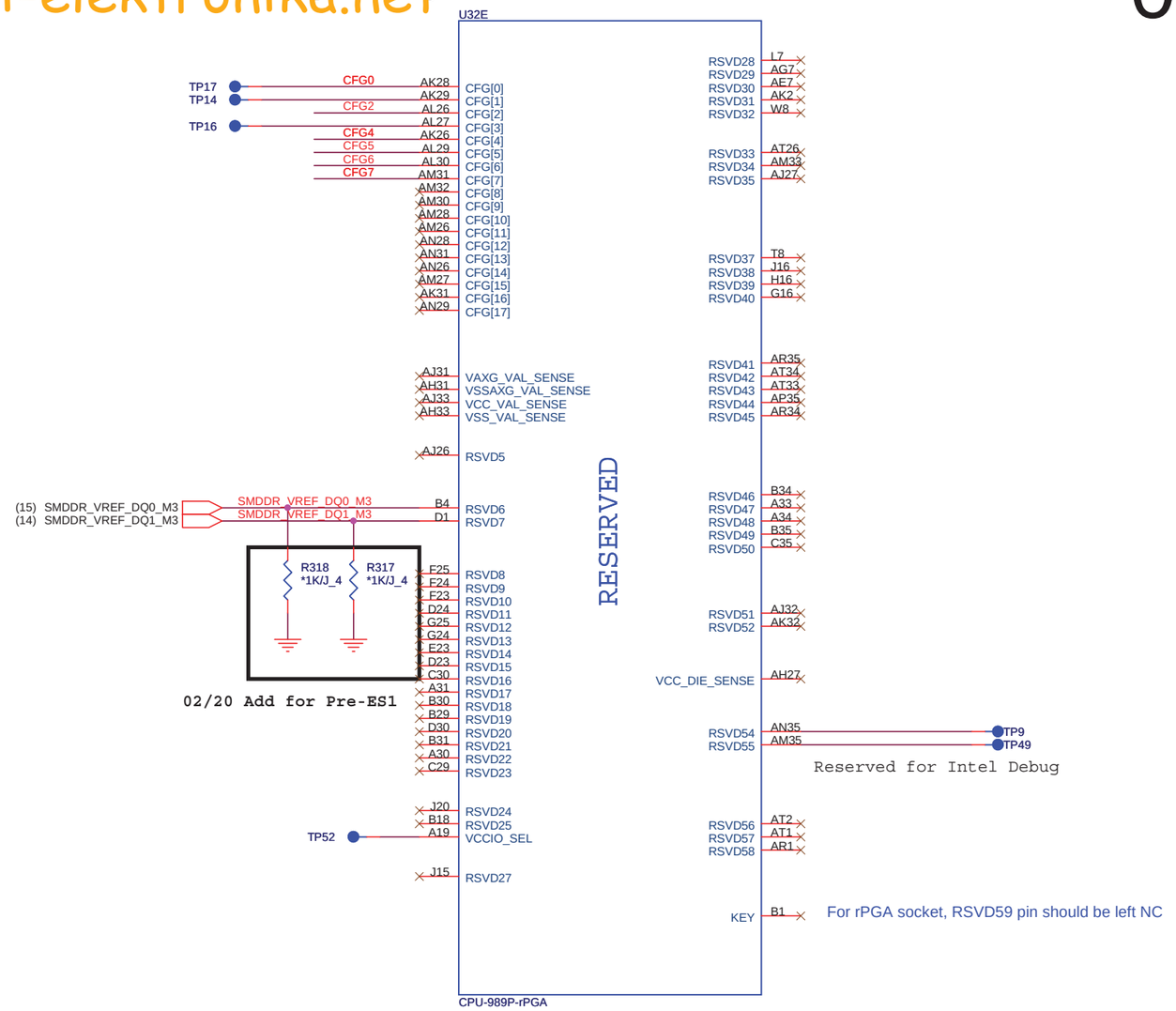
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



02/20 Add for Pre-ES1

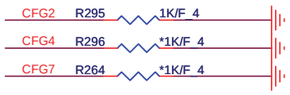
Reserved for Intel Debug

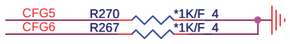
For rPGA socket, RSVD59 pin should be left NC

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : KL2D

Quanta Computer Inc.

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	Sandy Bridge 4/4	1A

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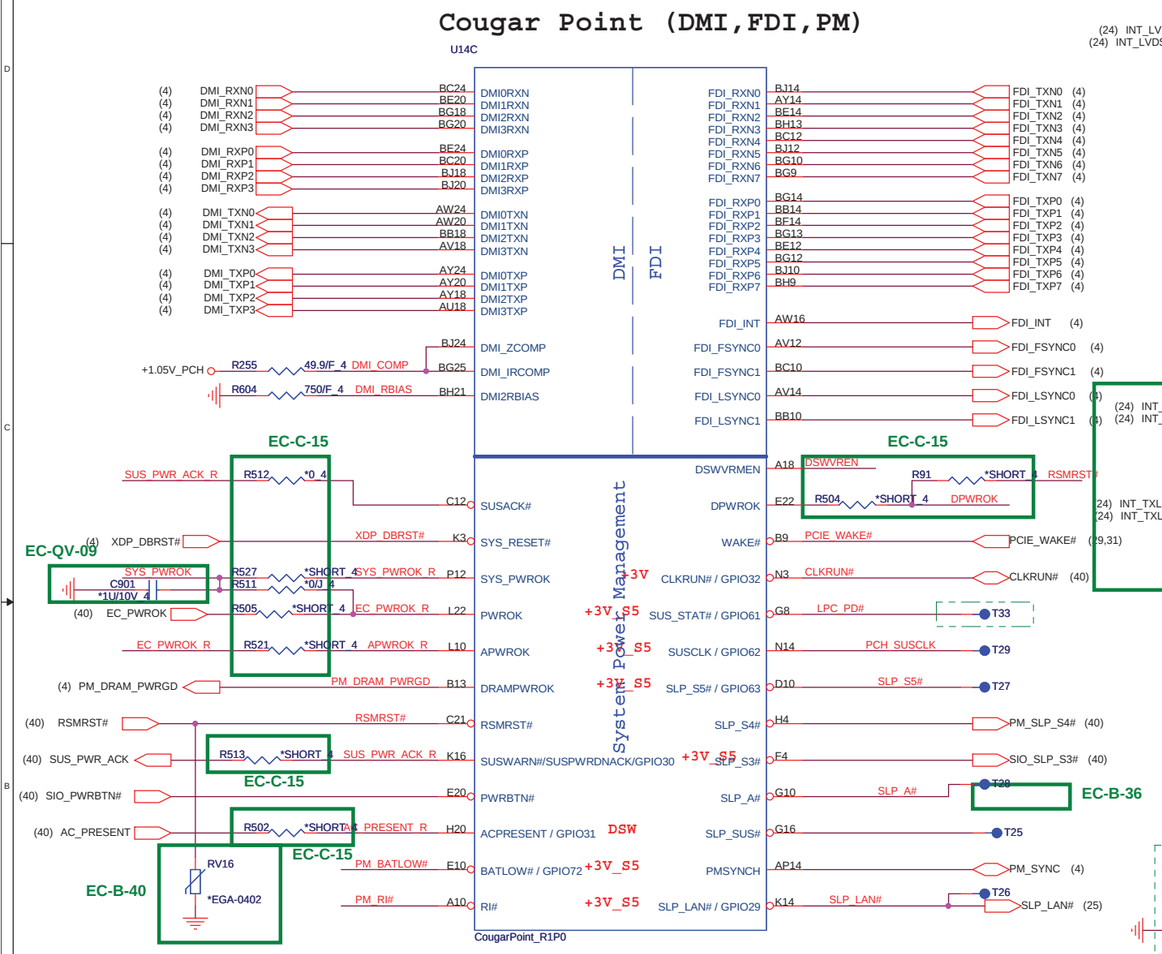
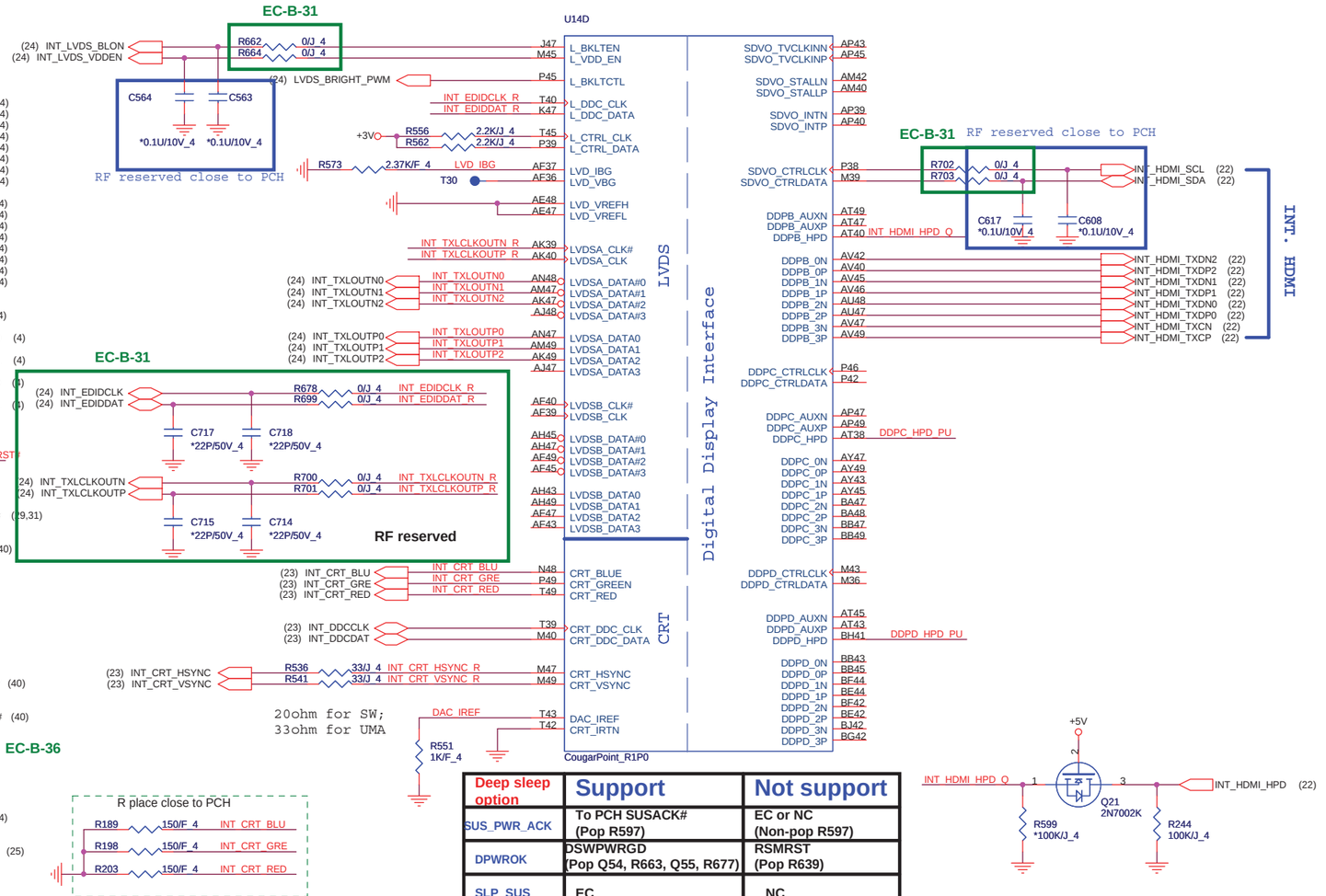
Cougar Point (DMI,FDI,PM)

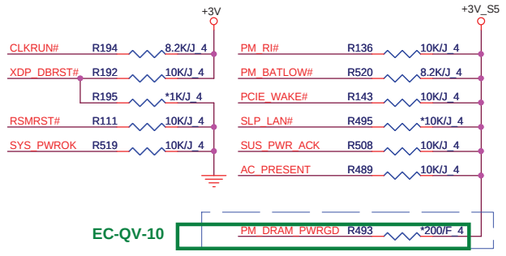


Cougar Point (LVDS,DDI)



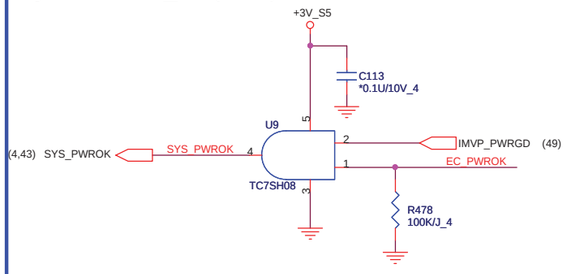
Deep sleep option	Support	Not support
SUS_PWR_ACK	To PCH SUSACK# (Pop R597)	EC or NC (Non-pop R597)
DPWROK	DSWPWRGD (Pop Q54, R663, Q55, R677)	RSMRST (Pop R639)
SLP_SUS	EC	NC

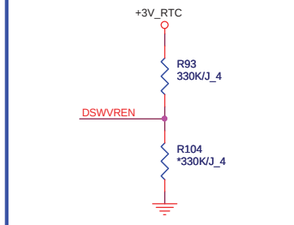
PCH Pull-high/low(CLG)



3/16 Change topology; 200ohm PU to +3V_S5

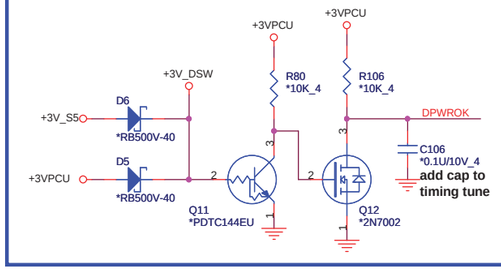
System PWR_OK(CLG)

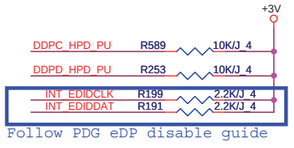




On Die DSW VR Enable
High = Enable (Default)
Low = Disable

DPWROK FOR DSW





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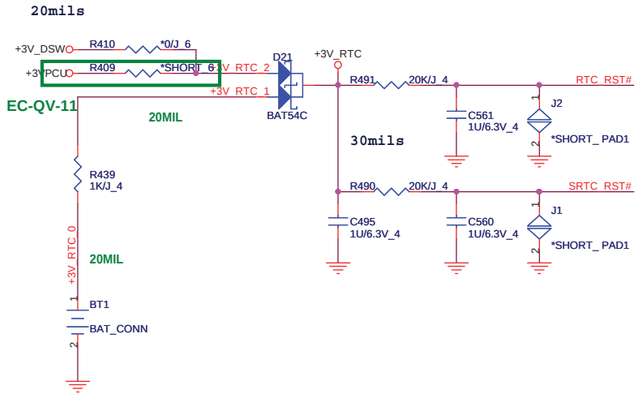
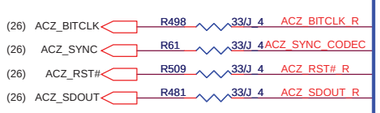
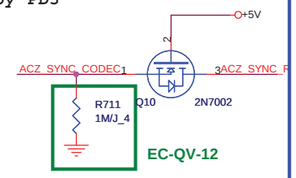
RTC Circuitry(RTC)



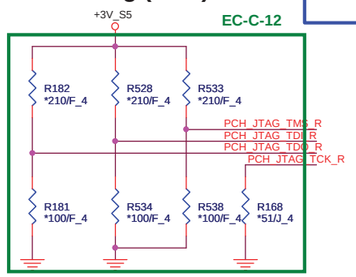
HDA Bus(CLG)



To Separate Codec Sync by PD3

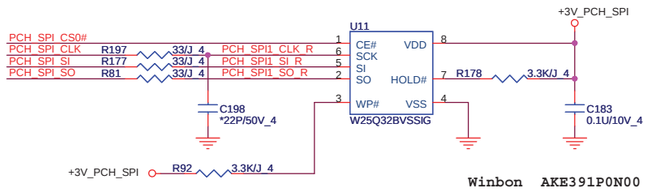


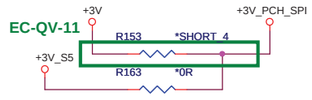
PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

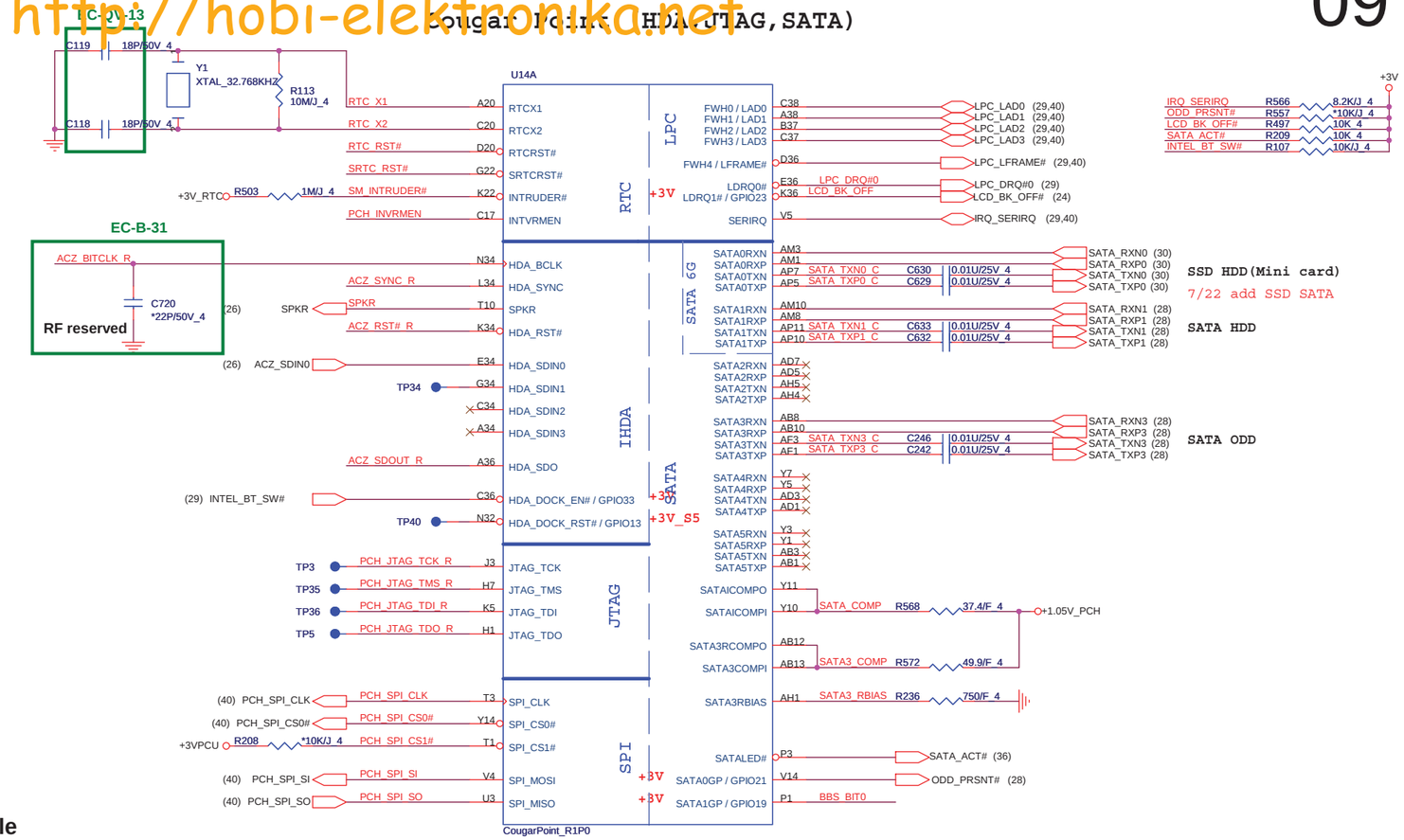
32Mbit (4M Byte), SPI





PCH2 (CLG)

CougarPoint (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R567 *1K/J_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R518 *1K/J_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R105 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] R514 *1K/J_4 BBS_BIT1 (10) R201 *1K/J_4 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R479 *1K/J_4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R249 2.2K/J_4 +1.8V R246 4.7K/J_4 DF_TVS (11) H_SNB_IVB# (4)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R547 *1K/J_4 PLL_ODVR_EN (11,40)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R75 1K/J_4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R188 *1K/J_4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

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Quanta Computer Inc.

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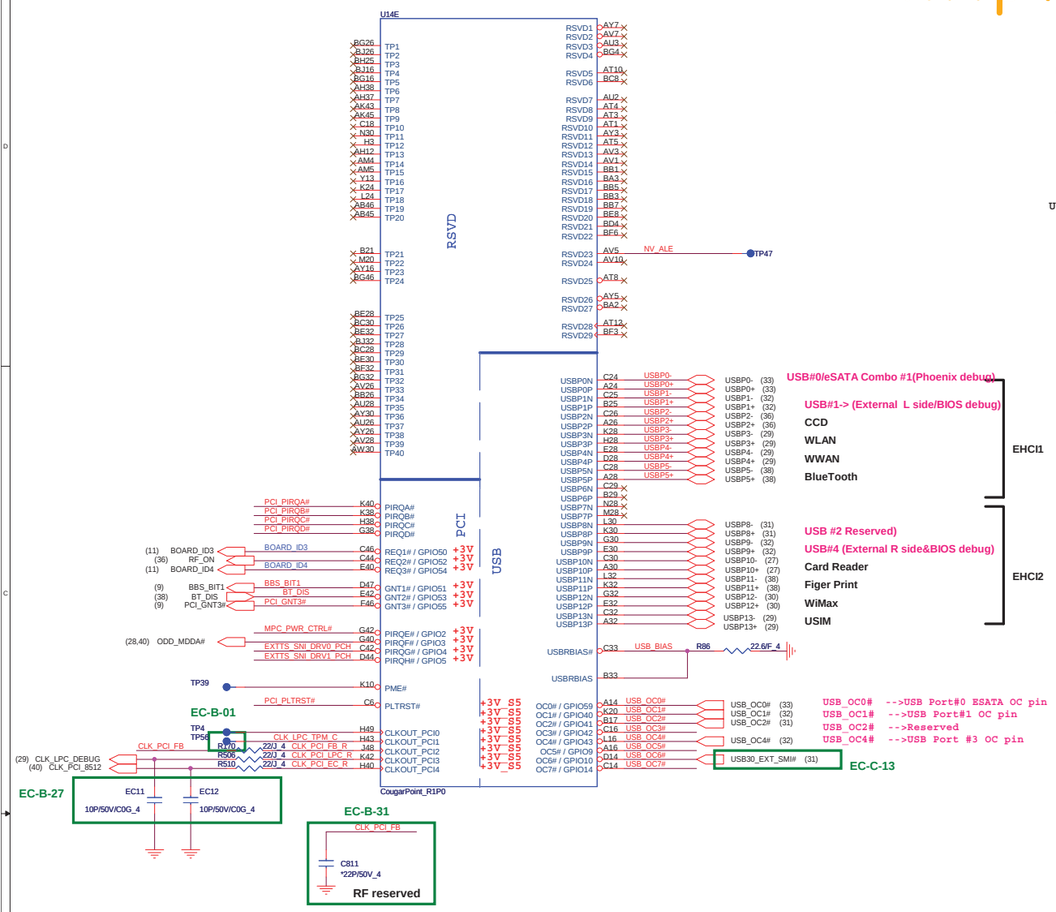
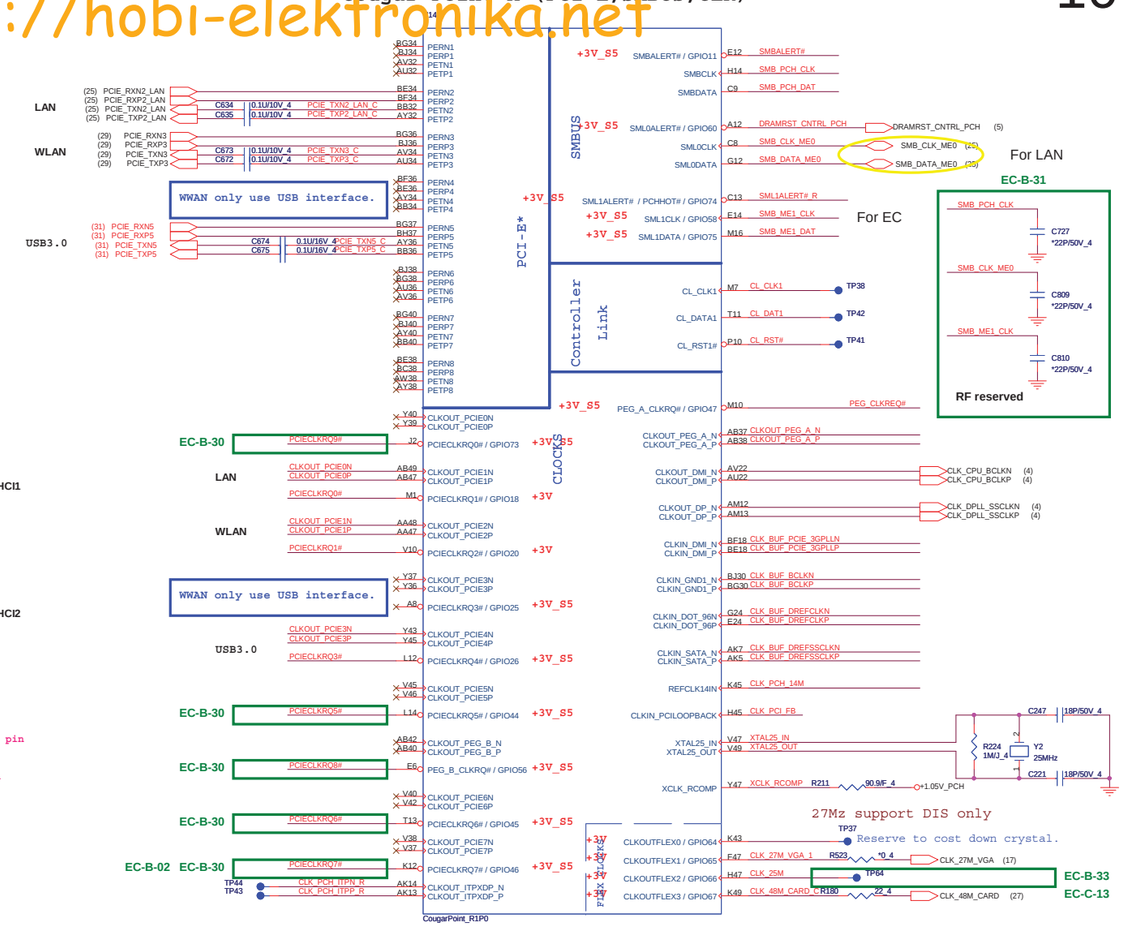
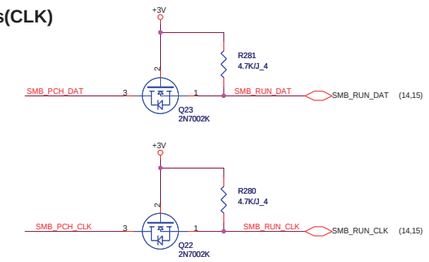
Cougar Point-M (PCI,USB,NVRAM)



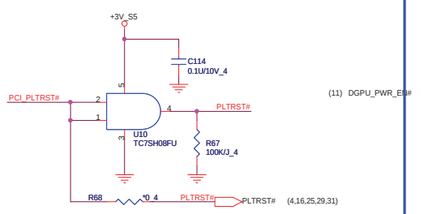
Cougar Point-M (PCI-E,SMBUS,CLK)



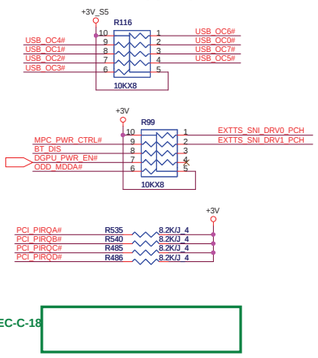
SMBus(CLK)



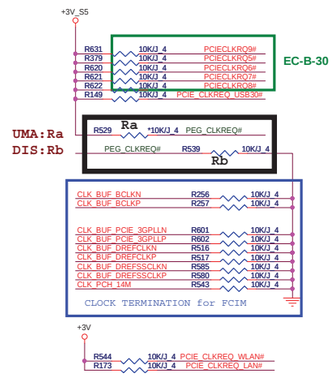
PLTRST#(CLG)



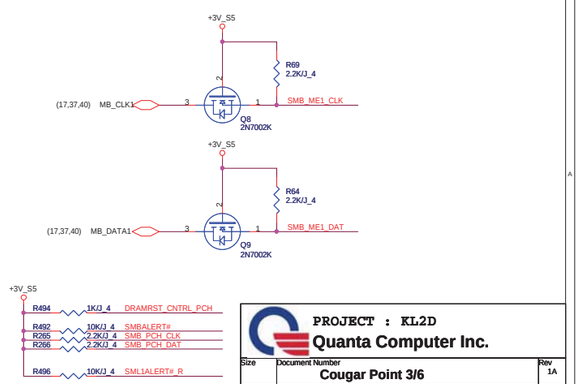
PCI/USBOC# Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



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Quanta Computer Inc.

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Cougar Point (GPIO,VSS_NCTF,REV0)

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U14F

Pin	Signal	Voltage
T7	BMBUSY# / GPIO0	+3V
A42	TACH1 / GPIO1	+3V
H36	TACH2 / GPIO6	+3V
E38	TACH3 / GPIO7	+3V
C10	GPIO8	+3V_S5
C4	LAN_PHY_PWR_CTRL / GPIO12	+3V_S5
G2	GPIO15	+3V_S5
U2	SATA4GP / GPIO16	+3V
D40	TACH0 / GPIO17	+3V
T5	SCLOCK / GPIO22	+3V
E8	GPIO24 / MEM_LED	+3V_S5
E16	GPIO27	DSW
P8	GPIO28	+3V_S5
K1	STP_PCI# / GPIO34	+3V
K4	GPIO35	+3V
V8	SATA2GP / GPIO36	+3V
M5	SATA3GP / GPIO37	+3V
N2	SLOAD / GPIO38	+3V
M3	SDATAOUT0 / GPIO39	+3V
V13	SDATAOUT1 / GPIO48	+3V
V3	SATA5GP / GPIO49	+3V
D6	GPIO57	+3V_S5
C40	TACH4 / GPIO68	+3V
B41	TACH5 / GPIO69	+3V
C41	TACH6 / GPIO70	+3V
A40	TACH7 / GPIO71	+3V
P4	A20GATE	
AU16	PECI	
P5	RCIN#	
AY11	PROCPWRGD	
AY10	THRMTRIP#	
T14	INIT3_3V#	
AY1	DF_TVS	
AH8	TS_VSS1	
AK11	TS_VSS2	
AH10	TS_VSS3	
AK10	TS_VSS4	
P37	NC_1	
BG2	VSS_NCTF_15	
BG48	VSS_NCTF_16	
BH3	VSS_NCTF_17	
BH47	VSS_NCTF_18	
BJ4	VSS_NCTF_19	
BJ44	VSS_NCTF_20	
BJ45	VSS_NCTF_21	
BJ46	VSS_NCTF_22	
BJ5	VSS_NCTF_23	
BJ6	VSS_NCTF_24	
C2	VSS_NCTF_25	
C48	VSS_NCTF_26	
D1	VSS_NCTF_27	
D49	VSS_NCTF_28	
E1	VSS_NCTF_29	
E49	VSS_NCTF_30	
F1	VSS_NCTF_31	
F49	VSS_NCTF_32	
A4	VSS_NCTF_1	
A44	VSS_NCTF_2	
A45	VSS_NCTF_3	
A46	VSS_NCTF_4	
A5	VSS_NCTF_5	
A6	VSS_NCTF_6	
B3	VSS_NCTF_7	
B47	VSS_NCTF_8	
BD1	VSS_NCTF_9	
BD49	VSS_NCTF_10	
BE1	VSS_NCTF_11	
BF49	VSS_NCTF_12	
BF1	VSS_NCTF_13	
BF49	VSS_NCTF_14	

GPIO CPU/MISC NCTF

CougarPoint_R1P0

S_GPIO R553 100_4 T7
(40) EC_EXT_SMI# EC_EXT_SMI# A42
BOARD_ID0 EC-B-03 H36
(40) EC_EXT_SCI# EC_EXT_SCI# E38
SYSTEM_ID C10
(25) LAN_DISABLE# LAN_DISABLE# C4
HOST_ALERT#1_R G2
EC-B-04 (29) WLAN_OFF# U2
DGPU_PWROK DGPU_PWROK D40
+3V Follow DMRB4, need check
BIOS_REC T5
R542 *10K
(30) SDD_DA_DSS SDD_DA_DSS E8
GPIO27 E16
(9,40) PLL_ODVR_EN R546 *0/J_4 PLL_ODVR_EN_R P8
STP_PCI# K1
(38) BT_ON# BT_ON# K4
(10) DGPU_PWR_EN# V8
Need check EC-B-04 EC-C-19 (29) WWAN_OFF# M5
MFG_MODE N2
FDI_OVRVLTG M3
TEST_SET_UP V13
(37,40) TEMP_ALERT# V3
SV_DET D6

BOARD_ID1 EC-B-03 C40
T24 B41
SSD_DETECT# (30) C41
BOARD_ID2 A40
EC_A20GATE (40) P4
TP46 AU16
EC_RCIN# P5 EC_RCIN# (40)
H_PWRGOOD (4) AY11
PCH_THRMTRIP# R595 390/J_4 PM_THRMTRIP# (4) AY10
DF_TVS (9) AY1

3/16 Connected to GND
DG rev0.9

GPIO Pull-up/Pull-down(CLG)

+3V_S5
LAN_DISABLE# R157 10K/J_4

+3V
EC_EXT_SMI# R89 10K/J_4
EC_EXT_SCI# R487 10K/J_4
SSD_DETECT# R110 10K/J_4
STP_PCI# R193 10K/J_4
EC_A20GATE R550 10K/J_4
EC_RCIN# R549 10K/J_4
TEMP_ALERT# R217 10K/J_4
BT_ON# R537 10K/J_4
DGPU_PWROK R500 10K/J_4
EC-B-04 WLAN_OFF# R530 10K/J_4

GPIO27 R515 10K/J_4

	GPIO71	GPIO68	GPIO6
	BOARD_ID2	BOARD_ID1	BOARD_ID0
KL7	0	0	0
KL8	0	1	0
KL9	1	0	0
KL8A	0	1	1
KL9A	1	0	1

EC-B-05

+3V
R108 *10K/J_4 BOARD_ID0 R87 10K/J_4
R488 10K/J_4 BOARD_ID1 R480 *10K/J_4
R109 *10K/J_4 BOARD_ID2 R88 10K/J_4
R507 10K/J_4 BOARD_ID3 R501 *10K/J_4
R483 10K/J_4 BOARD_ID4 R484 *10K/J_4
R142 10K/J_4 SYSTEM_ID R144 *10K/J_4

(10) BOARD_ID3 BOARD_ID3
(10) BOARD_ID4 BOARD_ID4

SV_SET_UP
High = Strong (Default)

+3V
TEST_SET_UP R559 10K/J_4 R565 *0/J_4

+3V_S5 EC-QV-03
R526 *10K/J_4 SV_DET R524 100K/J_4

+3V_S5
HOST_ALERT#1_R R525 1K/J_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

SGPIO

+3V
S_GPIO R560 10K/J_4 R561 *0/J_4

+3V
R548 100K/J_4 FDI_OVRVLTG R545 *1K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

+3V
SDD_DA_DSS R681 *200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V
BIOS_REC R564 10K/J_4 R558 *0/J_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

+3V
MFG_MODE R202 10K/J_4 R200 *0/J_4

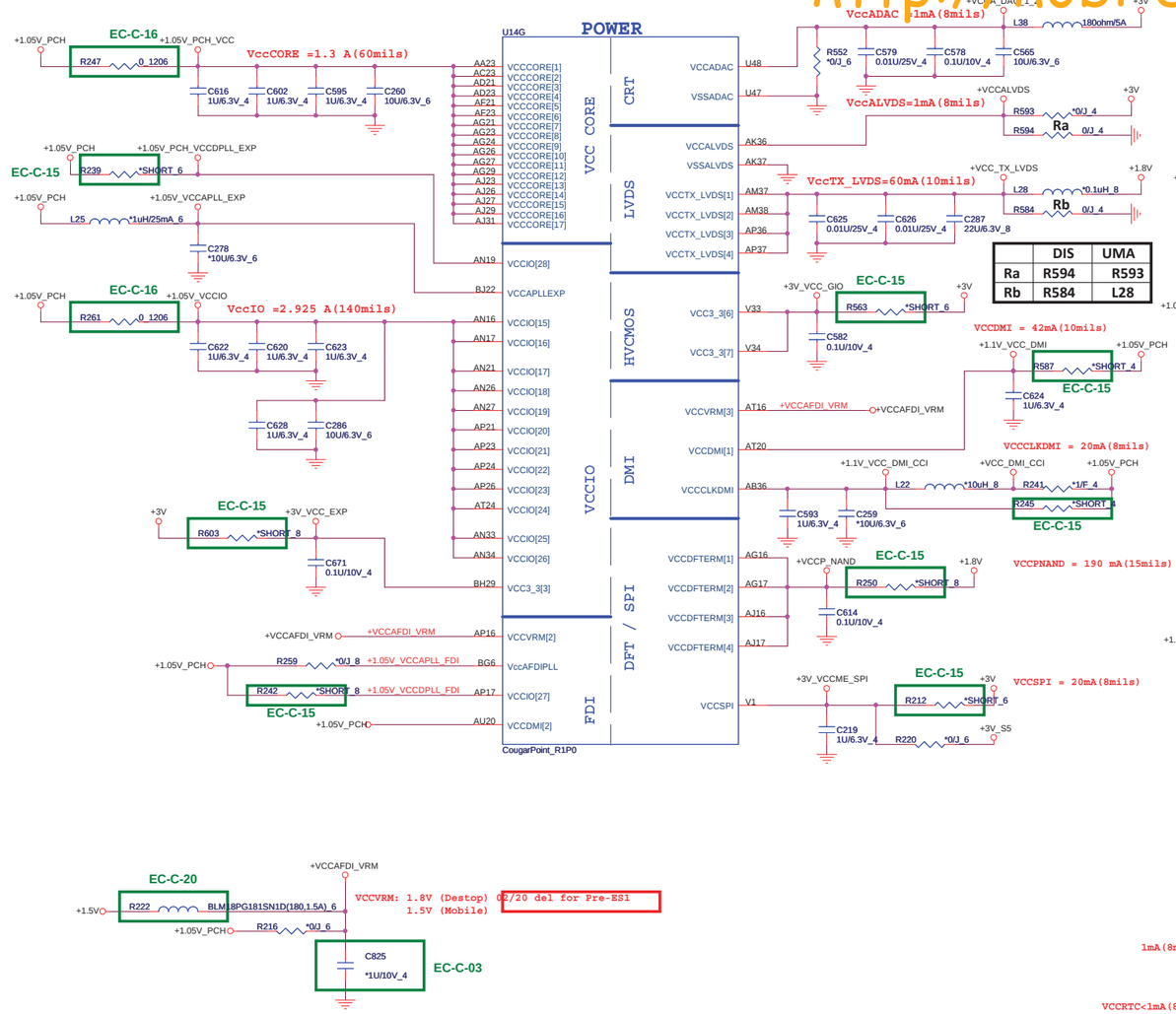
PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
	Cougar Point 4/6	1A

Date: Tuesday, January 04, 2011 Sheet 11 of 53

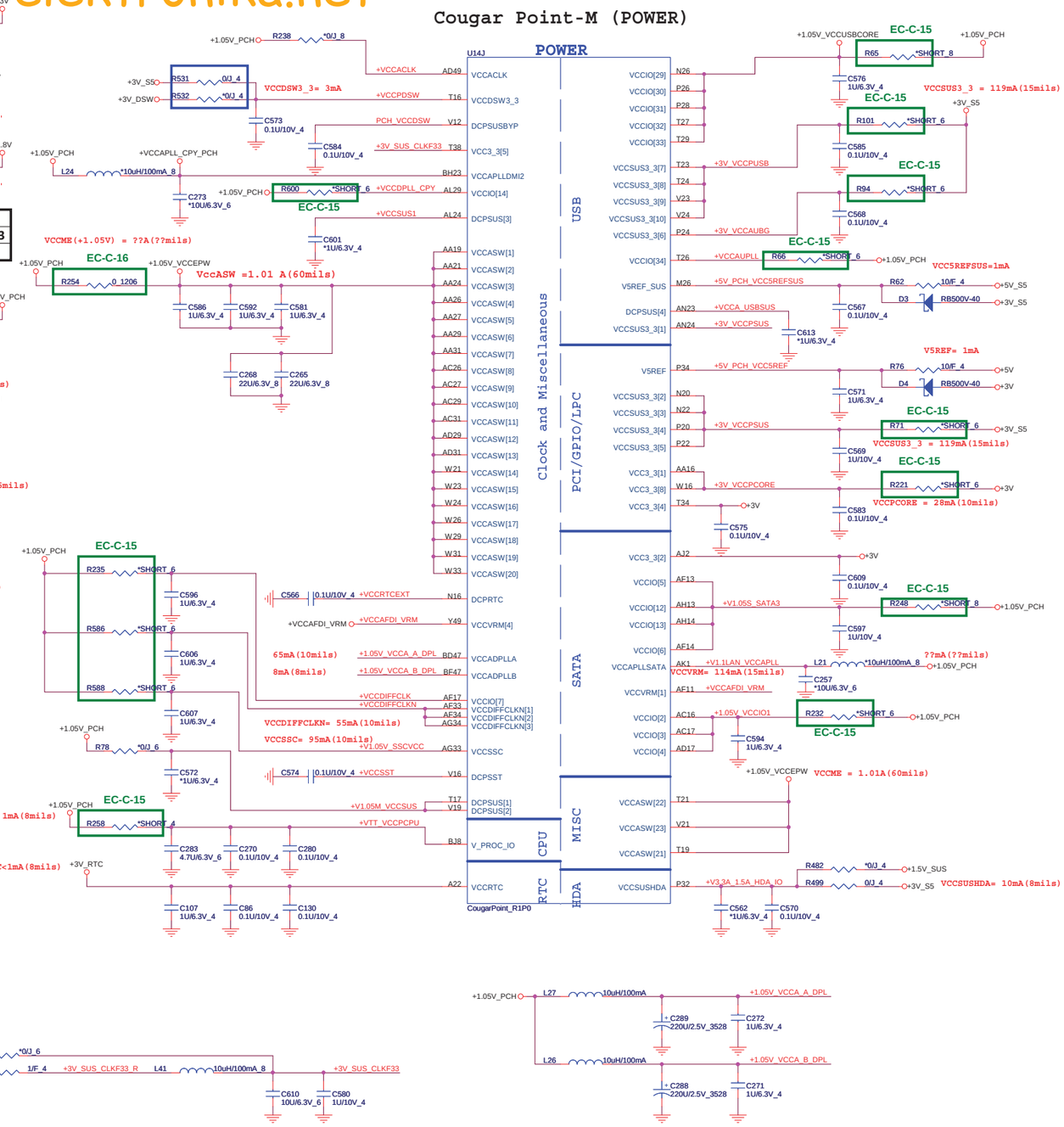
COUGAR POINT (POWER)

http://hobi-elektronika.net



	DIS	UMA
Ra	R594	R593
Rb	R584	L28

Cougar Point-M (POWER)



PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
	Cougar Point 5/6	1A

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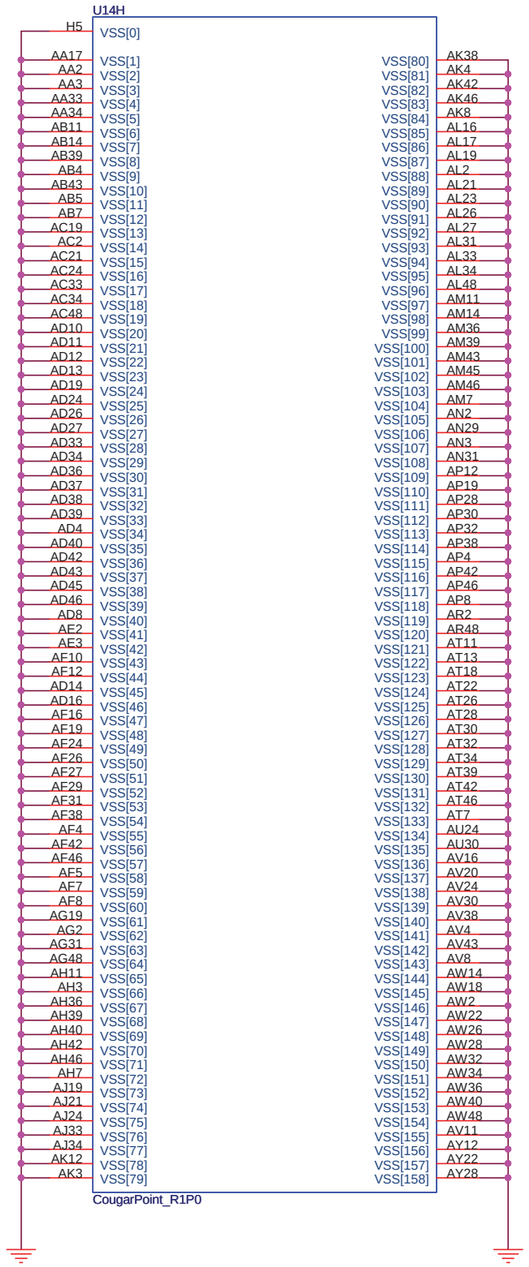
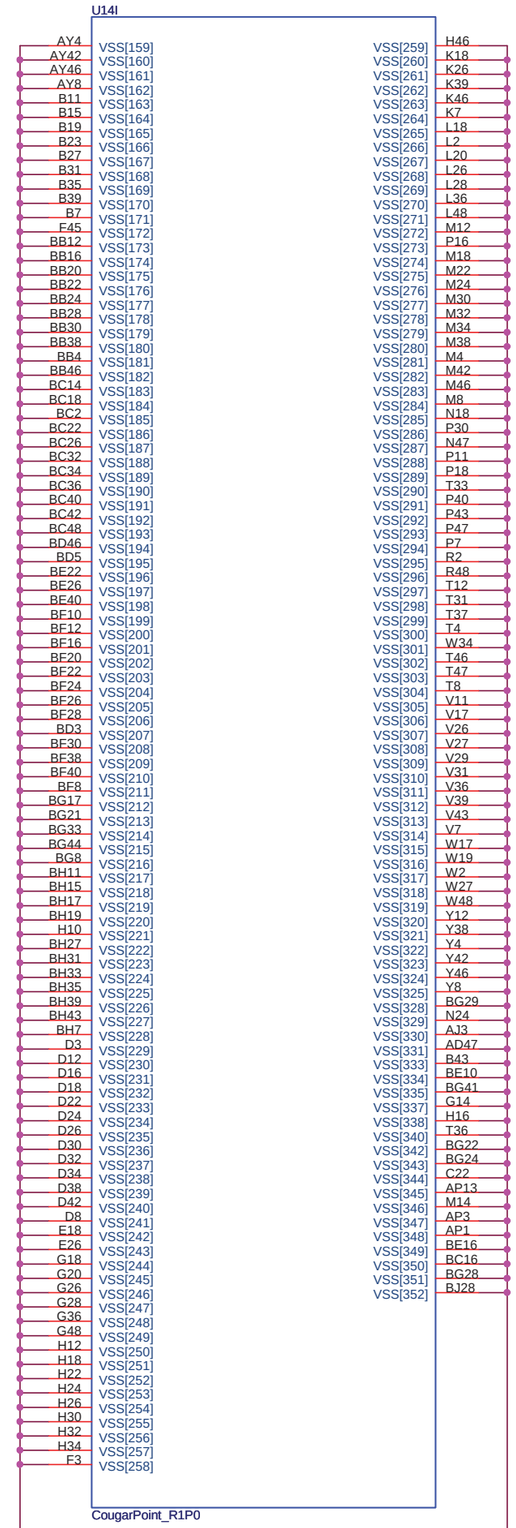
IBEX PEAK-M (GND)





PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
	Cougar Point 6/6	1A

Date: Thursday, November 04, 2010 Sheet 13 of 53

DDR_RVS(DDR)

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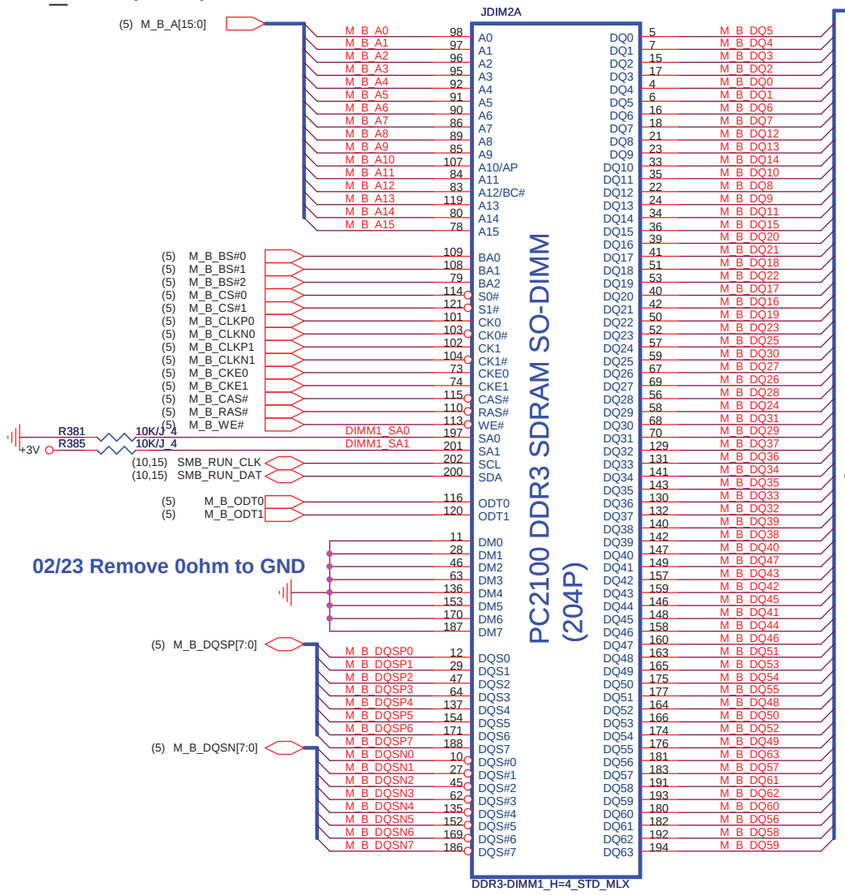
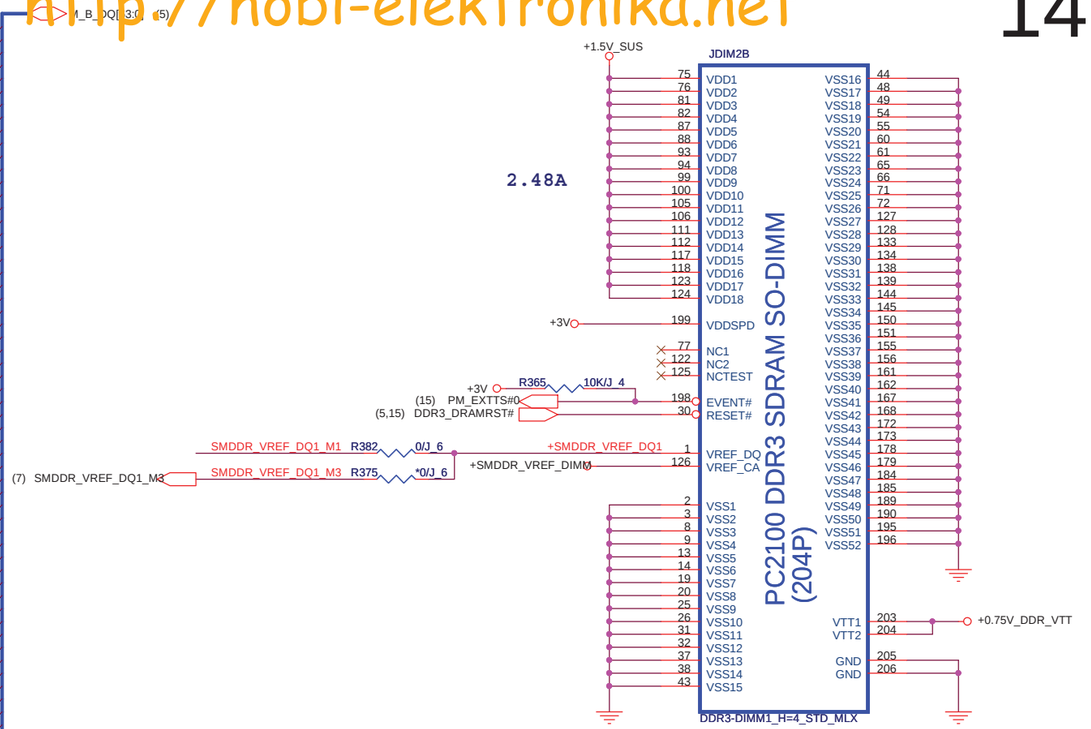
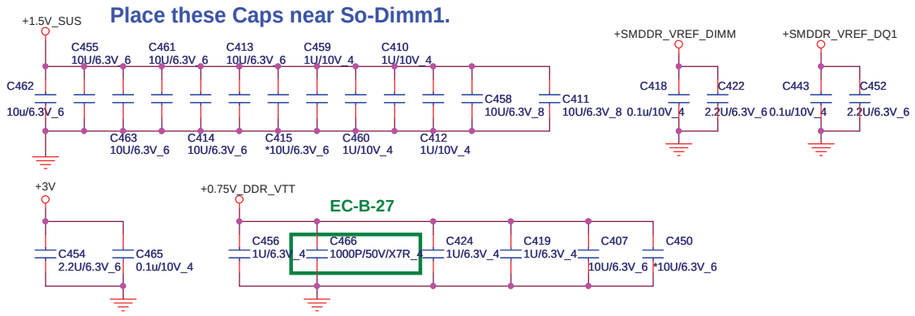


02/23 Remove 0ohm to GND



Place these Caps near So-Dimm1.

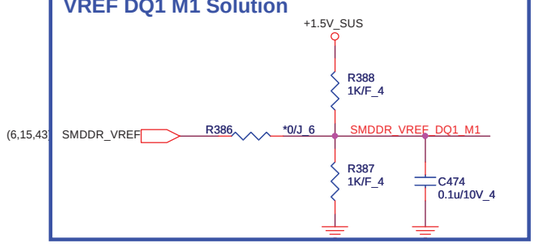


VREF DQ1 M2 Solution

6/22 Remove M2 Solution by MOW26

A16

VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

PROJECT KL5A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRIII SO-DIMM-0	1A

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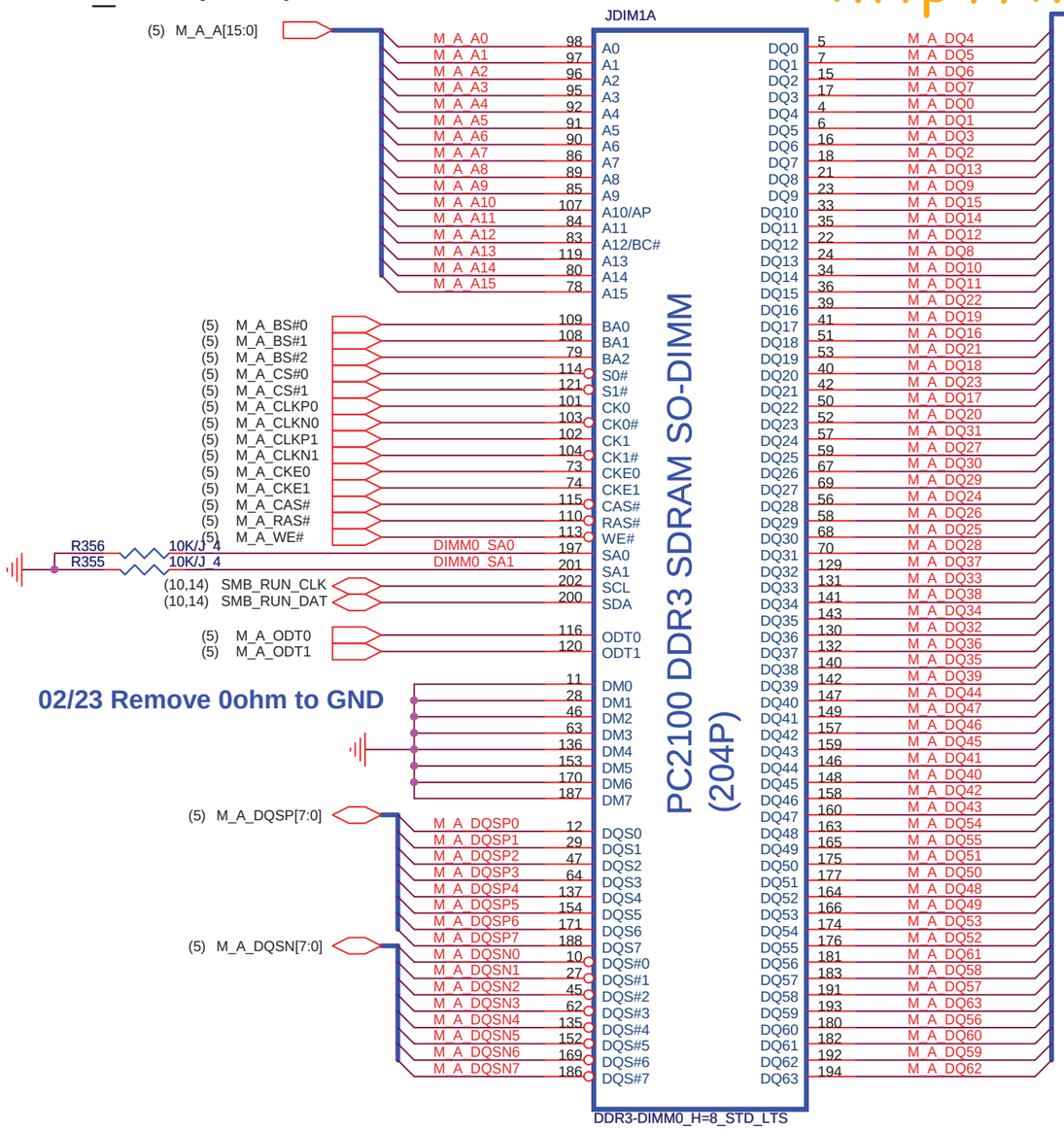
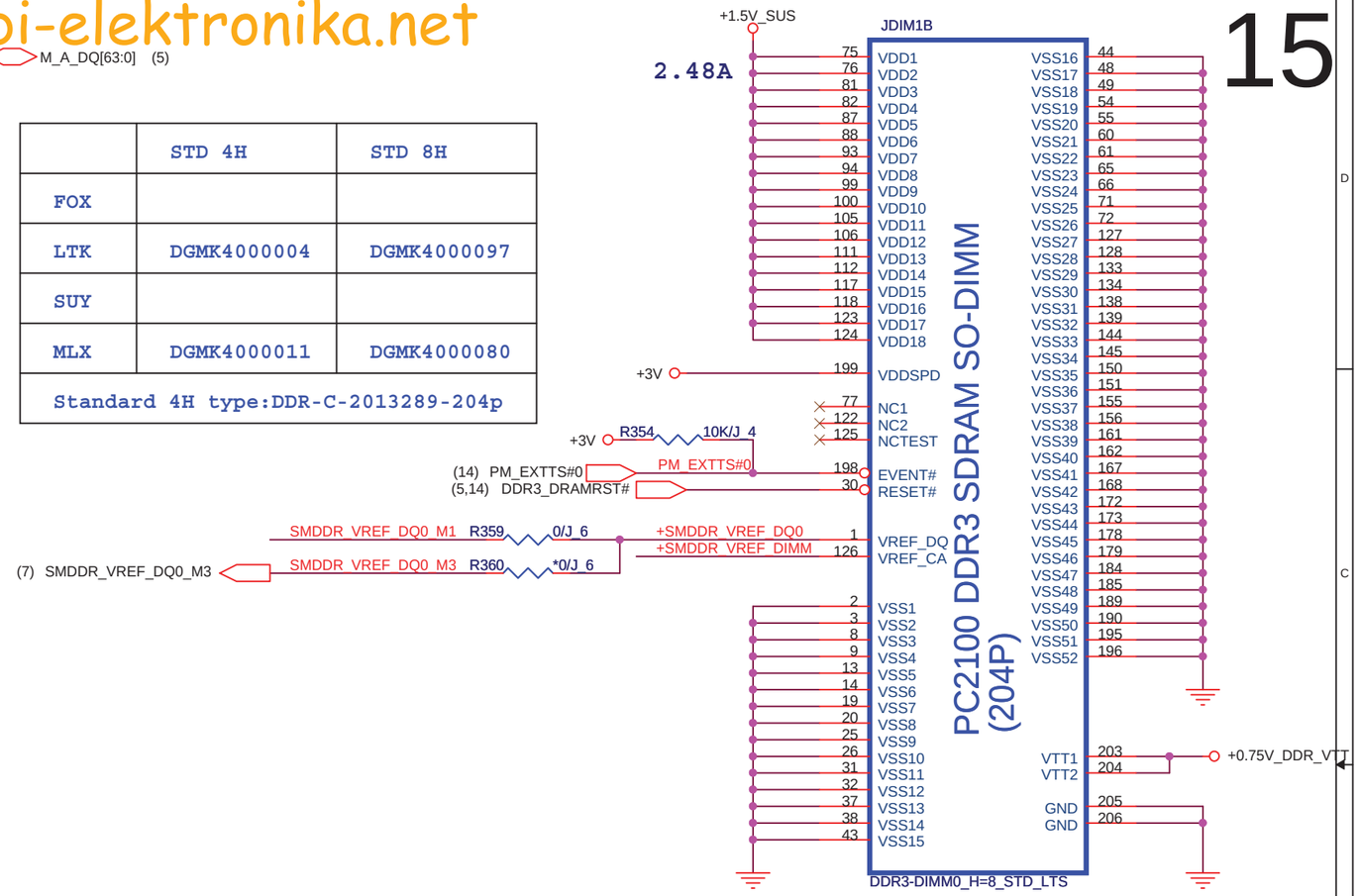
DDR_RVS (DDR)

http://hobi-elektronika.net

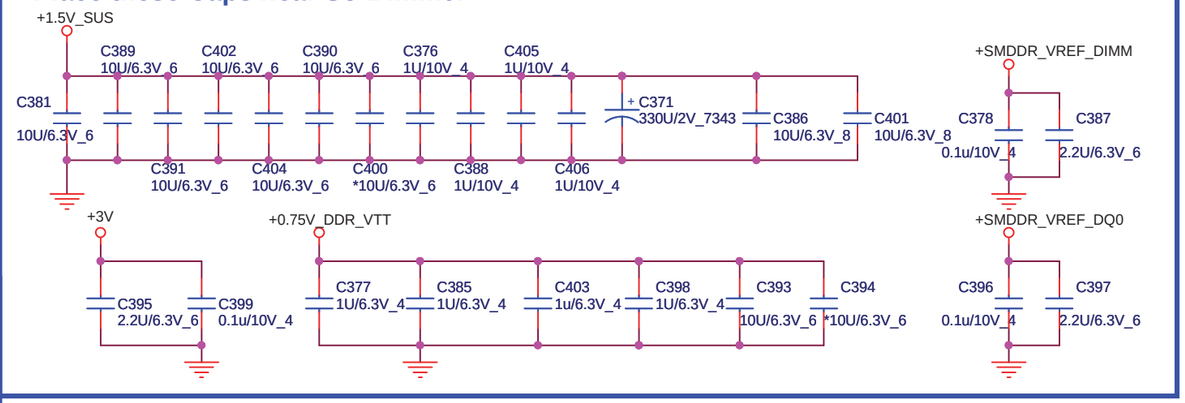


02/23 Remove 0ohm to GND

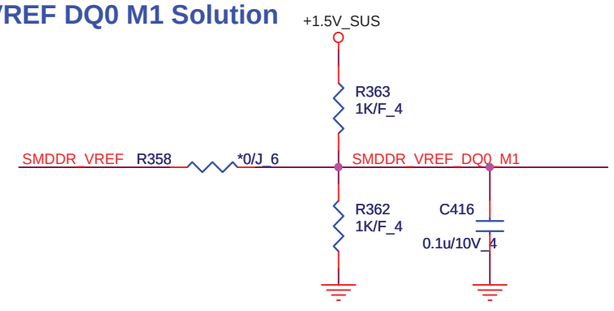
	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

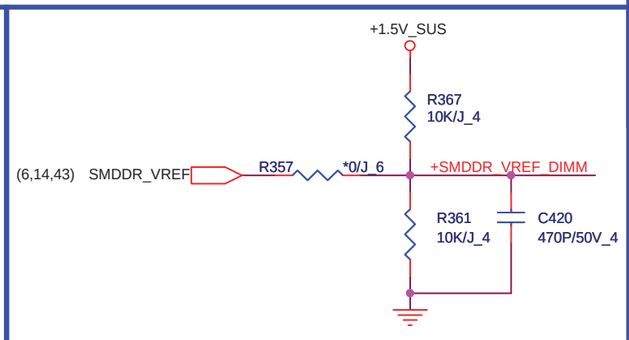


Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution





PROJECT KL5A

Quanta Computer Inc.

Size	Document Number	Rev
B	DDRIII SO-DIMM-1	1A

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http://hobi-elektronika.net

POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9~1.2V

2.5GT/s bit rate

U30A

PCIE INTERFACE

(4) PEG_TXP15	PEG_TXP15	AE30	PCIE_RX0P	PCIE_TX0P	AH30	C_PEG_RXP15	C218	0.1U/10V_4	PEG_RXP15 (4)
(4) PEG_TXN15	PEG_TXN15	AE31	PCIE_RX0N	PCIE_TX0N	AG31	C_PEG_RXN15	C208	0.1U/10V_4	PEG_RXN15 (4)
(4) PEG_TXP14	PEG_TXP14	AE29	PCIE_RX1P	PCIE_TX1P	AG29	C_PEG_RXP14	C205	0.1U/10V_4	PEG_RXP14 (4)
(4) PEG_TXN14	PEG_TXN14	AD28	PCIE_RX1N	PCIE_TX1N	AF28	C_PEG_RXN14	C203	0.1U/10V_4	PEG_RXN14 (4)
(4) PEG_TXP13	PEG_TXP13	AD30	PCIE_RX2P	PCIE_TX2P	AF27	C_PEG_RXP13	C230	0.1U/10V_4	PEG_RXP13 (4)
(4) PEG_TXN13	PEG_TXN13	AC31	PCIE_RX2N	PCIE_TX2N	AF26	C_PEG_RXN13	C229	0.1U/10V_4	PEG_RXN13 (4)
(4) PEG_TXP12	PEG_TXP12	AC29	PCIE_RX3P	PCIE_TX3P	AD27	C_PEG_RXP12	C195	0.1U/10V_4	PEG_RXP12 (4)
(4) PEG_TXN12	PEG_TXN12	AB28	PCIE_RX3N	PCIE_TX3N	AD26	C_PEG_RXN12	C201	0.1U/10V_4	PEG_RXN12 (4)
(4) PEG_TXP11	PEG_TXP11	AB30	PCIE_RX4P	PCIE_TX4P	AC25	C_PEG_RXP11	C194	0.1U/10V_4	PEG_RXP11 (4)
(4) PEG_TXN11	PEG_TXN11	AA31	PCIE_RX4N	PCIE_TX4N	AB25	C_PEG_RXN11	C188	0.1U/10V_4	PEG_RXN11 (4)
(4) PEG_TXP10	PEG_TXP10	AA29	PCIE_RX5P	PCIE_TX5P	Y23	C_PEG_RXP10	C169	0.1U/10V_4	PEG_RXP10 (4)
(4) PEG_TXN10	PEG_TXN10	Y28	PCIE_RX5N	PCIE_TX5N	Y24	C_PEG_RXN10	C181	0.1U/10V_4	PEG_RXN10 (4)
(4) PEG_TXP9	PEG_TXP9	Y30	PCIE_RX6P	PCIE_TX6P	AB27	C_PEG_RXP9	C184	0.1U/10V_4	PEG_RXP9 (4)
(4) PEG_TXN9	PEG_TXN9	W31	PCIE_RX6N	PCIE_TX6N	AB26	C_PEG_RXN9	C186	0.1U/10V_4	PEG_RXN9 (4)
(4) PEG_TXP8	PEG_TXP8	W29	PCIE_RX7P	PCIE_TX7P	W27	C_PEG_RXP8	C163	0.1U/10V_4	PEG_RXP8 (4)
(4) PEG_TXN8	PEG_TXN8	V28	PCIE_RX7N	PCIE_TX7N	Y26	C_PEG_RXN8	C168	0.1U/10V_4	PEG_RXN8 (4)
(4) PEG_TXP7	PEG_TXP7	V30	PCIE_RX8P	PCIE_TX8P	W24	C_PEG_RXP7	C162	0.1U/10V_4	PEG_RXP7 (4)
(4) PEG_TXN7	PEG_TXN7	U31	PCIE_RX8N	PCIE_TX8N	W23	C_PEG_RXN7	C153	0.1U/10V_4	PEG_RXN7 (4)
(4) PEG_TXP6	PEG_TXP6	U29	PCIE_RX9P	PCIE_TX9P	V27	C_PEG_RXP6	C148	0.1U/10V_4	PEG_RXP6 (4)
(4) PEG_TXN6	PEG_TXN6	T28	PCIE_RX9N	PCIE_TX9N	U26	C_PEG_RXN6	C151	0.1U/10V_4	PEG_RXN6 (4)
(4) PEG_TXP5	PEG_TXP5	T30	PCIE_RX10P	PCIE_TX10P	U24	C_PEG_RXP5	C145	0.1U/10V_4	PEG_RXP5 (4)
(4) PEG_TXN5	PEG_TXN5	R31	PCIE_RX10N	PCIE_TX10N	U23	C_PEG_RXN5	C138	0.1U/10V_4	PEG_RXN5 (4)
(4) PEG_TXP4	PEG_TXP4	R29	PCIE_RX11P	PCIE_TX11P	T26	C_PEG_RXP4	C137	0.1U/10V_4	PEG_RXP4 (4)
(4) PEG_TXN4	PEG_TXN4	P28	PCIE_RX11N	PCIE_TX11N	T27	C_PEG_RXN4	C127	0.1U/10V_4	PEG_RXN4 (4)
(4) PEG_TXP3	PEG_TXP3	P30	PCIE_RX12P	PCIE_TX12P	T24	C_PEG_RXP3	C115	0.1U/10V_4	PEG_RXP3 (4)
(4) PEG_TXN3	PEG_TXN3	N31	PCIE_RX12N	PCIE_TX12N	T23	C_PEG_RXN3	C125	0.1U/10V_4	PEG_RXN3 (4)
(4) PEG_TXP2	PEG_TXP2	N29	PCIE_RX13P	PCIE_TX13P	P27	C_PEG_RXP2	C111	0.1U/10V_4	PEG_RXP2 (4)
(4) PEG_TXN2	PEG_TXN2	M28	PCIE_RX13N	PCIE_TX13N	P26	C_PEG_RXN2	C105	0.1U/10V_4	PEG_RXN2 (4)
(4) PEG_TXP1	PEG_TXP1	M30	PCIE_RX14P	PCIE_TX14P	P24	C_PEG_RXP1	C101	0.1U/10V_4	PEG_RXP1 (4)
(4) PEG_TXN1	PEG_TXN1	L31	PCIE_RX14N	PCIE_TX14N	P23	C_PEG_RXN1	C95	0.1U/10V_4	PEG_RXN1 (4)
(4) PEG_TXP0	PEG_TXP0	L29	PCIE_RX15P	PCIE_TX15P	M27	C_PEG_RXP0	C88	0.1U/10V_4	PEG_RXP0 (4)
(4) PEG_TXN0	PEG_TXN0	K30	PCIE_RX15N	PCIE_TX15N	N26	C_PEG_RXN0	C83	0.1U/10V_4	PEG_RXP0 (4)

CLOCK

(10) CLK_PCIE_VGAP	AK30	PCIE_REFCLKP	
(10) CLK_PCIE_VGAN	AK32	PCIE_REFCLKN	

CALIBRATION

PCIE_CALRP	Y22	M72_PCIE_CALRP	R134	1.27K/F_4
PCIE_CALRN	AA22	M72_PCIE_CALRN	R218	2K/F_4

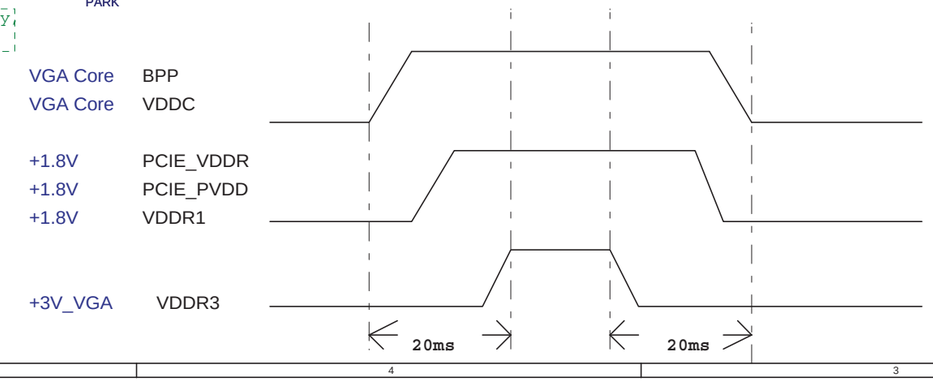
M93-S3--NC
PARK-S3--install

10K/F_4 1 2 R119 N10 NC_PWRGOOD

(4,10,25,29,31) PLTRST# AL27 PERSTB

PARK

100MHz (+/-300ppm) input frequency
0-0.7V single-ended swing



U30G

DP E/F POWER		DP A/B POWER	
+1.8V_DPE_VDD18	AG15, AG16 DPE_VDD18#1, DPE_VDD18#2	NC_DPA_VDD18#1, NC_DPA_VDD18#2	AE11, AE11 +1.8V_DPA_VDD18
+1.1V_DPE_VDD10	AG20, AG21 DPE_VDD10#1, DPE_VDD10#2	DPA_VDD10#1, DPA_VDD10#2	AF6, AF7 +1.1V_DPB_VDD10
	AG14, AH14, AM14, AM16, AM18 DPE_VSSR#1, DPE_VSSR#2, DPE_VSSR#3, DPE_VSSR#4, DPE_VSSR#5	DPA_VSSR#1, DPA_VSSR#2, DPA_VSSR#3, DPA_VSSR#4, DPA_VSSR#5	AE1, AE3, AG1, AG6, AH5
+1.8V_DPE_VDD18	AF16, AG17 DPF_VDD18#1, DPF_VDD18#2	NC_DPB_VDD18#1, NC_DPB_VDD18#2	AE13, AF13 +1.8V_DPA_VDD18
+1.1V_DPE_VDD10	AF22, AG22 DPF_VDD10#1, DPF_VDD10#2	DPB_VDD10#1, DPB_VDD10#2	AF8, AF9 +1.1V_DPB_VDD10
	AF23, AG23, AM20, AM22, AM24 DPF_VSSR#1, DPF_VSSR#2, DPF_VSSR#3, DPF_VSSR#4, DPF_VSSR#5	DPB_VSSR#1, DPB_VSSR#2, DPB_VSSR#3, DPB_VSSR#4, DPB_VSSR#5	AF10, AG9, AH8, AM6, AM8
R186 150/F_4 DPEF_CALR	AF17 DPEF_CALR	DPAB_CALR	AE10 DPAB_CALR R575 150/F_4
+1.8V_DPE_PVDD	+1.8V_DPE_PVDD AG18, AF19 DPE_PVDD, DPE_PVSS	DPA_PVDD, DPA_PVSS	AG8, AG7 +1.8V_DPA_PVDD
+1.8V_DPF_PVDD	R185 0_4 AG19, AF20 NC_DPF_PVDD, NC_DPF_PVSS	DPB_PVDD, DPB_PVSS	AG10, AG11 +1.8V_DPA_PVDD

DP PLL POWER

M93-S3--NC
PARK-S3--install

PARK

BLM18PG181SN1D(180,1.5A)_6
L14 +1.1V_GPU
1.1V(S100,D200mA)
C204 0.1U/10V_4 C216 10U/6.3V_6S C206 1U/10V_4

(Park-S3:110mA@1.0V)
(M9X-S2/S3:200mA@1.1V)

+1.1V_DPE_VDD10 +1.1V_DPE_VDD10 L45 BLM18PG181SN1D(180,1.5A)_6 +1.1V_GPU
C239 0.1U/10V_4 C214 1U/10V_4 C251 10U/6.3V_6S

+1.8V_DPA_VDD18 +1.8V_DPA_VDD18 L15 BLM18PG181SN1D(180,1.5A)_6 1.8V(130mA) +1.8V_GPU
C199 0.1U/10V_4 C223 1U/10V_4 C232 10U/6.3V_6S
M93-S3--NC
PARK-S3--install

+1.8V_DPE_VDD18 1.8V -(440mA) L42 BLM18PG181SN1D(180,1.5A)_6 +1.8V_GPU
C202 0.1U/10V_4 C604 1U/10V_4 C618 10U/6.3V_6S

+1.8V_DPA_PVDD +1.8V_DPA_PVDD L13 BLM18PG181SN1D(180,1.5A)_6 1.8V(20mA) +1.8V_GPU
C217 0.1U/10V_4 C215 1U/10V_4 C222 10U/6.3V_6S

+1.8V_DPF_PVDD +1.8V_DPF_PVDD L18 BLM18PG181SN1D(180,1.5A)_6 1.8V(20mA) +1.8V_GPU
C212 0.1U/10V_4 C237 1U/10V_4 C252 10U/6.3V_6S
M93-S3--NC
PARK-S3--install

+1.8V_DPE_PVDD +1.8V_DPE_PVDD L19 BLM18PG181SN1D(180,1.5A)_6 1.8V(20mA) +1.8V_GPU
C213 0.1U/10V_4 C231 1U/10V_4 C253 10U/6.3V_6S

Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	Robson_PCIE_Interface	1A

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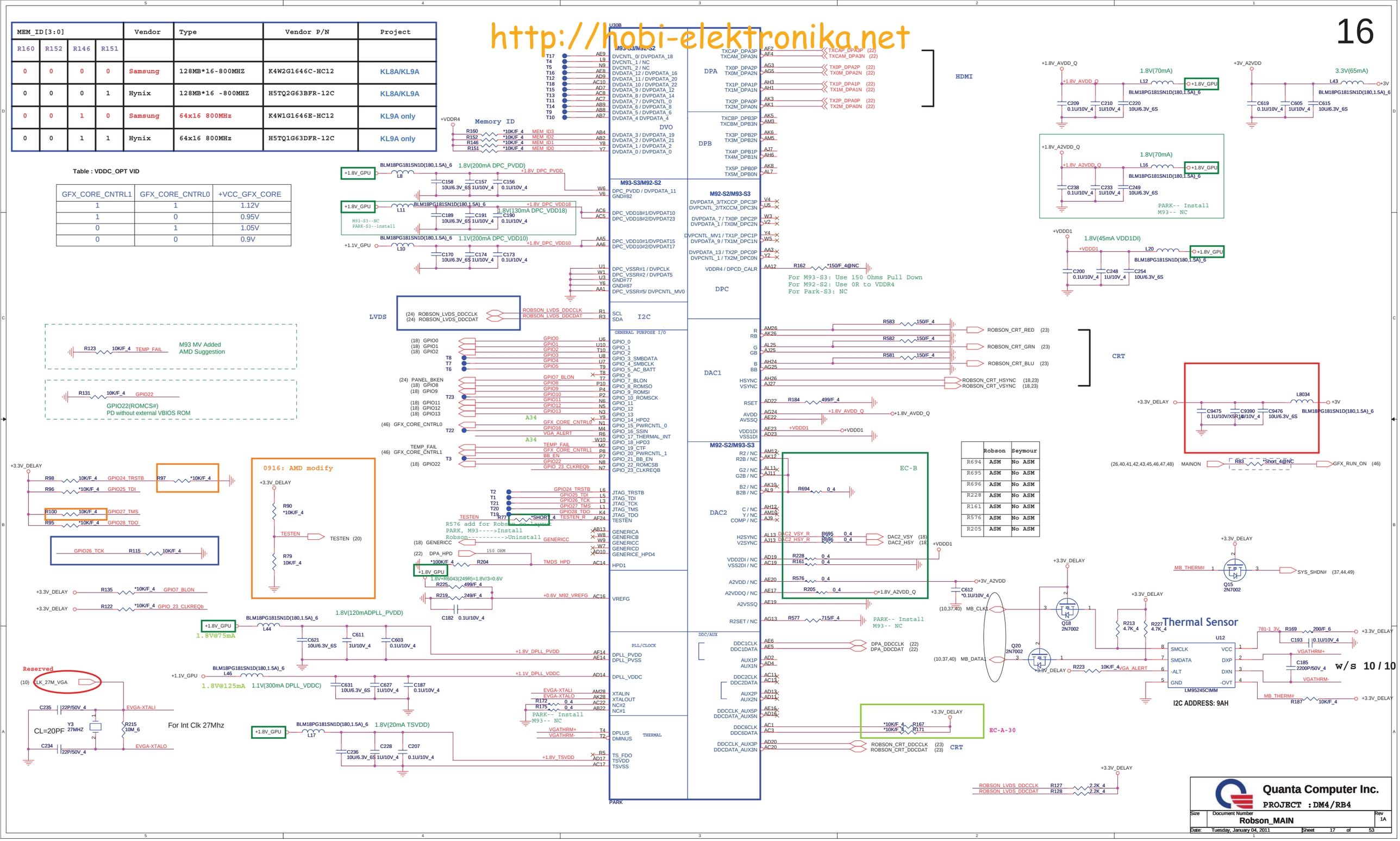
MEM_ID[3:0]				Vendor	Type	Vendor P/N	Project
R160	R152	R146	R151				
0	0	0	0	Samsung	128MB*16-800MHZ	K4W2G1646C-HC12	KL8A/KL9A
0	0	0	1	Hynix	128MB*16 -800MHZ	H5TQ2G63BFR-12C	KL8A/KL9A
0	0	1	0	Samsung	64x16 800MHz	K4W1G1646E-HC12	KL9A only
0	0	1	1	Hynix	64x16 800MHz	H5TQ1G63DFR-12C	KL9A only

Table : VDDC_OPT VID

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VCC_GFX_CORE
1	1	1.12V
1	0	0.95V
0	1	1.05V
0	0	0.9V



	Robson	Seymour
R694	ASM	No ASM
R695	ASM	No ASM
R696	ASM	No ASM
R228	ASM	No ASM
R161	ASM	No ASM
R576	ASM	No ASM
R205	ASM	No ASM

Quanta Computer Inc.

PROJECT : DM4/RB4

Size	Document Number	Rev
	Robson_MAIN	1A

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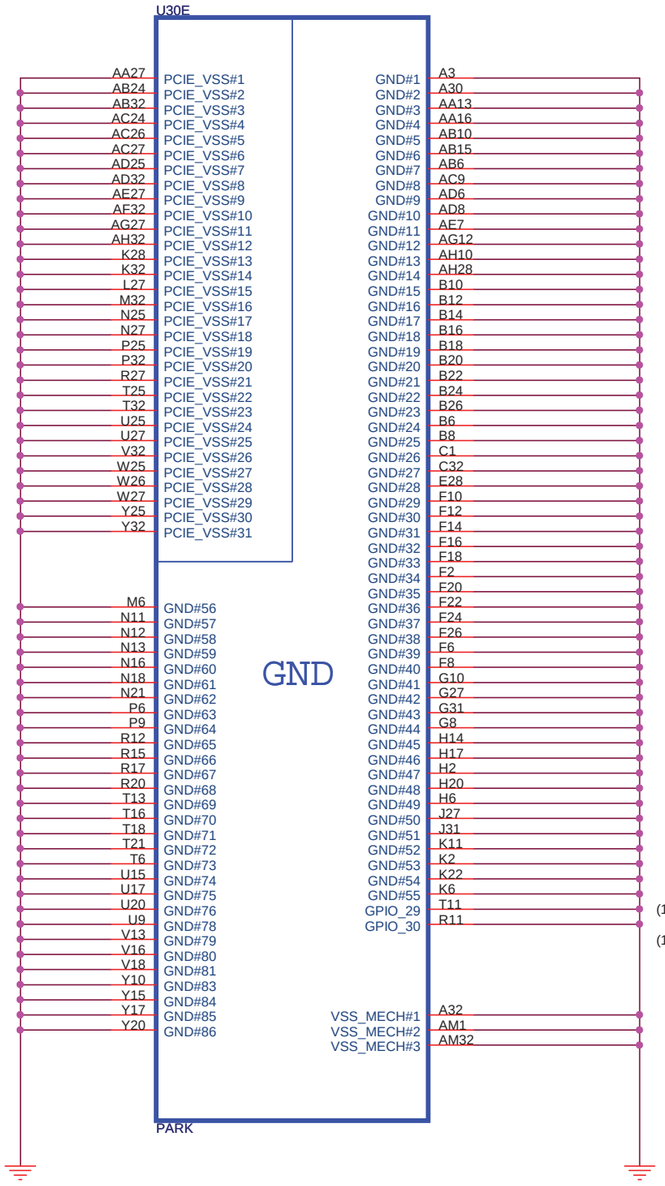
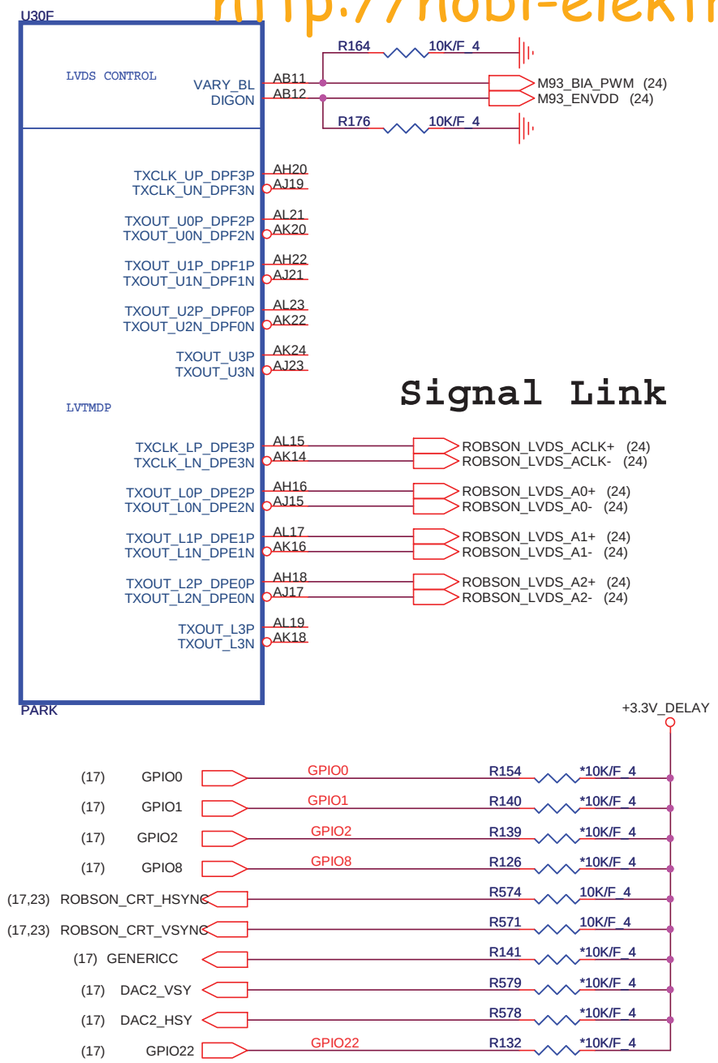
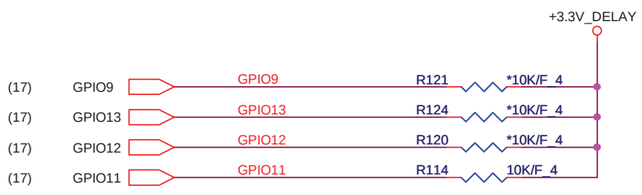




Signal Link



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

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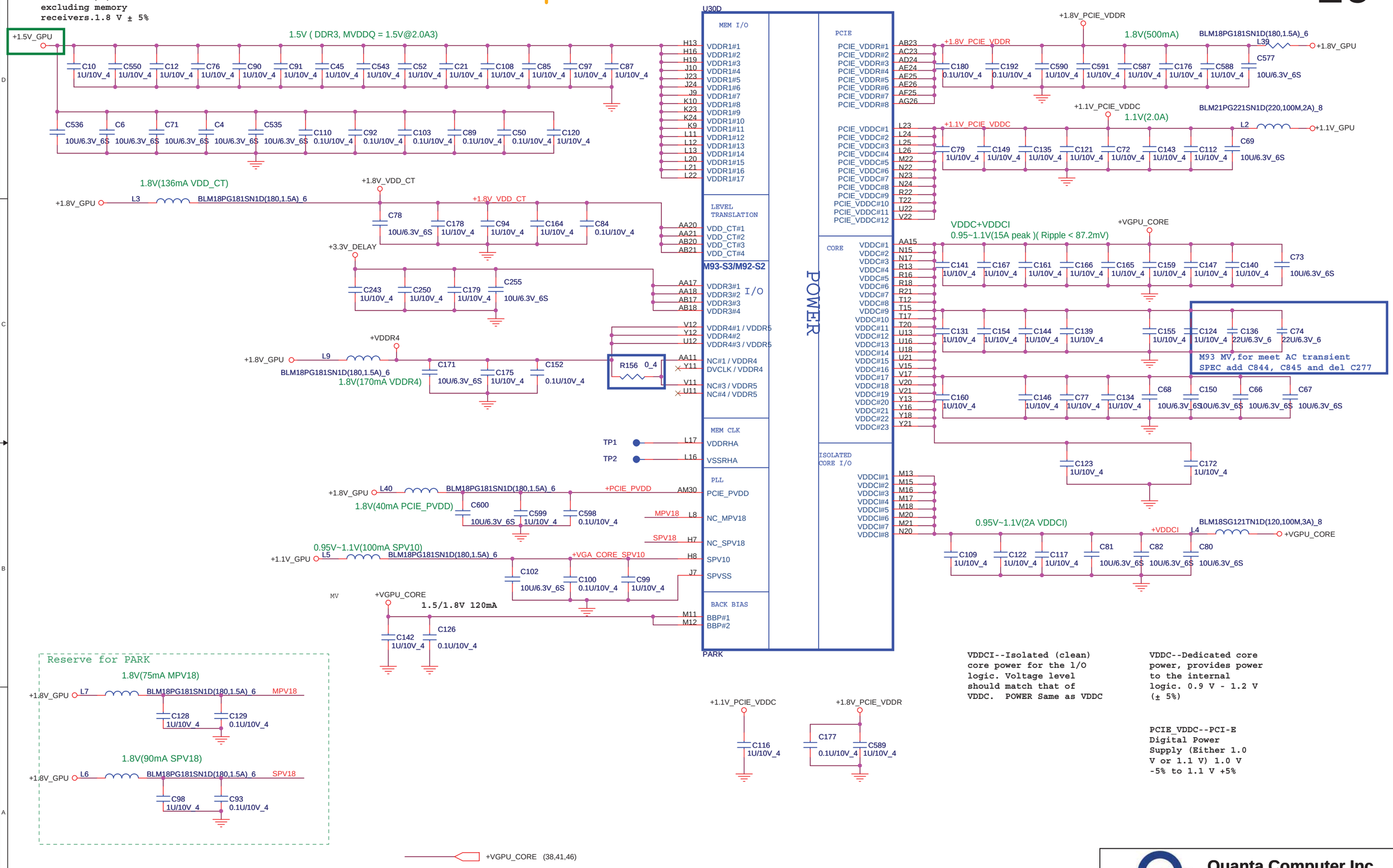
VDD_CT -- Level translation between core and I/O, excluding memory receivers.1.8 V ± 5%

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

Quanta Computer Inc.	PROJECT :DM4/RB4	
Size	Document Number: Robson_Power_and_NC	Rev 1A
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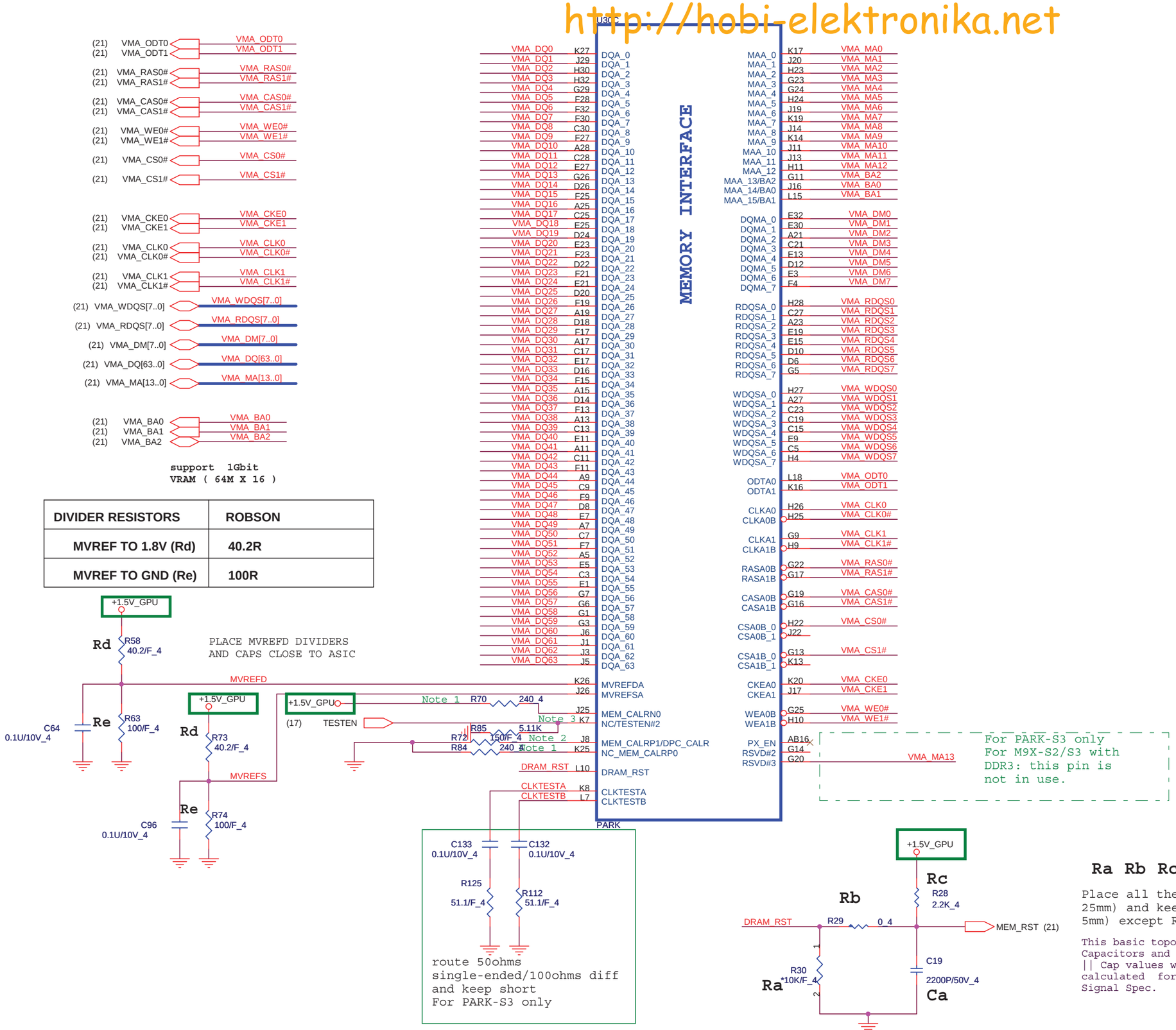

DIVIDER RESISTORS	ROBSON
MVREF TO 1.8V (Rd)	40.2R
MVREF TO GND (Re)	100R

Ra Rb Rc Rd

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24
R575 for Robson only

Quanta Computer Inc.
PROJECT :DM4/RB4

Size	Document Number	Rev
	Robson_MEM_Interface	1A
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1GB DDR3 2GB DDR3(128MB x16bit) x 4 pcs

(20) VMA_MA[13..0] — VMA_MA[13..0]
(20) VMA_DM[7..0]
(20) VMA_DQ[63..0]
(20) VMA_WDQS[7..0]
(20) VMA_RDQS[7..0]

EC-C-07 — U29 — VRAM _DDR3

VREFC_VMA1, VREFD_VMA1
VMA_MA0, VMA_MA1, VMA_MA2, VMA_MA3, VMA_MA4, VMA_MA5, VMA_MA6, VMA_MA7, VMA_MA8, VMA_MA9, VMA_MA10, VMA_MA11, VMA_MA12, VMA_MA13
(20) VMA_BA0, VMA_BA1, VMA_BA2
(20) VMA_CLK0, VMA_CLK0#, VMA_CKE0
(20) VMA_ODT0, VMA_CS0#, VMA_RAS0#, VMA_CAS0#, VMA_WE0#
VMA_RDQS3, VMA_RDQS0
VMA_DM3, VMA_DM0
VMA_WDQS3, VMA_WDQS0
(20) MEM_RST
VMA_ZQ1
VMA_DQ27, VMA_DQ28, VMA_DQ25, VMA_DQ30, VMA_DQ26, VMA_DQ29, VMA_DQ24, VMA_DQ31
VMA_DQ0, VMA_DQ2, VMA_DQ1, VMA_DQ6, VMA_DQ5, VMA_DQ7, VMA_DQ4, VMA_DQ3
+1.5V_GPU
R48 240

EC-C-07 — U4 — VRAM _DDR3

VREFC_VMA2, VREFD_VMA2
VMA_MA0, VMA_MA1, VMA_MA2, VMA_MA3, VMA_MA4, VMA_MA5, VMA_MA6, VMA_MA7, VMA_MA8, VMA_MA9, VMA_MA10, VMA_MA11, VMA_MA12, VMA_MA13
VMA_BA0, VMA_BA1, VMA_BA2
VMA_CLK0, VMA_CLK0#, VMA_CKE0
VMA_ODT0, VMA_CS0#, VMA_RAS0#, VMA_CAS0#, VMA_WE0#
VMA_RDQS2, VMA_RDQS1
VMA_DM2, VMA_DM1
VMA_WDQS2, VMA_WDQS1
MEM_RST
VMA_ZQ2
VMA_DQ21, VMA_DQ18, VMA_DQ20, VMA_DQ17, VMA_DQ23, VMA_DQ16, VMA_DQ22, VMA_DQ19
VMA_DQ14, VMA_DQ15, VMA_DQ11, VMA_DQ13, VMA_DQ10, VMA_DQ9, VMA_DQ8, VMA_DQ12
+1.5V_GPU
R25 240

EC-C-07 — U5 — VRAM _DDR3

VREFC_VMA3, VREFD_VMA3
VMA_MA0, VMA_MA1, VMA_MA2, VMA_MA3, VMA_MA4, VMA_MA5, VMA_MA6, VMA_MA7, VMA_MA8, VMA_MA9, VMA_MA10, VMA_MA11, VMA_MA12, VMA_MA13
VMA_BA0, VMA_BA1, VMA_BA2
(20) VMA_CLK1, VMA_CLK1#, VMA_CKE1
(20) VMA_ODT1, VMA_CS1#, VMA_RAS1#, VMA_CAS1#, VMA_WE1#
VMA_RDQS7, VMA_RDQS6
VMA_DM7, VMA_DM6
VMA_WDQS7, VMA_WDQS6
MEM_RST
VMA_ZQ3
VMA_DQ61, VMA_DQ59, VMA_DQ63, VMA_DQ57, VMA_DQ58, VMA_DQ56, VMA_DQ62, VMA_DQ60
VMA_DQ51, VMA_DQ52, VMA_DQ48, VMA_DQ55, VMA_DQ50, VMA_DQ54, VMA_DQ49, VMA_DQ53
+1.5V_GPU
R59 240

EC-C-07 — U28 — VRAM _DDR3

VREFC_VMA4, VREFD_VMA4
VMA_MA0, VMA_MA1, VMA_MA2, VMA_MA3, VMA_MA4, VMA_MA5, VMA_MA6, VMA_MA7, VMA_MA8, VMA_MA9, VMA_MA10, VMA_MA11, VMA_MA12, VMA_MA13
VMA_BA0, VMA_BA1, VMA_BA2
VMA_CLK1, VMA_CLK1#, VMA_CKE1
VMA_ODT1, VMA_CS1#, VMA_RAS1#, VMA_CAS1#, VMA_WE1#
VMA_RDQS4, VMA_RDQS5
VMA_DM4, VMA_DM5
VMA_WDQS4, VMA_WDQS5
MEM_RST
VMA_ZQ4
VMA_DQ36, VMA_DQ38, VMA_DQ33, VMA_DQ39, VMA_DQ32, VMA_DQ37, VMA_DQ35, VMA_DQ34
VMA_DQ44, VMA_DQ43, VMA_DQ47, VMA_DQ40, VMA_DQ45, VMA_DQ41, VMA_DQ46, VMA_DQ42
+1.5V_GPU
R467 240

Pull-up resistors

Net	Resistor	Value
VREFC_VMA1	R476	4.99K/F_4
VREFC_VMA1	R477	4.99K/F_4
VREFD_VMA1	R472	4.99K/F_4
VREFD_VMA1	R473	4.99K/F_4
VREFC_VMA2	R27	4.99K/F_4
VREFC_VMA2	R26	4.99K/F_4
VREFD_VMA2	R52	4.99K/F_4
VREFD_VMA2	R54	4.99K/F_4
VREFC_VMA3	R56	4.99K/F_4
VREFC_VMA3	R55	4.99K/F_4
VREFD_VMA3	R31	4.99K/F_4
VREFD_VMA3	R32	4.99K/F_4
VREFC_VMA4	R471	4.99K/F_4
VREFC_VMA4	R470	4.99K/F_4
VREFD_VMA4	R53	4.99K/F_4
VREFD_VMA4	R57	4.99K/F_4

Decoupling capacitors

Net	Capacitor	Value
VREFC_VMA1	C559	.1U/10V_4
VREFD_VMA1	C549	.1U/10V_4
VREFC_VMA2	C18	.1U/10V_4
VREFD_VMA2	C60	.1U/10V_4
VREFC_VMA3	C53	.1U/10V_4
VREFD_VMA3	C24	.1U/10V_4
VREFC_VMA4	C541	.1U/10V_4
VREFD_VMA4	C58	.1U/10V_4

VMA_CLK0 / VMA_CLK1 termination

Net	Resistor	Value
VMA_CLK0	R475	56.2/F_4
VMA_CLK0_COMM	C532	.01U/16V_4
VMA_CLK0#	R474	56.2/F_4
VMA_CLK1	R468	56.2/F_4
VMA_CLK1_COMM	C531	.01U/16V_4
VMA_CLK1#	R469	56.2/F_4

Decoupling capacitors (+1.5V_GPU)

Capacitor	Value
C552	1U/6.3V_4
C26	1U/6.3V_4
C17	1U/6.3V_4
C539	1U/6.3V_4
C16	1U/6.3V_4
C540	1U/6.3V_4
C556	1U/6.3V_4
C544	1U/6.3V_4
C542	1U/6.3V_4
C25	1U/6.3V_4
C20	1U/6.3V_4
C46	1U/6.3V_4
C38	1U/6.3V_4
C51	1U/6.3V_4
C42	1U/6.3V_4
C56	1U/6.3V_4
C557	1U/6.3V_4
C546	1U/6.3V_4
C548	1U/6.3V_4
C547	1U/6.3V_4
C545	1U/6.3V_4
C22	1U/6.3V_4
C23	1U/6.3V_4
C555	1U/6.3V_4
C15	1U/6.3V_4
C13	1U/6.3V_4
C14	1U/6.3V_4
C11	1U/6.3V_4
C41	1U/6.3V_4
C551	1U/6.3V_4
C48	1U/6.3V_4
C57	1U/6.3V_4
C54	10U/6.3V_6S
C538	10U/6.3V_6S
C537	10U/6.3V_6S
C9	10U/6.3V_6S
C5	10U/6.3V_6S
C7	10U/6.3V_6S
C8	10U/6.3V_6S
C558	10U/6.3V_6S
C34	10U/6.3V_6S
C554	10U/6.3V_6S
C533	10U/6.3V_6S
C534	10U/6.3V_6S

Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	Robson/VRAM_A0,A1	1A

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DIS HDMI

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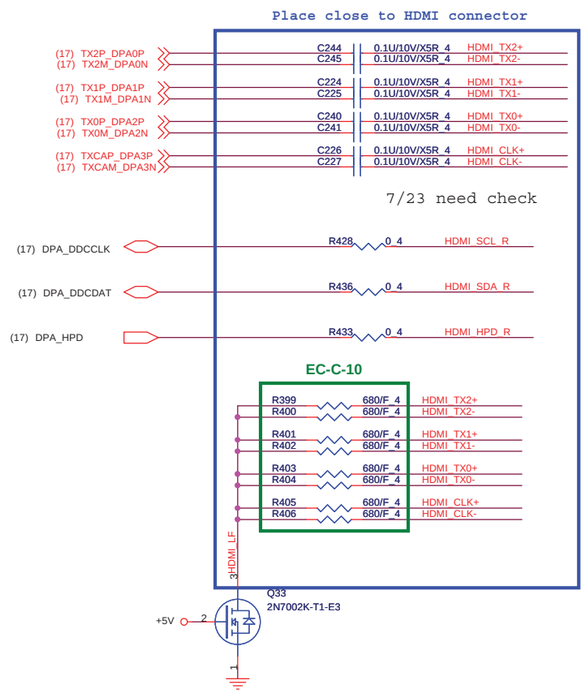
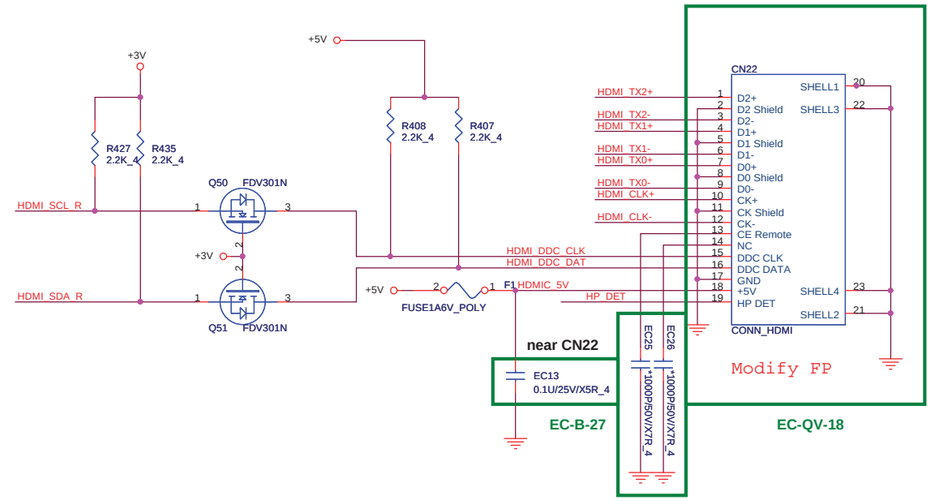
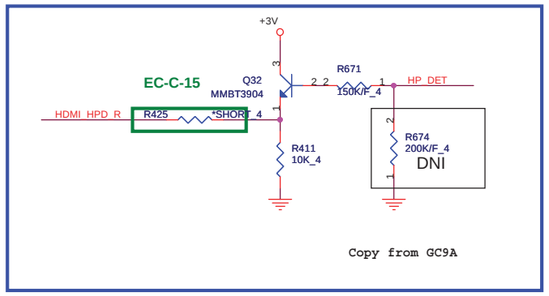
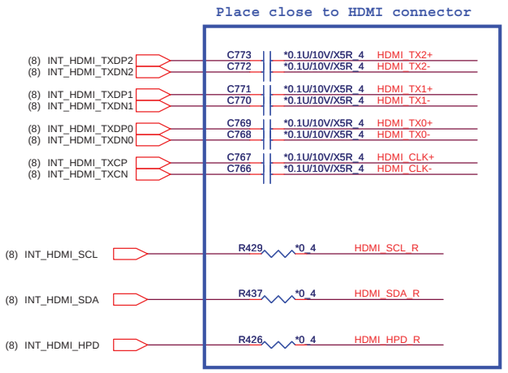


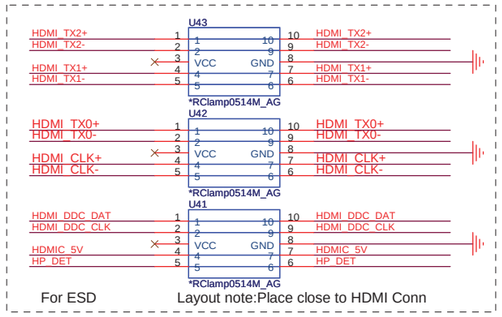


HDMI Hot-PLUG to EC and GPU

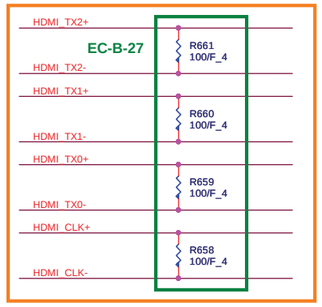


UMA Only





EMI reserve for HDMI



(8,9,12,23,26,28,35,36,37,38,40,41,42,49) +5V
(8,9,10,11,12,14,15,17,23,24,26,27,28,29,30,31,36,37,38,40,41,42,46,47,48,49) +3V

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

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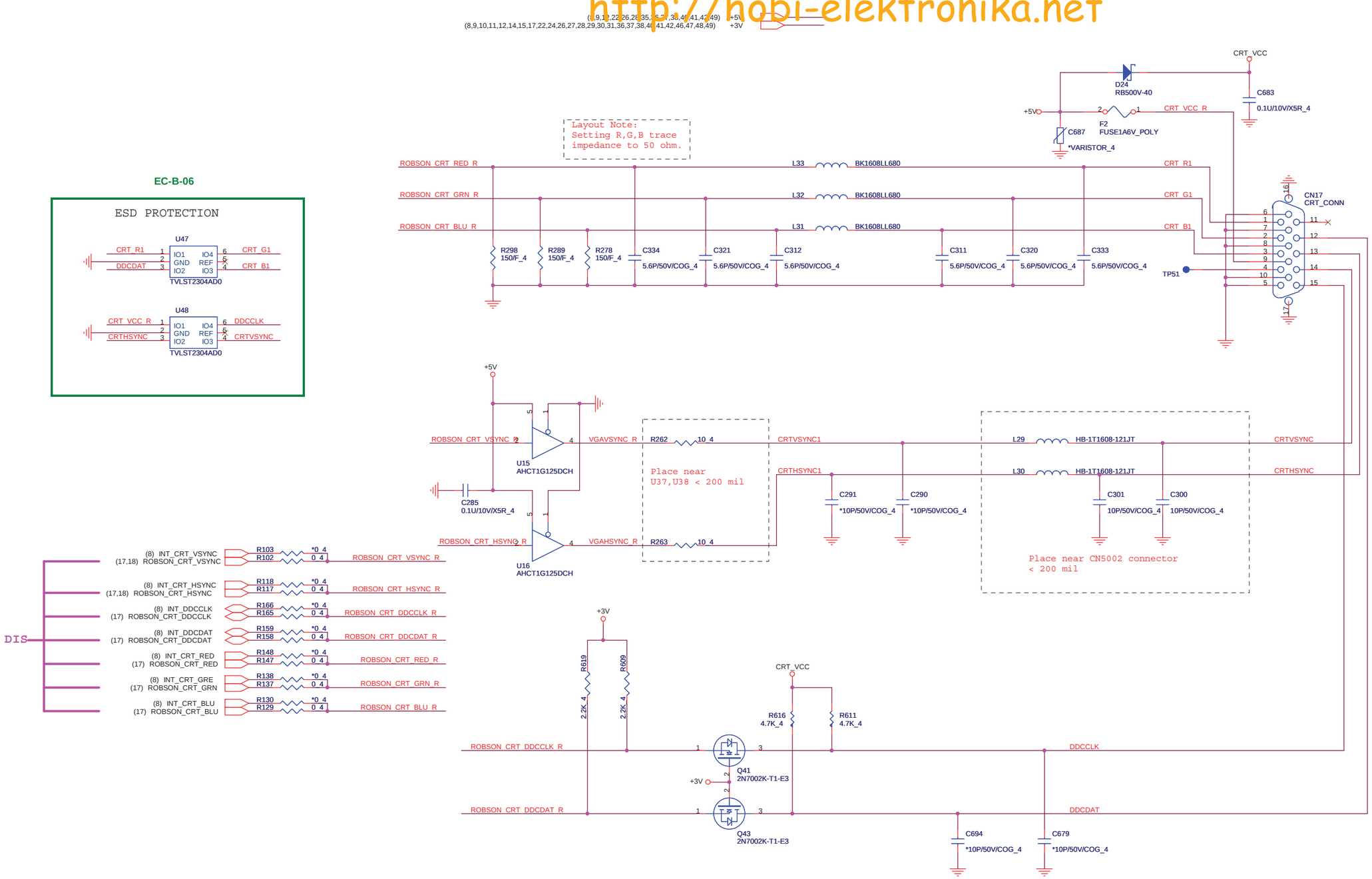

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
C	CRT CONN	1A

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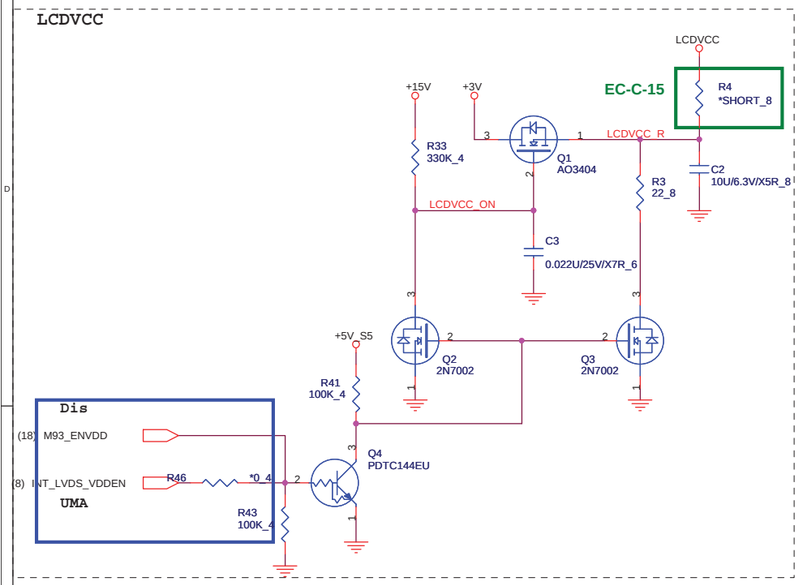

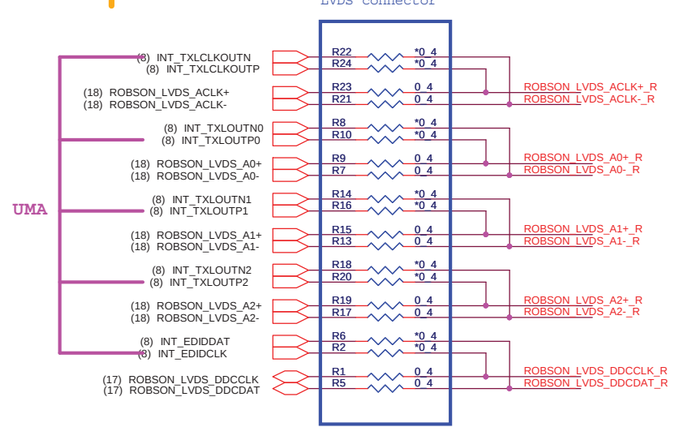

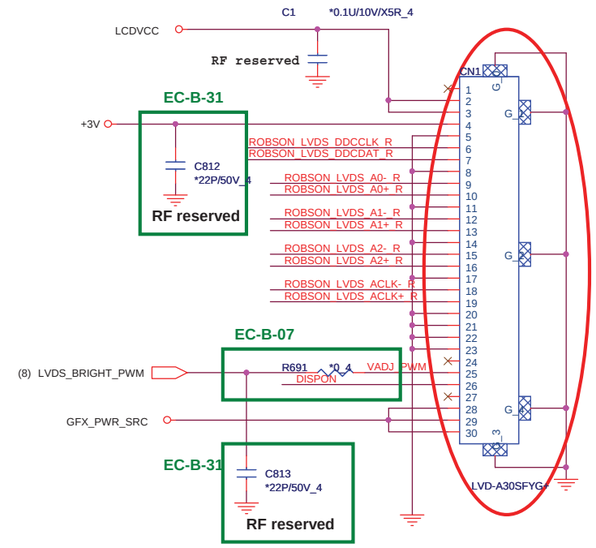

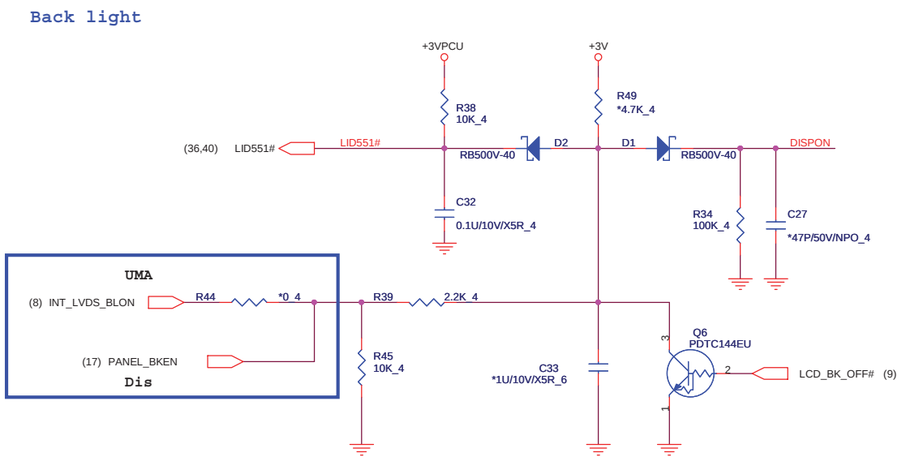

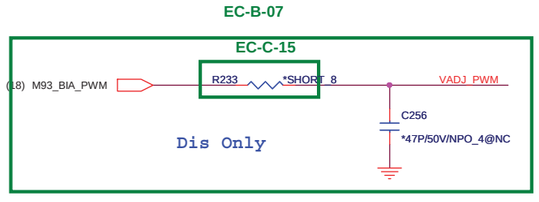

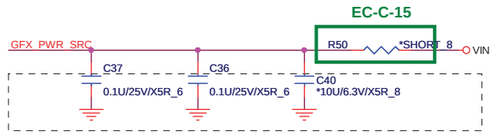

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
C	LCD CONN	1A

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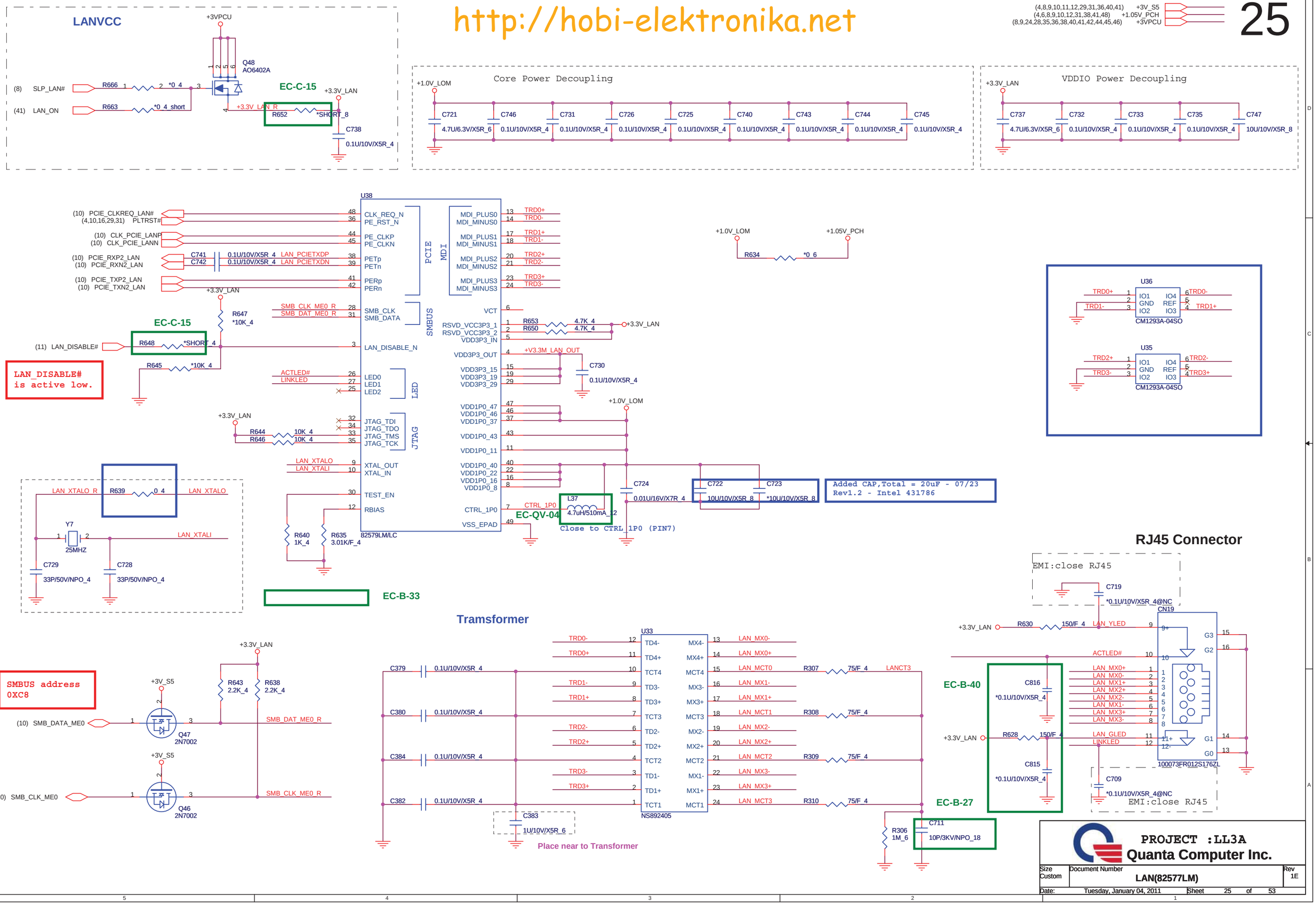
(4,8,9,10,11,12,29,31,36,40,41) +3V_S5
(4,6,8,9,10,12,31,38,41,48) +1.05V_PCH
(8,9,24,28,35,36,38,40,41,42,44,45,46) +3VPCU



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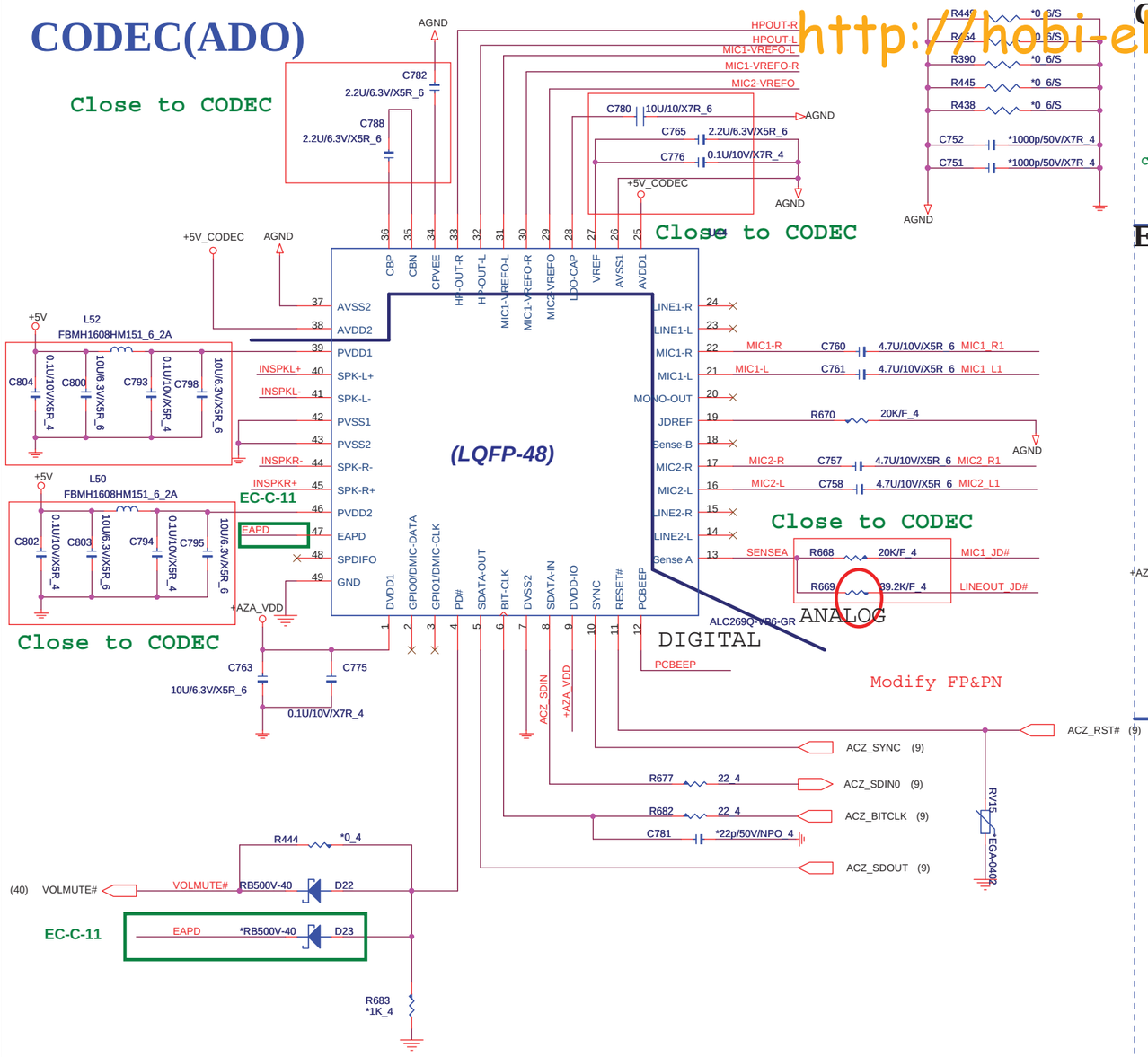
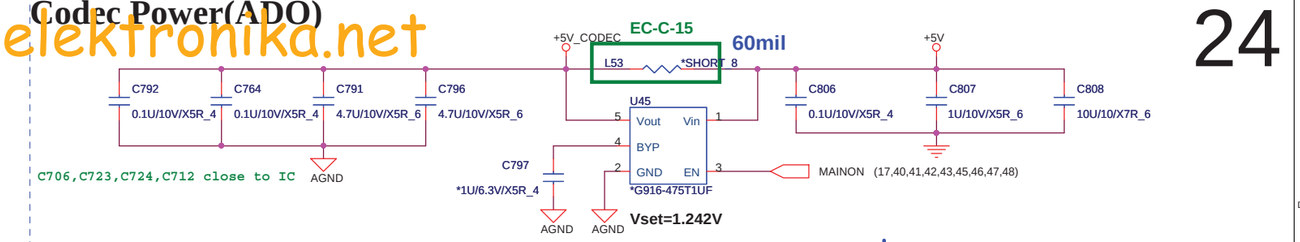
CODEC(ADO)



Codec Power(ADO)



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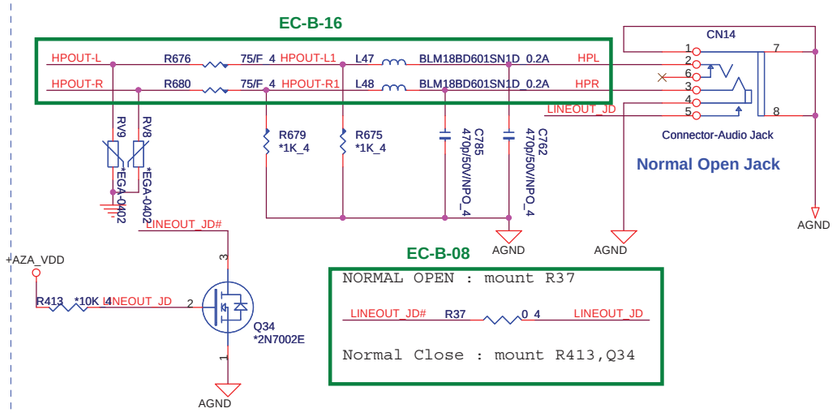
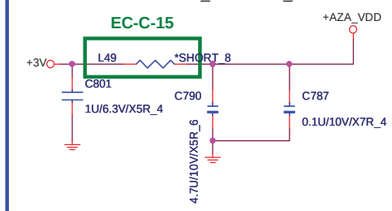
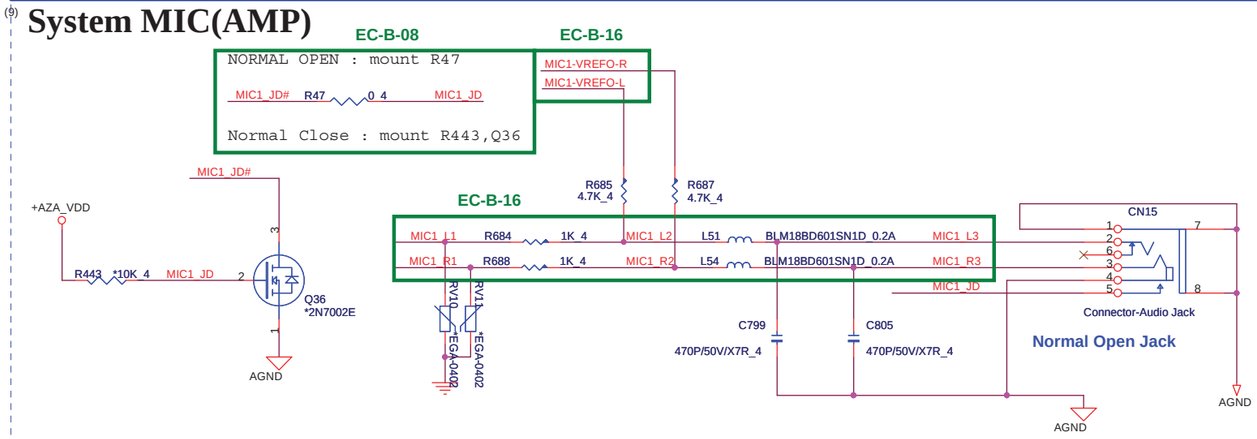


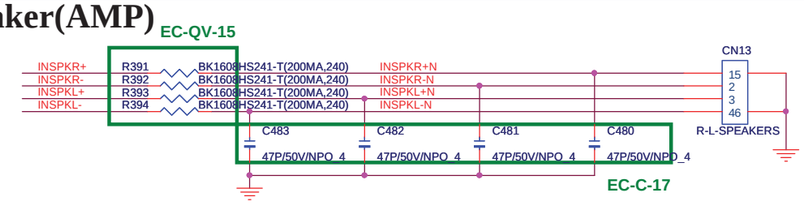
HDA Power(ADO)



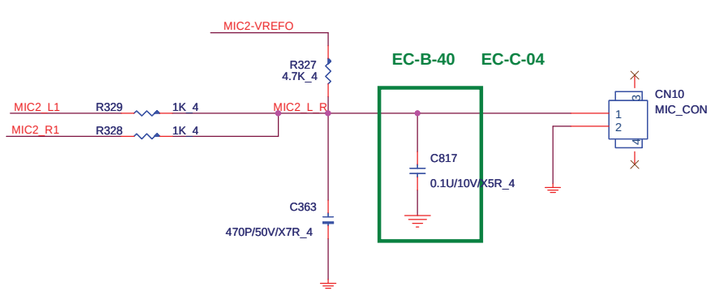
System MIC(AMP)



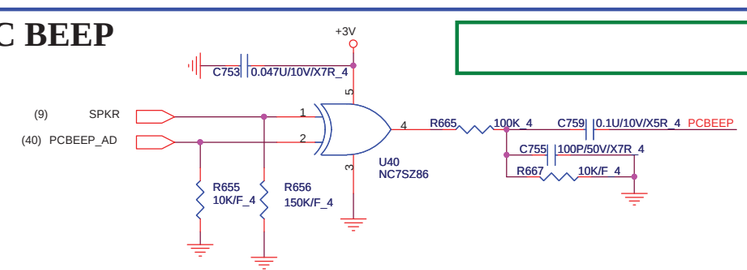
Speaker(AMP)



INTERNAL MIC



PC BEEP



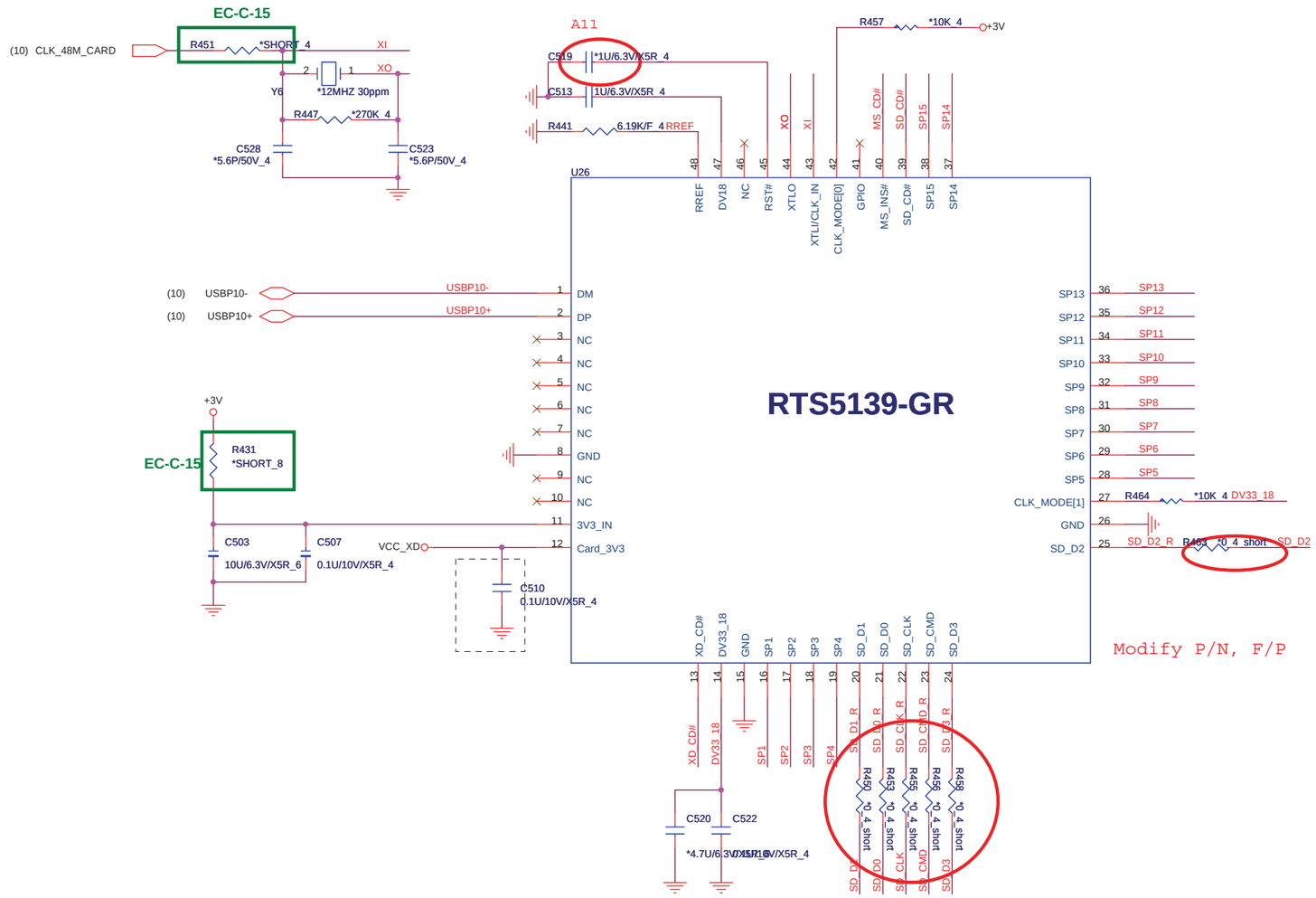
PROJECT KL5A

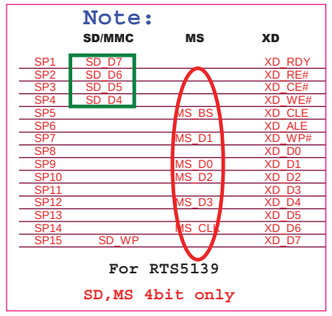
Quanta Computer Inc.

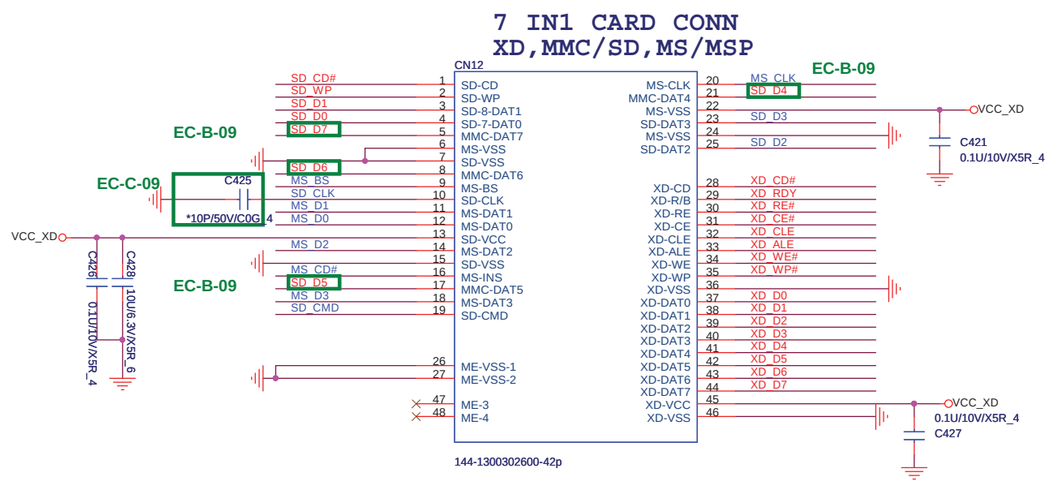
Size	Document Number	Rev
Custom	AL269/MIC/Line out	1A

Date: Tuesday, January 04, 2011 Sheet 26 of 53

Clock Mode strap	R9287	R9307
48MHz	×	×
24MHz	×	○
12MHz	○	×
12MHz (Crystal)	○	○







PROJECT KL5A

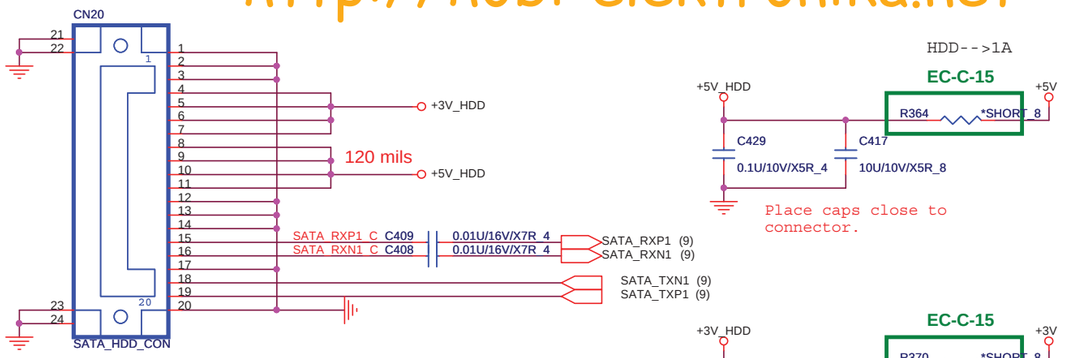
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card Reader (RTS5159)	1A

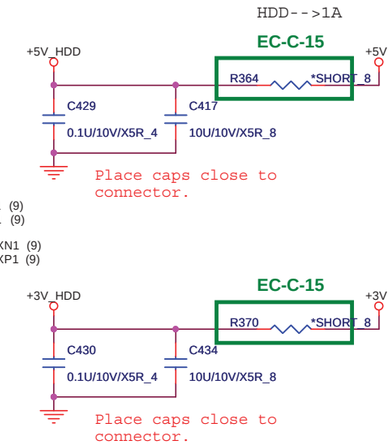
Date: Friday, November 19, 2010 Sheet 27 of 53

SATA HDD Connector.

http://hobi-elektronika.net

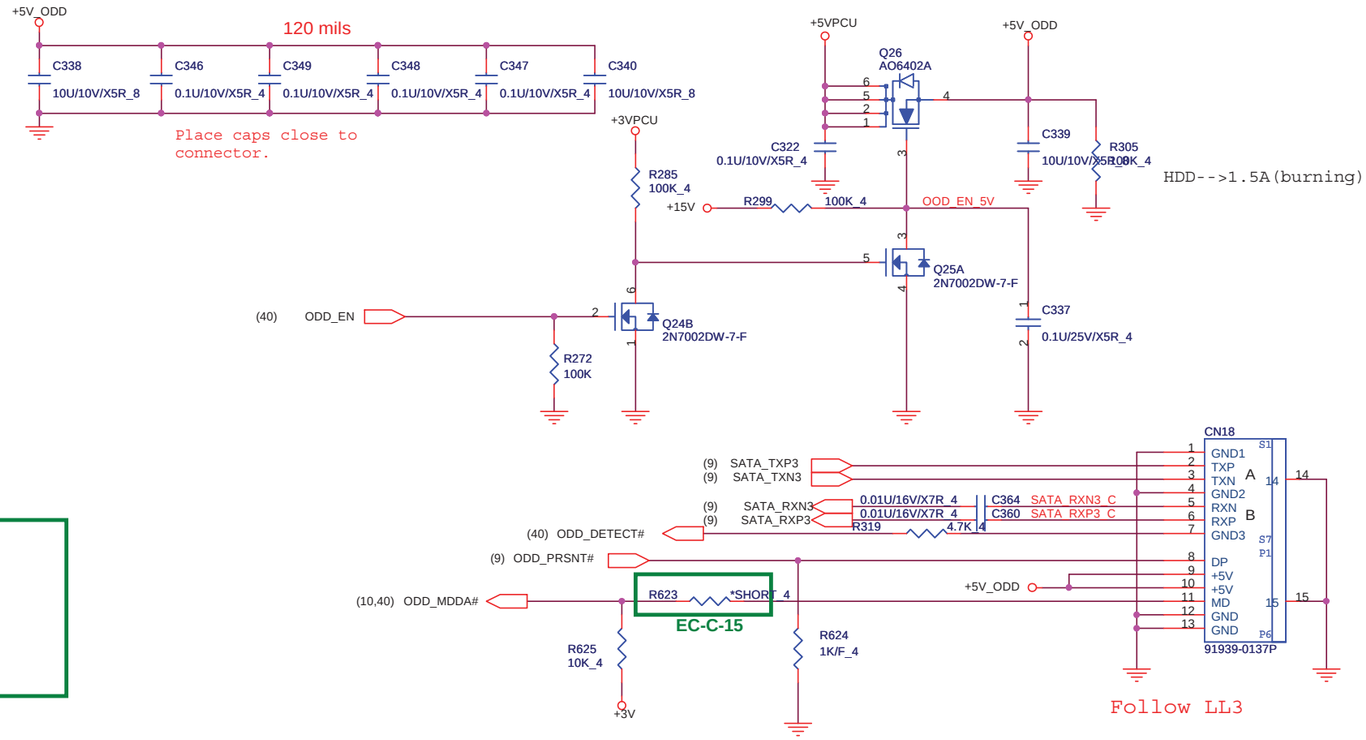


Modify PN&FP(LL7 OK)



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

SATA ODD Connector.

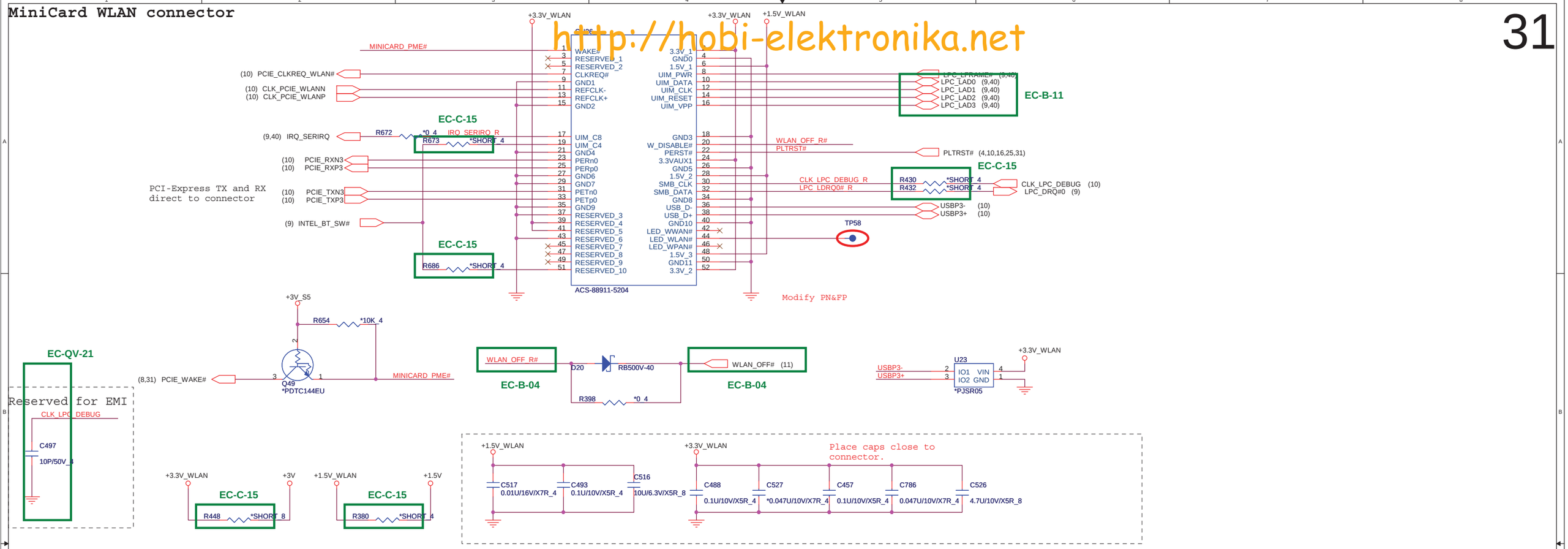


EC-B-10

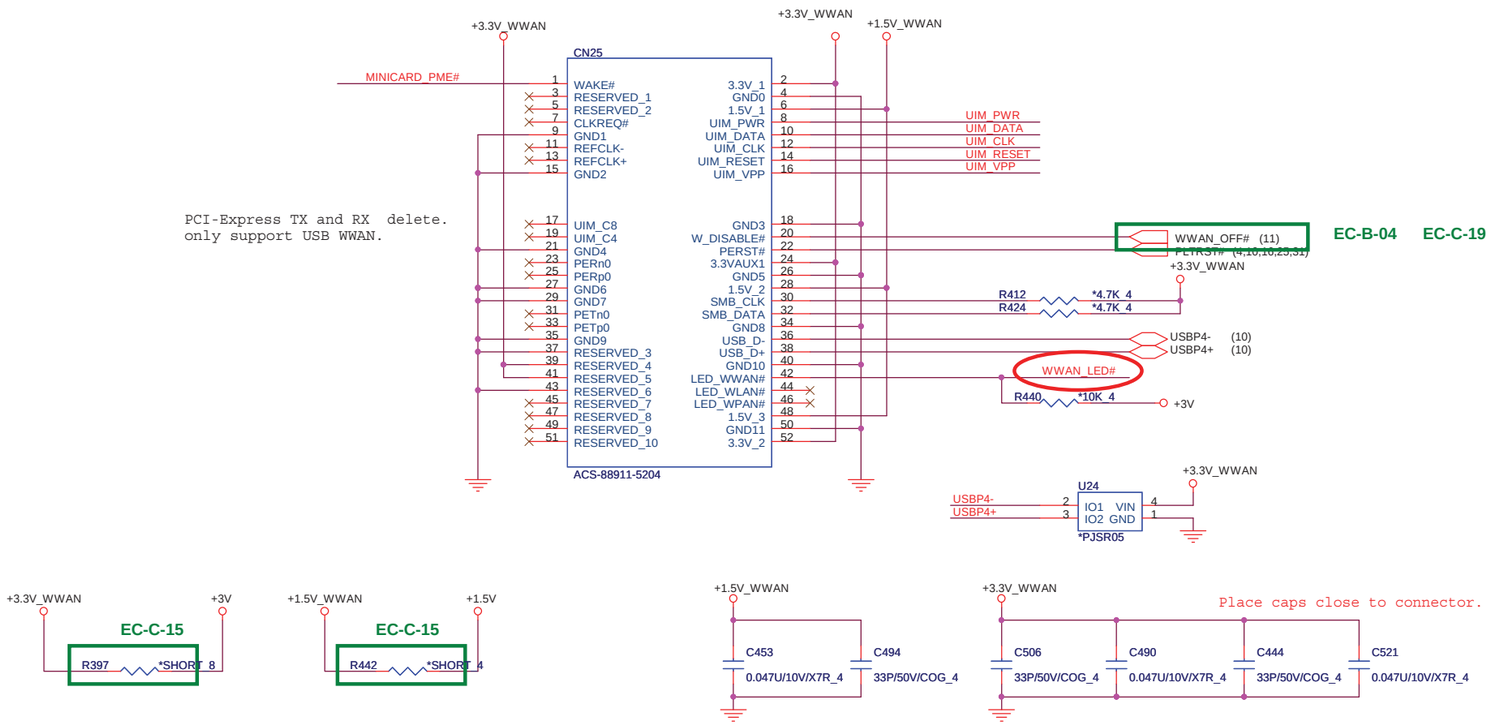
PROJECT KL5A	Quanta Computer Inc.
Size: Custom	Document Number: SATA HDD/ESATA/CD-ROM
Rev: 1A	
Date: Tuesday, January 04, 2011	Sheet 28 of 53

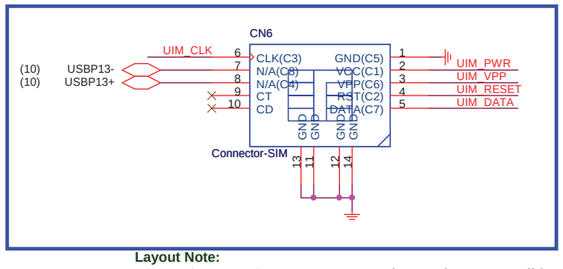
MiniCard WLAN connector

http://hobi-elektronika.net

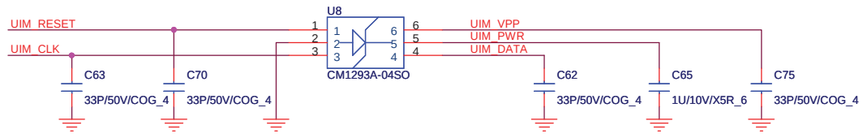


MiniCard WWAN (Reserved for KL9)





Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible

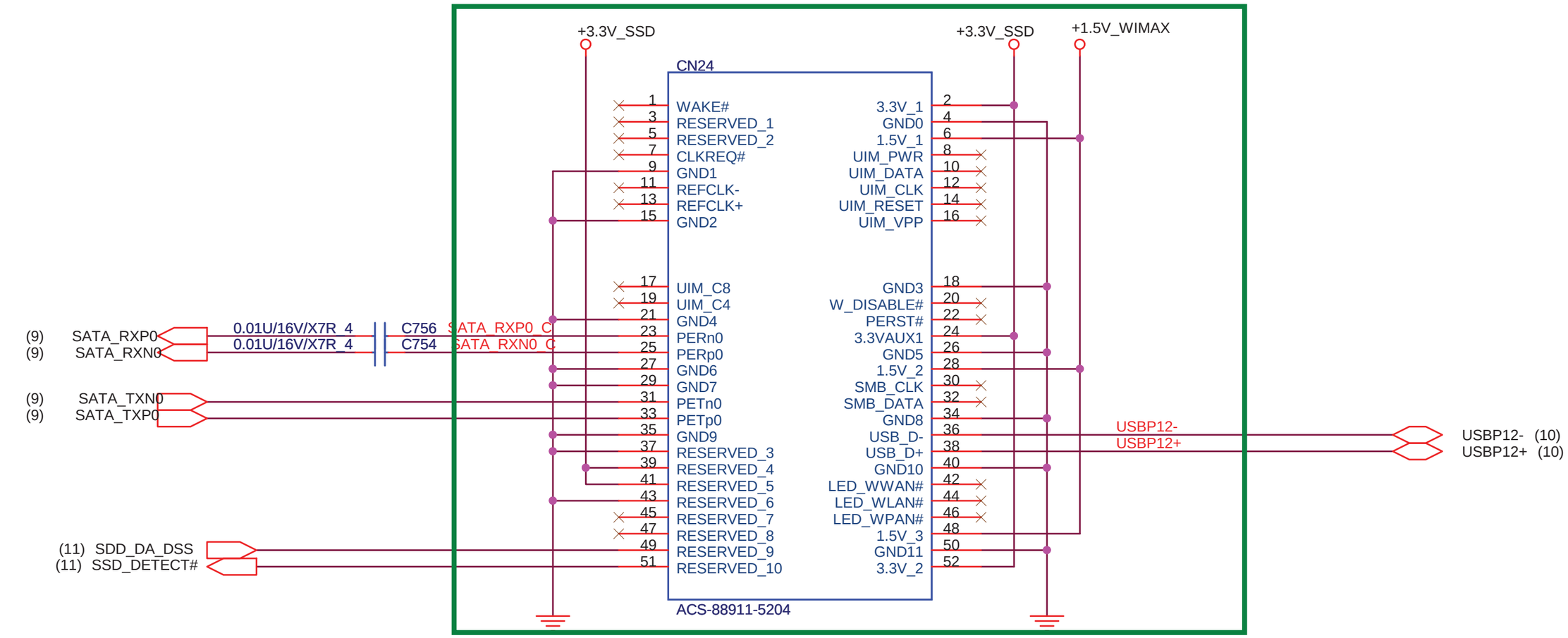


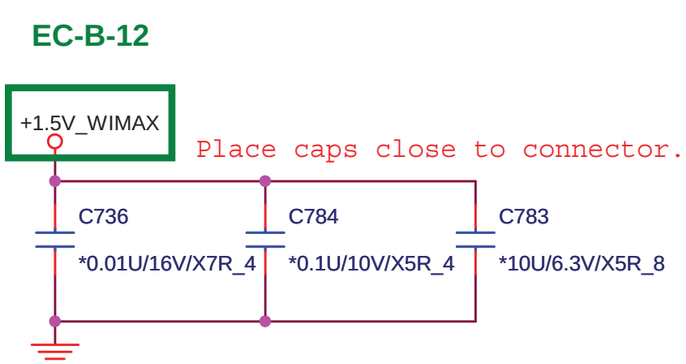
PROJECT : KL2D Quanta Computer Inc.		
Size Custom	Document Number MINI-Card (WLAN/WWAN)	Rev 1A
Date: Wednesday, January 05, 2011	Sheet 29 of 53	

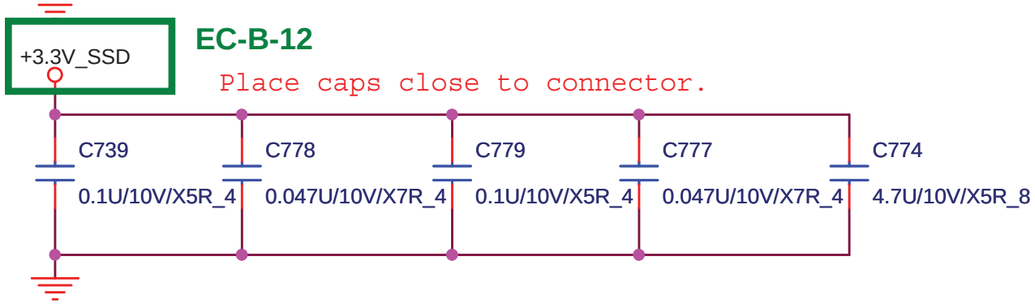
Mini PCI-E Card 3 SSD

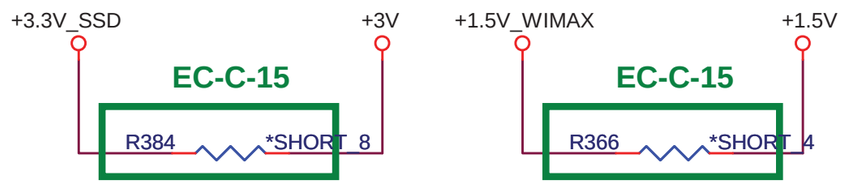
http://hobi-elektronika.net

(12,29,38,41,43) +1.5V
(8,9,10,11,12,14,15,17,22,23,24,26,27,28,29,31,36,37,38,40,41,42,46,47,48,49) +3V









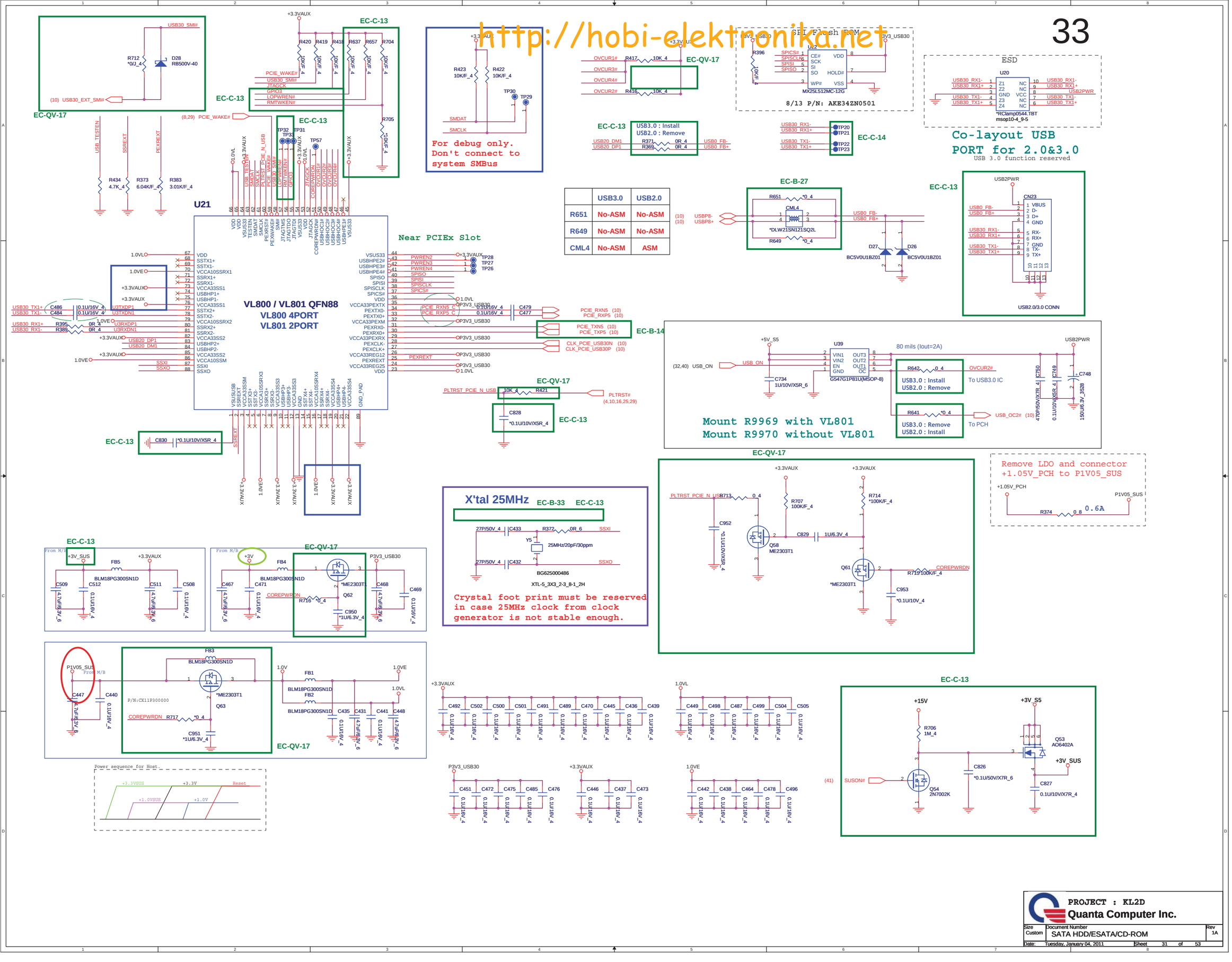
PROJECT :LL3A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI Card (SSD)	1E

Date: Tuesday, January 04, 2011 Sheet 30 of 53

http://hobi-elektronika.net



	USB3.0	USB2.0
R651	No-ASM	No-ASM
R649	No-ASM	No-ASM
CML4	No-ASM	ASM

PROJECT : KL2D

Quanta Computer Inc.

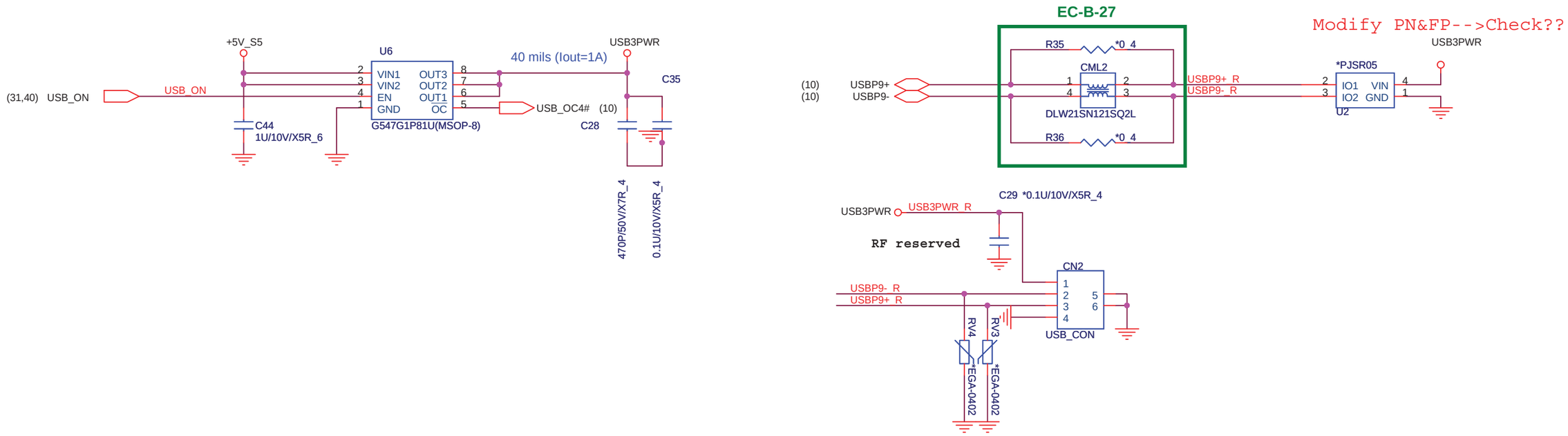
Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A

Date: Tuesday, January 04, 2011 Sheet 31 of 53

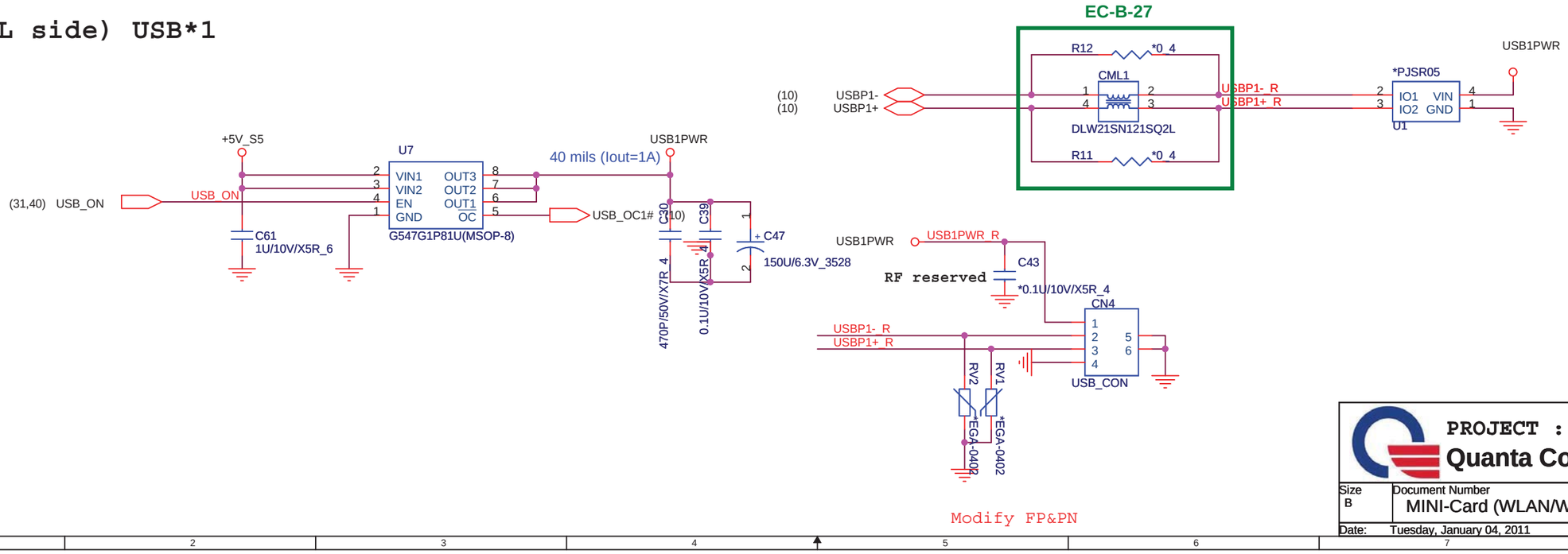
USB2.0*2

http://hobi-elektronika.net

External (R side) USB*1



External (L side) USB*1



PROJECT : KL2D

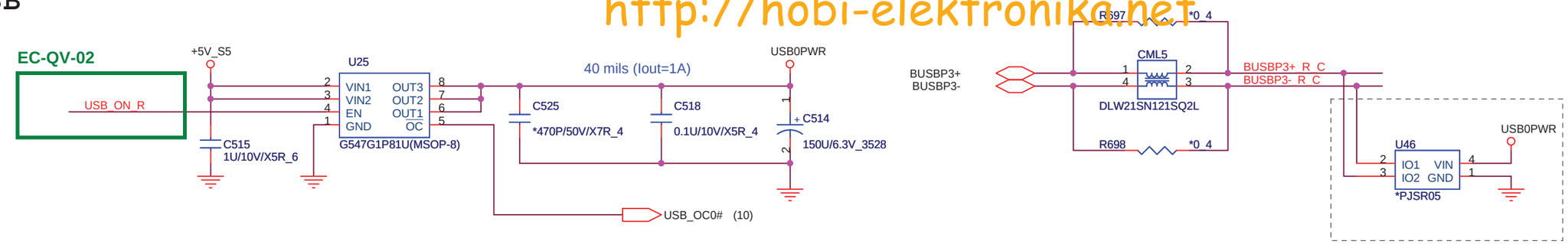
Quanta Computer Inc.

Size	Document Number	Rev
B	MINI-Card (WLAN/WWAN)	1A

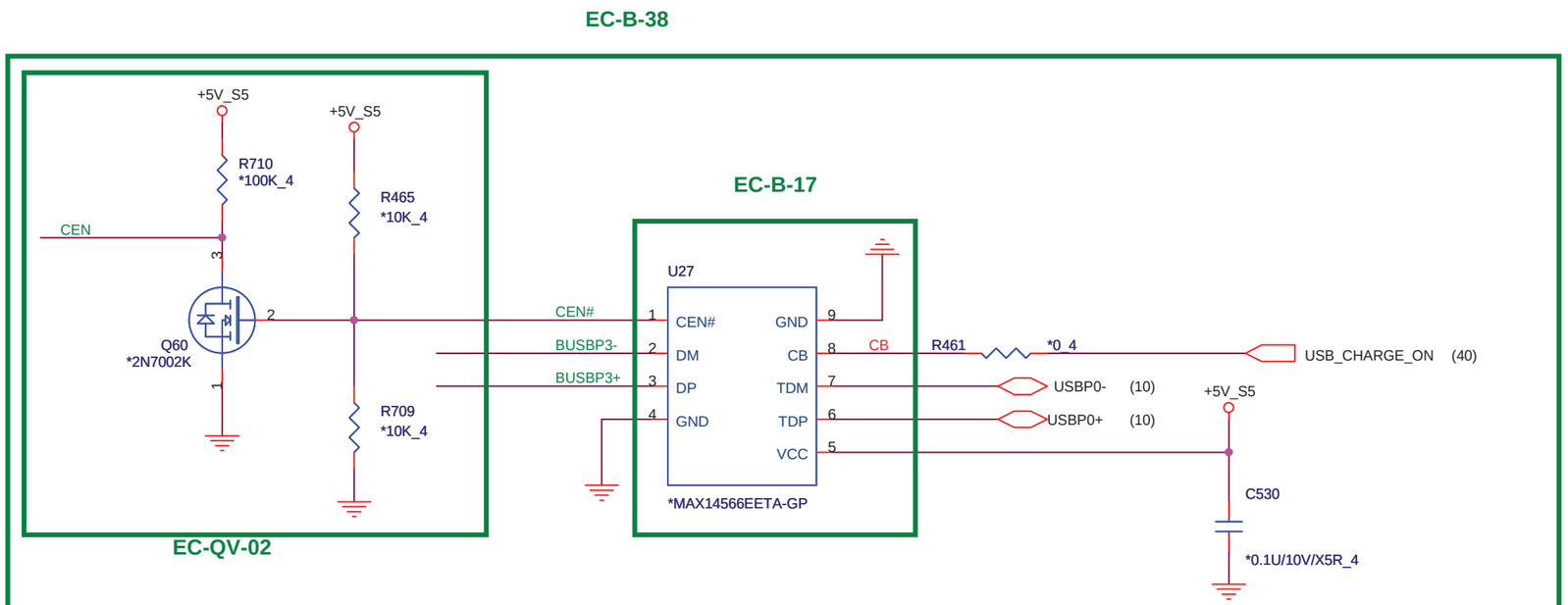
Date: Tuesday, January 04, 2011 Sheet 32 of 53

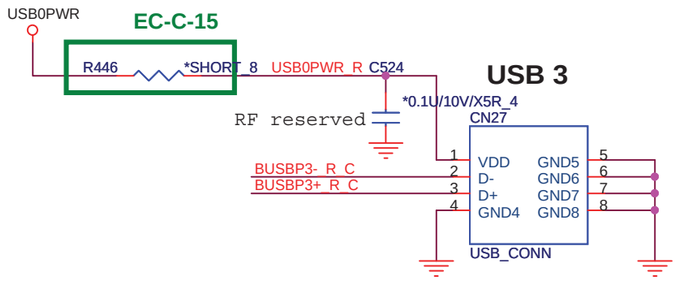
http://hobi-elektronika.net

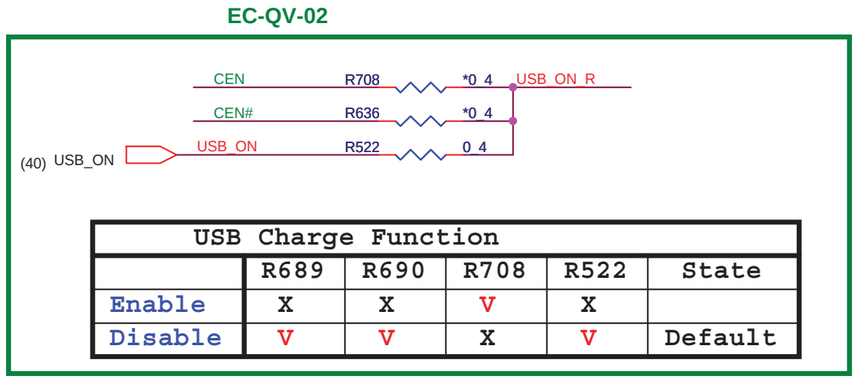
USB



USB charger







Stuff for bypass USB charger

USB Charge Function					
	R689	R690	R708	R522	State
Enable	X	X	V	X	
Disable	V	V	X	V	Default

PROJECT KL5A

Quanta Computer Inc.

Size	Document Number	Rev
B	USB Discharge	1A

Date: Tuesday, January 04, 2011 Sheet 33 of 53

G-SENSOR (3-Axial)

http://hobi-elektronika.net

(8,9,10,21,12,14,15,17,22,23,24,26,27,28,29,30,31,36,37,38,40,41,42,46,47,48,49) +3V
(24,28,31,38,41,43,44,45) +15V

EC-B-18

PROJECT :LL3A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	G-SENSOR	1E

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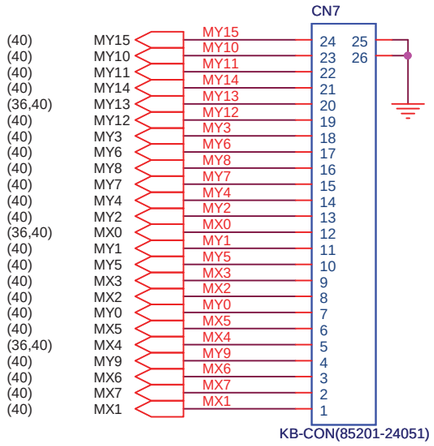
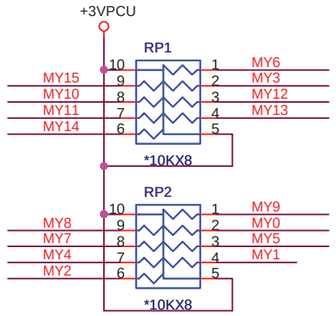
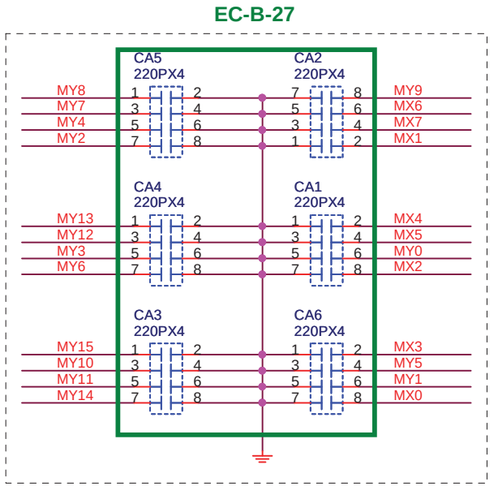
http://hobi-elektronika.net

KEYBOARD



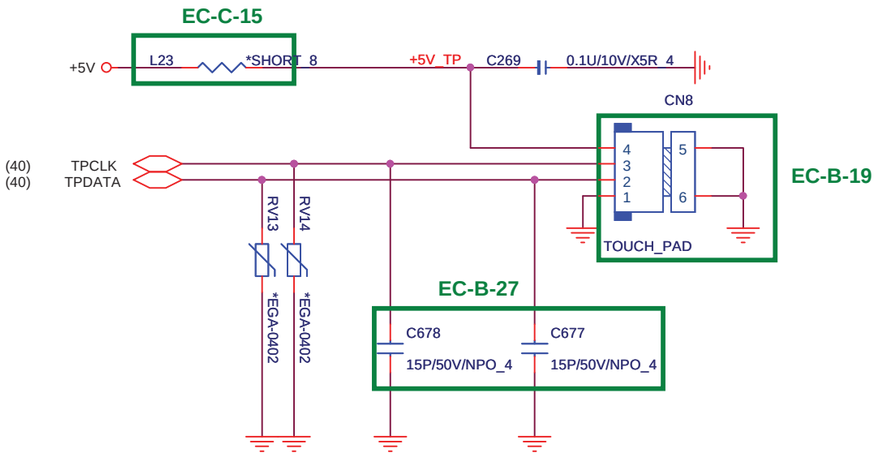
Follow LL3 KB





For EMI request

Touch pad



PROJECT KL5A

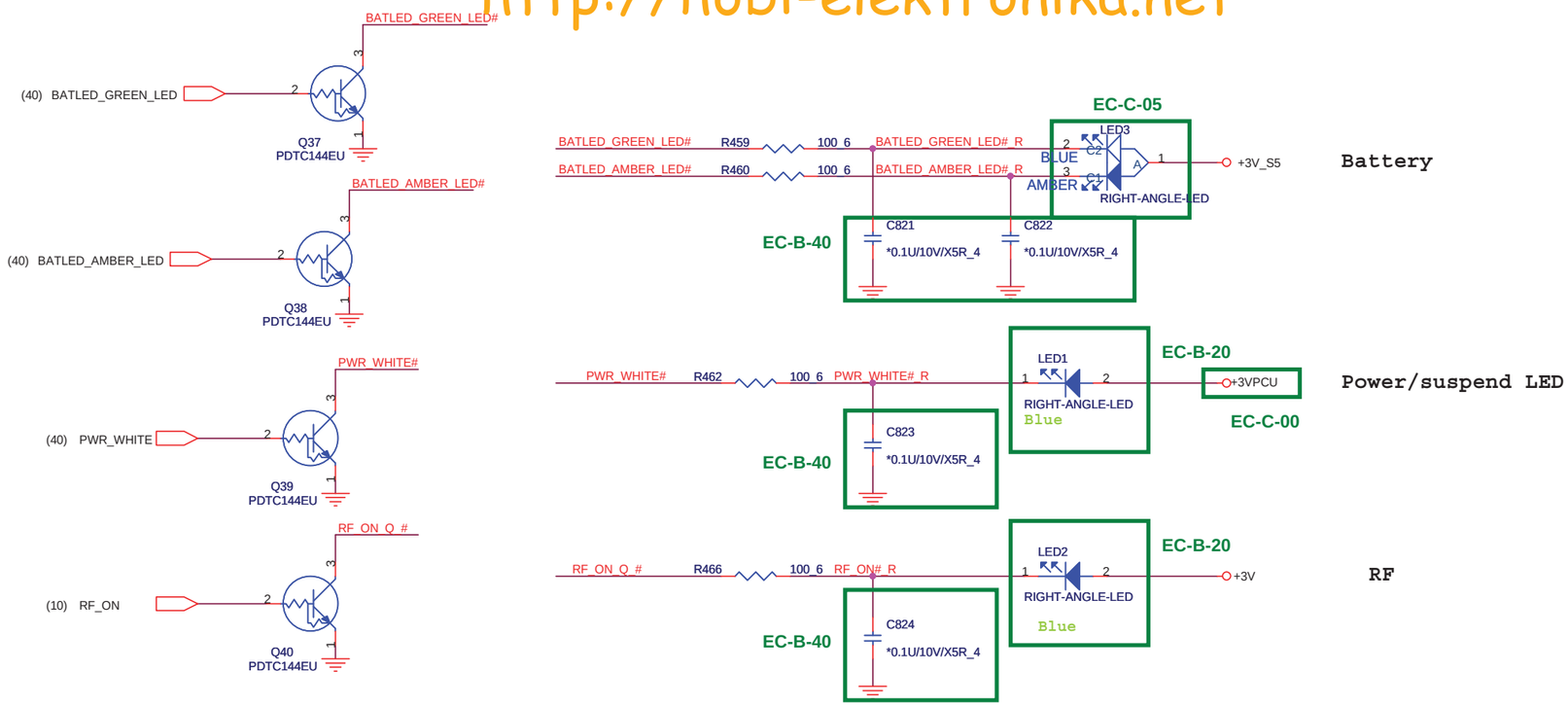
Quanta Computer Inc.

Size	Document Number	Rev
Custom	K/B, T/P	1A

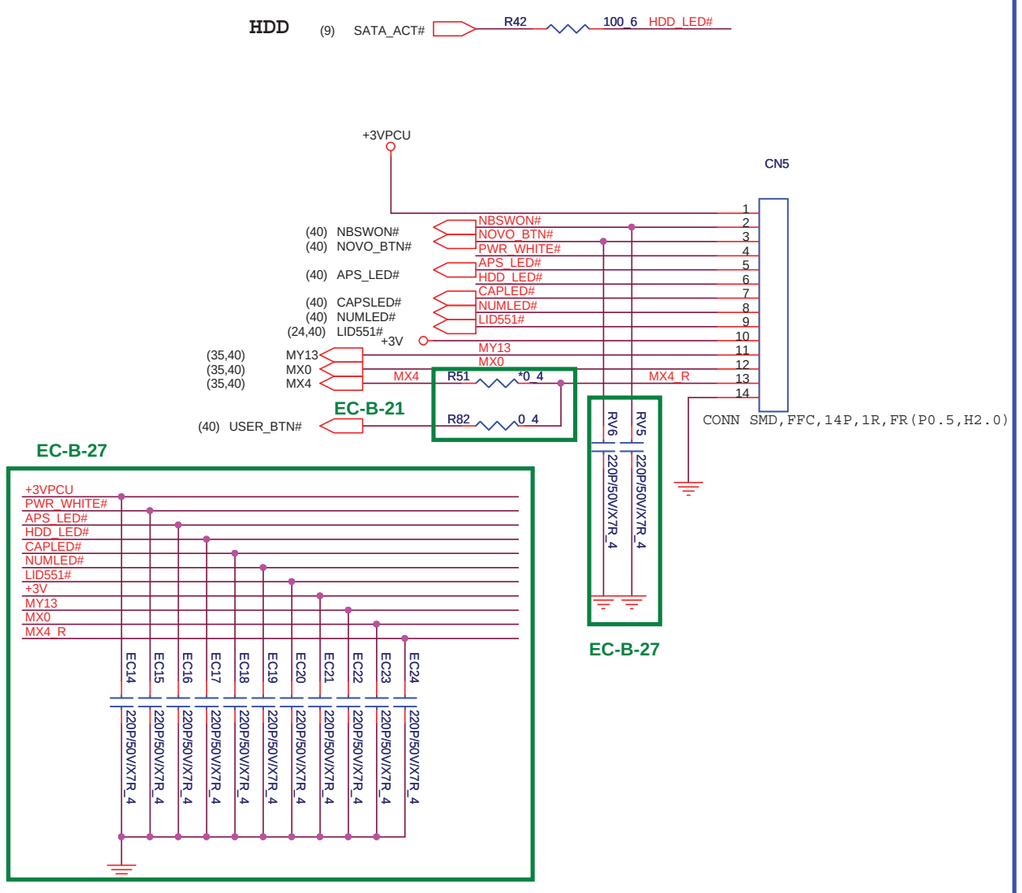
Date: Tuesday, January 04, 2011 Sheet 35 of 53

http://hobi-elektronika.net

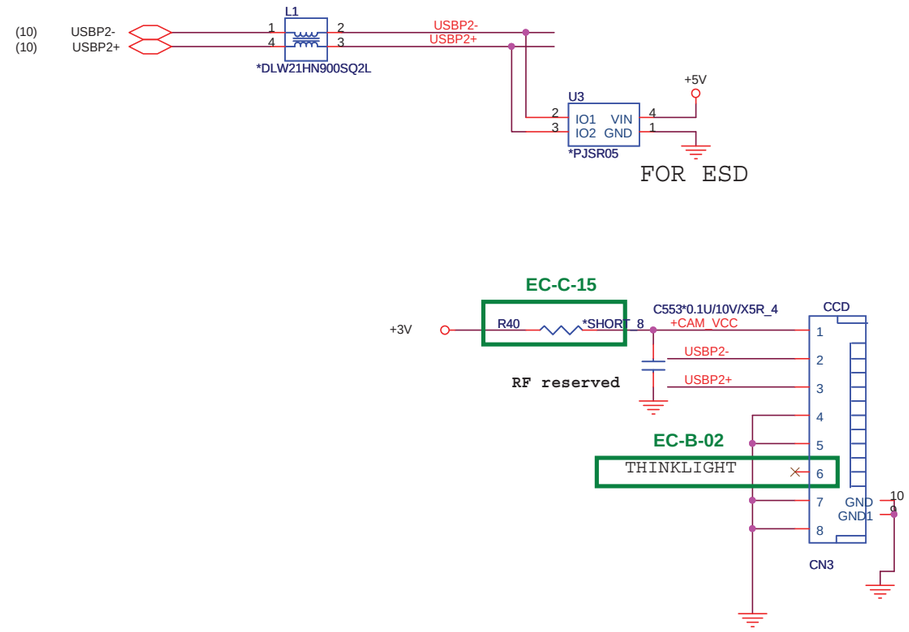
POWER / Battery /RF LED



B to B connector



CAMERA & Keyboard light



PROJECT : KL2D			
Quanta Computer Inc.			
Size: Custom	Document Number: B TO B CON/LED/CCD		Rev: 1A
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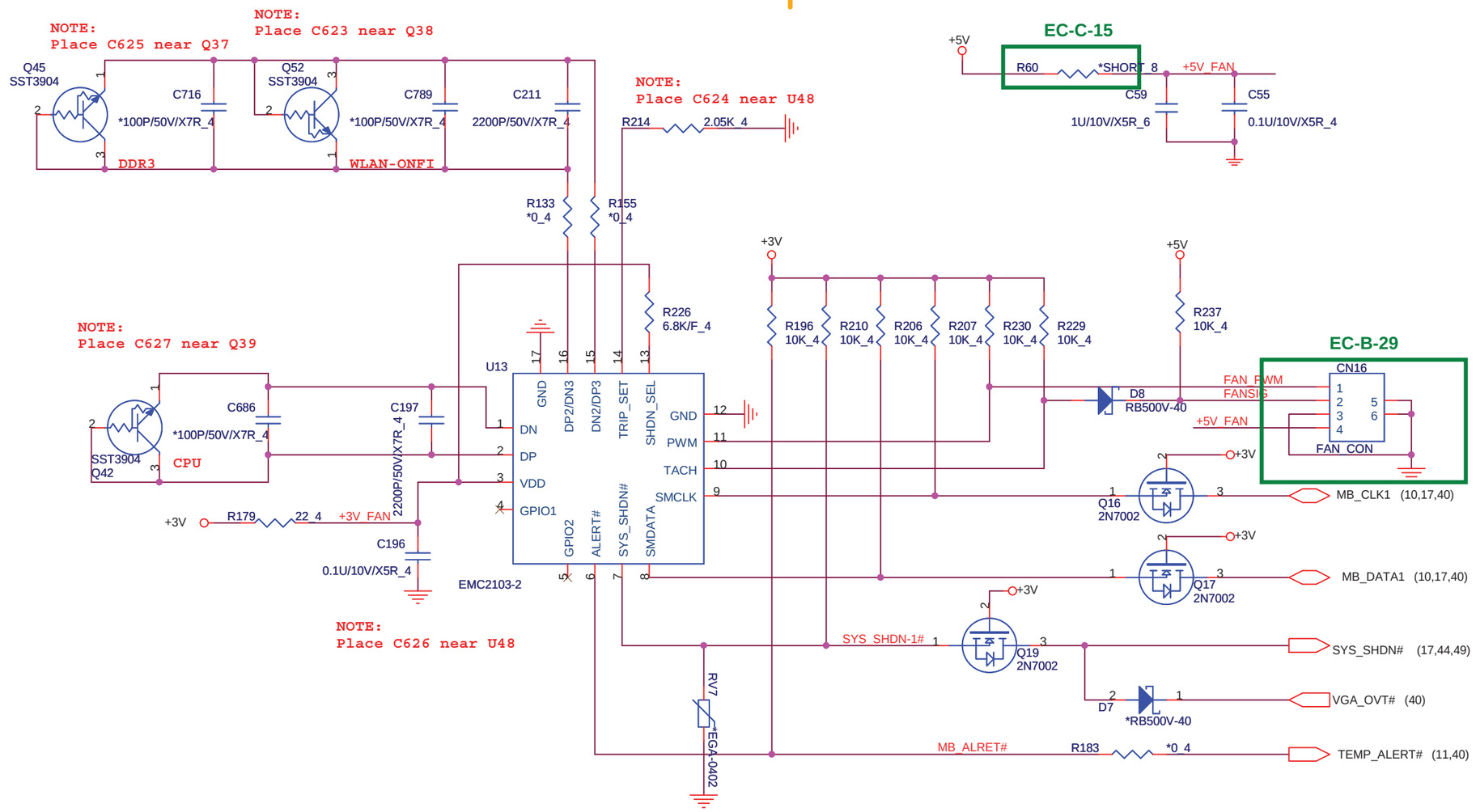
FAN CONTROL

http://hobi-elektronika.net



PROJECT KL5A

Quanta Computer Inc.

Size	Document Number	Rev
B	FAN /THERMAL	1A

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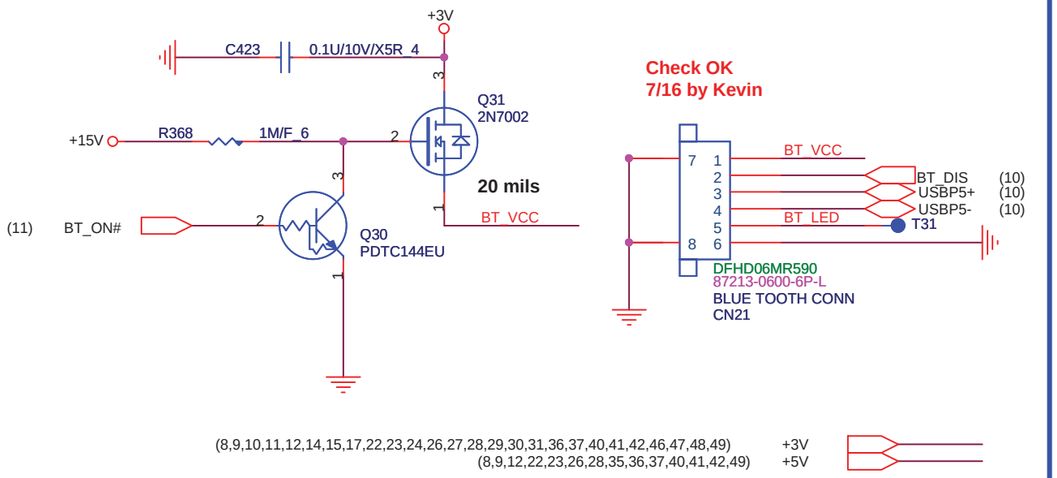
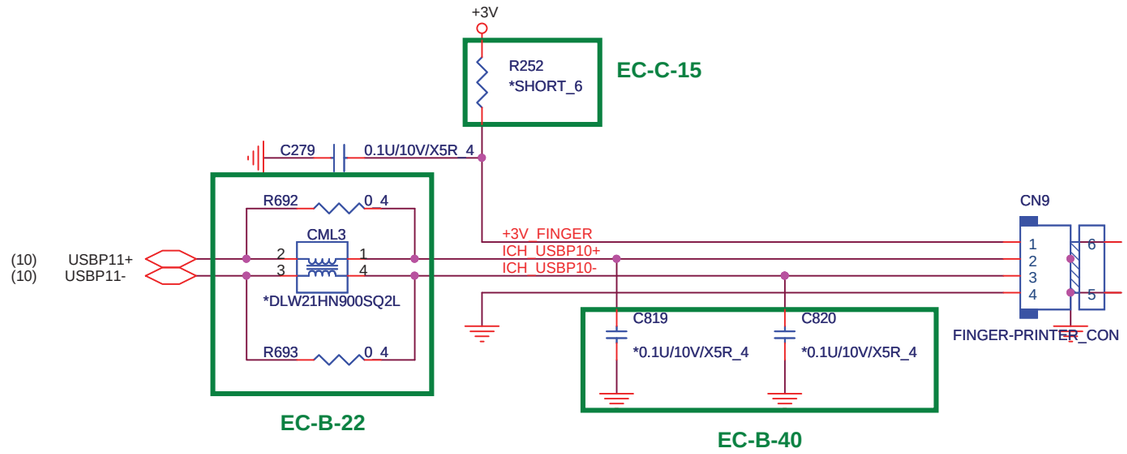
http://hobi-elektronika.net

BLUETOOTH



FINGER PRINTER

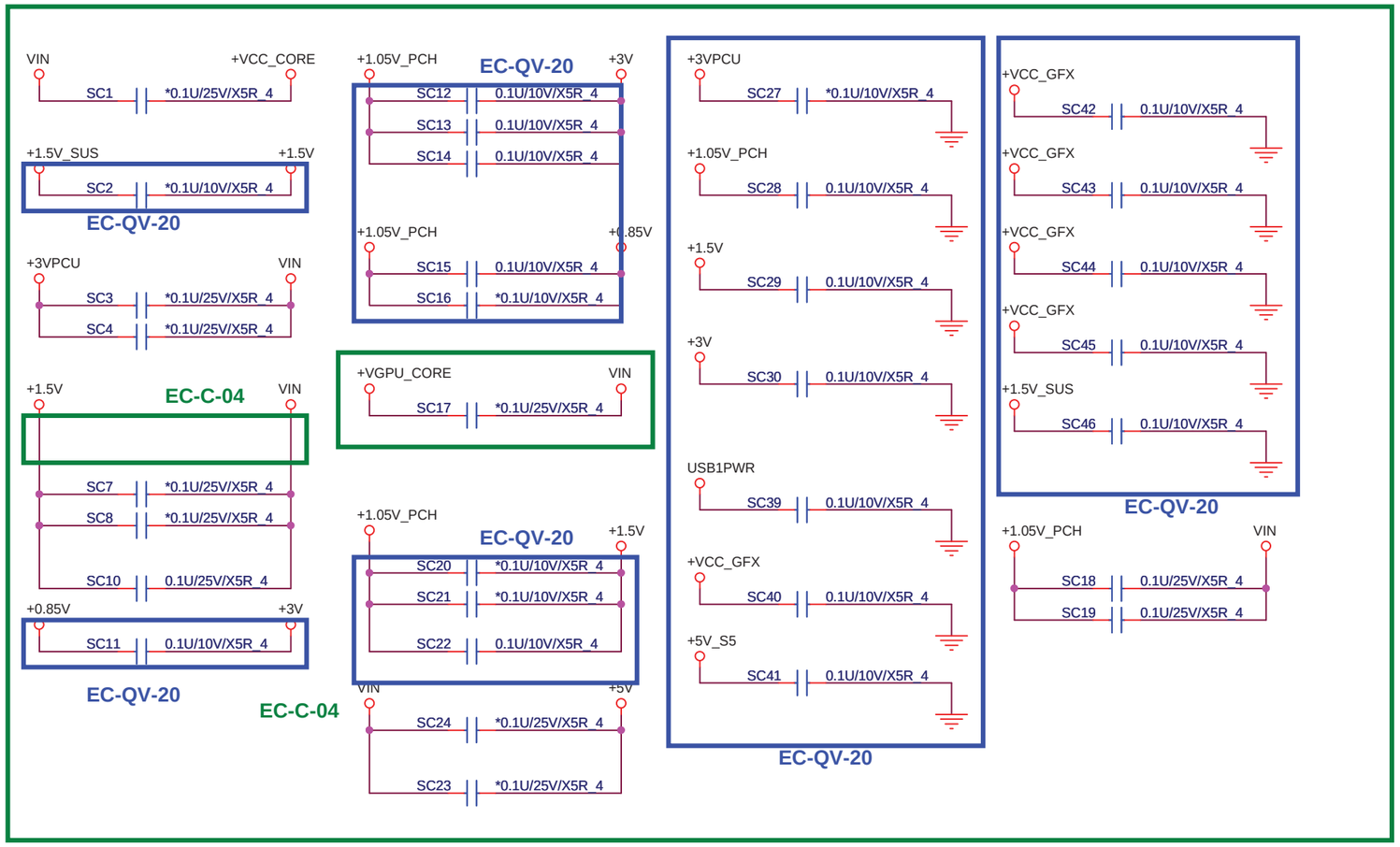


TPM

EC-B-23

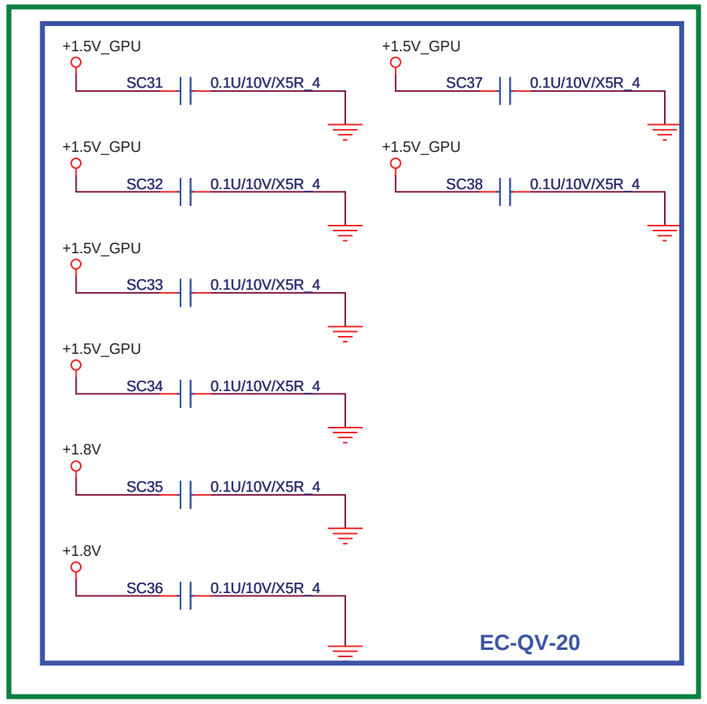
ESD suggestions

EC-B-28



EMI suggestions

EC-C-01



PROJECT :LL3A

Quanta Computer Inc.

Size	Document Number	Rev
B	BT/FP/TPM	1E

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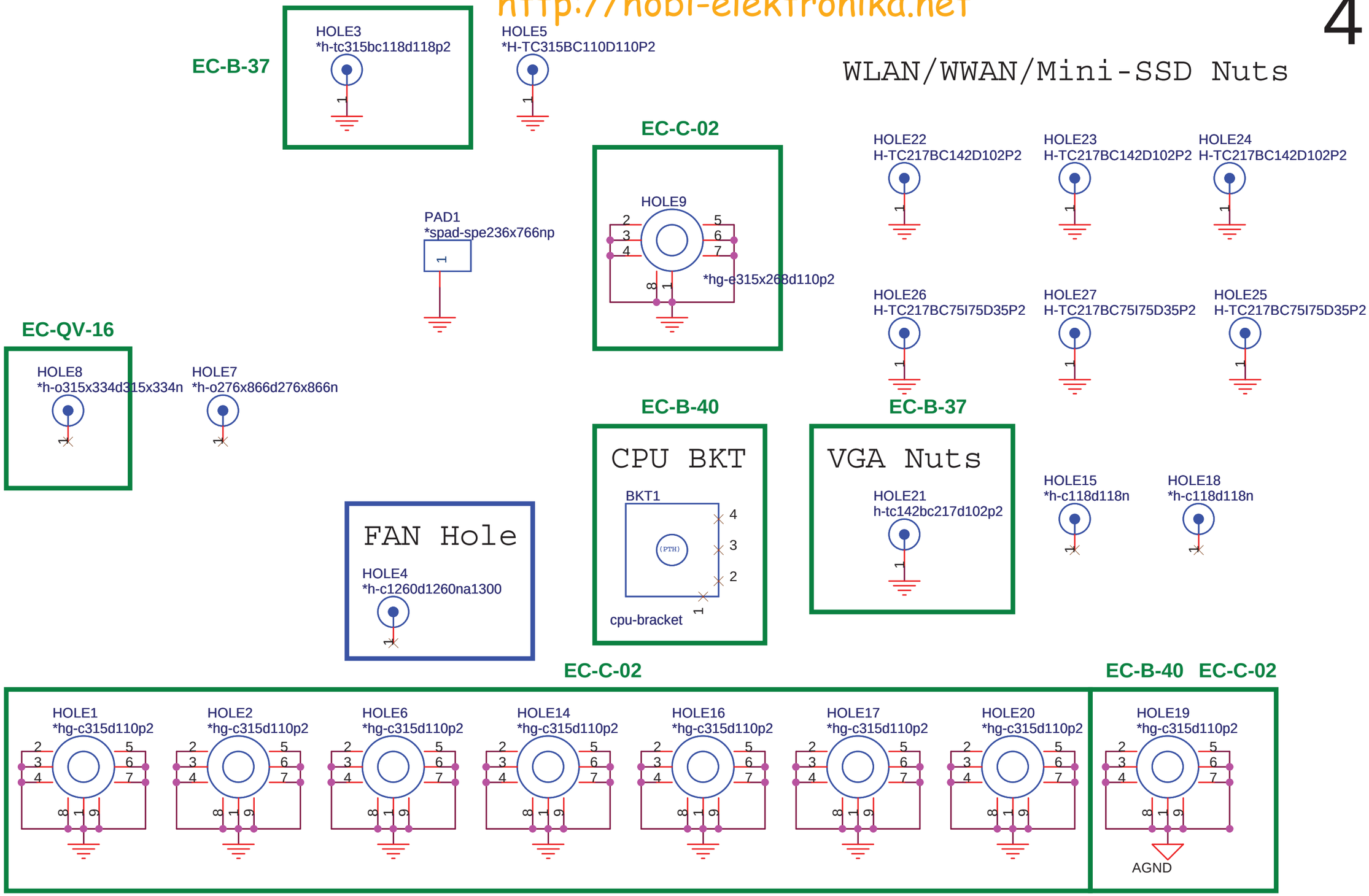
http://hobi-elektronika.net

WLAN/WWAN/Mini-SSD Nuts



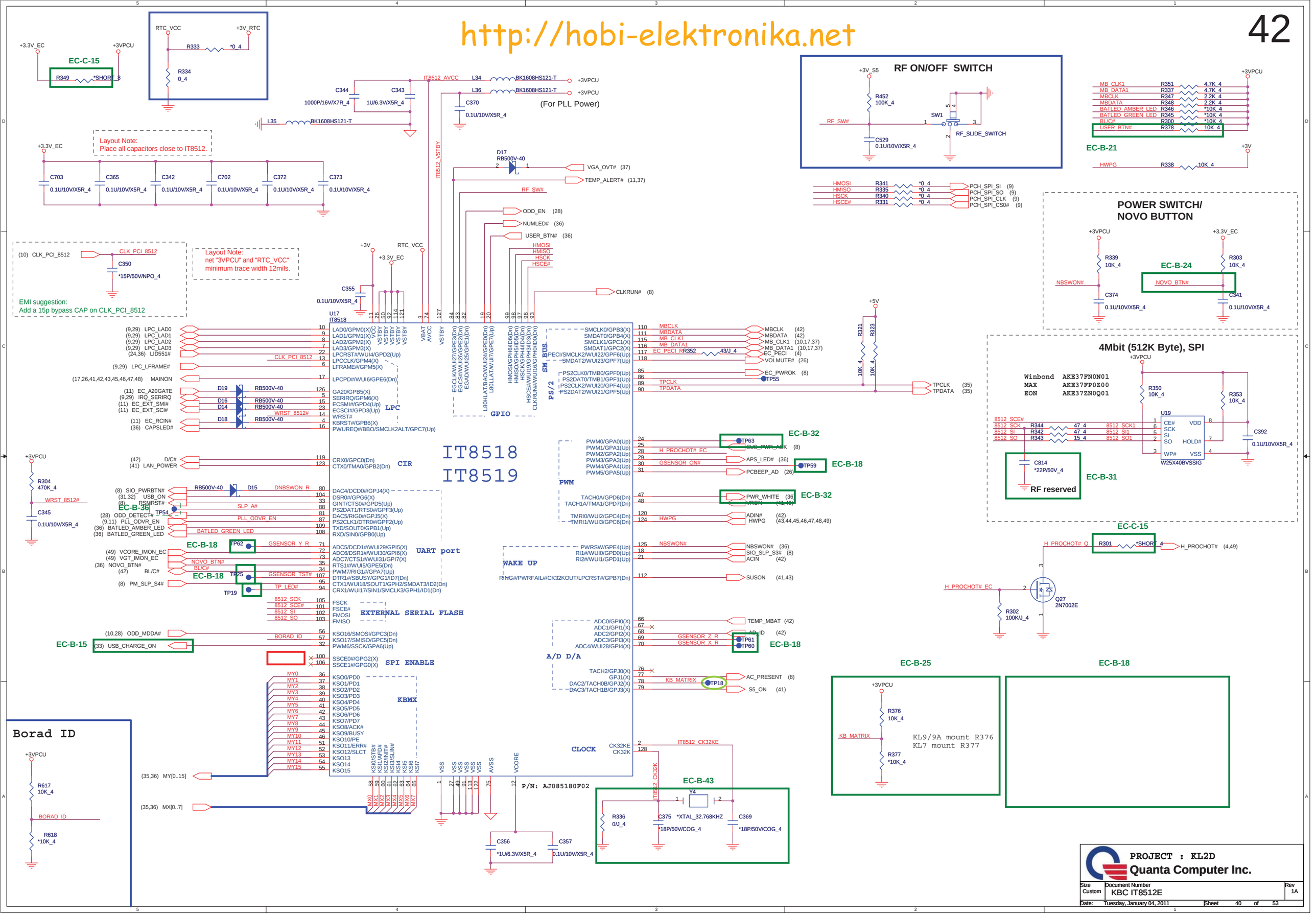
PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
A	HOLD & SKEW	1A

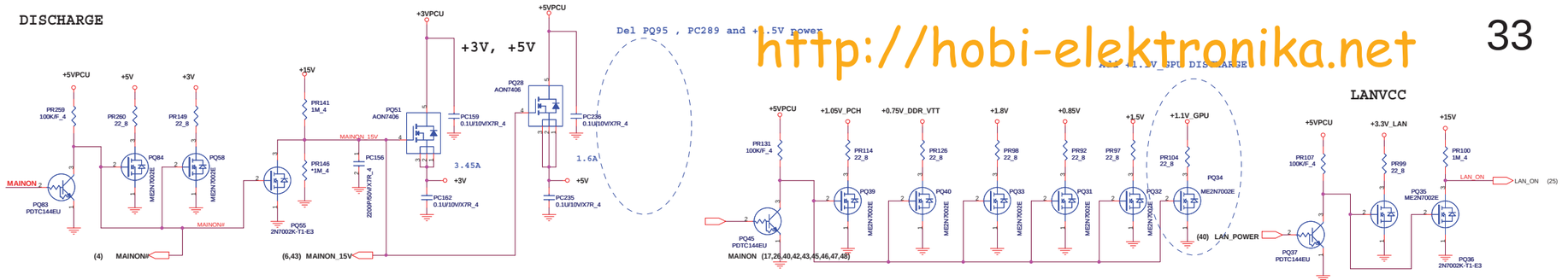
Date: Tuesday, January 04, 2011 Sheet 39 of 53

http://hobi-elektronika.net

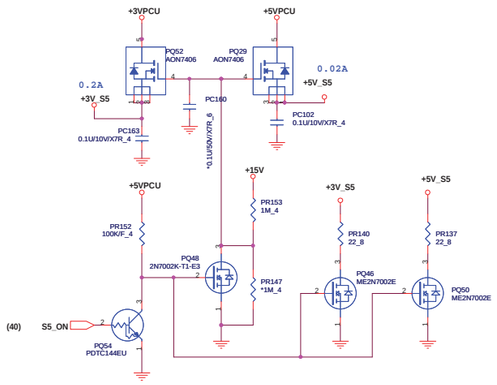


http://hobi-elektronika.net

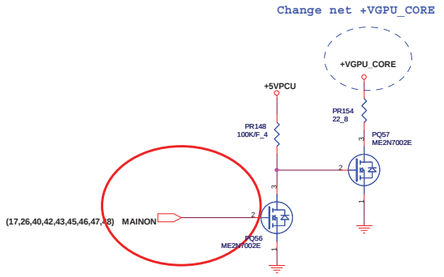
DISCHARGE

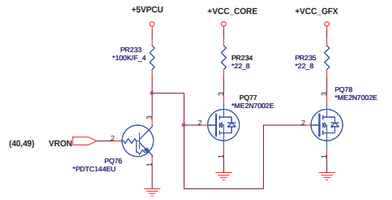


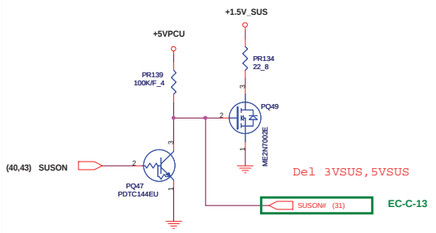
3V_S5, 5V_S5



Change net +VGPU_CORE







PROJECT KL5A Quanta Computer Inc.		
Size D	Document Number Discharge	Rev 1A
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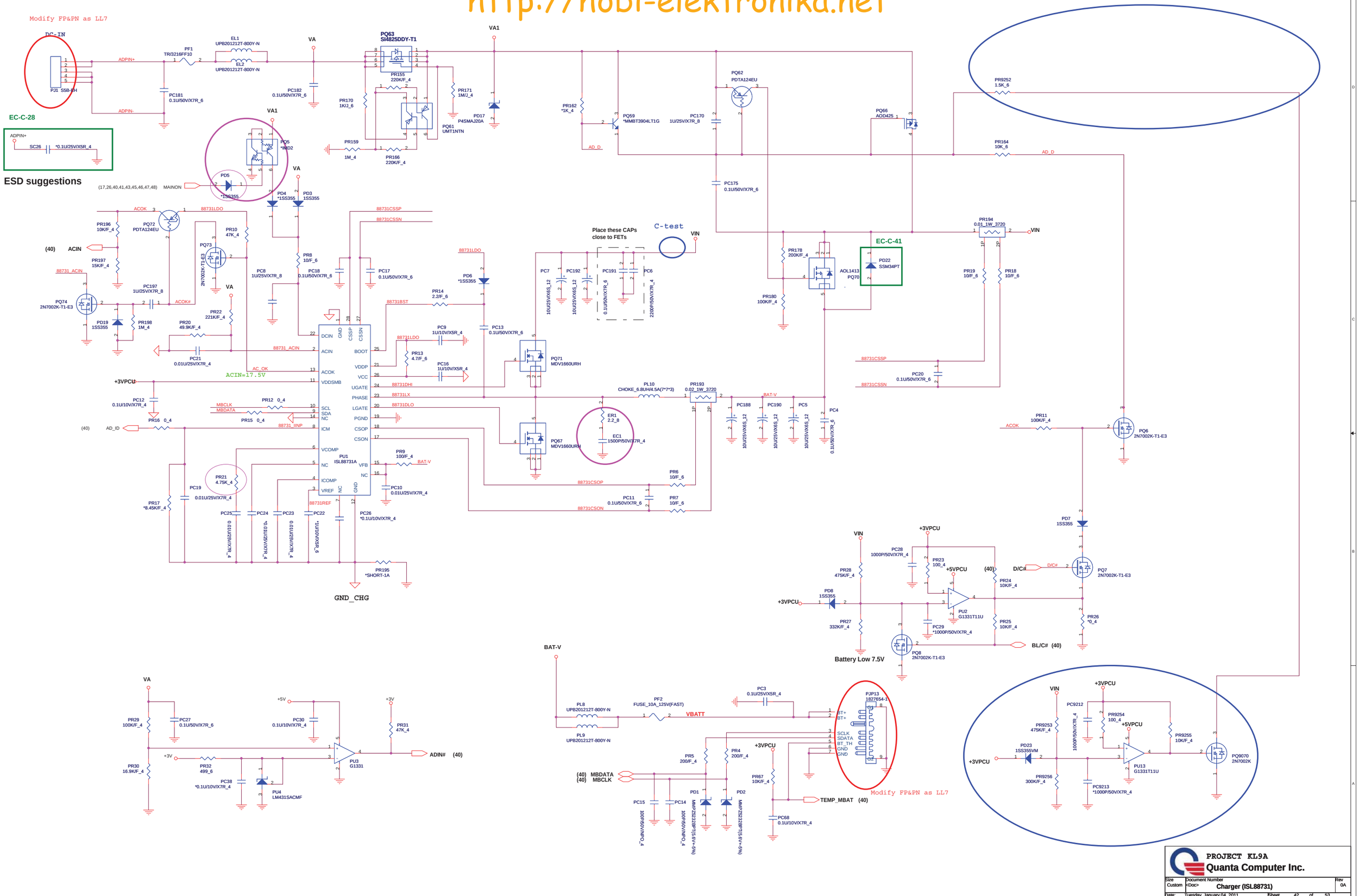


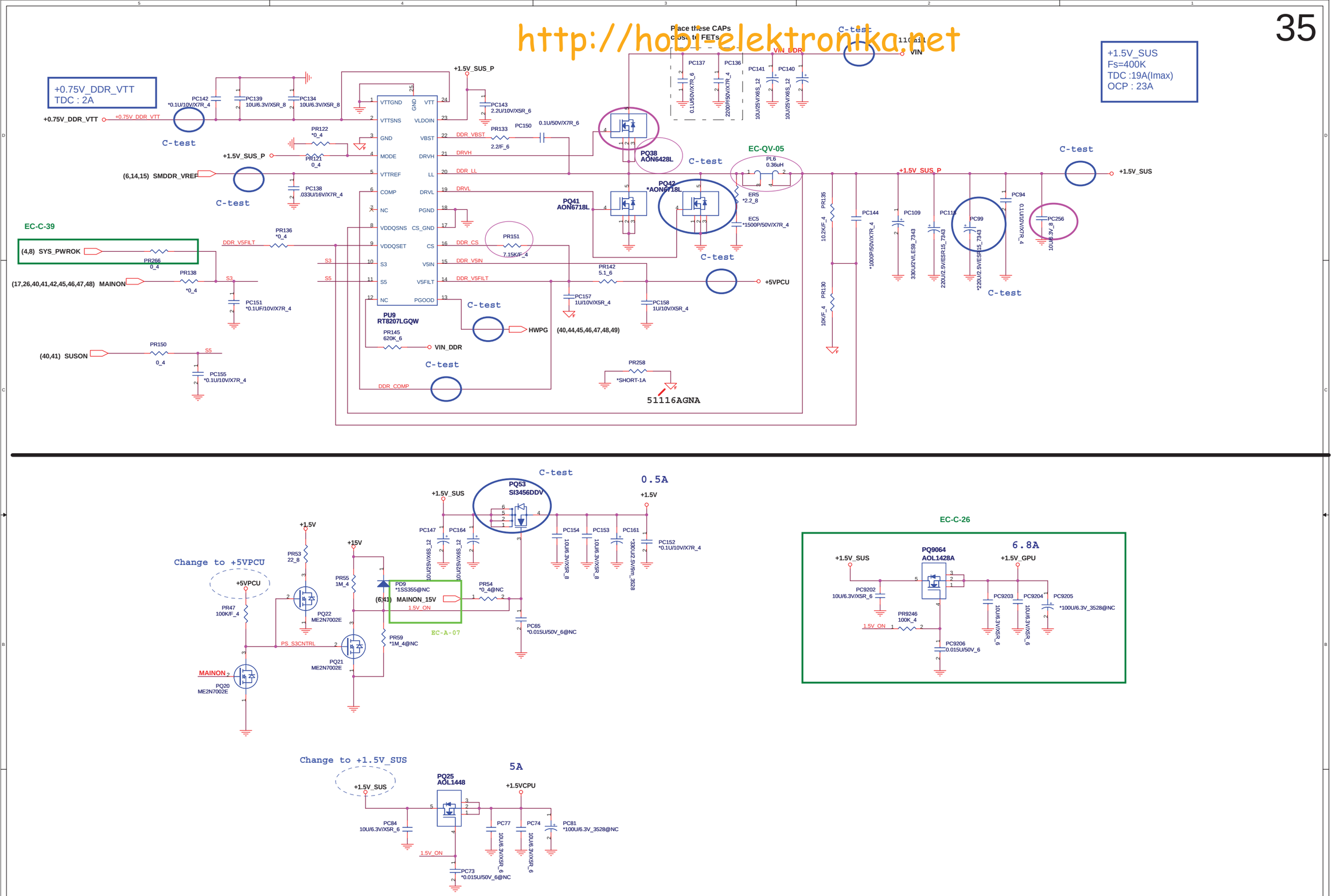
PROJECT KL9A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Charger (ISL88731)	0A

Date: Tuesday, January 04, 2011 Sheet 42 of 53

http://hobi-elektronika.net



PROJECT KL5A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3/0.75V(RT8207AGQW)	1A

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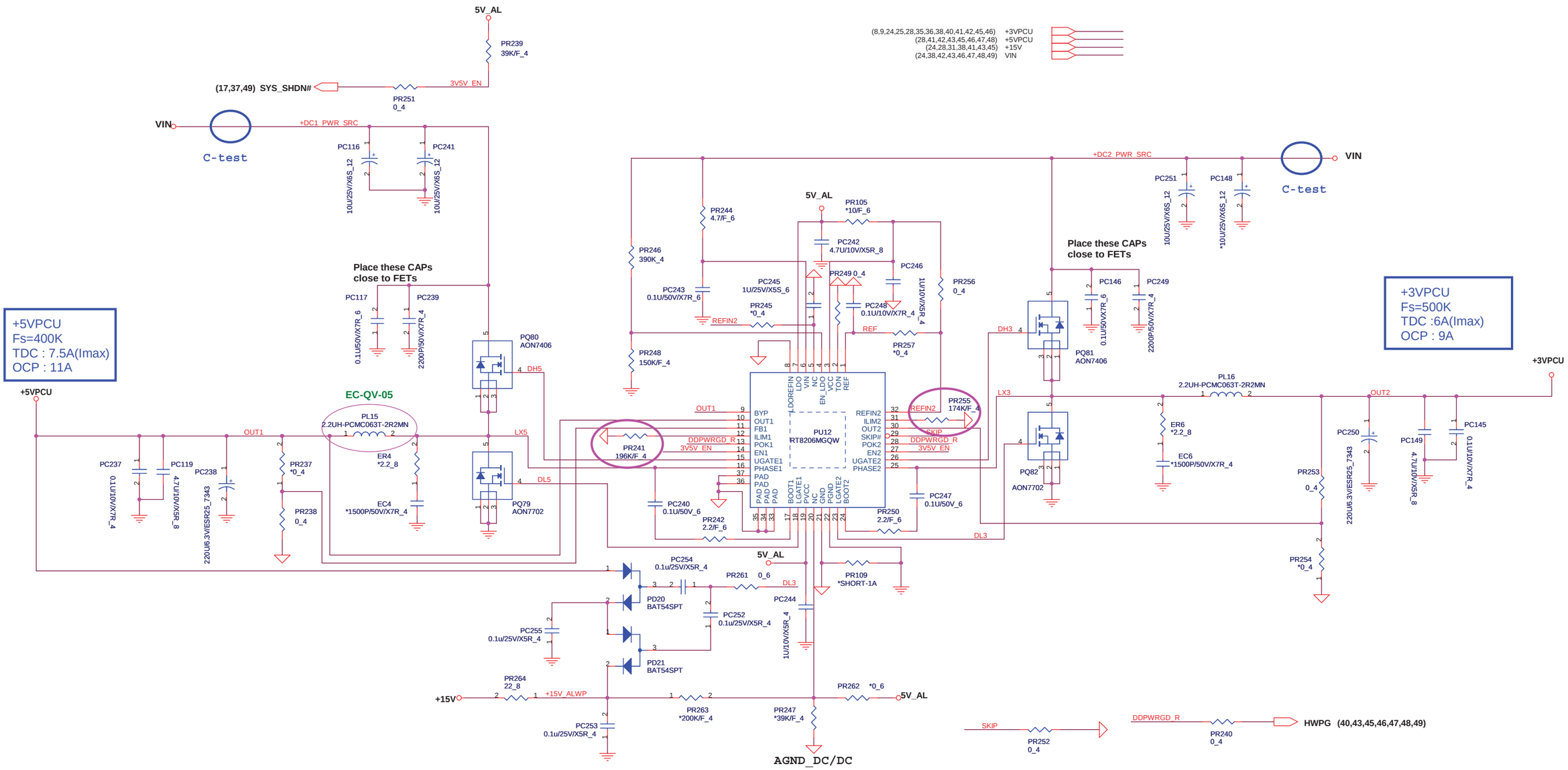

PROJECT KL5A

Quanta Computer Inc.

Size	Document Number	Rev
C	3V/5V (RT8206MGQW)	1A

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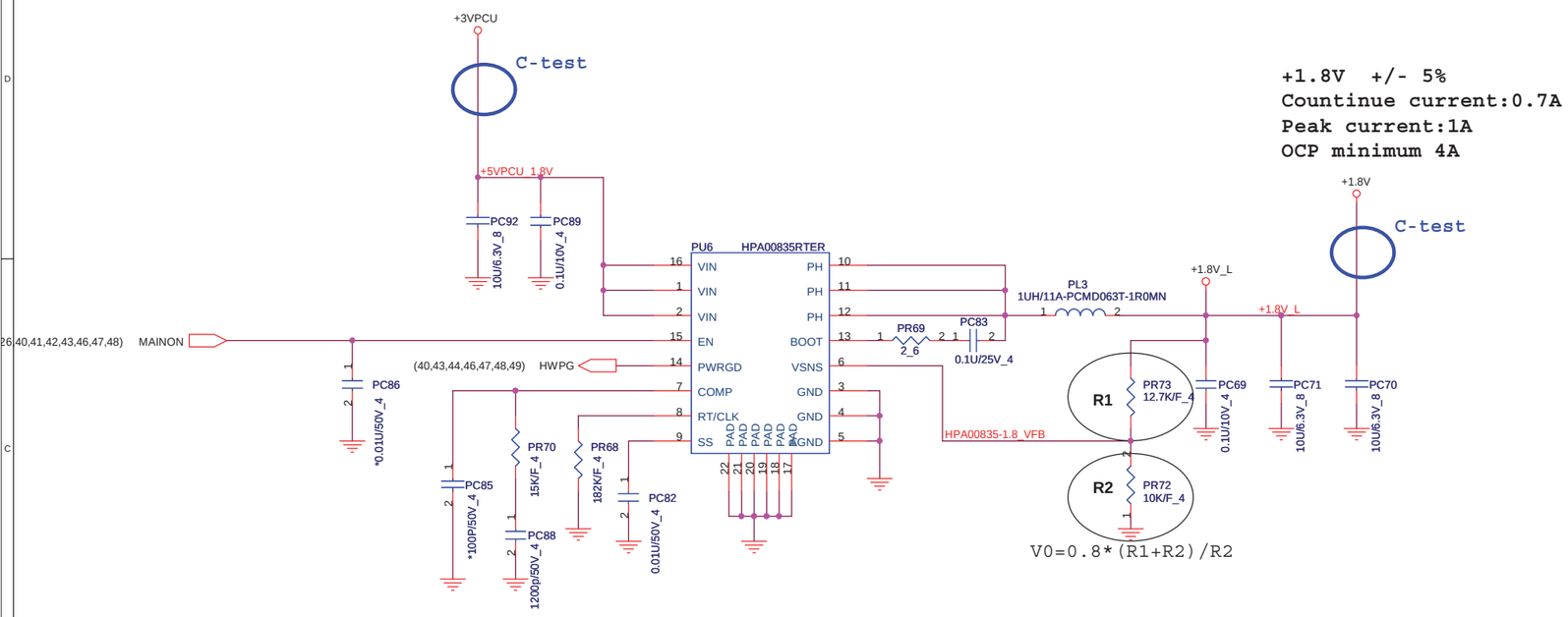
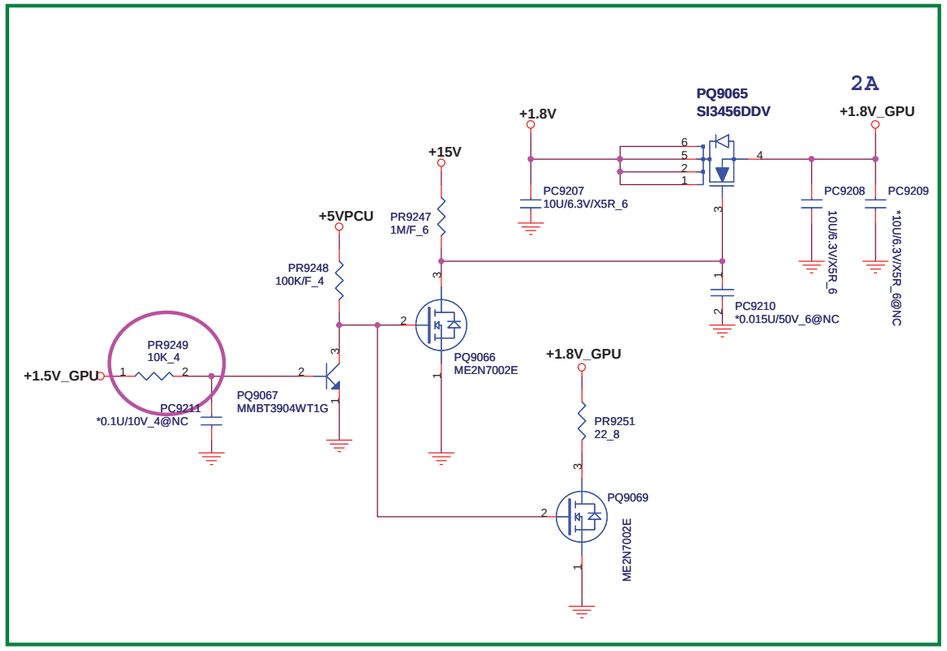


+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A
OCP minimum 4A

EC-C-26



PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.8V (HPA00835RTER)	1A

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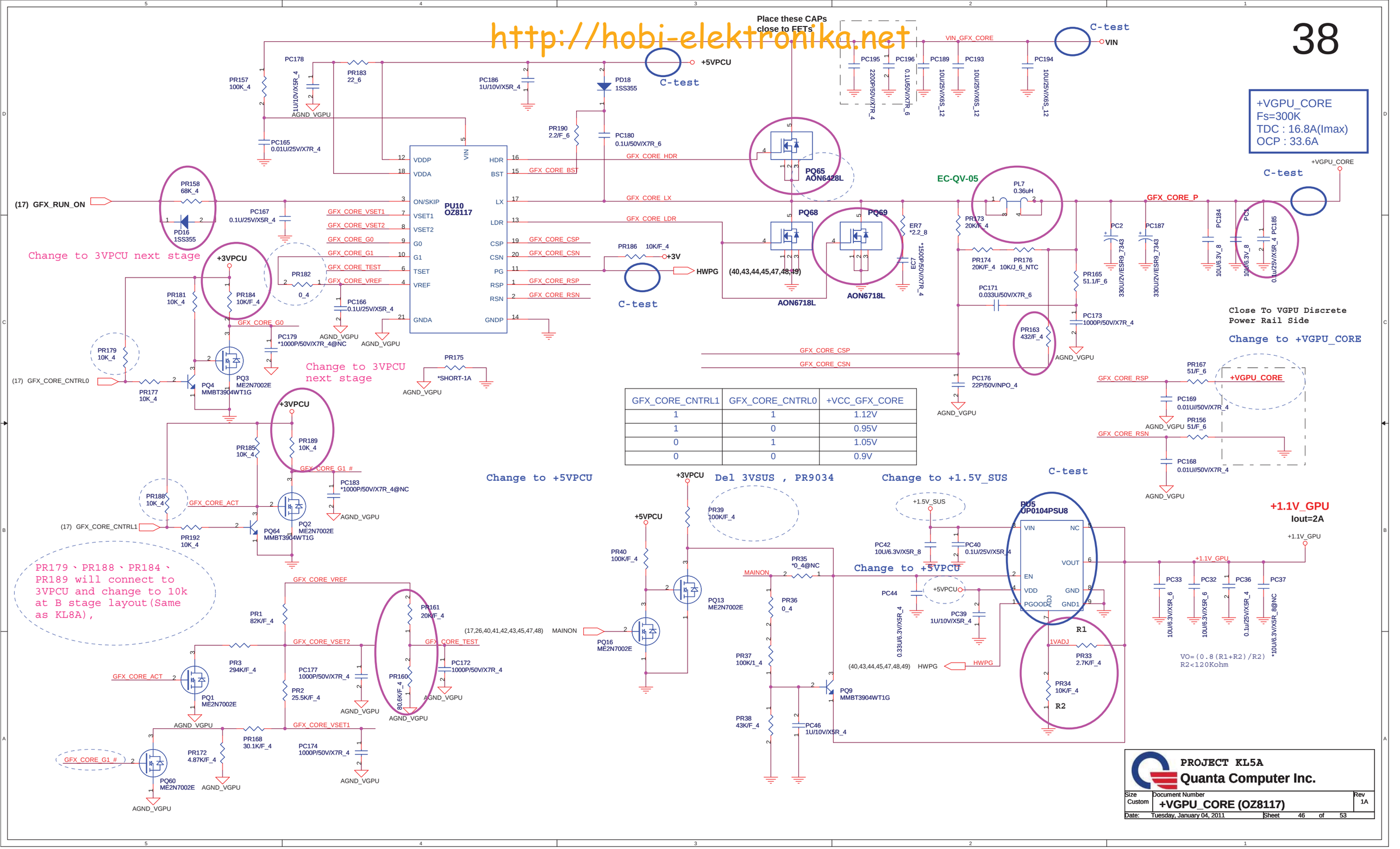

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VCC_GFX_CORE
1	1	1.12V
1	0	0.95V
0	1	1.05V
0	0	0.9V

PROJECT KL5A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGPU_CORE (OZ8117)	1A

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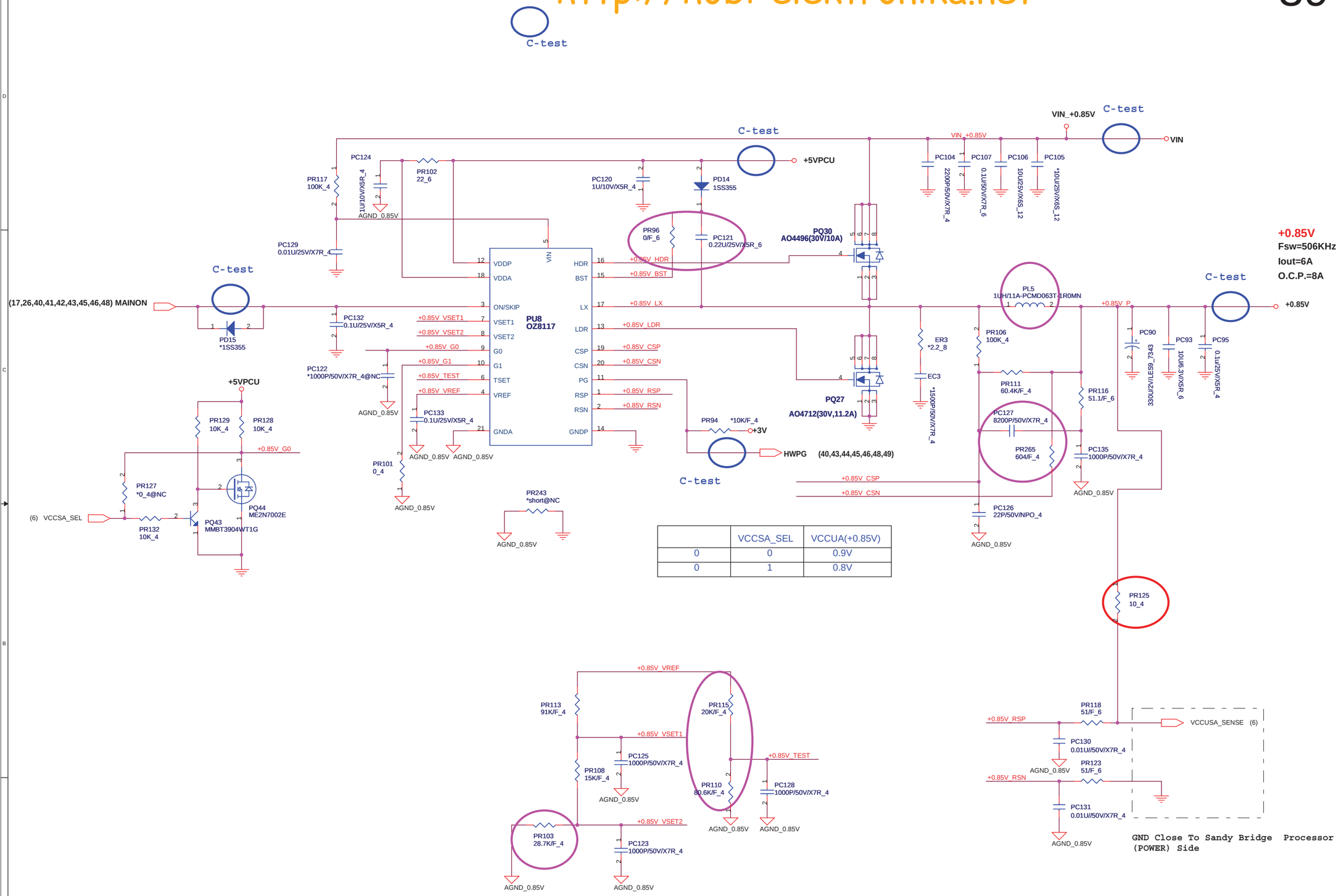

	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V

PROJECT KL5A

Quanta Computer Inc.

Size	Document Number	Rev
C	+0.85V (OZ8117)	1A

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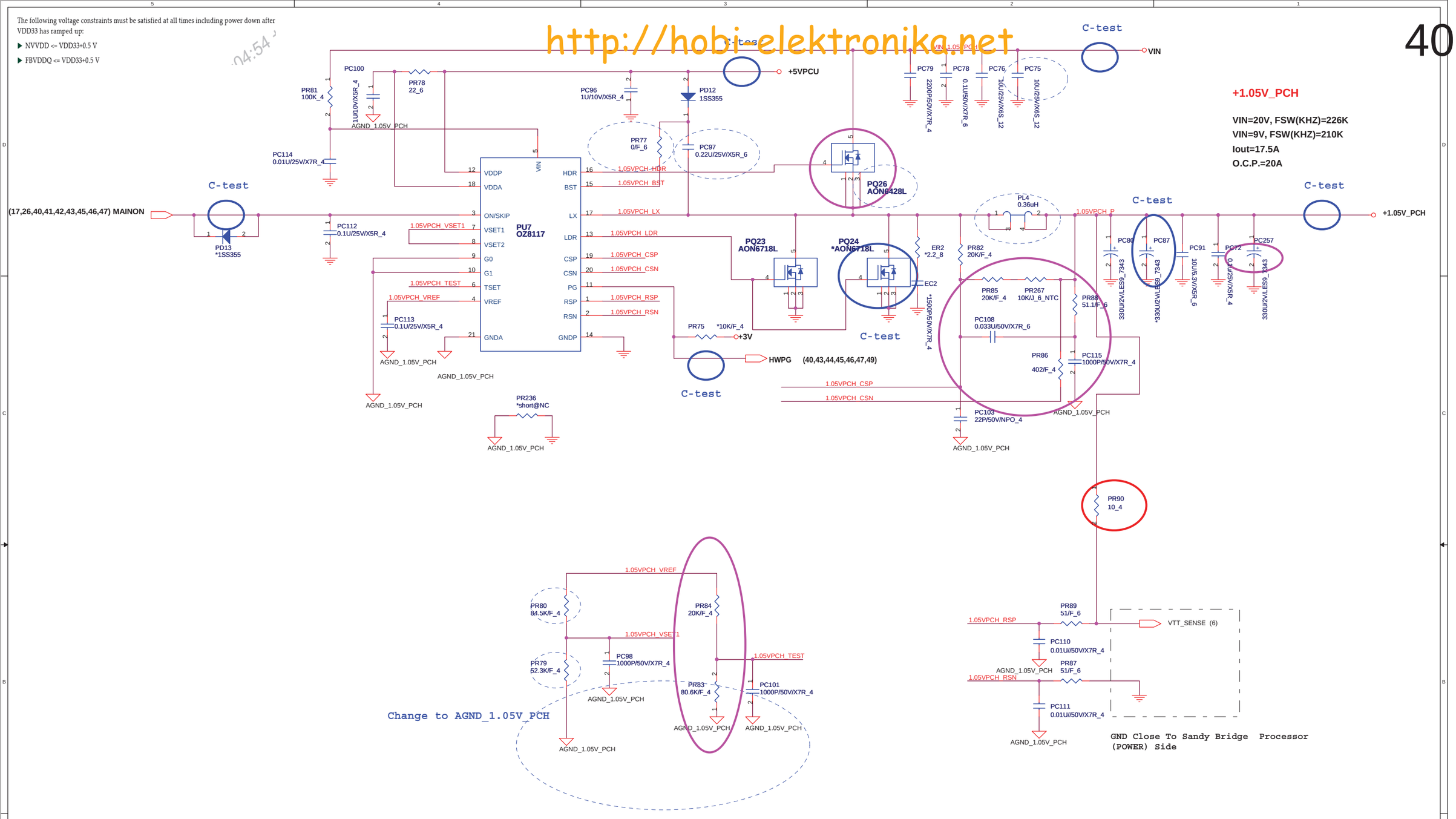
The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

- NVVDD <= VDD33+0.5 V
- FBVDDQ <= VDD33+0.5 V



Del +1.5V SW

PROJECT KL5A

Quanta Computer Inc.

Size	Document Number	Rev
C	+1.05_PCH (OZ8117)	1A

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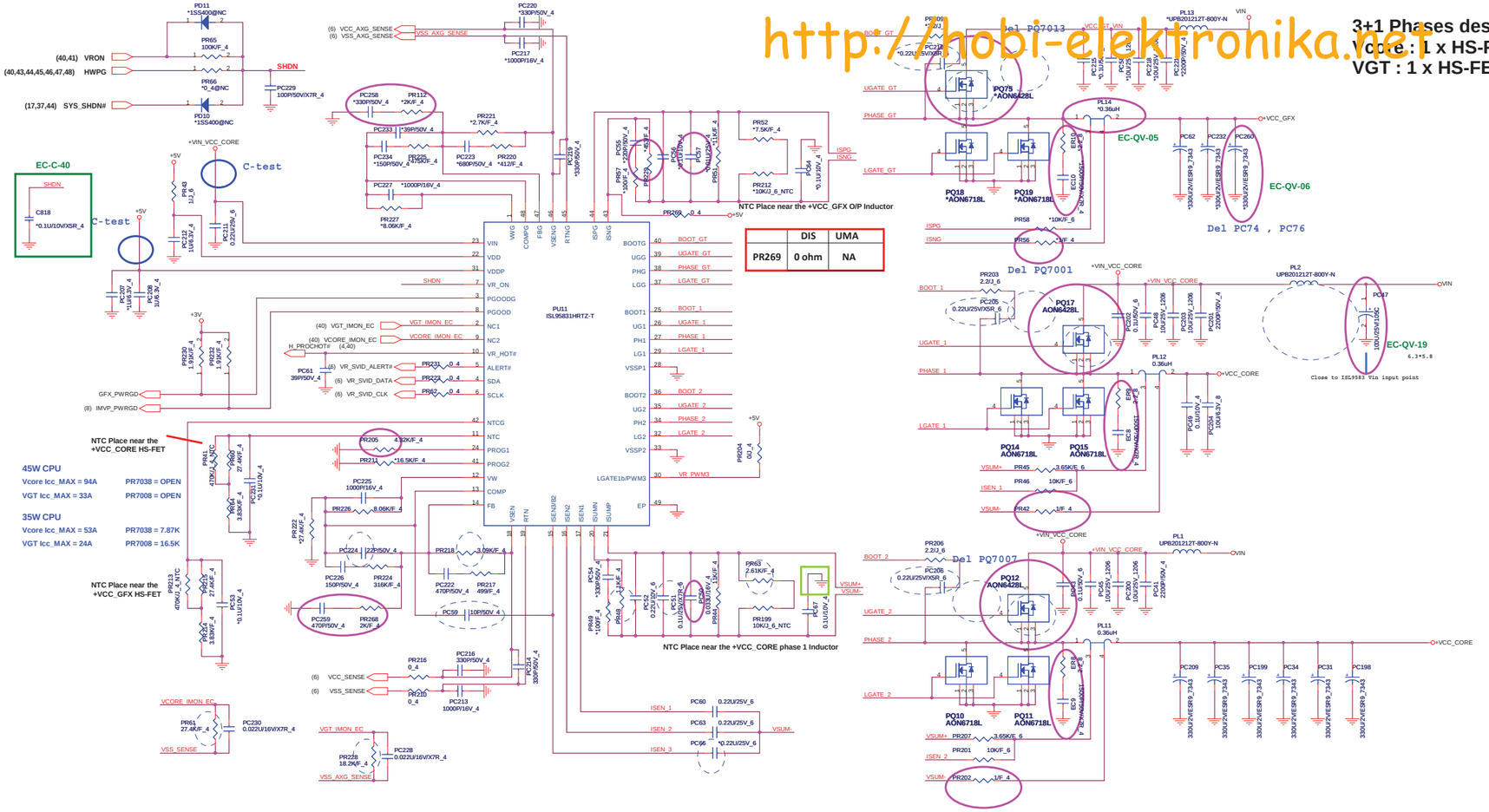
3+1 Phases design (45W CPU)
Vcore : 1 x HS-FET, 2 x LS-FET
VGT : 1 x HS-FET, 2 x LS-FET



	DIS	UMA
PR269	0 ohm	NA

PROJECT : KL6A

Quanta Computer Inc.

PD3

Size	Document Number	Rev
	IMVP7 2+1 (ISL95831HRTZ-T)	1A

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EC #	Page	Description	Part Affected
EC-B-00	**4**	Change U18 output type from coms to open-drain.	**U18**
EC-B-01	**10**	Remove TPM funtion. (LPC interface)	**U14**
EC-B-02	**10,38**	Remove keyboard light funtion.	**U14,CN3**
EC-B-03	**11**	Switch pins between BOARD_ID0 and BOARD_ID1.	**U14**
EC-B-04	**11,31**	Change net name from WIMAX_OFF# TO WLAN_OFF#, also add pull high 10K with GPIO16	**U14,R530**
EC-B-05	**11**	Add board id table.	
EC-B-06	**25**	Change ESD protection components.	**U47,U48**
EC-B-07	**26**	Modify the DIS backlight pin connecting to LVDS connector.	**CN1**
EC-B-08	**28**	Add R37 and R47 for normal-open audio jack.	**R37,R47**
EC-B-09	**29**	Add SD_4~SD_7 to support SD 3.0	**CN12**
EC-B-10	**30**	Remove 2nd battery switch.It is only for KL8/8A.	
EC-B-11	**31**	Correct the LPC connection for debug card.	**CN26**
EC-C-12	**32**	change capacitors connection from +3V to +3.3V_SSD,+1.5V to +1.5V_WIMAX	
EC-B-13	**32**	Remove unused nets in SSD connector.	**CN24**
EC-B-14	**33**	Switch the PCIE_TXN5 , PCIE_TXP5 for the right connection.	**U21**
EC-B-15	**35**	Change control signal of U25 enable pin from USB_ON to USB_CHARGE_ON for usb charge function.	**U25**
EC-B-16	**28**	Modify left & right sound reverse issue	
EC-B-17	**35**	Correct USB charge IC footprint.	**U27**
EC-B-18	**36,42**	Remove G-sensor circuits.	**U17**
EC-B-19	**37**	Correct the pin connection of CN8.	**CN8**
EC-B-20	**38**	Correct LED footprint.	**LED1,LED2**
EC-B-21	**38**	Add R51,R82 for user button defined as a power button function.	**R51,R82,R378**
EC-B-22	**40**	Add R692,R693 and disable EMI solution "CML3".	**R692,R693,CML3**
EC-B-23	**40**	Remove TPM circuits.	
EC-B-24	**42**	Correct connection and net name of NOVO_BTN#	
EC-B-25	**42**	Add KB_MATRIX signal for different keyboard matrix selection between KL7 and KL9.	**R376,R377**
EC-B-26	**46,48**	Add a +1.5V_GPU and +1.8V_GPU circuits for GPU power sequence tuning.	**PQ9064,PC9202,PC9203,P9204,PC9205,PC9206,PR9246**
EC-B-27	**10,24,27 33,34,14 37,38**	Add EMI solution	**EC11,EC12,R658,R659,R660,R661,EC13,C711,CML1,R11,R12,CML2,R35,R36,CML4,R649,R651,C677,C678 CA1,CA2,CA3,CA4,CA5,CA6,EC14~EC26,C466**
EC-B-28	**40**	Add ESD solution	**SC1~SC30**
EC-B-29	**39**	Follow PDC standard parts pin definition	**CN16**

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EC #	Page	Description	Part Affected
EC-B-30	**4,8**	Add net PCIECLKRQ5~9#	**U14**
EC-B-31	**4,8,9 10,26 42**	Add RF solutions	**R632,R633,C704,C705,C706,C713,R662,R664,R678,R699,R700,R701,R702,R703,C714,C715 C717,C718,C720,C727,C809,C810,C811,C812,C813,C814**
EC-B-32	**42**	Change EC GPIO	**U17**
EC-B-33	**10,33**	Change PCH GPIO66 net name to PCH_CLK_25M and connect to USB3.0 XTAL	**R636,R637**
EC-B-34	**4**	Delete XDP_DBRST# pull high RES	**U32,R598**
EC-B-35	**4**	Add VCCSA_SEL pulll down RES	**R598**
EC-B-36	**4**	Disconnect SLP_A# from PCH to EC	
EC-B-37	**41**	Modify hole footprint	**Hole21,Hole3**
EC-B-38	**35**	Un-stuff USB charger schematic	**R461,R465,C530,U27,R689,R690**
EC-B-39	**46**	Modify power sequence to fix S3 issue	**PR266**
EC-B-40	**8,27 28,53 40,38**	Reserve ESD solution	**RV16,C815,C816,C817,C818,C819,C820,C821,C822,C823,C824**
EC-B-41	**45**	Power add discharge current solution	**PD22**
EC-B-42	**9**	Follow vendor XTAL CAP suggestion	**C118,C119**
EC-B-43	**42**	Change EC PN & un-stuff XTAL	**Y4,C369,C375,R336,U17**
EC-B-44	**6 53**	Del +VCC_GFX power	**C684,C685,C690,C682,C302,C310,C313,C319,C314,C693,C323,C315,R597,R591 PL13,PC221,PC218,PC58,PC215,PQ75,PC232,PC62,PL14,PR56,PR58,ER10,EC10,PQ1,PQ19,PR209,PC210 PC64,PR52,PR212,PR51,PC57,PC56,PR229,PC220,PC217,PC219,PR221,PR220,PC223,PR112, PC258,PC233,PR225,PC234,PC227,PR227**

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EC #	Page	Description	Part Affected
EC-C-00	**36**	Change power LED pull high power plane to +3VPCU to fix system enter S3 can't flicker issue	**LED1**
EC-C-01	**38**	Add EMI solution	**SC31,SC32,SC33,SC34,SC35,SC36,SC37,SC38**
EC-C-02	**39**	Modify Hole footprint	**Hole1,Hole2,Hole6,Hole14,Hole16,Hole17,Hole20,Hole19,Hole9,Hole8**
EC-C-03	**12**	Reserve CAP for +VCCAFDI_VRM	**C825**
EC-C-04	**38**	Delete ESD solution SC9 due to +1.5V power plane was deleted & change SC17 power plane bridge, add some component	**SC9,SC17,SC25,SC39,SC40,SC41,SC42,SC43,SC44,SC45,SC14,SC18,SC19,SC28,SC29,SC30,SC10,SC11 SC12,SC13,SC15,SC22,SC46**
EC-C-05	**36**	Modify LED footprint to fix SMT issue	**LED3**
EC-C-06	**25**	Modify bead footprint to fix SMT issue	**L37**
EC-C-07	**21**	Modify VRAM footprint to fix SMT issue	**U4,U5,U28,U29**
EC-C-08	**4**	Un-stuff AND gate component	**U18,C366,R314,R313**
EC-C-09	**27**	Change SD_CLK CAP from 33p to 10p	**C425**
EC-C-10	**22**	Change RES value to fix HDMI test fail item	**R399,R400,R401,R402,R403,R404,R405,R406**
EC-C-11	**26**	Reserve diode for EAPD pin	**D23**
EC-C-12	**9**	Un-stuff JTAG RES	**R181,R182,R528,R534,R533,R538,R168**
EC-C-13	**31**	Add USB3.0 schematic	**CN23,R369,R371,CML4,R637,R657,R704,R705,Q53,Q54,C706,C826,C827,C828,R636,R155,R707,C829,Q58,C830**
EC-C-14	**31**	Modify TP footprint to 3050	**TP20,TP21,TP22,TP23**
EC-C-15		Modify 0 ohm RES to short pad	**R592,R608,R326,R274,R287,R292,R502,R504,R505,R512,R513,R521,R527,R91,R245,R258,R587,R301 R648,R451,R380,R442,R366,R425,R623,R673,R686,R77,R430,R432,R101,R212,R221,R232,R235,R239 R563,R586,R588,R600,R66,R71,R94,R391,R392,R393,R394,R252,R242,R248,R250,R603,R65,R233 R4,R50,R652,L49,L53,R431,R364,R370,R397,R448,R384,R446,L23,R40,R60,R349**
EC-C-16	**12**	Change 0.002 ohm RES to 0 ohm	**R247,R261,R254**
EC-C-17	**26**	Stuff ESD solution	**C480,C481,C482,C483**
EC-C-18	**10**	Remove RF_ON pull down RES	**R522**
EC-C-19	**29**	Add net WWAN_OFF# to disable WWAN function	
EC-C-20	**12**	Change 0 ohm RES to bead	**R222**
EC-C-21	**4**	For INTEL design guide definition and material shortage, will change to 25.5ohm	**R315**
EC-C-22	**6**	Stuff SVID DATA pull high RES	**R286**

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EC #	Page	Description	Part Affected
EC-QV-00	42	Add power circuit for charge issue.	PR9252,PR9253,PR9254,PR9255,PR9256,PC9212,PC9213,PD23,PU13,PQ9070
EC-QV-01	37	Add 0 Ohm for thermal sensor of DDR & WWAN	R133,R155
EC-QV-02	33	Modify the USB charge circuit(Add option and reverse circuit, change the USB switch EN to USB_ON_R)	R522,R636,R708,R709,R710,Q60
EC-QV-03	11	Change the SV_DET pull high to +3V_S5 from +3V	
EC-QV-04	25	Change footprint of L37 for SMT request	L37
EC-QV-05	43	Change footprint of PL4, PL6, PL7, PL15, PL16	PL4, PL6, PL7, PL15, PL16
EC-QV-06	49	Add capacitor in +VCC_GFX	PC260
EC-QV-07	4	Add un-stuff capacitor on H_PWRGOOD_R	C900
EC-QV-08	4	Change to component stuff	R325,Q29
EC-QV-09	8	Add un-stuff capacitor on SYS_PWROK	C901
EC-QV-10	8	Change R493 to un-stuff	R493
EC-QV-11	9	Change footprint to shortpad	R409,R153
EC-QV-12	9	Add 1M ohm on ACZ_SYNC_CODEC	R711
EC-QV-13	9	Change C119,C118 to 18p from 6p for RTC issue	C118,C119
EC-QV-14	30	Change component to un-stuff.	C783,C784,C736
EC-QV-15	26	Change the footprint for EMI solution stuff BEAD	R391,R392,R393,R394
EC-QV-16	39	Change HOLE8 to NTPH	
EC-QV-17	31	Modify USB3.0 circuit for power saving.	Q35,R414,R415, D28,R712,Q62,R716,C950,Q63,R717,C951,C952,R713,R714,Q61,C953,R715,R421
EC-QV-18	22	Change the footprint to 4 GND PIN for HDMI	CN22
EC-QV-19	49	Change PC47 to stuff	PC47
EC-QV-20	38	Change the P/N for cost saving	SC2,SC11,SC12,SC13,SC14,SC15,SC16,SC20,SC21,SC22,SC27,SC28,SC29,SC30,SC39,SC40,SC41,SC42 ,SC43,SC44,SC45,SC46,SC31,SC32,SC33,SC34,SC35,SC36,SC37,SC38
EC-QV-21	29	Change C497 to stuff	C497

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC RECORD QV	1A

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