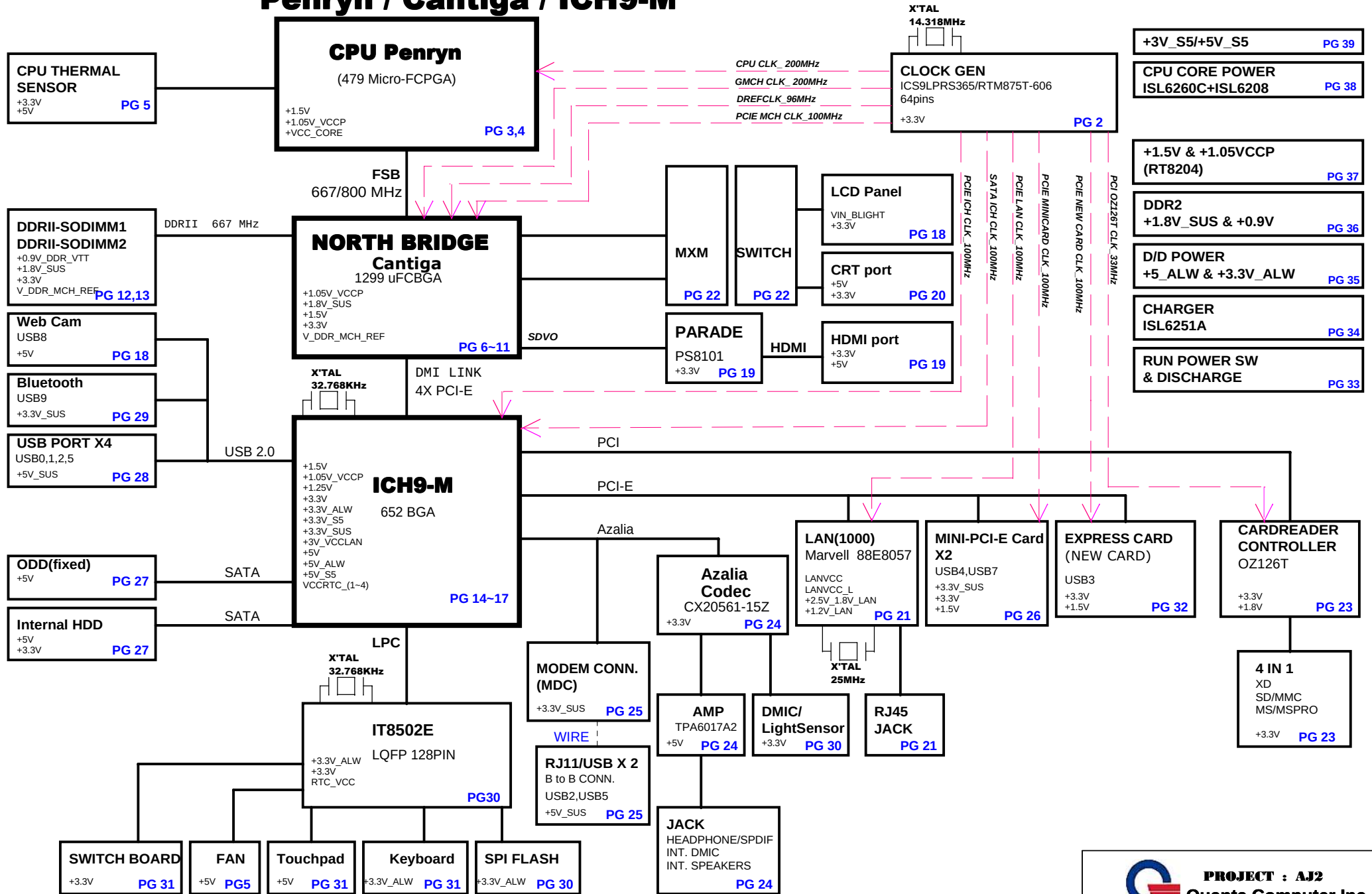


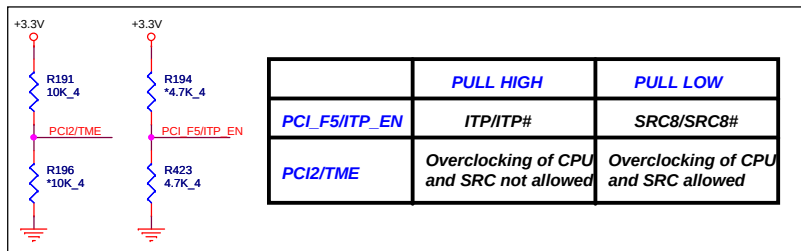
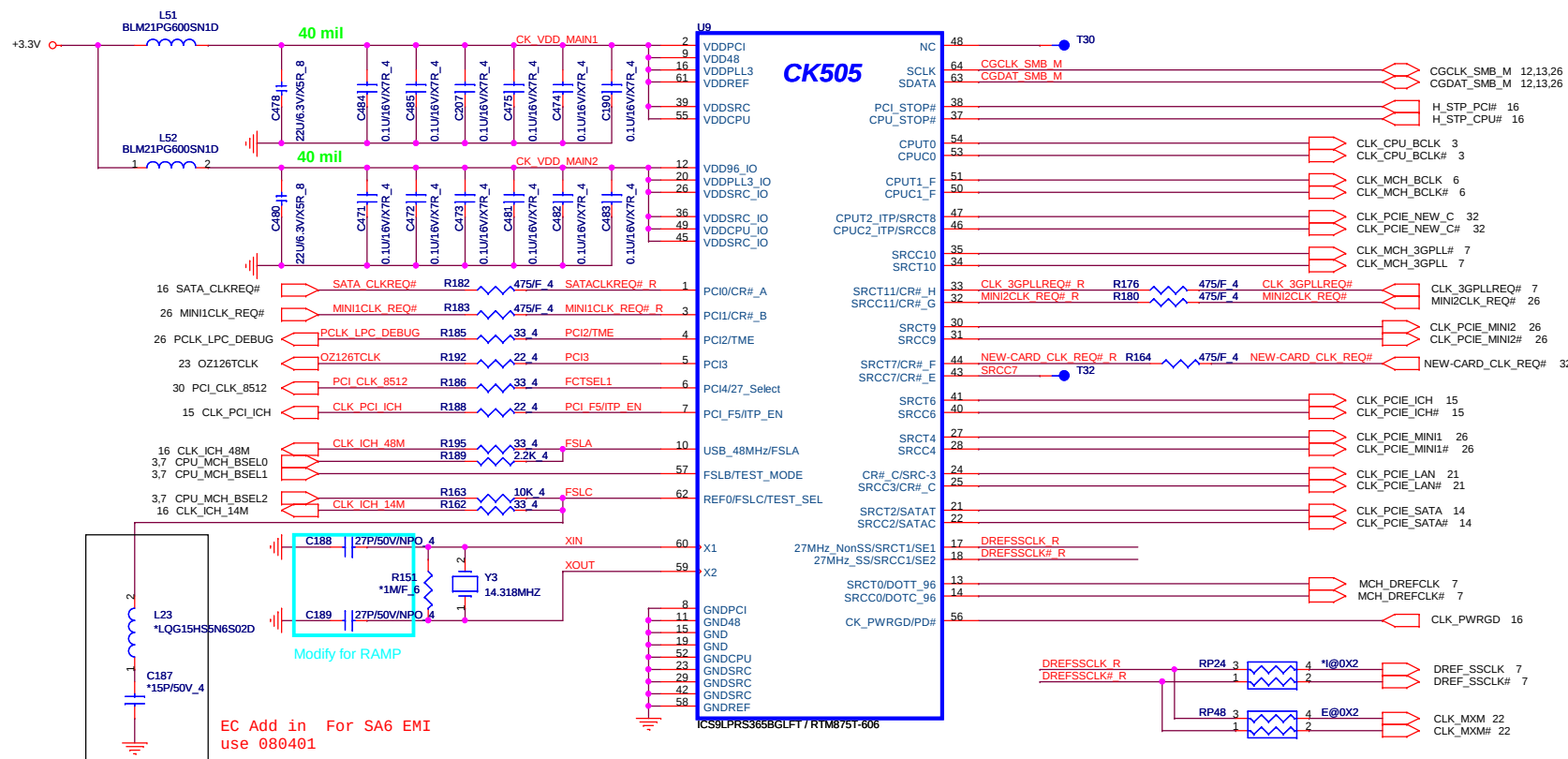
AJ2 BLOCK DIAGRAM

(Montevina Platform)

Penryn / Cantiga / ICH9-M



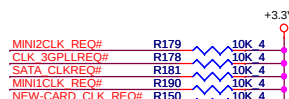
PROJECT : AJ2
Quanta Computer Inc.



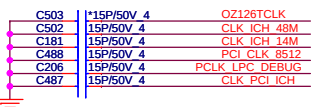
	<i>PULL HIGH</i>	<i>PULL LOW</i>
<i>PCI_F5/ITP_EN</i>	<i>ITP/ITP#</i>	<i>SRC8/SRC8#</i>
<i>PCI2/TME</i>	<i>Overclocking of CPU and SRC not allowed</i>	<i>Overclocking of CPU and SRC allowed</i>

CPU Clock select

GFC Clock Select						
FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100.00	100	33	
0	0	1	133.33	100	33	
0	1	1	166.66	100	33	
0	1	0	200.00	100	33	
0	0	0	266.66	100	33	
1	0	0	333.33	100	33	
1	1	0	400.00	100	33	
1	1	1	200.00	100	33	

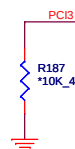
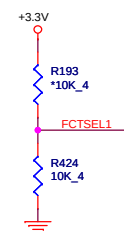


EMI CAP

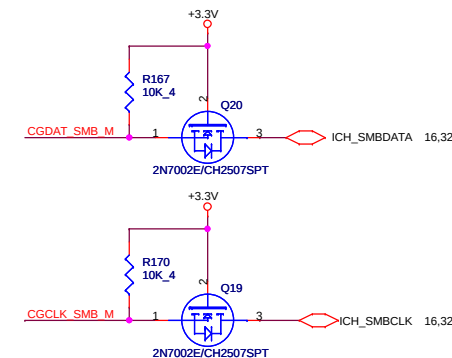


GCLK_SEL = FCTSEL1

FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96	DOT96#	SRC-1/LCDT_100	SRC-1#/LCDT_100
1 = External VGA	SRC-0	SRC-0#	27Mout-NSS	27Mout-SS

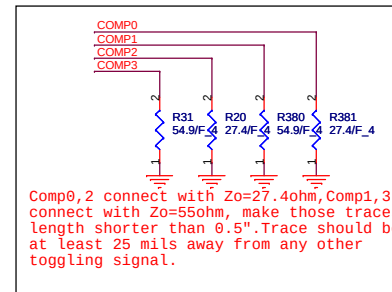


	<i>PULL HIGH</i>	<i>PULL LOW</i>
<i>PCI3</i>	<i>PIN37/38 is CPU_STOP/PCI_STOP PIN37/38 IS SRC5.</i>	<i>**SRC5_EN/PCI-3 (Internal Pull Low)</i>

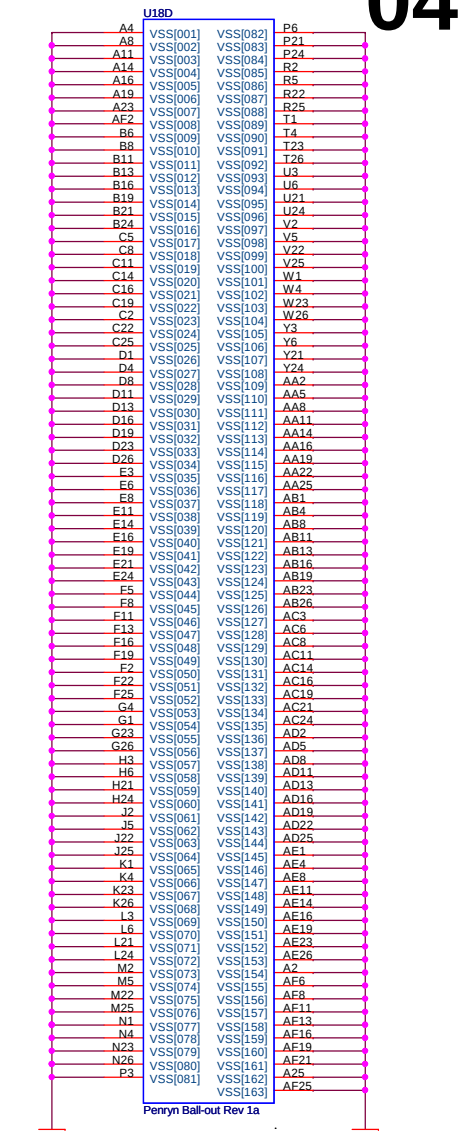
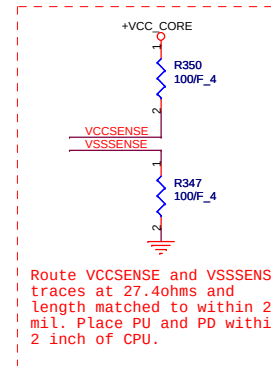
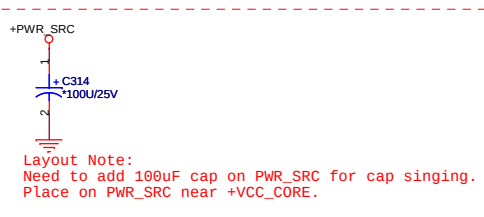
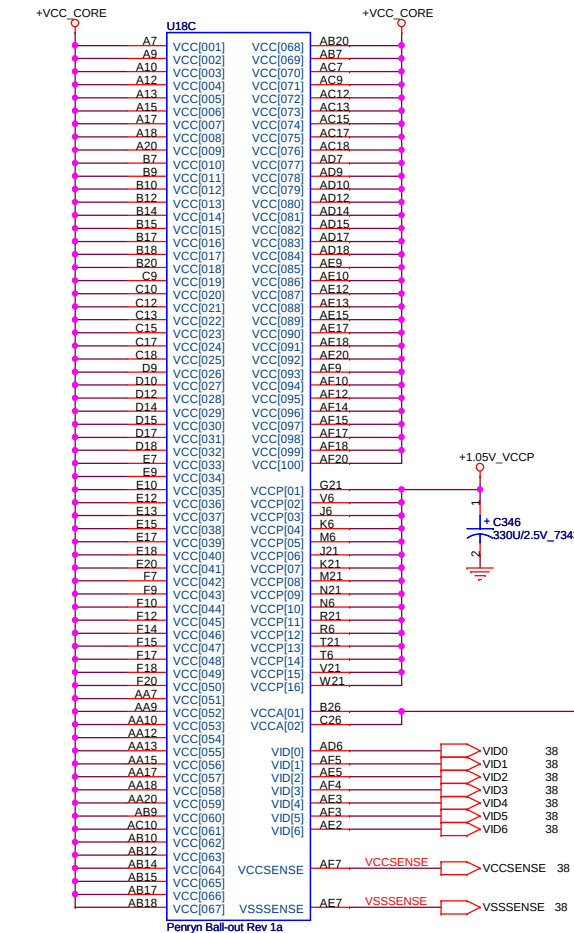
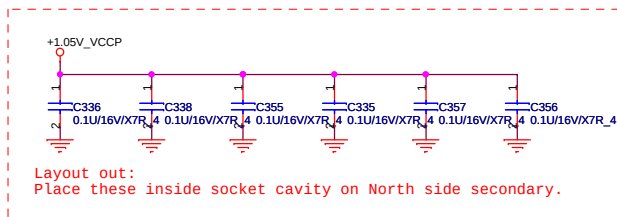
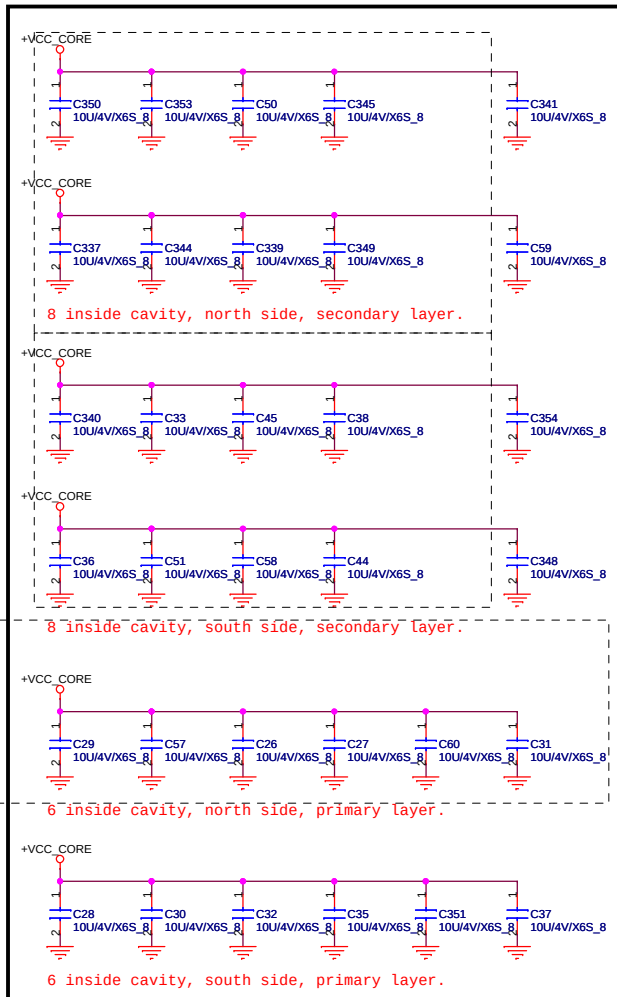


PROJECT : AJ2
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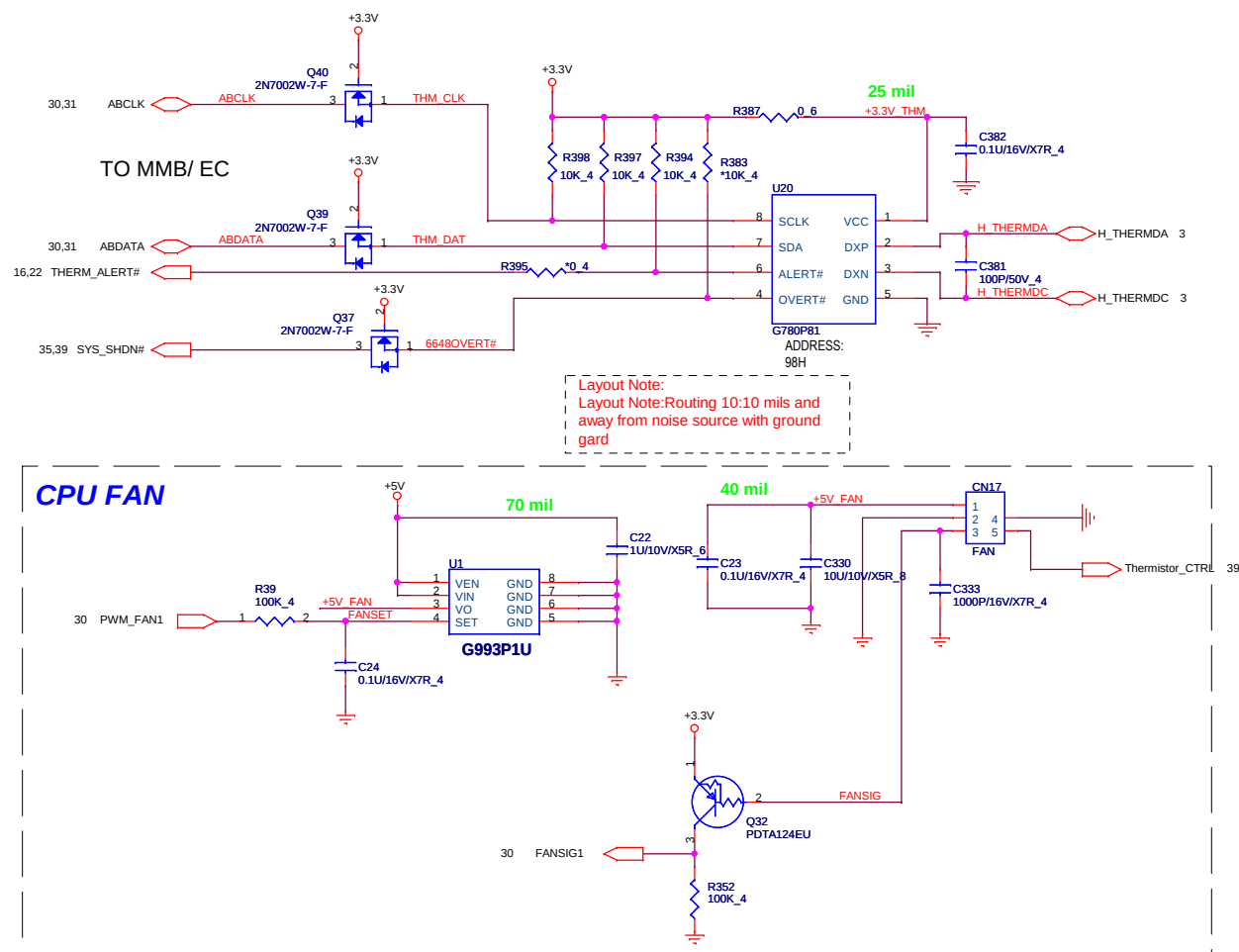
Size Custom	Document Number CLOCK GENERATOR	Rev 1A
Date: Tuesday, September 16, 2008	Sheet 2	of 43

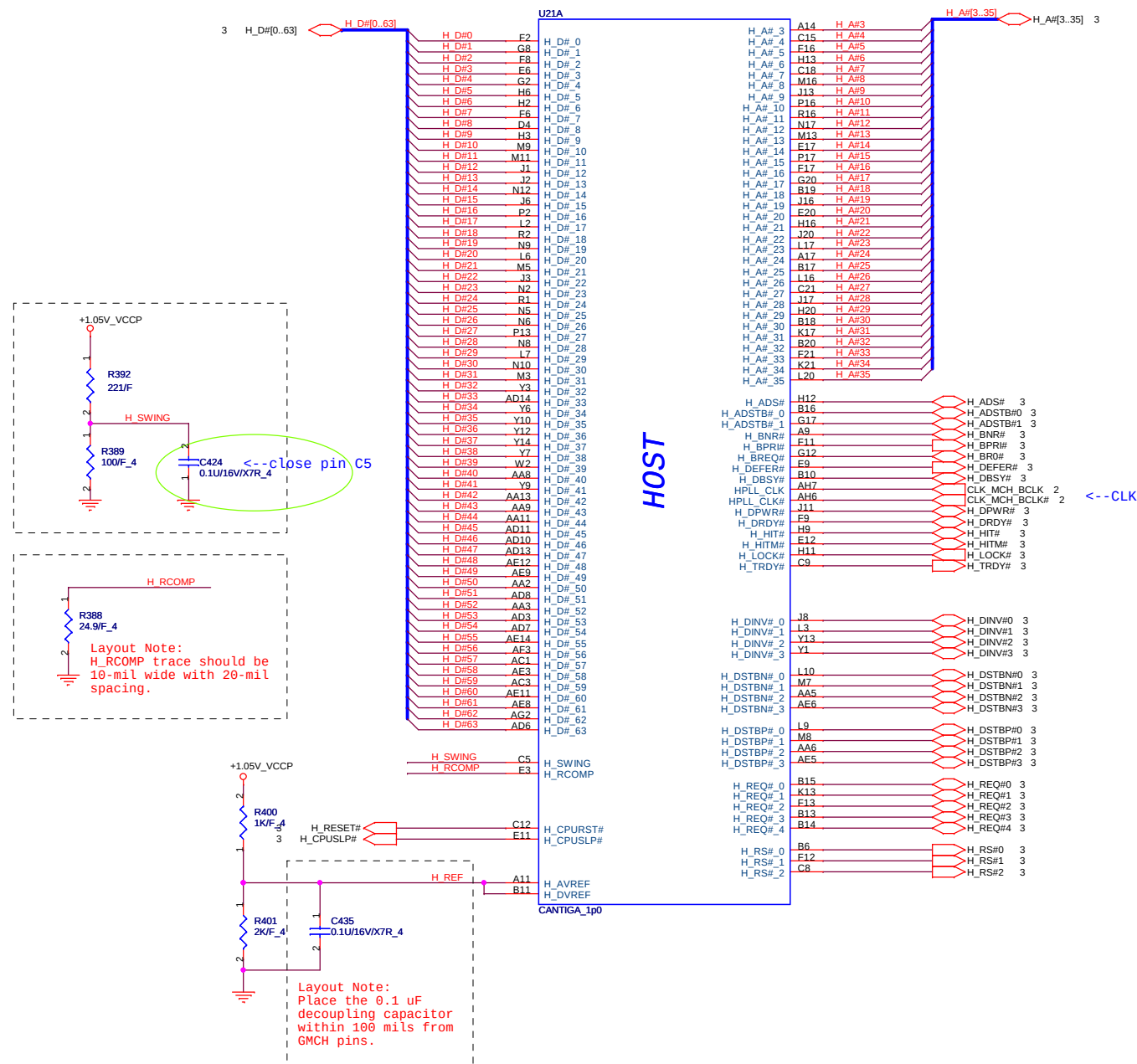


All use 22U 10V(+20%,X5R,1210)Pb-Free.

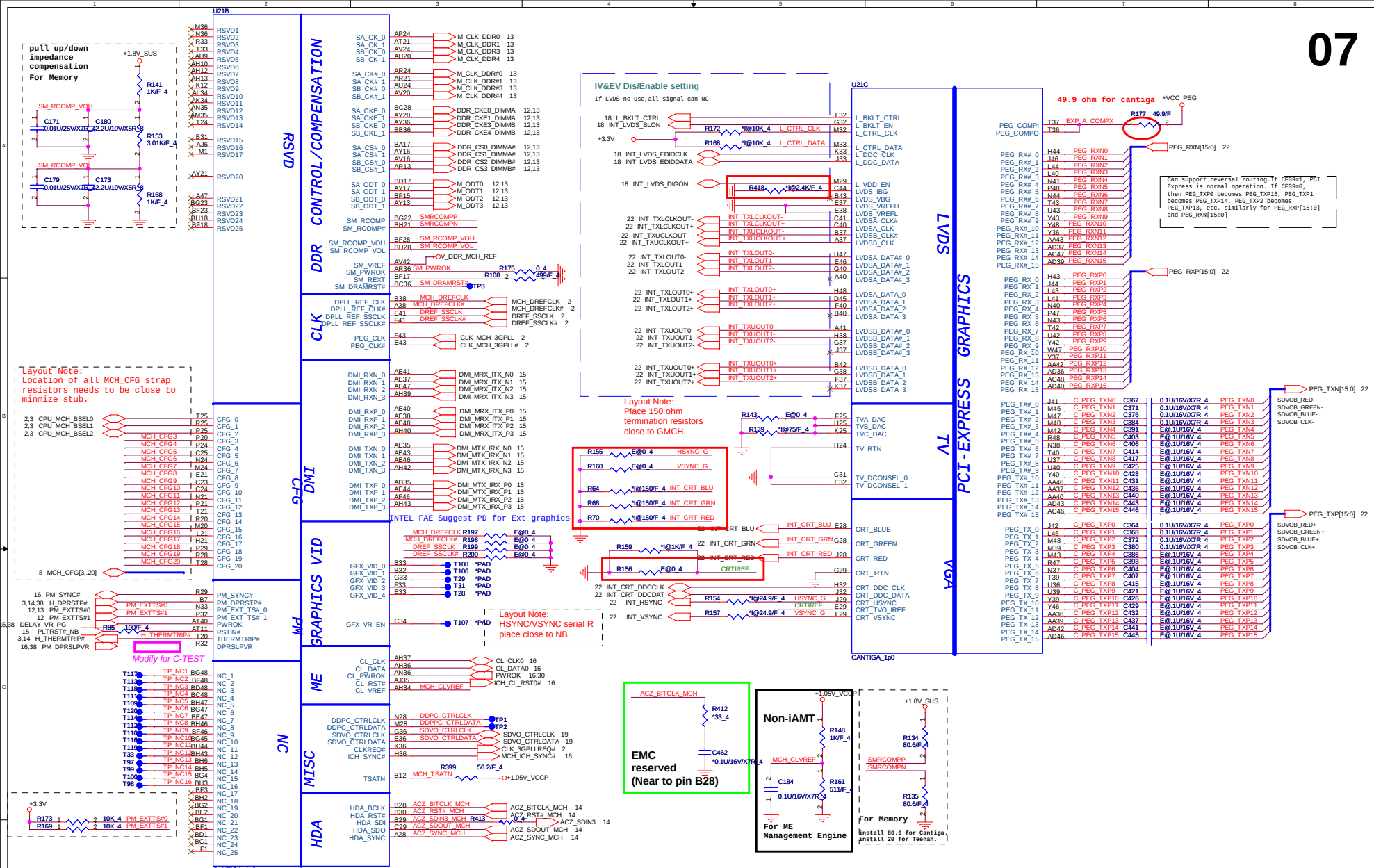


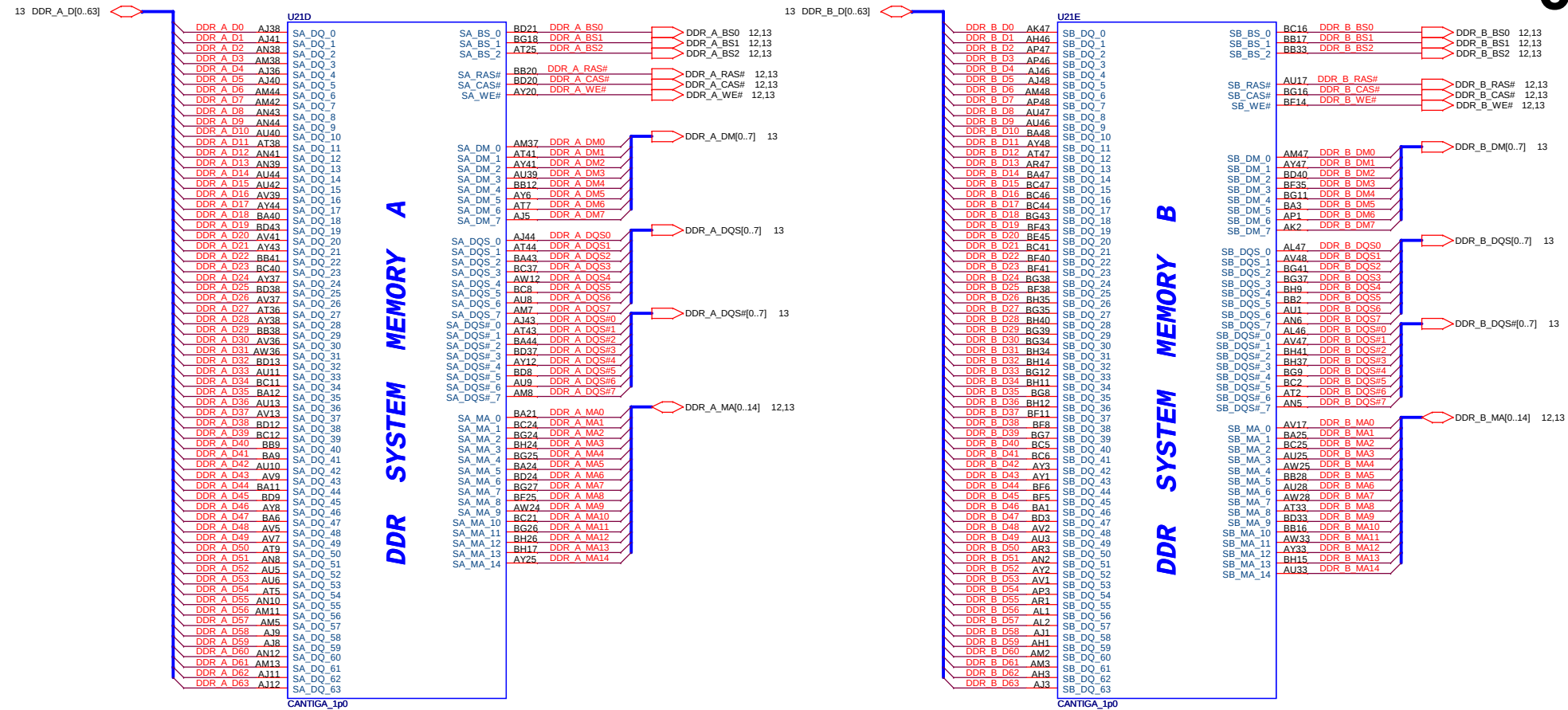
CPU Thermal monitor





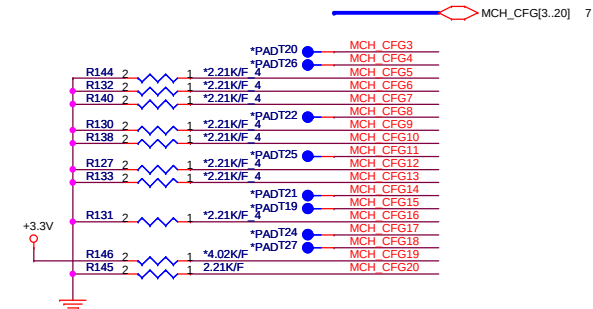
PROJECT : AJ2
Quanta Computer Inc.

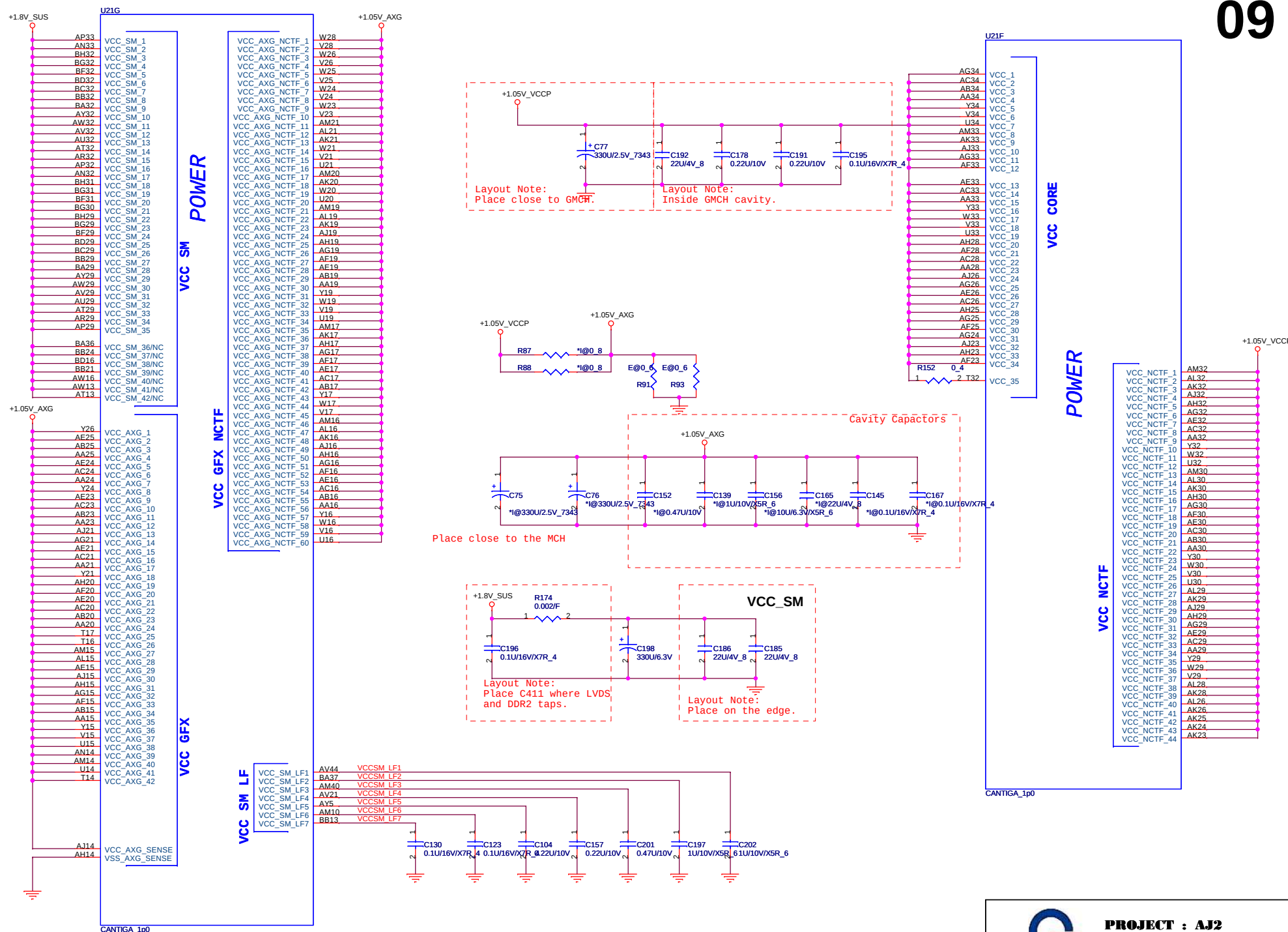


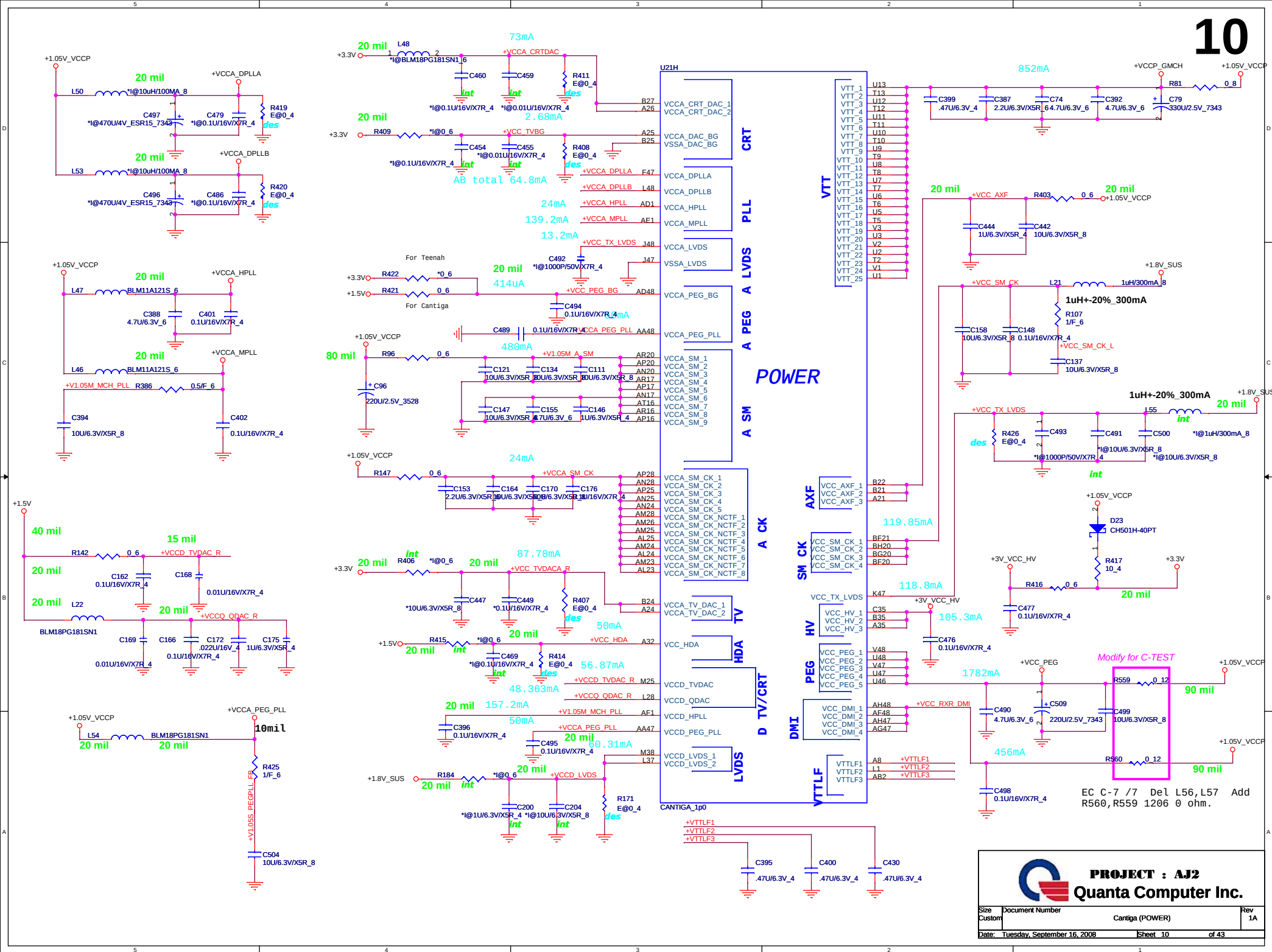


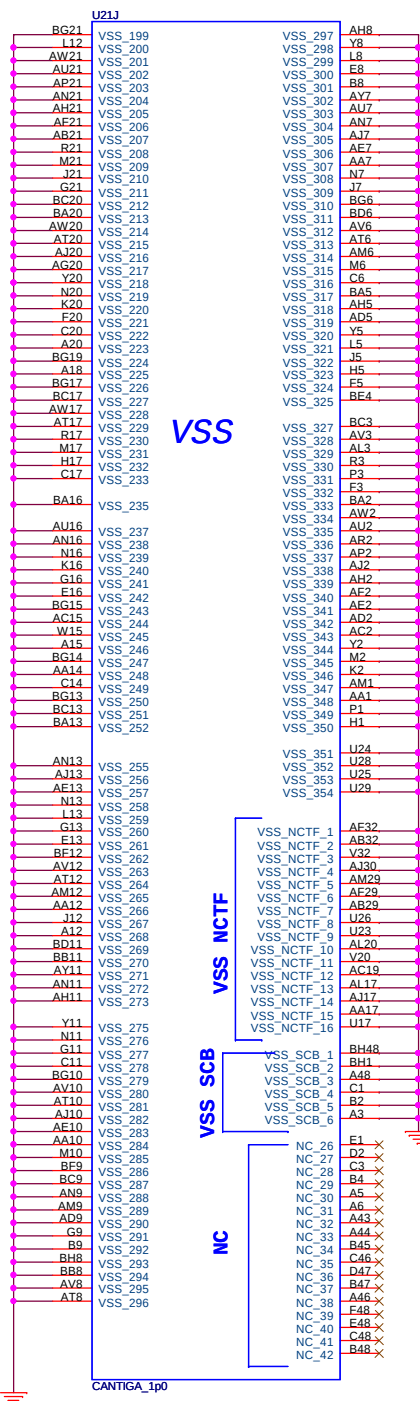
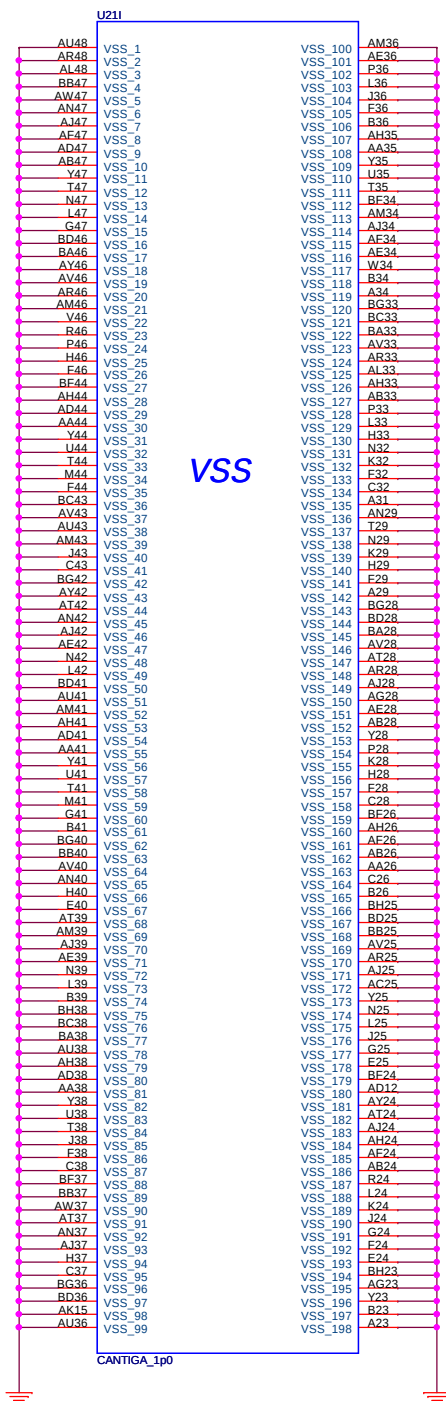
STRAPPING

CFG5	DMI X2 Select	Low=DMIX2 High=DMIX4(Default)
CFG6	iTPM Host Interface	Low= Enable High=Disable(Default)
CFG7	Intel Management Engine Crypto Strap	Low= Intel Management Engine Crypto TLS cipher suite with no Confidentiality High=Intel Management Engine Crypto TLS cipher suite with Confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG10	PCIe Loopback Enable	Low= Enable High=Disable(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	Digital Display Port(SBVO/DP/IHDMI) and PCIe Concurrent Operation.	Low=Only DP or only PCIe is operational (defaults) High=DP and PCIe x1 are operating simultaneously.
CFG13	CFG12	XOR / ALLZ / Clock Un-gating





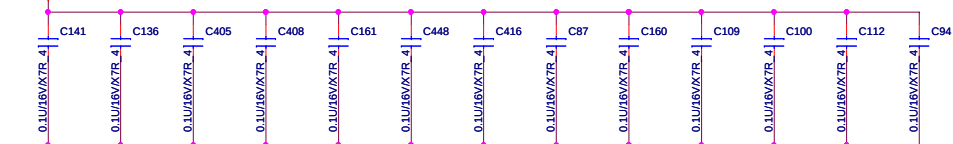




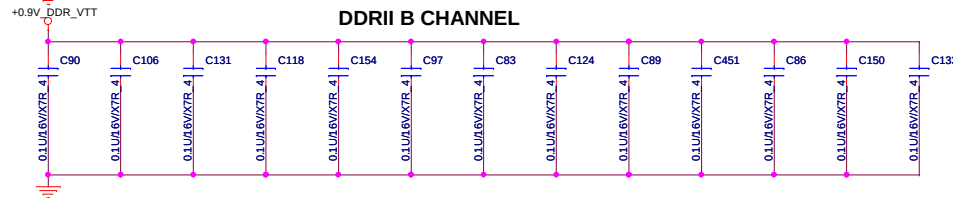
DDRII A CHANNEL

+0.9V_DDR_VTT

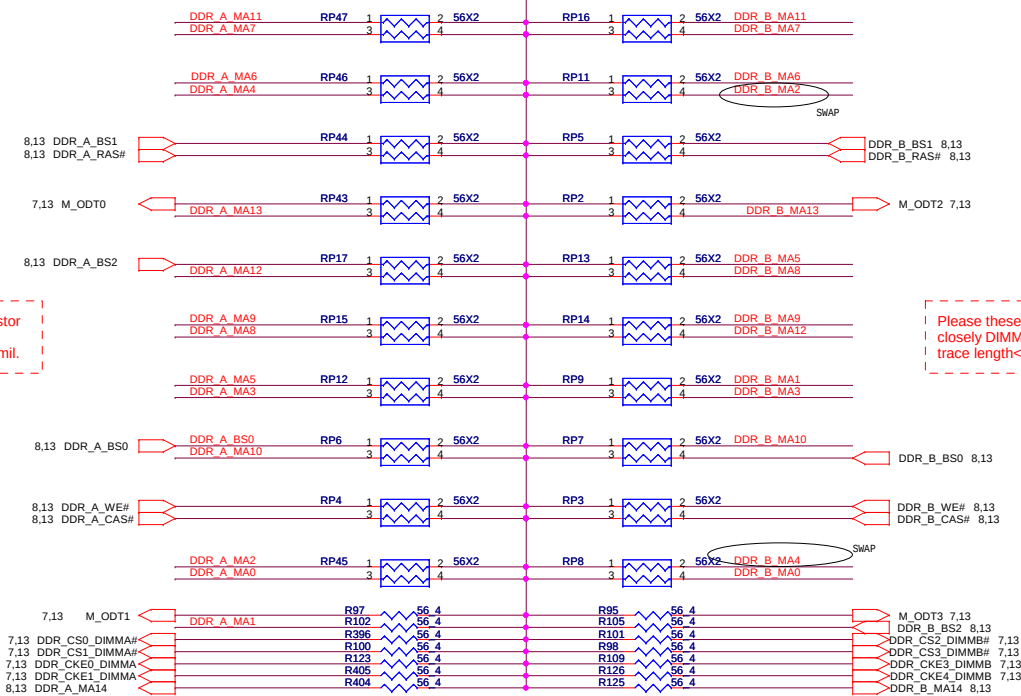
Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.



DDRII B CHANNEL



8.13 DDR_A_MA[0..13]

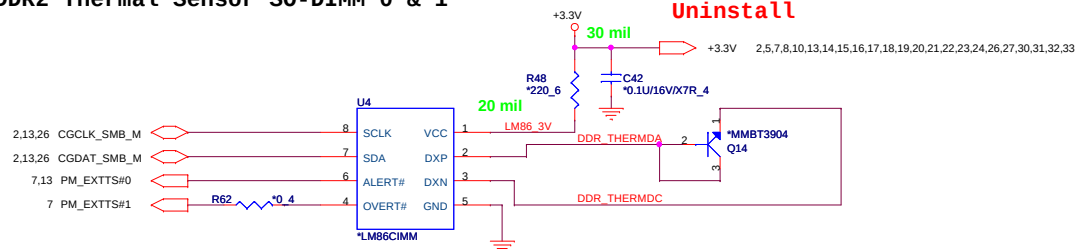


Please these resistor
closely DIMMA, all
trace length<750 mil.

Please these resistor
closely DIMMB, all
trace length<750 mil.

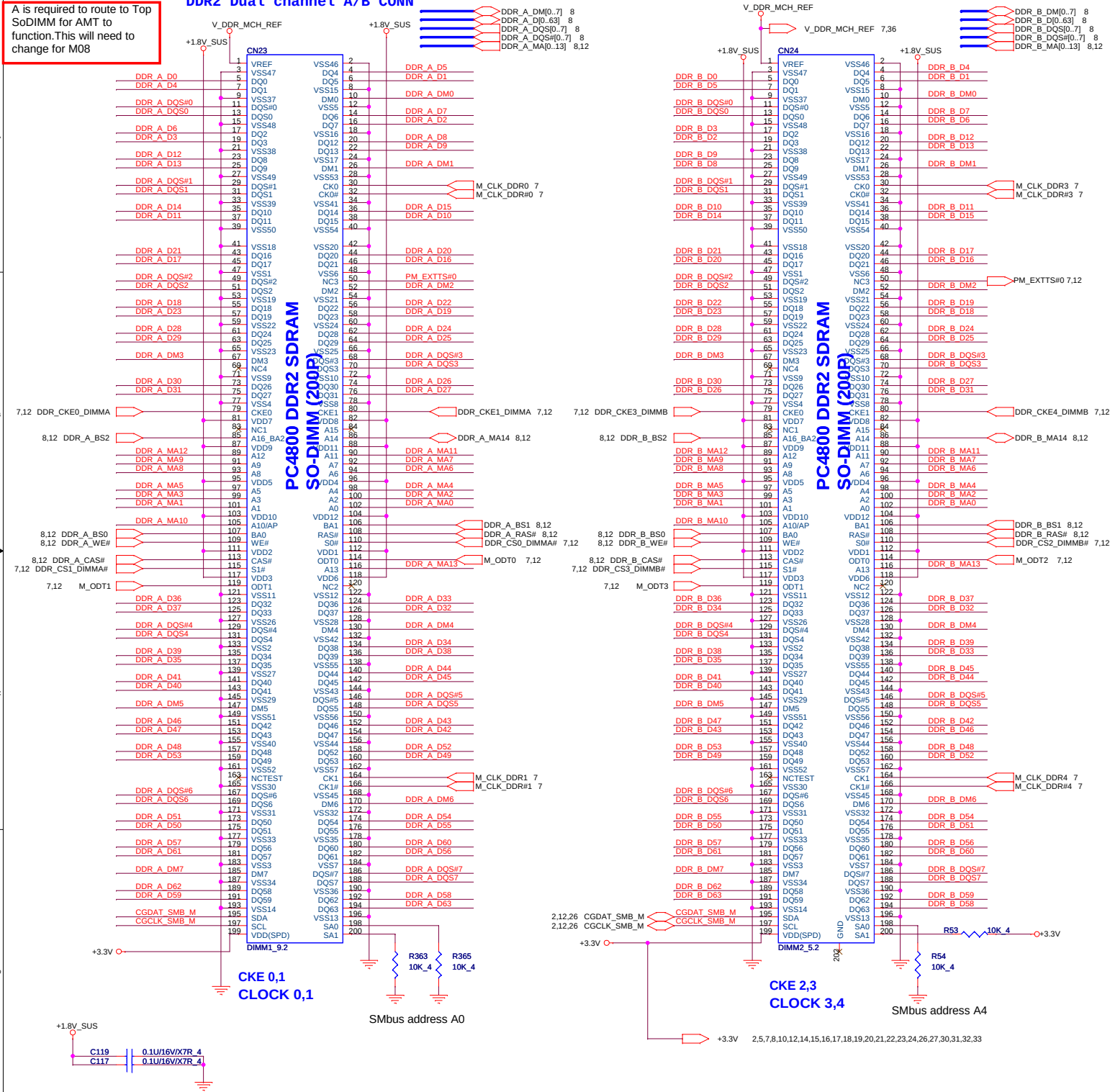
DDR2 Thermal Sensor S0-DIMM 0 & 1

Uninstall

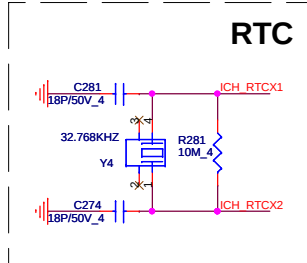
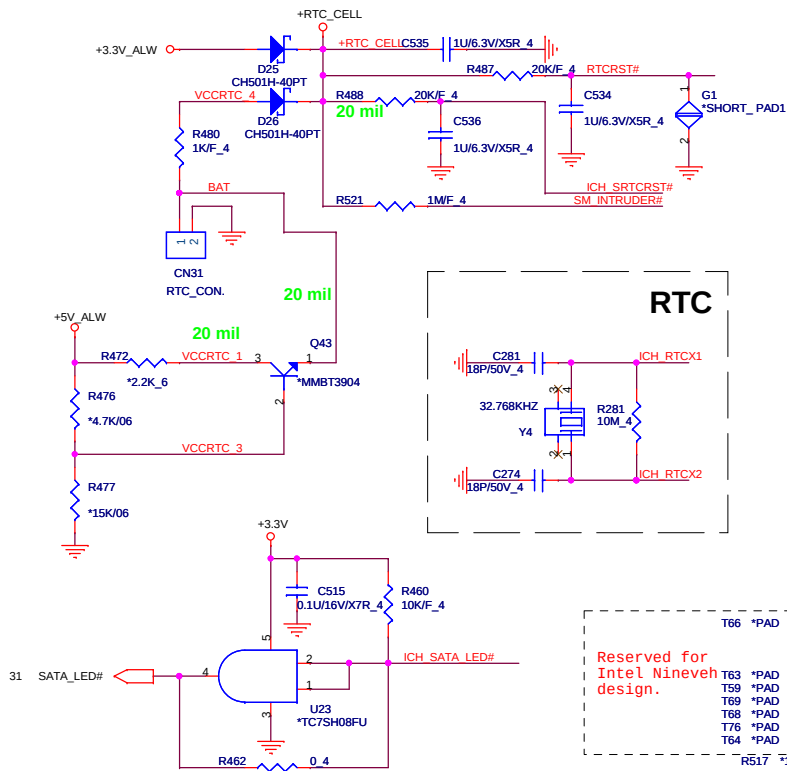


DDR2 Dual channel A/B CONN

A is required to route to Top SoDIMM for AMT to function. This will need to change for M08



PROJECT : AJ2
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ICH8-M LAN100_SLP Strap
(Internal VR for
VccLAN1_05 and
VccCL1_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

SB Strap

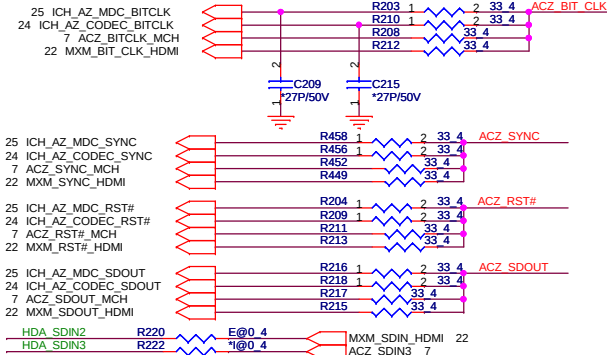
ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
--------------	---

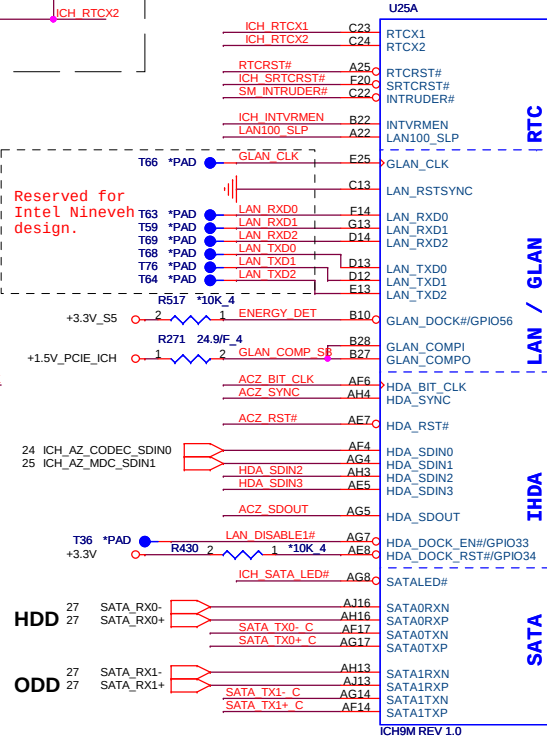
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1

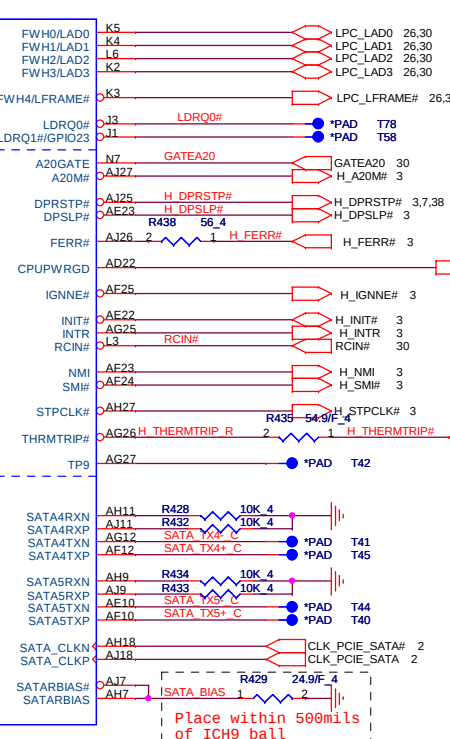
AZ Interface(MDC, CODEC, HDMI)



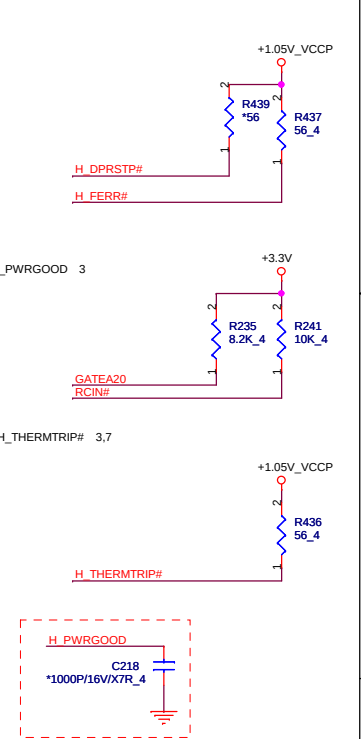
Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respectively. Basically, keep the same distance from T for all series termination resistors.



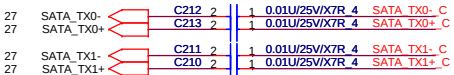
ICH9M REV 1.0



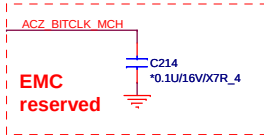
Place within 500mils of ICH9 ball



AC-TX for SATA

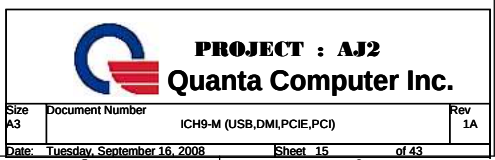
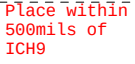
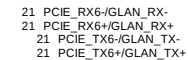
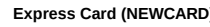
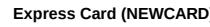
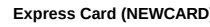


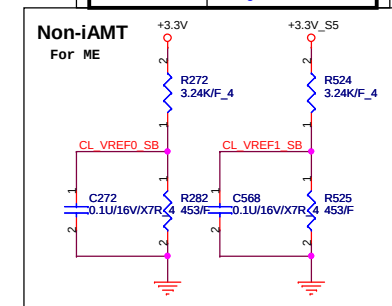
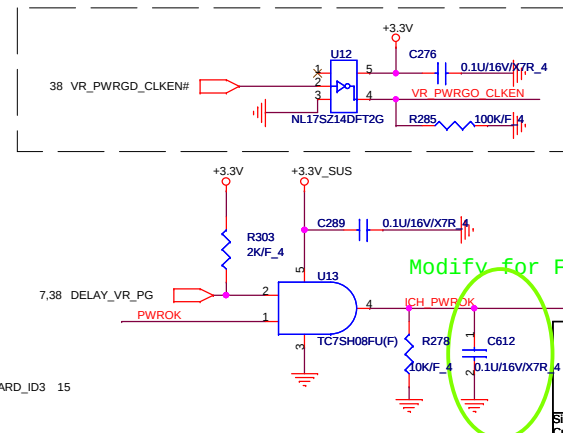
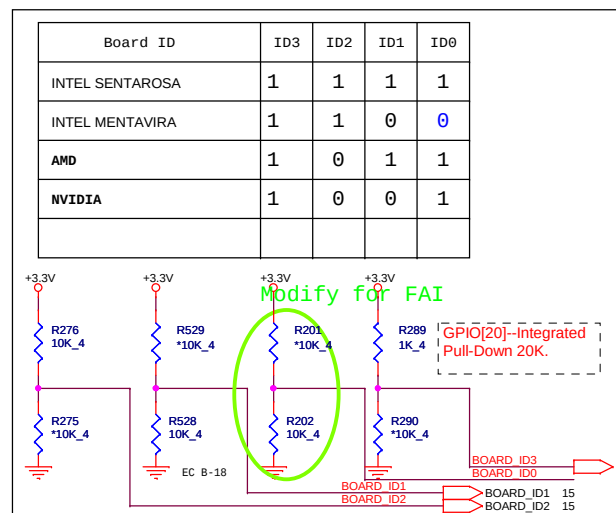
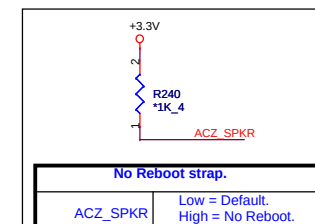
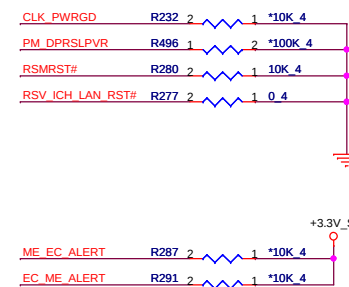
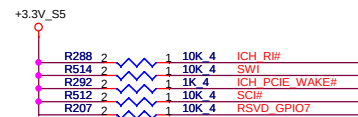
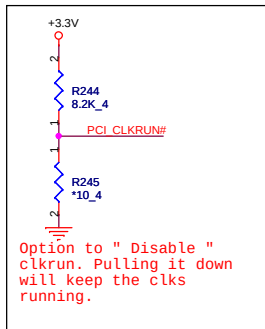
Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.

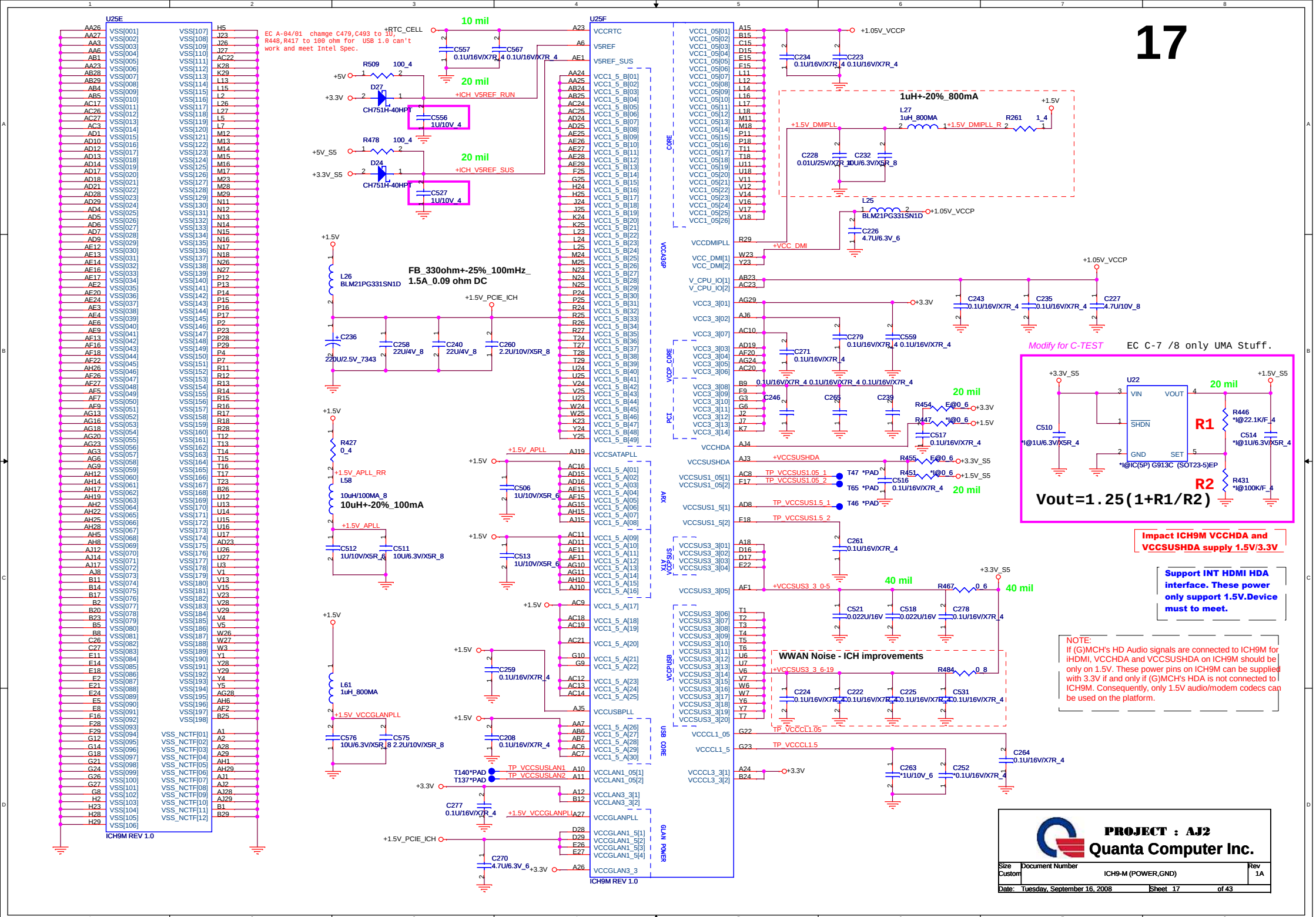


PROJECT : AJ2
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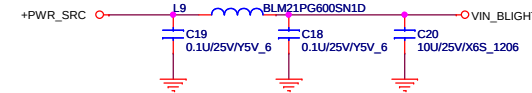
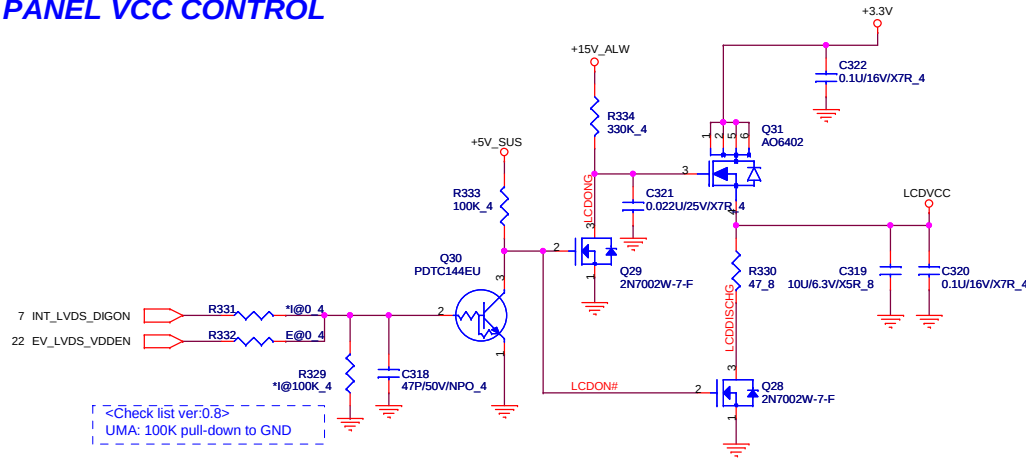
Size	Document Number	Rev
Custom	ICH9-M (CPU,IDE,SATA,LPC,AC97,LAN)	1A
Date:	Tuesday, September 16, 2008	Sheet 14 of 43





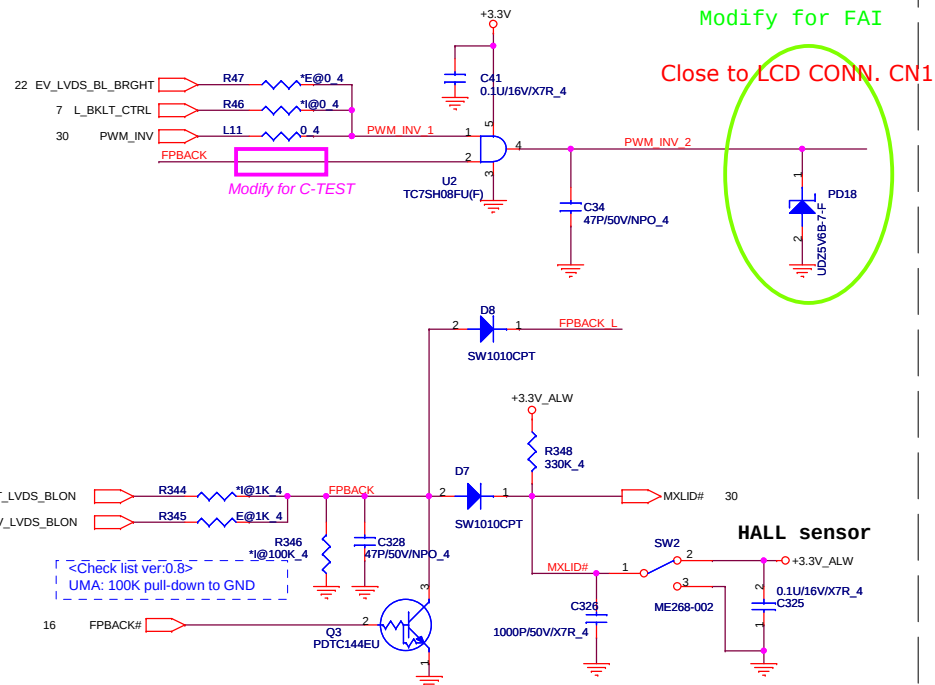


PANEL VCC CONTROL

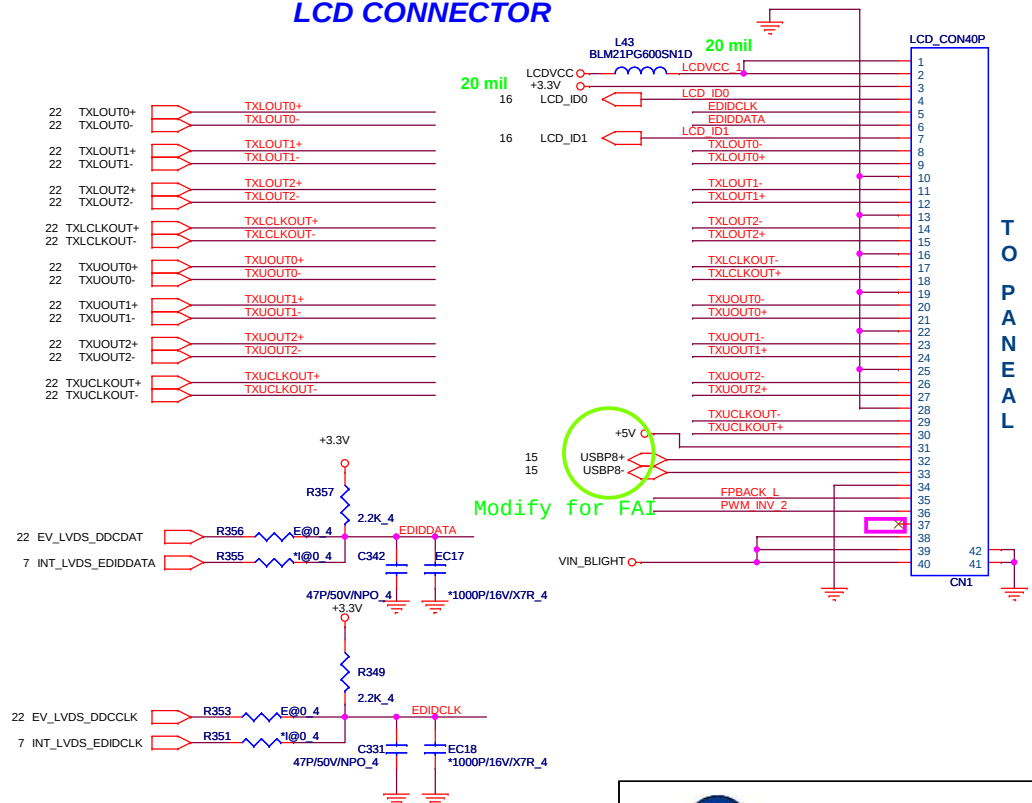


	Single LVDS 1366*768	Dial LVDS 1920*1080
LCD_ID0	TBD	TBD
LCD_ID1	HIGH	LOW

BACKLIGHT CONTROL



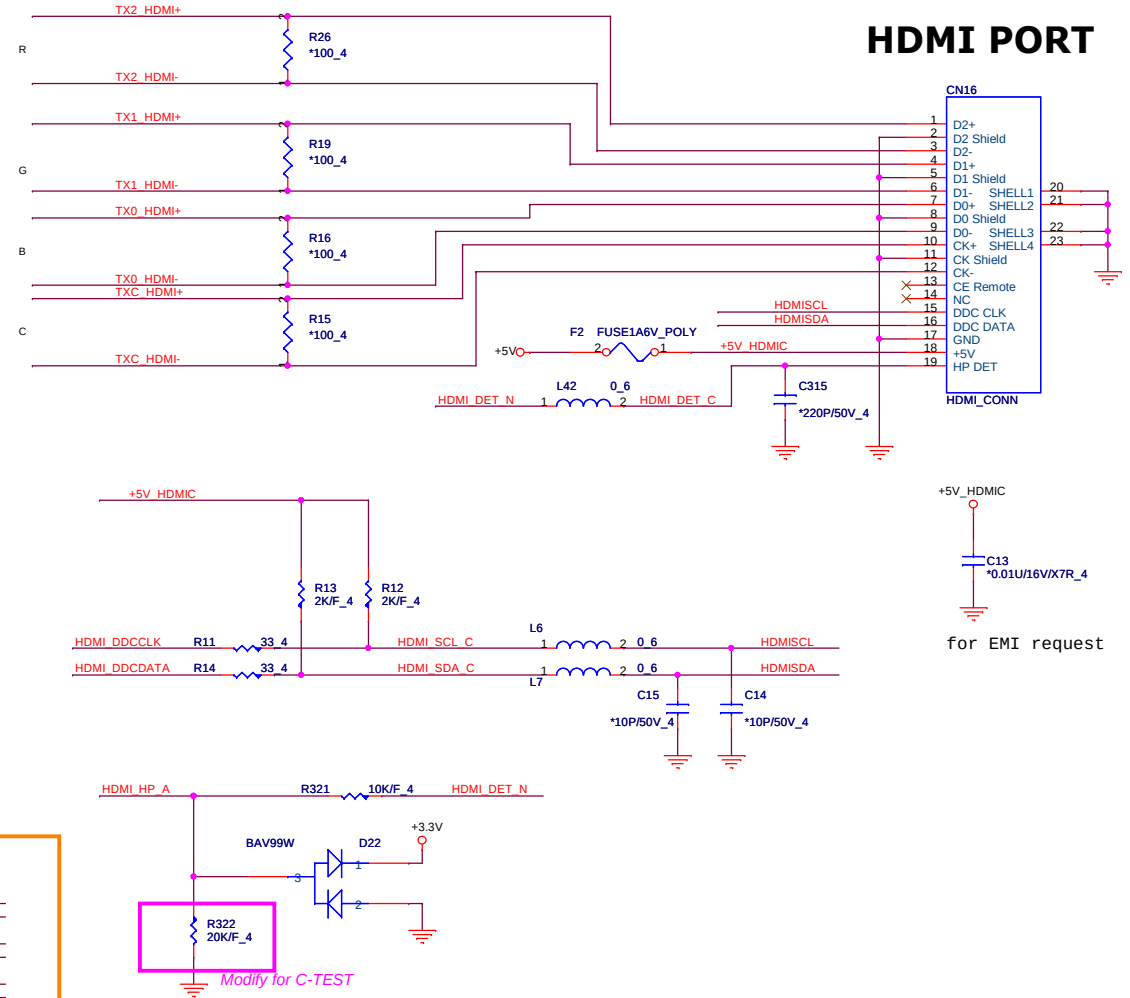
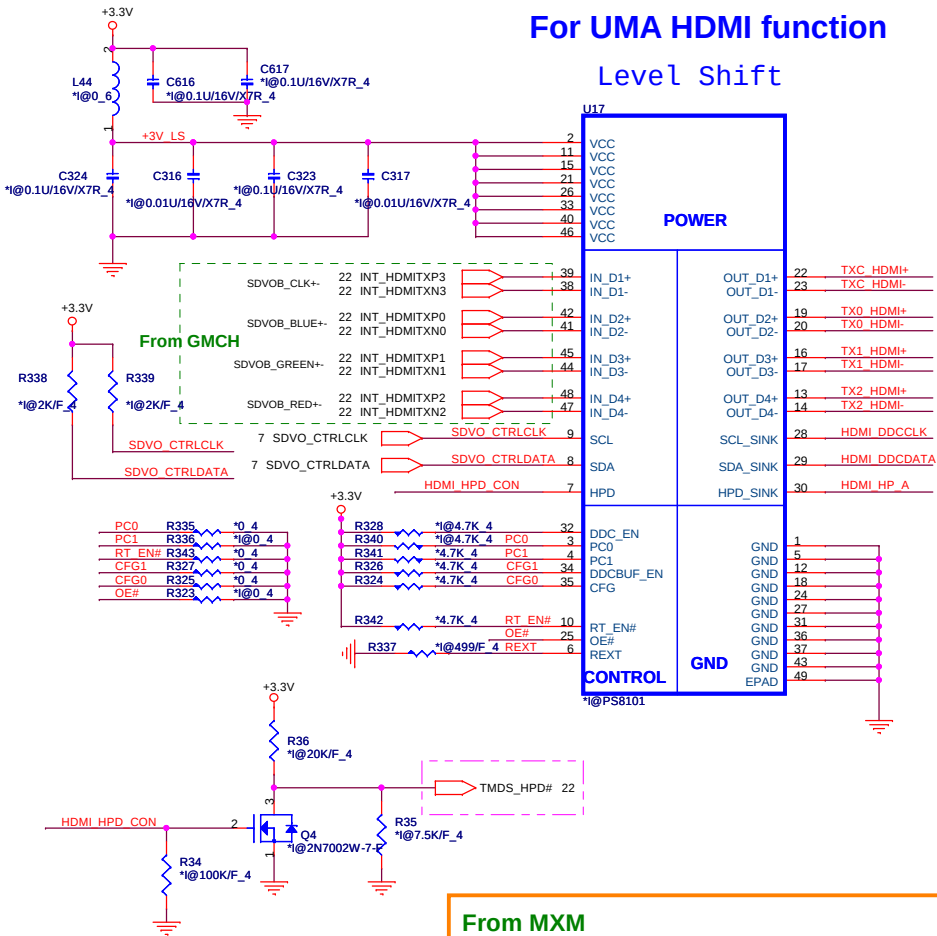
LCD CONNECTOR



PROJECT : AJ2
Quanta Computer Inc.

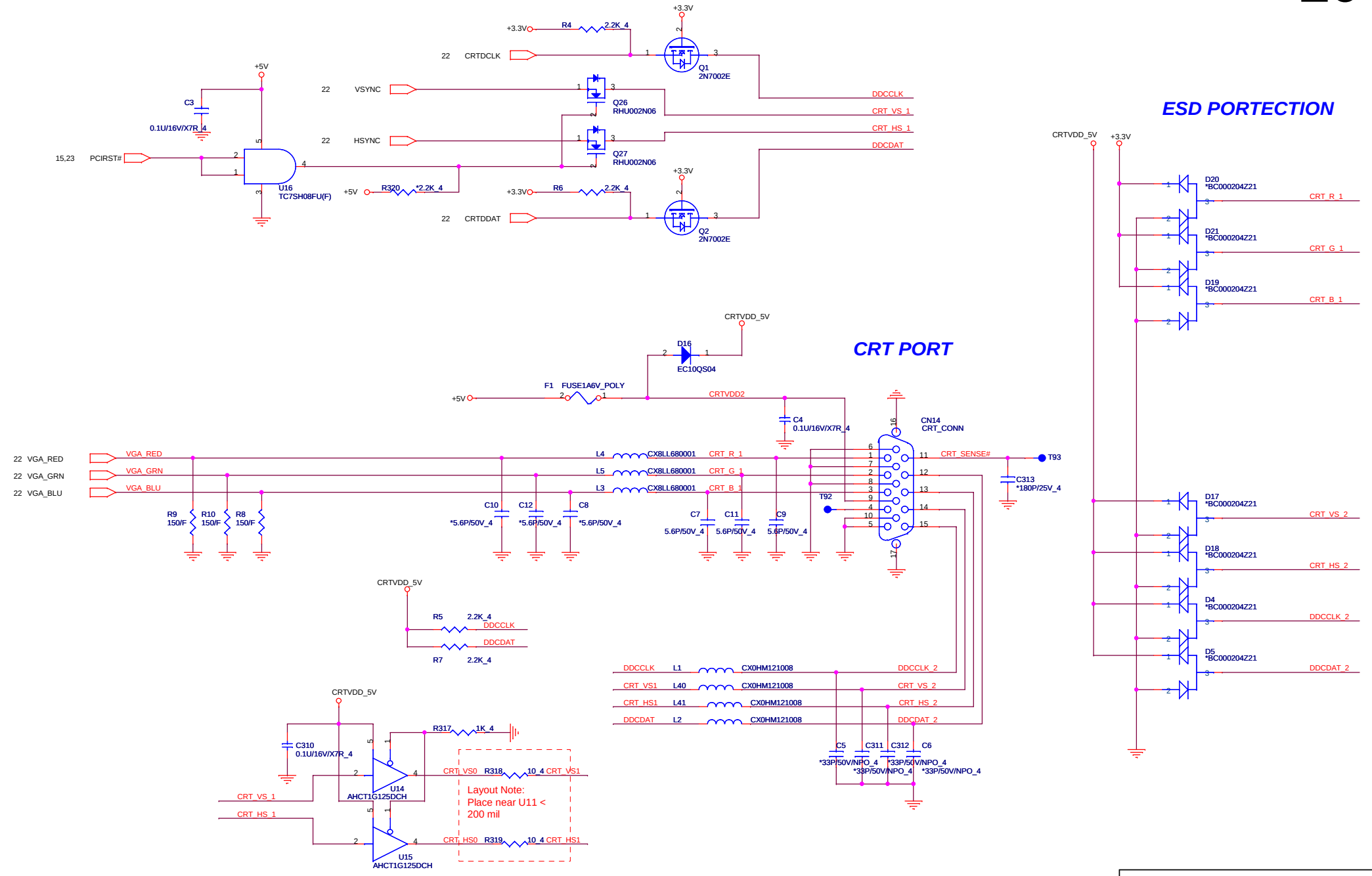
For UMA HDMI function

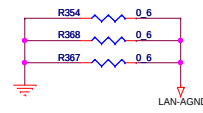
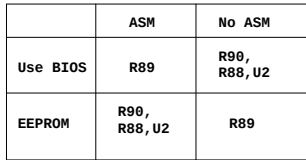
Level Shift



PROJECT : AJ2
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Size	Document Number	HDMI	Rev
Custom			1A
Date:	Tuesday, September 16, 2008	Sheet 19	of 43



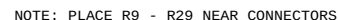


	ASM	No ASM
Use BIOS	R89	R90, R88, U2
EEPROM	R90, R88, U2	R89

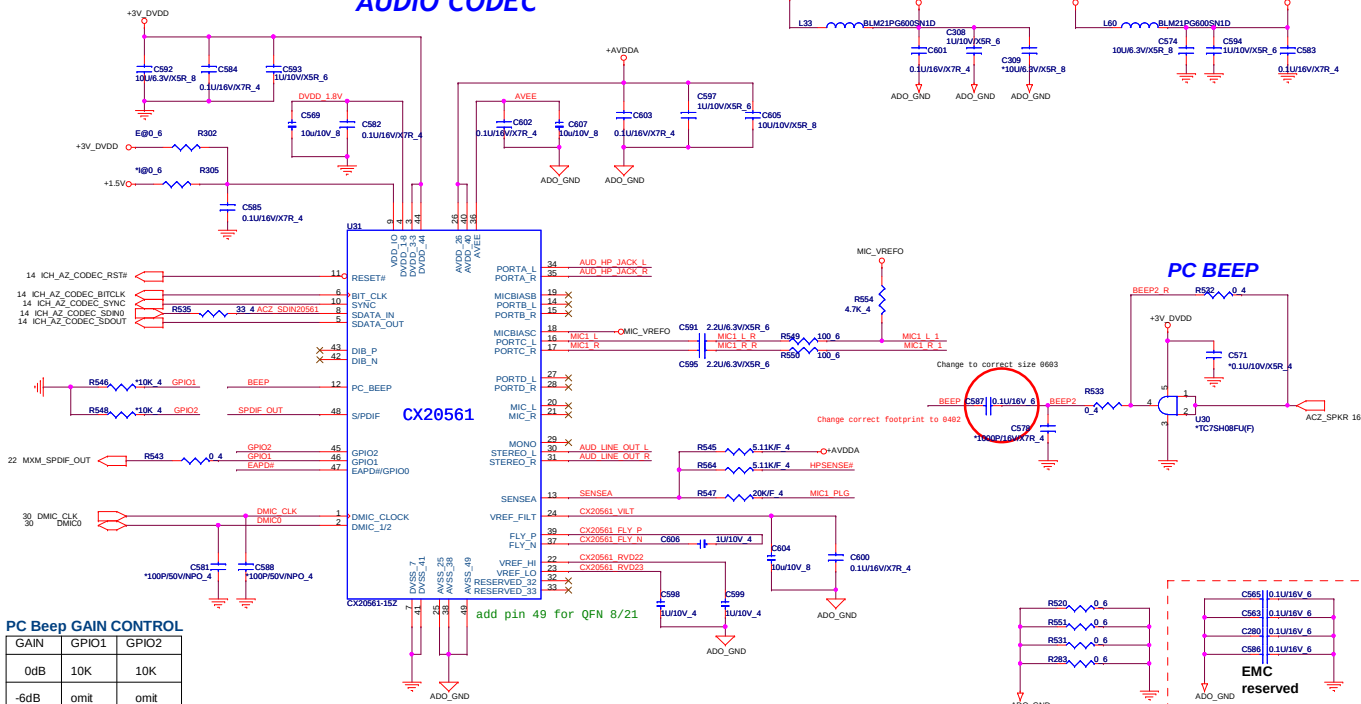


Size Custom	Document Number LAN(Marvell 88E8057)	Rev 1A
Date: Tuesday, September 16, 2008	Sheet 21	of 43

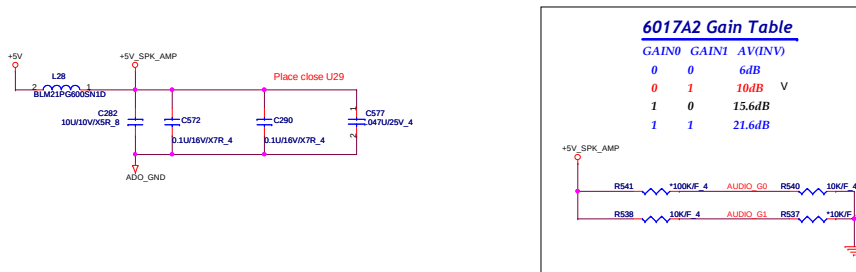
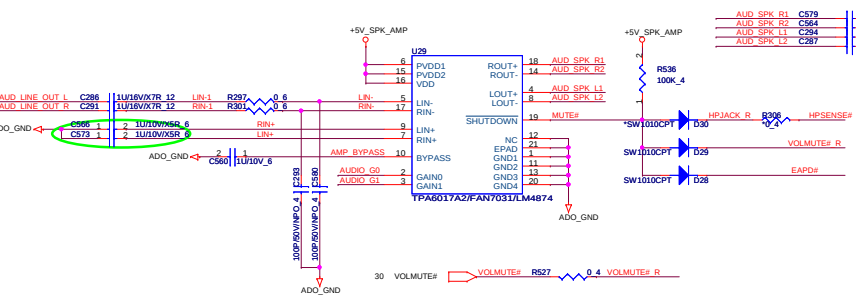




AUDIO CODEC

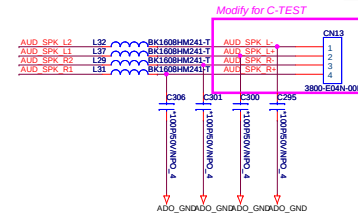


AUDIO AMPLIFIER

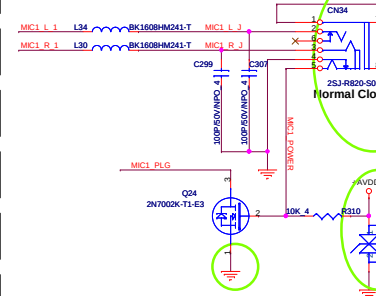


Int. Stereo Speakers

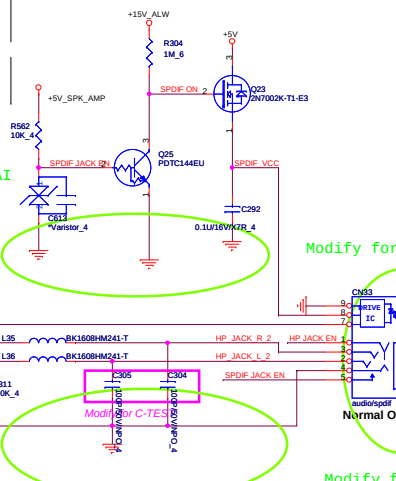
24



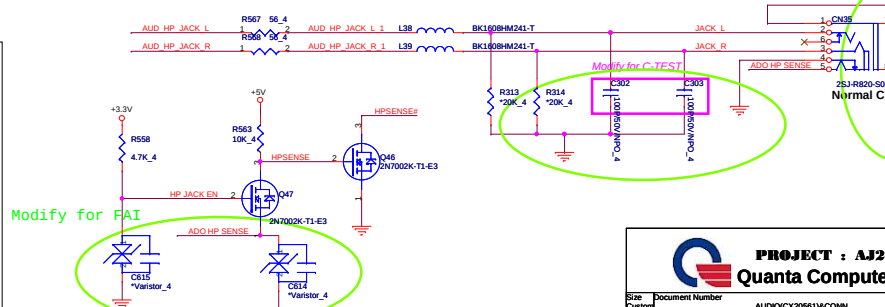
EXT. Mic in

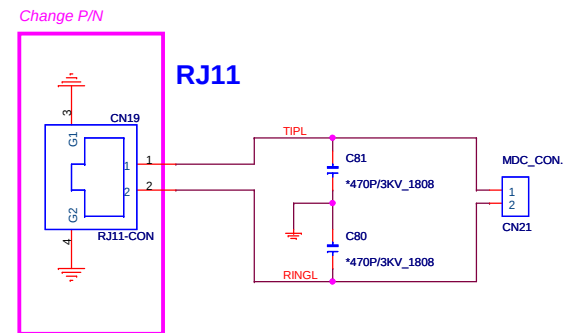
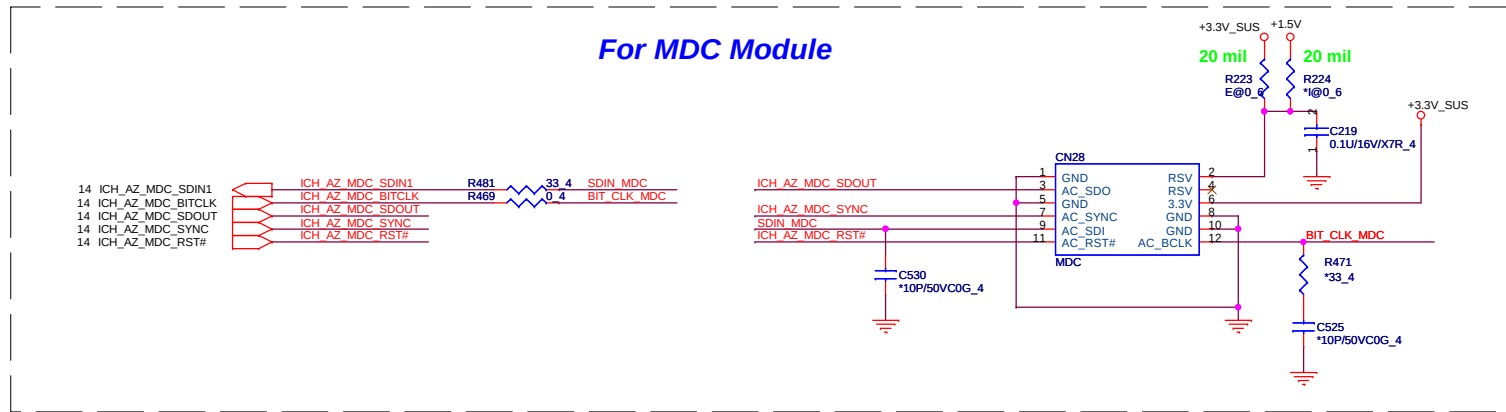


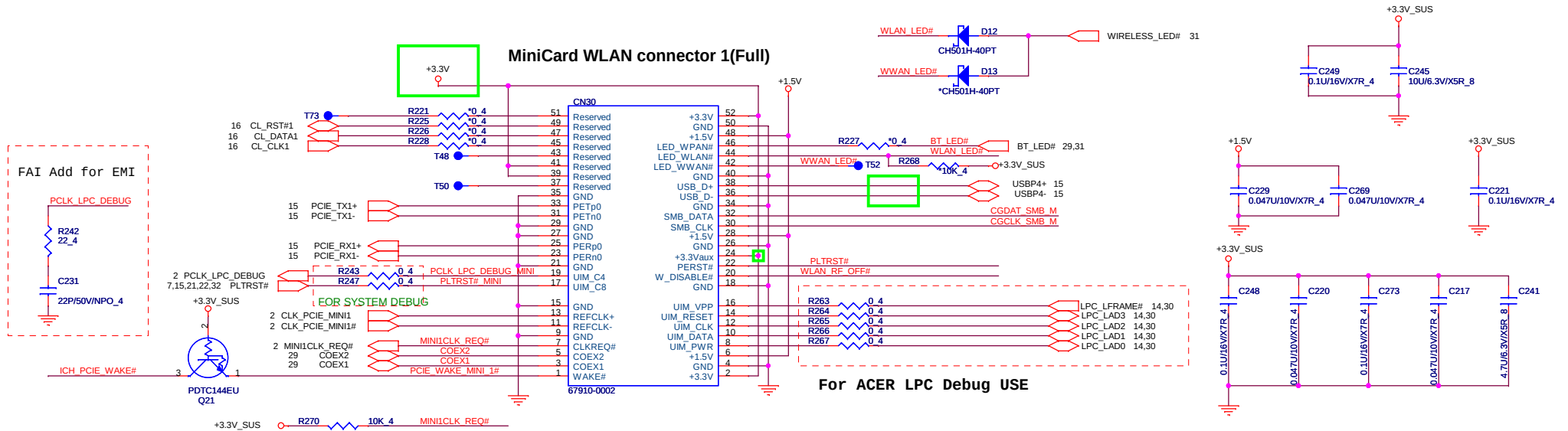
Headphone out + Spdif Out



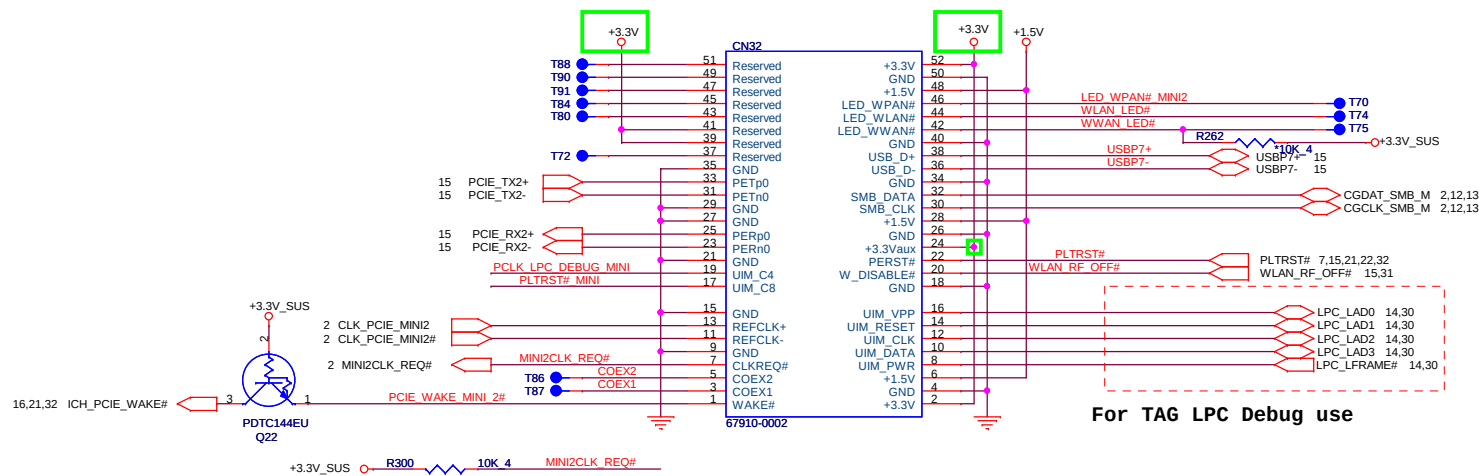
AUDIO JACK



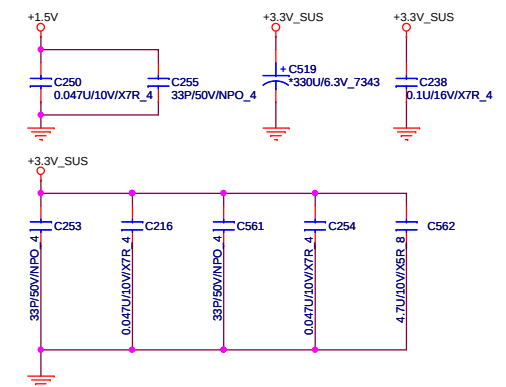




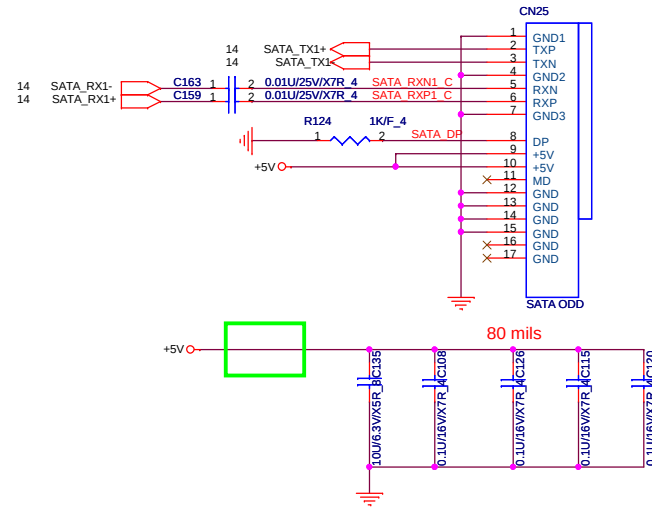
MiniCard connector 2 (half)



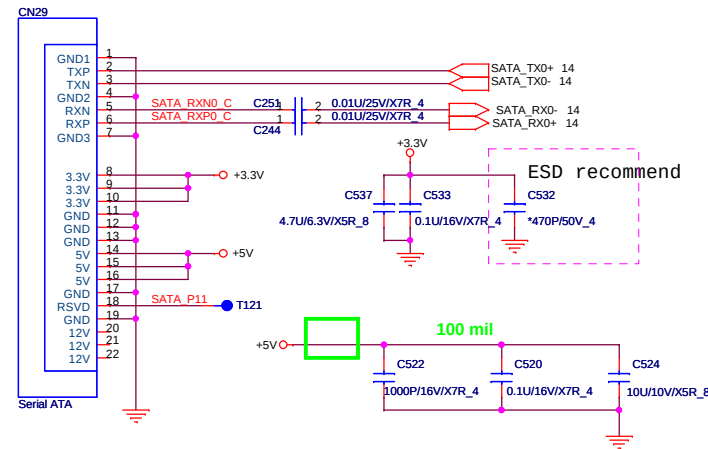
For TAG LPC Debug use

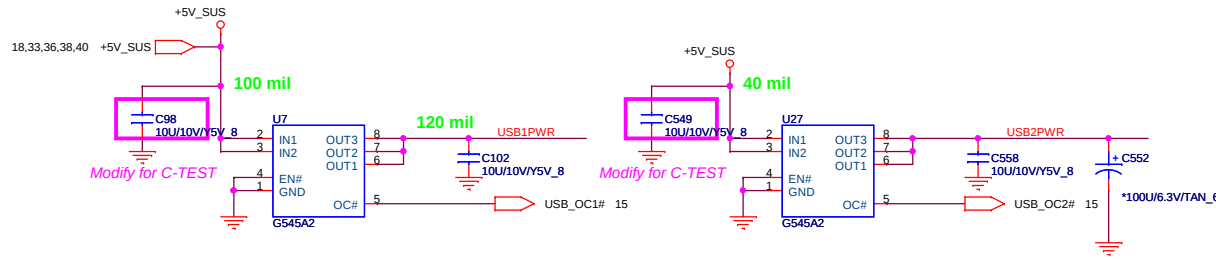


SATA CD-ROM

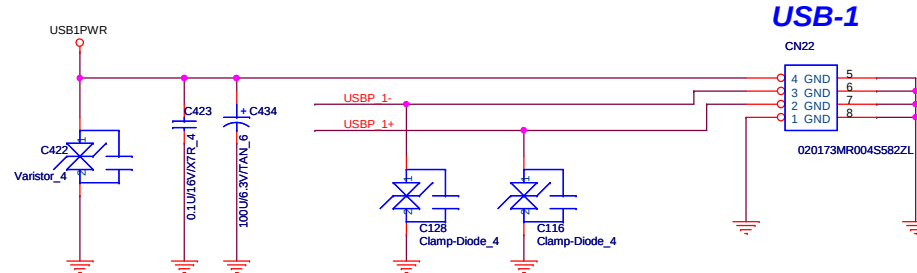
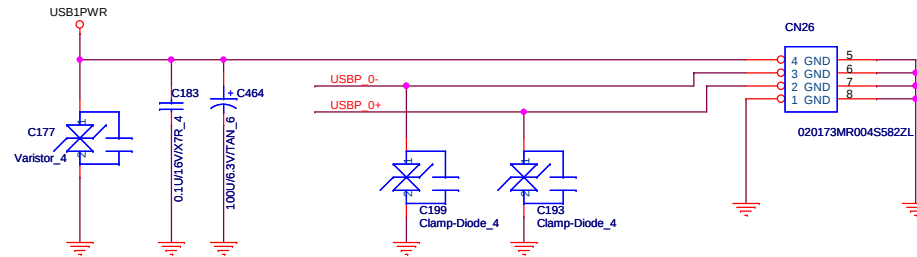
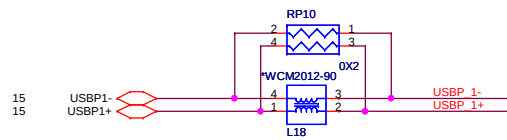
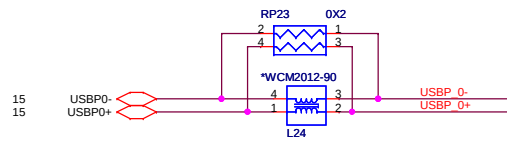
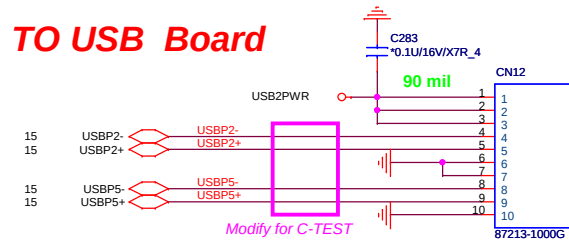


SATA CONNECTOR

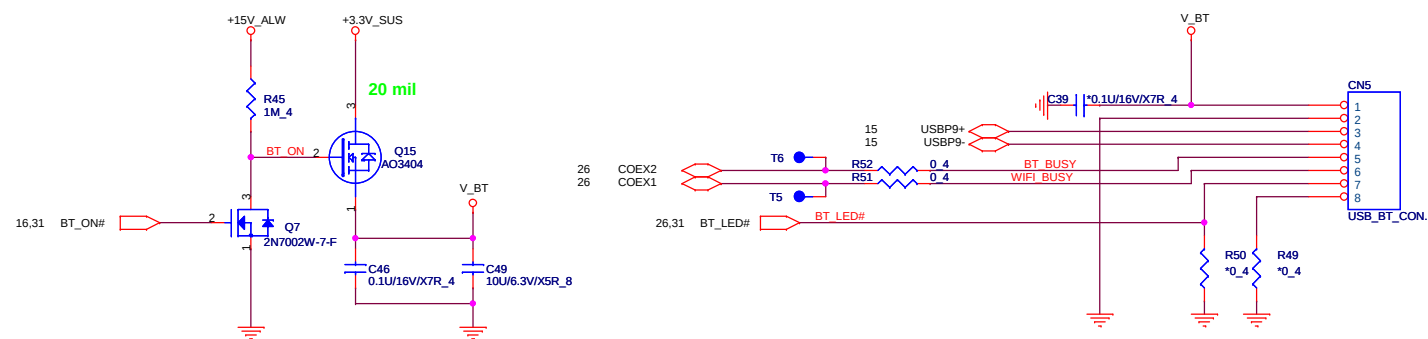




TO USB Board



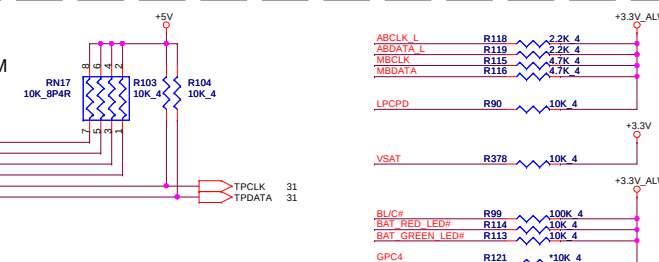
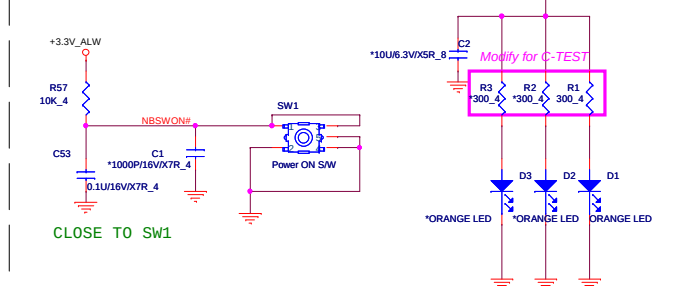
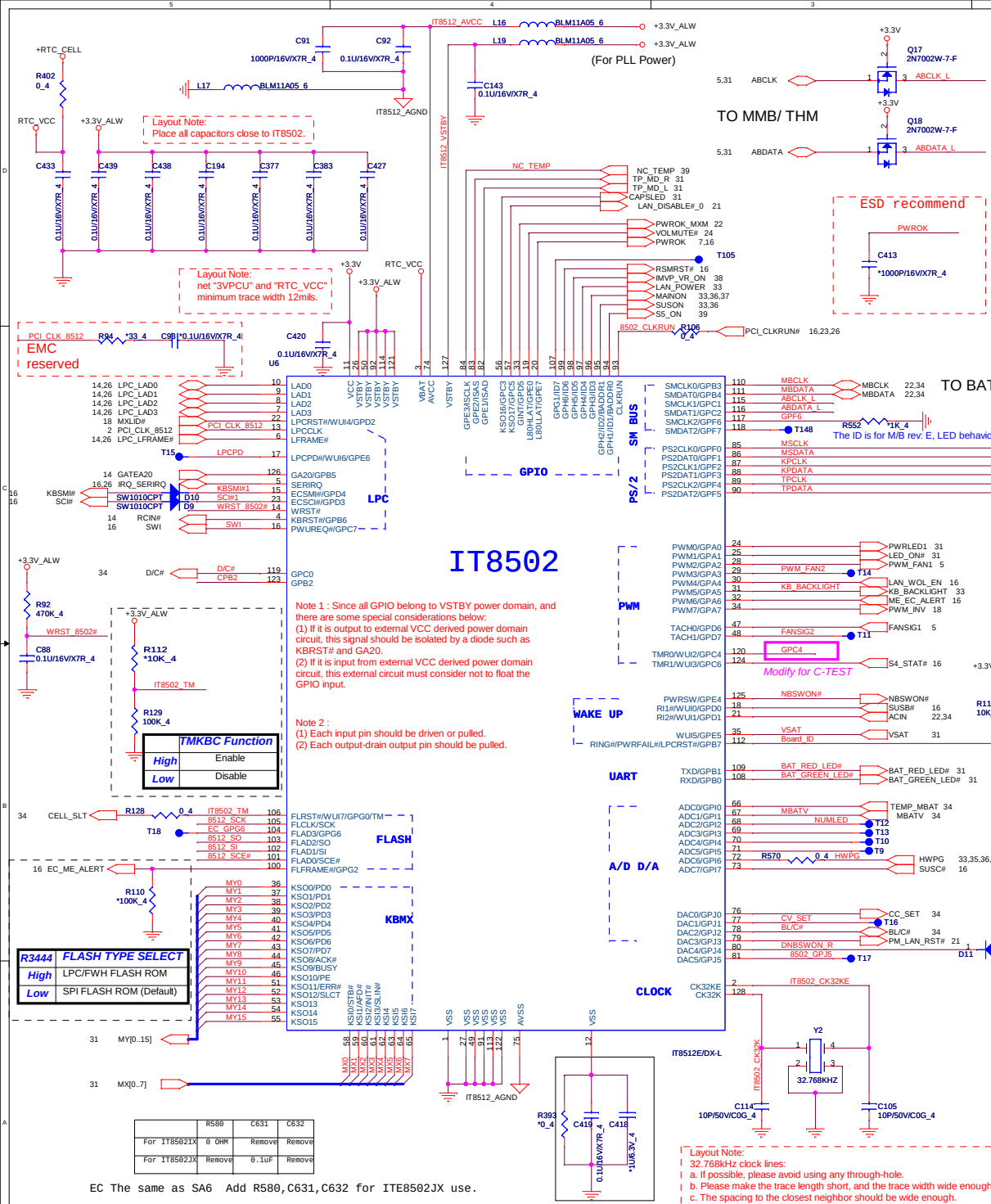
BLUETOOTH CONNECTOR



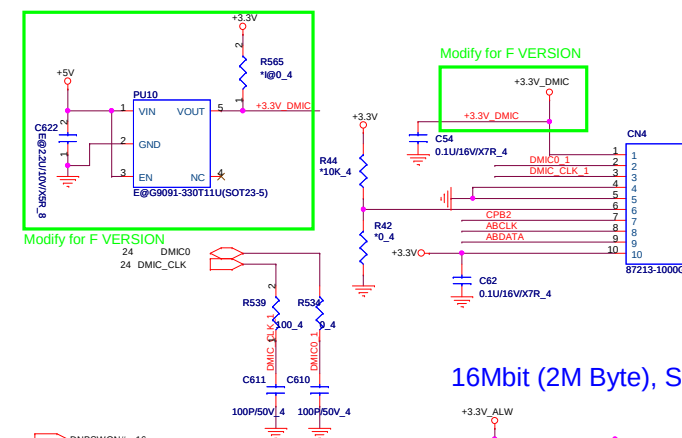
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Quanta Computer Inc.

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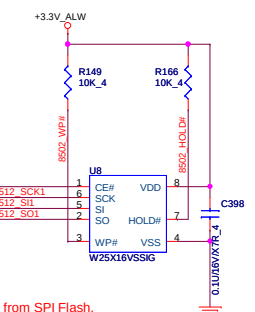
POWER SWITCH



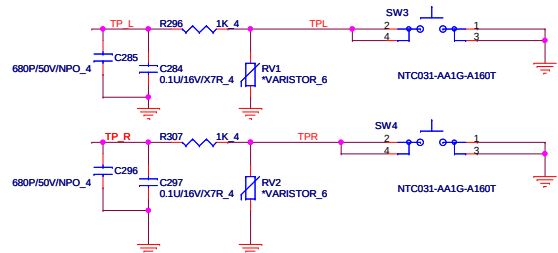
Didital Mic & Light Sensor



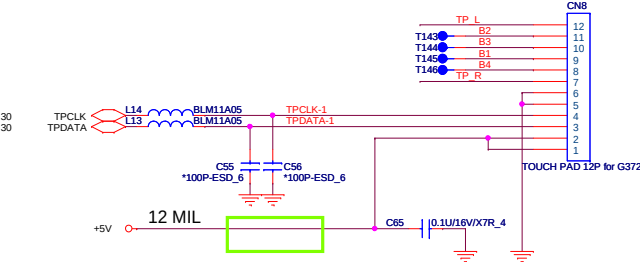
16Mbit (2M Byte), SPI



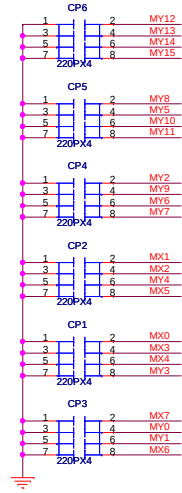
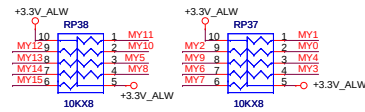
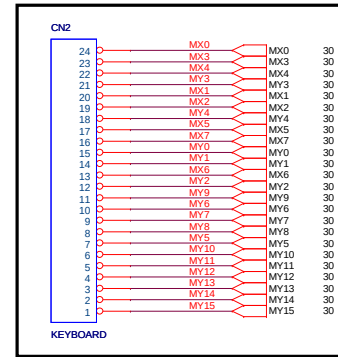
Layout Note:
Place R226,R205,R210 within 500 mils from SPI Flash



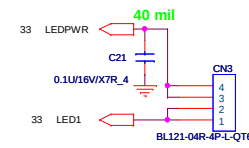
TOUCHPAD SWITCH CONN



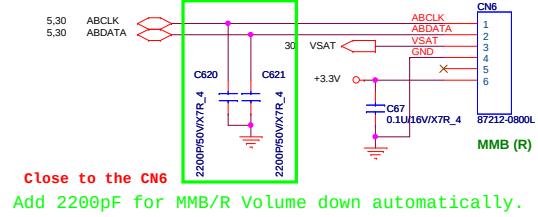
KEYBOARD For New Keyboard use.



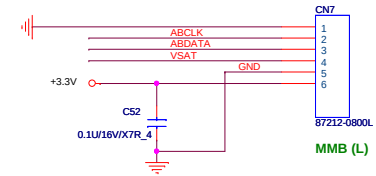
LED Power



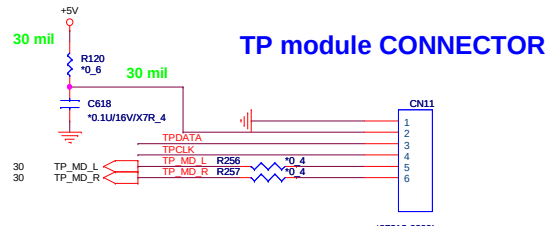
TO EC/ THM Modify for F VERSION



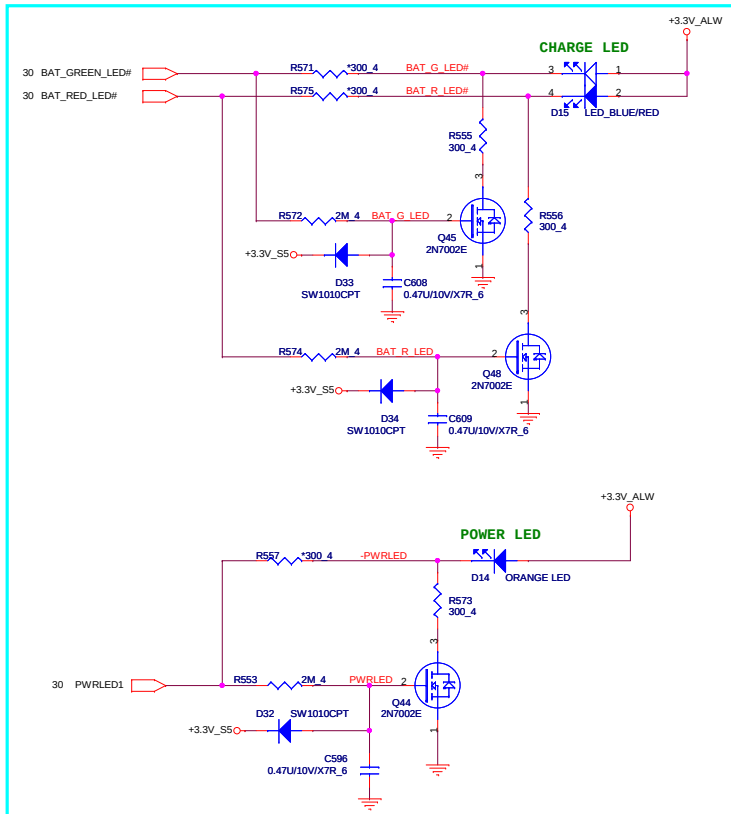
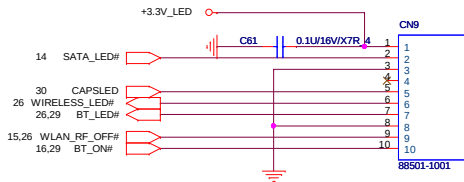
Close to the CN6
Add 2200pF for MMB/R Volume down automatically.



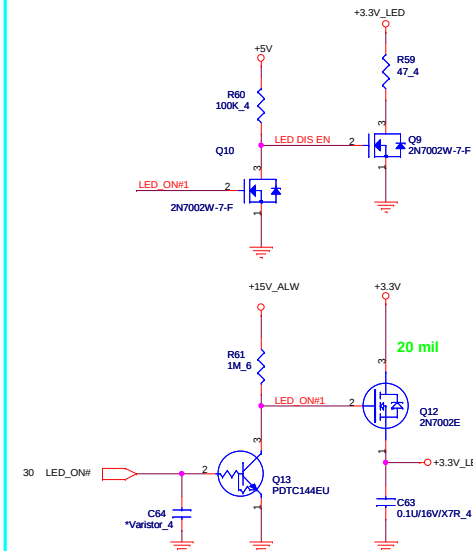
MMB

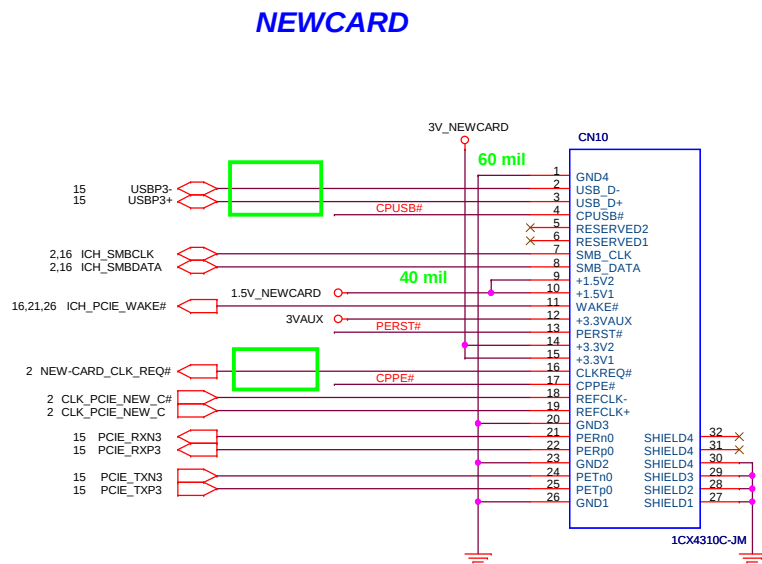
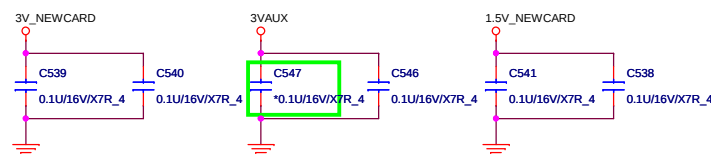


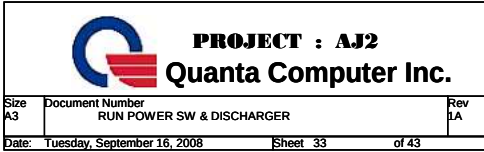
To LED board

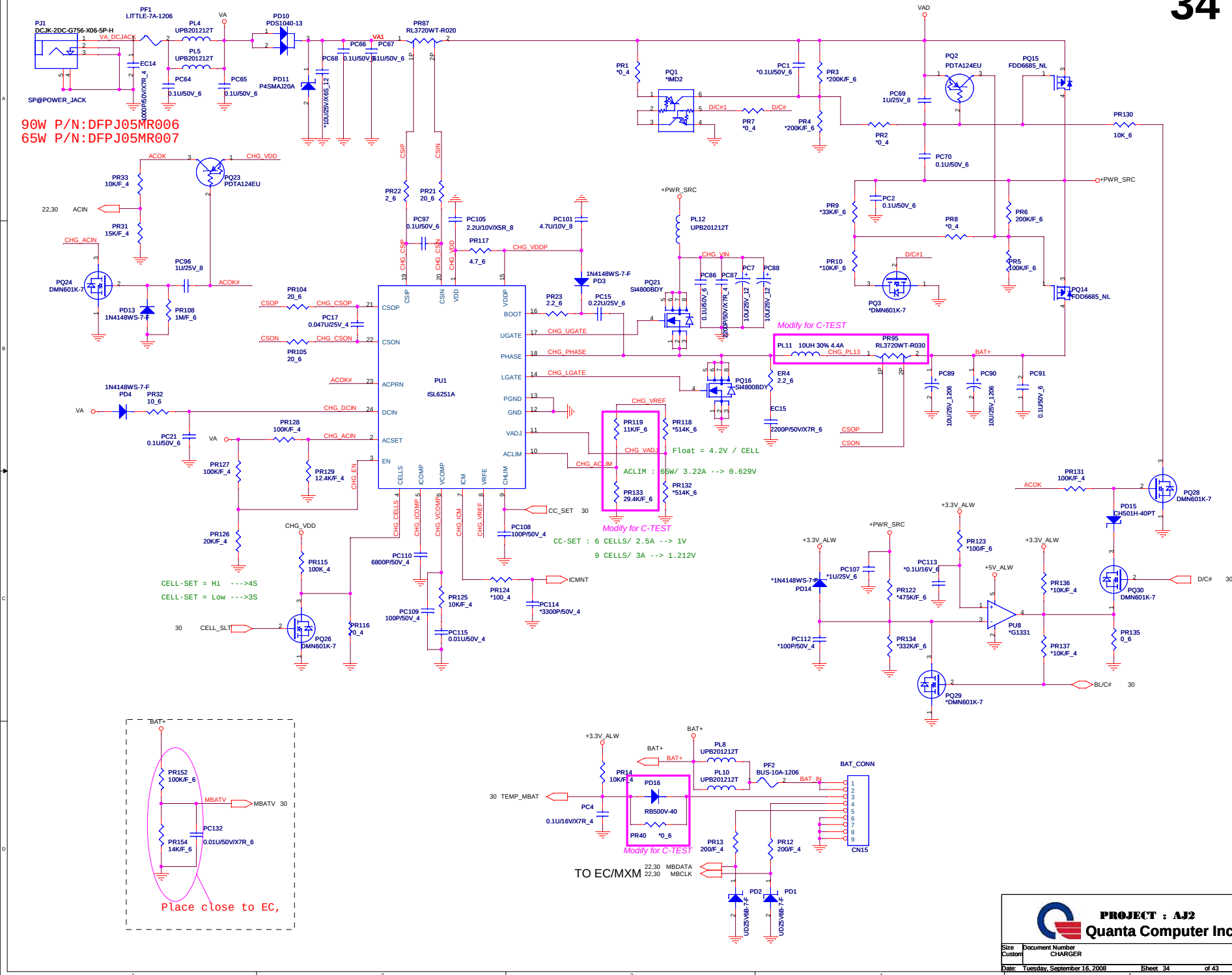


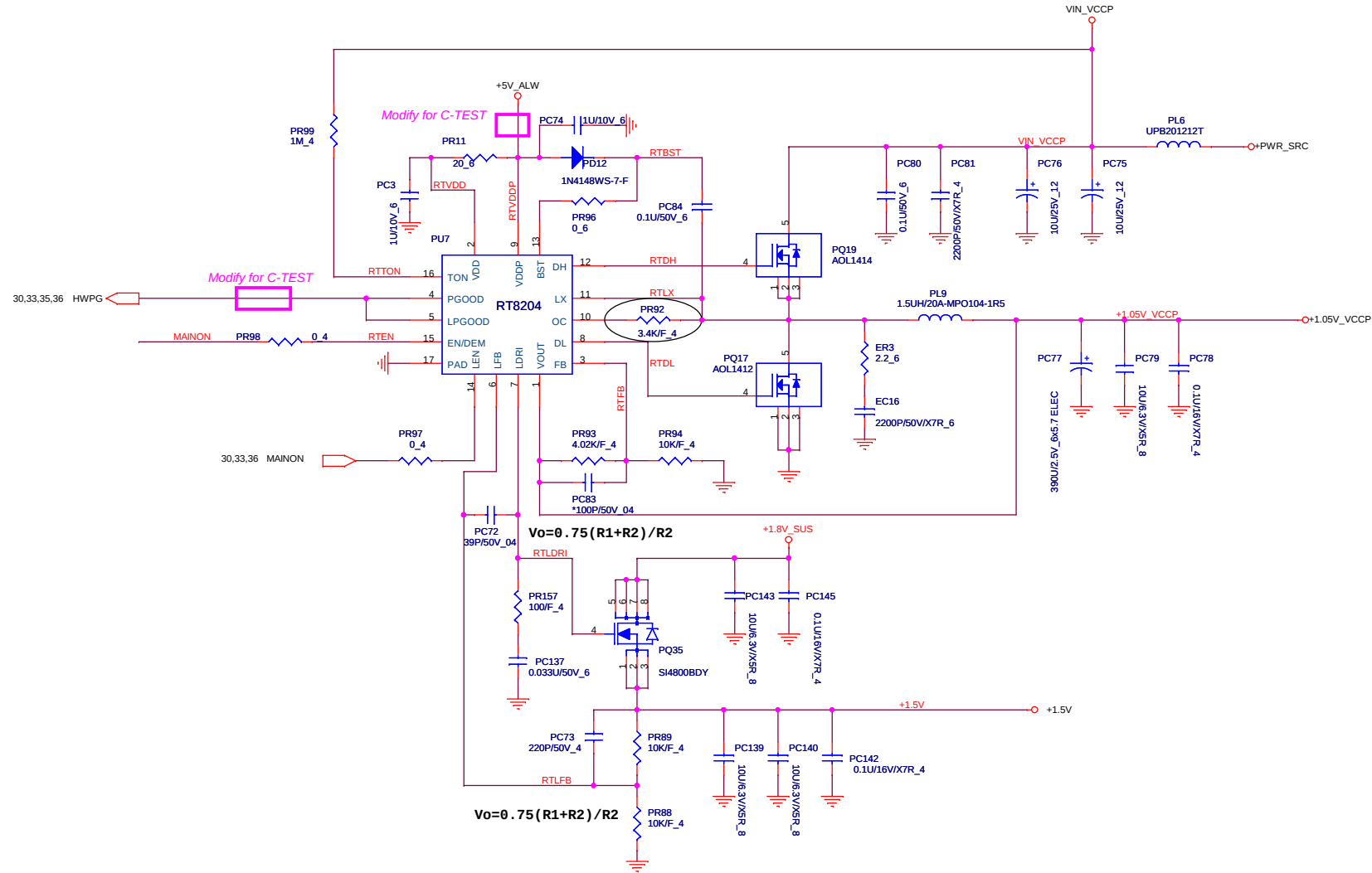
Modify for RAMP



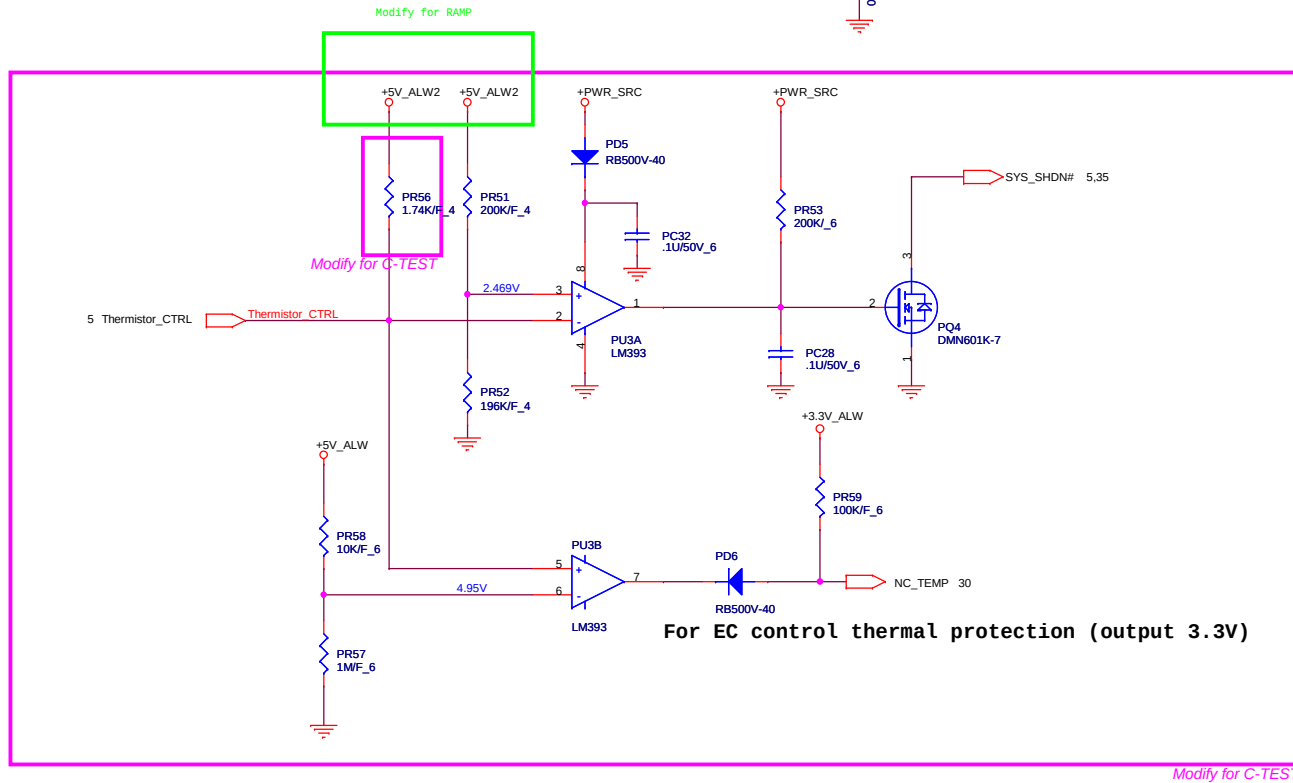
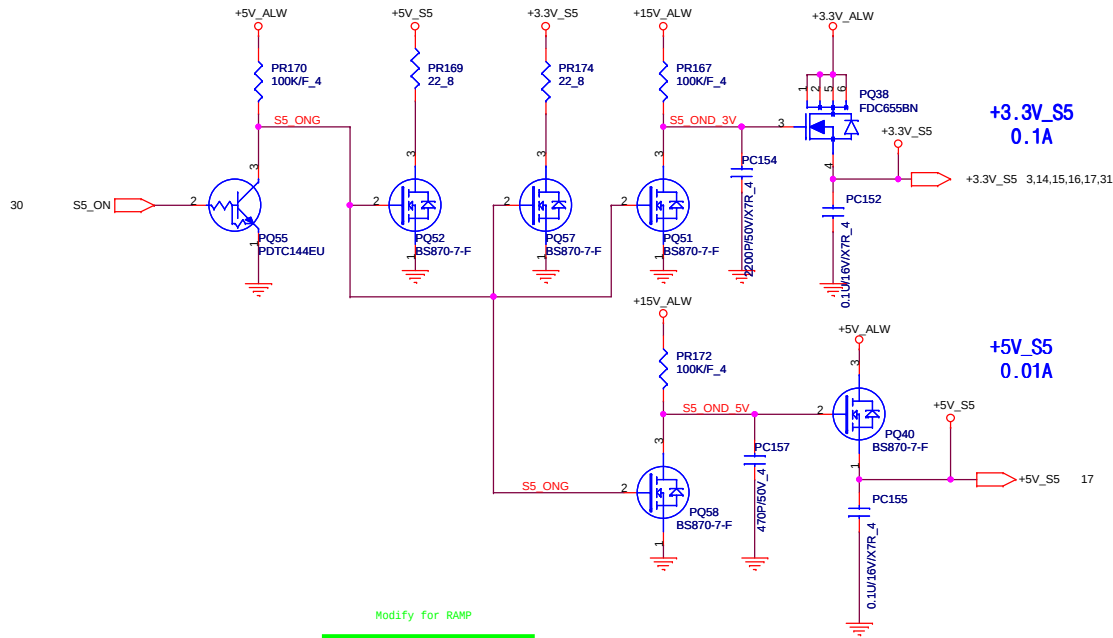








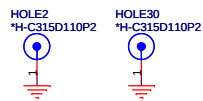
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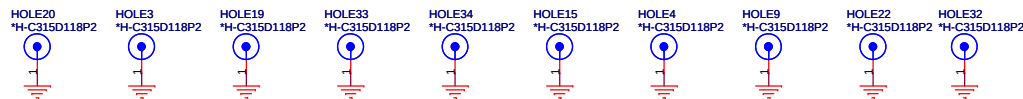
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Quanta Computer Inc.

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A-Type H-C315D102P2

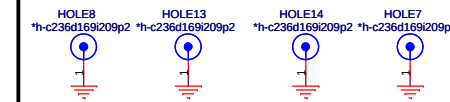


B-Type H-C315D118P2 *12 PCS.



C-Type H-TC315D169P1

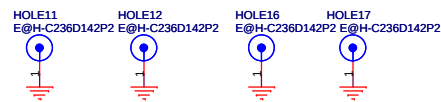
CPU SCREW HOLE



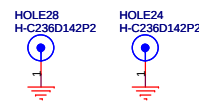
for wireless wire



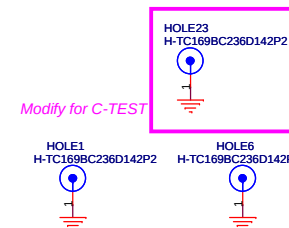
for MXM NUT*4



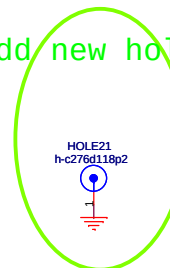
for MDC NUT*2



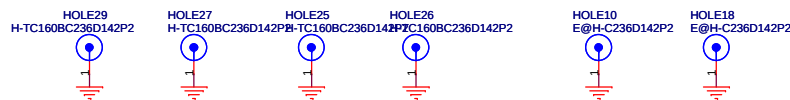
for NB UNT



Add new hole boss



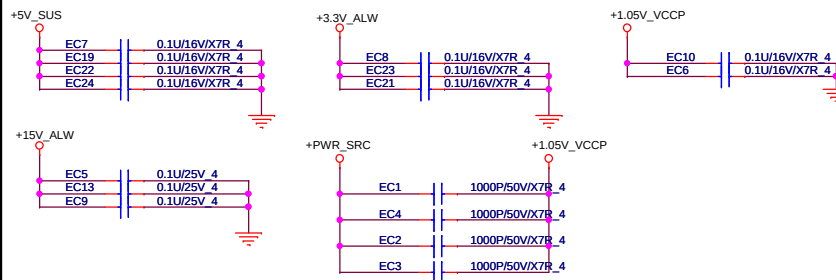
for Mini PCIE NUT*4



Full

Half

EMI Use



MODEM



Modify for C-TEST

Power JACK ESD PAD



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EC A06 page7 R154,R157 Change HSYNC, VSYNC value form 30.1 to 24.9/F
EC A08 page7 R418 Change LVDS_IBG value form 24K/F to 2.4K/F
EC A07 page7 R159 Change CRTIREF value form 75/F to 1K/F
EC A03 page9 Modify to *E@0_6 R91,R93 for UMA BOM .
EC A04 page16 Add R544,R561 for LCD GPIO fucction use!.
EC A19.page18 Change R344,345 value from 0 ohm to 1K ohm for lid S/W function .
EC A19.page18 ADD L11 Del R46,R47 for EC Backlight control function .
EC A04 page19 Del R341,D6 for HDMI LEVEL SHIFT use!.
EC A17.page19 Modify to correct net,ADD RN18 for MXM HDMI SCH.
EC A17.page21 Change Value to 75_6 (R40,358,359,360,362) ;C379 change to 10uf/4v.
EC A10 page22 C457,C468 Modify to *E@XX for UMA BOM.
EC A16.page22 Modify to correct net for UMA HDMI SCH.
EC A14.page25 Del C80,C81 CAP. for MDC RJ11 BOM.
EC A01 page28 USB CONN CN22,CN26 PIN define USB +-data swape it.
EC A05 page28 Change C102,C558 value&footprint 10U/10V_0805 (CH6102M9A01)
EC A12 page30 Del R120,R121 FOR Change the SMBus from 117 & 118 to 115 & 116 .
EC A02 page30 Modify LAN_DISABLE#_0 form pin68 to pin56.
EC A11 page31 Modify CN8 SCH. for TUCHPAD G372 PIN Define.
EC A15.page31 Modify MMB(L) CN7.Pin6 net TO GND .
EC A18.page31 Del. T/P module CONNECTOR SCH .
EC A20 page31 Modify LED POWER CONN. CN3 PIN define .
EC A09 page37 PR93 Change value from 4.7K/F to 4.02K/F for +1.05V use.
EC A13.page40 Del Hole11,12,16,17 MXM NUT for UMA BOM.

- 1.EC page2 _Remove 0 ohm resistance array(RP18,RP19,RP20,RP21,RP29,RP22,RP28,RP27,RP26,RP25).
- 2.EC page7 _Remove R89,R86 and NET(PLTRST#_R).
- 3.EC page10 _Change L56,L57 to R560,R559.
- 4.EC page15 _Not stuff U10,C257,R251,R293,R252,R253,R294,R295.
- 5.EC page17 _Not stuff U22,C510,R446,R431,C514 for MXM.
- 6.EC page18 _Remove 0 ohm resistance L10.
- 7.EC page18 _Modify LCD Connector's pin definition(PIN37 from GND to NC).
- 8.EC page19 _Change R322 value form 100K/F to 20K/F.
- 9.EC page21 _Not stuff U5,R77,R80 ; stuff R83.
- 10.EC page21 _Change R358,R359,R360,R362,R40 footprint from 0603 to 0805.
- 11.EC page21 _Change C25 value from 1500pF to 1000pF(same as C66).
- 12.EC page24 _Modify SPEAKER Connector's pin definition(mirror).
- 13.EC page24 _Change C298,C305,C304,C302,C303 footprint from 0603 to 0402.
- 14.EC page28 _Remove 0 ohm resistance array RP32,RP33.
- 15.EC page28 _Change C98,C549 value from 22uF to 10uF.
- 16.EC page30 _Add R552(1k) and R121(*10k) to pull low and pull high.
- 17.EC page30 _Remove R122(10k) and net EC_GPB7.
- 18.EC page30 _Change R1,R2(*),R3(*) value from 150 ohm to 300 ohm.
- 19.EC page31 _Modify MMB Connector's pin definition(mirror:CN6,CN7).
- 20.EC page31 _Modify LED Display circuit.
- 21.EC page33 _Change PL1 value from 22UH to 10UH.
- 22.EC page33 _Remove 0 ohm resistance PR65,PR60.
- 23.EC page34 _Change PL11's part number to CV01044TZ01.
- 24.EC page34 _Add PD16 and PR40(*) on BAT CON's pin3 to avoid leakage current.
- 25.EC page34 _Change PR95 part number to CS+0308FL00.
- 26.EC page34 _Change PR133 value from 11k/F ohm to 29.4k/F ohm .
- 27.EC page34 _Change PR119 value from 16k/F(MXM) or 75K/F(UMA) ohm to 11k/F(MXM) or 178K/F(UMA) ohm .
- 28.EC page35 _Change PL19 and PL18 part number to CV-2575TZ04.
- 29.EC page35 _Short PU6 pin9 and pin10.
- 30.EC page35 _Remove 0 ohm resistance PR77.
- 31.EC page35 _Stuff PC56.
- 32.EC page36 _Remove 0 ohm resistance PR147,PR148,PR138,PR143.
- 33.EC page36 _Modify PU9 pin23's net from +1.8V_SUSP to +1.8V_SUS.
- 34.EC page36 _Add PR175(*) connect to PU9 pin12 and pull high to +PWR_SRC_DDR(buffer).
- 35.EC page36 _Change PR149 value from 14k/F ohm to 10.7k/F ohm.
- 36.EC page36 _Change PR151 value from 0 ohm to 2.2 ohm.
- 37.EC page37 _Remove 0 ohm resistance PR90,PR91.
- 38.EC page38 _Remove 0 ohm resistance PR40,PR41,PR42,PR43,PR44,PR45,PR46.
- 39.EC page38 _Change PQ31 and PQ18 part number to BAM80230000.
- 40.EC page38 _Change PQ25,PQ27,PQ20,PQ22 part number to BAM80190000.
- 41.EC page38 _Change PC26 part number to CH733RM8874.
- 42.EC page39 _Stuff PR51,PR52,PR53,PR56,PR57,PR58,PR59,PC28, PC32,PD5, PD6,PQ4,PU3 for EC control thermal protection.
- 43.EC page40 _Change HOLE23's NUT to FBAJ2003010.
- 44.EC page40 _Add SPRING PAD1 to fix MODEM's cable.

- 1.EC page2 _Change C188,C189 value form 30P to 27P for RCT timing.
- 2.EC page2 _Change UAM BOM add original RP24 for LVDS spread spectrum clock issue.
- 3.EC page16 _Change BOARD_ID0 resister to pull low. (remove R201 and add R202).
- 4.EC page16 _Add C612 0.1uF/16v_4 near R27810/F_4 fix RTC CMOS checksum error.
- 5.EC page18 _Add PD18 Close to LCD CONN. CN1 fix U2 break down .
- 6.EC page18 _Del. USB8+- data remove the RP1&L8;Del. R32 0 ohm.
- 7.EC page18 _Change value C325 from 0.1U/16V/Y5V to 0.1U/16V/X7R .
- 8.EC page24 _Change GND CN33,34,35 from ADO_GND to Digital_GND for ESD solution.
- 9.EC page24 _Add *C619 Varistor_0402 near R310 for ESD use.
- 10.EC page26 _Change net CN30,32 name from +3.3v_sus to +3.3v .
- 11.EC page30 _Del. R552 for EC change to"slowly pulse" detect pin use .
- 12.EC page30 _Add +3.3V C54,C62 0.1UF/16V;C610,C611 100P/50V near CN4.
- 13.EC page30 _Move the R539,R534 from 24 page to 30 page.
- 14.EC page31 _Modify BOM to POWER,Charge LED bevhavior "solwly pulse" .
- 15.EC page26,27,31,32 _Del. 0 ohm RP30,RP31,R230,R233,R254,R255,R229,L20,L59,L12,R569,R248 cost doown .
- 16.EC page22 _ ADD PC162 100U/25V.
- 17.EC page35 _ ADD PD17 ;Change value PR67 to 200K/F_4 PR66 to 100K/F_4.
- 18.EC page36 _Change value PC130 to 27U/25V .
- 19.EC page38 _Change value PC118 to 27U/25V .

- 20.EC page30 _ ADD LDO(PU10) circuit to reduce DMIC noise.
- 21.EC page31 _Add 2200pF(C620,C621) for MMB/R Volume down automatically issue.
- 22.EC page21 _Change transformer's PCB footprint.