

ZB2

CPU CORE
SENTECH
SC4511TSTR
 Page: 32

SYSTEM 3V/5V
MAXIM
MAX1999
+3VPCU
+3V S5
+3VSUS
+3V
+5VPCU
+5VSUS
+5V
+15V
 Page: 33

+1.8VSUS
+1.8V
+0.9VSUS
+0.9V
+1.5V
+1.05V
 Page: 34
+2.5V
+1.2V
VGA_CORE
 Page: 36

BATTERY CHARGER
MAXIM
MAX8724
 Page: 35

CLOCK GEN
ICS954310BG
 Page: 4

Yonah/Merom
INTEL Mobile_479 CPU
 Page: 2, 3

VRAM x4
DDR2
16Mx16
32Mx16

CRT
 Page: 22
LVDS
 Page: 22

DDR-II SODIMM1
 Page: 12

DDR-II SODIMM2
 Page: 12

CALISTOGA-GM
1466 FCBGA
 Page: 5, 6, 7, 8, 9, 10

ATI
M52P
/M52PG
/M54P
 Page: 17, 18, 19, 20
UMA(option)

MINI-Card slot
Wireless LAN
 Page: 24

SATA HDD
 Page: 23

PATA HDD
 Page: 23

IDE-ODD
 Page: 23

ICH7-M
652 BGA
 Page: 13, 14, 15, 16

TI PCI7412
AD25
REQ0#
GNT0#
INTE#
INTF#
INTG#
 Page: 26

TYPE II
SLOT
 Page: 26

6 IN 1
Cardreader
 Page: 27

MINI-PCI
Wireless LAN
AD19
REQ2# / GNT2#
INTC# , INTD#
 Page: 24

REALTEK
RTL8100CL
AD16
REQ1#
GNT1#
INTB#
 Page: 25

RJ45
 Page: 25

AUDIO CODEC
Realtek
ALC883 (ALC260)
 Page: 28

AMP
MAX9755
 Page: 29

MODEM
 Page: 28

MIC IN
 Page: 29

SPEAKER
 Page: 29

LINE OUT
 Page: 29

KBC
NS PC97551/541V
 Page: 30

Touchpad
 Page: 29

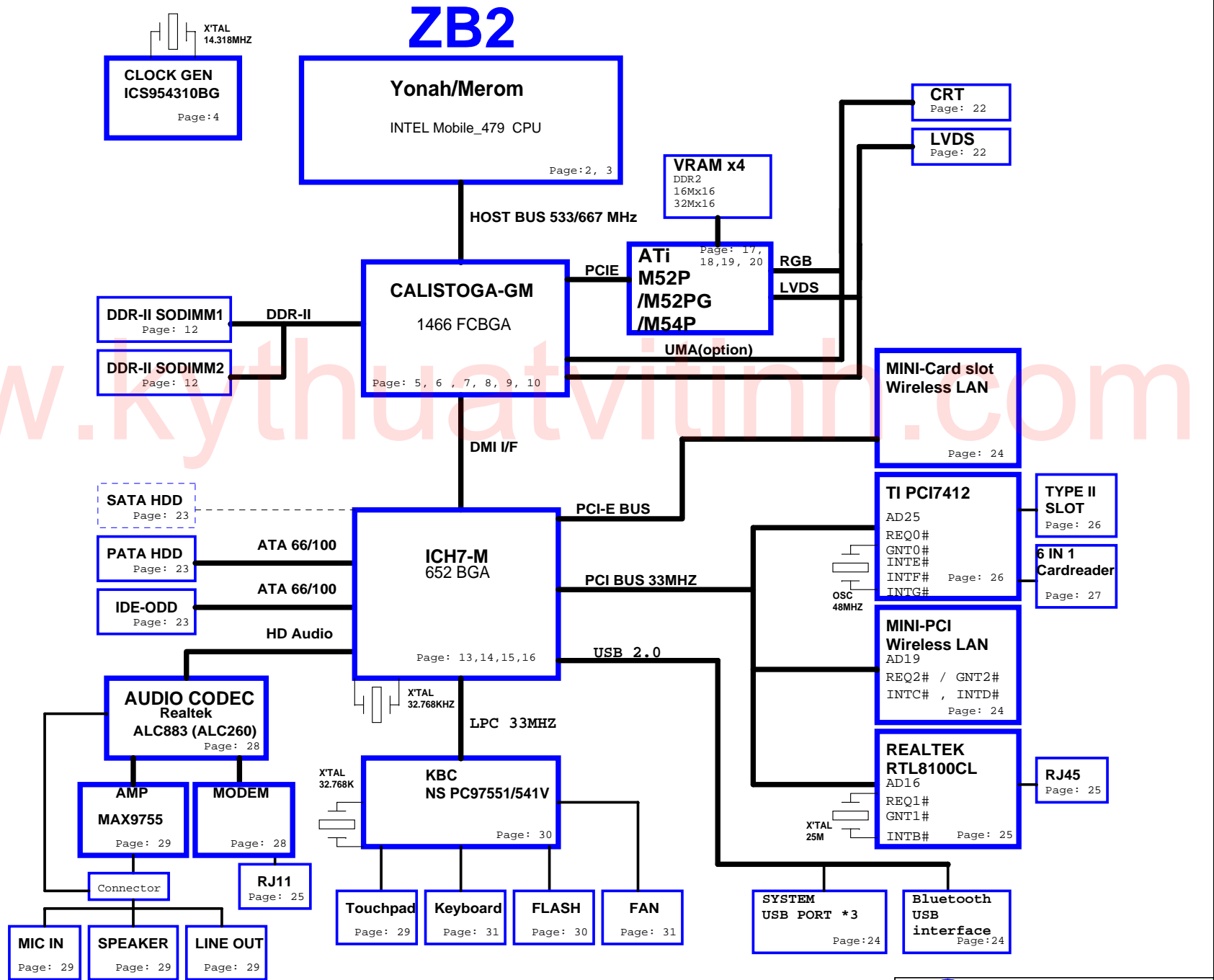
Keyboard
 Page: 31

FLASH
 Page: 30

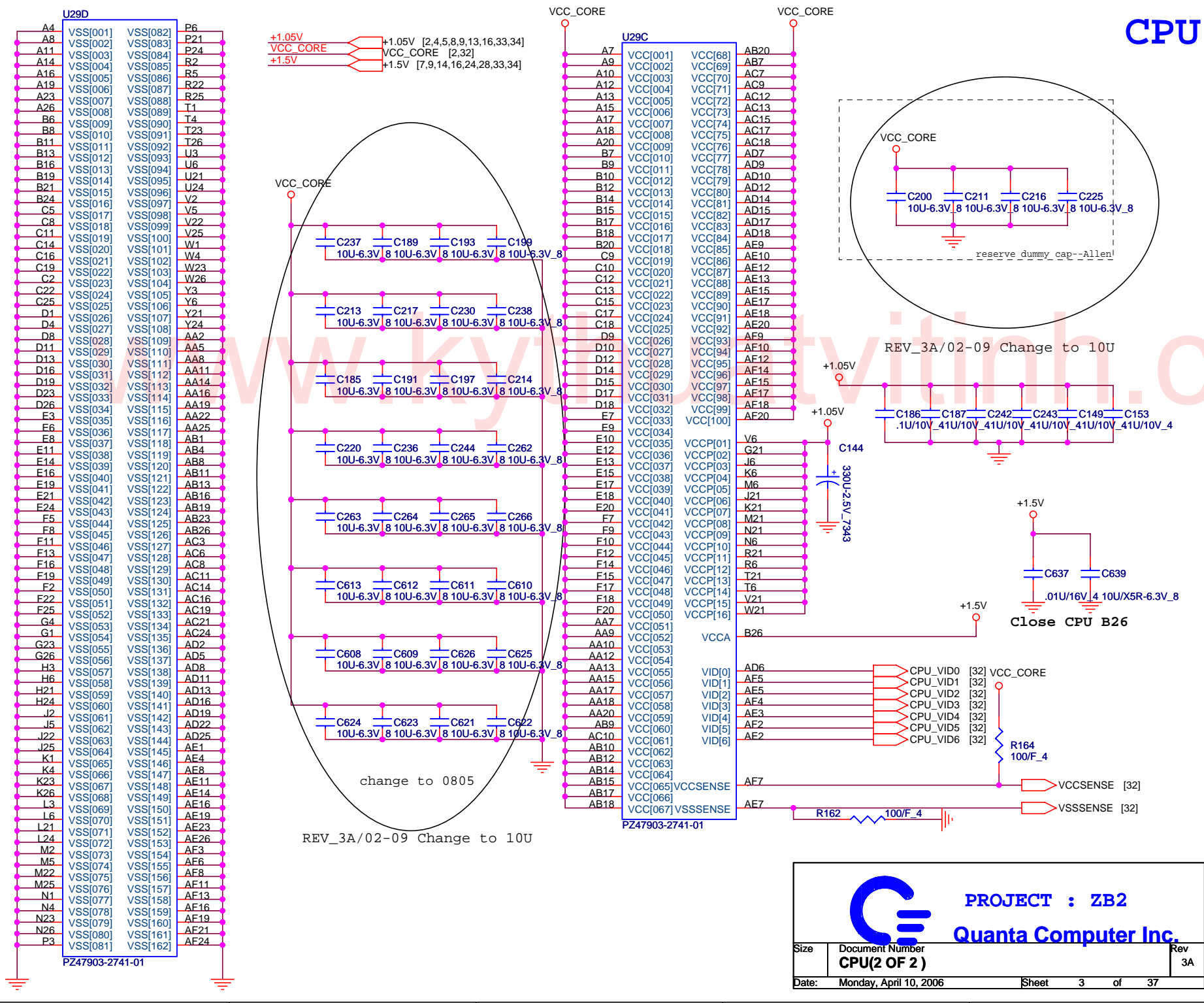
FAN
 Page: 31

SYSTEM
USB PORT *3
 Page: 24

Bluetooth
USB
interface
 Page: 24



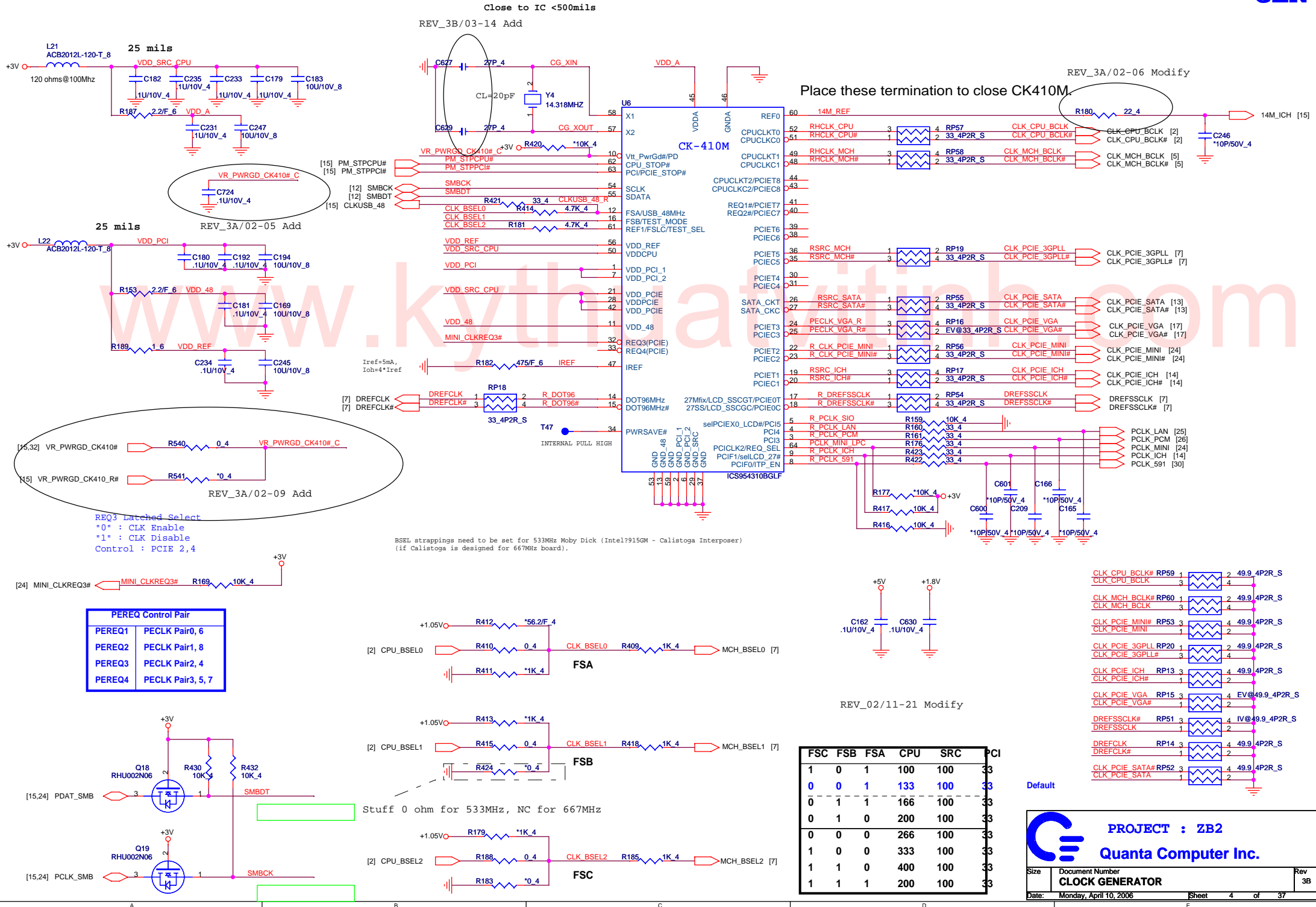
CPU

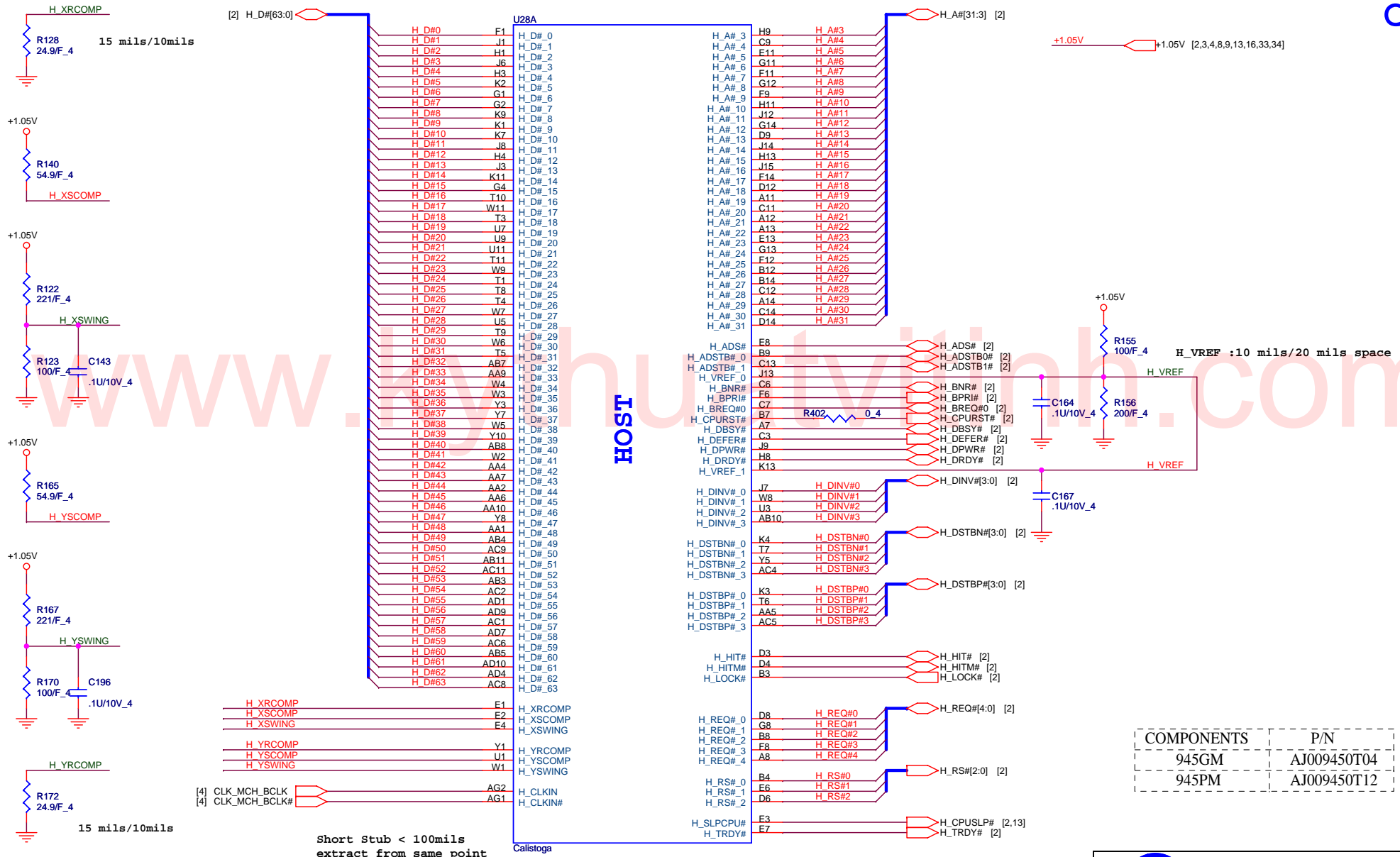


PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number CPU(2 OF 2)	Rev 3A
Date:	Monday, April 10, 2006	Sheet 3 of 37

Note : If Use Internal VGA Please NC "EV@xxx" Parts





[2] H_D#(63:0)

H_A#(31:3) [2]

+1.05V -1.05V [2,3,4,8,9,13,16,33,34]

H_VREF :10 mils/20 mils space

HOST

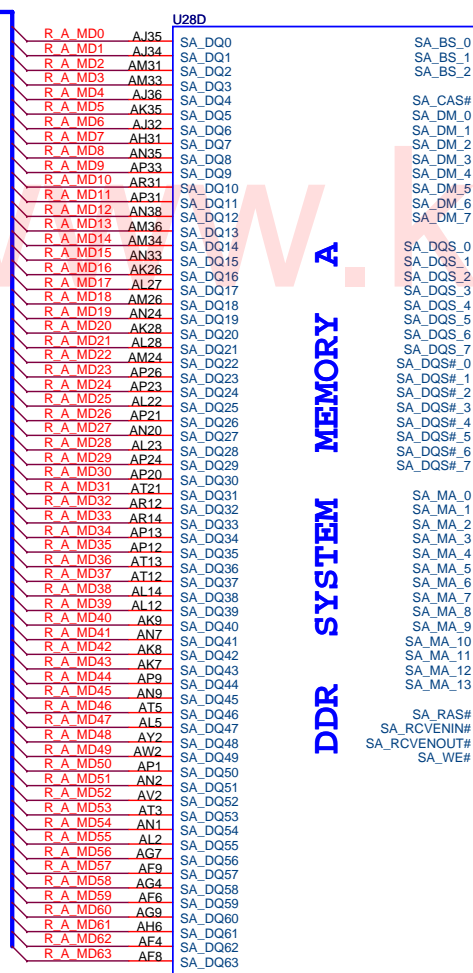
Short Stub < 100mils
extract from same point

Calistoga

PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST(1 OF 6)	1A
Date:	Monday, April 10, 2006	Sheet 5 of 37

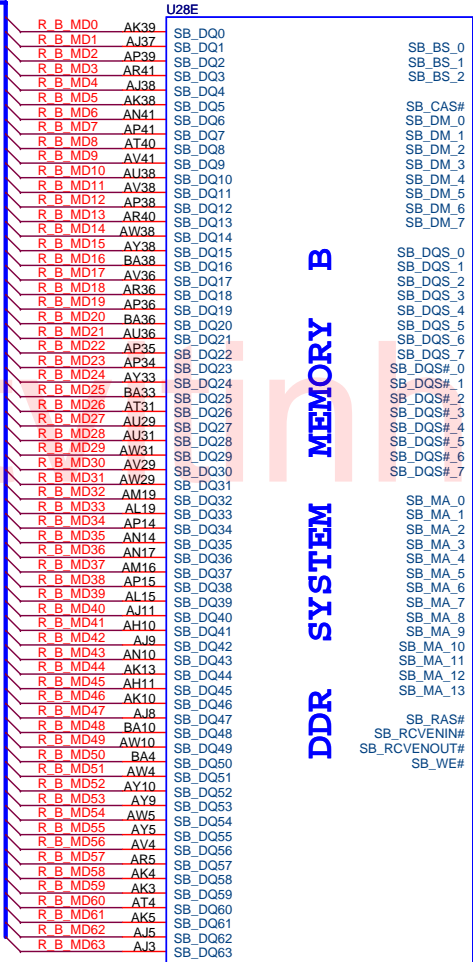
[12] R_A_MD[0..63]



U28D

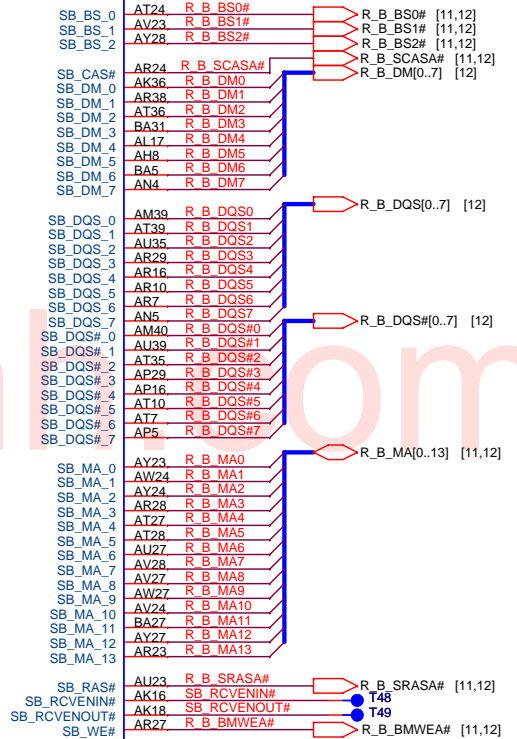
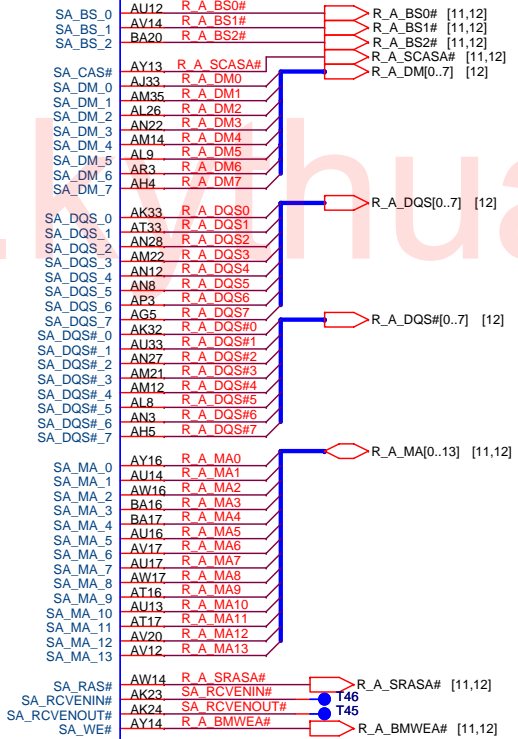
Calistoga

[12] R_B_MD[0..63]



U28E

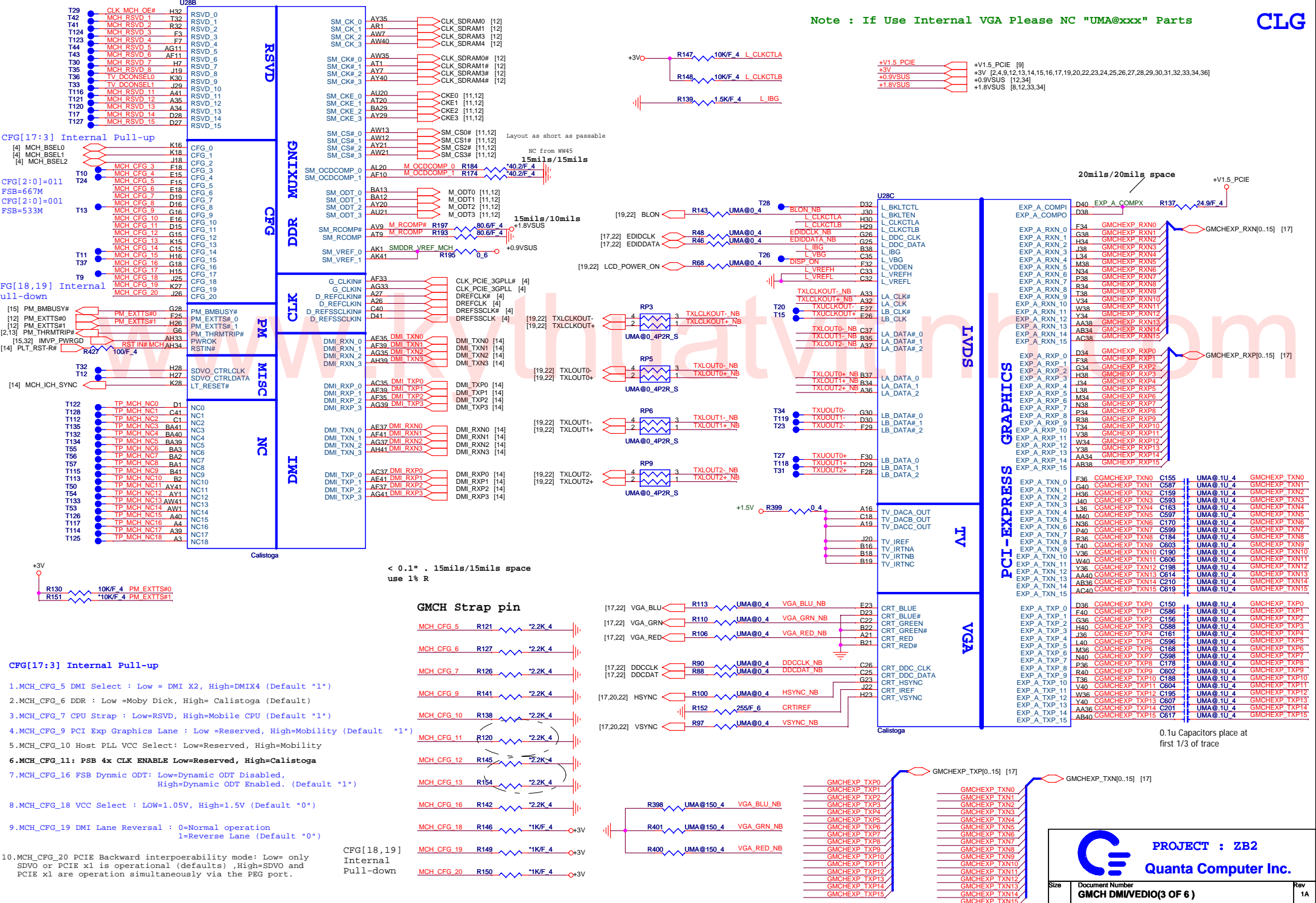
Calistoga



PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDR(2 OF 6)	1A
Date:	Monday, April 10, 2006	Sheet 6 of 37

Note : If Use Internal VGA Please NC "UMA@xxx" Parts



CFG[17:3] Internal Pull-up

CFG[2:0]=011 FSB=667M

CFG[2:0]=001 FSB=533M

CFG[18,19] Internal Pull-down

TP MCH NC0 D1

- TP MCH NC0 D1
- TP MCH NC1 C41
- TP MCH NC2 C1
- TP MCH NC3 BA41
- TP MCH NC4 BA40
- TP MCH NC5 BA39
- TP MCH NC6 BA3
- TP MCH NC7 BA2
- TP MCH NC8 BA1
- TP MCH NC9 A1
- TP MCH NC10 B2
- TP MCH NC11 AY41
- TP MCH NC12 AY1
- TP MCH NC13 AW41
- TP MCH NC14 AW1
- TP MCH NC15 A40
- TP MCH NC16 A4
- TP MCH NC17 A38
- TP MCH NC18 A3

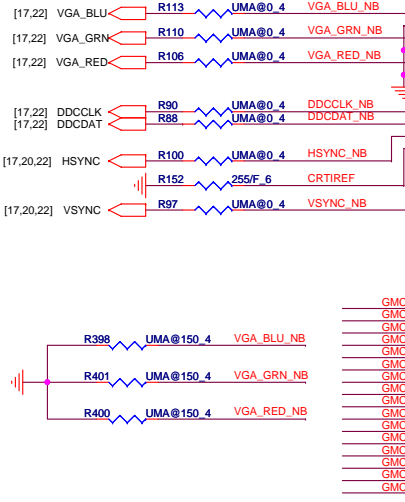
CFG[17:3] Internal Pull-up

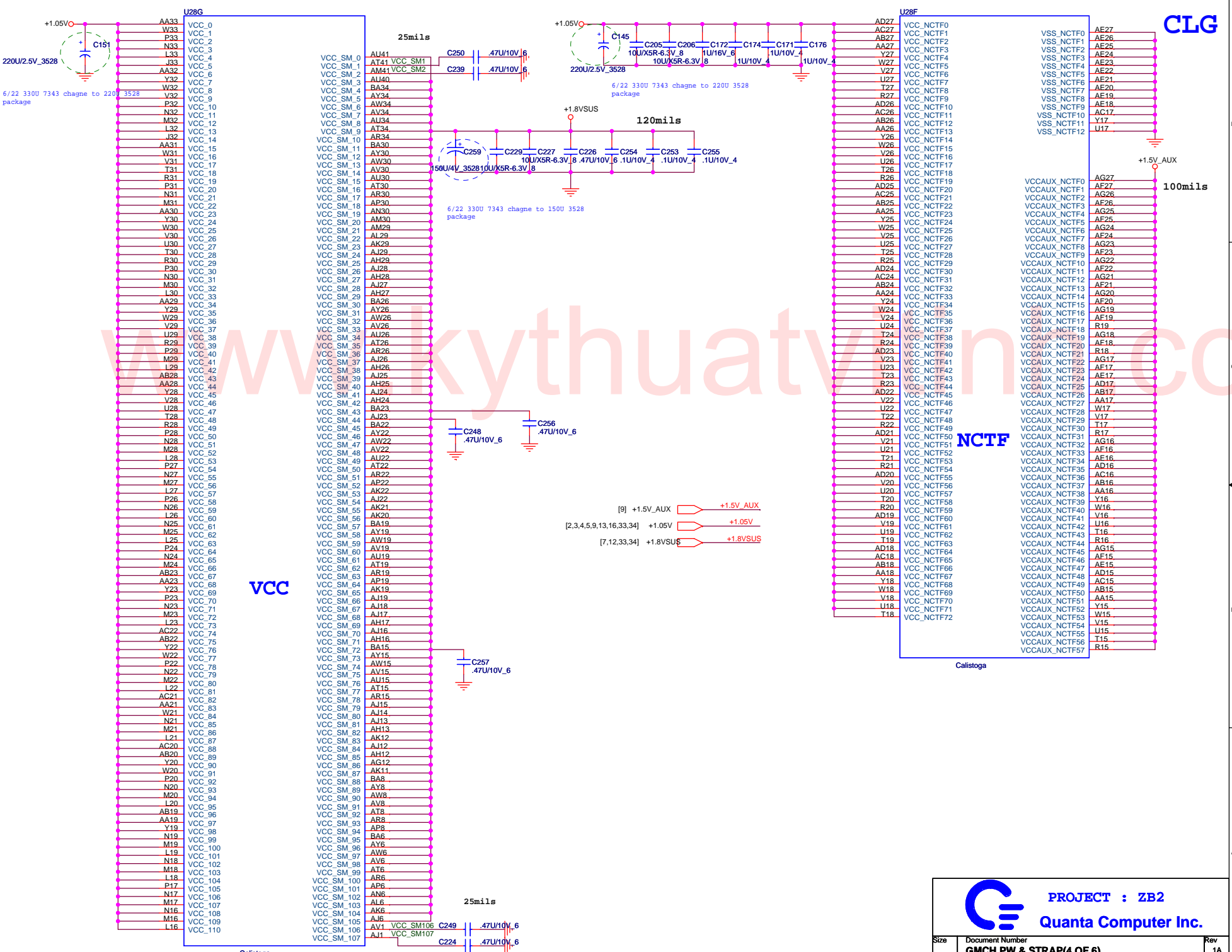
- MCH_CFG_5 DMI Select : Low = DMI X2, High=DMIX4 (Default "1")
- MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
- MCH_CFG_7 CPU Strap : Low=RSVD, High=Mobile CPU (Default "1")
- MCH_CFG_9 PCI Exp Graphics Lane : Low =Reserved, High=Mobility (Default "1")
- MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
- MCH_CFG_11: PSB 4x CLK ENABLE Low=Reserved, High=Calistoga
- MCH_CFG_16 FSB Dymnic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled. (Default "1")
- MCH_CFG_18 VCC Select : LOW=1.05V, High=1.5V (Default "0")
- MCH_CFG_19 DMI Lane Reversal : 0=Normal operation 1=Reverse Lane (Default "0")
- MCH_CFG_20 PCIe Backward interoperability mode: Low= only SDVO or PCIe x1 is operational (defaults), High=SDVO and PCIe x1 are operation simultaneously via the PEG port.

GMCH Strap pin

- MCH_CFG_5 R121 *2.2K 4
- MCH_CFG_6 R127 *2.2K 4
- MCH_CFG_7 R126 *2.2K 4
- MCH_CFG_9 R141 *2.2K 4
- MCH_CFG_10 R138 *2.2K 4
- MCH_CFG_11 R120 *2.2K 4
- MCH_CFG_12 R145 *2.2K 4
- MCH_CFG_13 R154 *2.2K 4
- MCH_CFG_16 R142 *2.2K 4
- MCH_CFG_18 R146 *1K/F 4 +3V
- MCH_CFG_19 R149 *1K/F 4 +3V
- MCH_CFG_20 R150 *1K/F 4 +3V

CFG[18,19] Internal Pull-down





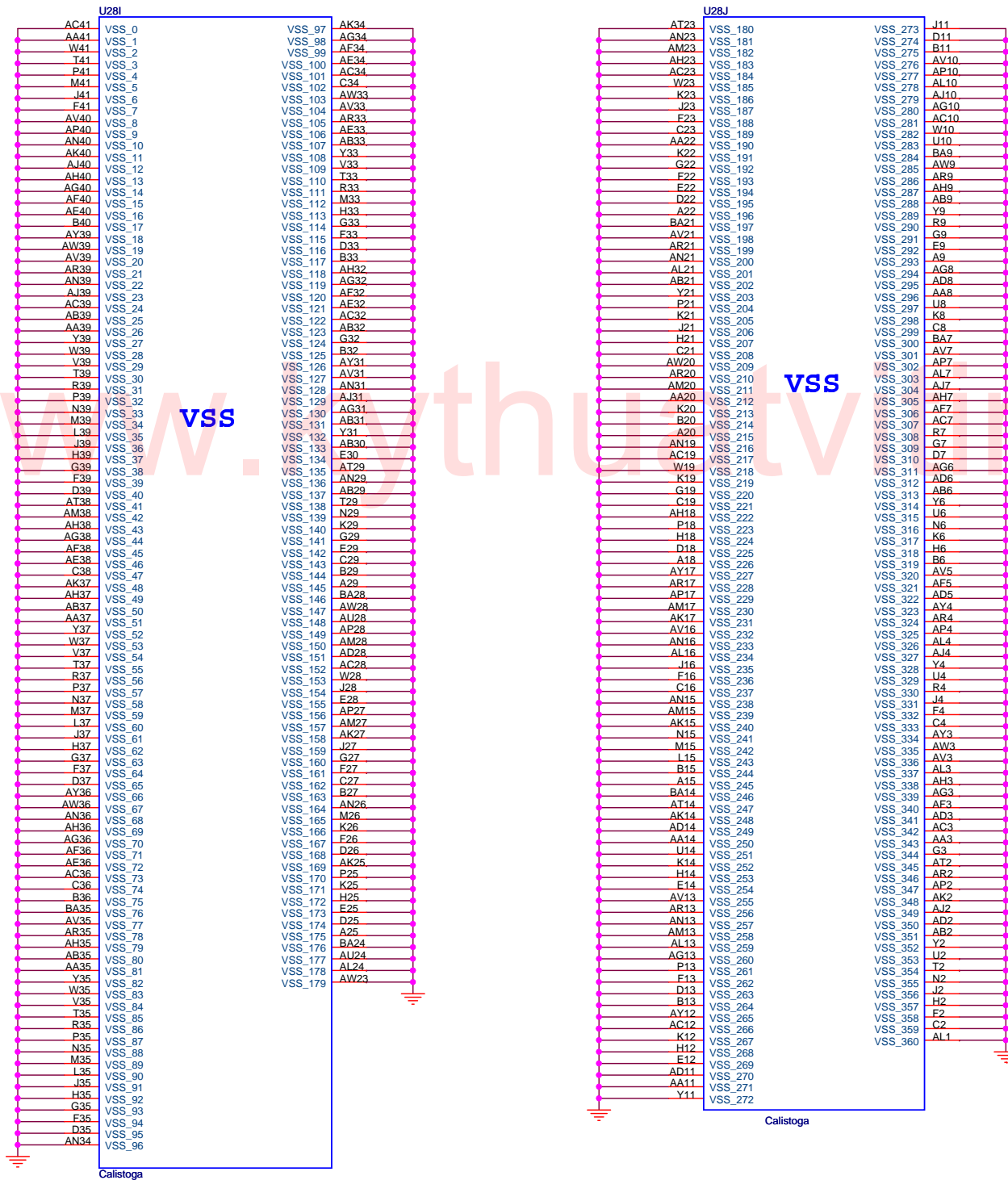
CLG

NCTF

Calistoga

PROJECT : ZB2
Quanta Computer Inc.

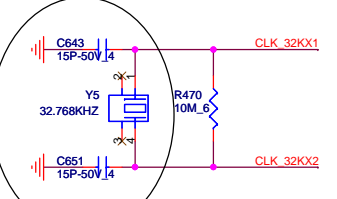
Size	Document Number	Rev
	GMCH PW & STRAP(4 OF 6)	1A
Date:	Monday, April 10, 2006	Sheet 8 of 37



PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH GND(6 OF 6)	1A
Date:	Monday, April 10, 2006	Sheet 10 of 37

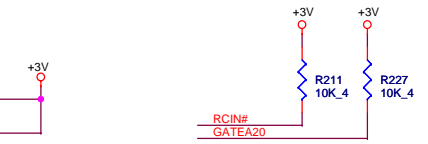
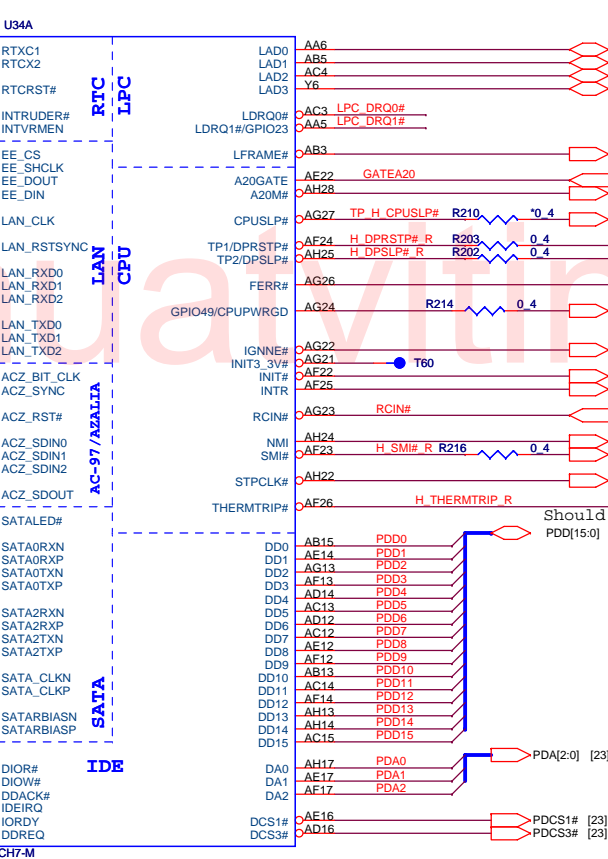
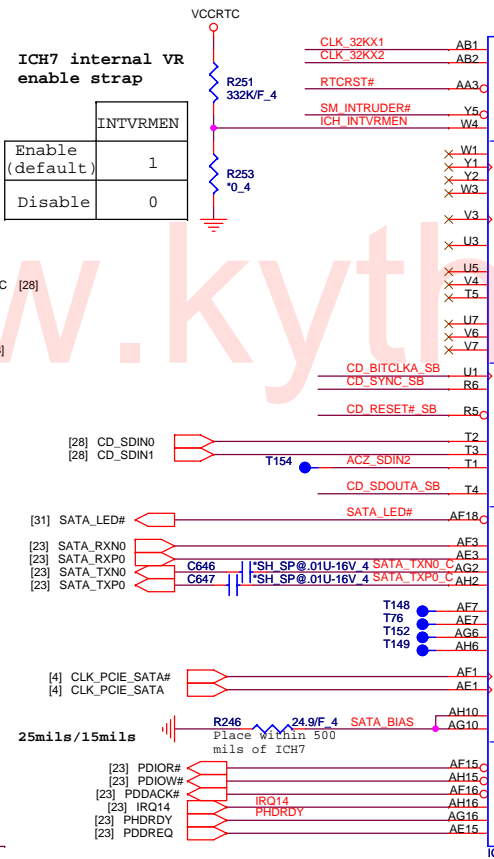
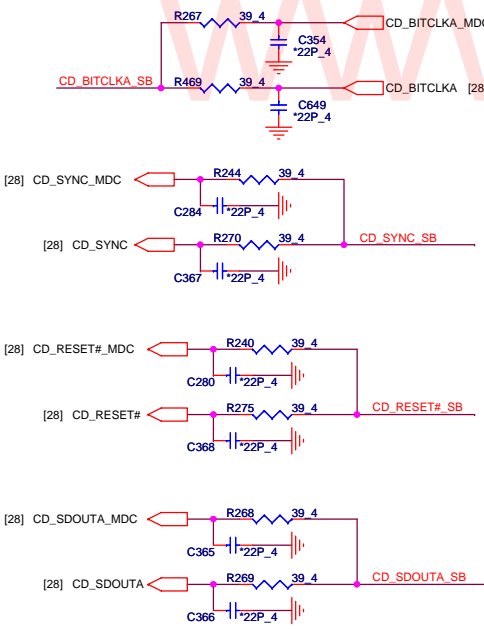
CLK:C1/C2: 18pF -> CL:12.5pF
 C1/C: 10pF -> CL Value = 8.5pF



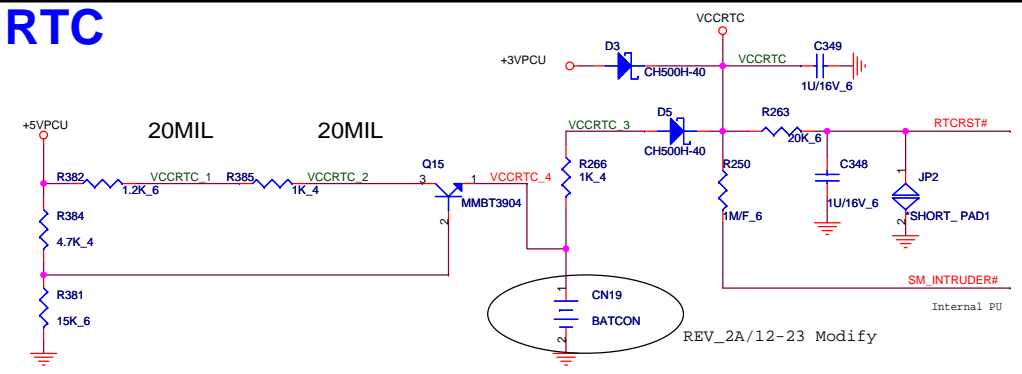
ICH7 internal VR enable strap

INTVRMEN	
Enable (default)	1
Disable	0

REV_3B/03-14 Modify

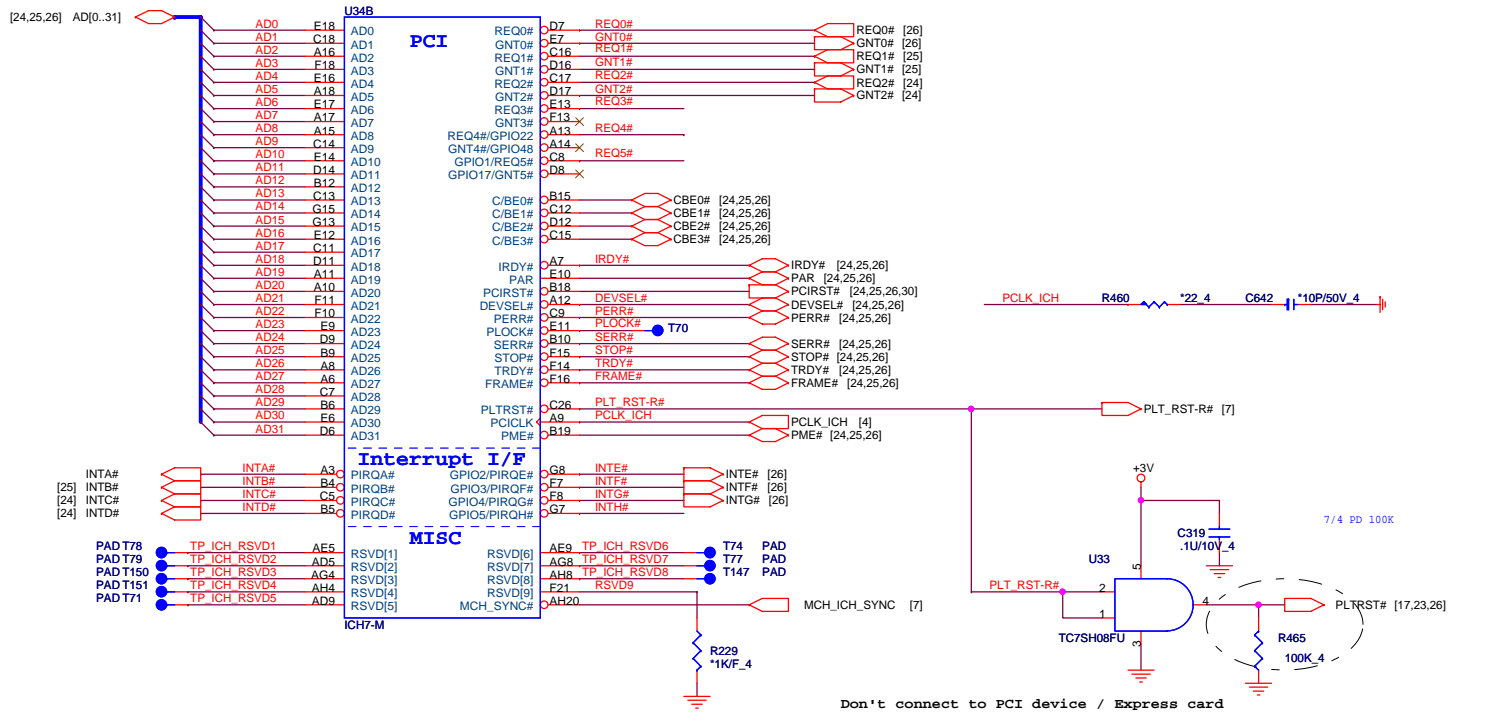
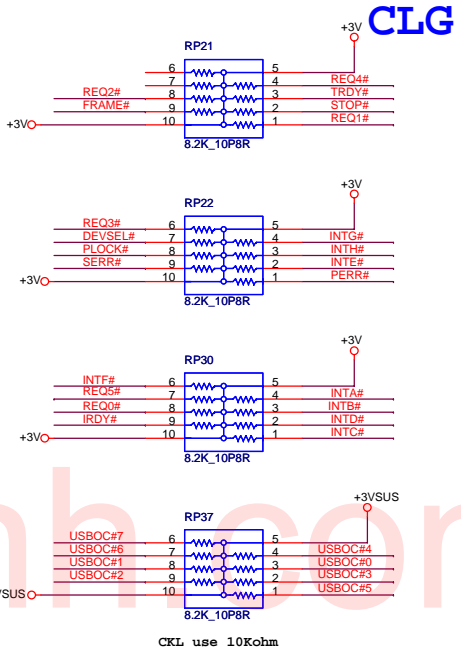
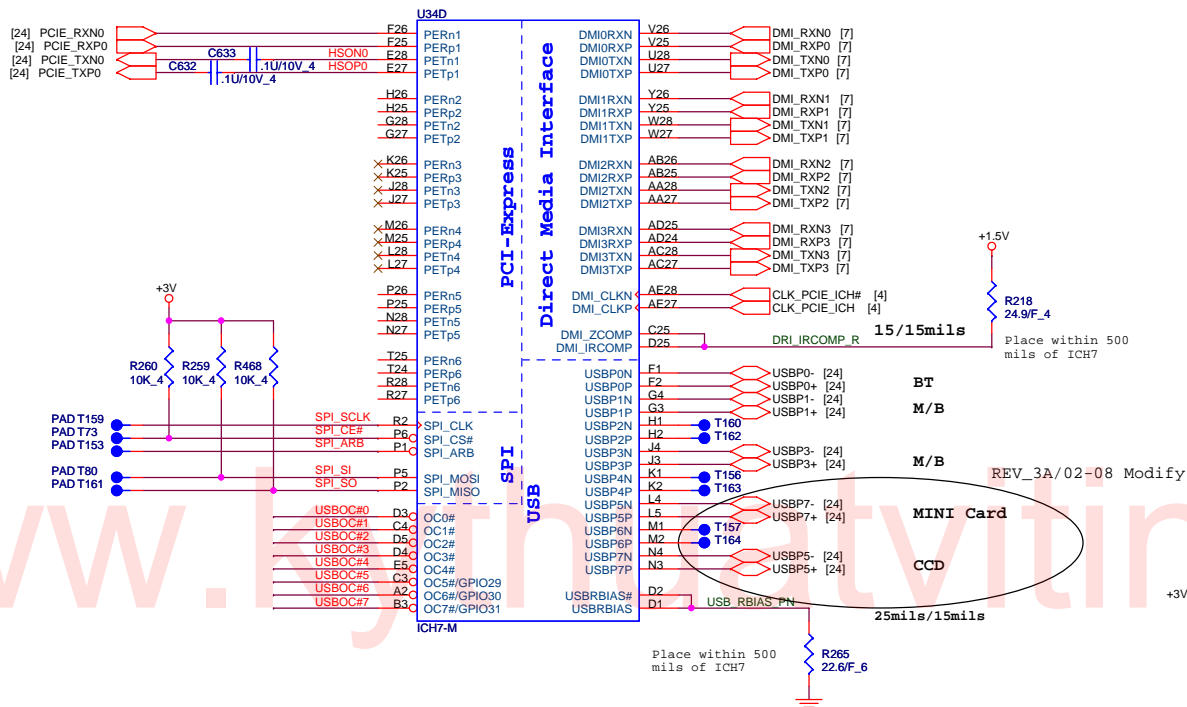


RTC



PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M HOST (1 OF 4)	3B
Date:	Monday, April 10, 2006	Sheet 13 of 37



ICH7 Boot BIOS select

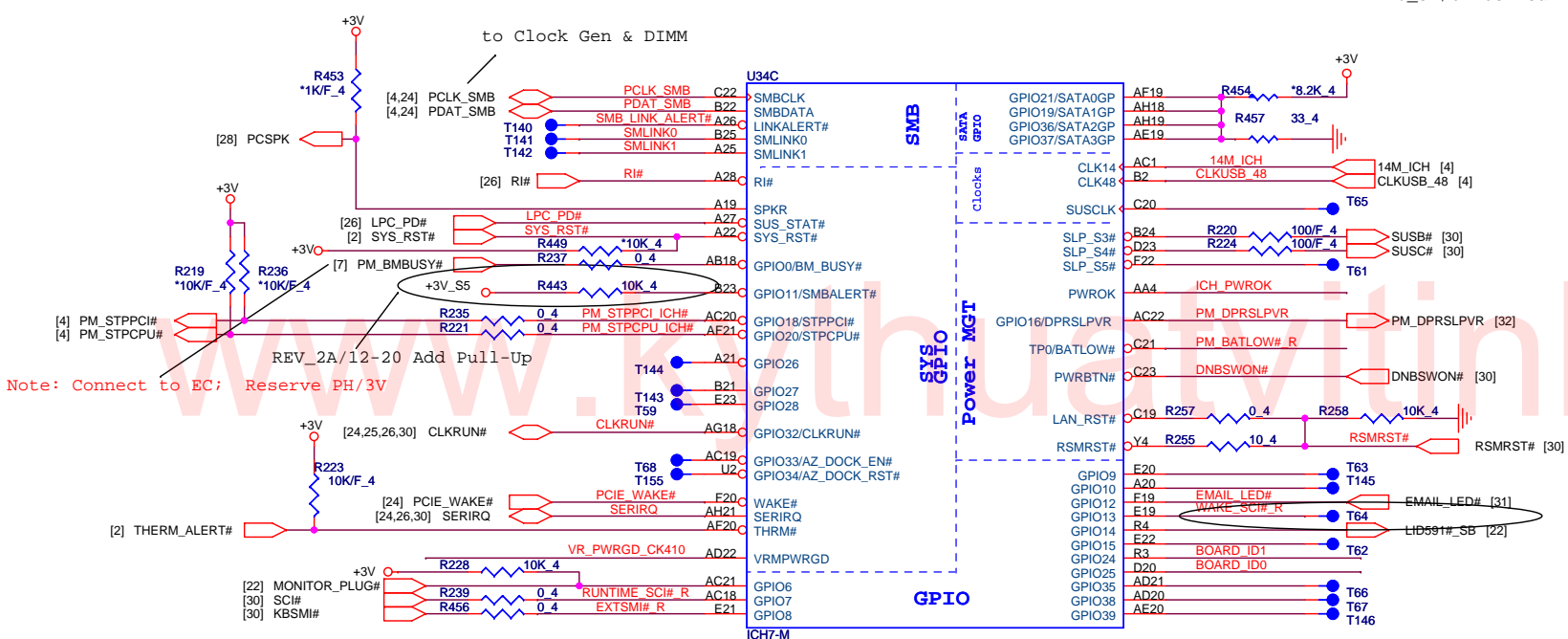
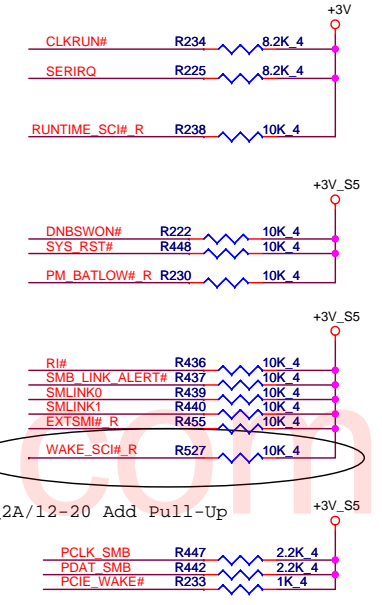
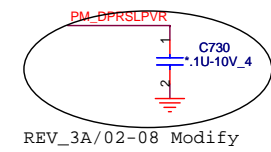
	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCCARD	AD25	REQ0# / GNT0#	INT E/F/G#
MINIPCI	AD19	REQ2# / GNT2#	INT C/D#
LAN	AD16	REQ1# / GNT1#	INT B#

PROJECT : ZB2
Quanta Computer Inc.

Size: Document Number
ICH7-M PCI E (2 OF 4) Rev: 3A

Date: Monday, April 10, 2006 Sheet: 14 of 37

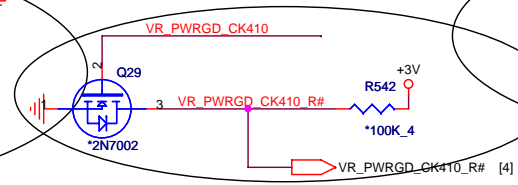


Note: Connect to EC; Reserve PH/3V

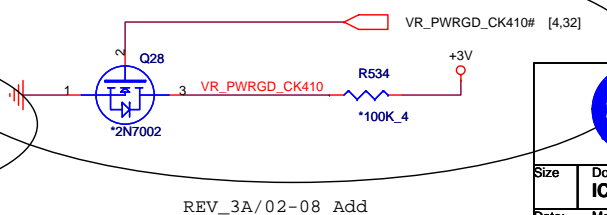
REV_3C/03-29 Modify

Board ID	CardReader	CCD
ID0 , ID1 00	X	X
ID0 , ID1 01	X	V
ID0 , ID1 10	V	X
ID0 , ID1 11	V	V

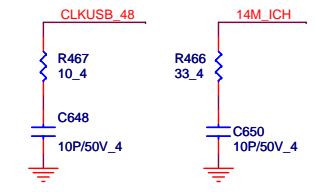
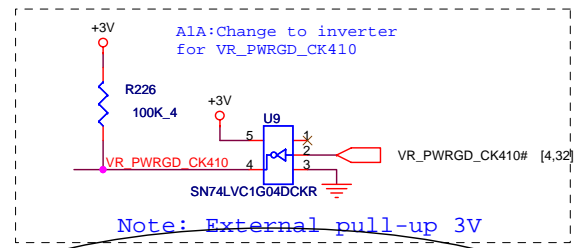
REV_3A/02-09 Add



REV_3A/02-08 Add



GPIO25 /suspend rail is a HW strap , don't pull down .



PROJECT : ZB2
Quanta Computer Inc.

Size Document Number Rev
ICH7-M GPIO (3 OF 4) 3C

Date: Monday, April 10, 2006 Sheet 15 of 37

NOTE: some of the PCIE testpoints will be available through via on traces.

Note : If Use Internal VGA Please NC "EV@xxxx" Parts

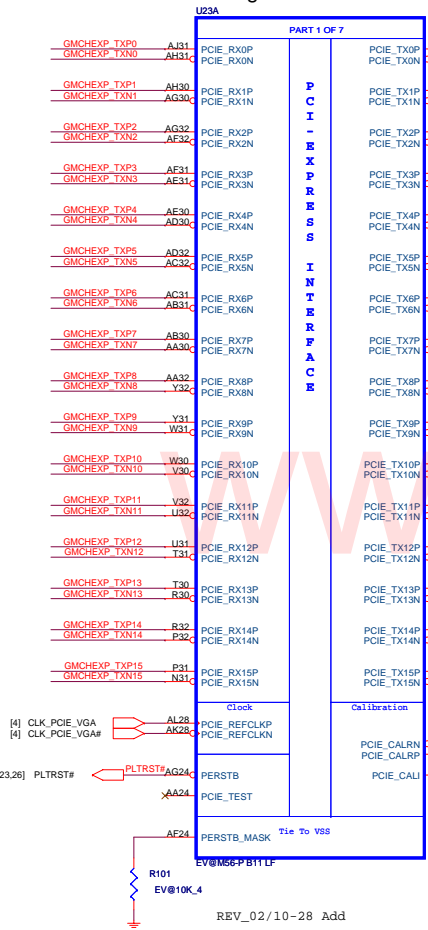
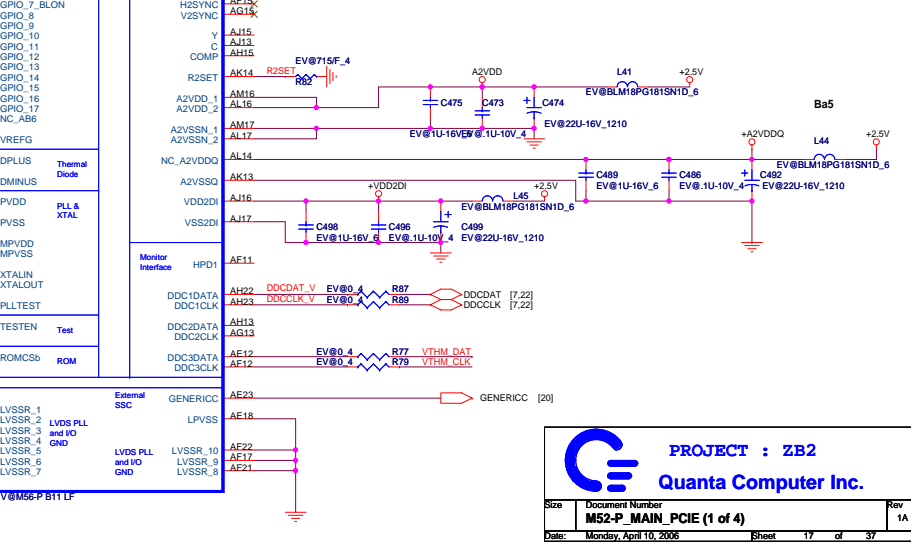
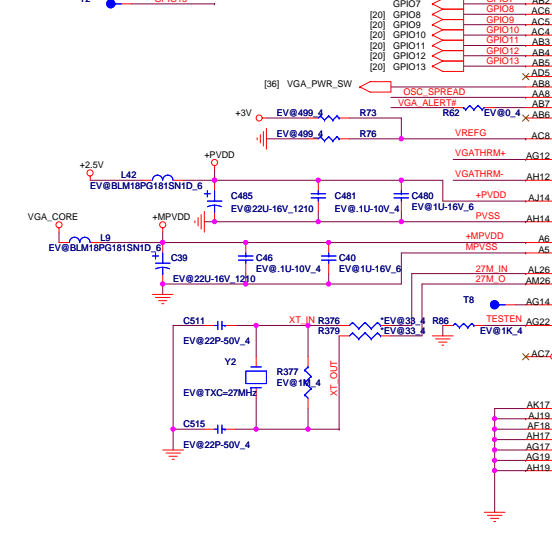
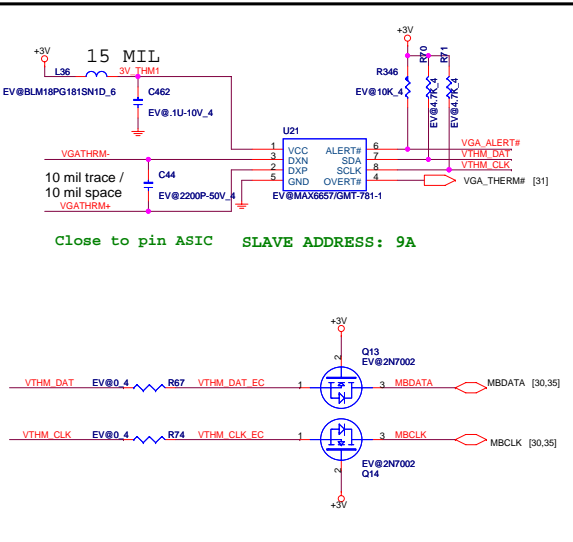
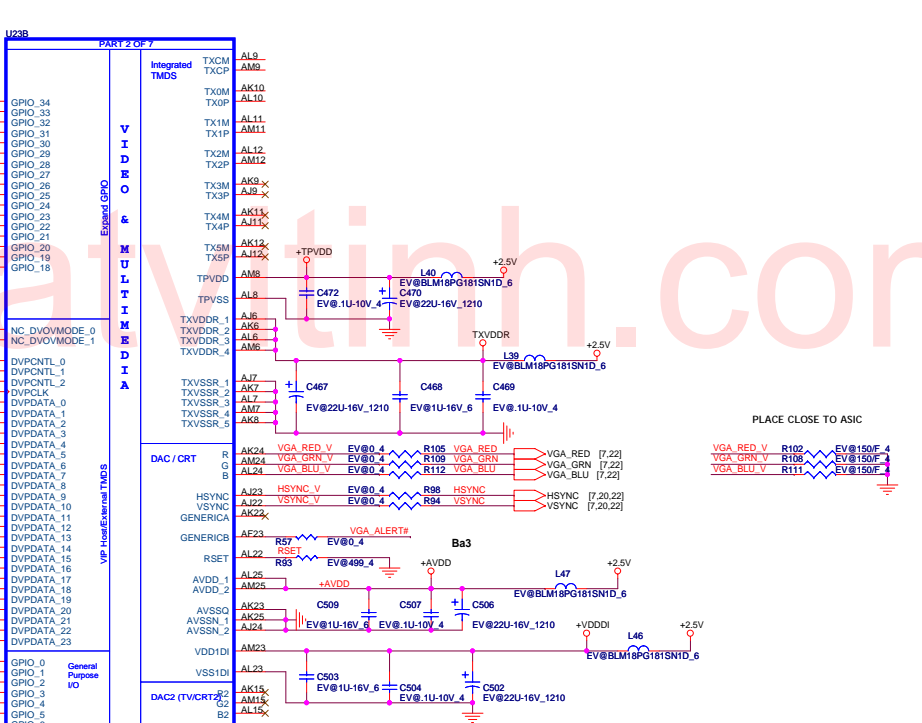
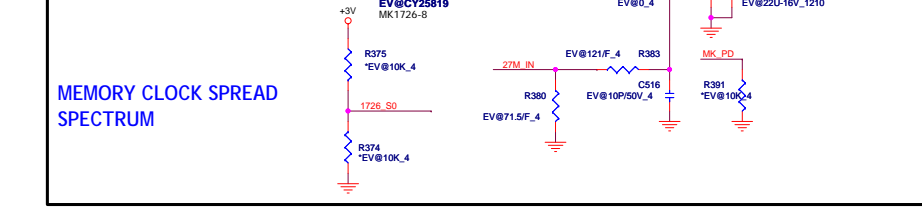


Table listing testpoints (e.g., AK27, AH25, AG27) and their corresponding GMCEXP pins (TXP0-RXN0, TXP1-RXN1, etc.) and voltage levels (EV@1U-10V_4).



RV410 MEMORY CHANNELS A and B

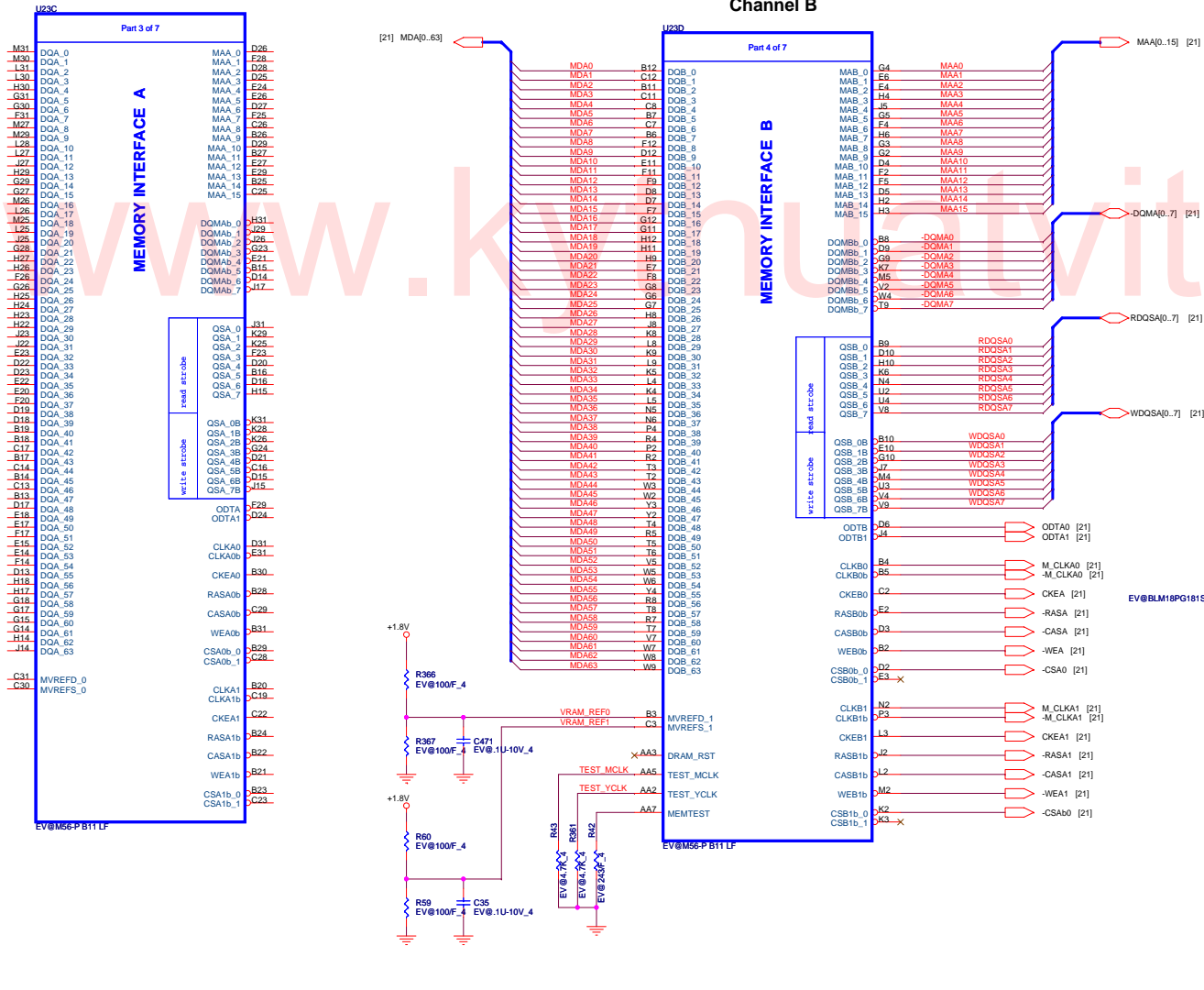
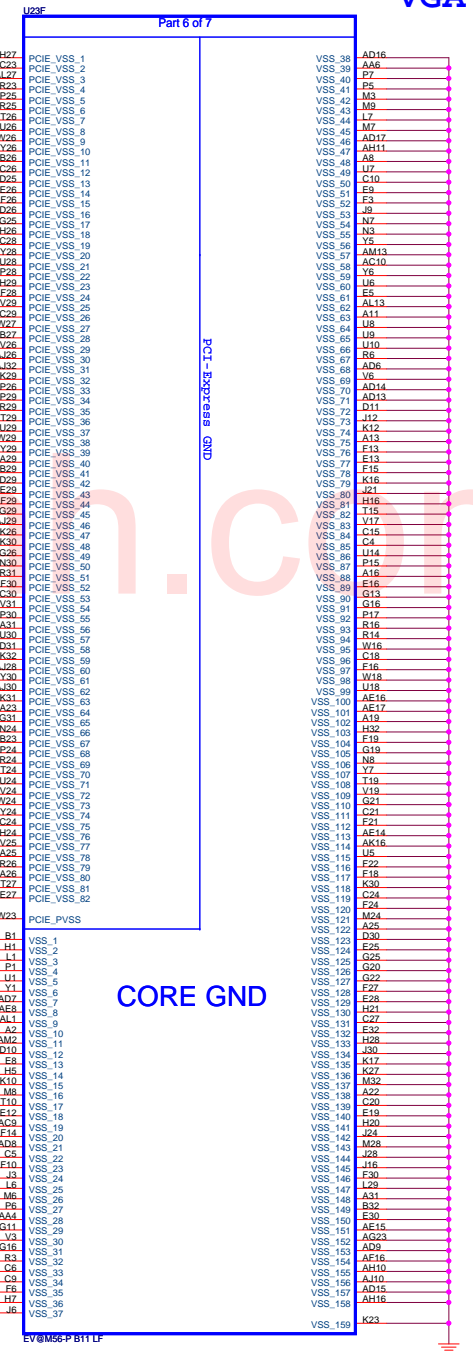
VGA

FOR M52P, M54P, M26X,
PIN B25 IS MA12 (BA0)
PIN C25 IS MA13 (BA1)
PIN E29 IS MA15 (BA2)
PIN E27 IS MA14
M50P IS THE SAME EXCEPT
PIN E29 IS CSBb_1
FOR M56P
PIN B25 IS MA14 (BA0)
PIN C25 IS MA15 (BA1)
PIN E29 IS MA13 (BA2)
PIN E27 IS MA12

FOR M52P, M54P, M26X, M50P
PIN H2 IS MAB12 (BA0)
PIN H3 IS MAB13 (BA1)
PIN F5 IS MAB15 (BA2)
PIN D5 IS MAB14
M50P IS THE SAME EXCEPT
PIN D5 IS CSBb_1
FOR M56P
PIN H2 IS MA14 (BA0)
PIN H3 IS MA15 (BA1)
PIN D5 IS MA13 (BA2)
PIN F5 IS MAB1

Channel A

Channel B



CORE GND

PROJECT : ZB2
Quanta Computer Inc.

PART 5 OF 7

C1	VDDR1_1
J1	VDDR1_2
R1	VDDR1_3
M1	VDDR1_4
V1	VDDR1_5
A1	VDDR1_6
A3	VDDR1_7
P9	VDDR1_8
J10	VDDR1_9
N9	VDDR1_10
P10	VDDR1_11
A9	VDDR1_12
Y10	VDDR1_13
F8	VDDR1_14
G9	VDDR1_15
Y9	VDDR1_16
J11	VDDR1_17
A21	VDDR1_18
M10	VDDR1_20
N10	VDDR1_21
Y8	VDDR1_22
J18	VDDR1_23
K21	VDDR1_24
VDDR1_25	VDDR1_25
A12	VDDR1_26
H12	VDDR1_27
A15	VDDR1_28
J20	VDDR1_29
J12	VDDR1_30
K11	VDDR1_31
K19	VDDR1_32
A18	VDDR1_33
L23	VDDR1_34
K20	VDDR1_35
VDDR1_36	VDDR1_36
K24	VDDR1_37
L24	VDDR1_38
H19	VDDR1_39
A24	VDDR1_40
K13	VDDR1_41
J32	VDDR1_42
A30	VDDR1_43
C32	VDDR1_44
F32	VDDR1_45
L32	VDDR1_46

POWER

I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

Memory / I/O

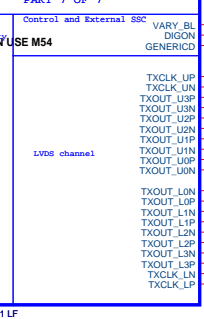
Memory / I/O

Memory / I/O

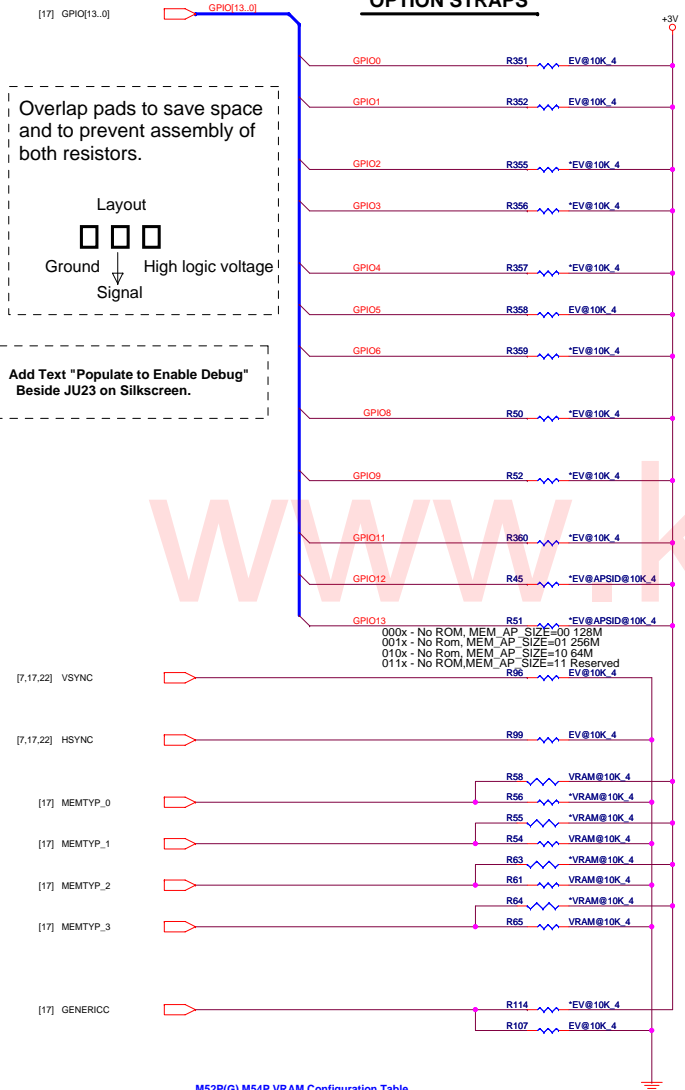
Memory / I/O

PART 7 OF 7

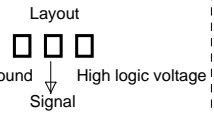
Forward	Control and External SSC	VARY BL DIGON GENERIC
AD12	B_LON_VGA	EV@0_4P2R_S_3
AE11	LCD_POWER_ON_VGA	EV@0_4P2R_S_1
AD23		
AJ21	TXCLK_UP	EV@0_4P2R_S_1
AK21	TXCLK_LN	EV@0_4P2R_S_1
AH21	TXOUT_U3P	EV@0_4P2R_S_1
AG21	TXOUT_U3N	EV@0_4P2R_S_1
AG20	TXOUT_U2P	EV@0_4P2R_S_1
AJ20	TXOUT_U2N	EV@0_4P2R_S_1
AK20	TXOUT_U1P	EV@0_4P2R_S_1
AJ20	TXOUT_U1N	EV@0_4P2R_S_1
AG18	TXOUT_U0P	EV@0_4P2R_S_1
AH18	TXOUT_U0N	EV@0_4P2R_S_1
AK19	TXOUT_L0N	EV@0_4P2R_S_1
AL19	TXOUT_L0P	EV@0_4P2R_S_1
AL20	TXOUT_L1N	EV@0_4P2R_S_1
AM20	TXOUT_L1P	EV@0_4P2R_S_1
AL21	TXOUT_L2N	EV@0_4P2R_S_1
AM21	TXOUT_L2P	EV@0_4P2R_S_1
AK18	TXOUT_L3N	EV@0_4P2R_S_1
AJ18	TXOUT_L3P	EV@0_4P2R_S_1
AL18	TXCLK_LN	EV@0_4P2R_S_1
AM18	TXCLK_LP	EV@0_4P2R_S_1



OPTION STRAPS



Overlap pads to save space and to prevent assembly of both resistors.



Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.

000x - No ROM, MEM_AP_SIZE=00 128M
001x - No Rom, MEM_AP_SIZE=01 256M
010x - No Rom, MEM_AP_SIZE=10 64M
011x - No ROM, MEM_AP_SIZE=11 Reserved
R51 *EV@APSID@10K_4

M56-P Strap

STRAPS	PIN	DESCRIPTION	Board DEFAULT
TX_PWRS_ENB	GPIO0 (Internal pull-down)	Transmitter Power Saving Enable 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1 (Internal pull-down)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
	GPIO(3:2) (Internal pull-down)	RSVD	
DEBUG_ACCESS	GPIO4 (Internal pull-down)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5 (Internal pull-down)	RSVD	
	GPIO6 (Internal pull-down)	RSVD	
Force_Comppliance	GPIO8 (Internal pull-down)	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13,12,11) (Internal pull-down)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128M 001x - No Rom, MEM_AP_SIZE=01 256M 010x - No Rom, MEM_AP_SIZE=10 64M 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	000
VIP_DEVICE	VSYN	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port devices present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYN, V2SYN, SENSER1CC	RSVD	
	VSYN	RSVD	
	HSYN	RSVD	
	PCIE_TEST	RSVD	

Memory Aperture Size Select
When no ROM is attached, GPIO_9 is set to 0
GPIO_[13:12] is used to select the memory aperture size.
GPIO_[13:12] = 00: 128M memory aperture, same as ROM strap 00
GPIO_[13:12] = 01: 256M memory aperture, same as ROM strap 01
GPIO_[13:12] = 10: 64M memory aperture, same as ROM strap 10
GPIO_[13:12] = 11: reserved, same as ROM strap 11

Default: 128M memory aperture.
GPIO_[13:12] = 01 (256M memory aperture) recommended for designs with 256MB or 512MB of physical memory.

M52P(G) M54P VRAM Configuration Table

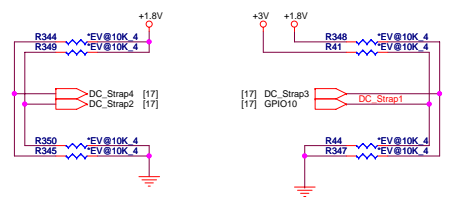
MEMTYP [3:0]	DESCRIPTION	Size
0000	DDR2, 16Mx16, 2pcs	64M
0001	DDR2, 16Mx16, 4pcs	128M
0010	DDR2, 32Mx16, 2pcs	128M
0011	DDR2, 32Mx16, 4pcs	256M
others	Reserved	

Default

Board Straps

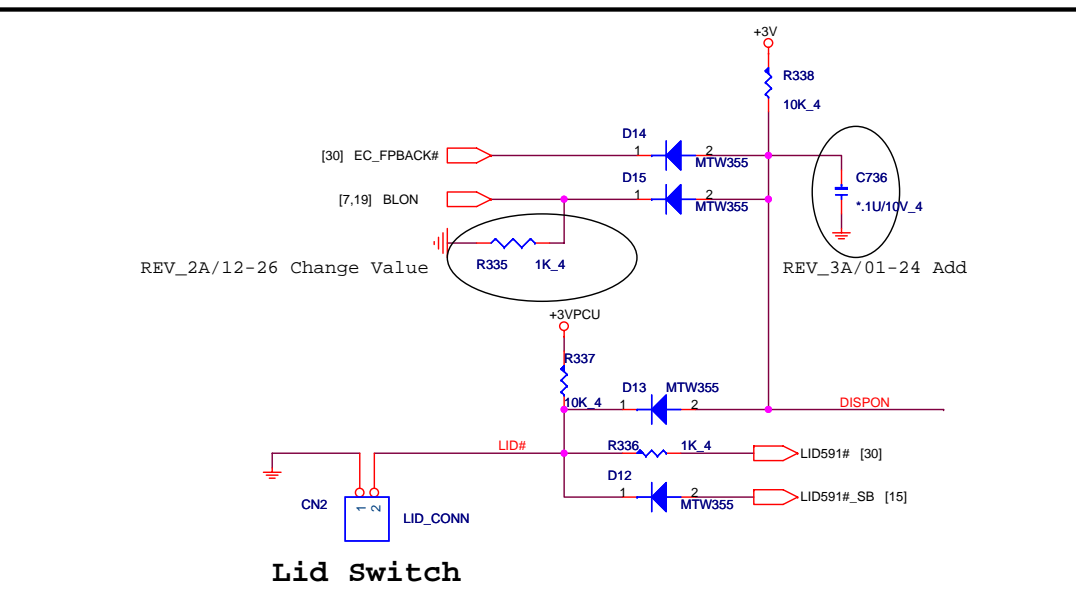
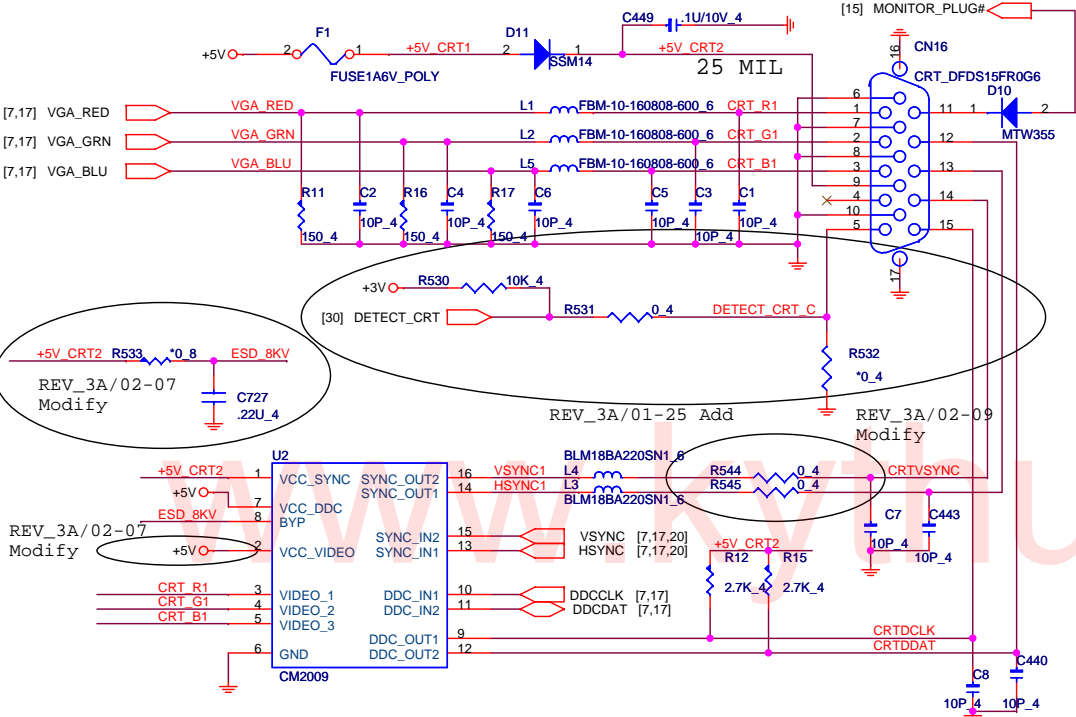
REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO25,26	Memory identification for BIOS 00 - DDR2 16X16X4pcs 128MB 01 - DDR2 32X16X4pcs 256MB 10 - DDR2 16X16X2pcs 64MB 11 - DDR2 32X16X2pcs 128MB	
DC_Strap1	GPIO(10)	Internal TMD5 Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Not detected	0
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected 1 - Enabled	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PALNTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1



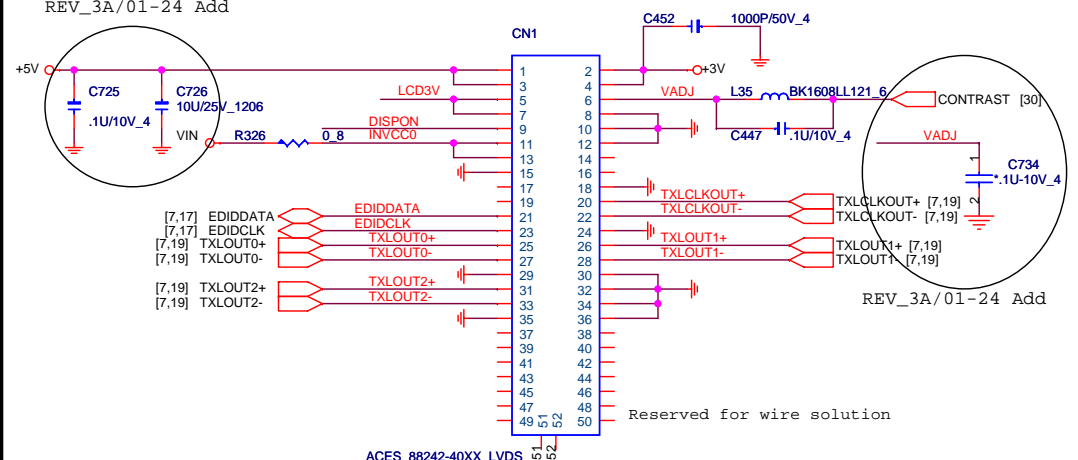
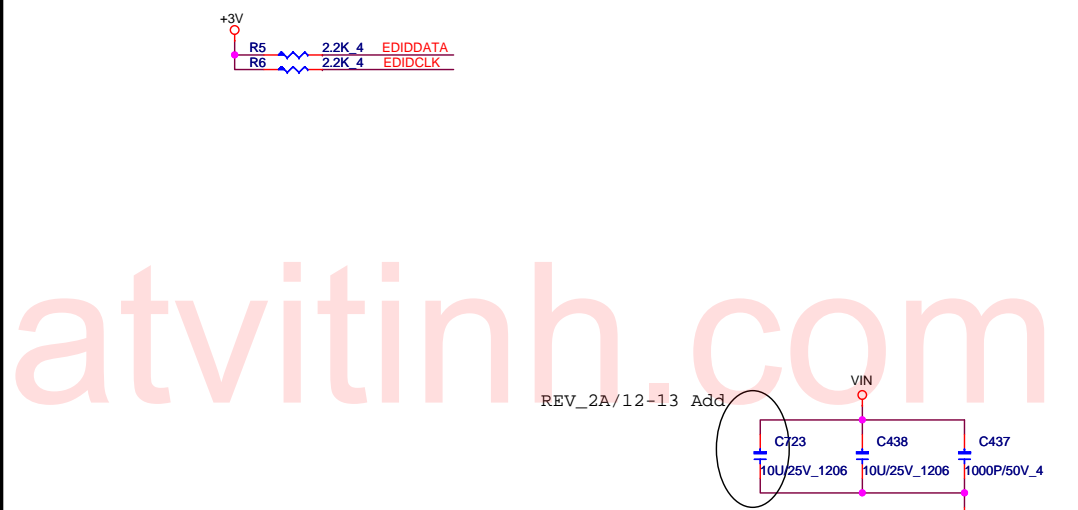
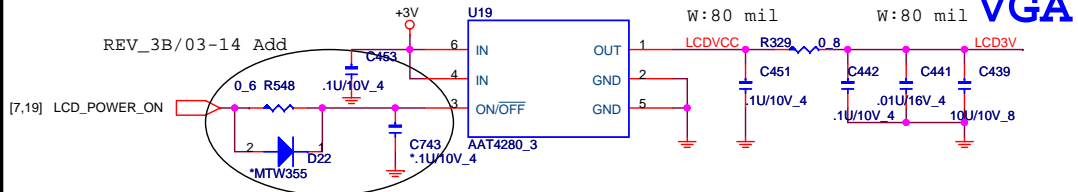
PROJECT : ZB2
Quanta Computer Inc.


CRT PORT



Lid Switch

VGA





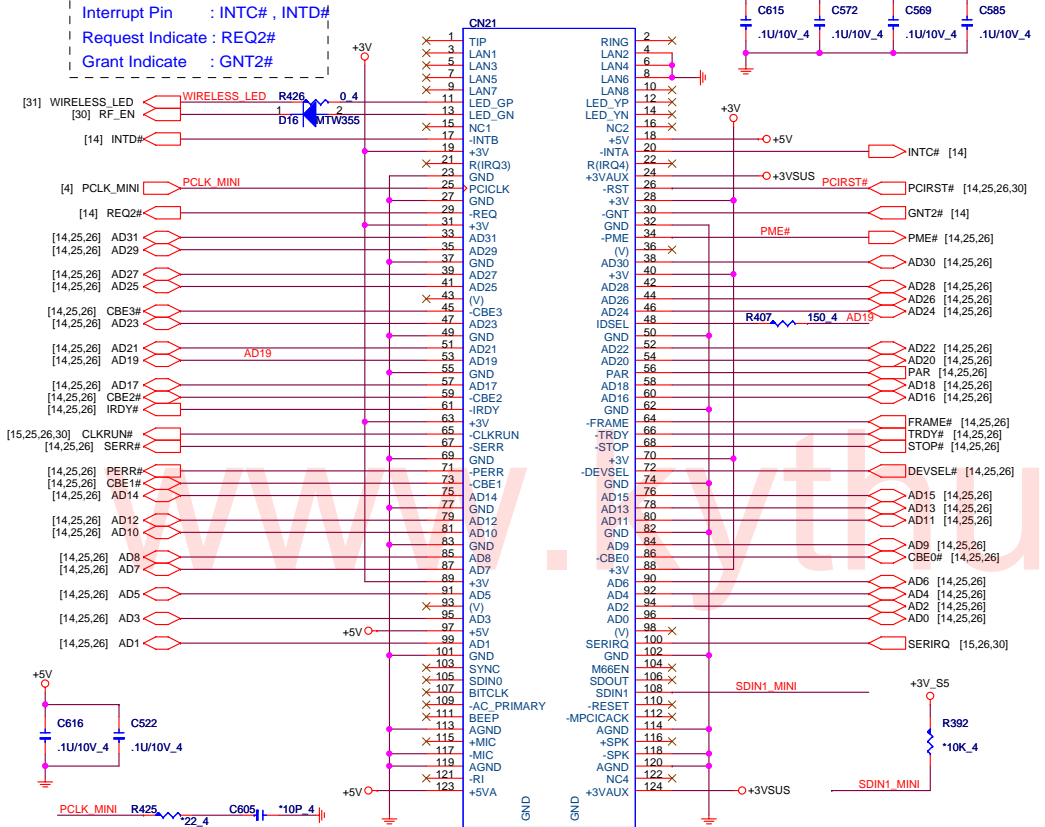
PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	LVDS,VGA Ports, LID	3B
Date:	Monday, April 10, 2006	Sheet 22 of 37

ID Select : AD19
 Interrupt Pin : INTC# , INTD#
 Request Indicate : REQ2#
 Grant Indicate : GNT2#

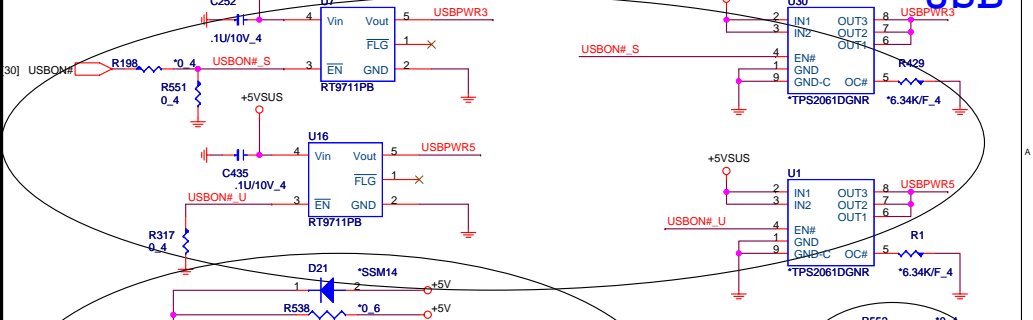
MINI-PCI

MPC



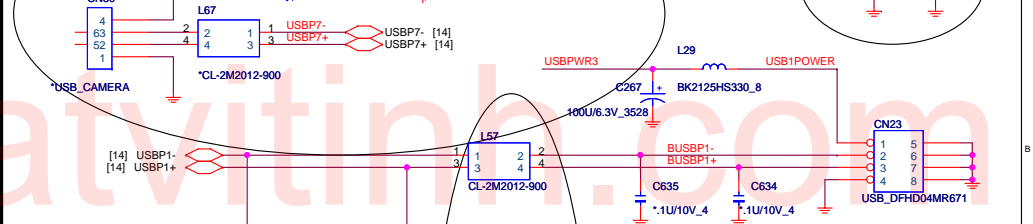
REV_3C/03-27 Modify

USB



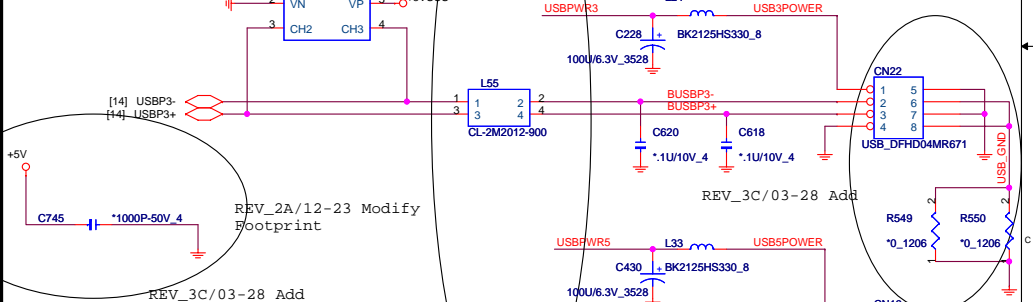
REV_3A/02-08 Add

REV_3C/03-28 Add



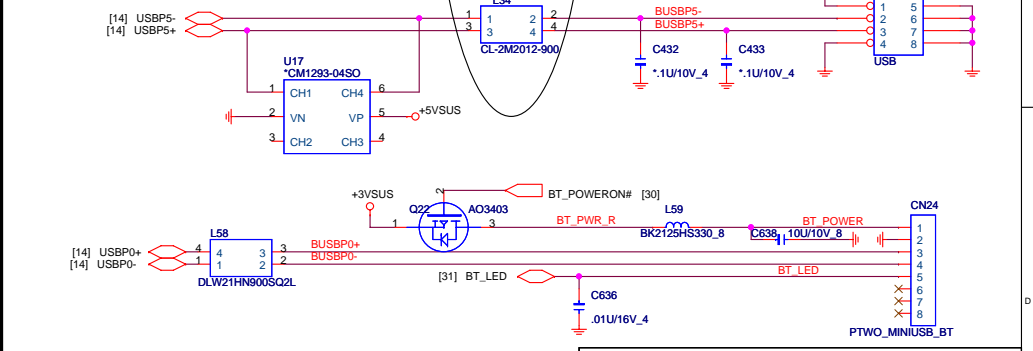
REV_03/11-04 Modify C type

REV_3C/03-27 For ESD

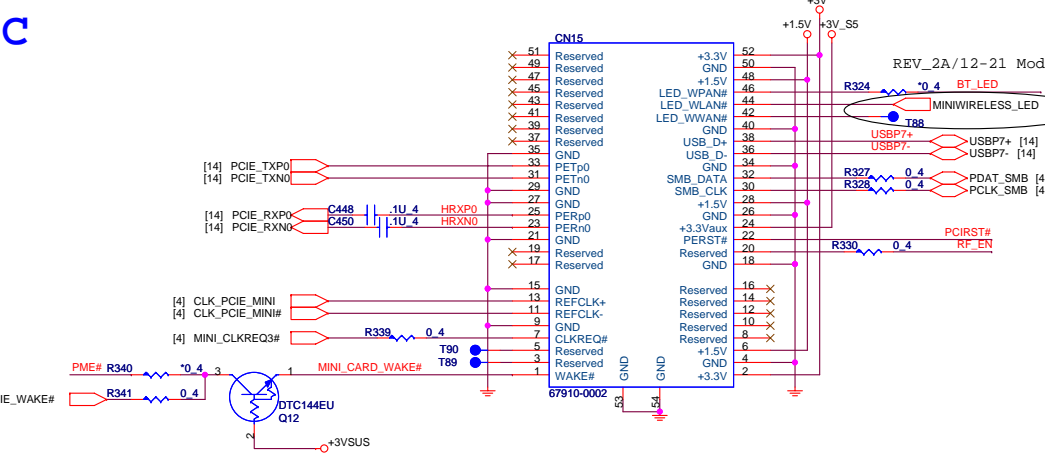


REV_2A/12-23 Modify Footprint

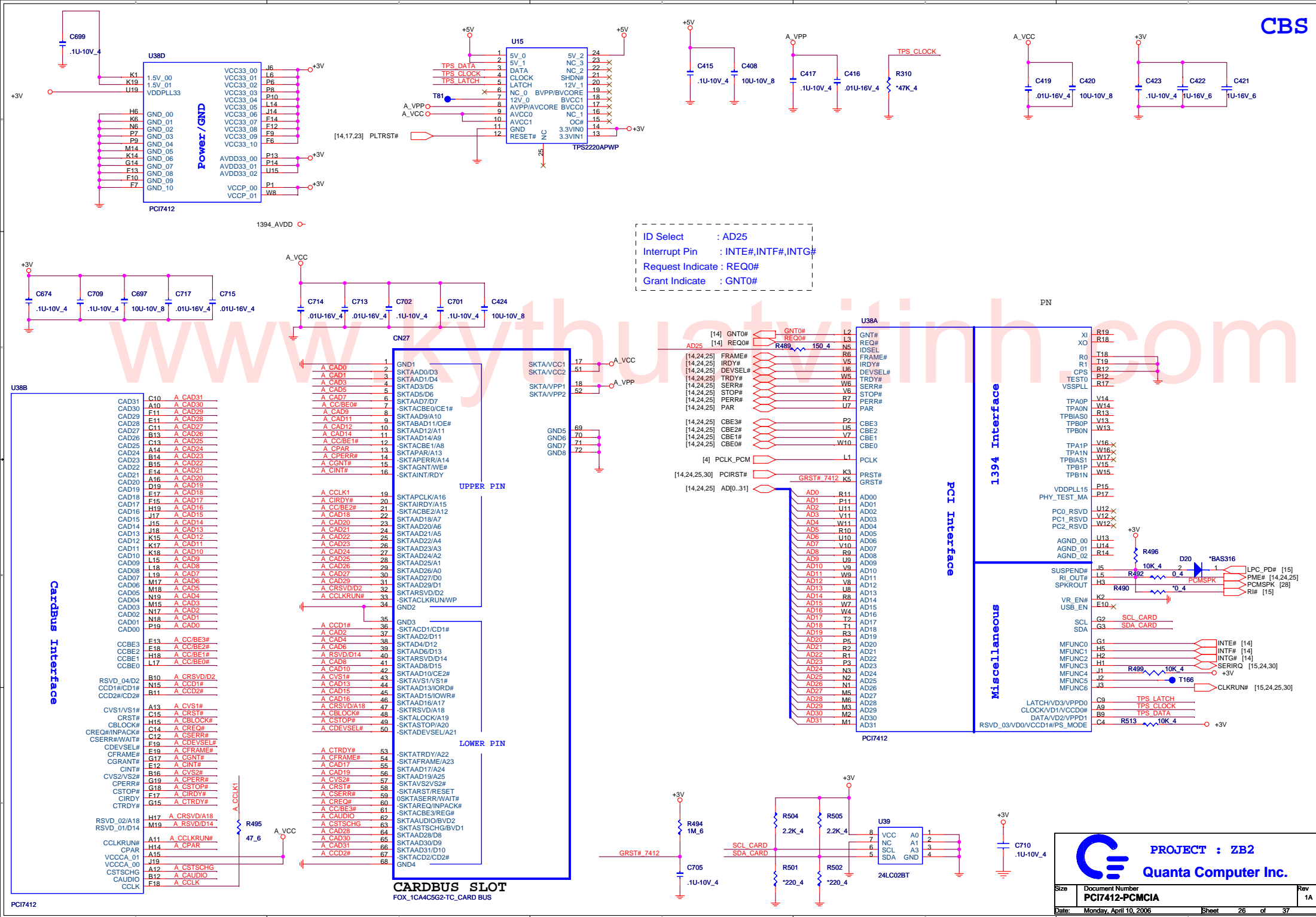
REV_3C/03-28 Add



MPC



PROJECT : ZB2
Quanta Computer Inc.
 Size Document Number
MINI PCI,USB
 Date: Monday, April 10, 2006 Sheet 24 of 37



ID Select : AD25
 Interrupt Pin : INTE#,INTF#,INTG#
 Request Indicate : REQ0#
 Grant Indicate : GNT0#

1394 Interface

PCI Interface

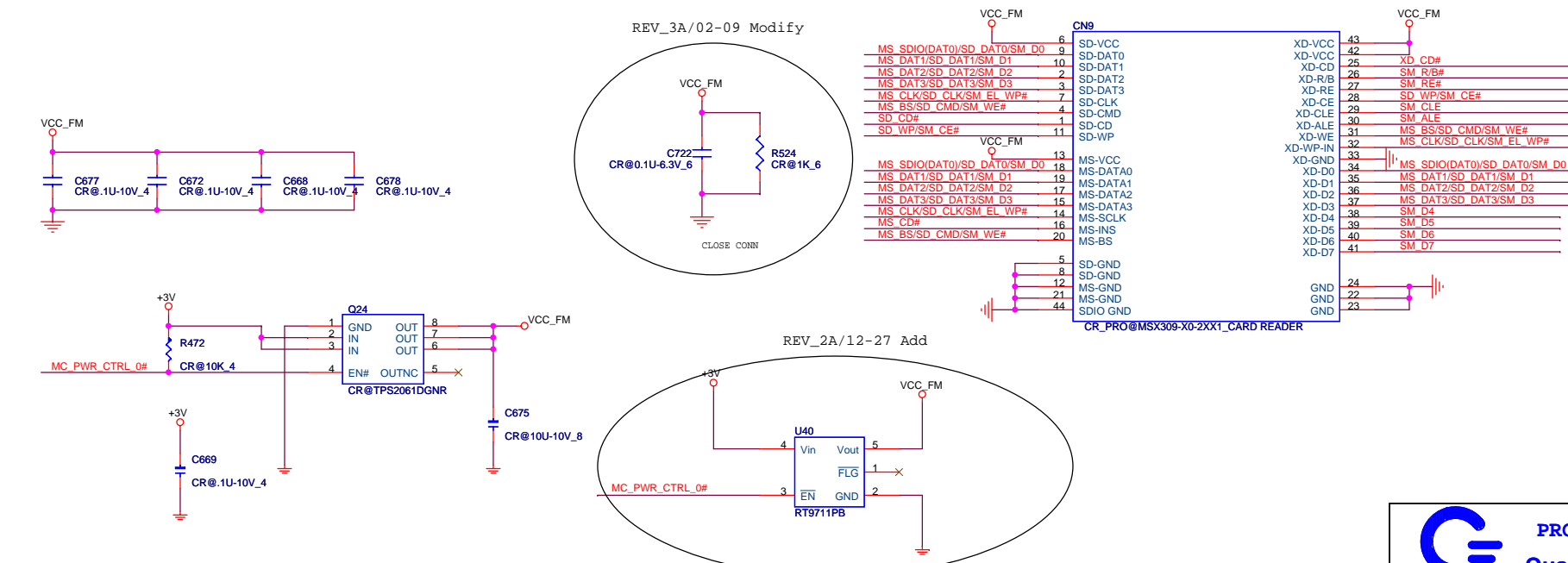
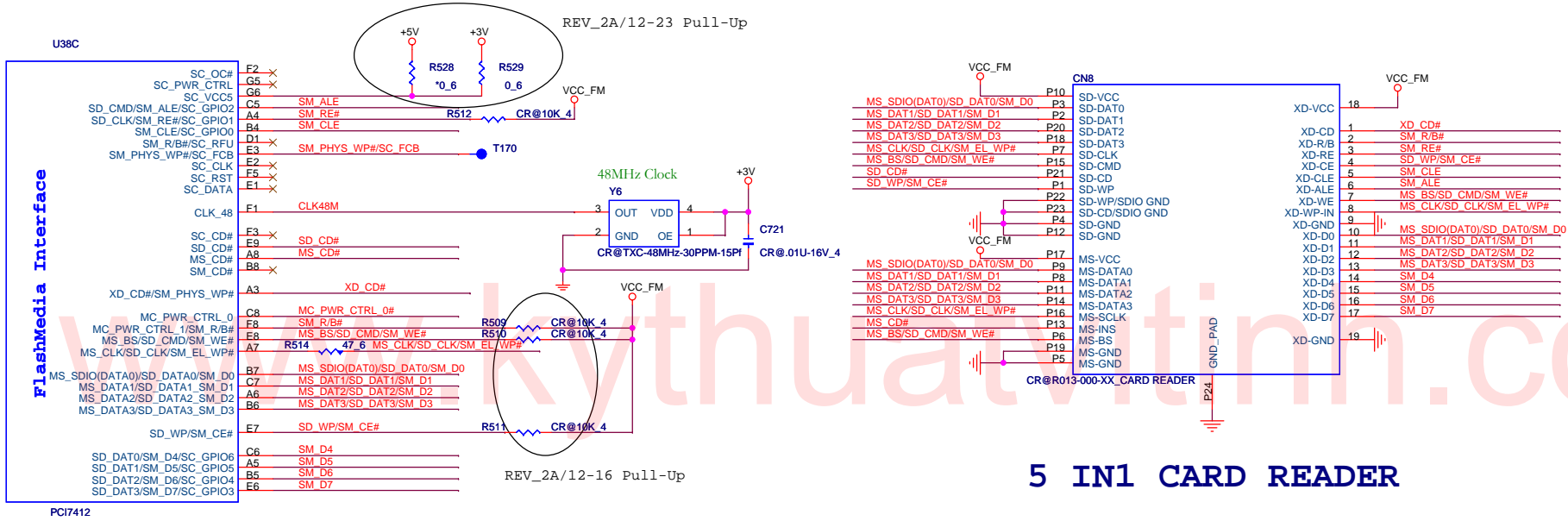
Miscellaneous

CARDBUS SLOT
 FOX_1C4C5G2-TC_CARD BUS

PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412-PCMCIA	1A
Date:	Monday, April 10, 2006	Sheet 26 of 37

DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

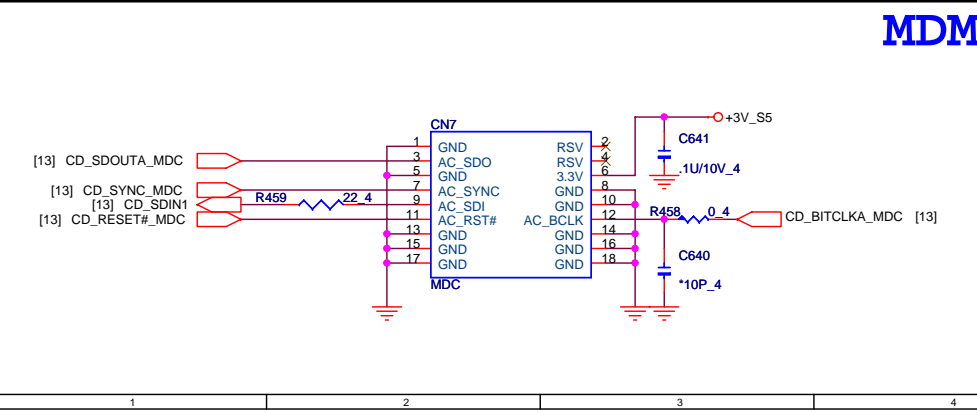
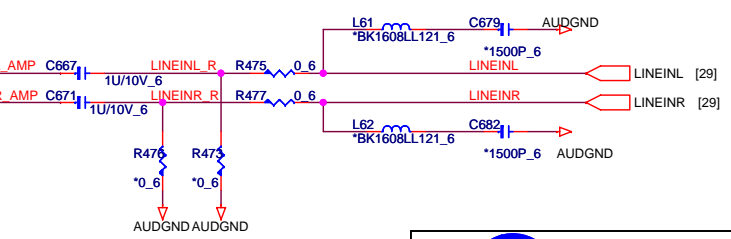
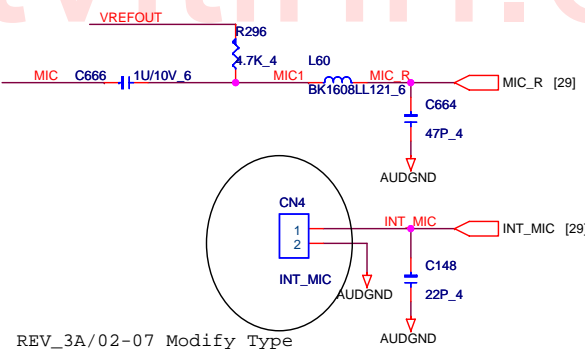
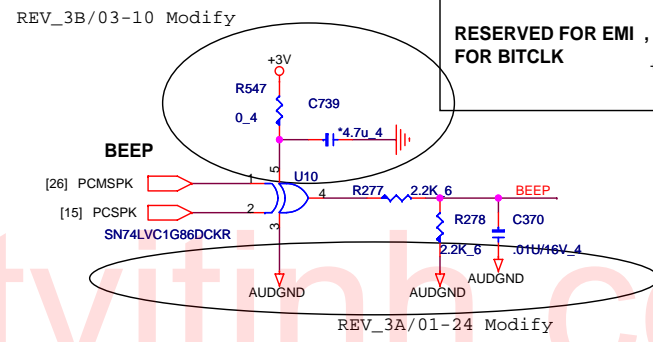
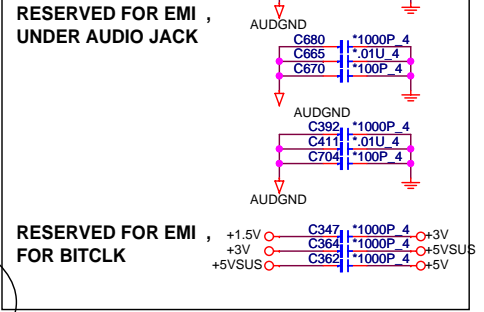
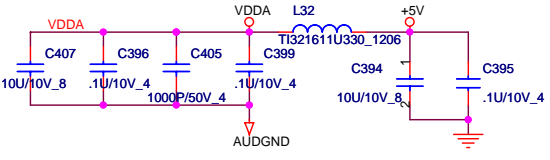
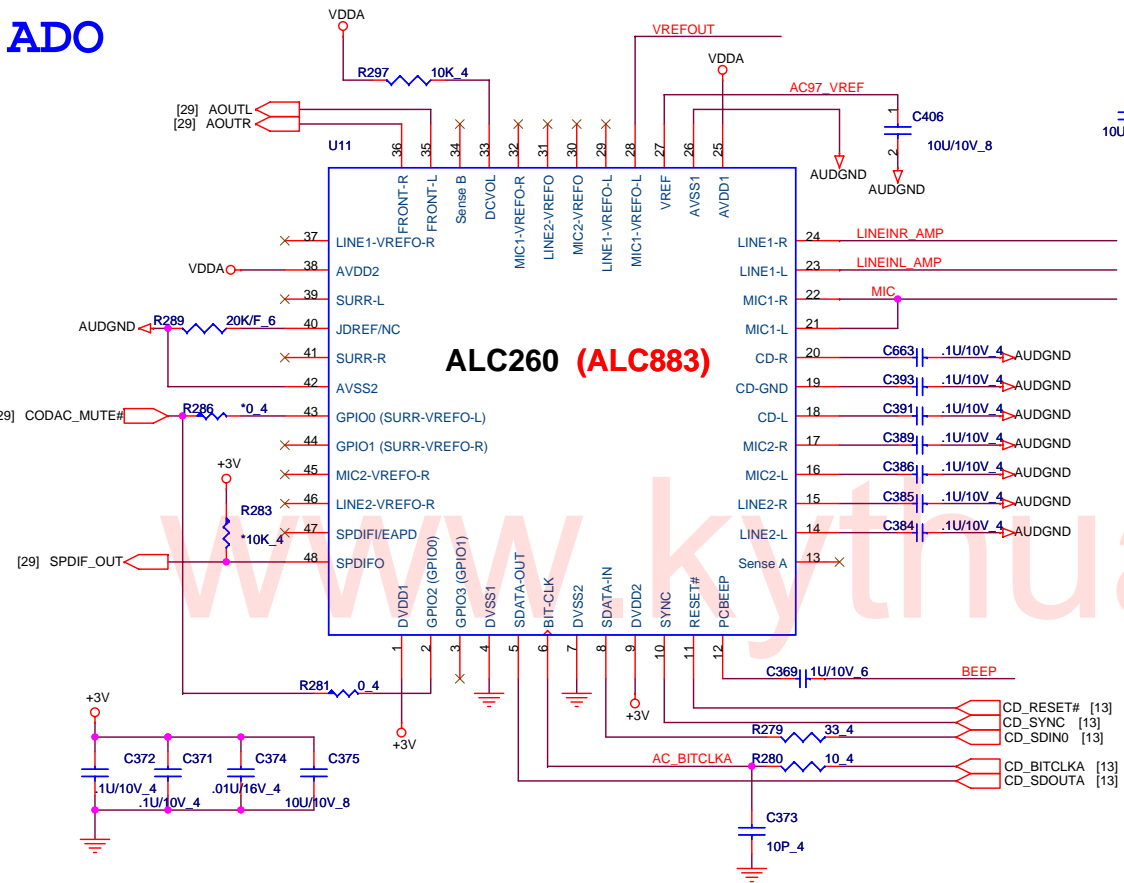


PROJECT : ZB2
Quanta Computer Inc.

Size: Document Number
PCI7412-CARD READER

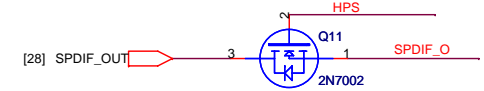
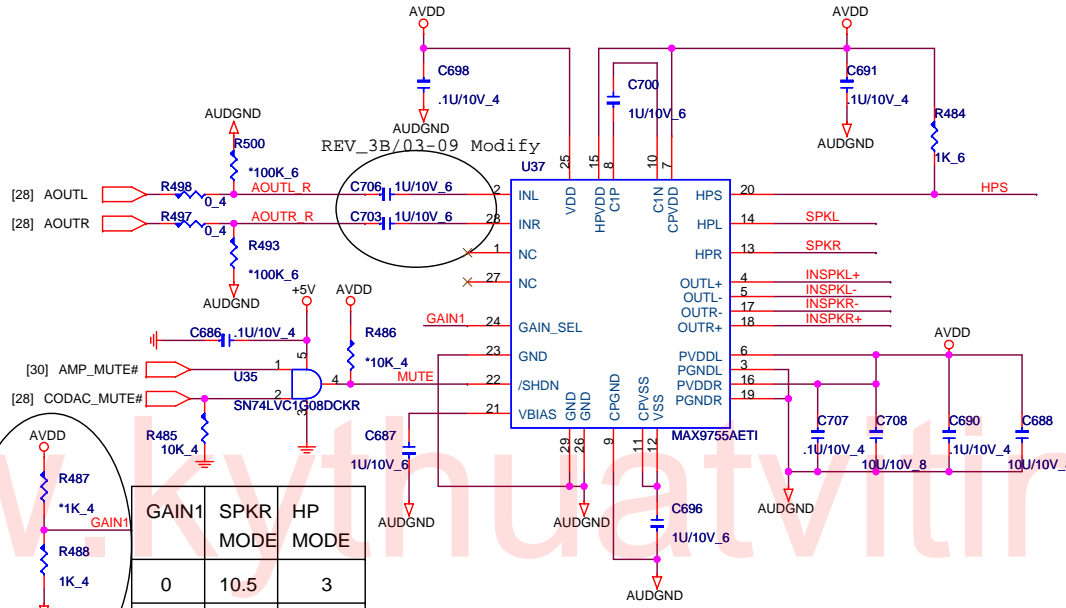
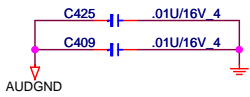
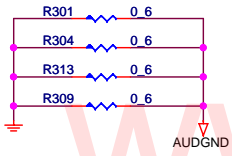
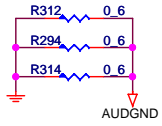
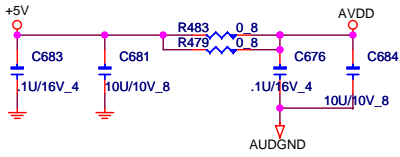
Date: Monday, April 10, 2006 Sheet 27 of 37

Rev 3A

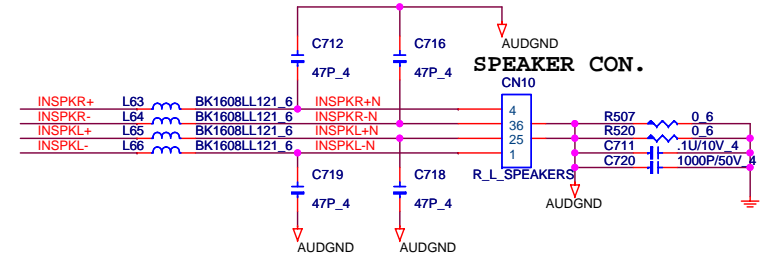


PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	REALTEK ALC883	3B
Date:	Monday, April 10, 2006	Sheet 28 of 37

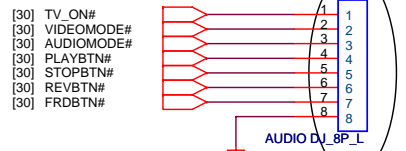


REV_2A/01-06 Modify

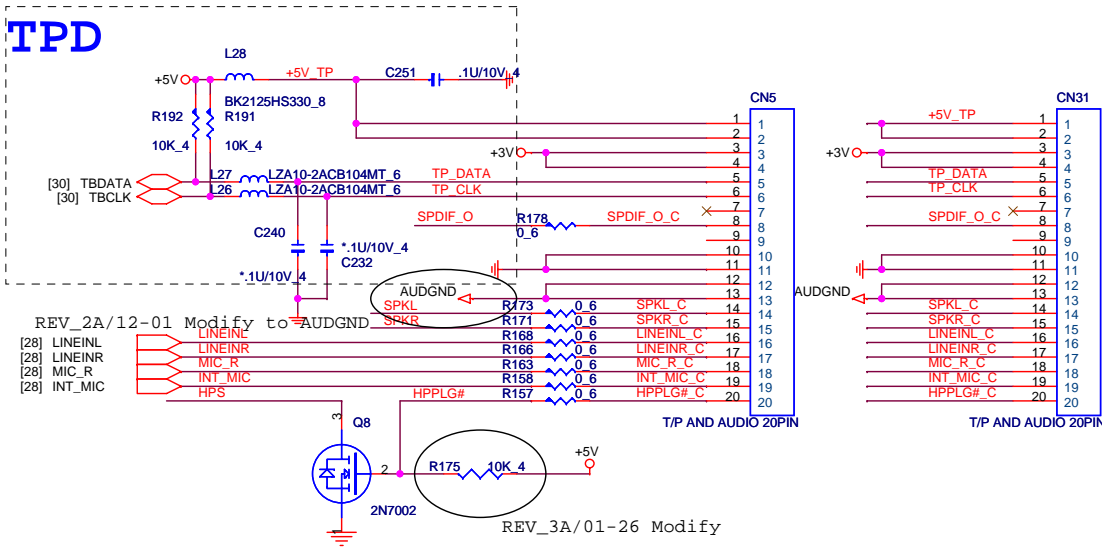


AUDIO DJ

ADJ



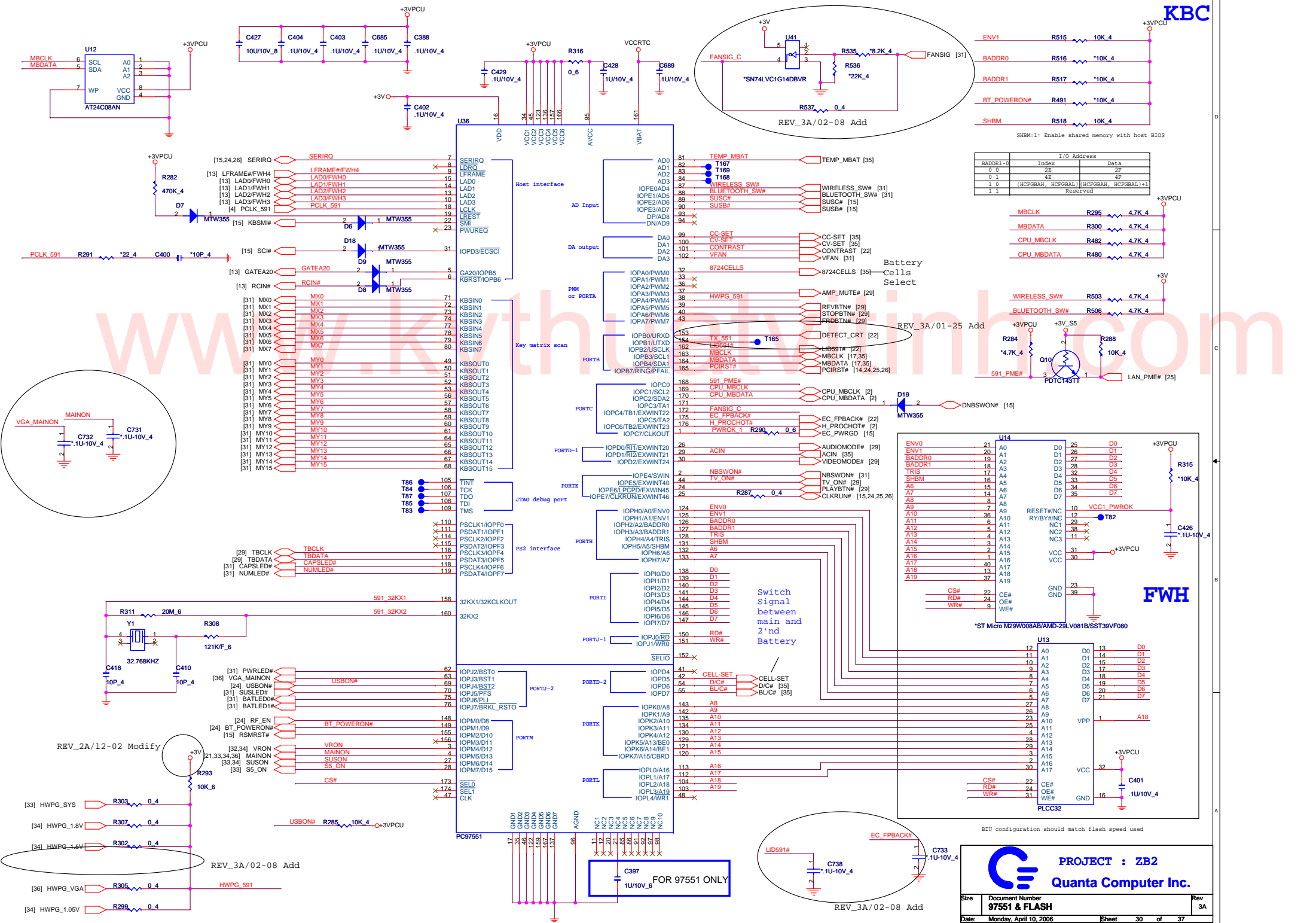
REV_3B/03-09 Modify Footprint



REV_3A/01-26 Modify

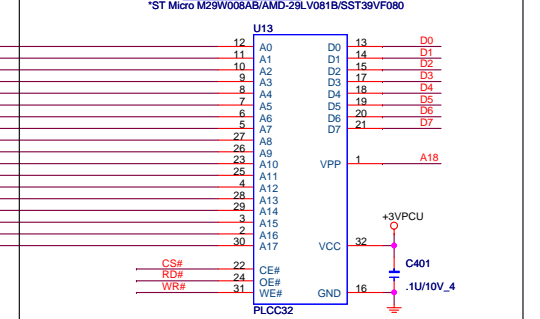
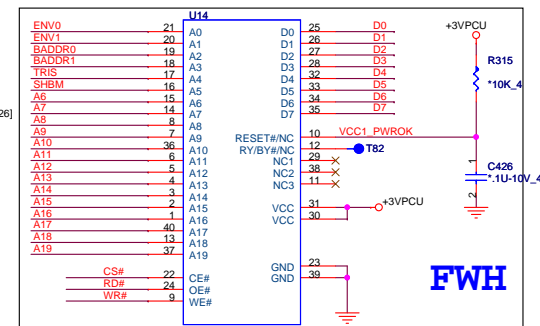
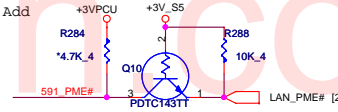
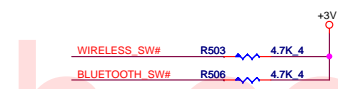
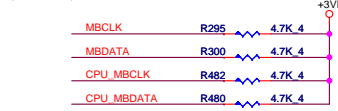
PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP(MAX 9755)	3B
Date:	Monday, April 10, 2006	Sheet 29 of 37



SHBM=1: Enable shared memory with host BIOS

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	{HCFG0A8, HCFG0B1} {HCFG0A8, HCFG0B1}+1	Reserved
1 1		Reserved



BIU configuration should match flash speed used

PROJECT : ZB2
Quanta Computer Inc.

Size: Document Number
97551 & FLASH

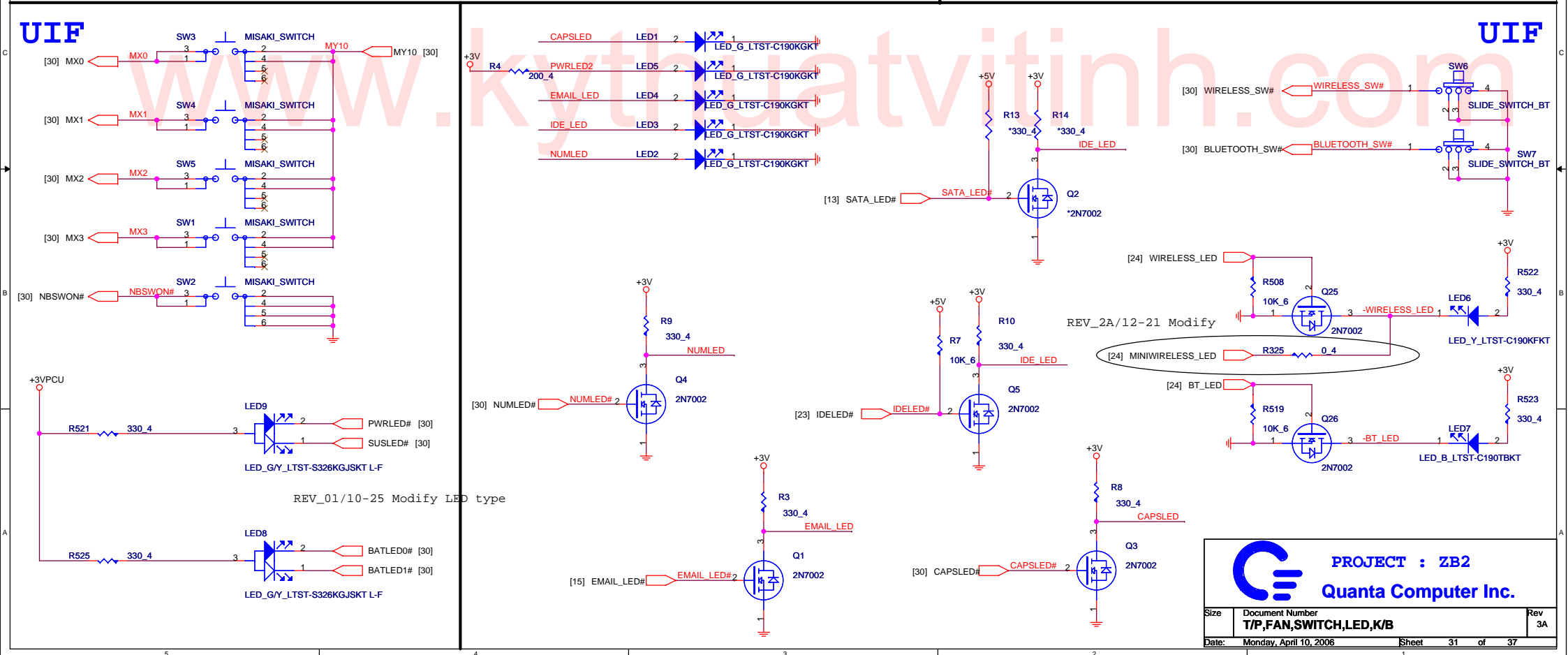
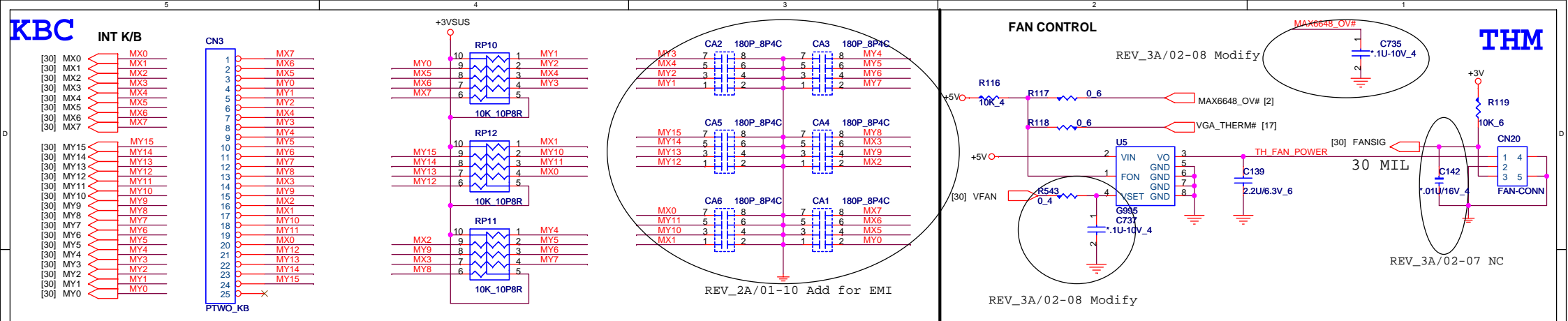
Date: Monday, April 10, 2006 Sheet 30 of 37

C397 FOR 97551 ONLY

REV_3A/02-08 Add

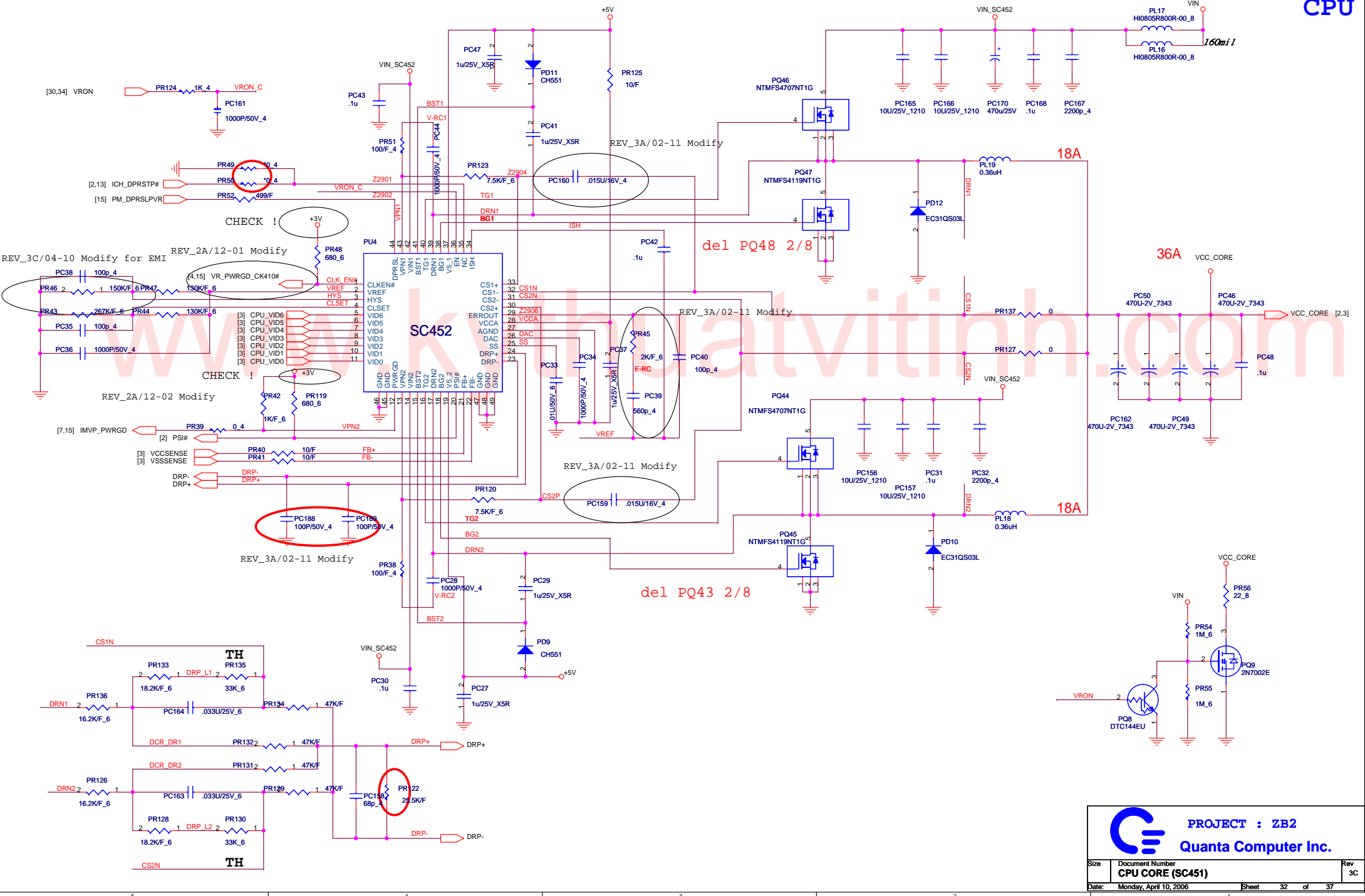
REV_3A/02-08 Add

REV_2A/12-02 Modify



PROJECT : ZB2
Quanta Computer Inc.

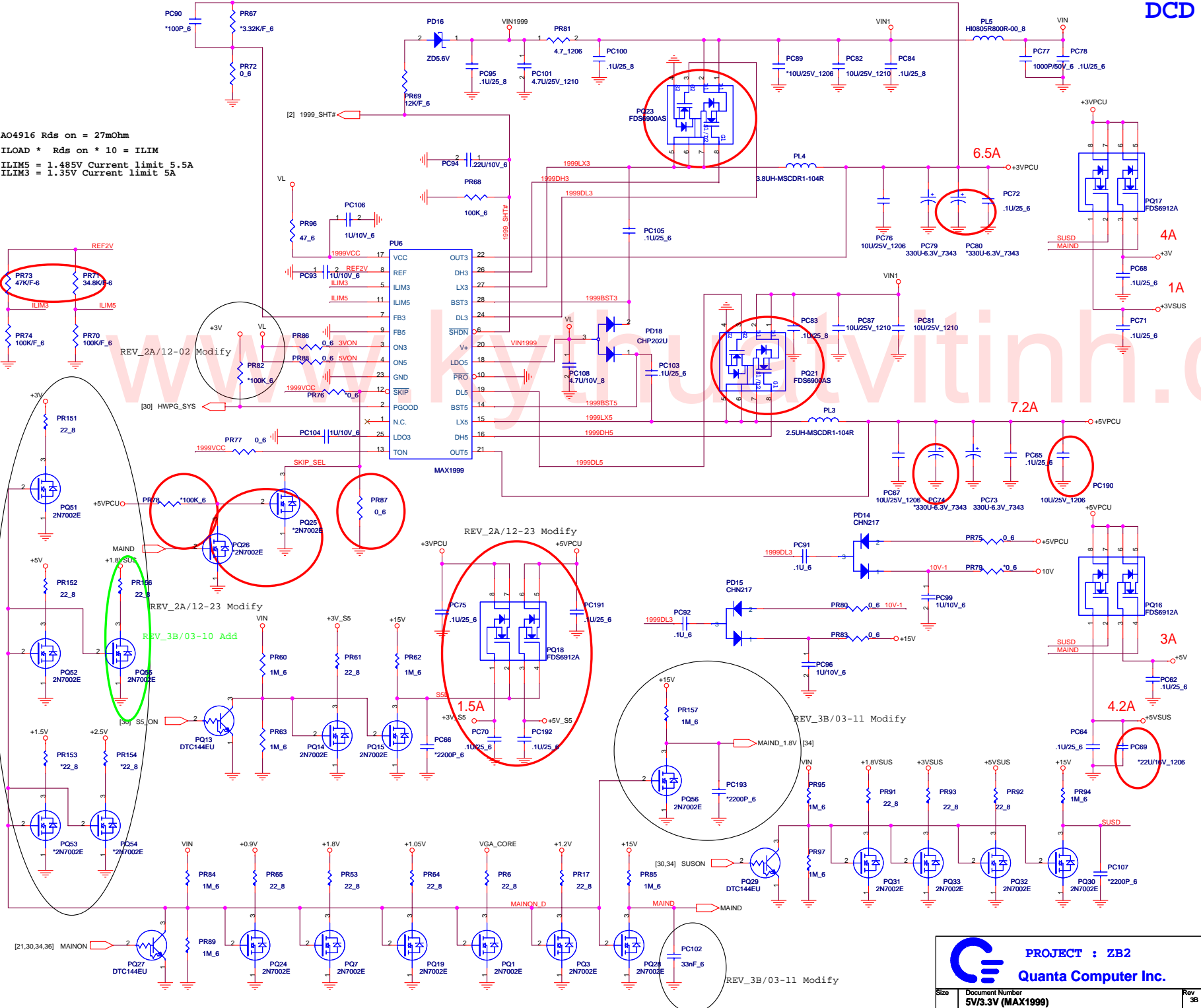
Size	Document Number	Rev
	T/P,FAN,SWITCH,LED,K/B	3A
Date:	Monday, April 10, 2006	Sheet 31 of 37



PROJECT : ZB2
Quanta Computer Inc.

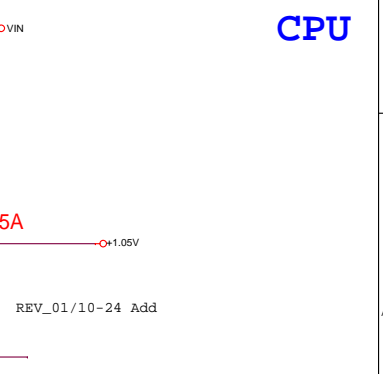
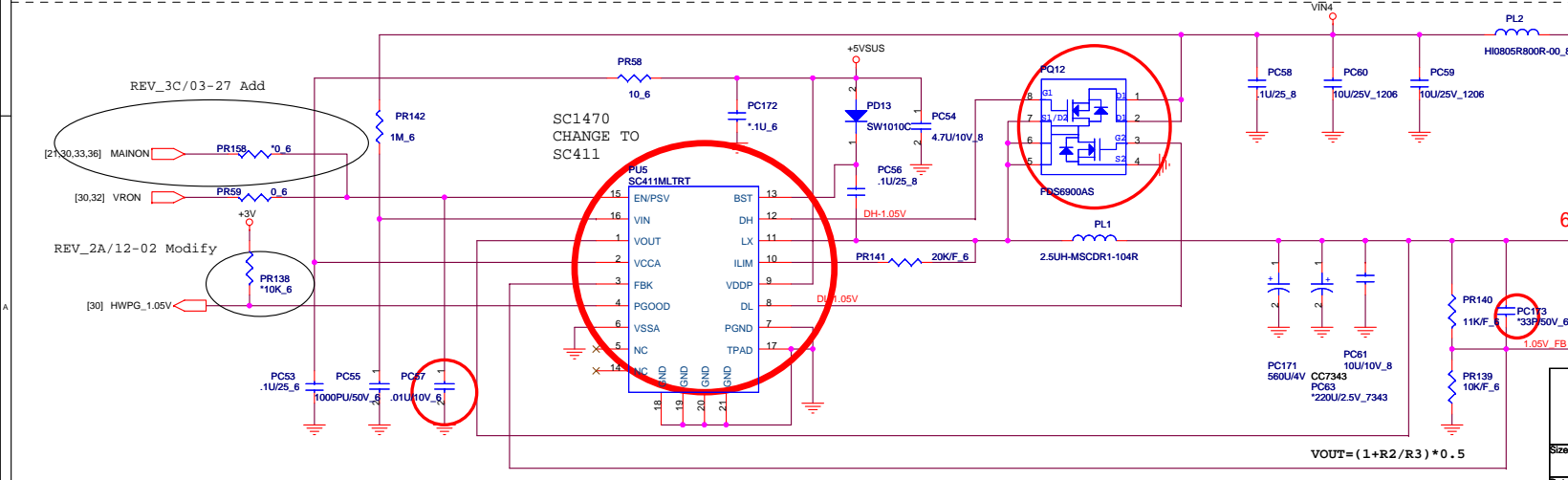
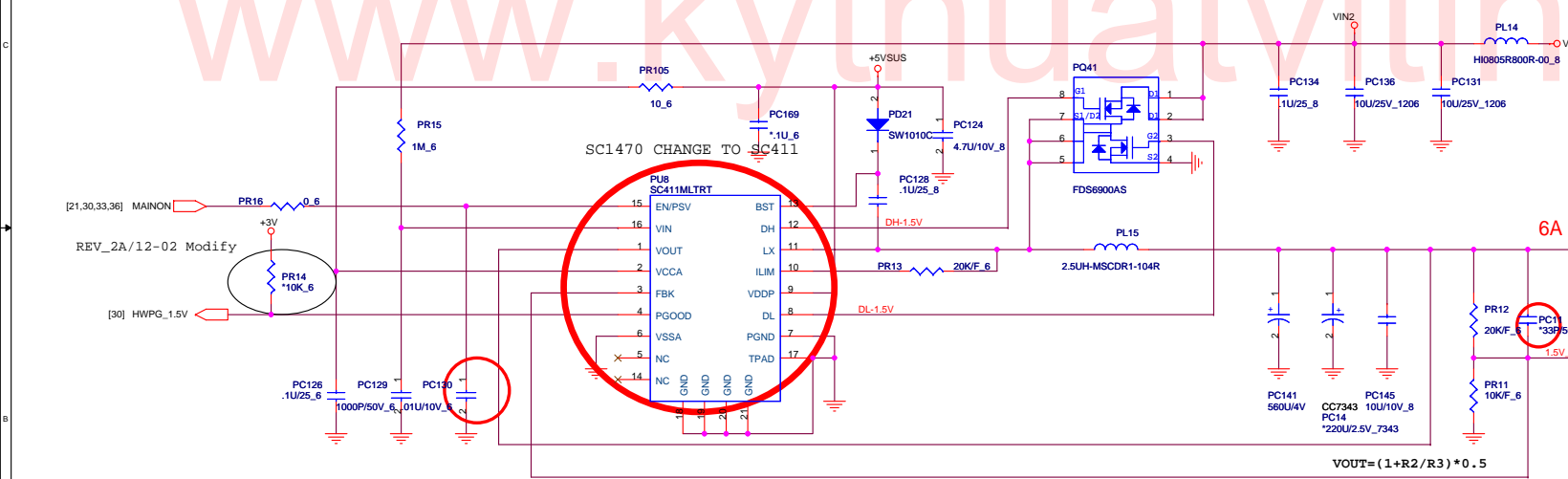
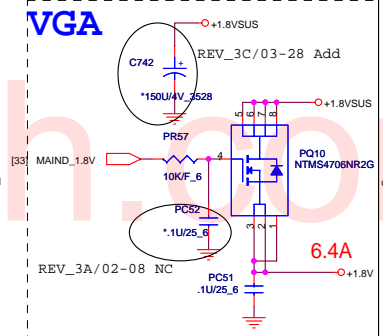
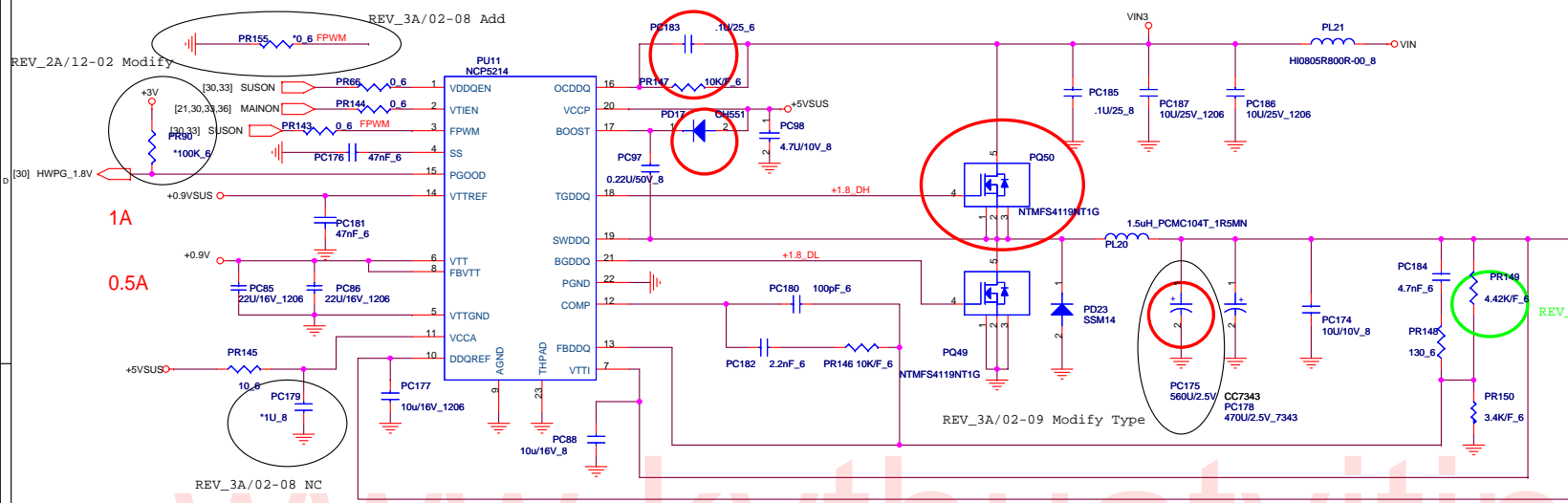
Size	Document Number	Rev
	CPU CORE (SC451)	3C
Date:	Monday, April 10, 2006	Sheet 32 of 37

AO4916 Rds on = 27mOhm
ILOAD * Rds on * 10 = ILIM
ILIM5 = 1.485V Current limit 5.5A
ILIM3 = 1.35V Current limit 5A



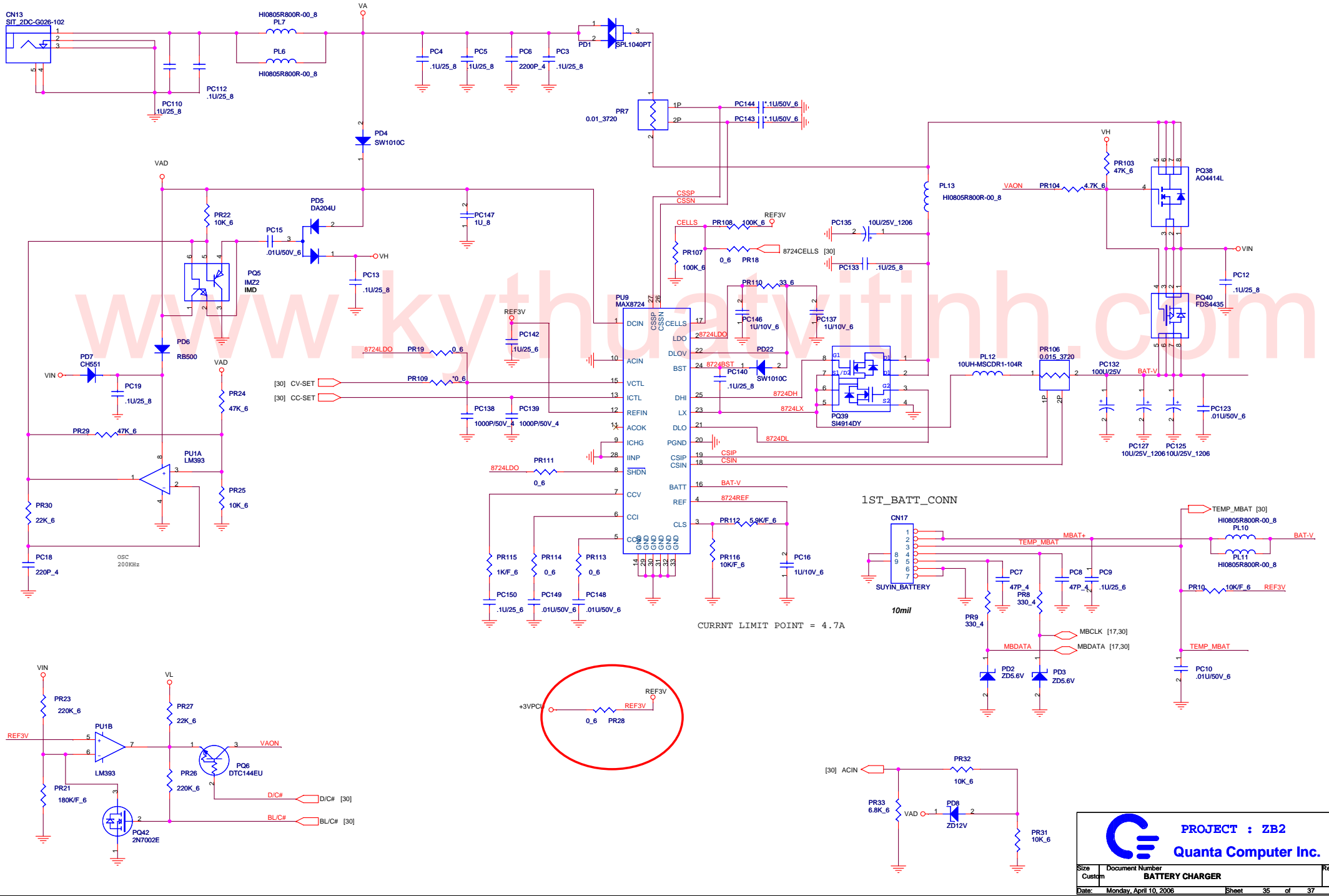
PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	5V/3.3V (MAX1999)	3B
Date:	Monday, April 10, 2006	Sheet 33 of 37

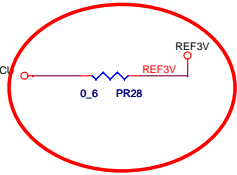


PROJECT : ZB2
Quanta Computer Inc.

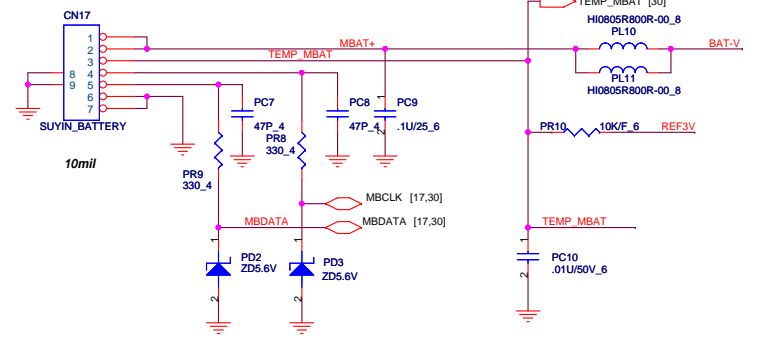
Size	Document Number	Rev
	1.8VSUS / +0.9VTERM/+1.05V/+2.5V	3C
Date:	Monday, April 10, 2006	Sheet 34 of 37



CURRENT LIMIT POINT = 4.7A

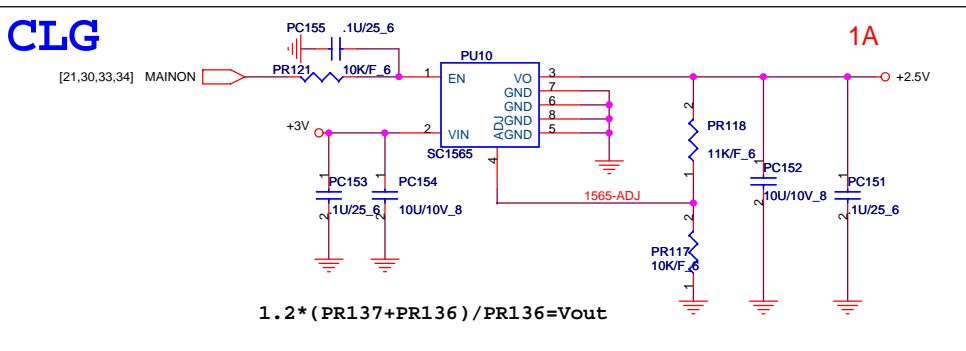
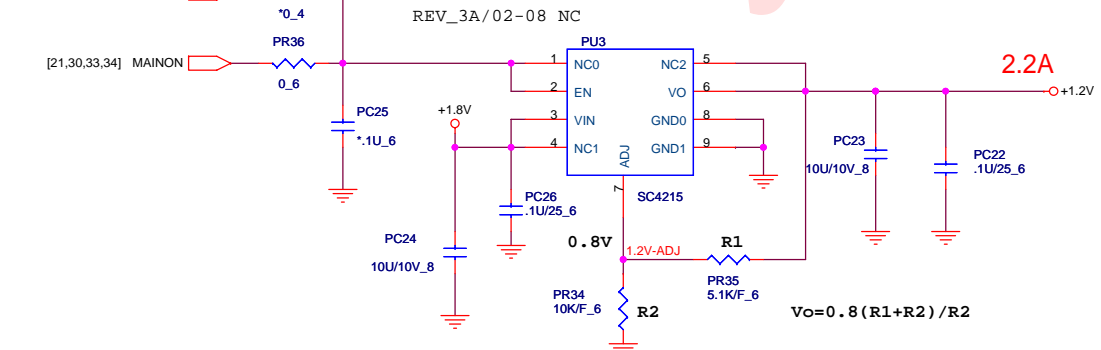
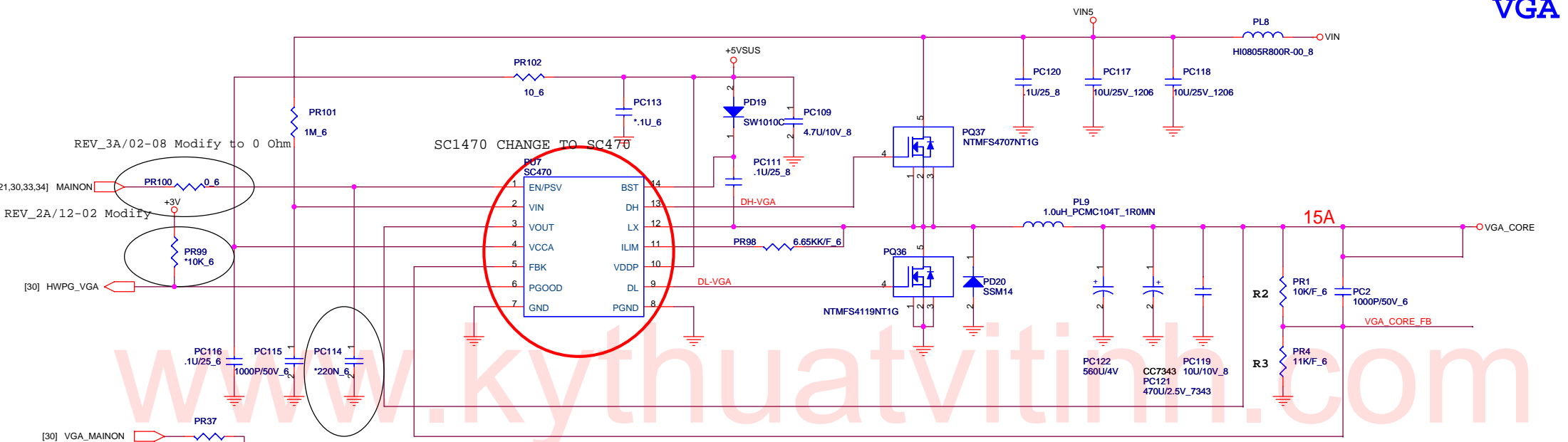


1ST_BATT_CONN



PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BATTERY CHARGER	1A
Date:	Monday, April 10, 2006	Sheet 35 of 37



HI--> VOUT = (1 + R2/R3) * 0.5
 LO--> VOUT = (1 + R2/(R3//R4)) * 0.5

- M52P (G)**
 PR1 : 10K
 PR4 : 11K
 PR2 : 110K

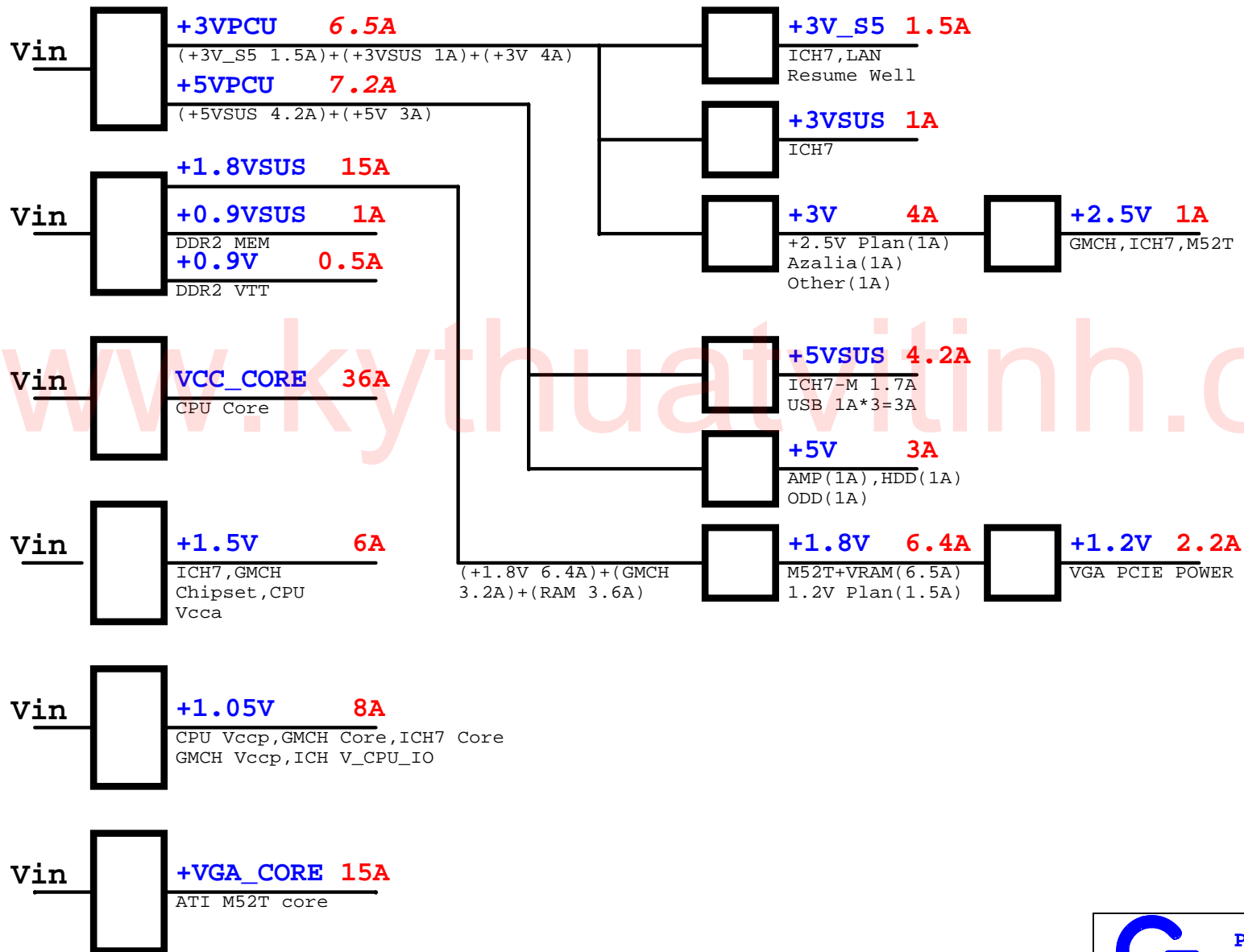
- M54P**
 PR1 : 12K
 PR4 : 12K
 PR2 : 60.4K


Power Play Mode

VGA_PWR_SW	VGA_CORE
HI	0.95V--M52P (G)
Default	1.0V --M54P
LO	1.0V--M54P

PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	VGA CORE/+1.2V	3A
Date:	Monday, April 10, 2006	Sheet 36 of 37




PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	POWER DIAGRAM	1A
Date:	Monday, April 10, 2006	Sheet 37 of 37