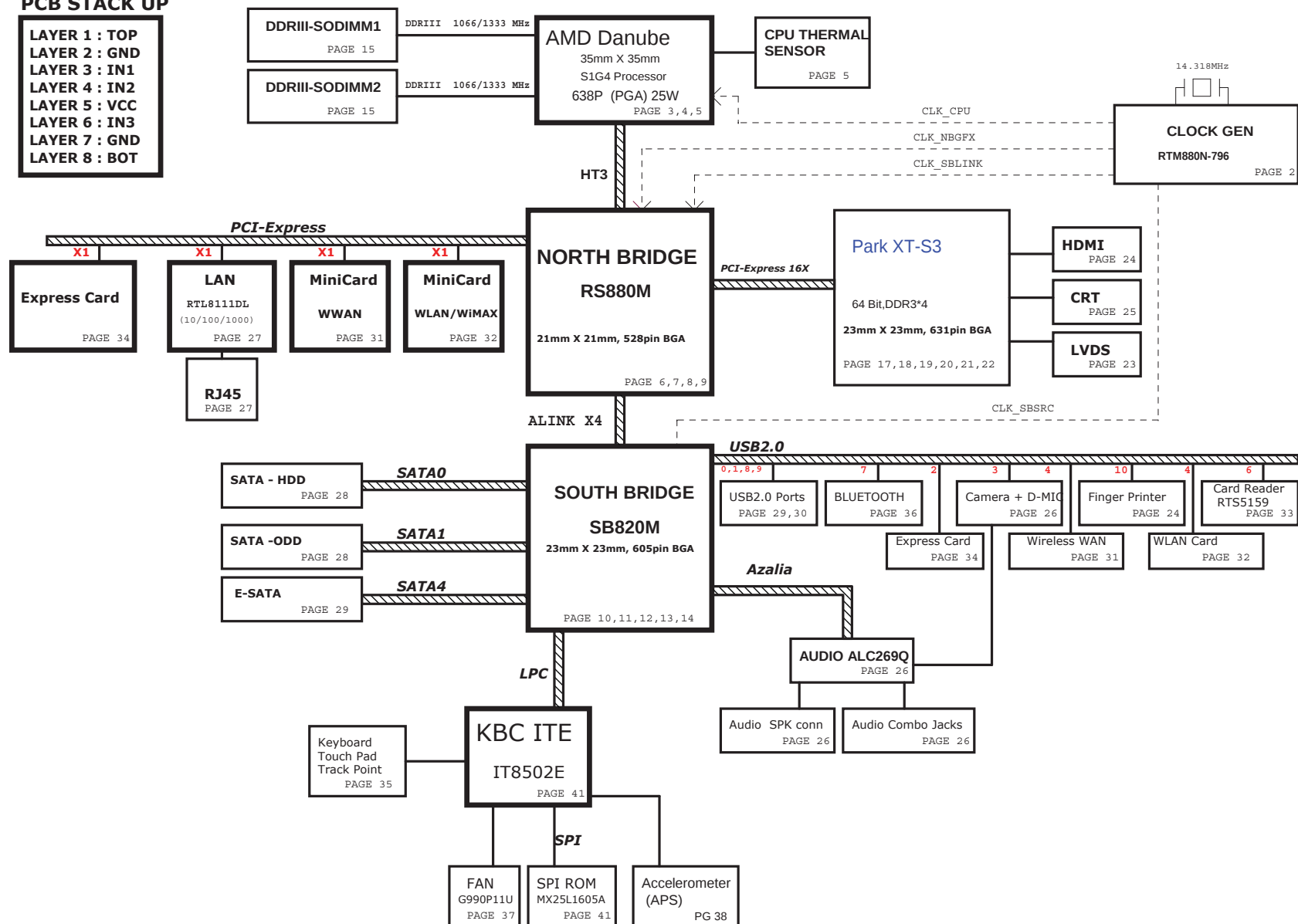


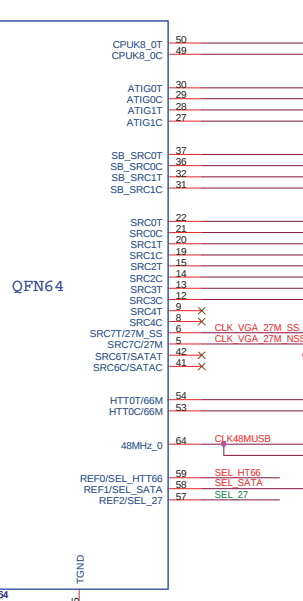
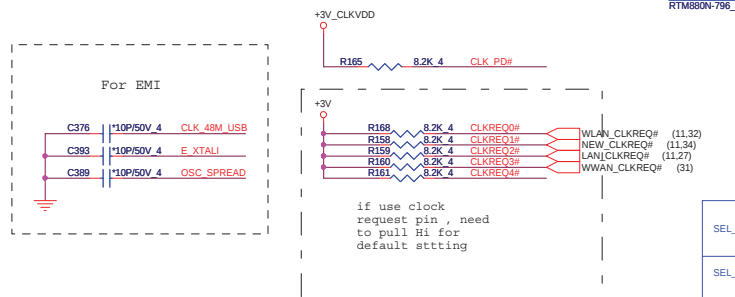
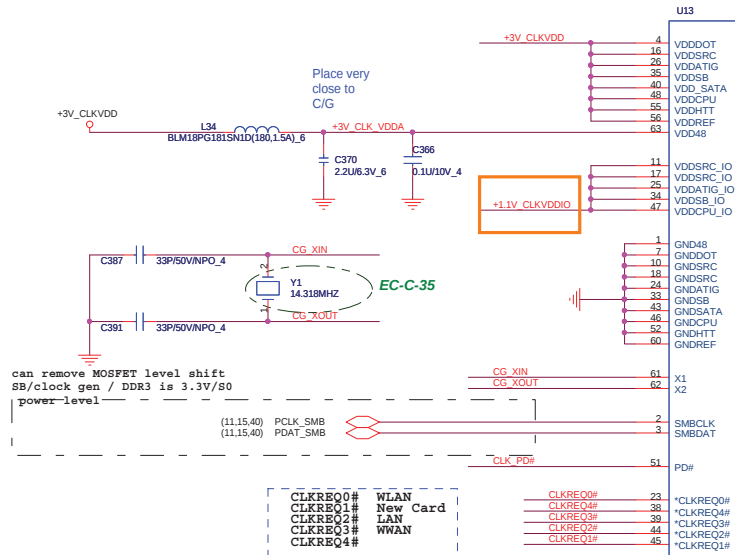
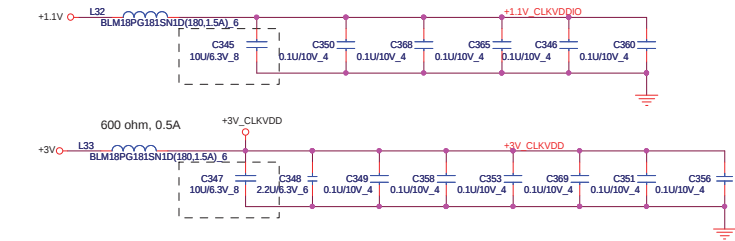
LD-Note Block Diagram -- AMD Danube

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

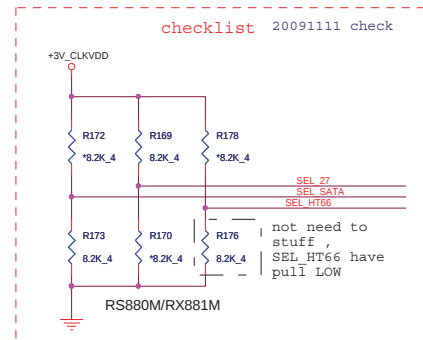
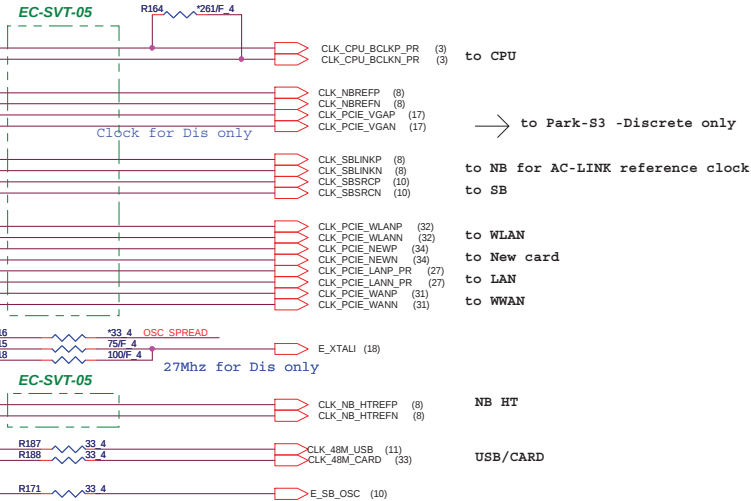


EXT GFX CLKP EXT GFX CLKN	RP47 STUFF	to Park-S3 external reference clock -Discrete only
SBLINK_CLKP SBLINK_CLKN	RP43 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_NSS CLK_VGA_27M_SS	R213,R215 STUFF	To Park-S3 27Mhz - Discrete only

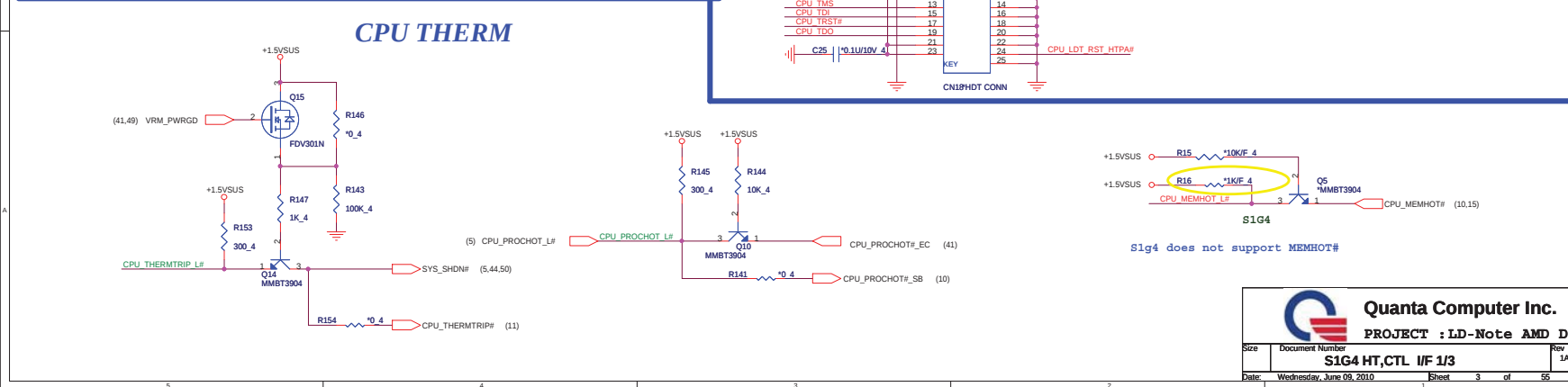
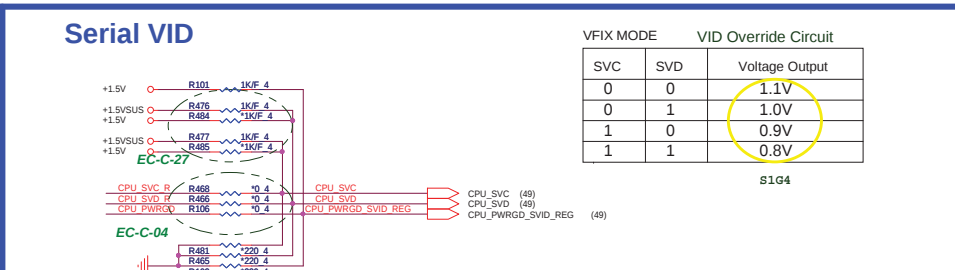
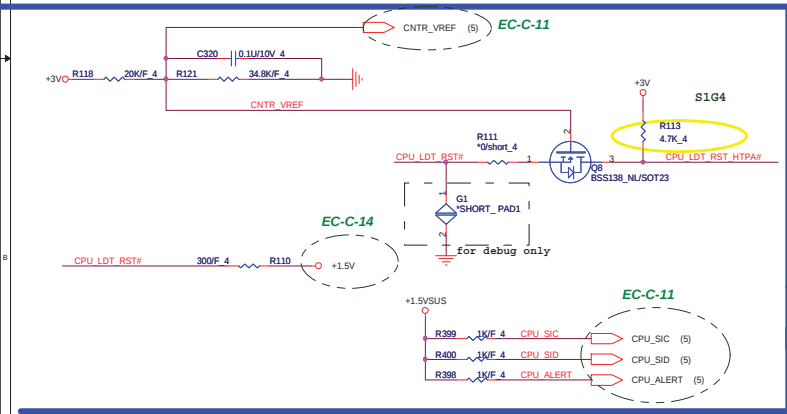
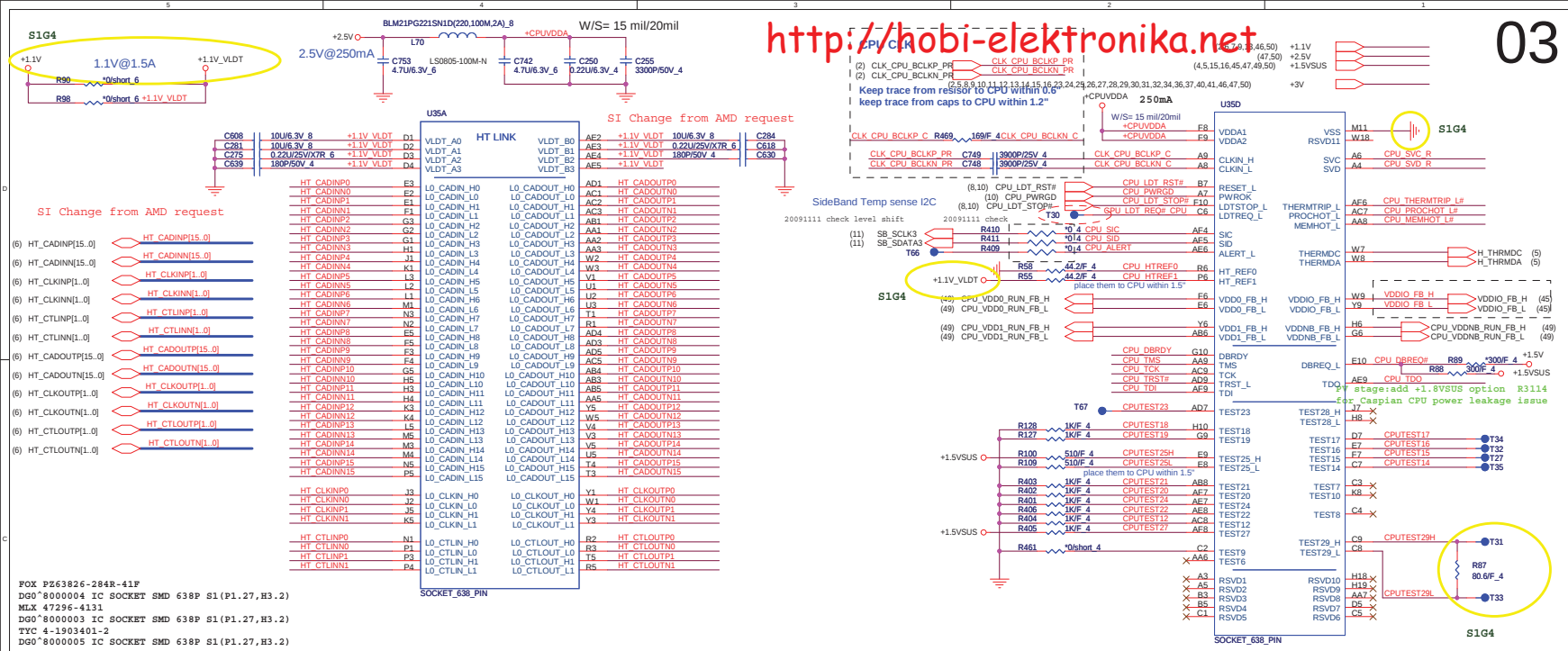


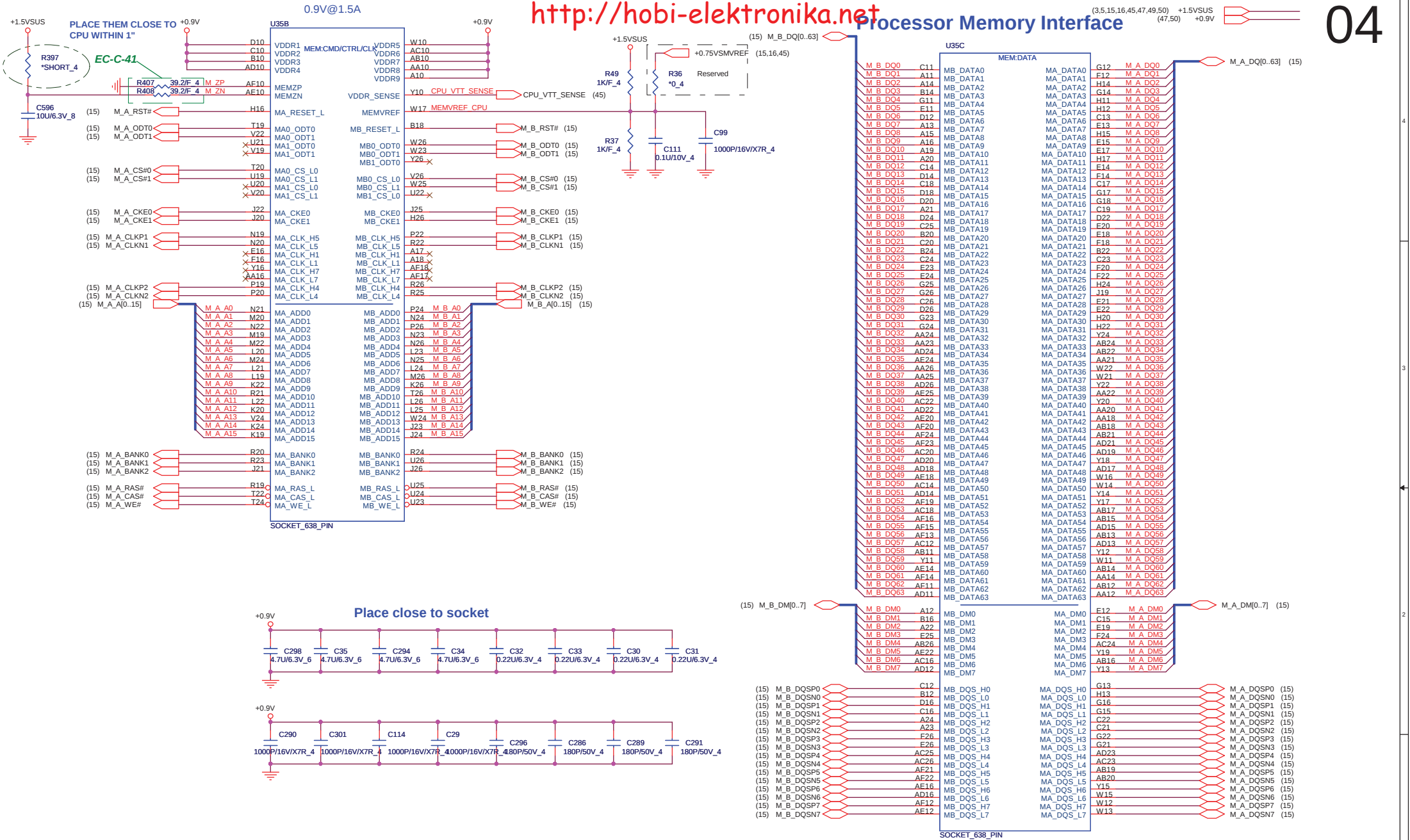
IC: ICS9LPRS476AKLFT
SLG: SLG8SP628VTR--AL8SP628000
RTL: RTM880N-796--AL000880001

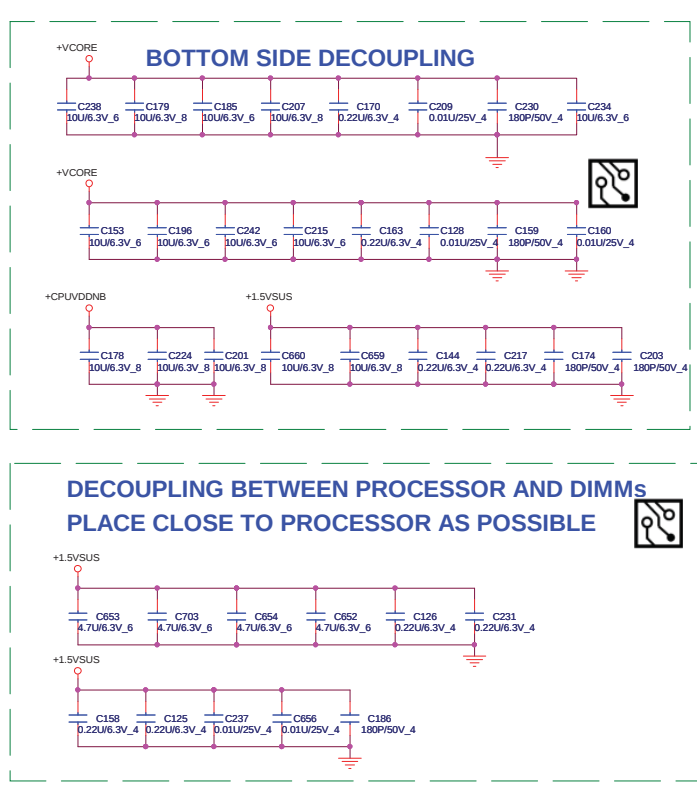
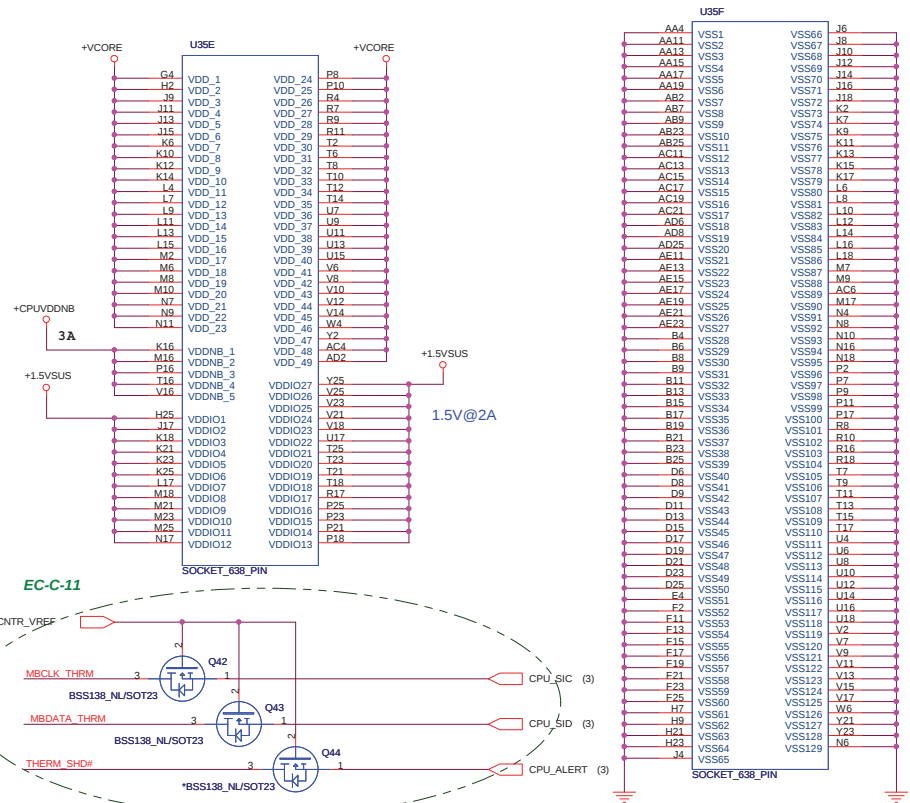
SEL_HTT66	1	66 Mhz 3.3V single ended HTT clock
SEL_SATA	0*	100 Mhz differential HTT clock
SEL_27	1*	100 Mhz non-spreading differential SRC clock
	0*	100 Mhz spreading differential SRC clock
	1*	27Mhz non-spreading singled clock
	0	100 Mhz spreading differential SRC clock



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

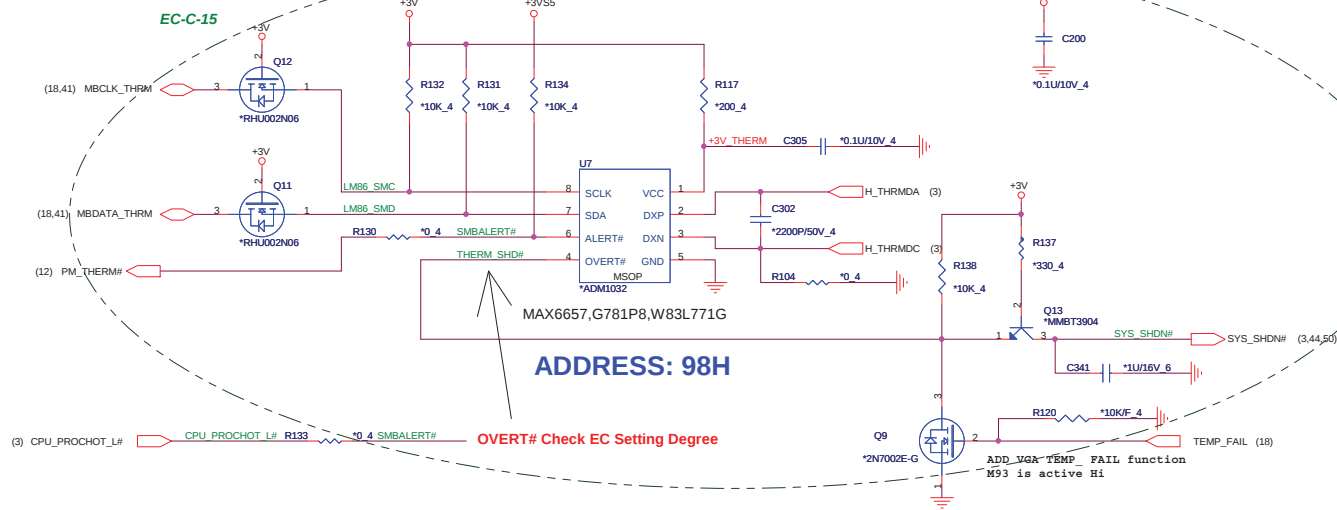


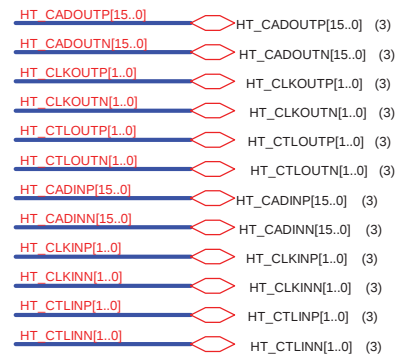




CPU H/W MONITOR

Thermal

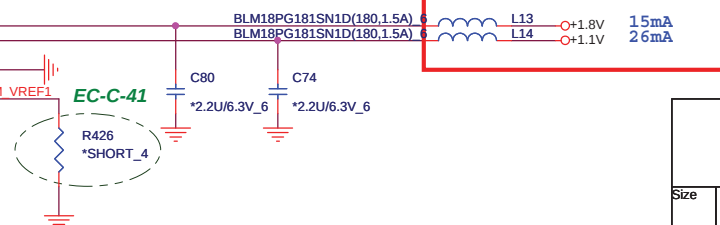




(2,3,7,9,13,46,50) +1.1V
(3,8,31,32,34,50) +1.5V
(8,9,14,46,50) +1.8V



Close to NB within 1"

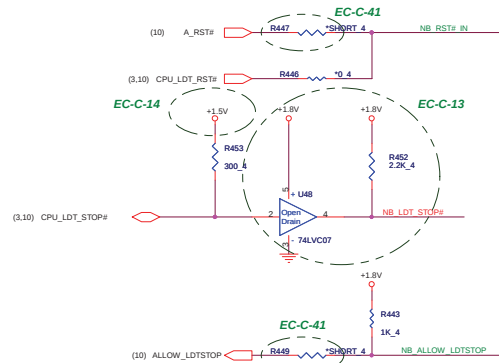


PROJECT : LD-Note AMD DIS

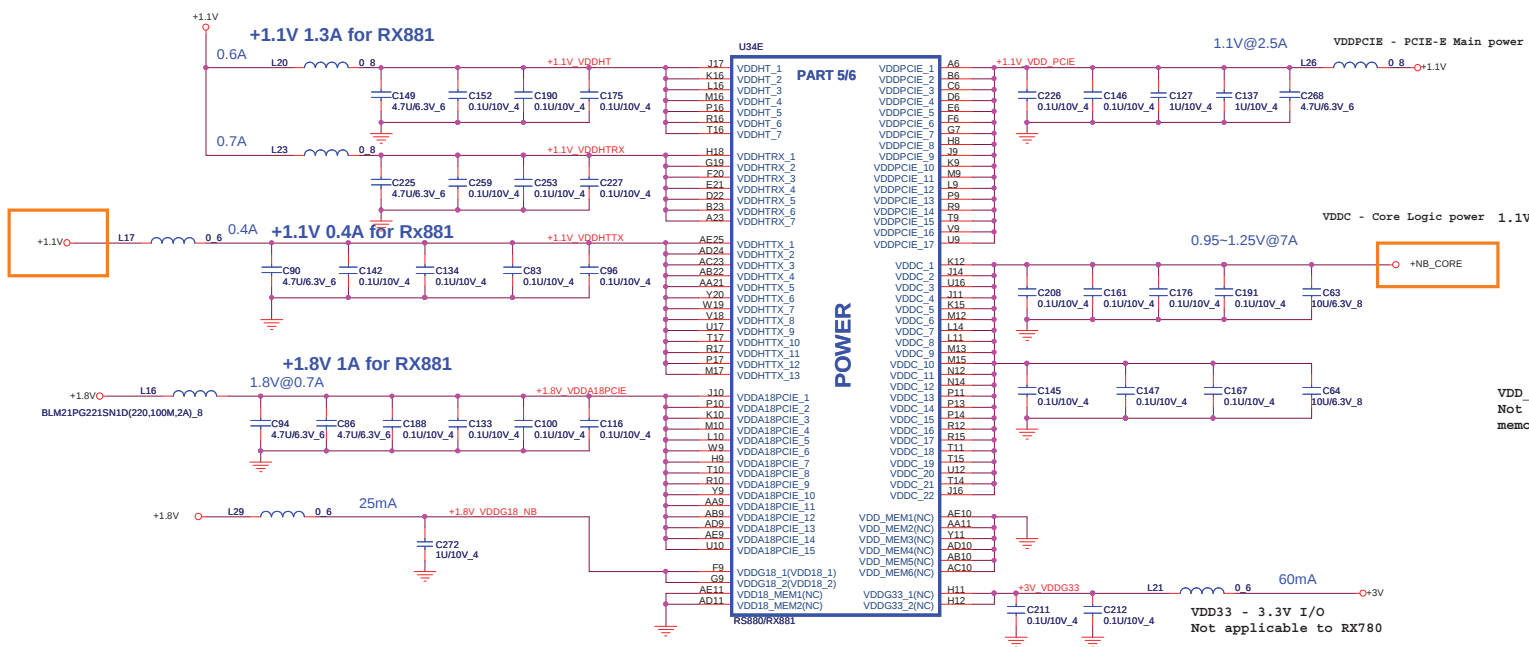
Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
Date:	Wednesday, June 09, 2010	Sheet 6 of 55

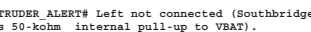


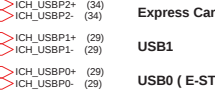
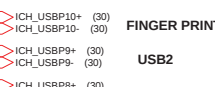
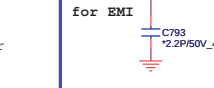
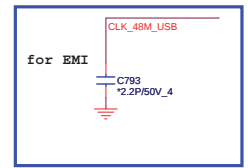
All PCIe lane should route 8" max for Gen2 connector and max 12" for Gen2 on board devices. Guam has the Lasso lane over 8" due to the large board, should use shorter lasso cable for Guam. Customer needs to follow the MBDG.



PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	AVDDI1	GND	GND
VDDHTRX	+1.1V	+1.1V	AVDDQ	GND	GND
VDDHTTX	+1.2V	+1.1V	PLLVDD	GND	GND
VDDA18PCIE	+1.8V	+1.8V	PLLVDD18	GND	GND
VDDG18	+1.8V	+1.8V	VDDA18PCIEPLL	GND	GND
VDD18_MEM	GND	GND	VDDA18HFPLL	GND	GND
VDDPCE	+1.1V	+1.1V	VDDLTP18	GND	GND
VDDC	+1.1V	+NB_CORE	VDDL18	GND	GND
VDD_MEM	GND	GND	VDDL18	NC	NC
VDDG33	+3.3V	+3.3V			
AVDD	GND	GND			







SATA PORT 0,1,2,3
can support AHCI
mode

SATA HDD

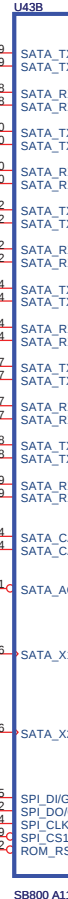
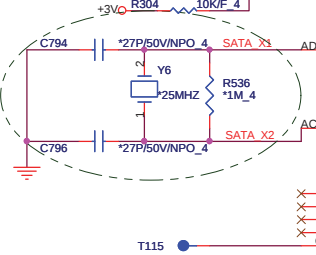
SATA ODD

E-SATA



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

EC-C-34



SB800
Part 2 of 5

SERIAL ATA

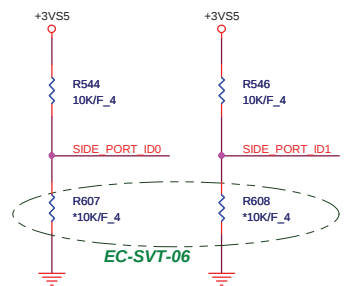
HW MONITOR

SPI ROM

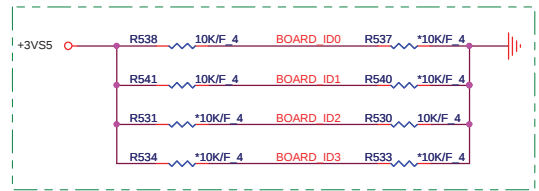


(2,3,5,8,9,10,11,13,14,15,16,23,24,25,26,27,28,29,30,31,32,34,36,37,40,41,46,47,50) +3VS5
(5,10,11,13,14,29,32,50) +3V

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

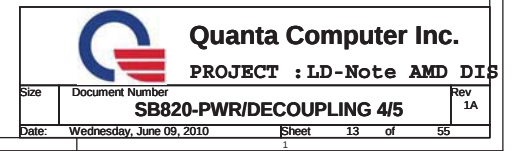


EC-SVT-03



EC-C-29
EC-C-44

EC_ID1	ID3	ID2	ID1	ID0	
	0	X	X	X	BL GC5C UMA (14")
	1	X	X	X	LD GC6C UMA (15")
0	X	0	0	0	SDV
0	X	0	0	1	SIT
0	X	0	1	0	SIT-R2
0	X	0	1	1	SVT
0	X	1	0	0	SOVP
	X	1	1	1	USB HW solution implementation

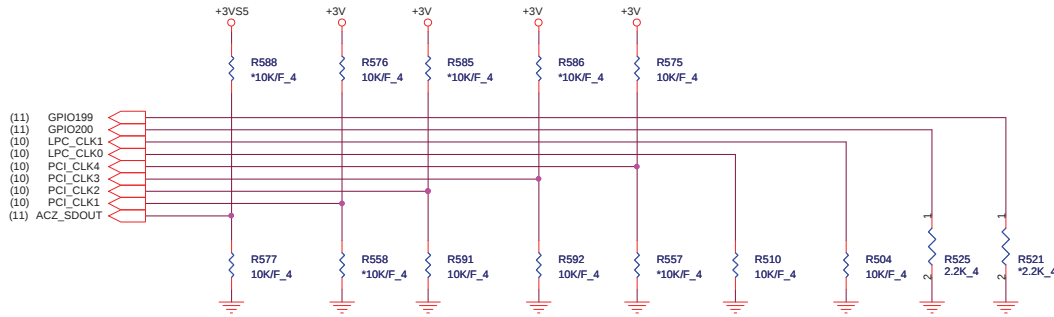


REQUIRED STRAPS

<http://hobi-elektronika.net>

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

14



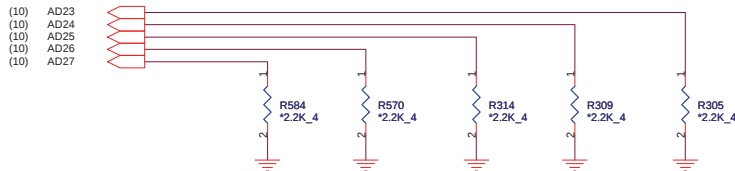
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	L, H=LPC ROM DEFAULT L, L=FWH ROM	

internal have
pull Hi 10K

NB_PWRGD_IN:
R588/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

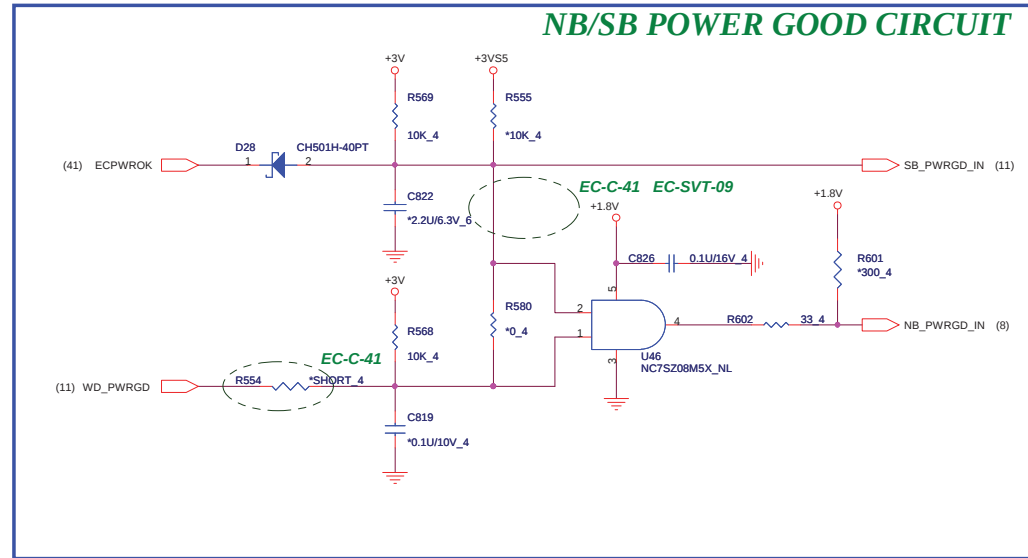
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB/SB POWER GOOD CIRCUIT



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



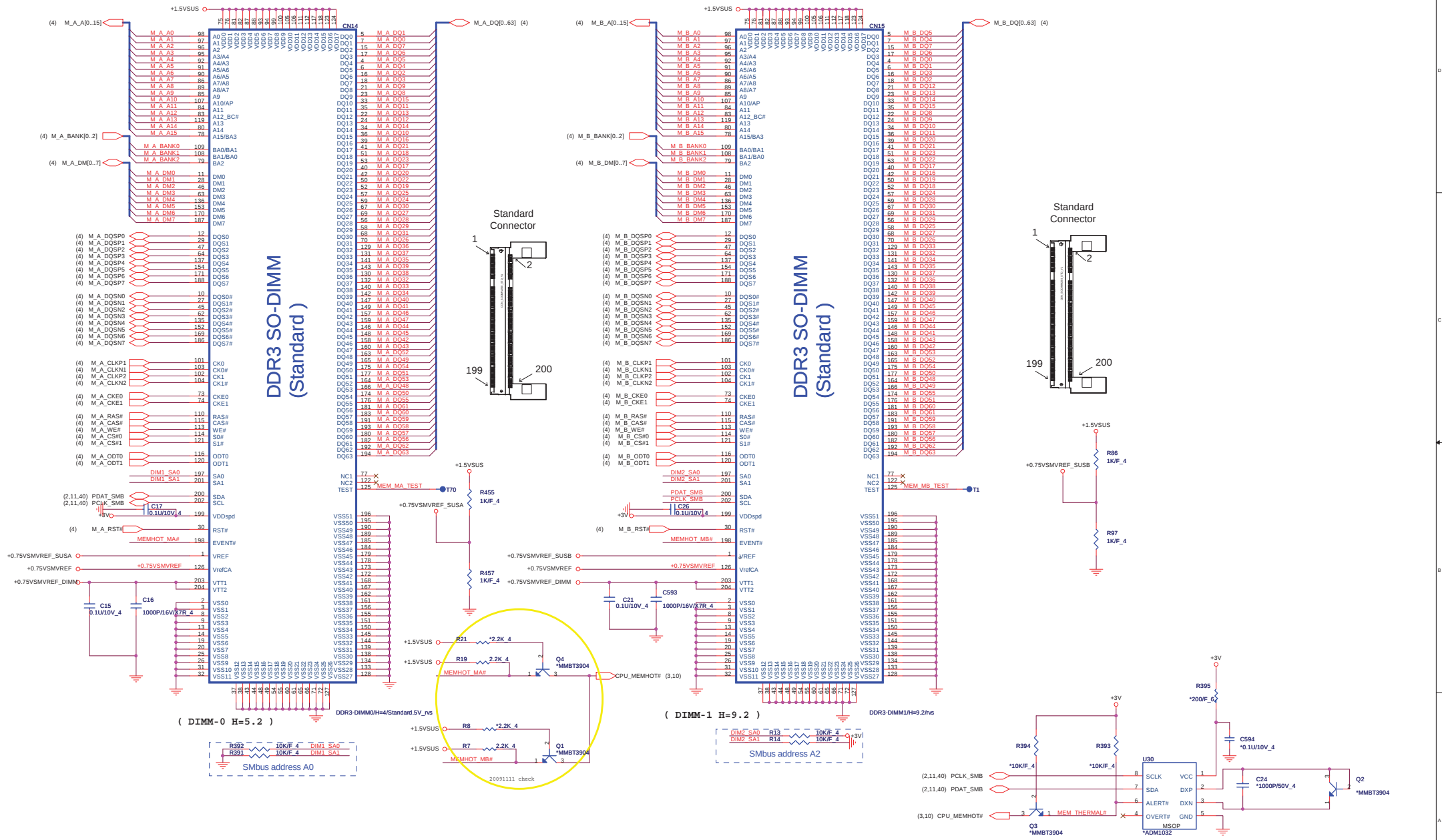
Quanta Computer Inc.

PROJECT : LD-Note AMD DIS

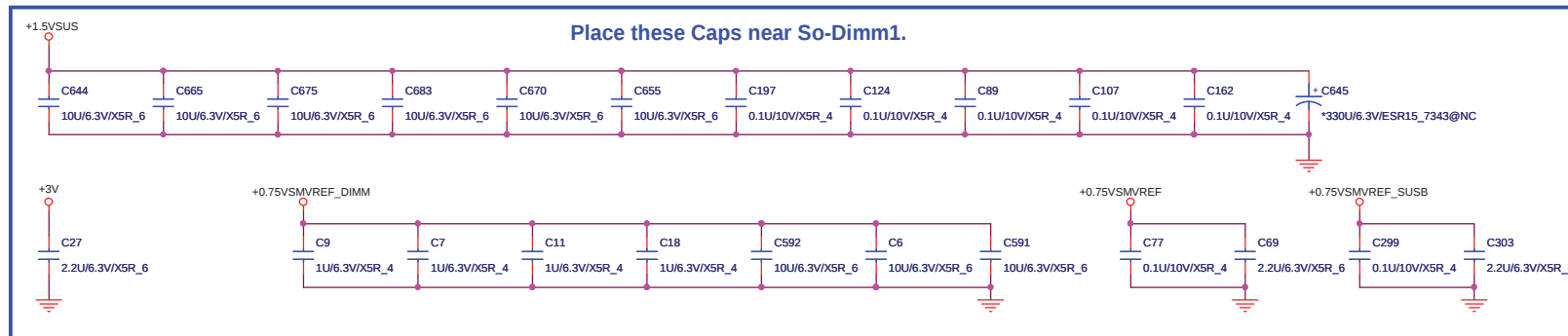
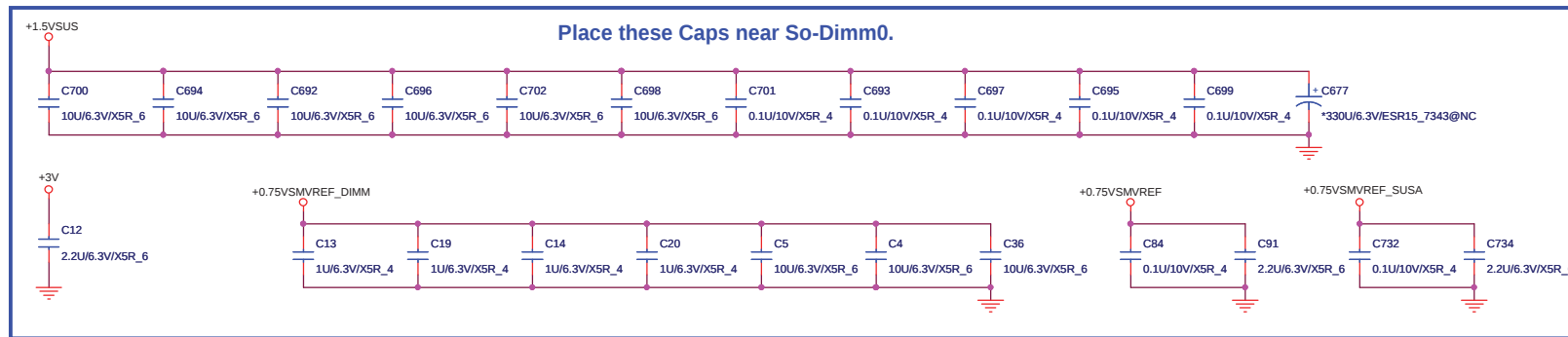
Size	Document Number	Rev
	SB820-STRAPS 5/5	1A
Date:	Monday, June 14, 2010	Sheet 14 of 55

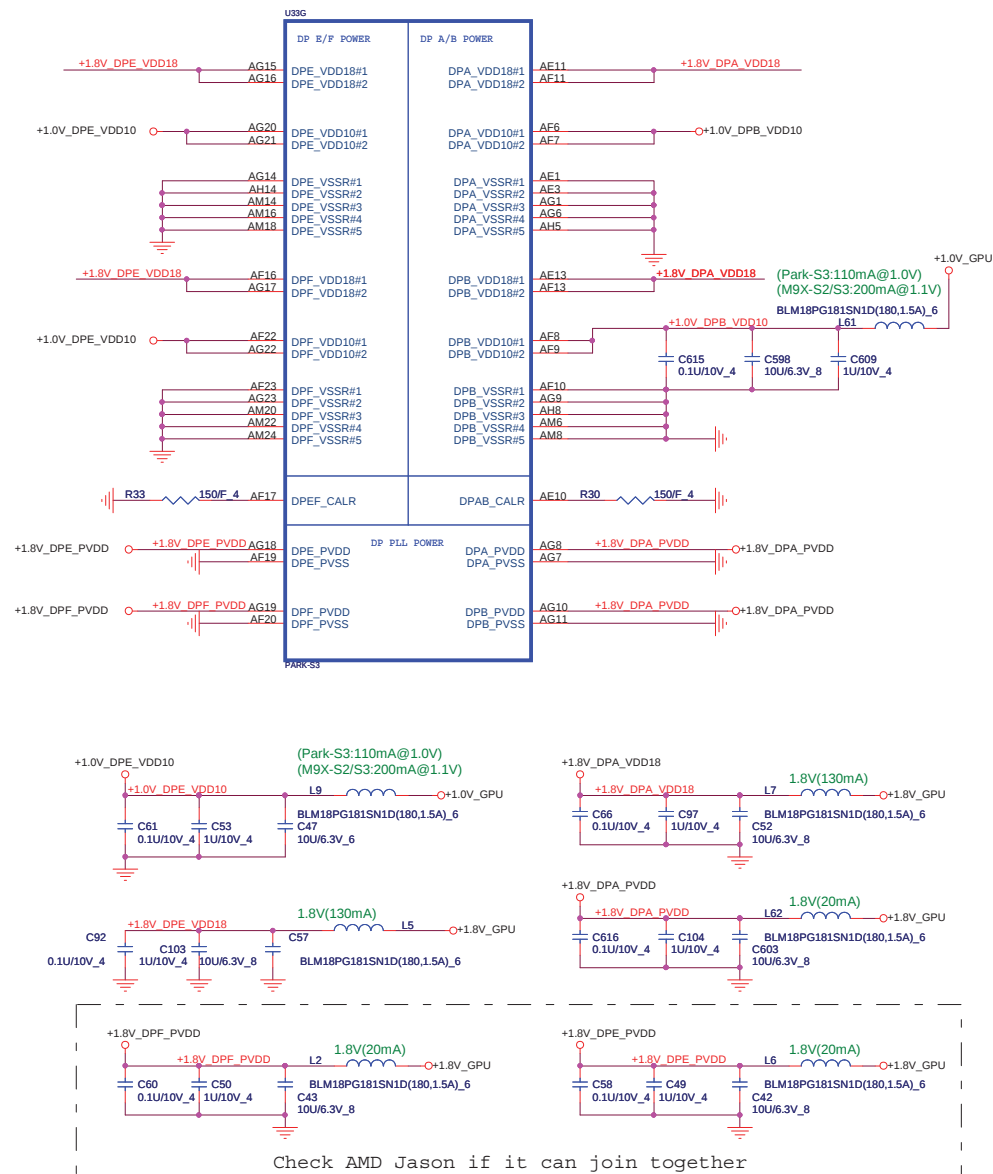
Place these Caps near So-Dimm0.

(4,16,45) +0.75VSMVREF
(3,4,5,16,45,47,49,50) +1.5VSUS
(16,45,50) +0.75VSMVREF_DIMM
30,31,32,34,36,37,40,41,46,47,50) +3V

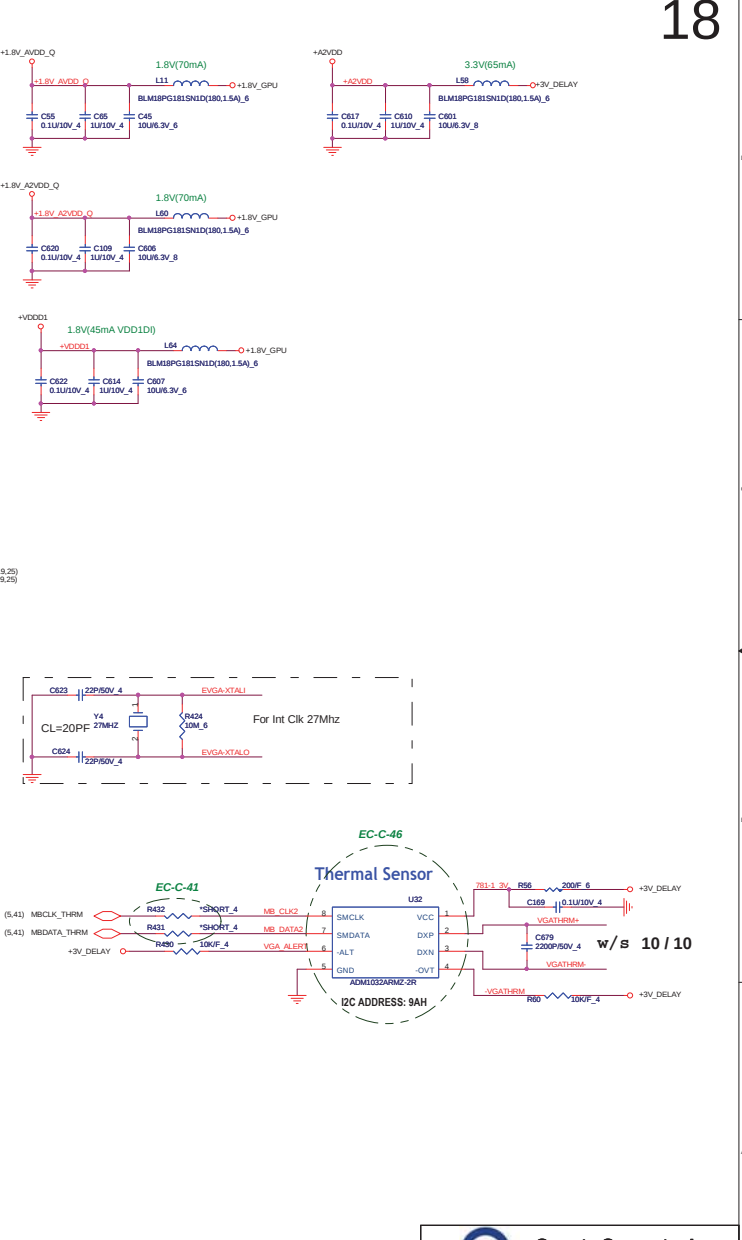
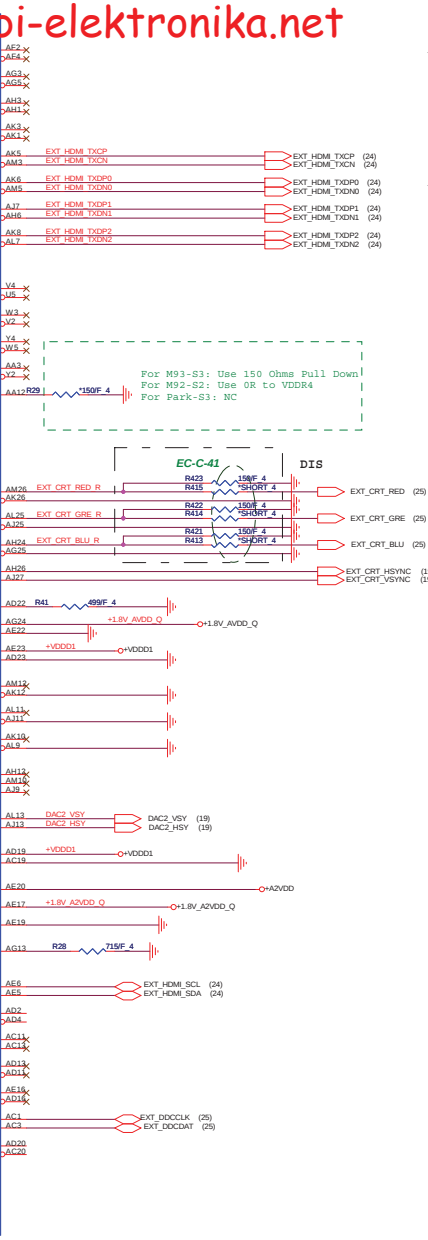
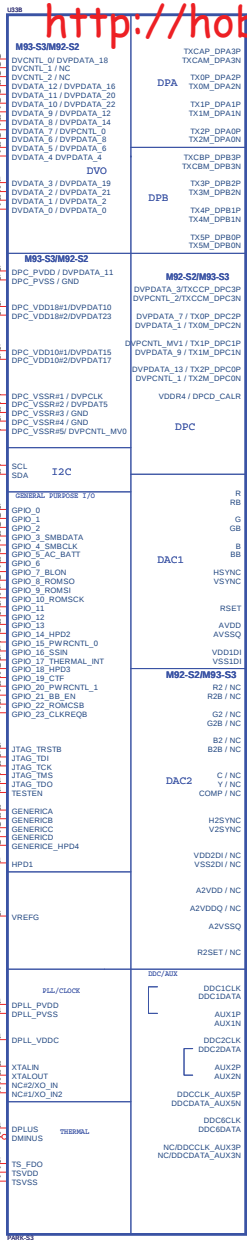
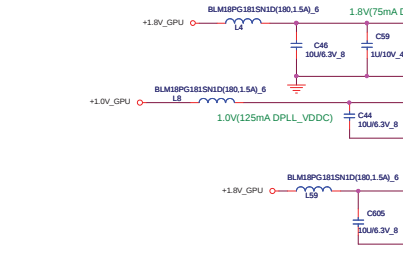


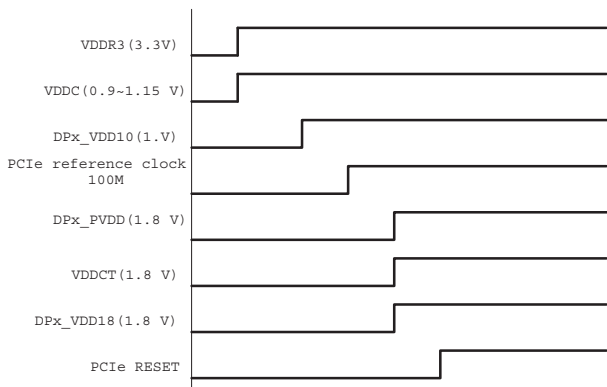
Close DDR3 socket



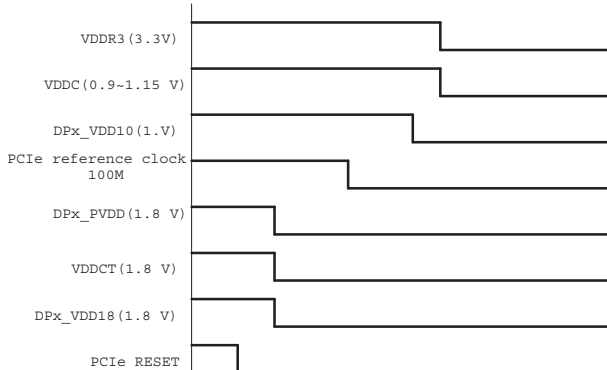


	GPIO20	GPIO15	
	PWRCNTL1	PWRCNTL0	VGA-CORE
L	1	1	0.9V
M	0	1	0.95V
H	1	0	1.12V

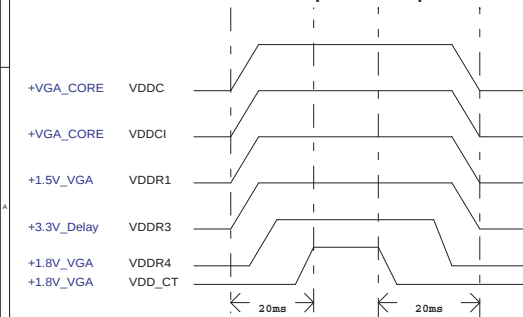




Power-down Sequence



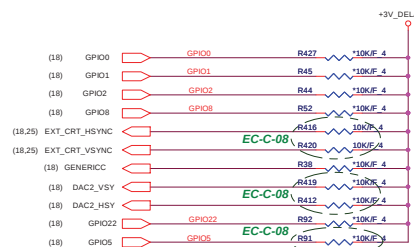
Power Up/Down Sequence

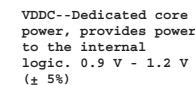


Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS ROM EN is set to 0.

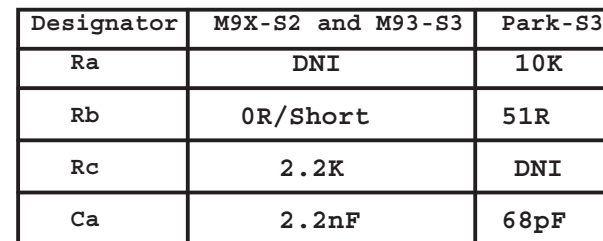
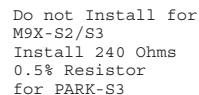
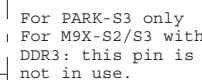
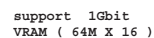




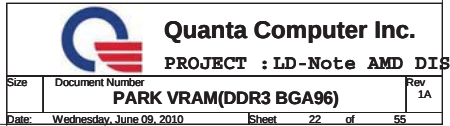
PCIE VDDC--PCI-E
Digital Power
Supply (Either 1.0
V or 1.1 V) 1.0 V
-5% to 1.1 V +5%

Quanta Computer Inc.

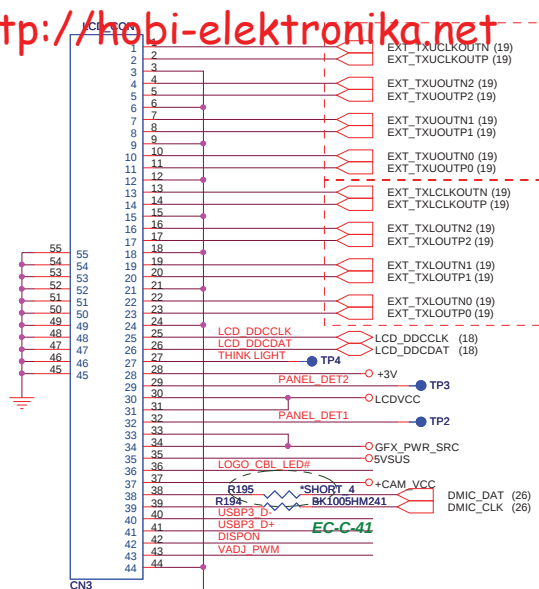
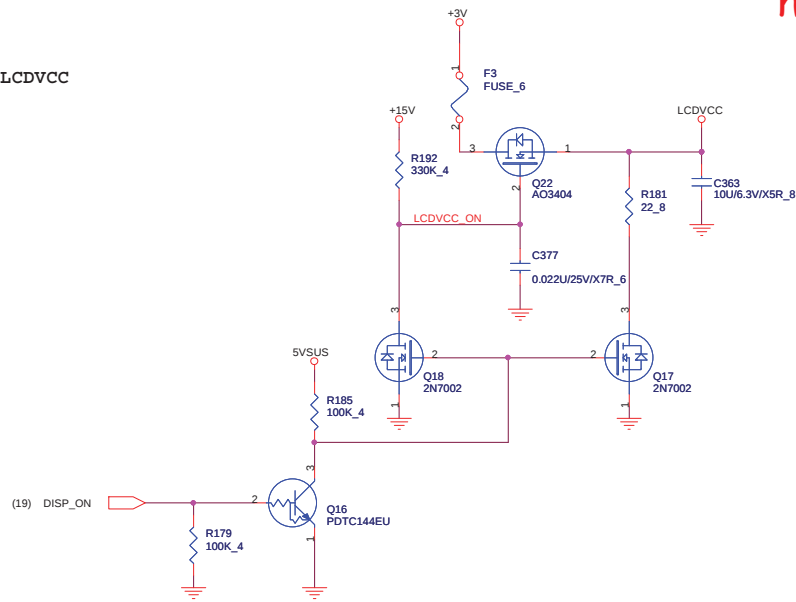
PROJECT :LD-Note AMD DIS



DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R



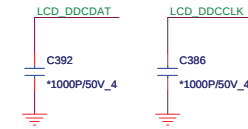
LCDVCC



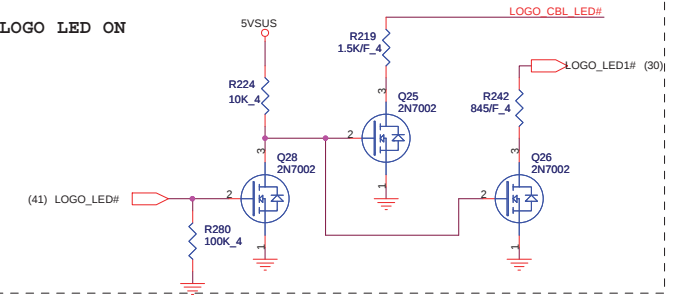
Address : A9H --Contrast
AAH --Backlight



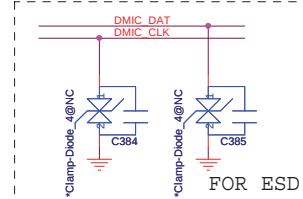
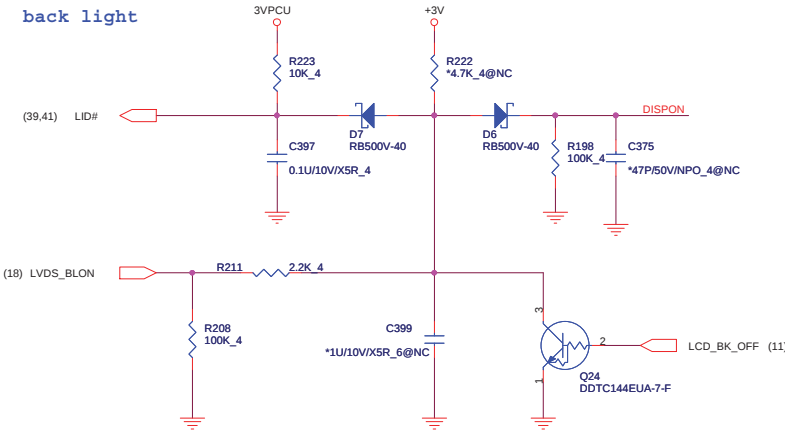
For EMI



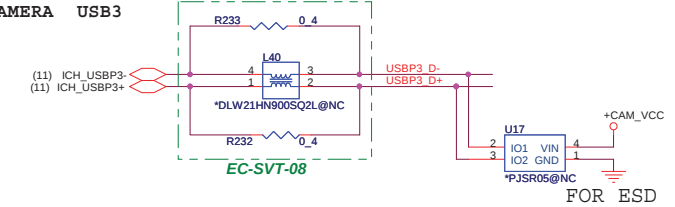
LOGO LED ON



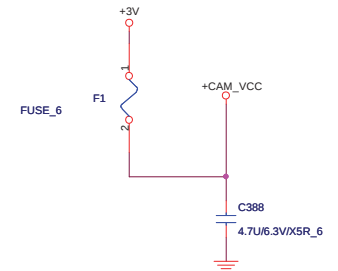
back light

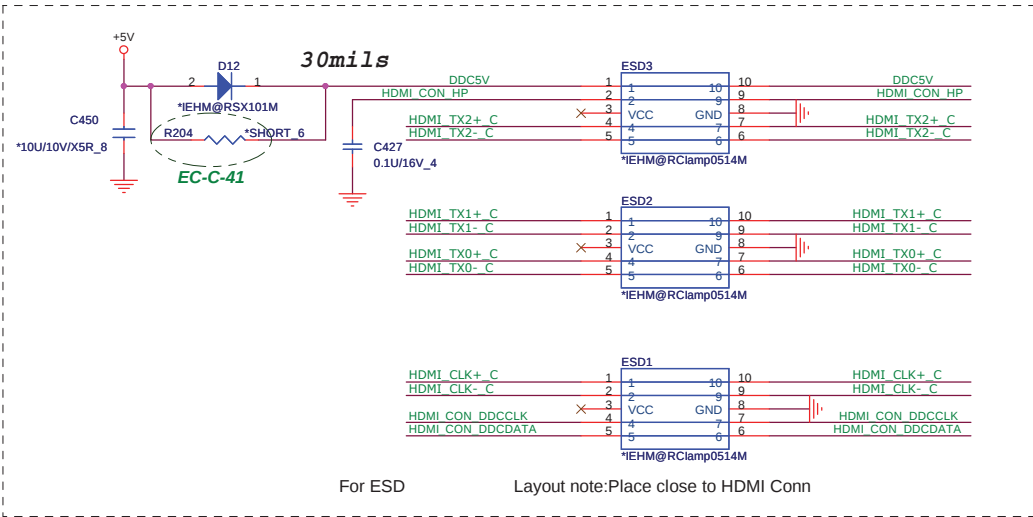
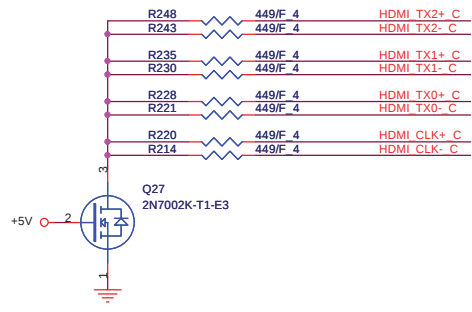
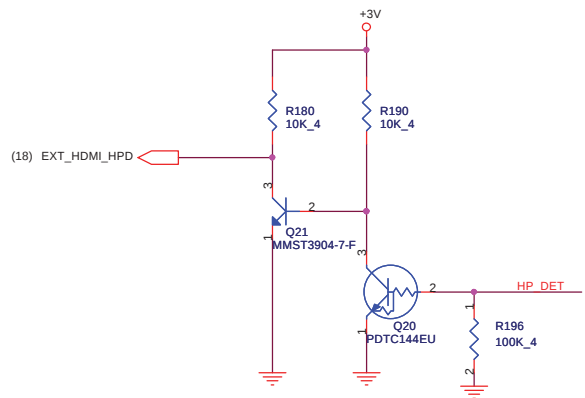
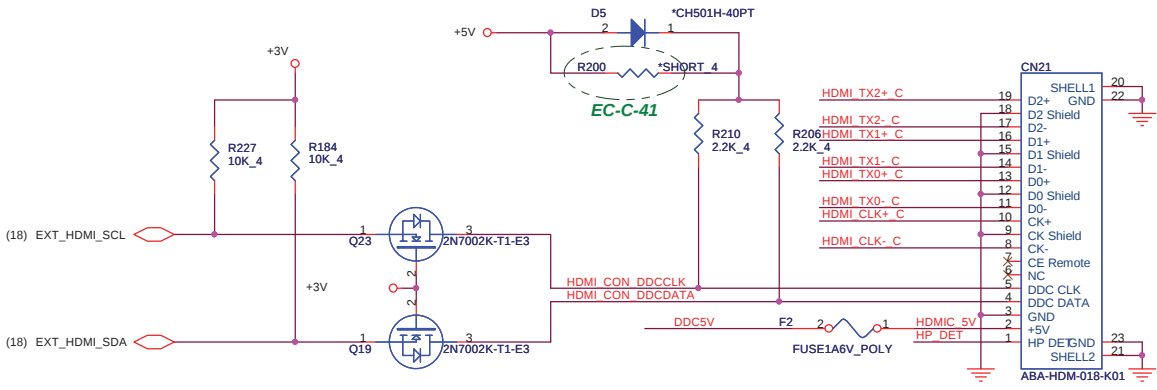
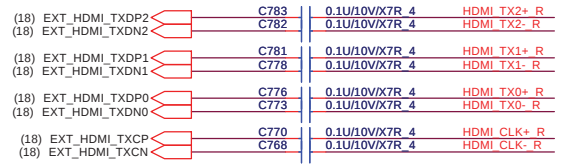
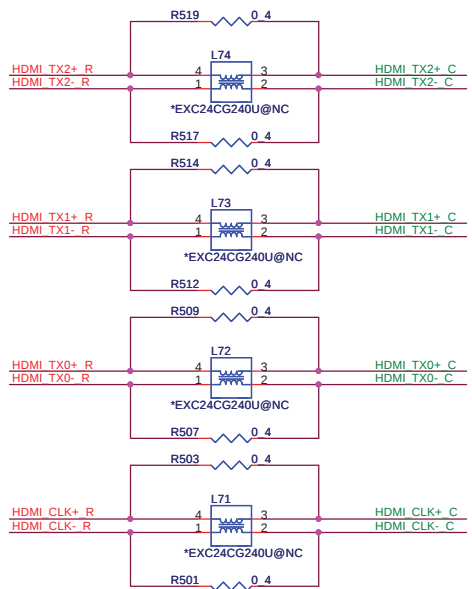


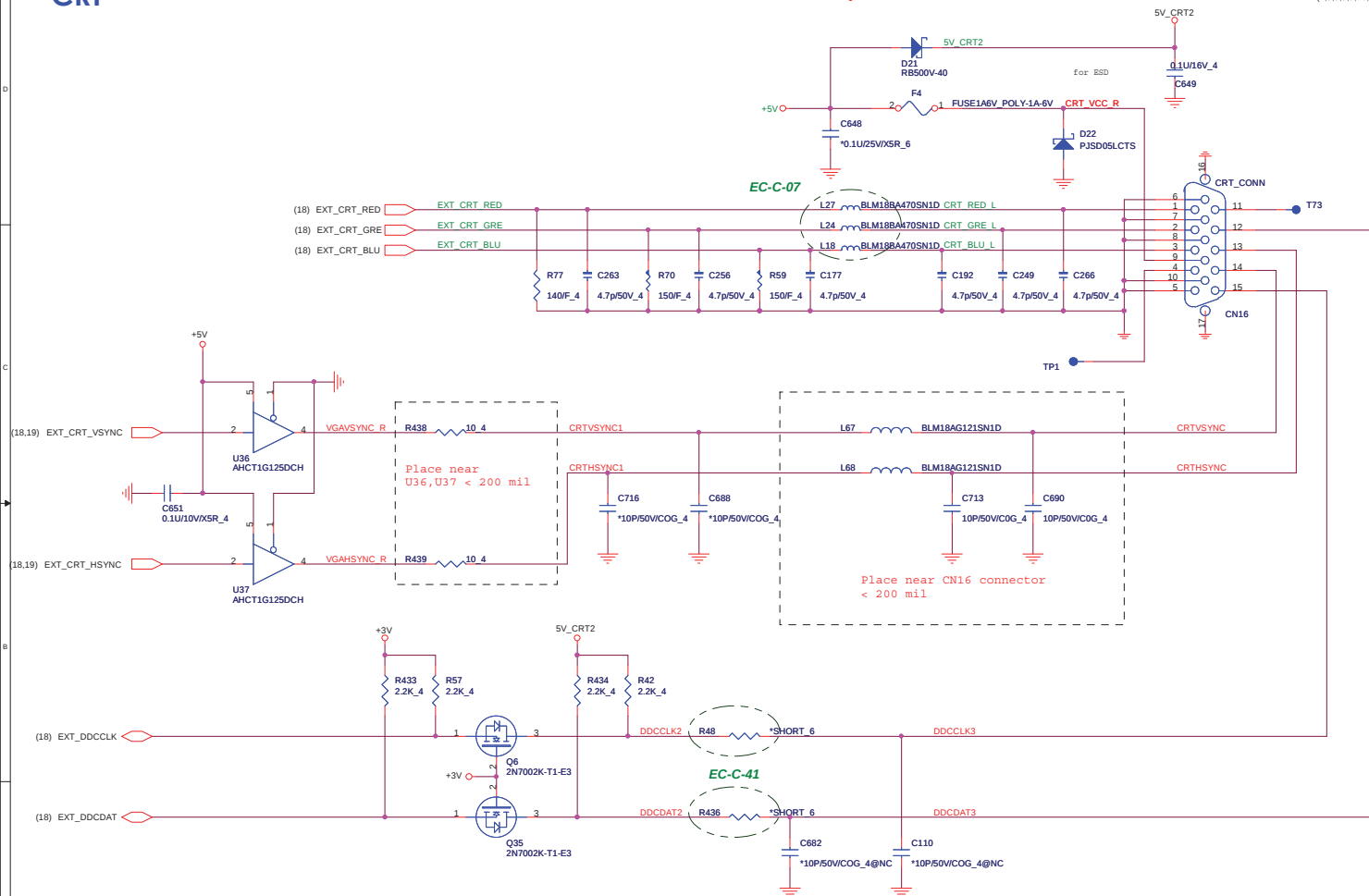
CAMERA USB3



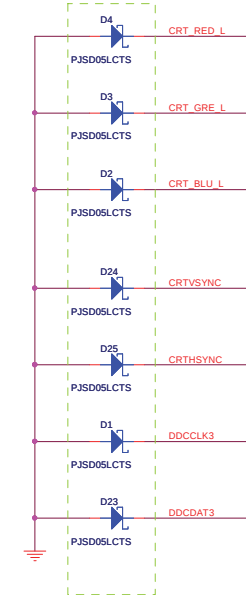
CAMERA VCC Control







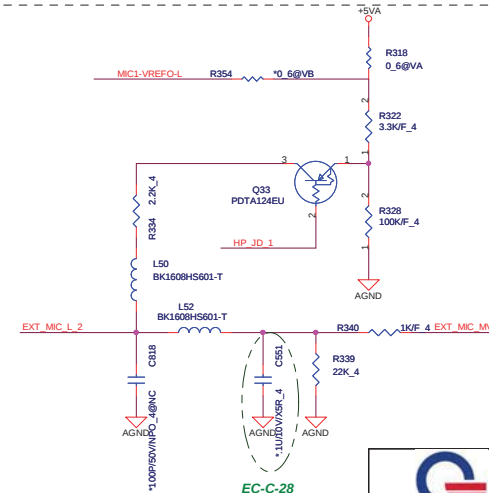
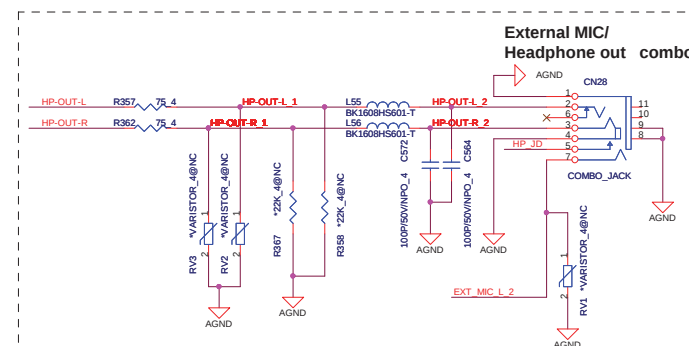
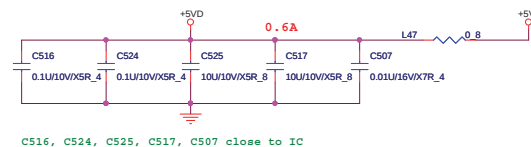
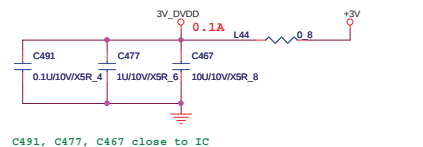
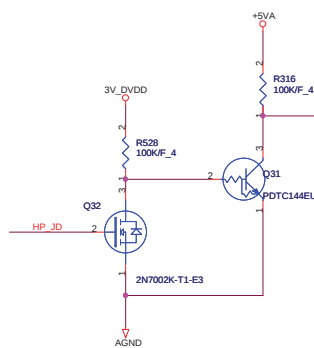
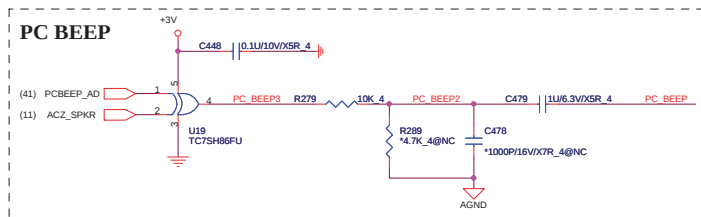
ESD PROTECTION



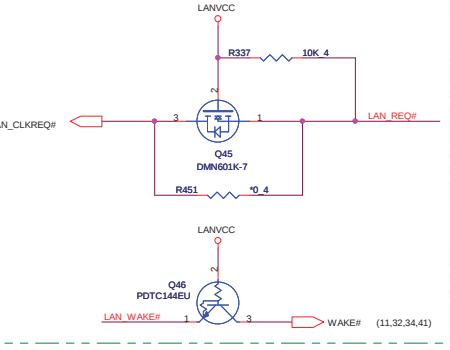
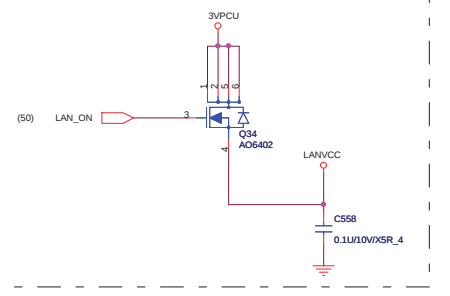
EC-C-41



Analog

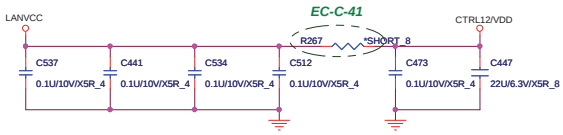


LANVCC



EC-C-26

寬>40mils ,長<200mils

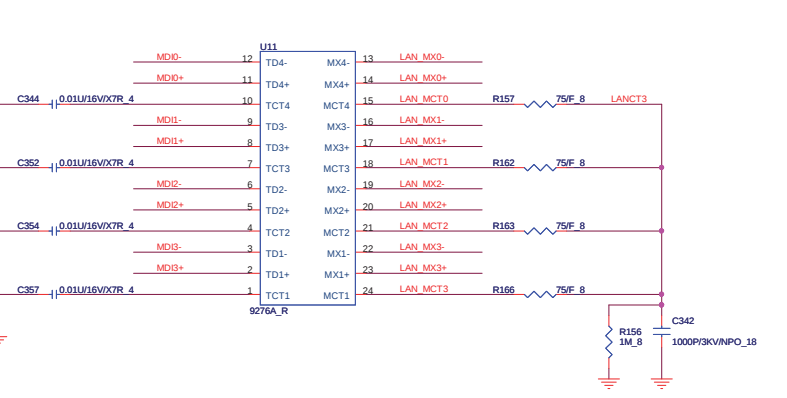


* C537,C441,C534,C512 are for U23 VDD33 pins- 1, 29, 37 and 40.

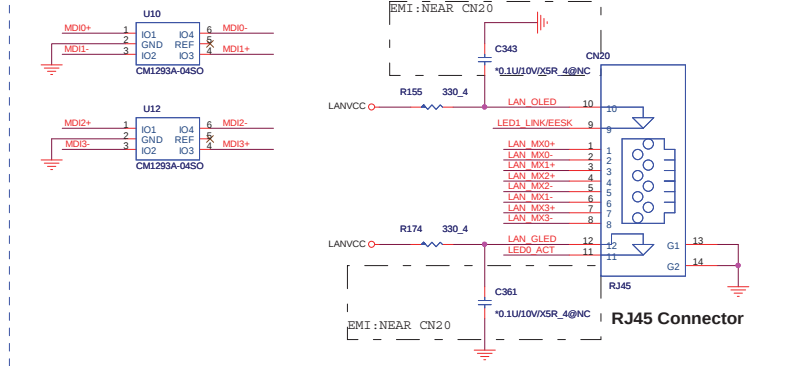
Place C473 ,C447 closed to U23 pins44,45.

Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

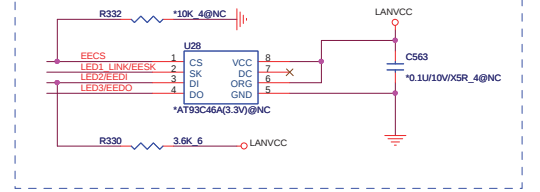
Transformer



RJ45 Connector



EEPROM



EC-C-41

3.3V : Enable switching regulator
0V : Disable switching regulator

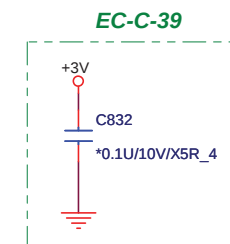
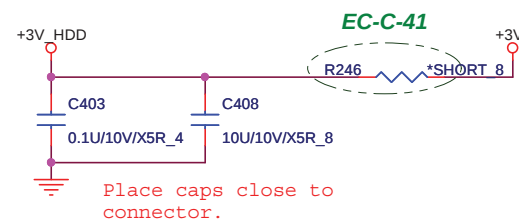
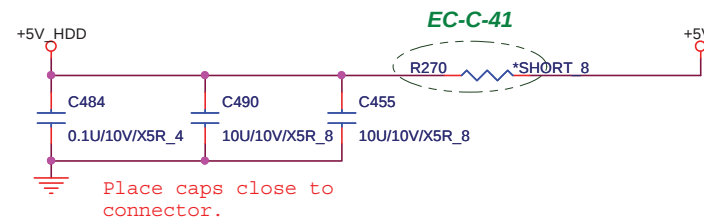
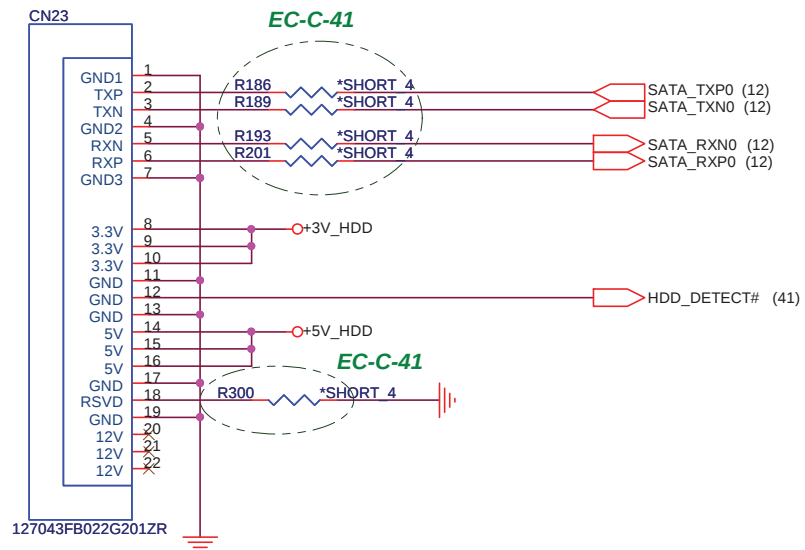
* C497 and C424 are for U23 EVDD12 pin 19.

* C440,C439,C538,C475,C539 are for U23 VDD12 pins- 10, 13, 30, 36, 39.

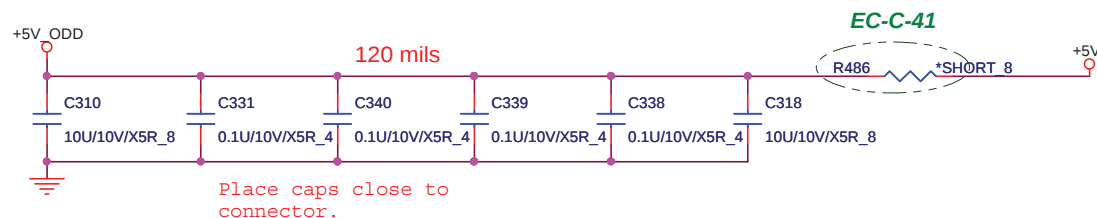
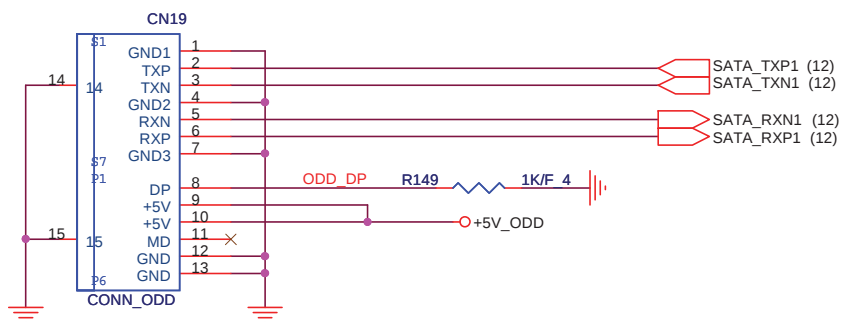
SATA HDD Connector.



28



ODD Connector

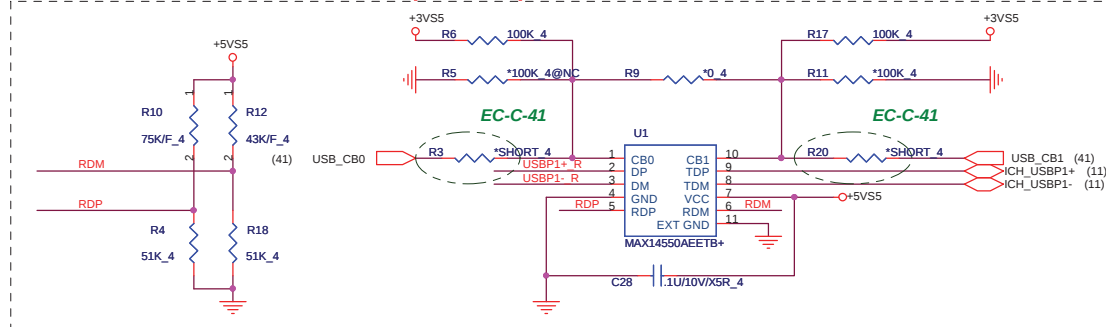


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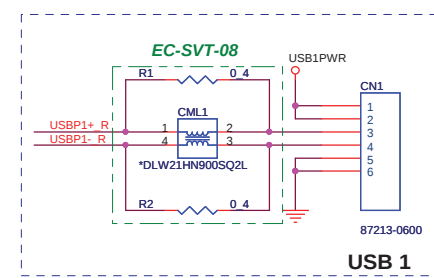
PROJECT :LD-Note AMD DIS

Size	Document Number	Rev 1A
SATA (HDD&CD_ROM)		
Date:	Wednesday, June 09, 2010	Sheet 28 of 55

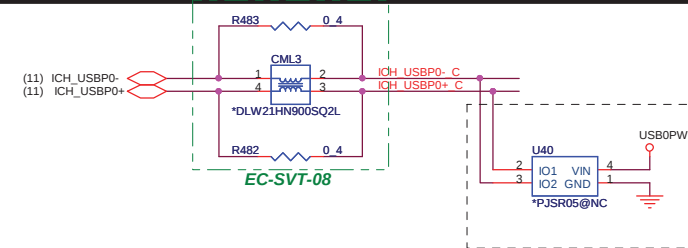
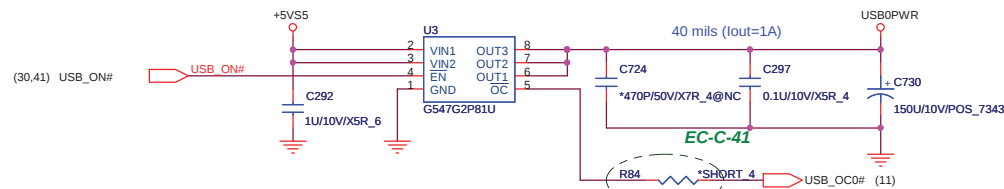
Support Black-berry function



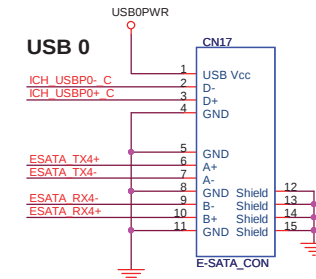
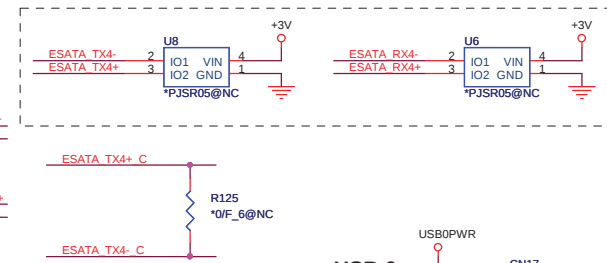
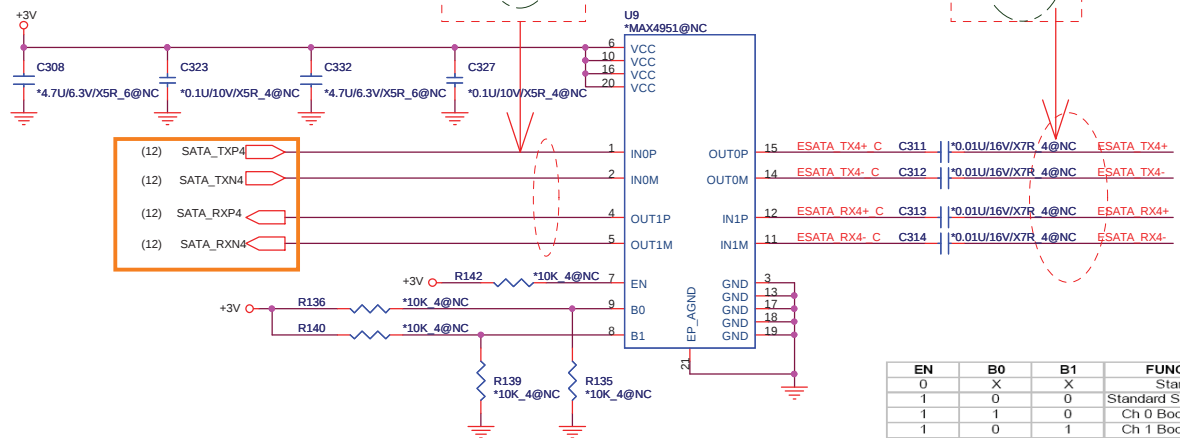
USB X1---> Wire to board conn



USB + E-SATA

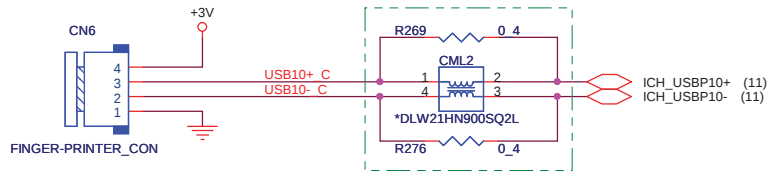


E-SATA RE-DRIVER

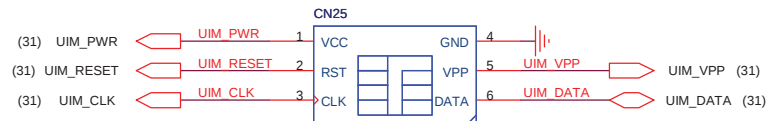


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

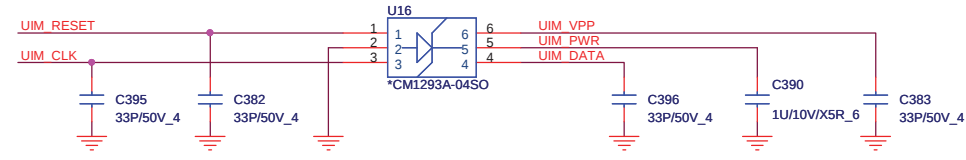
Finger Print



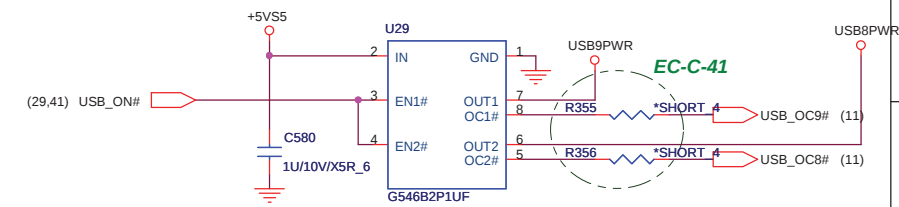
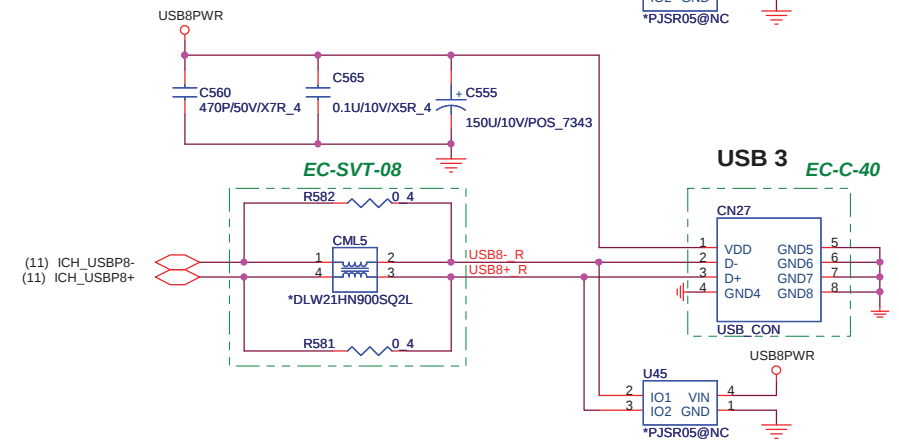
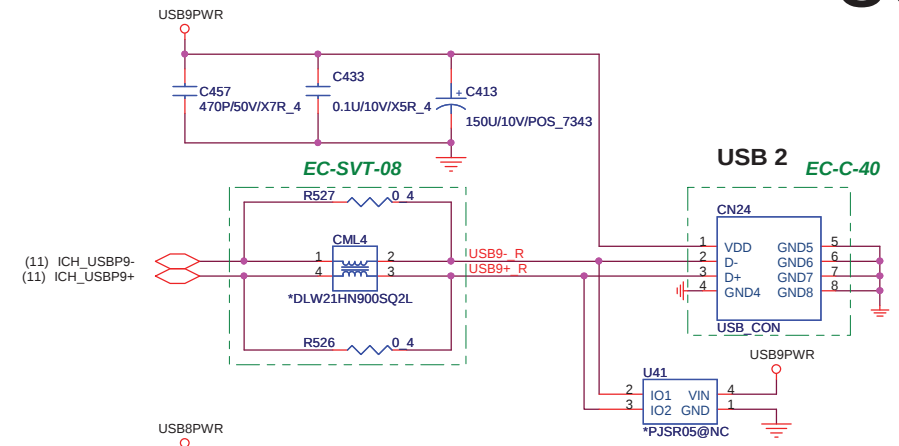
SIM Card CONN



Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible

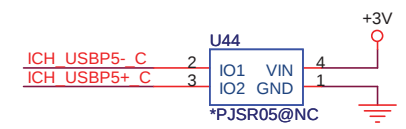
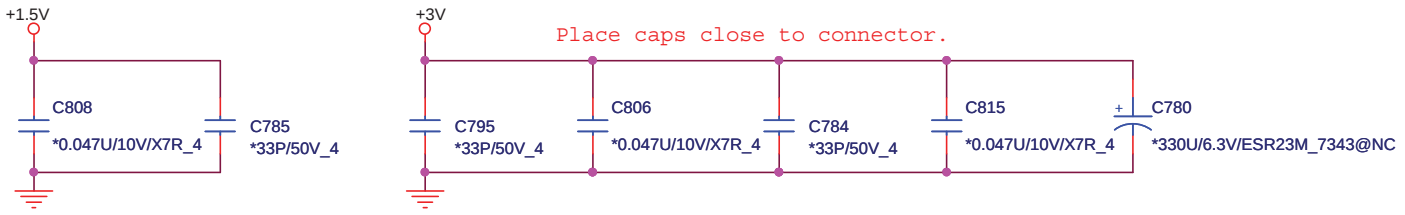
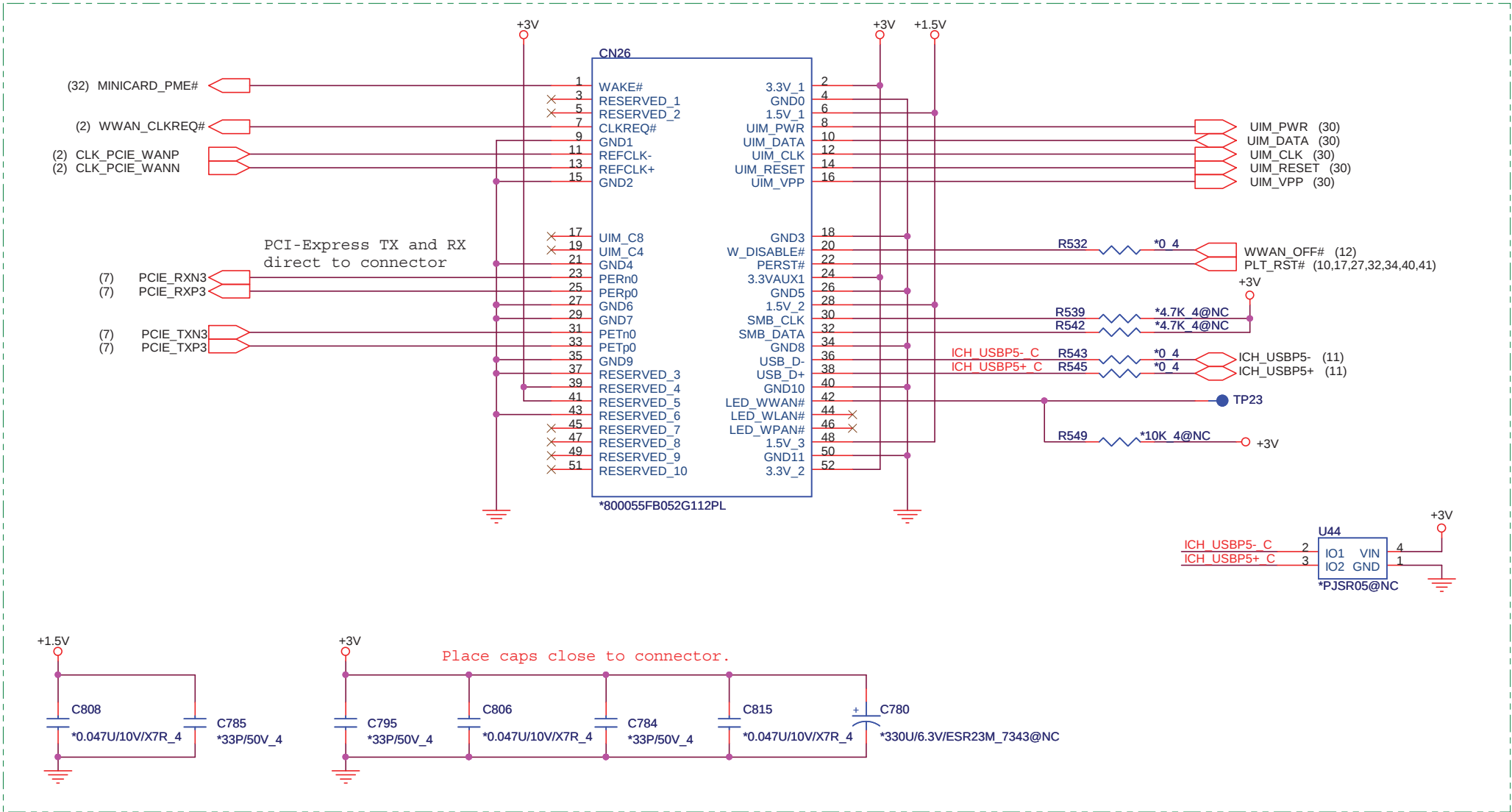


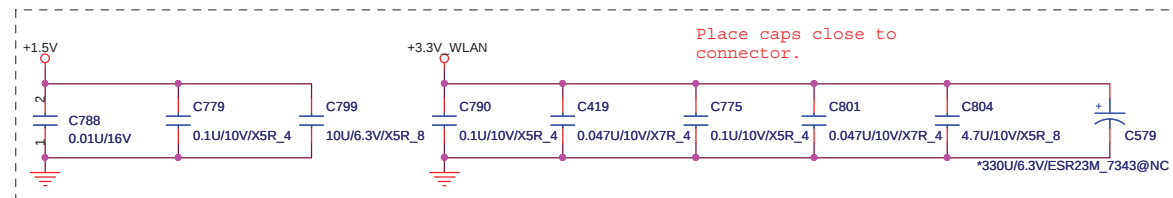
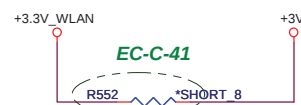
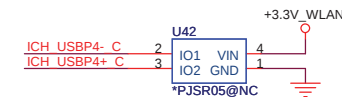
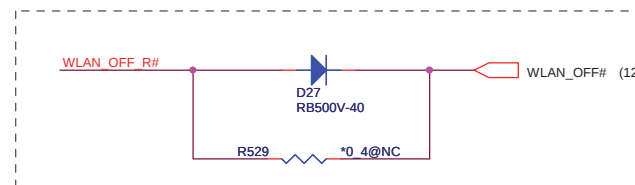
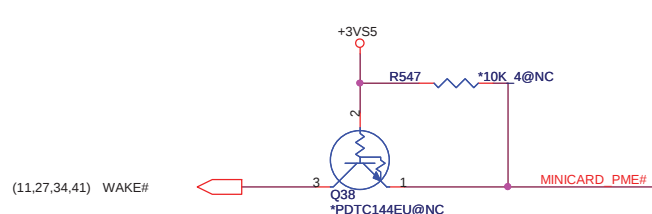
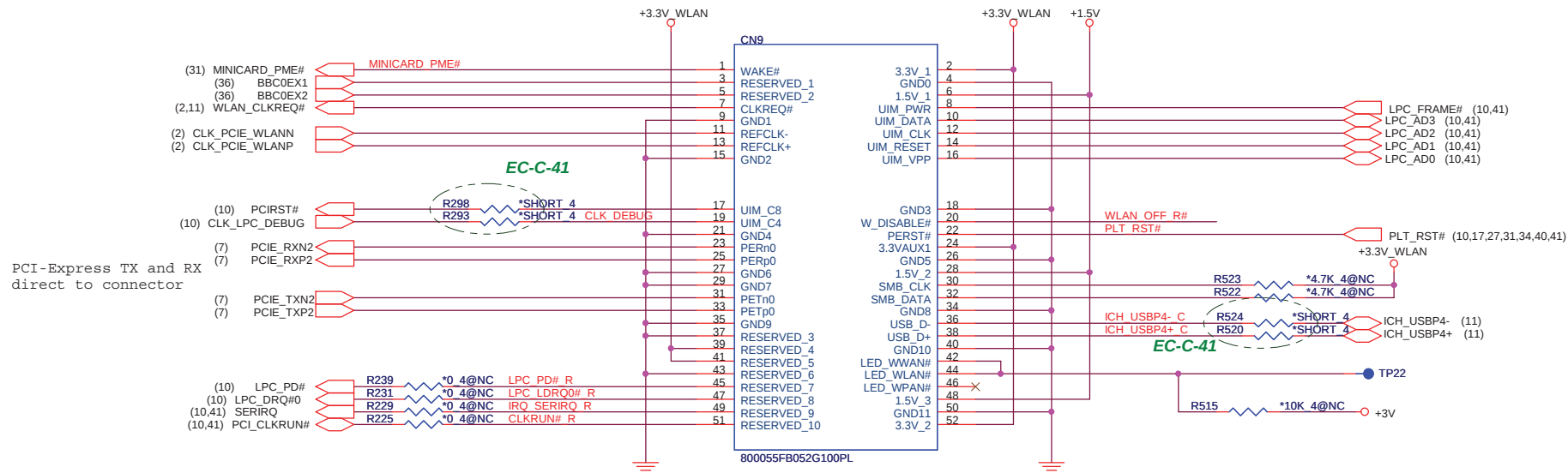
FRONT LEDs

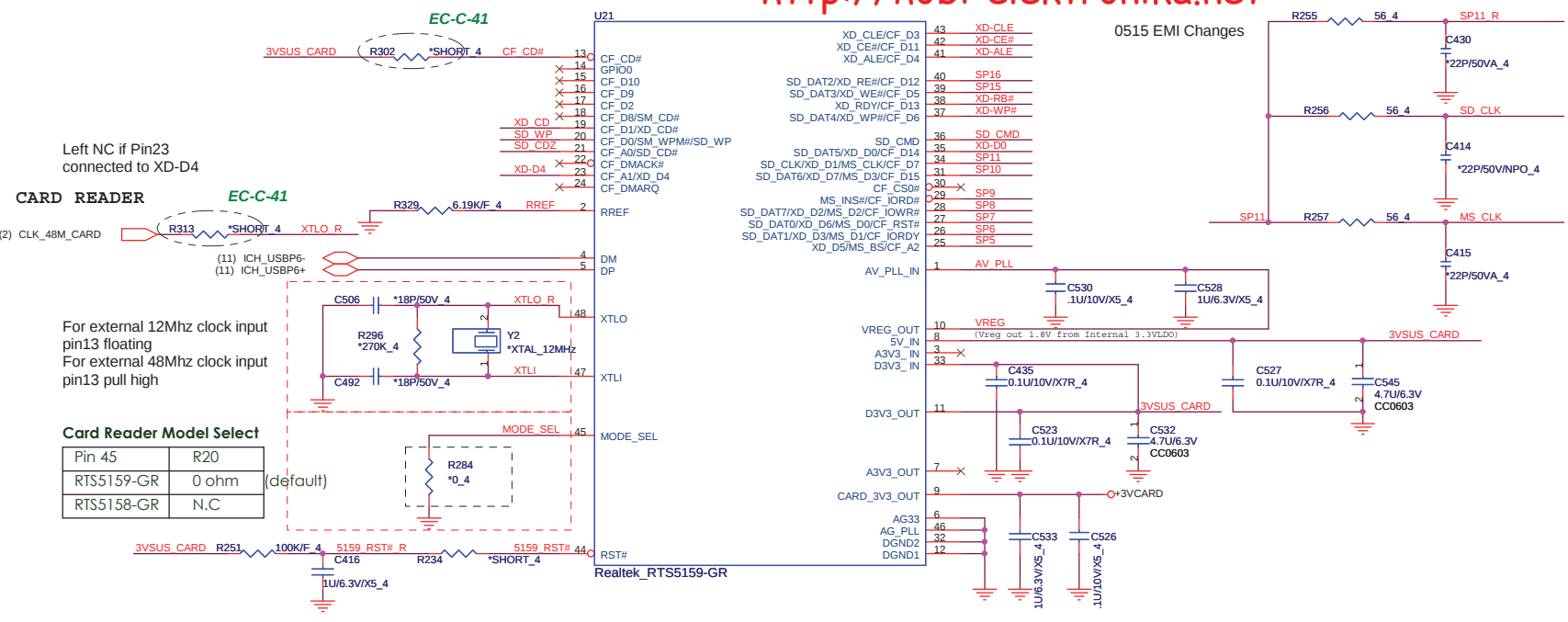


MiniCard WWAN connector

EC-C-30



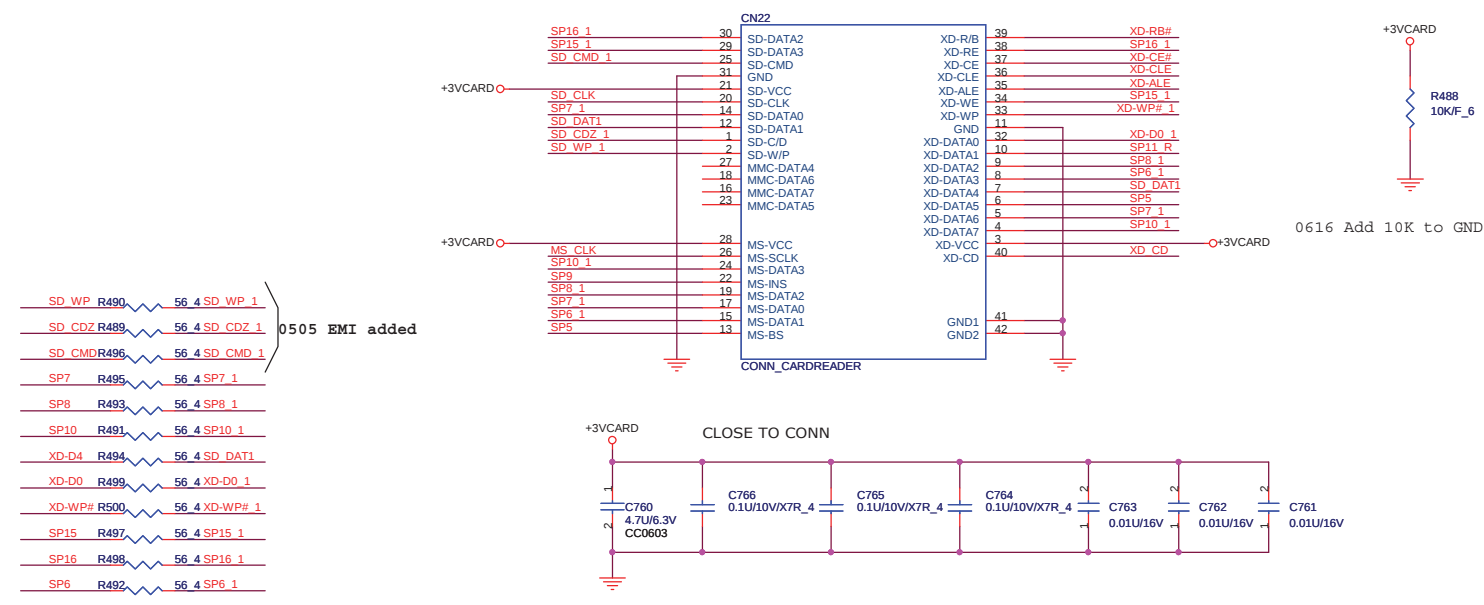




Note:

SD/MMC	MS	XD
SP0		XD CD#
SP1	SD WP	
SP2	SD WP	XD CD#
SP3	SD CD#	
SP4		XD D4
SP5	MS BS	XD D5
SP6	MS D1	XD D3
SP7	SD DAT0	MS D0
SP8	SD DAT7	MS D2
SP9	MS INS#	
SP10	SD DAT6	MS D3
SP11	SD CLK	MS SCLK
SP12	SD DAT5	XD D0
SP13	SD DAT4	XD WP#
SP14		XD R/B#
SP15	SD DAT3	XD WE#
SP16	SD DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE

7 in 1 Socket (MS, MS PRO, SD, MMC, xD)



Express Card

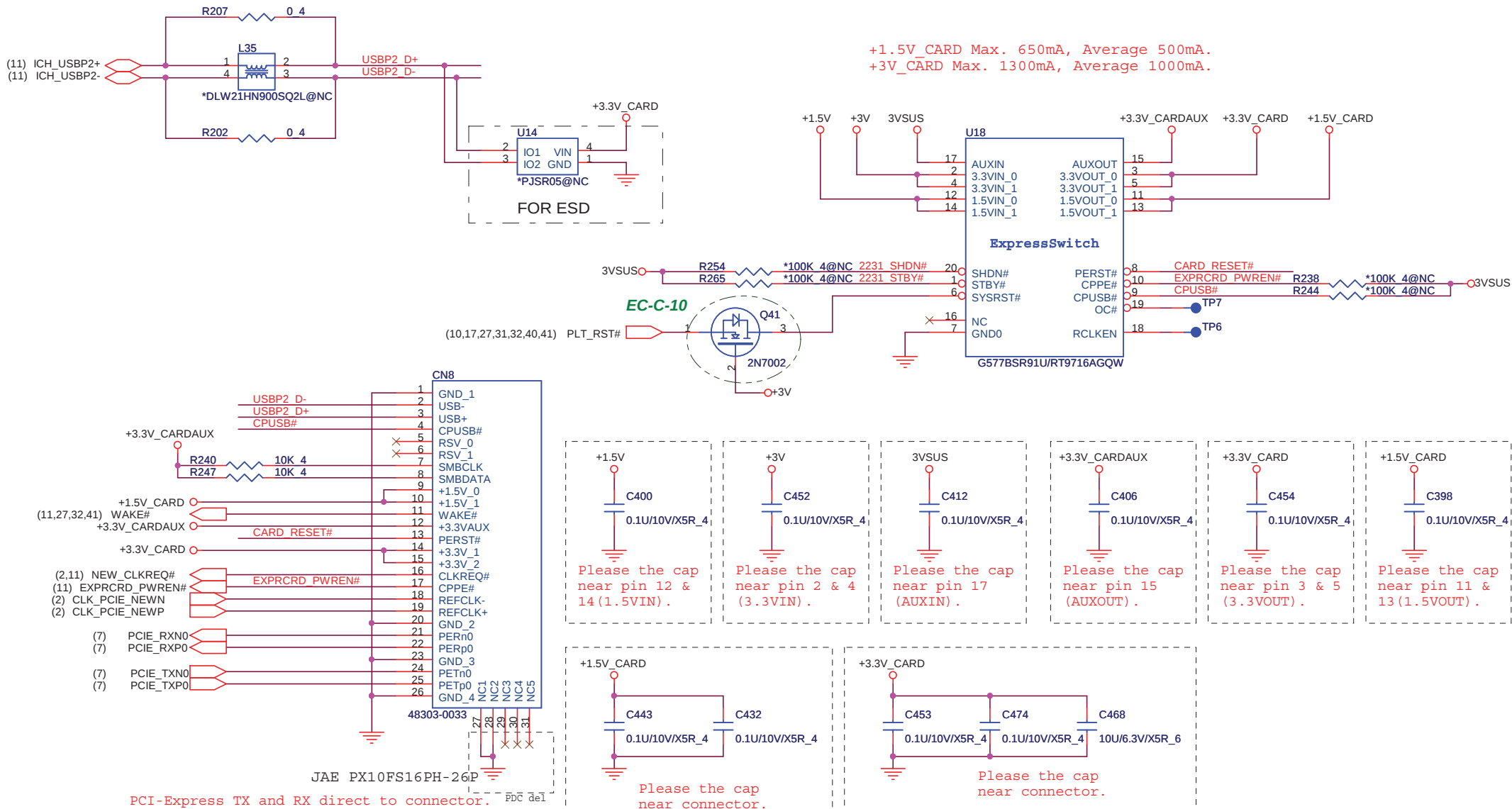
<http://hobi-elektronika.net>

(2,3,9,10,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,32,36,37,40,41,46,47,50)
(3,8,31,32,50)
(30,33,41,46,47,49,50)

+3V
+1.5V
3VSUS

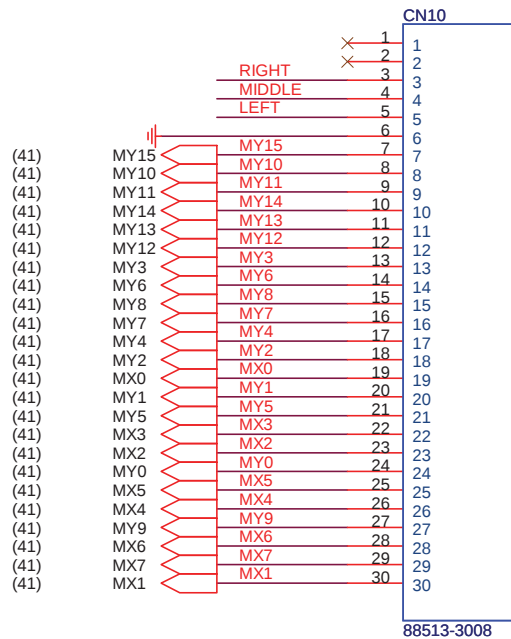


34



KEYBOARD

KEYBOARD connector

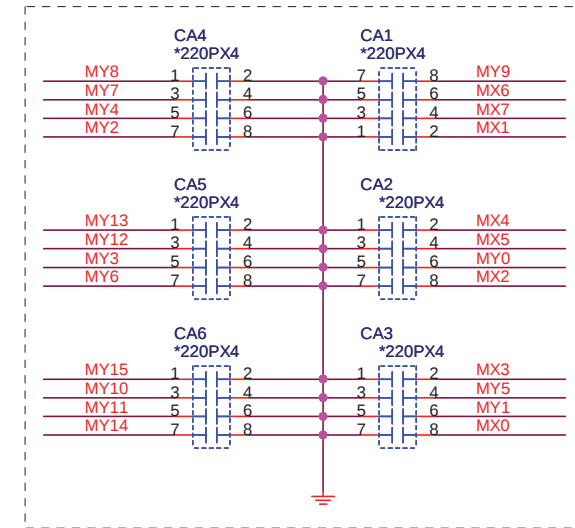
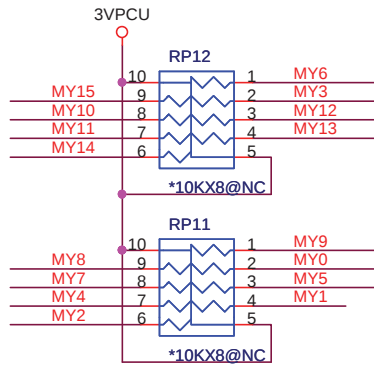


<http://hobi-elektronika.net>

(24,25,26,28,37,38,39,41,50) +5V
(10,23,27,39,41,43,44,45,46,47,48,50) 3VPCU

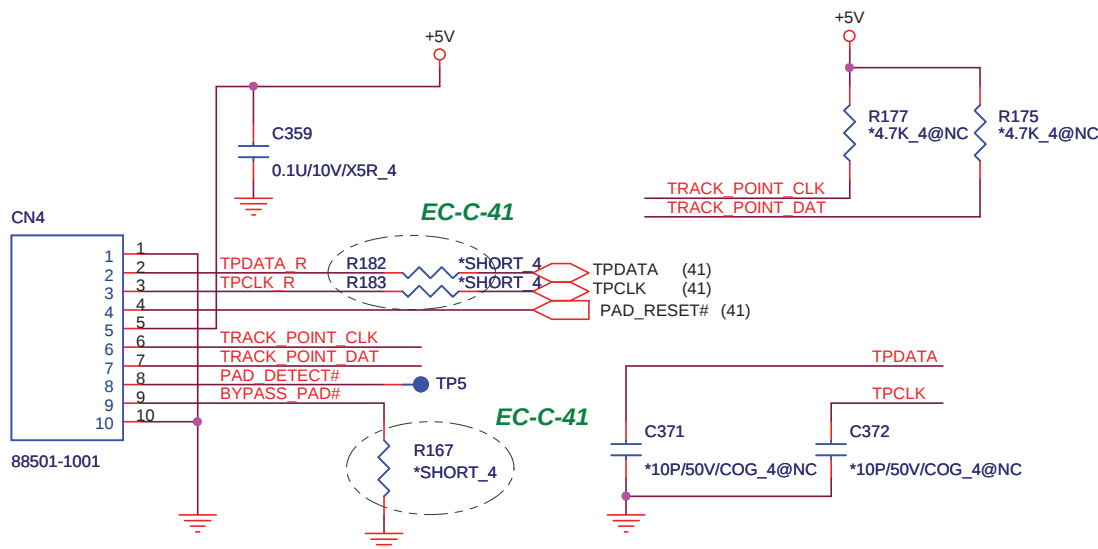


35

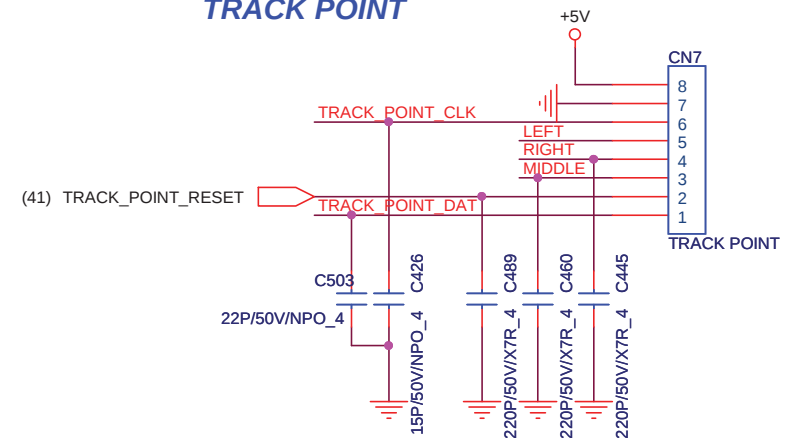


For EMI request

Touch pad



TRACK POINT



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PROJECT :LD-Note AMD DIS

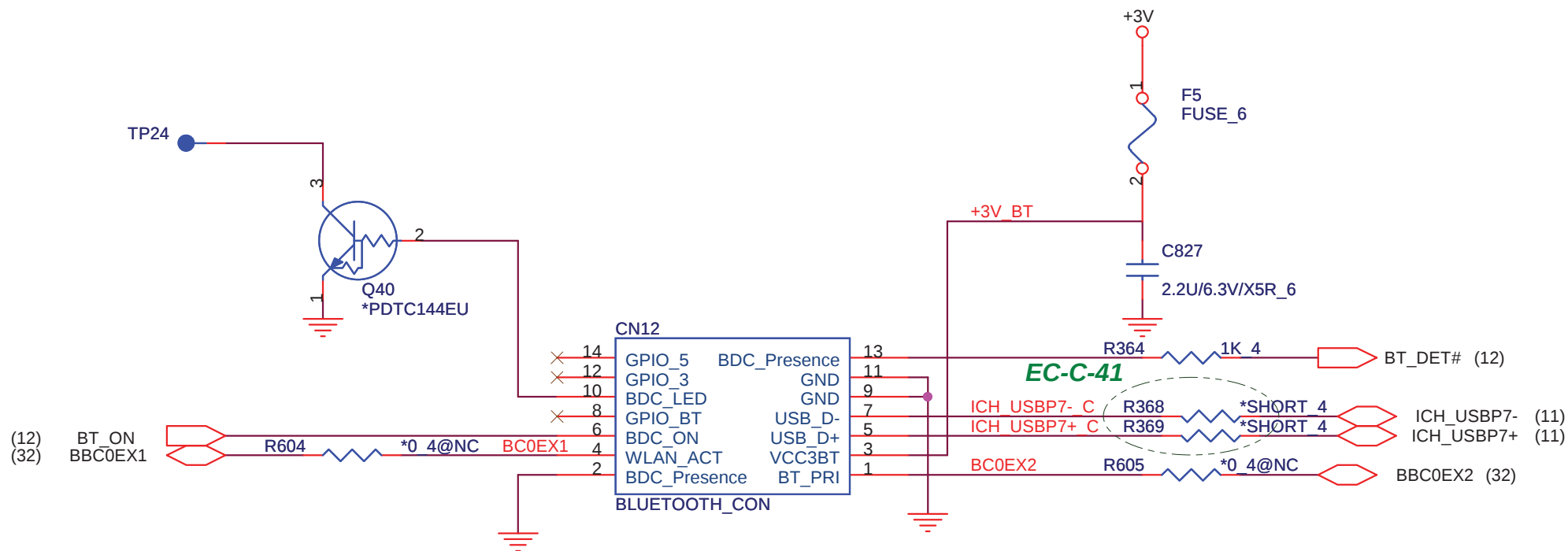
Size	Document Number	Rev
	K/B, T/P	1A
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BLUETOOTH

<http://hobi-elektronika.net>
(2,3,5,8,9,10,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,32,34,37,40,41,46,47,50)

+3V

36

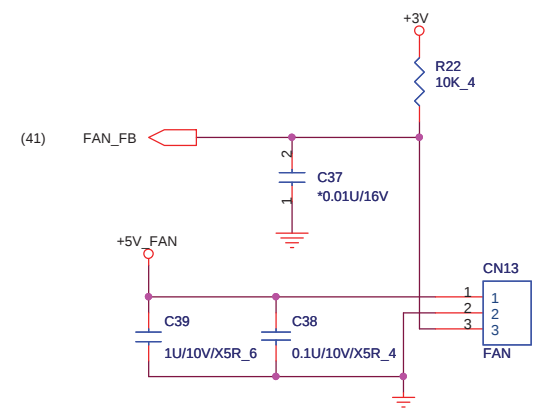
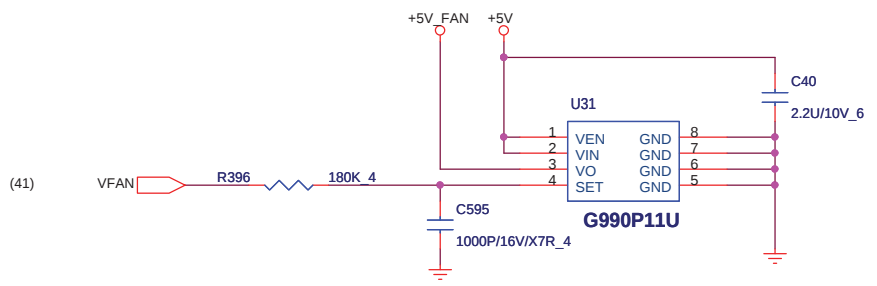


Quanta Computer Inc.

PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	B/T	1A
Date:	Wednesday, June 09, 2010	Sheet 36 of 55

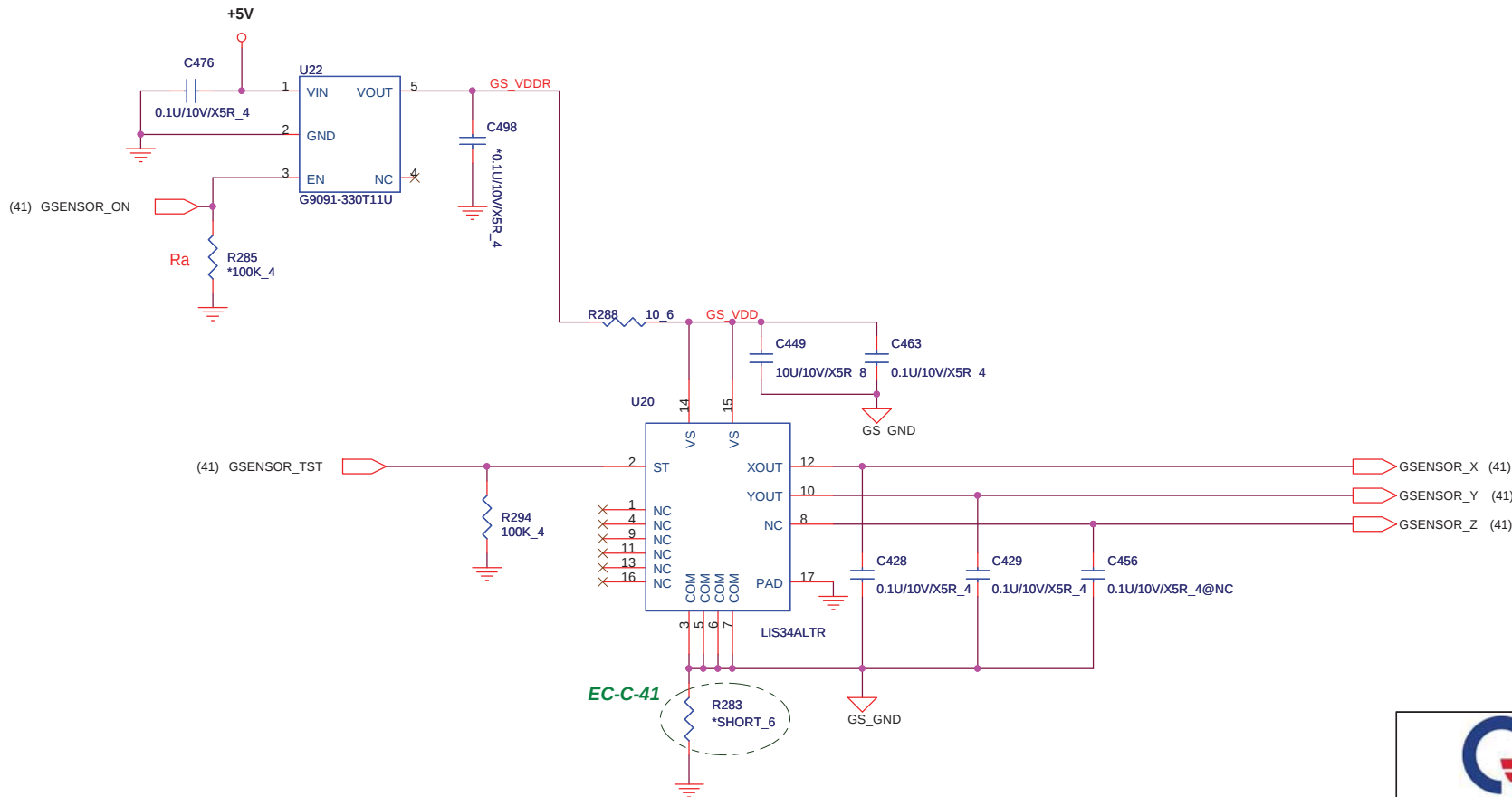
FAN CONTROL



G-SENSOR (3-Axial)

<http://hobi-elektronika.net>

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PROJECT : LD-Note AMD DIS

Size	Document Number	Rev
	G-SENSOR	1A
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FFC TO B LED RIGHT SIDE CONNECTOR

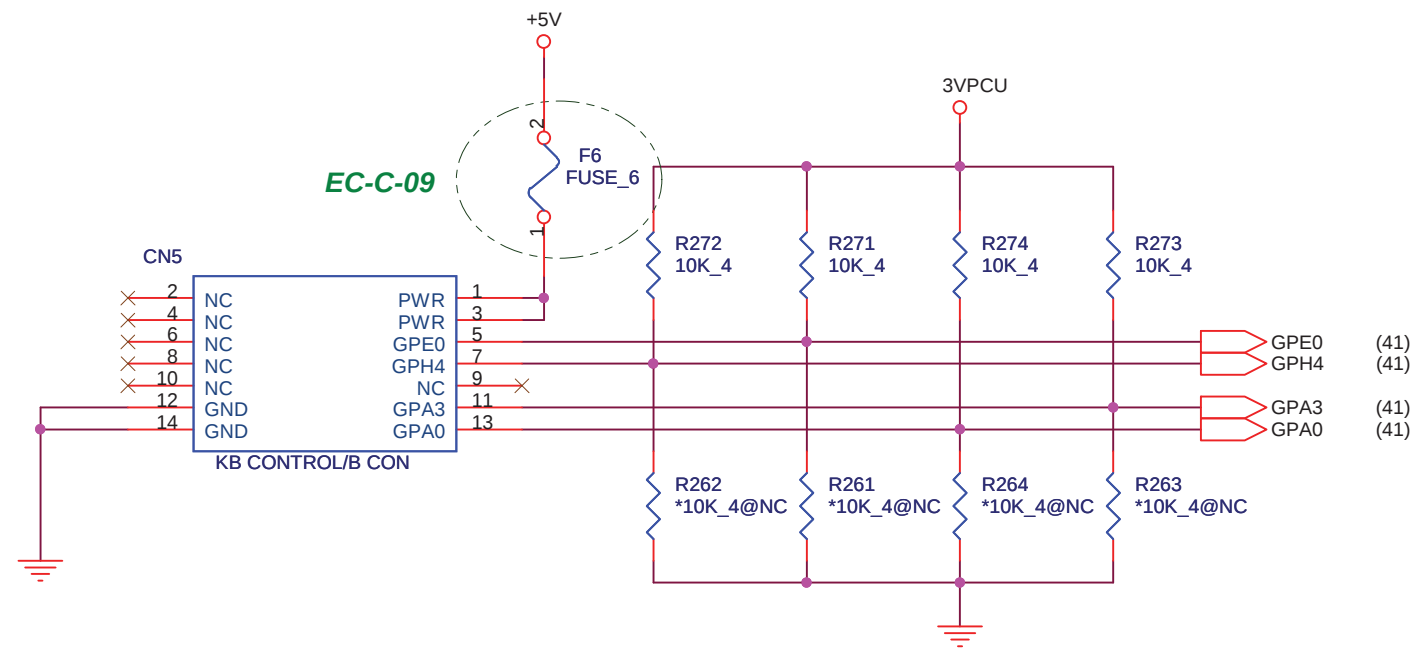
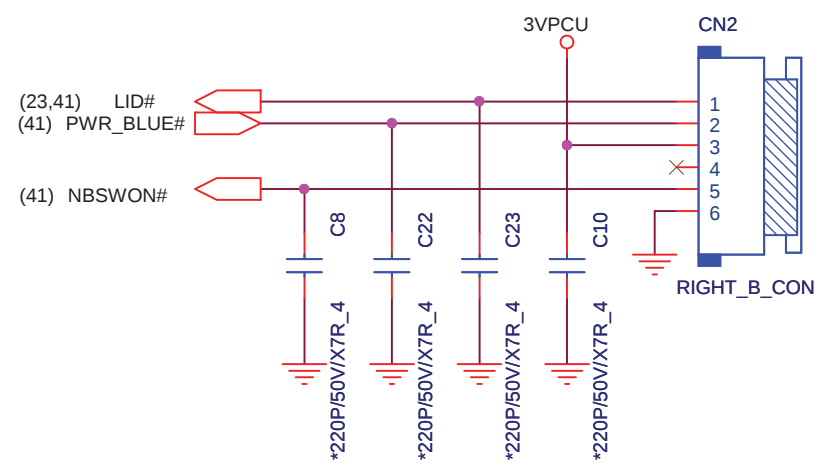
<http://hobi-elektronika.net>

(10,23,27,35,41,43,44,45,46,47,48,50)

3VPCU



39

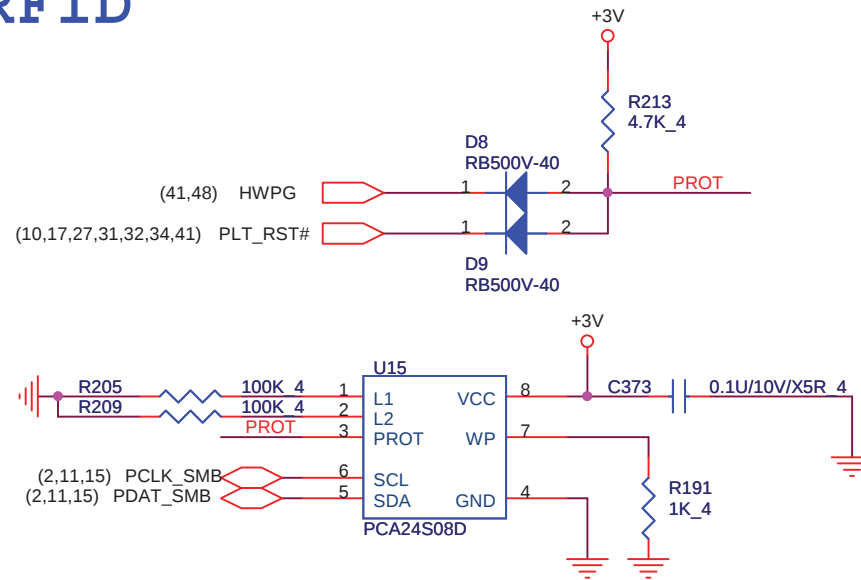




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PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	B TO B CON	1A
Date:	Wednesday, June 09, 2010	Sheet 39 of 55

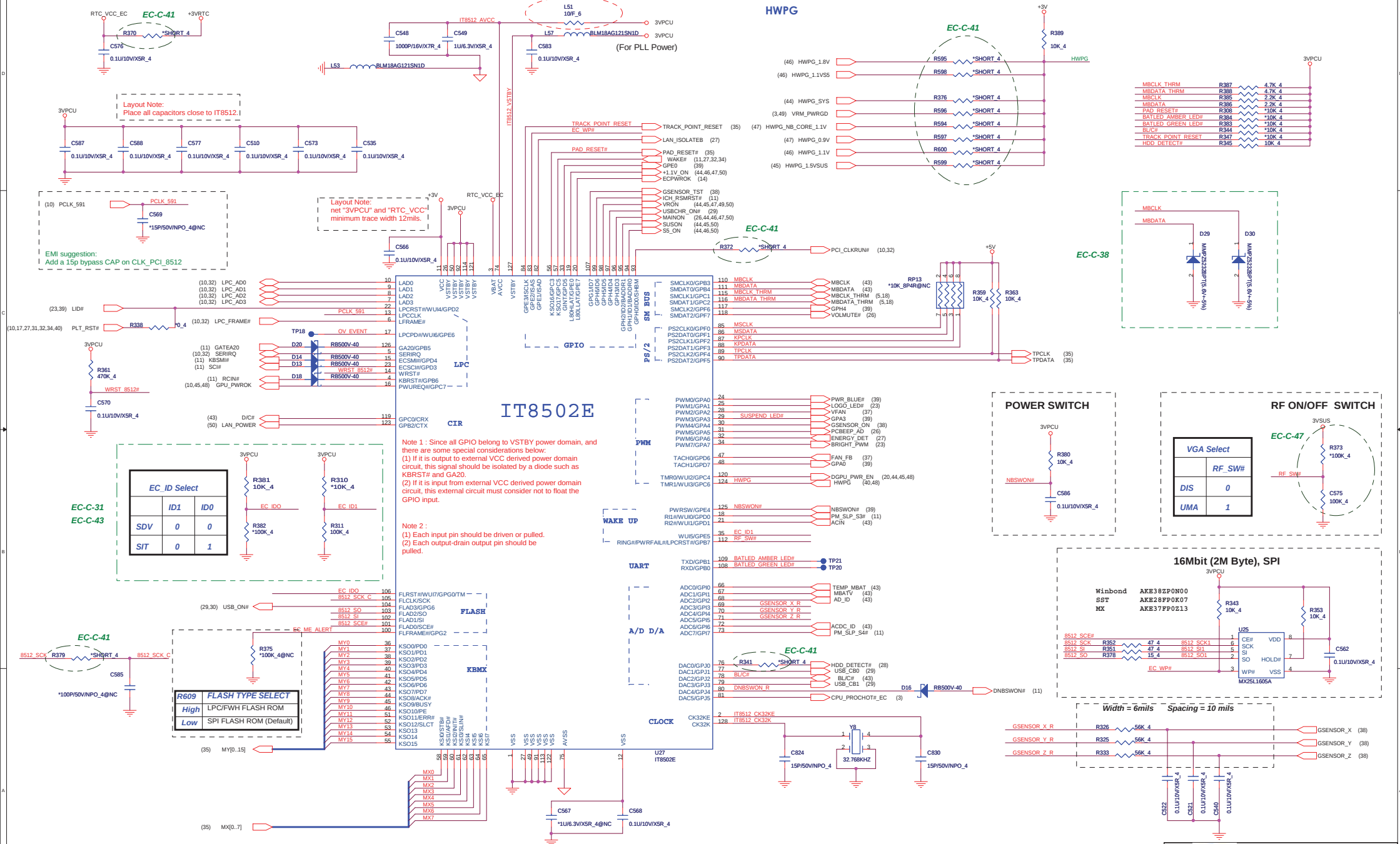
RFID



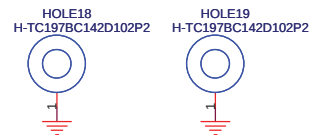
Quanta Computer Inc.

PROJECT :LD-Note AMD DIS

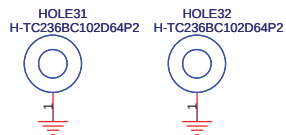
Size	Document Number	Rev 1A
	RFID EEPROM	
Date:	Wednesday, June 09, 2010	Sheet 40 of 55



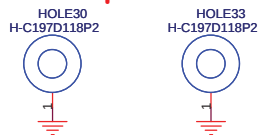
MiniCard WLAN



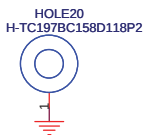
MiniCard WWAN



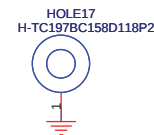
Hole for SB support



Bluetooth

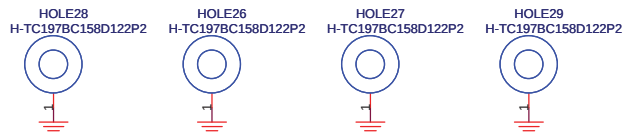


E/L KB nut



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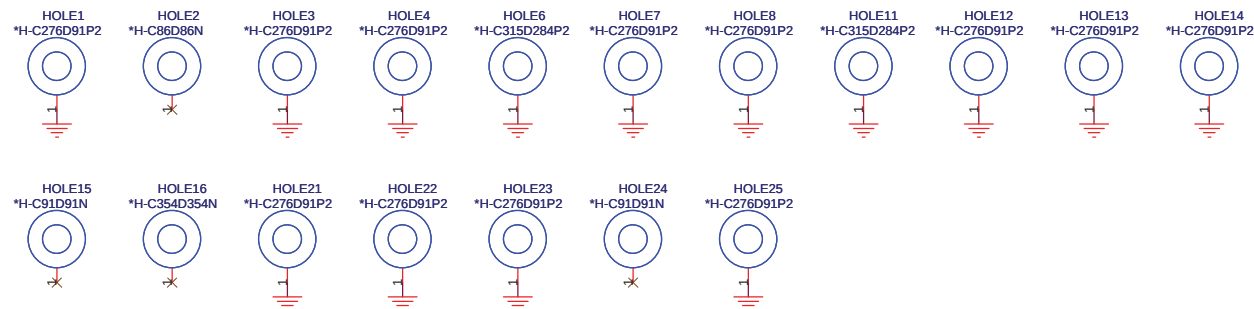
VGA NUT



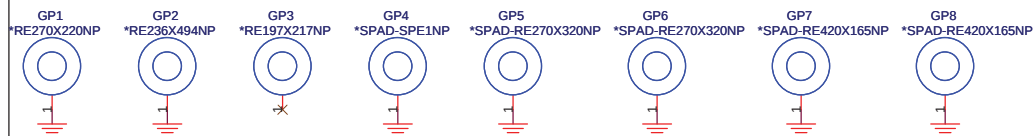
Hole for CPU support



Boundary Hole



PAD



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Size Document Number

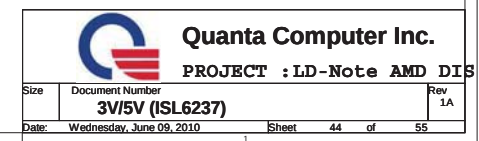
HOLD & SKEW

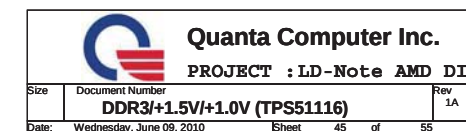
Rev
1A

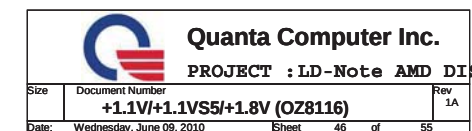
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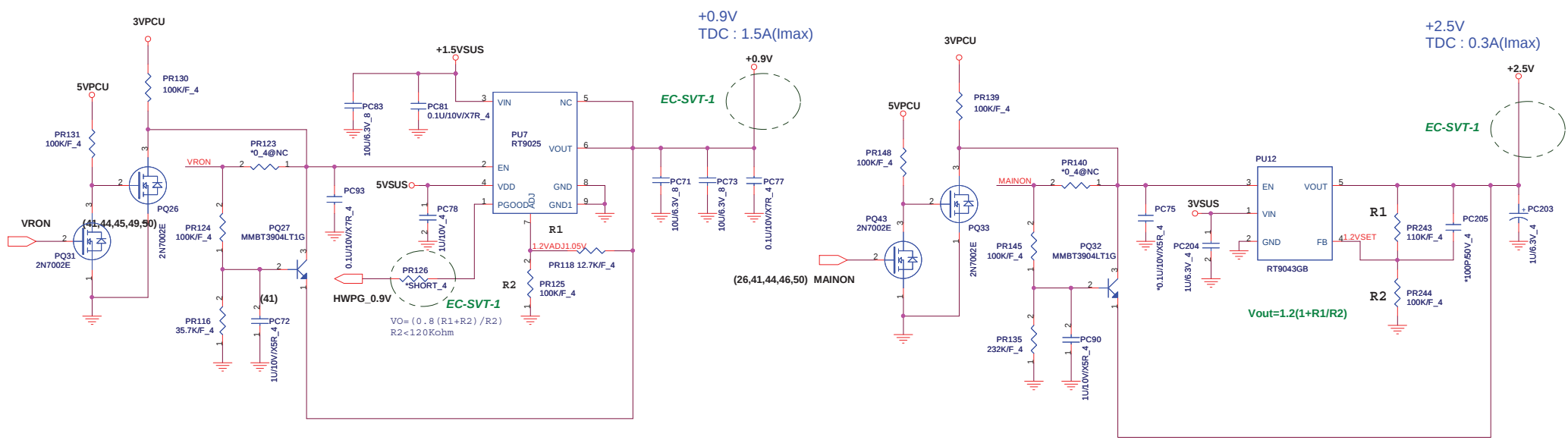
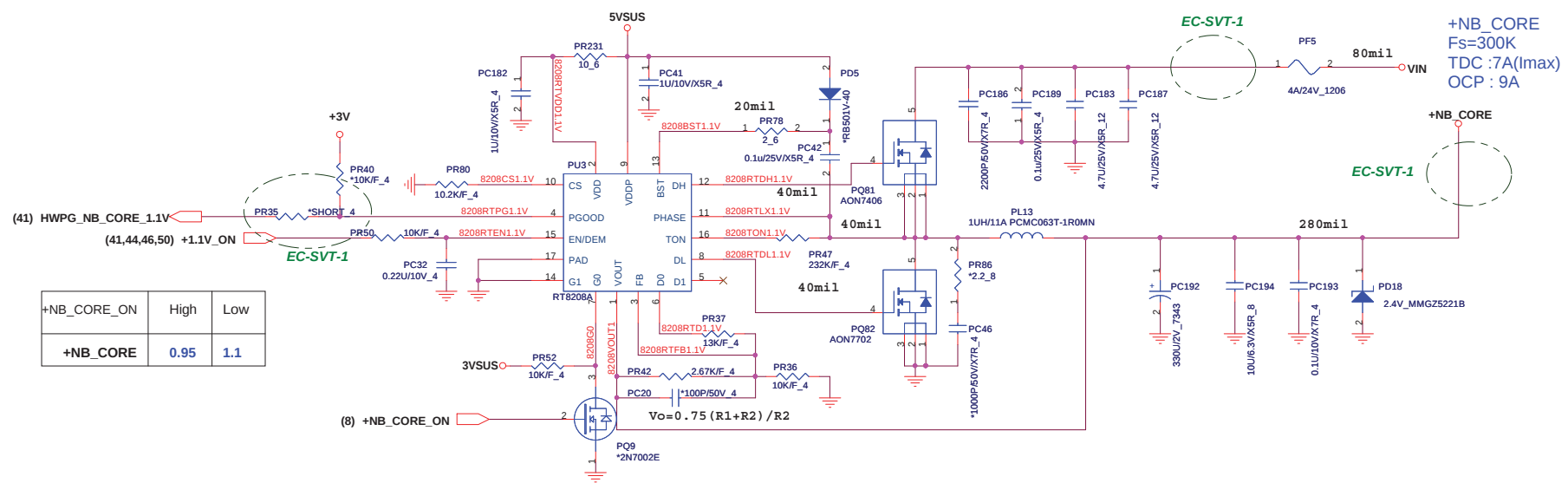
Sheet 42 of 55







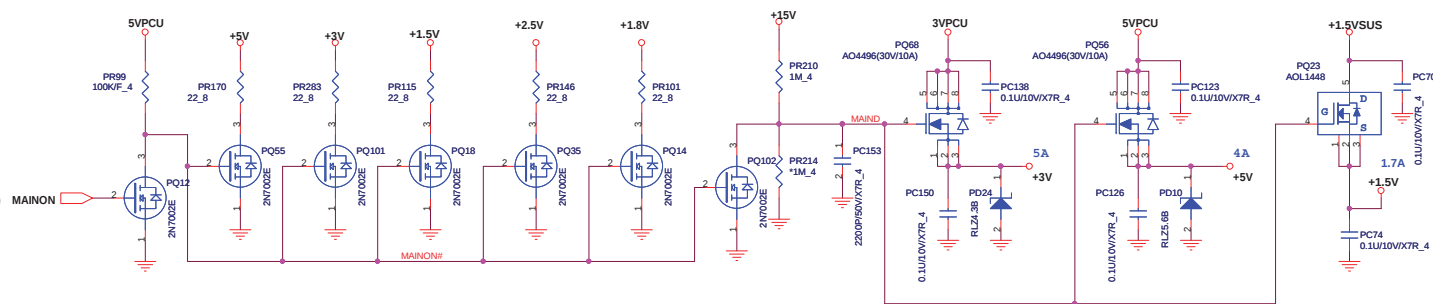




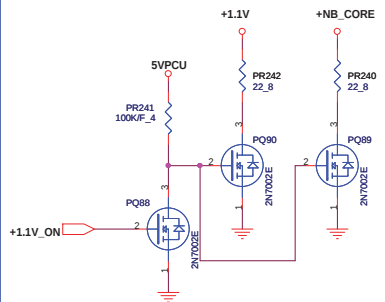
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



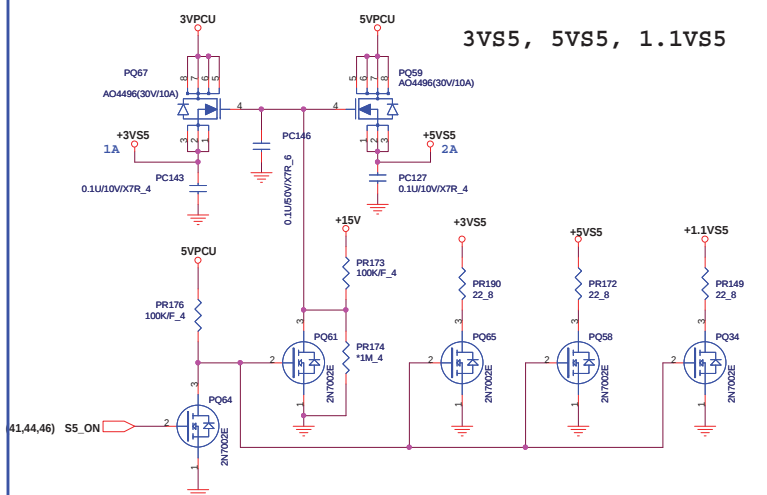
+3V, +5V, +2.5V, +1.8V, +1.5V



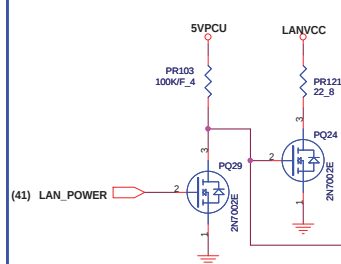
+1.1V, +NB_CORE



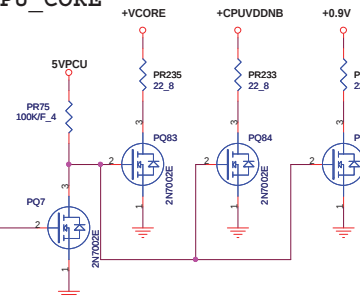
3VS5, 5VS5, 1.1VS5



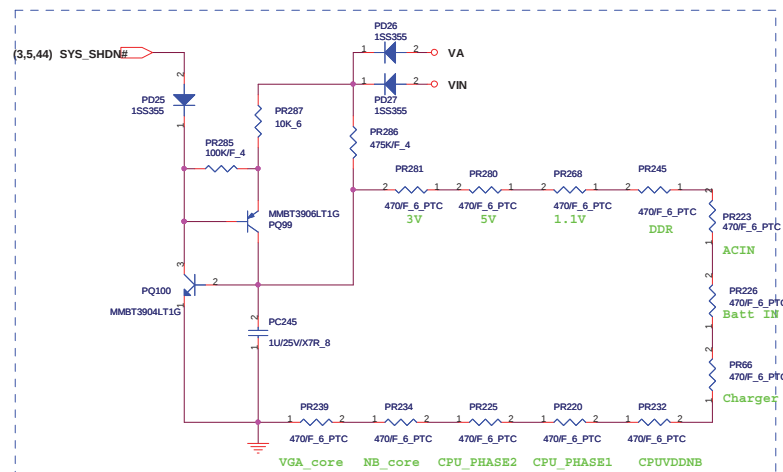
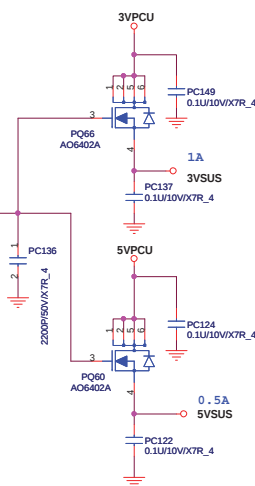
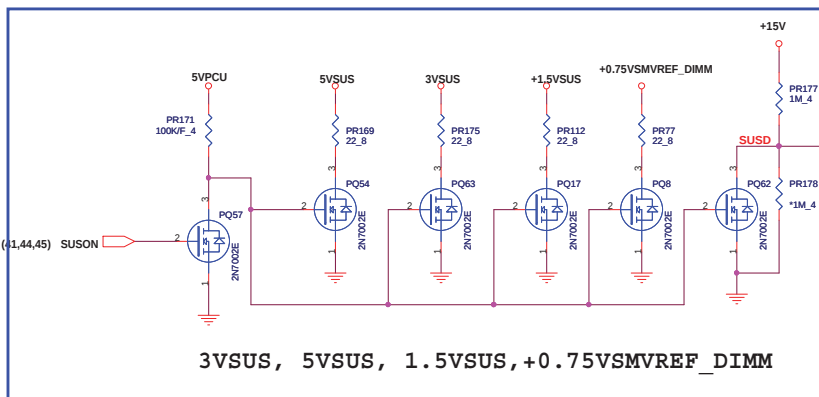
LANVCC

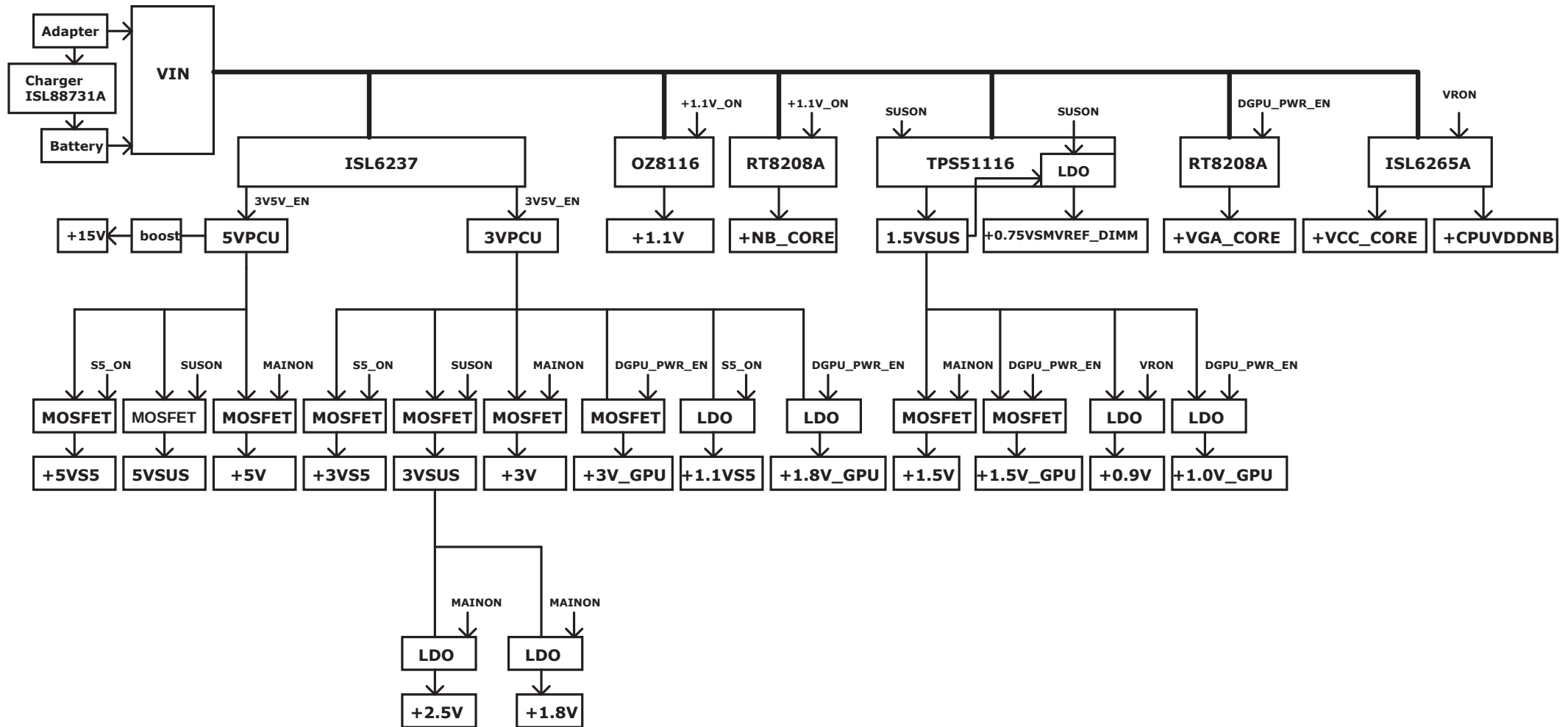


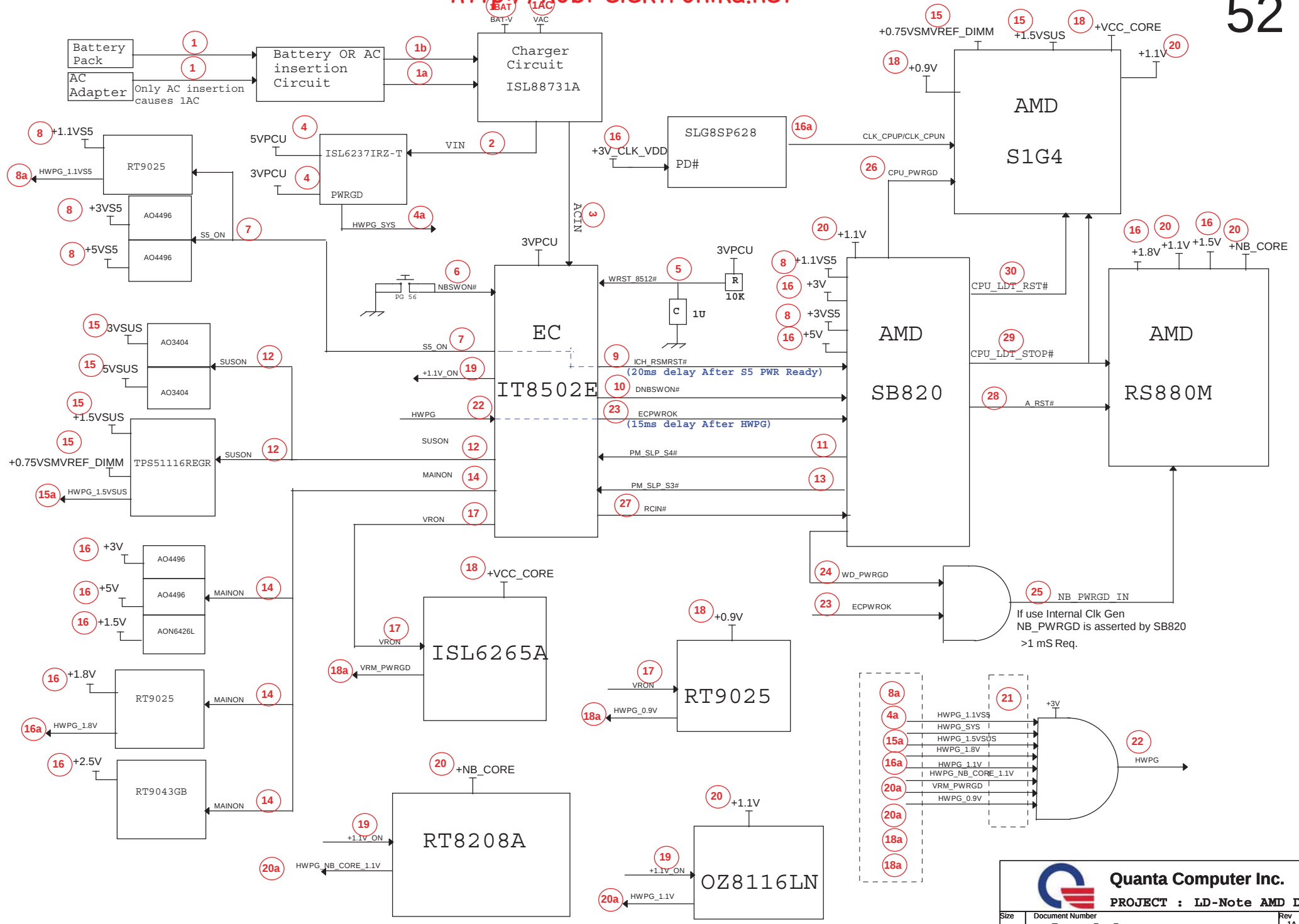
CPU_CORE

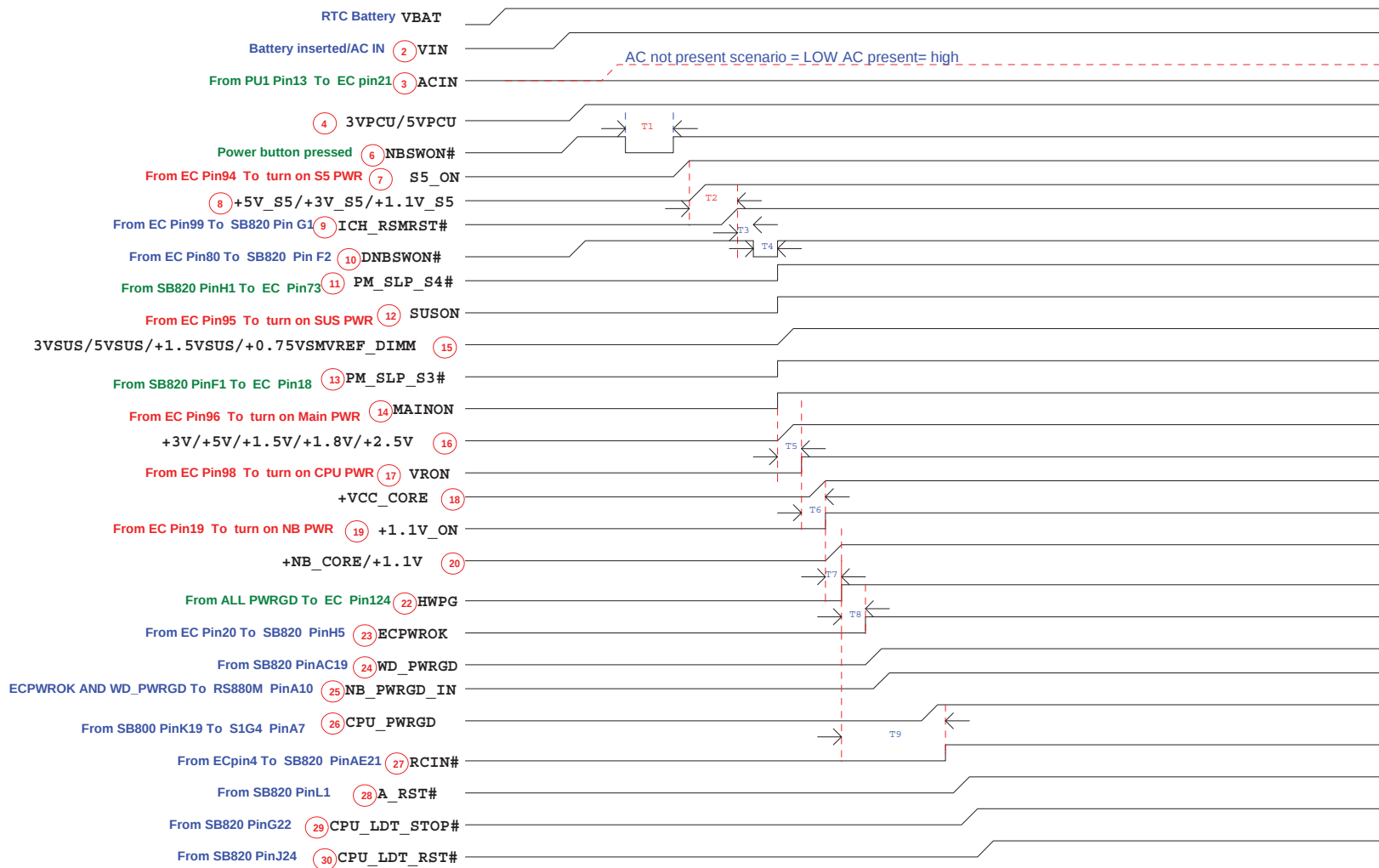


3VSUS, 5VSUS, 1.5VSUS, +0.75VSMVREF_DIMM









EC #	Page	Description	Part Affected
EC-C-01	20	Change error 10u footprint from 0603 to 0805	C51,C68,C78,C93,C236,C244,C247,C254,C257,C265,C270,C273,C602,C604,C705,C709,C714
EC-C-02		Layout change: Change TEST PAD size from 30mil to 20mil to increase ICT percentage	T1-T116,TP1-TP24
EC-C-03	23	Change X5R to X7R due to X5R stock is EOL	C362,C364
EC-C-04	3	Add value with " " " " due to it is a short pad originally	R106,R466,R468
	10		R573
	11		R268,R566
EC-C-05	10	Un-stuff 22P coupling CAP & change RES from 22ohm to 10ohm to fix LPC_CLK rising time issue	C777,R511
EC-C-06	48	Modify some RC value to meet VGA power up sequence From 10K to 0 ohm From 0.33U to NA From 0.01U to 2200P From 0.33U to 0.1U From 0.33U to 0.047U	PR165 PC115 PC117 PC103 PC113
EC-C-07	25	Change RGB bead value to fix EA rising time issue	L18,L24,L27
EC-C-08	19	AMD suggest remove pull high RES AMD suggest add pull high RES	R91,R412,R419 R416,R420
EC-C-09	39	Add fuse for EL keyboard UL suggestion	F6
EC-C-10	34	Add 2N7002 to reduce leakage current	Q41
EC-C-11	5	Add transistors for EC to monitor thermal of CPU (SB_TSI mode)	Q42,Q43,Q44
EC-C-12	11	Stuff the RES due to BOM error	R360
EC-C-13	8	Change BOM to meet "CPU_LDT_STOP#/" power sequence Replace Q36 with U48,delete R454,R451,change R452 from 4.7K to 2.2K	Q36,U48,R454,R451,R452
EC-C-14	3,8	AMD suggest "CPU_LDT_RST#/" & "CPU_LDT_STOP#/"connect to +1.5V power for prevent current leakage	R110,R453
EC-C-15	5	Delete thermal sensor schematic due to AMD suggest that don't use external thermal IC to prevent thermal shut down issue.	Q11,Q12,U7,R131,R132,R117,C302,C305,R138,R137,C341,Q13,R120
EC-C-16	46	To improve +1.1VSS rise time waveform. Modify CAP value.	PC80
EC-C-17	10	For RTC test accurately, modify 32.768KHz XTAL coupling CAP	C812,C813
EC-C-18	48	AMD fine tune VBIOS to meet VGA_CORE table	
EC-C-19	44	BOM error,remove the component	PC142
EC-C-20		Change the power jump to short pad	PJP1-PJP18
EC-C-21	45	Reserve RC circuit to modify power sequence	PR288,PC246
EC-C-22	45	Change RES value to fine tune +1.0_GPU prevent from voltage drop issue	PR152
EC-C-23	11	Add NEW_CLKREQ#, LAN_CLKREQ#, WLAN_CLKREQ# function at BIOS side	U38D pin AA16,AC18,AH21
EC-C-24	11	Delete single net SP_DDR3_RST# & 0 ohm RES	R337
EC-C-25	11	Add WAKE# net with +3VSS pull high	R606
EC-C-26	27	Add thansistor to avoide leakage current of CLK request and wake up function of LAN. Delete 0 ohm RES	Q45,Q46,R337 R317
EC-C-27	3	Un-stuff RES for leakage issue Stuff RES for leakage issue	R484,R485 R476,R477
EC-C-28	26	Vendor suggest reserve it,BOM not mount	C551
EC-C-29	12	Update board ID table for BIOS to verify PCB version	
EC-C-30	30	Because sku in't build WWAN, reserve all of components about WWAN function	CN25,U16,C395,C382,C396,C390,C383 CN26,R532,R543,R545,C808,C785,C795,C806,C784,C815
EC-C-31	41	Because we add LDO circuit to control G-Sensor power and we change GSENSOR_ON to high enable. We need to verify EC version	R381,R382
EC-C-32		Layout modify: modify SB & NB footprint due to customer request	U34,U43
EC-C-33	8	AMD comment DIS only supply 1.1V for NB_CORE,no need to stuff strap pin RES	R442
EC-C-34	12	AMD comment unstuff SB SATA 25MHz XTAL if we had stuff 25MHz internal XTAL	Y6,C794,C796,R536
EC-C-35	2	Follow up GC5C design to change 14.318 XTAL from 30ppm to 10ppm	Y1
EC-C-36	27	Change LAN chip version to reduce power consumption	U23
EC-C-37	26	Follow up GC5 design to change sense MIC switch from BJT to MOSFET	Q30
EC-C-38	41	ESD solution	D28,D29
EC-C-39	28	Reserve 0.1uF CAP due to ESD solution	C832
EC-C-40	30	Modify USB CONN footprint due to SMT request	CN24,CN27
EC-C-41		Change 0 ohm RES footprint from 0402 to short pad	R397,R431,R432,R459,R197,R200,R370,R372,R379,R250,R259,R563,R287,R306,R320,R182,R183 R426,R290,R186,R189,R193,R201,R148,R150,R151,R152,R20,R25,R3,R472,R473,R474,R475, R84,R355,R356,R293,R298,R520,R524,R167,R376,R594,R595,R596,R597,R598,R599,R600, R313,R300,R341,R195,R302,R368,R369,R413,R414,R415,R31,R32,R47,R447,R449,R450,R554, R571,R283,R436,R48,R227,R278,R346,R365,R204,R199,R252,R253,R267,R246,R270,R486,R552
EC-C-42	26	For MIC not be found issue, stuff R281,un-stuff R292,Q30,R286	R281,R292,Q30,R286
EC-C-43	41	Modify EC ID table for EC setting	R381,R382
EC-C-44	12	Modify board ID table for BIOS setting	R537,R538
EC-C-45	48	Remove 2N7002 due to BOM error	PQ51
EC-C-46	19	Change VGA thermal IC to ADM1032-2 in order to change address to 4D	U32
EC-C-47	41	BIOS set RF_SW# GPIO pull down to detect UMA & DISCRETE planer	R373,C575

EC #	Page	Description	Part Affected
EC-SVT-01		Delete all 0 ohm RES & jump for power portion schematic	
EC-SVT-02	43	Vendor suggest change RES value from 10K to 4.75K to fix 4 cell battery CC to CV ripple issue	PR45
EC-SVT-03	12	Change board ID for SVT planer revision	R540,R541,R533
EC-SVT-04	26	From vendor suggestion, change CAP value from 10u to 2.2u to fix beep sound issue	C556
EC-SVT-05	02	Delete all RP for CLKGEN output side	RP4,RP3,RP5,RP1,RP2,RP7,RP8,RP10,RP9,RP6
EC-SVT-06	12	Reserve GPIO pin for BIOS setting	R607,R608
EC-SVT-07	21	AMD suggest to un-stuff them due to CLKTESTA/B pin is for test	C216,C168,R65,R61
EC-SVT-08	23 29 29	Follow GCSC design to remove all common choke and fix EA test USB fail item at the same time	L40,R232,R233 CML1,R1,R2,CML3,R482,R483 CML2,R269,R276,CML4,R527,R526,CML5,R582,R581
EC-SVT-09	14	Delete R571 and short it directly to add test point for ICT fixture	R571