

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : PWR
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

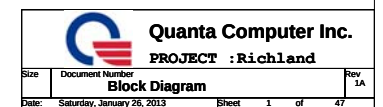


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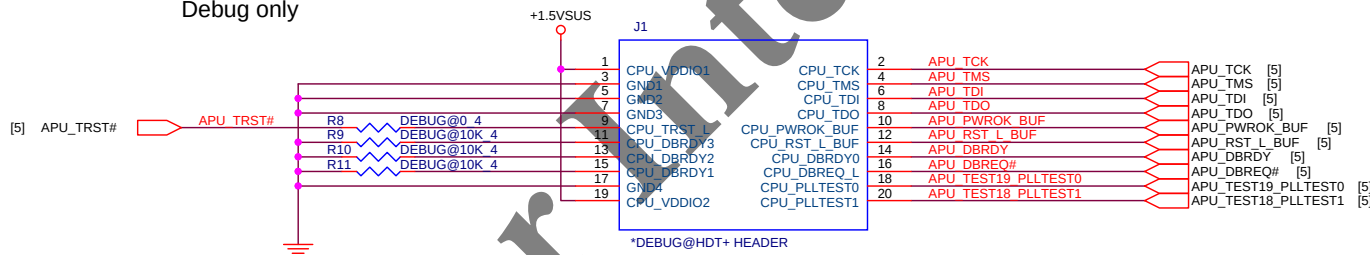
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
+VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3VPCU	+3.3V	AC/DC Insert enable	S0-S5
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P	S0
+1.5VSUS	+1.5V	S5_ON	S0-S3
+1.5V	+1.5V	MAIN_ON	S0
+1.2V_VDDPR	+1.2V	VDDA_PWRGD	S0
+1.1V_DUAL	+1.1V	+1.1V_DUAL_EN	S0-S5
+1.1V	+1.1V	MAIN_ON	S0
+VDD_CORE	~	VDDA_PWRGD	S0
+VDDNB_CORE	~	VDDA_PWRGD	S0
+VGPU_CORE		PX_MODE	S0
+1.8V_GPU	+1.8V	PE_GPIO1	S0
+1V_GPU	+1V	DGPU_PWREN	S0
+3V_GPU	+3.3V	PE_GPIO1	S0
+1.5V_GPU	+1.5V	PX_MODE_D	S0
+2.5V_VDDA	+2.5V	MAIN_ON	S0

GND PLANE	PAGE
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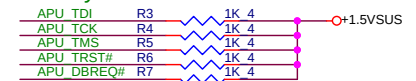
ITEM	Value Code	FUNCTIONS
1	CEC@	CEC
2	Debug@	HDT+ Debug
3	EV@	DISCRETE
4	IV@	UMA
5	U3@	Internal USB 3.0
6	1G4@	VRAM 1Gb*4
7	1G8@	VRAM 1Gb*8
8	2G@	VRAM 2Gb
9	AMD@	AMD VRAM
10	DIS@	DISCRETE
11	M2@	M2 FCH
12	M3@	M3 FCH
13	NMP@	LPC Debug Card
14	PX4@	PX4 Mode
15	PX5@	PX5 Mode
16	Sam@	Samsung VRAM
17	U2@	USB 2.0 (colay W USB 3.0)
18	E@	EMI

HDT+ Connector

Debug only



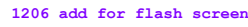
Close by HDT+ Conector

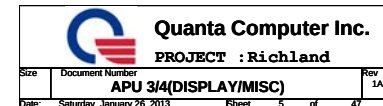
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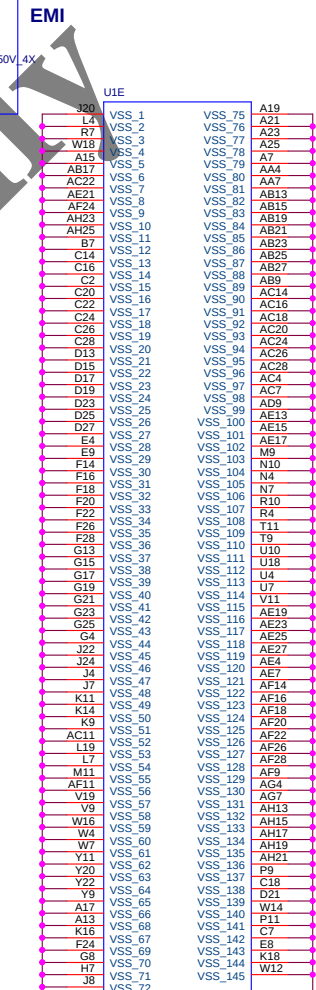
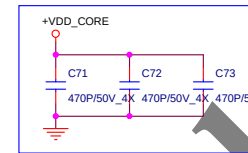
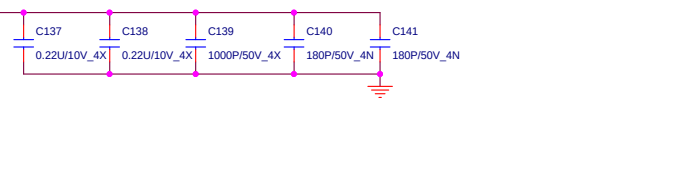
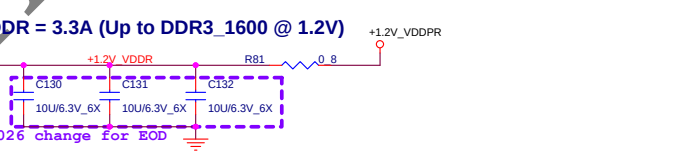
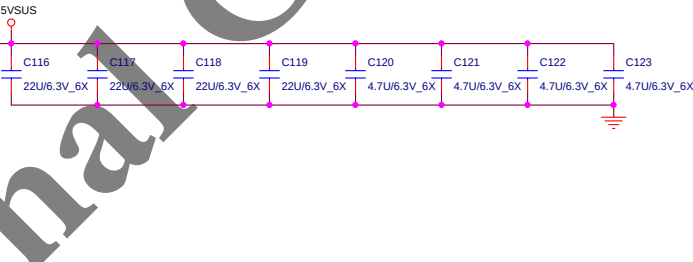
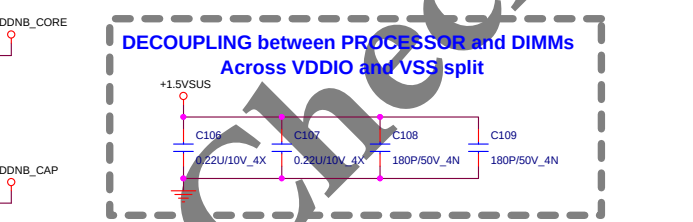
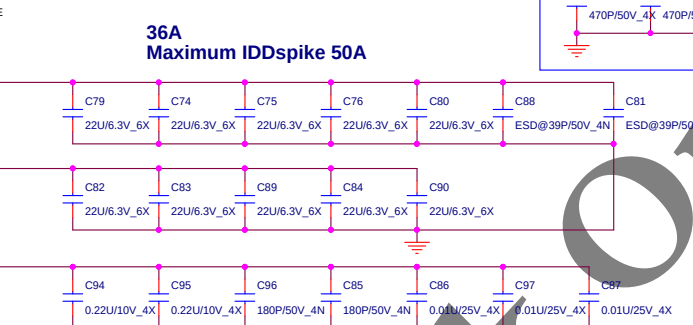
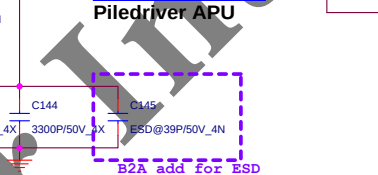
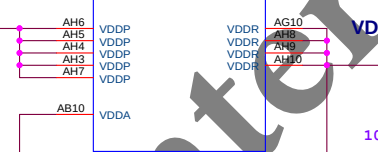
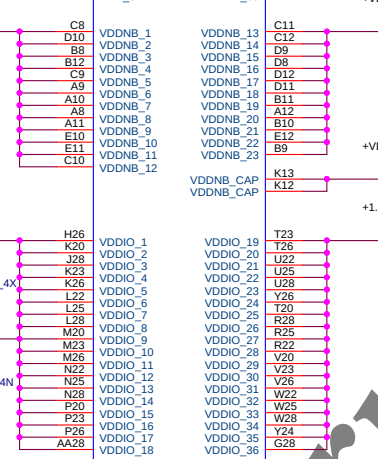
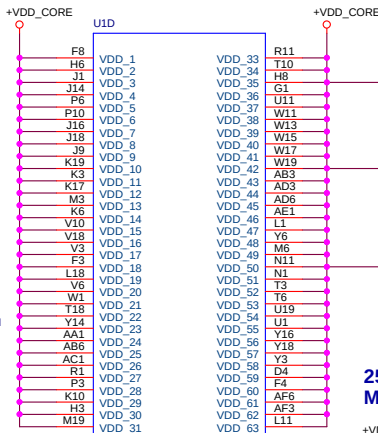
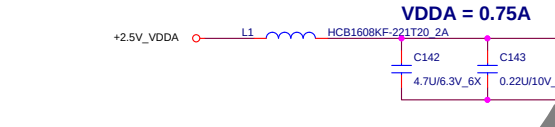
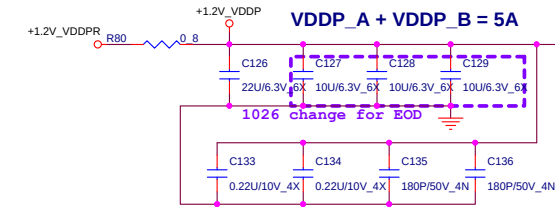
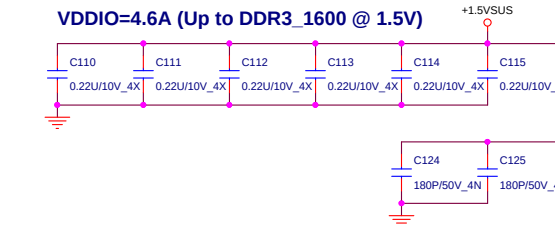
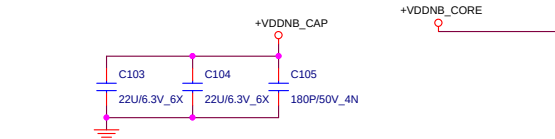
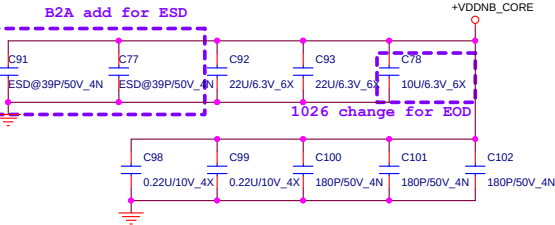
APU 1/4(PCIE/UMI/GPP/HDT)

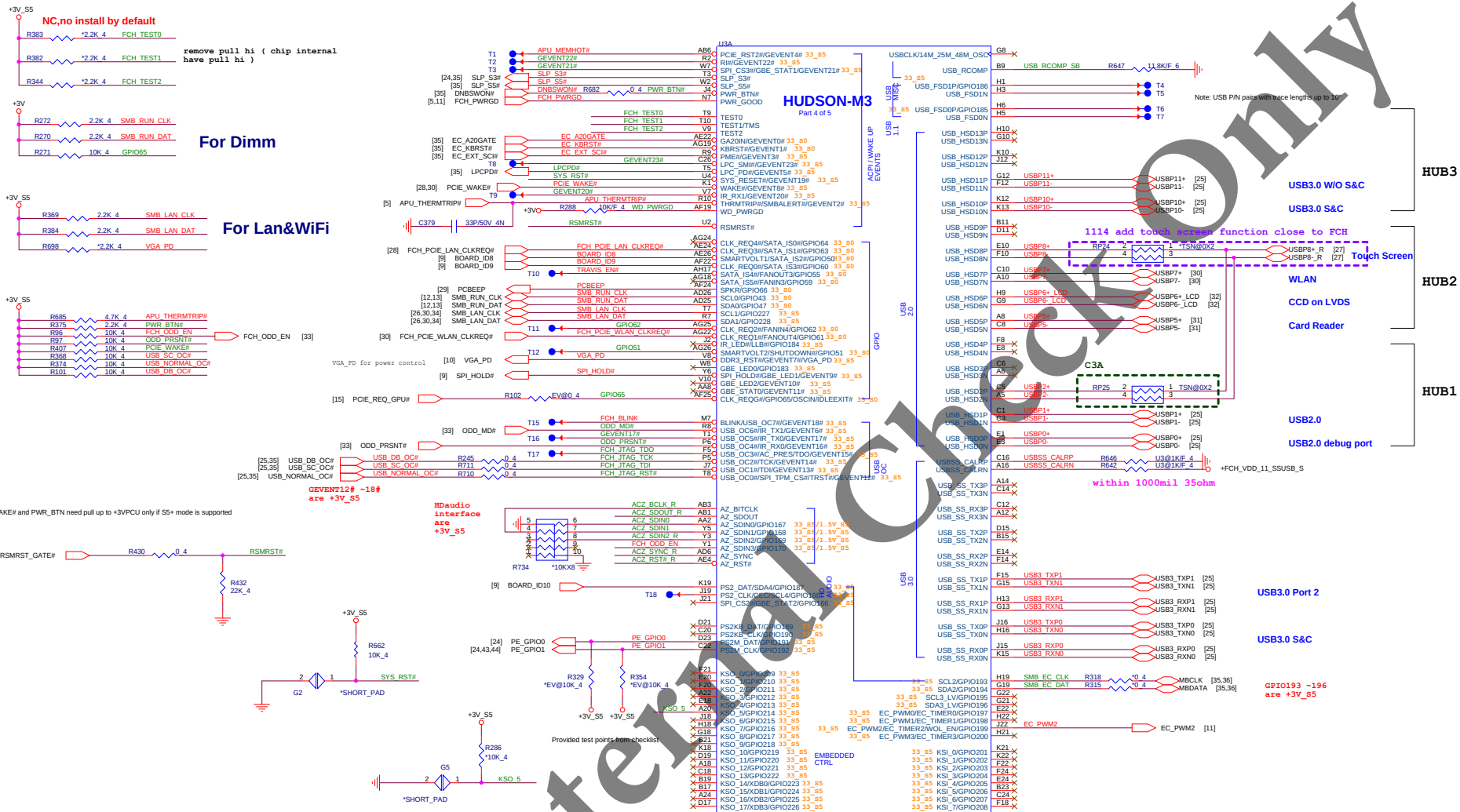
Size	Document Number APU 1/4(PCIE/UMI/GPP/HDT)	Rev 1A
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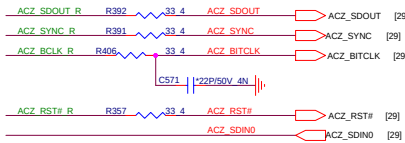


PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V





To Azalia

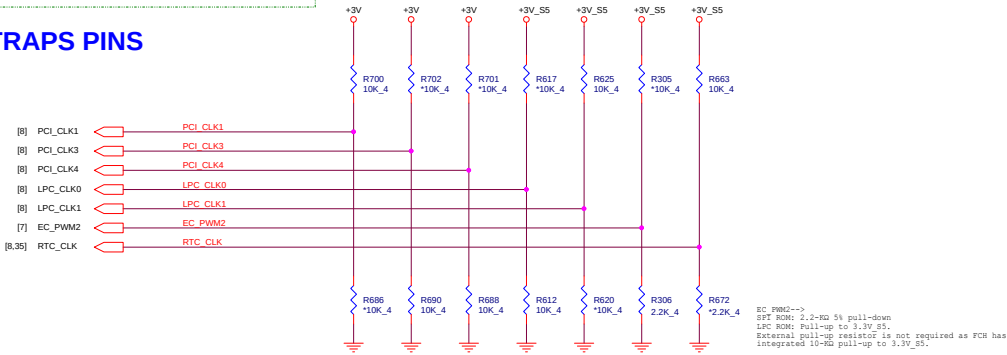






OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS



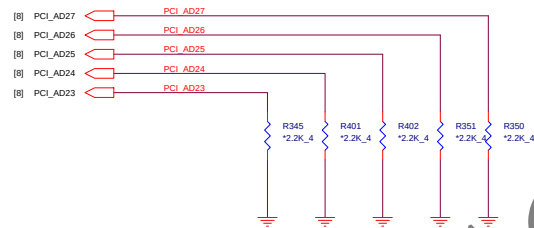
REQUIRED STRAPS

Remove PCI_CLK2 function

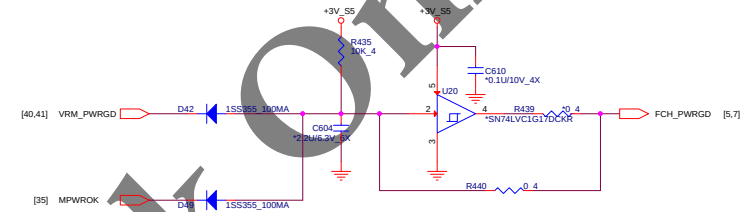
	*****	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	*****	ALLOW PCIE Gen2 DEFAULT	*****	USE DEBUG STRAP	non Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	*****	FORCE PCIE Gen1	*****	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



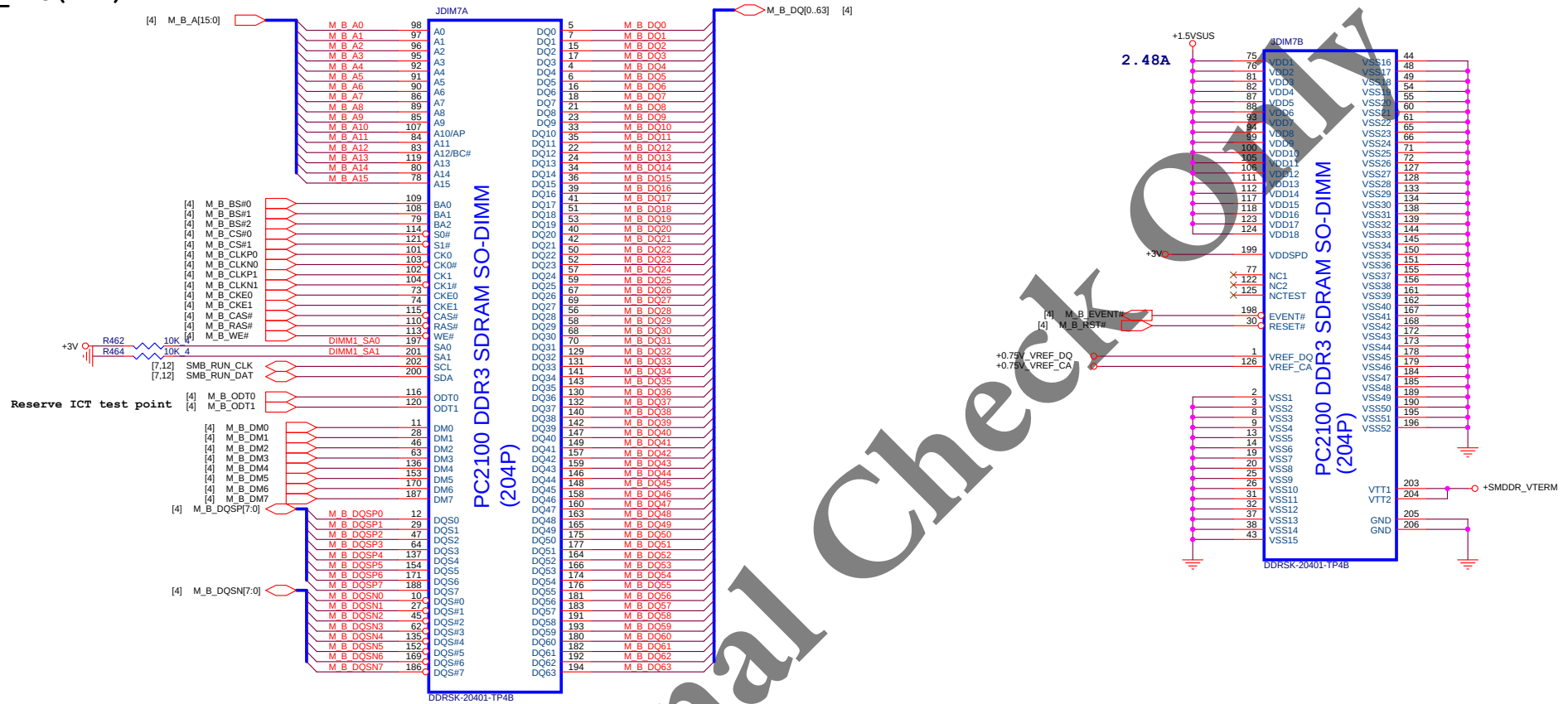
FCH_PWRGD_CKT



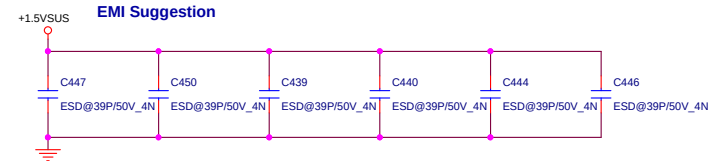
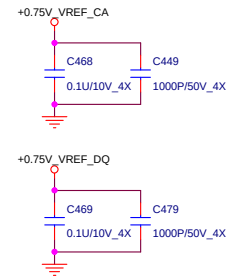
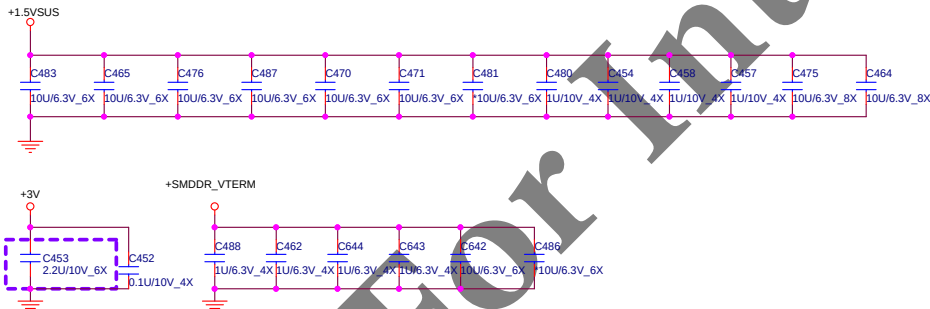
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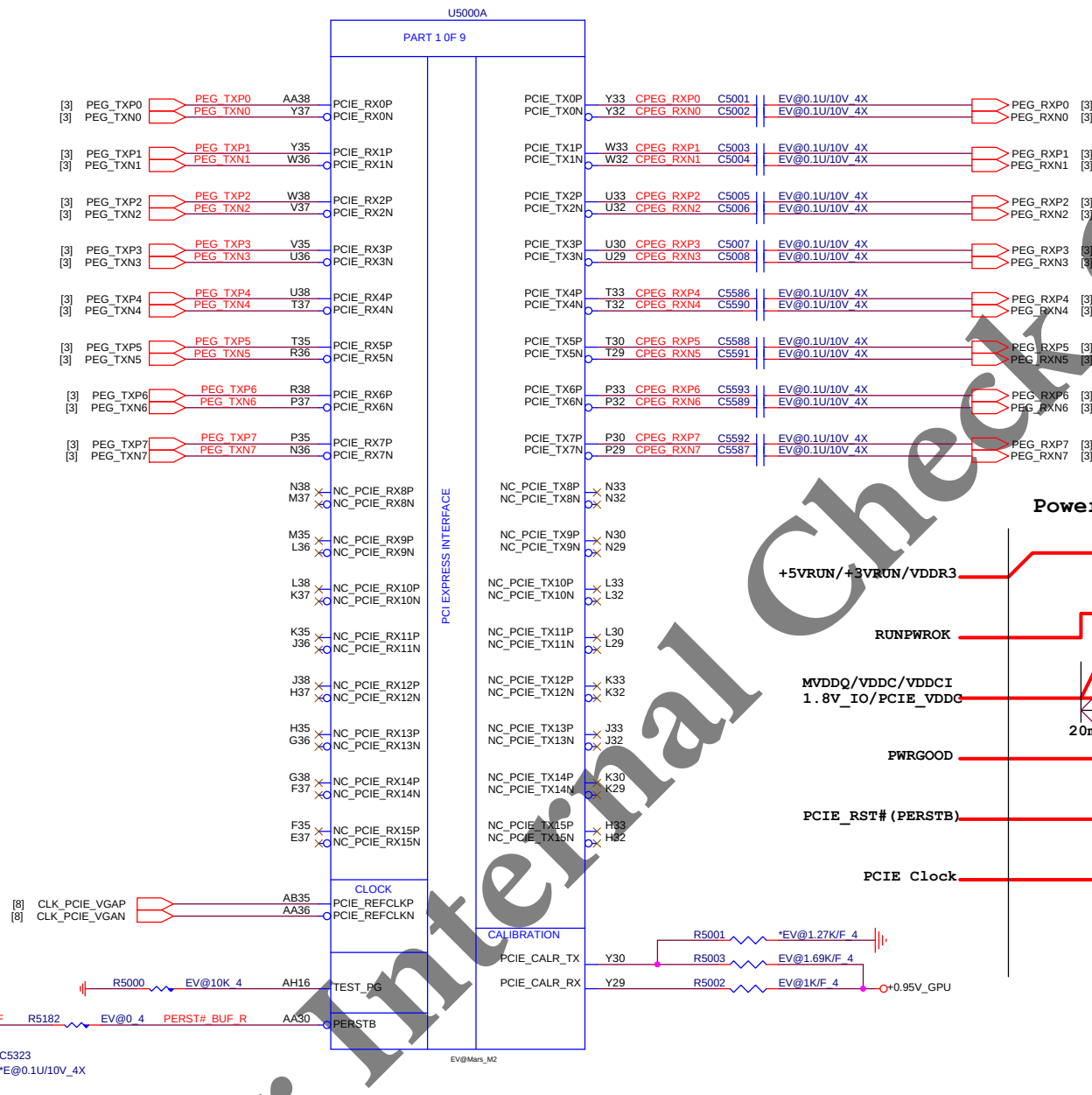
Size Document Number FCH 5/5(STRAP & PWRGD) Rev 1A
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DDR_RVS (DDR)



Place these Caps near So-Dimm1.





Mars Power-on sequence

1 => +3V_GPU

2 => +VDDC,+VDDCI,+1.5V_GPU,+0.95V_GPU

3 => +1.8V_GPU

PEG

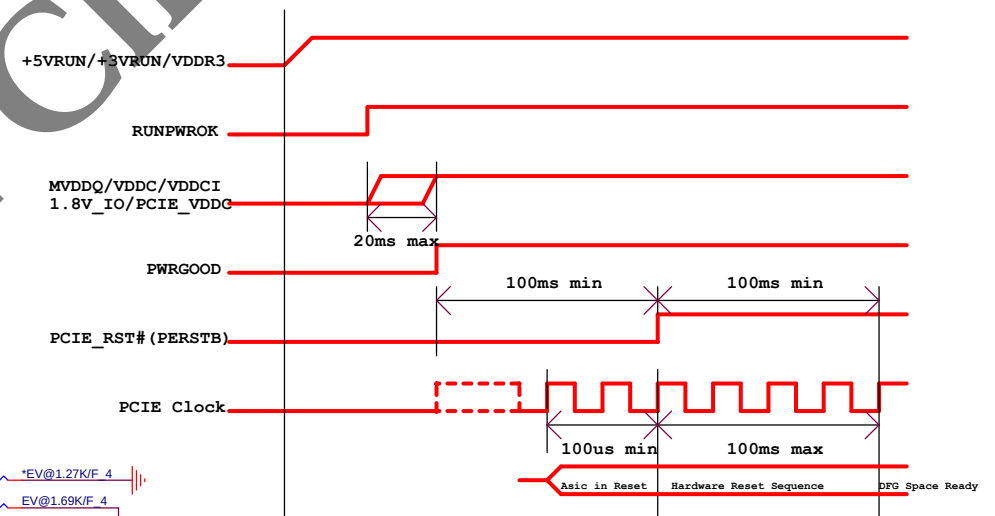
Intel platform: Lane0 ~ Lane15

Brazos platform: Lane12 ~ Lane15

Comal and Sabine platform: Lane8 ~ Lane15

Richland and Kabini platform: Lane0 ~ Lane7

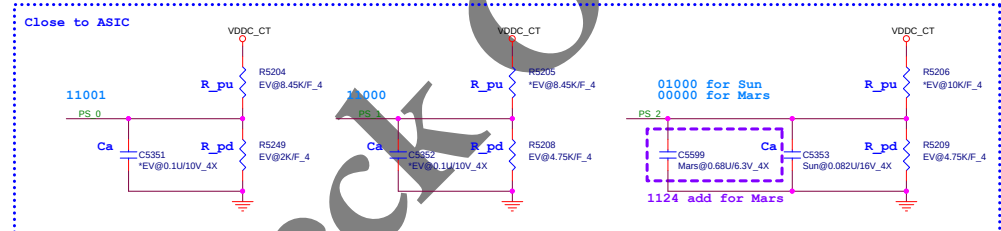
Power Up Reset Sequence



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	Mars_M2/ PEG*8	A1A
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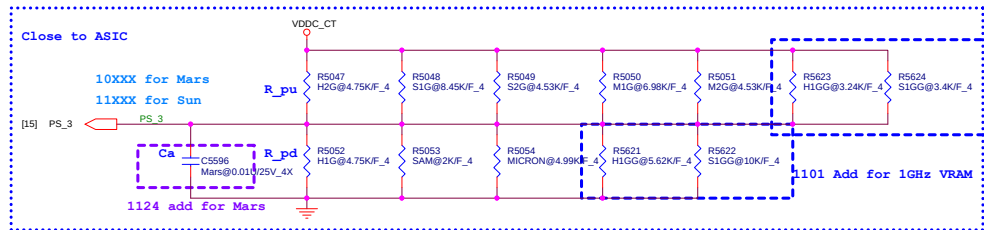
MLPS

R _{pu}	R _{pd}	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

MLPS Bit	Bits [5:1]
PS_0	11001
PS_1	11000
PS_2	01000
PS_3	11XXX





R _{pu}	R _{pd}	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

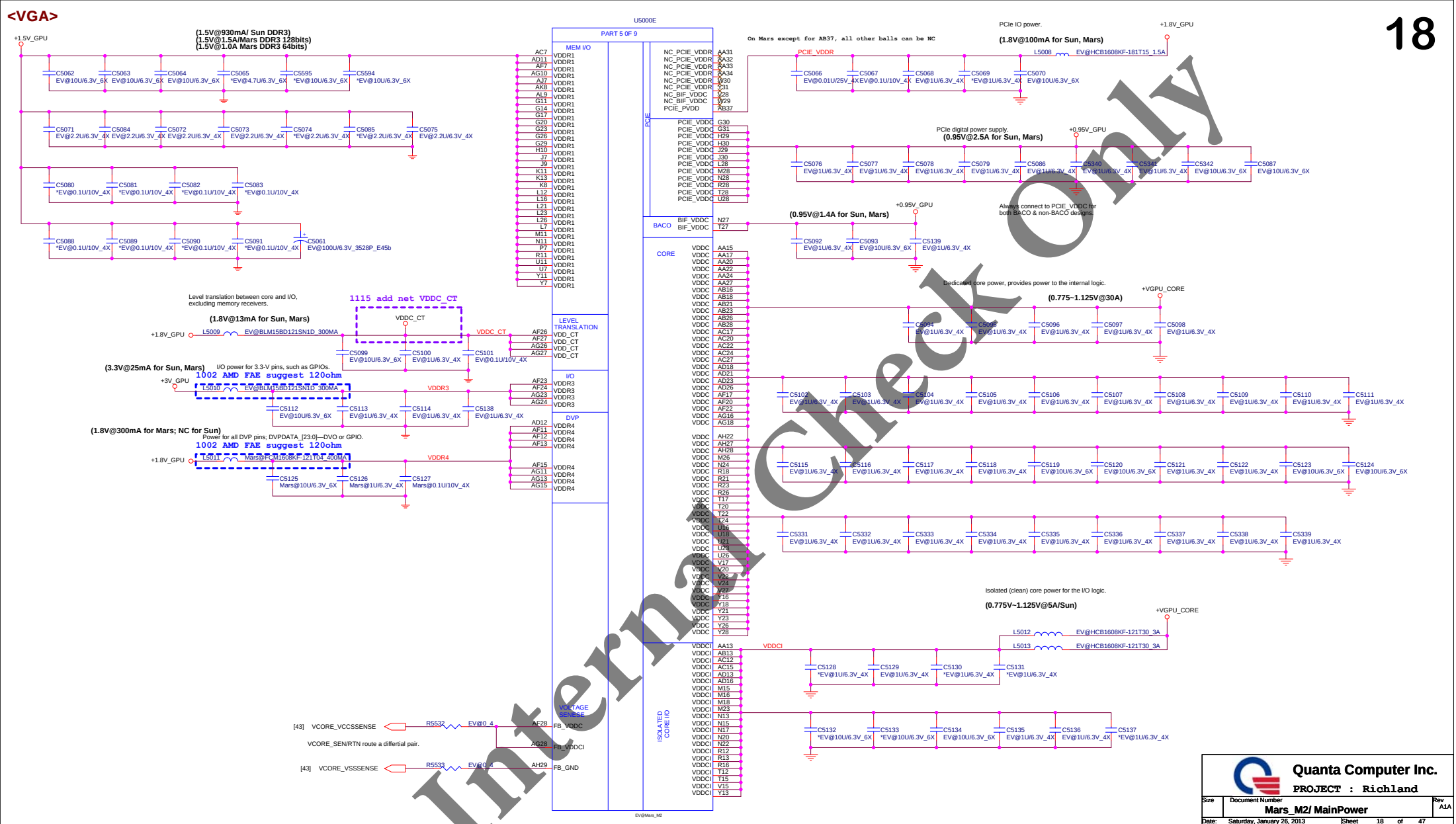
Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

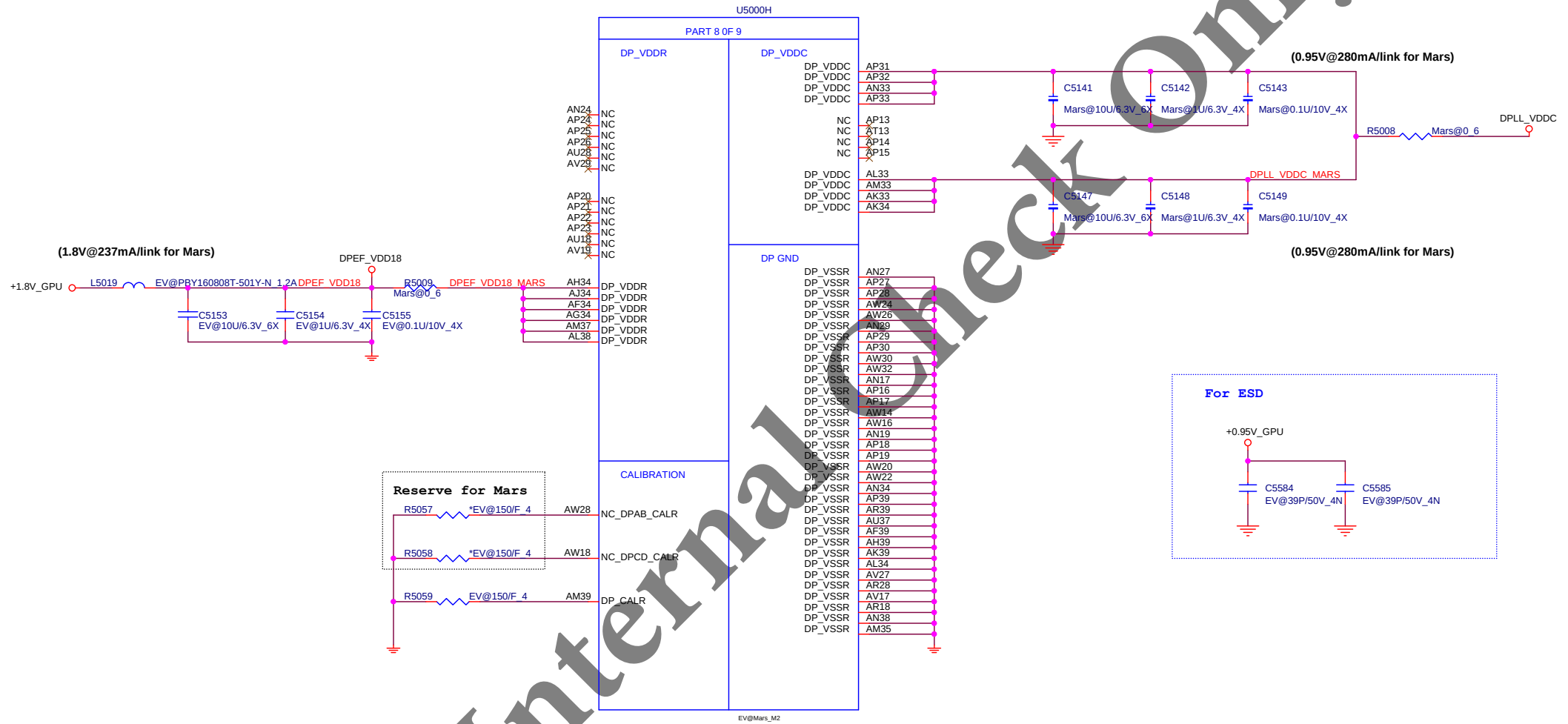
Vendor	Vendor P/N	B/S P/N (QCI P/N)	Size	MLPS
Hynix	H5TQ2G63DFR-11C (128M*16)(900MHz)	AKD5MGWWTW16 * 4	1GB	000
	H5TC4G63AFR-11C (256M*16)(900MHz)	AKD5PGWWTW05 * 4	2GB	111
	H5TQ2G63DFR-N0C (128M*16)(1GHz)	AKD5MGDTW01 * 4	1GB	101
Micron	MT41J128M16JT-107G:K (128M*16)(900MHz)	AKD5DGSTL00 * 4	1GB	011
	MT41K256M10HA-107G:E (256M*16)(900MHz)	AKD5PGSTL00 * 4	2GB	100
Samsung	K4W2G1646E-BC11 (128M*16)(900MHz)	AKD5MGGT520 * 4	1GB	001
	K4W4G1646B-HC11 (256M*16)(900MHz)	AKD5MGWWT516 * 4	2GB	010
	K4W2G1646B-BC1A (128M*16)(1GHz)	AKD5MGGT532 * 4	1GB	110

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

CONFIGURATION STRAPS – SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	0
STRAP_TX_CFG_DRV_FULL_SWING	PS_1[4]		Control the transmitter full-half- swing mode 0: 50% Tx output swing 1: Full Tx output swing	1
STRAP_TX_DEEMPH_EN	PS_1[5]		PCIe transmitter, de-emphasis enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
STRAP_BIF_GEN3_EN_A	PS_1[1]		PCIe GEN3 Capability 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	0 for Kabini
STRAP_BIF_VGA_DIS	PS_2[4]		VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space) 0: VGA controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
ROM_CONFIG[2:0]	PS_0[3..1]		Serial ROM type or Memory Aperture Size Select if GPIO22 = 1, defines memory aperture size if GPIO22 = 0, defines ROM type 100 = 512Kbit M25P16A (ST) 101 = 1Mbit M25P10A (ST) 110 = 2Mbit M25P20 (ST) 111 = 4Mbit M25P40 (ST) 101 = 8Mbit M25P80 (ST) 100 = 8Mbit Pm25LV012 (Chingis) 101 = 1Mbit Pm25LV010 (Chingis)	XXX
STRAP_BIOS_ROM_EN	PS_2[3]		Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
N/A	PS_0[4]		Reserved for internal use only. Must be 1 at reset	1
N/A	PS_1[3]	GENLK_CLK	Reserved	0
STRAP_BIF_CLK_PM_EN	PS_1[2]	GPIO8	PCIe reference clock power management capability is reported in the PCI 0: The CLKREQ# power management capability is disabled 1: The CLKREQ# power management capability is enabled	0
RESERVED	NA	GPIO21	Reserved	0
RESERVED	NA	GENERICC	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[0]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Timing diagram for PCIe reset sequence. The diagram shows the relationship between +5VRUN/+3VRUN/VDDR3, RUNPWROK, MVDQ/VDDC/VDDCI 1.8V_IO/PCIE_VDDO, PWRGOOD, PCIE_RST#(PERSTB), and PCIE Clock. Key timing parameters include a 20ms max delay for MVDQ/VDDC/VDDCI 1.8V_IO/PCIE_VDDO after RUNPWROK, and 100ms min/100ms max delays for PCIE_RST#(PERSTB) and PCIE Clock after PWRGOOD. The PCIE Clock is shown as a dashed line during the reset period and as a solid line with a square wave after reset.

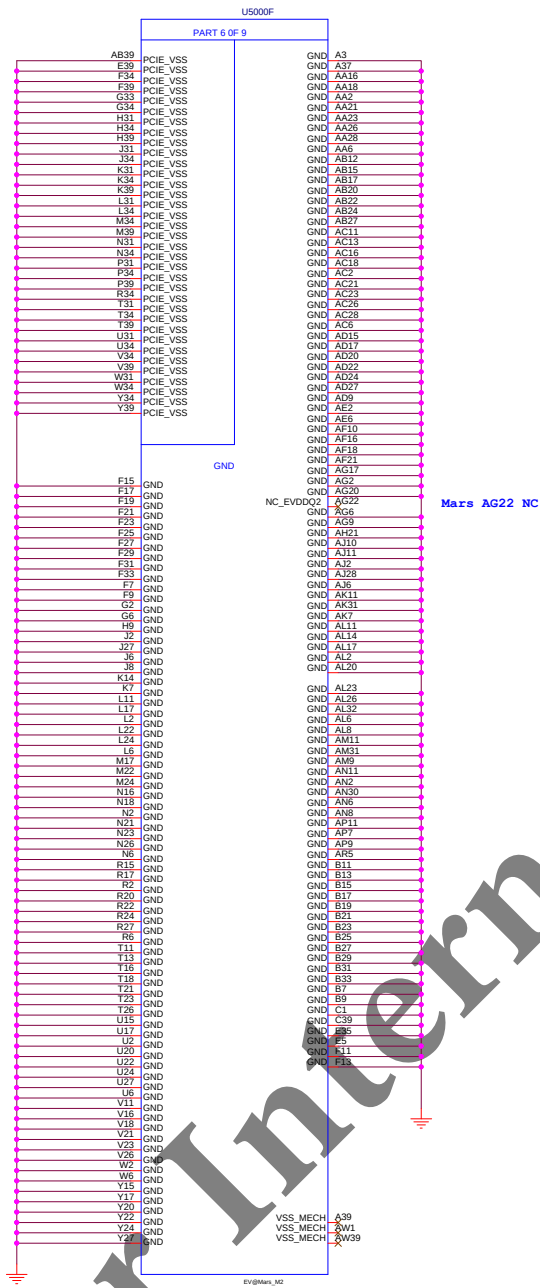




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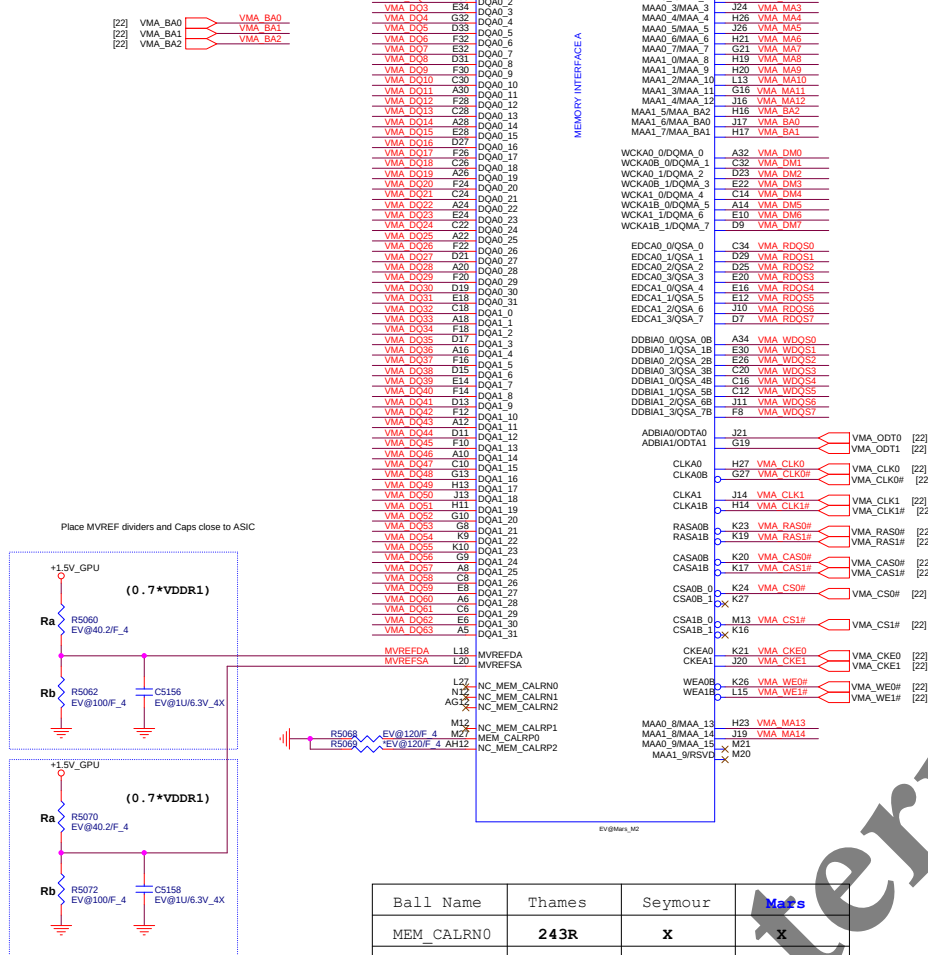
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	Mars_M2/ DP_Powers	A1A
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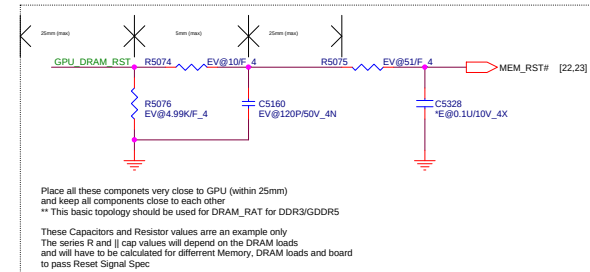
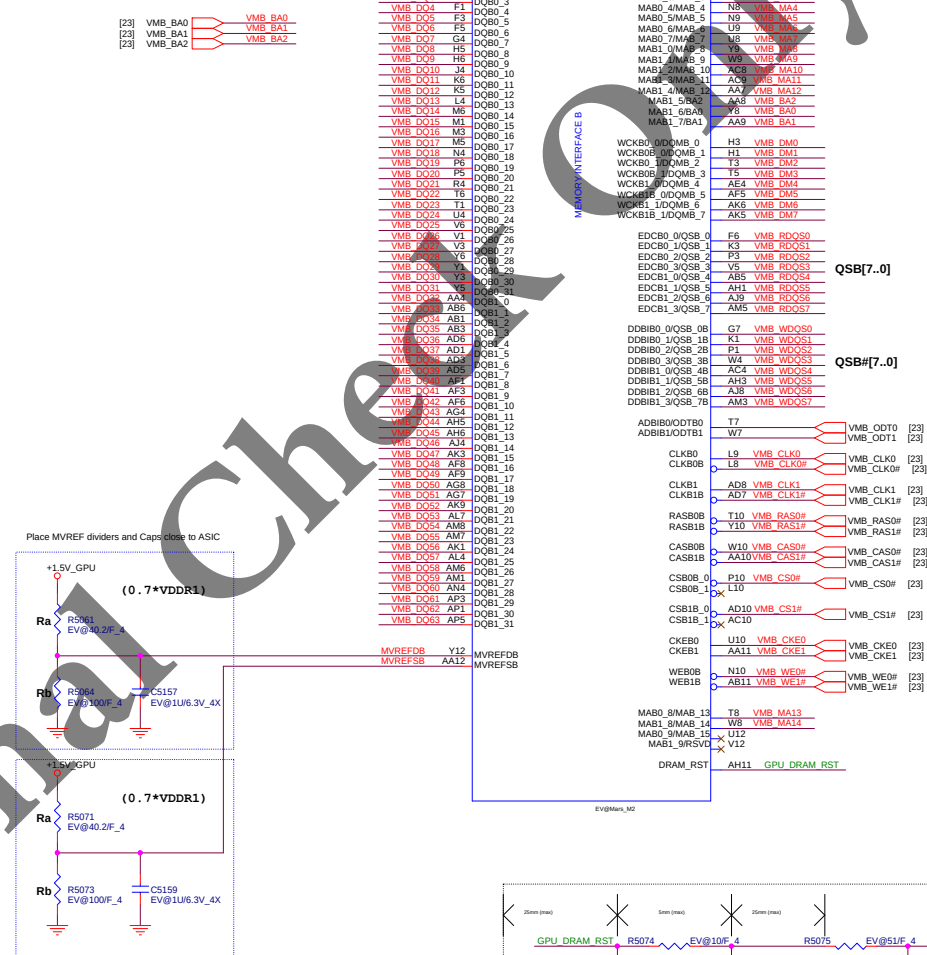


[22] VMA_DQ[63..0] VMA_DQ[63..0]
 [22] VMA_DM[7..0] VMA_DM[7..0]
 [22] VMA_RDQS[7..0] VMA_RDQS[7..0]
 [22] VMA_WDQS[7..0] VMA_WDQS[7..0]
 [22] VMA_MA[14..0] VMA_MA[14..0]

[23] VMB_DQ[63..0] VMB_DQ[63..0]
 [23] VMB_DM[7..0] VMB_DM[7..0]
 [23] VMB_RDQS[7..0] VMB_RDQS[7..0]
 [23] VMB_WDQS[7..0] VMB_WDQS[7..0]
 [23] VMB_MA[14..0] VMB_MA[14..0]



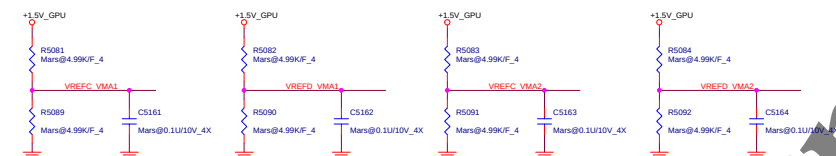
Ball Name	Thames	Seymour	Mars
MEM_CALRN0	243R	X	X
MEM_CALRN1	X	243R	X
MEM_CALRN2	243R	X	X
MEM_CALRP0	243R	X	120R
MEM_CALRP1	X	243R	X
MEM_CALRP2	243R	X	X



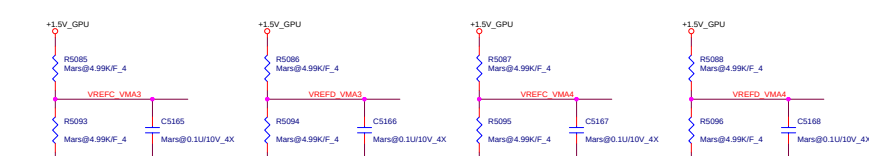
BOT Left

TOP Right

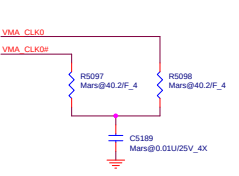
Group-A0 VREF



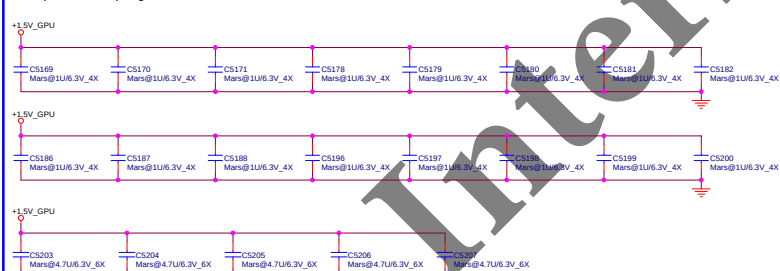
Group-A1 VREF



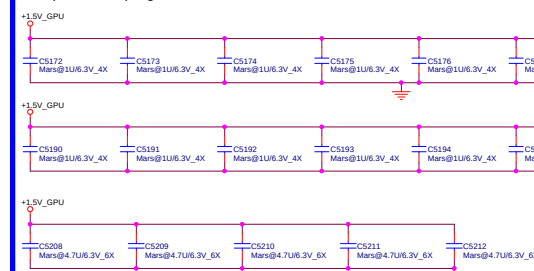
MEM_A0 CLK



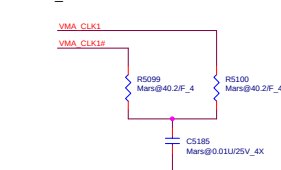
Group-A0 decoupling CAP

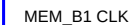
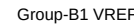
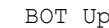


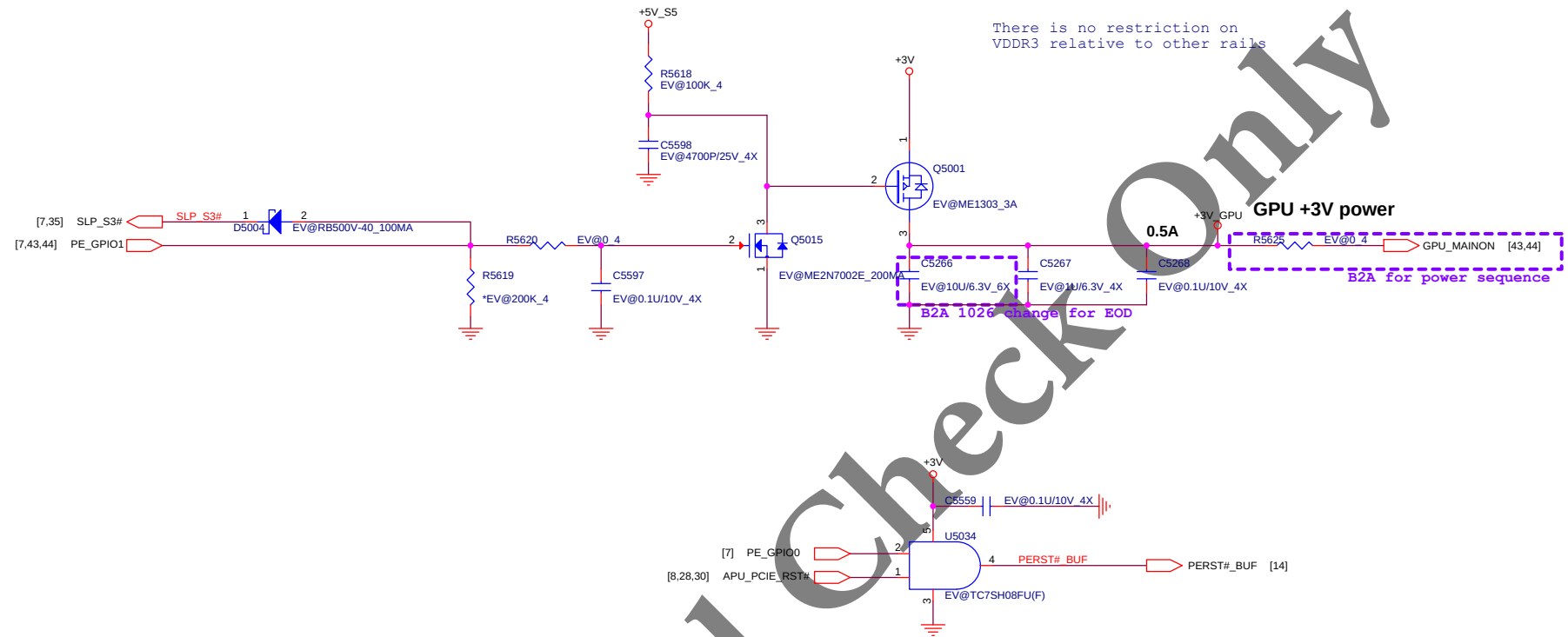
Group-A1 decoupling CAF



MEM A1 CLK







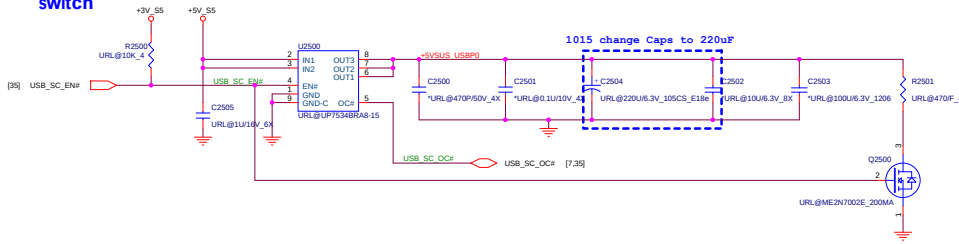
For Internal Check Only

USB 3.0 Power switch

<USB> <U3B>

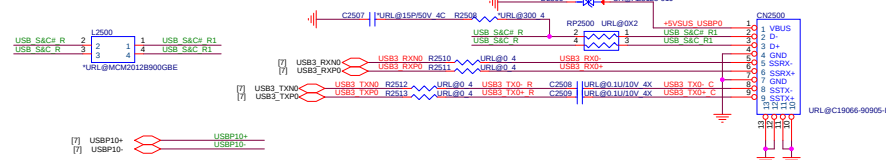
USB w S&C MAXIM solution <SLC>

25



USB 3.0 CONN <U3B> <USB> <EMI>

Right-Low Side USB3.0 Support S&C



SW2	SW3	14600
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	0	Pass-Through(USB) mode
1	1	pass-through(USB) with CDP Emulation

Charger , AM
Charger , FM
USB , PM
USB , CM

SW2	SW3	14644
CB0	CB1	Status
0	0	2A Auto mode for Apple device
0	1	Force dedicated charger mode
1	0	Pass-Through(USB) mode
1	1	pass-through(USB) with CDP Emulation

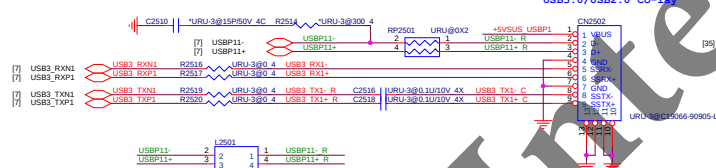
Charger , AM2
Charger , FM
USB , PM
USB , CM

SW2	SW3	14641
CB0	CB1	Status
0	0	2A Auto mode for Apple device
0	1	Force 1A for Apple device
1	0	Pass-Through(USB) mode
1	1	pass-through(USB) with CDP Emulation

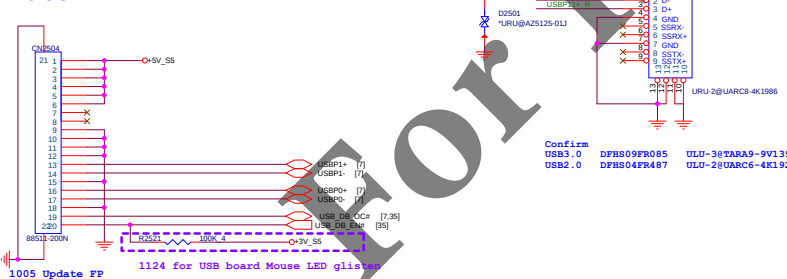
Charger , AM2
Charger , FM
USB , PM
USB , CM

USB 3.0 CONN <U3B> <U2B> <EMI>

Right-Up Side USB3.0/USB2.0 Co-Lax



USB 2.0 CONN



Confirm
USB3.0 DFHS09FR085 ULO-38TARA9-9V1391
USB2.0 DFHS04FR487 ULO-28UARC6-4K1926

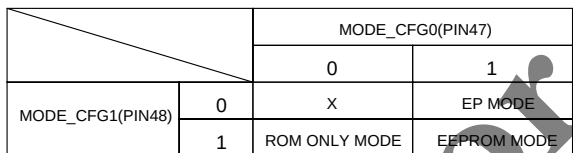
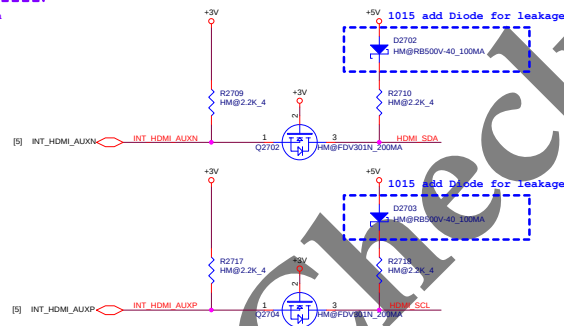
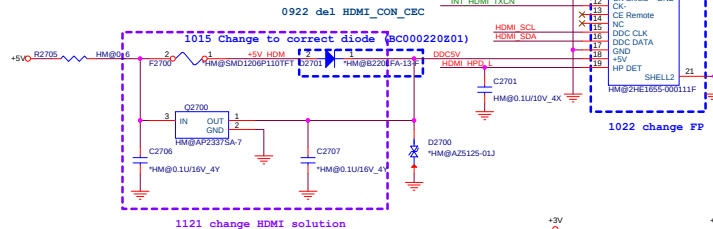
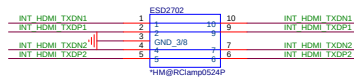
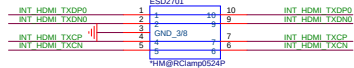
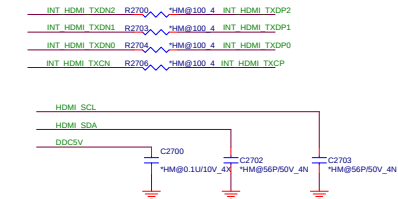


Figure 1 shows the pin connections for the HDMI module. The connections are as follows:

- INT_HDMI_TXD0N0 (Left) to INT_HDMI_TXD0N0 (Right)
- INT_HDMI_TXDP0 (Left) to INT_HDMI_TXDP0 (Right)
- INT_HDMI_TXD1N1 (Left) to INT_HDMI_TXD1N1 (Right)
- INT_HDMI_TXDP1 (Left) to INT_HDMI_TXDP1 (Right)
- INT_HDMI_TXD2N2 (Left) to INT_HDMI_TXD2N2 (Right)
- INT_HDMI_TXDP2 (Left) to INT_HDMI_TXDP2 (Right)
- INT_HDMI_TXCN (Left) to INT_HDMI_TXCN (Right)
- INT_HDMI_TXCP (Left) to INT_HDMI_TXCP (Right)



[5] INT_HDMI_HPD

3V

R2701
HM1K_5

Q2701B
5S

HM2N7002KDW_115MA

5V

R2702
HM10K_4

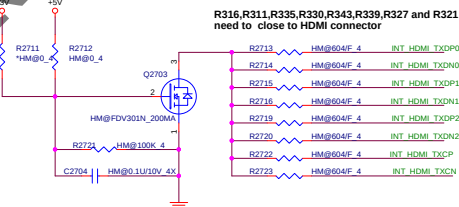
HM(2N7002KDW_115MA

2

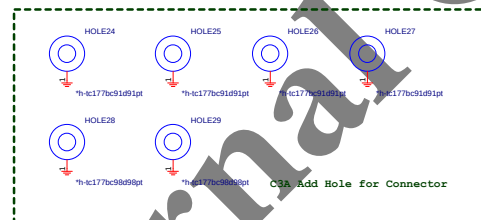
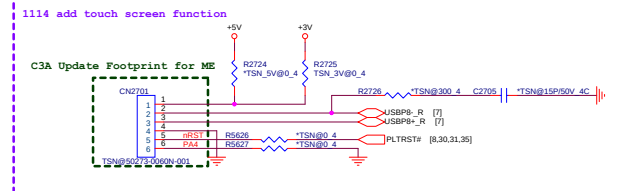
HDMI_HPD_1

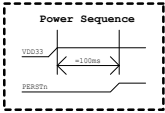
Q2701A

R2709
HM(10K_

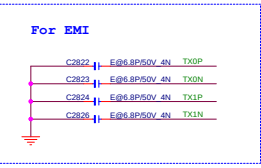
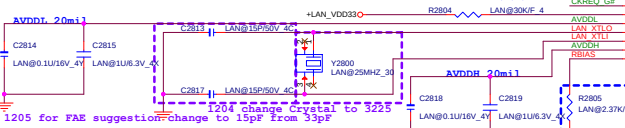
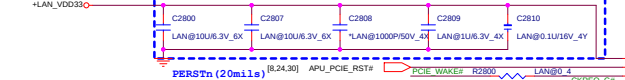


```
1114 add touch screen function
```





0.163A(30mils)



Atheros
AR8161/8162

GIGA:AR8161B
10/100:AR8162B

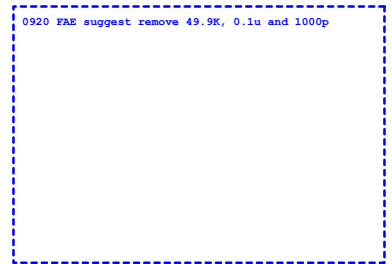
<LAN> <LNG> <LN1>

28

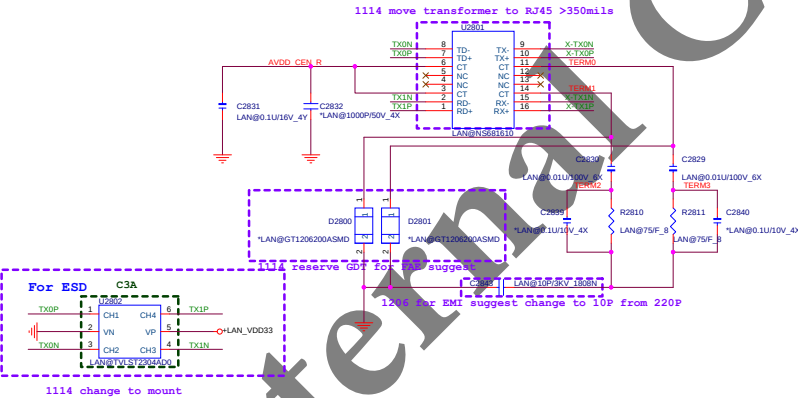
LAN-Wake up function <LAN>

Wake on LAN function <LAN>

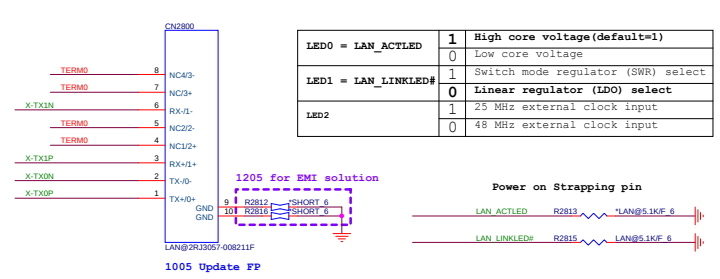
PLACE NEAR LAN IC SIDE <LAN> <LNG>



TRANSFORMER CONN <LAN> <LNG>

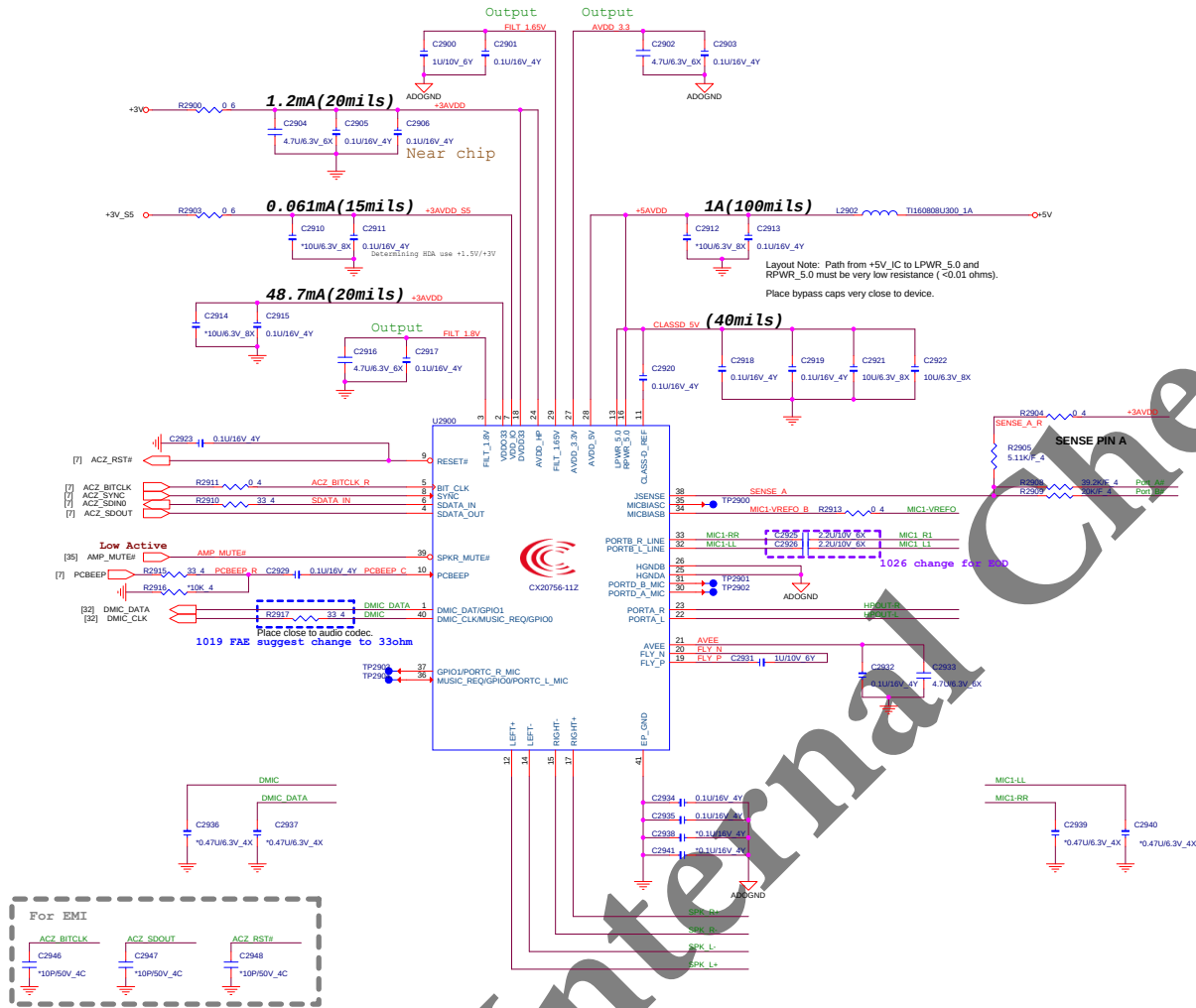


RJ45 <LAN> <LNG> <LN1>

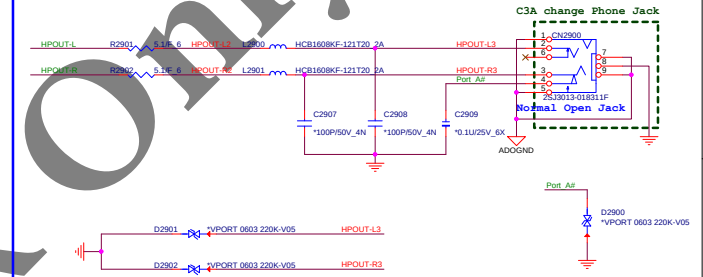


LED0 = LAN_ACTLED	1	High core voltage(default=1)
	0	Low core voltage
LED1 = LAN_LINKLED#	1	Switch mode regulator (SWR) select
	0	Linear regulator (LDO) select
LED2	1	25 Mhz external clock input
	0	48 Mhz external clock input

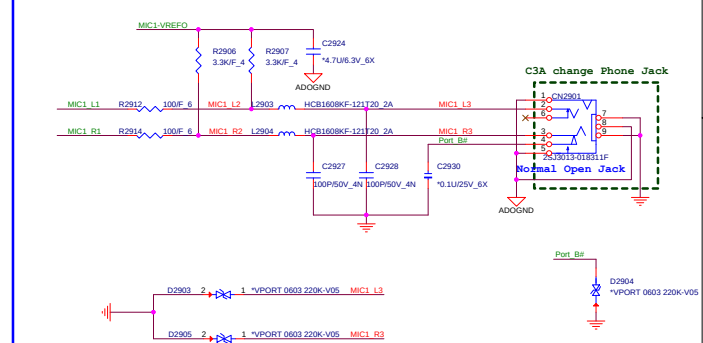
Codec (CX20756-11Z) <ADO> <EMI>



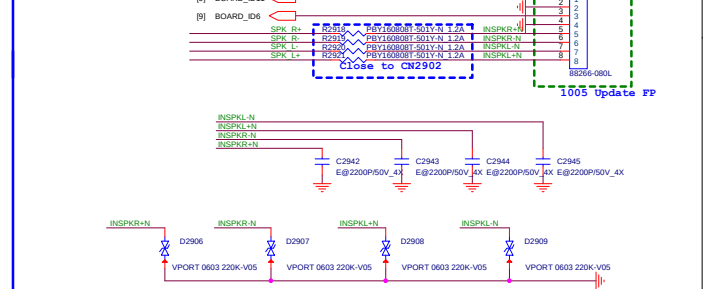
HP <ADO> <EMC>



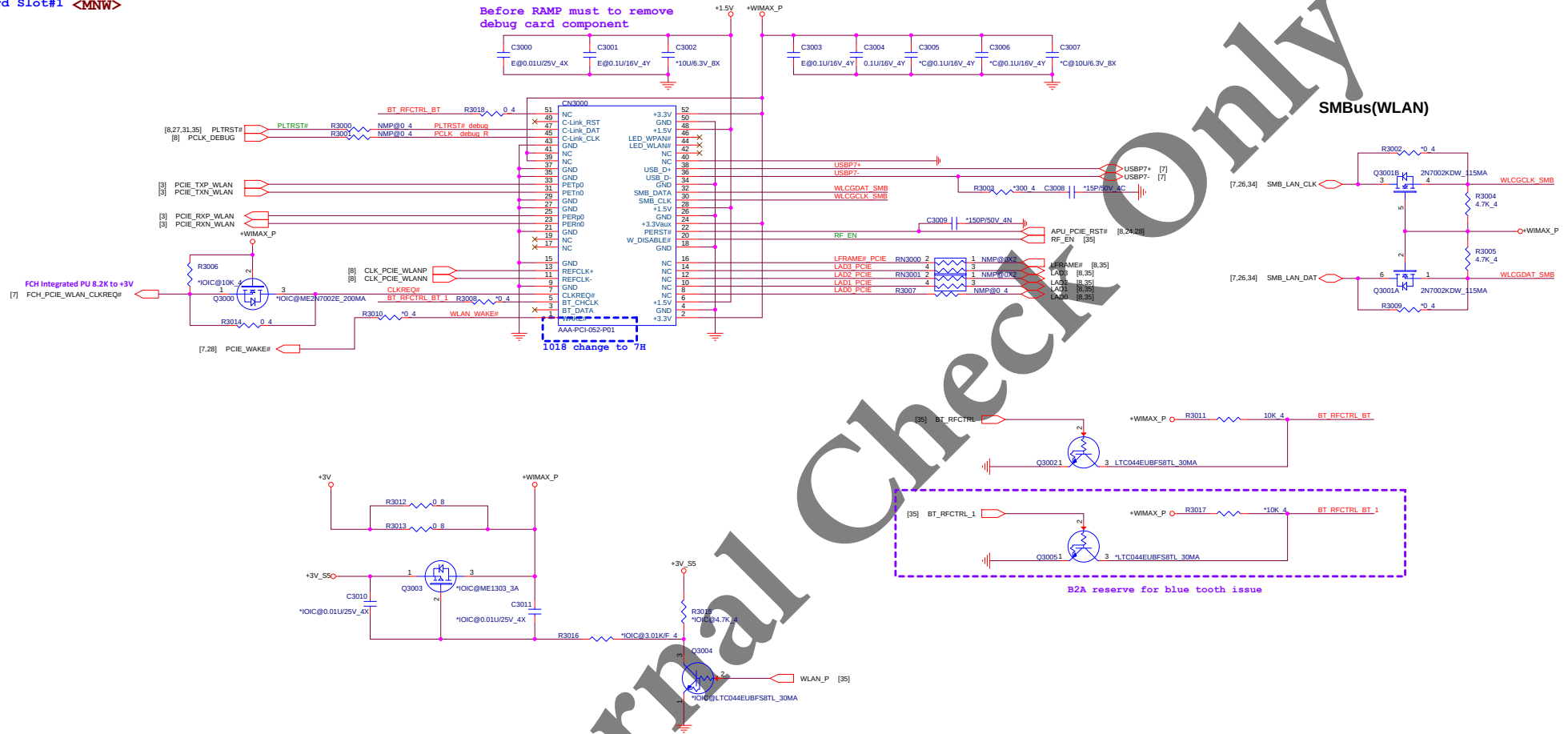
External MIC <ADO> <EMC>



Internal Speaker
<ADO> <EMC>

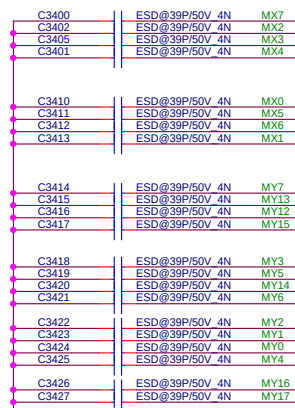


MINI Card Slot#1 <MNW>
(WiFi)

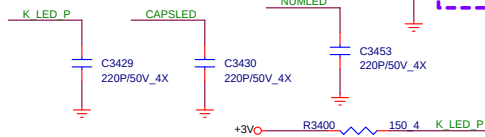


KEY BOARD Connector <KBC> <EMI>

INT KeyBoard

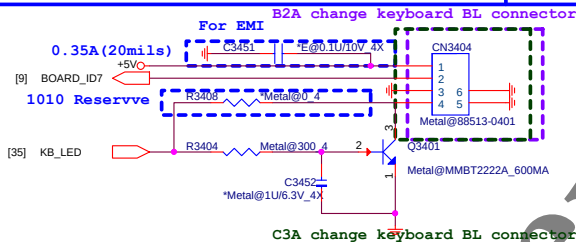


ESD Issue

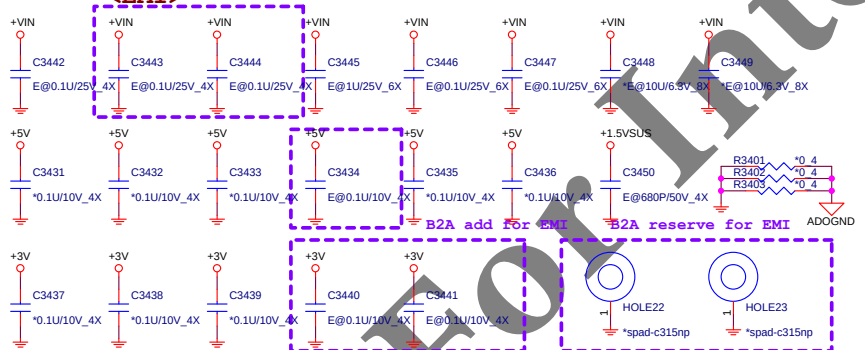


KEY BOARD LED

<KBP> <EMI>

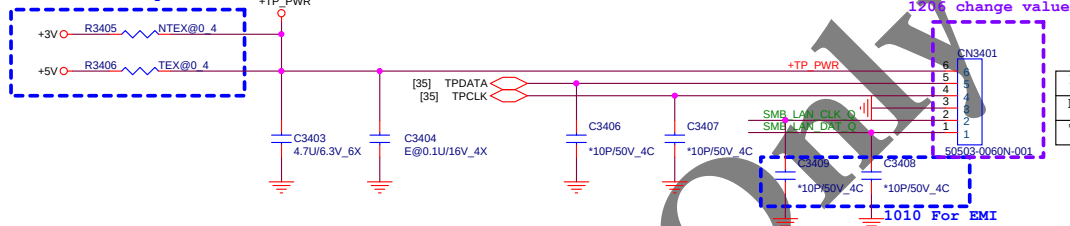


EMI PAD <EMI> B2A add for EMI



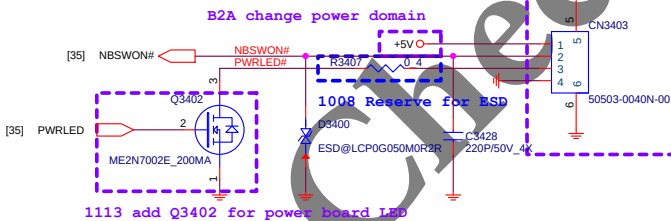
TOUCH PAD BOARD <TPD> <EMI>

1101 BOM option

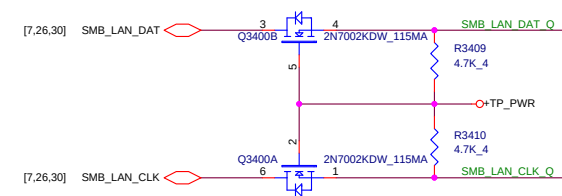


ID_Detect	default
Metal	+3.3V
TEXTURE	+5V

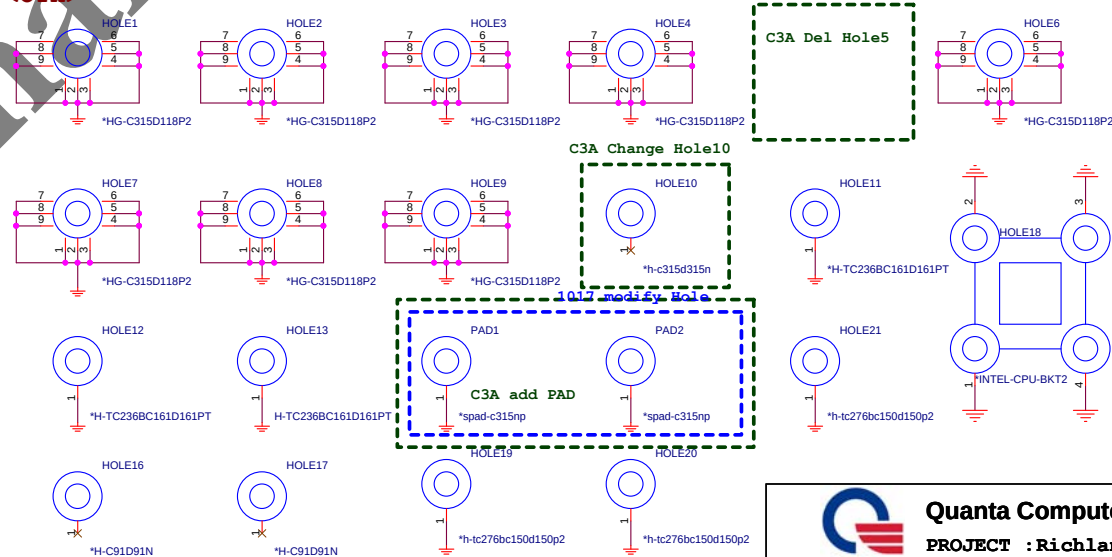
Power Board (UIF) <PSW>

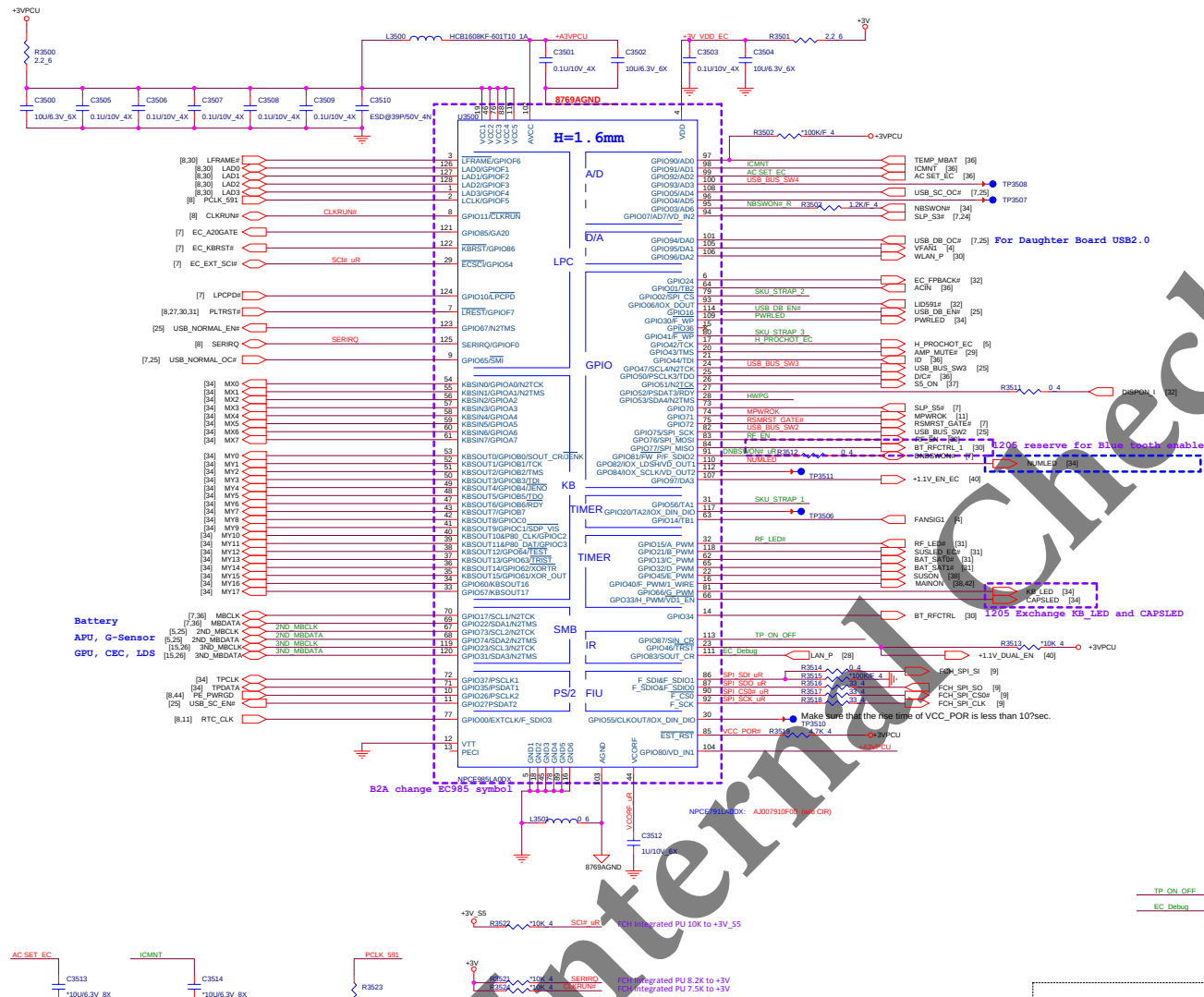


TP board <TPD>



HOLE <OTH>



SM BUS
PU

<KBC>

SMBus Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	3D Sensor	32H
	EC EEPROM	A0H
	VGA Board Thermal Sensor	98H
3	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H

Strap <KBC> SHBM

RF EN

R3510

10K 4

SHBM-0: Enable shared memory with host BIOS

Disables (1) if using PWM device on LPC

Enables (1) if using SPI flash for both system BIOS and EC firmware

ID EEPROM <KBC>

R3510

10K 4

ADDRESS: A0H

0.003A(20mils)

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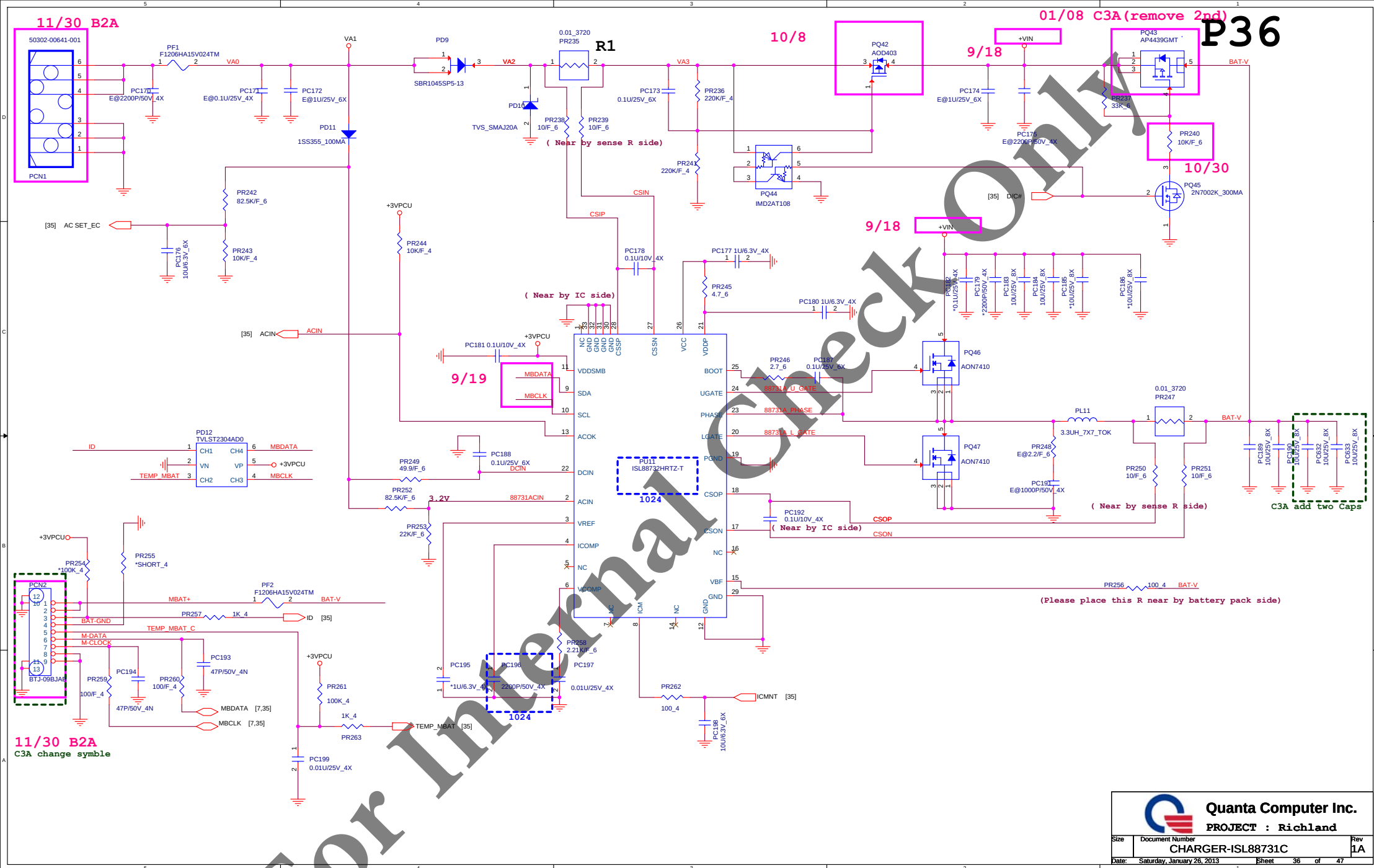
R3510

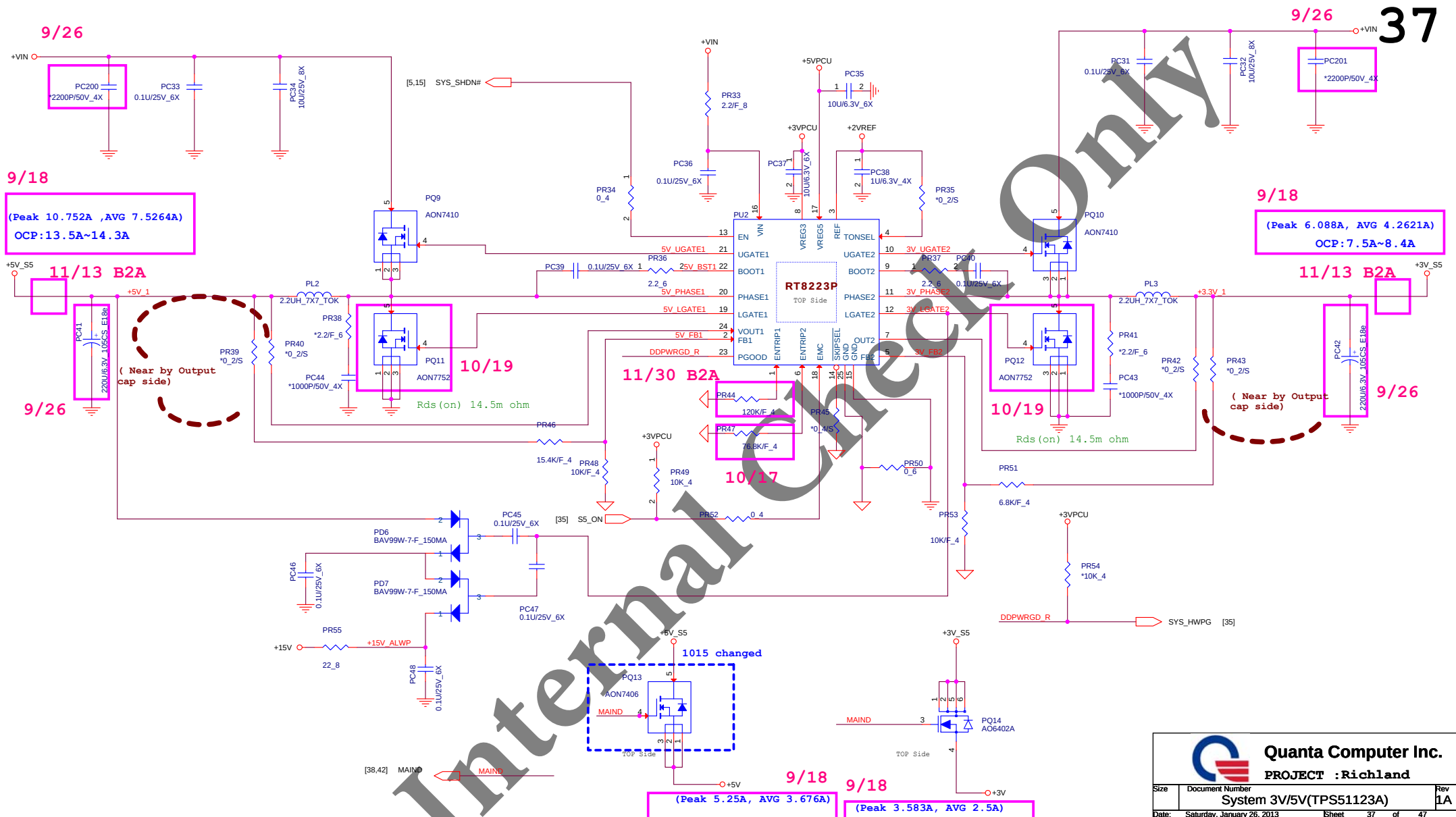
10K 4

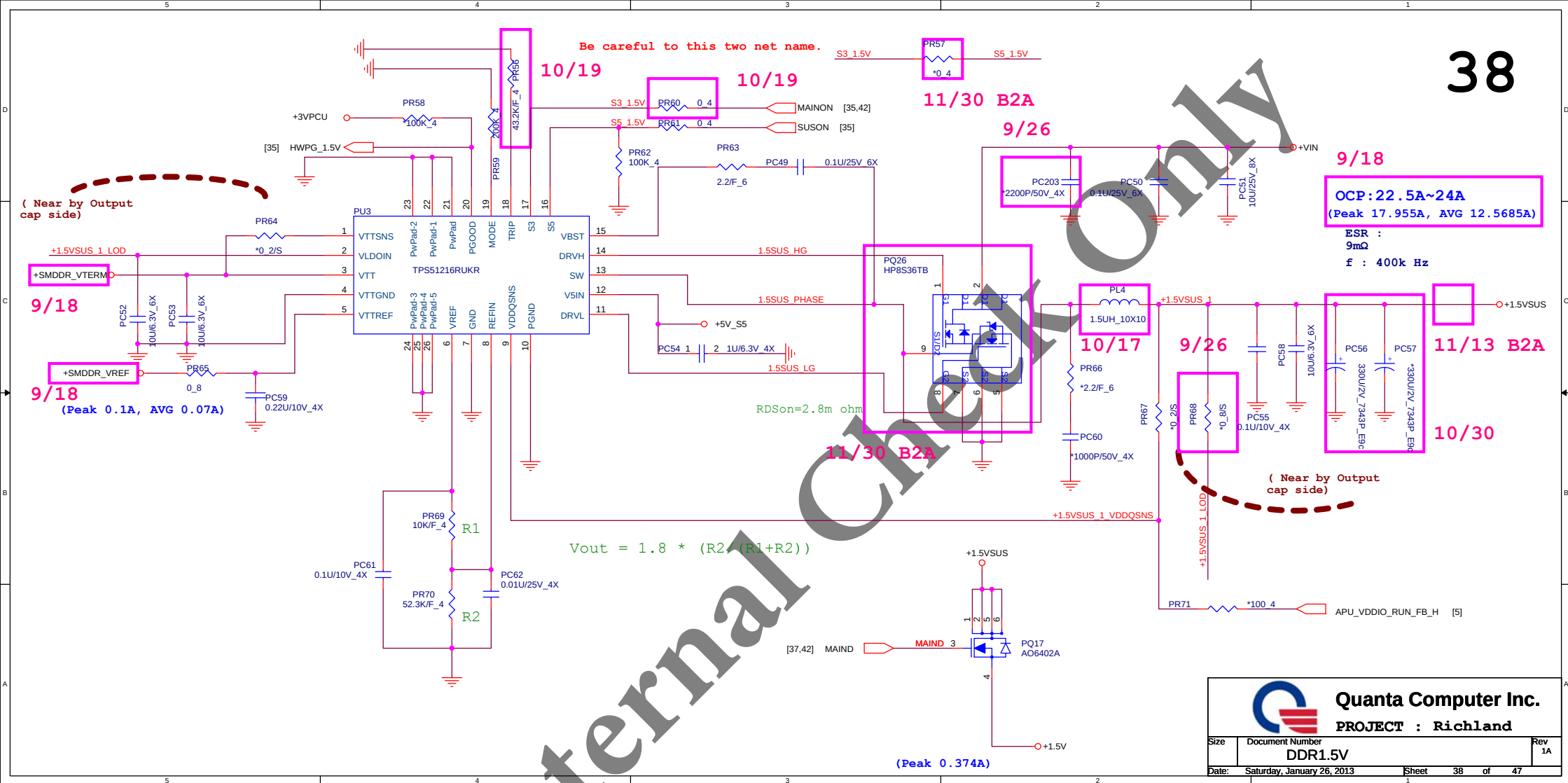
R3510

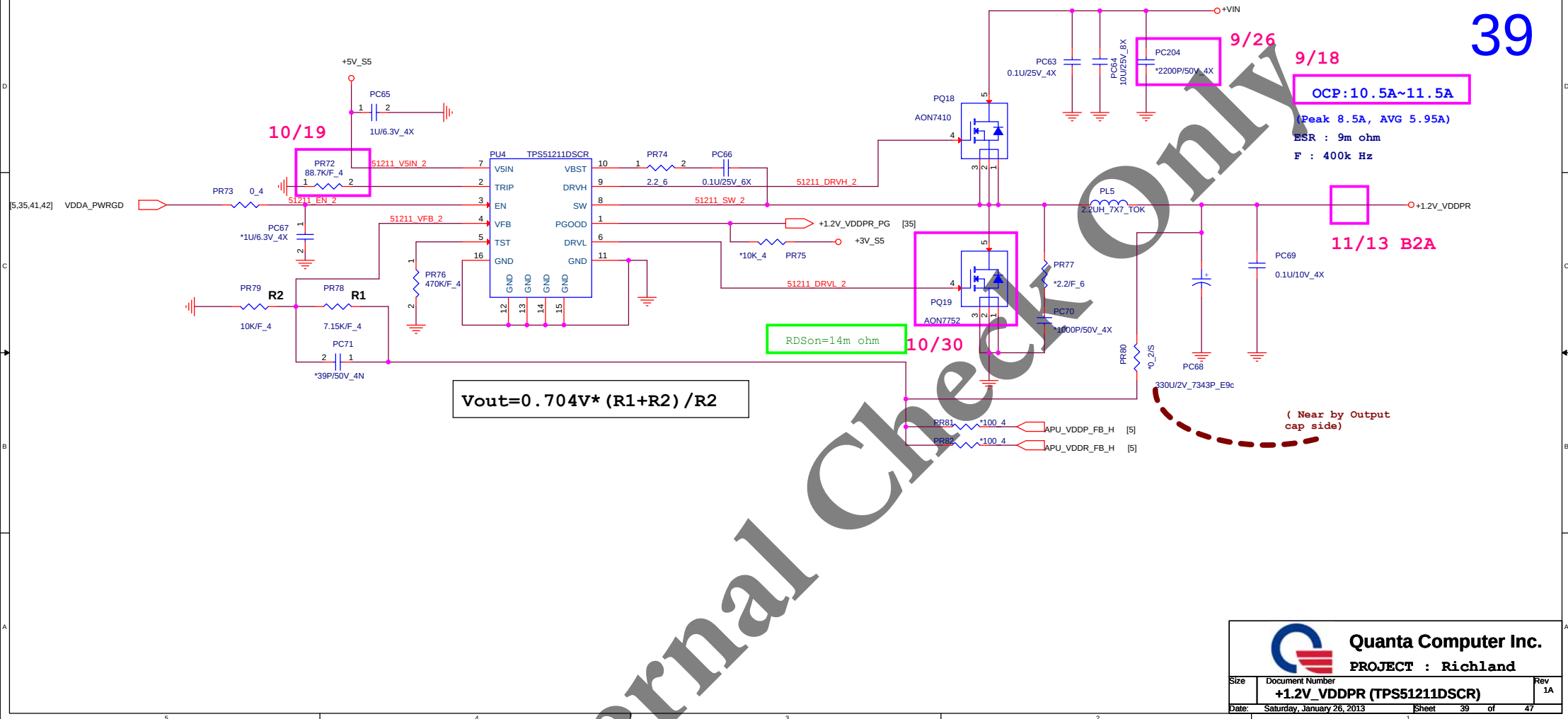
10K 4

R3510



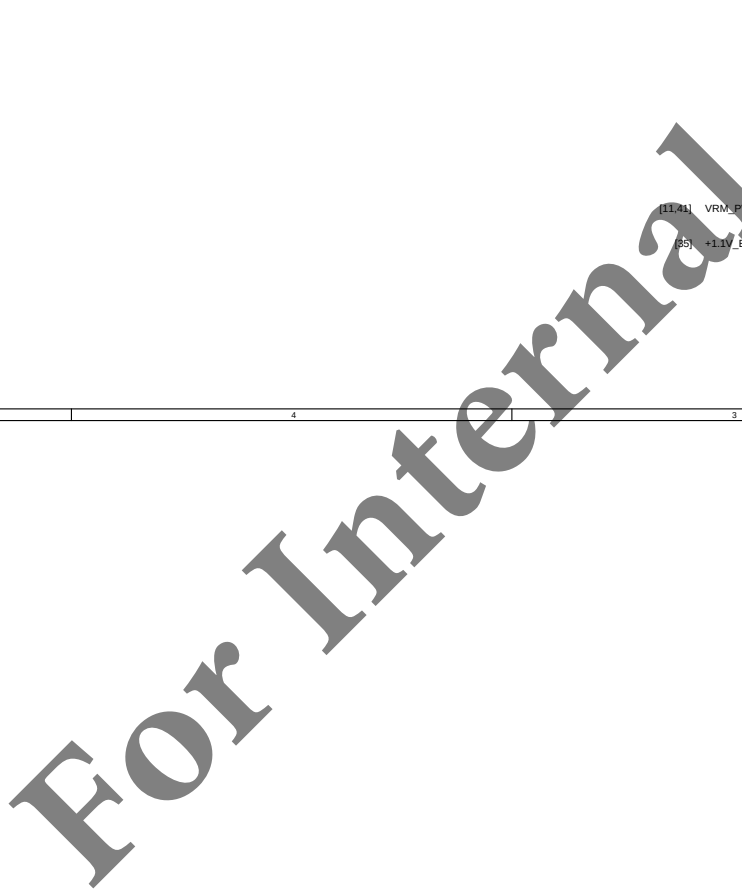






Quanta Computer Inc.
PROJECT : Richland

Size	Document Number	Rev
	+1.2V_VDDPR (TPS51211DSCR)	1A
Date:	Saturday, January 26, 2013	Sheet 39 of 47



$$V_{out} = 0.704V * (R1 + R2) / R2$$

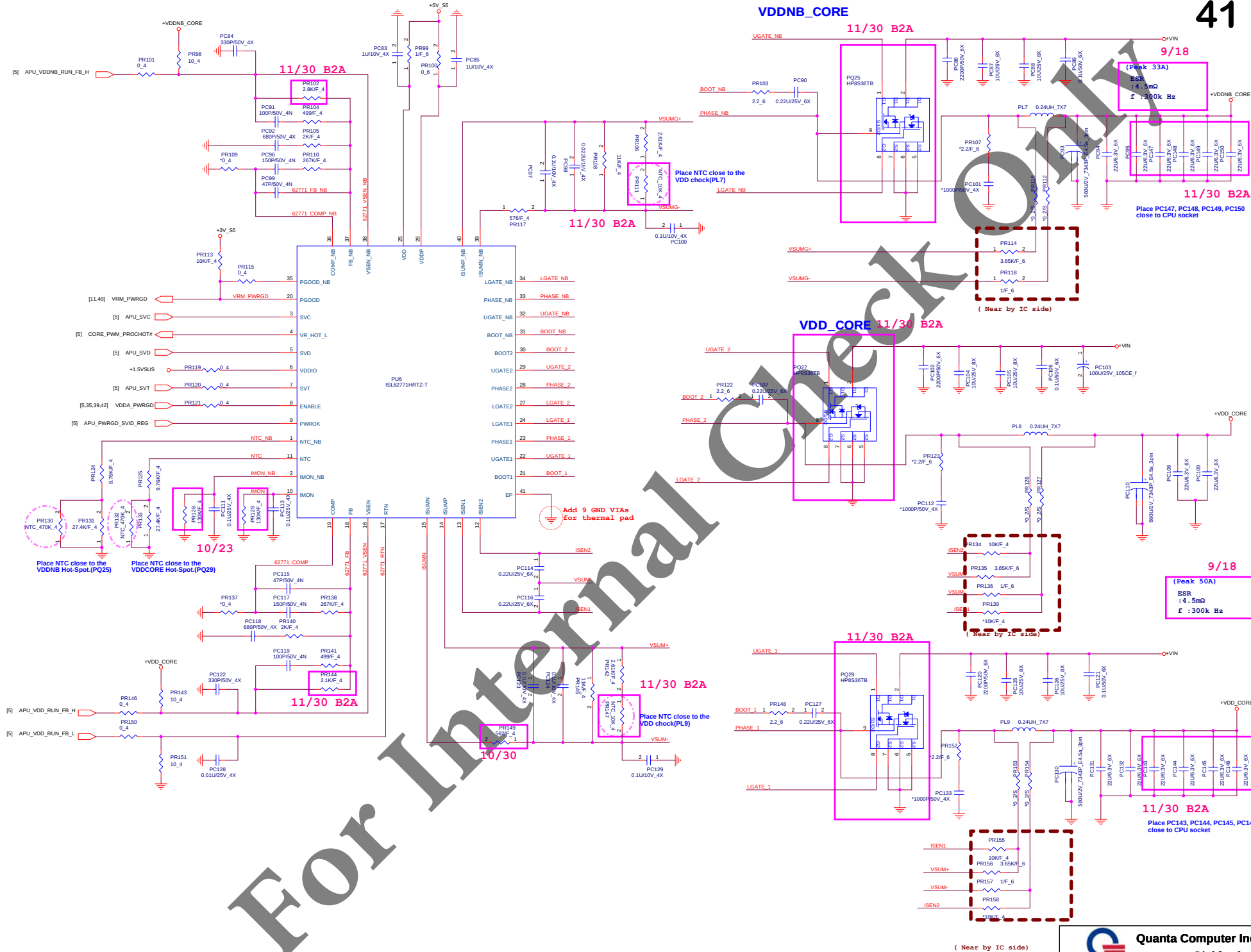
OCP: 6.5A~7.5A
(Peak 5.145A, AVG 3.6A)
ESR : 9m ohm
F : 290k Hz

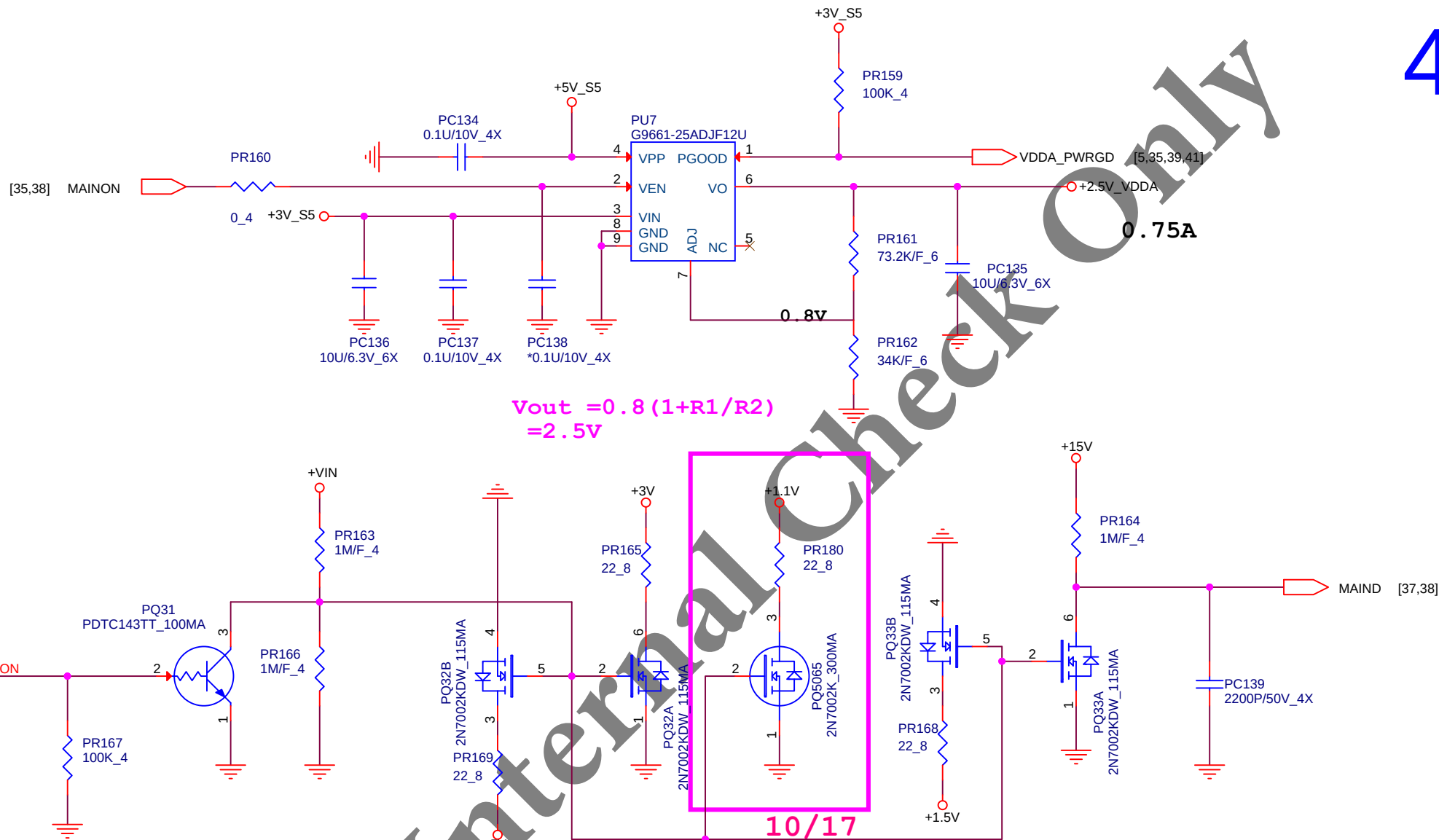
11/13 B2A

(Near by Output
cap side)

(Peak 4A)

 Quanta Computer Inc. PROJECT : Richland		
Size	Document Number	Rev
	+1.1V_DUAL (TPS52121DSCR)	1A
Date:	Saturday, January 26, 2013	Sheet 40 of 47

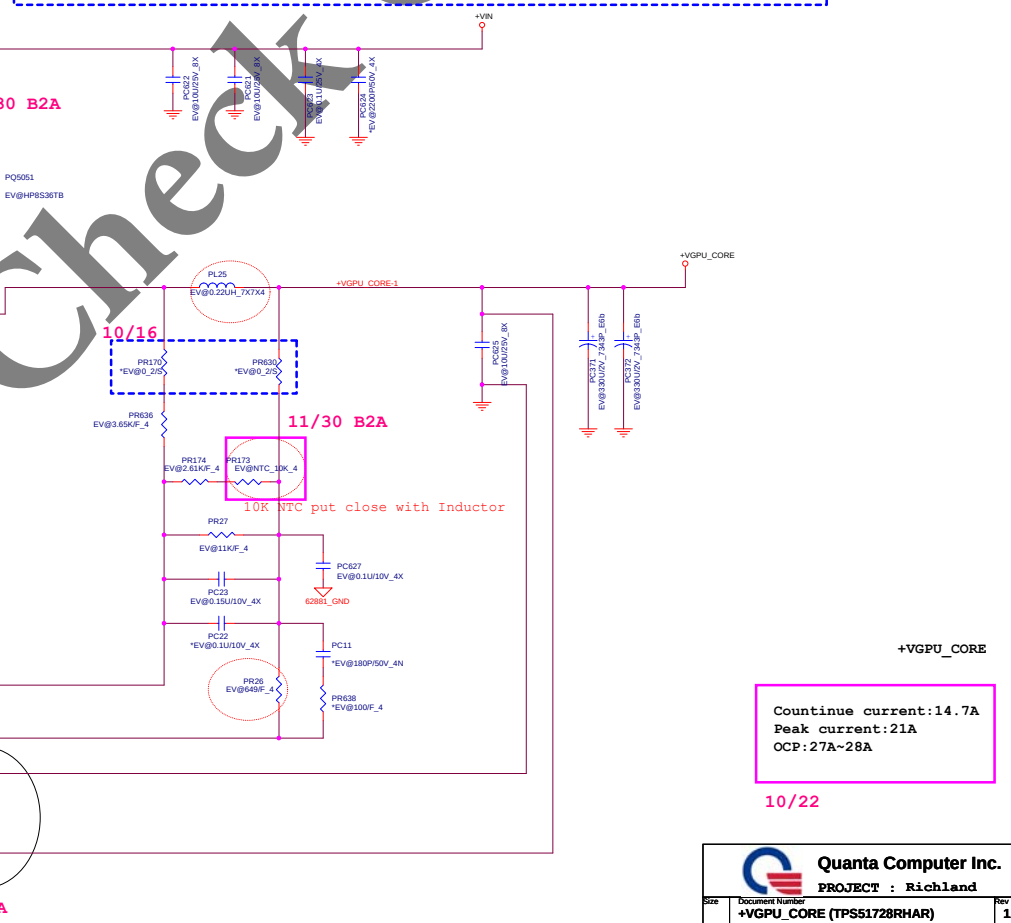


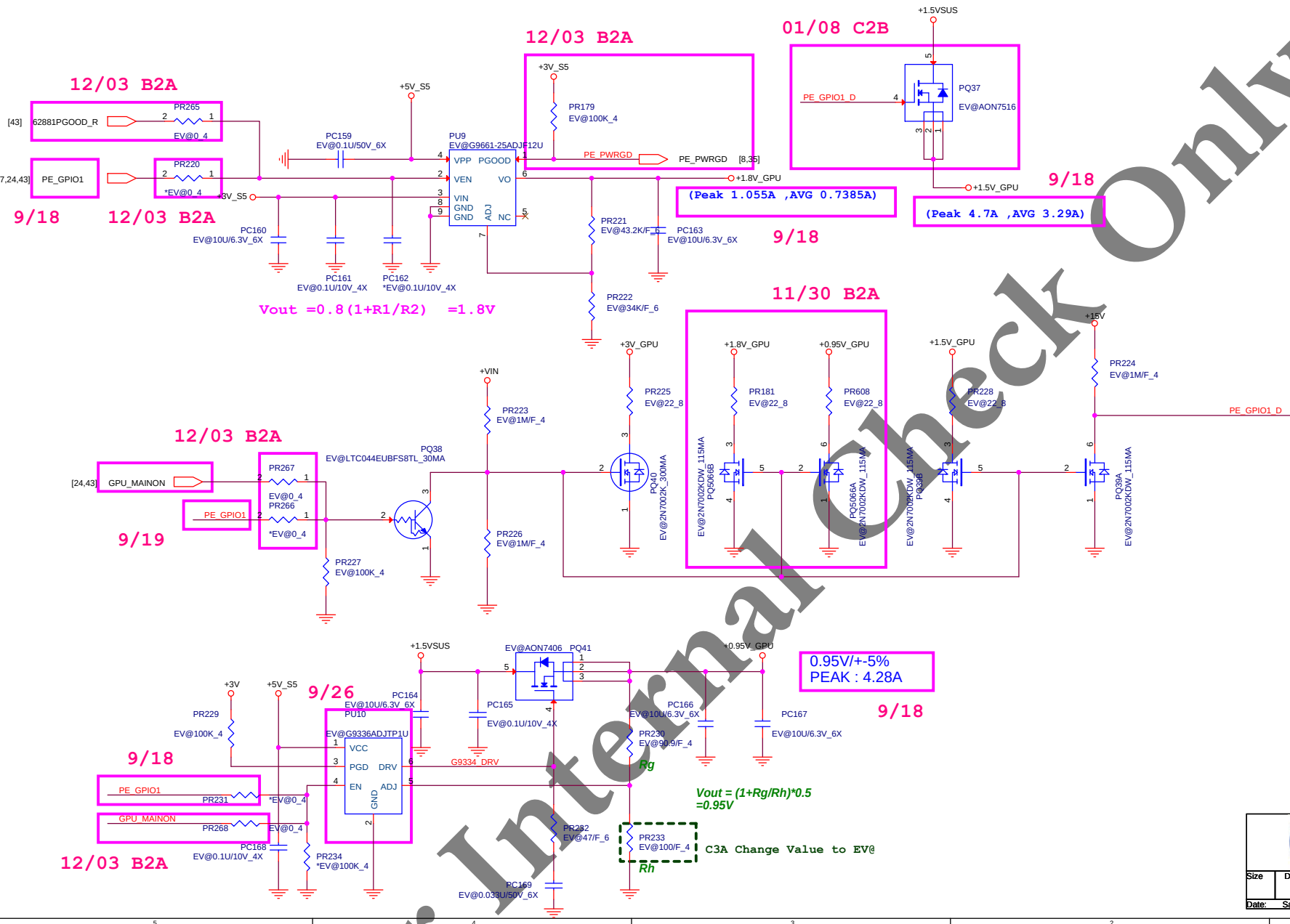


Quanta Computer Inc.
PROJECT : Richland

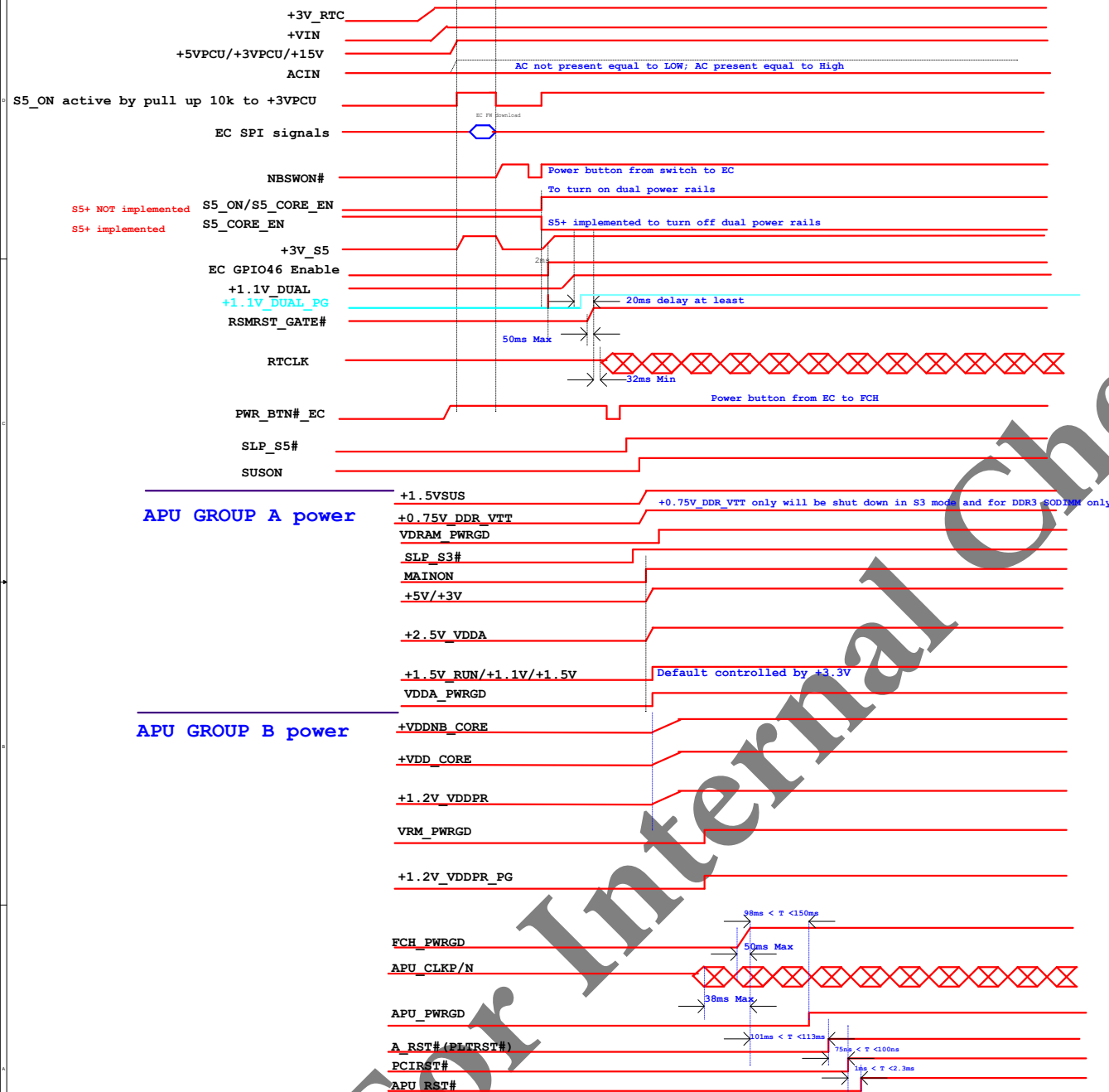
Size	Document Number	Rev
	DISCHARGE	1A
Date:	Saturday, January 26, 2013	Sheet 42 of 47

VDDC (V)	GFX_CORE_CNTRL4 (VID5) (GPIO_6)	GFX_CORE_CNTRL3 (VID4) (GPIO_30)	GFX_CORE_CNTRL2 (VID3) (GPIO_29)	GFX_CORE_CNTRL1 (VID2) (GPIO_20)	GFX_CORE_CNTRL0 (VID1) (GPIO_15)
1.125	0	1	1	1	1
1.100	1	0	0	0	0
1.075	1	0	0	0	1
1.050	1	0	0	1	0
1.025	1	0	0	1	1
1.000	1	0	1	0	0
0.975	1	0	1	0	1
0.950	1	0	1	1	0
0.925	1	0	1	1	1
0.900	1	1	0	0	0
0.875	1	1	0	0	1
0.850	1	1	0	1	0
0.825	1	1	0	1	1
0.800	1	1	1	0	0
0.775	1	1	1	0	1





BD8/BD8D Power On Sequence: S5 > S0



APU Power on sequence required:

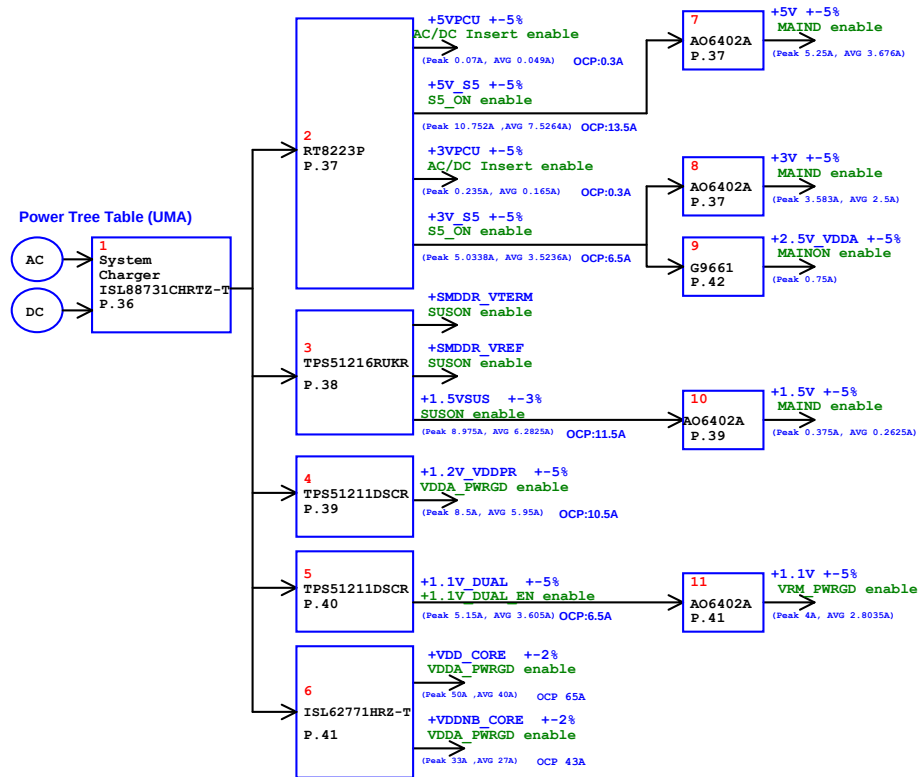
Llano APU:

1.Group A (+1.5VSUS, +2.5V_VDDA) ramp before Group B
(+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

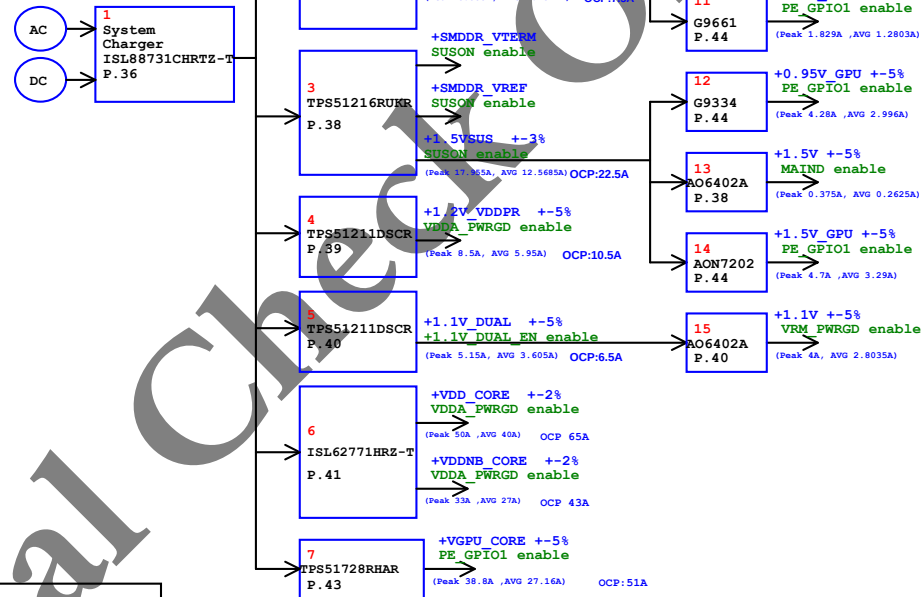
HUDSON-M2/M3:

1.+3V_S5 ramp before +1.1V_DUAL
2.+3V ramp before +1.1V
3.+3V_RTC must ramp at least 5 secs before the +3V_S5

Power Tree Table (UMA)



Power Tree Table (DIS)



Power Distribution List

Power	Distribution

Model	REV	CHANGE LIST					MODEL	BY6D
BY6D MB	A1A						PAGE	FROM
							1	A1A
							2	A1A
							3	A1A
							4	A1A
							5	A1A
							6	A1A
							7	A1A
							8	A1A
							9	A1A
							10	A1A
							11	A1A
							12	A1A
							13	A1A
							14	A1A
							15	A1A
							16	A1A
							17	A1A
							18	A1A
							19	A1A
							20	A1A
							21	A1A
							22	A1A
							23	A1A
							24	A1A
							25	A1A
							26	A1A
							27	A1A
							28	A1A
							29	A1A
							30	A1A
							31	A1A
							32	A1A
							33	A1A
							34	A1A
							35	A1A
							36	A1A
							37	A1A
							38	A1A
							39	A1A
							40	A1A
							41	A1A
							42	A1A
							43	A1A
							44	A1A
							45	A1A
							46	A1A
DOC NO. 204	PROJECT MODEL :		BY6D	APPROVED BY:		DATE:	2011/10/02	
	PART NUMBER:			DRAWING BY:	Wei-Sheng	REVISION:	A1A	