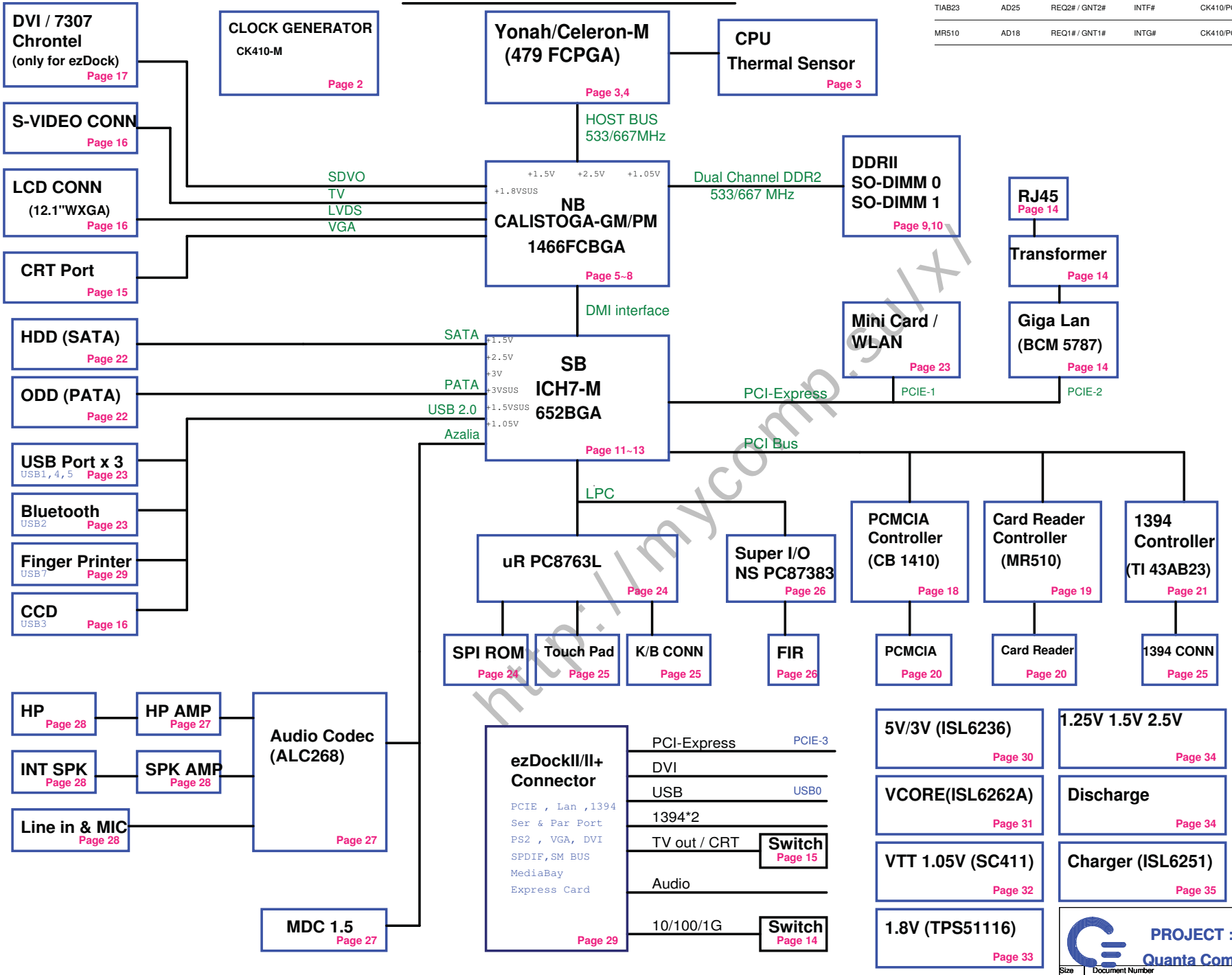
ZU2 SYSTEM BLOCK DIAGRAM

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
CB1410	AD17	REQ0# / GNT0#	INTE#	CK410/PCI3
TIAB23	AD25	REQ2# / GNT2#	INTF#	CK410/PCI8
MR510	AD18	REQ1# / GNT1#	INTG#	CK410/PCI4



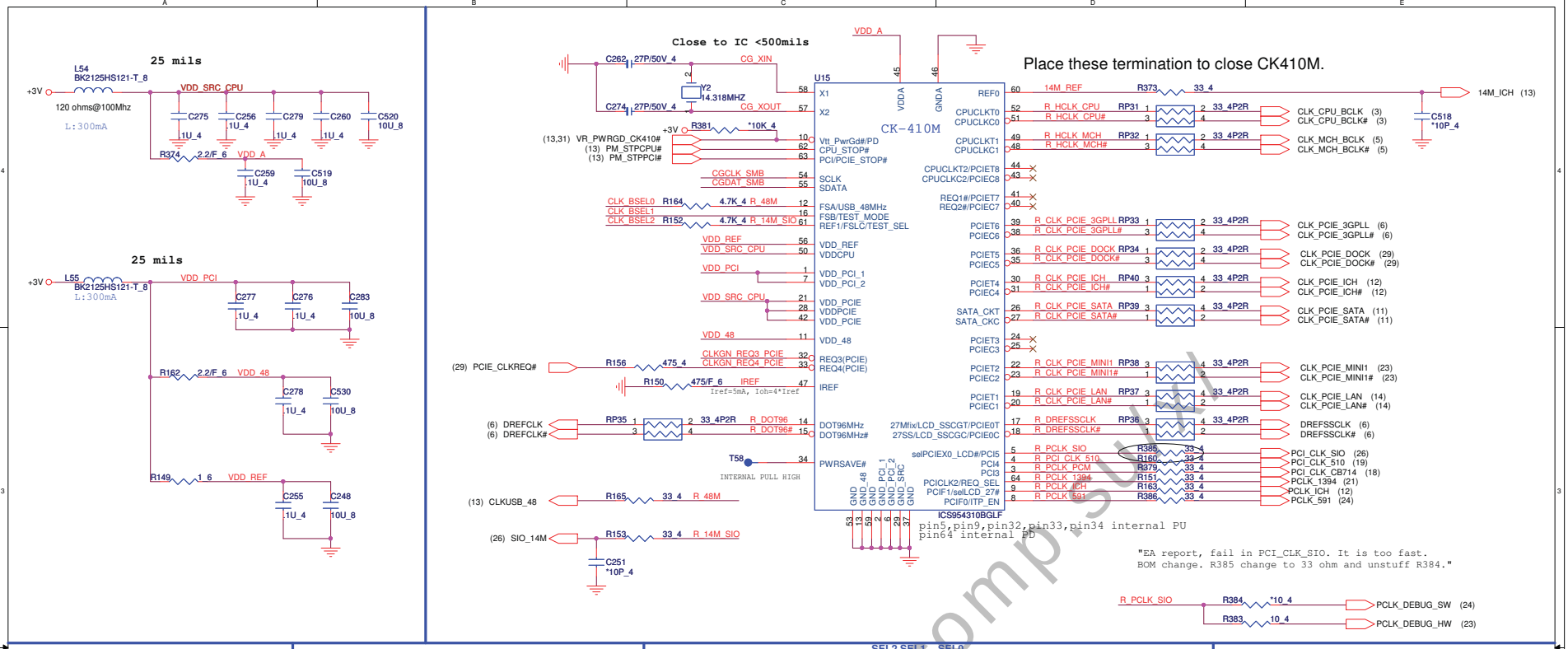
PROJECT : ZU2

Quanta Computer Inc.

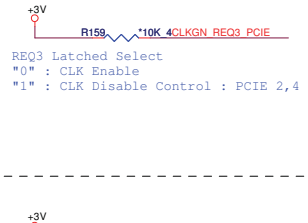
Size	Document Number	Rev
	Block Diagram	1A

Date: Wednesday, March 21, 2007 Sheet 1 of 39

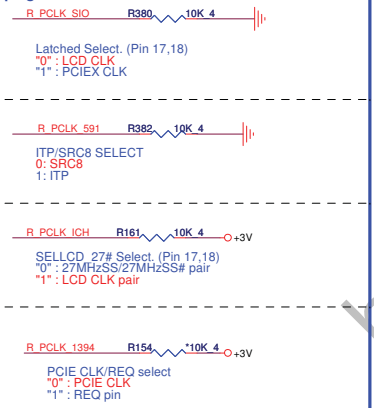
http://mycomp.su/xi



PCIE CLK enable/disable control



Starpping

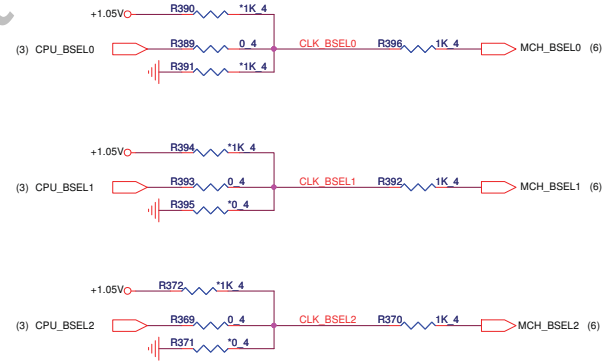


Frequence select

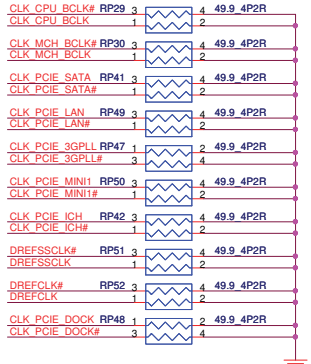
SEL2 SEL1 SEL0

FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	
0	0	1	133	100	33	
0	1	1	166	100	33	Default
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	200	100	33	

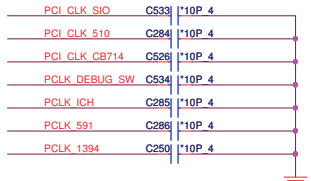
BSEL strappings need to be set for 533MHz Moby Dick
(Intel7915GM - Calistoga Interposer)
(if Calistoga is designed for 667MHz board).



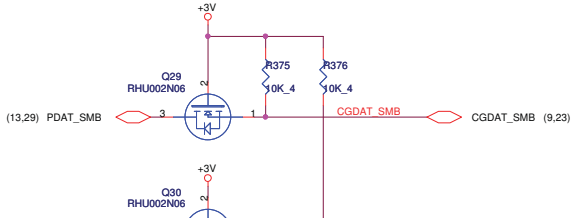
Terminal Resistor



Reserve for EMI



SM BUS level shift



PCLK_SMB/PDAT_SMB(SB&LAN&MINI CARD&EZ,+3V_S5) CGCLK_SMB/CGDAT_SMB(CLK GEN&DDR,+3V)

Power check

+3V (3,6,8,9,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,29,30,31,32,34)
+1.05V (3,4,5,8,11,13,31,32,34)

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	Clock Gen.	1B
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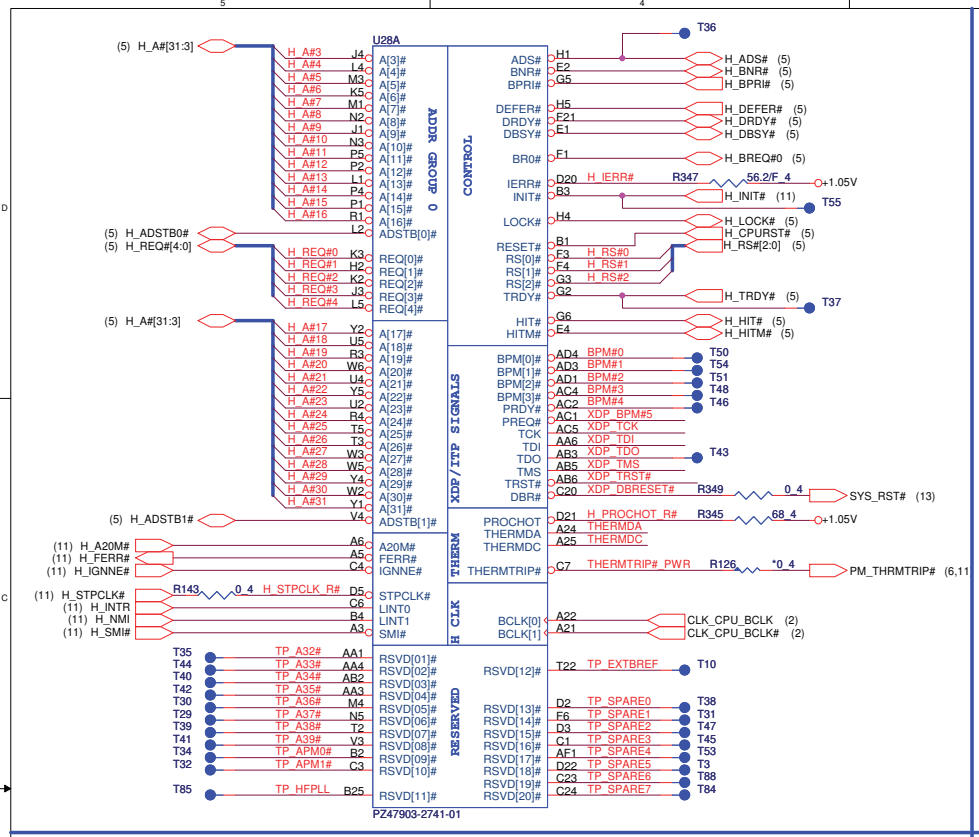
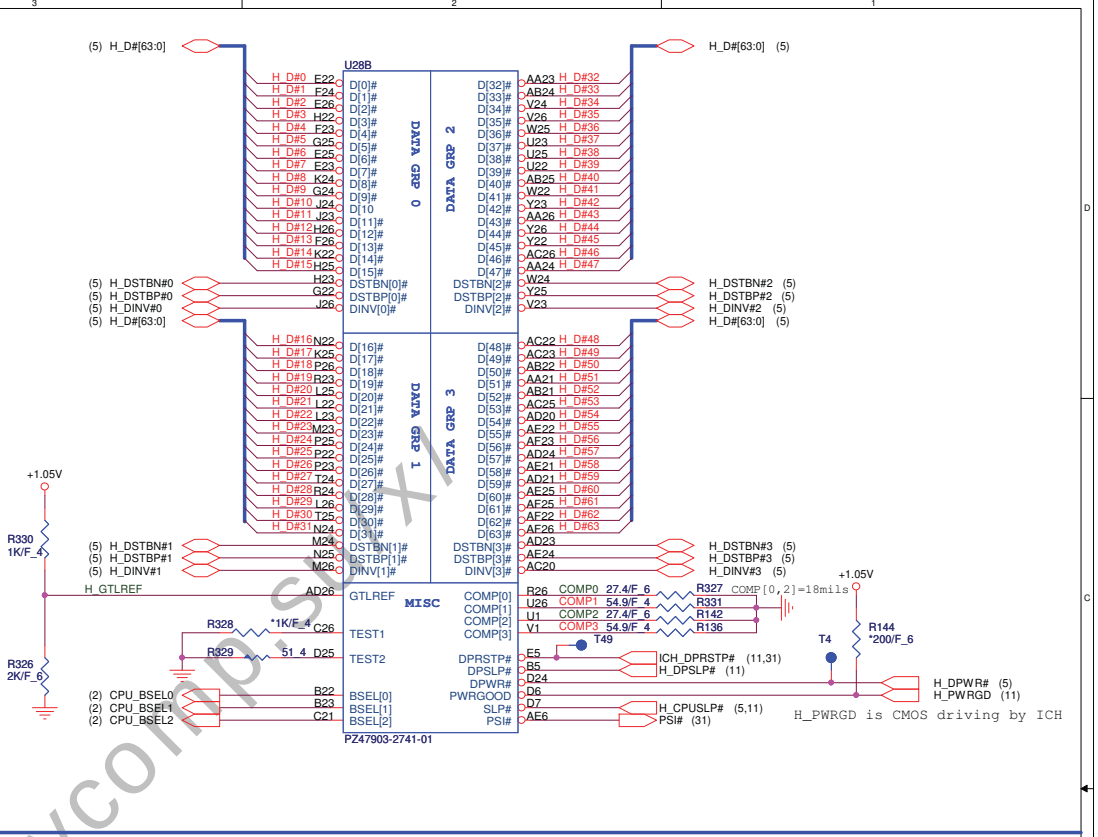
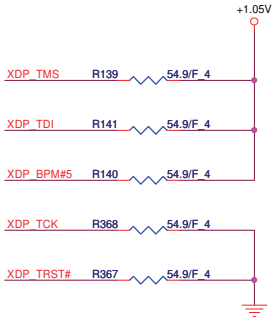
http://mycomp.su/

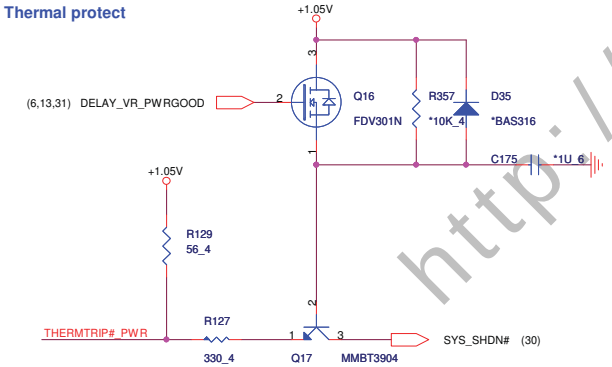




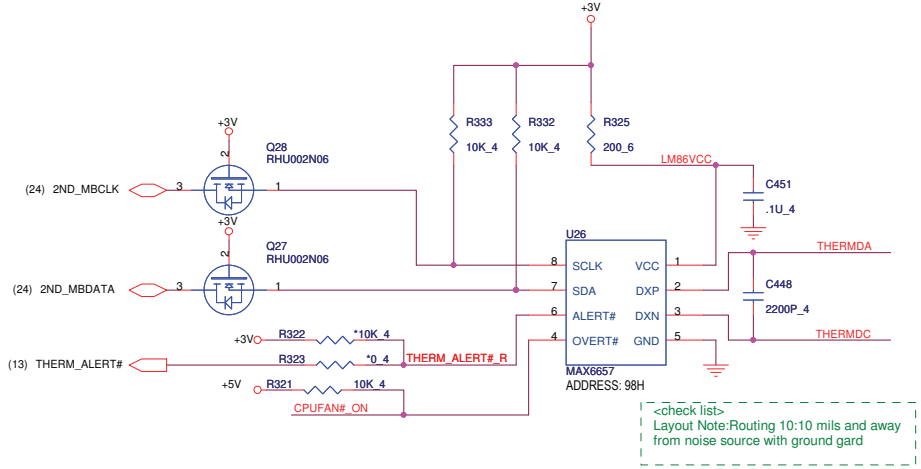
XDP/ITP



Thermal protect

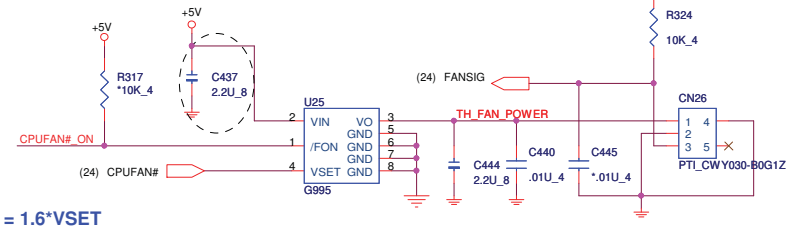


CPU Thermal monitor



CPU FAN

ZU2 change C437 from 10U_8 to 2.2U_6(1/26)
Add one 2.2uF in U46 G955's VIN.GMT request to add it.

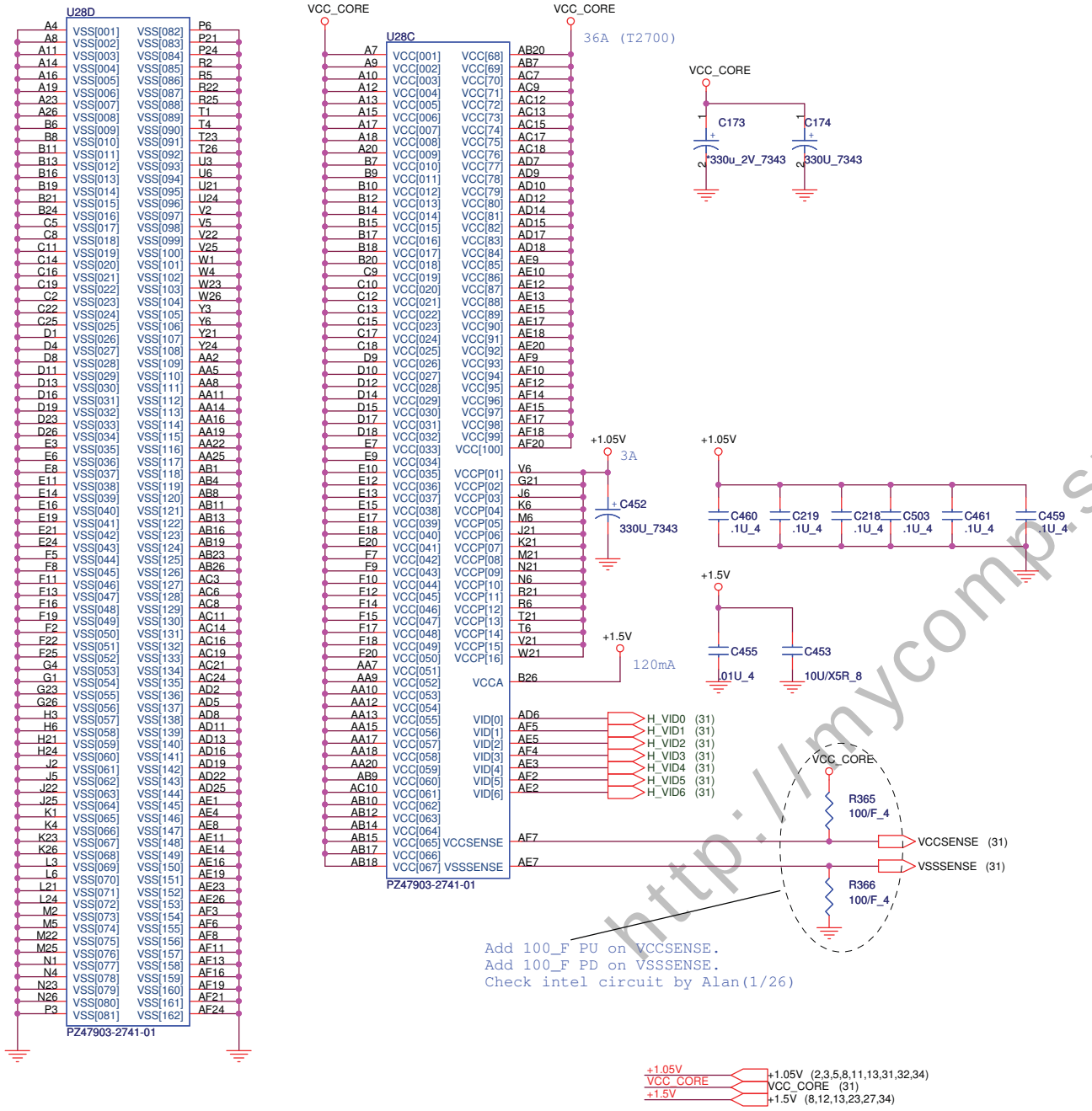


FANPWR = 1.6*VSET

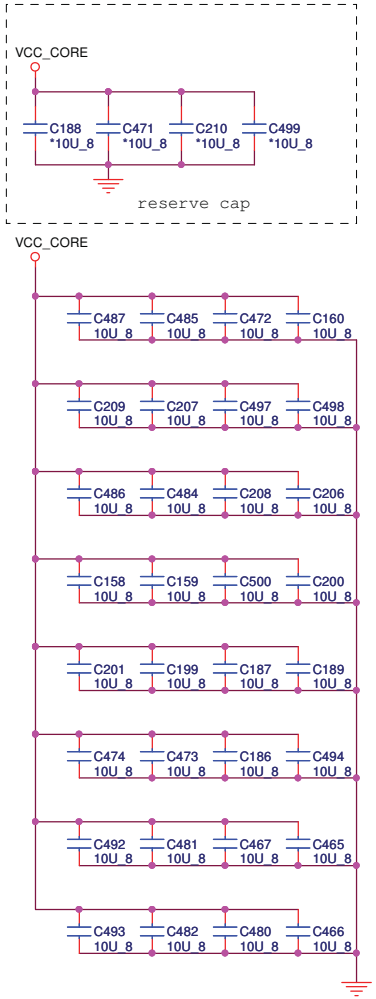
G995/Pin1- internal pull high (+5V)

PROJECT : ZU2		
Quanta Computer Inc.		
Size	Document Number: YOHNA (HOST)	Rev 1A
Date: Thursday, March 22, 2007	Sheet 3 of 39	

http://mycomp.sk/



VCC_CORE CAP.



http://mycomp.su/xl

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	Yonah/Merom CPU(POWER/GND)-2	1A

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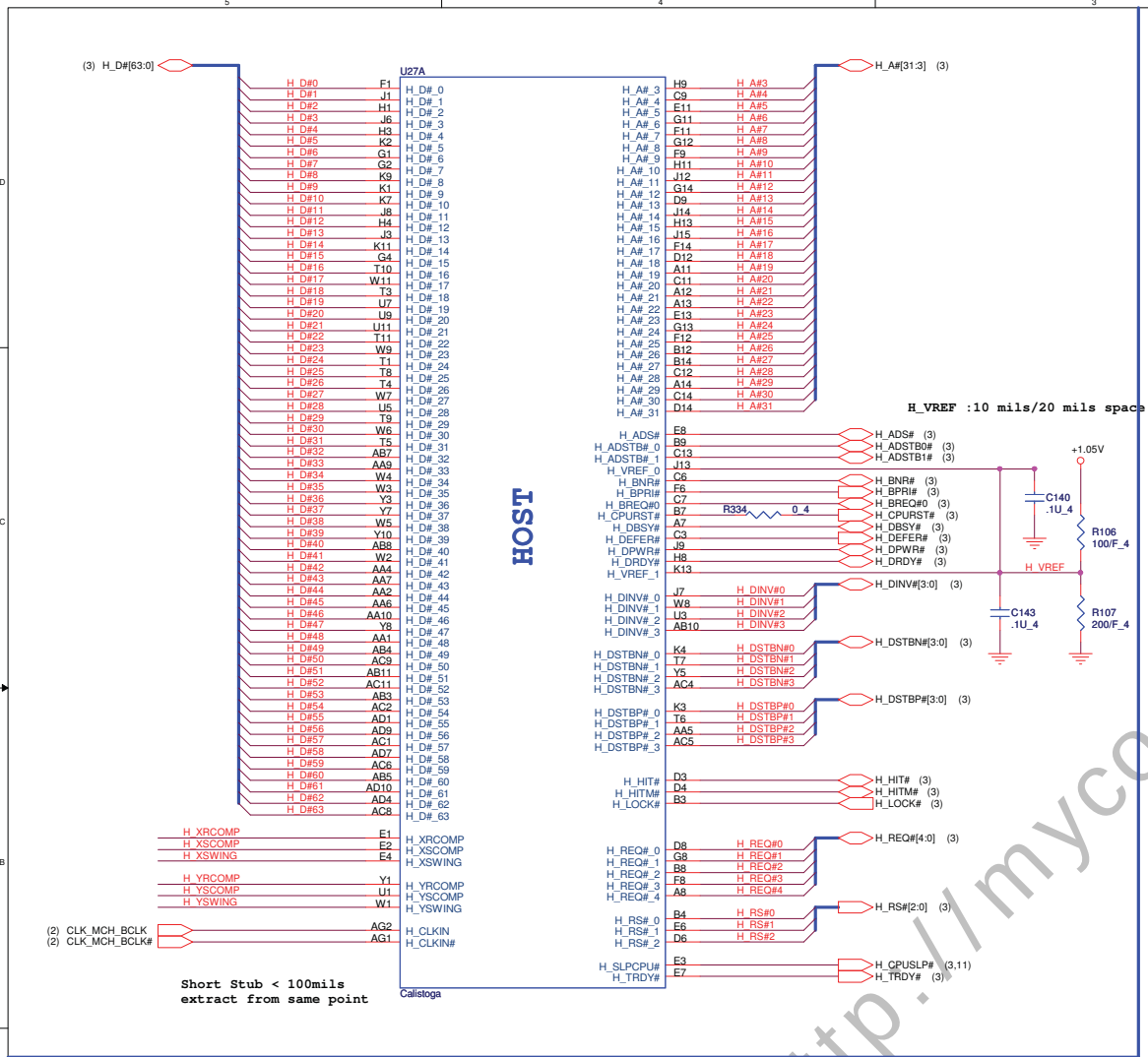
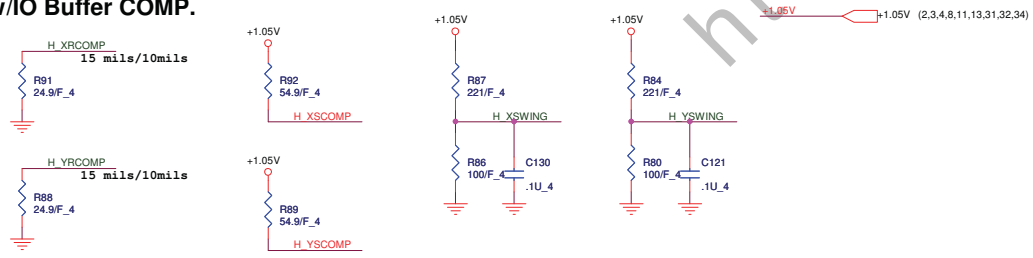
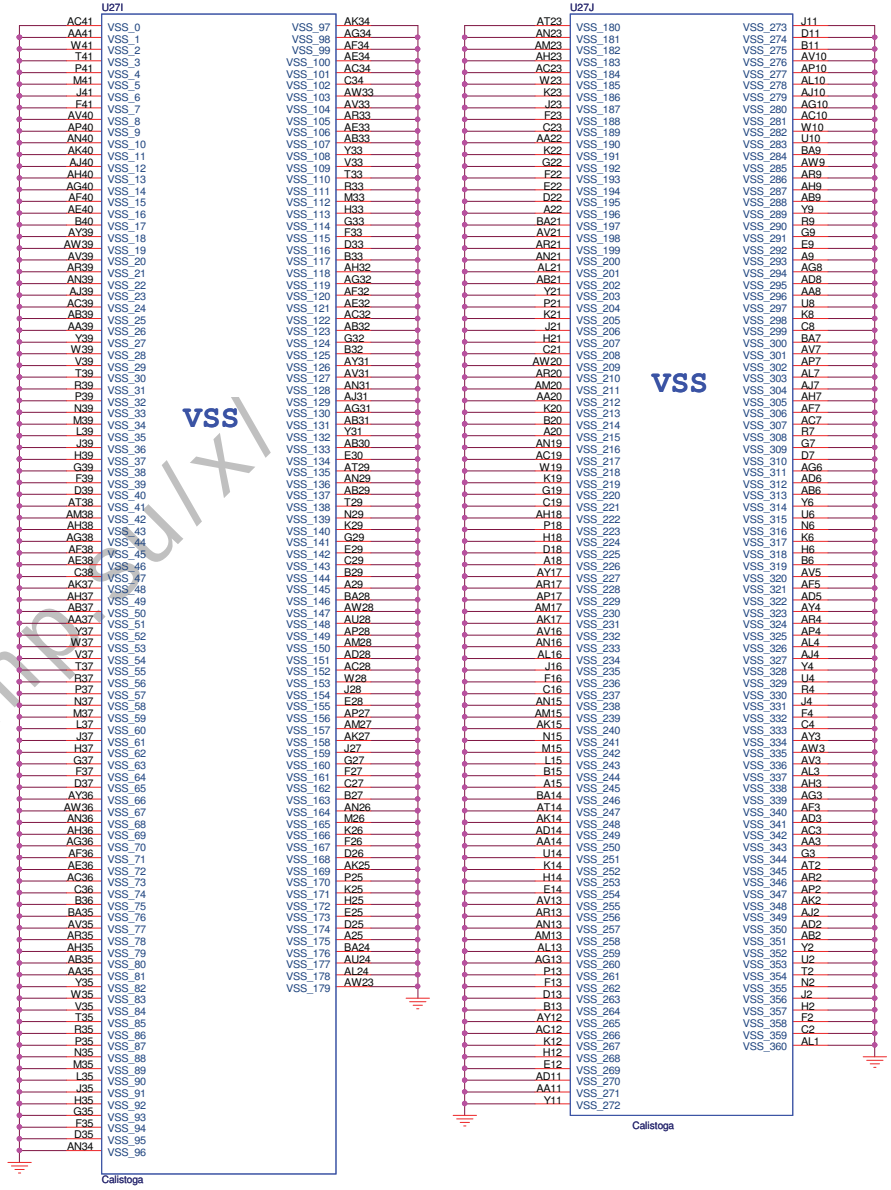


Slew/IO Buffer COMP.





COMPONENTS	P/N
945GM	AJSL8Z20T25
ICH7-M	AJSL8YB0T21

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (HOST/GND)	1A

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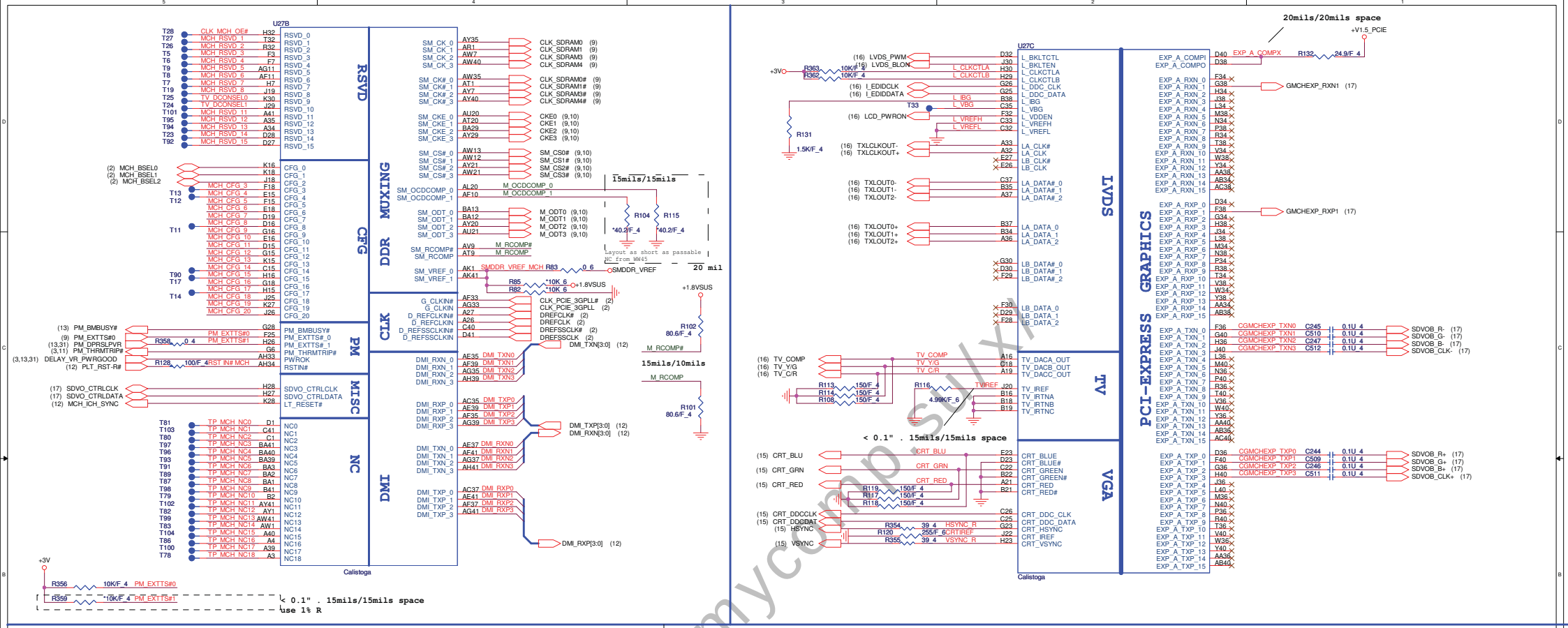
http://mycomputer/xl



GMCH Strap pin

CFG[3..17] has internal PU

MCH_CFG_5 R341 *2.2K_4

MCH_CFG_5 DMI speed mode
Low = DMI X2
High=DMIX4

MCH_CFG_6 R348 *2.2K_4

MCH_CFG_6 DDR
Low =Moby Dick
High= Calistoga (Default)

MCH_CFG_7 R112 *2.2K_4

MCH_CFG_7 CPU Strap
Low=RSVD
High=Mobile CPU

MCH_CFG_9 R111 *2.2K_4

MCH_CFG_9 PCI Exp Graphics Lane
Low =Reserved
High=Normal

MCH_CFG_10 R346 *2.2K_4

MCH_CFG_10 Host PLL VCC Select
Low=Reserved
High=Mobility

MCH_CFG_11 R343 *2.2K_4

MCH_CFG_11 PSB 4x CLK ENABLE
Low=Reserved
High=Calistoga

MCH_CFG_12 R336 *2.2K_4

MCH_CFG_13 R109 *2.2K_4

MCH_CFG_12,13 XOR/ALLZ
0,0=Partial clock gating disable
0,1=All-Z mode enable
1,0=XOR mode enable
1,1=Normal

MCH_CFG_16 R344 *2.2K_4

MCH_CFG_16 FSB Dynmic ODT
Low=Dynamic ODT Disabled
High=Dynamic ODT Enabled.

CFG[18..20] has internal PD

MCH_CFG_18 R360 *1K/F_4 +3V

MCH_CFG_18 VCC Select
LOW=1.05V
High=1.5V

MCH_CFG_19 R361 *1K/F_4 +3V

MCH_CFG_19 DMI LANE Reversal
Low=Normal
High=LANES Reversed

MCH_CFG_20 R364 *1K/F_4 +3V

MCH_CFG_20 PCIE Backward interpoerability mode
Low= only SDVO or PCIE x1 is operational (defaults)

High=SDVO and PCIE x1 are operation simultaneously via the PEG port

+V1.5_PCIE (8)
+3V (2,3,8,9,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,29,30,31,32,34)
SMDDR_VREF (9,33,34)
+1.8VSUS (8,9,33,34)

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (DMI&PCIE&VGA)	1A

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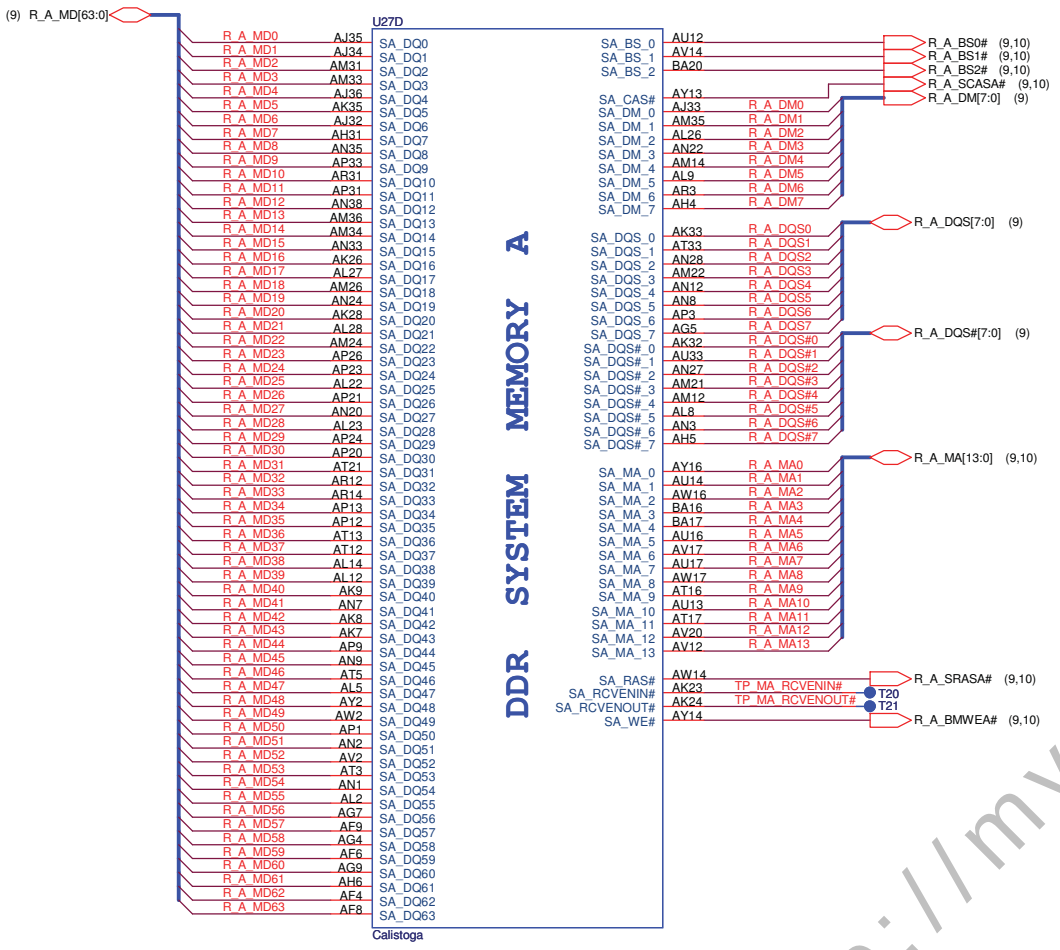
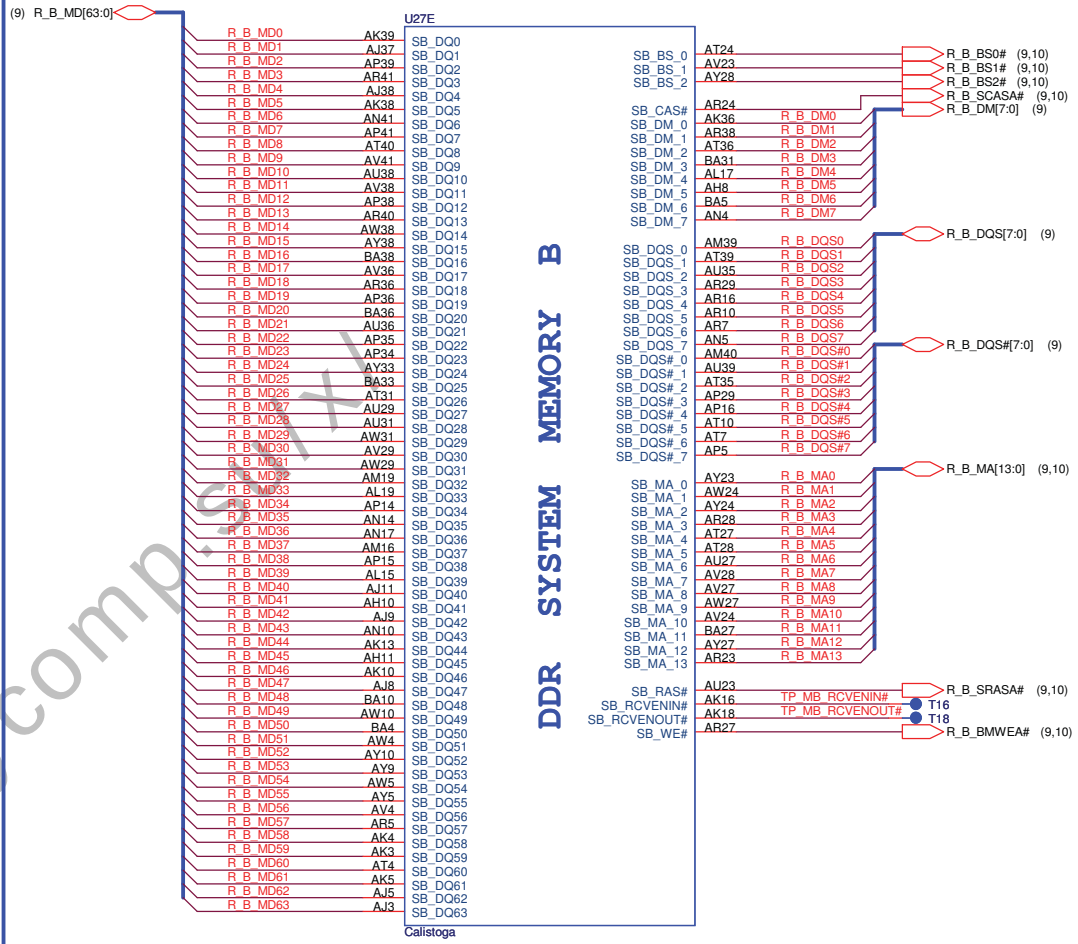
http://mycomp sulx/





http://mycomp.sx/

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (DDR2)	1A

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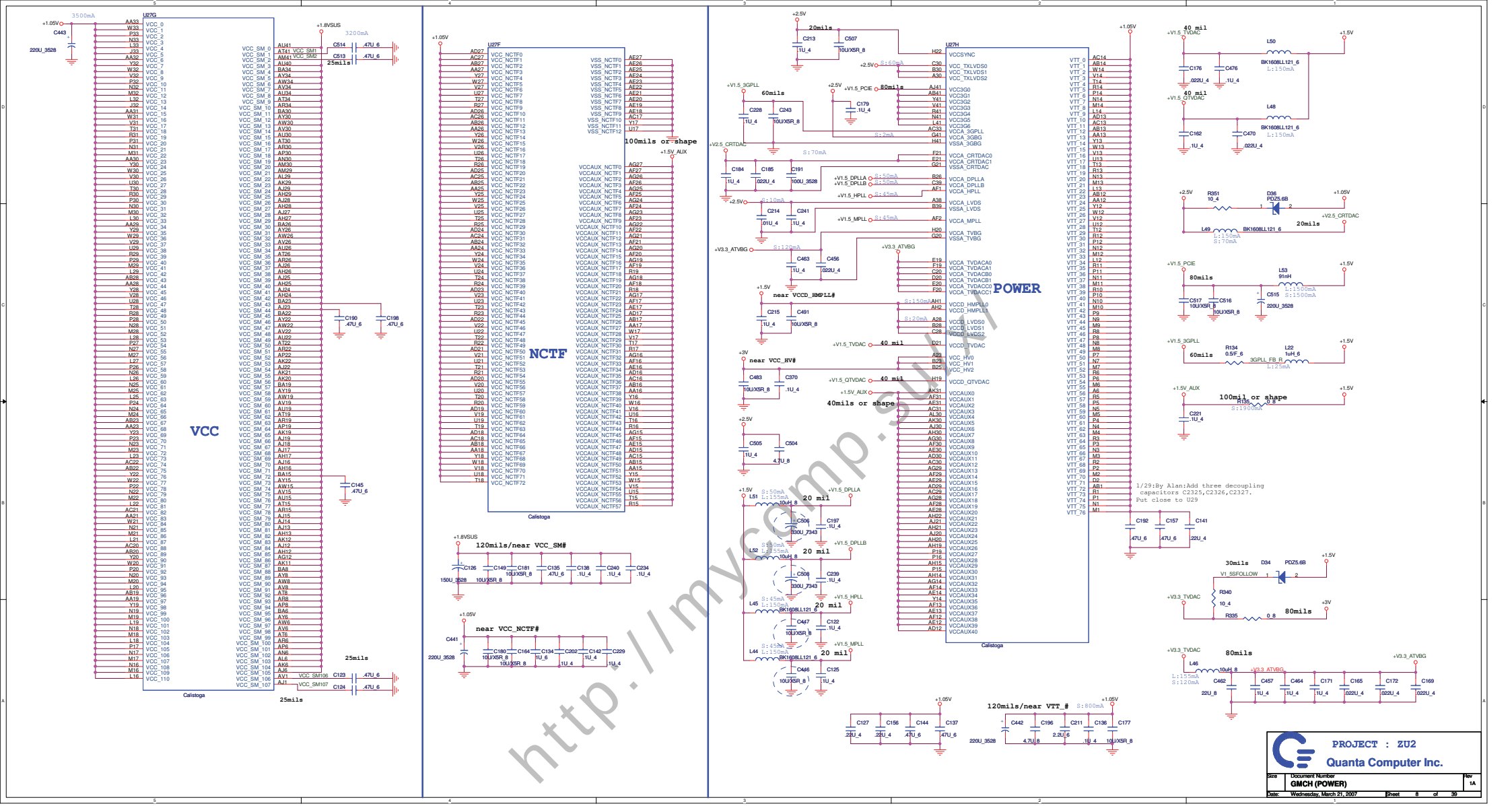

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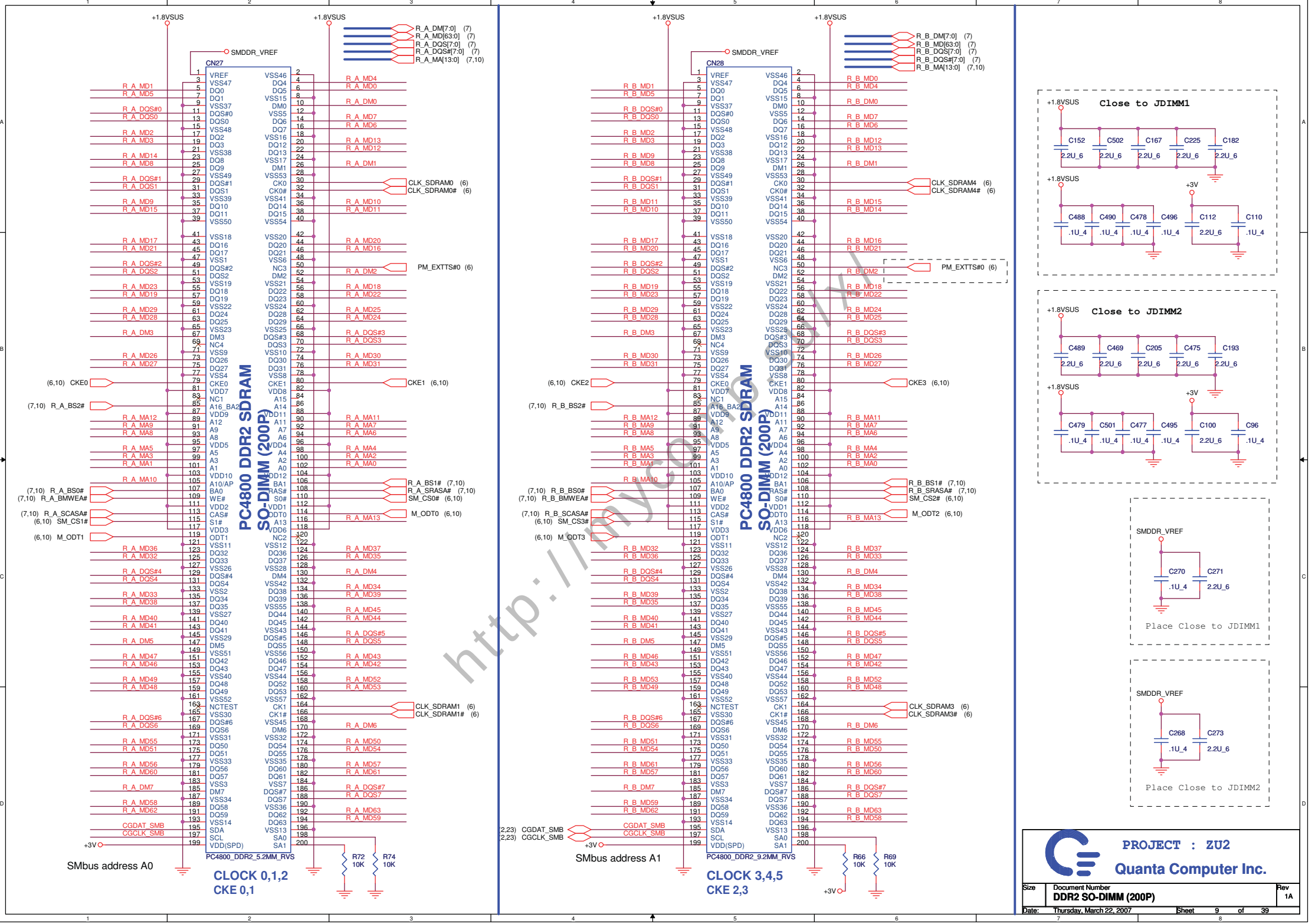

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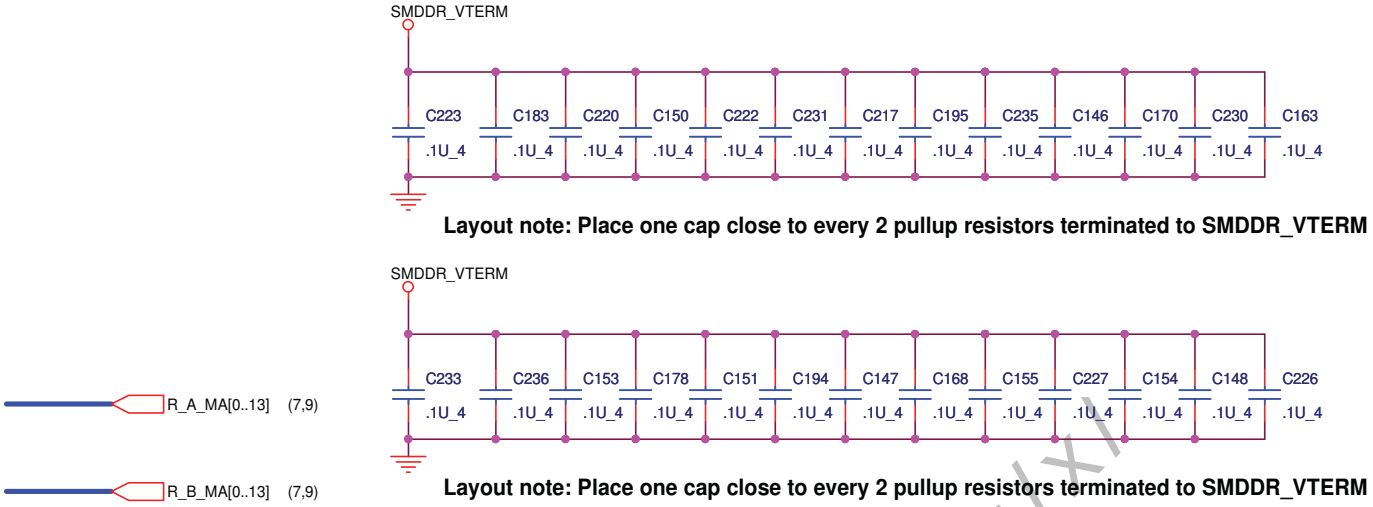

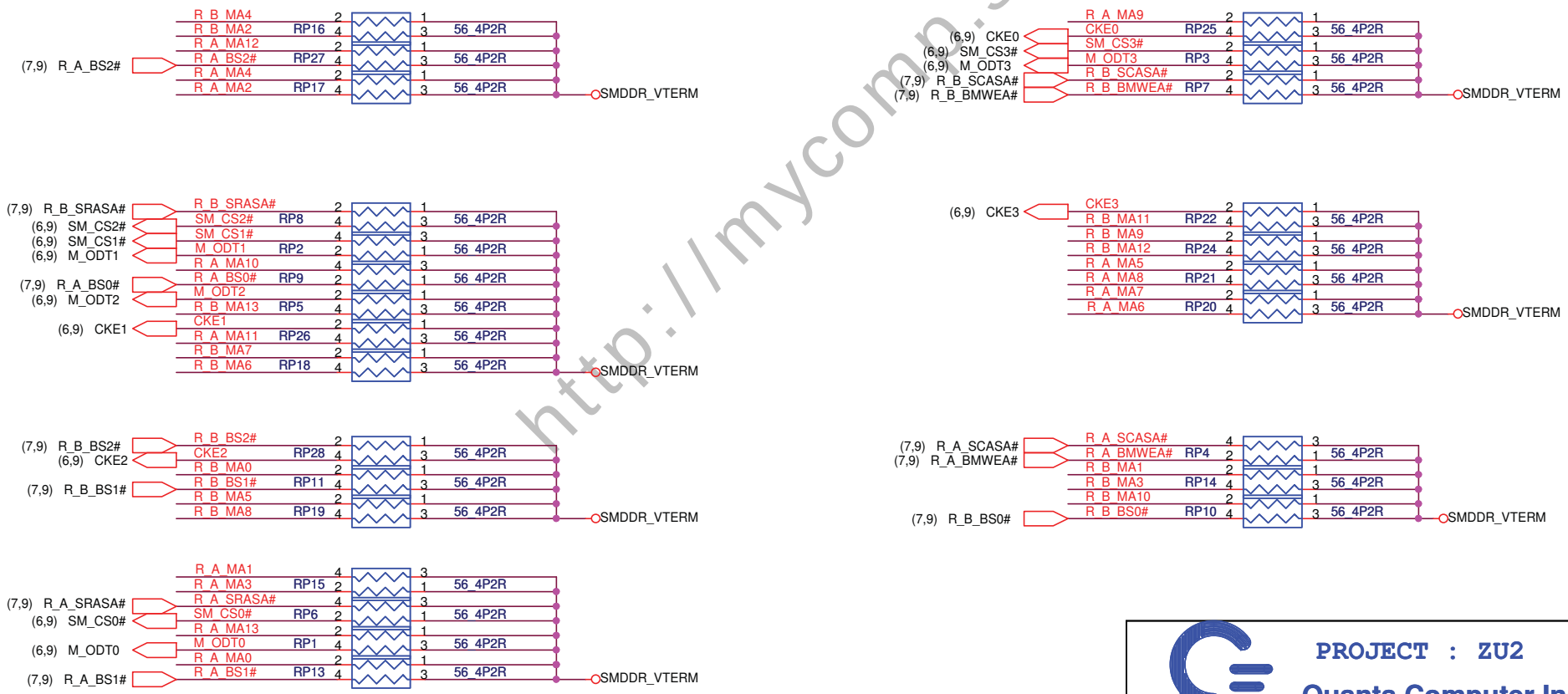

http://mycomp.su/xi/

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 RES. ARRAY	1A

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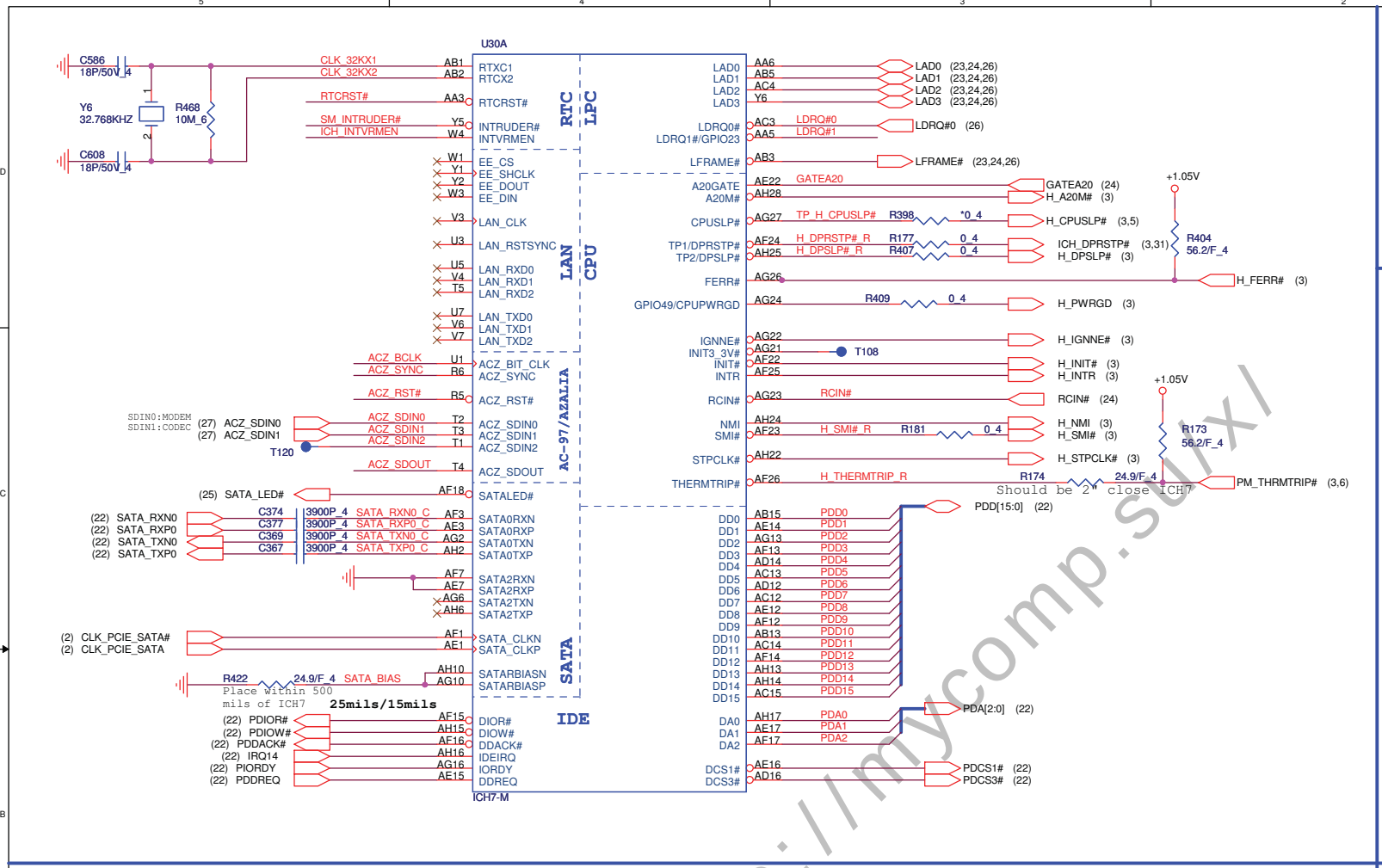
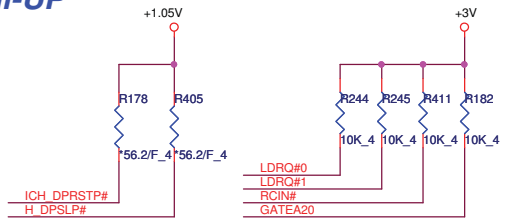
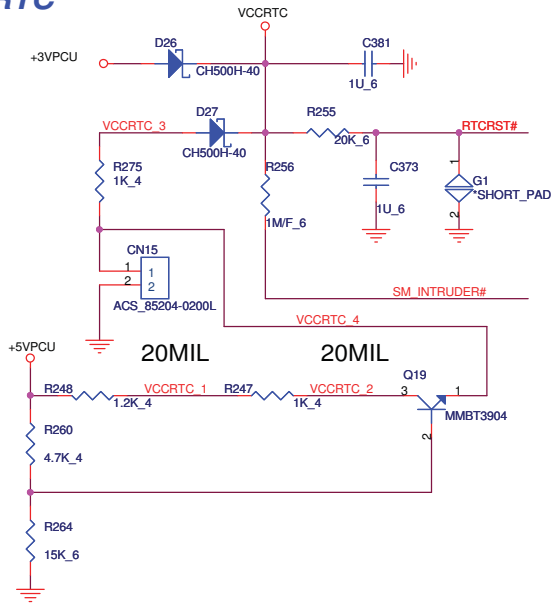


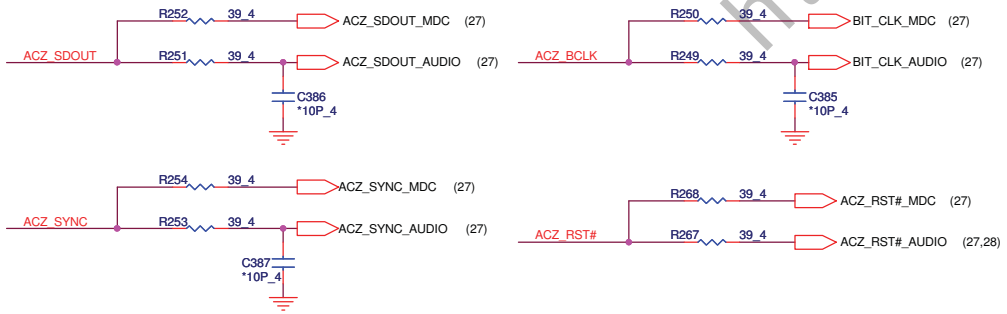
Pull-UP



RTC

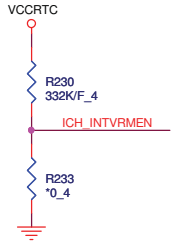


HDA interface



COMPONENTS	P/N
945GM	AJSL8Z20T25
ICH7-M	AJSL8YB0T21

ICH7 internal VR enable strap



	INTVRMEN
Enable (default)	1
Disable	0

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M (CPU, SATA, IDE,LPC)	1A

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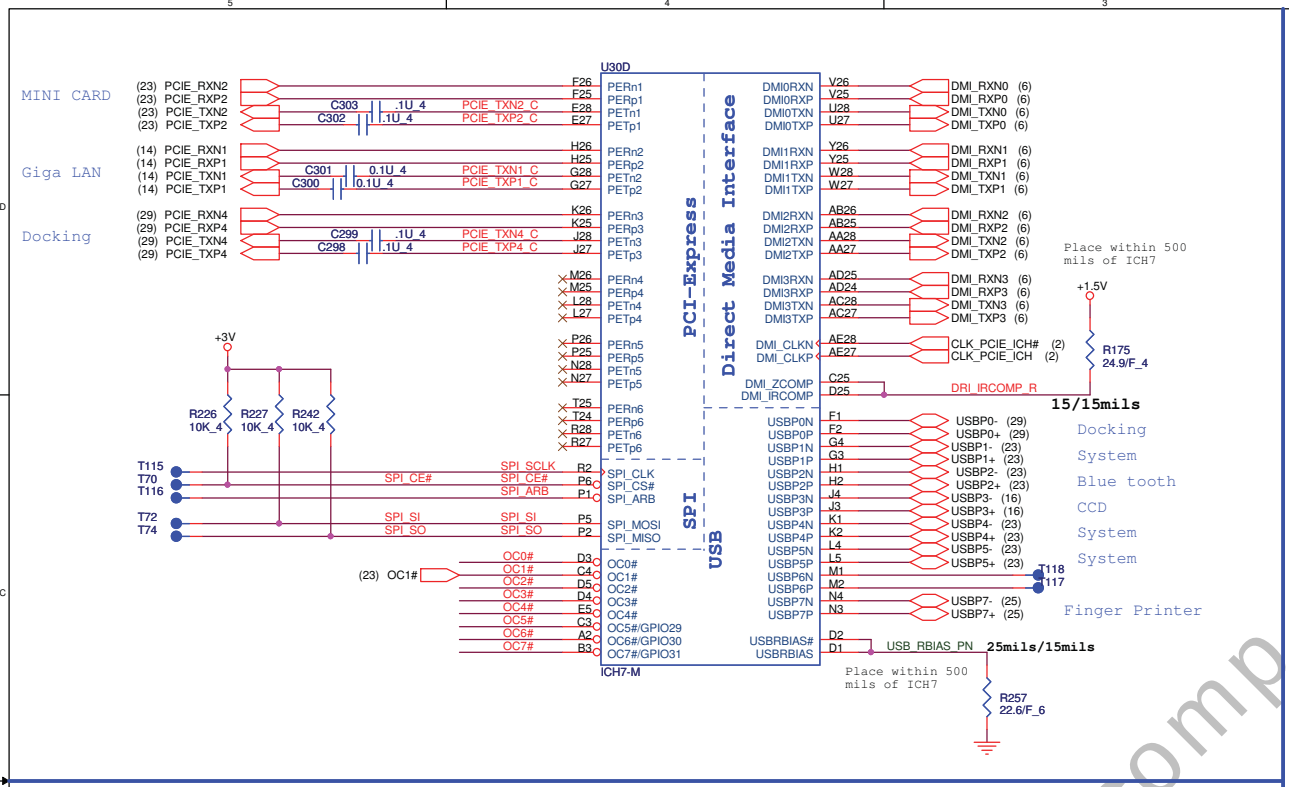
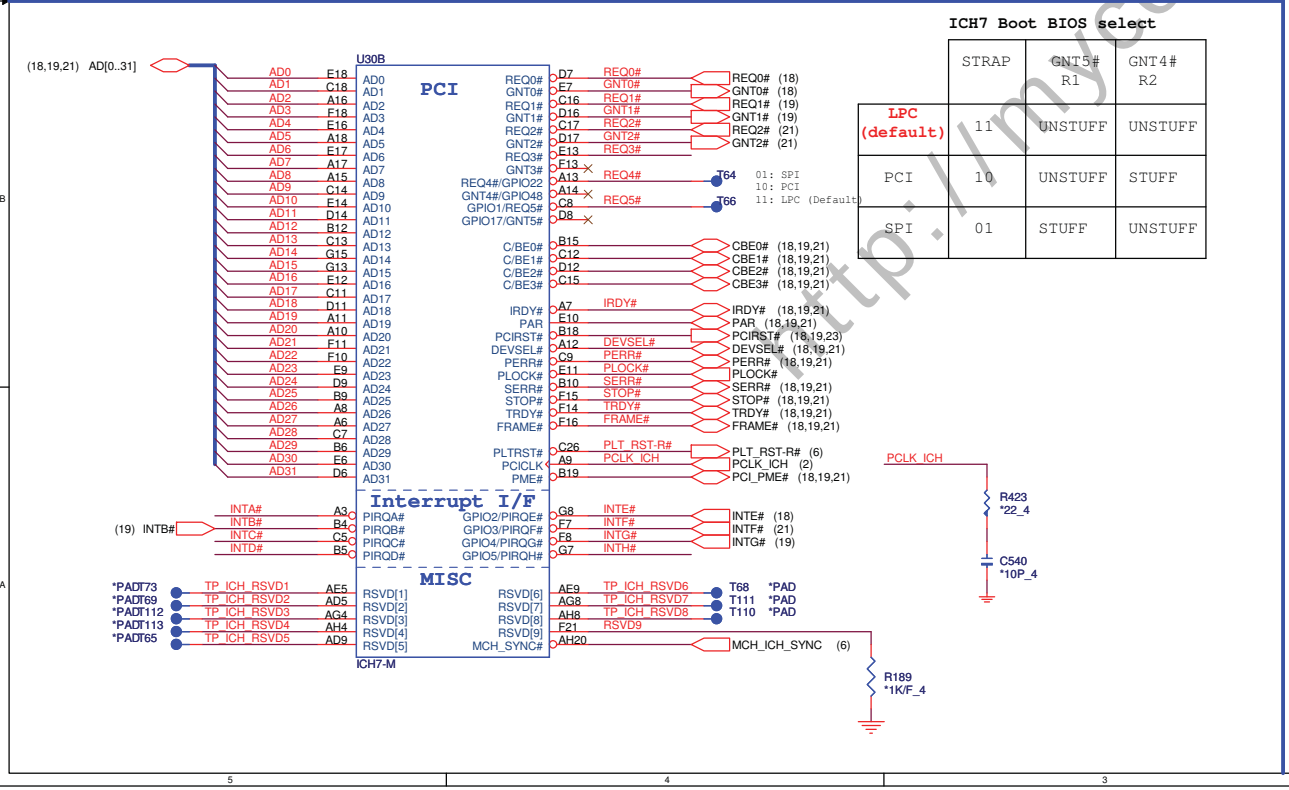
http://mycomp.su/x/

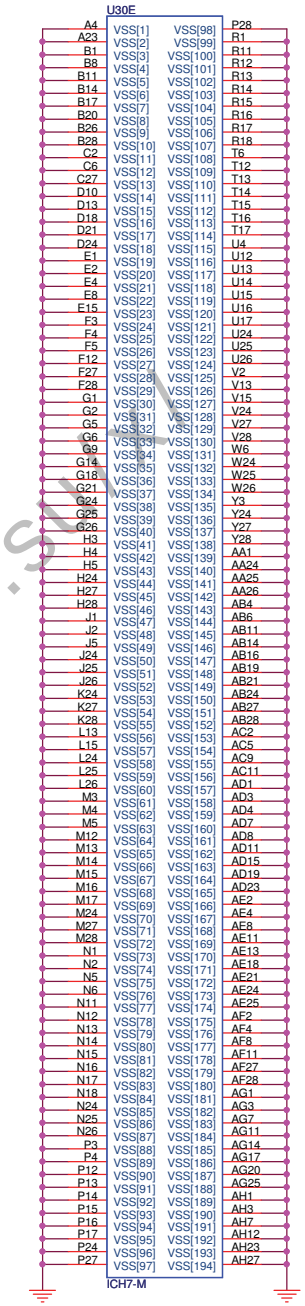




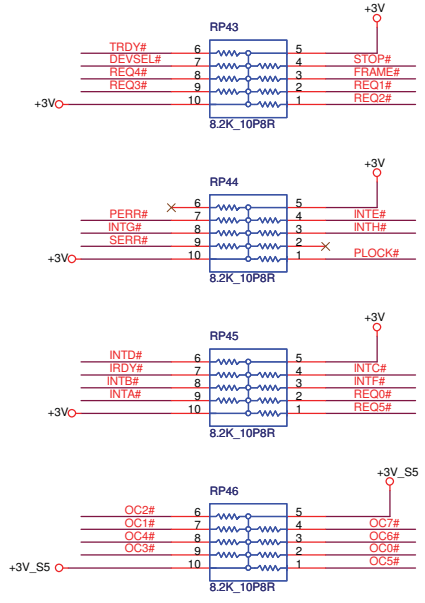
ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

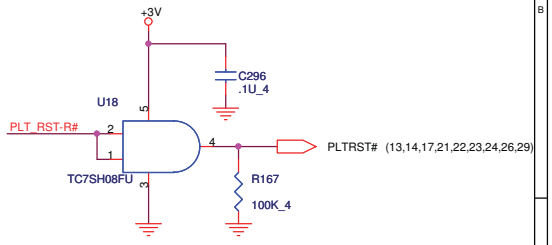
01: SPI
10: PCI
11: LPC (Default)



Pull-UP resistor



Platform Reset



PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	ICH6-M (USB & DMI & PCIE & PCI)	1A

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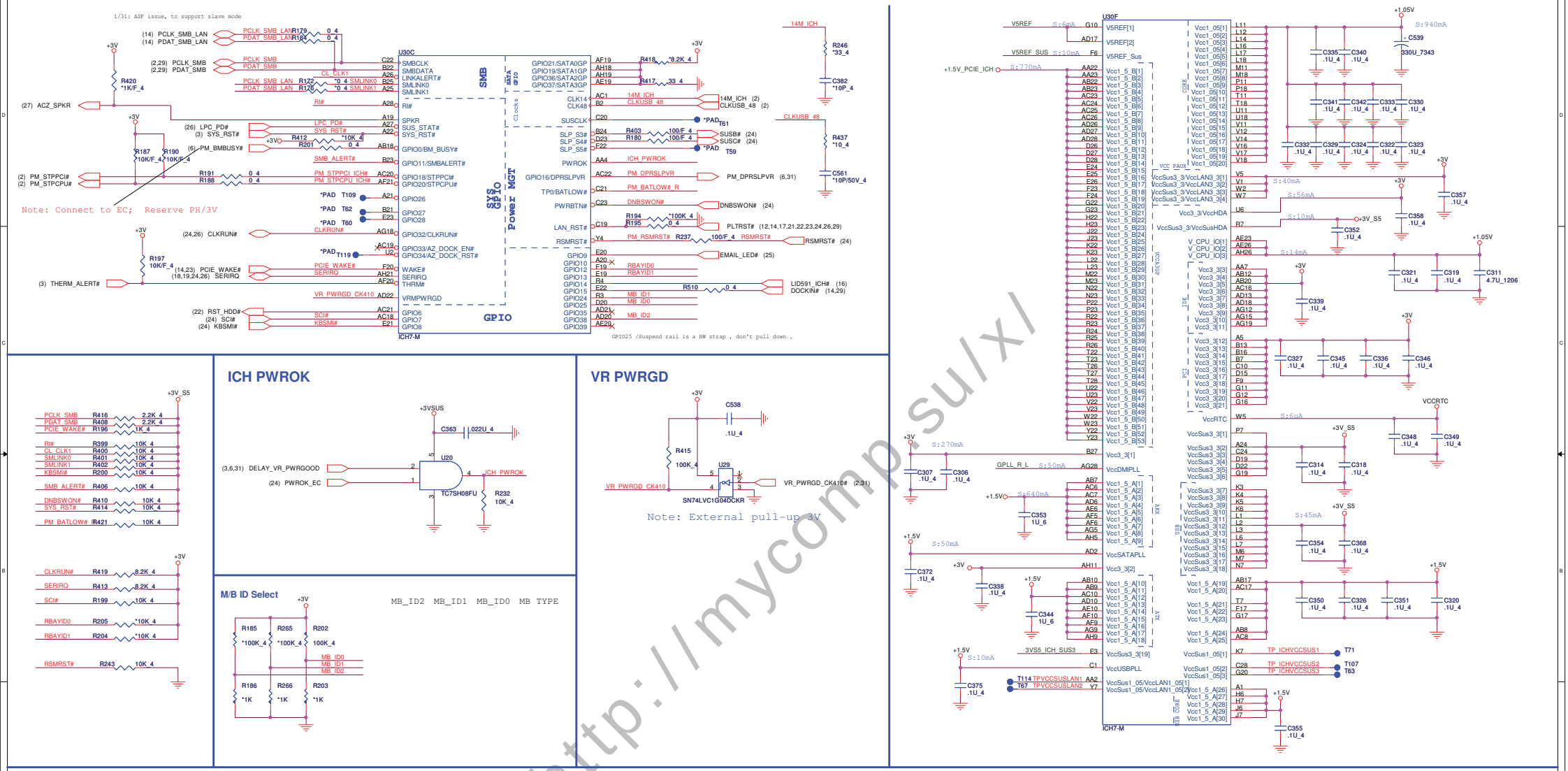
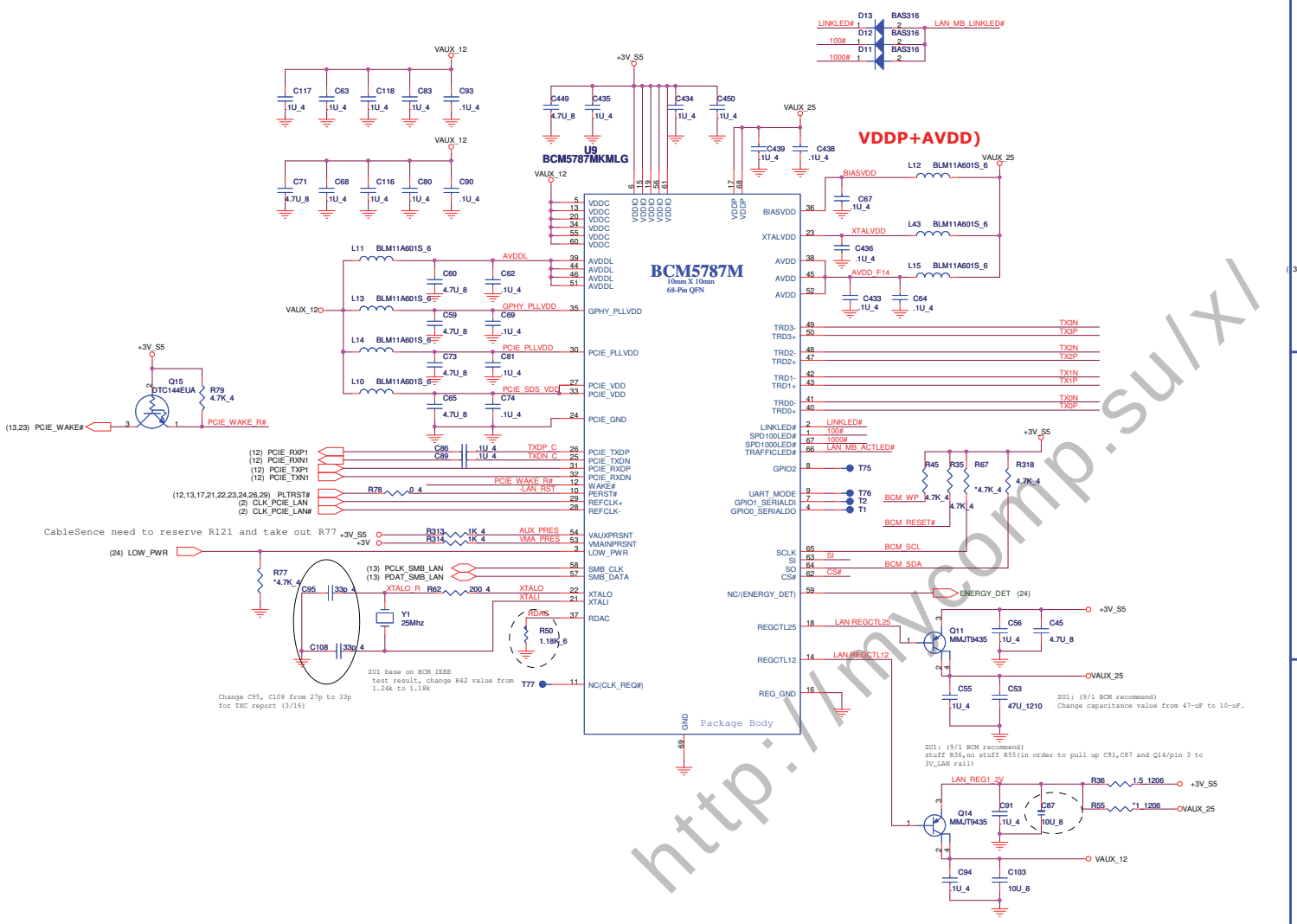
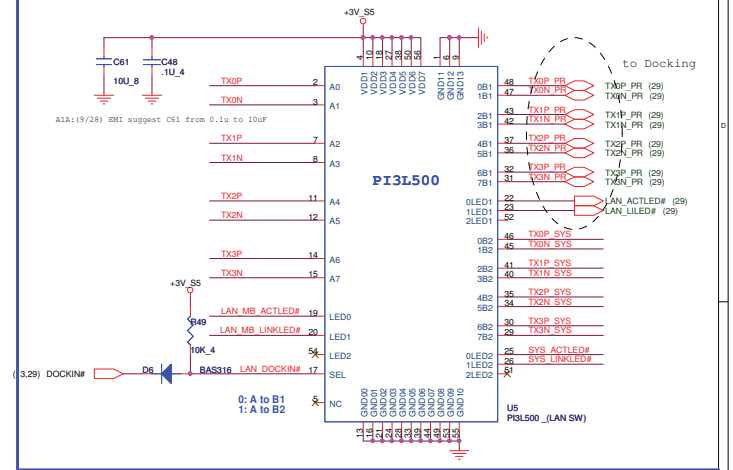


http://mycomp.su/xl

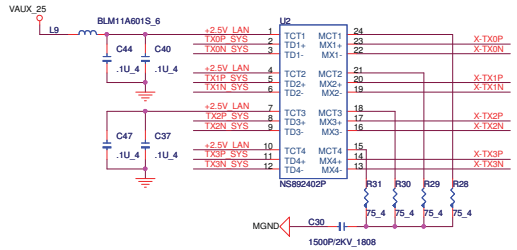
Giga LAN BCN5787M



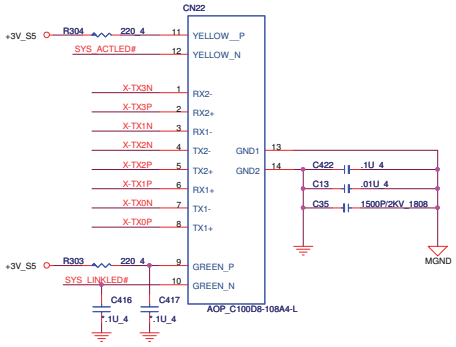
LAN Switch



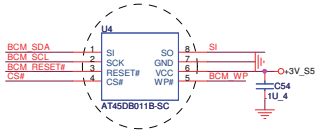
LAN Transformer



RJ45

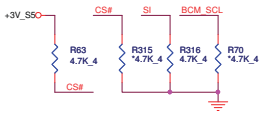


Flash ROM/EEPROM



EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1



http://mycomp.su/xl

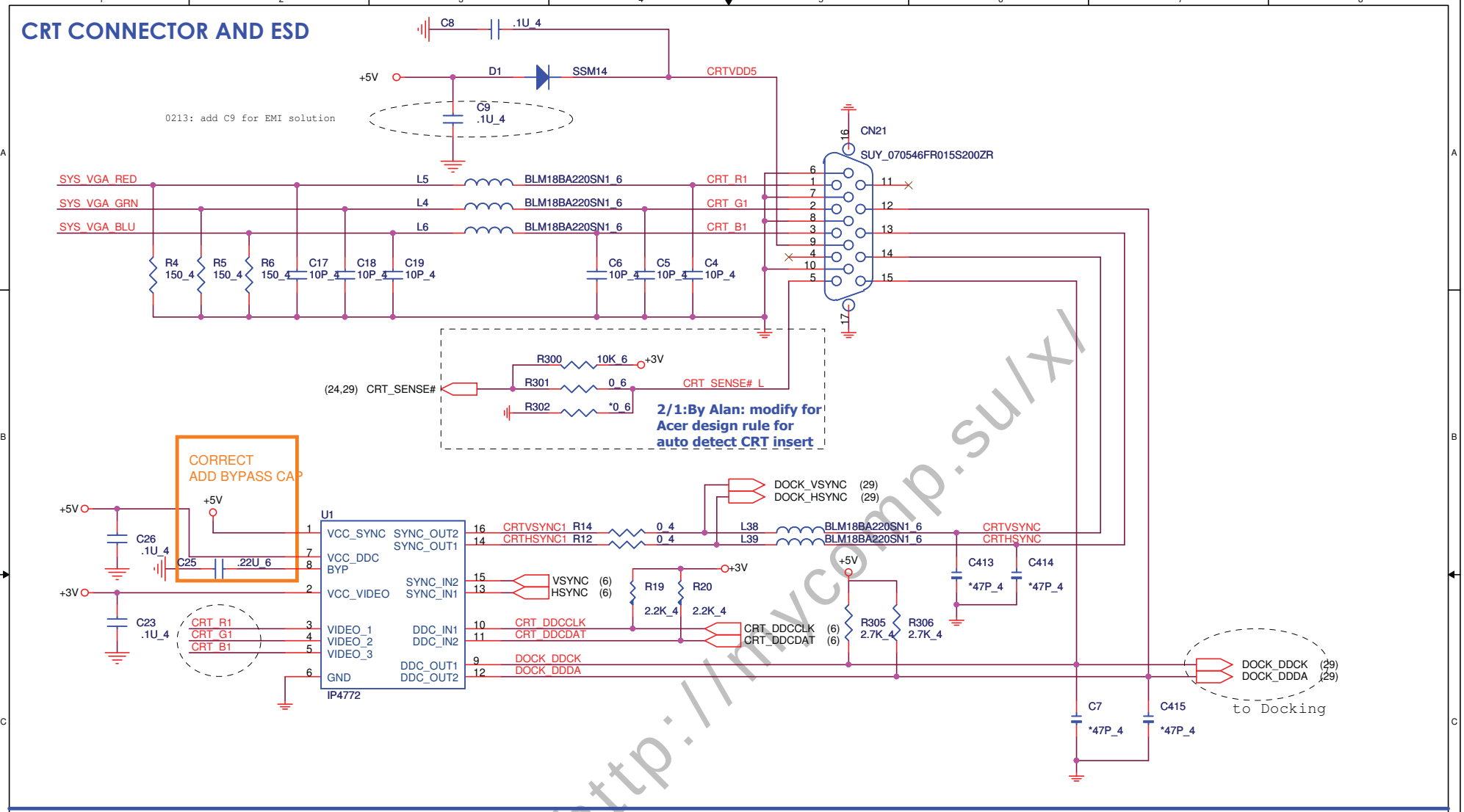
PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	GigaLAN (BCM5787M) / RJ45	1B

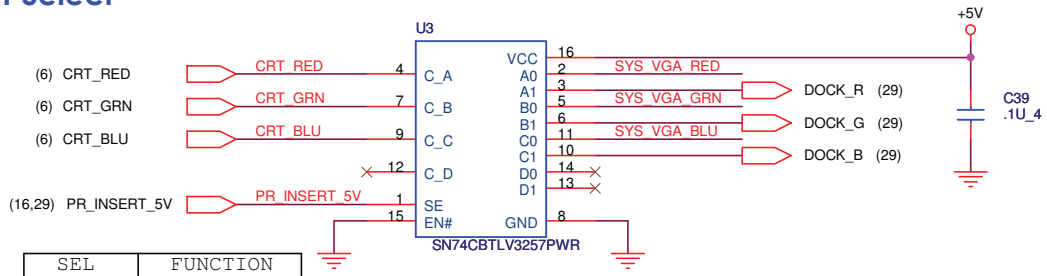
Date: Thursday, March 22, 2007 Sheet 14 of 39

CRT CONNECTOR AND ESD



http://mycomp.su/xl

CRT Select



SEL	FUNCTION
LOW	IN_0
HIGH	IN_1

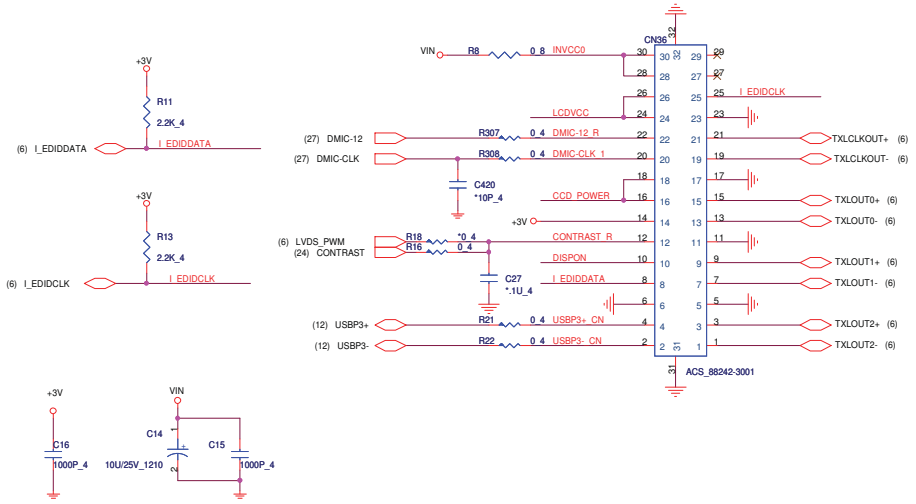
PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	CRT	1A

Date: Thursday, March 22, 2007 Sheet 15 of 39

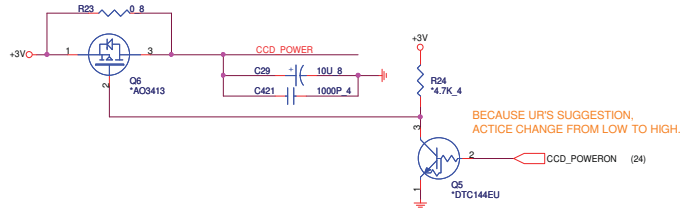
LVDS



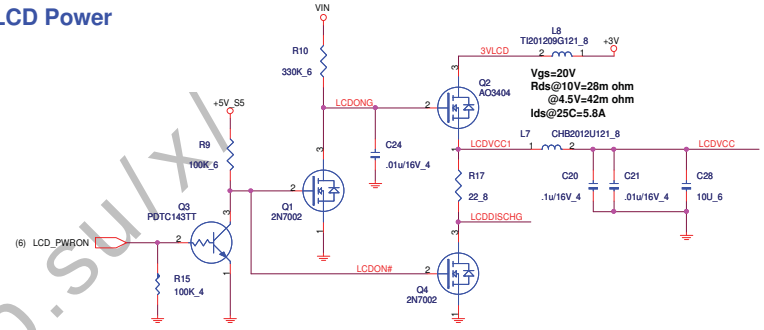
ZU1:(12/28) EMI request: reserve L-C footprint for debug use (R52,C650)

(3/19)Change MB LCD connector pin define(CN3) and LCD cable pin define to cover production line issue
(Inverter short with signal to burn system)->ZR1 issue
(1)pin 27,29->NC
(2)pin 8->INT_LVDS_EDIDDATA

CAMERA MODULE

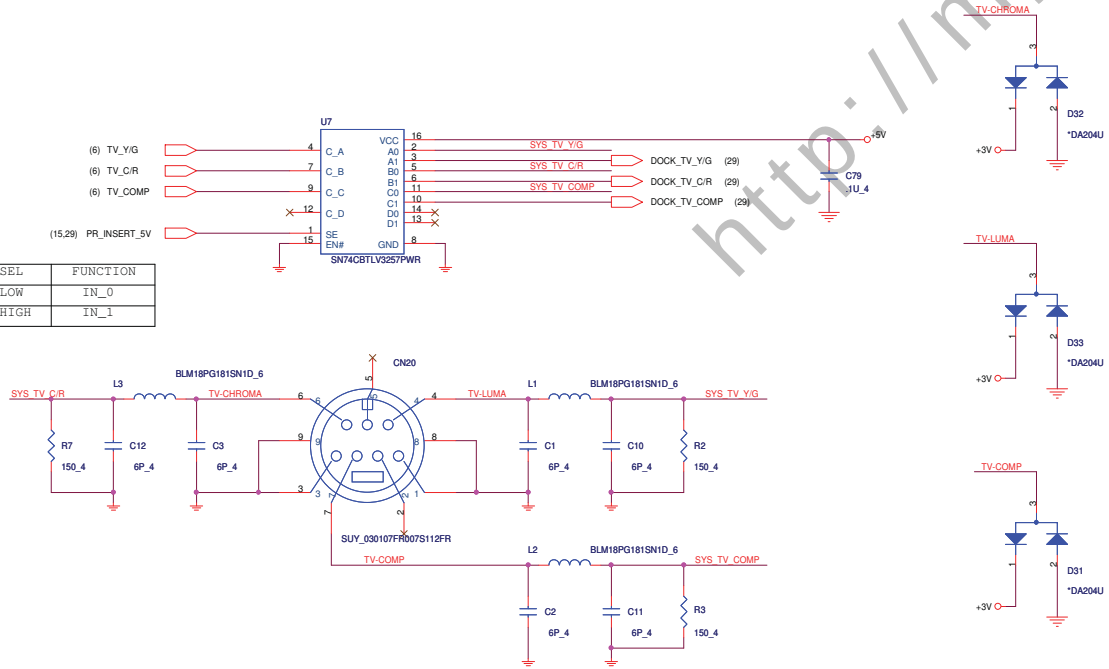


LCD Power



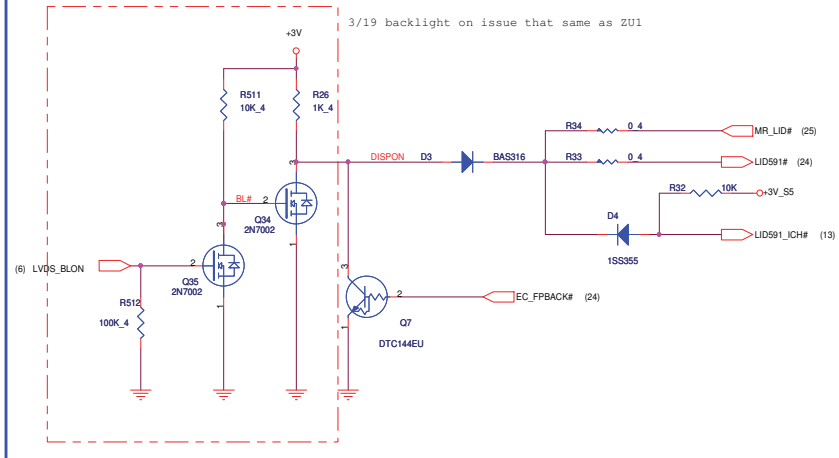
1/29:By Alan: AAT4280 fail on power ON rising time and falling time. EA.Additionally, some LCD panels will have garbage. follow ZR1 circuit.

TV Out (SVHS) MiniDIN 7-pin



SEL	FUNCTION
LOW	IN_0
HIGH	IN_1

MR Sensor



PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	LVDS/MR senseor/SVIDEO	1B

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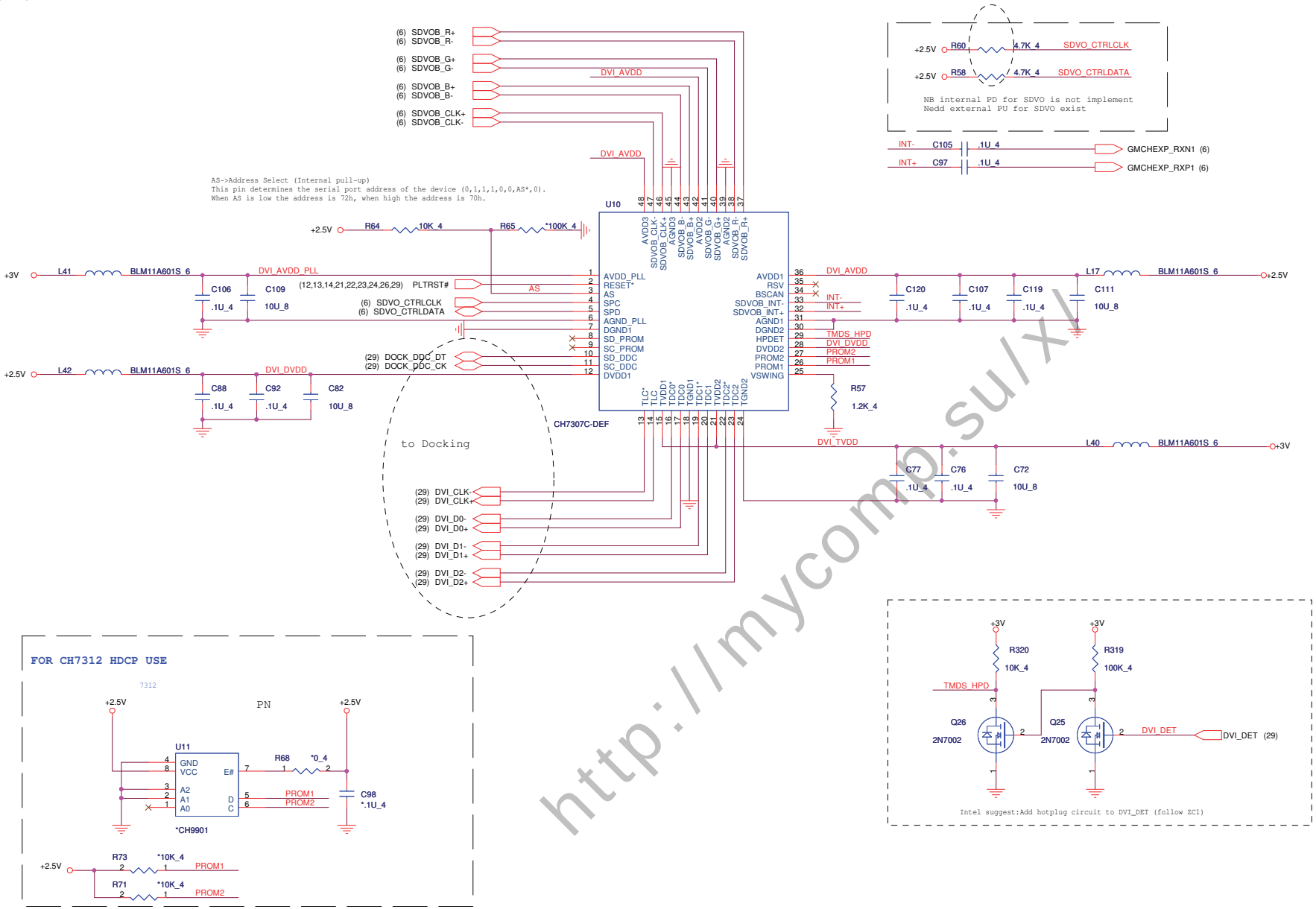
http://mycomp.su/xl

SDVO-DVI



http://mycomp.su/xl

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	DVI (CH7307)	1A

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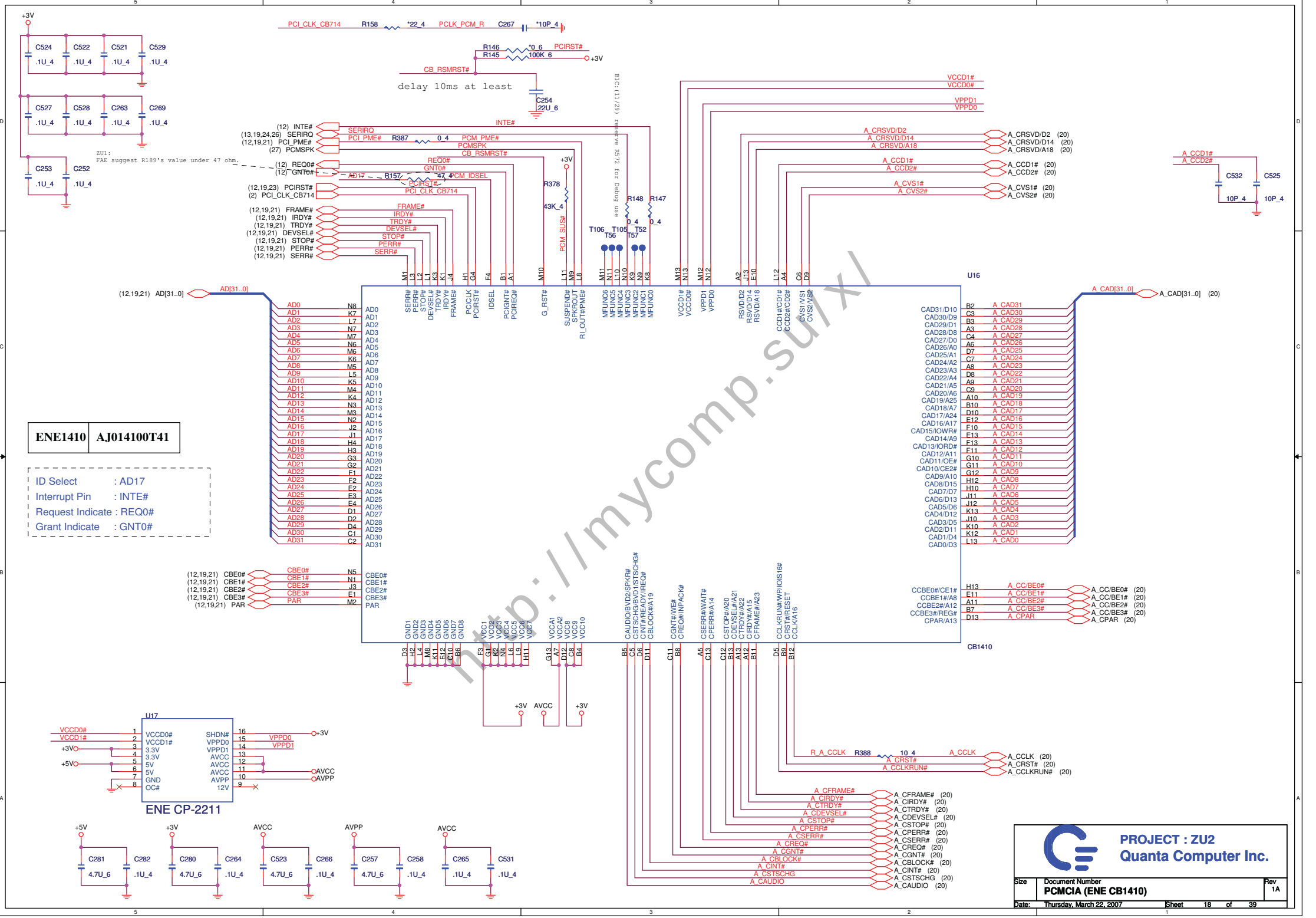
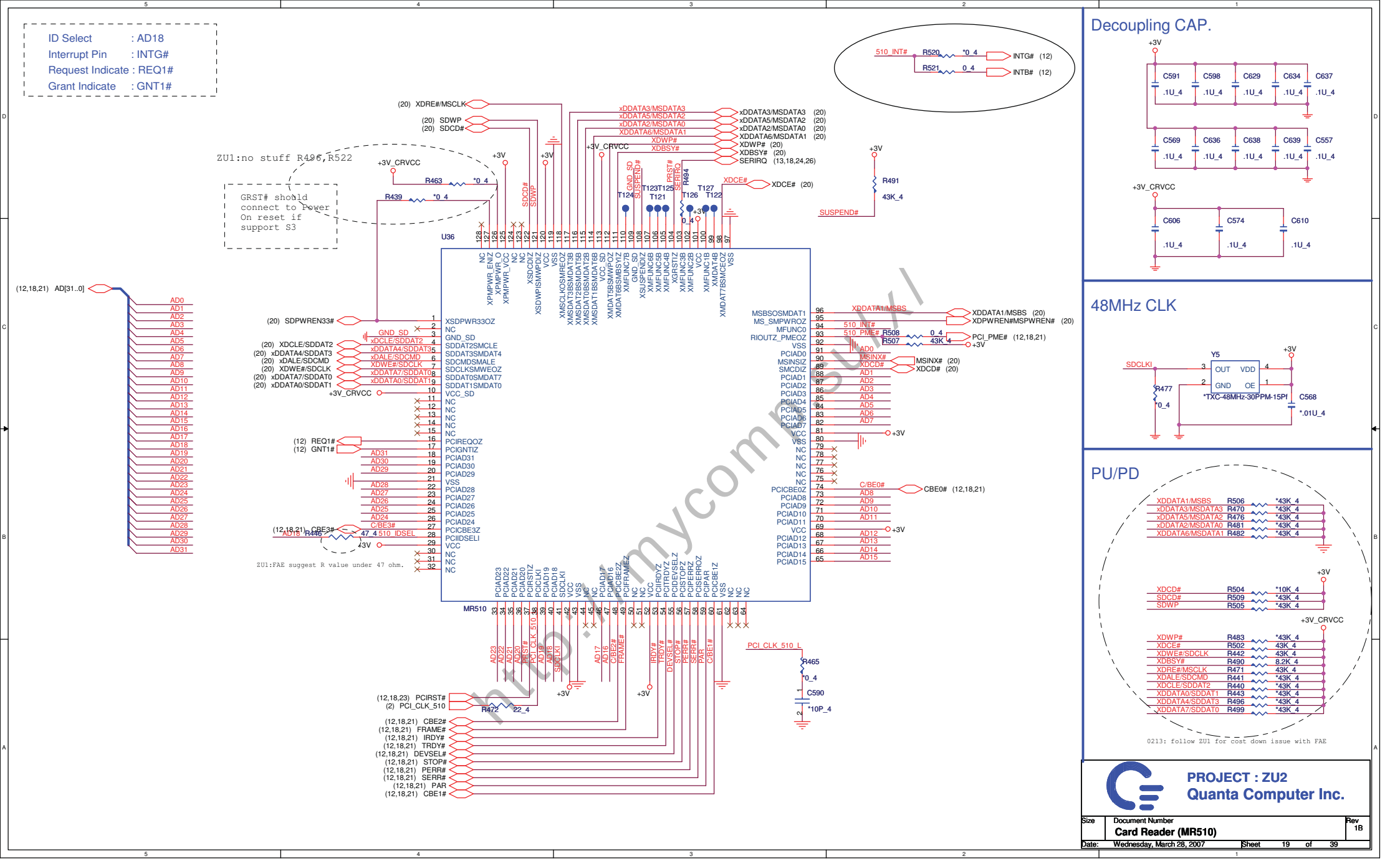
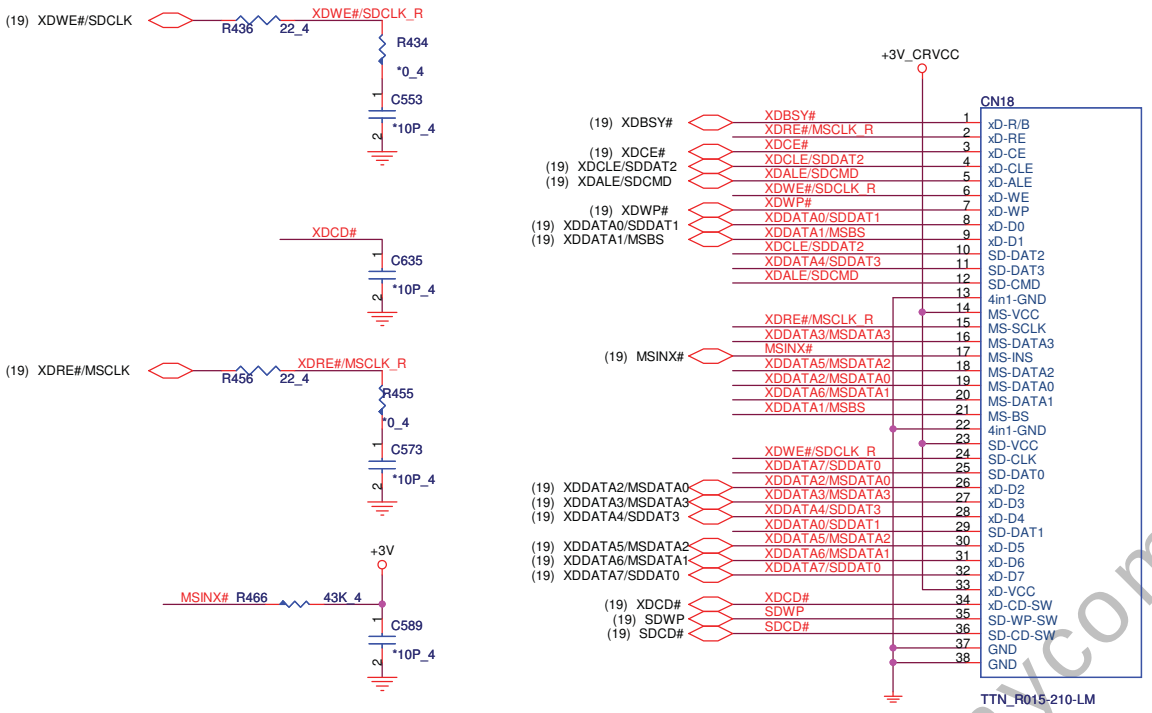


http://mycomp.su/x/

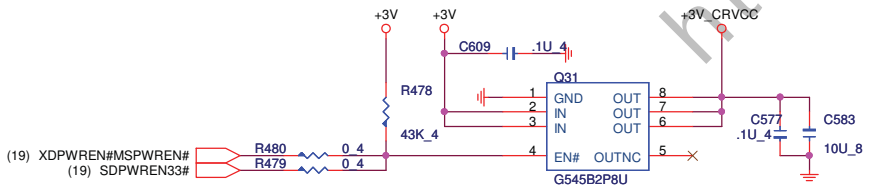


http://mycomsuk/

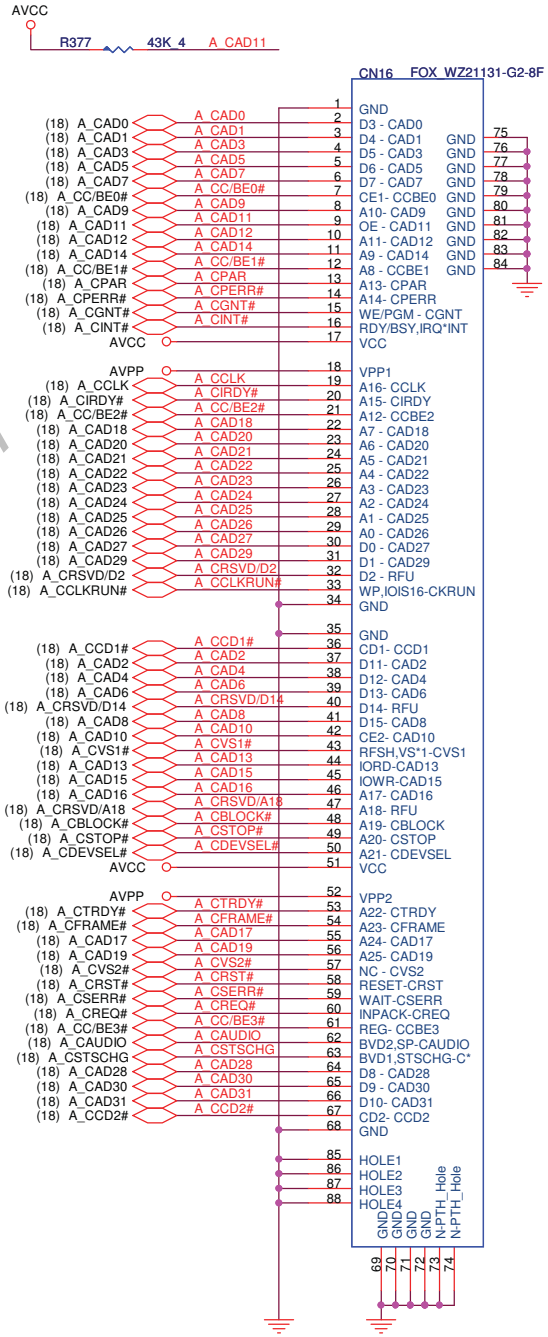
CardReader



CardReader Power switch



PCMCIA



http://mycomp.su/xl

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	CARD Reader & PCMCIA SLOT	1A

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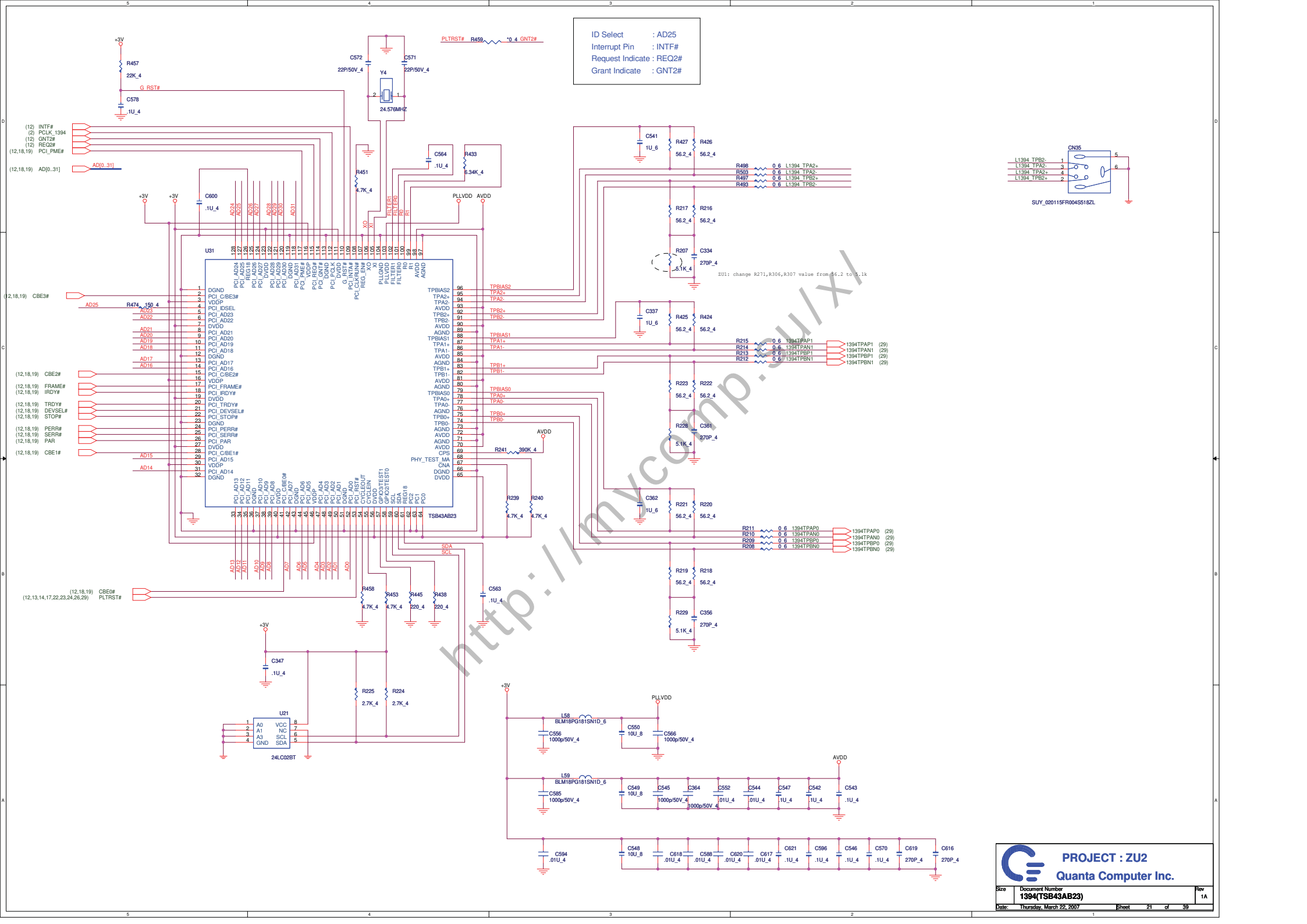
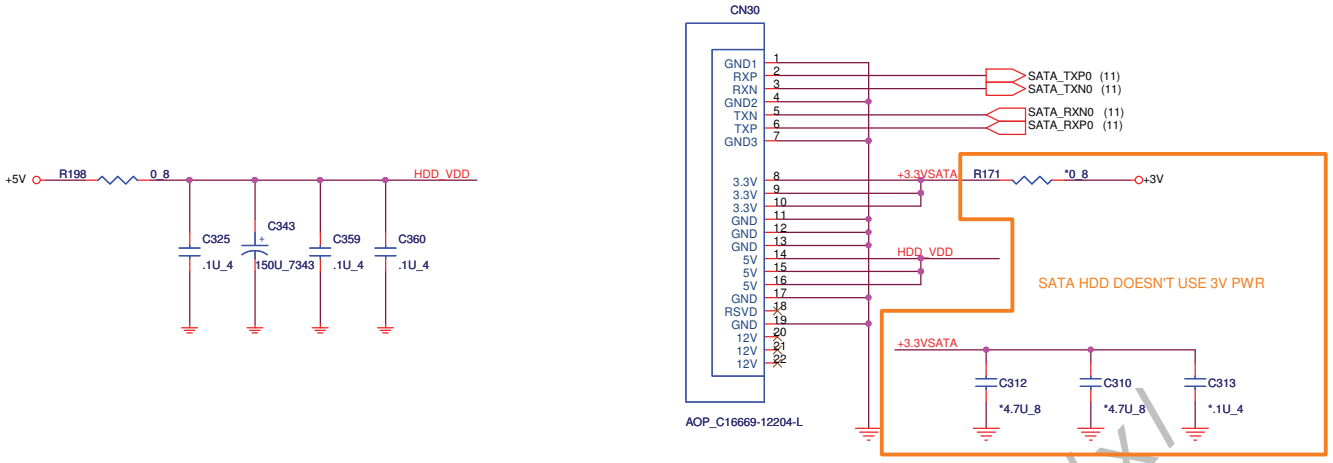
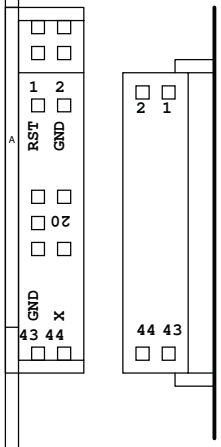


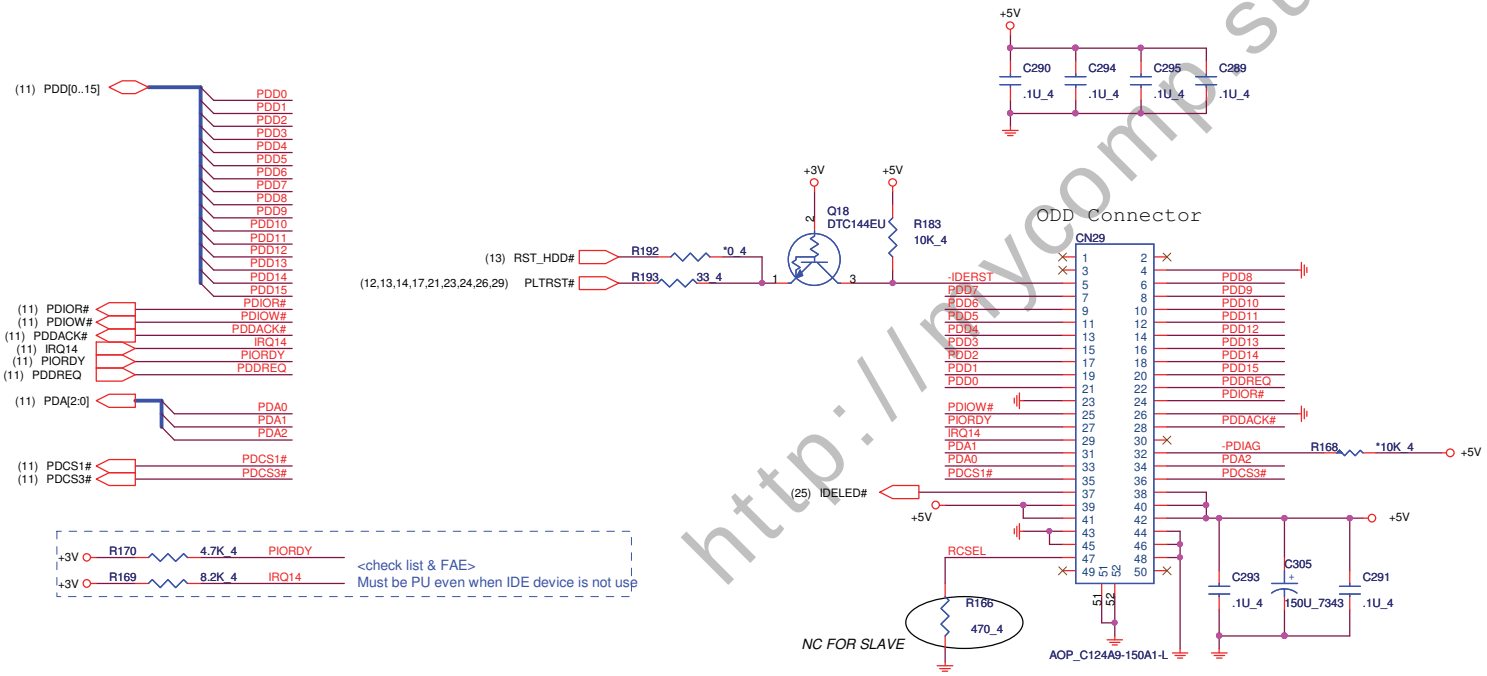
http://mycomp.su/xl

SATA HDD





PATA ODD



http://mycomp.su/xi

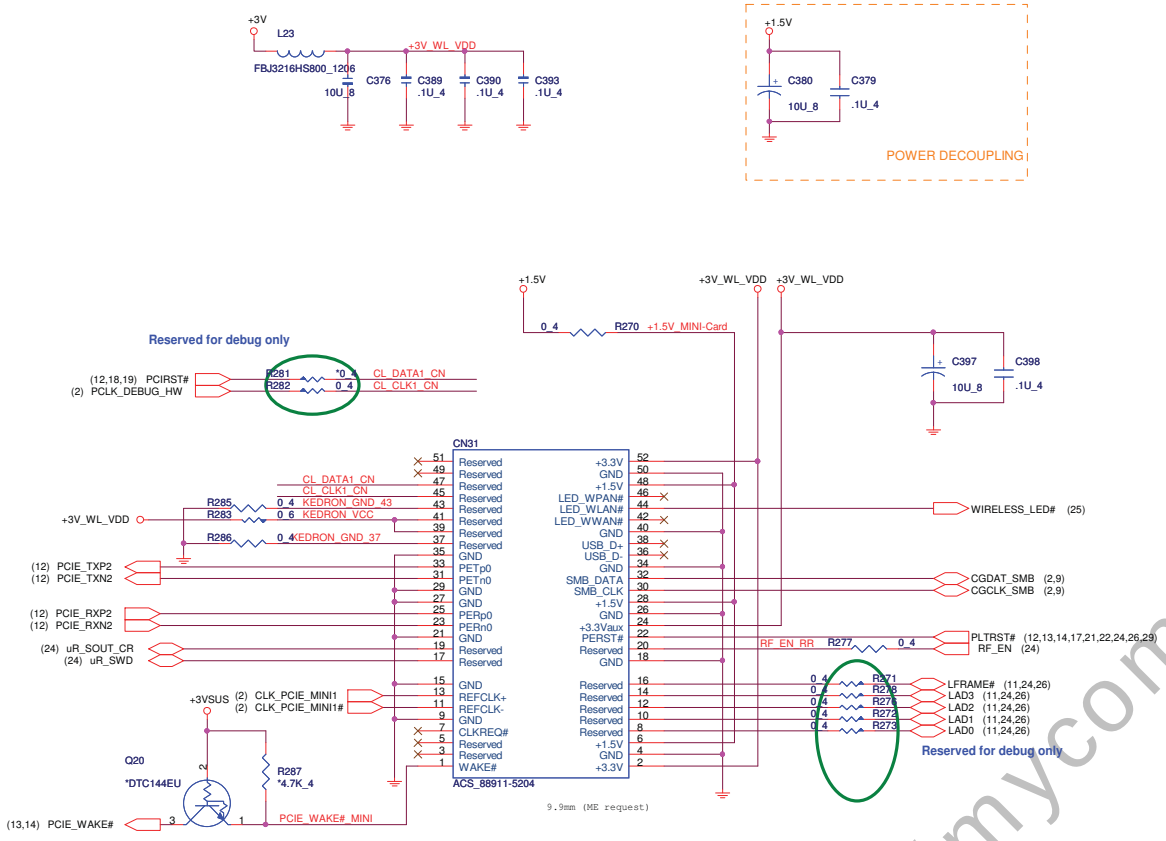
PROJECT : ZU2

Quanta Computer Inc.

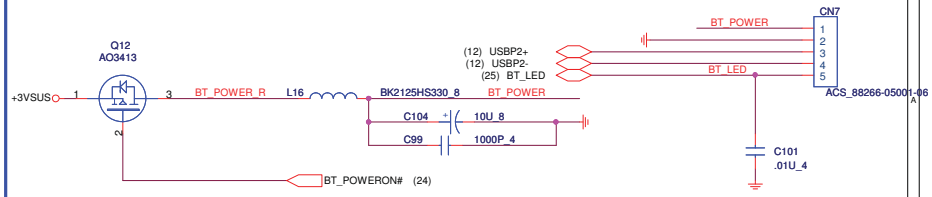
Size	Document Number	Rev
	SATA-HDD & PATA-ODD	1A

Date: Thursday, March 22, 2007 Sheet 22 of 39

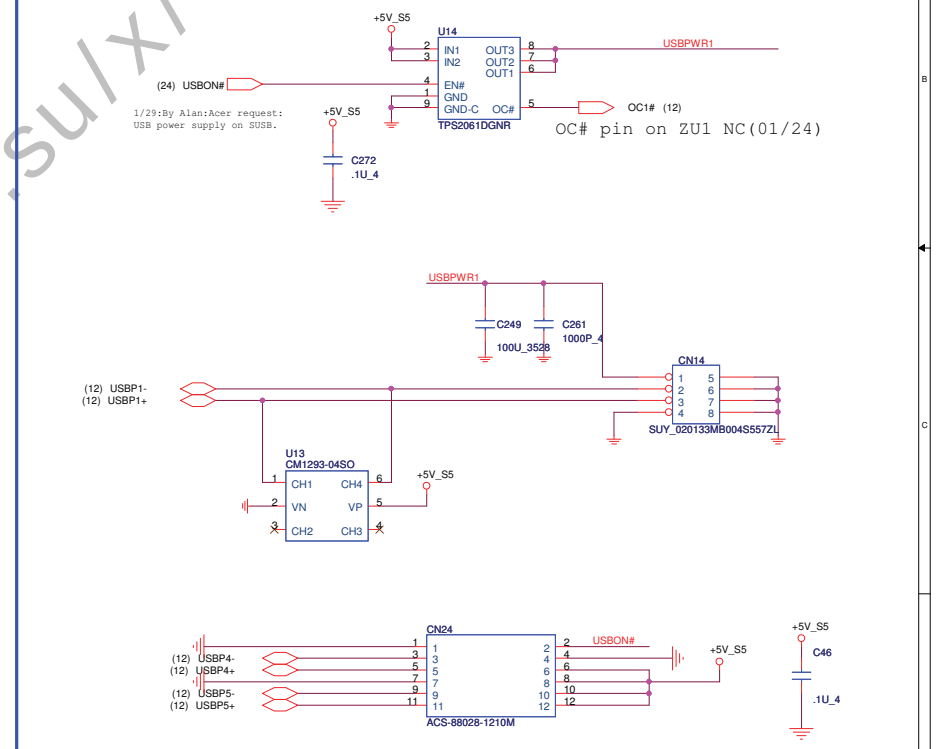
MINI-Card



BLUETOOTH MODULE CONNECTOR



System USB



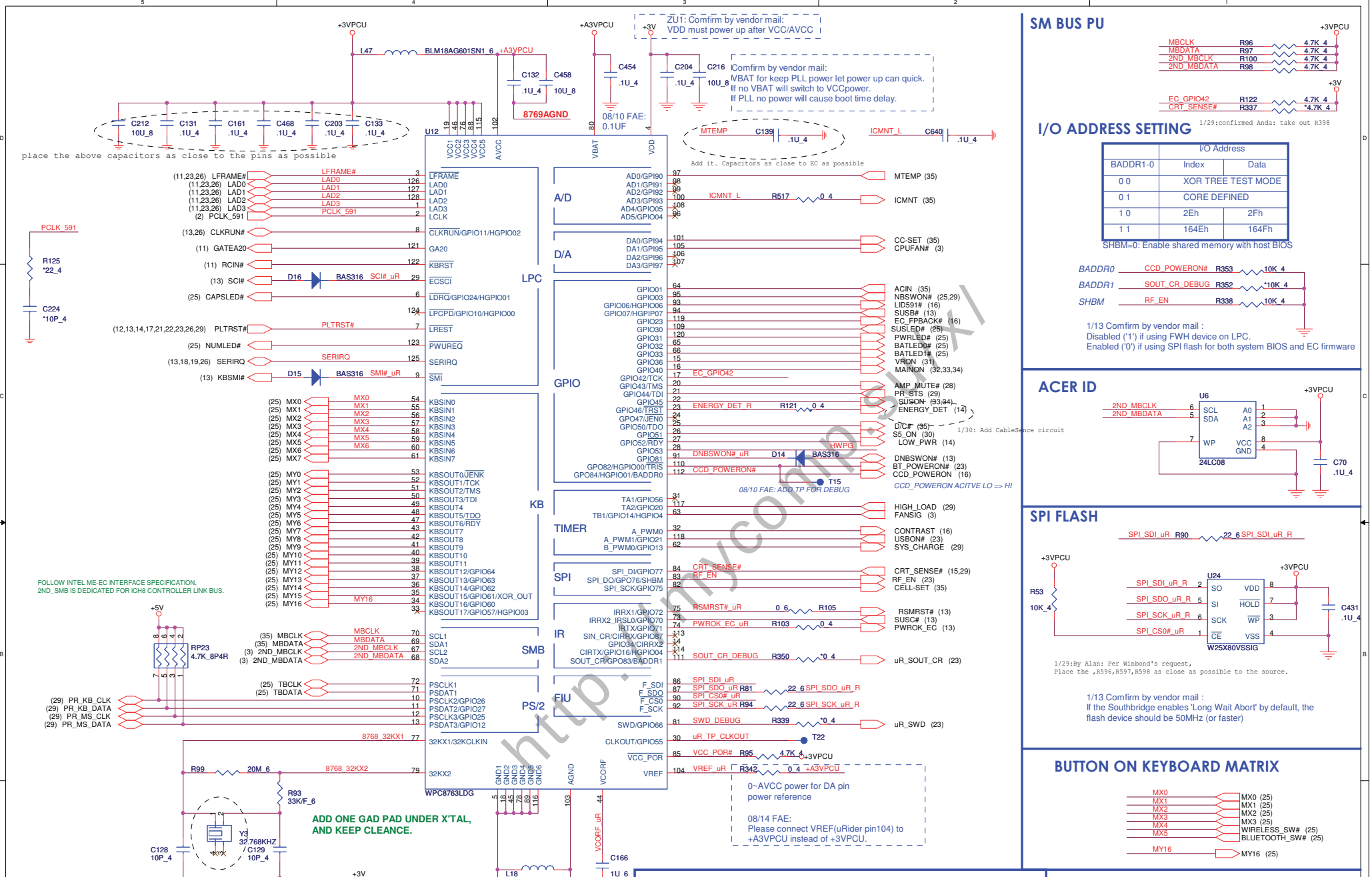
http://mycomp.su/xl

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	Mini card/USB/Bluetooth	1B

Date: Wednesday, March 28, 2007 Sheet 23 of 39



SM BUS PU

MBCLK	R96	4.7K_4	+3VPCU
MBDATA	R97	4.7K_4	+3VPCU
2ND_MBCLK	R100	4.7K_4	+3VPCU
2ND_MBDATA	R98	4.7K_4	+3VPCU
EC_GPIO42	R122	4.7K_4	+3V
CRT_SENSE#	R337	*4.7K_4	+3V

1/29:confirmed Anda: take out R398

I/O ADDRESS SETTING

BADDR1-0	I/O Address Index	I/O Address Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0	CCD_POWERON#	R353	10K_4
BADDR1	SOUT_CR_DEBUG	R352	*10K_4
SHBM	RF_EN	R338	10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ACER ID

U6 24LC08: SCL, SDA, WP, A0, A1, A2, VCC, GND
2ND_MBCLK, 2ND_MBDATA, +3VPCU, C70 .1U_4

SPI FLASH

SPI_SDI_uR R90 22_6 SPI_SDI_uR_R
R53 10K_4, +3VPCU
U24 W25X80VSSIG: SO, SI, SCK, CE, VDD, HOLD, WP, VSS
SPI_SDI_uR_R, SPI_SDO_uR_R, SPI_SCK_uR_R, SPI_CS0#_uR
C431 .1U_4

1/29:By Alan: Per Winbond's request,
Place the ,R596,R597,R598 as close as possible to the source.

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

BUTTON ON KEYBOARD MATRIX

MX0 (25), MX1 (25), MX2 (25), MX3 (25), MX4 (25) WIRELESS_SW# (25), MX5 BLUETOOTH_SW# (25), MY16 (25)

DEBUG PORTS

EC Debug Port

+3VPCU; SOUT_CR_DEBUG, SWD_DEBUG; (2) PCLK_DEBUG_SW; CN9 *ACS_88231-04001

Reserved for LPC debug card

+3V; CN8; LAD0, LAD1, LAD2, LAD3, LFRAME#, PLTRST#, SERIRQ; BOT CONTACT; *ACS_88502-1001

INTERNAL KEYBOARD STRIP SET

+3VPCU; MY0 R110 10K_4

PROJECT : ZU2

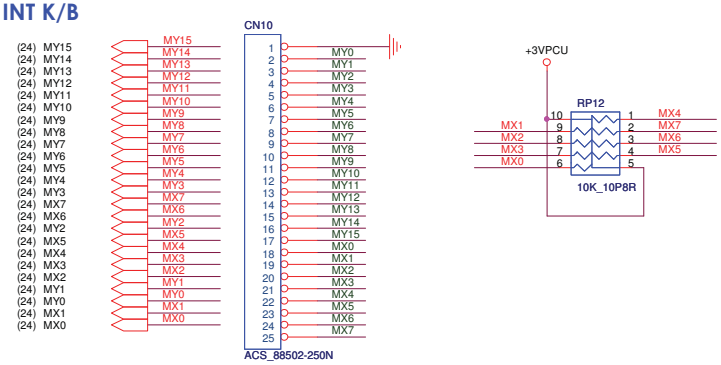
Quanta Computer Inc.

Size	Document Number	Rev
	EC (PC8763LDG)/ FLASH	1B

Date: Thursday, March 22, 2007 Sheet 24 of 39

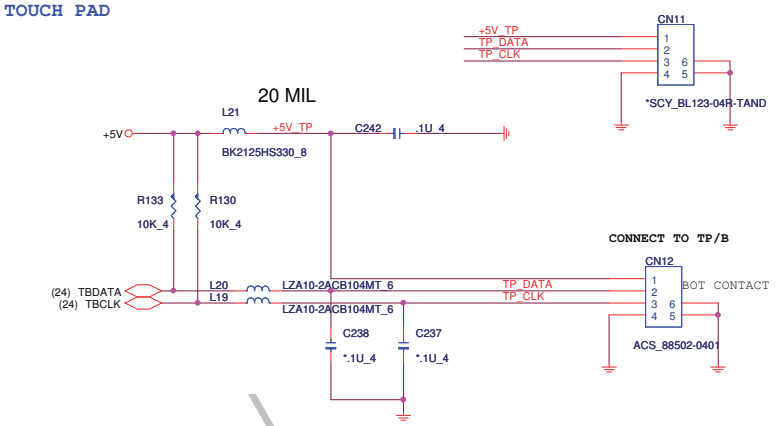
http://mycomp.su/

INT K/B

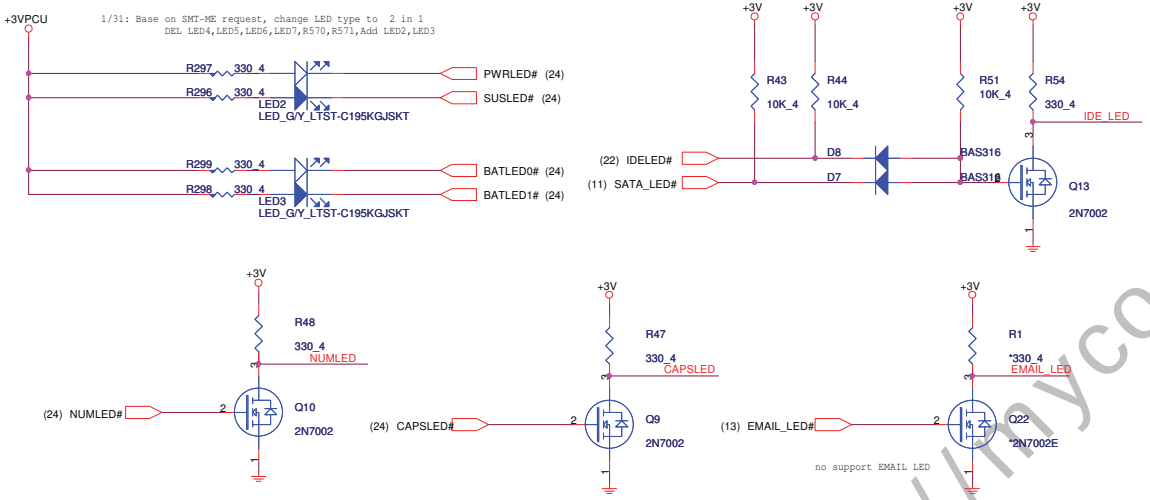


uR REQUEST
MY DOES NOT NEED PU.
MY CAN NOT USE EMI BYPASS CAP, DUE TO FLASH.

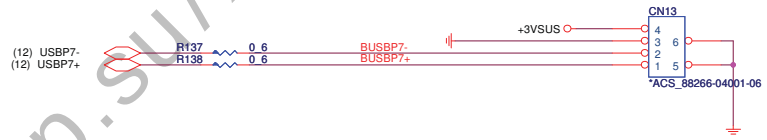
TOUCH PAD



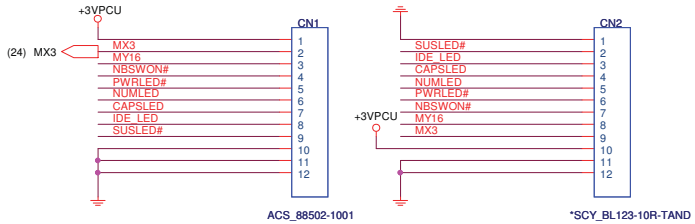
LED

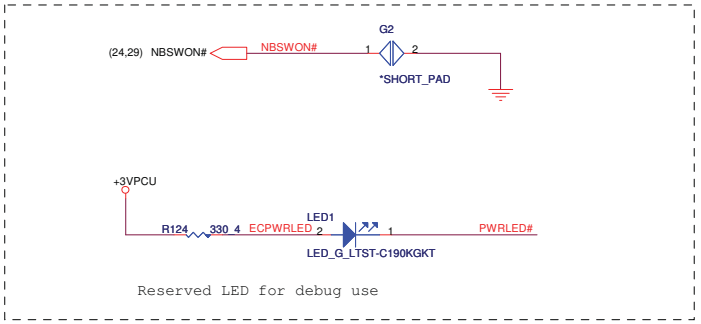


Finger Printer

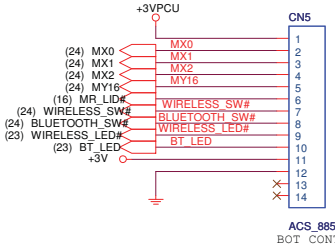


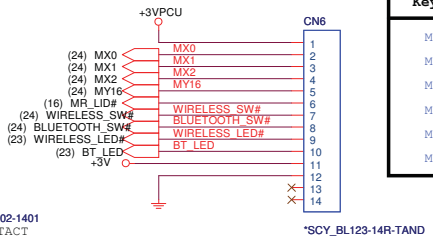
LED Board





Function Board





Keyboard Matrix	Button
MX0/MY16	acer EAP Buttton
MX1/MY16	acer EMAIL Buttton
MX2/MY16	acer WWW Buttton
MX3/MY16	acer EPM Buttton
MX4/MY16	WIRELESS Button
MX5/MY16	BLUETOOTH Button

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PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	SWITCH,LED,KB,Finger,TP	1B

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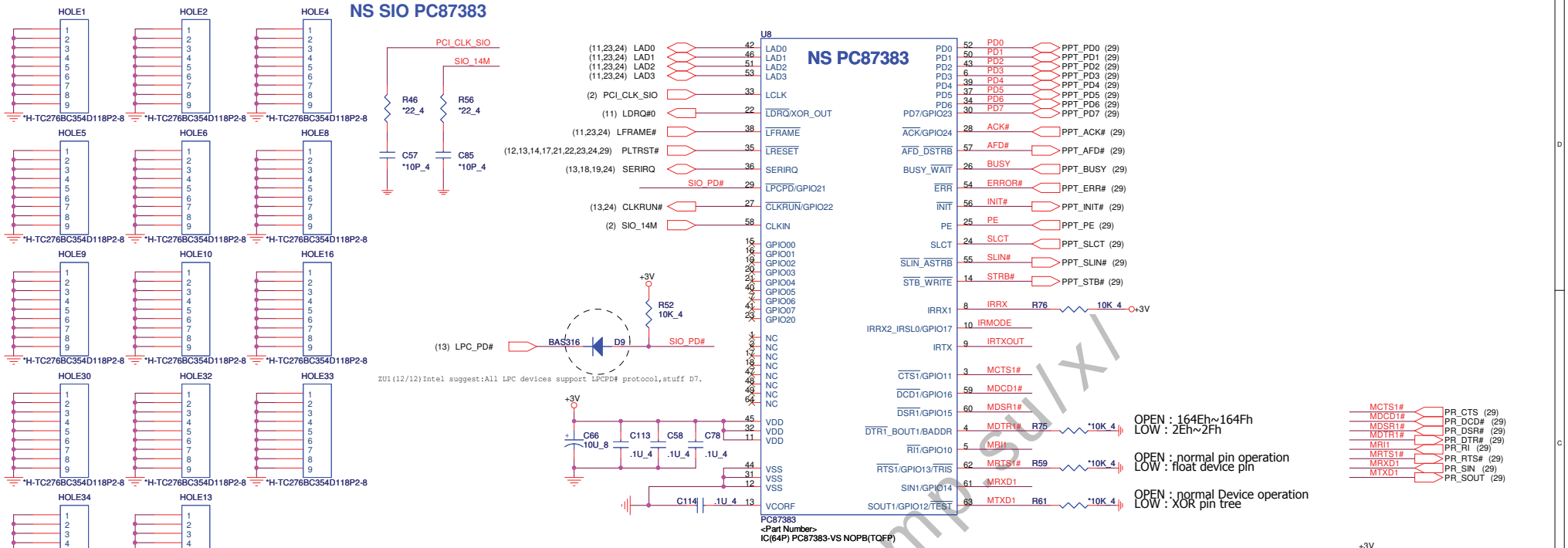
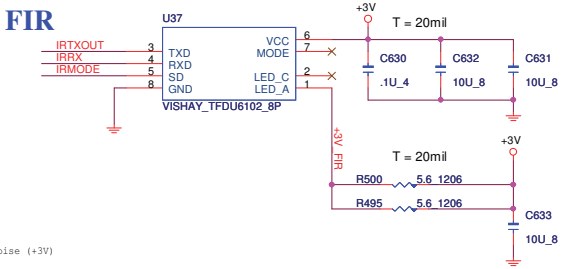
NS SIO PC87383

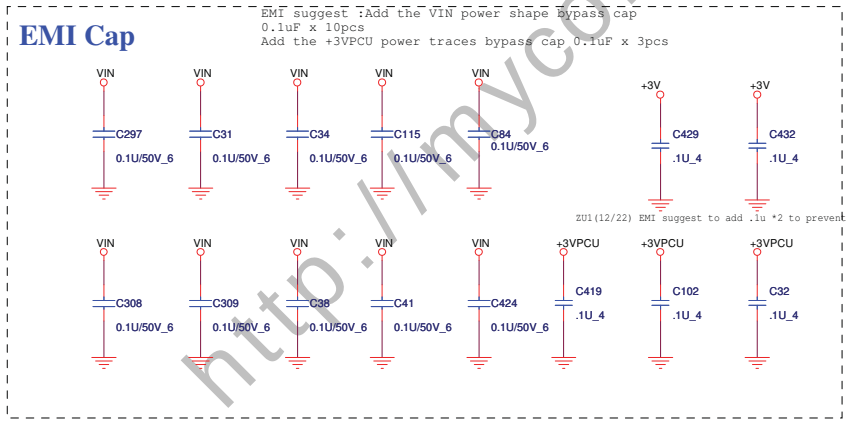


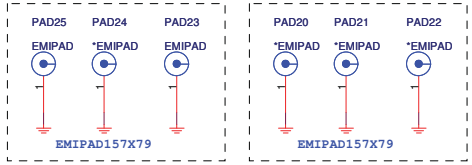
FIR



EMI Cap

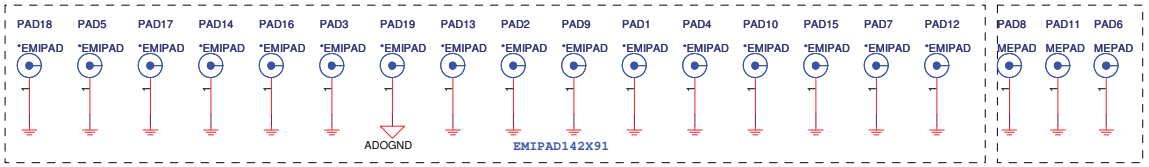
EMI suggest :Add the VIN power shape bypass cap
0.1uF x 10pcs
Add the +3VPCU power traces bypass cap 0.1uF x 3pcs





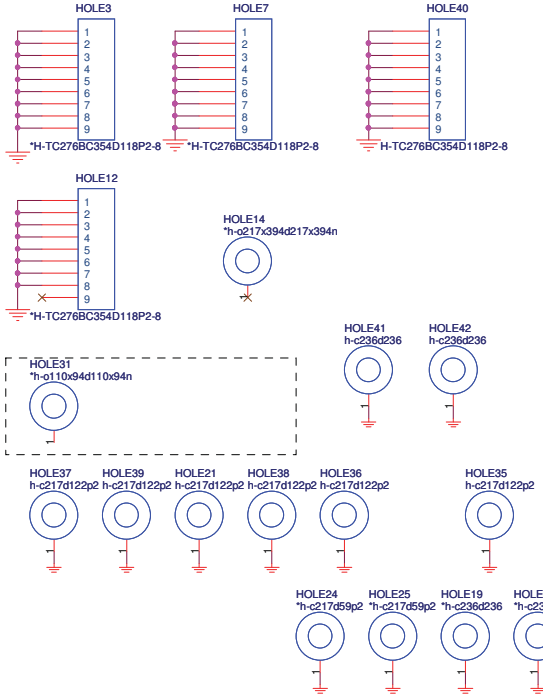
C2A:(12/22) EMI suggest add three clip to contact with CPU cooler's fins (PAD23,24,25)

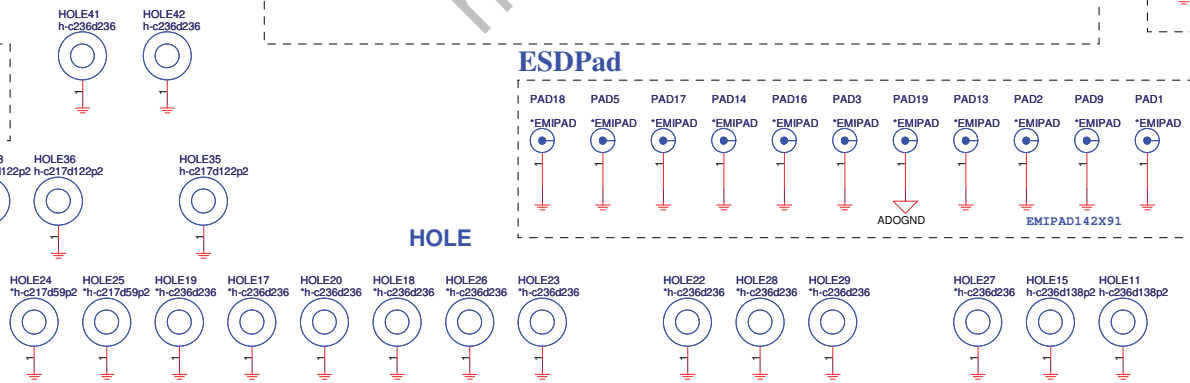
ESDPad



C2A:(12/22) Add theree PAD per ME request (fix wire)

HOLE





http://mycomp.su/x/

PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	SUPER-IO/FIR/HOLE	1A

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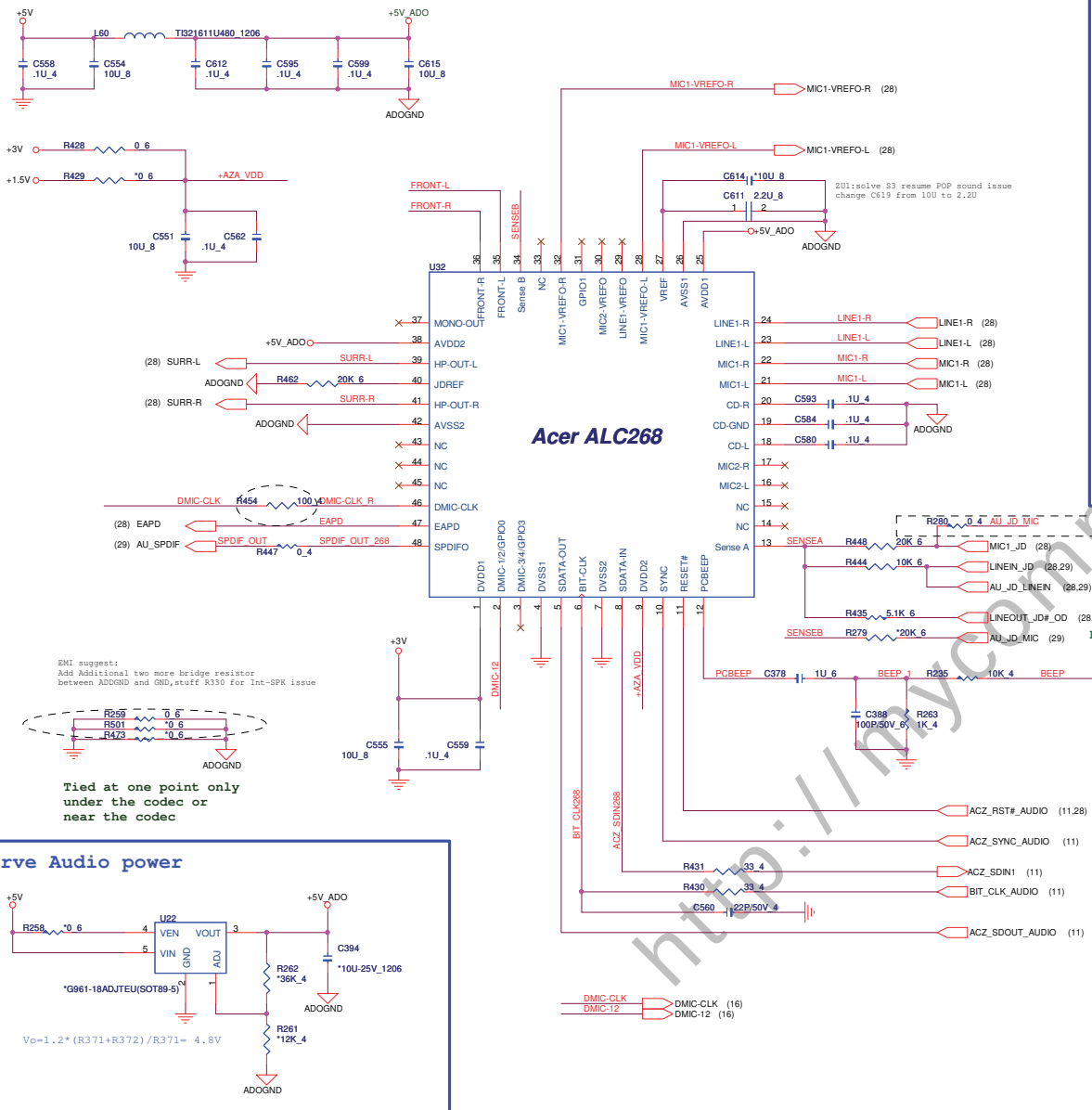
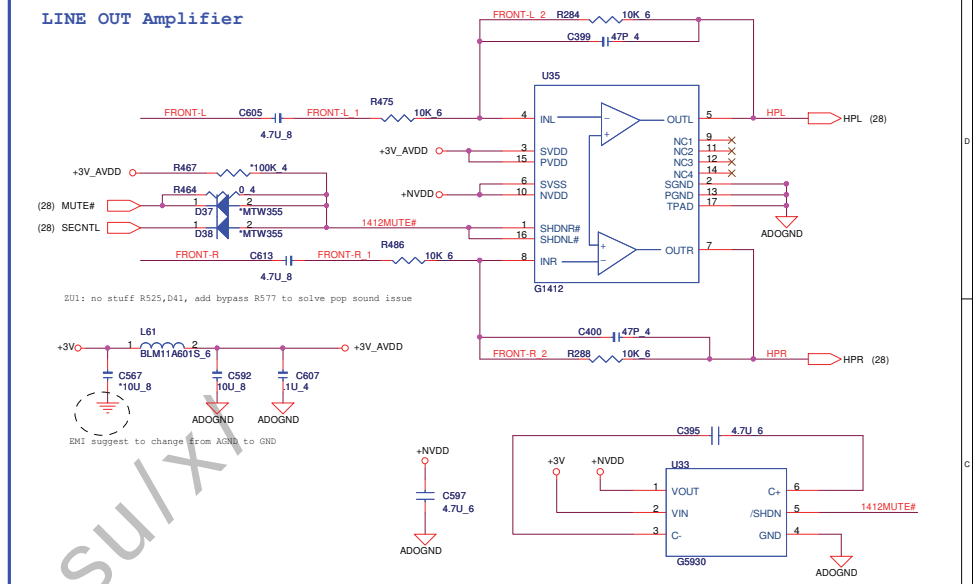
CODEC (ALC268)

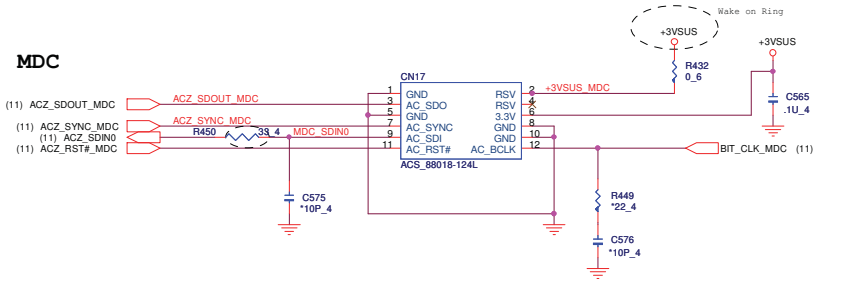


LINE OUT Amplifier



Reserve Audio power

MDC



PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO(ALC268)/AMP/MDC	1A

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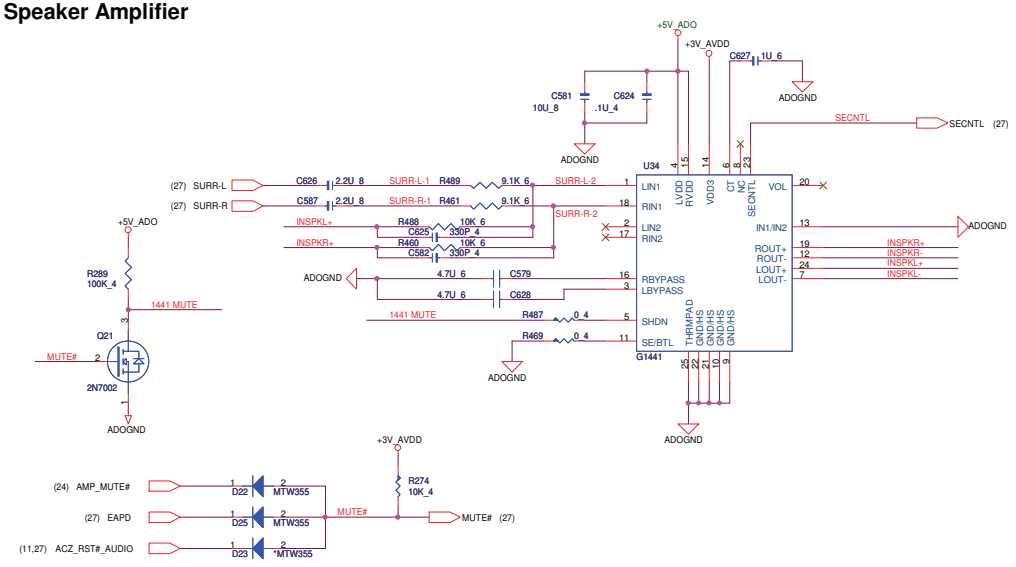
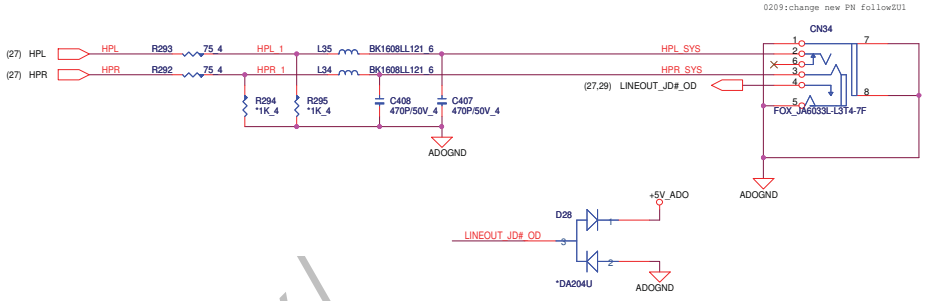
http://mycomp.su/xp

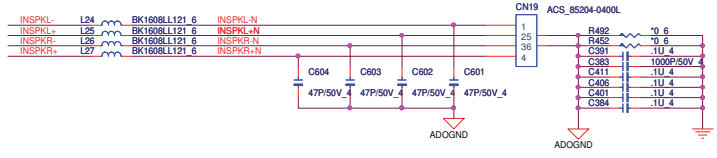
Speaker Amplifier



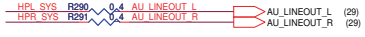
SYSTEM LINE OUT



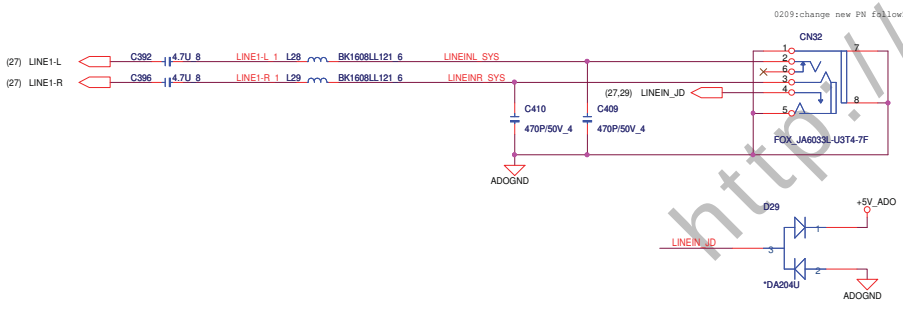
SPEAKER



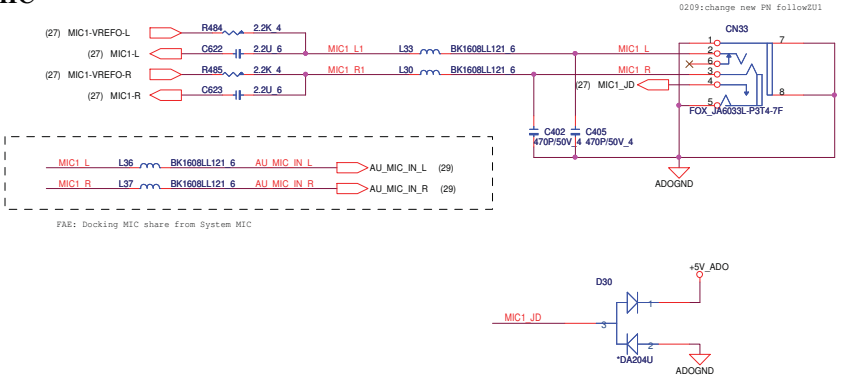
Docking LINE OUT/SPDIF



SYSTEM LINE IN



SYSTEM MIC



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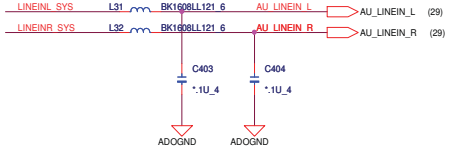

http://mycomp.su/xl

Size	Document Number		Rev
	Speaker AMP / Audio JACK		1A
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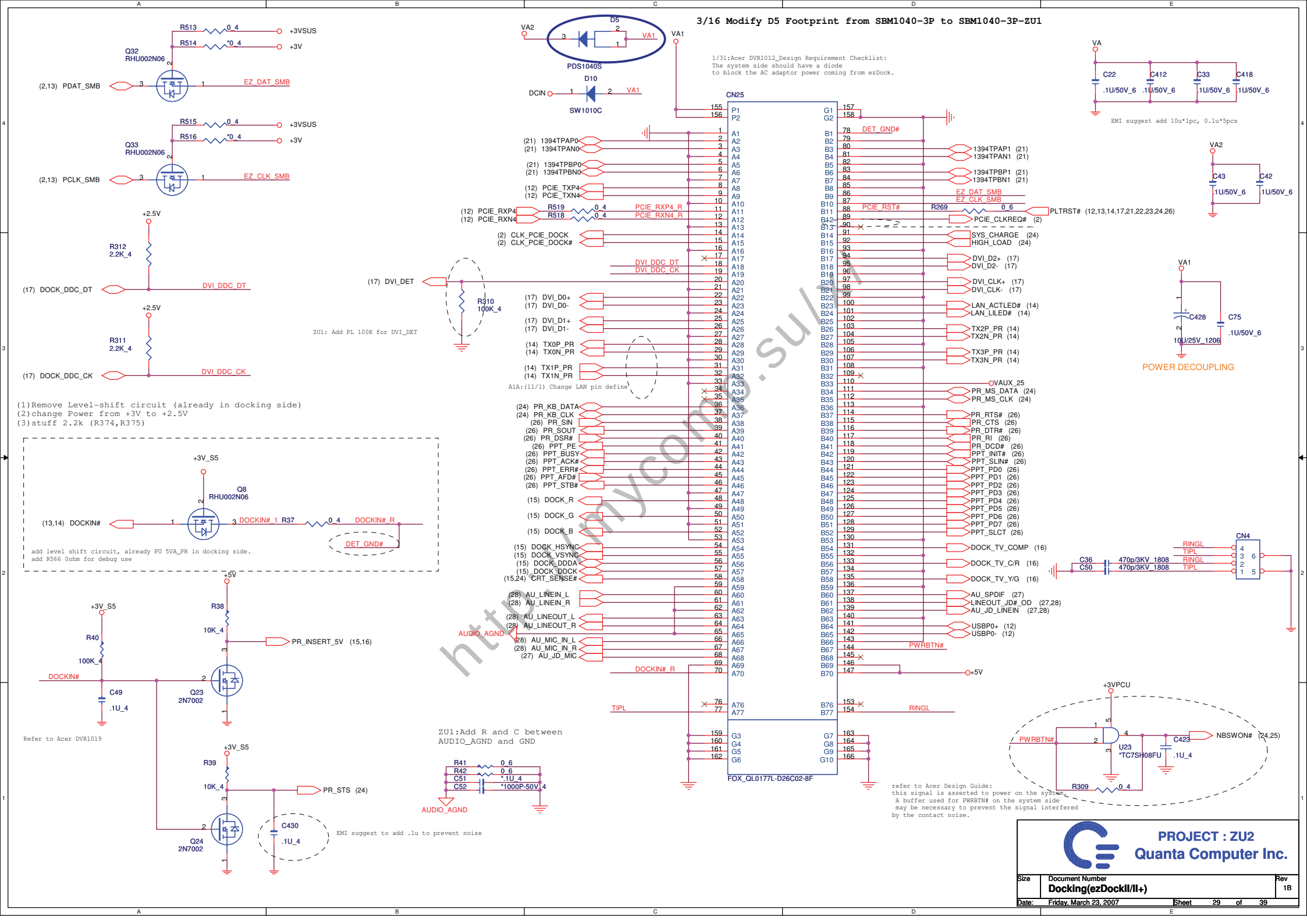
PROJECT : ZU2

Quanta Computer Inc.

3/16 Modify D5 Footprint from SBM1040-3P to SBM1040-3P-ZU1



http://mycomp.sulu/

PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	Docking(ezDockII/II+)	1B

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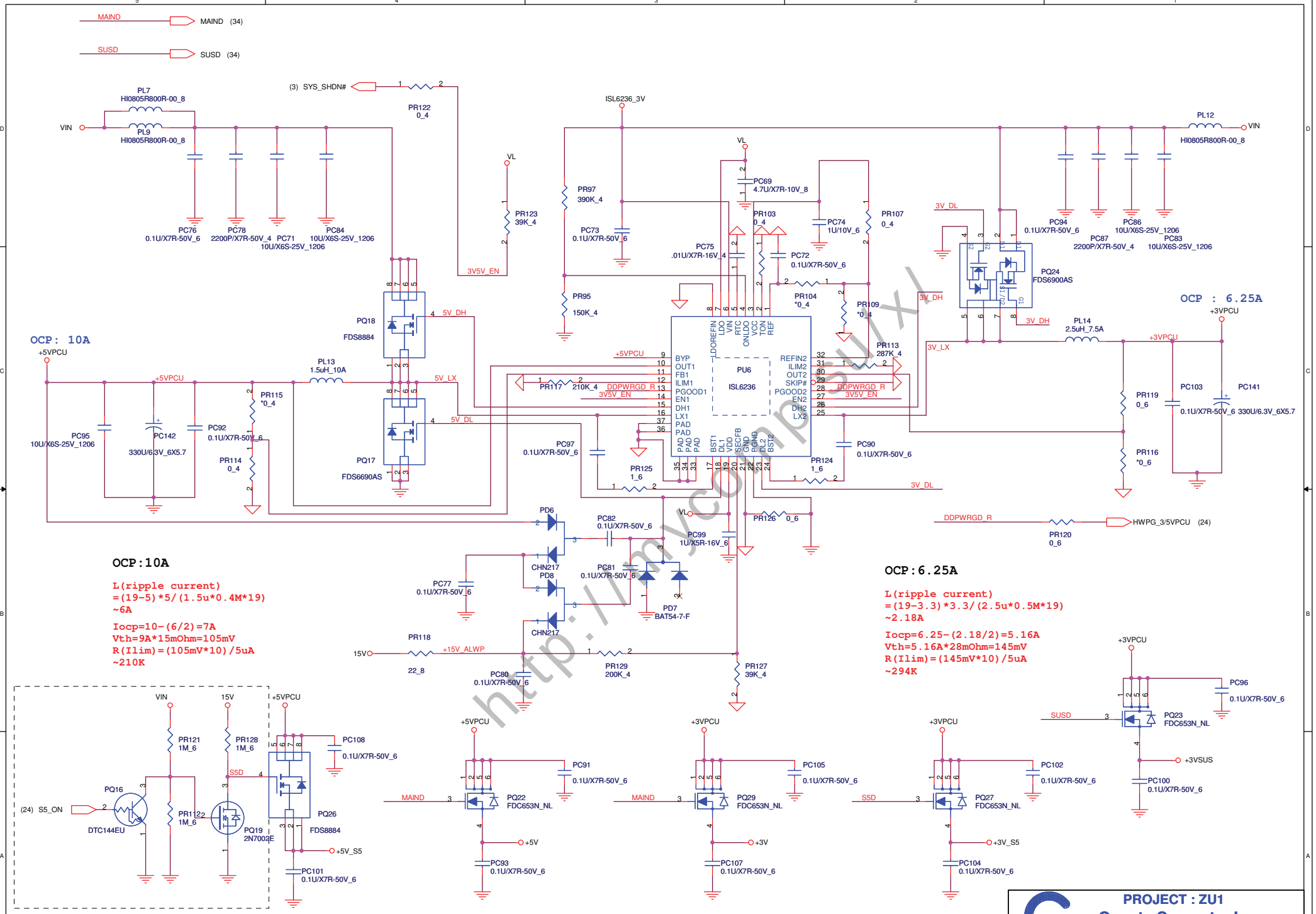

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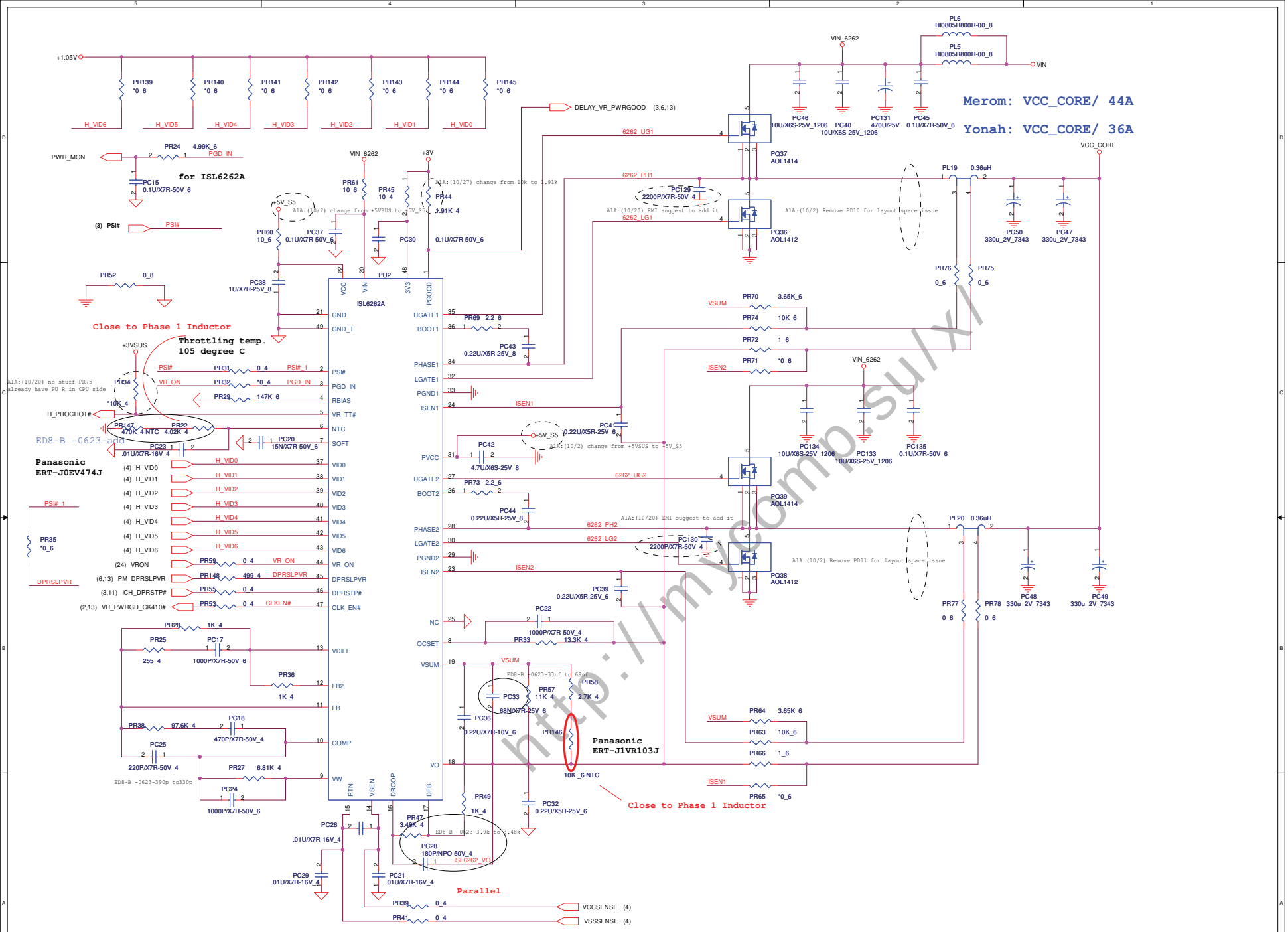

Size	Document Number	Rev
Custom	CPU Core (ISL6262A)	1D

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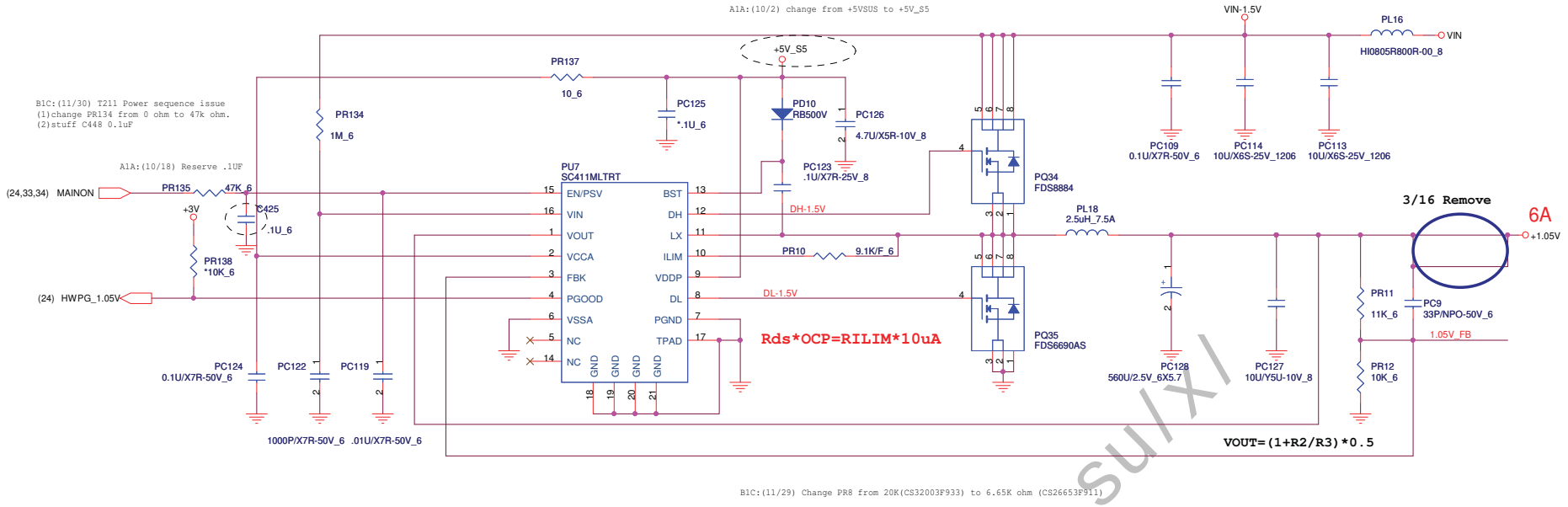

http://mycomp.su/xl

PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	VTT 1.05V (SC411)	1D
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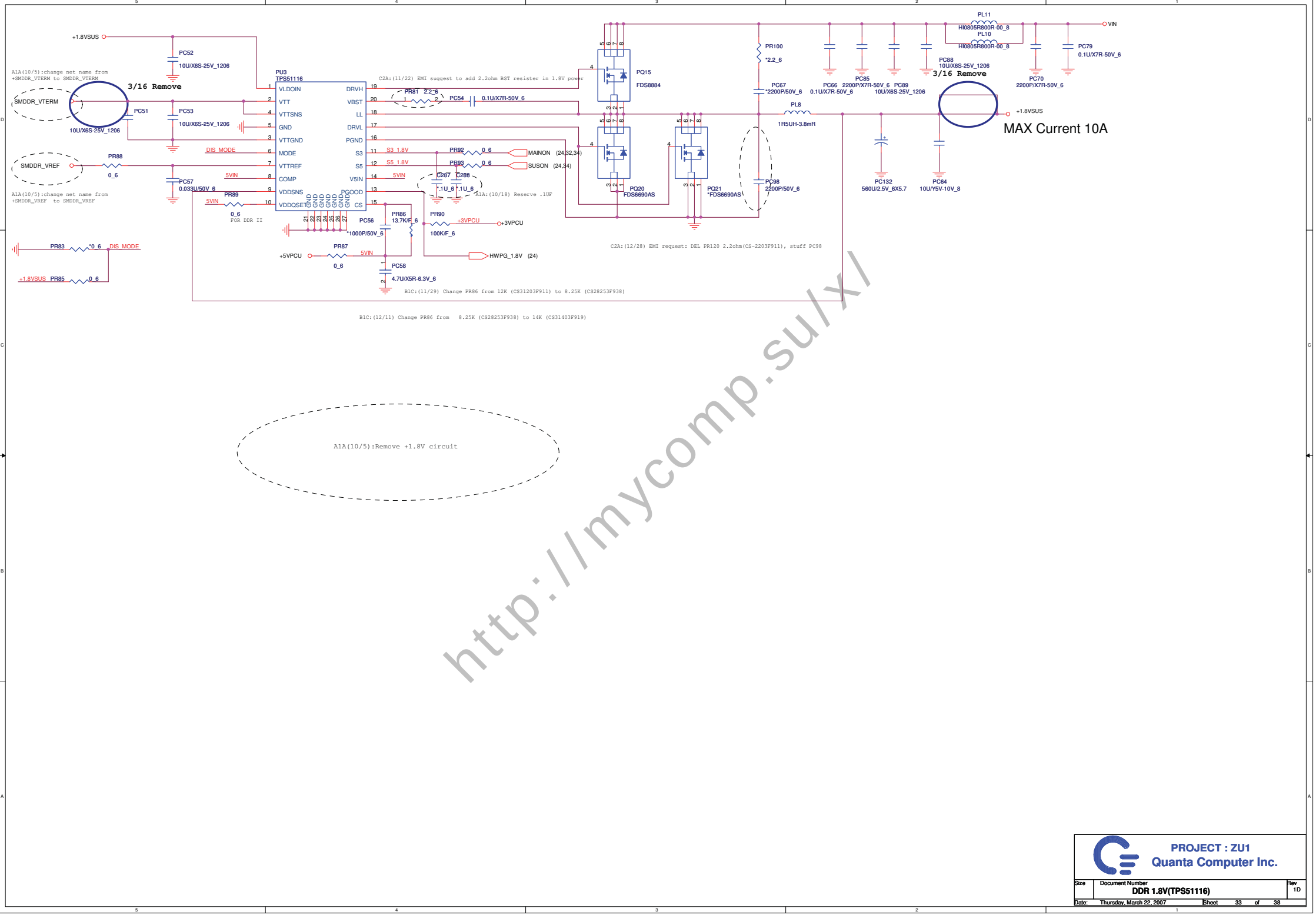

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PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1D

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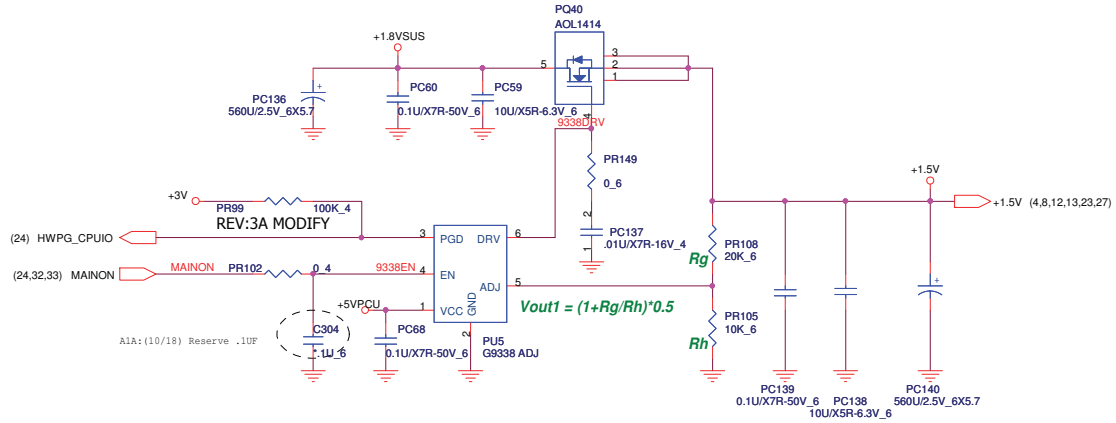

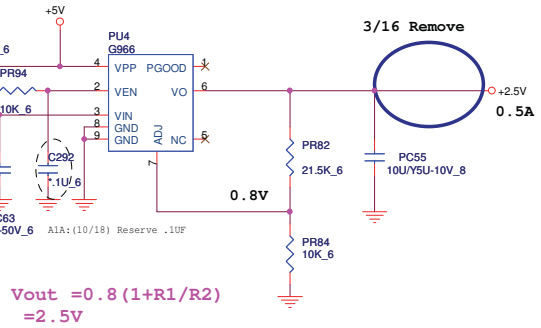

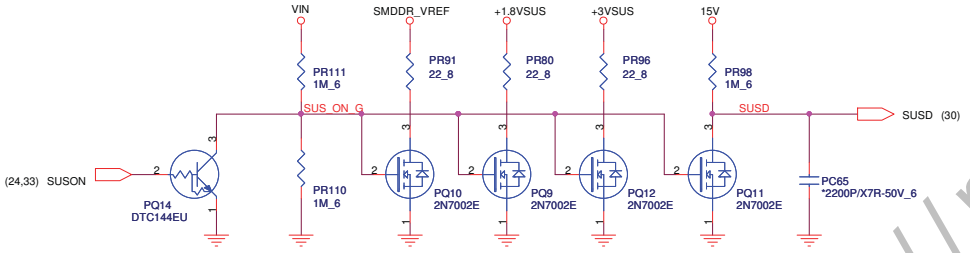

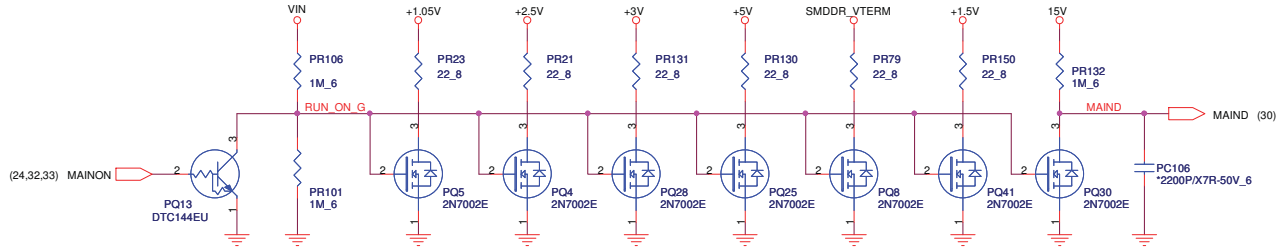

http://mycomp.su/x/

PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.5V/2.5V)	1D

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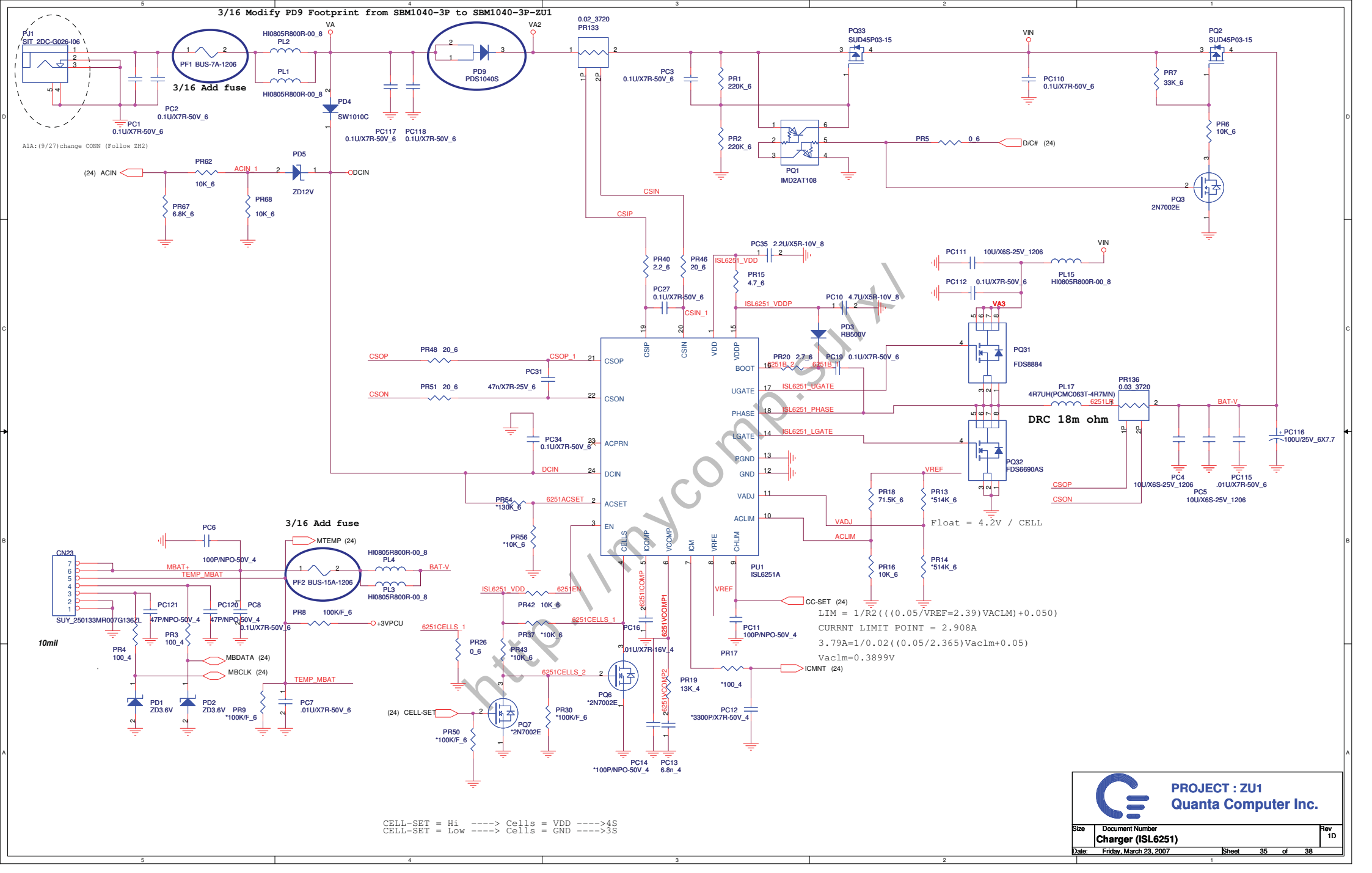

http://mycomp.su/x/