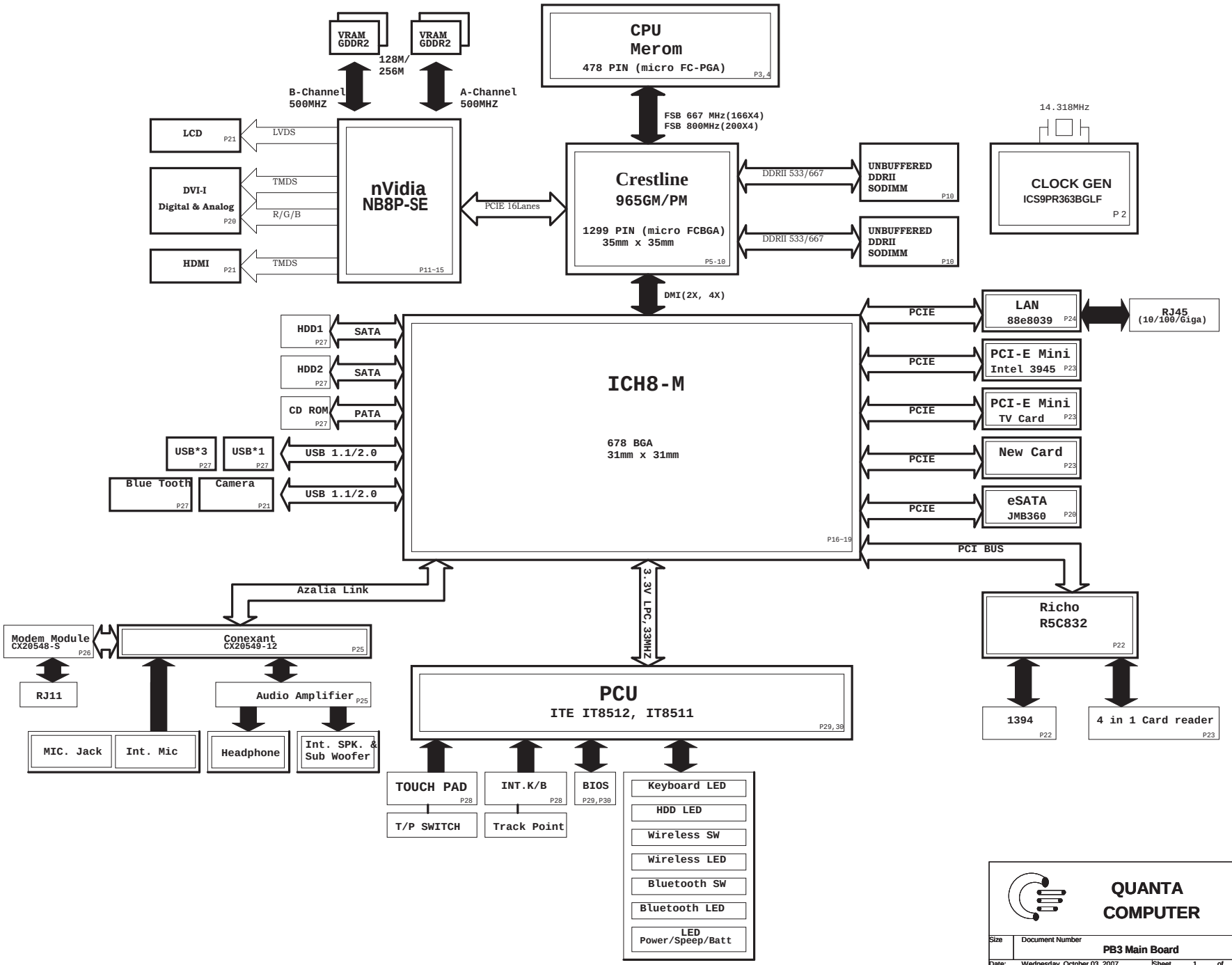
PB3 Block Diagram



QUANTA COMPUTER

Size	Document Number	Rev
	PB3 Main Board	1A

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Clock Generator

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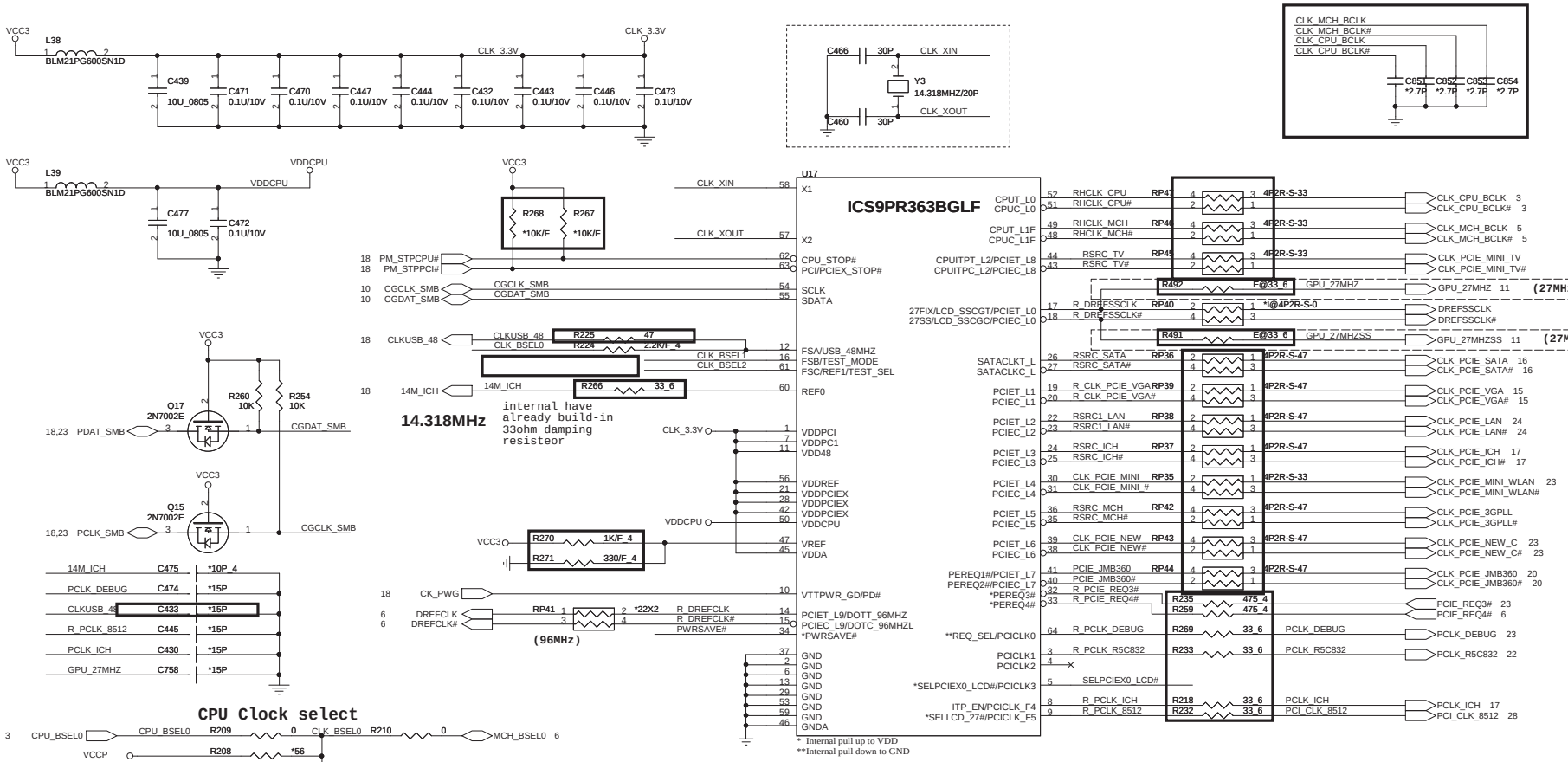
02



FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	**166.66**	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

ITP_EN(PIN8)

LOW : PIN43/44 SRC

HIGH : PIN43,44 CPUITP

PCIE_REQ1#	**PCIE_L0**	**PCIE_L6**
PCIE_REQ2#	**PCIE_L1**	**PCIE_L8**
PCIE_REQ3#	**PCIE_L2**	**PCIE_L4**
PCIE_REQ4#	**PCIE_L3**	**PCIE_L5 PCIE_L7**

PIN 64 : High for REQ_SEL
Low for PCICLK output

VREF
Keep Rpull-up=1K ohm and variable Rpull-down to measure CPU and PCIEX Vtop

Rpull-up R703	Rpull-down R704	CPU-T Vtop (mV)	PCIEX-T Vtop (mV)
1K	203	836	933
1K	222	799	906
1K	236	774	868
1K	275	721	834
1K	298	688	797
1K	329	664	778
1K	362	615	720
1K	372	595	706
1K	380	566	671
1K	385	513	634

PIN 5 R717	PIN 9 R715	PIN 14/15
LO (10K)	LO (10K)	**PCIEX9**
	HI (NC)	DOT96
HI (NC)	LO (10K)	PCIEX9
	HI (NC)	**DOT96**

QUANTA COMPUTER

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	Clock Generator	1A

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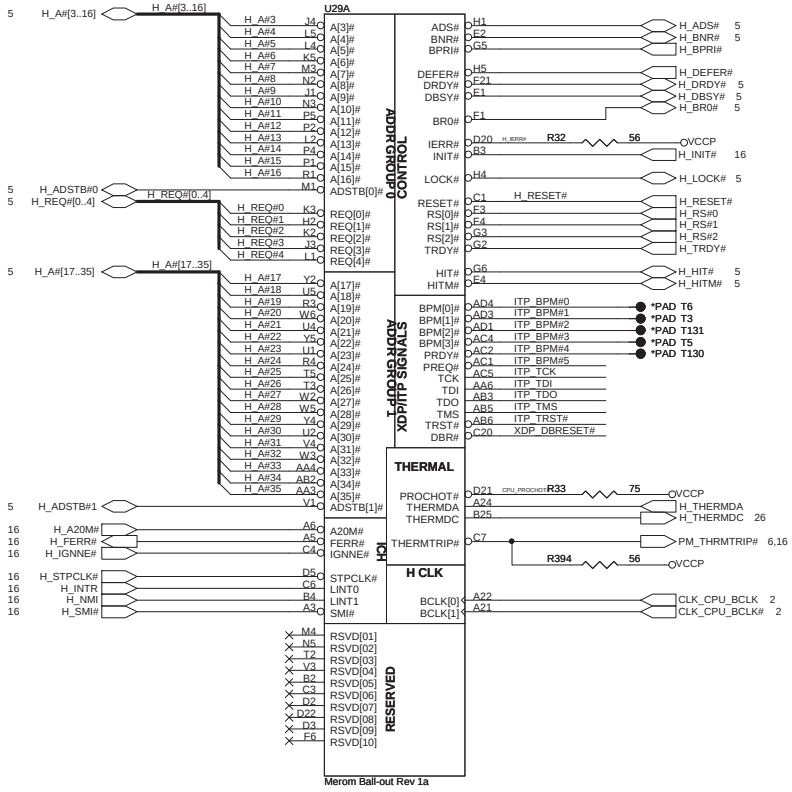
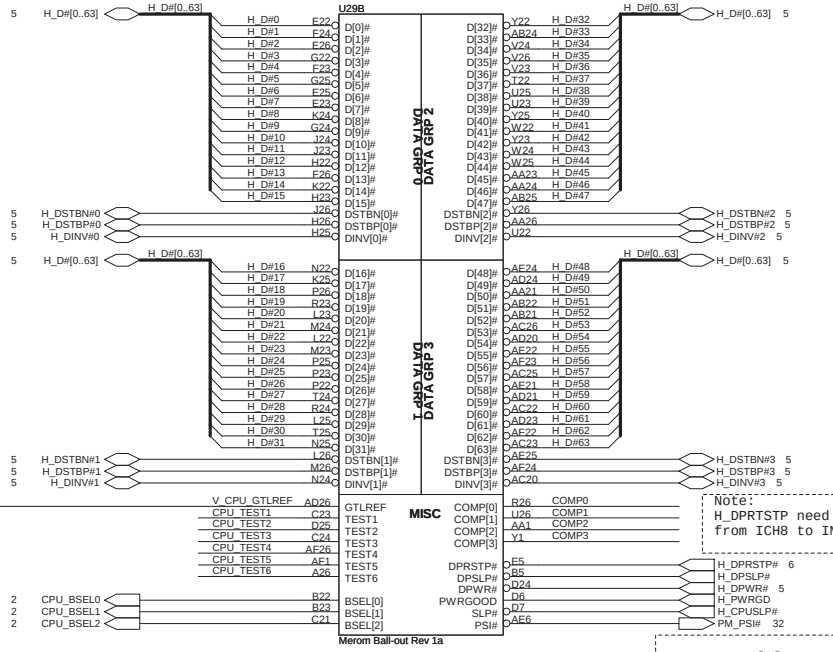
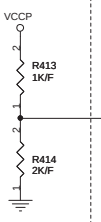
CPU-Host Bus



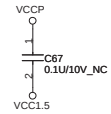


Layout Note:
Place voltage divider within 0.5" of GTLREF pin



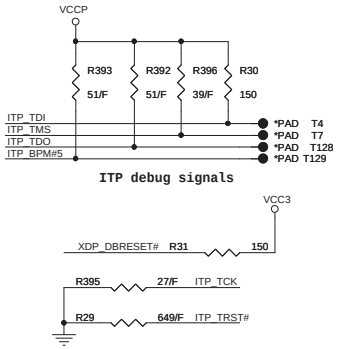
Note:
H_DPRTSTP need to daisy chain from ICH8 to IMVP6 to CPU.

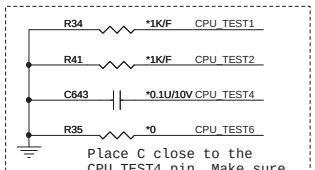
Reserved for EMI.



Populate ITP700Flex for bringup

Layout Note:
Place R4,R361,R346 & R7 close to CPU.



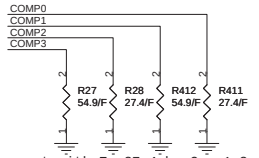


Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

PAD T8 CPU_TEST3
PAD T132 CPU_TEST5

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0



Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

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	CPU-Host Bus	1A
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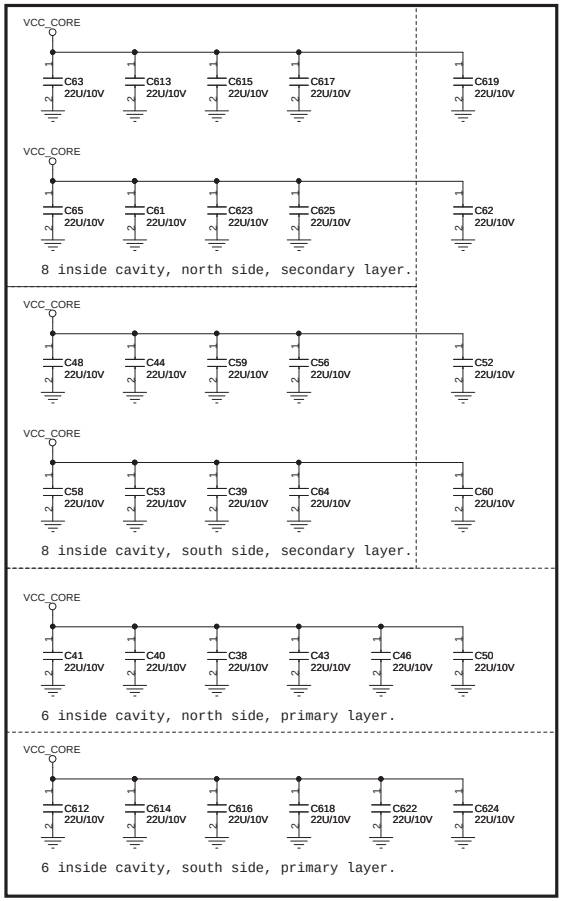
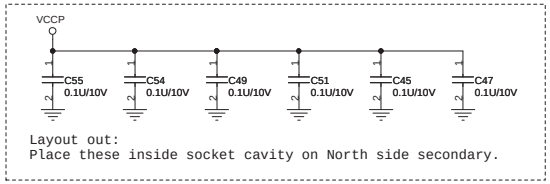
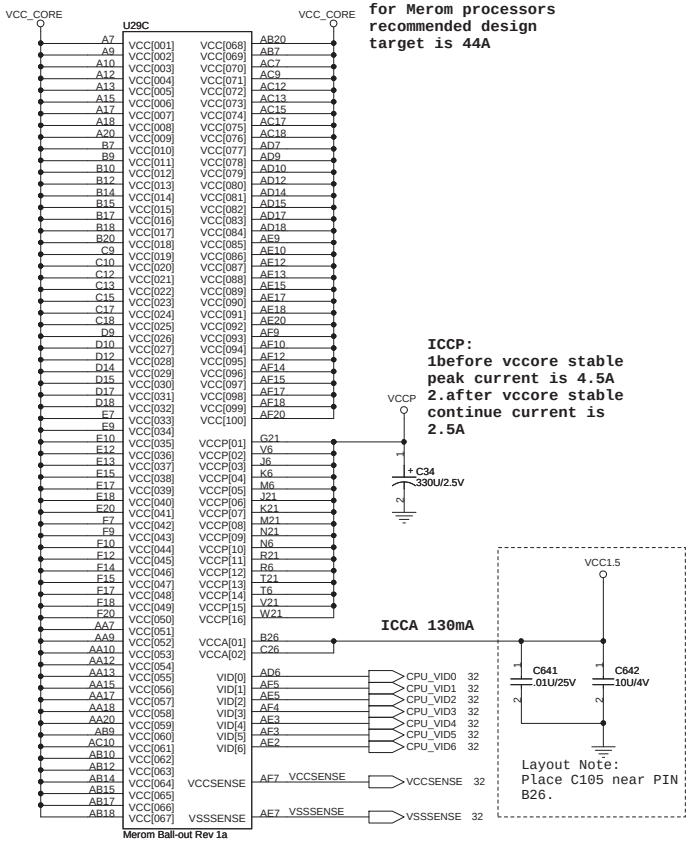
CPU Power & GND

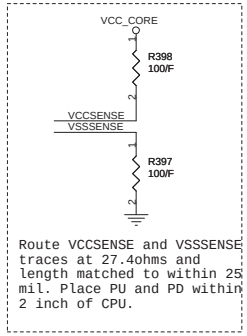


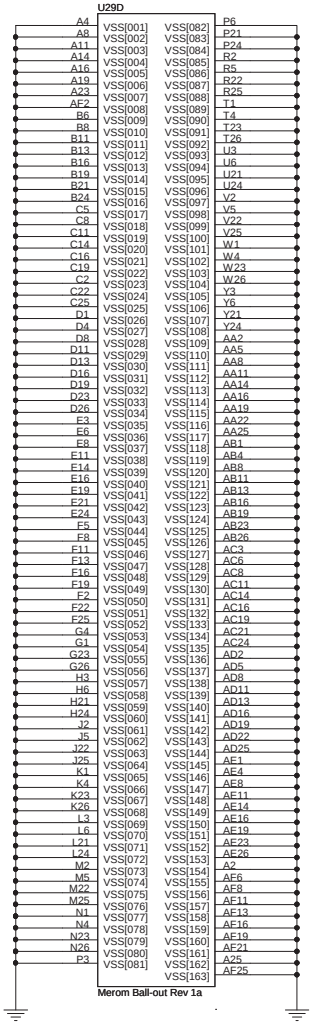


ICCODE:
for Merom processors
recommended design
target is 44A



ICCP:
1before vccore stable
peak current is 4.5A
2.after vccore stable
continue current is
2.5A





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	CPU-Power/NC	1A
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Crestline-Host, VSS

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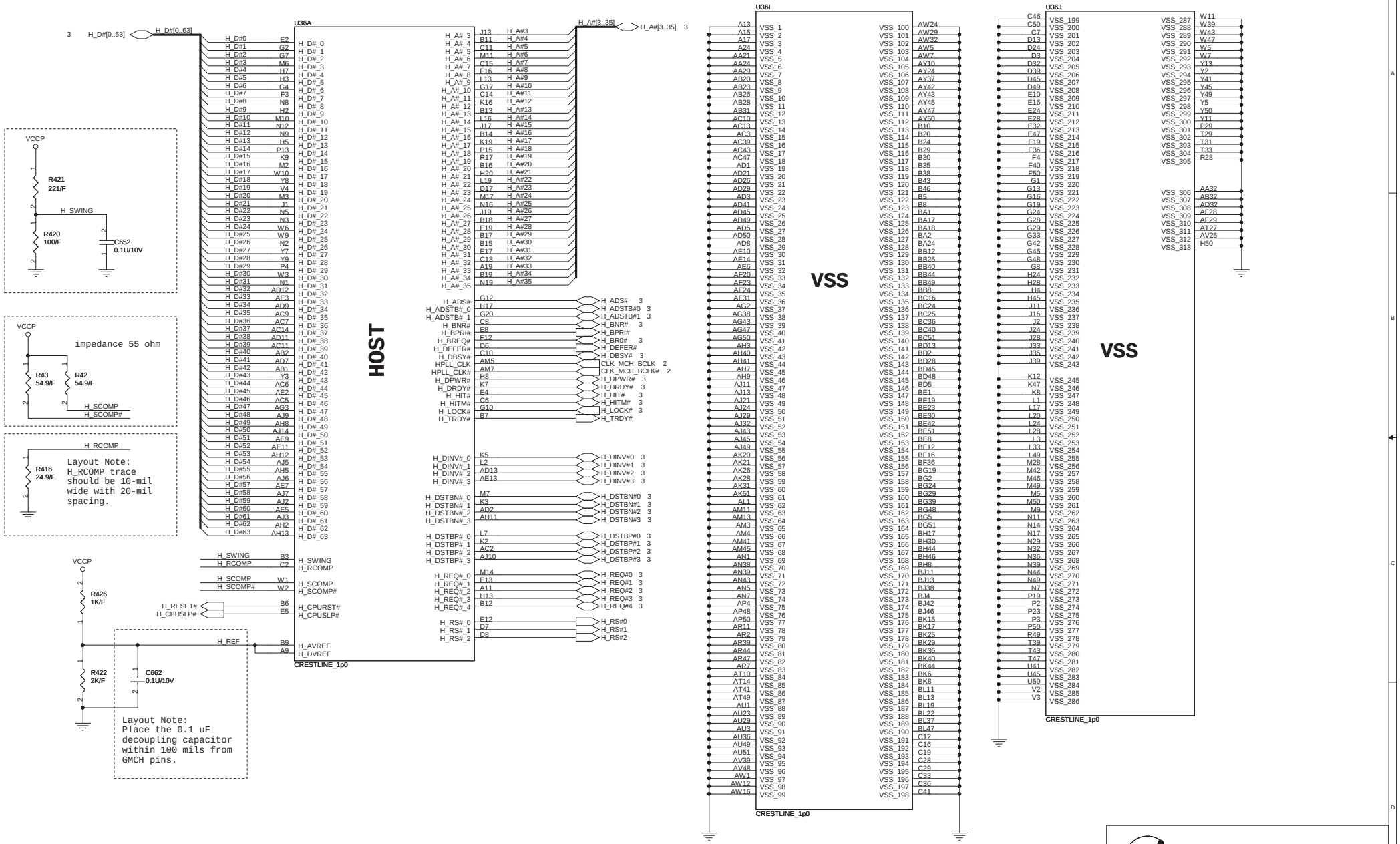

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	Crestline-Host, VSS	1A
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Crestline-VGA, DMI

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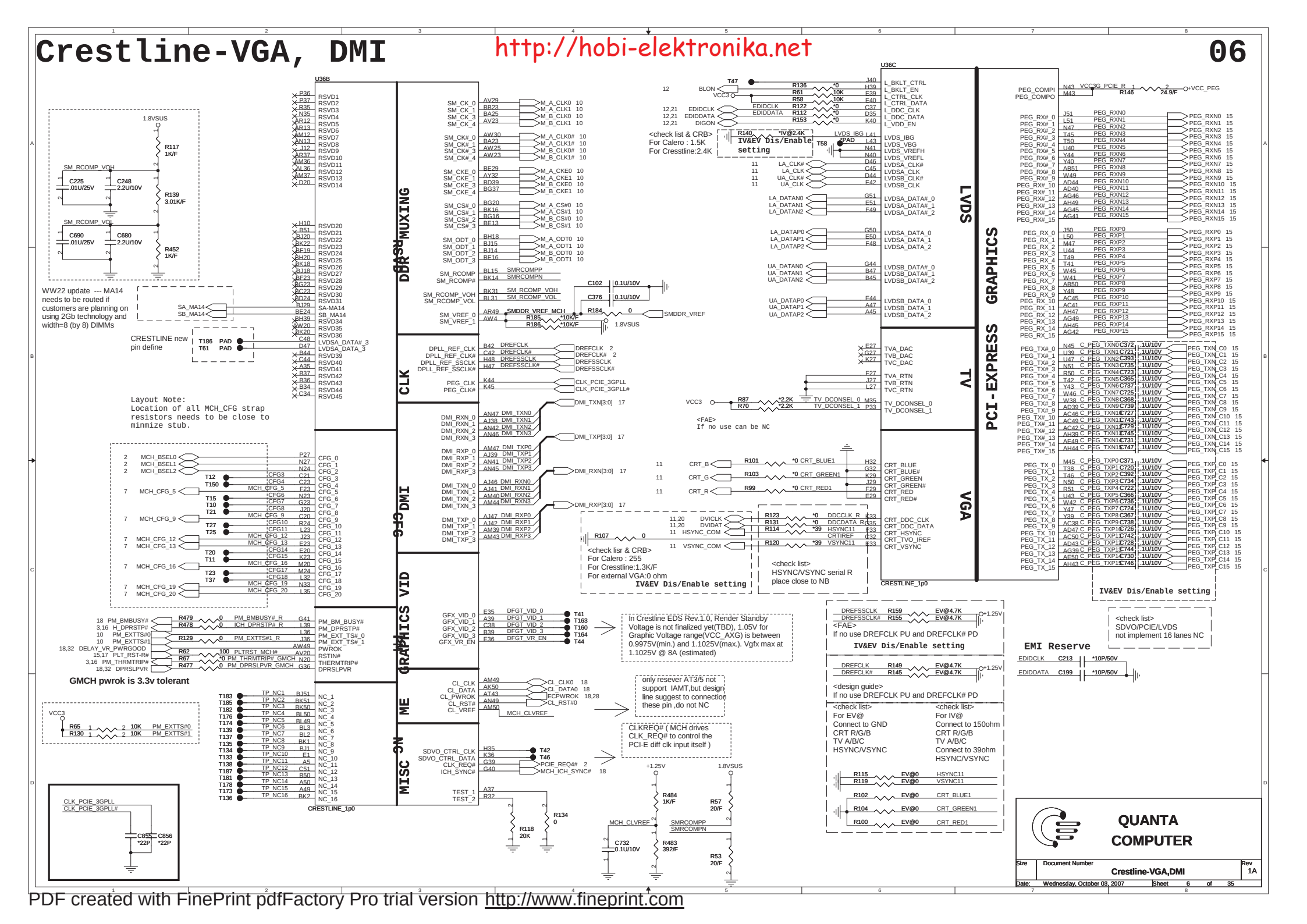
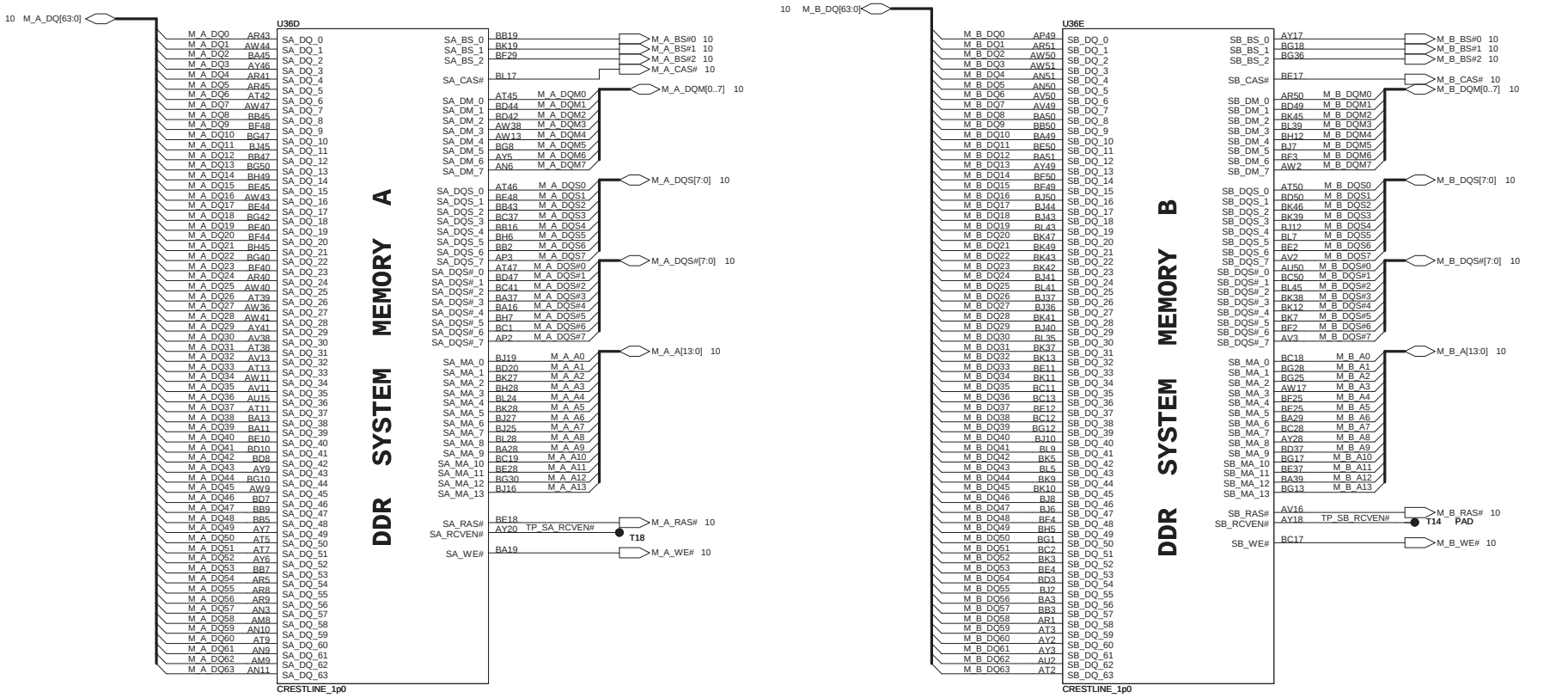




MCH_CFG_5 Low = DMIX2
High = IDMIX4(Default)

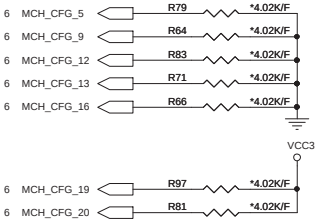
MCH_CFG_9 Low = Reverse Lane
High = Normal operation(Default)

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

MCH_CFG_16 Low = ODT Disable
High = ODT Enable(Default)

MCH_CFG_19 Low = Normal operation(Default)
High = Reverse Lane

MCH_CFG_20 Low = Only SDVO or PCIE X1 is operational(Default)
High = SDVO andPCIE X1 are operating simultaneously via the PEG port



Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

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	Crestline-DDR II	1A
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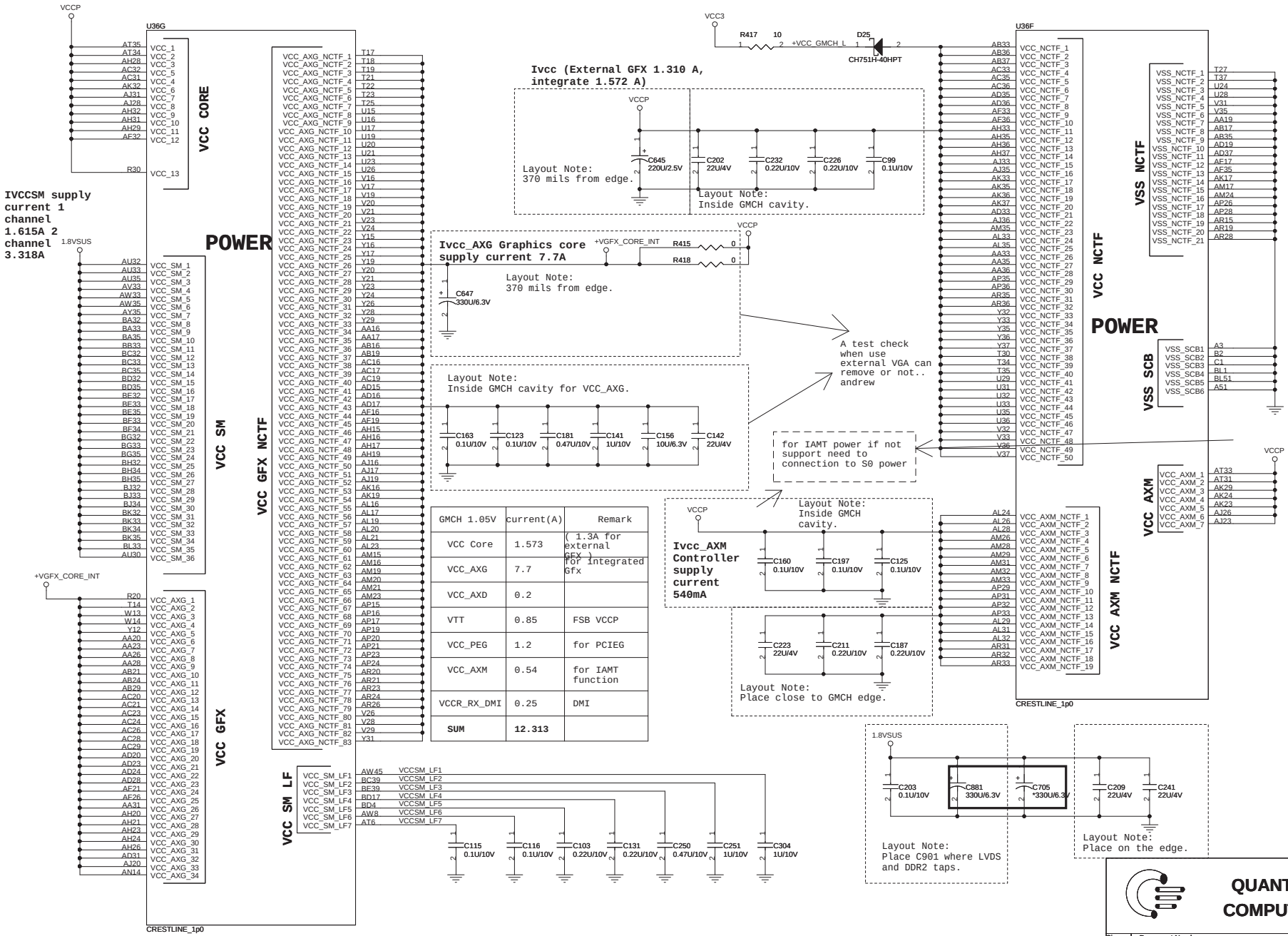

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX) for integrated Gfx
VCC_AXG	7.7	
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	12.313	

Crestline-Power

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CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCSYNC connect
to GND

FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC

FB_180ohm+-25%
100mHz_1500mA
0.09ohm DC

10uH+-20%_100mA

0.1Caps should be placed 200 mils with in its pins.

Ivcca_PEG_BG supply current 100mA

Ivcc_VTT FSB supply current 0.85A

Place on the edge.

Reserved L81 pad for inductor.

Place caps close to VCC_AXD.

Ivcc_DMI supply current 100mA

Place caps close to VCC_AXF

Ivcc_PEG supply current 1.2A

Ivcc_RX_DMI supply current 250mA

+3V_VCC_HV

40 mil wide

FB_220ohm+-25%_100MHz
_2A_0.1ohm DC

U36H

CRESTLINE_1p0

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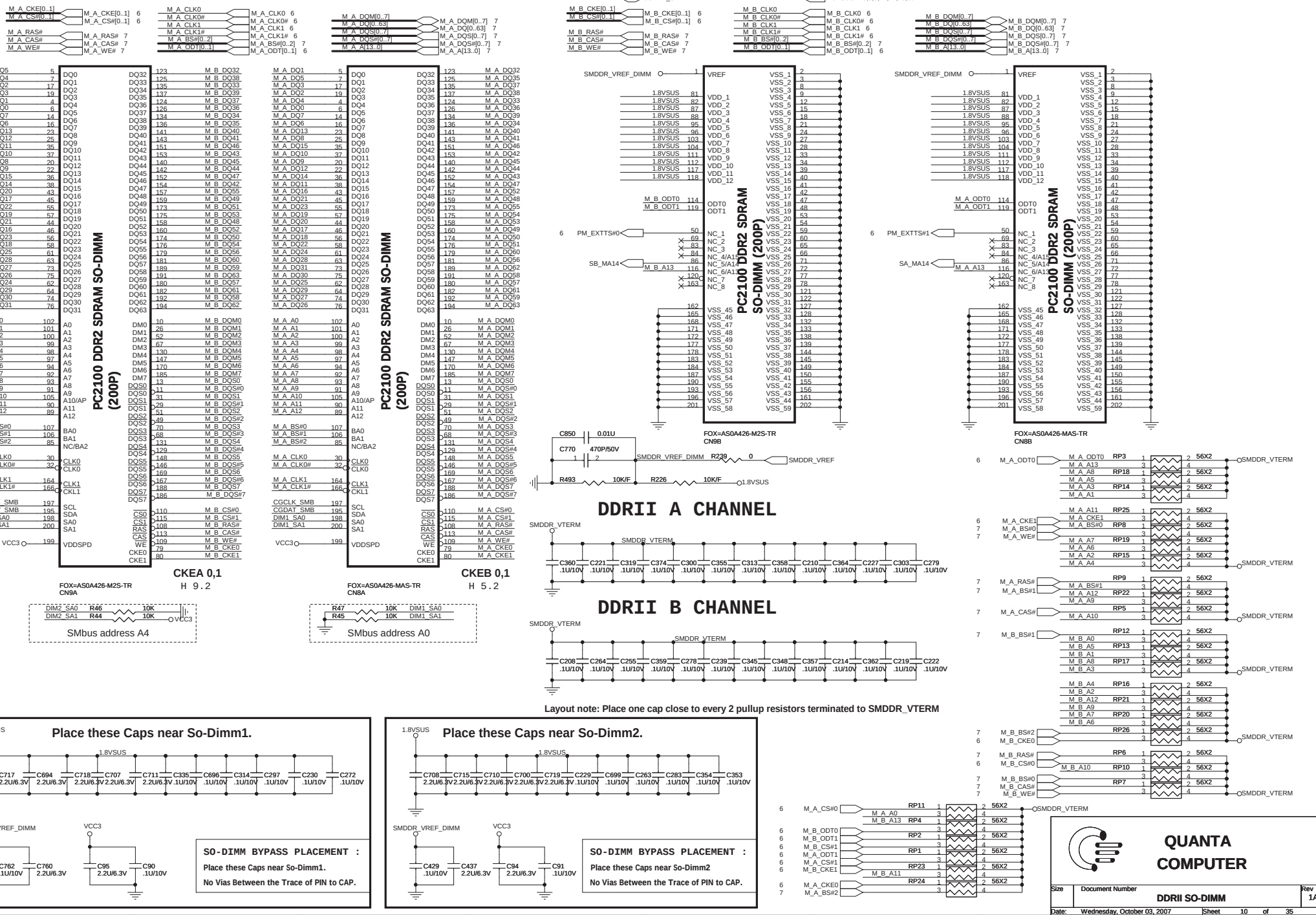
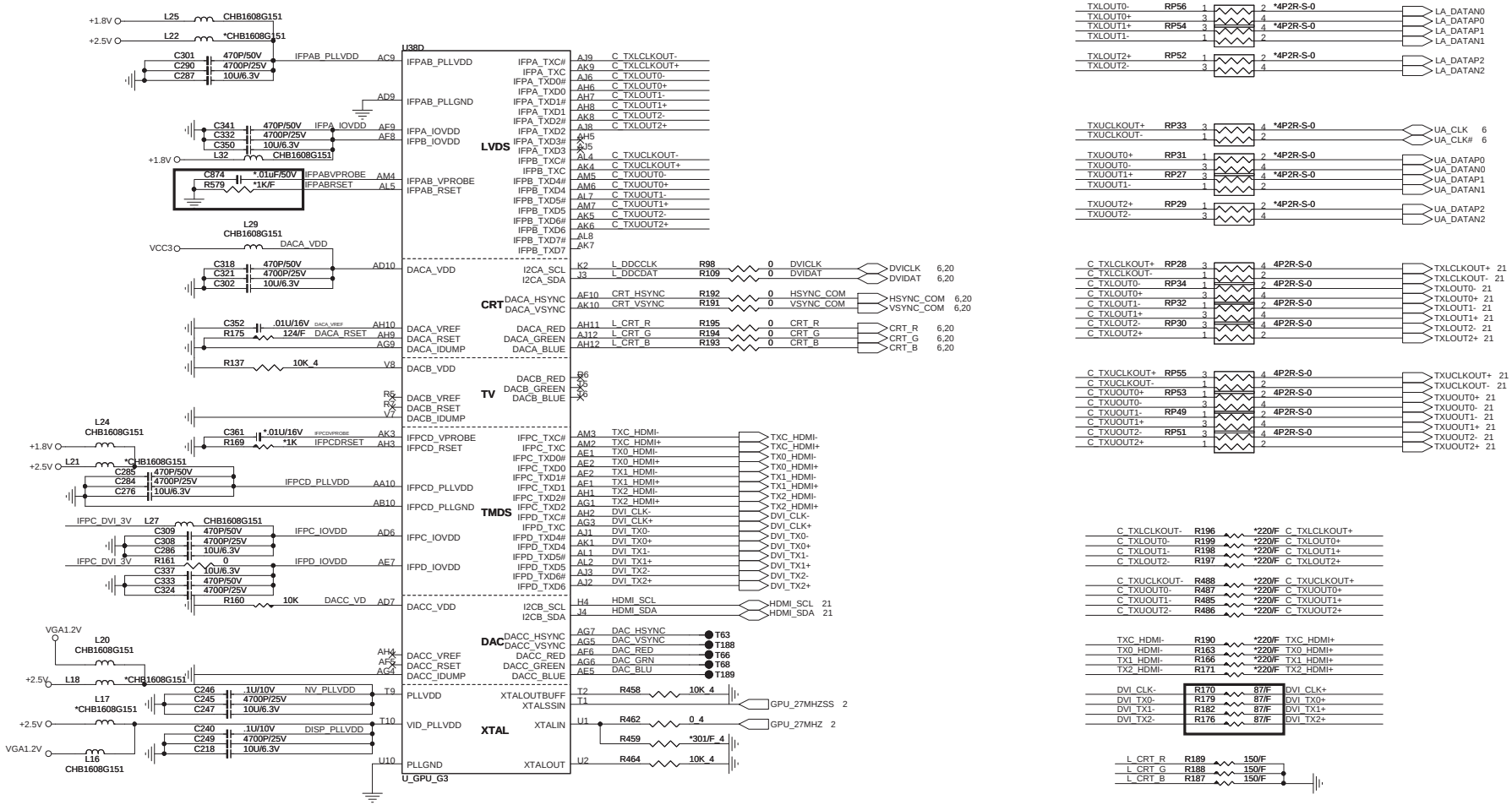
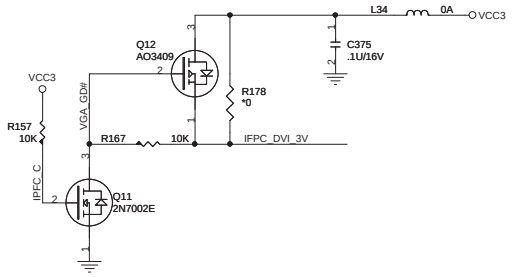
DDRII-SO DIMM







QUANTA COMPUTER

Size	Document Number	Rev
	NVG73M-LVDS,DVI,CRT,TV	1A
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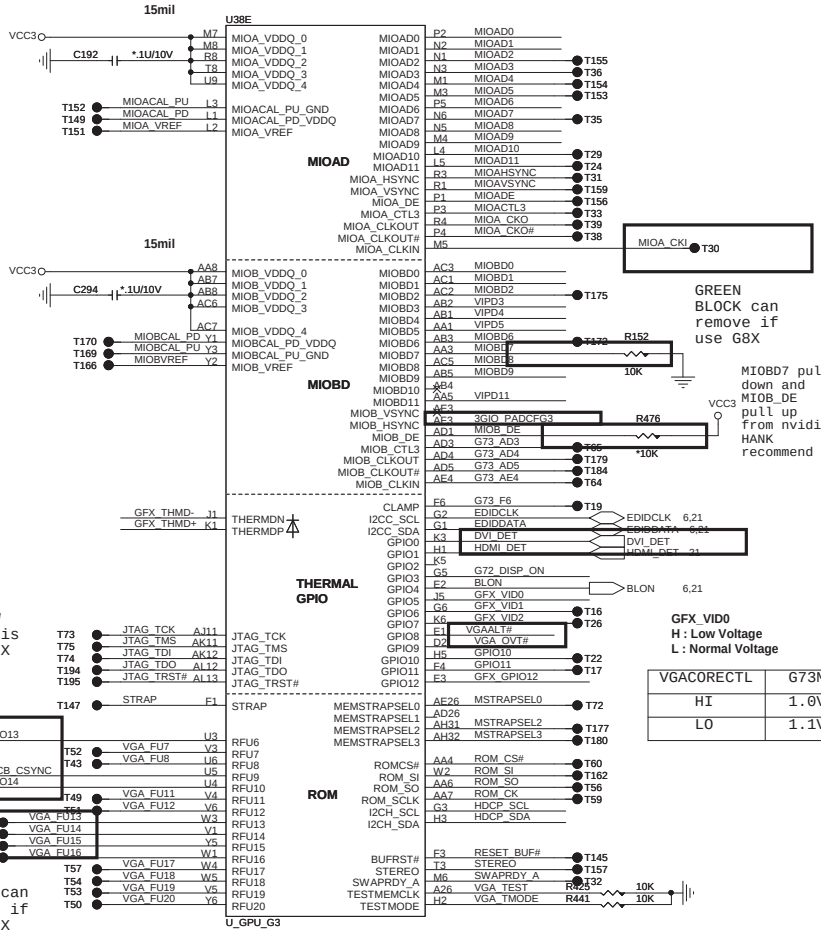
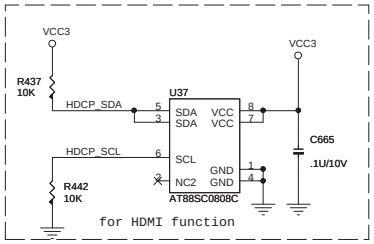
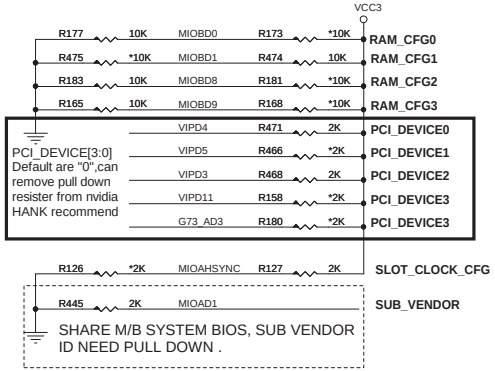
NVG73M ROM, GPIO, Strap

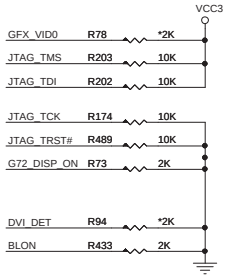




PCI DEVICE

PCI_DEVICE[3:0]				DESCRIPTION
R471	R466	R468	R158	
	1000			G72M/G73M
	0110			G72M-Z
	0111			G72M-V/G73M-V
	0001			NB8M-SE
	1010			NB8P-SE
	1110			NB8P-GS

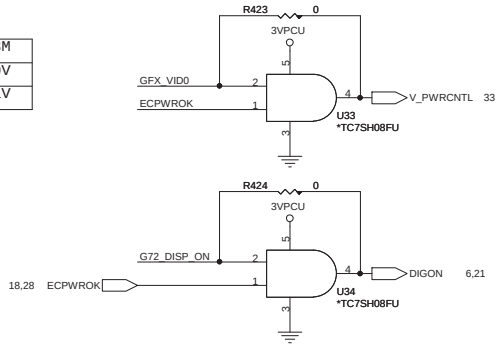




GFX_VID0
H : Low Voltage
L : Normal Voltage

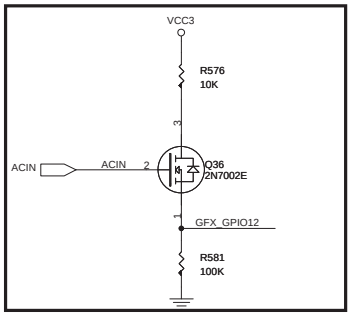
VGACORECTL	G73M
HI	1.0V
LO	1.1V

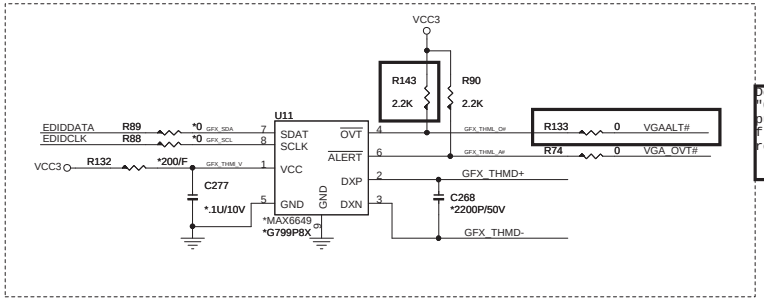
For VGA core power switch

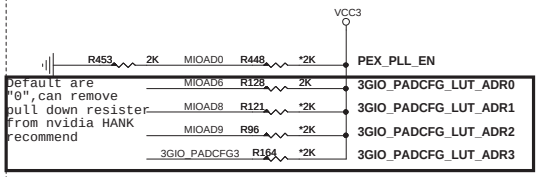


G73M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix







QUANTA COMPUTER

Size	Document Number	Rev
	NVG73M-ROM,GPIO,Strap	1A
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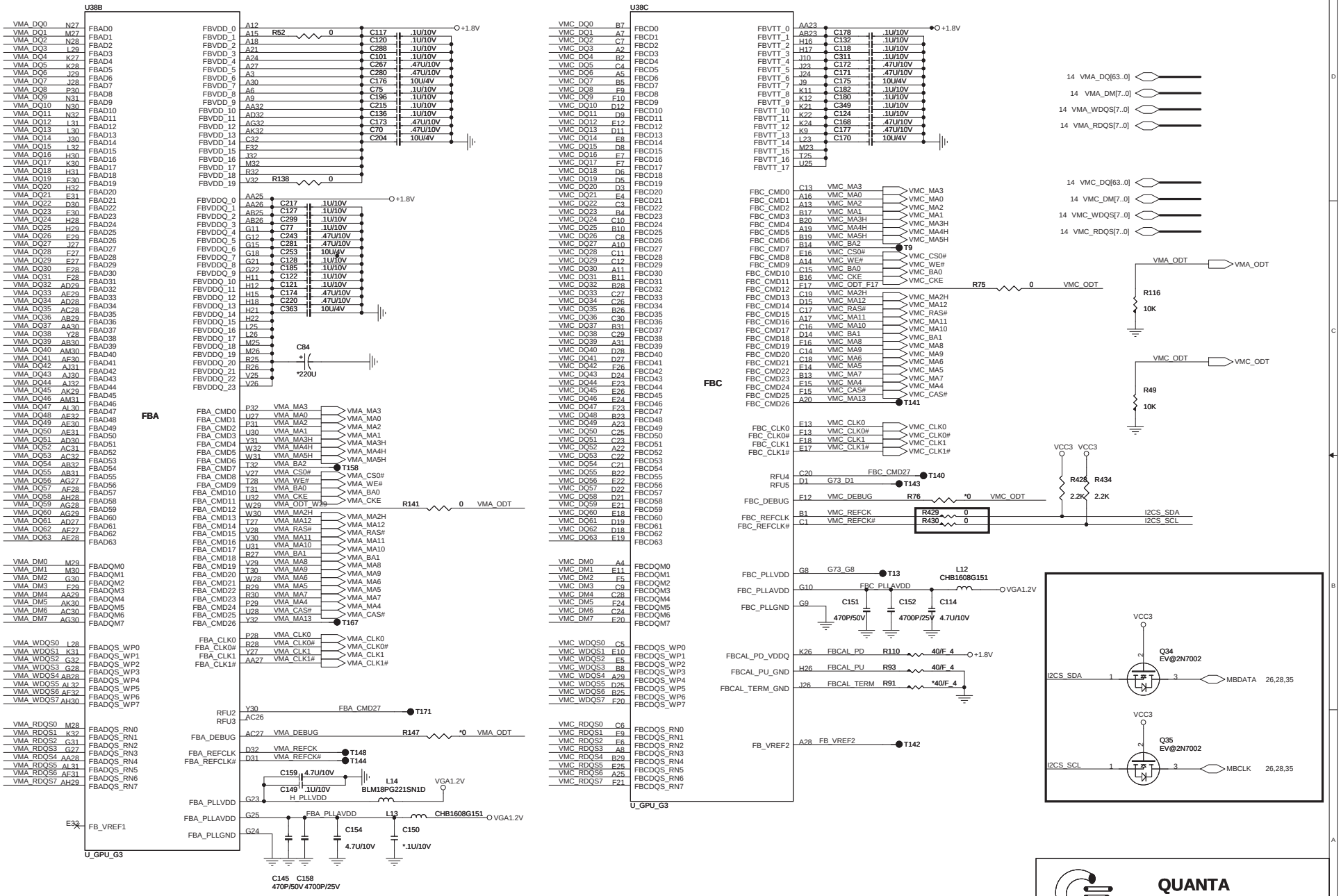

QUANTA COMPUTER		
Size	Document Number	Rev
	NVG73M Memory I/F	1A
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GDDRII

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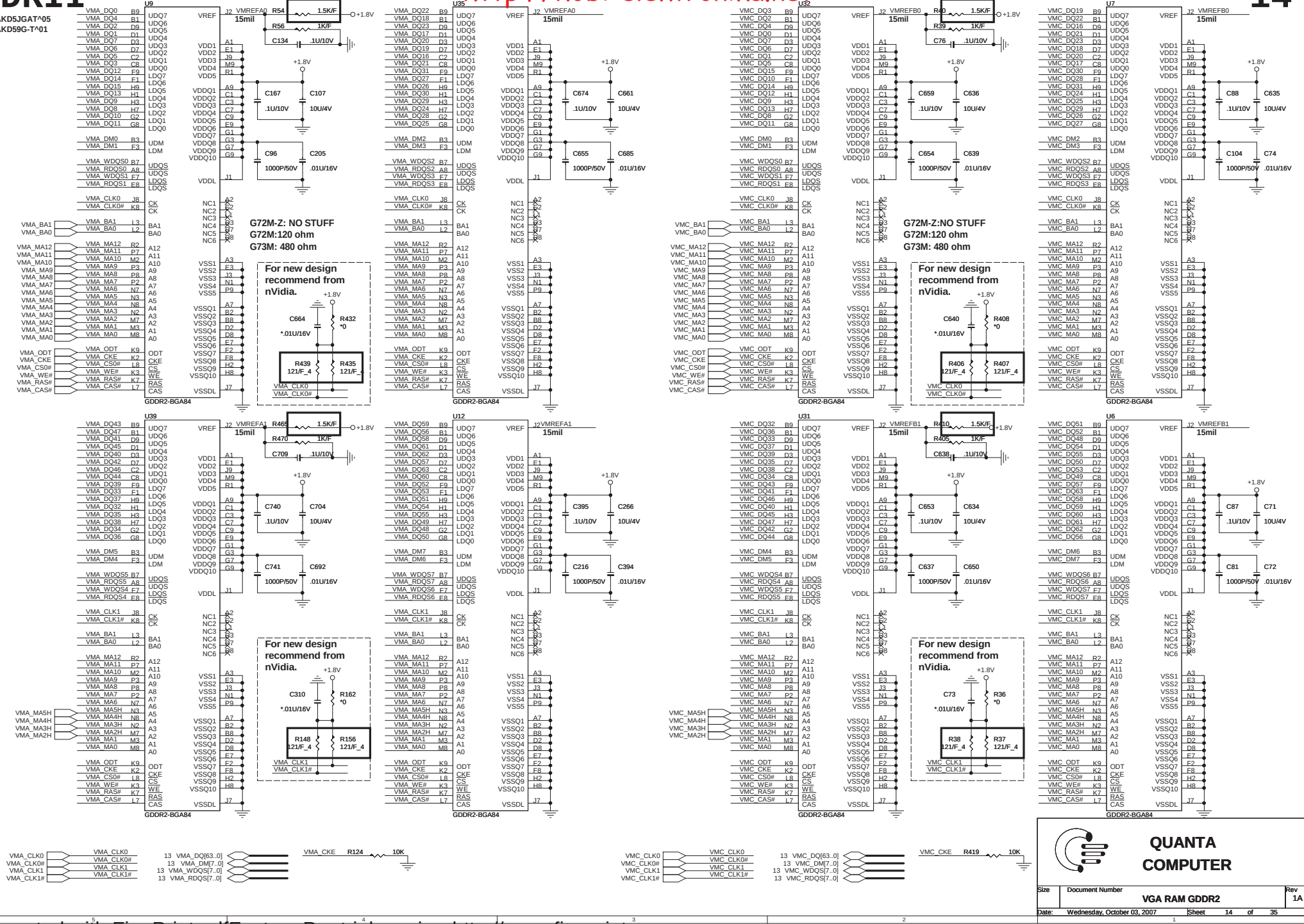
256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01



QUANTA COMPUTER

Size	Document Number	Rev
	VGA RAM GDDR2	1A
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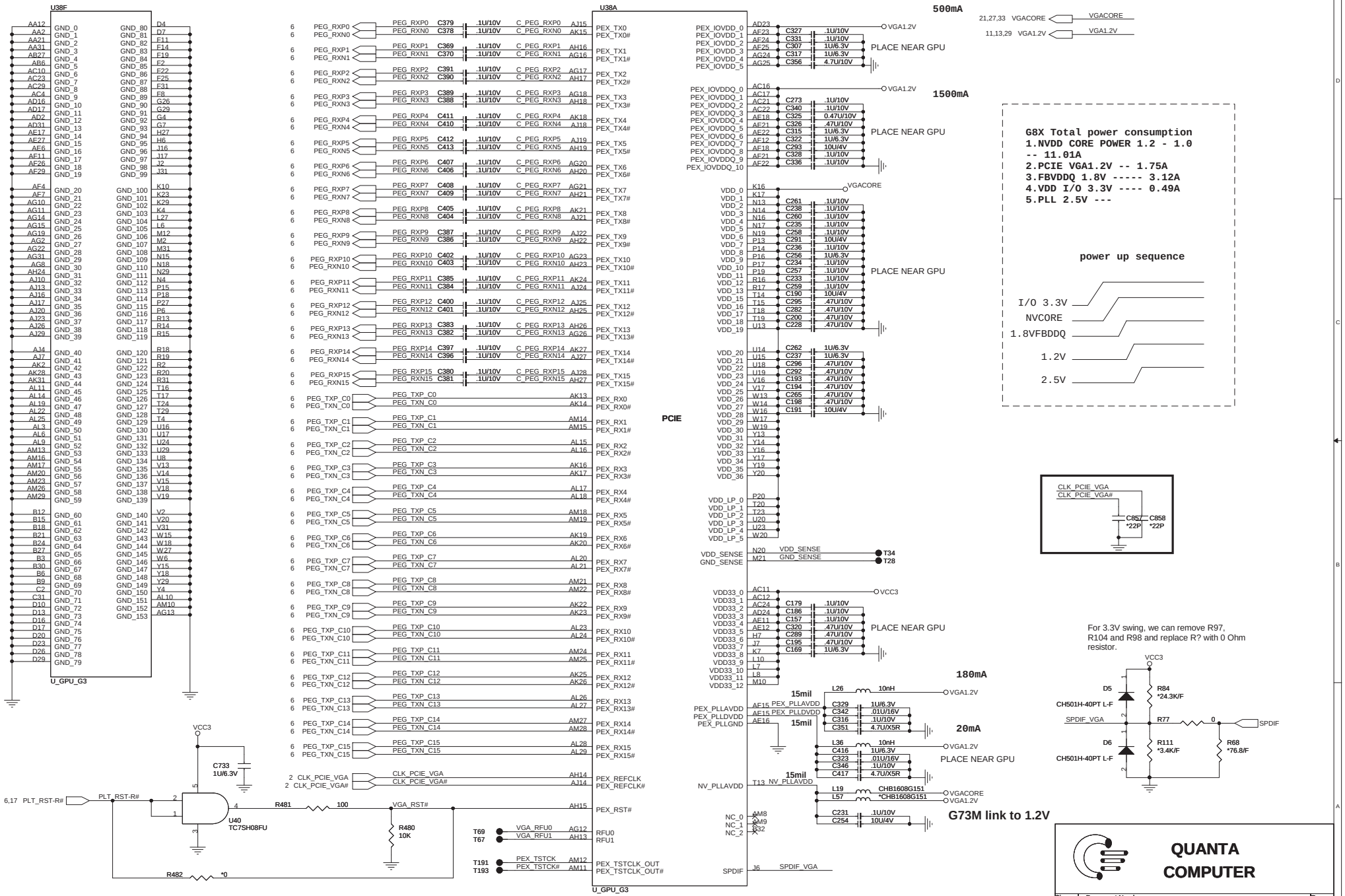
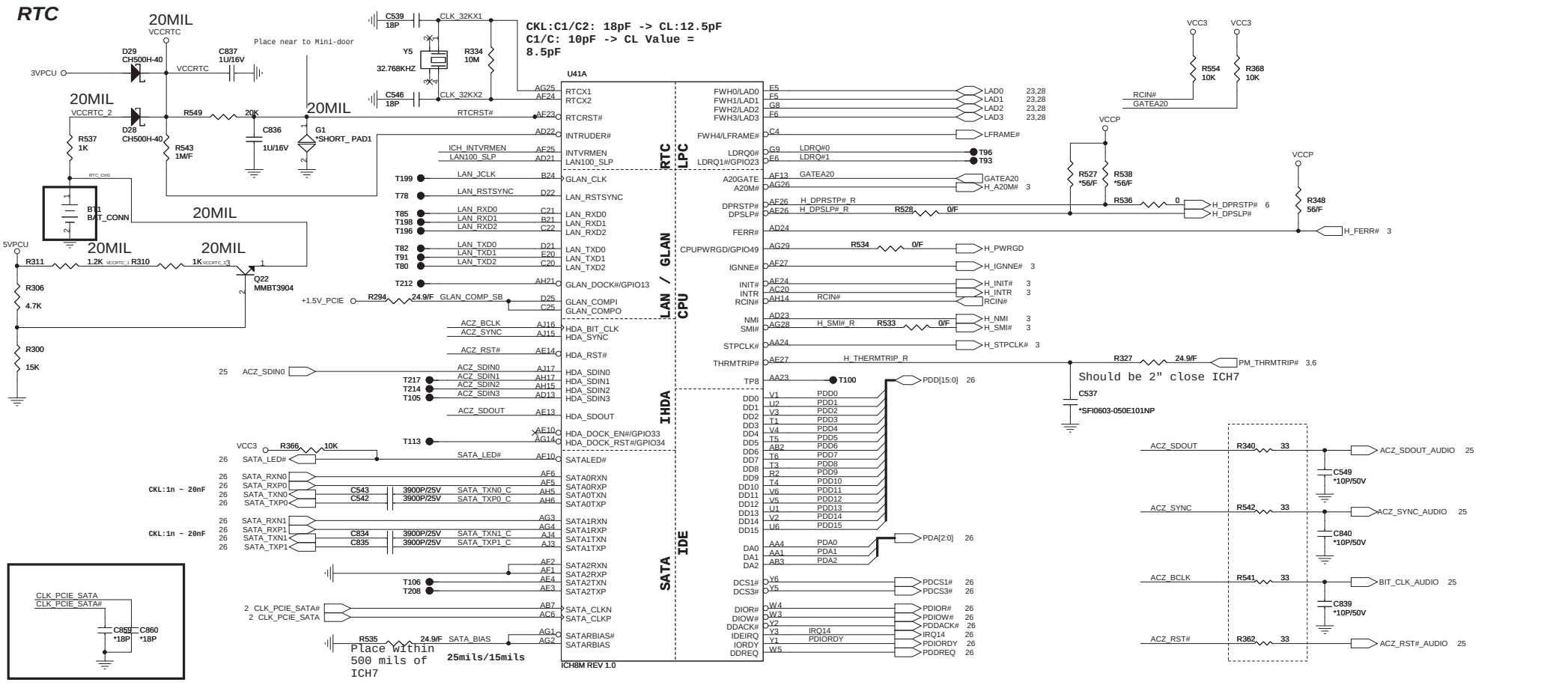
NVG73M (PCIE I/F)





SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

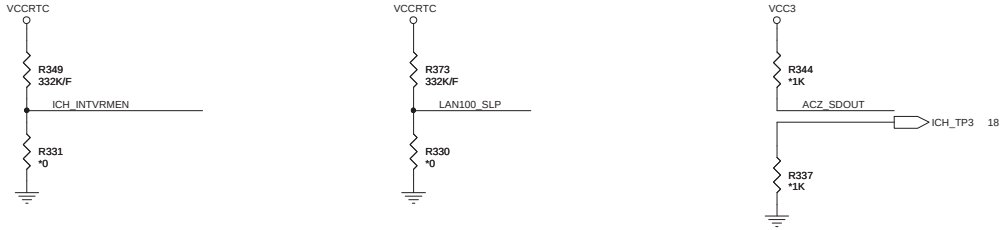
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

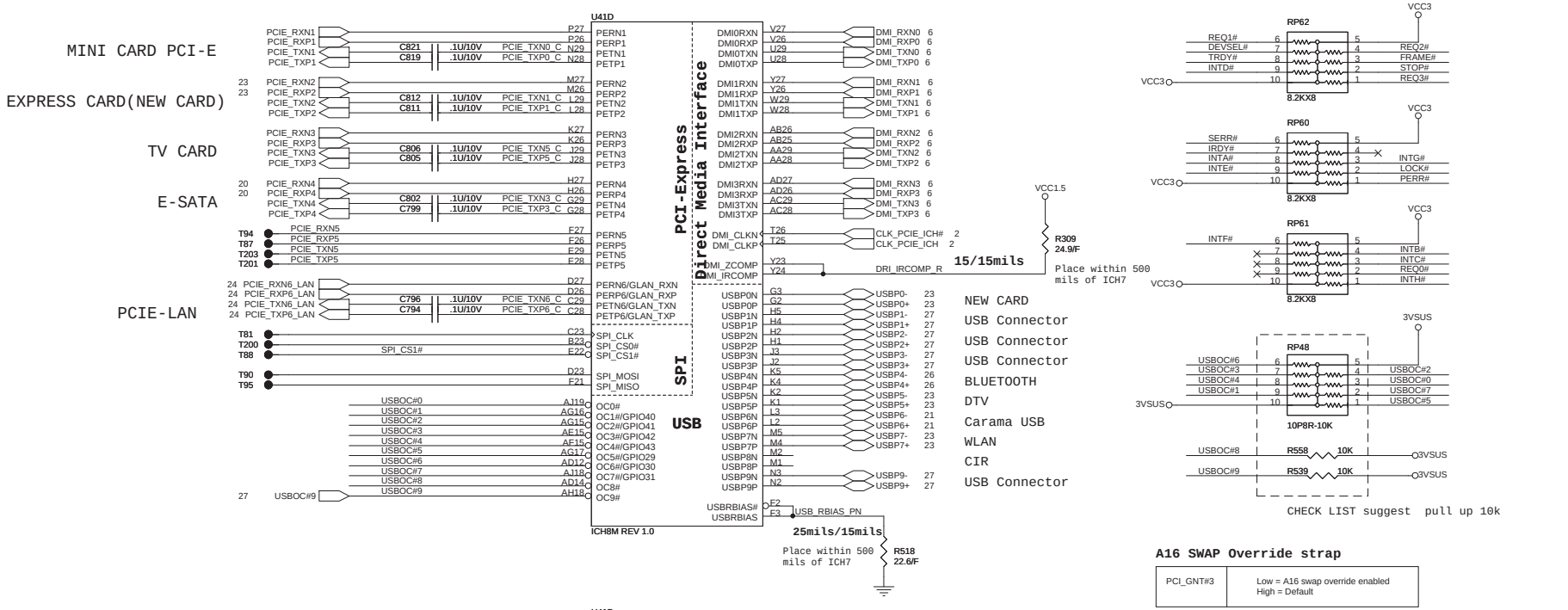
XOR Chain Entrance Strap

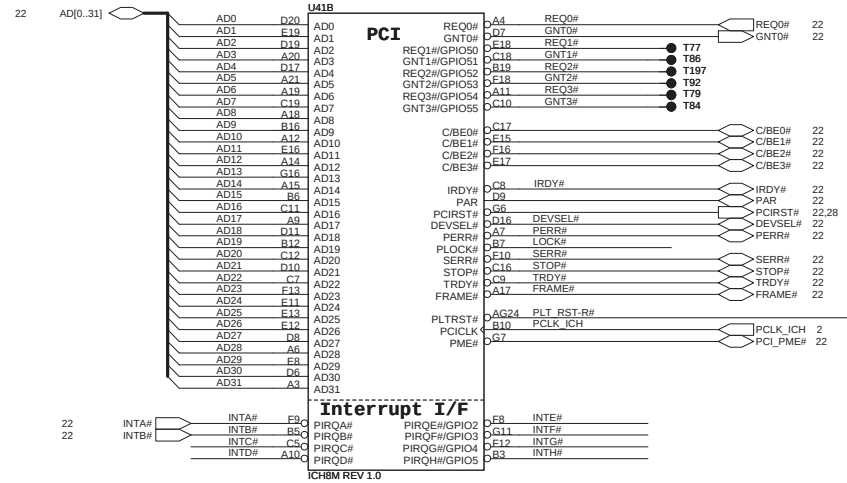
ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



QUANTA COMPUTER

Size	Document Number	Rev
	ICH8-M Host	1A
Date: Wednesday, October 03, 2007	Sheet 16 of 35	





A16 SWAP Override strap

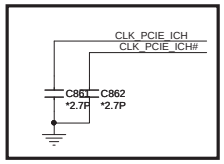
PCI_GNT#3	Low = A16 swap override enabled High = Default

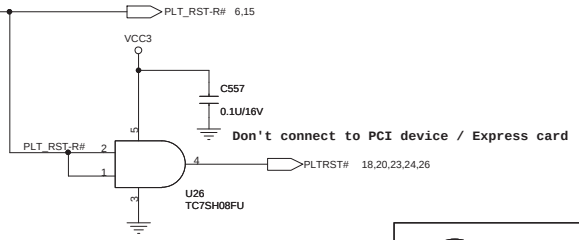
GNT3# R291 *1K

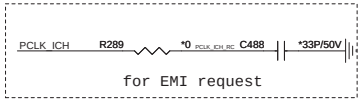
ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R296 *1K
GNT0# R290 *1K

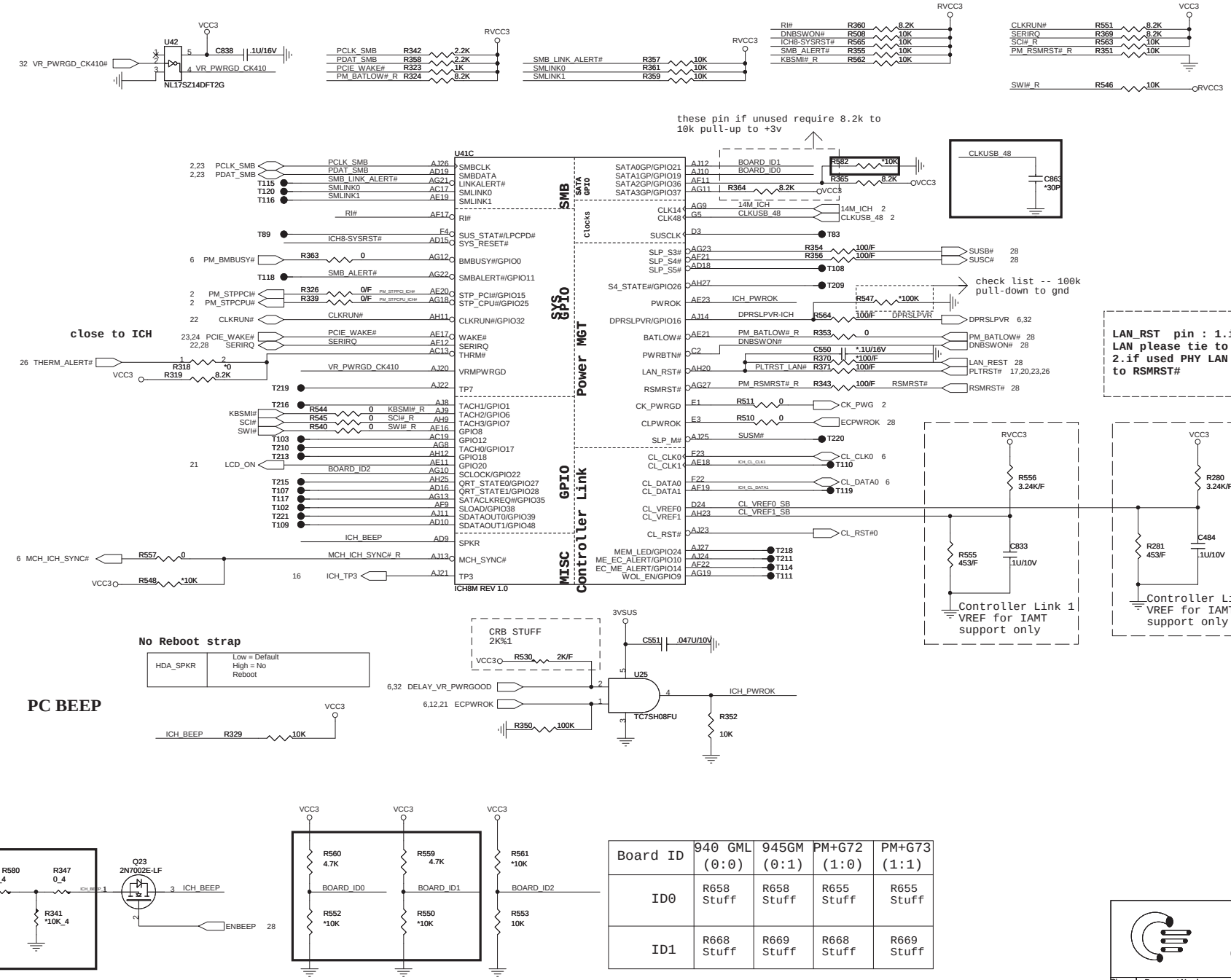




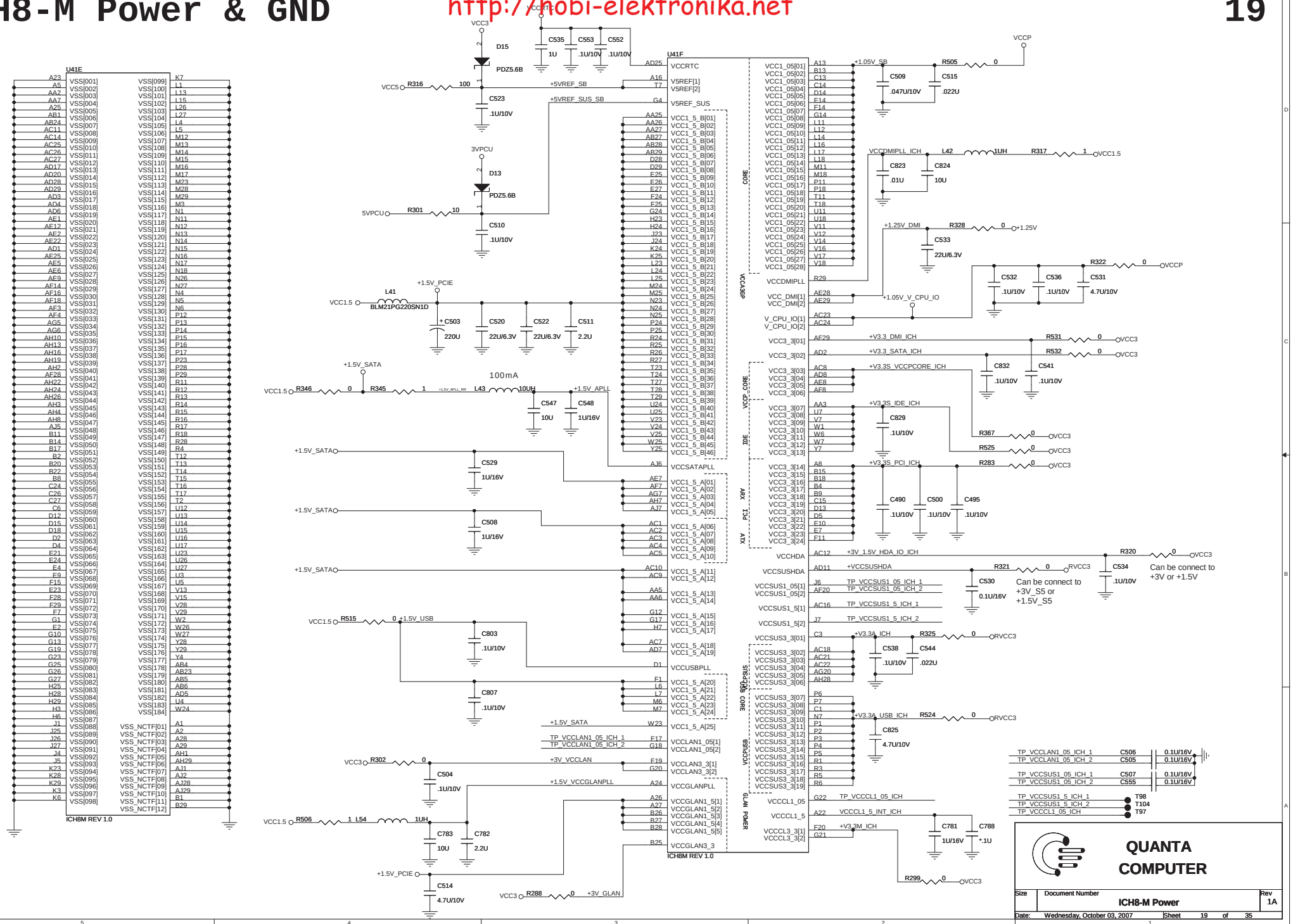


QUANTA COMPUTER

Size	Document Number	Rev
	ICH8-M PCIE, USB, DMI, PCI	1A
Date: Wednesday, October 03, 2007	Sheet 17 of 35	

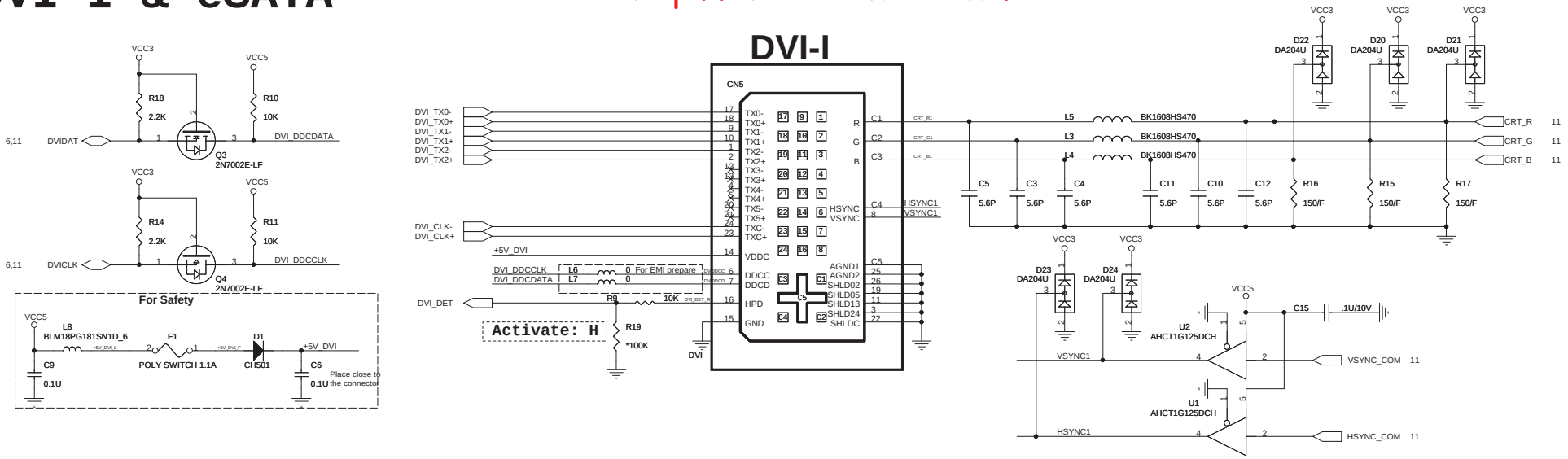


ICH8-M Power & GND

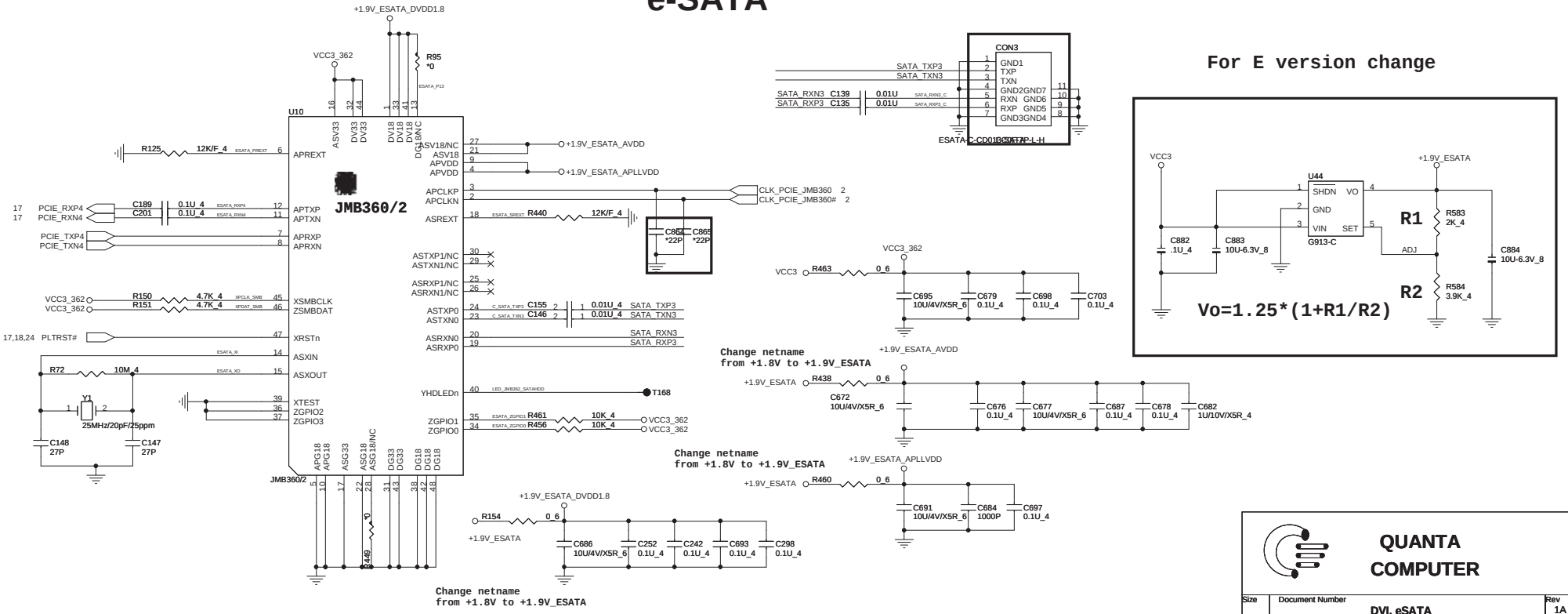


DVI-I & eSATA

DVI-I

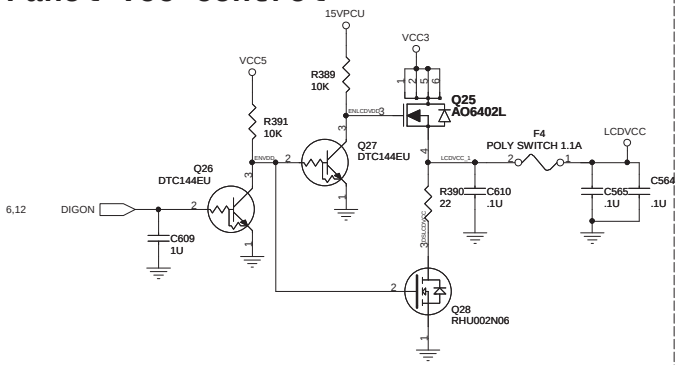


e-SATA

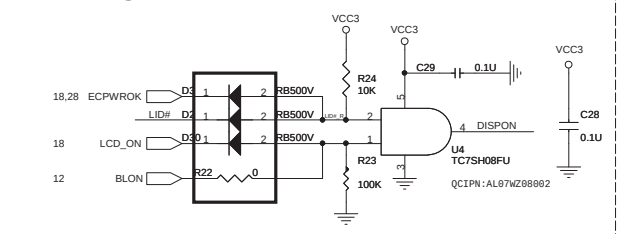


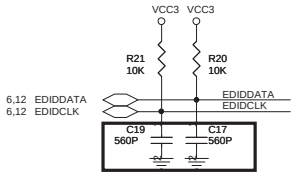
LCD Connector & HDMI Connector

Panel VCC Control

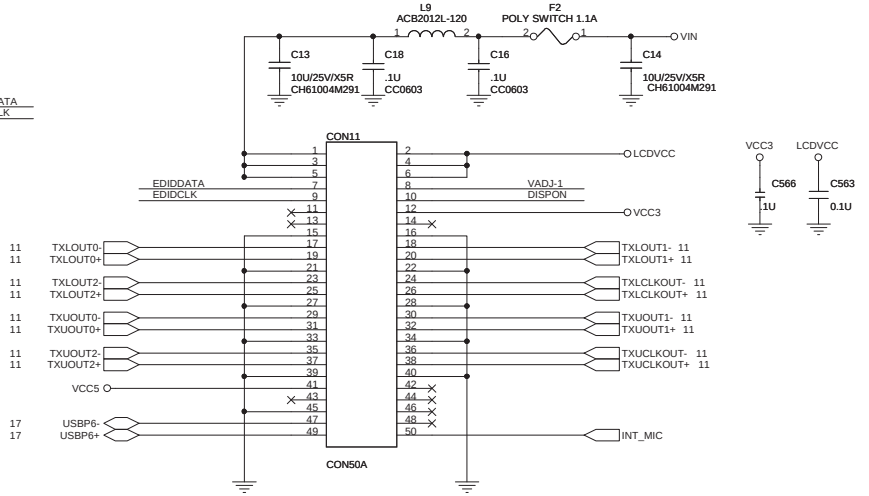


Backlight Control

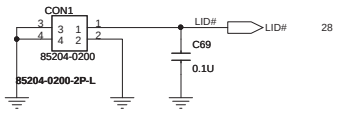


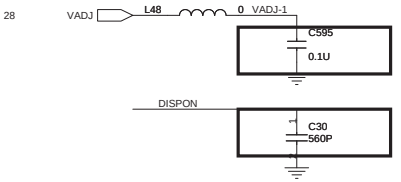


LCD Connector



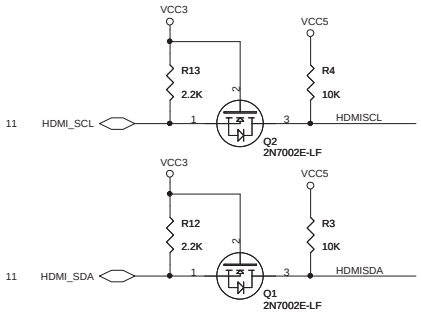
Lid

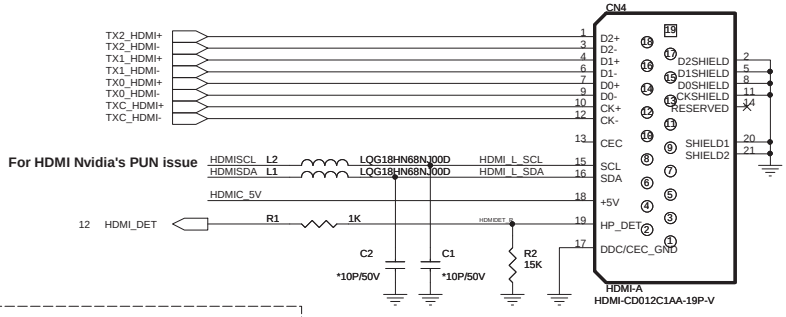


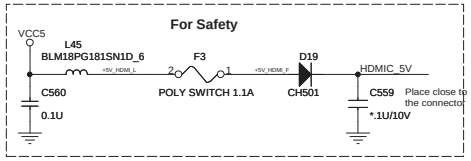


HDMI

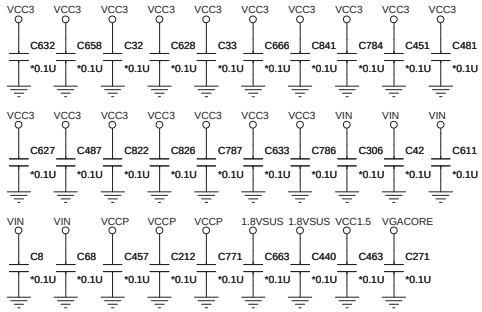
HDMI I2C pull-high to 5V







EMI Reserve



QUANTA COMPUTER

Size	Document Number	Rev
	LCD, HDMI	1A
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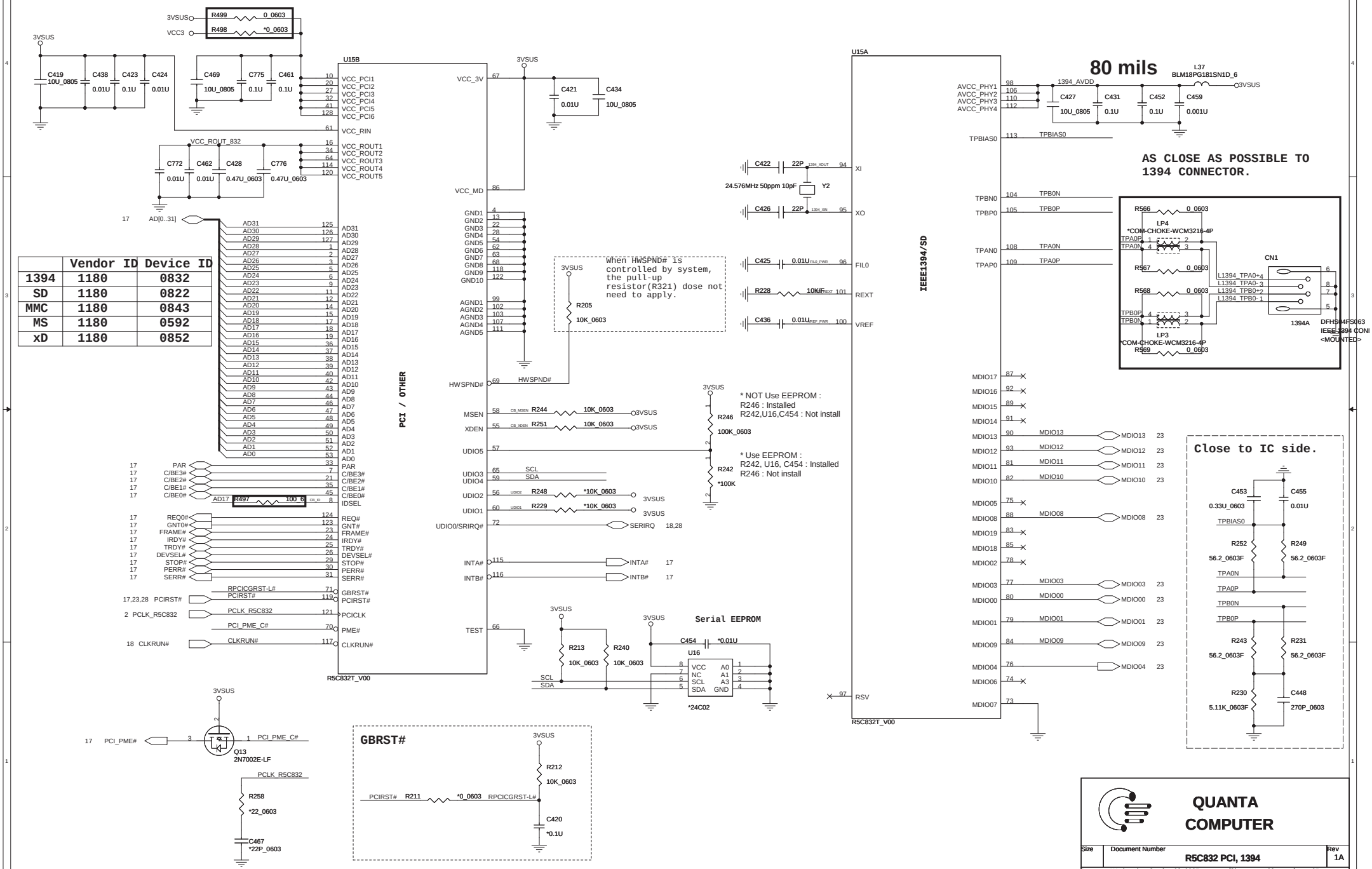

	Vendor ID	Device ID
1394	1180	0832
SD	1180	0822
MMC	1180	0843
MS	1180	0592
xD	1180	0852

QUANTA COMPUTER

Size	Document Number	Rev
	R5C832 PCI, 1394	1A
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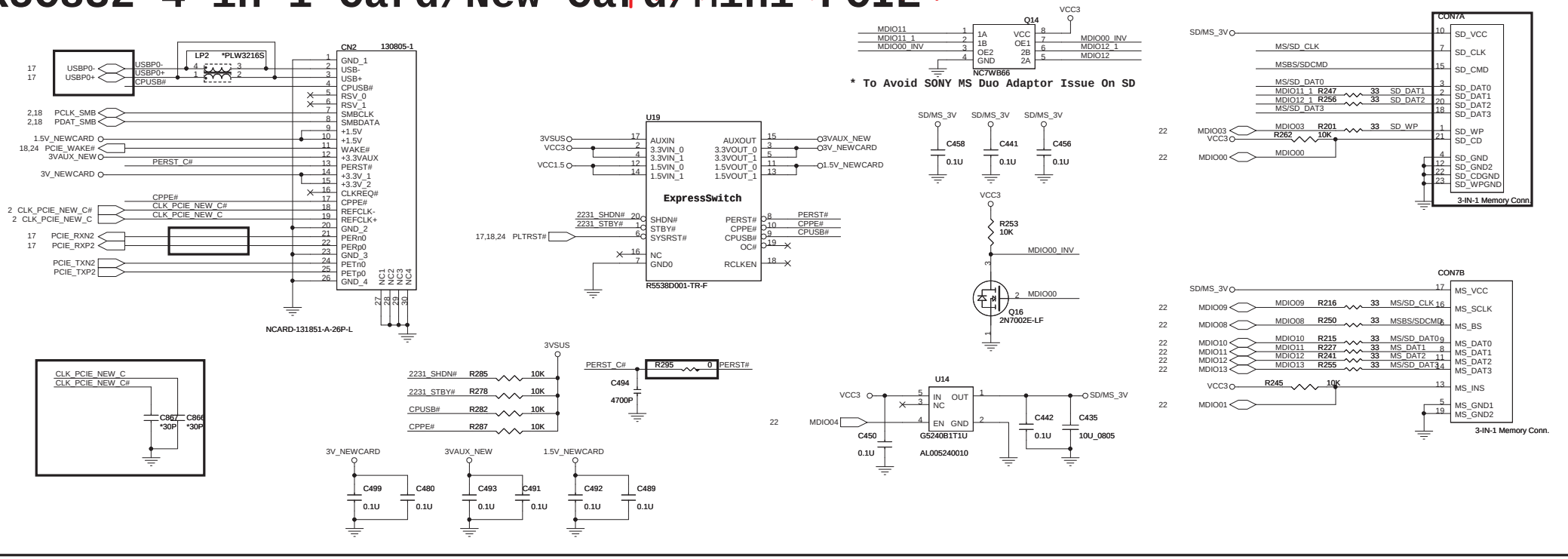
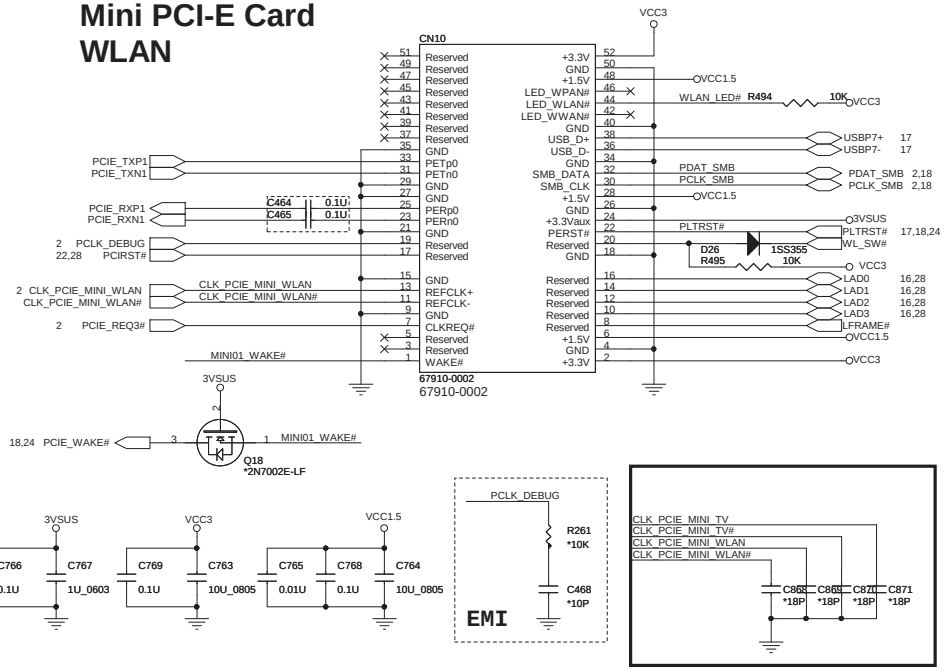
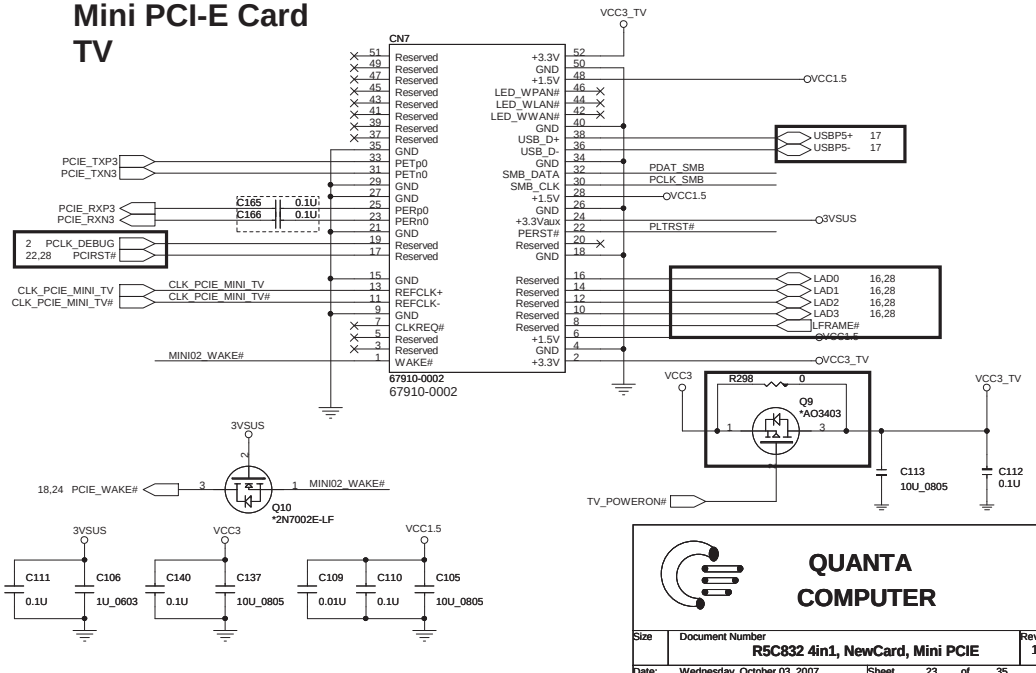
R5C832-4 in 1 Card/New Card/Mini PCIE



Mini PCI-E Card WLAN

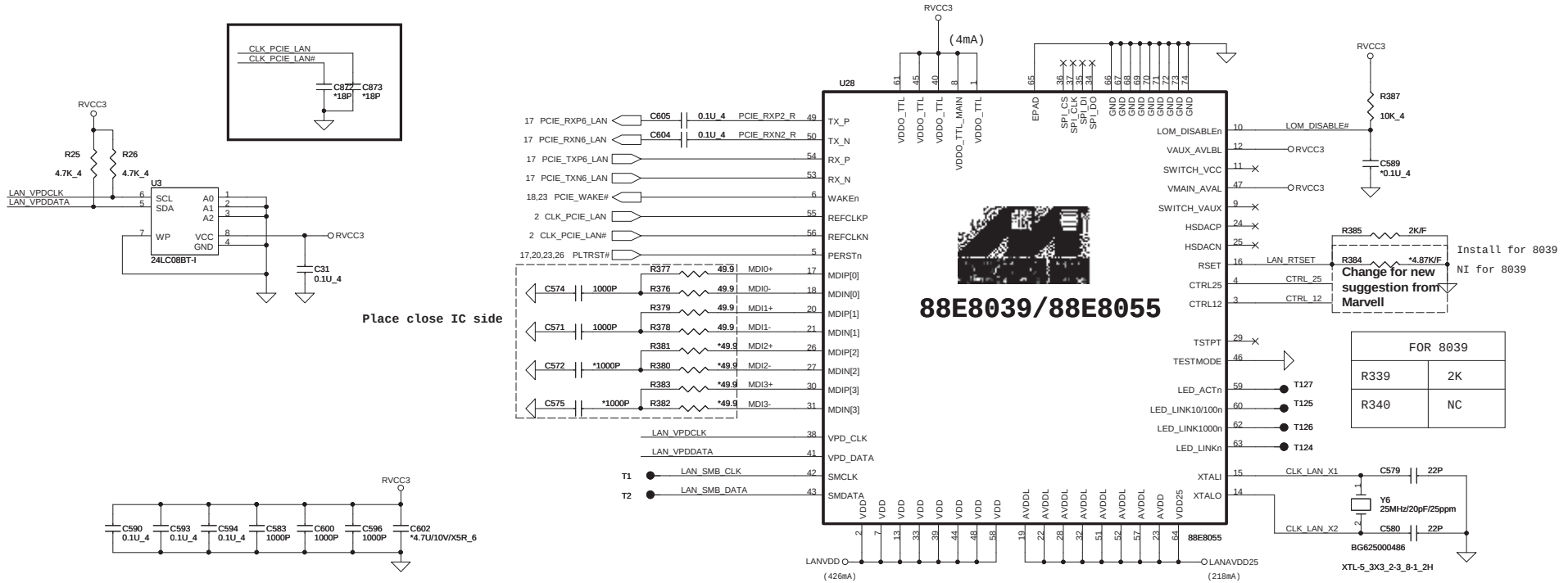


Mini PCI-E Card TV



QUANTA COMPUTER

Size	Document Number	Rev
	R5C832 4in1, NewCard, Mini PCIE	1A
Date: Wednesday, October 03, 2007	Sheet 23 of 35	



Giga: P/N: AJ080550002
10/100M: P/N: AJ080390005

FCE P/N:BG625000C03
P/N:BG625000486

1G -- FCE NS892402P DB0ZH1LAN06
10/100 -- FCE NS892404 DBED2LLAN05

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Size	Document Number	Rev
	Marvell 10/100, Gigabit LAN	1A
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Codec Conexant & Amp.

VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

Near To Codec

Please put a 0ohm resistor under Codec.
Follow the Codec layout guideline
(For ESD solution)

Analog Ground
Codec
Digital Ground

(MUTE: EAPD=L)

Spray the briger on the gap of A/DGND uniformly.

Port-A, Port-B, depend on layout routing easy or not to change port function.

External Mic.

Normal Open Type

H.P AMPLIFIER

MAX4411
QFN20-4X4-5-25P

Int. Speaker Amplifier

High pass filter

MAX9710ETP
QFN20-5X5-65-26P

SPEAKER CON.

Modem B/B CONN.

MAX8863

2nd low pass filter(338HZ)

Cutoff:770Hz

Cutoff:8.8Hz

Mixer & 1nd low pass filter(338HZ)

5V 2A

MAX9711

QUANTA COMPUTER			
Size	Document Number		Rev
	Audio Codec Conexant 20549		1A
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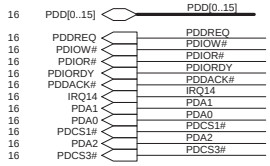
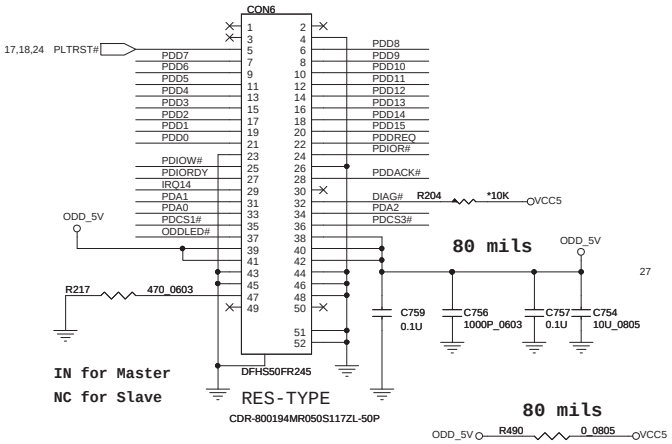
SATA HDD, ODD, Thermal, BT, FP, TP, FAN

ODD

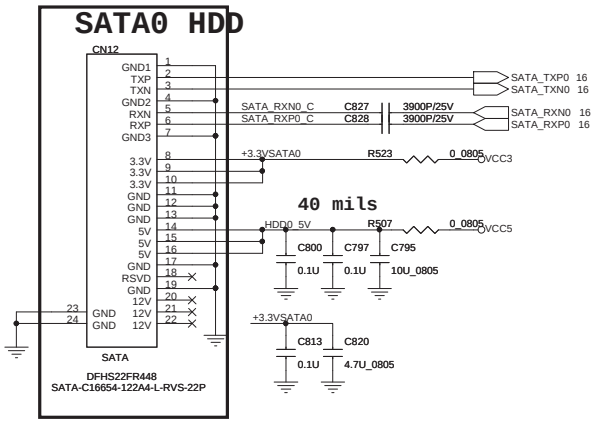


CD-ROM CONNECTOR

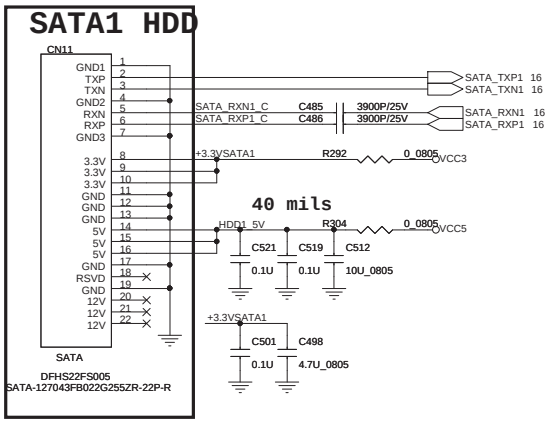
SMT TYPE CNN

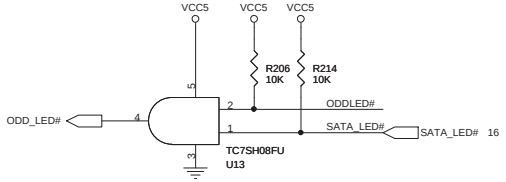


SATA0 HDD

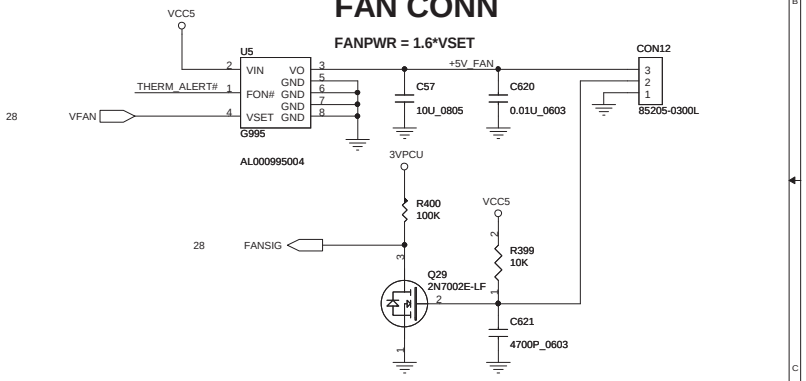


SATA1 HDD



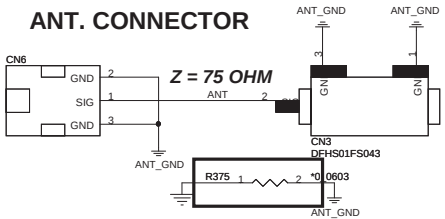


FAN CONN

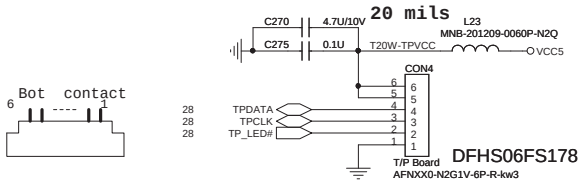


Layout rotate 180 degree

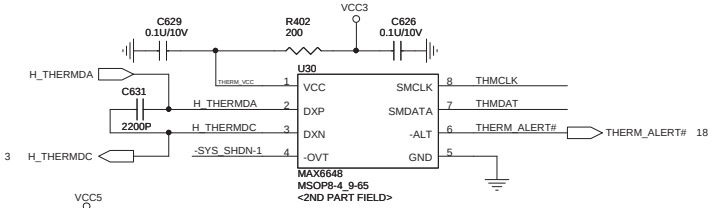
ANT. CONNECTOR



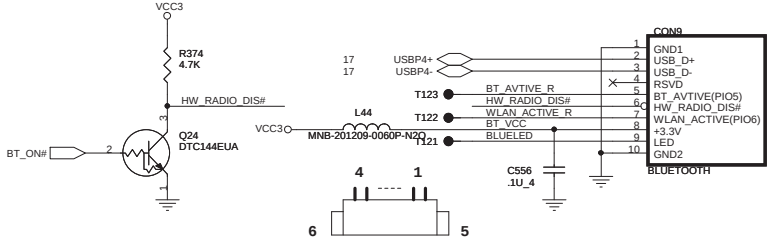
TOUCH PAD

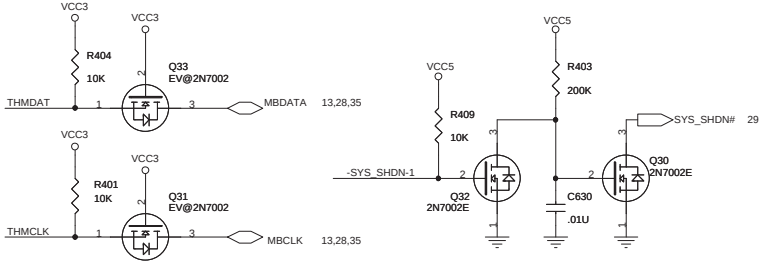


Thermal Senser



BT Connector





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Size	Document Number	Rev
	SATA, ODD, Thermal, BT, FP, TP, FAN	1A
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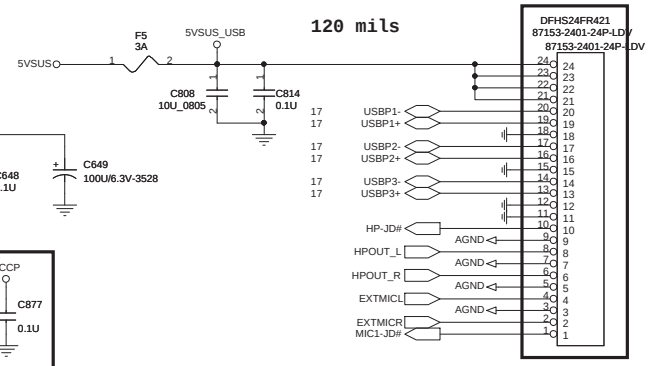
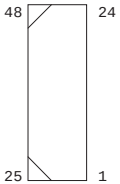
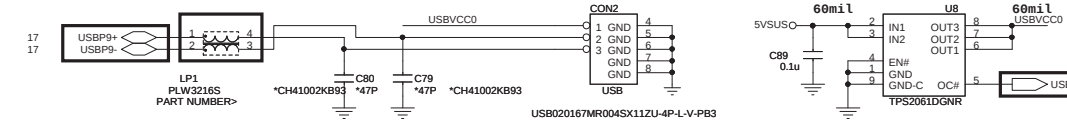
Int. Keyboard, USB, CIR, SW/B

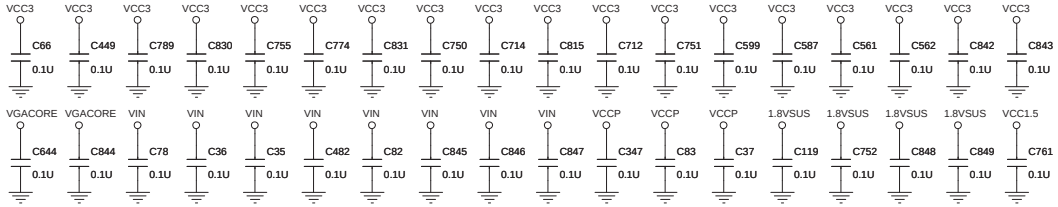
USB Right

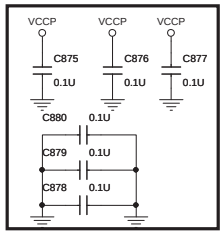




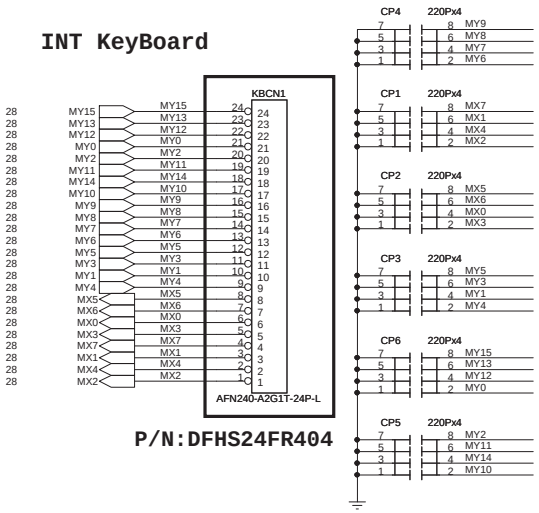
USB Left

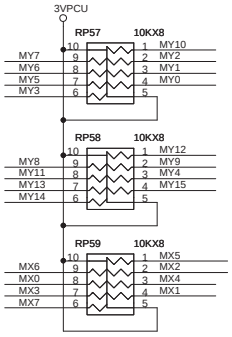




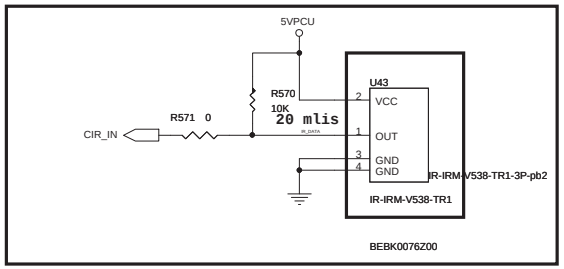


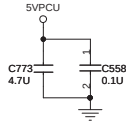
INT KeyBoard



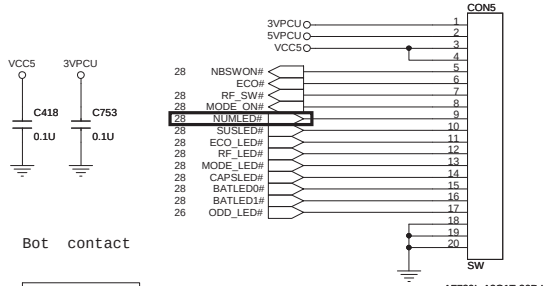


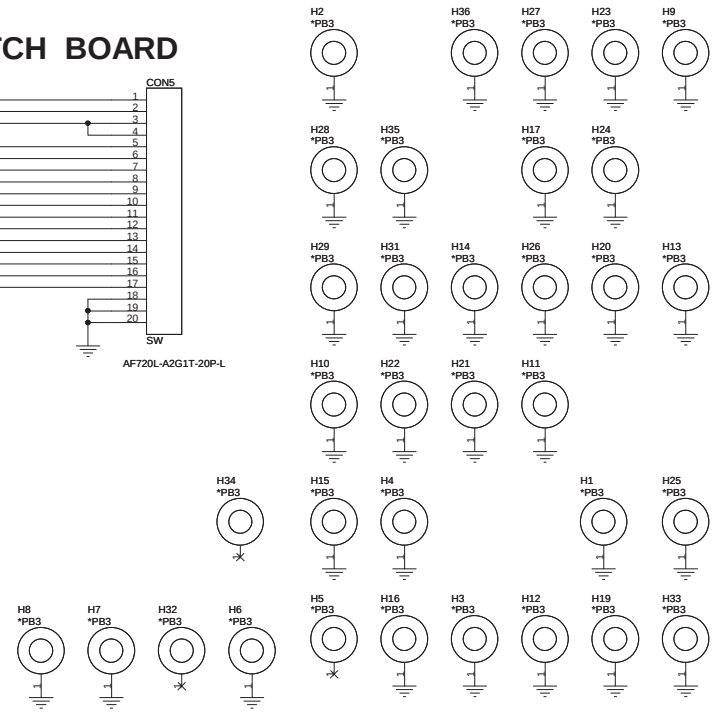
CIR





SWITCH BOARD





QUANTA COMPUTER

Size	Document Number	Rev
	Keyboard, USB, CIR, SW	1A
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IT8512

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

(For PLL Power)

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

8Mbit (1M Byte), SPI

SST_SST25VF016B

Model ID

MID
2 1
0 0: PB3C 865GM
0 1: PB3 NB8P-SE

Size	Document Number		Rev
	EC-ITE8512		1A
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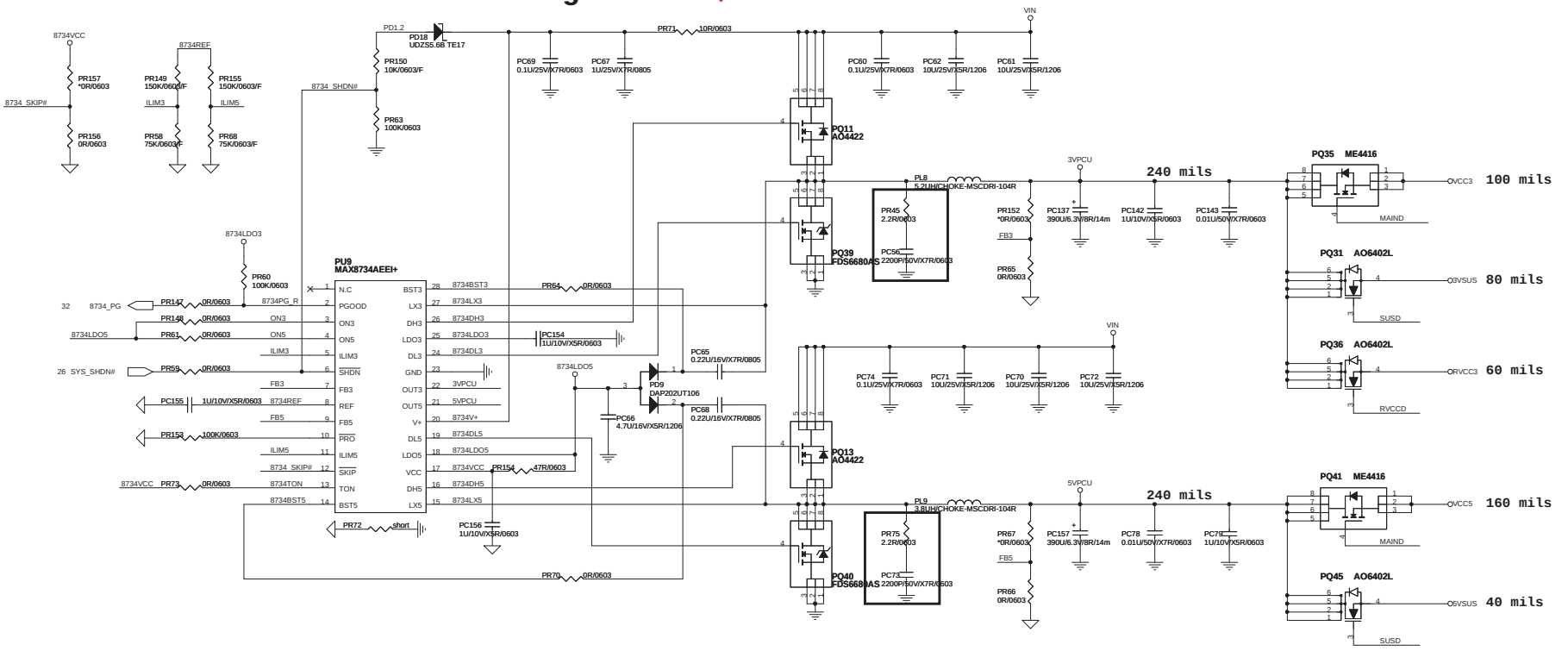
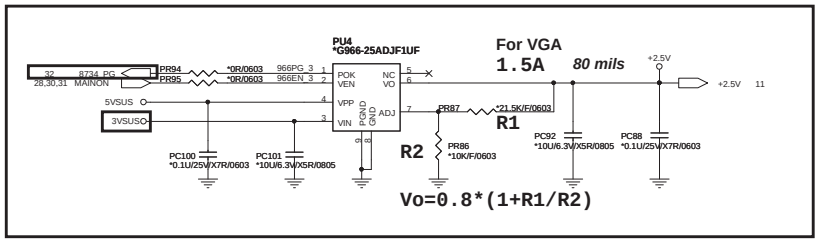
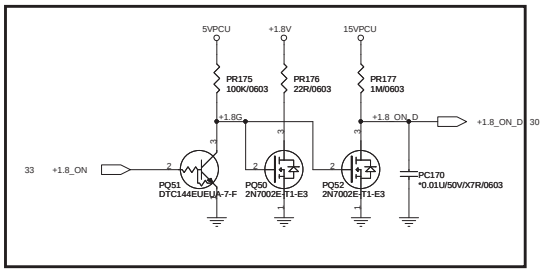
QUANTA COMPUTER

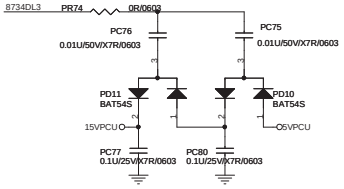
3VPCU& 5VPCU& VCC2.5& Discharge

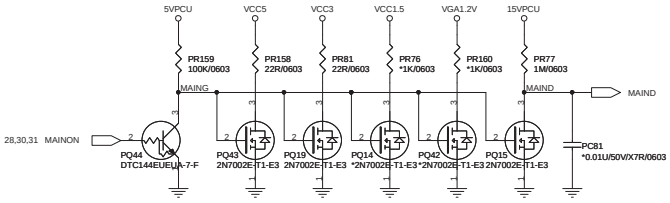


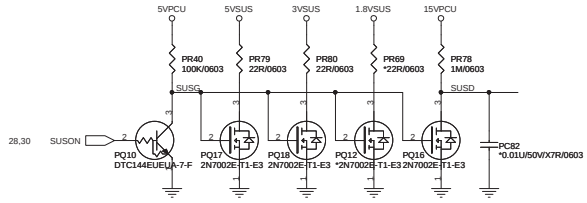
For E version change

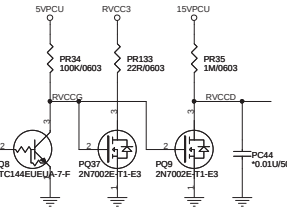












QUANTA COMPUTER

Size	Document Number	Rev
	3VPCU, 5VPCU	1A
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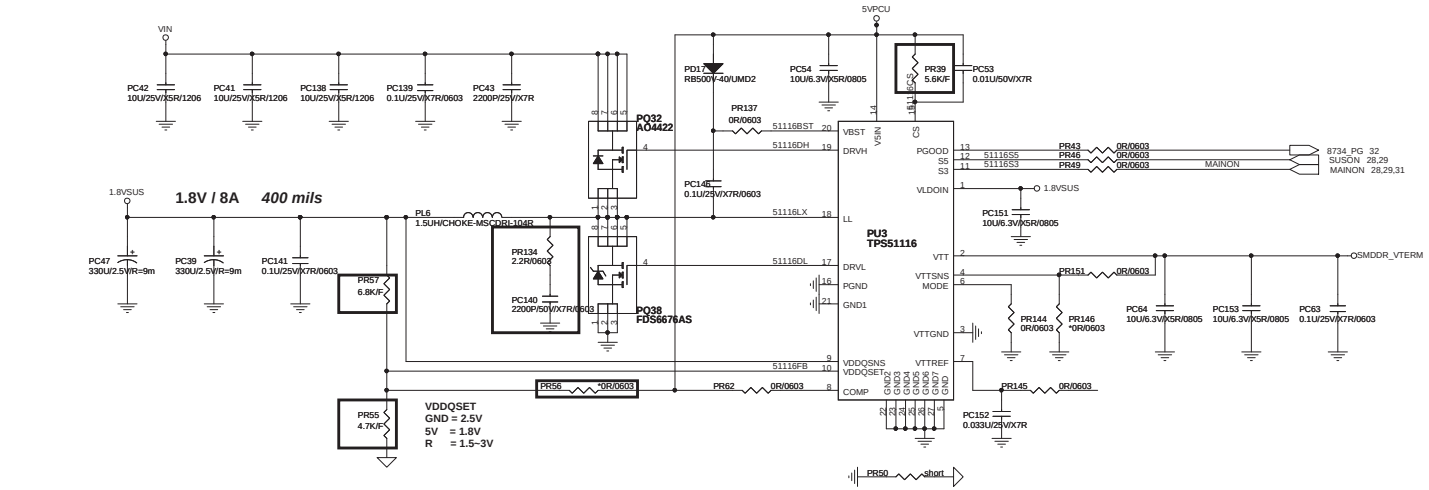

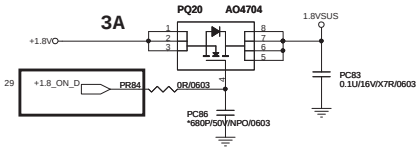

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Size	Document Number	Rev
	1.8VSUS, SMDDR_VTERM	1A

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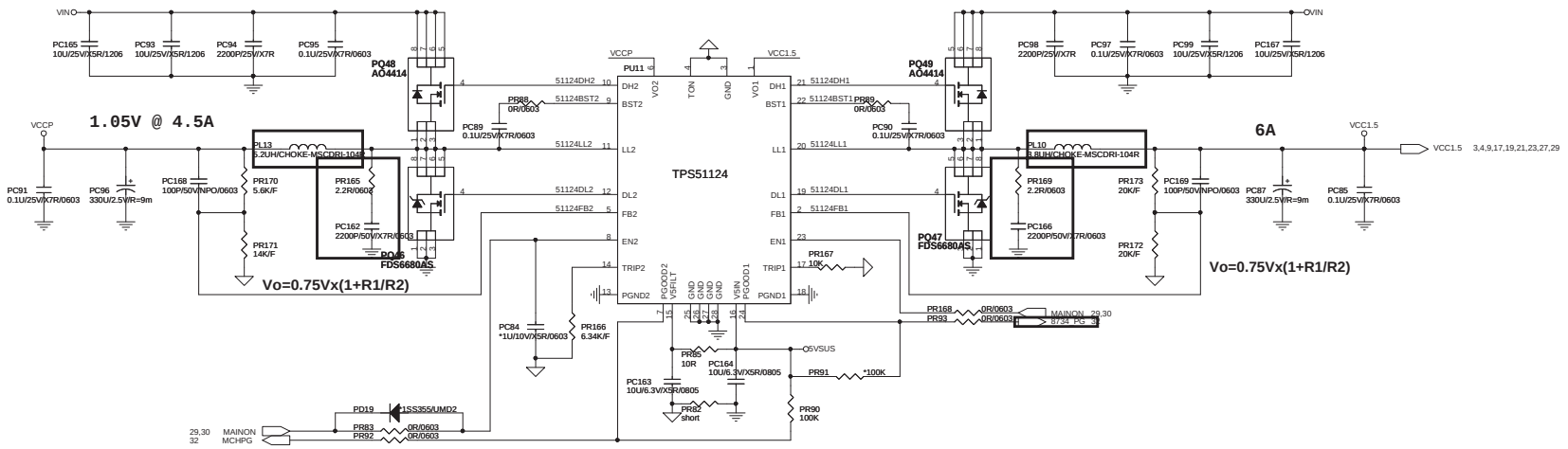
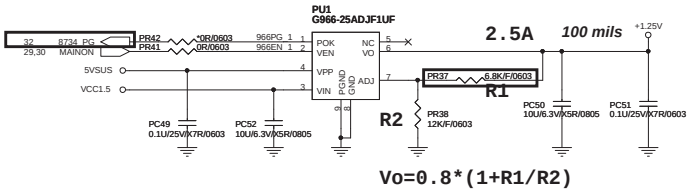
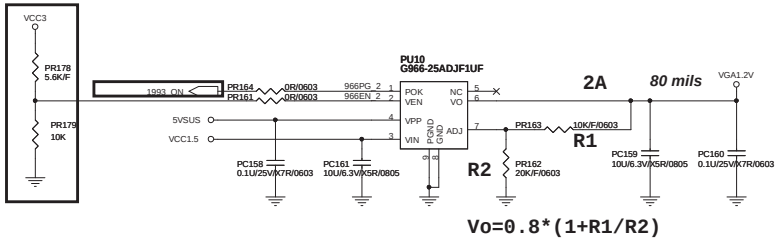
VCCP&VCC1.5V&VCC1.25&VGA1.2

2,3,4,5,8,9,16,19,21,27 VCCP
3,4,9,17,19,21,23,27,29 VCC1.5
6,9,19 +1.25V
11,13,29 VGA1.2V







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	VCCP/VCC1.5	1A

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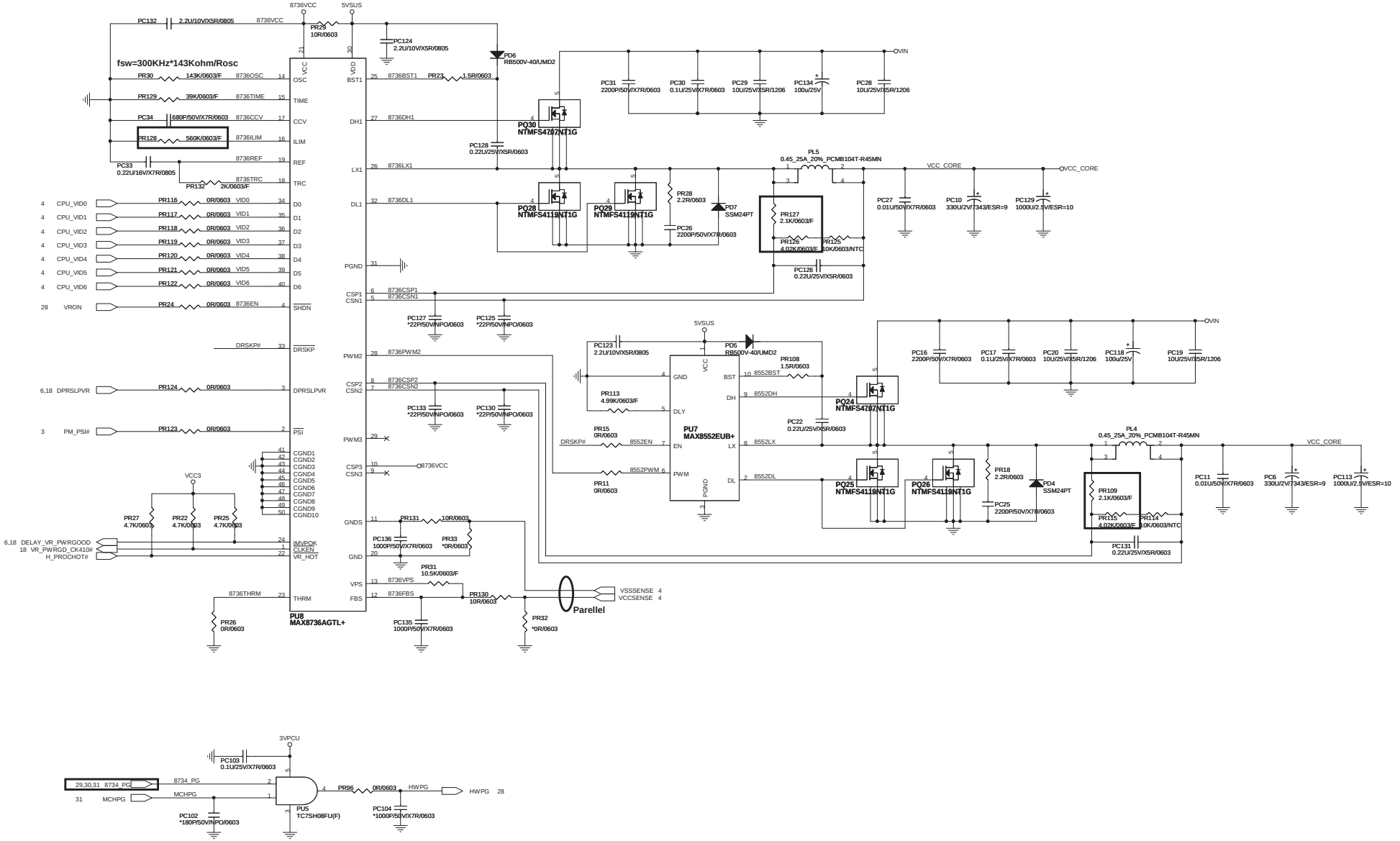
dV_Target/dt=12.5mV/us*71.5kohm/R_TIME
R_ILIM(PK)=8V*R_TRC/I(PK)LIMIT*Rsense



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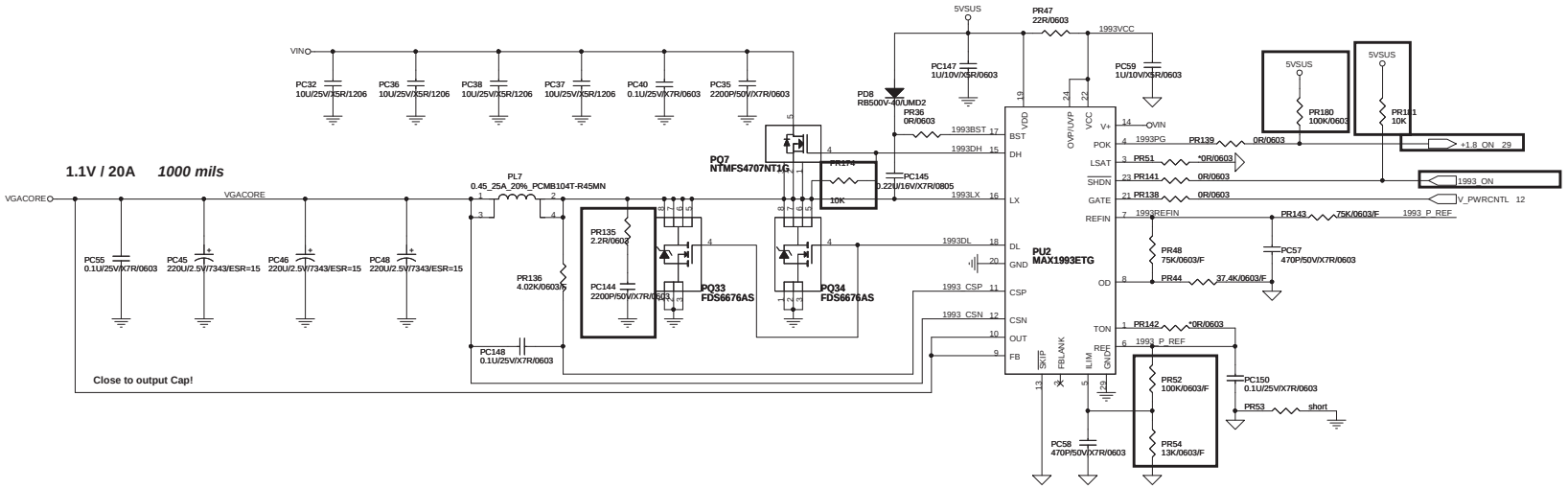
Size	Document Number		Rev
	CPU Core		1A
Date: Wednesday, October 03, 2007		Sheet 32 of 35	



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Size	Document Number	Rev
	VGA Core	1A

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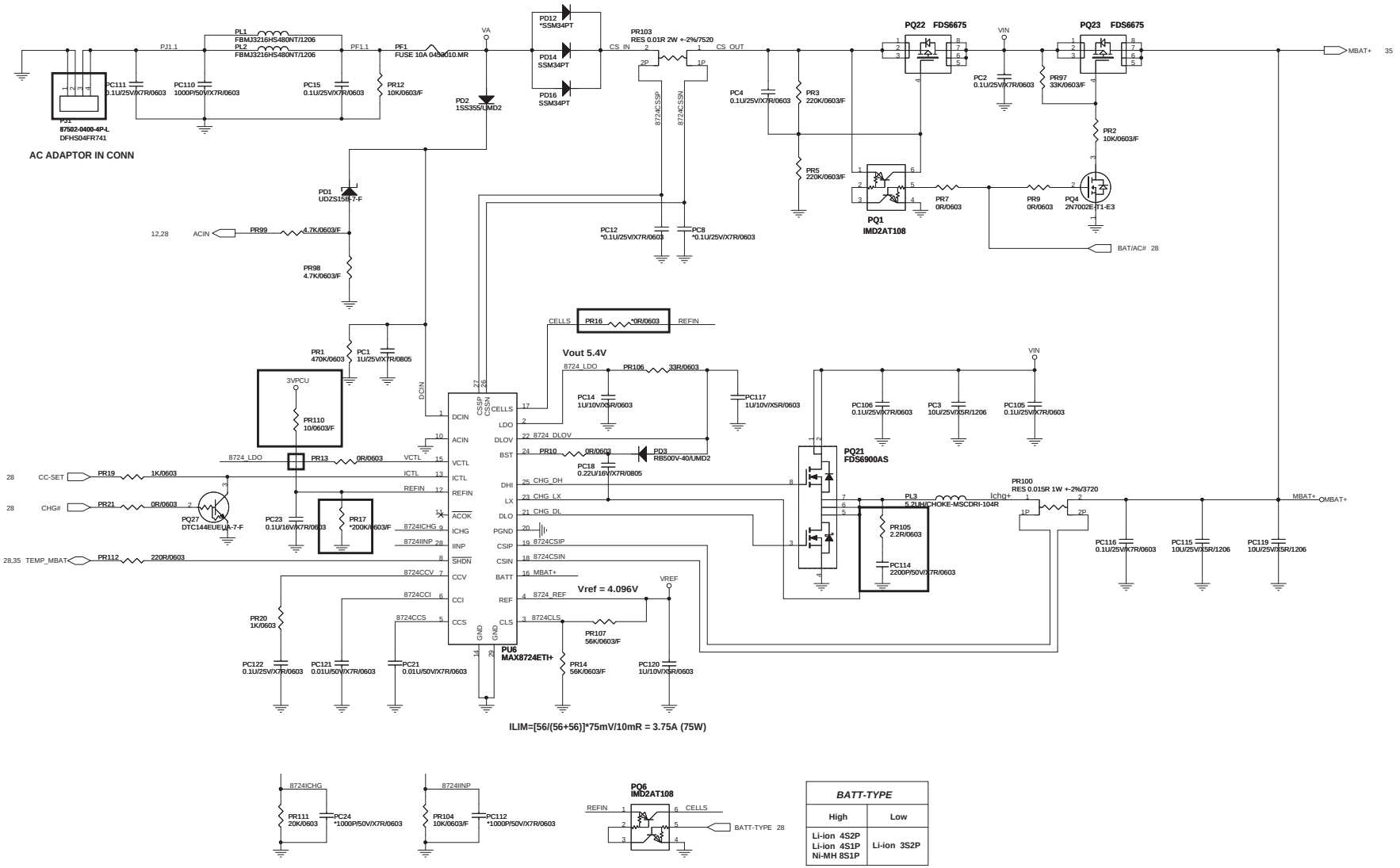
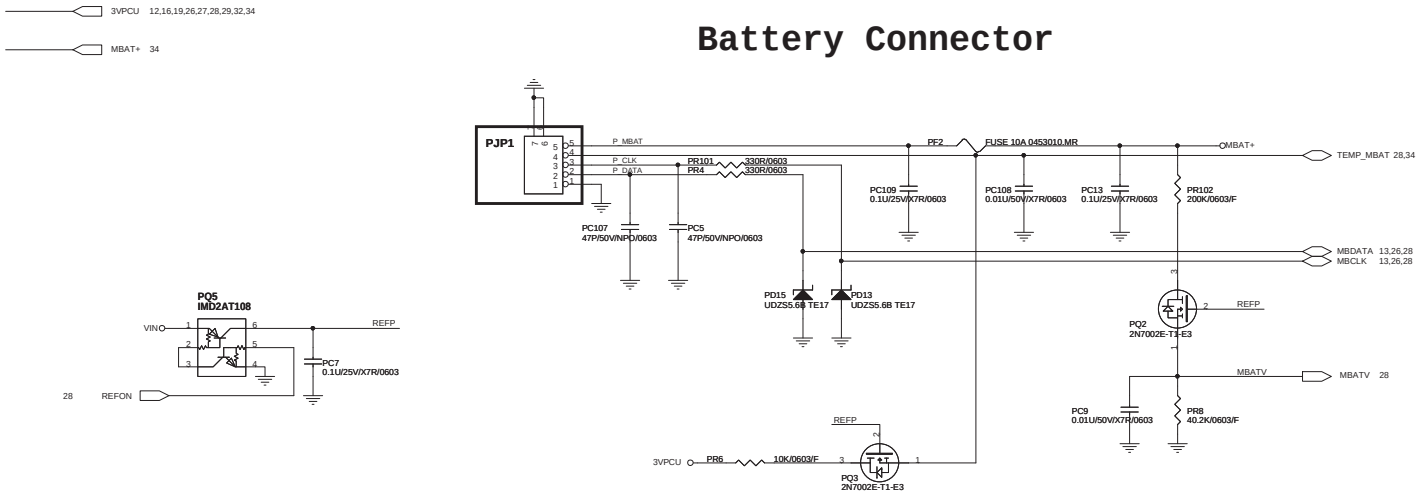


Battery Connector



TEMP_MBAT voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

MBATV voltage :	
Li-ion 4S*P	16.8V*40.2/(200+40.2)= 2.812V 12.0V*40.2/(200+40.2)= 2.008V
Ni-MH 8S1P	8.0V*40.2/(200+40.2)= 1.34V

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Size	Document Number	Rev
	Battery Connector	1A

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