UM9 UMA SYSTEM DIAGRAM

+3V/+5V PG.42
+1.8V PG.44
CPU Core PG.45
+1.05_PCH PG.48
+1.5V/+0.75V PG.43
+1.05VTT PG.44
UMA VGACORE PG.49
Charger PG.41

14.318MHz
CLOCK GEN
SLG8SP585VTR PG.2

SODIMM1 Max. 4GB PG.13
SODIMM2 Max. 4GB PG.14
DDR3 Channel A
DDR3 Channel B
1066MHz

INTEL Arrandale
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.3~6

FDI
DMI

PI3VDP411LSZDE PG.28
HDMI
HDMI PG.28
CRT
CRT board PG.39
LVDS
LVDS PG.22

FAN & THERMAL
GMT G990/
EMC1422-1-AIZL-TR PG.37

INTEL PCH
Ibex Peak-m
27mm X 25mm
1071pin FCBGA
TDP 5W
PG.7~11

SATA0
HDD PG.35
SATA1
ODD PG.35

WWAN
USB 2.0
PORT5

PCI-E x 1
LANE6
LANE1

LAN
Atheros/AR8152
10/100

WLAN
USB 2.0
PORT4

SATA port 4
DB board P39
eSATA
Combo port

DB Board
USB2.0 Ports X2 PG.39
Webcam PG.21
CRT Board
USB2.0 Ports X2 PG.39
USB 2.0
PORT0,1
PORT11
PORT2,3
PORT12
PORT8
Card Reader
RTS5138 PG.24
BT
BT365 PG.32

Stackup
TOP
GND
IN1
IN2
VCC
BOT

LPC
KBC
ITE 8502 PG.29
KB PG.34
TP PG.34
4M ROM PG.30

Azalia
AUDIO CODEC
ALC269Q-GR PG.26
Speaker PG.26
HP/MIC PG.27
Analog MIC PG.39
DB Board

SUBWOOFER
MAX9759 PG.27

Quanta Computer Inc.
PROJECT : UM9 UMA
Size | Document Number: BLOCK DIAGRAM | Rev 1A
Date: Wednesday, January 27, 2010 | Sheet 1 of 51

PDC (Power Cap quantities follow UM3)

25mA

+1.05V_PCH — L10 HCB1608KF-181T15_6 — +VDDIO_CLK

C171	0.1U/ 10V
C263	0.1U/ 10V
C176	10U/6.3V_8

Place each 0.1uF cap close to pin

300mA

+3.3V_RUN — L9 HCB1608KF-181T15_6 — +VDDSE_CLK

C165	10U/6.3V_8
C168	0.1U/ 10V
C163	0.1U/ 10V
C164	0.1U/ 10V
C175	0.1U/ 10V
C174	0.1U/ 10V

Place each 0.1uF cap close to pin

U10

CK505
QFN32

+VDDSE_CLK	1	VDD_USB	
	5	VDD_LCD	
	17	VDD_SRC	
	24	VDD_CPU	
	29	VDD_REF	
+VDDIO_CLK	15	VDD_SRC_IO	
	18	VDD_CPU_IO	
	9	VSS_SATA	
	2	VSS_USB	
	8	VSS_LCD	
	12	VSS_SRC	
	21	VSS_CPU	
	26	VSS_REF	
+3.3V_RUN — R218 10K/J_4 — CK_PWRGD_R	16	CPU_STOP#	
	25	CK_PWRGD/PD#_3.3	
(8) CLK_PCH_14M — CLK_PCH_14M — C275 *10P/50V_4_NC — R222 33/J_4 CPU_SEL	30	REF_0/CPU_SEL	
XTAL_OUT	27	XOUT	
XTAL_IN	28	XIN	
(29,37) SMBDAT2	31	SDATA	
(29,37) SMBCLK2	32	SCLK	
	23	CPU-0	CLK_BUF_BCLKP (8)
	22	CPU-0#	CLK_BUF_BCLKN (8)
	20	CPU-1	
	19	CPU-1#	
	3	DOT96T_LPR	CLK_BUF_DREFCLKP (8)
	4	DOT96C_LPR	CLK_BUF_DREFCLKN (8)
	13	SRC-1	CLK_BUF_PCIE_3GPLLP (8)
	14	SRC-1#	CLK_BUF_PCIE_3GPLLN (8)
	10	SATA	CLK_BUF_DREFSSCLKP (8)
	11	SATA#	CLK_BUF_DREFSSCLKN (8)
	6	27MHz_nonSS	
	7	27MHz_SS	
	33	GND	

SLG8SP585VTR

Place R8044 within 0.5" of C/G

+3.3V_RUN — R225 *10K/J_4_NC — CPU_SEL — R224 10K/J_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

+3.3V_RUN — R216 1K/J_4 — CK_PWRGD_R

(45) VR_PWRGD_CLKEN# — 2N7002W-7-F Q19 — R221 *100K/J_4_NC

C265 50 *100P_NC

Y4 14.318MHZ

XTAL_IN — C274 33P/50V_4

XTAL_OUT — C272 33P/50V_4

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number: Clock Gen(ICS9LRS3197AKLFT)	Rev 1A
Date: Monday, February 01, 2010	Sheet 2 of 51	

DPLL_REF_SSCLK:Embedded Display Port PLL Differential Clock In. If no eDP, do we need implement these R?

	DIS	SG
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

03

U11A

DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS

IC,AUB_CFD_rPGA,R1P0

U11B

MISC
THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

CPU THERMTRIP

JTAG MAPPING

Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

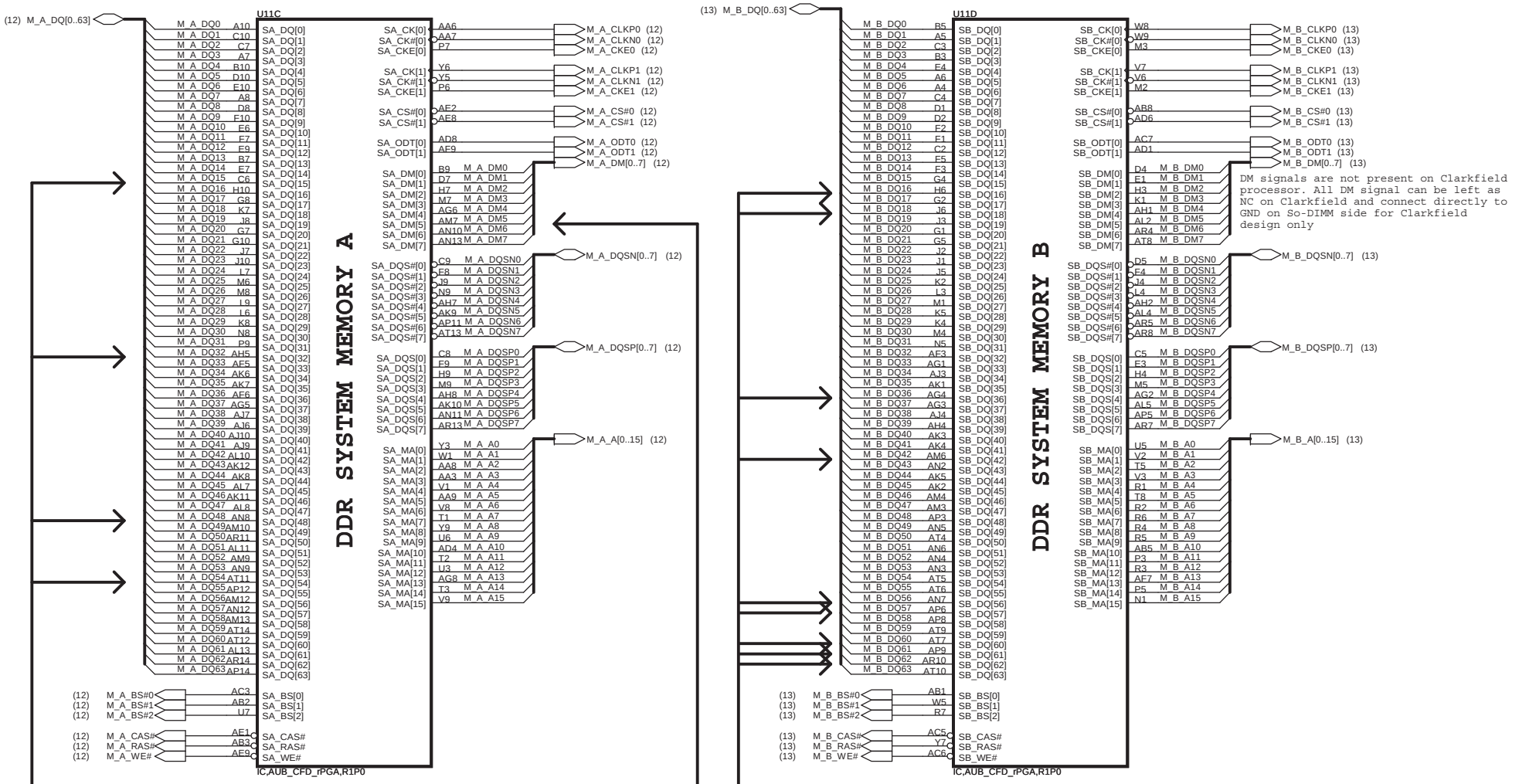
Intel Suggest to reserve 0 ohm below for CPU AP29 and AR29 pins.

Use a voltage divider with VDDQ (1.5 V) rail ON in S3) and resistor combination of 1.5K ±1% (to VDDQ)/750±1% (to GND) to convert to processor VTT level.

Quanta Computer Inc.
PROJECT : UM9 UMA

Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	1A
Date: Monday, February 01, 2010	Sheet 3 of 51	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number: PROCESSER 2/4(DDR)	Rev: 1A
Date: Monday, February 01, 2010	Sheet 4 of 51	

18A

Name different with power

+VCC_CORE

C324 *22U/6.3V_8_NC
C334 *22U/6.3V_8_NC
C330 *22U/6.3V_8_NC
C329 *22U/6.3V_8_NC
C41 *22U/6.3V_8_NC
C40 22U/6.3V_8
C325 22U/6.3V_8
C316 22U/6.3V_8
C333 22U/6.3V_8
C54 22U/6.3V_8
C42 22U/6.3V_8
C336 22U/6.3V_8
C328 *10U/6.3V_8_NC
C32 *10U/6.3V_8_NC
C31 *10U/6.3V_8_NC
C323 *10U/6.3V_8_NC
C53 10U/6.3V_8
C39 10U/6.3V_8
C49 10U/6.3V_8
C30 10U/6.3V_8
C28 10U/6.3V_8
C339 10U/6.3V_8
C317 10U/6.3V_8
C331 10U/6.3V_8
C322 10U/6.3V_8
C55 10U/6.3V_8
C335 10U/6.3V_8
C33 10U/6.3V_8

C29 *470U_NC
C23 *470U_NC

Follow UM3

U11F

CPU CORE SUPPLY

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

IC,AUB_CFD_rPGA,R1P0

POWER

1.1V RAIL POWER

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

+1.05V_VTT

C313 10U/6.3V_8
C311 10U/6.3V_8
C319 10U/6.3V_8
C304 10U/6.3V_8
C44 *10U/6.3V_0805_NC
C315 *10U/6.3V_0805_NC
C45 *10U/6.3V_0805_NC
C62 *10U/6.3V_0805_NC
C65 *10U/6.3V_0805_NC
C309 22U/6.3V_8
C68 22U/6.3V_8
C312 *22U/6.3V_8_NC

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

+1.05V_VTT

C64 22U/6.3V_8
C66 22U/6.3V_8

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

CPU VIDS

PSI# → H_PSI# (45)

VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6] PROC_DPRSLPVR

→ VID0 (45) VID1 (45) VID2 (45) VID3 (45) VID4 (45) VID5 (45) VID6 (45) DPRSLPVR (45)

VTT_SELECT → TP17

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

SENSE LINES

ISENSE → I_MON (45)

VTT_SENSE → VTT_SENSE (44)
VSS_SENSE_VTT → TP16

R281 100/F_4 +VCC_CORE
R280 100/F_4

VCC_SENSE → VCCSENSE (45)
VSS_SENSE → VSSSENSE (45)

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

+VCC_GFX_CORE

C43 10U/6.3V_8
C50 10U/6.3V_8

C314 330U/2V_7343
C318 22U/6.3V_8
C321 22U/6.3V_8

U11G

GRAPHICS

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

SENSE LINES

VAXG_SENSE → VCC_AXG_SENSE (49)
VSSAXG_SENSE → VSS_AXG_SENSE (49)

GRAPHICS VIDs

GFX_VID[0] GFX_VID[1] GFX_VID[2] GFX_VID[3] GFX_VID[4] GFX_VID[5] GFX_VID[6]

→ GFXVR_VID_0 (49) GFXVR_VID_1 (49) GFXVR_VID_2 (49) GFXVR_VID_3 (49) GFXVR_VID_4 (49) GFXVR_VID_5 (49) GFXVR_VID_6 (49)

R258 4.7K/F_4

GFX_VR_EN → GFXVR_EN (49)
GFX_DPRSLPVR
GFX_IMON → GFXVR_IMON (49)

R10 *1K/F_4_NC

2A

POWER

DDR3 - 1.5V RAILS

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

+1.5V_SUS

C71 1U/6.3V
C70 1U/6.3V
C69 1U/6.3V
C72 1U/6.3V
C75 1U/6.3V
C76 22U/6.3V_8
C74 22U/6.3V_8
C77 330U/2V_7343

FDI

+1.05V_VTT

C67 22U/6.3V_8
C52 22U/6.3V_8

VTT1_45 VTT1_46 VTT1_47

PEG & DMI

+1.05V_VTT

C305 22U/6.3V_8
C306 22U/6.3V_8
C307 22U/6.3V_8
C63 *22U/6.3V_8_NC

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

1.1V

VTT0_59 VTT0_60 VTT0_61 VTT0_62 VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68

+1.05V_VTT

C310 10U/6.3V_8
C308 *10U/6.3V_0805_NC
C51 22U/6.3V_8
C320 *22U/6.3V_8_NC

1.8V

VCCPLL1 VCCPLL2 VCCPLL3

+1.8V_RUN

C38 22U/6.3V_8
C37 4.7U/6.3V
C327 2.2U/ 6.3V
C36 1U/6.3V
C326 1U/6.3V

IC,AUB_CFD_rPGA,R1P0

VID0 VID1 VID2 VID3 VID4 VID5 VID6 DPRSLPVR H_PSI#

R282 R271 R284 R273 R283 R272 R285 R274 R288 R277 R289 R279 R286 R275 R287 R276 R270 R268 1K/J_4 *1K/J_4_NC

+1.05V_VTT

C341 *100P_NC

50

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

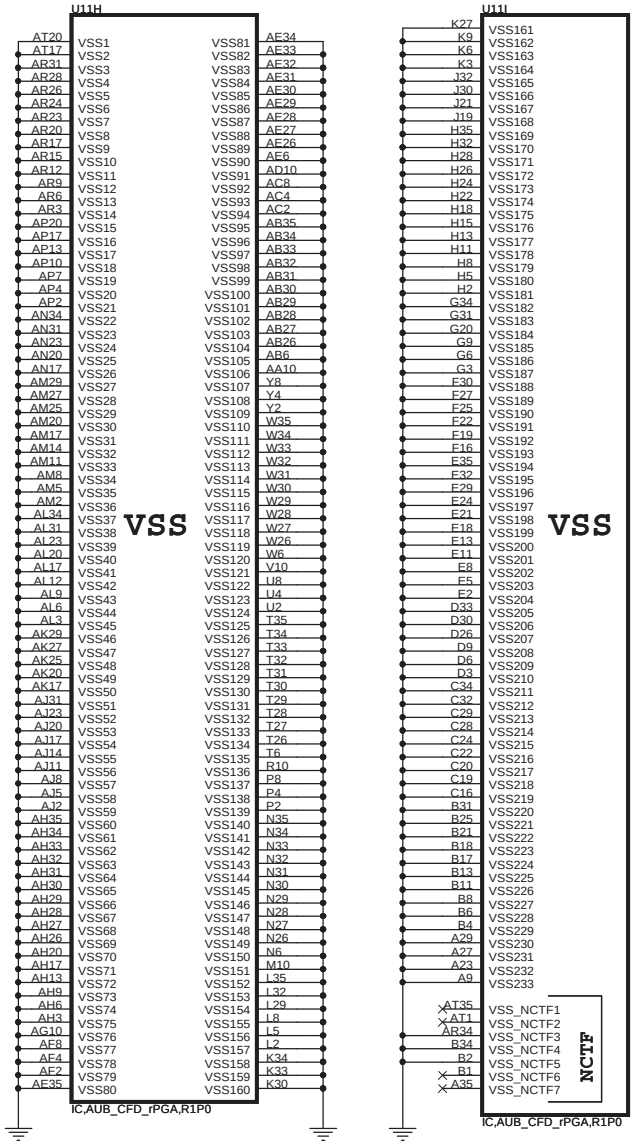
C397 close to R8361

Quanta Computer Inc.

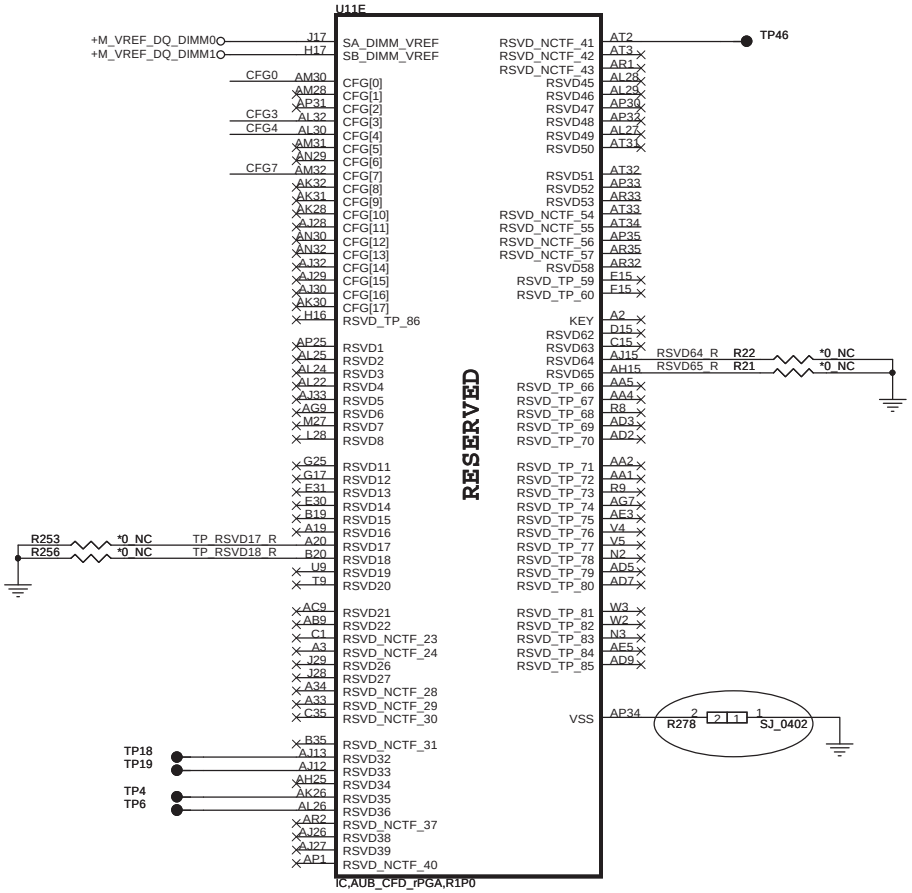
PROJECT : UM9 UMA

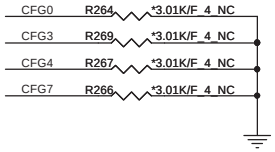
Size	Document Number	Rev
	PROCESSER 3/4(POWER)	1A
Date: Monday, February 01, 2010	Sheet 5 of 51	

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only

CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

Quanta Computer Inc.
PROJECT : UM9 UMA

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

Date: Wednesday, January 27, 2010 Sheet 6 of 51

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U9A

Ibex-M 1 OF 10

RTC
LPC
IHDA
JTAG
SATA
SPI

HDD
ODD
ESATA

DG: Place TX cap close to connector

SATA port 2/3 are not support in HM55 .
They are only in PM 55

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

must add test point.

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

iTPM ENABLE/DISABLE

From UM3

TPM Function	
Enable	Mount
Disable	NC (Default)

Close to VGA side

UMA:CRT 55ohm, UMA CRT display ripple issue.

UMA CRT,LVDS&HDMI signals
IBEX PEAK-M (LVDS,DDI)

U9D

Ibex-M 4 OF 10

SDVO
Digital Display Interface
DISPLAY PORT B
DISPLAY PORT C
DISPLAY PORT D
LVDS--A
LVDS--B
CRT

R8337 (IREF), UMA:0.5% ,DIS:5%
Sch check list 2.0 use 5% R

For UMA HDMI Function

Q14 2N7002K-T1-E3

For AUDIO

No Reboot strap.

SPKR	Low = Default. High = No Reboot.

RTC 1mA

FM9, UM3 use 1%

Res. of TDI near PCH

JTAG_TDI, JTAG_TMS, TRST# Internal 20K PU.
JTAG_TCK Internal 20K PD

From UM3

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

NC all Res. when PCH is production stage.

Res. of RST#
PCH ES1 stage : pop
PCH ES2 stage : NC

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	1A
Date: Monday, February 01, 2010	Sheet 7 of 51	

IBEX PEAK-M (GND)

U9I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	U30
BE46	VSS[203]	VSS[303]	U31
BE48	VSS[204]	VSS[304]	U32
BE50	VSS[205]	VSS[305]	U34
BE6	VSS[206]	VSS[306]	P38
BE8	VSS[207]	VSS[307]	V11
BF3	VSS[208]	VSS[308]	P16
BF49	VSS[209]	VSS[309]	V19
BF51	VSS[210]	VSS[310]	V20
BG18	VSS[211]	VSS[311]	V22
BG24	VSS[212]	VSS[312]	V30
BG4	VSS[213]	VSS[313]	V31
BG50	VSS[214]	VSS[314]	V32
BH11	VSS[215]	VSS[315]	V34
BH15	VSS[216]	VSS[316]	V35
BH19	VSS[217]	VSS[317]	V38
BH23	VSS[218]	VSS[318]	V43
BH31	VSS[219]	VSS[319]	V45
BH35	VSS[220]	VSS[320]	V46
BH39	VSS[221]	VSS[321]	V47
BH43	VSS[222]	VSS[322]	V49
BH47	VSS[223]	VSS[323]	V5
BH7	VSS[224]	VSS[324]	V7
C12	VSS[225]	VSS[325]	V8
C50	VSS[226]	VSS[326]	W2
D51	VSS[227]	VSS[327]	W52
E12	VSS[228]	VSS[328]	Y11
E16	VSS[229]	VSS[329]	Y12
E20	VSS[230]	VSS[330]	Y15
E24	VSS[231]	VSS[331]	Y19
E30	VSS[232]	VSS[332]	Y23
E34	VSS[233]	VSS[333]	Y28
E38	VSS[234]	VSS[334]	Y30
E42	VSS[235]	VSS[335]	Y31
E46	VSS[236]	VSS[336]	Y32
E48	VSS[237]	VSS[337]	Y38
E6	VSS[238]	VSS[338]	Y43
E8	VSS[239]	VSS[339]	Y46
F49	VSS[240]	VSS[340]	P49
F5	VSS[241]	VSS[341]	Y5
G10	VSS[242]	VSS[342]	Y6
G14	VSS[243]	VSS[343]	Y8
G18	VSS[244]	VSS[344]	P24
G2	VSS[245]	VSS[345]	T43
G22	VSS[246]	VSS[346]	AD51
G32	VSS[247]	VSS[347]	AT8
G36	VSS[248]	VSS[348]	AD47
G40	VSS[249]	VSS[349]	Y47
G44	VSS[250]	VSS[350]	AT12
G52	VSS[251]	VSS[351]	AM6
AF39	VSS[252]	VSS[352]	AT13
H16	VSS[253]	VSS[353]	AM5
H20	VSS[254]	VSS[354]	AK45
H30	VSS[255]	VSS[355]	AK39
H34	VSS[256]	VSS[356]	AV14
H38	VSS[257]	VSS[366]	
H42	VSS[258]		

IbexPeak-M_Rev1_0

+3.3V_RUN

PCIE_CLK_REQ1# R208 10K
PCIE_CLK_REQ2# R199 10K

+3.3V_SUS

PCIE_CLK_REQ0# R127 10K
PCIE_CLK_REQ3# R176 10K
PCIE_CLK_REQ4# R131 10K
PCIE_CLK_REQB#_R R115 10K
PCIE_CLK_REQ5# R133 10K
PEG_CLKREQ# R180 10K

2N7002W-7-F
Q18

SMB_CLK_ME1 → SMBCLK1 (29)

+3.3V_SUS

Q17
2N7002W-7-F

SMB_DATA_ME1 → SMBDAT1 (29)

+3.3V_RUN

RP7
2.2KX2

Q15
2N7002W-7-F

(12,13,39) WLAN_SMBCLK → ICH_SMBCLK

+3.3V_RUN

Q16
2N7002W-7-F

(12,13,39) WLAN_SMBDATA → ICH_SMBDATA

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U9B

Ibex-M 2 OF 10

PCI-E*

[WWAN]

[WLAN]
(39) PCIE_RXN1 → PCIE_RXN1
(39) PCIE_RXP1 → PCIE_RXP1
(39) PCIE_TXN1 → C183 0.1U/10V → PCIE_TXN1_C
(39) PCIE_TXP1 → C182 0.1U/10V → PCIE_TXP1_C

[LAN]
(39) PCIE_RXN6_LAN → PCIE_RXN6_LAN
(39) PCIE_RXP6_LAN → PCIE_RXP6_LAN
(39) PCIE_TXN6_LAN → C154 0.1U/10V → PCIE_TXN6_LAN_C
(39) PCIE_TXP6_LAN → C160 0.1U/10V → PCIE_TXP6_LAN_C

PCIECLKRQ0#/GPIO73 Internal 20K PU

MiniWLAN
(39) CLK_PCIE_WLANN
(39) CLK_PCIE_WLANP
(39) PCIE_CLK_REQ1#

MiniWWAN

LAN
(39) CLK_PCIE_LANN
(39) CLK_PCIE_LANP
(39) PCIE_CLK_REQB#_R

SMBus
(+3V_S5) SMBALERT# / GPIO11
SMBCLK
SMBDATA
(+3V_S5) SML0ALERT# / GPIO60
SML0CLK
SML0DATA
(+3V_S5) SML1ALERT# / GPIO74
(+3V_S5) SML1CLK / GPIO58
(+3V_S5) SML1DATA / GPIO75

B9 SMBALERT# 10K/J_4 R175
H14 ICH_SMBCLK 2.2K/J_4 R150
C8 ICH_SMBDATA 2.2K/J_4 R147
J14 SMBL0ALERT# 10K/J_4 R146
C6 SMB_CLK_ME0 2.2K/J_4 R137
G8 SMB_DATA_ME0 2.2K/J_4 R138
M14 SML1ALERT# 10K/J_4 R125
F10 SMB_CLK_ME1 2.2K/J_4 R154
G12 SMB_DATA_ME1 2.2K/J_4 R153

+3.3V_SUS

Controller Link
CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9

PEG
(+3V_S5) PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P

H1 PEG_CLKREQ#
AD43
AD45
AN4 → CLK_PCIE_3GPLLN (3)
AN2 → CLK_PCIE_3GPLLP (3)

From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N → AT1 → CLK_DREFSSCLKN (3)
CLKOUT_DP_P / CLKOUT_BCLK1_P → AT3 → CLK_DREFSSCLKP (3)

CLKIN_DMI_N → AW24 → CLK_BUF_PCIE_3GPLLN (2)
CLKIN_DMI_P → BA24 → CLK_BUF_PCIE_3GPLLP (2)

CLKIN_BCLK_N → AP3 → CLK_BUF_BCLKN (2)
CLKIN_BCLK_P → AP1 → CLK_BUF_BCLKP (2)

CLKIN_DOT_96N → F18 → CLK_BUF_DREFCLKN (2)
CLKIN_DOT_96P → E18 → CLK_BUF_DREFCLKP (2)

CLKIN_SATA_N / CKSSCD_N → AH13 → CLK_BUF_DREFSSCLKN (2)
CLKIN_SATA_P / CKSSCD_P → AH12 → CLK_BUF_DREFSSCLKP (2)

REFCLK14IN → P41 → CLK_PCH_14M (2)
C214 *5.6P/50V_4_NC
CLKIN_PCILOOPBACK → J42 CLK_PCI_FB → CLK_PCI_FB (9)
T22

XTAL25_IN → AH51 XTAL25_IN
XTAL25_OUT → AH53 XTAL25_OUT
R223 *0_NC RC0402
Intel recommendation
XCLK_RCOMP → AF38 XCLK_RCOMP
R105 90.9/F_4 +1.05V_PCH

Clock Flex
(+3V) CLKOUTFLEX0 / GPIO64 → T45 CLK_FLEX0 → T19
(+3V) CLKOUTFLEX1 / GPIO65 → P43 CLK_FLEX1 → T20
(+3V) CLKOUTFLEX2 / GPIO66 → T42 CLK_FLEX2 → T17
(+3V) CLKOUTFLEX3 / GPIO67 → N50 CLK_FLEX3
R192 22/J_4 → CLK_48M_CARD (25)
C244 10P/50V_4

R502 1M/F_4
XTAL25_IN — Y5 — XTAL25_OUT
C271 27P 50 NPO
25MHz
C270 27P 50 NPO
For UMA

Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number: PCH 2/5 (PCIE, SMBUS, CK)	Rev 1A
Date: Monday, February 01, 2010	Sheet 8 of 51	

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)

U9E — Ibex-M 5 OF 10

U9C — Ibex-M 3 OF 10

PCI

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

C/BE0# C/BE1# C/BE2# C/BE3#

PIRQA# PIRQB# PIRQC# PIRQD#

REQ0# REQ1# / GPIO50 (+5V) REQ2# / GPIO52 (+5V) REQ3# / GPIO54 (+5V)

GNT0# GNT1# / GPIO51 (+3V) GNT2# / GPIO53 (+3V) GNT3# / GPIO55 (+3V)

PIRQE# / GPIO2 (+5V) PIRQF# / GPIO3 (+5V) PIRQG# / GPIO4 (+5V) PIRQH# / GPIO5 (+5V)

PCIRST# SERR# PERR# IRDY# PAR DEVSEL# FRAME# PLOCK# STOP# TRDY# PME# PLTRST#

CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

NVRAM

NV_CE#0 NV_CE#1 NV_CE#2 NV_CE#3

NV_DQS0 NV_DQS1

NV_DQ0 / NV_IO0 … NV_DQ15 / NV_IO15

NV_ALE NV_CLE

NV_RCOMP NV_RB#

NV_WR#0_RE# NV_WR#1_RE#

NV_WE#_CK0 NV_WE#_CK1

USB

USBP0N/P … USBP5N/P

USBP6N/P USBP7N/P USBP8N/P USBP9N/P USBP10N/P USBP11N/P USBP12N/P USBP13N/P

USBRBIAS# USBRBIAS

USB_OC0# … USB_OC7#

DMI

DMI0RXN DMI1RXN DMI2RXN DMI3RXN

DMI0RXP DMI1RXP DMI2RXP DMI3RXP

DMI0TXN DMI1TXN DMI2TXN DMI3TXN

DMI0TXP DMI1TXP DMI2TXP DMI3TXP

DMI_ZCOMP DMI_IRCOMP

FDI

FDI_RXN0 … FDI_RXN7

FDI_RXP0 … FDI_RXP7

FDI_INT FDI_FSYNC0 FDI_FSYNC1 FDI_LSYNC0 FDI_LSYNC1

FDI_TXN0 … FDI_TXN7

FDI_TXP0 … FDI_TXP7

System Power Management

SYS_RESET# SYS_PWROK PWROK MEPWROK LAN_RST# DRAMPWROK RSMRST# PWRBTN# RI# WAKE# PMSYNCH

SLP_S3# SLP_S4# SLP_M# TP23

(+3V_S5) SUS_PWR_DN_ACK / GPIO30

(+3V_S5) ACPRESENT / GPIO31

(+3V) CLKRUN# / GPIO32

(+3V_S5) SUS_STAT# / GPIO61

(+3V_S5) SUSCLK / GPIO62

(+3V_S5) SLP_S5# / GPIO63

(+3V_S5) BATLOW# / GPIO72

(+3V_S5) SLP_LAN# / GPIO29

BATLOW#/GPIO72 Internal 20K PU

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

NV_ALE R99 *1K_NC

NV_CLE R100 *1K_NC

Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable

Sch check list R2.0 :WAKE# use 10K

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend
(single & double load) on PDG v1.1

Reserve capacitor pads for improving WWAN.

C243 10P/50V_4 C245 10P/50V_4

Check

U8 *MC74VHC1G08DFT2G_NC C222 *0.1U/10V_NC

PLT_RST-R# PLTRST# (3,29,39)

R139 100K_4 R155 *100K_4_NC R149 SJ_0402

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	1A

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IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

U9F

Ibex-M
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GPIO MISC

CPU

RSVD

NCTF

PCH_GPIO0 Y3 BMBUSY# / GPIO0 (+3V)
(29) SIO_EXT_SMI# C38 TACH1 / GPIO1 (+3V)
(29) SIO_EXT_SCI# D37 TACH2 / GPIO6 (+3V)
(29) SIO_EXT_WAKE# J32 TACH3 / GPIO7 (+3V)
TP28 PCH_GPIO8 F10 GPIO8 (+3V_S5)
LAN_PHY_PWR_CTRL K9 LAN_PHY_PWR_CTRL / GPIO12 (+3V_S5)
(27) TEST_WOOFER_EN TEST_WOOFER_EN T7 GPIO15 (+3V_S5)
SATA4GP AA2 SATA4GP / GPIO16 (+3V)
(39) PCIE_MCARD1_DET# 1 R140 2 PCIE_MCARD1_DET# F38 TACH0 / GPIO17 (+3V)
SJ_0402
PCIE_MCARD2_DET#, If WWAN have issue check this
PCIE_MCARD2_DET# Y7 SCLOCK / GPIO22 (+3V)
R111 *10K_4_NC GPIO27 AB12 GPIO27 (+3V_S5)
GPIO27 reserve for internal VR.
TP_PCH_GPIO28 V13 GPIO28 (+3V_S5)
SATA2GP AB7 SATA2GP / GPIO36 (+3V)
SATA3GP AB13 SATA3GP / GPIO37 (+3V)
(32) BT_RADIO_DIS# BT_RADIO_DIS# P3 SDATAOUT0 / GPIO39 (+3V)
GPIO46 F1 PCIECLKRQ7# / GPIO46 (+3V_S5)
(39) WWAN_RADIO_DIS# WWAN_RADIO_DIS# AB6 SDATAOUT1 / GPIO48 (+3V)
(29) CRIT_TEMP_REP# CRIT_TEMP_REP# AA4 SATA5GP / GPIO49 (+3V)
GPIO24 register not cleared by CF9h reset event.
GPIO45 H10 GPIO24 (+3V_S5)
VGA_TYPE H3 PCIECLKRQ6# / GPIO45 (+3V_S5)
USB_MCARD2_DET# F8 GPIO57 (+3V_S5)
(39) USB_MCARD2_DET# GPIO35 M11 STP_PCI# / GPIO34 (+3V)
(39) WLAN_RADIO_DIS# WLAN_RADIO_DIS# V6 SATACLKREQ# / GPIO35 (+3V)
V3 SLOAD / GPIO38 (+3V)

CLKOUT_PCIE6N AH45
CLKOUT_PCIE6P AH46
CLKOUT_PCIE7N AF48
CLKOUT_PCIE7P AF47
A20GATE U2 → GATEA20 (29)
CLKOUT_BCLK0_N/CLKOUT_PCIE8N AM3 → CLK_CPU_BCLKN (3)
CLKOUT_BCLK0_P/CLKOUT_PCIE8P AM1 → CLK_CPU_BCLKP (3)
PECI BG10 → H_PECI (3)
RCIN# T1 → RCIN# (29)
PROCPWRGD BE10 → H_PWRGOOD (3)
THRMTRIP# BD10 PCH_THRMTRIP# R R97 56/J_4 → H_THERM (3)
+1.05V_VTT R98 56/J_4
C422 *100P_NC

TP1 BA22
TP2 AW22
TP3 BB22
TP4 AY45
TP5 AY46
TP6 AV43
TP7 AV45
TP8 AF13
TP9 M18
TP10 N18
TP11 AJ24
TP12 AK41
TP13 AK42
TP14 M32
TP15 N32
TP16 M30
TP17 N30
TP18 H12
TP19 AA23
NC_1 AB45
NC_2 AB38
NC_3 AB42
NC_4 AB41
NC_5 T39
INIT3_3V# P6
TP24 C10

A4 VSS_NCTF_1
A49 VSS_NCTF_2
A5 VSS_NCTF_3
A50 VSS_NCTF_4
A52 VSS_NCTF_5
A53 VSS_NCTF_6
B2 VSS_NCTF_7
B4 VSS_NCTF_8
B52 VSS_NCTF_9
B53 VSS_NCTF_10
BE1 VSS_NCTF_11
BE53 VSS_NCTF_12
BE1 VSS_NCTF_13
BF53 VSS_NCTF_14
BH1 VSS_NCTF_15
VSS_NCTF_16 BH2
VSS_NCTF_17 BH52
VSS_NCTF_18 BH53
VSS_NCTF_19 BJ1
VSS_NCTF_20 BJ2
VSS_NCTF_21 BJ4
VSS_NCTF_22 BJ49
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ50
VSS_NCTF_25 BJ52
VSS_NCTF_26 BJ53
VSS_NCTF_27 D1
VSS_NCTF_28 D2
VSS_NCTF_29 D53
VSS_NCTF_30 E1
VSS_NCTF_31 E53

ibexPeak-M_Rev1_0

U9H

VSS[0] AB16
VSS[1] AA19
VSS[2] AA20
VSS[3] AA22
VSS[4] AM19
VSS[5] AA24
VSS[6] AA26
VSS[7] AA28
VSS[8] AA30
VSS[9] AA31
VSS[10] AA32
VSS[11] AB11
VSS[12] AB15
VSS[13] AB23
VSS[14] AB30
VSS[15] AB31
VSS[16] AB32
VSS[17] AB39
VSS[18] AB43
VSS[19] AB47
VSS[20] AB5
VSS[21] AB8
VSS[22] AC2
VSS[23] AC52
VSS[24] AD11
VSS[25] AD12
VSS[26] AD16
VSS[27] AD23
VSS[28] AD30
VSS[29] AD31
VSS[30] AD32
VSS[31] AD34
VSS[32] AU22
VSS[33] AD42
VSS[34] AD46
VSS[35] AD49
VSS[36] AD7
VSS[37] AE2
VSS[38] AE4
VSS[39] AE12
VSS[40] Y13
VSS[41] AH49
VSS[42] AU4
VSS[43] AE35
VSS[44] AP13
VSS[45] AN34
VSS[46] AE45
VSS[47] AE46
VSS[48] AF49
VSS[49] AF5
VSS[50] AF8
VSS[51] AG2
VSS[52] AG52
VSS[53] AH11
VSS[54] AH15
VSS[55] AH16
VSS[56] AH24
VSS[57] AH32
VSS[58] AV18
VSS[59] AH43
VSS[60] AH47
VSS[61] AH7
VSS[62] AJ19
VSS[63] AJ2
VSS[64] AJ20
VSS[65] AJ22
VSS[66] AJ23
VSS[67] AJ26
VSS[68] AJ28
VSS[69] AJ32
VSS[70] AJ34
VSS[71] AT5
VSS[72] AJ4
VSS[73] AK12
VSS[74] AM41
VSS[75] AN19
VSS[76] AK26
VSS[77] AK22
VSS[78] AK23
VSS[79] AK28
VSS[80] AK30
VSS[81] AK31
VSS[82] AK32
VSS[83] AK34
VSS[84] AK35
VSS[85] AK38
VSS[86] AK43
VSS[87] AK46
VSS[88] AK49
VSS[89] AK5
VSS[90] AK8
VSS[91] AL2
VSS[92] AL52
VSS[93] AM11
VSS[94] BB44
VSS[95] AD24
VSS[96] AM20
VSS[97] AM22
VSS[98] AM24
VSS[99] AM26
VSS[100] AM28
VSS[101] BA42
VSS[102] AM30
VSS[103] AM31
VSS[104] AM32
VSS[105] AM34
VSS[106] AM35
VSS[107] AM38
VSS[108] AM39
VSS[109] AM42
VSS[110] AU20
VSS[111] AM46
VSS[112] AV22
VSS[113] AM49
VSS[114] AM7
VSS[115] AA50
VSS[116] BB10
VSS[117] AN32
VSS[118] AN50
VSS[119] AN52
VSS[120] AP12
VSS[121] AP42
VSS[122] AP46
VSS[123] AP49
VSS[124] AP5
VSS[125] AP8
VSS[126] AR2
VSS[127] AR52
VSS[128] AT11
VSS[129] BA12
VSS[130] AH48
VSS[131] AT32
VSS[132] AT36
VSS[133] AT41
VSS[134] AT47
VSS[135] AT7
VSS[136] AV12
VSS[137] AV16
VSS[138] AV20
VSS[139] AV24
VSS[140] AV30
VSS[141] AV34
VSS[142] AV38
VSS[143] AV42
VSS[144] AV46
VSS[145] AV49
VSS[146] AV5
VSS[147] AV8
VSS[148] AW14
VSS[149] AW18
VSS[150] AW2
VSS[151] BF9
VSS[152] AW32
VSS[153] AW36
VSS[154] AW40
VSS[155] AW52
VSS[156] AY11
VSS[157] AY43
VSS[158] AY47

ibexPeak-M_Rev1_0

+3.3V_RUN

RCIN# R206 10K_4
GATEA20 R205 10K_4
BT_RADIO_DIS# R200 10K_4
SATA2GP R110 10K_4
SATA3GP R108 10K_4
SATA4GP R214 10K_4
PCIE_MCARD1_DET# R R141 10K_4
PCIE_MCARD2_DET# R117 10K_4
SIO_EXT_SMI# R168 10K_4
SIO_EXT_SCI# R169 10K_4
SIO_EXT_WAKE# R120 10K_4
WLAN_RADIO_DIS# R210 10K_4
CRIT_TEMP_REP# R215 10K_4
USB_MCARD2_DET# R130 10K_4

+3.3V_SUS

TEST_WOOFER_EN R129 10K_4
PCH_GPIO8 R144 *10K_4_NC
TP_PCH_GPIO28 R112 10K_4
GPIO46 R178 10K_4
GPIO45 R179 10K_4
LAN_PHY_PWR_CTRL R132 10K_4

VGA Strap

+3.3V_SUS
Madison
R148 *10K_4_NC
VGA_TYPE
Park
R143 *10K_4_NC
Check ....

R124 10K_4 GPIO35

GPIO[7,6,1,17], PCIECLKRQ6#/GPIO45, GPIO28 Internal 20K PU

+3.3V_RUN
PCH_GPIO0 R212 10K_4
WWAN_RADIO_DIS# R114 10K_4

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up (8.2~ KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

WWAN_RADIO_DIS#	1-X High = Strong (Default)

Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled

(7,29) PCH_MELOCK R121 *1K/J_4_NC

(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

Quanta Computer Inc.
PROJECT : UM9 UMA

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	1A
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Cap quantities follow UM3

C8335 UMA:22u, DIS:10u, solve UMA CRT display ripple issue.

U9G POWER — Ibex-M 7 OF 10

VCC CORE
1.524A
3.208A
3.208A
0.357A
0.035A
3.208A

PCI E*
0.357A
0.035A
0.061A
0.156A
0.085A

CRT
LVDS
HVCMOS
DMI
NAND / SPI
FDI

U9J POWER — Ibex-M 10 OF 10

Clock and Miscellaneous
PCI/GPIO/LPC
CPU
RTC
HDA
USB
SATA
PCI/GPIO/LPC
0.072A
0.072A
0.073A
3.208A
0.163A
0.357A
>1mA
2mA
6mA

3.208A
0.163A
>1mA
>1mA
0.357A
3.208A
0.035A
1.998A

V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V

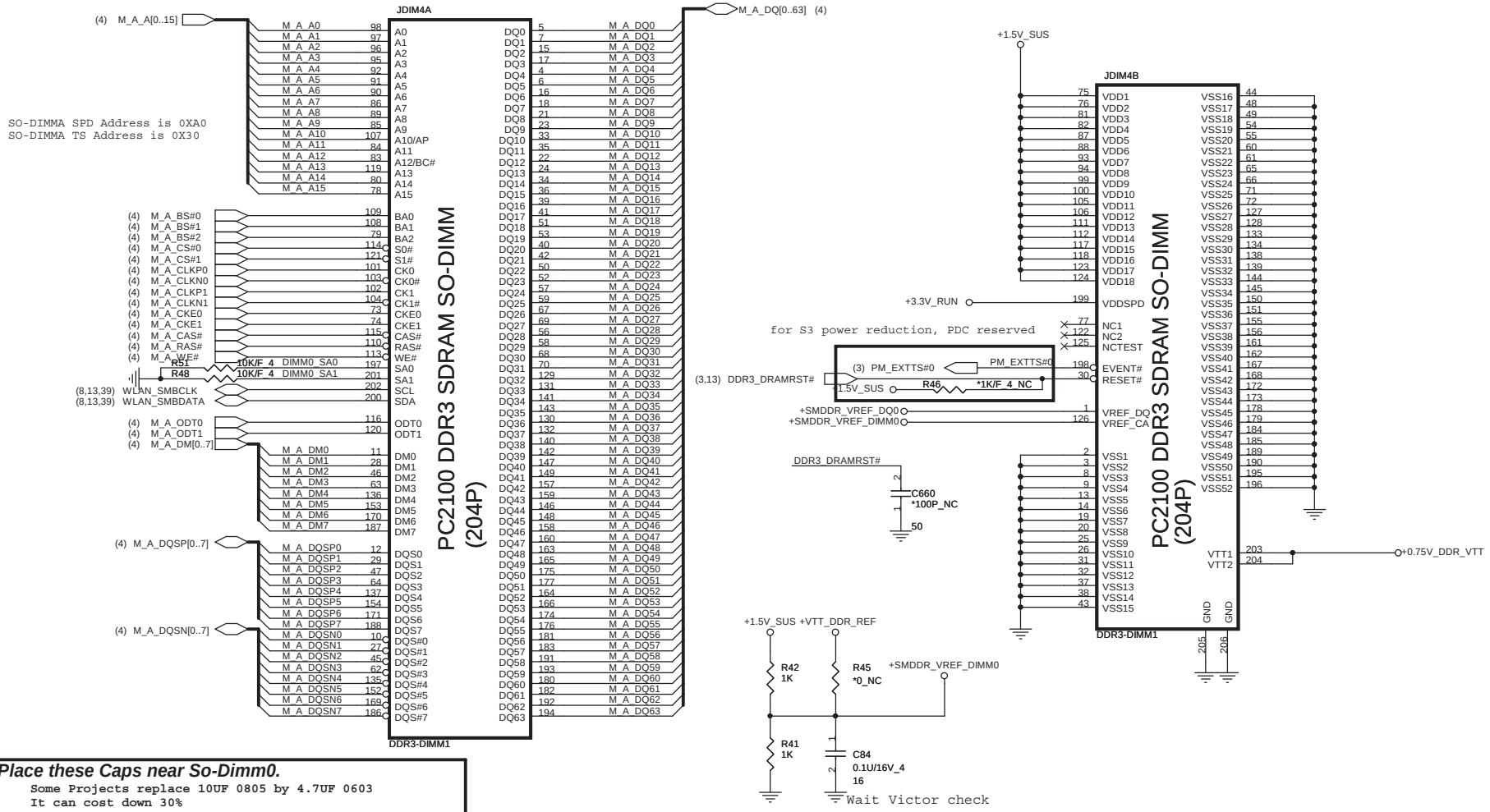
Ensure AF32 and AF34, AH34 are not shorted to the AH35 and AJ35 pins
The above recommendations will create an inductance affect on the AF32 and AF34, AH34 pins and help to filter out the noise

Change CRB from 10uH (DCR = 0.9? which may cause high IR drop) to 10 uH (DCR = 0.36?)

CV01001MN32 DCR MAX:1.15 ohm

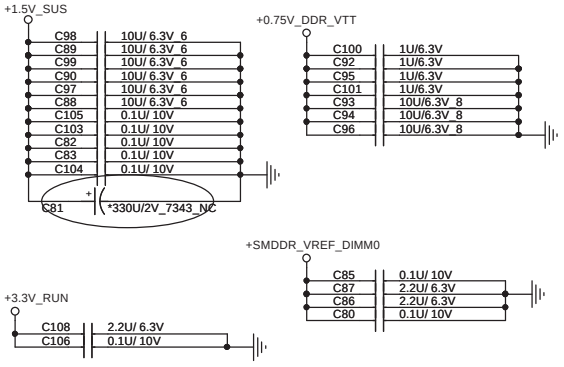
IbexPeak-M_Rev1_0

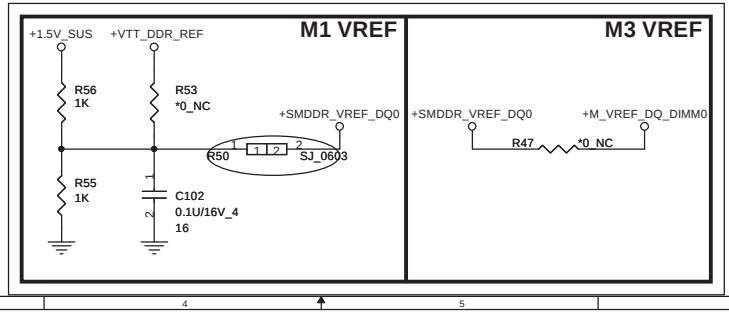
Quanta Computer Inc.	PROJECT : UM9 UMA	
Size	Document Number: PCH 5/5 (POWER)	Rev 1A
Date: Monday, February 01, 2010	Sheet 11 of 51	



Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





Quantities and M1/M3 follow UM3
Locations follow PDC

Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number: DDR3 DIMM-0	Rev: 1A
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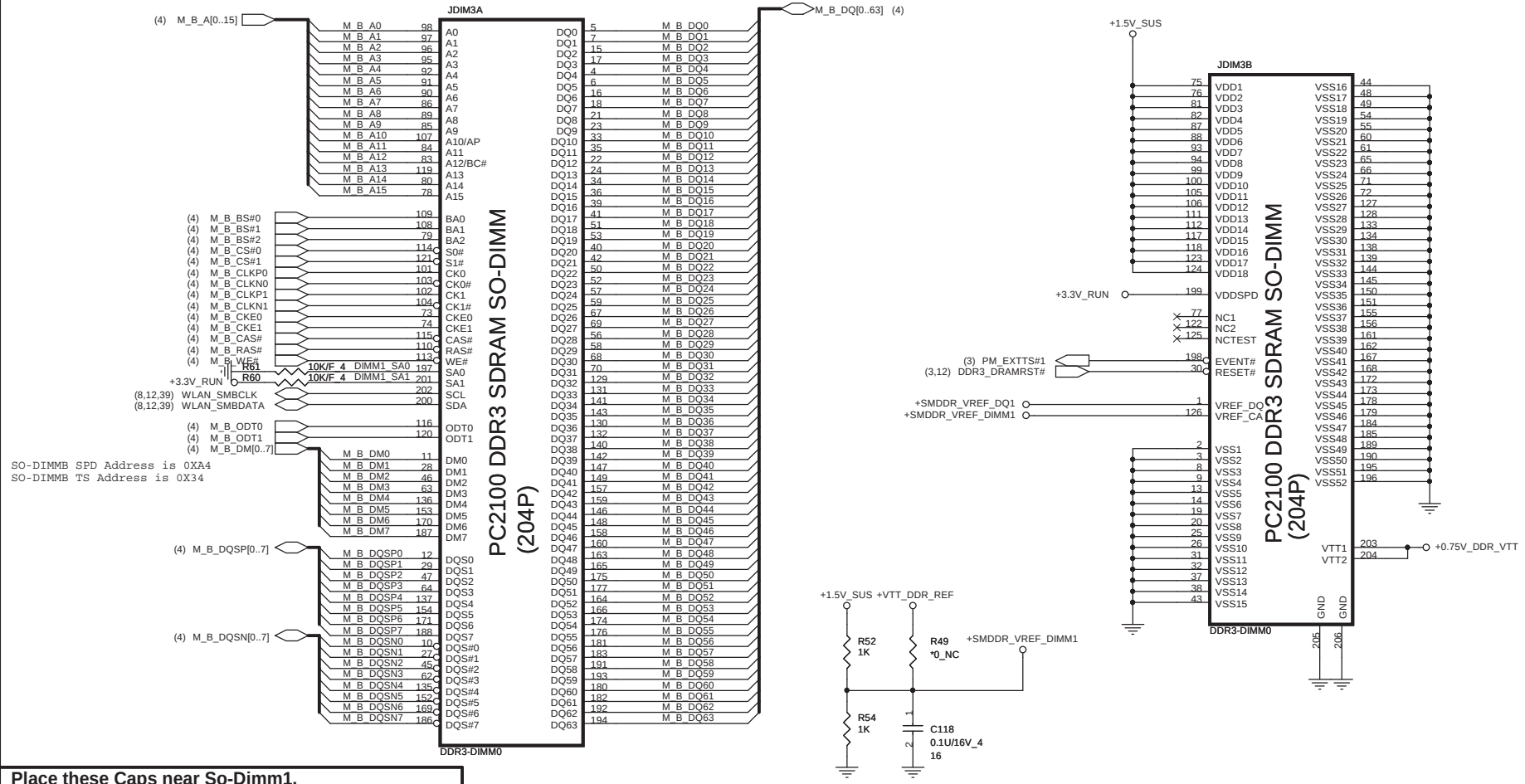
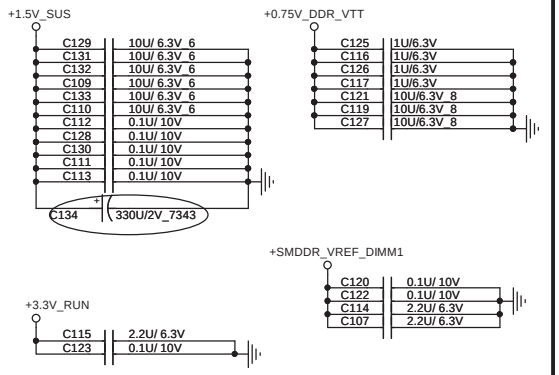
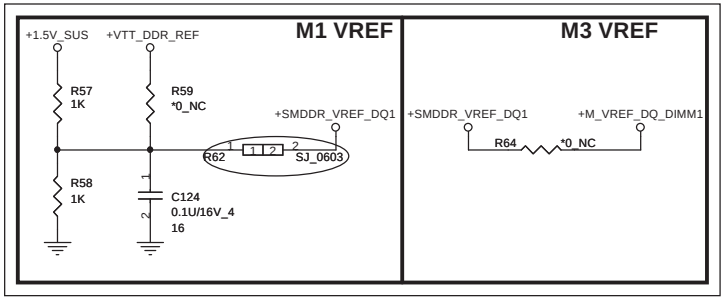


Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603

It can cost down 30%





Quantities and M1/M3 follow UM3
Locations follow PDC

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	DDR3 DIMM-1	1A

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Quanta Computer Inc.

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Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	Blank	1A

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Quanta Computer Inc.

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Size	Document Number	Rev
	Blank	1A

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Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	Blank	1A

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	Blank	1A

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Quanta Computer Inc.

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Size	Document Number	Rev
	Blank	1A

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Quanta Computer Inc.

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Size	Document Number	Rev
	Blank	1A

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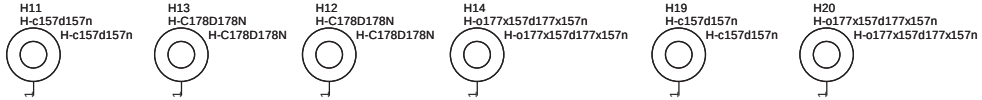
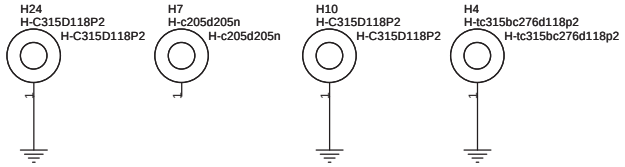
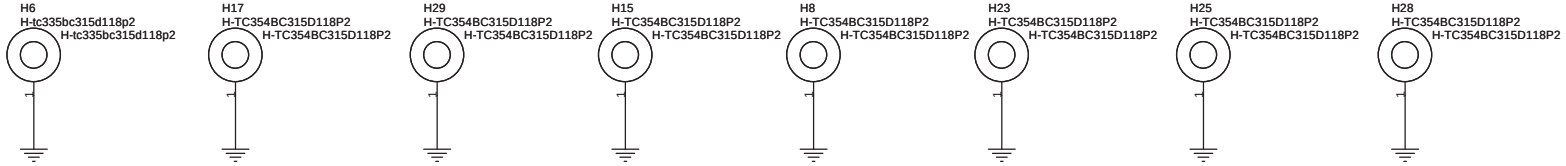
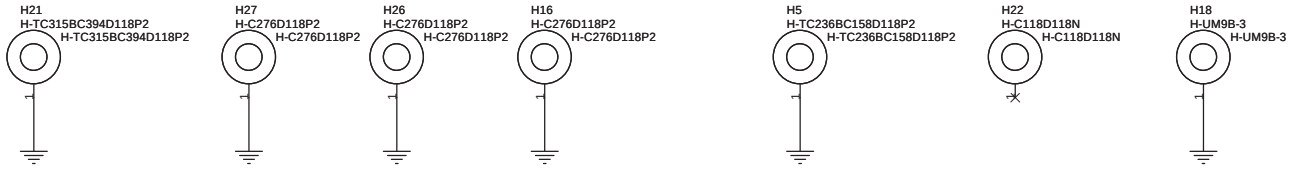
9/28
Del H1&H2



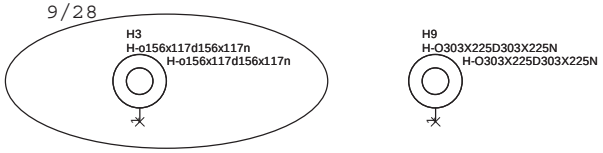




Nut



9/28



Quanta Computer Inc.
PROJECT : UM9 UMA

Size	Document Number	Rev
	SCREW PAD	1A
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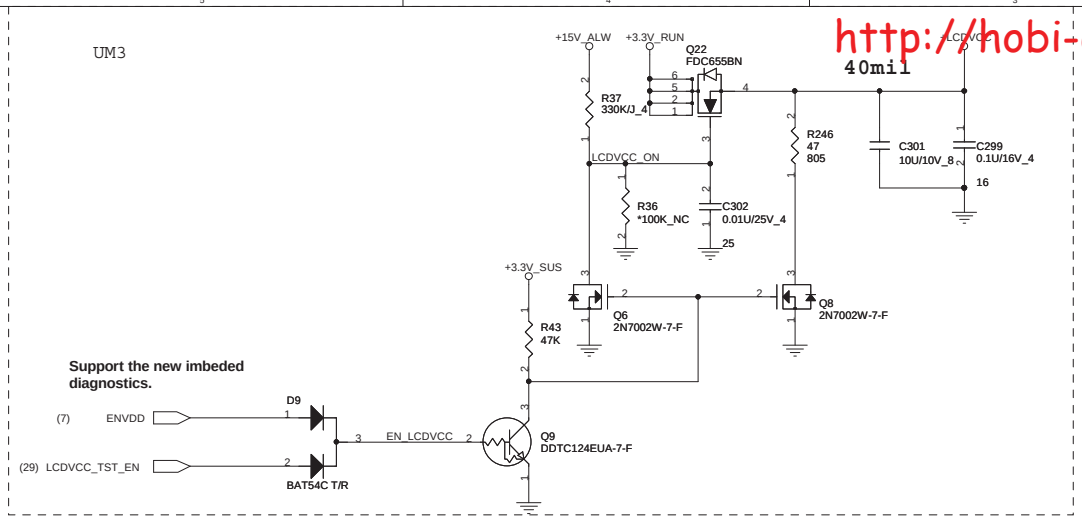

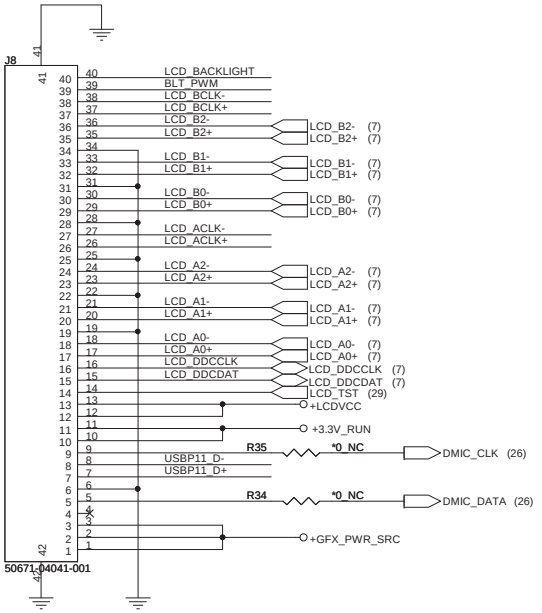

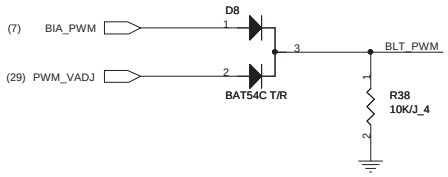

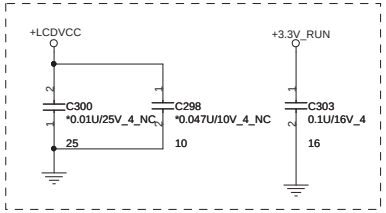

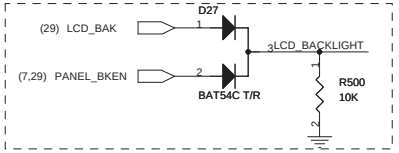

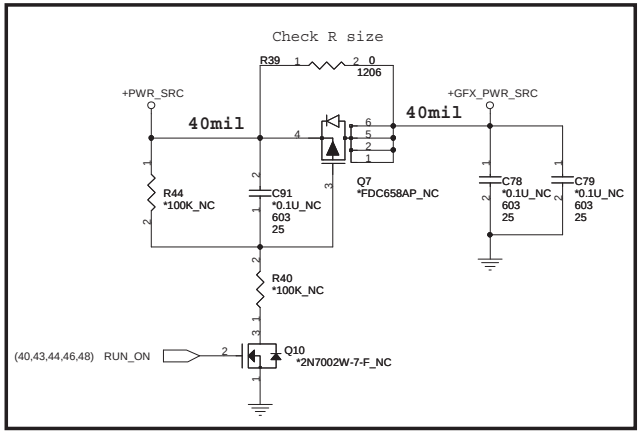

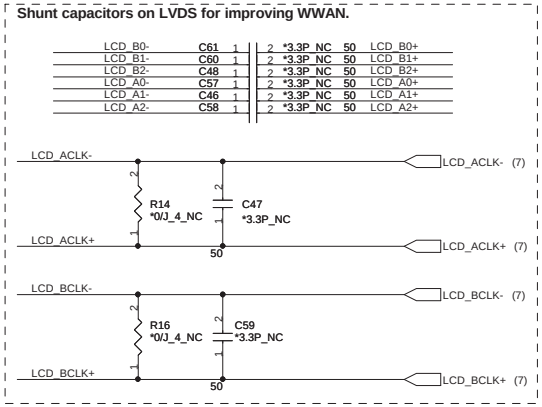

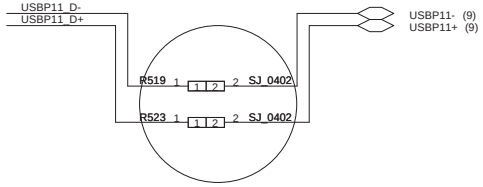

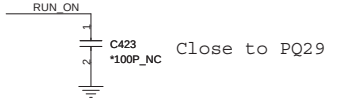

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	LCD CONN / HDMI CONN	1A

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UM3

This page to CRT board

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	CRT CONN	1A

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To CRT BOARD

Quanta Computer Inc.		
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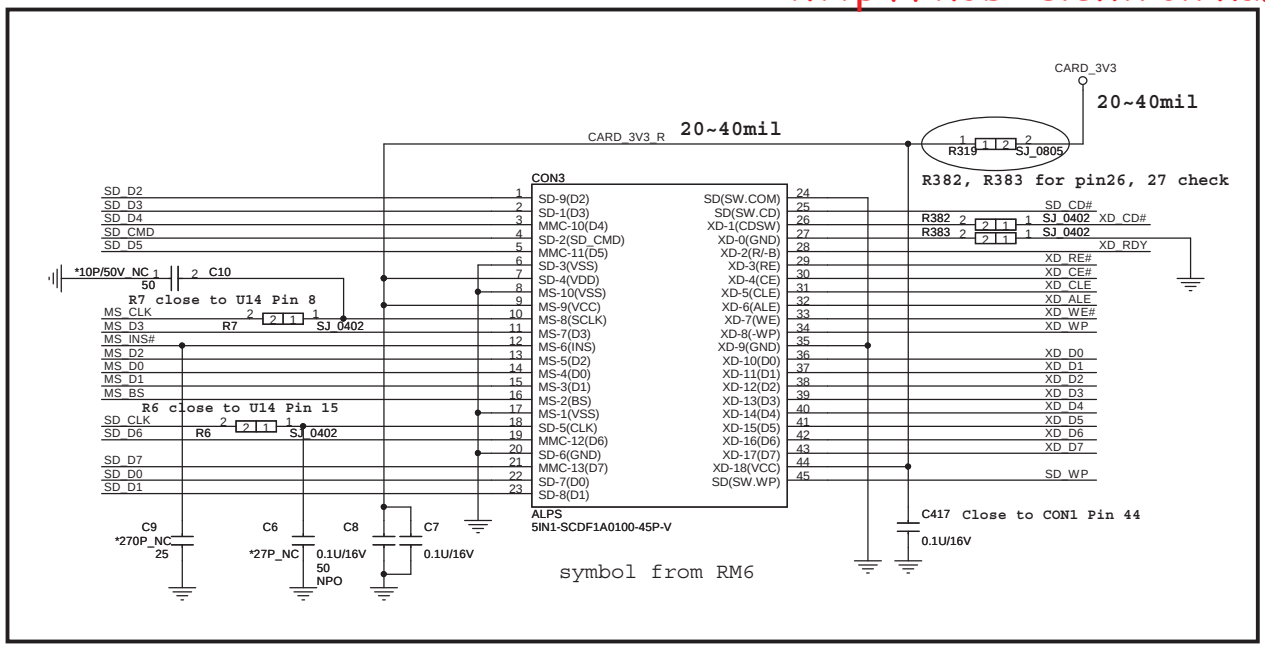
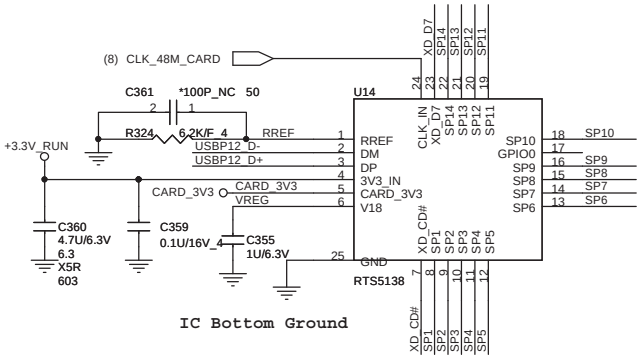
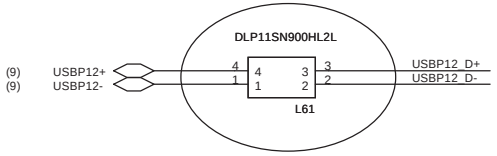




RTS5138-QFN24

SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin



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	Card Reader(RST5138)	1A

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UM3, symbol from PDC

***NOTE: ALC269_VB type add the LDO circuit in IC**

PIN NAME	R350	R344	R349	C398	CODEC IC
28 MIC1_VREF0-L			POP	NC	ALC269
31 CPVREF	POP	NC			VA

VA type: PIN28 作爲MIC之偏壓
PIN31接A-GND

PIN NAME	R350	R344	R349	C398	CODEC IC
28 MIC1_VREF0-L			NC	POP	ALC269
31 CPVREF	NC	POP			VB

VB type: PIN31 作爲MIC之偏壓
PIN28接CAP作爲內部LDO output 輸出濾波用

ZM1_MB_FOR_8BIT_0212-3.DSN

AVDD1, AVDD2 TYP=48mA

DVDD & DVDD-IO TYP=50mA

ALC269

Analog Plane

Digital Plane

Int. Stereo Speakers
5V / 4 Ohm / 2W

PD#=0V : Power down Class D SPK amplifer
PD#=3.3V : Power up Class D SPK amplifer
Internal pulled high.

Reserve RC for EMI

Digital GND Analog GND
Tied at one point only under the ALC269 or near the ALC269

UM3_DIS_20090824_1000_SSI_STEPHEN.DSN

Check the GND of MIC Conn. in the DB need add 0 ohm PD to A-GND

Quanta Computer Inc.
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	Azelia CODEC(ALC269)	1A
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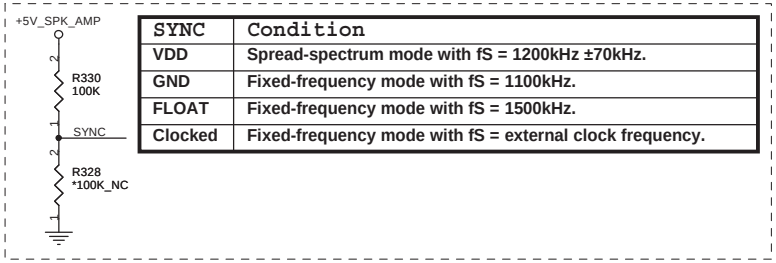
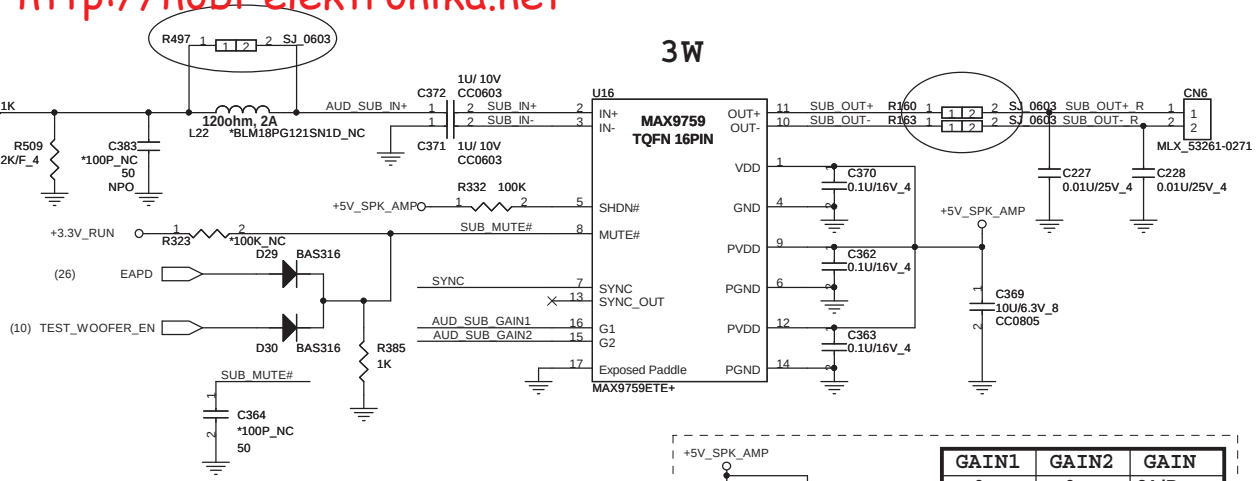
FM9

INTERNAL SUBWOOFER AMP Only for 17''

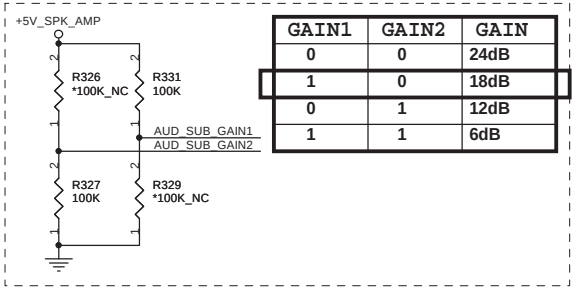
3W

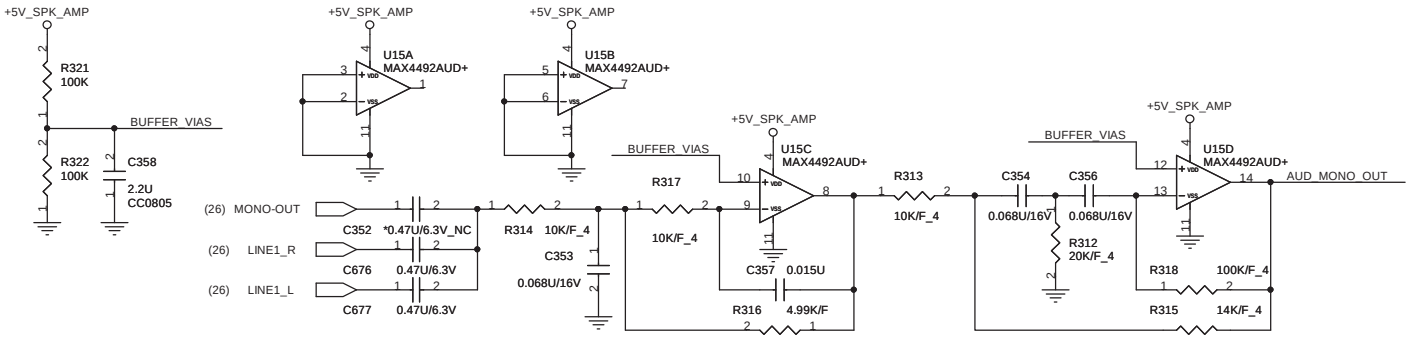
SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.

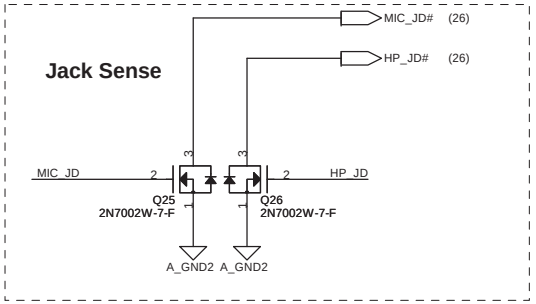


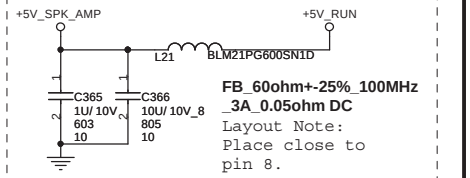


GAIN1	GAIN2	GAIN
0	0	24dB
1	0	18dB
0	1	12dB
1	1	6dB







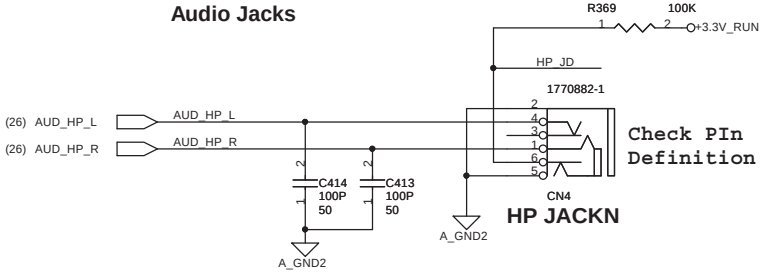


FB_60ohm+-25%_100MHz _3A_0.05ohm DC

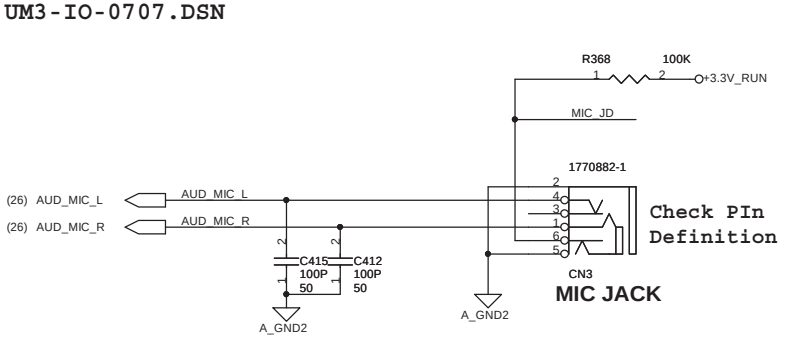
Layout Note: Place close to pin 8.

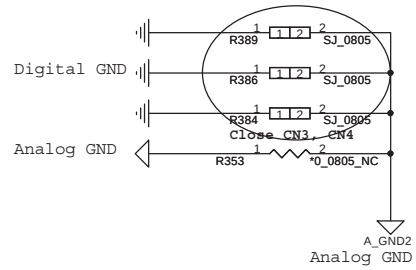
NB_MUTE#	TEST_WOOFER_EN	AUD_SPK PD#	SUB_MUTE#
0	0	L (Disable SPK)	L (Disable Woofer)
0	1	L (Disable SPK)	H (Test Woofer)
1	0	H (Test SPK)	L (Disable Woofer)
1	1	H (Test SPK)	H (Test Woofer)

UM3-IO-0707.DSN
Audio Jacks



UM3-IO-0707.DSN





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Size	Document Number	Rev
	AUDIO CONN	1A

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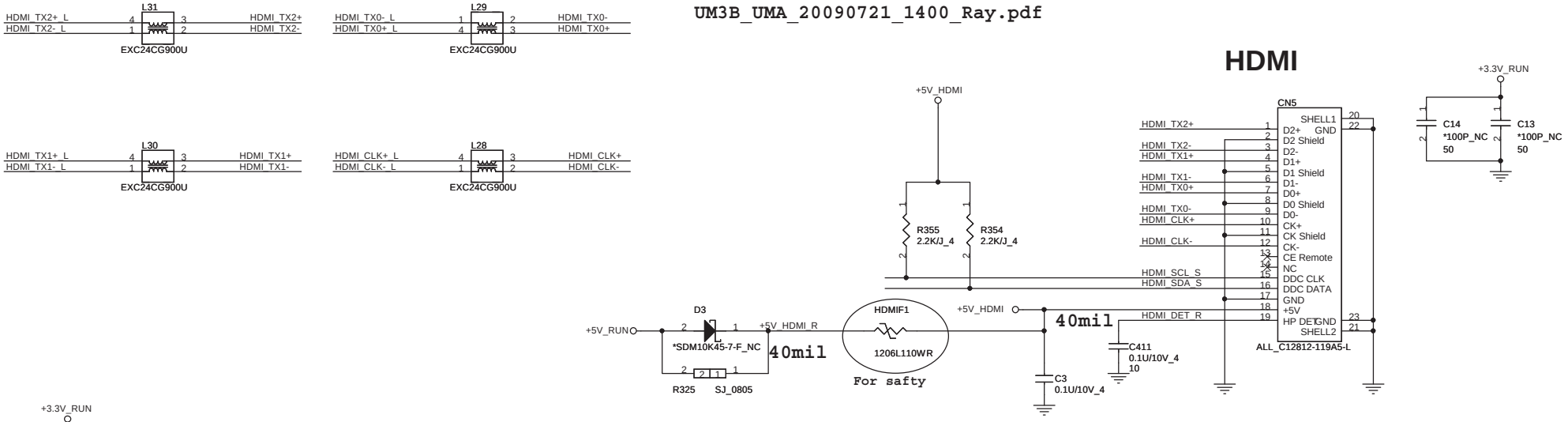
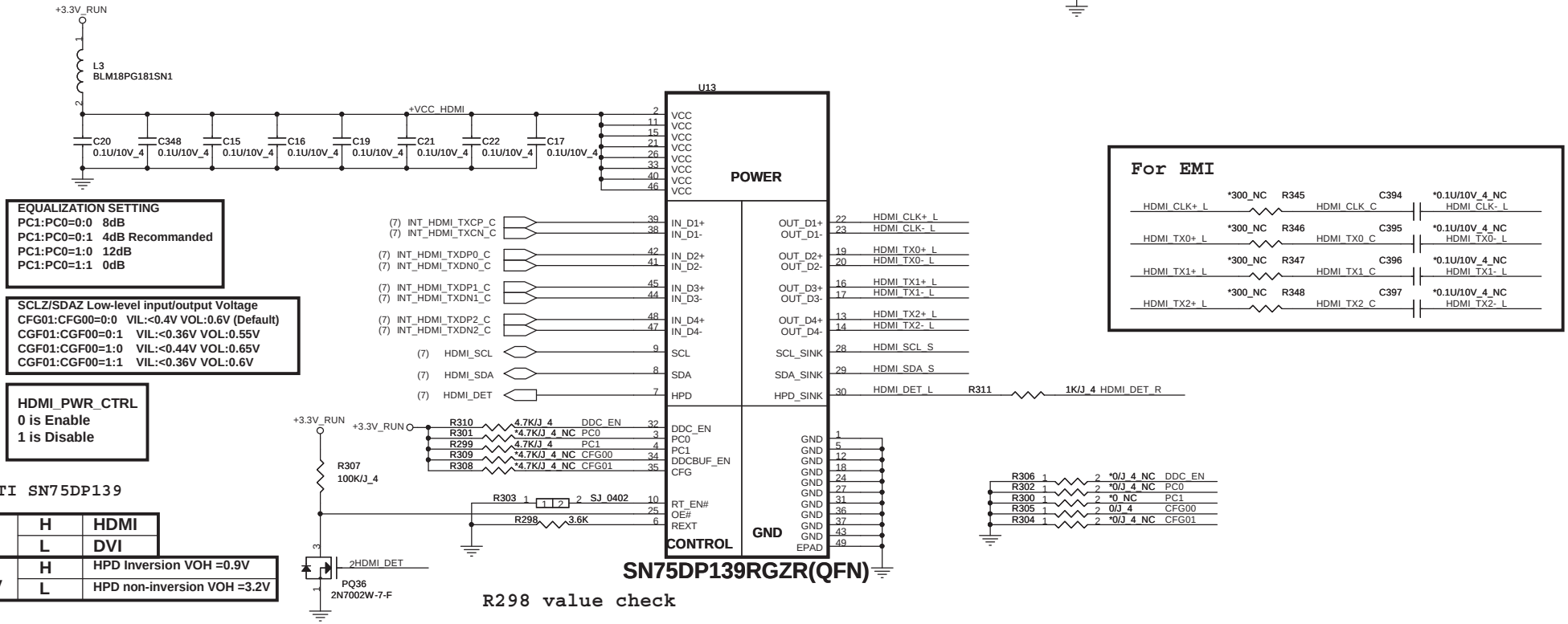
UM3B_UMA_20090721_1400_Ray.pdf

HDMI





SN75DP139RGZR(QFN)

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CFG01:CFG00=0:1 VIL:<0.36V VOL:0.55V
CFG01:CFG00=1:0 VIL:<0.44V VOL:0.65V
CFG01:CFG00=1:1 VIL:<0.36V VOL:0.6V

HDMI_PWR_CTRL
0 is Enable
1 is Disable

TI SN75DP139

PIN 4 I2C_EN	H	HDMI
	L	DVI
PIN 34 HPDINV	H	HPD Inversion VOH =0.9V
	L	HPD non-inversion VOH =3.2V

R298 value check

For EMI

Quanta Computer Inc.
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UM3

U6

ITE8502E
LQFP-128L

(34) KSO[0..17]
(34) KSI[0..7]

KSO17 57
KSO16 56
KSO15 55
KSO14 54
KSO13 53
KSO12 52
KSO11 51
KSO10 46
KSO9 45
KSO8 44
KSO7 43
KSO6 42
KSO5 41
KSO4 40
KSO3 39
KSO2 38
KSO1 37
KSO0 36

KSO17/GPC5
KSO16/GPC3
KSO15
KSO14
KSO13
KSO12/SLCT
KSO11/ERR
KSO10/PE
KSO9/BUSY
KSO8/ACK
KSO7/PD7
KSO6/PD6
KSO5/PD5
KSO4/PD4
KSO3/PD3
KSO2/PD2
KSO1/PD1
KSO0/PD0

KEYBOARD

KSI7 65
KSI6 64
KSI5 63
KSI4 62
KSI3 61
KSI2 60
KSI1 59
KSI0 58

KSI7
KSI6
KSI5
KSI4
KSI3/SLIN
KSI2/INT
KSI1/AFD
KSI0/STB

+3.3V_ALW

C281 10U/ 6.3V_6 603 6.3
C144 1U/6.3V_4
C289 0.1U/16V_4 16
C285 0.1U/16V_4 16
C280 0.1U/16V_4 16

Place these caps close to ITE8502.

+RTC_CELL
R66 SJ_0402
+VBAT1_EC
VBAT1
VCC +3.3V_RUN
VSTBY1 VSTBY2 VSTBY3 VSTBY4 VSTBY5 VSTBY6 +3.3V_ALW
C139 0.1U/16V_4 16

ADC/DAC

ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/GPI4 ADC5/GPI5 ADC6/GPI6 ADC7/GPI7
HWPG (37,40,45)
PAD T28
SUS_PWR_ACK (9)
PAD T29
V_ID1
PBAT_PRES# (47)
IINP (41)
SIO_SLP_S5# (9)
SIO_SLP_S5#

DAC0/GPJ0 DAC1/GPJ1 DAC2/GPJ2 DAC3/GPJ3 DAC4/GPJ4 DAC5/GPJ5
CRIT_TEMP_REP# (10)
SIO_EXT_WAKE# (10)
USB_LEFT_EN# (39)
FAN1_DA (37)
RSMRST# (9)
PM_PWRBTN#_R (9)
USB_LEFT_EN#
D18 SDM10K45-7-F

SMBDAT0 SMBCLK0 RP5 2.2KX2
SMBDAT1 SMBCLK1 RP4 10KX2
USB_LEFT_EN# R235 10K
SUS_ON R83 100K
IMVP_VR_ON R232 *100K_NC
+3.3V_RUN
SERIRQ LCD_BAK R243 R244 10K *10K_NC
SMBDAT2 SMBCLK2 RP3 10KX2

PWM

PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/GPA6 PWM7/GPA7
BREATH_LED# (36)
PAD T30
FAN1_PWM (37)
PWM_VADJ (22)
PAD T31
PAD T32
PAD T4
EC_BEEP (26)

TACH0/GPD6 TACH1/GPD7
FAN1_TACH (37)
PANEL_BKEN (7,22)

TMRI0/WUI2/GPC4 TMRI1/WUI3/GPC6
LID_SW# (34)
SIO_SLP_S3# (9)

R240 0
+3.3V_RUN
R239 *100K_NC
ICH_AZ_CODEC_RST0#
Q21 *2N7002W-7-F_NC
R238 *390K_NC
C288 *0.1U/10V_NC 10
Q20 *MMST3904-7-F_NC
(7,26) ACZ_RST#_AUDIO

IR/UART

PAD T33
PAD T27
RXD/GPB0 TXD/GPB1 GPC0 CTX0/GPB2 CRX1/GPH1/ID1 CTX1/GPH2/ID2
H_CPUDET# (3)
IMVP_PWRGD (3,45)
RUN_ON_1 (40)
BAT1_LED (36)
IMVP_VR_ON (45)
IMVP_VR_ON
PAD T25

LPC/FWH FLASH

PAD T21
FLFRAME/GPG2/LF FLRST/GPG0/TM FLAD3/GPG6
SUS_ON (42,46)
KB_DET# (34)
SUS_ON
PAD T34
PAD T7
FLAD2/SO FLAD1/SI FLAD0/SCE FLCLK
EC_FLASH_SPI_DO (30)
EC_FLASH_SPI_DIN (30)
EC_FLASH_SPI_CS# (30)
EC_FLASH_SPI_CLK (30)
PAD T6
PAD T9
PAD T8

EGPC

ECPWROK
EGAD/GPE1 EGCS/GPE2 EGCLK/GPE3
ECPWROK (9)
ALW_ON (36)
PAD T26
PAD T35

GPIO

GPH3/ID3 GPH4/ID4 GPH5/ID5 GPH6/ID6 GPG1/ID7
BID2
USB_RIGHT_EN#
BID1
LCD_SIZE_ID
LCD_SIZE_ID2
BID2 (30)
USB_RIGHT_EN# (30,39)
BID1 (30)
LCD_SIZE_ID (30)
LCD_SIZE_ID2 (30)

R65 *100K_NC +3.3V_ALW
RI1/WUI0/GPD0 RI2/WUI1/GPD1 WUI5/GPE5
PAD T36
D12 SDM10K45-7-F
ACAV_IN (36,41)
BAT2_LED (36)

RING/PWRFAIL/LPCRST/GPB7
AC_PRESENT (9)

PWRSW/GPE4
SYS_PWR_SW# (36)

GINT/GPD5
LCDVCC_TST_EN (22)
PAD T5

ITE8502E
lqfp128-16x16-4

LPC

(3,9,39) PLTRST# R67 SJ_0402
(9) CLK_33M_KBC
(7,39) LFRAME#
(7,39) LAD0
(7,39) LAD1
(7,39) LAD2
(7,39) LAD3

LPCRST/WUI4/GPD2
LPCCLK
LFRAME
LAD0
LAD1
LAD2
LAD3

(9) CLKRUN#
(7) SERIRQ
(10) SIO_EXT_SMI#
(10) SIO_EXT_SCI#
(10) GATEA20
(22) LCD_TST

CLKRUN/GPH0/ID0
SERIRQ
ECSMI/GPD4
ECSCI/GPD3
GA20/GPB5
LPCPD/WUI6/GPE6

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

D11 D13 D17 SDM10K45-7-F

(10) RCIN#
T12 PAD
(22) LCD_BAK
D10 SDM10K45-7-F
WRST#
LCD_BAK

KBRST/GPB6
WRST
PWUREQ/GPC7

(26) NB_MUTE#
ICH_AZ_CODEC_RST0#

L80HLAT/GPE0
L80LLAT/WUI7/GPE7

SMBUS

(41,47) SMBCLK0
(41,47) SMBDAT0
(8) SMBCLK1
(8) SMBDAT1
(2,37) SMBCLK2
(2,37) SMBDAT2

SMBCLK0 110
SMBDAT0 111
SMBCLK1 115
SMBDAT1 116
SMBCLK2 117
SMBDAT2 118

SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/GPF6
SMDAT2/GPF7

PS/2

R507 SJ_0402
(7,10) PCH_MELOCK
T11 PAD
(47) PS_ID
T10 PAD
(34) CLK_TP_SIO
(34) DAT_TP_SIO

PS2CLK0/GPF0
PS2DAT0/GPF1
PS2CLK1/GPF2
PS2DAT1/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5

Charge and BAT
PCH
VGA, LAN, Clock
Thermal IC

+3.3V_ALW
R63 100K WRST#
C137 1U/ 10V 603 10

ITE8502_XTAL1 128
ITE8502_XTAL2 2
ITE8502IX_JX 12

CK32K
CK32KE
VCORE
VSS1 1
VSS3 27
VSS4 49
VSS5 91
VSS6 113
VSS7 122
AVCC 74
AVSS 75

+3.3V_ALW
L6 BLM11A05S 603
+AVCC_EC
C147 0.1U/16V_4 16
L5 BLM11A05S 603

Board ID Straps

Madison
Discrete
+3.3V_ALW
R234 *10K_NC
R78 10K
R94 *10K_NC
R88 *10K_NC
R89 10K
R91 10K
R233 *10K_NC
R79 *10K_NC
R95 10K
R86 10K
R90 *10K_NC
R92 *10K_NC
USB_RIGHT_EN#
BID1
LCD_SIZE_ID
BID2
LCD_SIZE_ID2
V_ID1
Park
UMA
VGA_TYPE
VGA_IDENTIFY

	LCD_SIZE_ID (99)	LCD_SIZE_ID2 (107)
13.3"	0	0
14"	1	0
17"	0	1

BID1	BID0 USB_RIGHT_EN#	UM9(UMA)	UM9C (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	OT (A00)	OT (A00)
0	0	(A01)	(A01)

32KHz Clock.(Layout close to EC)

C141 18P/50V_4 ITE8502_XTAL1
W3 32.768KHZ
R496 10M/J_4
C140 18P/50V_4 ITE8502_XTAL2

CLK_33M_KBC
R241 10
C284 2.2P 50

ITE8502IX_JX
C287 0.1U/16V_4 16

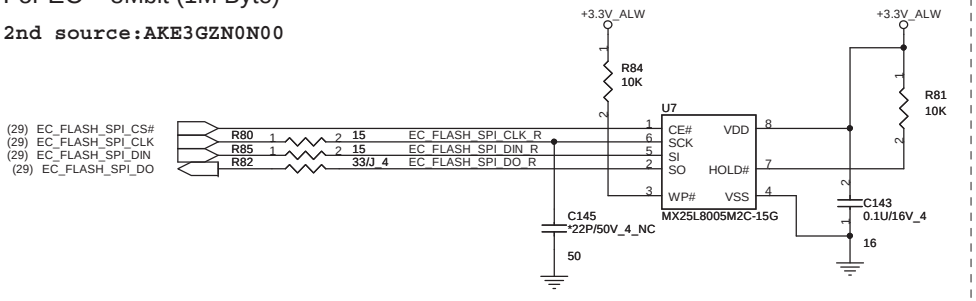
Close to PU9
IMVP_VR_ON
C424 *100P_NC 50
IMVP_PWRGD
C283 *100P_NC 50

Quanta Computer Inc.
PROJECT : UM9 UMA

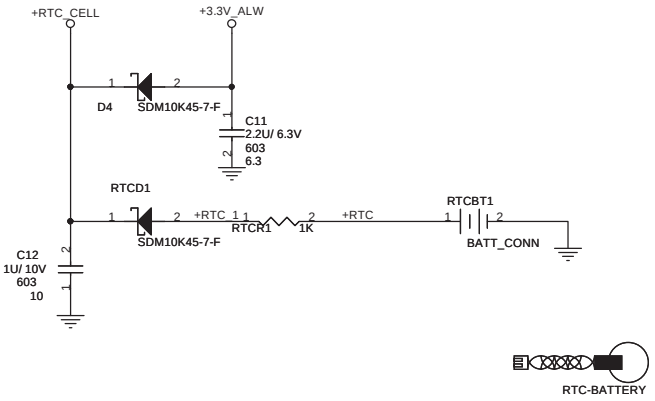
Size	Document Number	Rev
	SIO ITE8502	1A
Date: Monday, February 01, 2010	Sheet 29 of 51	

For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



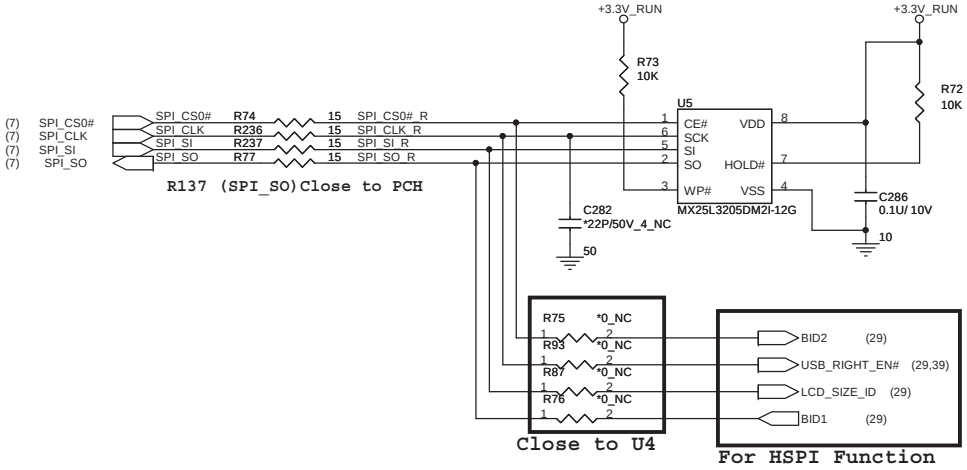
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00

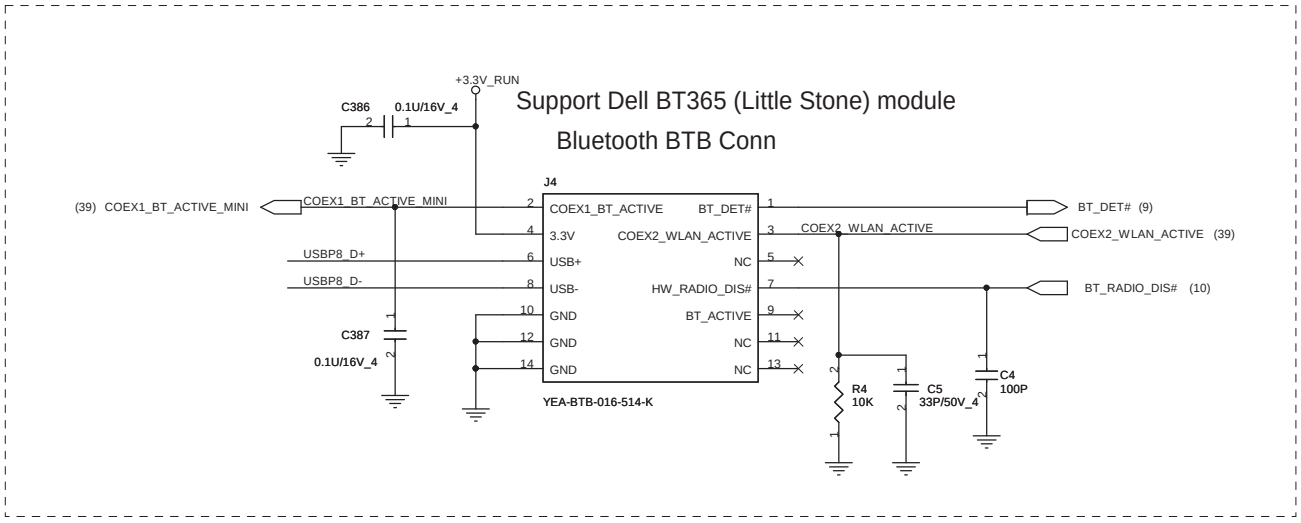


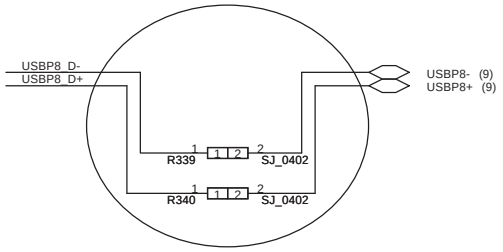
Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number: FLASH/RTC	Rev: 1A
Date: Monday, February 01, 2010	Sheet 30 of 51	

UM3

WWAN To DB

WLAN To DB





Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number: MINI-Card WLAN / BT	Rev: 1A
Date: Monday, February 01, 2010	Sheet 32 of 51	

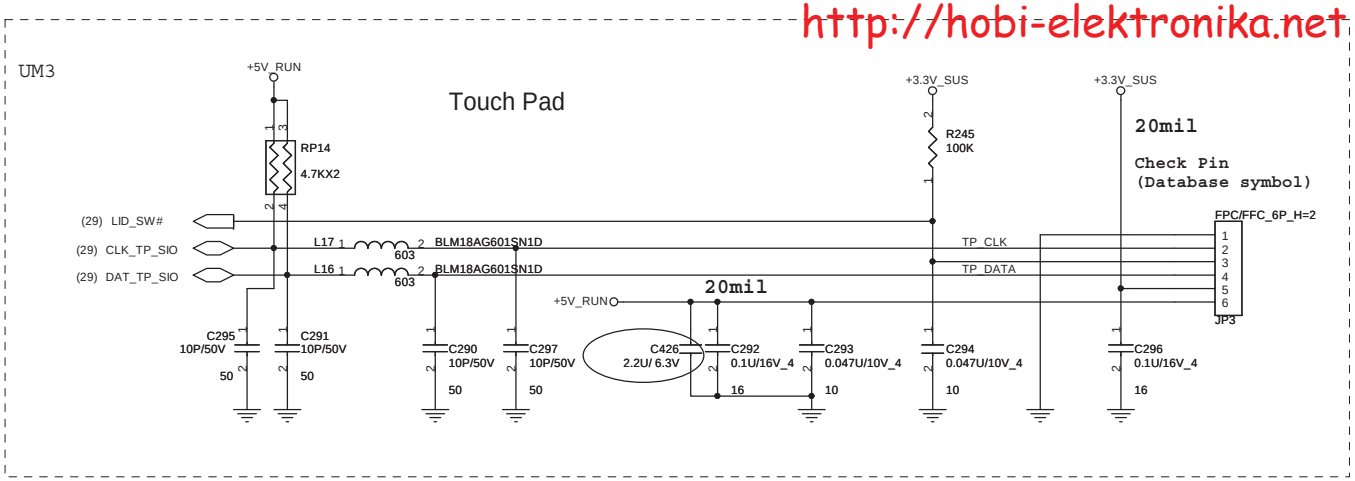
eSATA and USB To DB

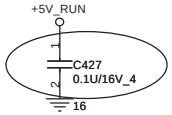
Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	eSATA & Right USB	1A

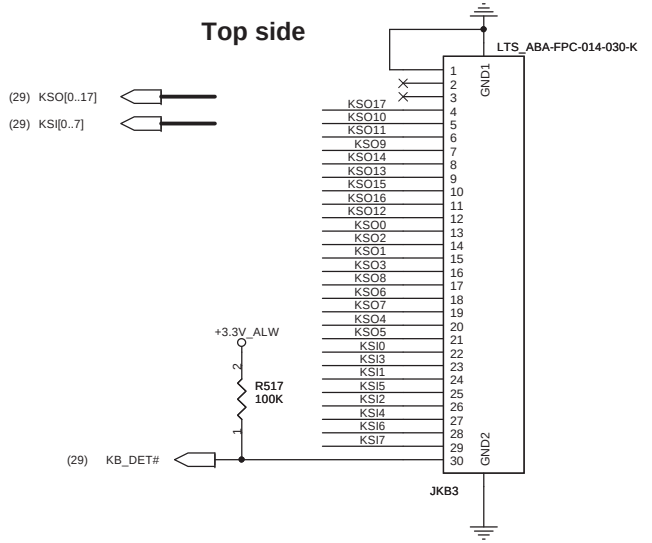
Date: Wednesday, January 27, 2010 Sheet 33 of 51

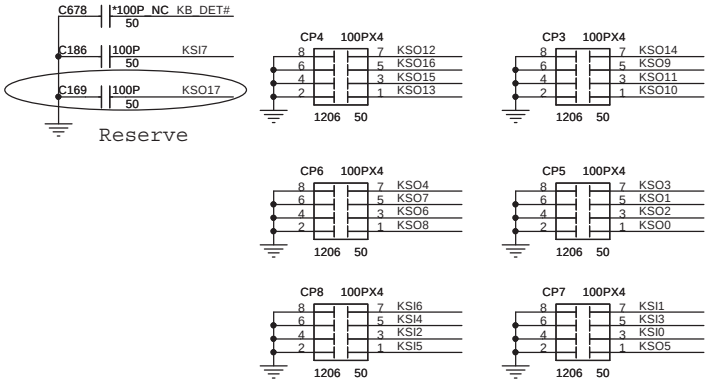




KEYBOARD CONNECTOR

Top side





100P CAPS CLOSE TO JKB3

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	TOUCH PAD, KB	1A
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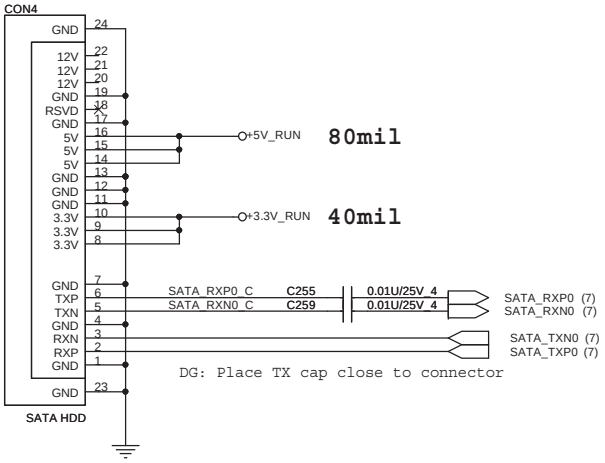
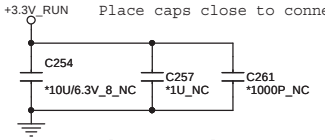
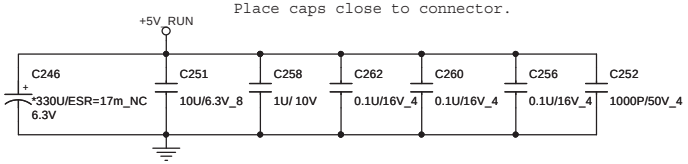
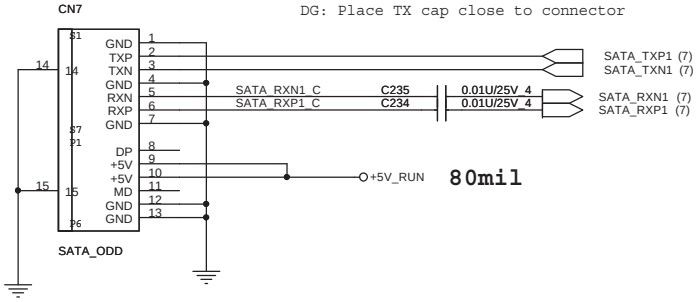
SATA Connector.

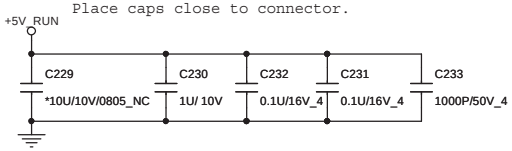






ODD Connector





Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	SATA (HDD&CD_ROM)	1A

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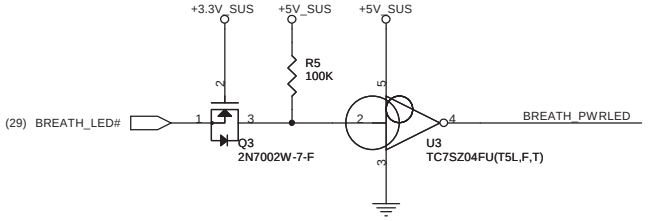
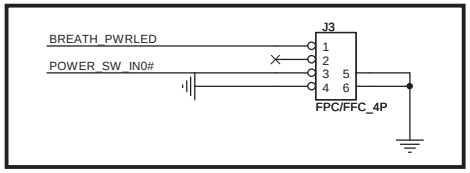
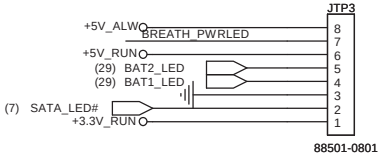
Power



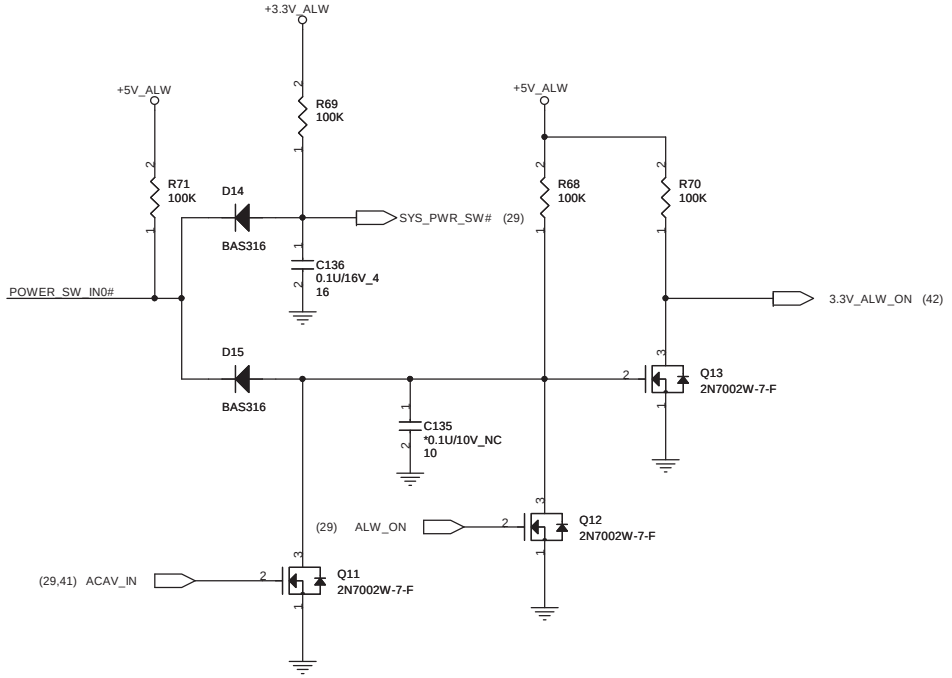
Power button Cable

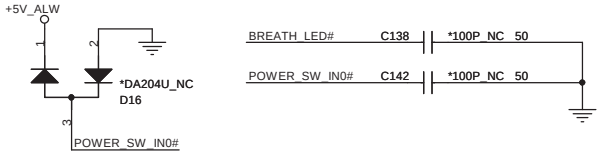


Check Connector P/N and footprint



3VALW ON POWER LOGIC





Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number: SWITCH, LED	Rev 1A
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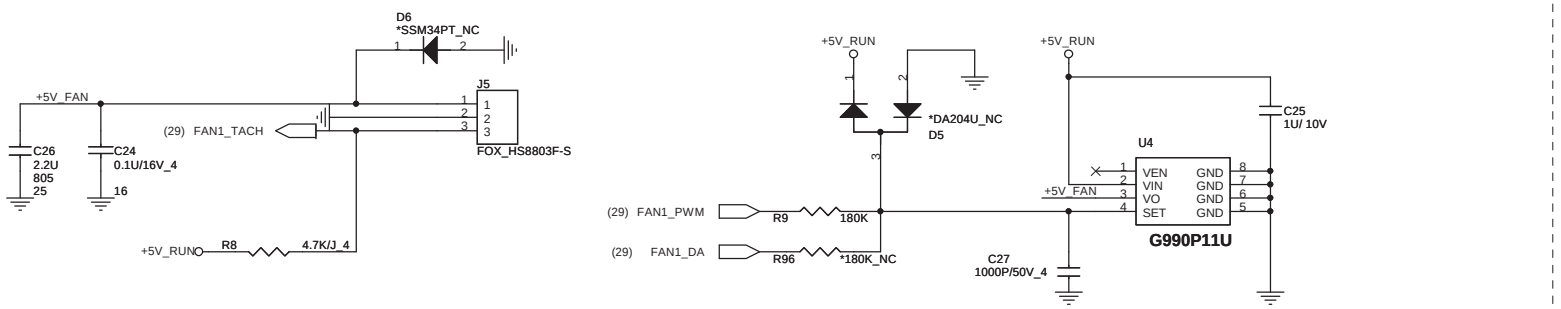
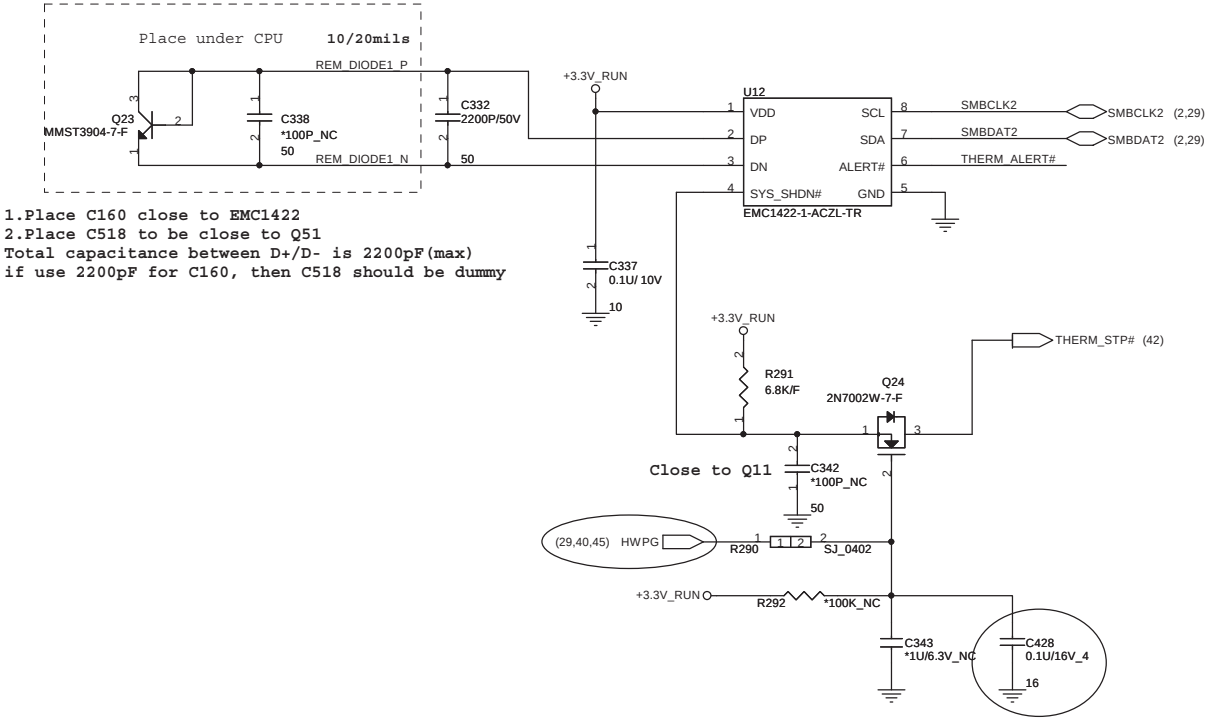
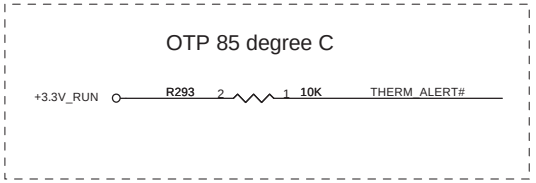
FAN CONTROL

6/23 COPY FROM RM6



UM3

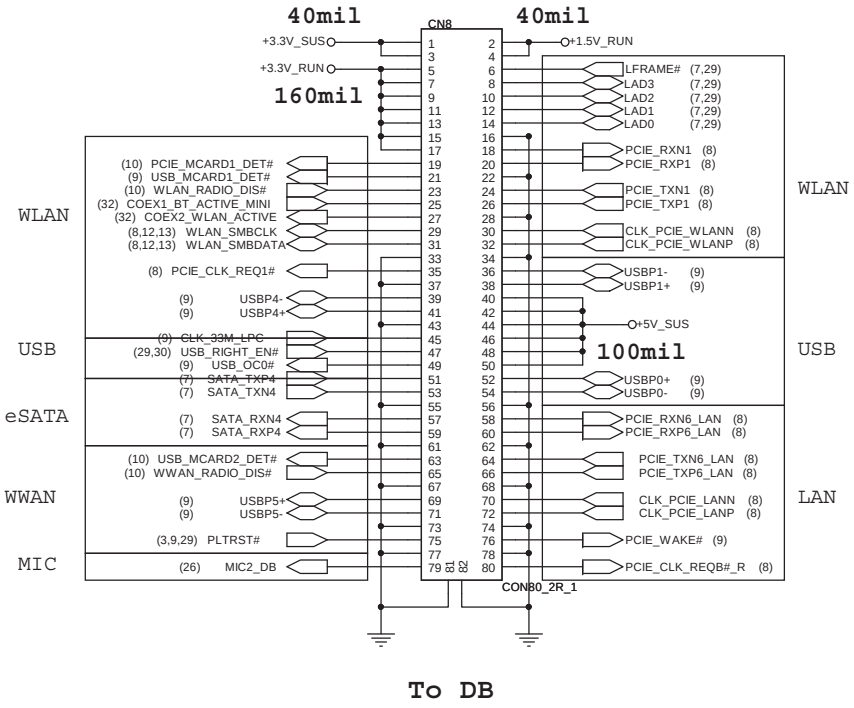




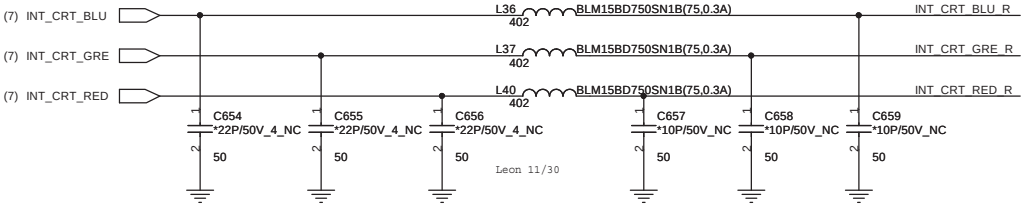
Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number: FAN & THERMAL	Rev 1A
Date: Monday, February 01, 2010	Sheet 37 of 51	

LAN To DB

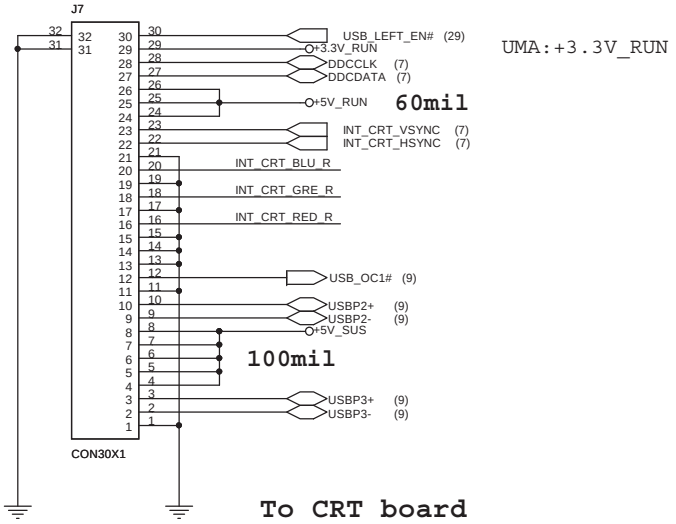
Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number: LAN(AR8152/RJ-45)	Rev: 1A
Date: Wednesday, January 27, 2010	Sheet 38 of 51	



To DB

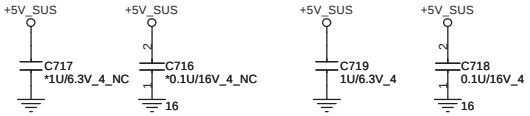


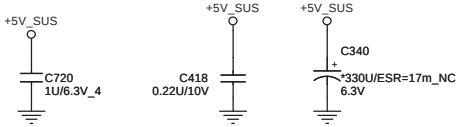
Close to PCH



UMA:+3.3V_RUN

To CRT board



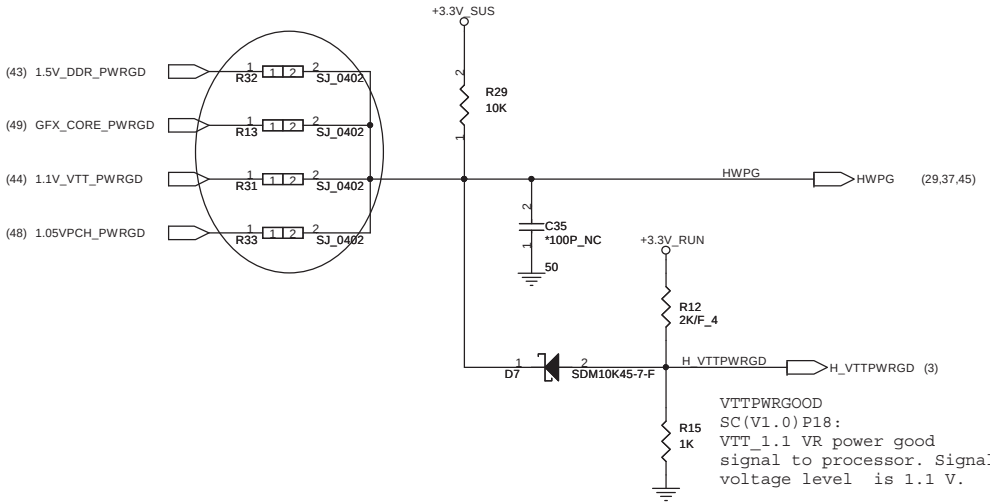


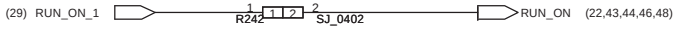
Quanta Computer Inc.

PROJECT : UM9 UMA

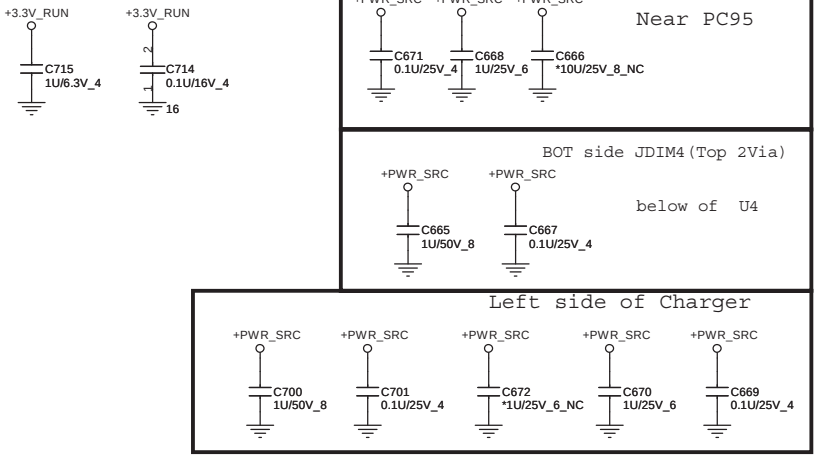
Size	Document Number	Rev
	BTB CONN	1A
Date: Monday, February 01, 2010	Sheet 39 of 51	

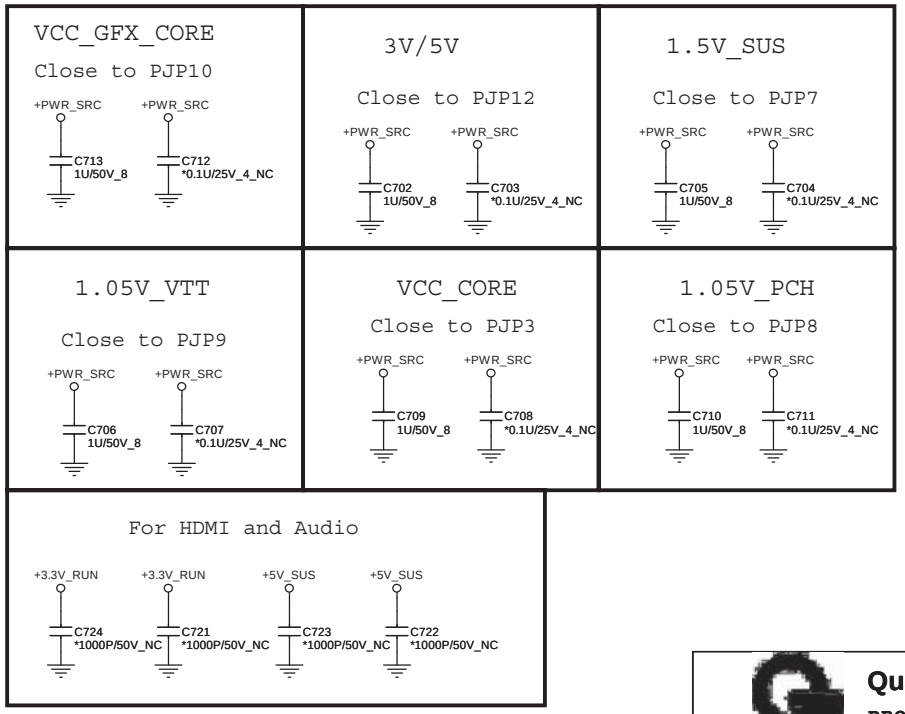
UM3





For FDI bus noise





Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	System Reset Circuit	1A

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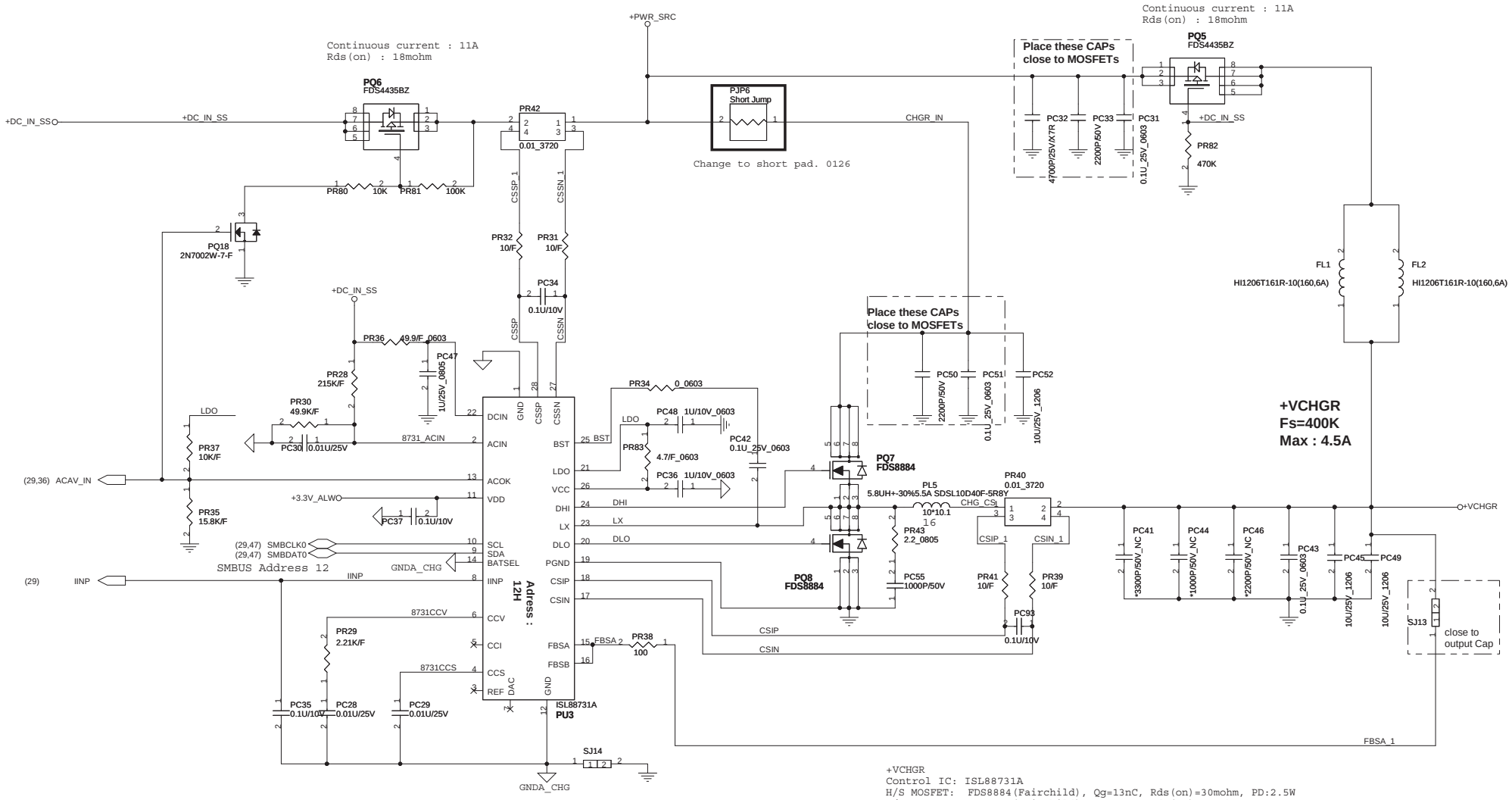
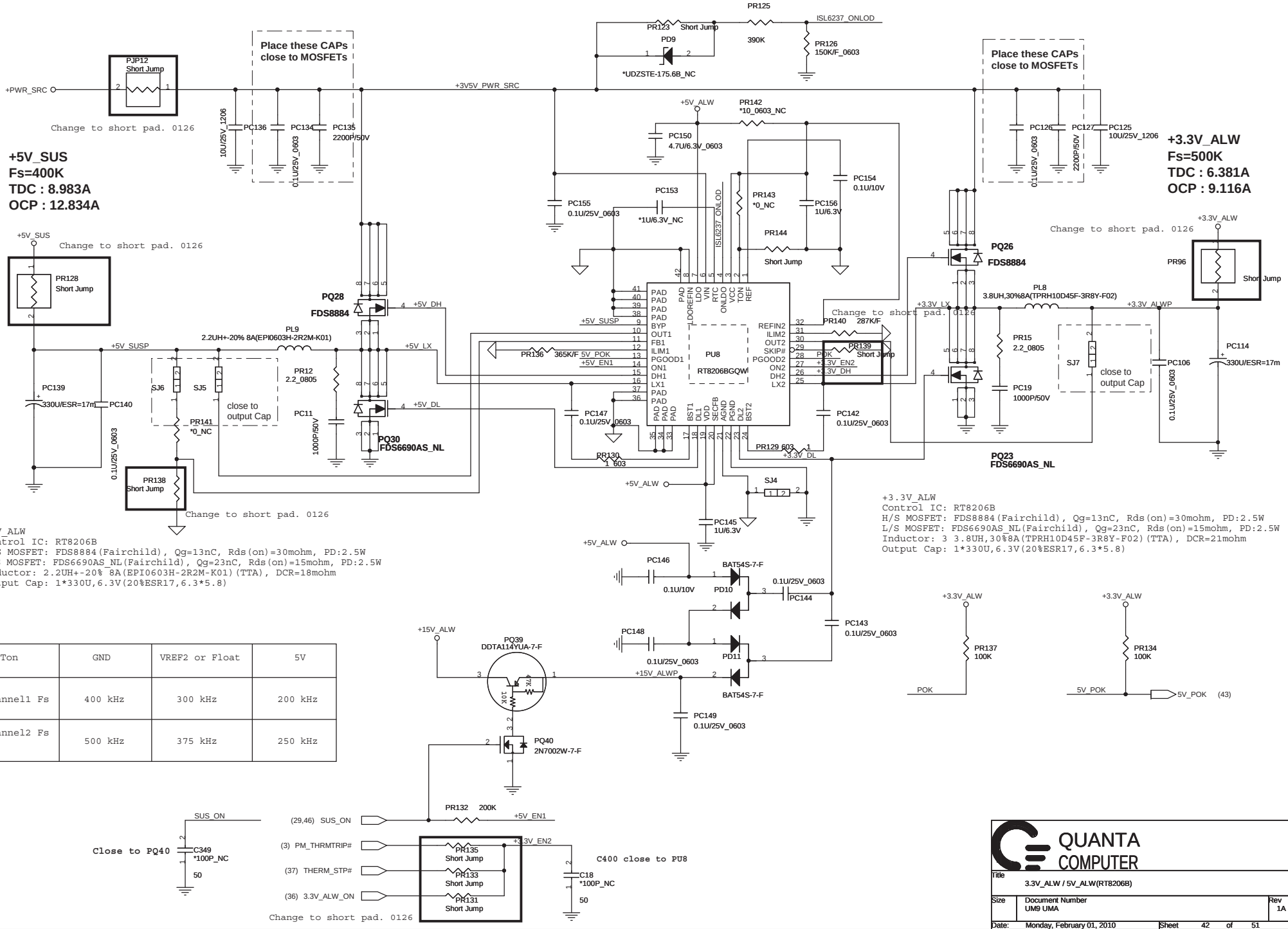
UM9-UMA-0910 OF POWER.DSN



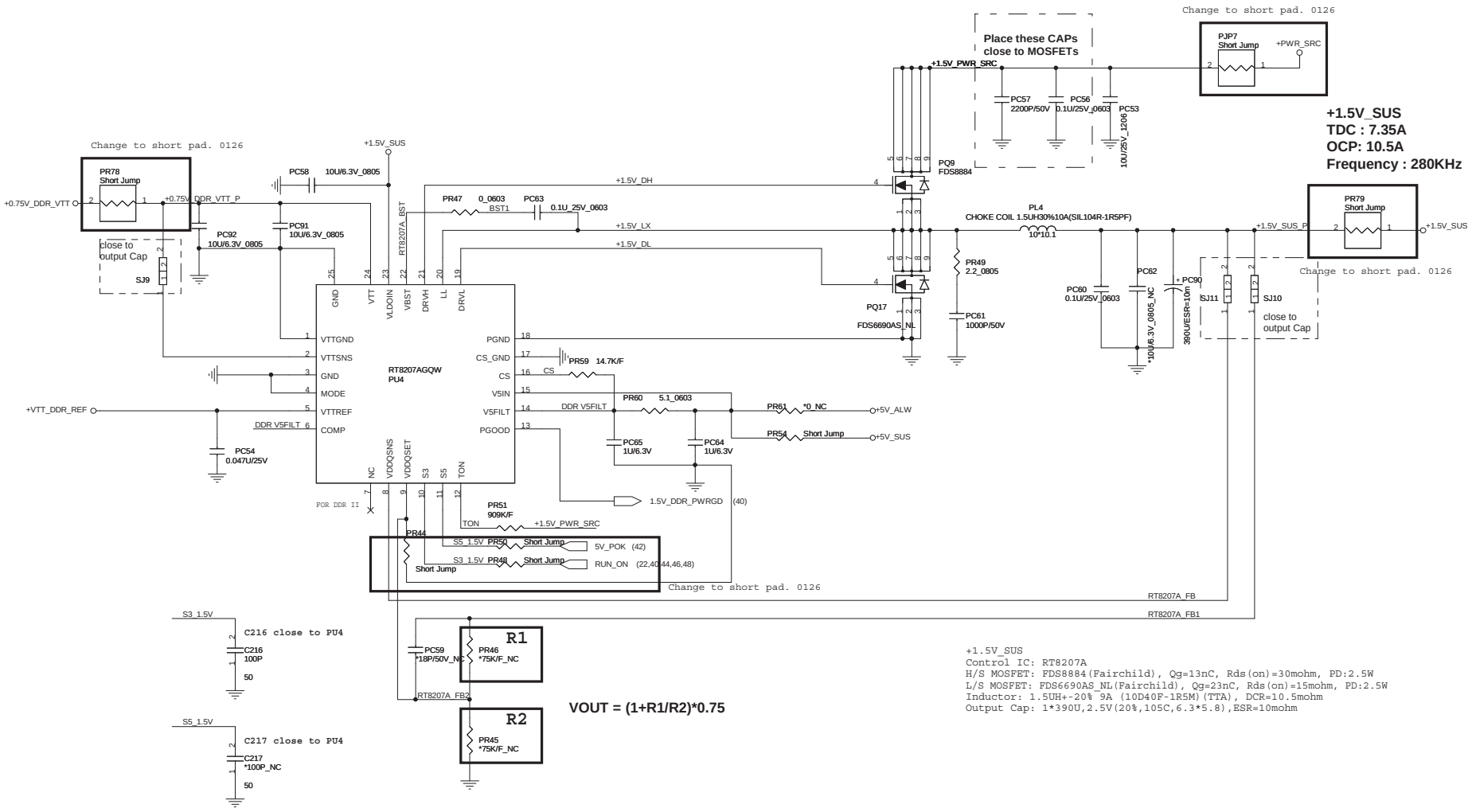
+VCHGR
Control IC: ISL88731A
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
Inductor: 5.8UH +-30% 5.5A SDSL10D40F-5R8Y(TTA), DCR=21mohm
Output Cap: 2*10U 25V(+-10%,X6S,1206)

QUANTA COMPUTER

Title	Charger (ISL88731)	
Size	Document Number UM9 UMA	Rev 2A
Date: Monday, February 01, 2010	Sheet 41 of 51	



Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz



+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 1.5UH+-20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

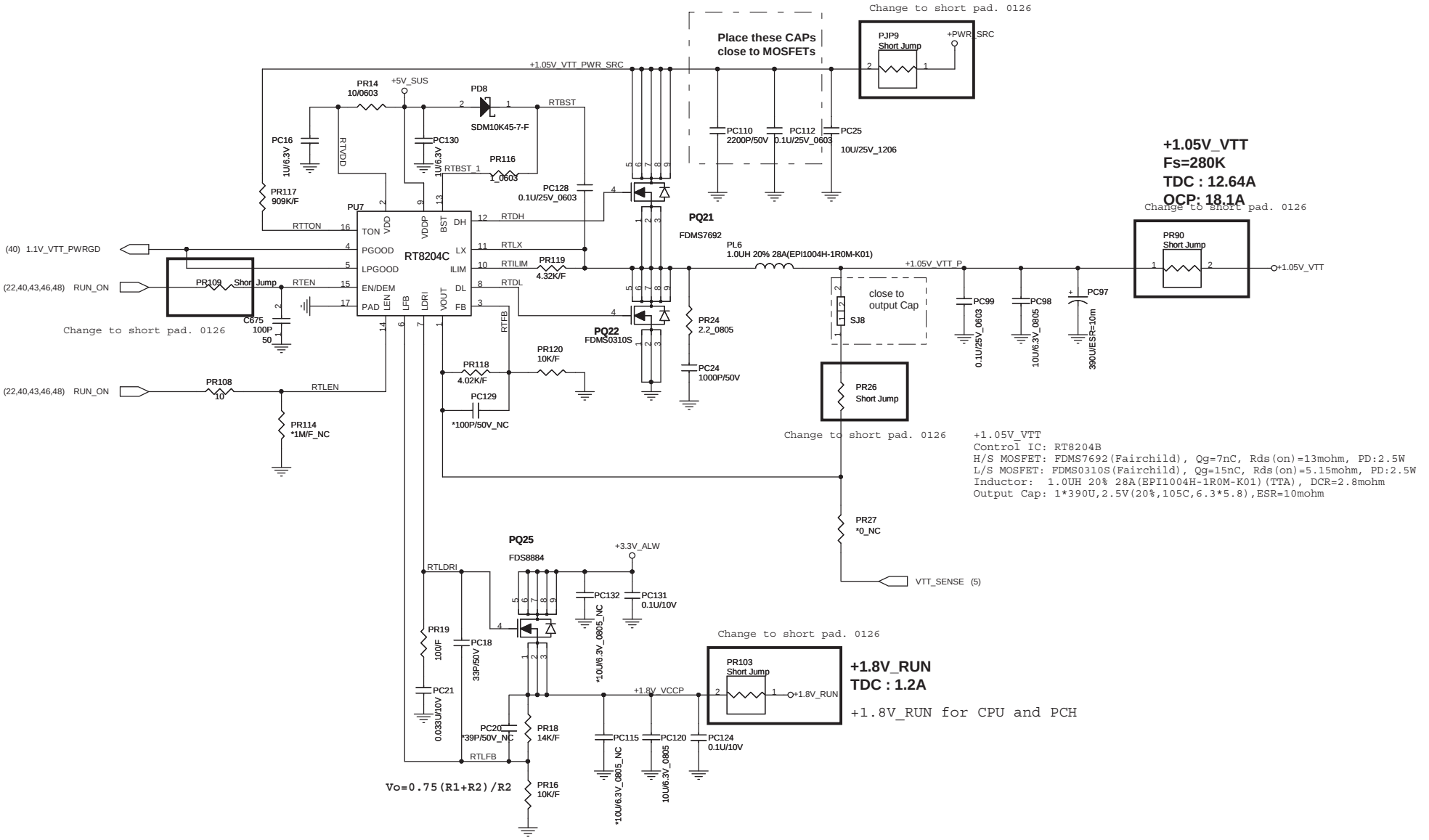
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

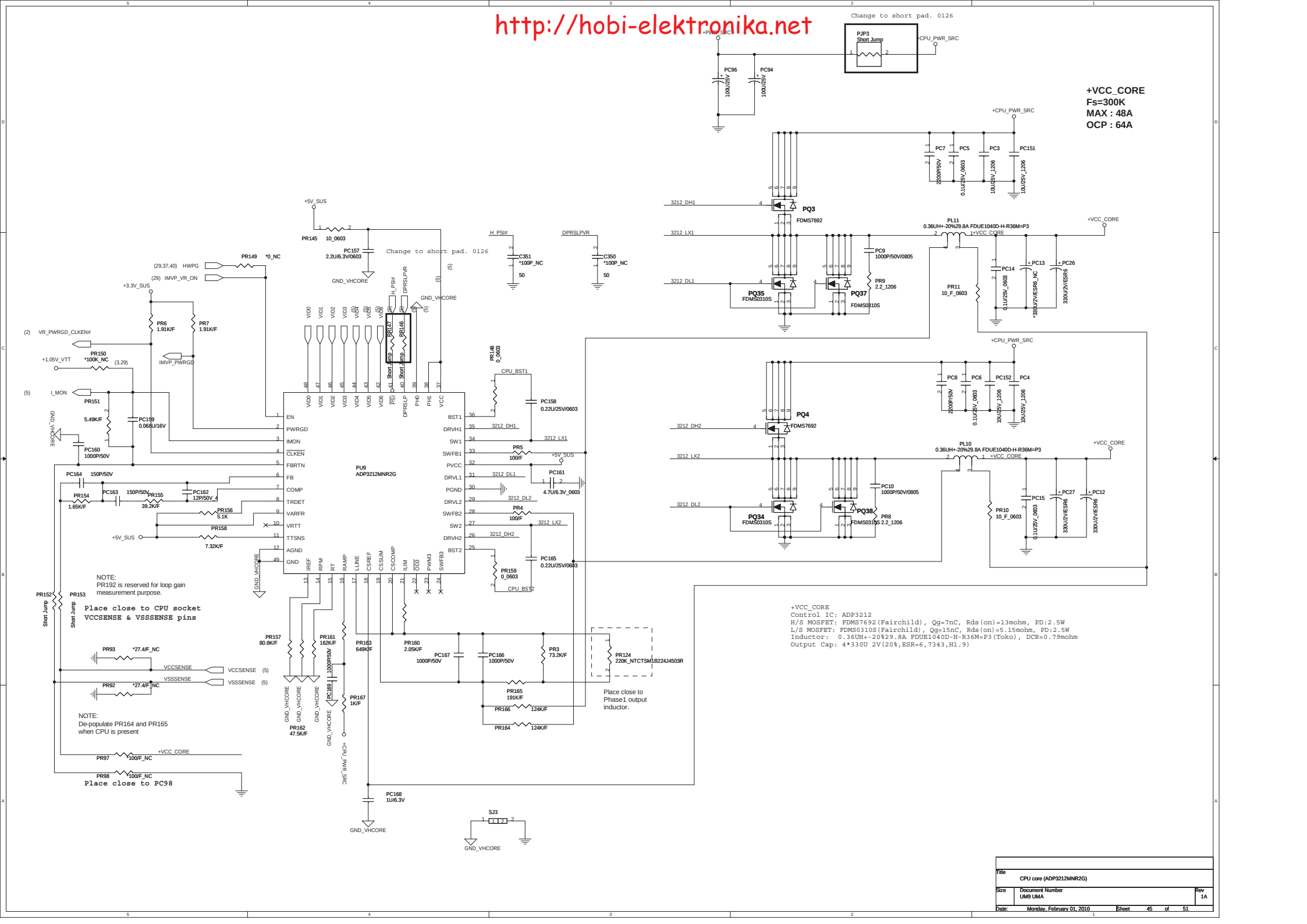
Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

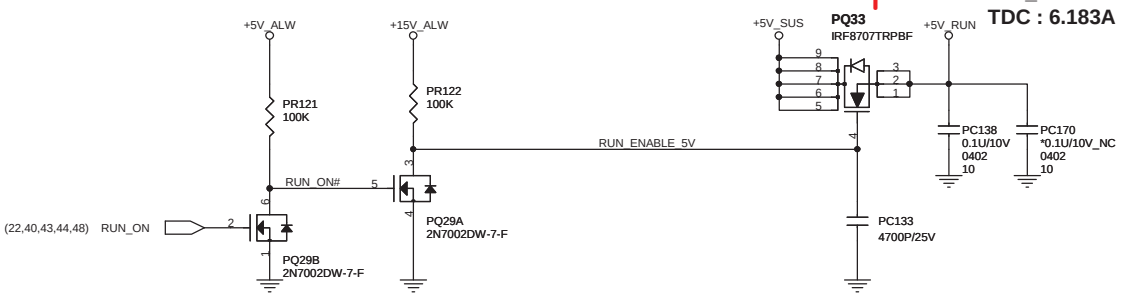
Title	DDR3 +1.5V_SUS(RT8207AGQW)		
Size	Document Number UM9 UMA		Rev 1A
Date:	Monday, February 01, 2010	Sheet 43 of 51	

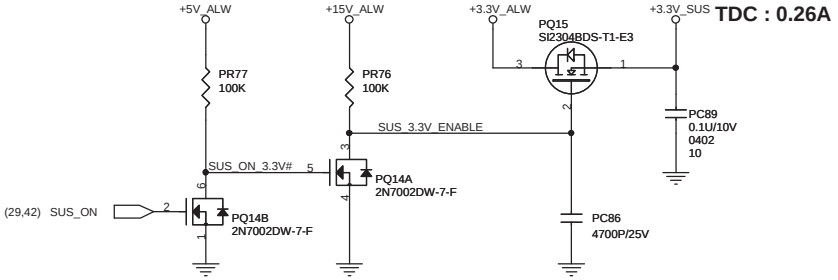


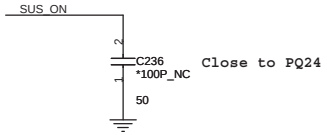
Title	+1.05V_VTT(RT8204C)	
Size	Document Number UM9 UMA	Rev 2A
Date: Monday, February 01, 2010	Sheet 44 of 51	

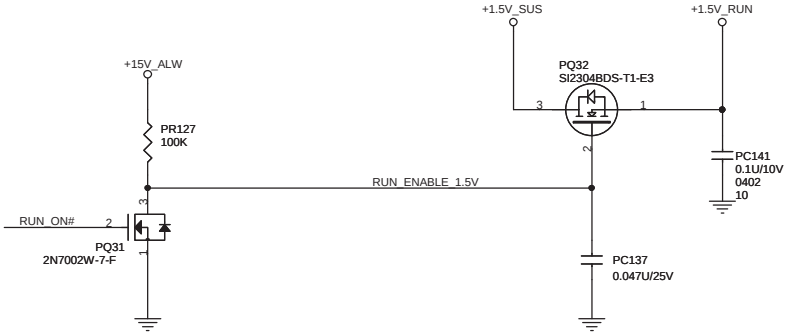


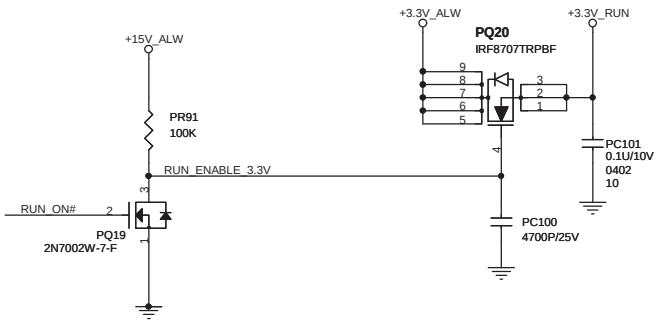
Title	CPU core (ADP3212MNR2G)	
Size	Document Number UM9 UMA	Rev 1A
Date: Monday, February 01, 2010	Sheet 45 of 51	



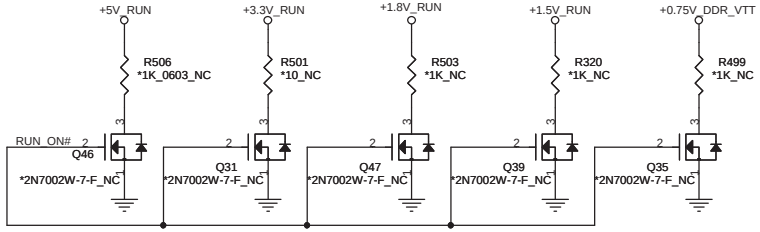


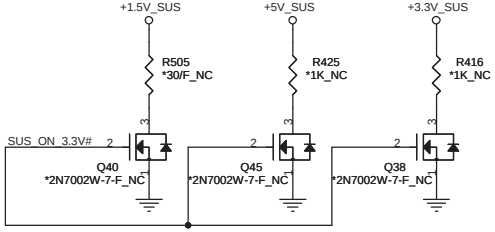






Reserve discharge path





QUANTA COMPUTER

Title	RUN / SUS POWER SW	
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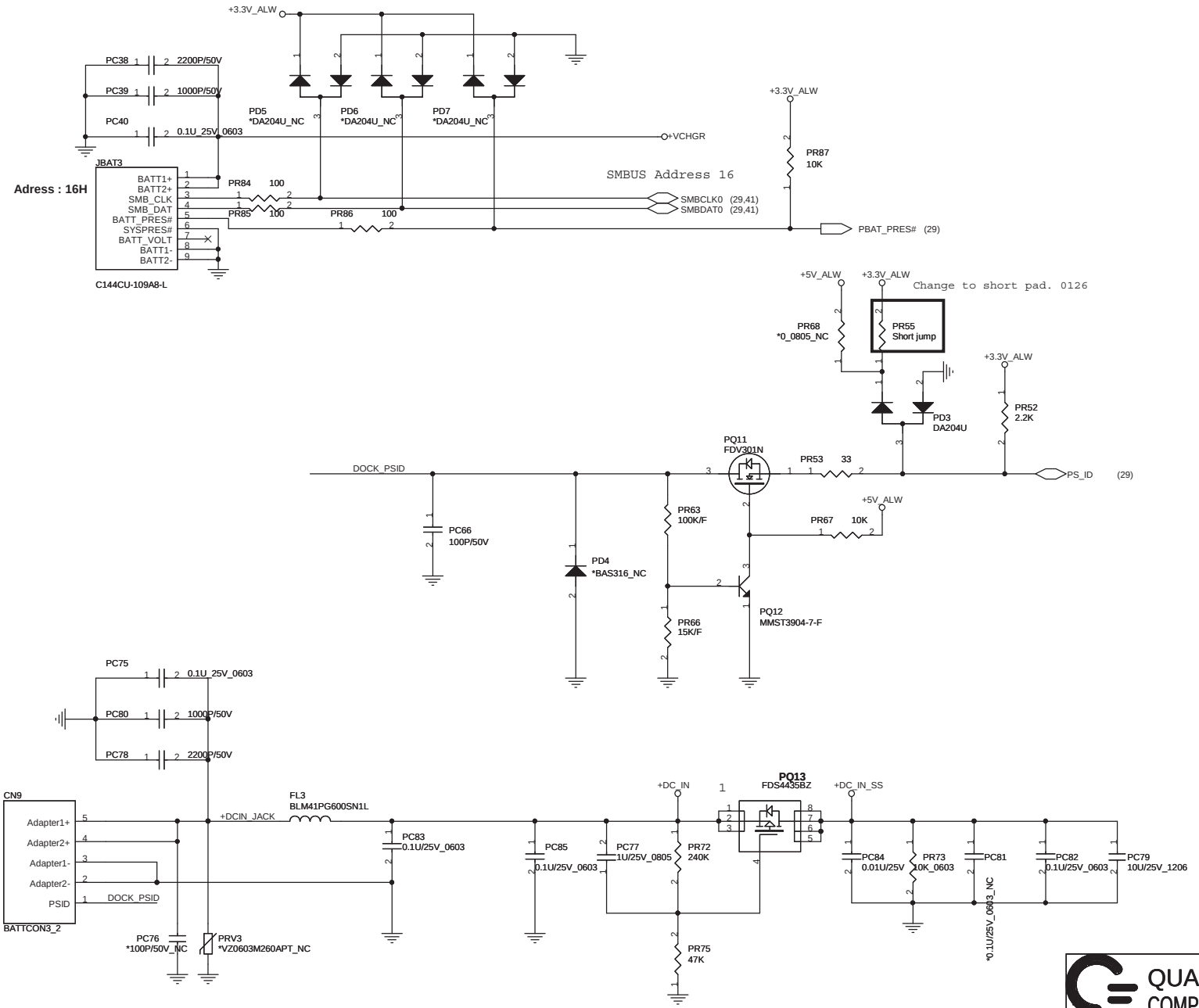

QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
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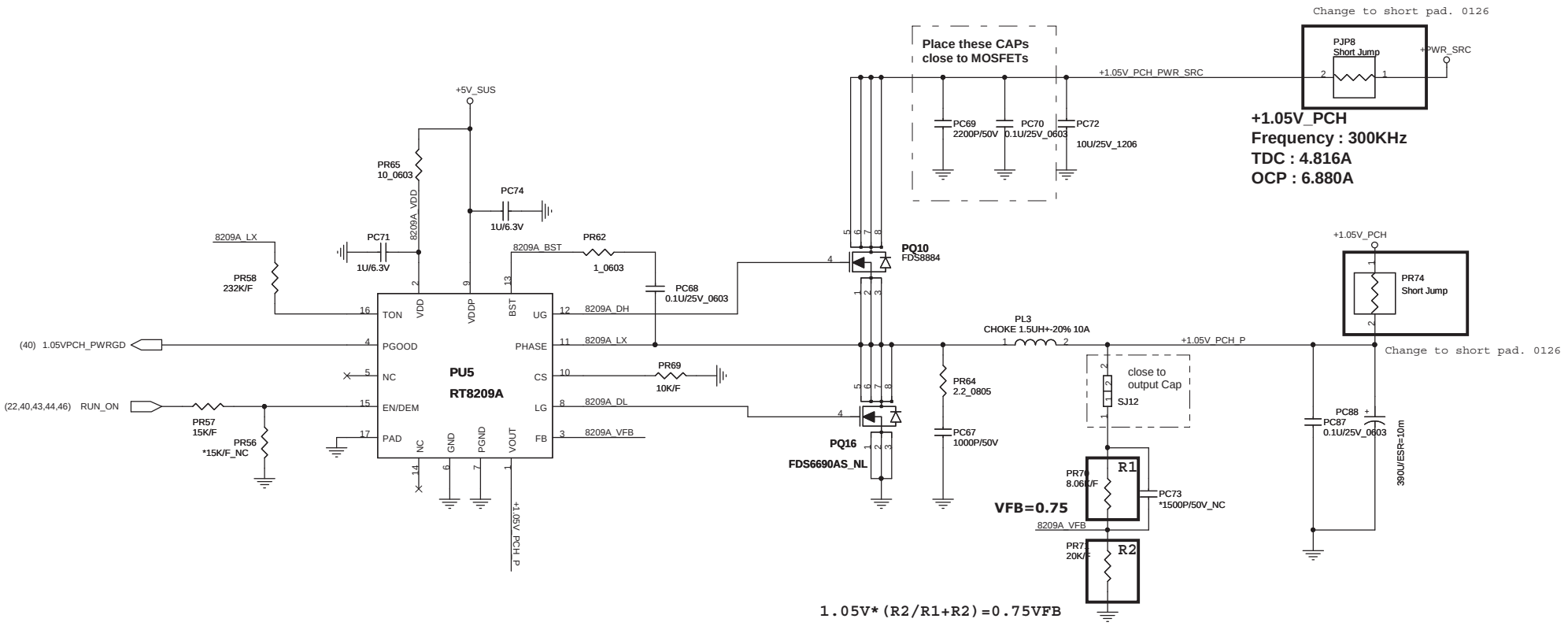

+1.05V_PCH
Control IC: RT8209A
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 1.5UH+-20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

Title	+1.05V_PCH(RT8209A)	
Size	Document Number UM9 UMA	Rev 2B
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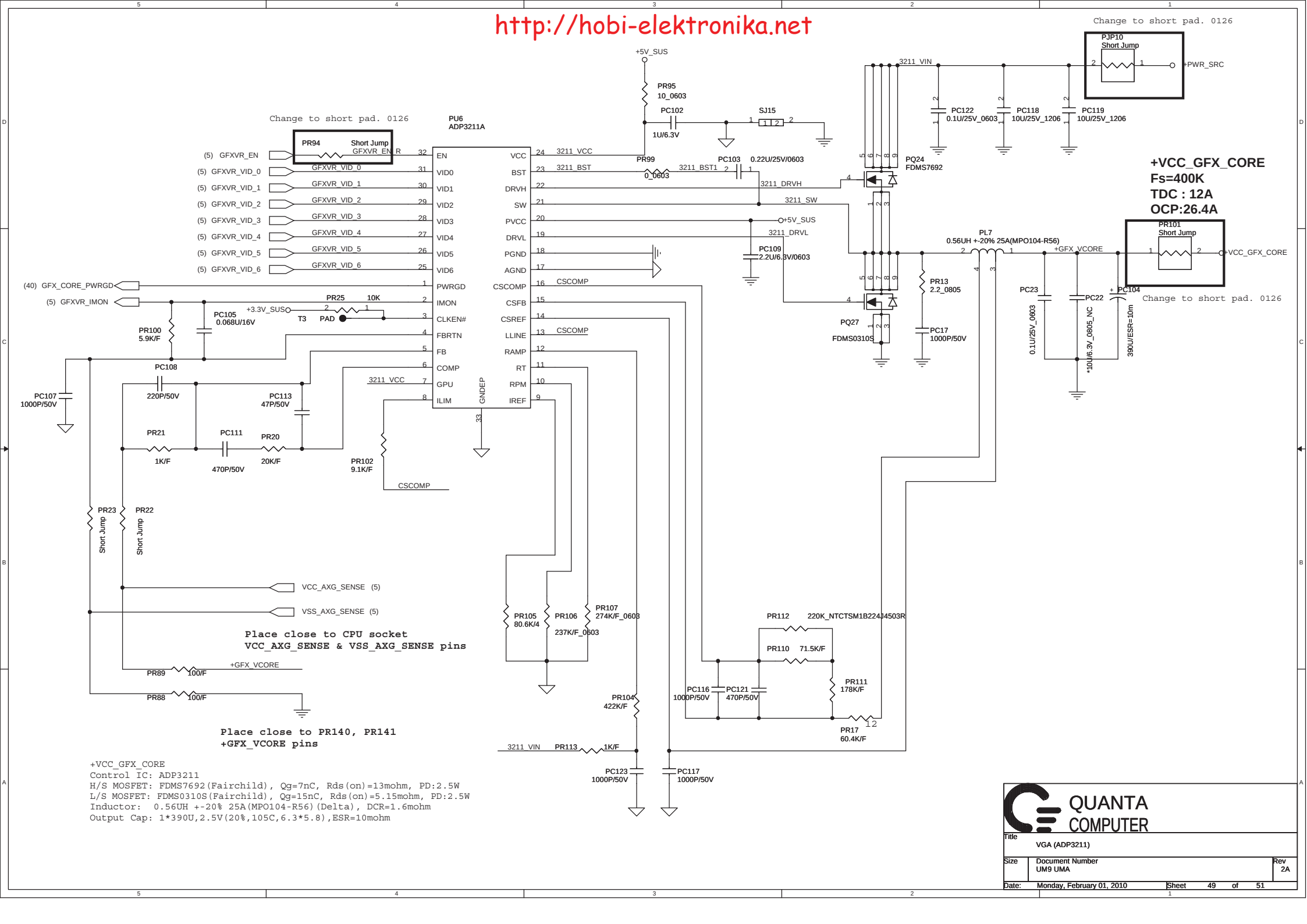

+VCC_GFX_CORE
Control IC: ADP3211
H/S MOSFET: FDMS7692(Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
Inductor: 0.56UH +-20% 25A(MPO104-R56)(Delta), DCR=1.6mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

QUANTA COMPUTER

Title	VGA (ADP3211)	
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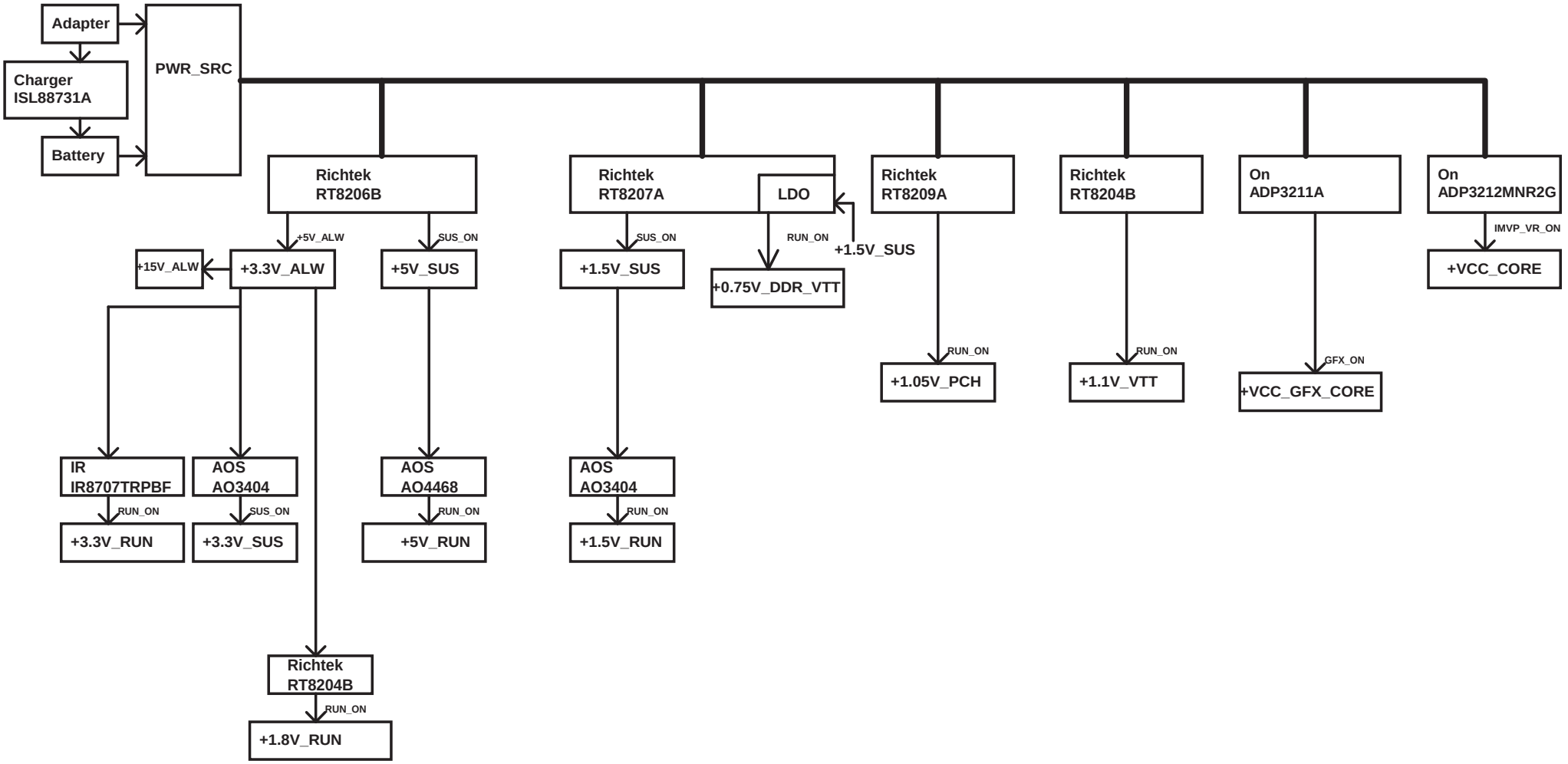

Quanta Computer Inc.

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FM9 Power Design Block Diagram 2009/02/25

(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

Power Jack
Adapter input
+DC_IN (1)
SI4835
+DC_IN_SS (1)
SI4835
+PWR_SRC (1)
Charger
ISL88731
Page 45
+VCHGR (1)
Battery
SI4835
+PWR_SRC (1)

+5V_VCC1 (from +5V_ALW2)
SYSTEM POWER
TPS51427A
Page 46
LDO
VR
+5V_ALW2 (1)
+3.3V_ALW (4)
+5V_ALW (4)
+3.3V_ALW_ON(From 3VALW ON POWER LOGIC) (3)
ALW_ON(For +5V_ALW and +15V_ALW turn on) (3)

(4) +5V_ALW
Diode & Cap
Page 46
+15V_ALW (4)
3V_ALW_PWRGD
5V_ALW_PWRGD

+5V_ALW
VRAM DDR3 POWER
TPS51116
Page 47
VR
LDO
+1.5V_SUS (6)
1.5V_DDR_PWRGD (6)
+0.75V_DDR_VTT (13)
(5) SUS_ON
(12) RUN_ON

+5V_ALW
PCH CORE POWER
TPS51218
Page 48
VR
+1.05V_PCH
1.05V_PWRGD (14)
(12) RUN_ON

(4) +5V_ALW
SI4800
Page 52
+5V_SUS (6)
(5) SUS_ON

(4) +3.3V_ALW
SI4800
Page 52
+3.3V_SUS (6)
(5) SUS_ON

(4) +5V_ALW
SI4800
Page 52
+5V_RUN (14)
(12) RUN_ON

(4) +3.3V_ALW
FDS8880
Page 52
+3.3V_RUN (14)
(12) RUN_ON

(14) +3.3V_RUN
SI2303
Page 17
+3.3V_DELAY (14)
(10) GFX_ON

(6) +1.5V_SUS
FDS6298
Page 52
+1.5V_RUN (14)
(12) RUN_ON

+5V_SUS
GFX CORE POWER
MAX8792ETD
Page 50
VR
+VCC_GFX_CORE
GFX_CORE_PWRGD (11)
(10) GFX_ON
(4) +5V_ALW

+5V_ALW (4)
GFX PCIE POWER
RT9018B
Page 50
VR
+1.1V_GFX_PCIE
GFX_PCIE_PWRGD (11)
(10) GFX_ON

+5V_ALW (4)
GFX POWER
RT9024PE
Page 44
VR
+1.8V_RUN_GFX
1.8V_RUN_GFX_PWRGD (14)
(12) RUN_ON

+5V_SUS
+3.3V_SUS
CPU CORE POWER
ISL6262A
TWO PHASE SOLUTION
Page 51
VR
+VCC_CORE
IMVP_PWRGD (17)
VR_PWRGD_CLKEN#
(16) IMVP_VR_ON

+5V_ALW (4)
CPU Memory Control & I/O Power
TPS51218
Page 49
VR
+1.1V_VTT
1.1V_VTT_PWRGD (14)
(12) RUN_ON

+5V_ALW (4)
CPU VCCPLL
RT9018B
Page 44
VR
+1.8V_RUN
1.8V_RUN_PWRGD (14)
(12) RUN_ON

(17) CK_PWRGD_R
CLK GEN
Page 15

Reset Circuit
Page 42
Inverter
AND Gate
Wire AND
AND Gate
(17) VR_PWRGD_CLKEN#
CK_PWRGD_R (17)
(6) 1.5V_DDR_PWRGD
(12) RUN_ON_1
RUN_ON (12)
(14) 1.1V_VTT_PWRGD
(14) 1.05V_PWRGD
(11) GFX_PCIE_PWRGD
(11) GFX_CORE_PWRGD
(14) 1.8V_RUN_PWRGD
(14) 1.8V_RUN_GFX_PWRGD
(17) IMVP_PWRGD
(18) RESET_OUT#
HWPG (15)
H_VTTPWRGD (15)
ICH_PWRGD (19)

(2) SYS_PWR_SW#
EC
IT8512
Page 29
3.3V_ALW_ON (3)
ALW_ON (3)
SUS_ON (5)
SIO_PWRBTN# (8)
ICH_RSMRST# (7)
SIO_SLP_S5# (9)
SIO_SLP_S3# (9)
(15) HWPG
RUN_ON_1 (12)
IMVP_VR_ON (16)
(17) IMVP_PWRGD
RESET_OUT# (18)

(19) ICH_PWRGD
PCH
Page 7~12
SIO_SLP_S4# (9)
To control DIMM VREF
PM_DRAM_PWRGD (20)
CLK_CPU_BCLK (21)
H_PWRGOOD (22)
PLTRST#(PCI_PLTRST#) (23)
(15) H_VTTPWRGD

CPU
Page 3~6

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