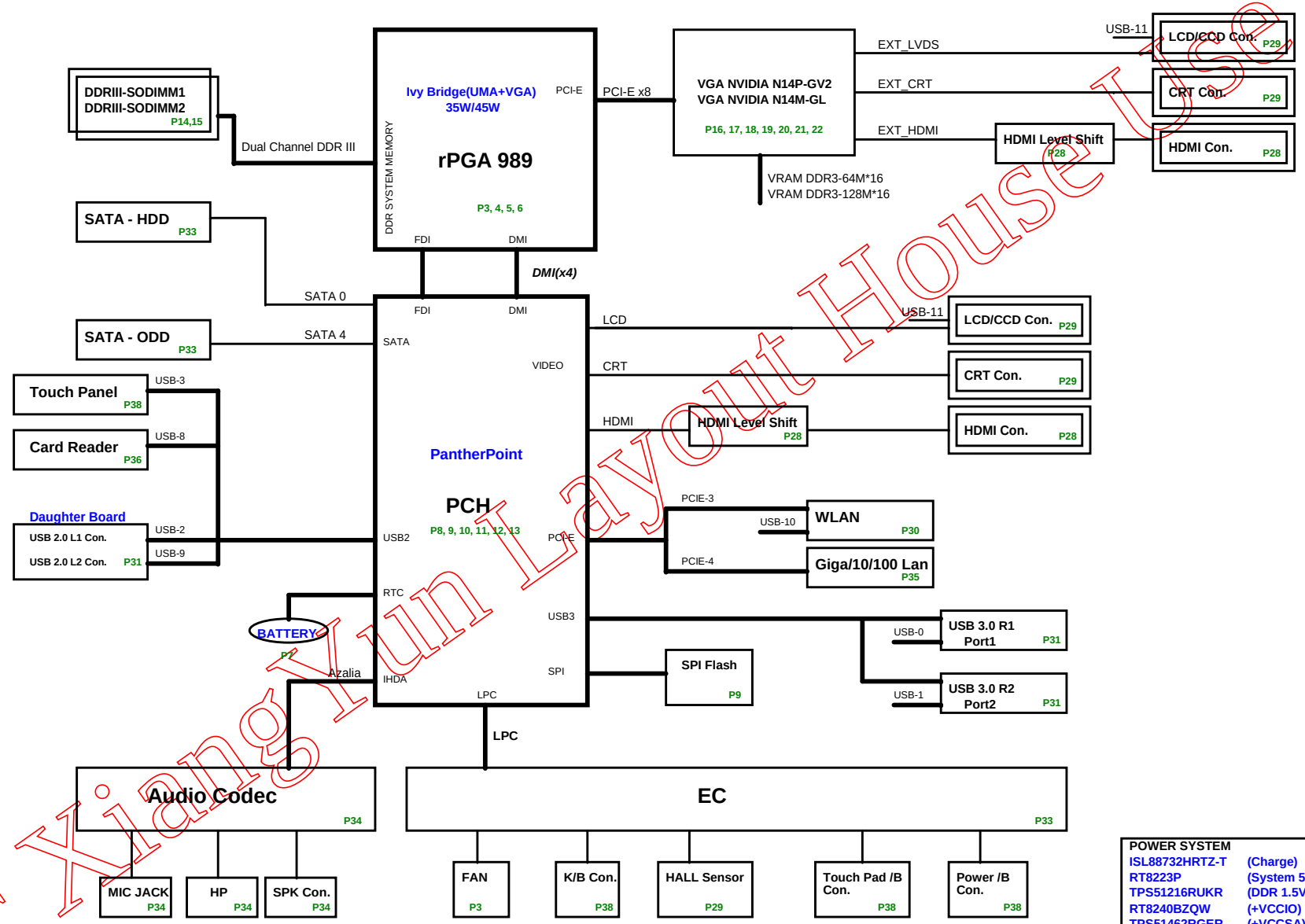
BD5 Block Diagram



POWER SYSTEM		
ISL88732HRTZ-T	(Charge)	P40
RT8223P	(System 5V/3V)	P41
TPS51216RUKR	(DDR 1.5V)	P42
RT8240BZQW	(+VCCIO)	P43
TPS51462RGER	(+VCCSA)	P44
ISL95836HRZ-T	(+VCC_CORE)	P45
G9661-25ADJF12U	(+1.8V)	P46
RT8812A	(NV_GPU_CORE)	P47
	(other GPU)	P48

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POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
+VIN	10V~+19V		S0~S5
+3V_RTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3VPCU	+3.3V	AC/DC Insert enable	S0~S5
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+1.5VSUS	+1.5V	S5_ON	S0~S3
+1.5V	+1.5V	MAIN_ON	S0
+VCCIO	+1.05V	MAIN_ON	S0
+VCCSA	~	HWPG_VCCIO	S0
+VCORE+VGFX	~	MPWROK	S0
+3V_GPU	+3.3V	DGPU_PWR_EN_R	S0
+VGPU_CORE	~	DGPU_PWR_EN_RC	S0
+1.5V_GPU	+1.5V	GPU_PWR_GD	S0
+1.05V_GPU	+1.05V	GPU_PWR_GD	S0

GND PLANE	PAGE
GND_SIGNAL	32
8769GND	37
GND	ALL
ADOGND	34

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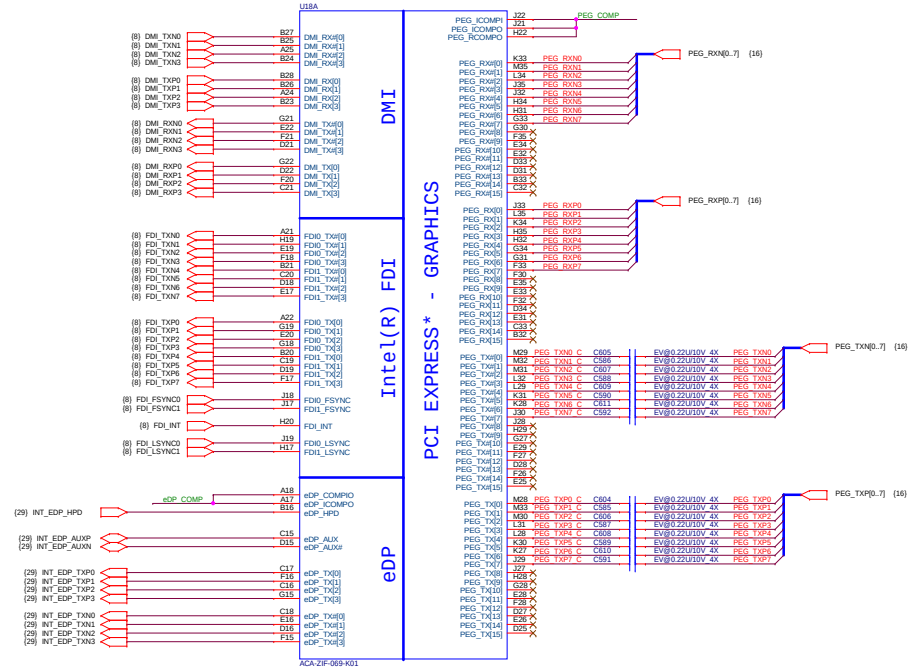
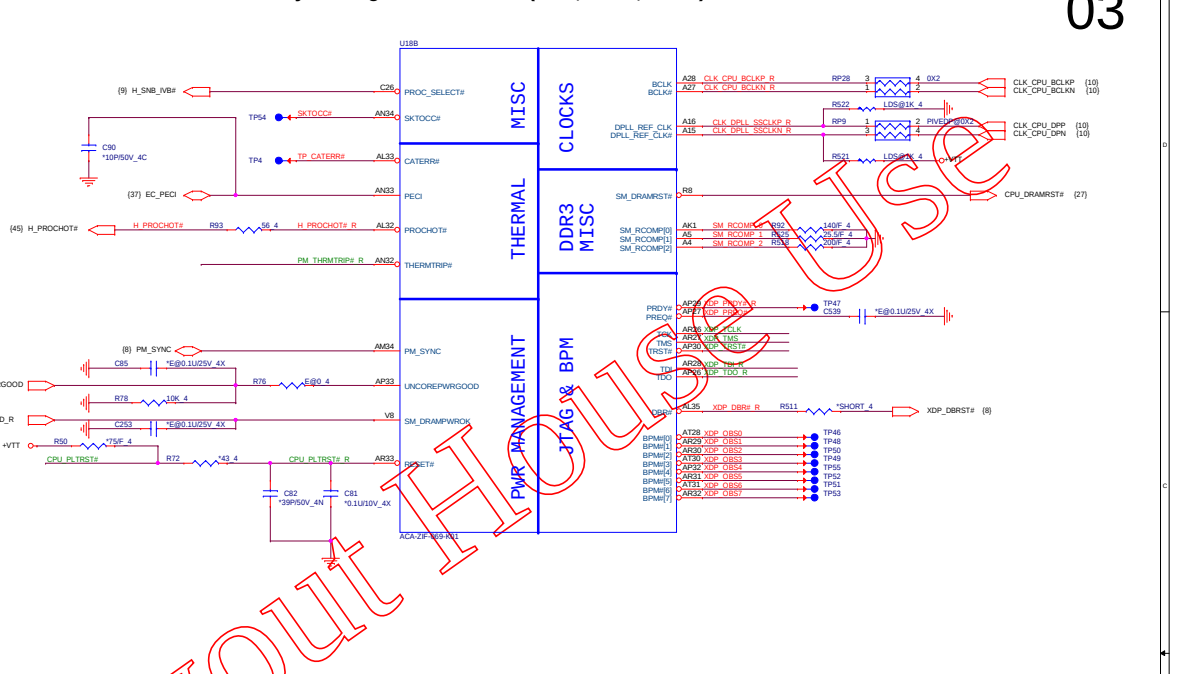
Ivy Bridge Processor (DMI,PEG,FDI) <CPU/VGA>

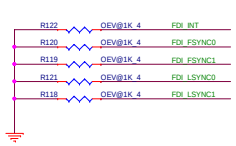


Ivy Bridge Processor (CLK,MISC,JTAG) <CPU>

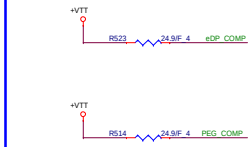


03

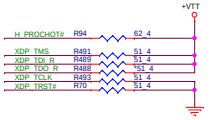
FDI Disabling (Discrete Only) <OEV>



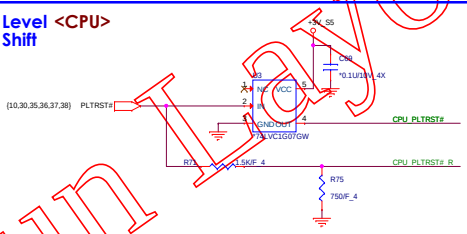
DP & PEG Compensation <CPU>



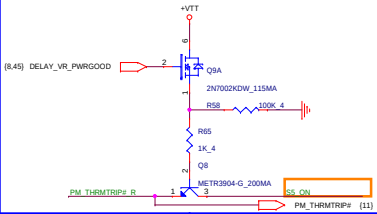
Processor pull-up <CPU>



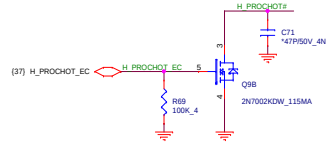
Level <CPU> Shift



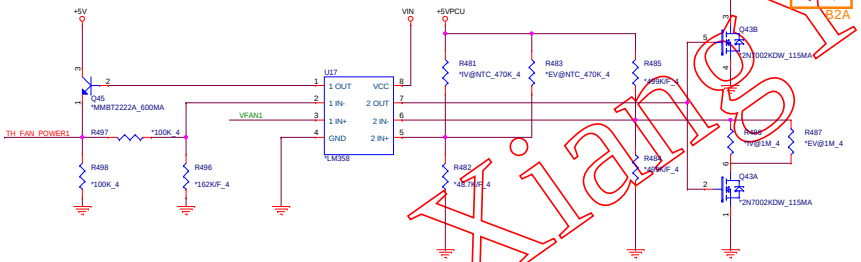
Thermal Trip & Process HOT <CPU>



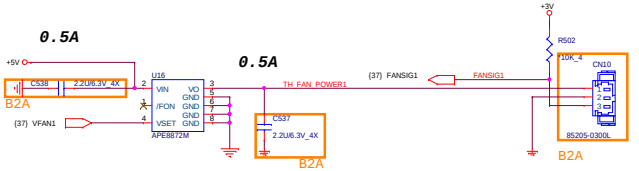
Intel Turbo mode only <CPU>



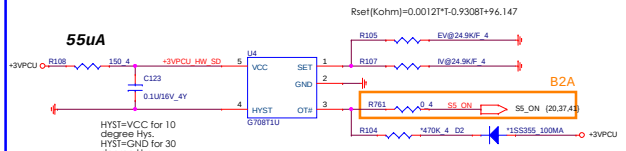
<THC>



FAN Control-->For one FAN solution <THC>



CPU Thermal sensor / MB Local TEMP <THP/UGA/VGA>



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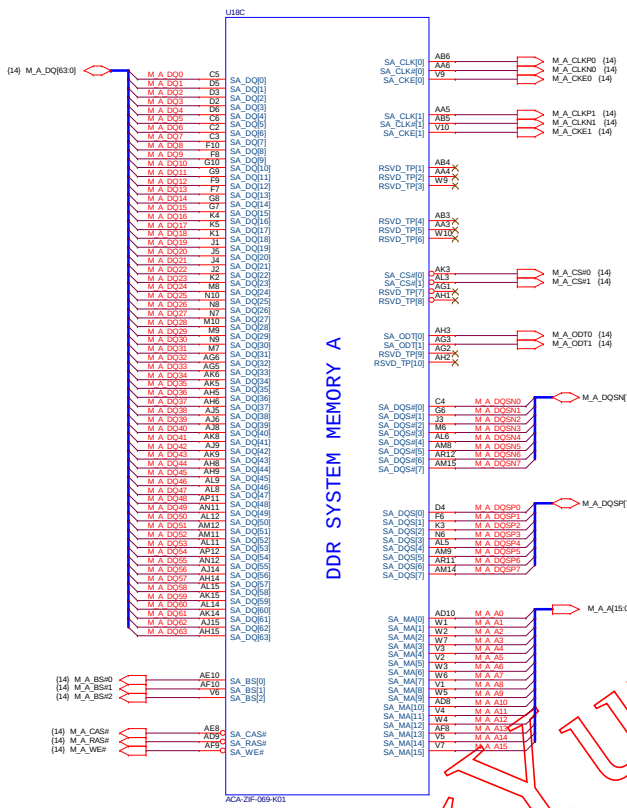
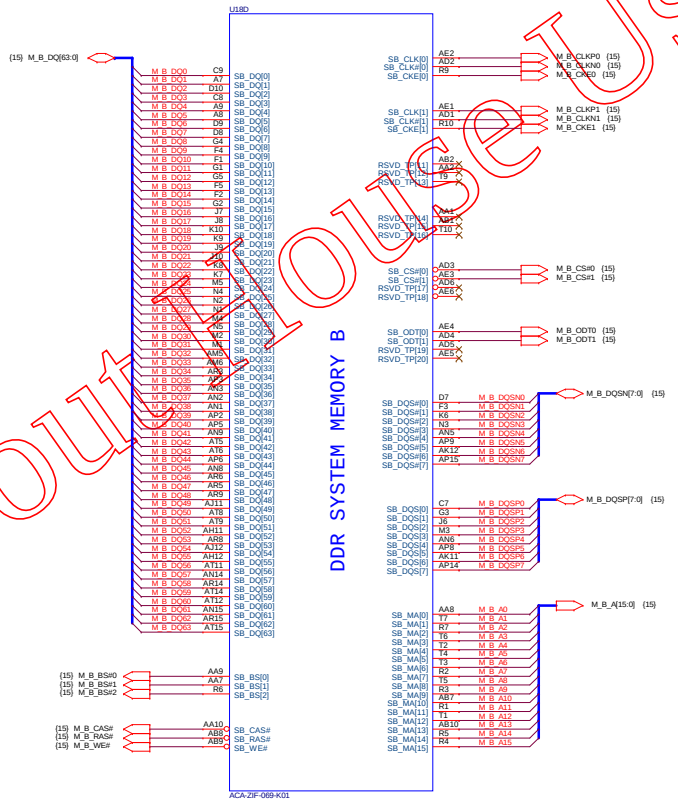
Ivy Bridge Processor (DDR3) <CPU>





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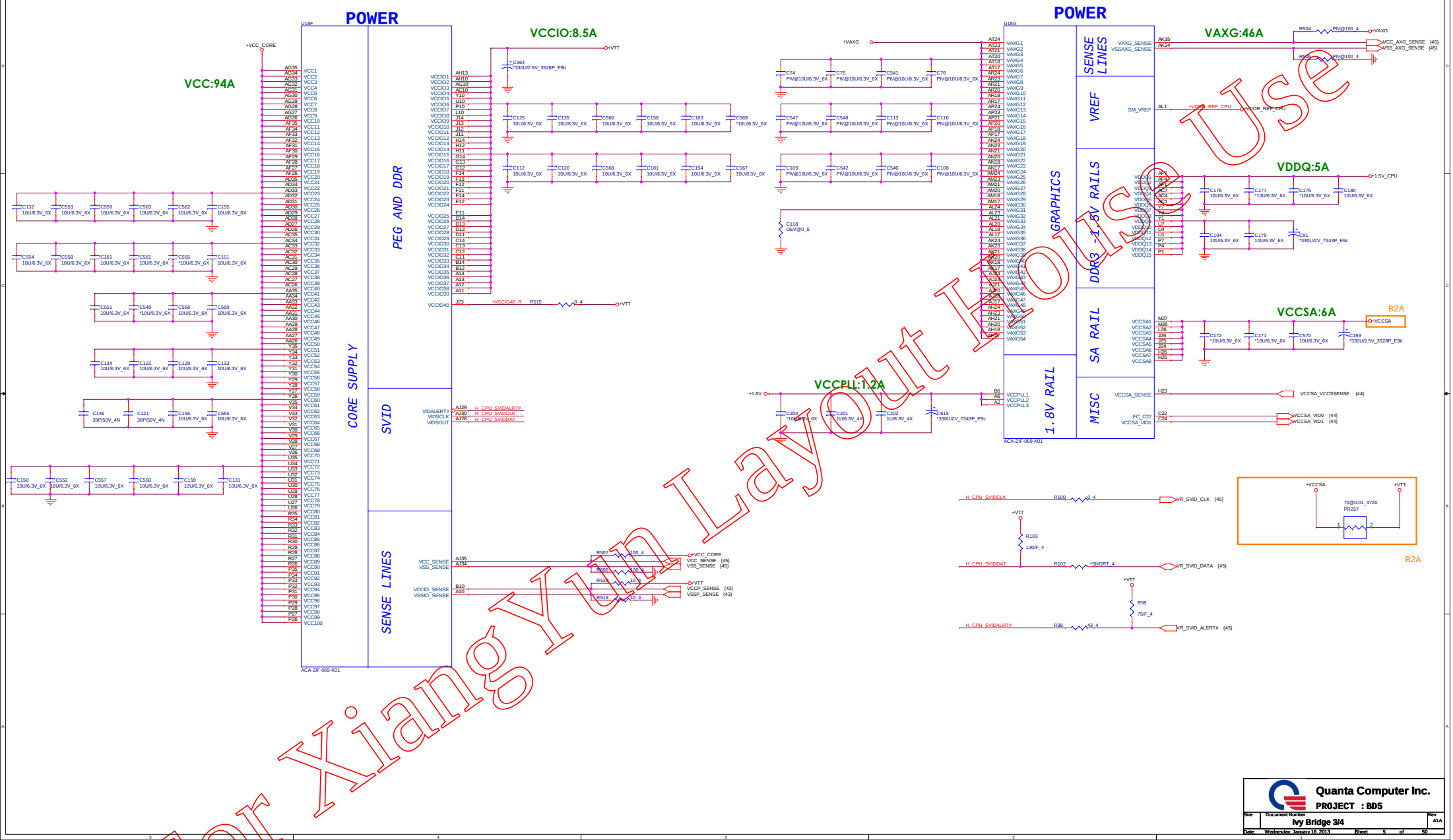
Ivy Bridge Processor (POWER) <CPU>

Ivy Bridge Processor (GRAPHIC POWER) <CPU/OEV/PIV>



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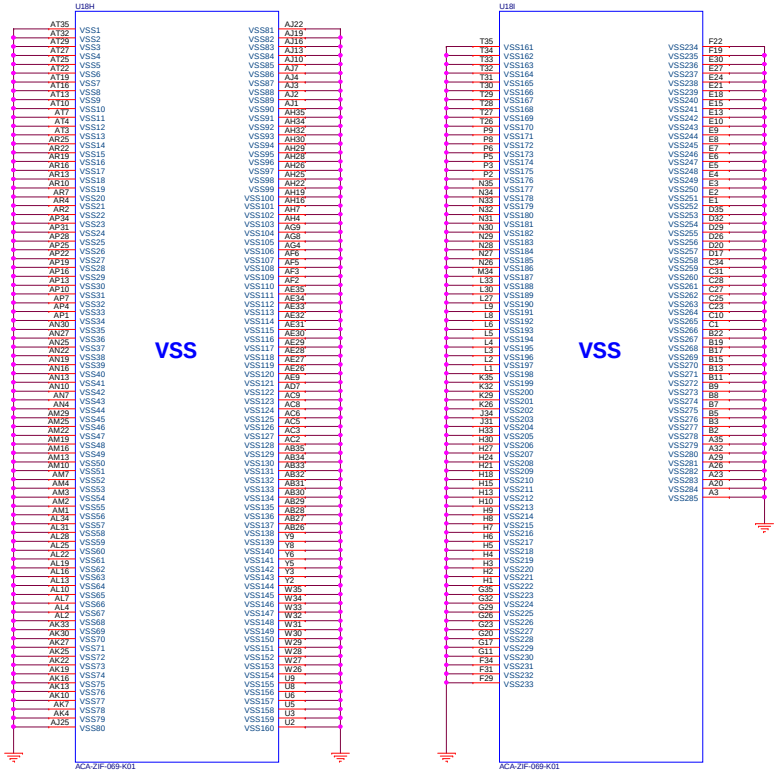
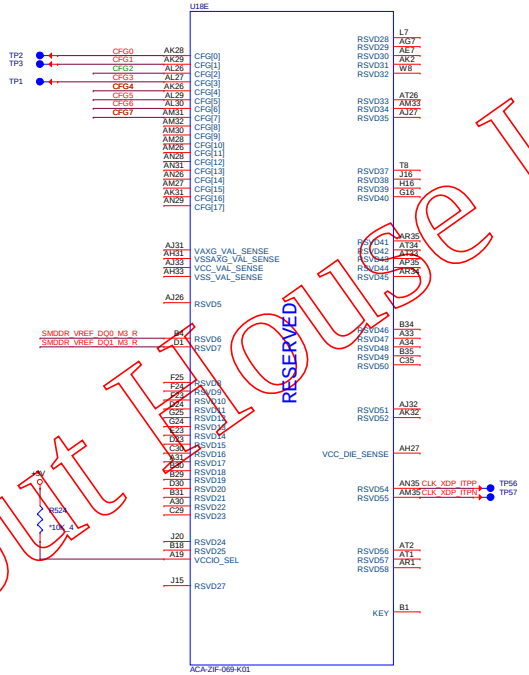
Ivy Bridge Processor (GND) <CPU>

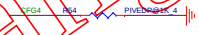
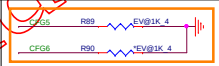
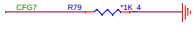


Ivy Bridge Processor (RESERVED, CFG) <CPU>



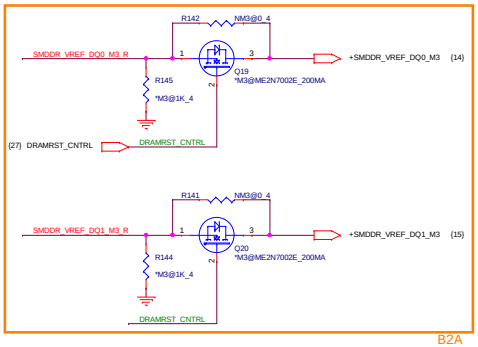
Processor Strapping CPU/VGA

The CFG signals have a default value of '1' if not terminated on the board.

Pin Name	Configuration	
CFG2 (PEG Static Lane Reversal --> 16 Lane)	1=Normal Operation 0=Lane Reversed	
CFG3 (Reserved)		
CFG4 (DP Presence Strap)	1=Disable; No physical DP attached to eDP 0=Enable; An ext DP device is connected to eDP	
CFG5 CFG6 (PCIE Bifurction)	00=x8,x4,x4 - Device 1 function 1 and 2 enable 01=Reserved - (Device 1 function 1 disable ; function 2 enable) 10=x8,x8 -Device 1 function 1 enable ; function 2 enable 11=(Default) x16 -Device 1 function 1 and 2 disable	
CFG7 (PEG Defer Training)	1=PEG train immediately following xxRESETB de assertion 0=PEG wait for BIOS training	

B2A

DDR3 VREF DQ (M3) S3P



B2A

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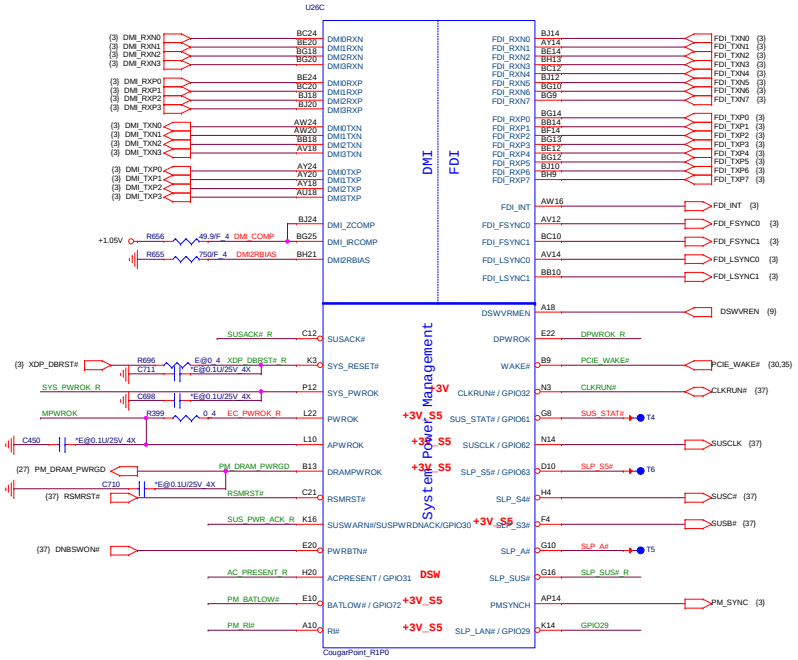
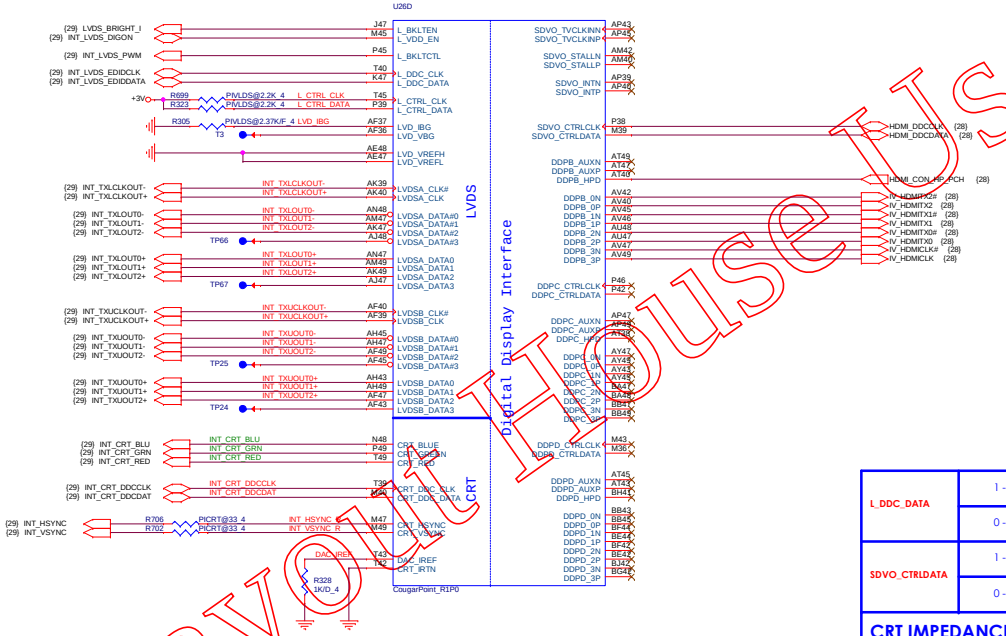
Panther Point (DMI,FDI,PM) <CLG>

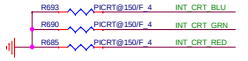


Panther Point (LVDS,DDI) <CLG/UGA/HMG>

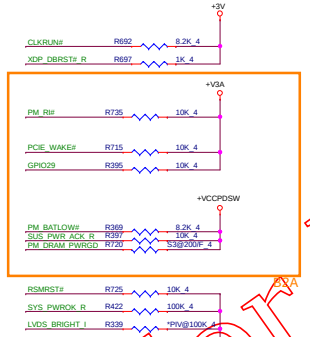


L_DDC_DATA	1 -- LVDS ENABLE
	0 -- LVDS DISABLE
SDVO_CTRLDATA	1 -- PORT B Detected
	0 -- PORT B Disable

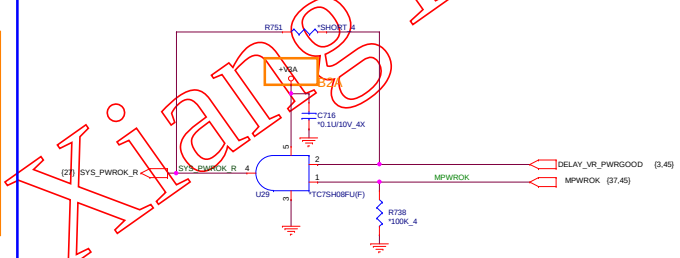
CRT IMPEDANCE MATCHING <CLG>



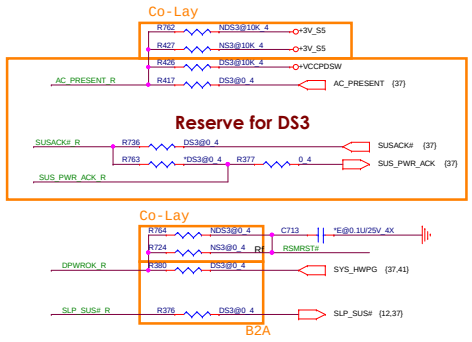
PCH Pull-high/low <CLG>



System PWR_OK <CLG>



Deep Sx <CLG>



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	V	NA
SUS_PWR_ACK	V	NA
SUSACK#_R	V	V
DPWROK	V	NA
SLP_SUS	V	NA

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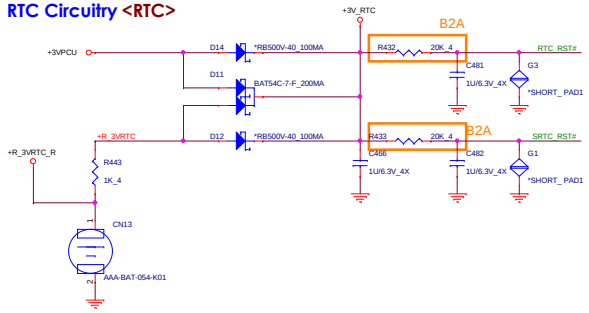
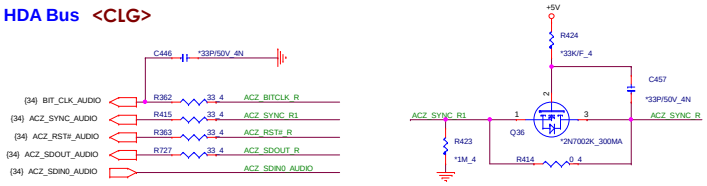
RTC Circuitry <RTC>

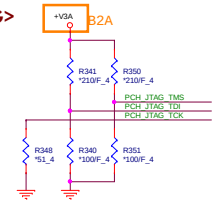


PU & Password Clear <CLG>

HDA Bus <CLG>

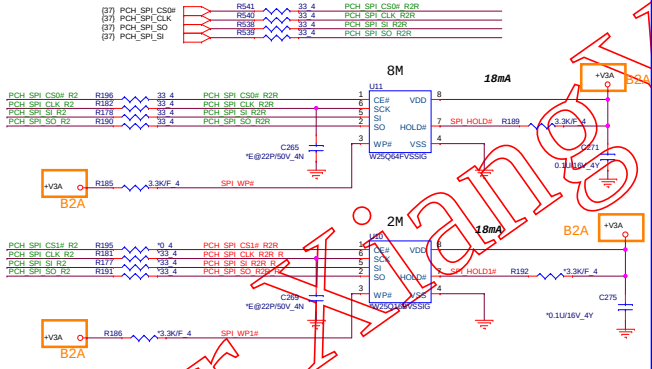


PCH JTAG Debug<CLG>

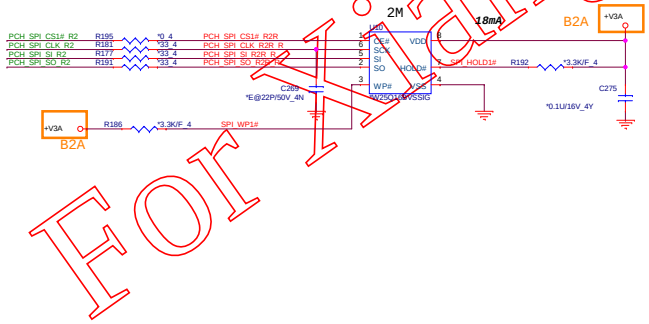


PCH Dual SPI <CLG>

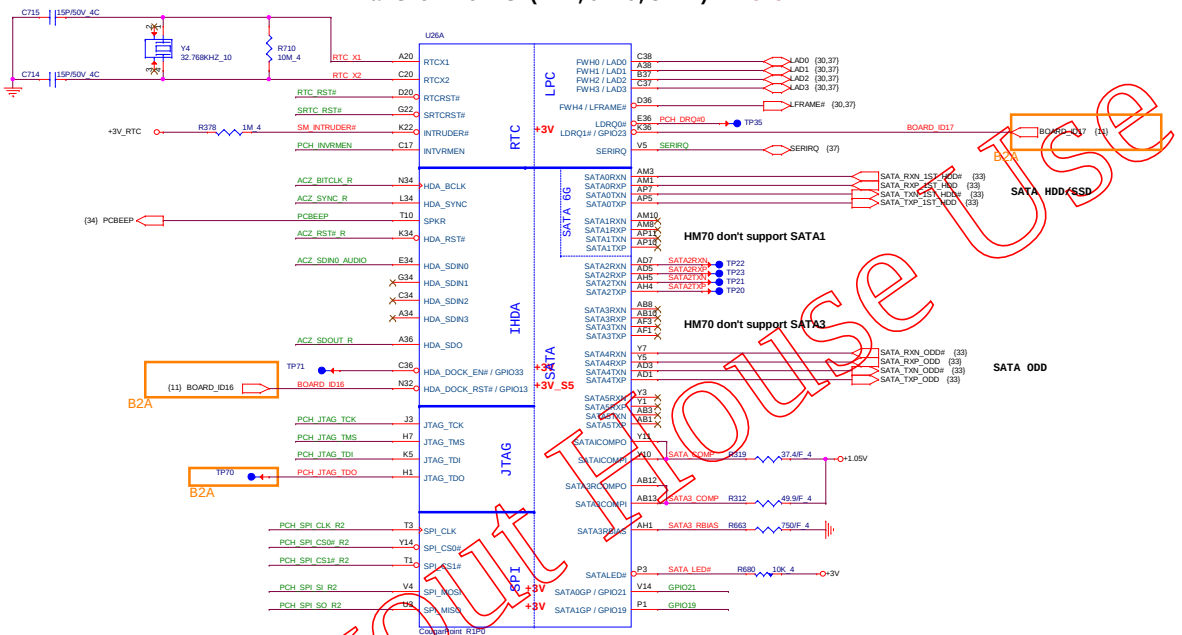
EC+BIOS @4M



ME@2M

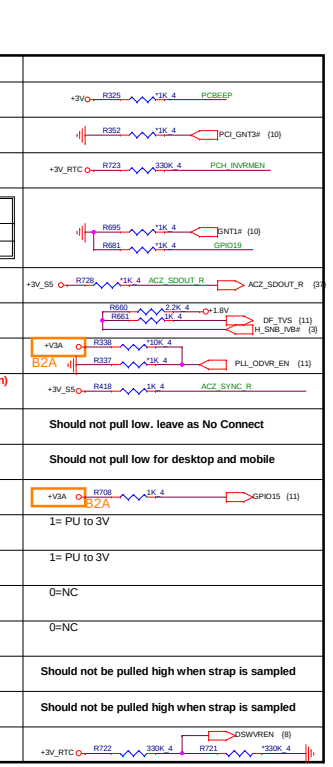


Panther Point (HDA,JTAG,SATA) <CLG>



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)
GNT2#/ GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected
SATA3GP/ GPIO37	Reserved	PWROK	0 = Default
SATA2GP/ GPIO36	Reserved	PWROK	0 = Default
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable



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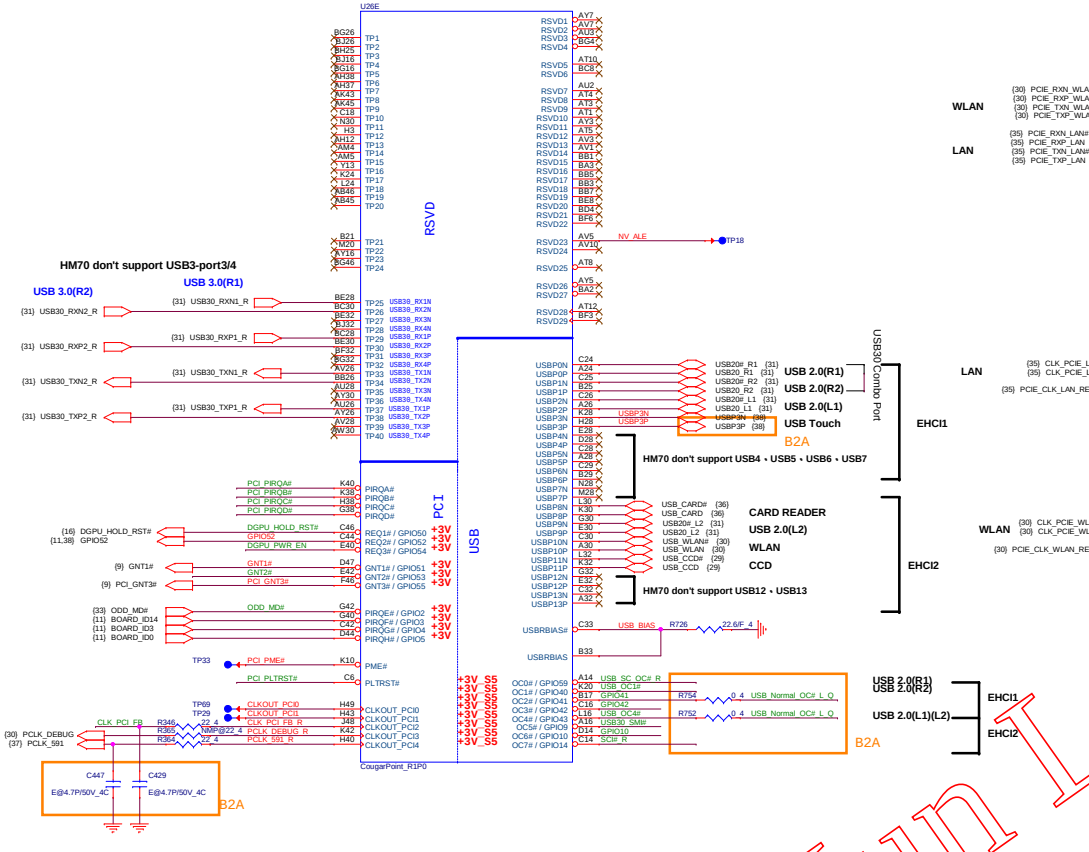
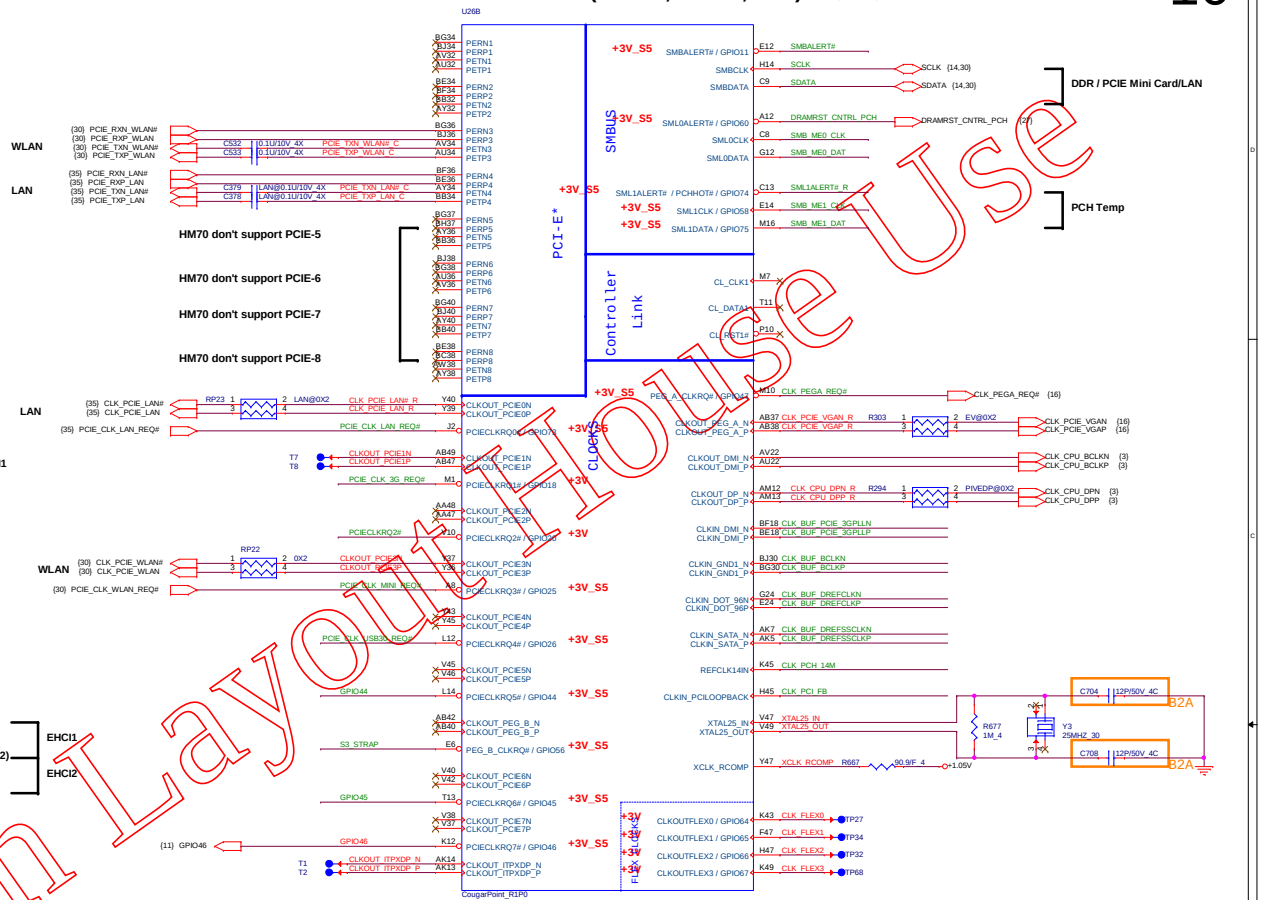
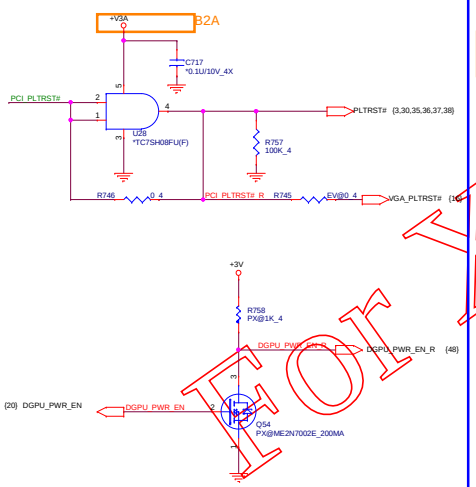
Panther Point-M (PCI,USB,NVRAM) <CLG>



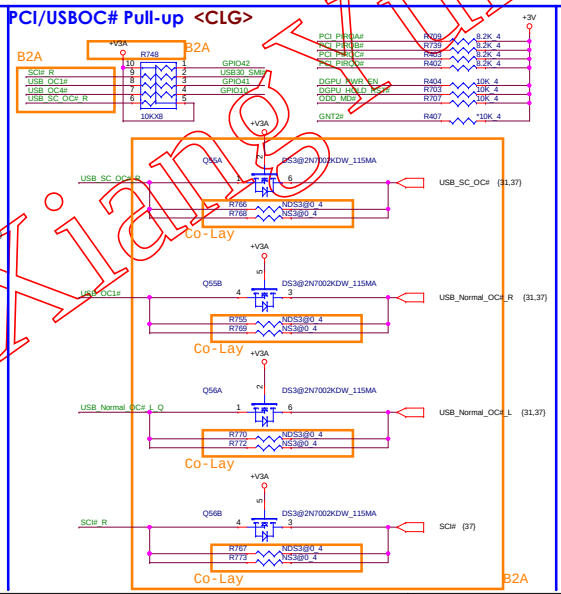
Panther Point-M (PCI-E,SMBUS,CLK) <CLG,U3B,MNW>



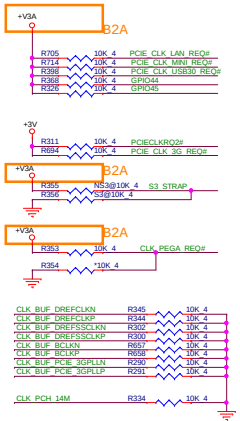
PLTRST# <CLG,VGA>



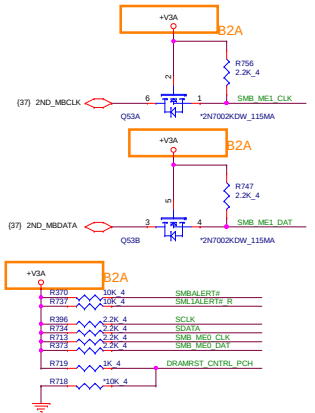
PCI/USBOC# Pull-up <CLG>



CLK_REQ/Strap Pin <CLG,VGA>



SMBus/Pull-up <CLG>



	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●	●	●	●
CLK_FLEX3		●	●	●	

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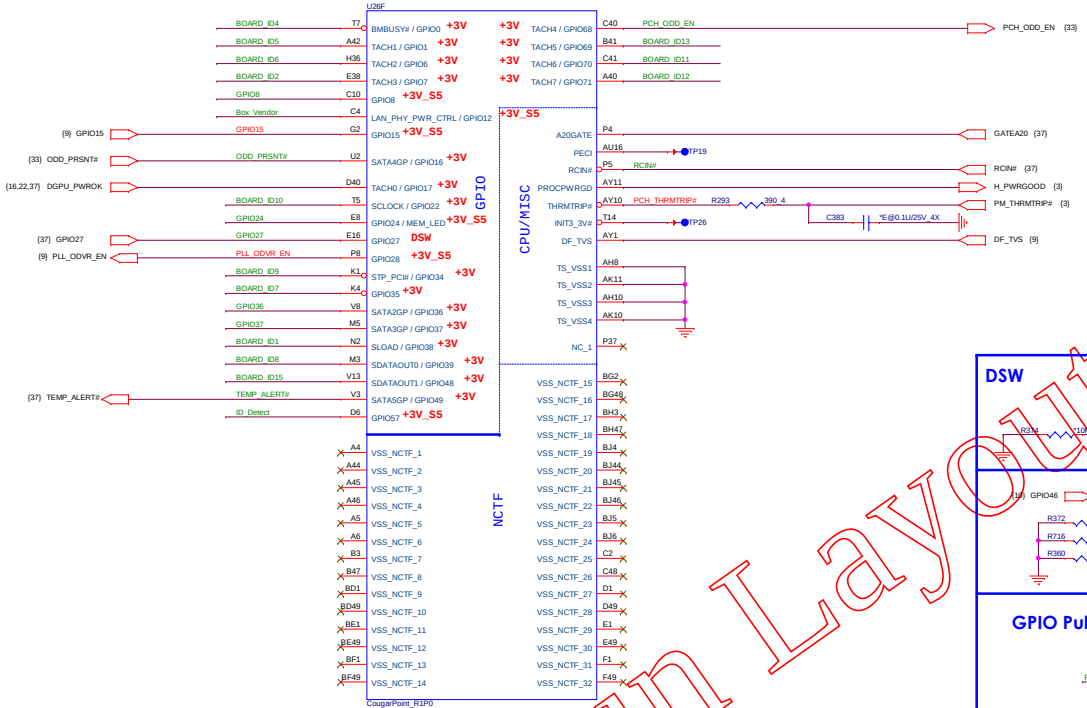
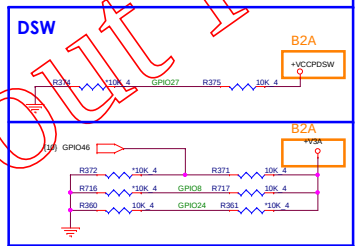
Panther Point (GPIO,VSS_NCTF,RSVD) <CLG>



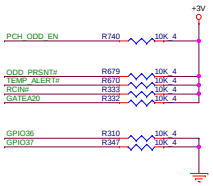
BOARD ID SETTING <CLG>

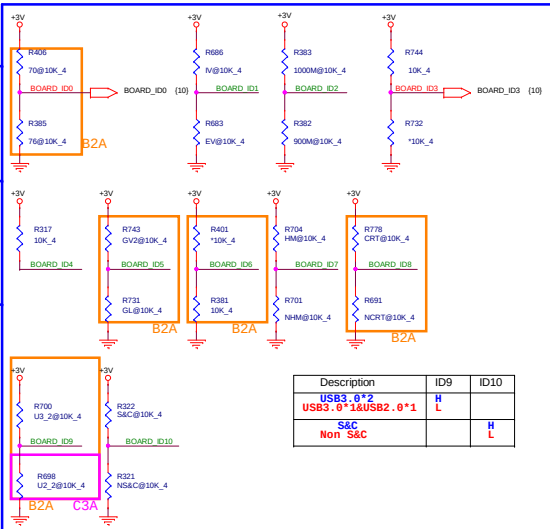
Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID12	ID13	ID14	ID15	ID16	ID17
HM70 HM76	H L														
UMA SKU VGA SKU		H L													
VRAM-1000MHz VRAM-900MHz			H L												
Standard ULV				H L											
17" 14"					H L										
GV2 GL						H L									
W/ 4K2K W/O 4K2K							H L								
W/ HDMI W/O HDMI								H L							
W/ CRT W/O CRT									H L						
Only VGA Optimus										H L					
WIN7 WIN8											H L				
HM75_76 NM70												H L			
EDP LVDS													H L		
Celeron 1.37G_17														H L	
45W 35W															H L

DSW

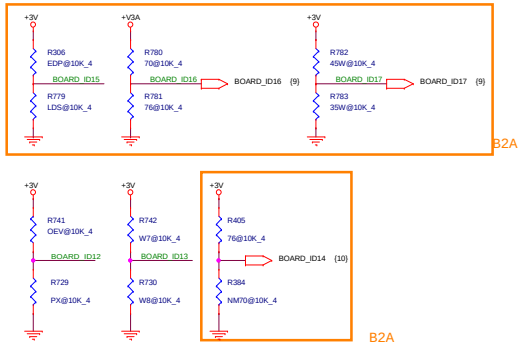


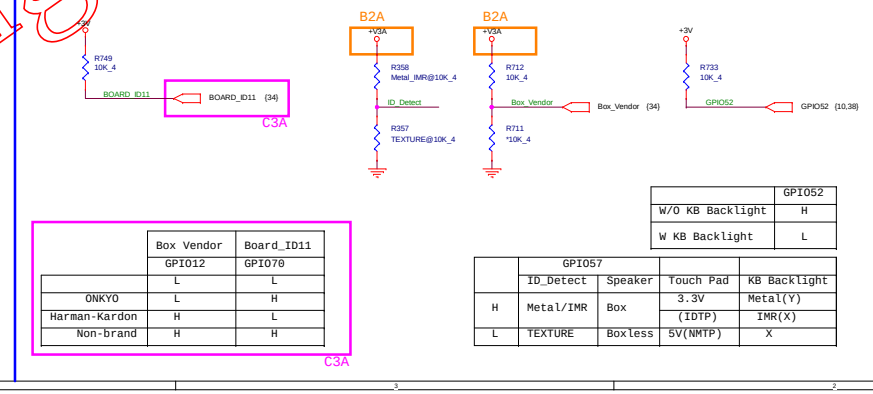
GPIO Pull-up/Pull-down <CLG>





Description	ID9	ID10
USB3.0*2 USB3.0*1&USB2.0*1	H L	
S&C Non S&C		H L





	Box Vendor	Board_ID11
	GPIO12	GPIO70
	L	L
ONKYO	L	H
Harman-Kardon	H	L
Non-brand	H	H

	GPIO52
W/O KB Backlight	H
W KB Backlight	L

	GPIO57			
	ID_Detect	Speaker	Touch Pad	KB Backlight
H	Metal/IMR	Box	3.3V	Metal(Y)
			(IDTP)	IMR(X)
L	TEXTURE	Boxless	5V(NMTP)	X

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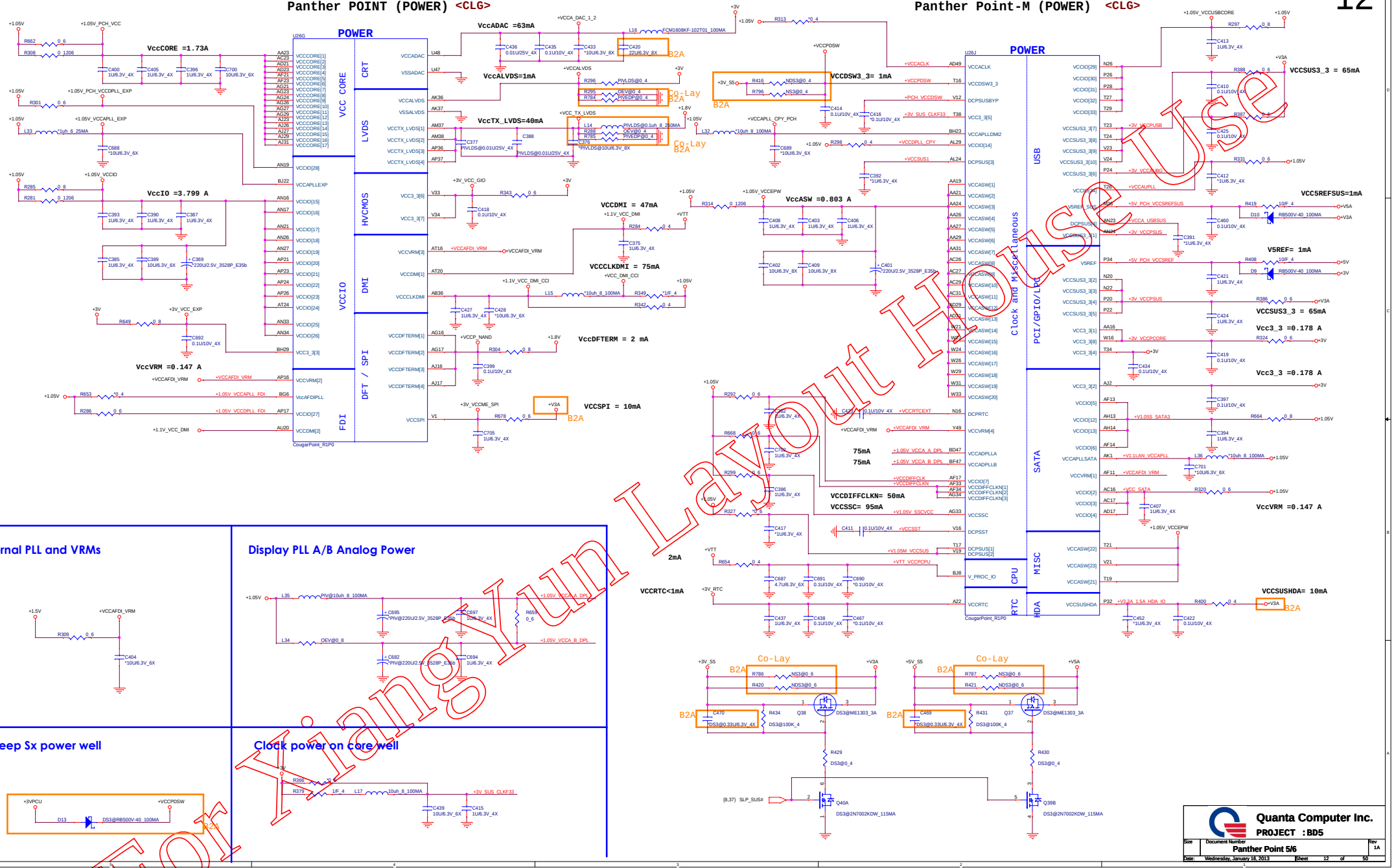
Panther POINT (POWER) <CLG>

Panther Point-M (POWER) <CLG>



Internal PLL and VRMs

Display PLL A/B Analog Power

Deep Sx power well

Clock power on core well

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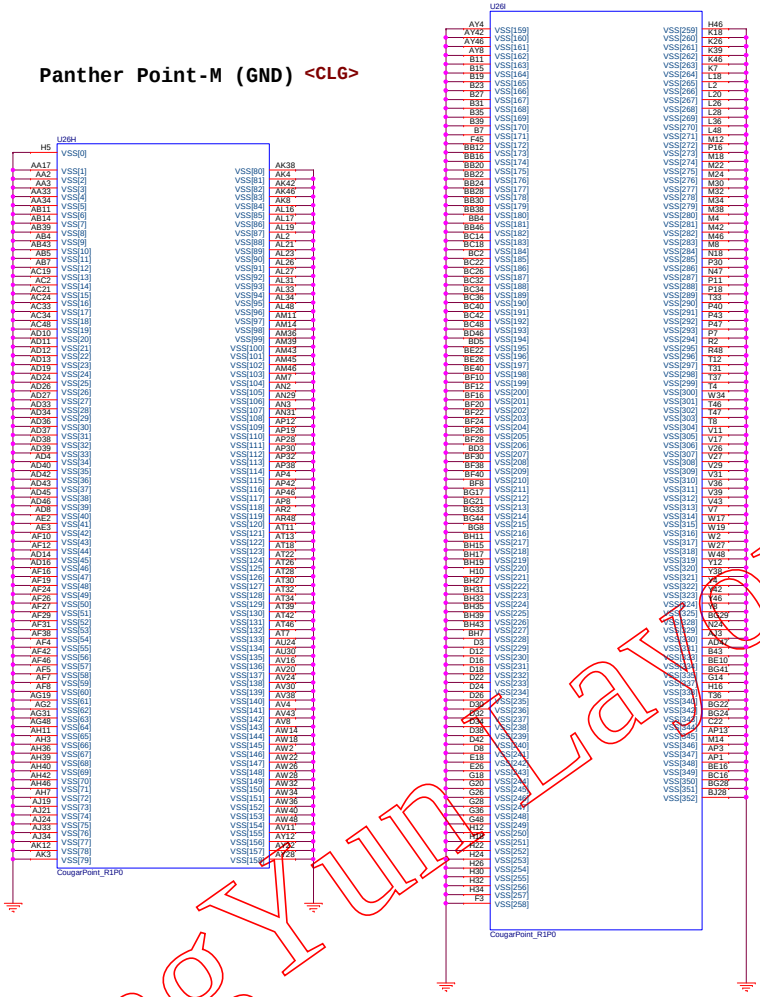
Panther Point-M (GND) <CLG>



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	Panther Point 6/6	1A

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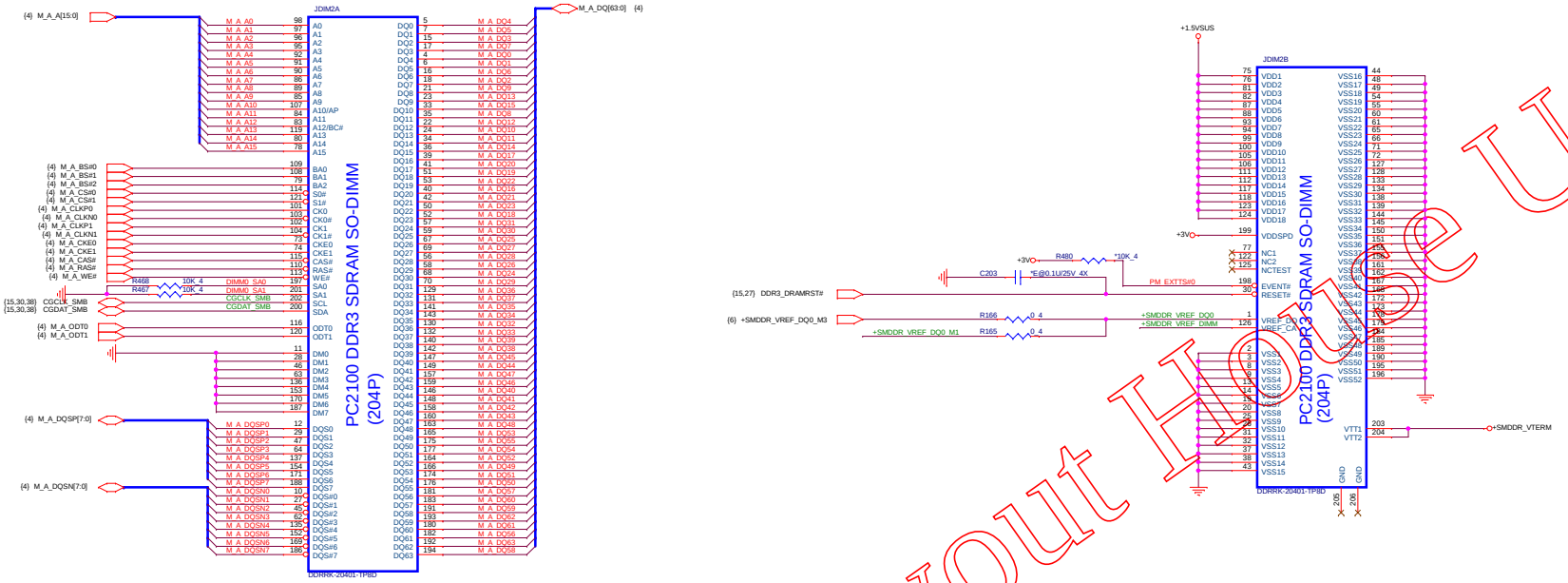
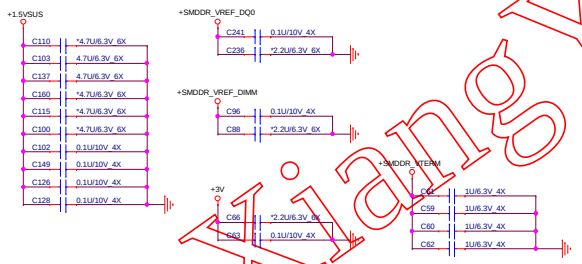
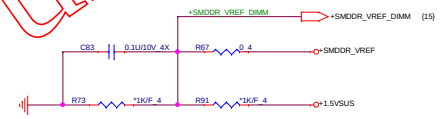
H=8 (Rev)



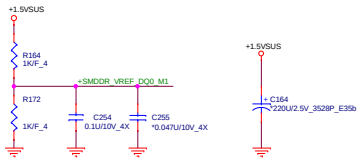
DDR Power Decoupling <DDR>



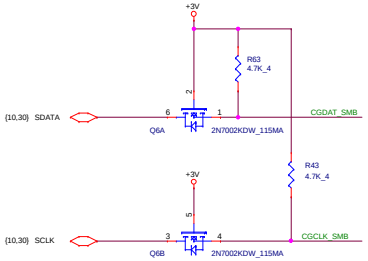
DDR3 VREF CA <DDR>



DDR3 VREF DQ (M1) <DDR>



SMBUS ISOLATE



Quanta Computer Inc.		
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Size	Document Number	Rev
	DDR3 DIMM-0	1A
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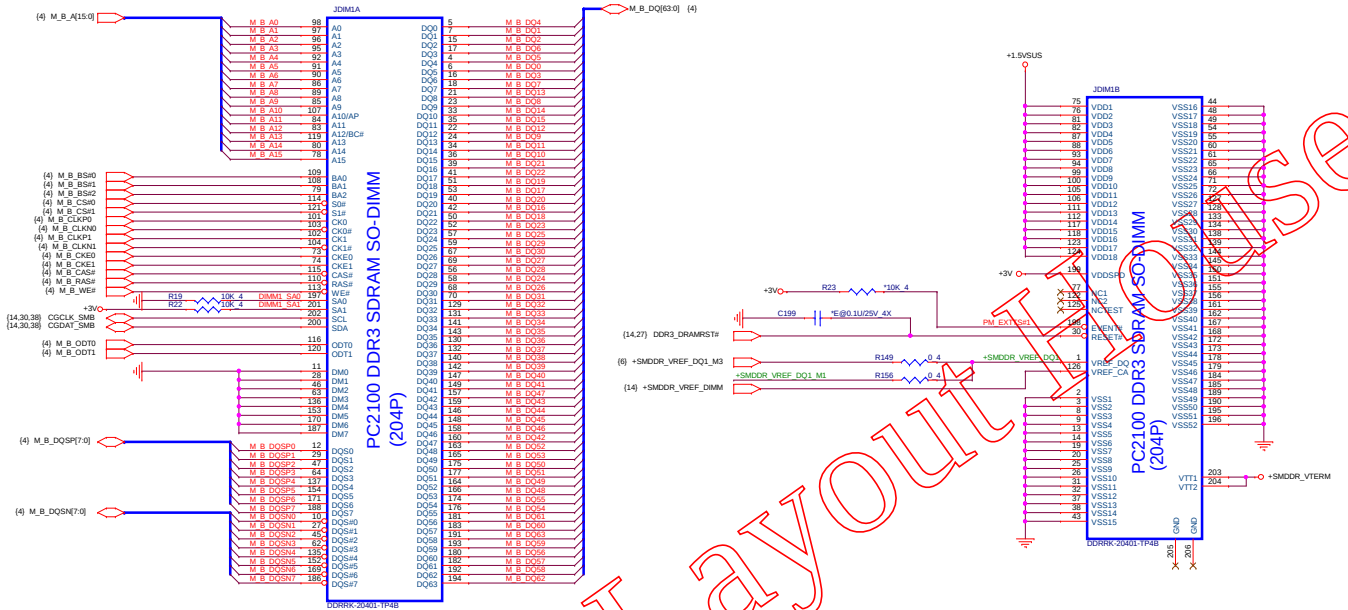
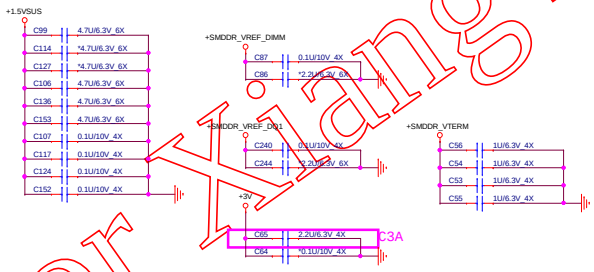
<DDR>

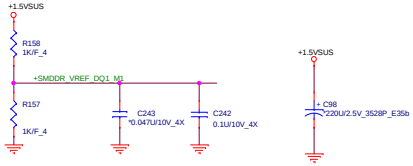
H=4 (Rev)



<DDR> DDR Power Decoupling



DDR3 VREF DQ (M1) <DDR>



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	DDR3 DIMM-1	1A

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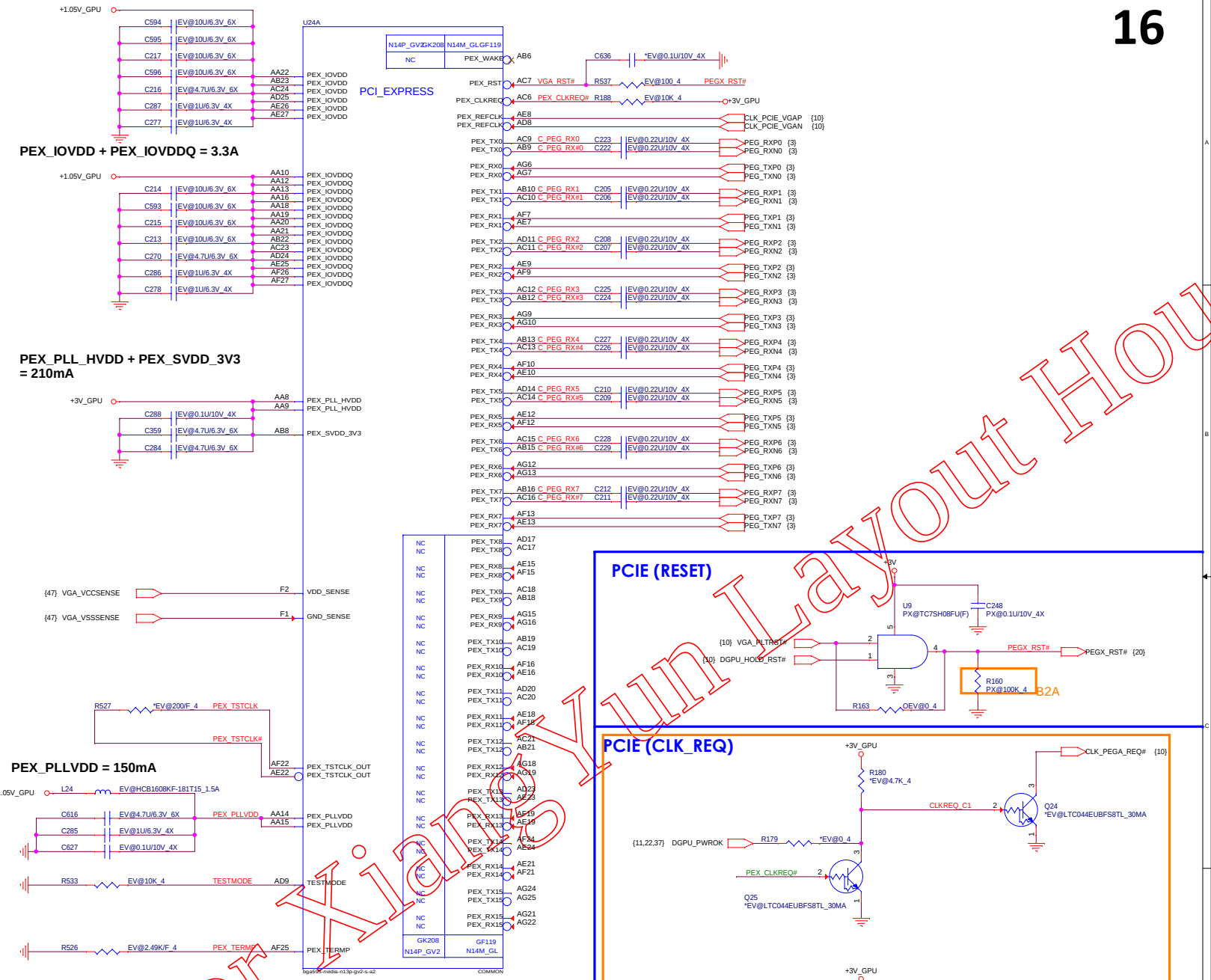

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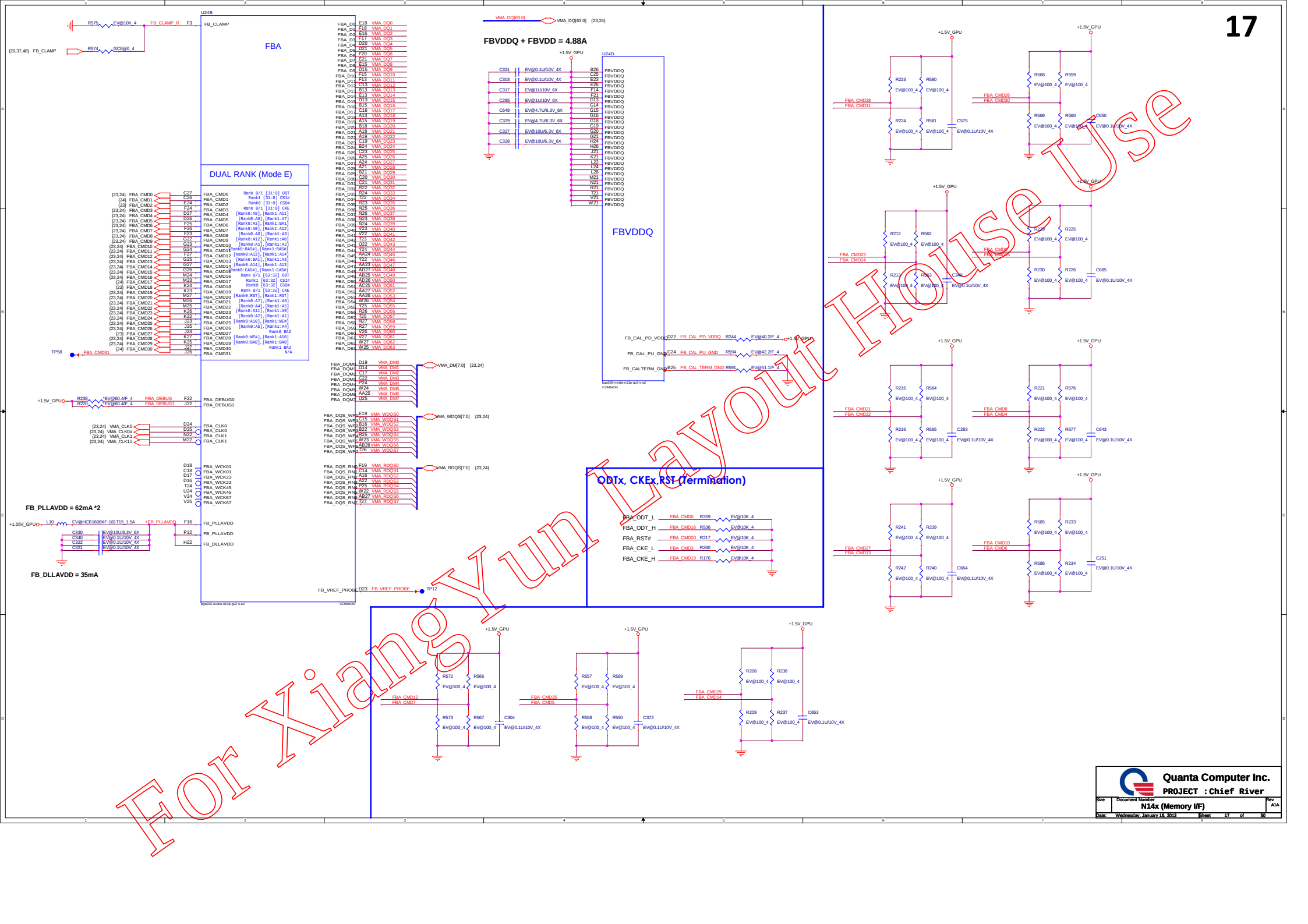

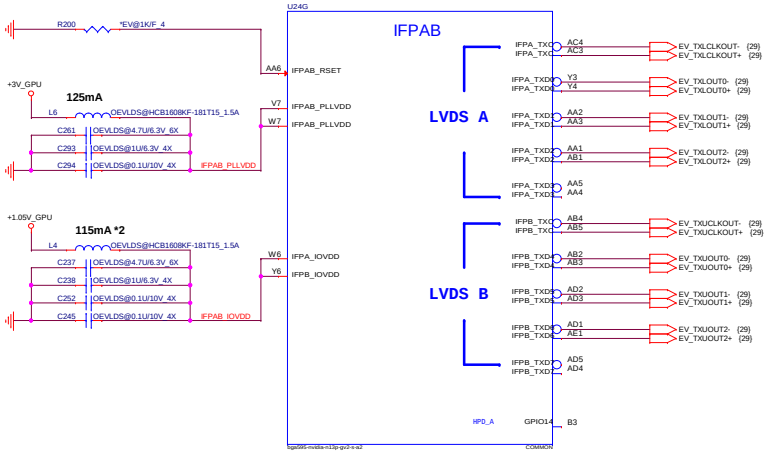

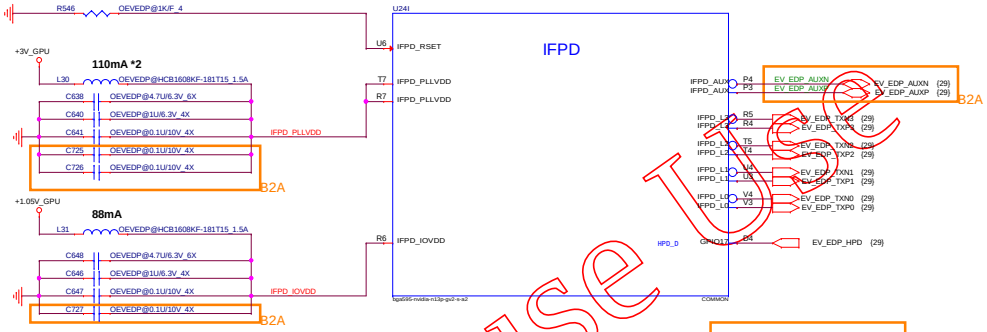

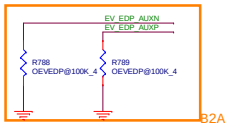

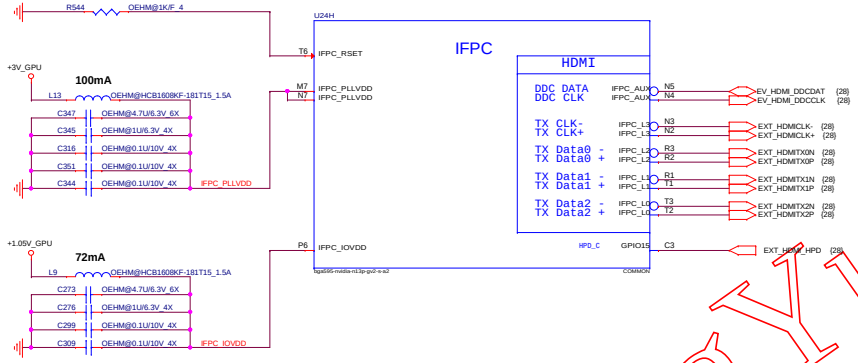

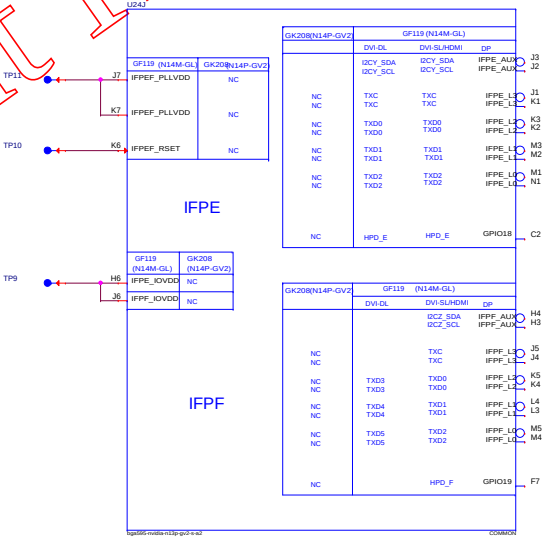

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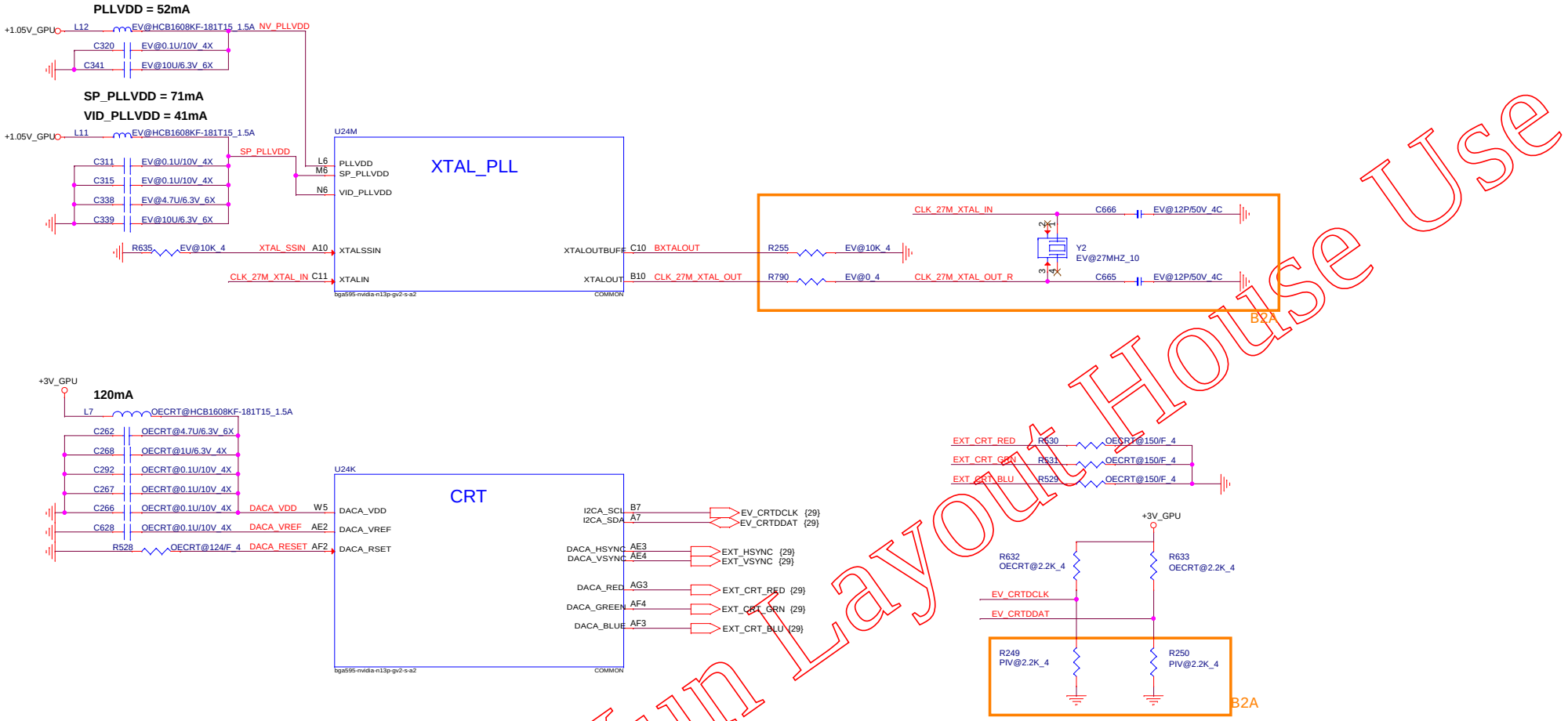

Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	N14x (XTAL/CRT I/F)	A1A

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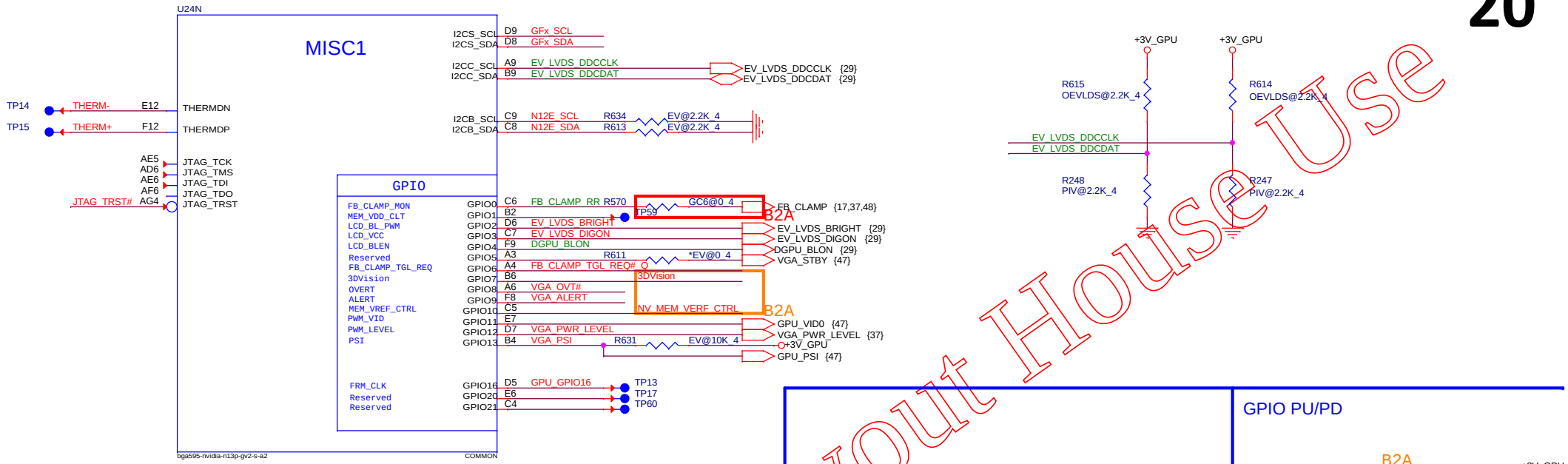

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	N14x (GPIO)	A1A

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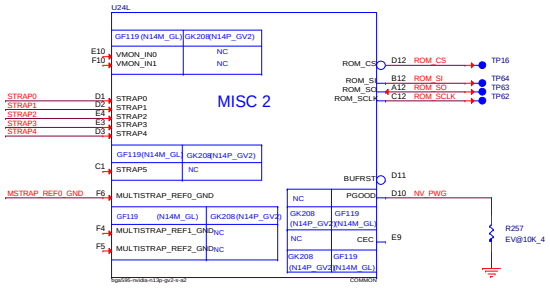

MULT STRIP [N14P_GV2]

PCI_DEVID STRAP	PCI DEVICE ID 0x1292 -->QS 0x12AD -->ES	DP_PLL_VDD33	1 [Default]
RAM_CFG	RAM_CFG[3:0] for memory configuration	PEX_PLL_EN_TERM	PCIE PLL termination 0:Disable [Default] ; 1:Enable
SUB_VENDOR	0:No VBIOS ROM ; 1 BIOS ROM [Default]	3GIO_PADCFG	[0000] --> Gen3 support
FB[1:0]	[1:0] --> 256MB	PCIE_MAX_SPEED	[1] -->Allow boot to PCIE Gen3
VGA_DEVICE	0:3D Device ; 1:VGA Device	PCIE_SPEED_CHANG_ GEN3	[1] -->Enable Gen3
I2CS_Slave Address	0:9E [Default] ; 1:9C	SORx_EXPOSED	SOR0_EXP=0,SOR1_EXP=1 [IFPA/B:LVDS] ; [IFPC:HDMI]
USER STRAP	Panel EDID Support		

Strap Pin name	Strapping Bits 3	Strapping Bits 2	Strapping Bits 1	Strapping Bits 0	SETTING	NOTE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDER	PCI_DEVID[5]	PEX_PLL_EN_TERM		
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]		
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE		
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]		
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]		
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]		
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		
STRAP4	RESERVED	PCIE_SPEED_CHAN CE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V		

4.99K	1000	0000	24.9K	1100	0100
10K	1001	0001	30.1K	1101	0101
15K	1010	0010	34.8K	1110	0110
20K	1011	0011	45.3K	1111	0111
Resistor Value	VDD33	GND	Resistor Value	VDD33	GND

Binary Strap [N14M_GL]

Strap Pin name	Strap Mapping	Polarity	SETTING
ROM_SCLK	SMB_ALT_ADDR	Pull-down to GND	
ROM_SI	SUB_VENDER	Pull-UP to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIO ROM	
ROM_SO	VGA_DEVICE	Pull-down to GND (no dispaly)	
STRAP0	RAMCFG[0]	USER defined	
STRAP1	RAMCFG[1]	USER defined	
STRAP2	RAMCFG[2]	USER defined	
STRAP3	RAMCFG[3]	USER defined	
STRAP4	PCIE_MAX_SPEED	Pull-down to GND	

		Vendor P/N	STN B/S P/N	Size	Strap		Note
128M (2G bit)	Hynix H1	H5TQ2G63DFR-N0C (128M*16) GL/GV2		x4=1GB	GL:0x06 0110	GV2:0x06 0110	1000MHz
				x8=2GB		GV2:0x06 0110	1000MHz
	Hynix H2	H5TQ2G63DFR-11C (128M*16) GL/GV2		x4=1GB	GL:0x06 0110	GV2:0x06 0110	900MHz
				x8=2GB		GV2:0x06 0110	900MHz
	Samsung S1	K4W2G1646E-BC1A (128M*16) GL/GV2		x4=1GB	GL:0x05 0101	GV2:0x07 0111	1000MHz
				x8=2GB		GV2:0x07 0111	1000MHz
	Samsung S2	K4W2G1646E-BC11 (128M*16) GL/GV2		x4=1GB	GL:0x05 0101	GV2:0x07 0111	900MHz
				x8=2GB		GV2:0x07 0111	900MHz
	Micron M1	MT41J128M16JT-107G:K (128M*16) GL/GV2		x4=1GB	GL:0x01 0001	GV2:0x05 0101	900MHz
				x8=2GB		GV2:0x05 0101	900MHz
	Micron M2	MT41J128M16JT-093G:K (128M*16) GL/GV2		x4=1GB	GL:0x01 0001	GV2:0x05 0101	1000MHz
				x8=2GB		GV2:0x05 0101	1000MHz
256M (4Gbit)	Micron M3	MT41K256M16HA-107G:E (256M*16) GL/GV2		x4=2GB	GL:0x0D 1101	GV2:0x01 0001	900MHz
				x8=4GB		GV2:0x01 0001	900MHz
	Samsung S3	K4W4G1646B-HC11 (256M*16) GL/GV2		x4=2GB	GL:0x0B 1011	GV2:0x03 0011	900MHz
				x8=4GB		GV2:0x03 0011	900MHz
	Hynix H3	H5TQ4G63MFR-11C (256M*16) GL		x4=2GB	GL:0x03 0011		900MHz
				N/A			
	Hynix H4	H5TQ4G63AFR-11C (256M*16) GL		x4=2GB	GL:0x04 0100		900MHz
				N/A			

N14P_GV2	H1/H2	S1/S2	M1/M2	S3	M3
ROM_SI	34.8K	45.3K	30.1K	20K	10K
	CS33482FB22	CS34532FB18	CS33012FB18	CS32002FB29	CS31002FB26

N14M_GL	Strap3	Strap2	Strap1	Strap0
H1	D0	C1	B1	A0
H2	D0	C1	B1	A0
H3	D0	C0	B1	A1
H4	D0	C1	B0	A0
S1	D0	C1	B0	A1
S2	D0	C1	B0	A1
S3	D1	C0	B1	A1
M1	D0	C0	B0	A1
M2	D0	C0	B0	A1
M3	D1	C1	B0	A1

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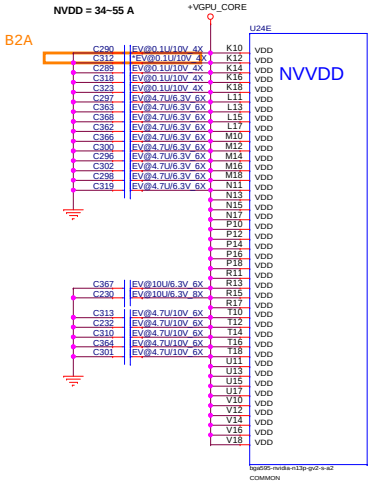
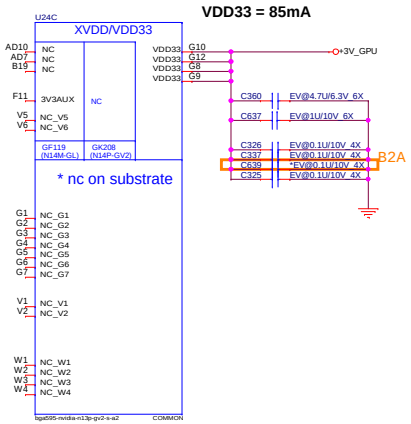
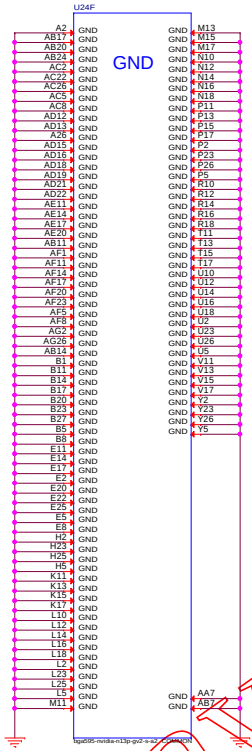
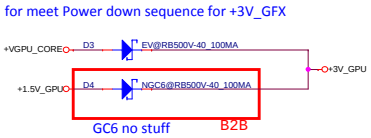
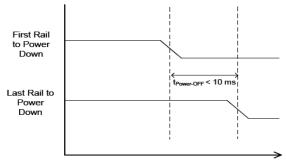




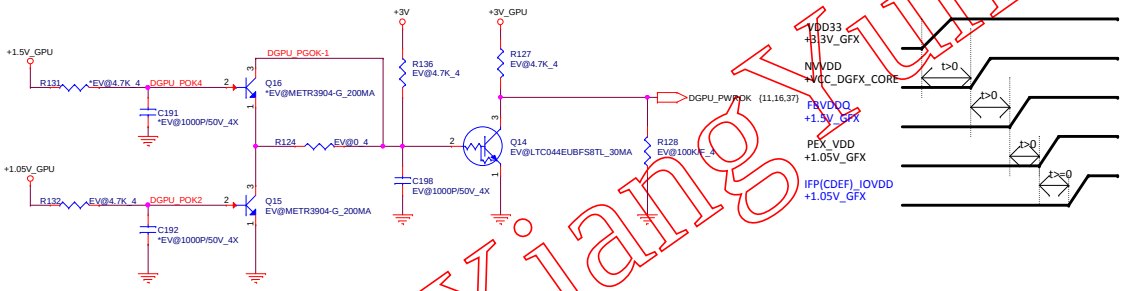


Power down sequence





Power up sequence



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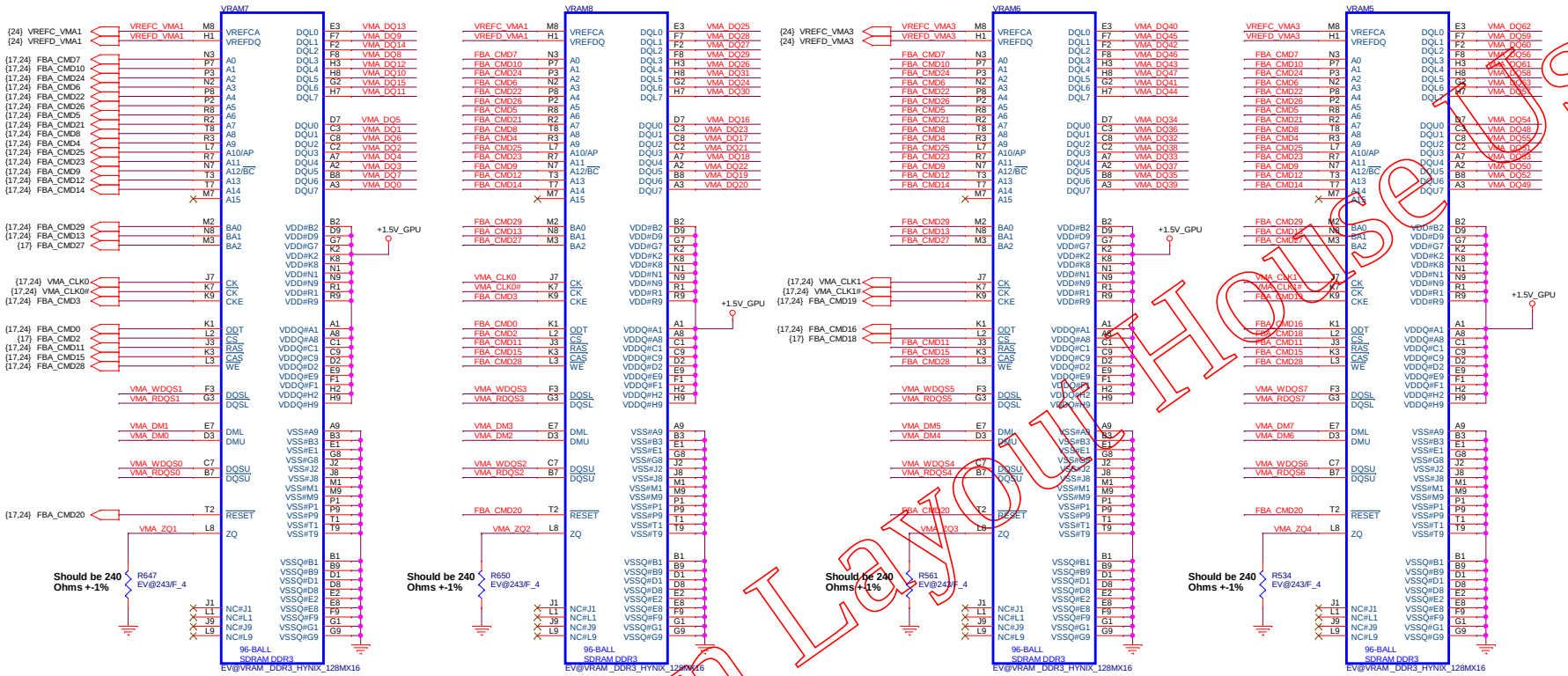
RANK0: 256MB/512MB DDR3

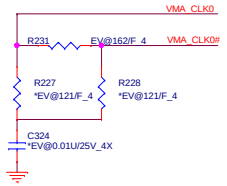
{17,24} VMA_DQ[63..0]
{17,24} VMA_DM[7..0]
{17,24} VMA_WDQS[7..0]
{17,24} VMA_RDQS[7..0]

DataBus [0:31]

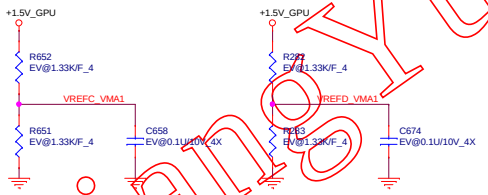
DataBus [64:32]



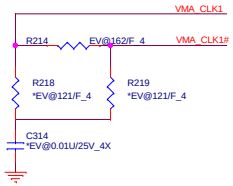
CLK-A0 Termination



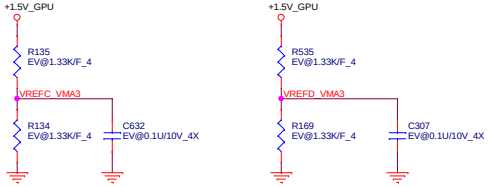
MEM Reference Voltage (Low)



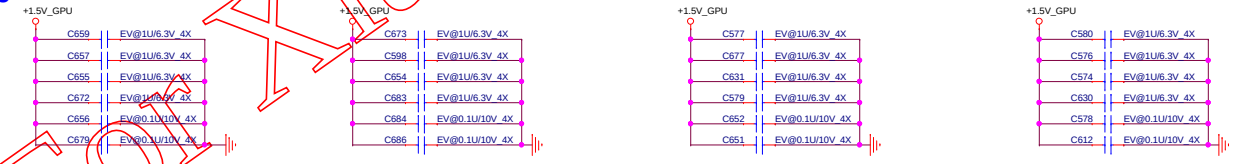
CLK-A1 Termination



MEM Reference Voltage (High Bus)



VRAM De-Coupling



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	N14x (DDR/Rank0)	A1A
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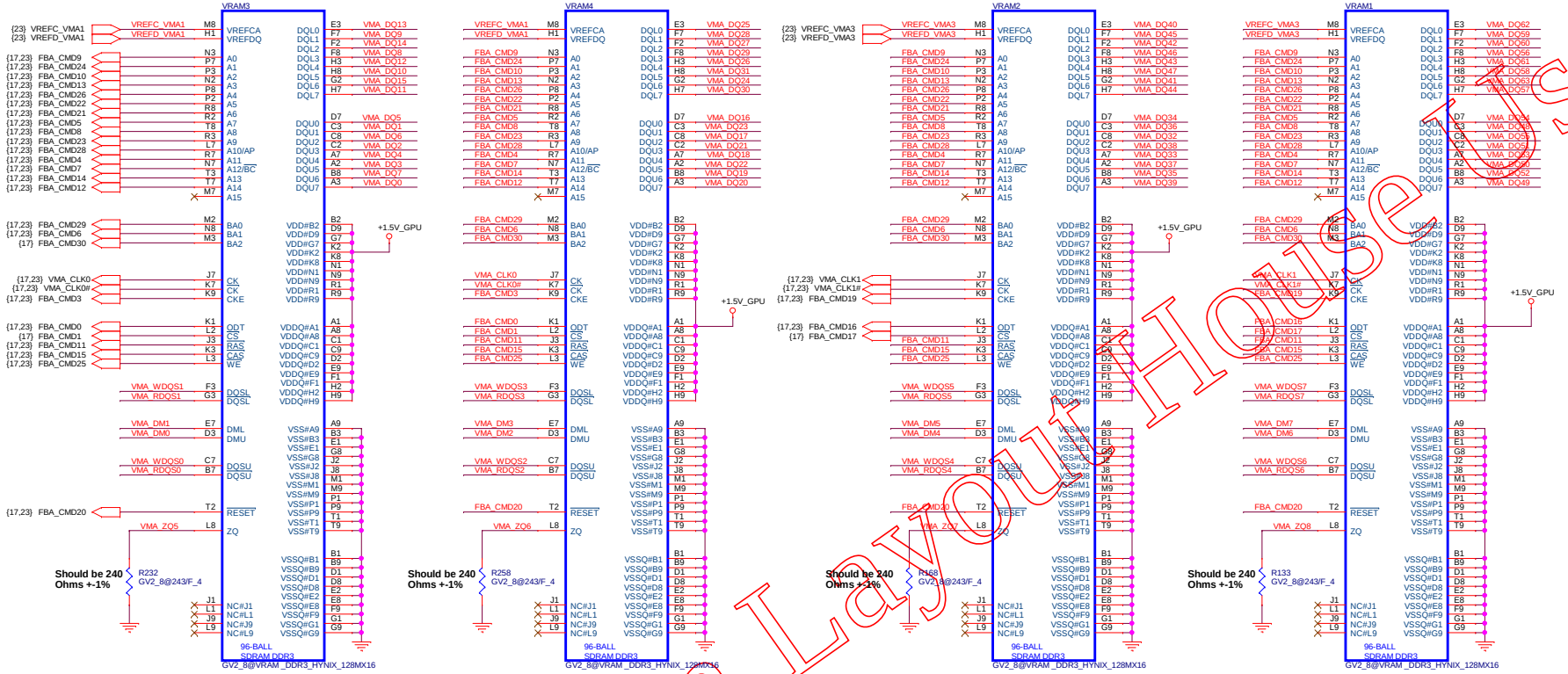
RANK1: 256MB/512MB DDR3

{17,23} VMA_DQ[63..0]
{17,23} VMA_DM[7..0]
{17,23} VMA_WDQS[7..0]
{17,23} VMA_RDQS[7..0]

DataBus [0:31]

DataBus [64:32]



VRAM De-Coupling

Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	N14x (DDR/Rank1)	A1A
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Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	VRAM_A: DDR3*4PCS	A1A

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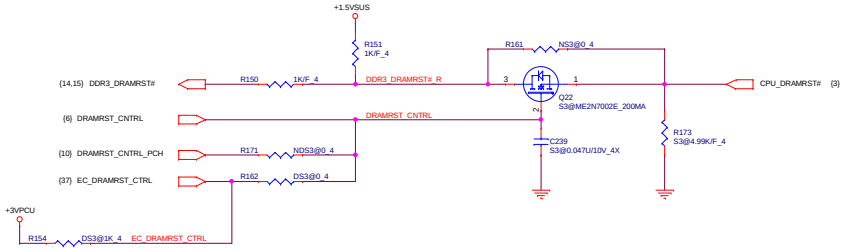
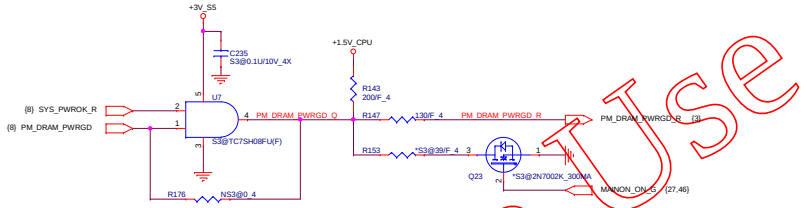
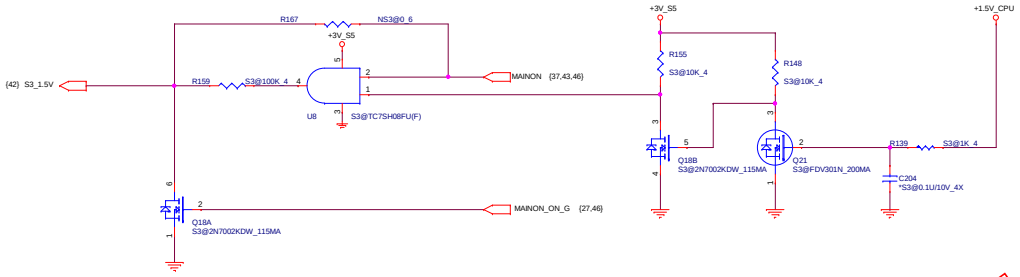
S3 power Reduction (SM_DRAMRST#) <S3P>



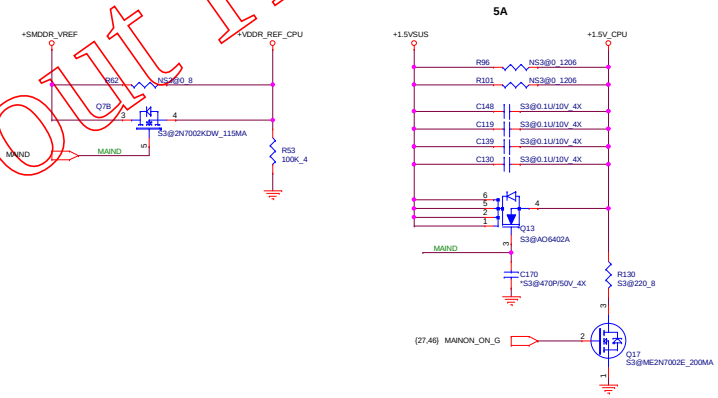
S3 power Reduction (SM_DRAMPWROK) <S3P>



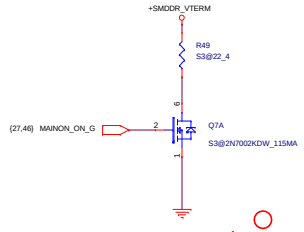
For S3 power Reduction Sequence <S3P>



S3 power Reduction (CPU Power) <S3P>



For S3 power Reduction VTT discharge <S3P>



Quanta Computer Inc.
PROJECT : BD5
Size: Document Number: S3 power Reduction
Rev: 1A
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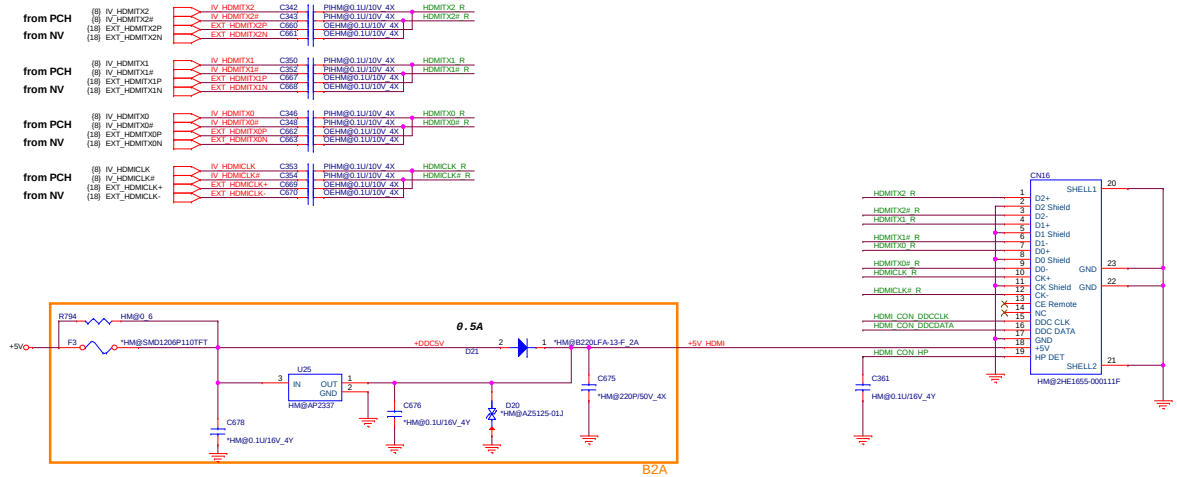
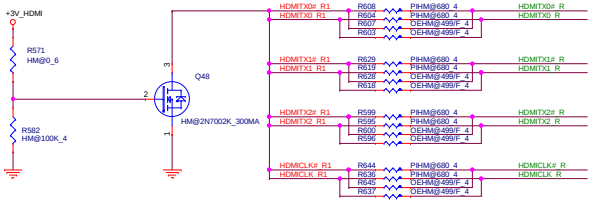
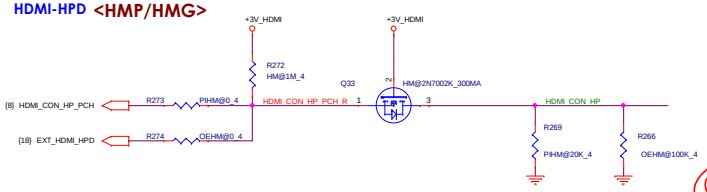
HDMI Conn <HDM>



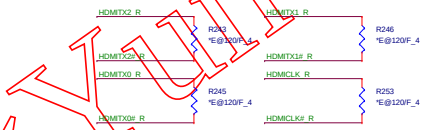
HDMI-passive level shift <HMP/HMG>



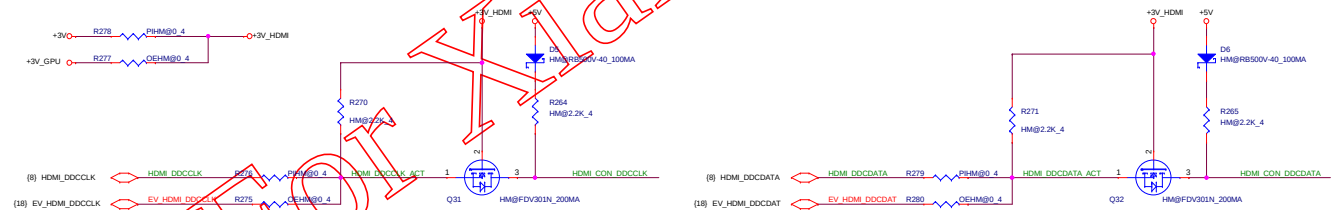
HDMI-HPD <HMP/HMG>



FOR EMI <EMC>



HDMI-SMBus <HDM>



Quanta Computer Inc.		
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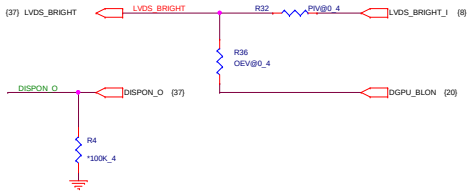
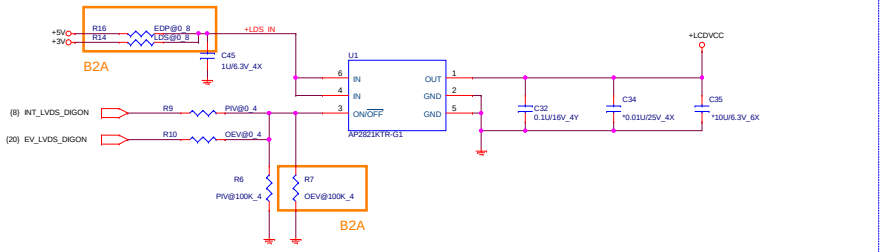
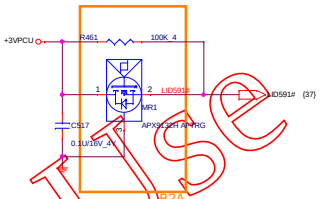
Panel backlight control <LDS>



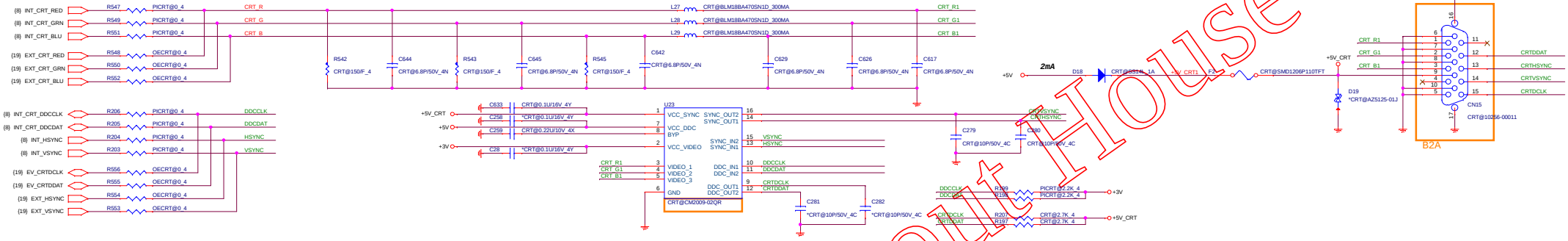
LCD POWER SWITCH <LDS>



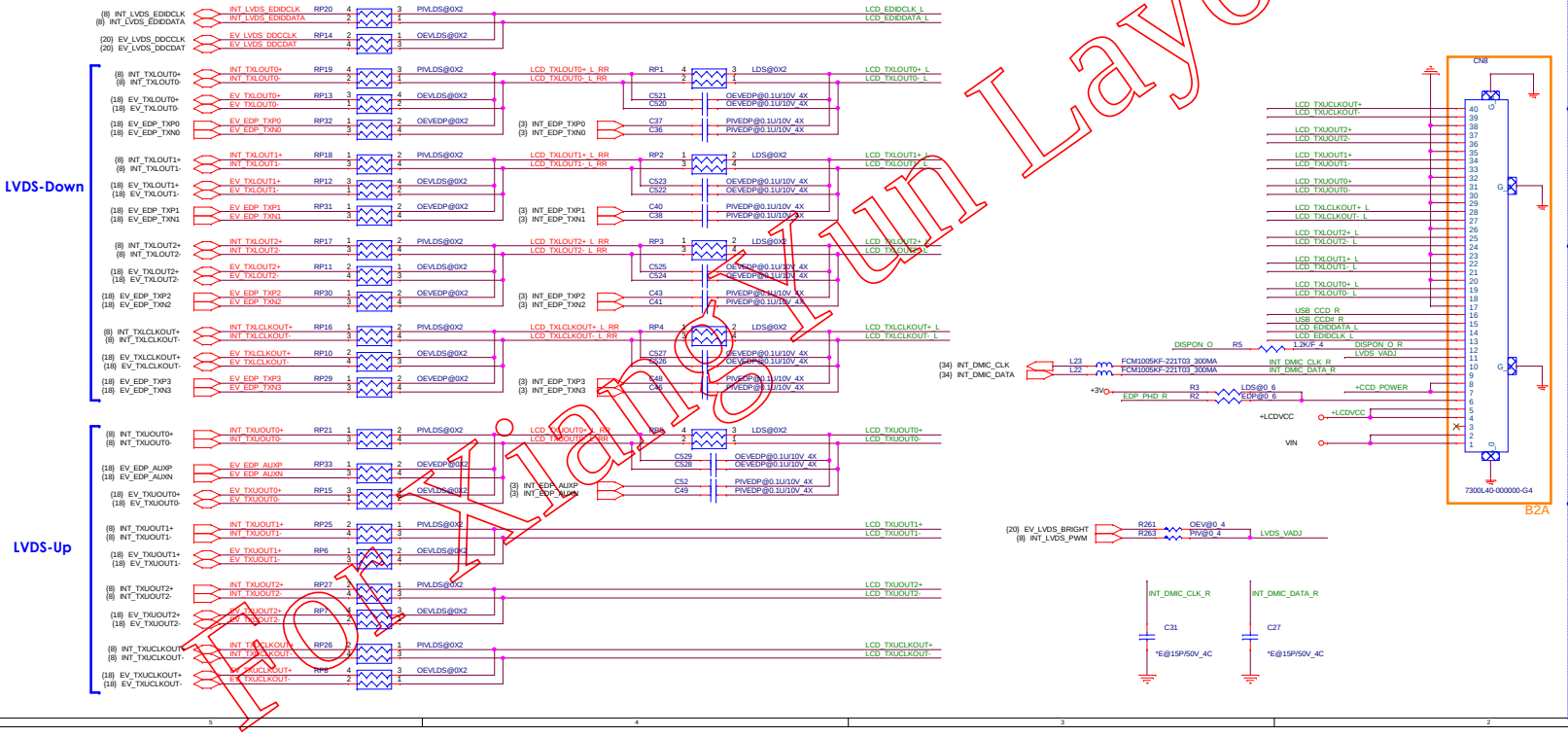
HALL Sensor <HSR>



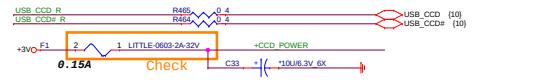
CRT <CRT>

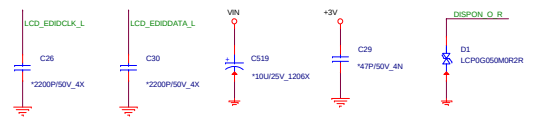


LCD Panel Module <LDS>

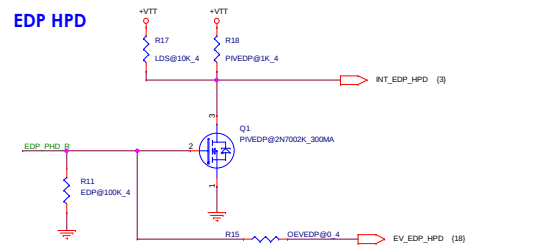


CCD <CCD>

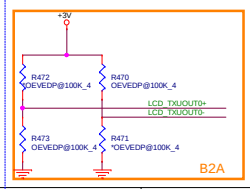




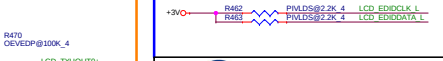
EDP HPD



EDP PU/PD



SMBus



Quanta Computer Inc.
PROJECT : BD5

Size	Document Number	Rev
	LCD/CRT/CCD	1A

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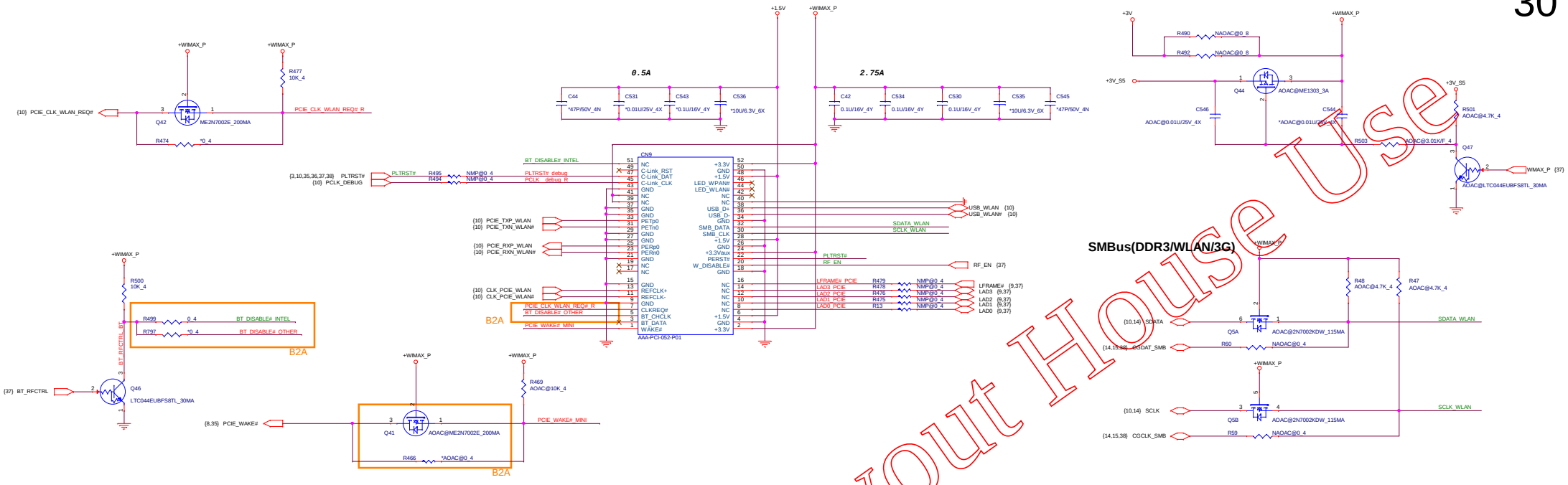
MINI Card Slot#1(WiFi / Wimax / Combo) <MNW>



AOAC <MNW>

SMBus(DDR3/WLAN/3G)

Quanta Computer Inc.
PROJECT : BD5

Size	Document Number	Rev
	MINI CARD(WLAN)	1A

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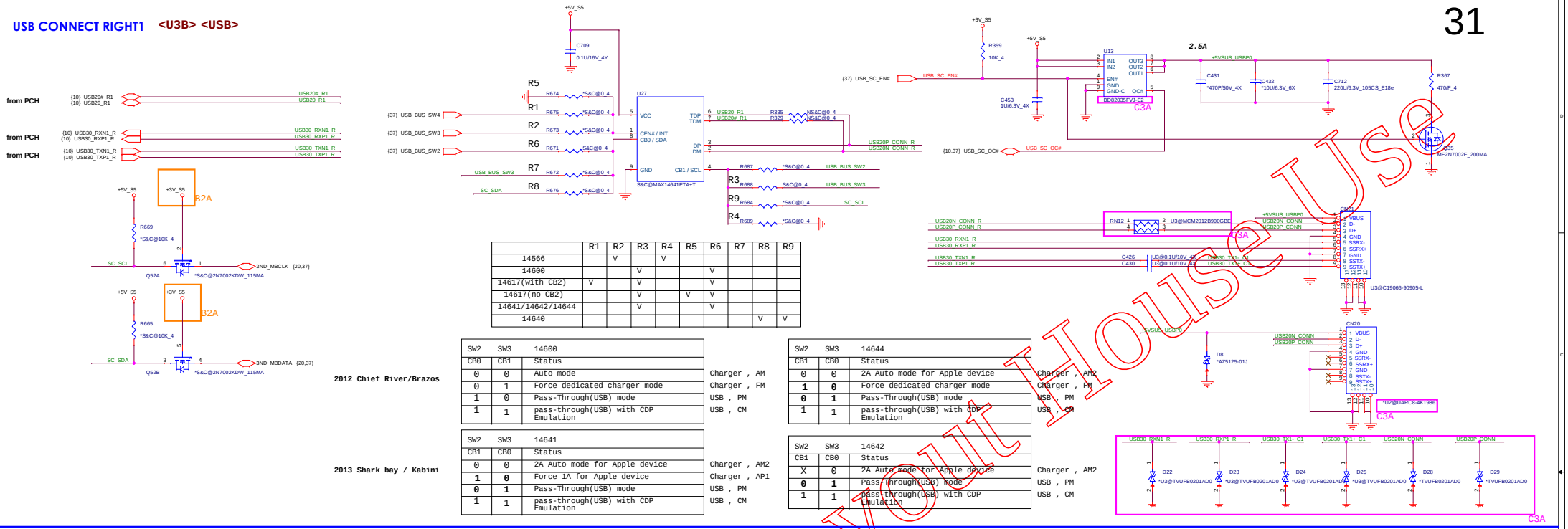
USB CONNECT RIGHT1 <U3B> <USB>



	R1	R2	R3	R4	R5	R6	R7	R8	R9
14566		V		V					
14600			V			V			
14617(with CB2)	V		V			V			
14617(no CB2)			V		V	V			
14641/14642/14644			V			V			
14640								V	V

2012 Chief River/Brazos

SW2	SW3	14600	
CB0	CB1	Status	
0	0	Auto mode	Charger , AM
0	1	Force dedicated charger mode	Charger , FM
1	0	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

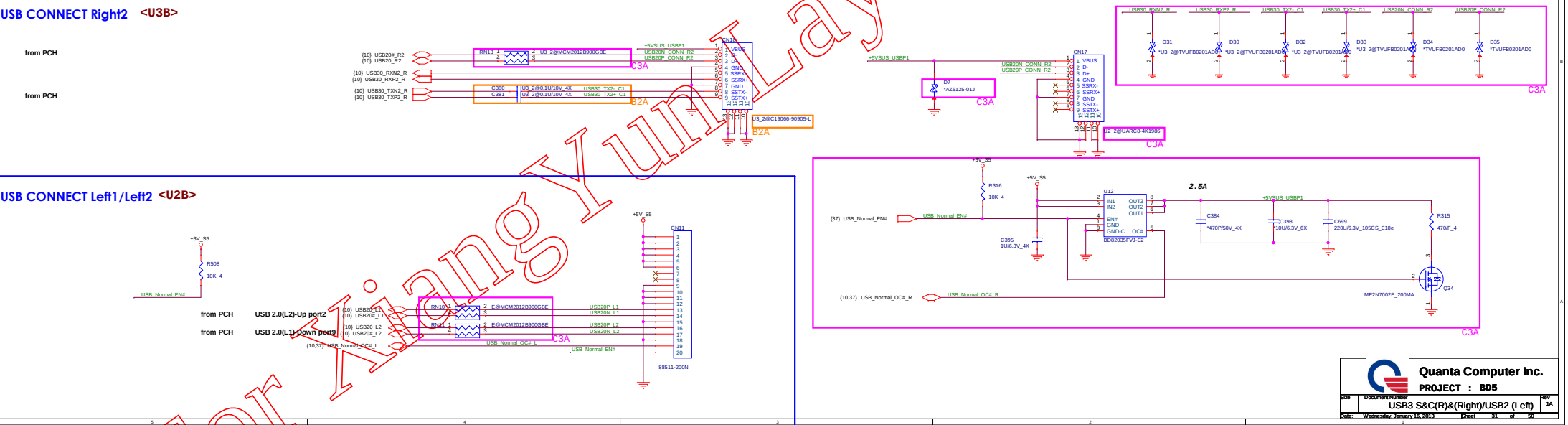
SW2	SW3	14644	
CB1	CB0	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
1	**0**	Force dedicated charger mode	Charger , FM
0	**1**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

2013 Shark bay / Kabini

SW2	SW3	14641	
CB1	CB0	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
1	**0**	Force 1A for Apple device	Charger , AP1
0	**1**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

SW2	SW3	14642	
CB1	CB0	Status	
X	0	2A Auto mode for Apple device	Charger , AM2
0	**1**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

USB CONNECT Right2 <U3B>



USB CONNECT Left1/Left2 <U2B>

Quanta Computer Inc.
PROJECT : BD5
Size | Document Number | Rev 1A
USB3 S&C(R)&(Right)/USB2 (Left)
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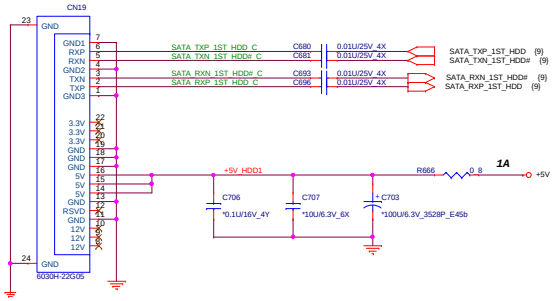
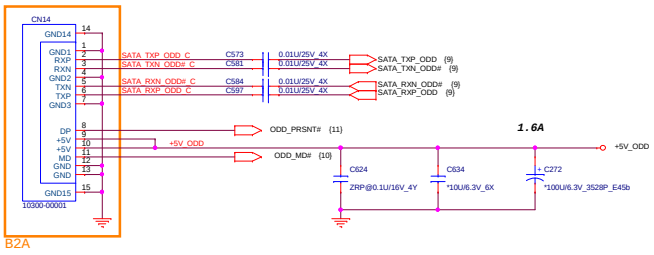
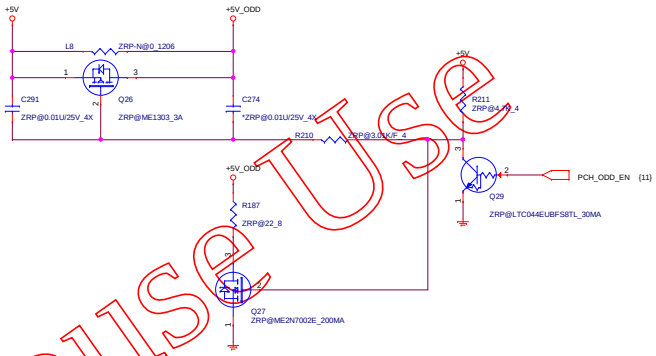
SATA HDD <HDD>



SATA ODD <ODD>



ODD Zero power . (Only for Intel) <OZP>



Quanta Computer Inc.
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	HDD/ODD	1A

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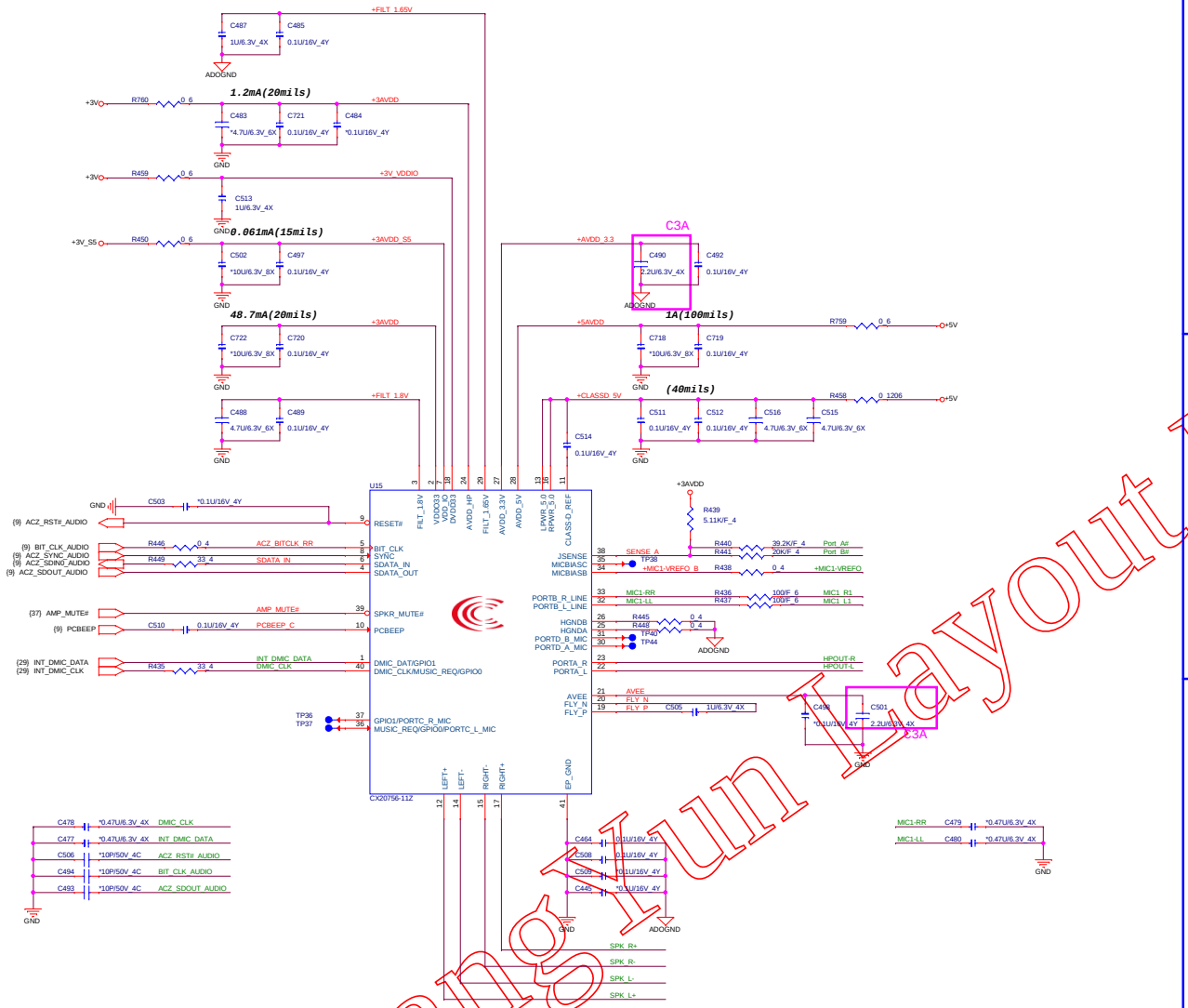
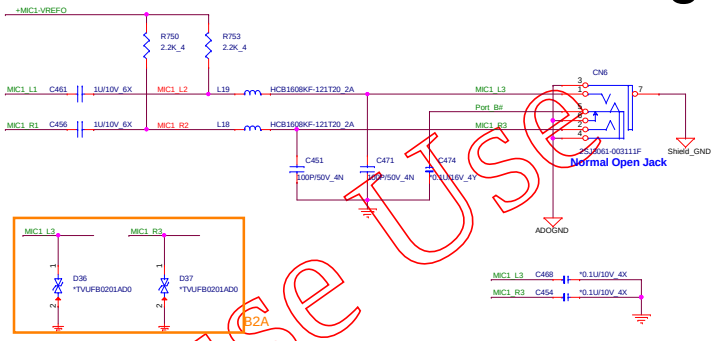
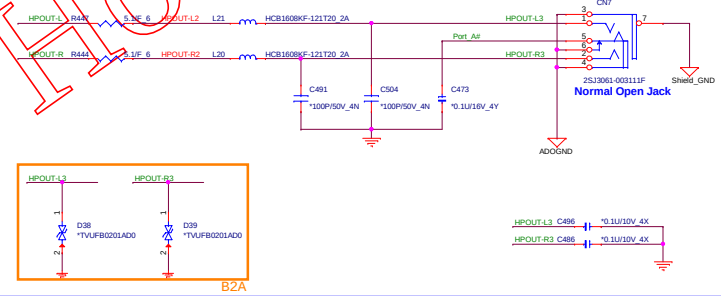
Codec (CX20756-11Z) <ADO>



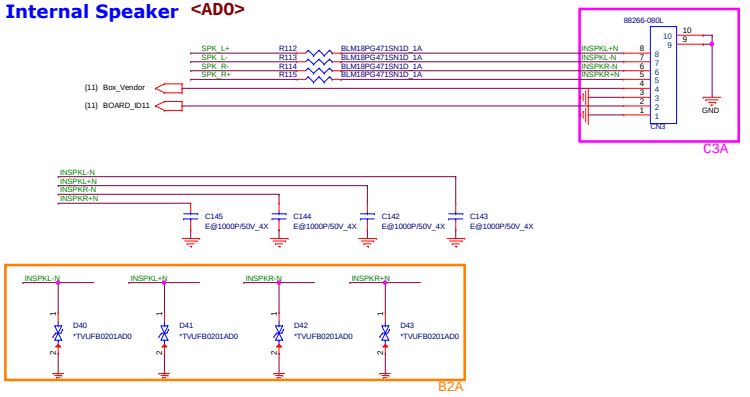
External MIC <ADO>



Headphone <ADO>



Internal Speaker <ADO>



Quanta Computer Inc.
PROJECT : BD5

Size	Document Number	Rev
	Audio Codec (CX20671)	A1A

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Atheros Lan <LAN/LN1.LNG>

	L2,C1,C2,C3
Switch mode	Mount
LDO mode	NC

L1

	L1
Switch mode	Mount
LDO mode	NC

0.163A(20mils)

Atheros AR8161/8162

B2A

TRANSFORMER <LAN/LN1.LNG>

B2A

B2A

Quanta P/N : CYBS401N201

RJ45 <LAN>

LED0 = LAN_ACTLED	1	High core voltage(default=1)
	0	Low core voltage
LED1 = LAN_LINKLED#	1	Switch mode regulator (SWR) select
	0	Linear regulator (LDO) select
LED2	1	25 MHz external clock input
	0	48 MHz external clock input

Quanta Computer Inc.
PROJECT : BD5

Size	Document Number	Rev
	Atheros LAN (AR8161B/62B)	A1A

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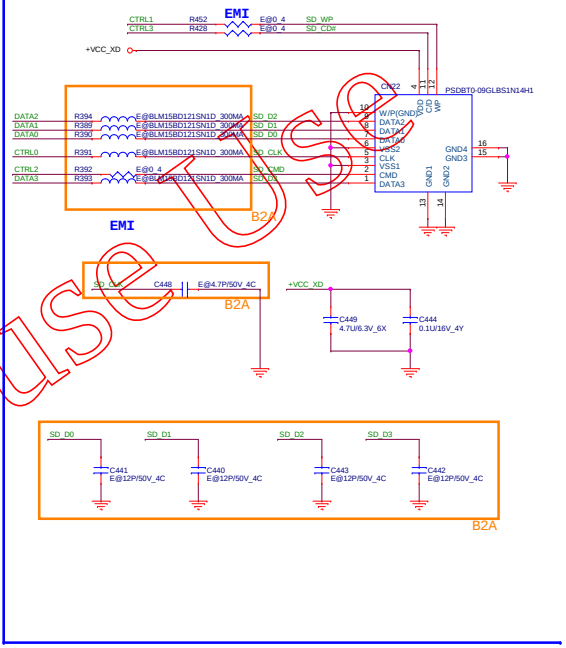
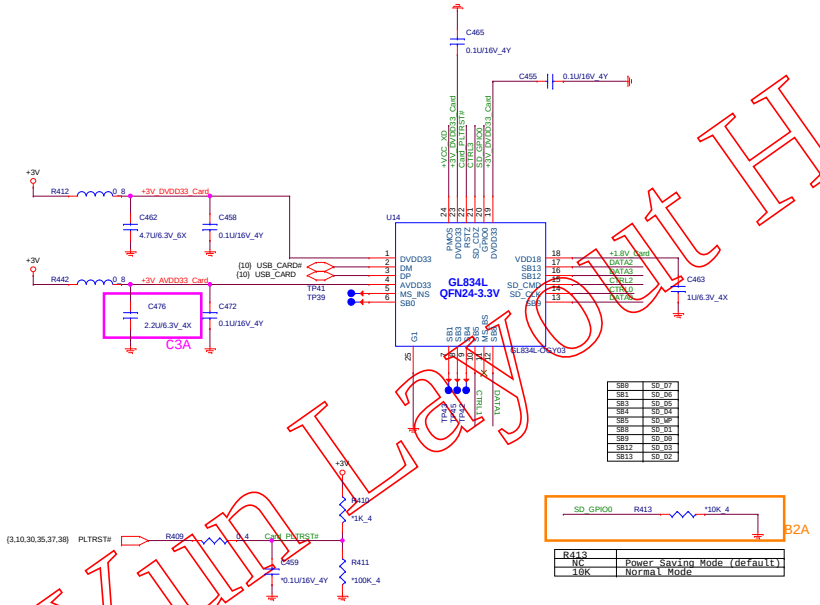
2 IN 1 Card Reader <MMC>



Card Reader (GL834L) <MMC>



SB0	SD_D7
SB1	SD_D6
SB3	SD_D5
SB4	SD_D4
SB5	SD_WP
SB8	SD_D1
SB9	SD_D0
SB12	SD_D3
SB13	SD_D2

R413	
NC	Power Saving Mode (default)
10K	Normal Mode

Quanta Computer Inc.
PROJECT : BD5

Size	Document Number	Rev
	Card Reader(GL834L)	XLA

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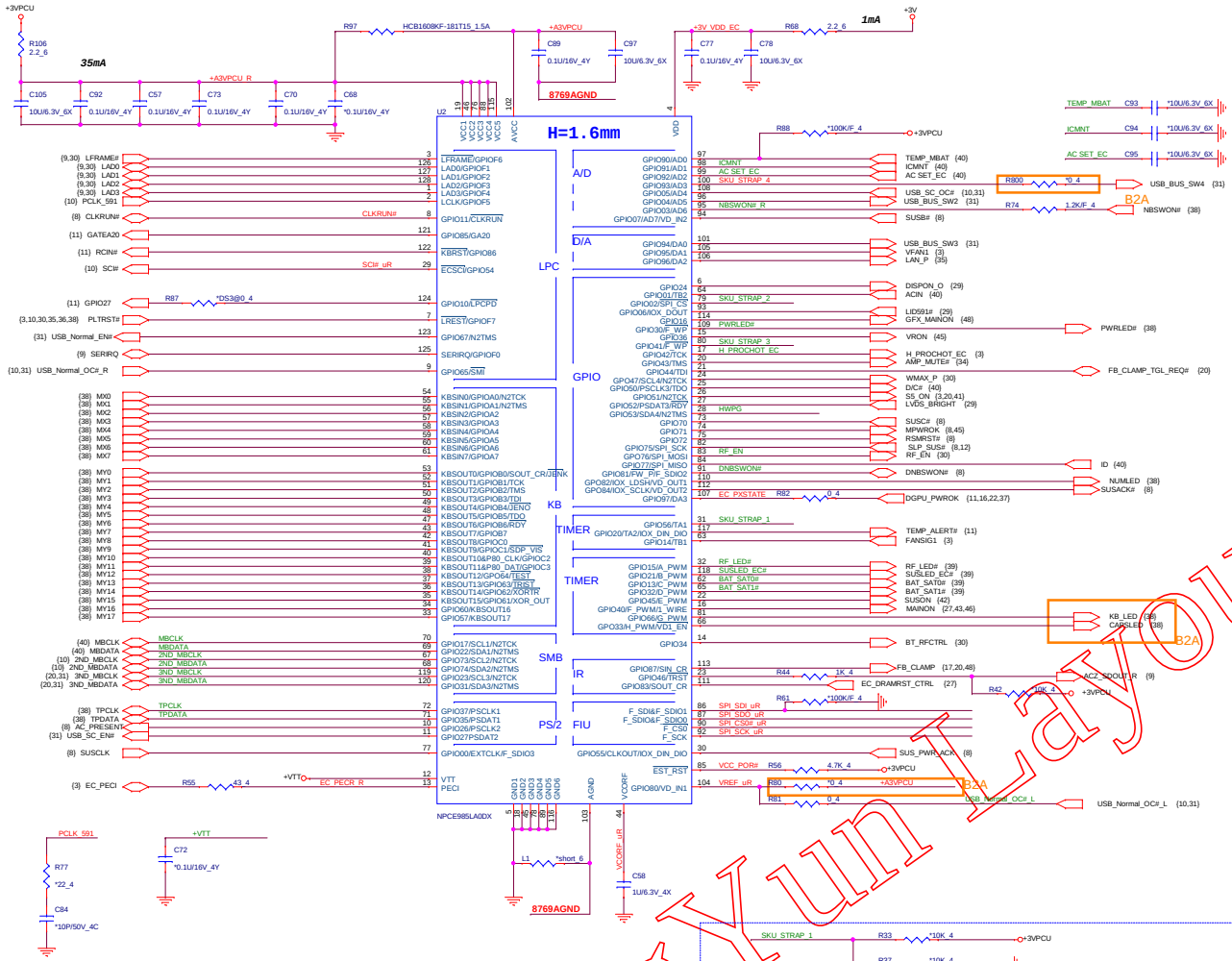
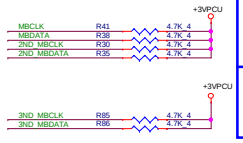
EC <KBC>

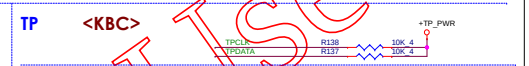


SM BUS PU/Address <KBC>

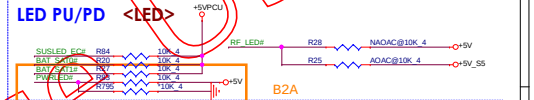


SMBUS	Devices	Address
1	Battery(A)	
2	PCH(S5)	
	G-sensor(S0)	
	IDROM(A)	
3	VGA Thermal(S0)	
	CEC(A)	

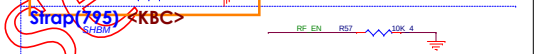
TP <KBC>



LED PU/PD <LED>

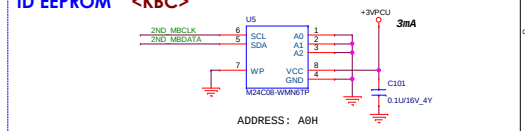


Strap(795) <KBC>

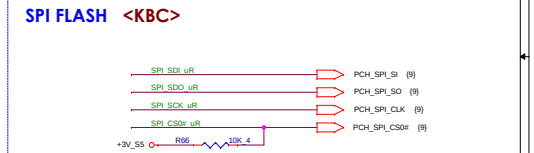


INTERNAL KEYBOARD STRIP SET <KBC>

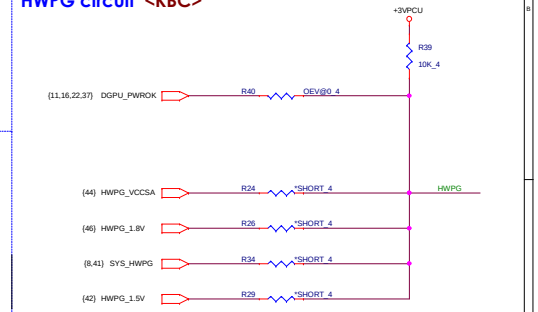
ID EEPROM <KBC>



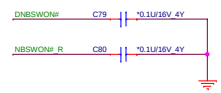
SPI FLASH <KBC>



HWPG circuit <KBC>



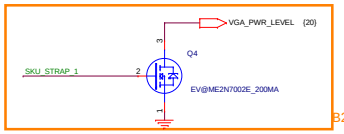
Power Button <KBC>



Capetown@/Aswan@ EV@ / IV@

MS Strap	SKU_STRAP_2	SKU_STRAP_3
14'' Capetown UMA	1	0
14'' Capetown DIS	1	1
17'' Aswan UMA	0	0
17'' Aswan DIS	0	1

SKU_STRAP_4	
H	Shark Bay
L	Chief River



Quanta Computer Inc.
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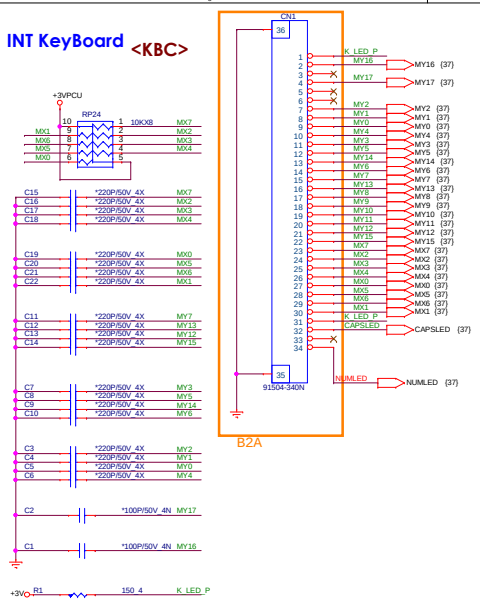
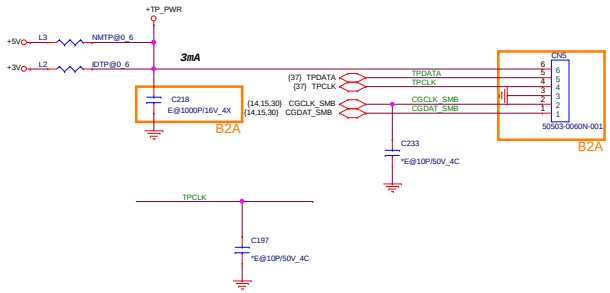
INT KeyBoard <KBC>

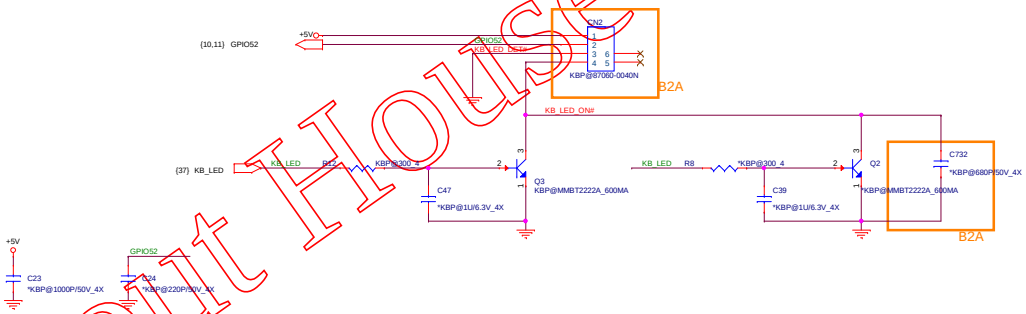


TP board <TPD>

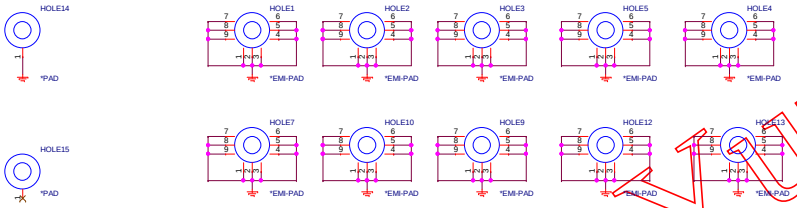


Power board w LED <PSW>

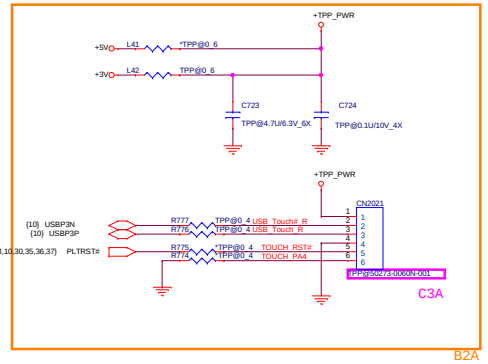
K/B LED power <KBP>



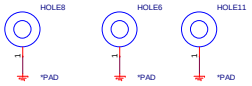
HOLE



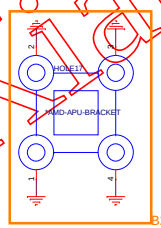
TOUCH PANEL <TPP>



VGA HOLE



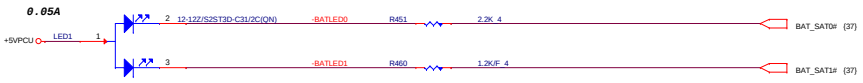
CPU HOLE



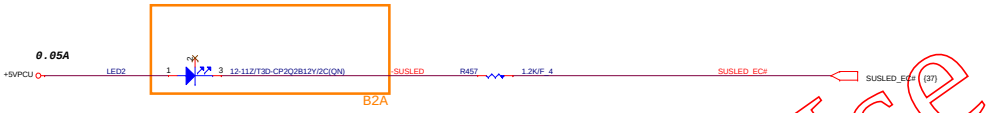
MINI Card NUT

Quanta Computer Inc.		
PROJECT : BD5		
Size	Document Number: KB/TP/PB/HOLE	Rev: 1A
Date: Wednesday, January 16, 2013	Sheet 38 of 50	

LED-Battery <LED><W+A>

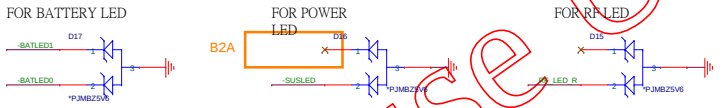


LED-Power <LED><W+A>

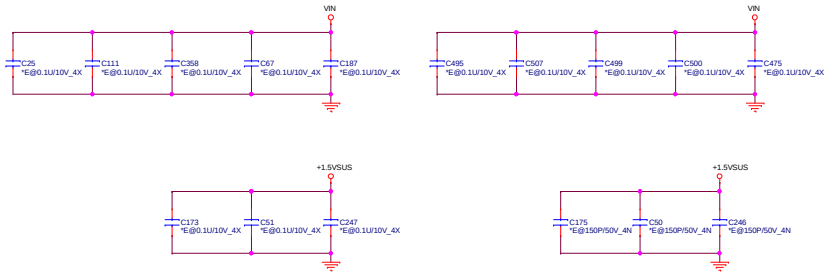


LED-WiFi <LED>

ESD Protect <EMC>



EMI



Quanta Computer Inc.
PROJECT : BD5

Size	Document Number	Rev
	LED/EMI	1A

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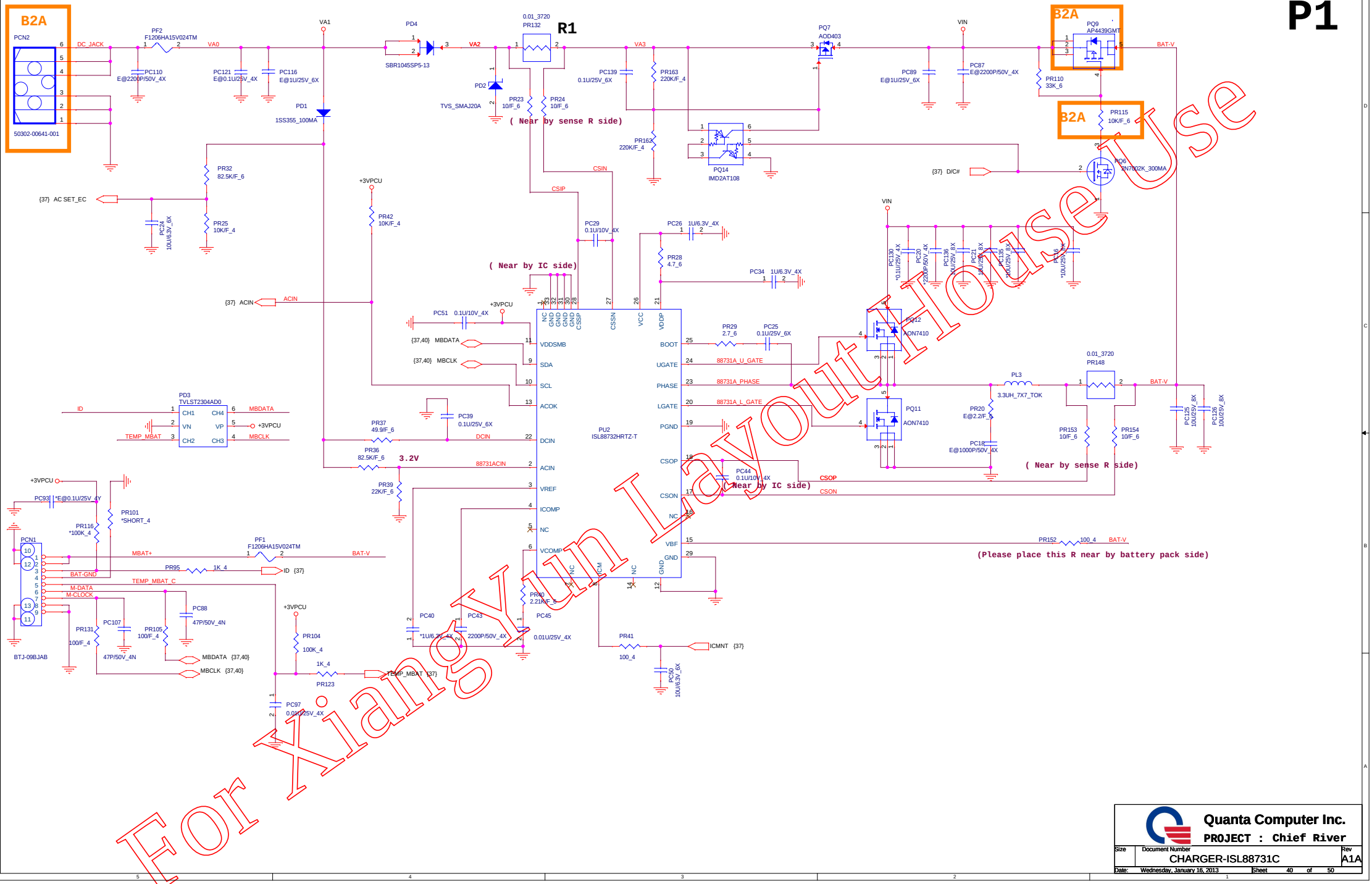
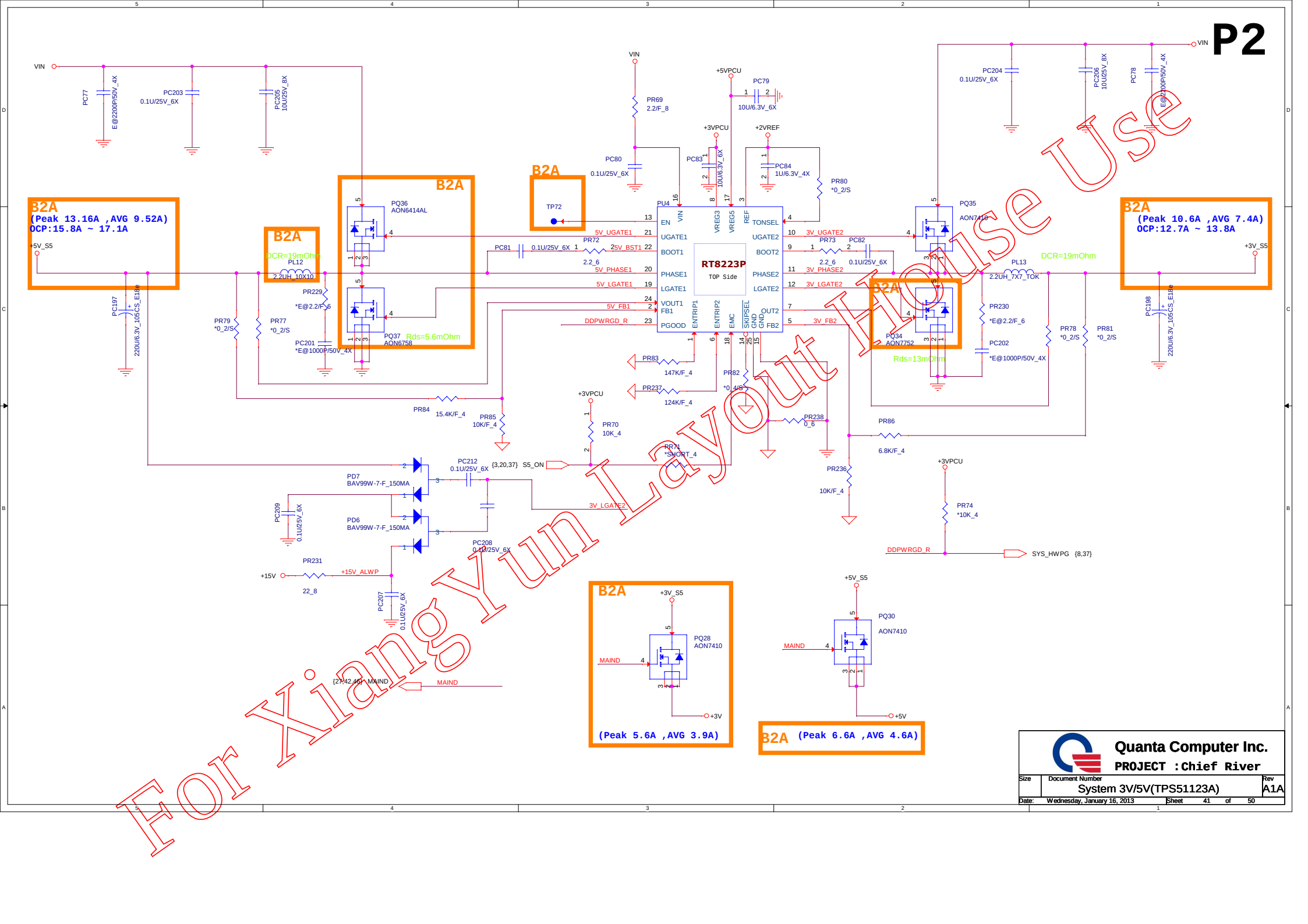

P1
B2A
PCN2
50302-00641-001
DC_JACK
PF2
F1206HA15V024TM
VA0
VA1
PC110
E@2200P/50V_4X
PC121
E@0.1U/25V_4X
PC116
E@1U/25V_6X
PD1
1SS355_100MA
PD4
SBR1045SP5-13
VA2
R1
0.01_3720
PR132
PD2
TVS_SMAJ20A
PR23
10/F_6
PR24
10/F_6
(Near by sense R side)
VA3
PC139
0.1U/25V_6X
PR163
220K/F_4
PR162
220K/F_4
PQ14
IMD2AT108
PQ7
AOD403
VIN
PC89
E@1U/25V_6X
PC87
E@2200P/50V_4X
B2A
PQ9
AP4439GMT
BAT-V
PR110
33K_6
B2A
PR115
10K/F_6
PQ6
2N7002K_300MA
{37} D/C#
PR32
82.5K/F_6
{37} AC SET_EC
PC24
10U/6.3V_6X
PR25
10K/F_4
+3VPCU
PR42
10K/F_4
CSIN
CSIP
PC29
0.1U/10V_4X
(Near by IC side)
PC26
1U/6.3V_4X
PR28
4.7_6
PC34
1U/6.3V_4X
{37} ACIN
ACIN
PC51
0.1U/10V_4X
{37,40} MBDATA
{37,40} MBCLK
PU2
ISL88732HRTZ-T
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
PR29
2.7_6
PC25
0.1U/25V_6X
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ12
AON7410
PQ11
AON7410
PL3
3.3UH_7X7_TOK
PR20
E@2.2/F_6
PC18
E@1000P/50V_4X
0.01_3720
PR148
PR153
10/F_6
PR154
10/F_6
PC125
10U/25V_8X
PC126
10U/25V_8X
(Near by sense R side)
PC44
0.1U/10V_4X
(Near by IC side)
CSOP
CSON
PR152
100_4
BAT-V
(Please place this R near by battery pack side)
PD3
TVLST2304AD0
ID
TEMP_MBAT
MBDATA
+3VPCU
MBCLK
PR37
49.9/F_6
PC39
0.1U/25V_6X
DCIN
PR36
82.5K/F_6
3.2V
88731ACIN
PR39
22K/F_6
PC93
*E@0.1U/25V_4Y
PR101
*SHORT_4
PR116
*100K_4
PCN1
BTJ-09BJAB
MBAT+
PF1
F1206HA15V024TM
BAT-V
PR95
1K_4
ID {37}
BAT-GND
TEMP_MBAT_C
M-DATA
M-CLOCK
PC107
47P/50V_4N
PR131
100/F_4
PR105
100/F_4
PC88
47P/50V_4N
MBDATA {37,40}
MBCLK {37,40}
PR104
100K_4
1K_4
PR123
TEMP_MBAT {37}
PC97
0.01U/25V_4X
PC40
*1U/6.3V_4X
PC43
2200P/50V_4X
PC45
0.01U/25V_4X
PR40
2.21K/F_6
PR41
100_4
ICMNT {37}
PC50
10U/6.3V_6X
For Xiangyun Layout Use Only
Quanta Computer Inc.
PROJECT : Chief River
Size
Document Number
CHARGER-ISL88731C
Rev
A1A
Date: Wednesday, January 16, 2013
Sheet 40 of 50


P2
B2A
(Peak 13.16A ,AVG 9.52A)
OCP:15.8A ~ 17.1A
B2A
(Peak 10.6A ,AVG 7.4A)
OCP:12.7A ~ 13.8A
B2A
(Peak 5.6A ,AVG 3.9A)
B2A (Peak 6.6A ,AVG 4.6A)
RT8223P
TOP Side
PU4
PQ36 AON6414AL
PQ37 AON6758
PQ35 AON7410
PQ34 AON7752
PQ28 AON7410
PQ30 AON7410
PL12 2.2UH_10X10
PL13 2.2UH_7X7_TOK
DCR=19mOhm
Rds=5.6mOhm
Rds=13mOhm
VIN
+5V_S5
+3V_S5
+3VPCU
+5VPCU
+2VREF
+15V
+5V
+3V
5V_UGATE1
5V_BST1
5V_PHASE1
5V_LGATE1
5V_FB1
3V_UGATE2
3V_PHASE2
3V_LGATE2
3V_FB2
DDPWRGD_R
SYS_HWPG {8,37}
S5_ON {3,20,37}
MAIND {27,42,46}
+15V_ALWP
PD7 BAV99W-7-F_150MA
PD6 BAV99W-7-F_150MA
PR69 2.2/F_8
PR70 10K_4
PR71 *SHORT_4
PR72 2.2_6
PR73 2.2_6
PR74 *10K_4
PR77 *0_2/S
PR78 *0_2/S
PR79 *0_2/S
PR80 *0_2/S
PR81 *0_2/S
PR82 *0_4/S
PR83 147K/F_4
PR84 15.4K/F_4
PR85 10K/F_4
PR86 6.8K/F_4
PR229 *E@2.2/F_6
PR230 *E@2.2/F_6
PR231 22_8
PR236 10K/F_4
PR237 124K/F_4
PR238 0_6
PC77 E@2200P/50V_4X
PC78 E@2100P/50V_4X
PC79 10U/6.3V_6X
PC80 0.1U/25V_6X
PC81 0.1U/25V_6X
PC82 0.1U/25V_6X
PC83 10U/6.3V_6X
PC84 1U/6.3V_4X
PC197 220U/6.3V_105CS_E18
PC198 220U/6.3V_105CS_E18
PC201 *E@1000P/50V_4X
PC202 *E@1000P/50V_4X
PC203 0.1U/25V_6X
PC204 0.1U/25V_6X
PC205 10U/25V_8X
PC206 10U/25V_8X
PC207 0.1U/25V_6X
PC208 0.1U/25V_6X
PC209 0.1U/25V_6X
PC212 0.1U/25V_6X
Quanta Computer Inc.
PROJECT :Chief River
System 3V/5V(TPS51123A)
Size
Document Number
Rev
A1A
Date: Wednesday, January 16, 2013
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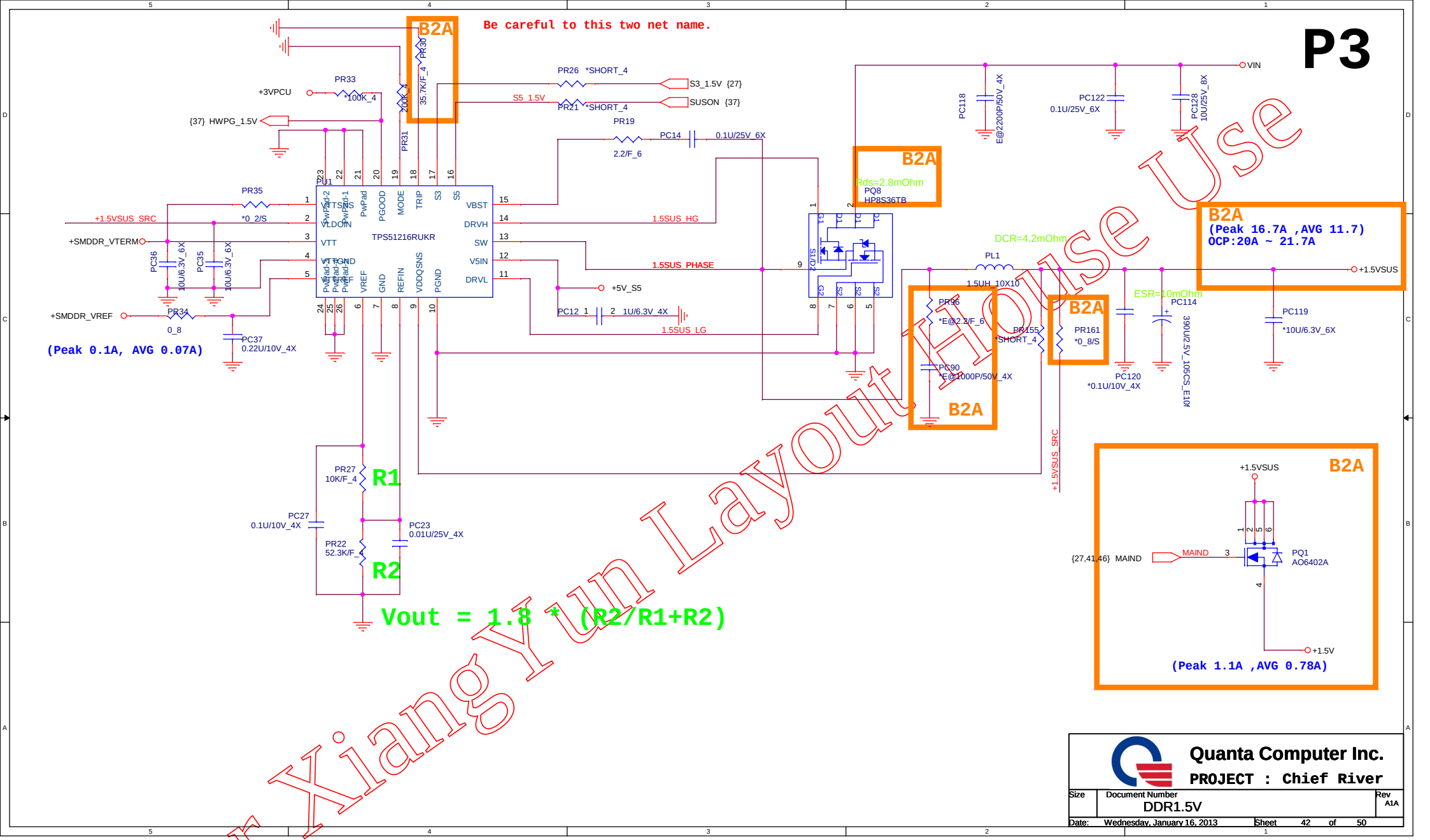
For Xiang Yun Layout House Use


P3
B2A
Be careful to this two net name.
PR33
+3VPCU
*100K_4
{37} HWPG_1.5V
PR30
200K_4
35.7K/F_4
PR31
PR26 *SHORT_4
S3_1.5V {27}
S5_1.5V
PR21 *SHORT_4
SUSON {37}
PR19
2.2/F_6
PC14
0.1U/25V_6X
PU1
TPS51216RUKR
PR35
*0_2/S
+1.5VSUS_SRC
+SMDDR_VTERM
PC36
10U/6.3V_6X
PC35
10U/6.3V_6X
+SMDDR_VREF
PR34
0_8
PC37
0.22U/10V_4X
(Peak 0.1A, AVG 0.07A)
1.5SUS_HG
1.5SUS_PHASE
1.5SUS_LG
+5V_S5
PC12 1 2 1U/6.3V_4X
PR27
10K/F_4
R1
PC27
0.1U/10V_4X
PC23
0.01U/25V_4X
PR22
52.3K/F_4
R2
Vout = 1.8 * (R2/R1+R2)
PC118
E@220P/50V_4X
PC122
0.1U/25V_6X
PC128
10U/25V_8X
VIN
B2A
Rds=2.8mOhm
PQ8
HP8S36TB
DCR=4.2mOhm
PL1
1.5UH_10X10
B2A
(Peak 16.7A ,AVG 11.7)
OCP:20A ~ 21.7A
+1.5VSUS
ESR=10mOhm
PC114
390U/2.5V_105CS_E10
PC119
*10U/6.3V_6X
PR96
*E@2.2/F_6
PR155
*SHORT_4
PC90
*E@1000P/50V_4X
PR161
*0_8/S
PC120
*0.1U/10V_4X
+1.5VSUS_SRC
B2A
+1.5VSUS
{27,41,46} MAIND
MAIND
PQ1
AO6402A
+1.5V
(Peak 1.1A ,AVG 0.78A)
For XiangYun Layout House Use
Quanta Computer Inc.
PROJECT : Chief River
Size
Document Number
DDR1.5V
Rev
A1A
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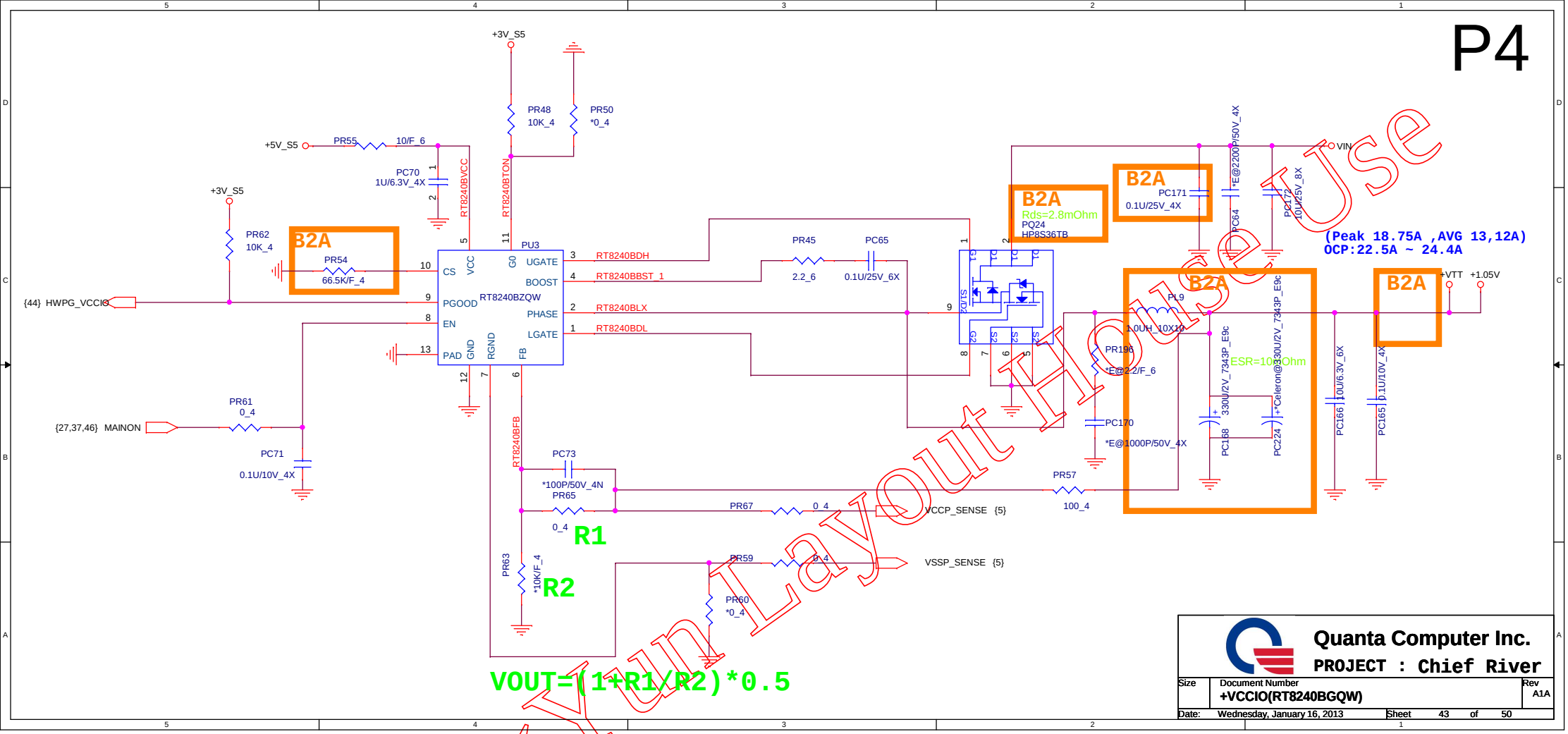
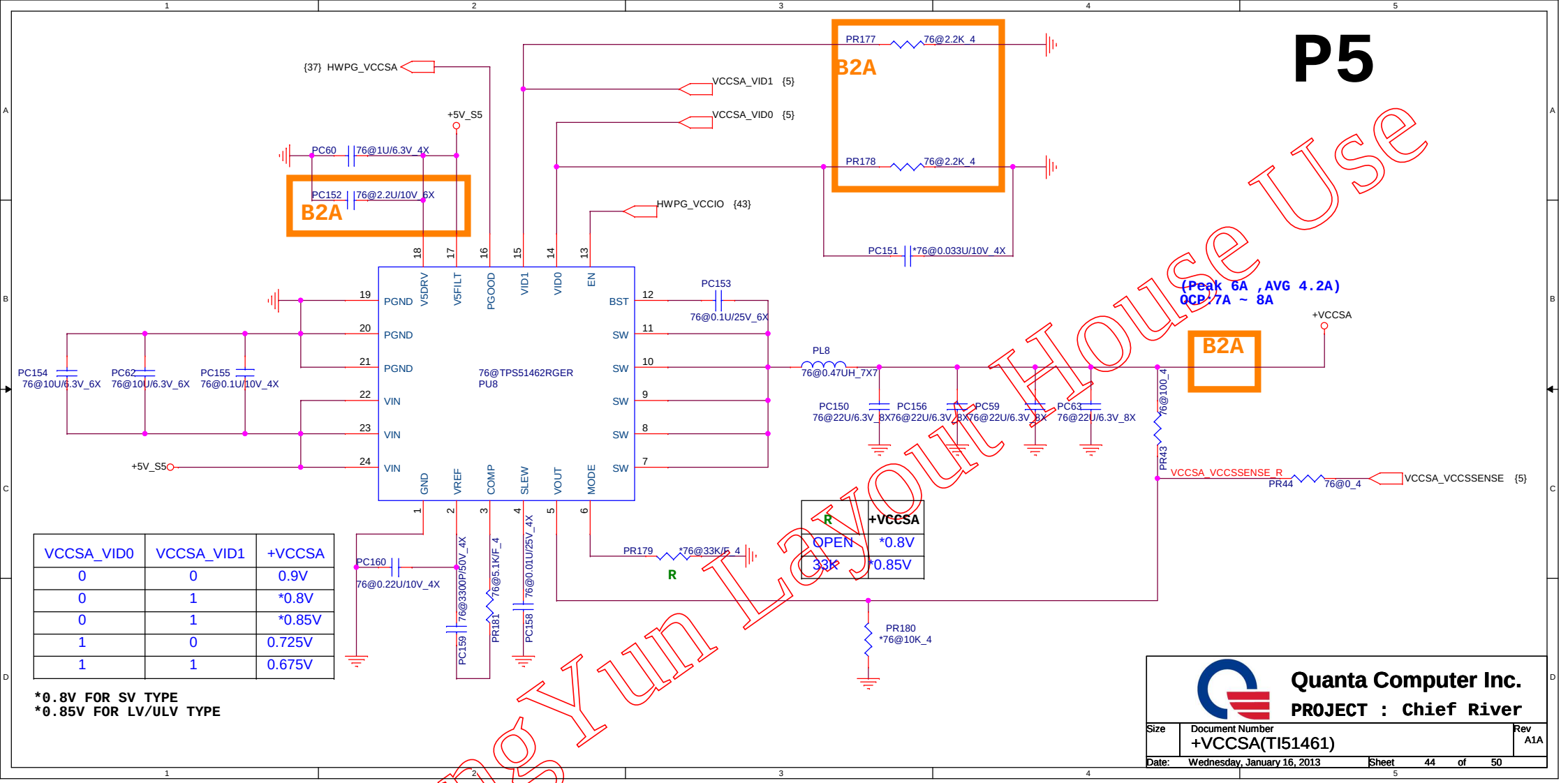
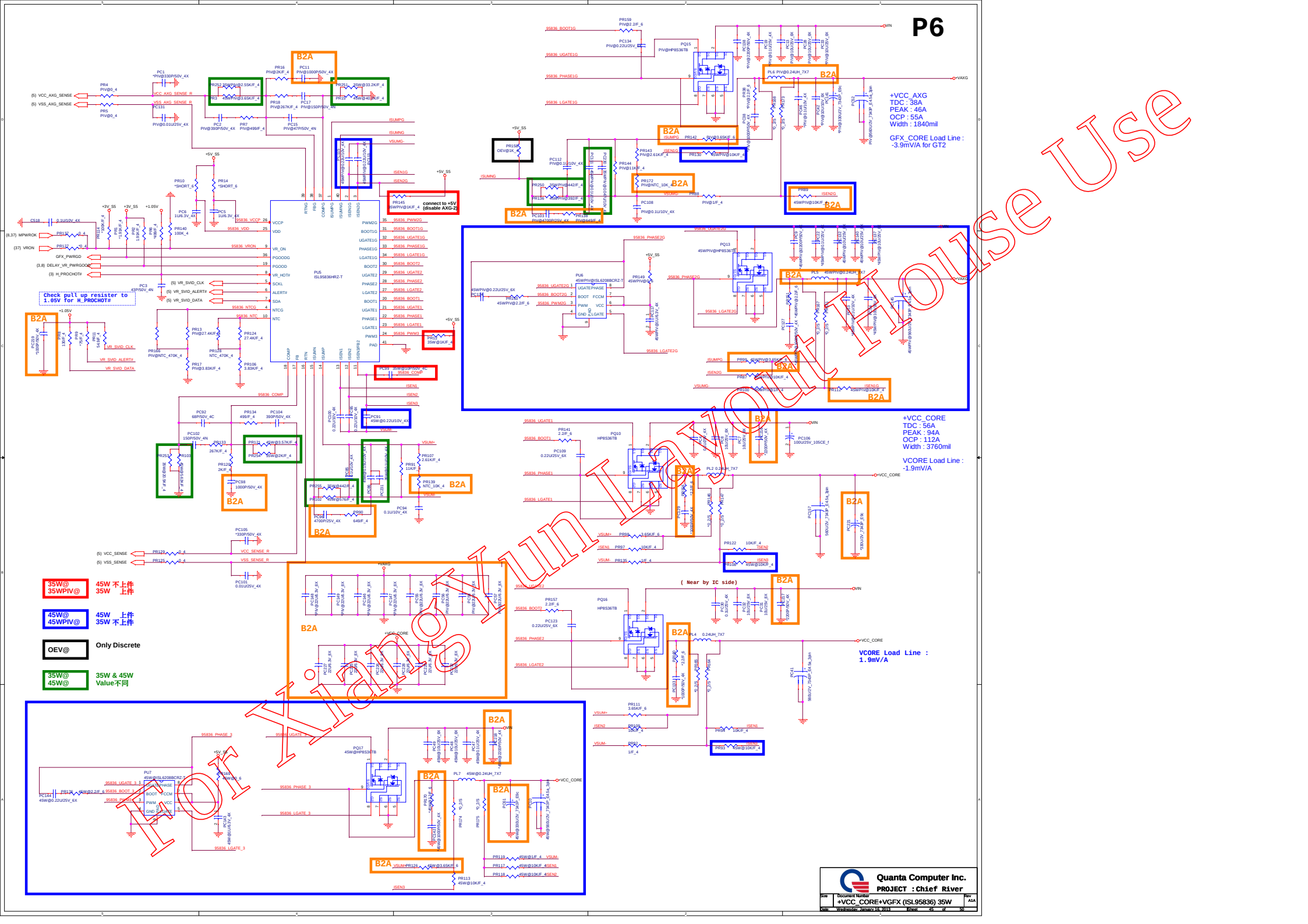
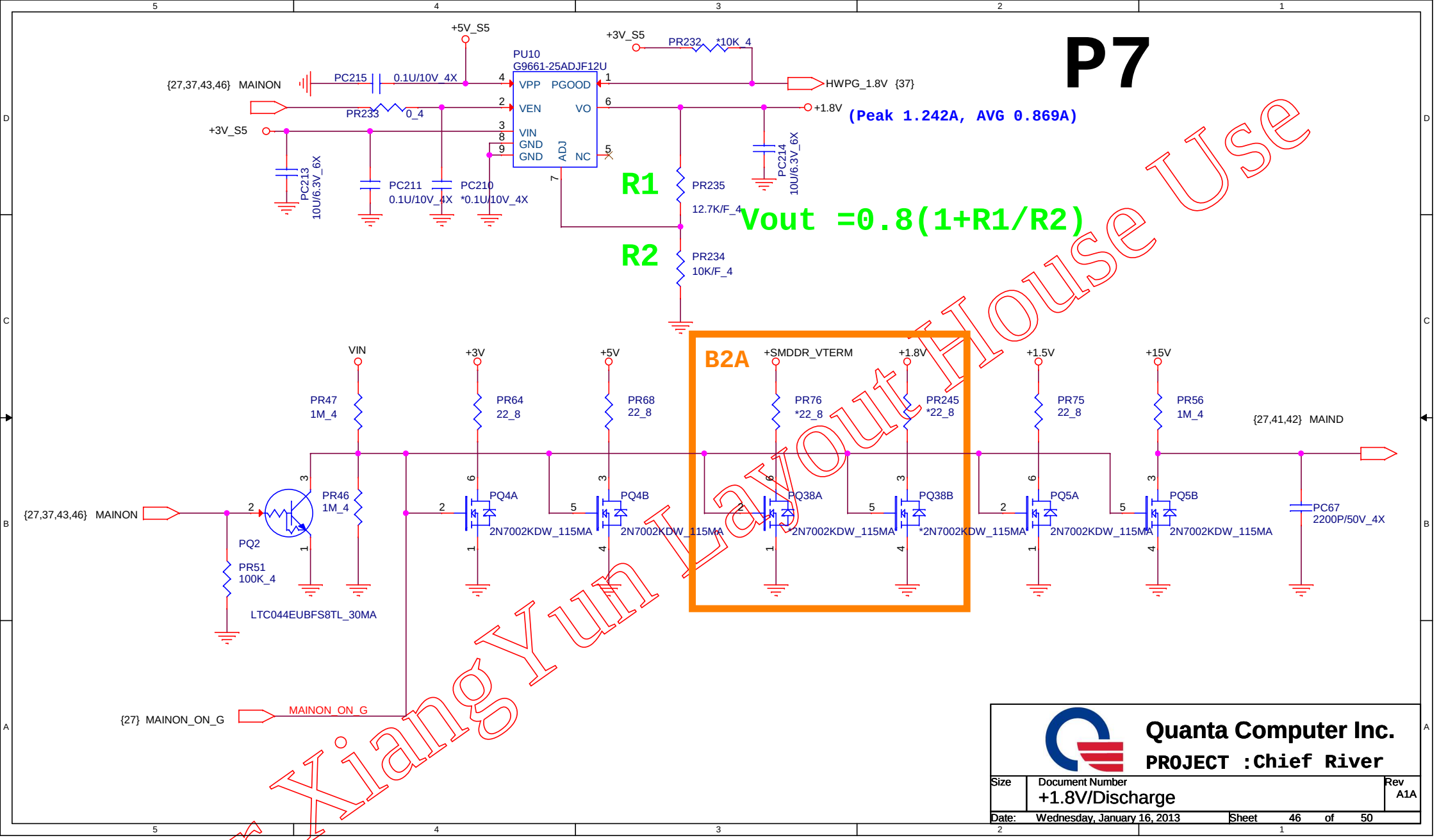


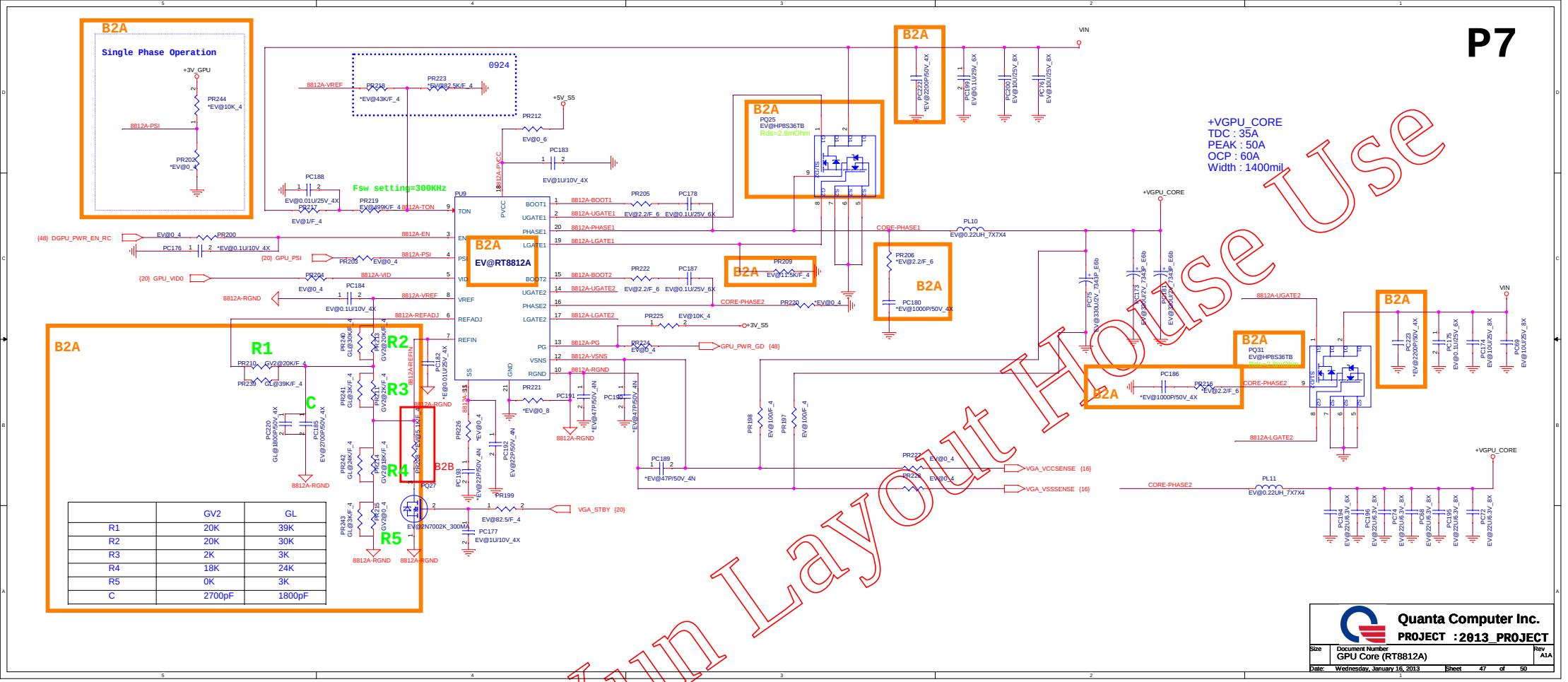



P6
+VCC_AXG
TDC : 38A
PEAK : 46A
OCP : 55A
Width : 1840mil
GFX_CORE Load Line :
-3.9mV/A for GT2
+VCC_CORE
TDC : 56A
PEAK : 94A
OCP : 112A
Width : 3760mil
VCORE Load Line :
-1.9mV/A
VCORE Load Line :
1.9mV/A
Check pull up resister to
1.05V for H_PROCHOT#
(Near by IC side)
35W@
35WPIV@
45W 不上件
35W 上件
45W@
45WPIV@
45W 上件
35W 不上件
OEV@
Only Discrete
35W@
45W@
35W & 45W
Value不同
Quanta Computer Inc.
PROJECT : Chief River
+VCC_CORE+VGFX (ISL95836) 35W
Wednesday, January 16, 2013
For Xiaolun Layout Use
For Xiaolun Layout House Use

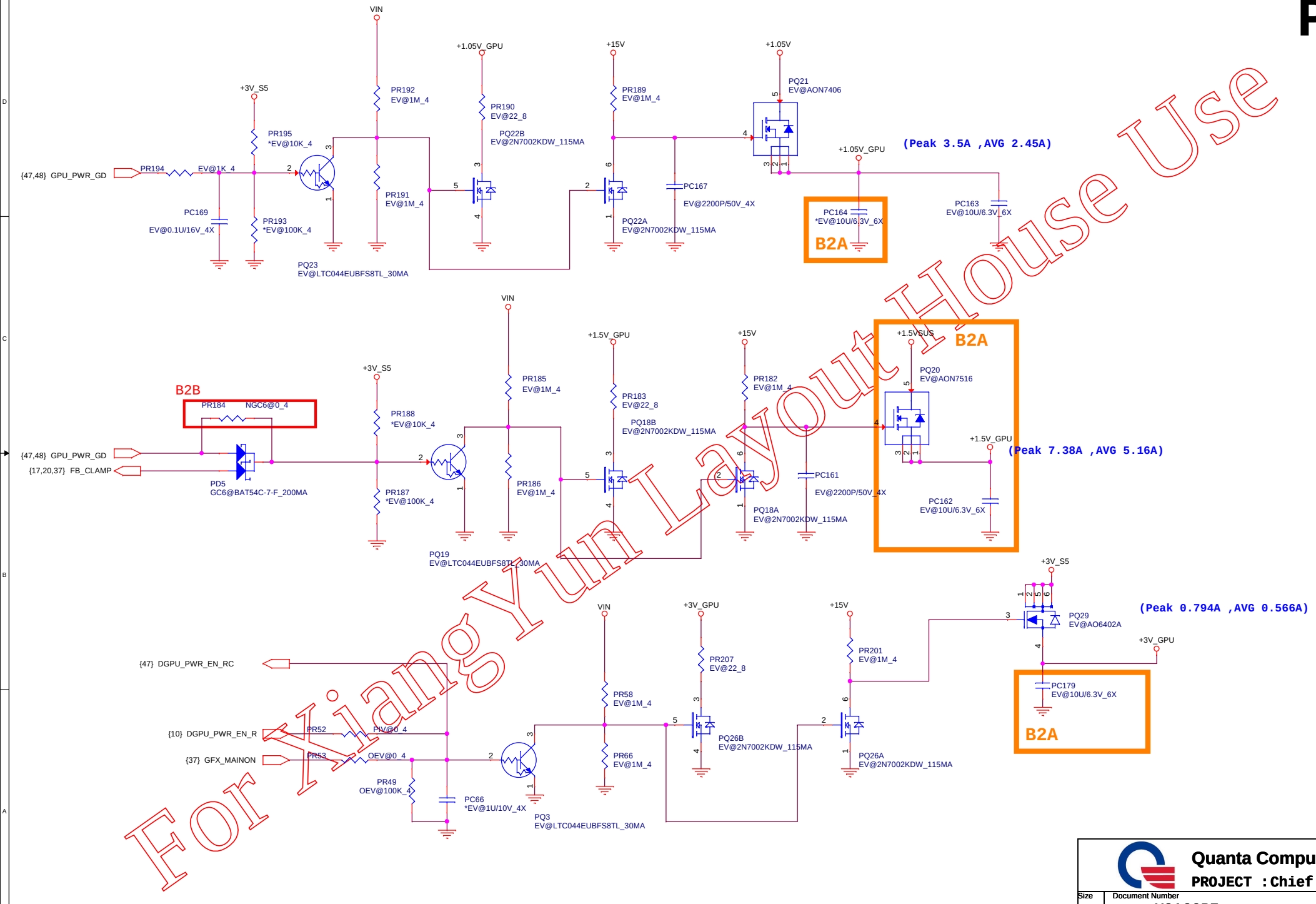
P7



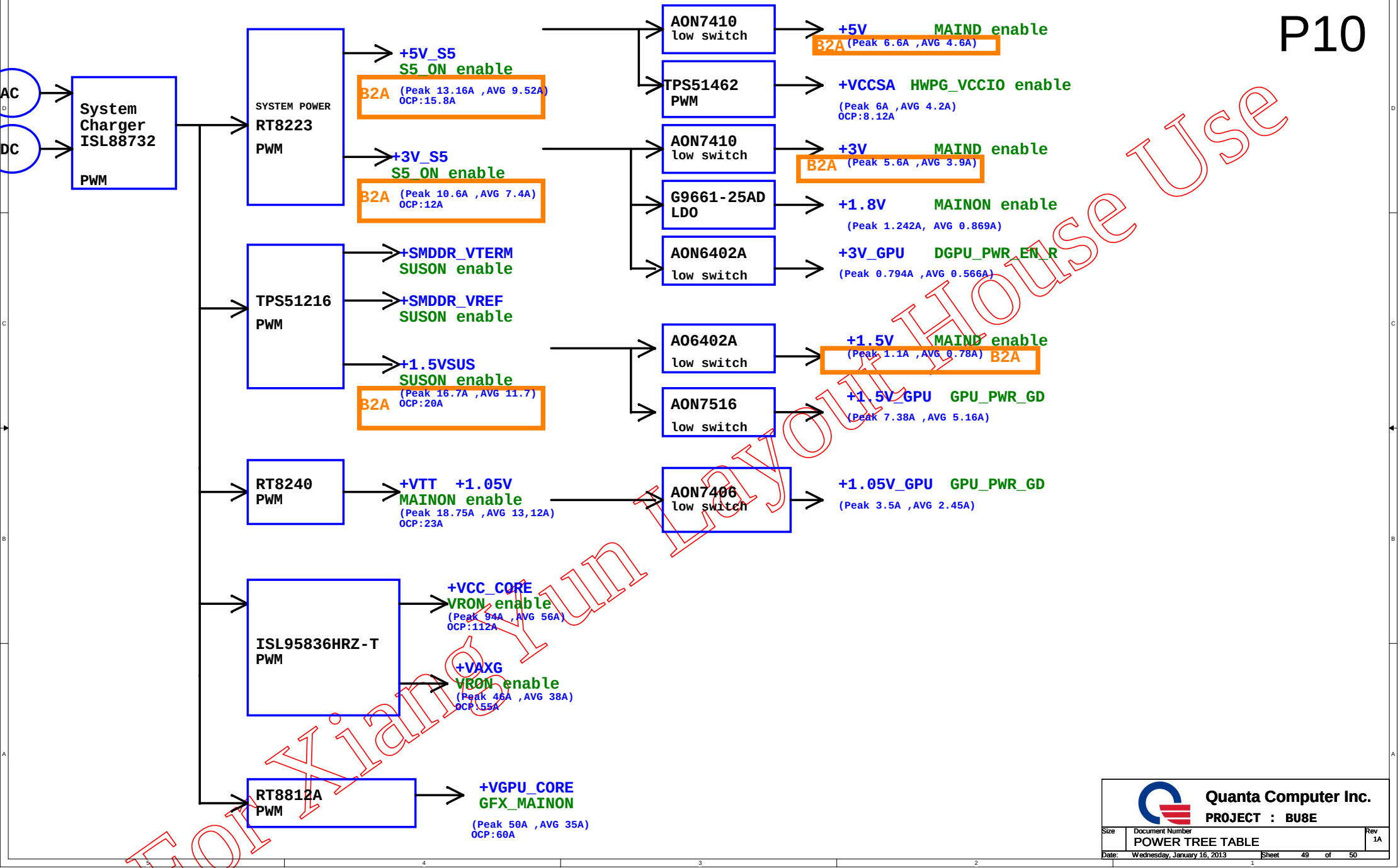
Quanta Computer Inc.		
PROJECT :Chief River		
Size	Document Number: +1.8V/Discharge	Rev: A1A
Date: Wednesday, January 16, 2013	Sheet 46 of 50	



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



Quanta Computer Inc.		
PROJECT : Chief River		
Size	Document Number: +VGACORE	Rev: A1A
Date: Wednesday, January 16, 2013	Sheet 48 of 50	



Quanta Computer Inc.
PROJECT : BU8E

Size	Document Number	Rev
	POWER TREE TABLE	1A

Date: Wednesday, January 16, 2013 Sheet 49 of 50

CHANGE LIST

Model	REV	
BD5 MB	A1A	First Release
	B2A	PAGE 3: Change C537,C538 size and stuff R761
		PAGE 5: add PR257
		PAGE 6: modify R142,Q19,R145,R141,Q20,R144 value for DDR3 VREF DQ (M3).
		PAGE 8: modify R735,R715,R395,R369,R397,R720 value to S3
		PAGE 9: change GPIO13 to BOARD_ID16,GPIO23 to BOARD_ID17
		PAGE 10: add USB port3 for Touch Panel function,add R766,R768,R755,R769,R770,R772,R767,R773,Q55,Q56 for S3,change C704,C708 to 12PF
		PAGE 11: change R406,R385,R743,R731,R401,R381,R778,R691,R700,R698,R306,R779,R780,R781,R405,R384 for BOARD_ID select
		PAGE 12: change C420,R295,R784,L14,R288,R785,R416,R796 value and change R786,R420,C470,R787,R421,C469 value for S3
		PAGE 16: change R180,R179,Q25,Q24,Q57 value for CLK PEG
		PAGE 18: change C725,C726,C727 value,and add R788,R789 for EDP PD
		PAGE 19: add R790 for XTAL,and change R249,R250 value
		PAGE 20: change R251,R612,R252,R791,R792 value
		PAGE 21: add R793 for co-lay
		PAGE 22: change C312,C639 value
		PAGE 28: change R794,F3,U25,D21 value for HDMI
		PAGE 29: change R14,R16,R7,MR1,CN15,CN8,F1,R472,R470,R473,R471 value
		PAGE 30: change R499,R797,Q41,R466 value for AOAC
		PAGE 31: add D7,D22,D23,D24,D25,D28,D29,D31,D30,D32,D33,D34,D35 for ESD,change C380,C381,CN18,CN17,R316,R395,U12,C384,C398,C699,R315,Q34 value
		PAGE 33: change CN14 value
		PAGE 34: add D36,D37,D38,D39,D40,D41,D42,D43 for ESD
		PAGE 35: change C234,C221,C190,C184,C174,C168 value,and add C730,C728,C729,C731 for EMI,add D44,D45,D46,D47 for ESD
		PAGE 36: change R413,R394,R389,R390,R391,R392,R393,C448,C441,C440,C442,C443 value
		PAGE 37: change R80,Q4 value,add R799,R798 for STRAP select
		PAGE 38: change CN1,CN2,CN5,CN4,R95,Q10 value and change C218 value for EMI,and add L41,L42,C723,C724,CN2021,R777,R776,R775,R774 for Touch PAD Panel function
		PAGE 39: change LED2 symbol
	B2B	PAGE 20: change R570 value
		PAGE 22: change D4 value
	C3A	PAGE 15: change C65 size to 0402
		PAGE 31: change RN10,RN11,RN12,RN13 pin define
		PAGE 34: change C490,C501 size to 0402
		PAGE 36: change C476 size to 0402

MODEL BD5

PAGE	FROM	To
1		
2		
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18		
19		
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43		

DOC NO. 204

PROJECT MODEL :	BD5	APPROVED BY:	Kent Su	DATE:	2012/12/14
PART NUMBER:		DRAWING BY:	Kent Su	REVISON:	

Quanta Computer Inc.
PROJECT : BD5

Size | Document Number: Change list | Rev: D2A
Date: Wednesday, January 16, 2013 | Sheet 50 of 50