ZQ2B SOLE UMA SYSTEM DIAGRAM

AMD Smarter Choice
Danube Platform
(Main Stream)

VER : 1A

BOM P/N	Description	Model	SidePort	ODD
31ZQ2MB00A0	ZQ2B 6L JM MB (W/GRN,SAM,W/O CPU)ASSY	JM	Sansung	Slim
31ZQ2MB00E0	ZQ2B 6L JM MB (W/GRN,HYU,W/O CPU)ASSY	JM	Hynix	Slim
31ZQ2MB00H0	ZQ2B 6L JV MB (W/GRN,W/O CPU,VRAM)ASSY	JV	No Support	Standard

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

IV@ -----> iGPU
SP@ -----> Option Notice
SIDE@ -----> SidePort VRAM
GA@ ----> Green Adapter (Default stuff)

Sideport-L75,L76,R583,R392,C832,R455,R550,R502
NB A11-R105,R108
SB A12-R267,R271
JV/JM-CN16,R450,R456
EC-D8,D27
UMA-R461
VRAM-R358,R359,R360,R363,R365,R72

- CHARGER (ISL88731A) PAGE 26
- AMD CPU CORE (ISL6265) PAGE 28 — CPU
- NB_CORE (UP6111AQDD) PAGE 30 — NB
- 0.9V/DDR 1.5V(RT8207) PAGE 31
- SYSTEM 5V/3V (RT8206) PAGE 27
- 1.1V(UP6111AQDD) PAGE 29
- Discharge /Thermal protec PAGE 32

DDR3- SODIMM1 PAGE 5 — DDR3 channel A
DDR3- SODIMM2 PAGE 5 — DDR3 channel B

AMD Champlain
S1G4 Processor
35mm X 35mm
638P (PGA) 35W
PAGE 2,3,4

CPU THERMAL SENSOR (Reserve Only) PAGE 4

PWM FAN SCH. PAGE 24 — CPU (PROCHOT), E.C. (CPUFAN#)

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

From SB CLK GEN
SB820M PAGE 10
CLK_PCI_775
PCLK_DEBUG
25MHz
32.768KHz

CPU SideBand TemperatureSense I2C

HT3
1.8GHz

PCI-Expresss

NORTH BRIDGE
RS880M GFX Engine: 500MHz
A11
21mm X 21mm, 528pin BGA
TDP: 13W
0.95 ~ 1.1V
PAGE 6,7,8,9

Side Port — gDDR3 VRAM DDR III-800MHz PAGE 6
HDMI — HDMI PAGE 16
CRT — CRT PAGE 15
LVDS — LVDS PAGE 23

A-LINK

P0 — LAN Atheros PCIE-LAN AR8151 (10/100/1000) PAGE 17 — 25MHz
RJ45 PAGE 17
P2 — Mini PCI-E Card (Wireless LAN) PAGE 18

SOUTH BRIDGE
SB820M
A12
23mm X 23mm, 605pin BGA
No PCI I/F
TDP: 4.9W
PAGE 10,11,12,13, 14

SATA - HDD PAGE 19 — SATA0 150MB 3 Gb/s
SATA - ODD PAGE 19 — SATA1 150MB 3 Gb/s

P0 — USB2.0 Port on board x1 PAGE 30
P9 — Blue Tooth PAGE 22
P13 — Web-Camera PAGE 15
P4 — Mini Card WLAN & Debug PAGE 18 — PCLK_DEBUG
P10 — CardReader AU6347 PAGE 21 — 12MHz
EC

P8, 11, 12 — USB BOARD USB2.0 Ports x3 PAGE 22
Power BOARD PAGE 22 — KBC
Switch BOARD PAGE 22 — KBC
There are three Daughter boards.

LPC
Azalia

CLK_PCI_775
Winbond KBC
NPCE781L &
Green Adapter
PAGE 25
CPU SideBand TemperatureSense I2C

Audio CODEC
RTL ALC271X
PAGE 20

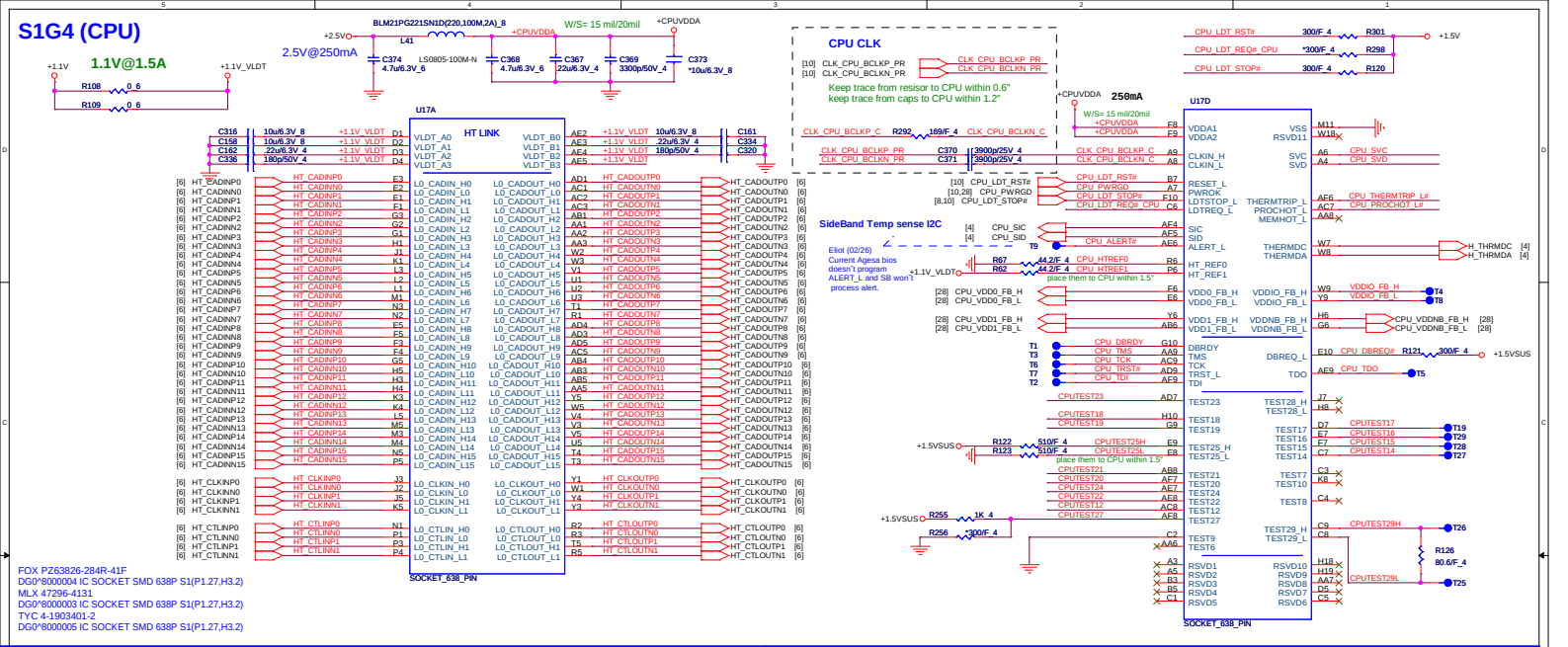
Green ADP. PAGE 25
Keyboard TouchPad PAGE 24
SPI ROM PAGE 25
Digital MIC PAGE 15 & 20
AUDIO CONN (H.P./ MIC) PAGE 20
Speaker CN PAGE 20

SSID: 035E
SVID: 1025

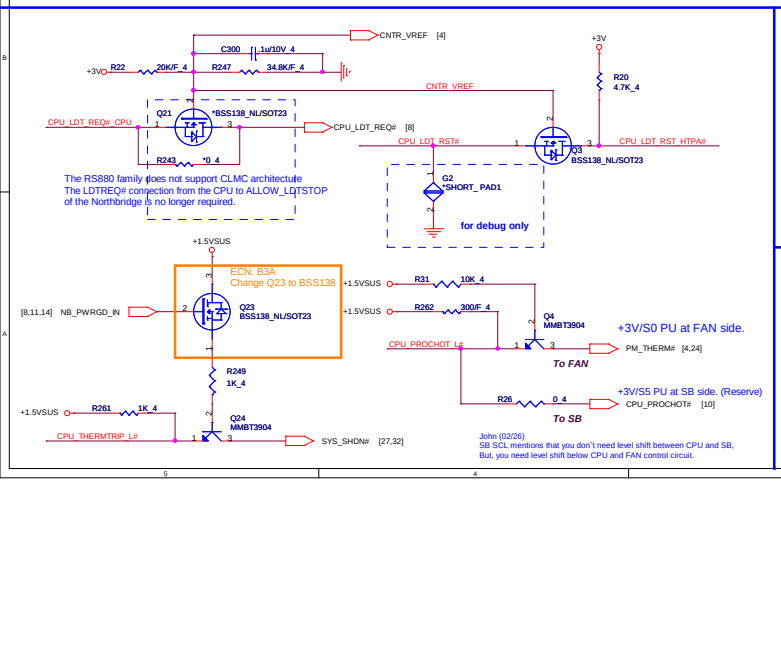
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date: Thursday, March 04, 2010	Sheet 1 of 36	

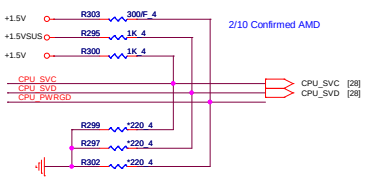
S1G4 (CPU)



FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)



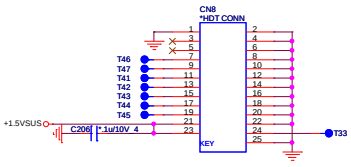
Serial VID



VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

HDT Connector



CPUTEST24	R258	1K_4
CPUTEST23	R260	1K_4
CPUTEST20	R259	1K_4
CPUTEST22	R257	1K_4
CPUTEST12	R34	1K_4
CPUTEST15	R127	*300/F_4
CPUTEST14	R128	*300/F_4
CPUTEST19	R98	1K_4
CPUTEST18	R99	1K_4
CPUTEST21	R35	1K_4

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	S1G4 HT,CTL I/F 1/3	1A
Date: Thursday, March 04, 2010	Sheet 2 of 36	

35W CPU support 0.9V
45W CPU support 1.05V

VDDR=> 0.9V support 1066 / 800 DDR
VDDR= >1.05V support 1333 / 1066 / 800 DDR

VDDR=>1.75A

Processor Memory Interface

PLACE THEM CLOSE TO CPU WITHIN 1"

U17B — MEM:CMD/CTRL/CLK

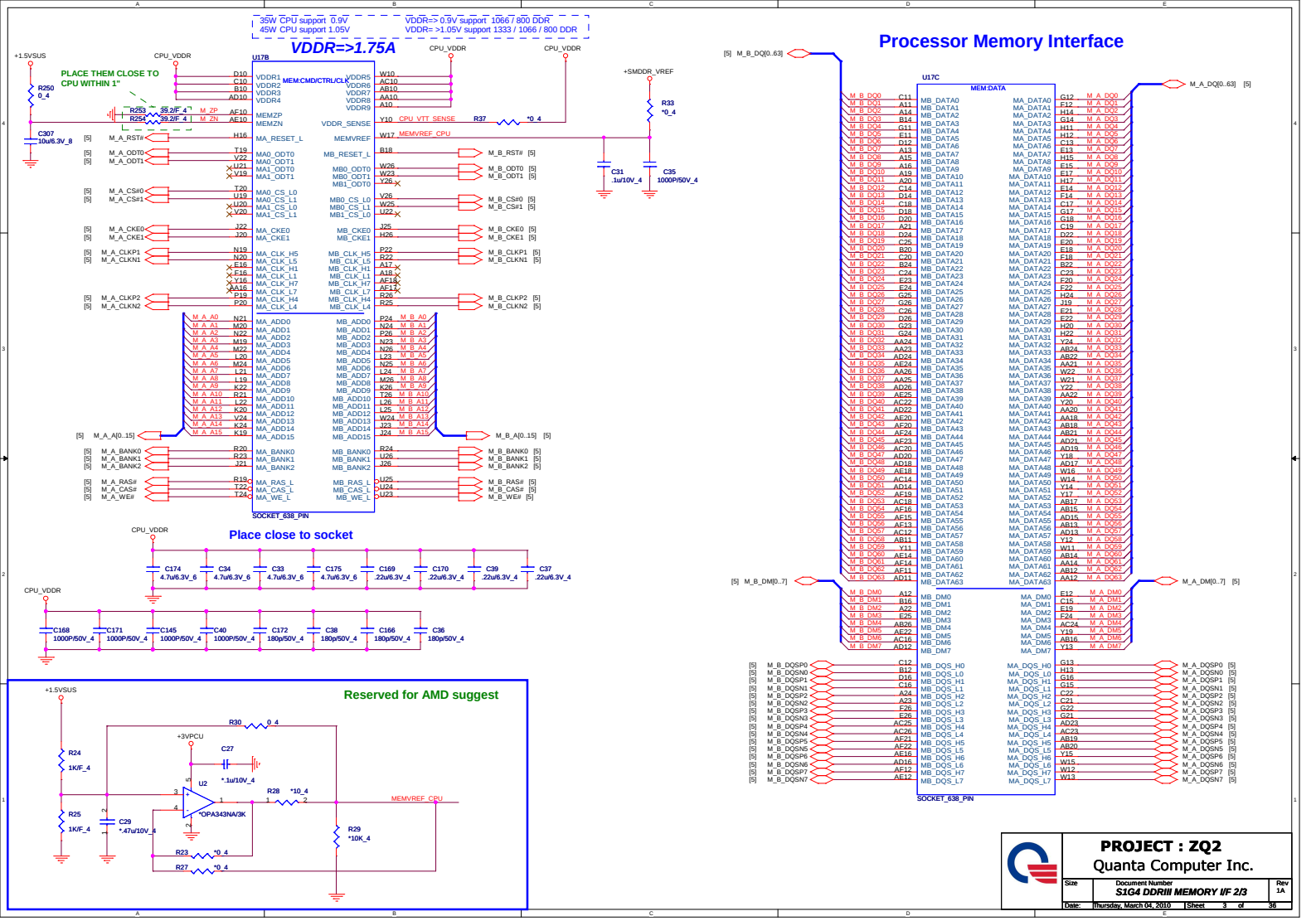
U17C — MEM:DATA

SOCKET_638_PIN

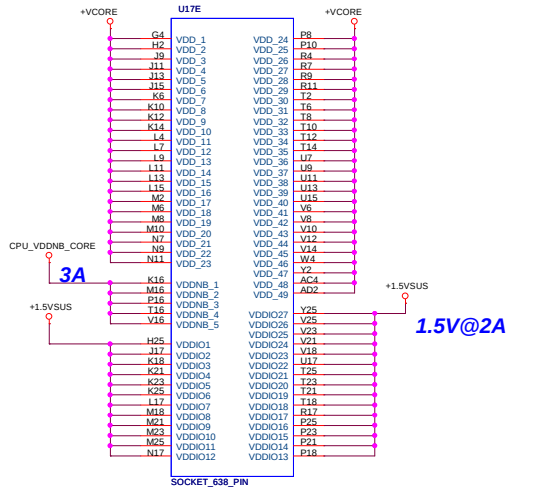
Place close to socket

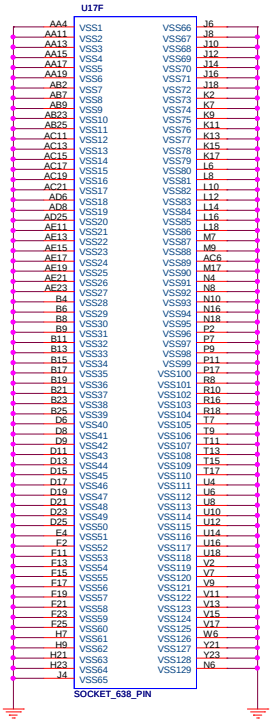
Reserved for AMD suggest

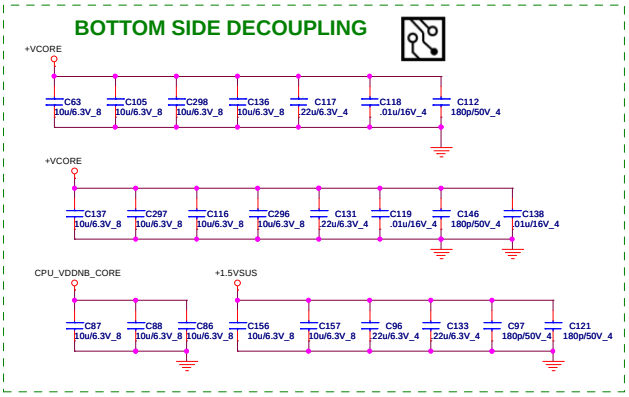
*OPA343NA/3K

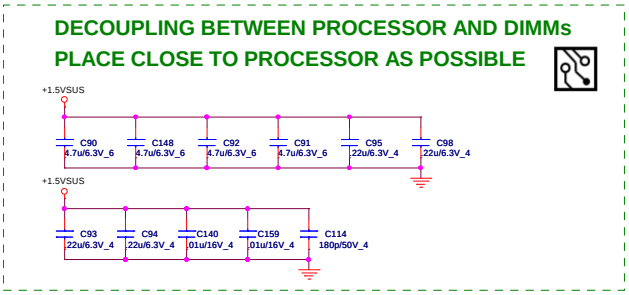


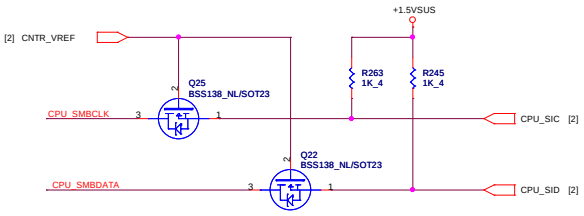
PROJECT : ZQ2	
Quanta Computer Inc.	
Size	Document Number: SIG4 DDRIII MEMORY I/F 2/3 — Rev: 1A
Date: Thursday, March 04, 2010	Sheet 3 of 36



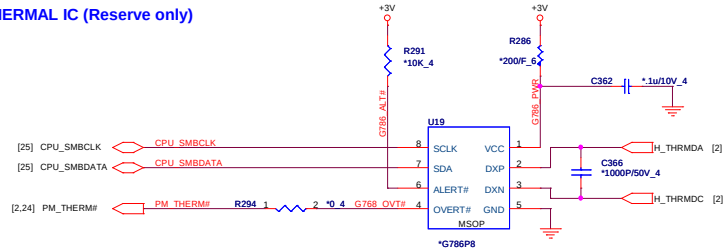








PROCESSOR POWER AND GROUND



PROJECT : ZQ2
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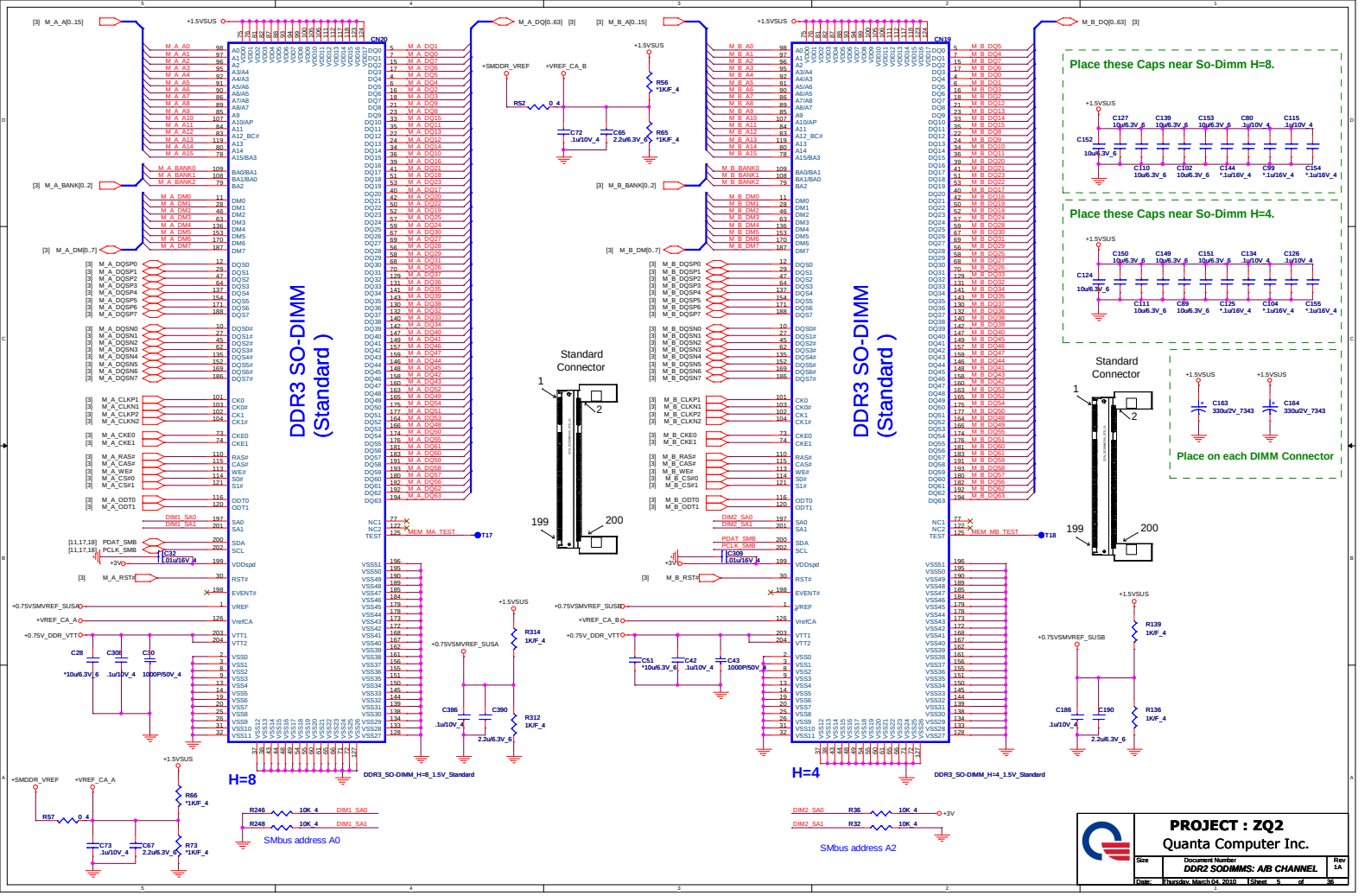
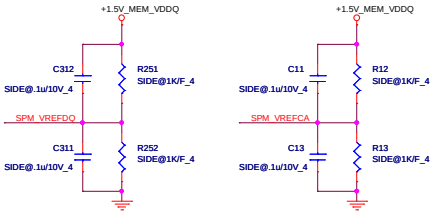
Size	Document Number	Rev
	S1G4 PWR & GND 3/3	1A
Date: Thursday, March 04, 2010	Sheet 4 of 36	


DDR3 SO-DIMM (Standard)
H=8
H=4
Standard Connector
Place these Caps near So-Dimm H=8.
Place these Caps near So-Dimm H=4.
Place on each DIMM Connector
SMbus address A0
SMbus address A2
PROJECT : ZQ2
Quanta Computer Inc.
DDR2 SODIMMS: A/B CHANNEL
Thursday, March 04, 2010

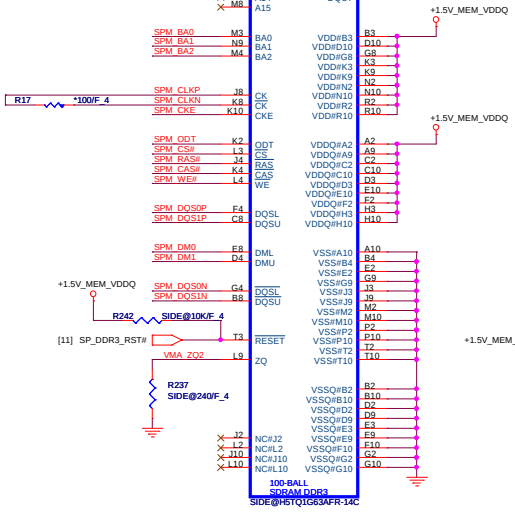
SIDE PORT

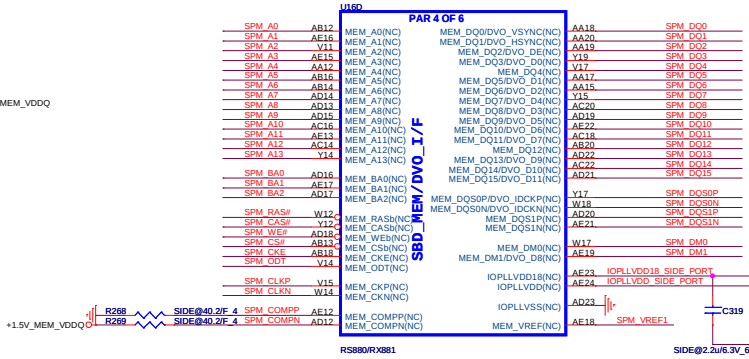


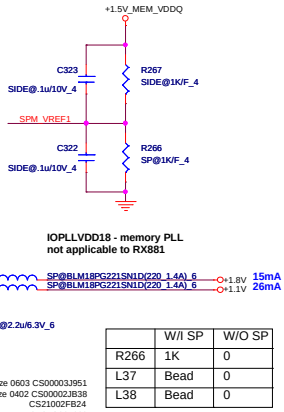
Signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

This block is for Side-Port only



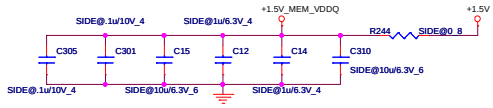




	W/I SP	W/O SP
R266	1K	0
L37	Bead	0
L38	Bead	0

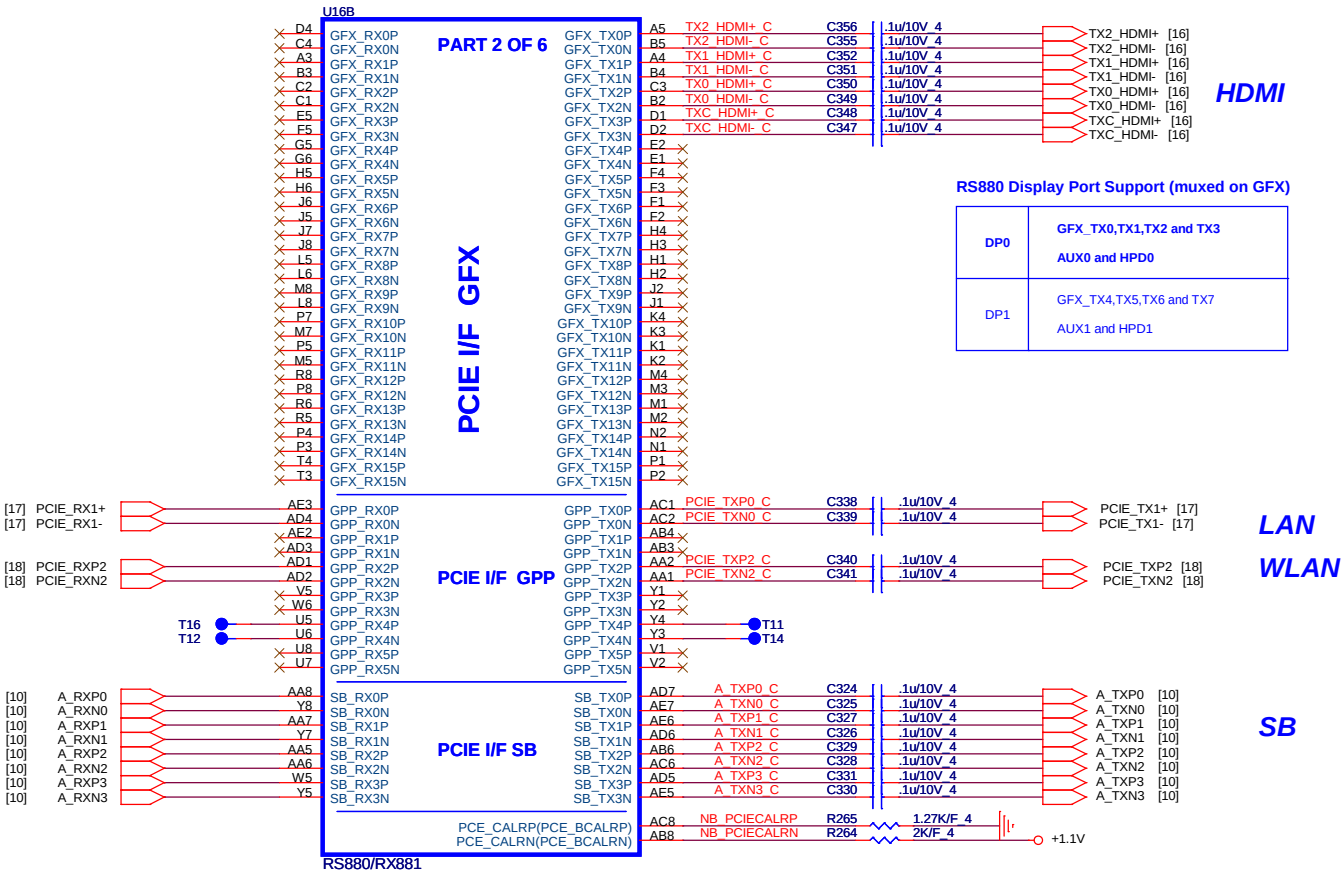
0ohm size 0603 CS00003J951
size 0402 CS00002JB38
1K ohm CS21002FB24
Bead CX8PG221003

40 mil~50 mil



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
Date: Thursday, March 04, 2010	Sheet 6 of 36	



PROJECT : ZQ2			
Quanta Computer Inc.			
Size	Document Number		Rev
	RS880M-PCIE I/F 2/4		1A
Date:	Thursday, March 04, 2010	Sheet 7 of	36

For Check list JTAG

R279 *4.7K_4 NB_PWRGD_IN
+3V
R88 *4.7K_4 INT_EDIDDATA
R96 *4.7K_4 INT_EDIDCLK
+3V
R94 *4.7K_4 HDMI_DDC_DATA

For A11 version

(02/10) Don`t need 49.9 ohm PD.

R47 *49.9/F_4 CLK_SBLINKP
R48 *49.9/F_4 CLK_SBLINKN

All RS880 variants do not support analog TV-out functionality. As such, Y, C_Pr, and COMP_Pb

U18C
PART 3 OF 6
RS880/RX881

+3V_AVDD_NB
+1.8V_AVDDDI_NB
+1.8V_AVDDQ_NB
AVDD1(NC) F12
AVDD2(NC) E17
AVDDDI(NC) F14
AVSSDI(NC) G15
AVDDQ(NC) H15
AVSSQ(NC) H14
C_Pr(DFT_GPIO5) E17
Y(DFT_GPIO2) F17
COMP_Pb(DFT_GPIO4) F15

CRT/TVOUT

[15] INT_CRT_RED R102 140/F_4
[15] INT_CRT_GRE R103 150/F_4
[15] INT_CRT_BLU R104 150/F_4
RED(DFT_GPIO0) G18
REDb(NC) G17
GREEN(DFT_GPIO1) E18
GREENb(NC) E19
BLUE(DFT_GPIO3) F19
BLUEb(NC) F18

VGA

[15] INT_CRT_HSYNC
[15] INT_CRT_VSYNC
[15] INT_DDCDATA
[15] INT_DDCCLK
R79 715/F_6
INT_CRT_HSYNC
INT_CRT_VSYNC
DAC_HSYNC(PWM_GPIO4) A11
DAC_VSYNC(PWM_GPIO6) B11
DAC_SDA(PCE_TCALRN) E8
DAC_SCL(PCE_RCALRN) F8
DAC_RSET_NB
DAC_RSET(PWM_GPIO1) G14

TXOUT_L0P(NC) A22
TXOUT_L0N(NC) B22
TXOUT_L1P(NC) A21
TXOUT_L1N(NC) B21
TXOUT_L2P(NC) B20
TXOUT_L2N(NC) A20
TXOUT_L3P(NC) A19
TXOUT_L3N(NC) B19
LA_DATAP0 [15]
LA_DATAN0 [15]
LA_DATAP1 [15]
LA_DATAN1 [15]
LA_DATAP2 [15]
LA_DATAN2 [15]
TXOUT_L0P(DBG_GPIO0)
TXOUT_L0N(DBG_GPIO2)
TXOUT_U0P(NC) B18
TXOUT_U0N(NC) A18
TXOUT_U1P(PCIE_RESET_GPIO3) A17
TXOUT_U1N(PCIE_RESET_GPIO2) B17
TXOUT_U2P(NC) C20
TXOUT_U2N(NC) D21
TXOUT_U3P(PCIE_RESET_GPIO5) D18
TXOUT_U3N(NC) D19
TXCLK_LP(DBG_GPIO1) B16
TXCLK_LN(DBG_GPIO3) A16
TXCLK_UP(PCIE_RESET_GPIO4) D16
TXCLK_UN(PCIE_RESET_GPIO1) D17
LA_CLK [15]
LA_CLK# [15]

PLL PWR LVTM

20mA +1.8V_VDDA18HTPLL H17
120mA +1.8V_VDDA18PCIEPLL D7
VDDA18HTPLL
VDDA18PCIEPLL1 E7
VDDA18PCIEPLL2
VDDTP18(NC) A13
VSSLTP18(NC) B13
+1.8V_VDDLTP18_NB
15mA
VDDLT18_1(NC) A15
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14
VDDLT33_2(NC) B14
+1.8V_VDDLT_18_NB
300mA
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

PM

[10,25] A_RST#_SB
[2,11,14] NB_PWRGD_IN
SYSRESETb D8
POWERGOOD A10
LDTSTOPb C10
ALLOW_LDTSTOP C12
NB_LDT_STOP#
NB_ALLOW_LDTSTOP

CLOCKs

[10] CLK_NB_HTREFP_PR
[10] CLK_NB_HTREFN_PR
HT_REFCLKP C26
HT_REFCLKN C24
[10] CLK_NB_REF_CLKP
[10] CLK_NB_REF_CLKN
CLK_NB_REF_CLKP
CLK_NB_REF_CLKN
REFCLK_P(OSCIN) E11
REFCLK_N(PWM_GPIO3) F11
R46 4.7K_4
R45 4.7K_4
NBGFX_CLKP T2
NBGFX_CLKN T1
GFX_REFCLKP
GFX_REFCLKN
T15
T13
GPP_REFCLKP U1
GPP_REFCLKN U2
GPP_REFCLKP
GPP_REFCLKN
[10] CLK_SBLINKP
[10] CLK_SBLINKN
V4
V2
GPPSB_REFCLKP(SB_REFCLKP)
GPPSB_REFCLKN(SB_REFCLKN)
LVDS_DIGON(PCE_TCALRP) E9
LVDS_BLON(PCE_RCALRP) E7
LVDS_ENA_BL(PWM_GPIO2) G12
INT_LVDS_DIGON [15]
INT_DPST_PWM [15]
INT_LVDS_BLON [15]

MIS.

[16] HDMI_DDC_DATA
[16] HDMI_DDC_CLK
I2C_DATA A9
I2C_CLK B9
DDC_DATA/AUX0N(NC) B8
DDC_CLK/AUX0P(NC) A8
AUX1P(NC) B7
AUX1N(NC) A7
DDC_DATA & DDC_CLK Not applicable to RX881
STRP_DATA B10
RSVD G11
AUX_CAL(NC) C8
TMDS_HPD(NC) D9
HPD(NC) D10
INT_HDMI_HPD [16]
TVCLKIN(PWM_GPIO5) D12
SUS_STAT# NB
R111 *0/short_4
SUS_STAT# [11]
THERMALDIODE_P AE8
THERMALDIODE_N AD8
TESTMODE D13
TEST_EN
R112 *3K_4
R87 1.8K/F_4
Made provision for external pull-down which is not installed by default. Pulled up externally for bypassing EEPROM strapping and using default values.
+30] +NB_CORE_ON
+NB_CORE_ON
T74
RS880_AUX_CAL

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	V
0 Enable	

INT_CRT_VSYNC R277 3K_4 +3V

RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available

0 = Memory Side port available

Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

INT_CRT_HSYNC R276 *SP@3K_4 +3V
R100 SIDE@3K_4

For extrnal EEPROM Debug only

RS780/RX780/RS880

+NB_CORE_ON R278 2K/F_4

Display Port interface from PCIeGraphics (RS880/rs880M only)

RS880_AUX_CAL R282 *150/F_4

RS880M --- ADD

+3V L11 BLM18PG221SN1D(220_1.4A)_6 +3V_AVDD_NB
C120 *10u/6.3V_8
C123 2.2U/6.3V_6
AVDD-DAC Analog not applicable to RX780

+1.1V L39 BLM18PG221SN1D(220_1.4A)_6 +1.1V_PLLVDD
C359 2.2U/6.3V_6
PLLVDD - Graphics PLL not applicable to RX780

+1.8V L15 BLM18PG221SN1D(220_1.4A)_6 +1.8V_VDDLTP18_NB
C135 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

L40 BLM21PG221SN1D(220,100M,2A)_8 +1.8V_VDDLT_18_NB
C360 4.7u/6.3V_6
C357 .1u/10V_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

+1.8V R86 0_6 +1.8V_AVDDDI_NB
C113 .1u/10V_4
AVDDI-DAC Digital not applicable to RX780

+1.8V L13 BLM18PG221SN1D(220_1.4A)_6 +1.8V_PLLVDD18
C147 *10u/6.3V_8
C128 4.7u/6.3V_6
PLLVDD18 - Graphics PLL not applicable to RX780

L9 BLM18PG221SN1D(220_1.4A)_6 +1.8V_AVDDQ_NB
C108 2.2U/6.3V_6
AVDDQ-DAC Bandgap Reference not applicable to RX780

+1.8V
20mils width
VDDA18PCIEPLL -PCIE PLL
L10 BLM18PG221SN1D _6 +1.8V_VDDA18PCIEPLL
C122 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL
20mils width
L14 BLM18PG221SN1D _6 +1.8V_VDDA18HTPLL
C106 2.2U/6.3V_6

+1.8V
9/16 need modify PN
R107 2.2K_4
DDR3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor on the Northbridge side.

+1.8V
U16
Open Drain
74LVC07
[2,10] CPU_LDT_STOP#
NB_LDT_STOP#

R285 1K_4 +1.8V
[2] CPU_LDT_REQ#
R284 *0_4
NB_ALLOW_LDTSTOP
[10] ALLOW_LDTSTOP
R283 0_4

The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.

PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
RS880M-SYSTEM I/F 3/4
Rev 1A
Date: Thursday, March 04, 2010
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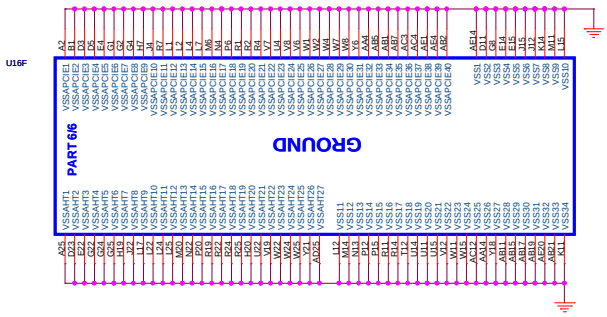
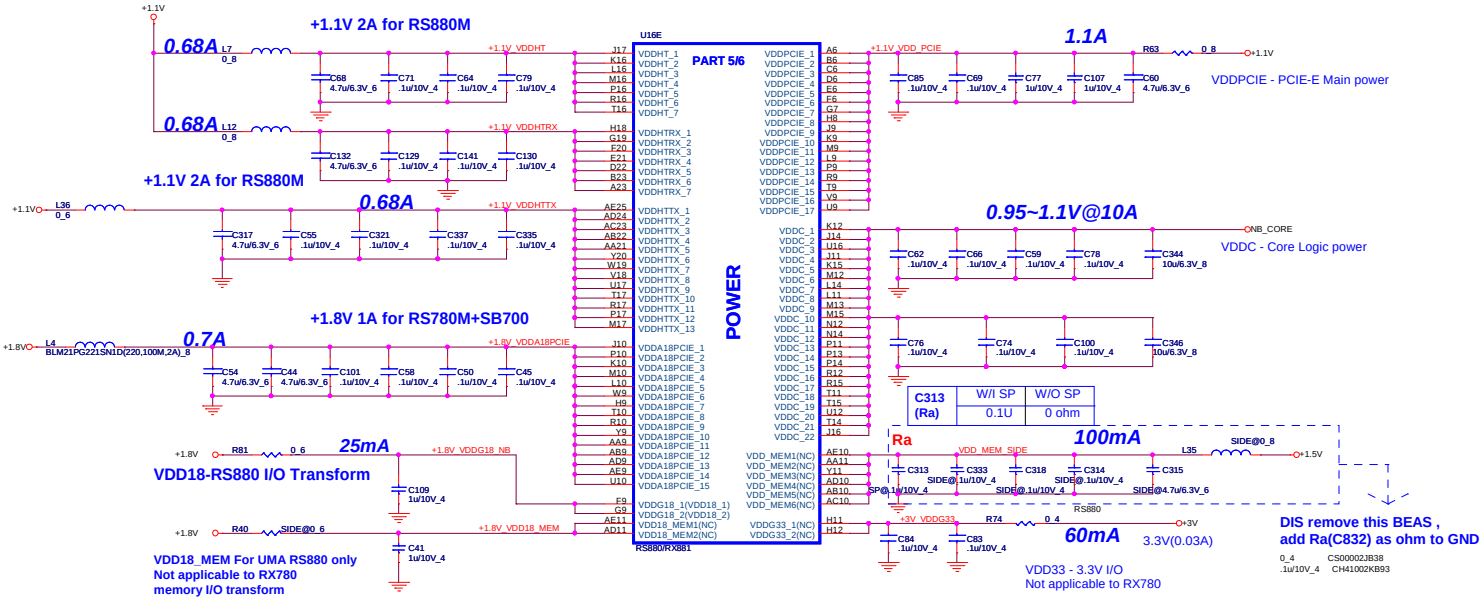
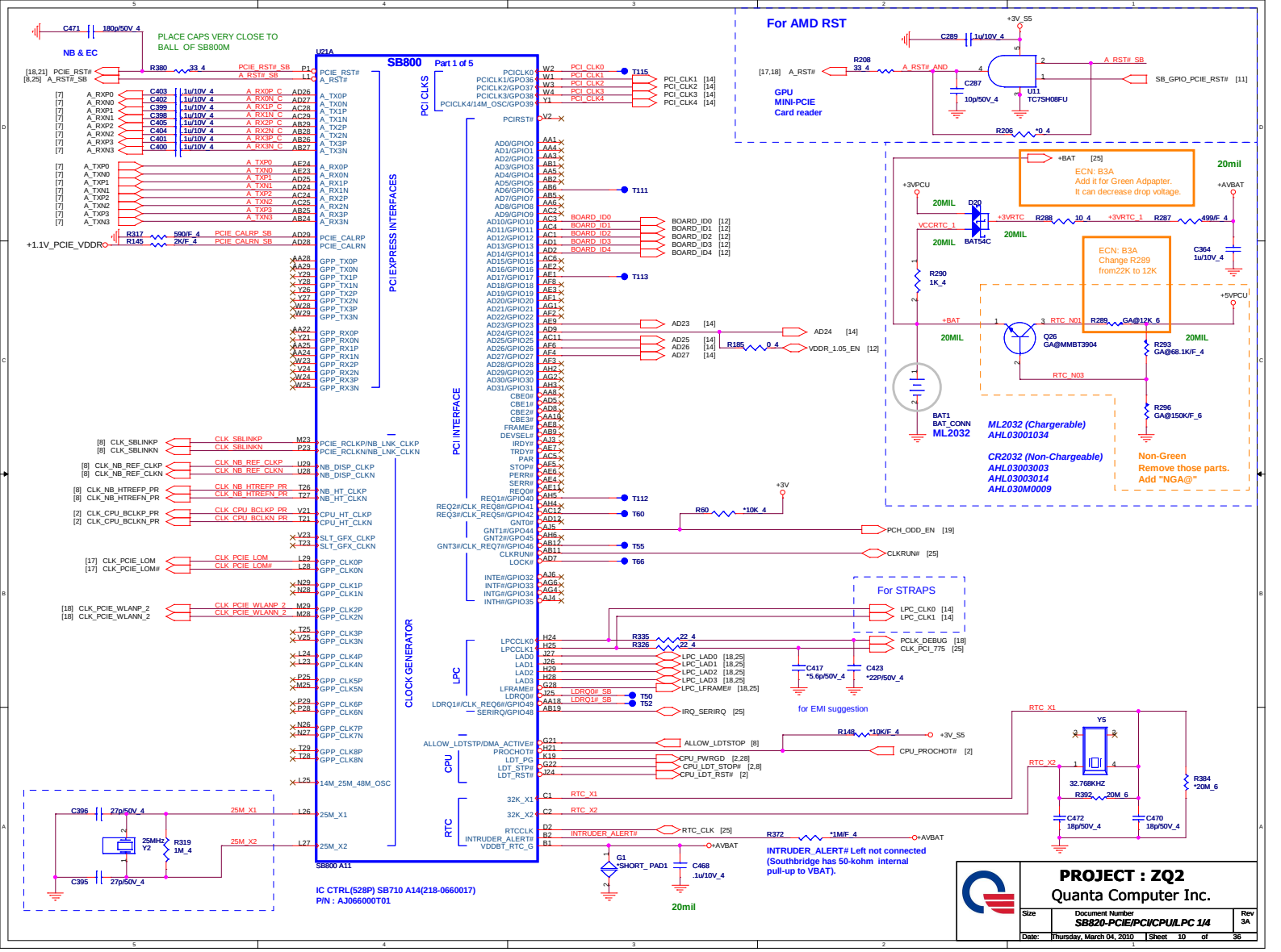




PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number: RS880M-POWER4/4	Rev: 1A
Date: Thursday, March 04, 2010	Sheet 9 of 36	


For AMD RST
GPU
MINI-PCIE
Card reader
NB & EC
PLACE CAPS VERY CLOSE TO
BALL OF SB800M
SB800
Part 1 of 5
U21A
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
ECN: B3A
Add it for Green Adpapter.
It can decrease drop voltage.
ECN: B3A
Change R289
from22K to 12K
ML2032 (Chargerable)
AHL03001034
CR2032 (Non-Chargeable)
AHL03003003
AHL03003014
AHL030M0009
Non-Green
Remove those parts.
Add "NGA@"
For STRAPS
for EMI suggestion
INTRUDER_ALERT# Left not connected
(Southbridge has 50-kohm internal
pull-up to VBAT).
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01
PROJECT : ZQ2
Quanta Computer Inc.
SB820-PCIE/PCI/CPU/LPC 1/4
Thursday, March 04, 2010
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NC only ,Can't be install

+3V_S5
R368 *2.2K_4 SB_TEST0
R217 *2.2K_4 SB_TEST1
R210 *2.2K_4 SB_TEST2

SCL0/SDATA0 is 3V tolerance. AMD datasheet define it
Clk Gen/ Robson/ TV tuner/ DDR2/ Thermal/ Accelerometer

+3V
R150 2.2K_4 PCLK_SMB
R147 2.2K_4 PDAT_SMB

SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

+3V_S5
R188 10K_4 SB_SMBCLK1
R215 10K_4 SB_SMBDATA1

SCL2/SDATA2 is 3V/S5 tolerance.
AMD datasheet define it

+3V_S5
R153 10K_4 SB_SCLK2
R149 10K_4 SB_SDATA2

+3V
R195 4.7K_4 SUS_STAT#

+3V
R316 8.2K_4 CLK_PCIE_LAN_REQ#
R178 8.2K_4 CLK_PCIE_2_REQ#

JTAG DEBUG

+3V_S5
CN13
C279 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

To Azalia

ACZ_SDOUT R200 33_4 ACZ_SDOUT_AUDIO [20]
C283 *10P/50V_4
ACZ_SYNC R202 33_4 ACZ_SYNC_AUDIO [20]
C284 *10P/50V_4
ACZ_BCLK R203 33_4 ACZ_BITCLK_AUDIO [20]
C285 *10P/50V_4
ACZ_RST# R201 33_4 ACZ_RST#_AUDIO [20]
ACZ_SDIN0 ACZ_SDIN0 [20]

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

U21D
SB800
Part 4 of 5

T71 SB_PCI_PME# J2
K1
D3
F1
[25] SUSB# SUSC# H1
[25] SUSC# F2
[25] DNBSWON# H5
[14] SB_PWRGD_IN G6
[8] SUS_STAT# B3
SB_TEST0 C4
SB_TEST1 F6
SB_TEST2 AD21
[25] SIO_A20GATE AE21
[25] SIO_RCIN# K2
SIO_RCIN# J29
LANLINK_STATE# H2
T114 J1
[25] SIO_EXT_SMI# H6
[25] SIO_EXT_SCI# F3
T116 J6
SYS_RST# AC19
[17,18] PCIE_WAKE# G1
IR_RX1 AD19
T117 AA16
SB_THERMTRIP# AB21
T69 AC18
[2,8,14] NB_PWRGD_IN AE20
AE19
[25] ICH_RSMRST# AF19
AD22
AE22
F5
F4
AH21
AB18
E1
AJ21
H8
D5
D7
G5
K3
AA20
H3
D1
E6
D4
E8
F7
F8
M3
N1
L2
M2
M1
M4
N2
P2
T1
T4
L6
L5
T9
U1
U3
T2
U2
T5
V5
P5
M5
P9
T7
P7
M7
H4
M9
V7
E23
E24
F21
G29
D27
F28
F29
E27

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC
USB_RCOMP
A10 USB_14_48M T110
G19 USB_RCOMP_SB R169 11.8K/F_6
USB_FSD1P/GPIO186 J10
USB_FSD1N H11
USB_FSD0P/GPIO185 H9 USB_FDS12P T63
USB_FSD0N J8 USB_FDS12N T58
USB_HSD13P B12
USB_HSD13N A12
USB_HSD12P F11
USB_HSD12N E11
USB_HSD11P E14
USB_HSD11N E12
USB_HSD10P J12
USB_HSD10N J14
USB_HSD9P A13
USB_HSD9N B13
USB_HSD8P D13
USB_HSD8N C13
USB_HSD7P G12
USB_HSD7N G14
USB_HSD6P G16
USB_HSD6N G18
USB_HSD5P D16
USB_HSD5N C16
USB_HSD4P B14
USB_HSD4N A14
USB_HSD3P E18
USB_HSD3N E16
USB_HSD2P J16
USB_HSD2N J18
USB_HSD1P B17 USBP1+ T54
USB_HSD1N A17 USBP1- T53
USB_HSD0P A16
USB_HSD0N B16
USBP13+ [15]
USBP13- [15]
USBP12+ [22]
USBP12- [22]
USBP11+ [22]
USBP11- [22]
USBP10+ [21]
USBP10- [21]
USBP9+ [22]
USBP9- [22]
USBP8+ [22]
USBP8- [22]
USBP4+ [18]
USBP4- [18]
USBP0+ [22]
USBP0- [22]

CAMERA
USBX3 board
USBX3 board
Card reader
BLUETOOTH
USBX3 board
WLAN Min-Card
EHCI3/ OHCI3
EHCI2/ OHCI2
EHCI1/ OHCI1

On Board USB Connector
Only USB Port0 can be configured as debug port.

T59 [22] OC_7# [22] OC_6# [22] OC_4#
Eliot (02/26)
Current Agesa bios doesn't program ALERT_L and SB won't process alert.
SB_PM_THERM#
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

HD audio interface is +3VS5 voltage

[14] ACZ_SDOUT
ACZ_BCLK
ACZ_SDOUT
ACZ_SDIN0
ACZ_SYNC
ACZ_RST#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

+3V_S5
R197 10K_4 GBE_COL
R191 10K_4 GBE_CRS
R182 10K_4 GBE_MDIO
R196 10K_4 GBE_RXERR
R190 10K_4 GBE_PHY_INTR
T49 ADP_PRES0
GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPIO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

[02/22] AMD FAE and checklist request PL.

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
D25 SB_SCLK2
F23 SB_SDATA2
B26 SB_GPIO195
E26 SB_GPIO196
F25 T48
F22
E21
GPIO199 [14]
GPIO200 [14]

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226

Check list
SB_GPIO195 R146 10K_4
SB_GPIO196 R144 10K_4

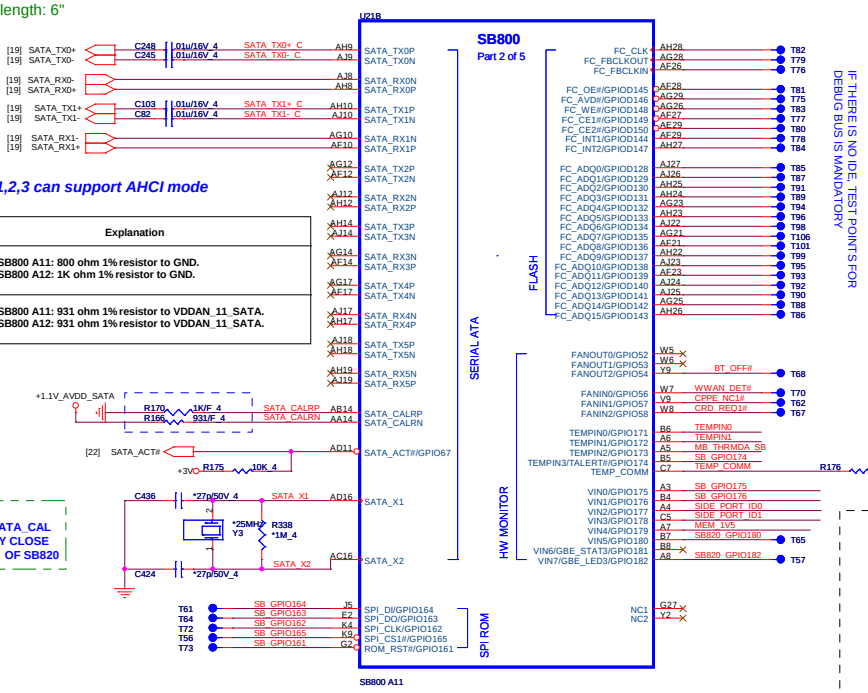
SB800 A11

PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
SB820-ACPI/GPIO/USB 2/4
Rev 1A
Date: Thursday, March 04, 2010 Sheet 11 of 36

Max trace length: 6"

SATA HDD

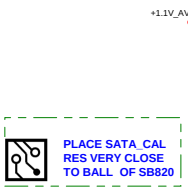
SATA ODD



SATA PORT 0,1,2,3 can support AHCI mode

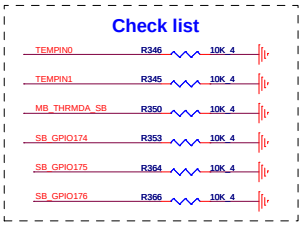
Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11_SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11_SATA.

E-SATA

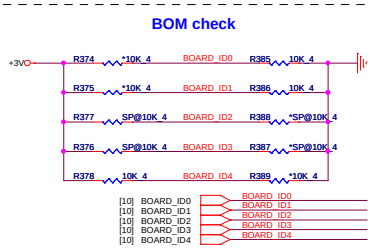


IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

Check list



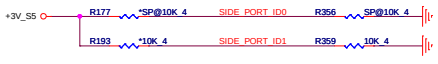
BOM check



	1	0
ID0	15"	14"
ID1	DIS	UMA
ID2	W/I	W/O
ID3	JM	JV
ID4	6L	8L

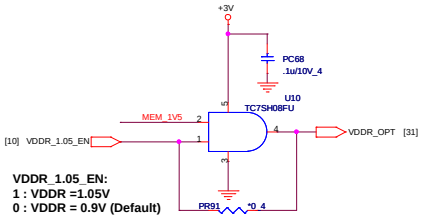
Sideport

DDR3 Sideport Memory Device



	1	0
ID0	SAM	HYU
ID1	RSV	RSV

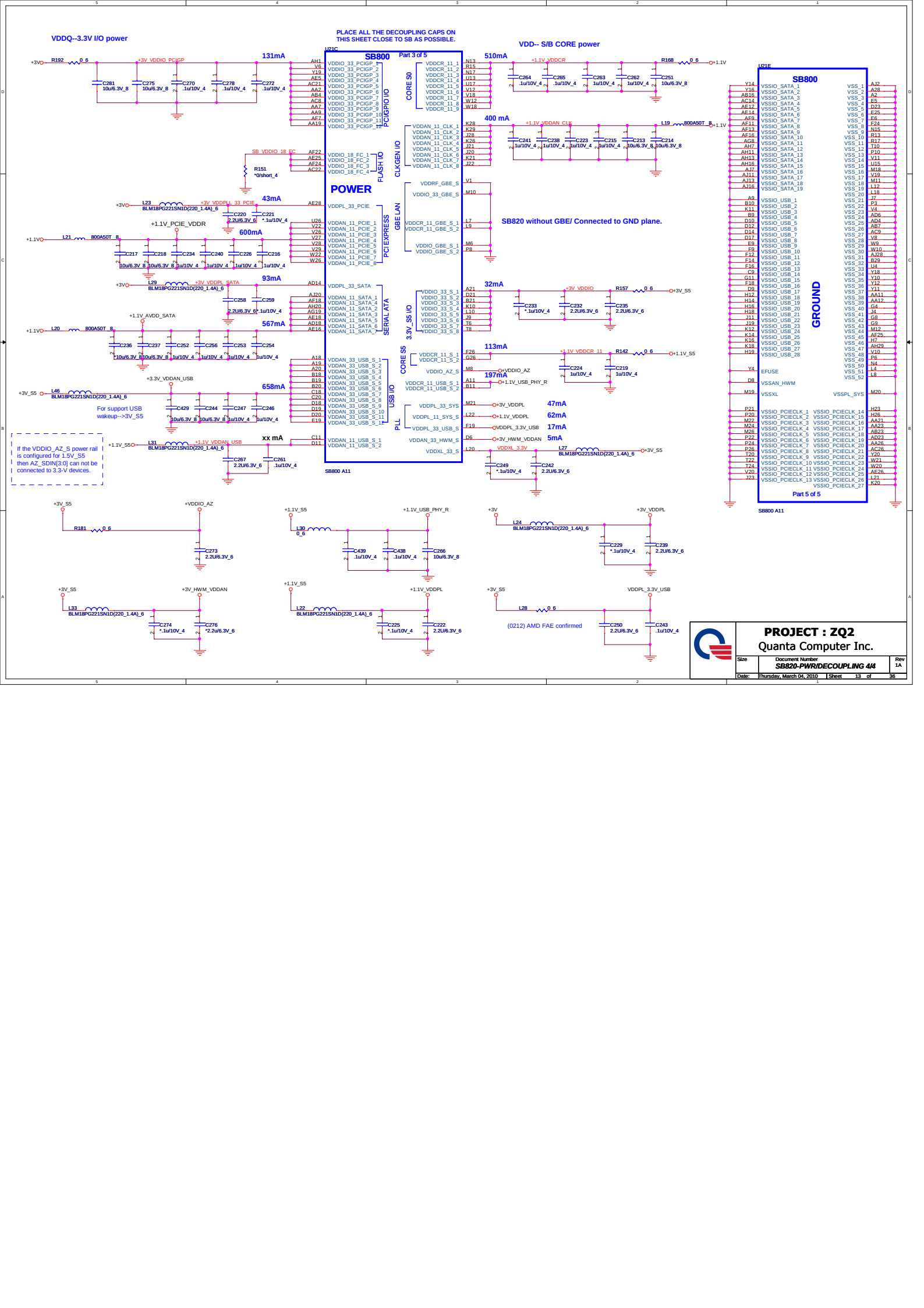
Vendor	Vendor P/N	STN B/S P/N	Size	BOARD_ID2 GPIO12	SIDE_PORT_ID1 GPIO178	SIDE_PORT_ID0 GPIO177
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	1 (W/Sideport)	0	1



VDDR_1.05_EN:
1 : VDDR =1.05V
0 : VDDR = 0.9V (Default)

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-SATA/IDE/SPI 3/4	1A
Date: Thursday, March 04, 2010	Sheet 12 of 36	

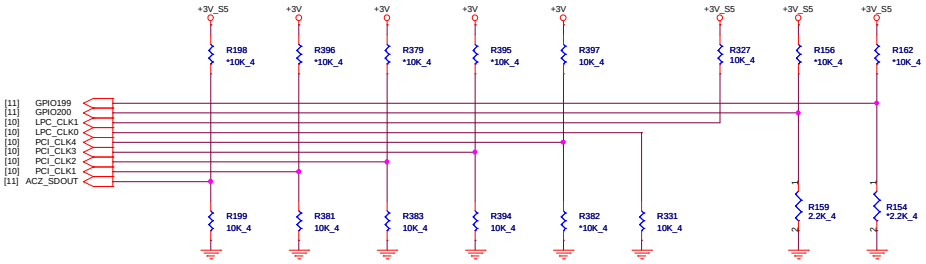

VDDQ--3.3V I/O power
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
VDD-- S/B CORE power
SB800
Part 3 of 5
POWER
SB820 without GBE/ Connected to GND plane.
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.
For support USB wakeup-->3V_S5
(0212) AMD FAE confirmed
SB800 A11
GROUND
Part 5 of 5
PROJECT : ZQ2
Quanta Computer Inc.
SB820-PWR/DECOUPLING 4/4
Rev 1A
Thursday, March 04, 2010
Sheet 13 of 36

REQUIRED STRAPS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

SB820M is supported Gen.1 mode only.

For internal clock GEN.

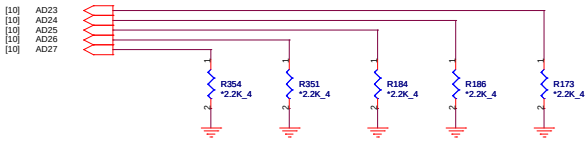


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K

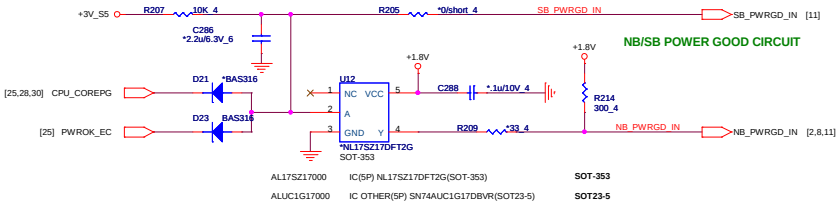
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-STRAPS	1A

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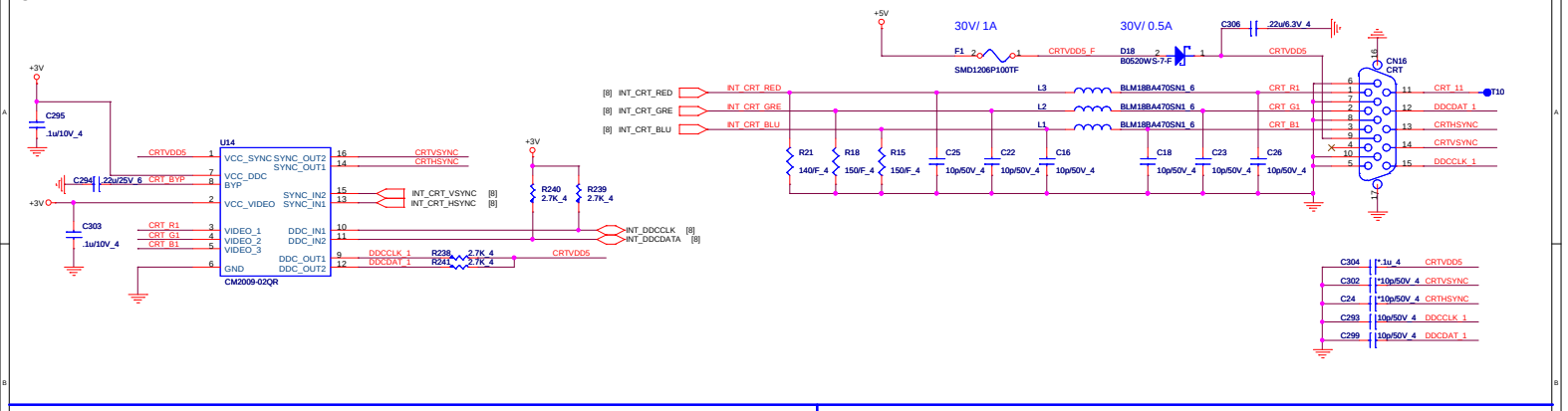
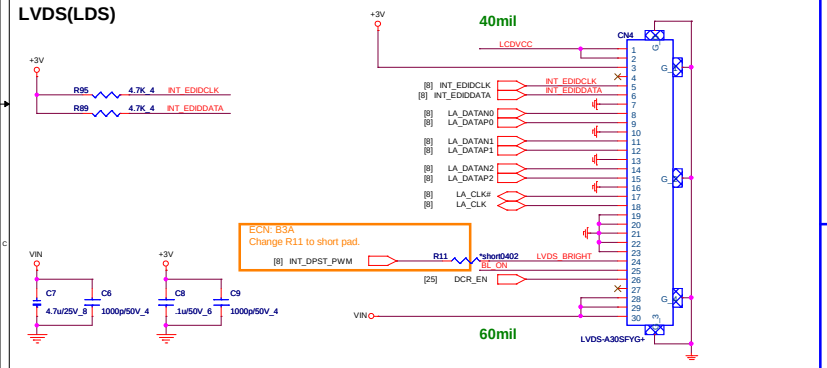
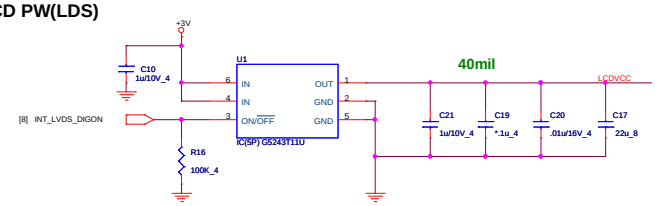
CRT



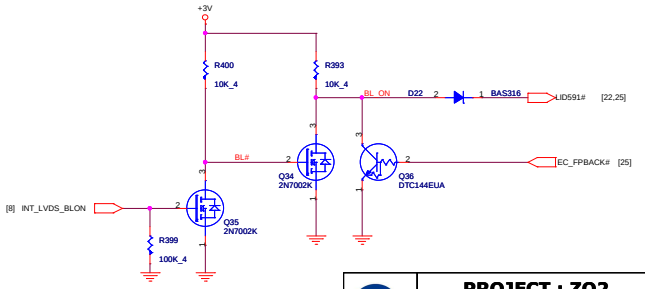
LVDS(LDS)



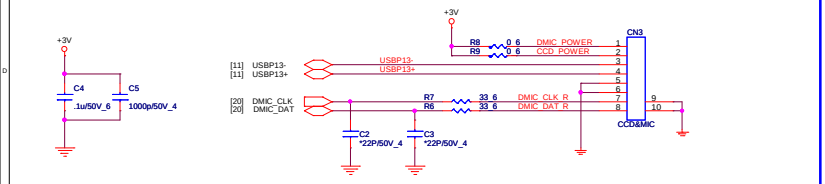
LCD PW(LDS)



Backlight Control(LDS)



CAMERA Module(CCD)



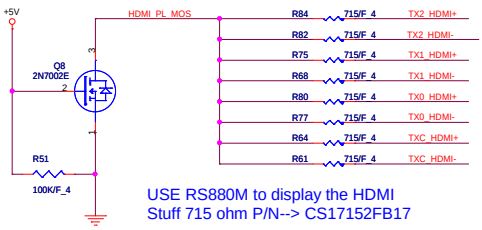
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS/LID	3A

Date: Thursday, March 04, 2010 Sheet 15 of 36

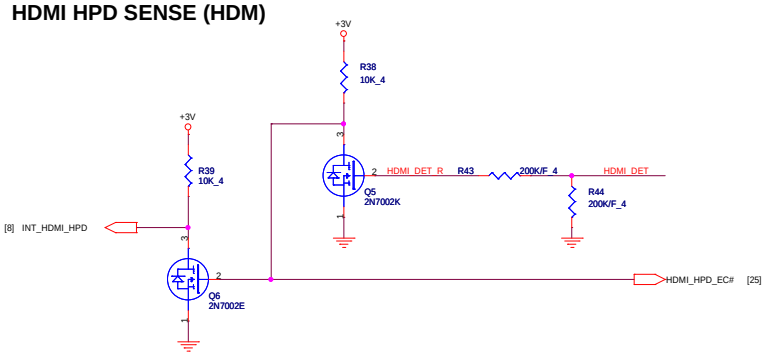
HDMI (HDM)

Close to HDMI Connector

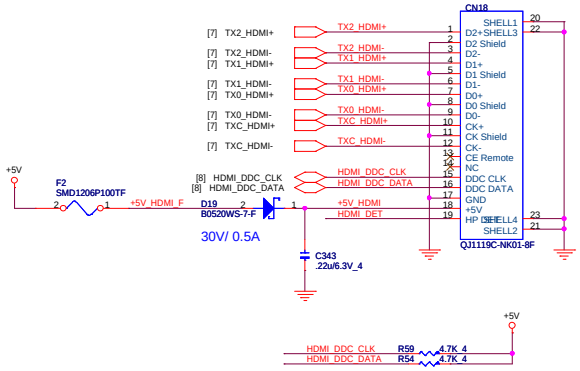


USE RS880M to display the HDMI
Stuff 715 ohm P/N--> CS17152FB17

HDMI HPD SENSE (HDM)

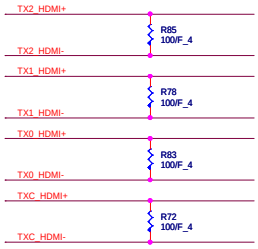


HDMI PORT (HDM)



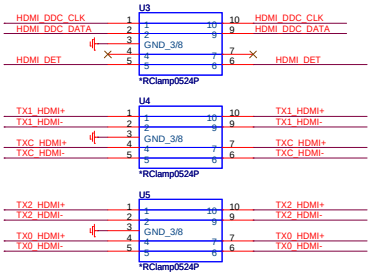
EMI reserve for HDMI(EMC)

Close connector



ESD Protect (EMC)

close to HDMI connector



Size	Document Number		Rev
	HDMI		1A
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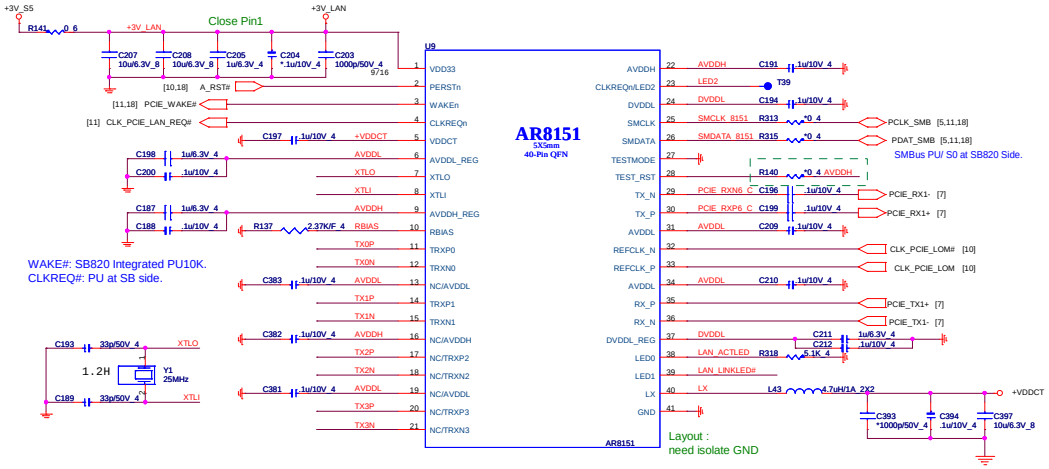
PROJECT : ZQ2
Quanta Computer Inc.

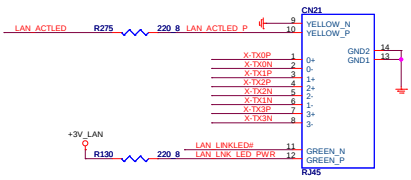
Giga-LAN AR8151

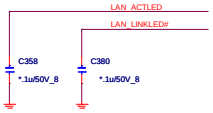


WAKE#: SB820 Integrated PU10K.
CLKREQ#: PU at SB side.

Layout :
need isolate GND

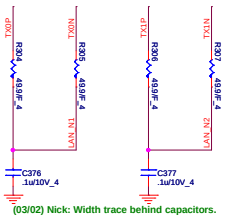
RJ45(LAN)



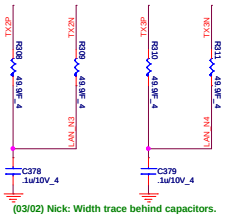


Sertek (03/01):
EMI capacitors, 470pF is enough.
Don't over 490 pF.

TRANSFORMER(LAN)

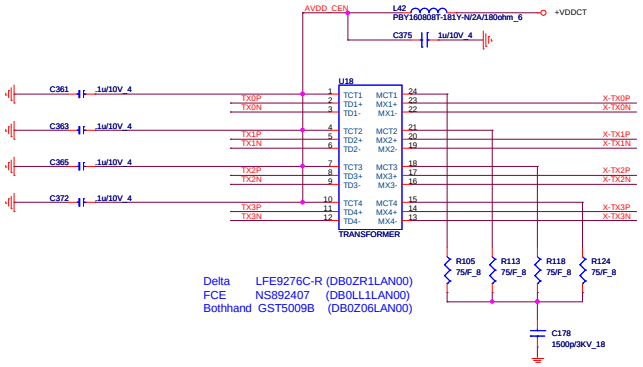


(03/02) Nick: Width trace behind capacitors.



(03/02) Nick: Width trace behind capacitors.

Close Transformer U28



Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)
Bothhand GST5009B (DB0Z06LAN00)

PROJECT : ZQ2
Quanta Computer Inc.

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	LAN (AR8151)	1A
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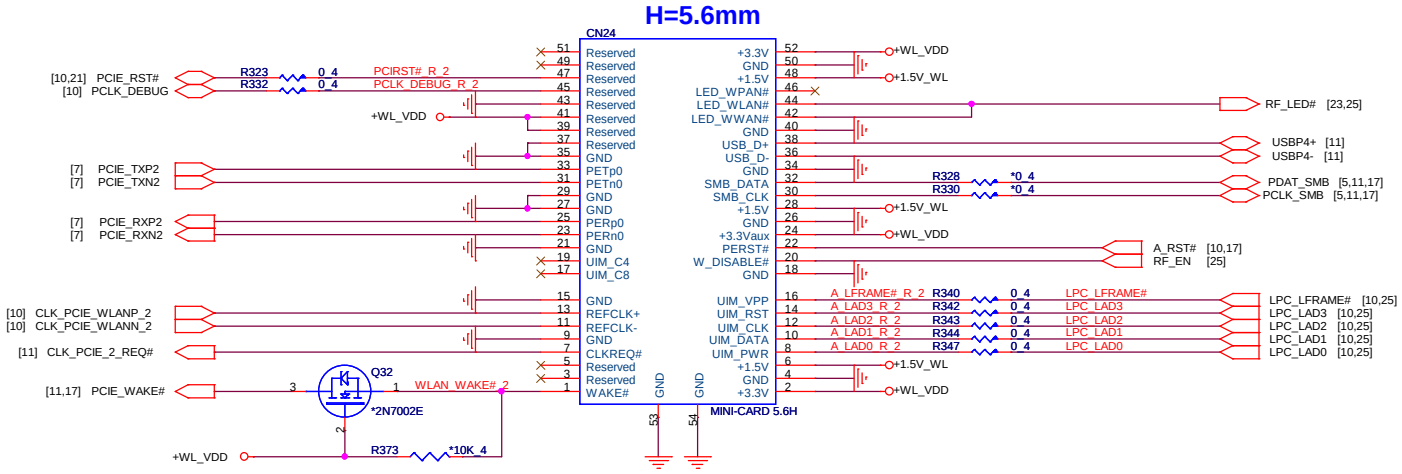
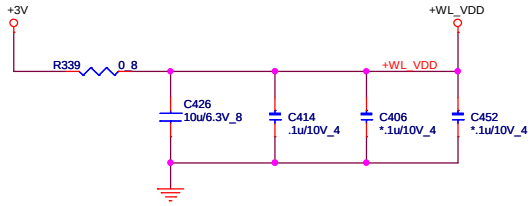
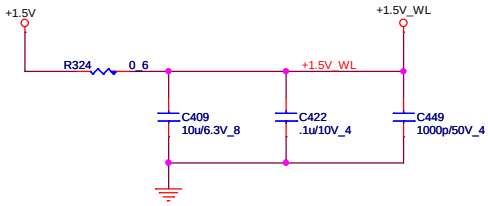
MINI-CARD WLAN(MNC)







PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	Mini-Card/WL	1A
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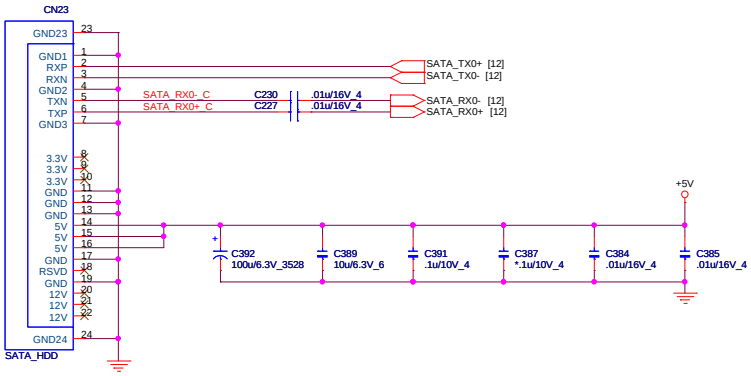
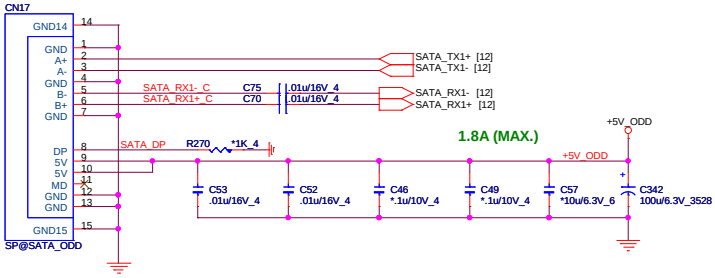
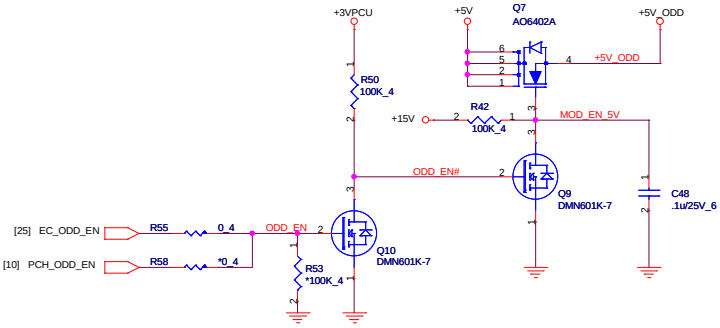
SATA HDD(HDD)



SATA ODD (ODD)



ODD POWER(ODD)



JM-9.5mm (H=2.4mm)/ Slim

Main	DFHS13FR078, DFHS13FR077
Second	DFHS13FR075

JV-12.7mm(H=5.5mm)/ Standard

Main	DFHS13FR017
Second	DFHS13FR006, DFHS13FR005

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A

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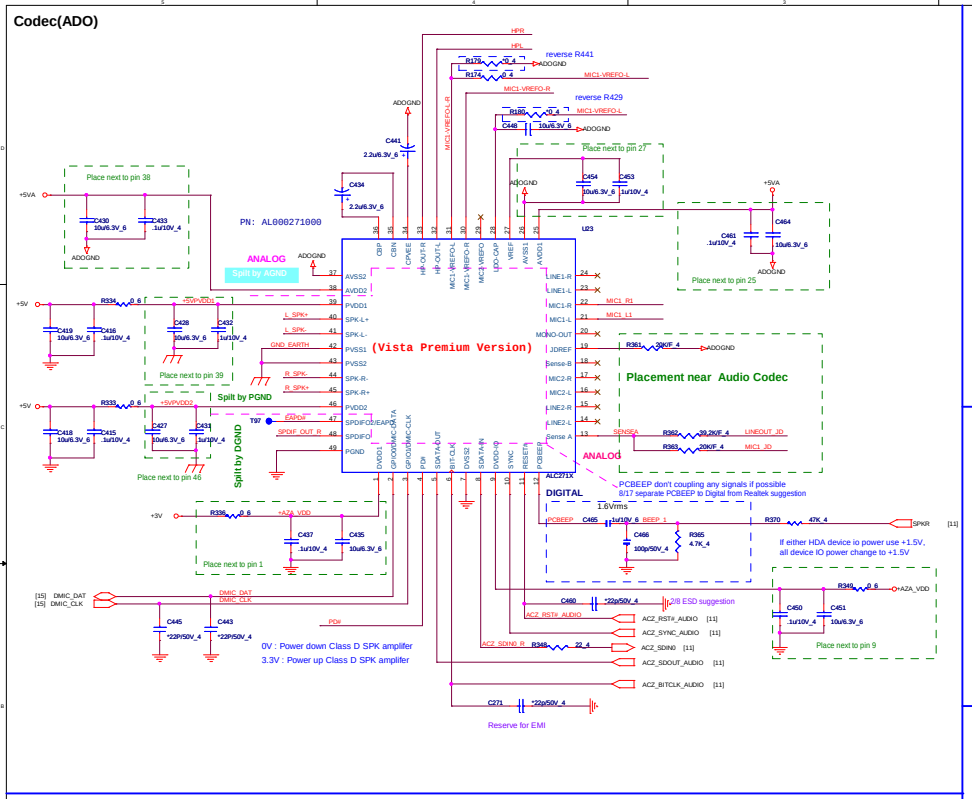
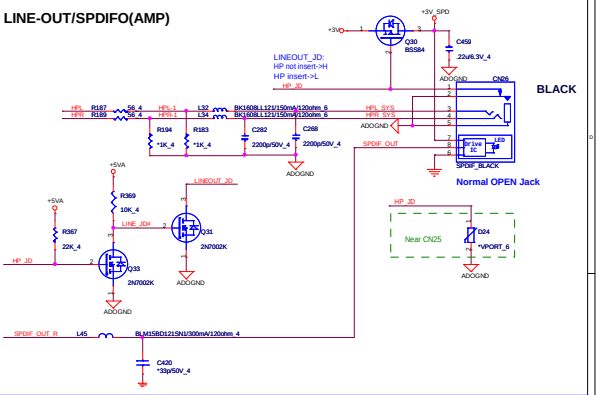
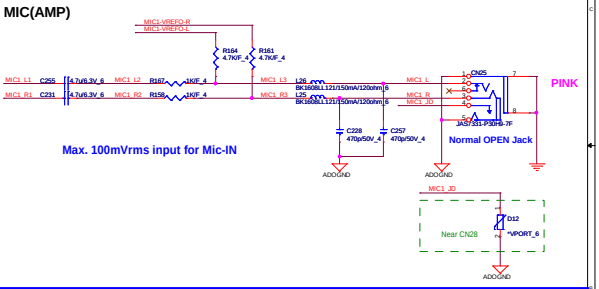
Codec(ADO)



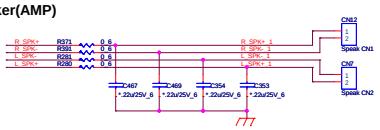
LINE-OUT/SPDIFO(AMP)



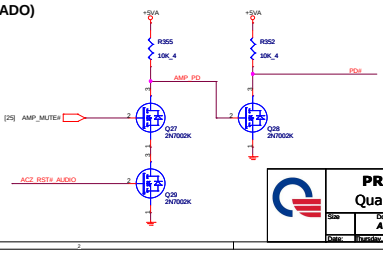
MIC(AMP)



Internal Speaker(AMP)



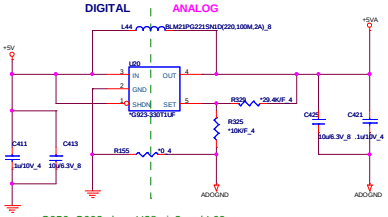
Mute(ADO)



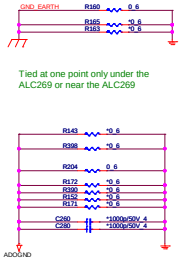
Power (ADO)

Demodulation Filter

BEAD place close to CODEC.



GND_EARTH don't coupling AGND and SPK signals



PROJECT : ZQ2	
Quanta Computer Inc.	
Size	Document Number: ALC271X / AMP / SPK — Rev: 1A
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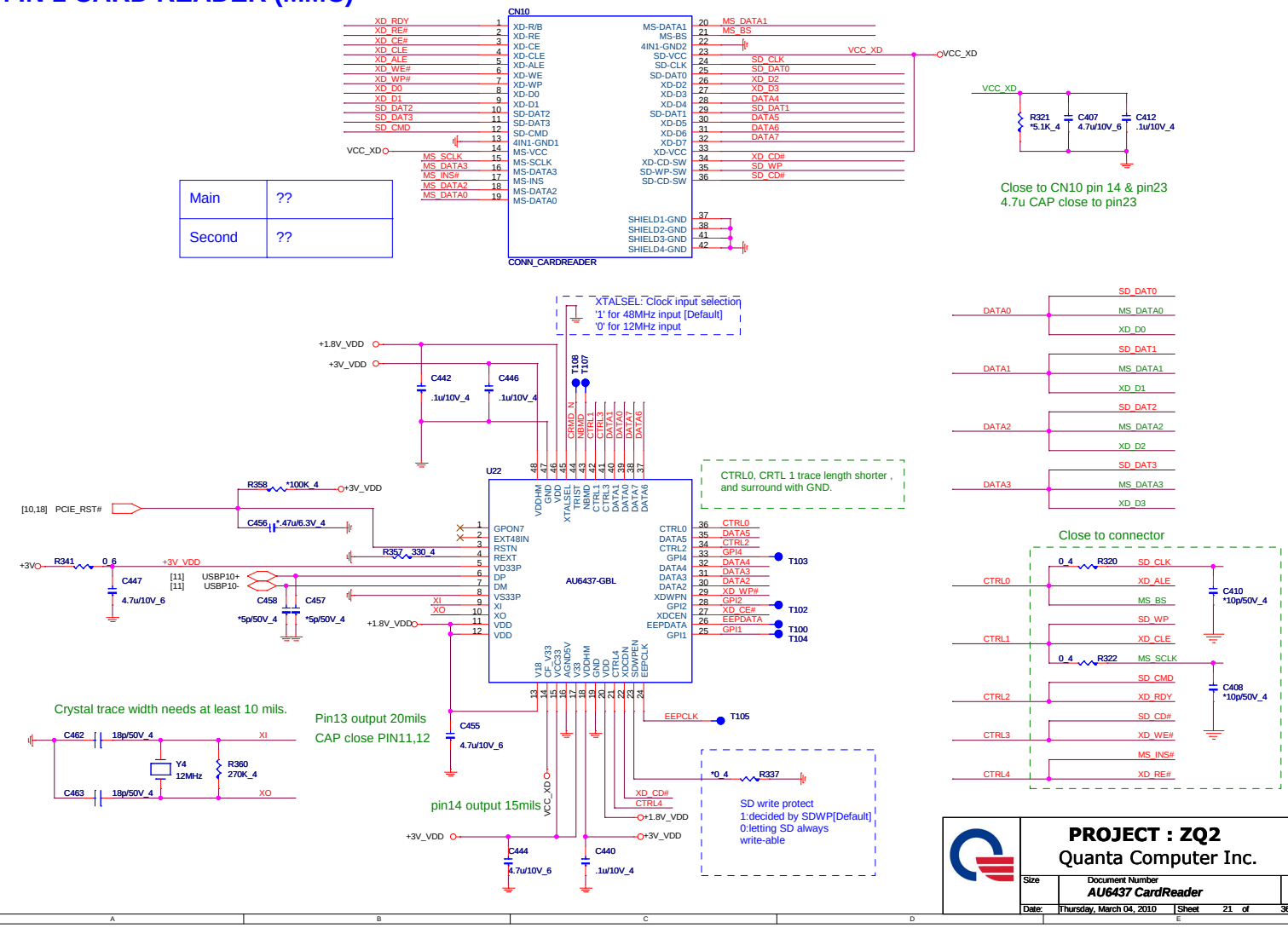
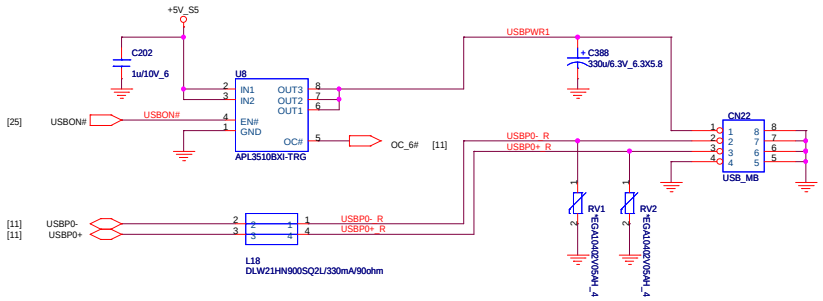
4 IN 1 CARD READER (MMC)

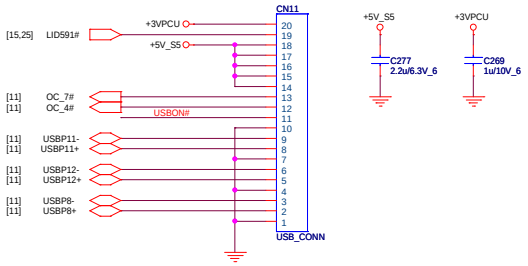


PROJECT : ZQ2	Quanta Computer Inc.
Size	Document Number: AU6437 CardReader
Rev: 1A	
Date: Thursday, March 04, 2010	Sheet 21 of 36

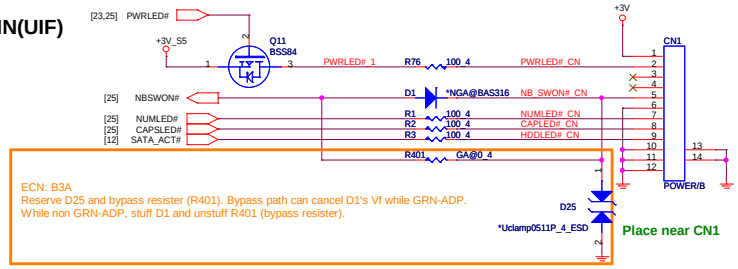
USB PORT(USB/MB)



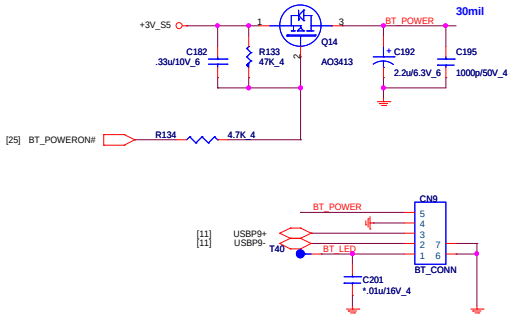
USB BOARD CONN(USB/SB)



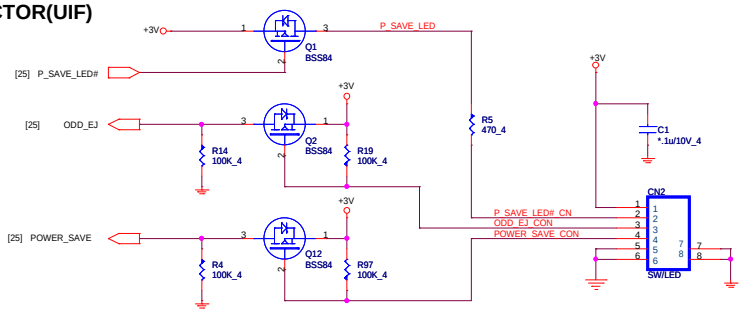
POWER BOARD CONN(UIF)



BLUETOOTH CONN(BTM)



LED BOARD CONNECTOR(UIF)



PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	USB/BT/TP	3A
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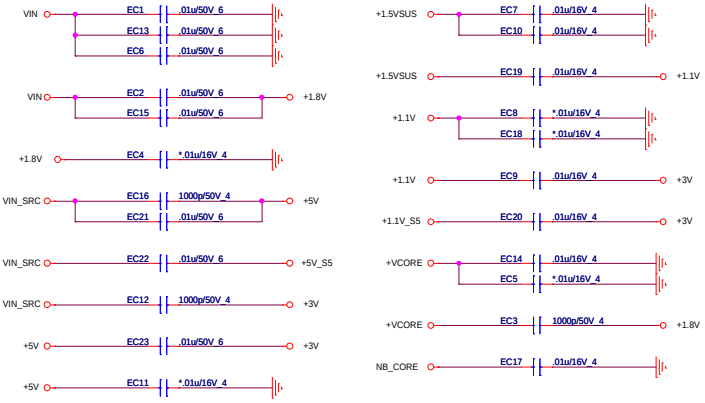
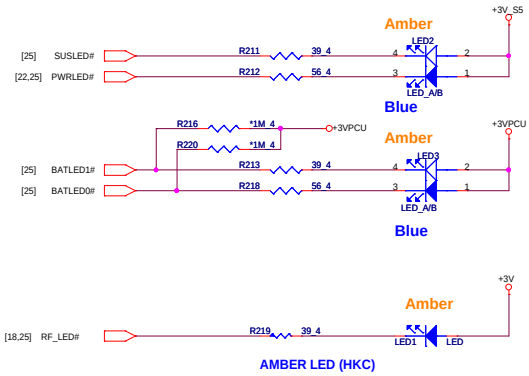
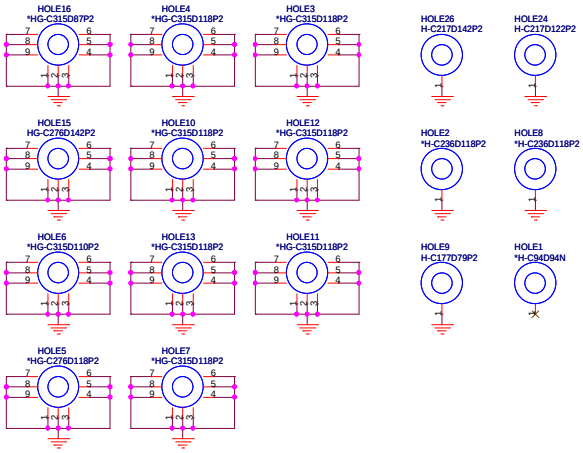
EE RETURN-PATH CAPACITORS(EMC)

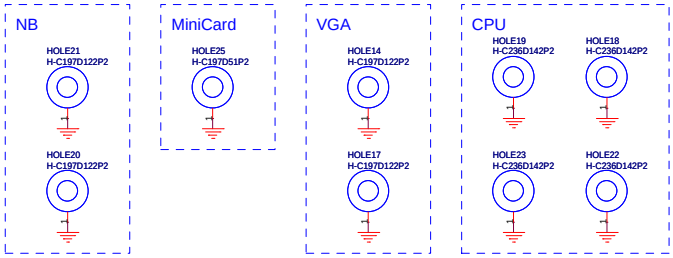


LED(UIF)



HOLE(OTH)





PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	POWER/USB/BT/TP/MDC	1A
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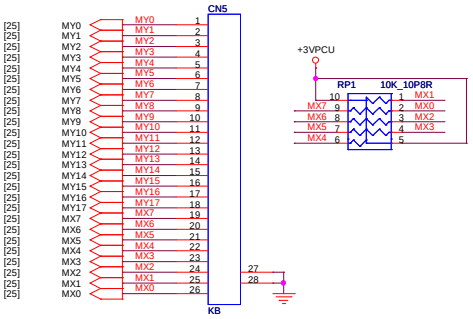
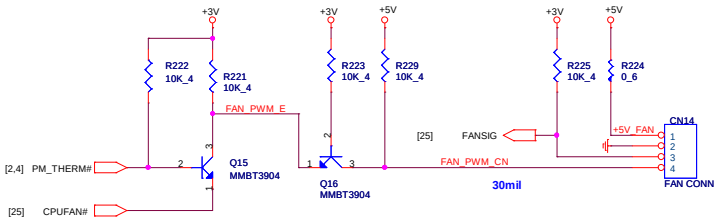
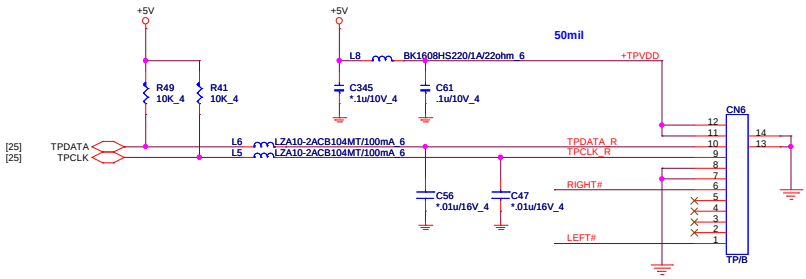
K/B(KBC)

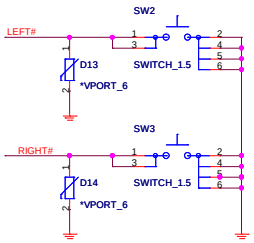


CPU FAN(THM)



TOUCHPAD BOARD CONN(TPD)





PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	KB/FAN/EE RETURN CAP	1A
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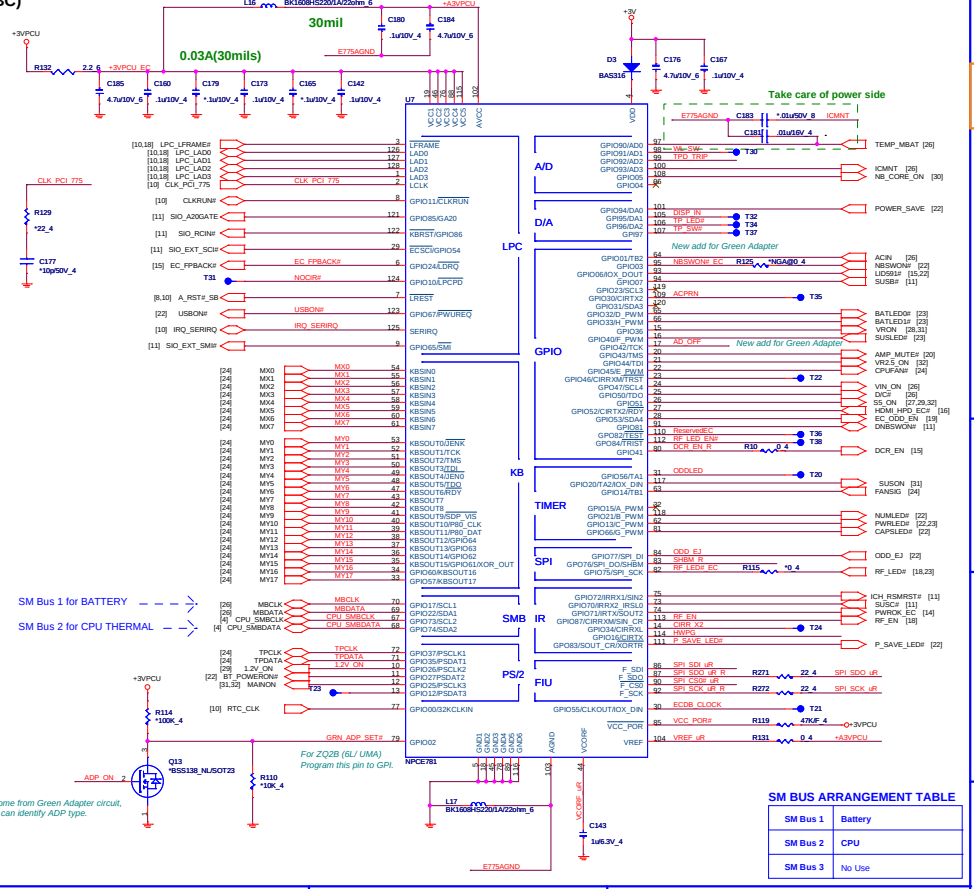
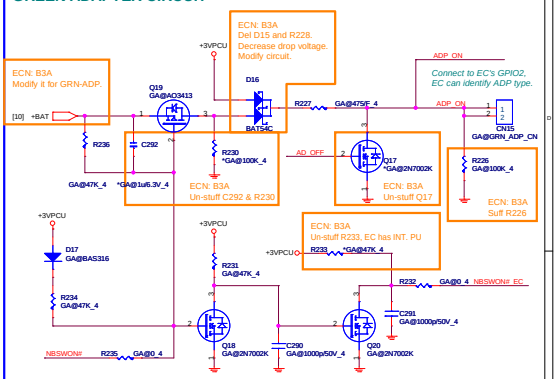
EC(KBC)



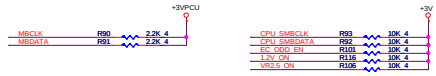
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU
SM Bus 3	No Use

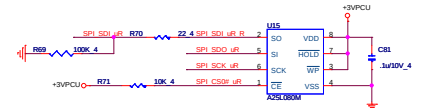
GREEN ADAPTER CIRCUIT



SM BUS PU(KBC)



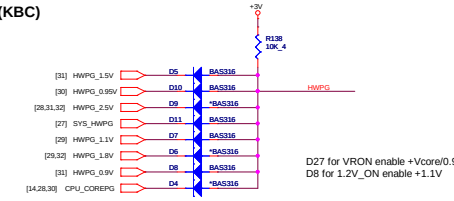
SPI FLASH(KBC)



If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

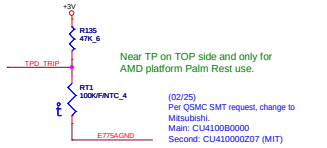
Winbond W25X16AVSSIG AKE382P0N01
MXIC MX25L1605AM2C-15G AKE37FP0Z13
EON EN25F16-100HIP AKE38ZA0Q00
AMIC A25L016 AKE38ZN0800

HWPG(KBC)

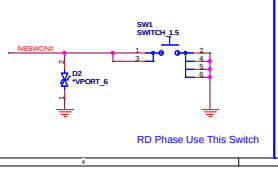


D27 for VRON enable +Vcore/0.9V
D8 for 1.2V_ON enable +1.1V

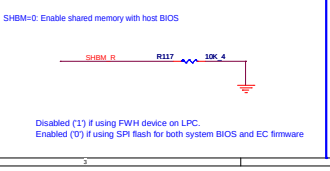
PALM REST THERMAL SENSOR (THM)



POWER-ON SWITCH (KBC)



POWER-ON SWITCH (KBC)



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Quanta Computer Inc.

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	3A

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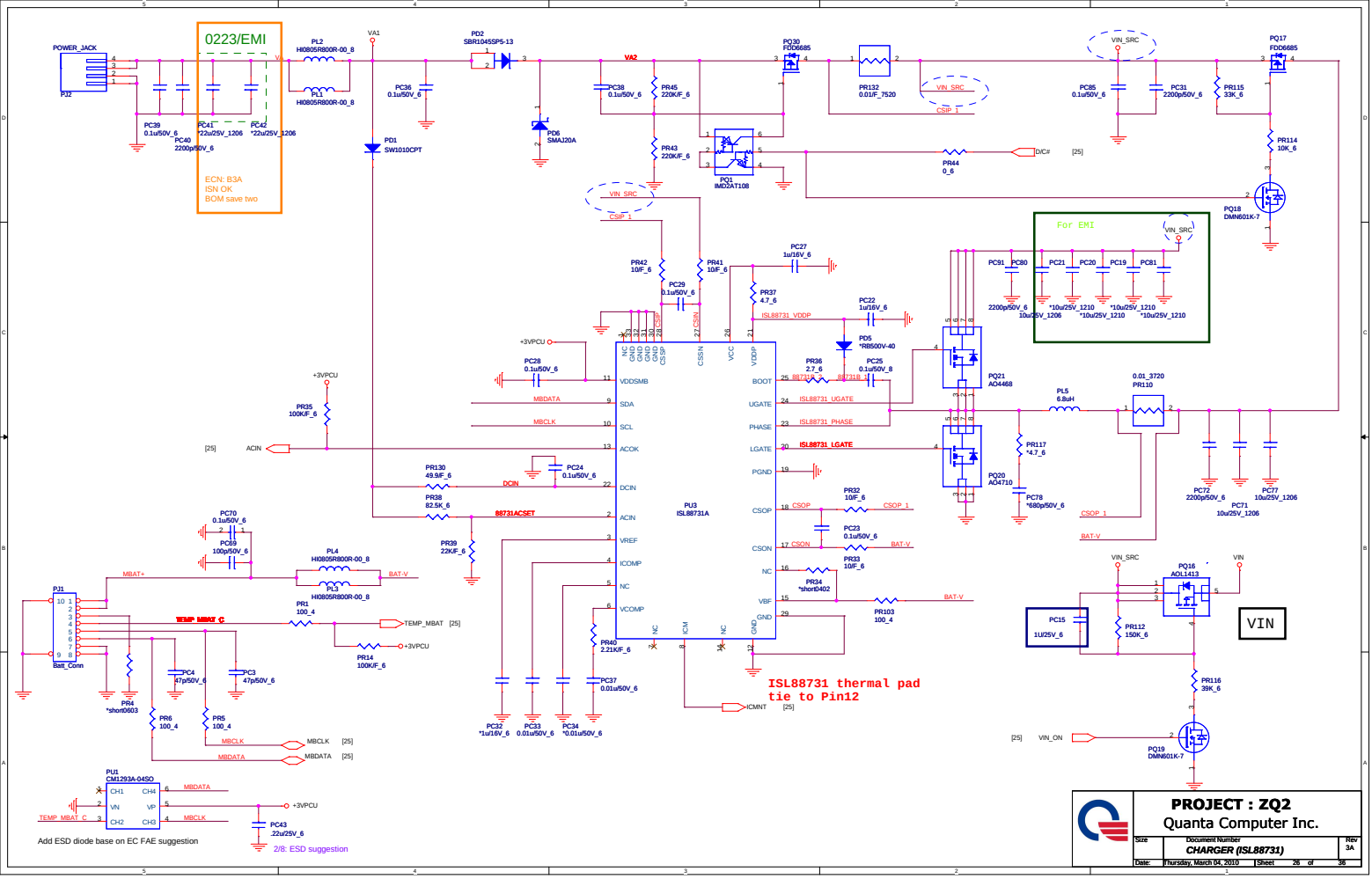
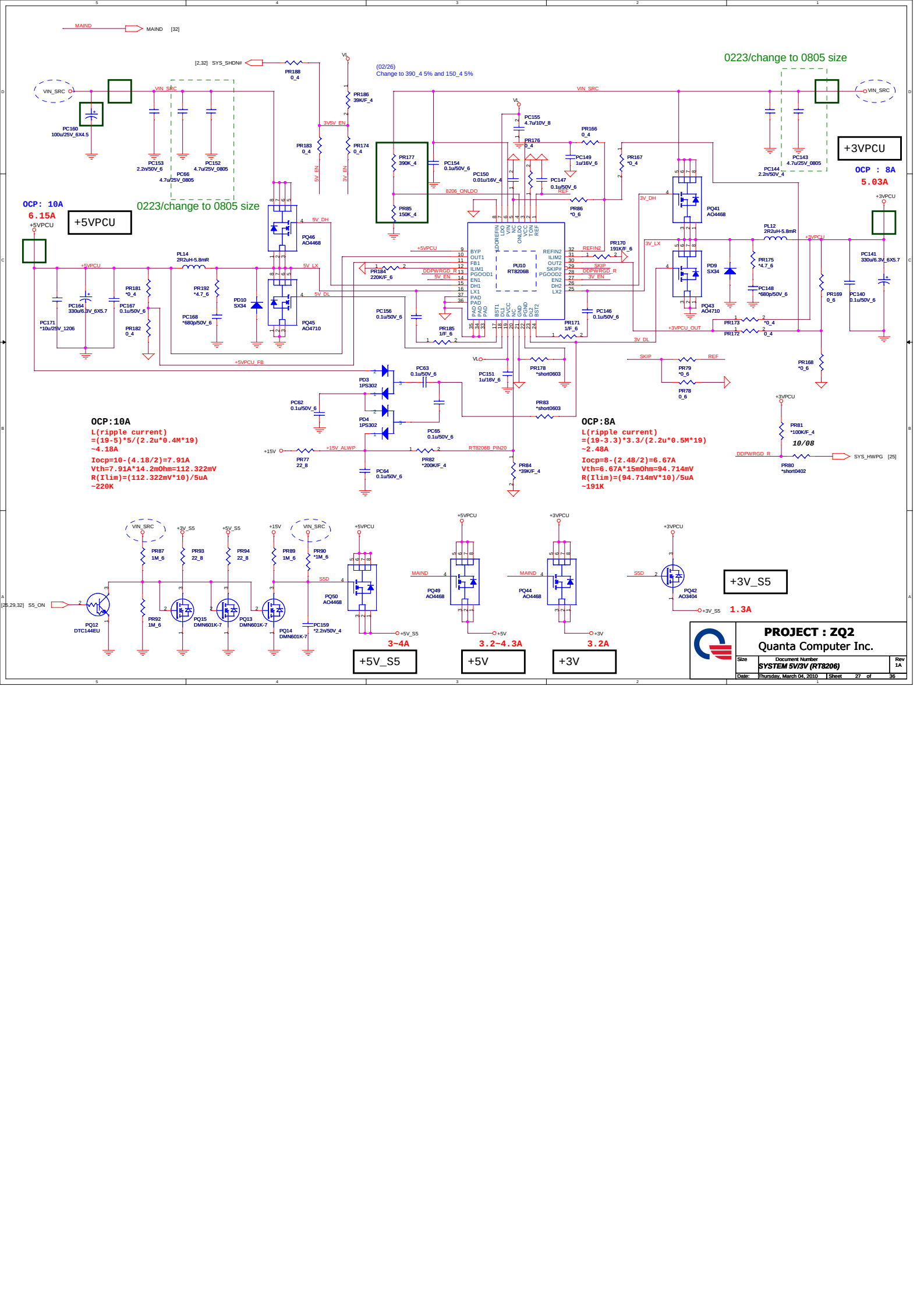

0223/EMI
ECN: B3A
ISN OK
BOM save two
For EMI
ISL88731 thermal pad
tie to Pin12
Add ESD diode base on EC FAE suggestion
2/8: ESD suggestion
PROJECT : ZQ2
Quanta Computer Inc.
CHARGER (ISL88731)
Thursday, March 04, 2010
26
36
3A


MAIND
MAIND [32]
[2,32] SYS_SHDN#
VIN_SRC
PR188 0_4
PR186 39K/F_4
3V5V_EN
PR183 0_4
PR174 0_4
5V_EN
3V_EN
PC160 100u/25V_6X4.5
PC153 2.2n/50V_6
PC66 4.7u/25V_0805
PC152 4.7u/25V_0805
0223/change to 0805 size
(02/26)
Change to 390_4 5% and 150_4 5%
0223/change to 0805 size
+3VPCU
OCP : 8A
5.03A
OCP: 10A
6.15A
+5VPCU
+5VPCU
0223/change to 0805 size
PR177 390K_4
PR85 150K_4
PC154 0.1u/50V_6
PC150 0.01u/16V_4
8206_ONLDO
PC155 4.7u/10V_8
PR176 0_4
PR166 0_4
PC149 1u/16V_6
PC147 0.1u/50V_6
REF
PR86 *0_6
PR167 *0_4
PC144 2.2n/50V_4
PC143 4.7u/25V_0805
PQ41 AO4468
3V_DH
3V_LX
PL12 2R2uH-5.8mR
PR175 *4.7_6
PC148 *680p/50V_6
PD9 SX34
PQ43 AO4710
PC141 330u/6.3V_6X5.7
PR169 0_6
PC140 0.1u/50V_6
PR173 *0_4
PR172 0_4
+3VPCU_OUT
3V_DL
PR168 *0_6
PU10 RT8206B
PR184 220K/F_6
DDPWRGD_R
5V_EN
PR170 191K/F_6
REFIN2
SKIP
PR171 1/F_6
PC146 0.1u/50V_6
PR185 1/F_6
PC156 0.1u/50V_6
PR178 *short0603
PC151 1u/16V_6
PR83 *short0603
PR79 *0_6
PR78 0_6
SKIP
REF
PR81 *100K/F_4
10/08
PR80 *short0402
DDPWRGD_R
SYS_HWPG [25]
PC164 330u/6.3V_6X5.7
PC167 0.1u/50V_6
PC171 *10u/25V_1206
PR181 *0_4
PR182 0_4
PL14 2R2uH-5.8mR
PR192 *4.7_6
PC168 *680p/50V_6
PD10 SX34
PQ46 AO4468
PQ45 AO4710
5V_DH
5V_LX
5V_DL
+5VPCU_FB
PD3 1PS302
PD4 1PS302
PC63 0.1u/50V_6
PC62 0.1u/50V_6
PC65 0.1u/50V_6
PC64 0.1u/50V_6
PR77 22_8
PR82 *200K/F_4
PR84 *39K/F_4
+15V
+15V_ALWP
RT8206B_PIN20
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
PR87 1M_6
PR93 22_8
PR94 22_8
PR89 1M_6
PR90 *1M_6
S5D
PQ50 AO4468
PC159 *2.2n/50V_4
PR92 1M_6
PQ15 DMN601K-7
PQ13 DMN601K-7
PQ14 DMN601K-7
PQ12 DTC144EU
[25,29,32] S5_ON
+3V_S5
PQ42 AO3404
1.3A
PQ49 AO4468
PQ44 AO4468
MAIND
3~4A
3.2~4.3A
3.2A
+5V_S5
+5V
+3V
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
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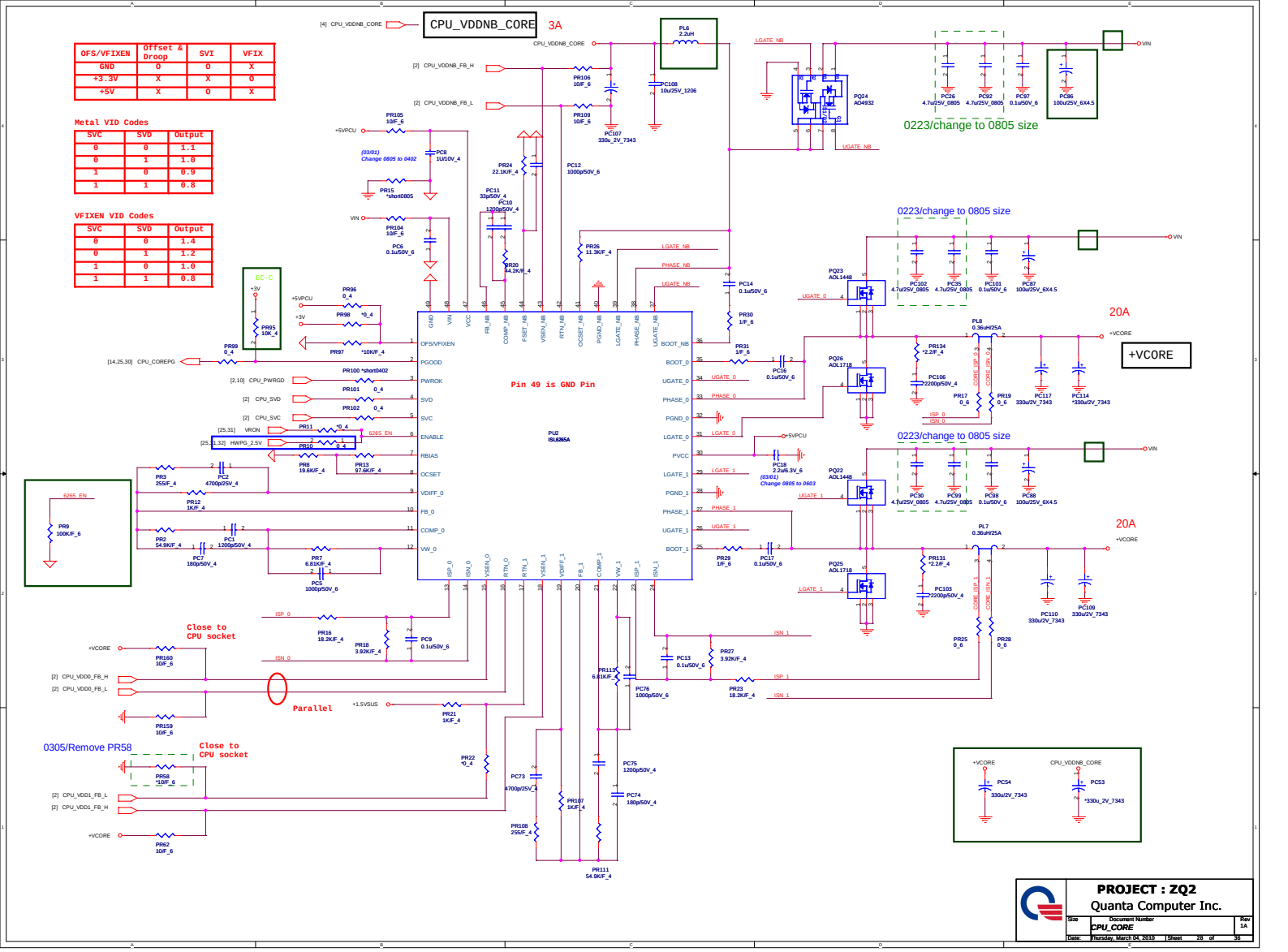
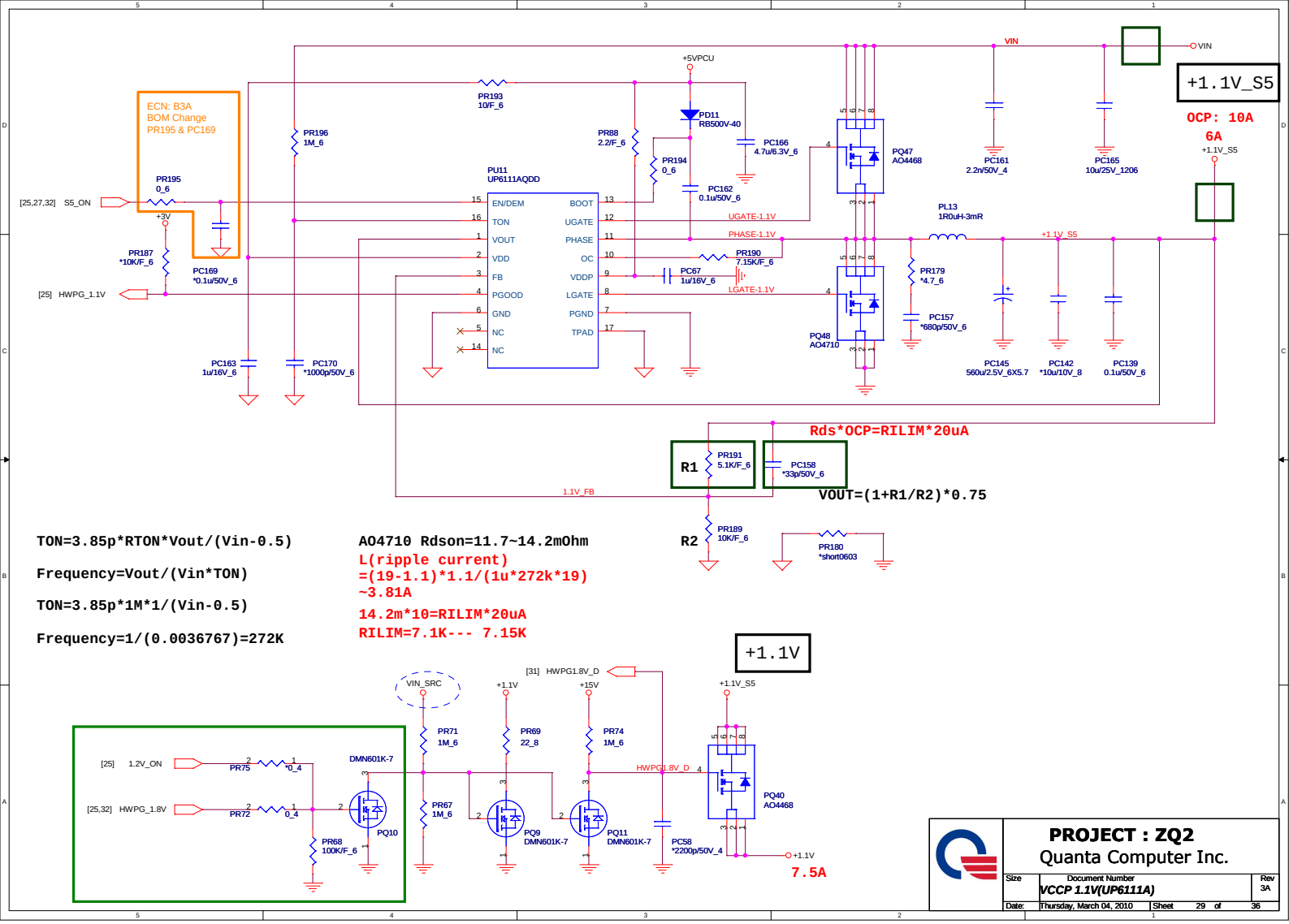

CPU_VDDNB_CORE
3A
OFS/VFIXEN
Offset & Droop
SVI
VFIX
GND
0
0
X
+3.3V
X
X
0
+5V
X
0
X
Metal VID Codes
SVC
SVD
Output
0
0
1.1
0
1
1.0
1
0
0.9
1
1
0.8
VFIXEN VID Codes
SVC
SVD
Output
0
0
1.4
0
1
1.2
1
0
1.0
1
1
0.8
Pin 49 is GND Pin
0223/change to 0805 size
20A
+VCORE
Close to CPU socket
Parallel
0305/Remove PR58
PROJECT : ZQ2
Quanta Computer Inc.
CPU_CORE
Thursday, March 04, 2010



PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number: VCCP 1.1V(UP6111A)	Rev: 3A
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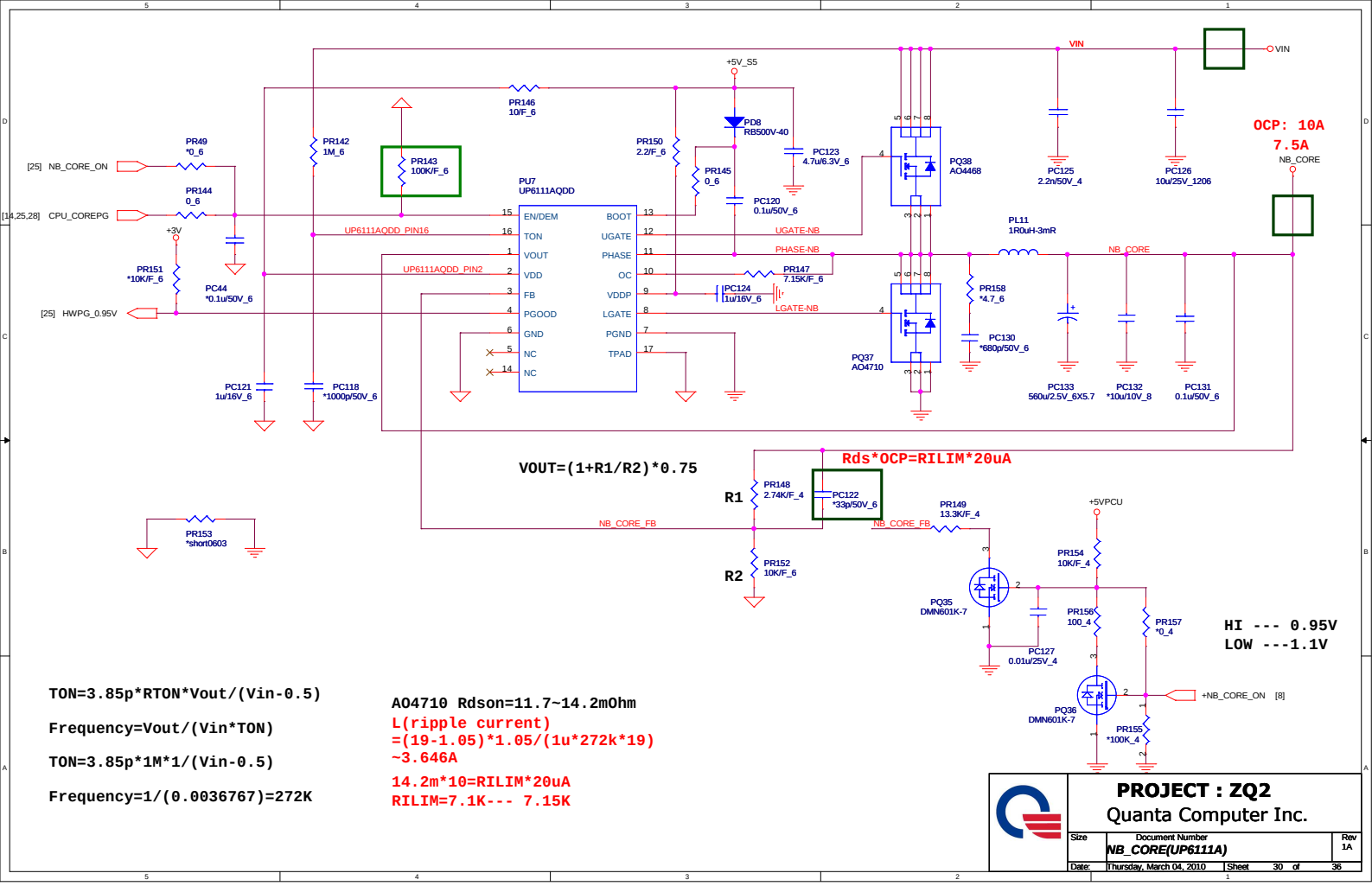

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

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Quanta Computer Inc.

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	NB_CORE(UP6111A)	1A
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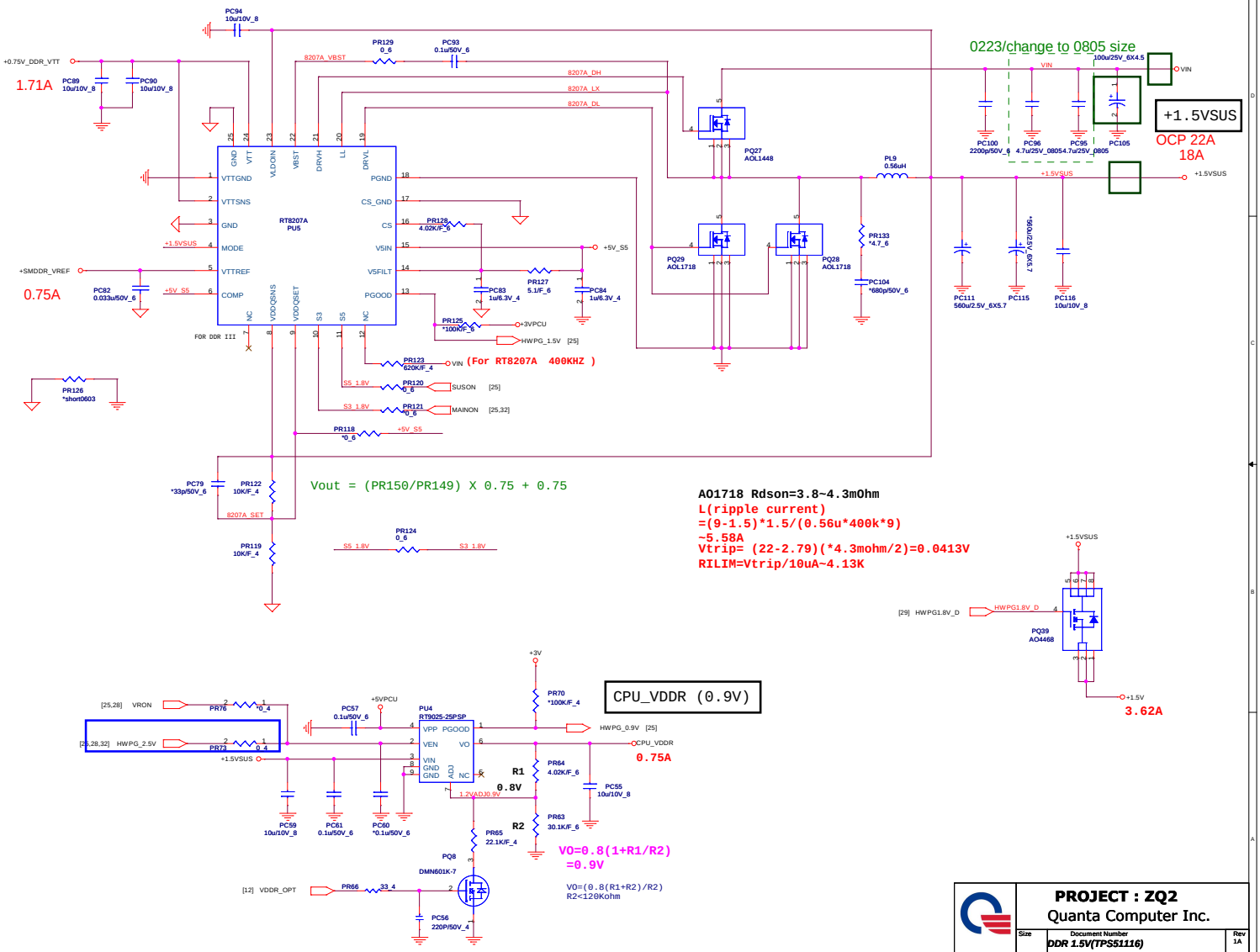
[PWM]



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

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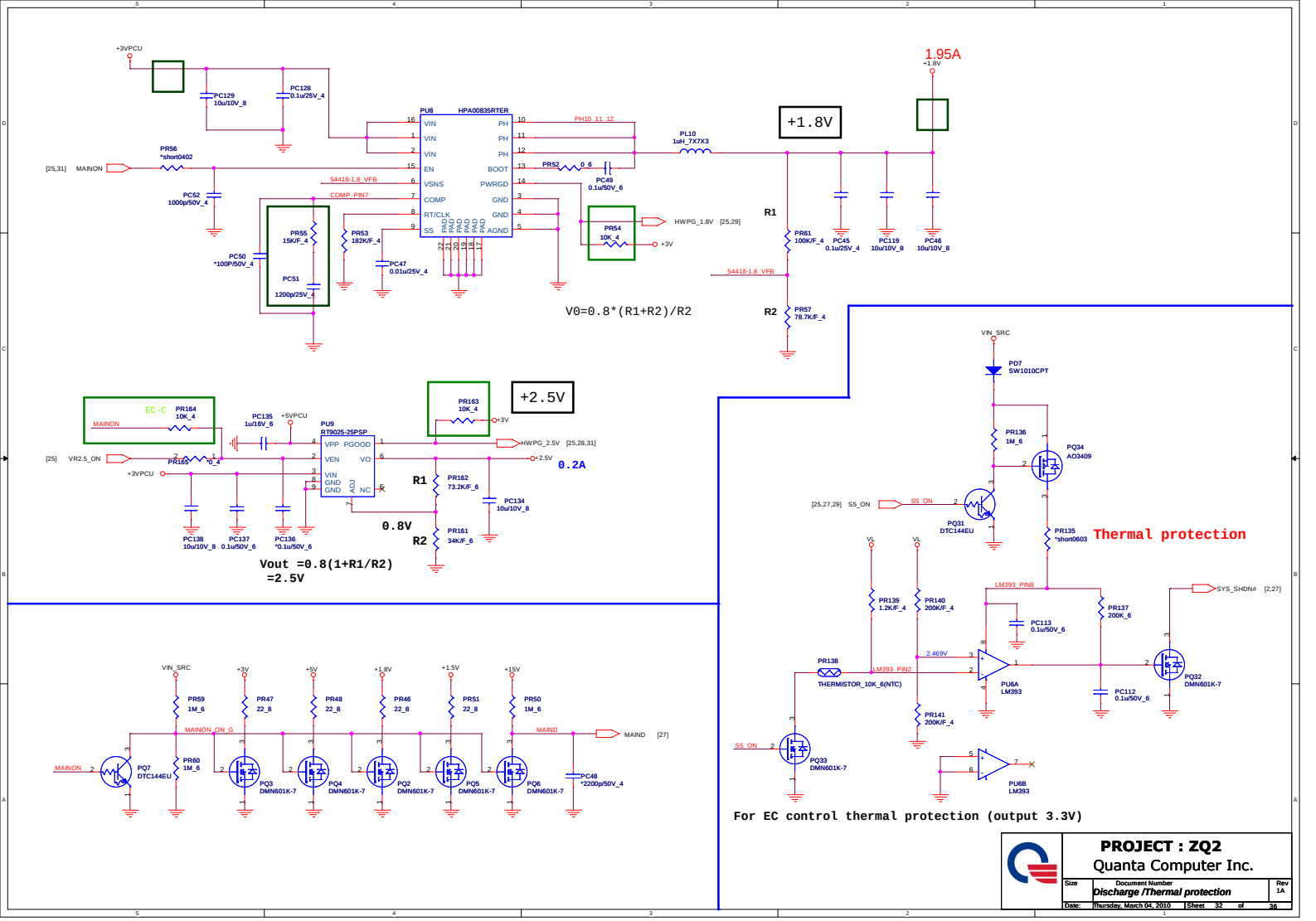

PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge /Thermal protection	1A
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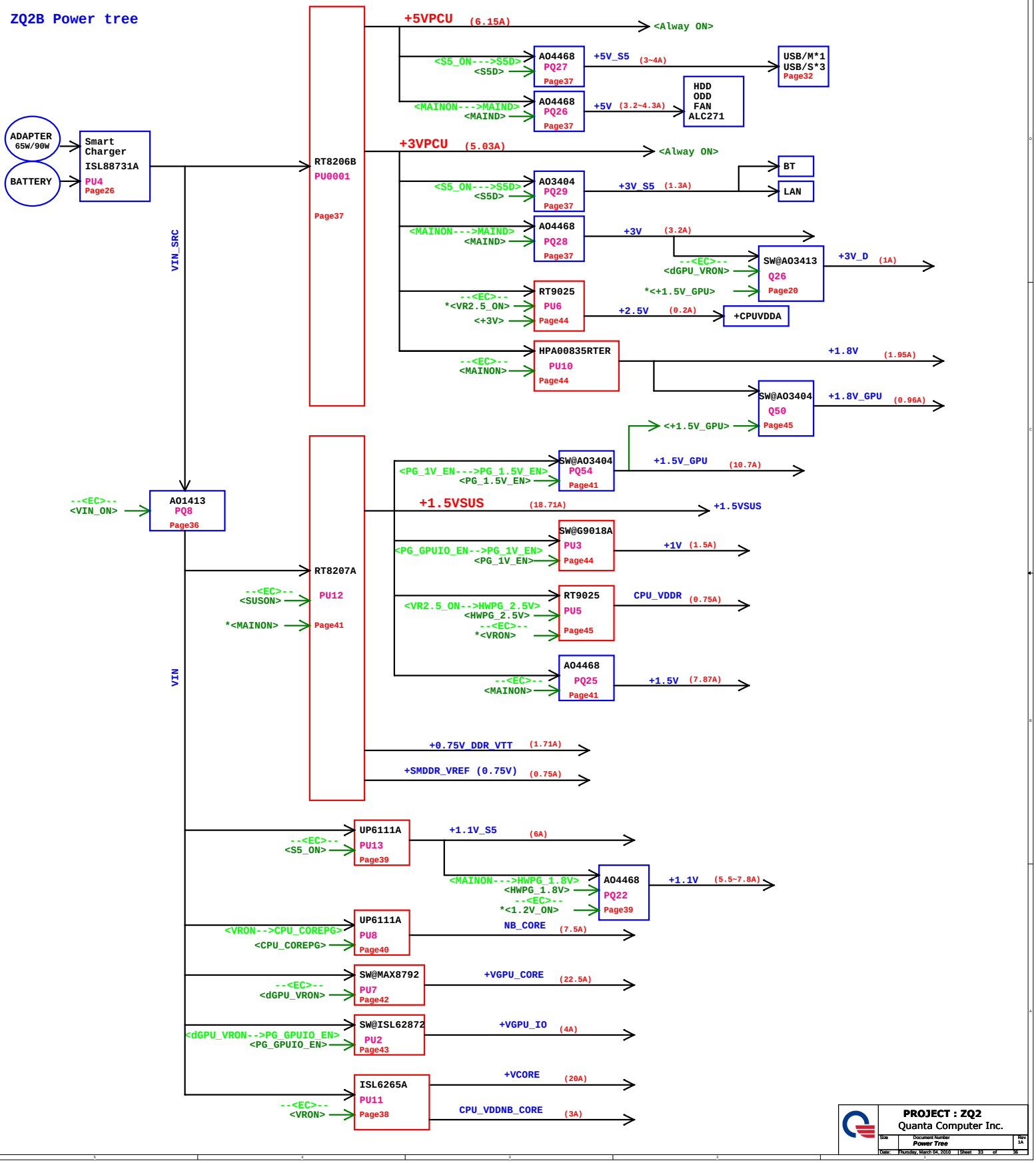
ZQ2B Power tree

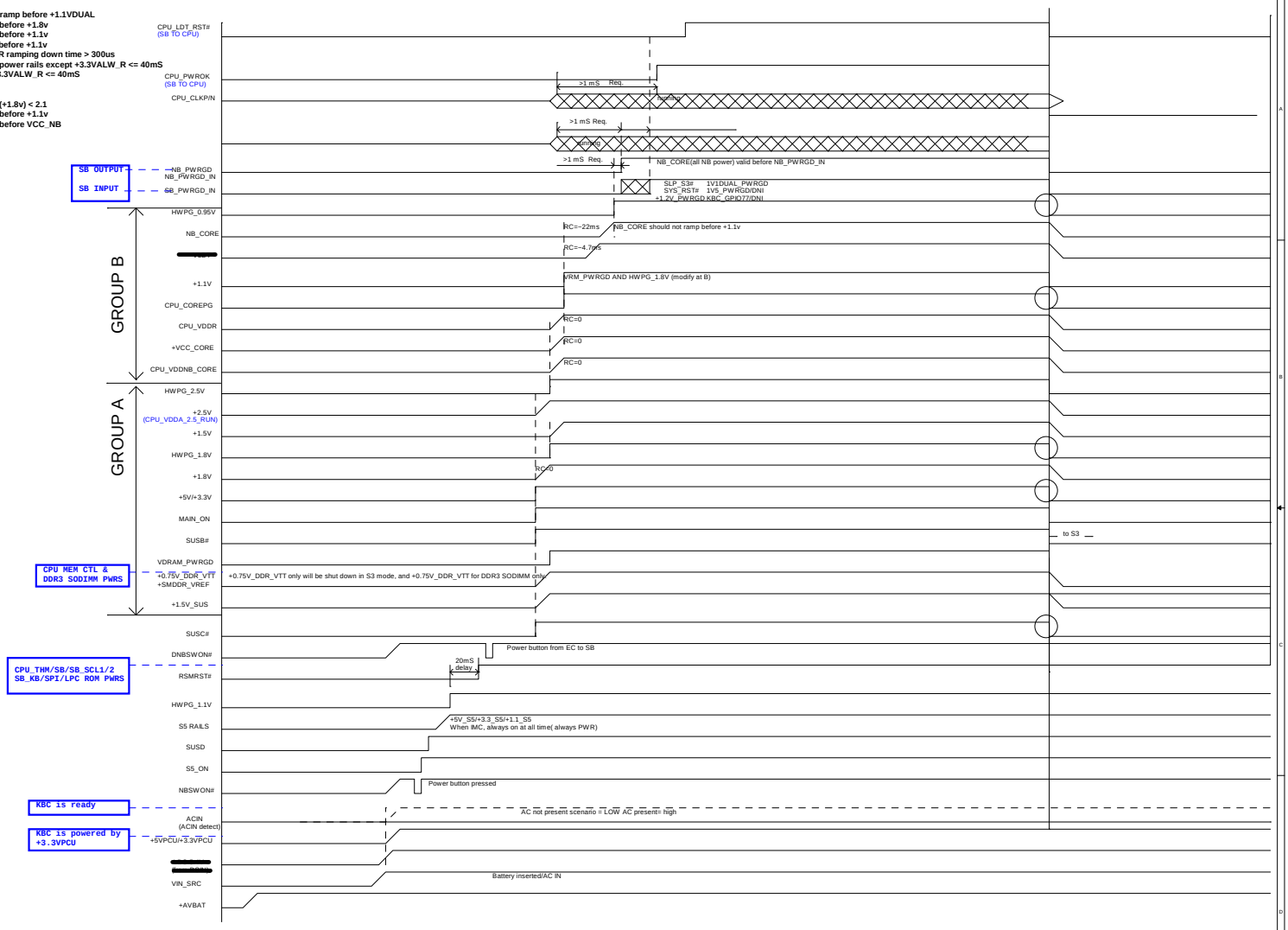


PROJECT : ZQ2
Quanta Computer Inc.
Power Tree
Thursday, March 04, 2010

Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Power Squence Chart	1A
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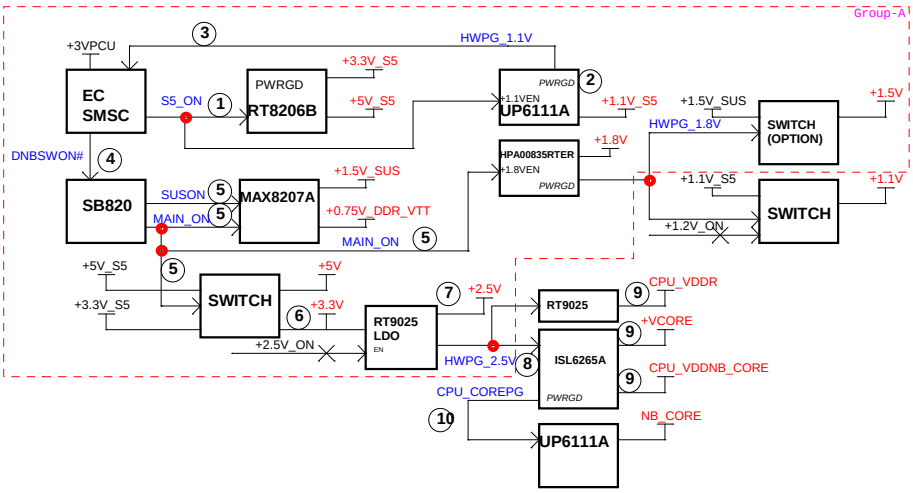
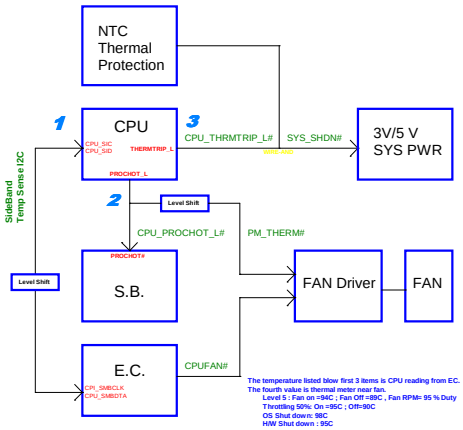


Power on Sequence required:

SB800:
1, +3.3V_S5 ramp before +1.1_S5
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

H/W Thermal Follow Chart



POWER RAILS Sequencing

1	S5_ON	13	+1.8V
2	+3.3V_S5	14	HWPG_1.8V
3	+5V_S5	15	+1.5V
4	+1.1V_S5	16	+2.5V
5	HWPG_1.1V	17	HWPG_2.5V
6	DNBSWON#	18	CPU_VDDNB_CORE
7	SUSON	19	+VCC_CORE
8	+1.5V_SUS	20	CPU_VDDR
9	+SMDDR_VTERM	21	CPU_COREPG
10	MAIN_ON	22	+1.1V
11	+5V	23	NB_CORE
12	+3.3V	24	

SB820 Sequencing

1	+3.3V_S5
2	ICH_RSMRST#
3	S0 POWER
4	PCIE_RCLKP/N
5	PCICLK[4:0]
6	SB_PWRGD_IN
7	NB_PWRGD_IN
8	LDT_PG
9	KBRST#
10	A_RST#
11	PCIRST#
12	LDT_RST#

RS880 Sequencing

1	+3.3V
2	NB POWER RAILS
3	ATX PS_PWRGD
4	NB INPUT CLOCKS
5	CPUCLK
6	NB_PWRGD
7	SB_PWRGD
8	LDT_PG/CPU_PWRGD
9	PCIRST#,NB_RST#
10	LDT_RST#
11	
12	

EC Sequencing

1	3VPCU
2	NBSWON#
3	VIN_ON
4	S5_ON
5	ICH_RSMRST#
6	-DNBSWON#
7	SUSB#/SUSC#
8	SUSON/USB_ON#
9	MAIN_ON/HWPG
10	VRON
11	PWROK
12	

PROJECT : ZQ2
Quanta Computer Inc.
Size | Document Number: PWR ON SEQ and THERM POLICY | Rev 1A
Date: Thursday, March 04, 2010 | Sheet 35 of 36

CHANGE LIST

Model	REV	CHANGE LIST
ZQ2B MB	1A	A1A The First Release.
	3A	B3A Page 02 Q23 cahnge from FDV301V to BSS138. Becasue FDV301V EOL.
		B3A Page 10 Add off-page net of +BAT for Green Adpapter. It can decrease drop voltage. R289 change value to 12K beucase charge current.
		B3A Page 15 Change R11's footprint to short pad. BOM cancel R11.
		B3A Page 22 Reserve D25 and add R401. It can cancel D1's Vf while GRN-ADP.
		B3A Page 25 Del D15 and R228. And change PWR source of ADP_ON. All for decrease drop voltage. And un-stuff Q17 in oreder to EC suggestion.
		B3A Page 25 BOM change for fine-tune. Stuff R226 and BOM unstuff C292, R230 and R233.
		B3A Page 26 BOM save PC41 and PC42.
		B3A Page 29 BOM change for Pr195 and PC169 in order to AMD power up timing requirement.

MODEL	ZQ2B	
	FROM	To
	X	1A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	

DOC NO.	PROJECT MODEL :	ZQ2B	APPROVED BY:		DATE:	2010/03/05
	PART NUMBER:		DRAWING BY:		REVISON:	1A

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Change list	1A
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