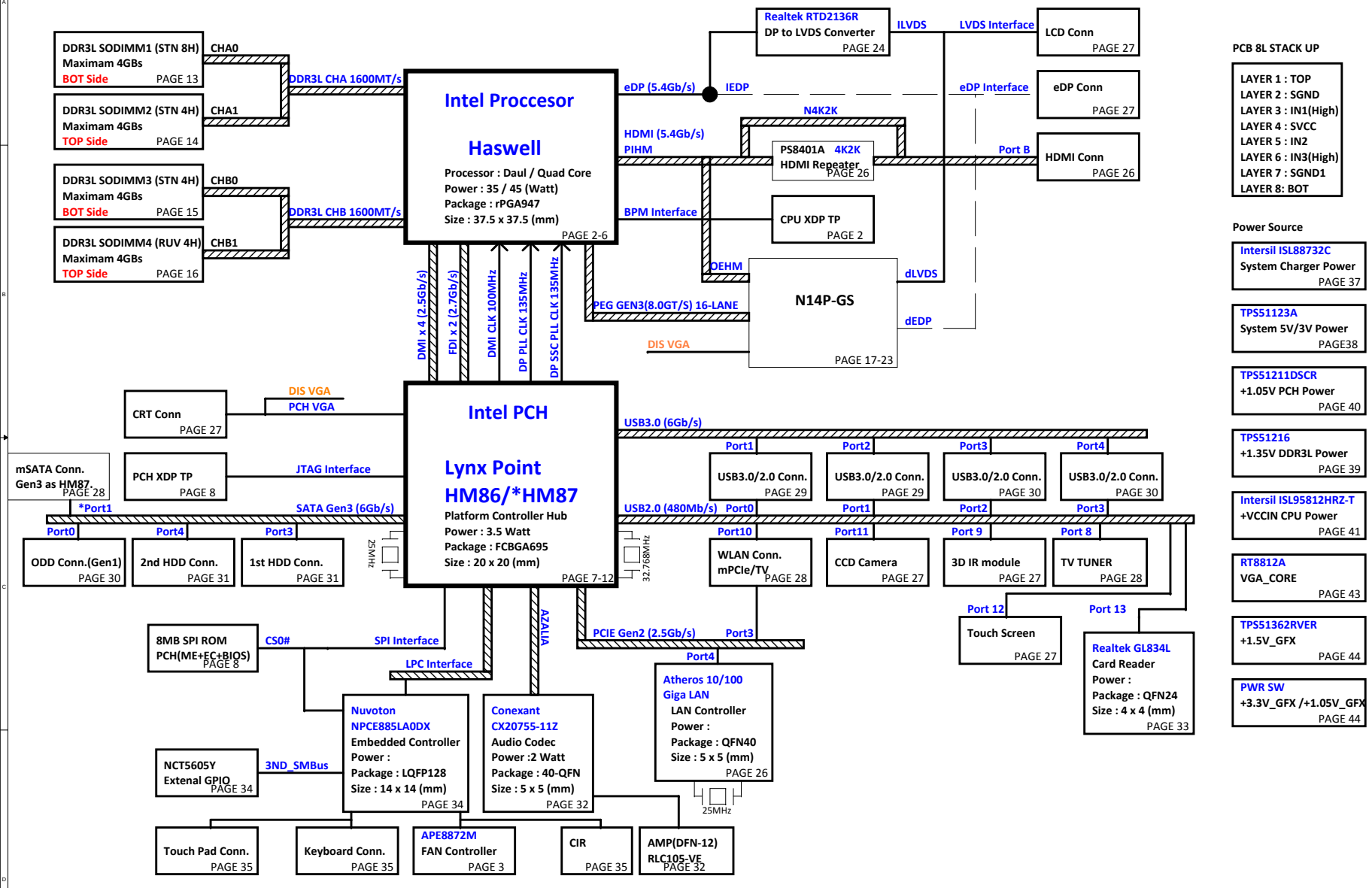
(17.3") Intel Shark Bay Platform Block Diagram

01



PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3(High)
LAYER 7 : SGND1
LAYER 8: BOT

Power Source

Intersil ISL88732C
System Charger Power
PAGE 37

TPS51123A
System 5V/3V Power
PAGE38

TPS51211DSCR
+1.05V PCH Power
PAGE 40

TPS51216
+1.35V DDR3L Power
PAGE 39

Intersil ISL95812HRZ-T
+VCCIN CPU Power
PAGE 41

RT8812A
VGA_CORE
PAGE 43

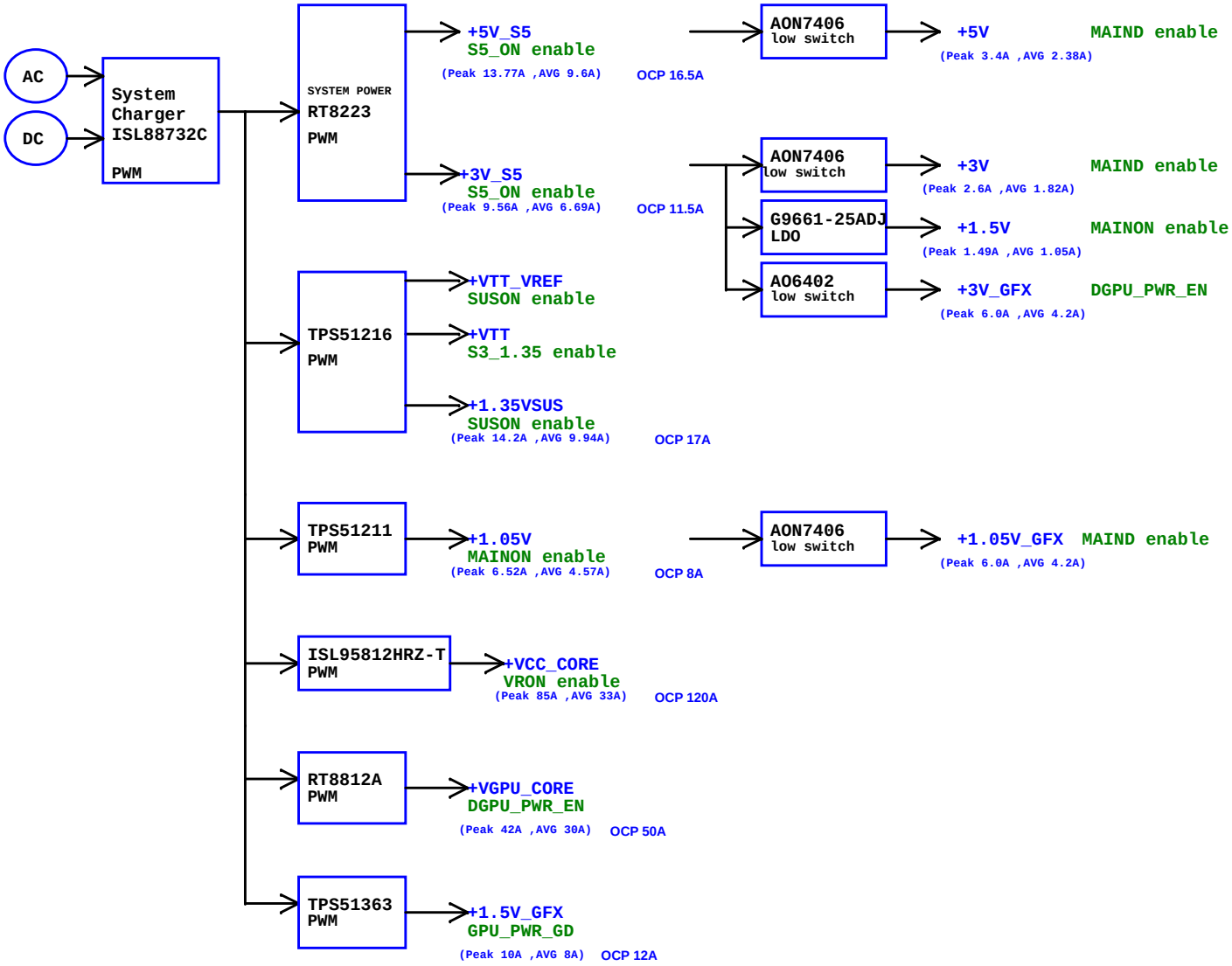
TPS51362RVER
+1.5V_GFX
PAGE 44

PWR SW
+3.3V_GFX /+1.05V_GFX
PAGE 44

Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	Block Diagram	1A

Date: Monday, December 17, 2012 Sheet 1 of 45



POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.5V	+1.5V	MAIN_ON	S0
+1.35V_SUS	+1.35V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+1.05V	+1.05V	MAIN_ON	S0

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	POWER TREE TABLE	1A

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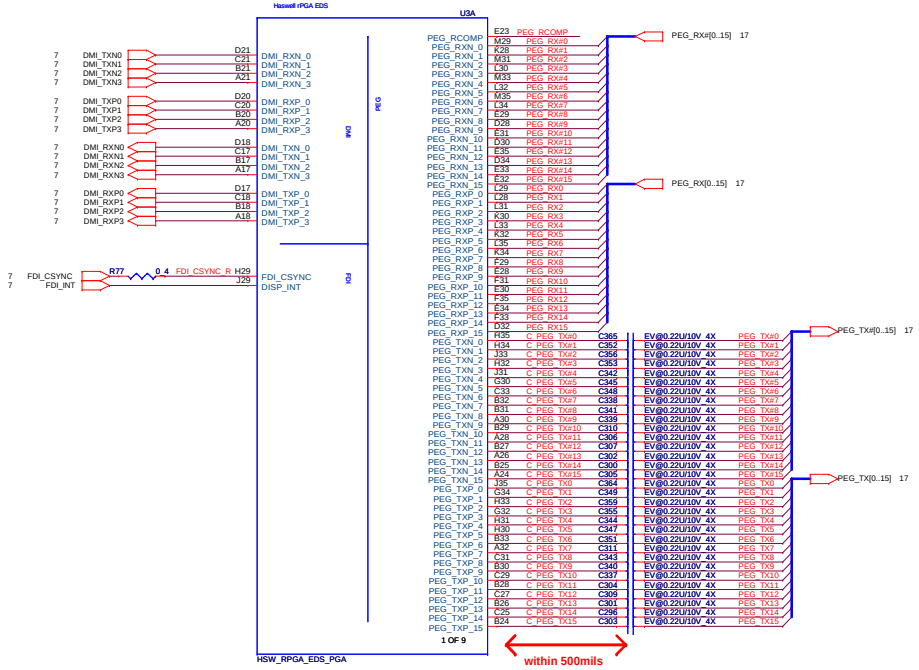
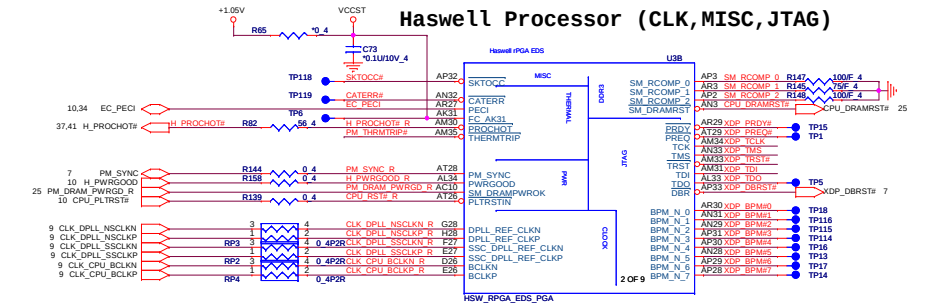
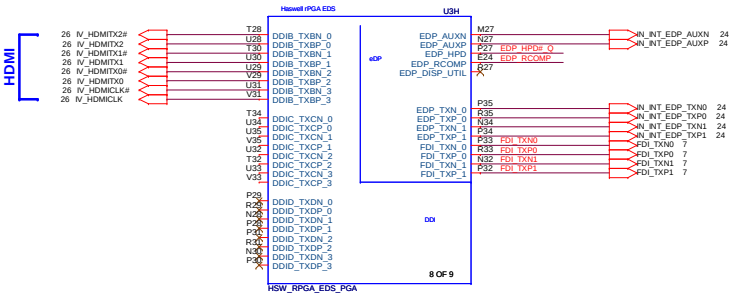
Haswell Processor (DMI,PEG,FDI)



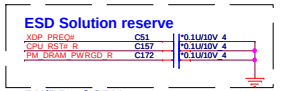
Haswell Processor (CLK,MISC,JTAG)



Haswell Processor (DDI,eDP,FDI)

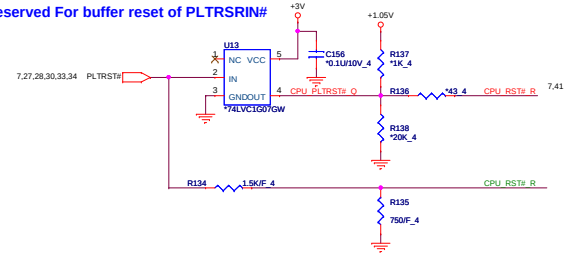


ESD Solution reserve

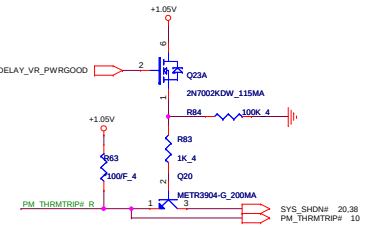


CPU

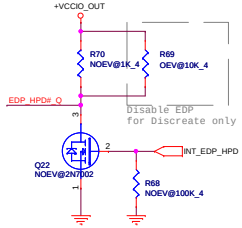
Reserved For buffer reset of PLTRSRIN#



Thermal Trip & Process HOT CPU

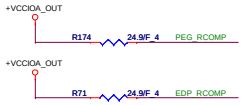


eDP Hot Plug Detect CPU

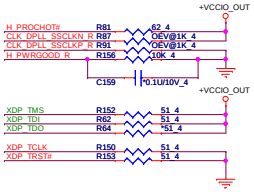


FDI Disabling (Discrete Only) <CPU>

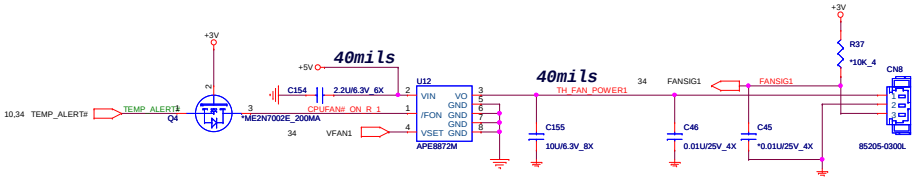
DP & PEG Compensation <CPU>



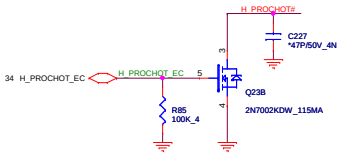
PU/PD of CPU



FAN Control-->For one FAN solution <THC>

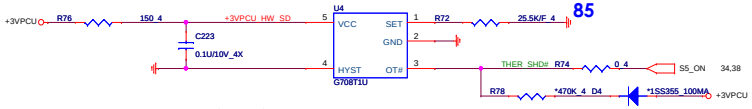


Intel Turbo mode only CPU



CPU Thermal sensor / MB Local TEMP <THC>

Local TEMP = 85



Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 85dgree
Hysteresis is 30C

Quanta Computer Inc.
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Size	Document Number	Rev
	Haswell 1/5 (PEG/DMI/FDI)	1A
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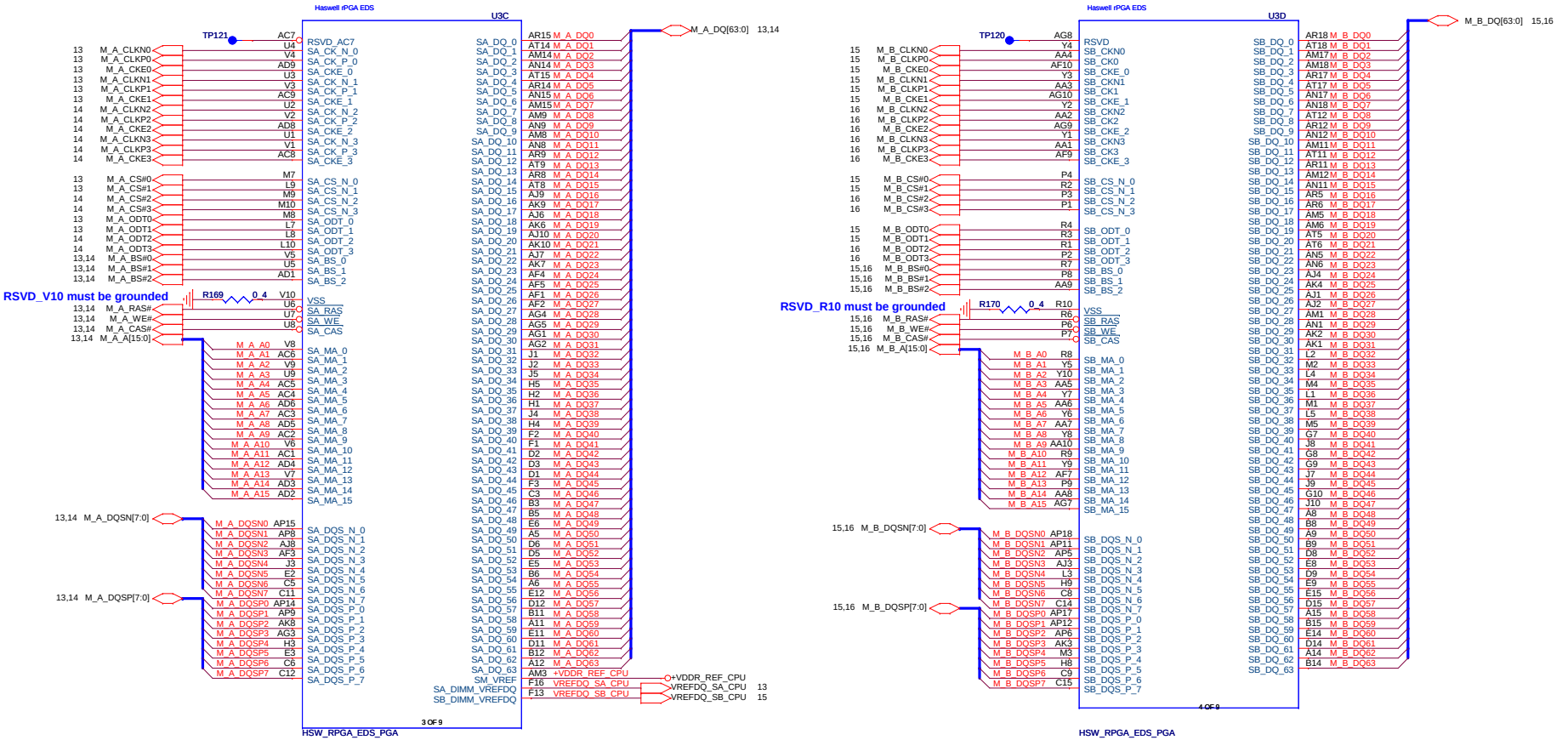
03

Haswell Processor (DDR3)



Quanta Computer Inc.	
PROJECT : BDBE	
Size	Document Number: Haswell 2/5 (DDR3 I/F) — Rev: 1A
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Haswell Processor (POWER)

05

+1.35V_CPU 4.2A

Haswell rPGA EDS

U3E

+VCCIN 95A

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

REV 1.0 change, depop R724

300mA

300mA

5 OF 9

HSW_RPGA_EDS_PGA

Power Test Propose

REV 1.0 change
Pop R741

REV 1.0 change
Pop R743

MOW WW12-->if PWR_DEBUG# is routed to the XDP the R741 value is 150 ohm

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to CPU

DG V0.7 -> 110 Ohm
SCH V0.7 -> 130 Ohm

Place PU resistor close to CPU

DG V0.7 -> 44 Ohm
SCH V0.7 -> 43 Ohm

Quanta Computer Inc.

PROJECT : BDBE

Size	Document Number	Rev
	Haswell 4/5 (POWER)	1A

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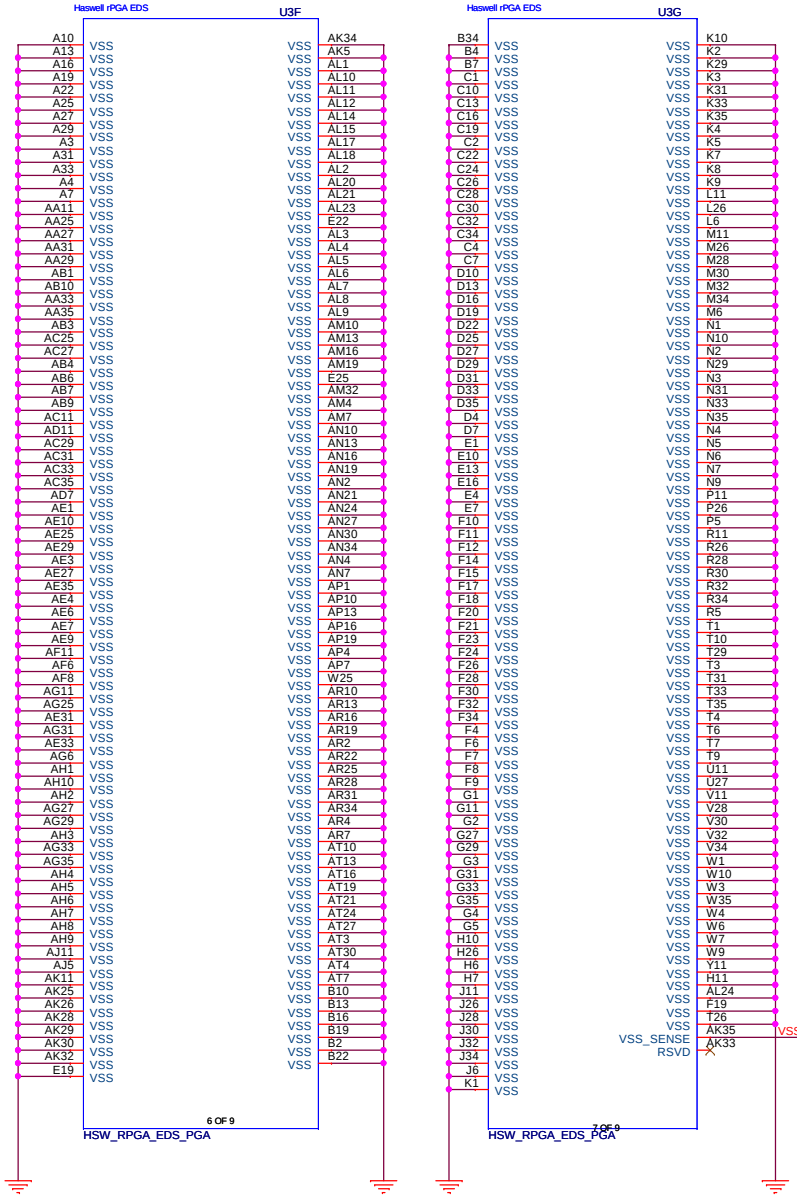
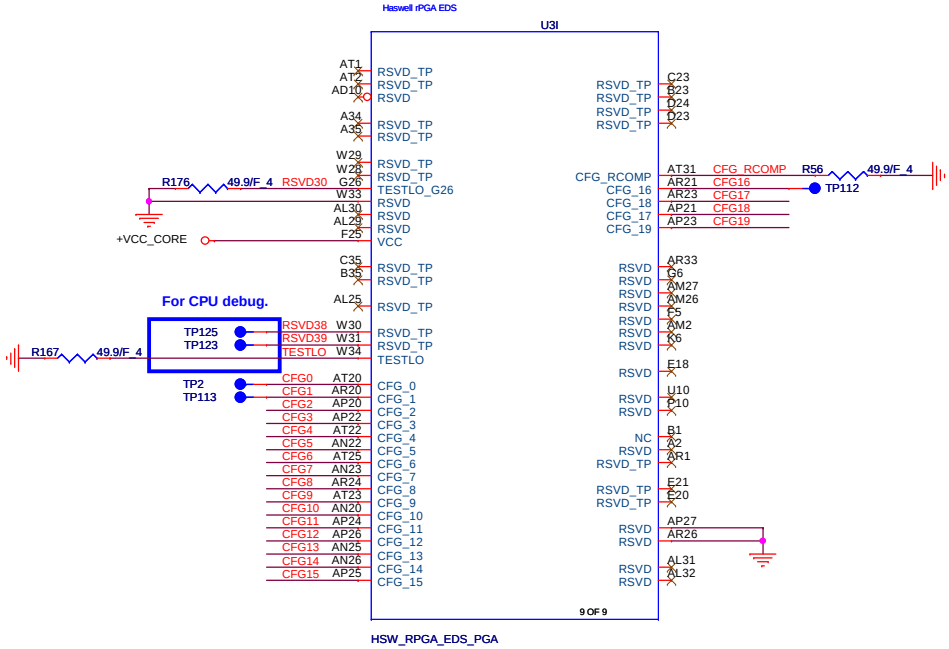
Haswell Processor (GND)



Haswell Processor (CFG,RSVD)



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R140 *1K_4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R60 NOEV@1K_4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R143 *1K_4 CFG5 R141 *1K_4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	CFG7 R142 *1K_4

Quanta Computer Inc.

PROJECT : BDBE

Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	1A

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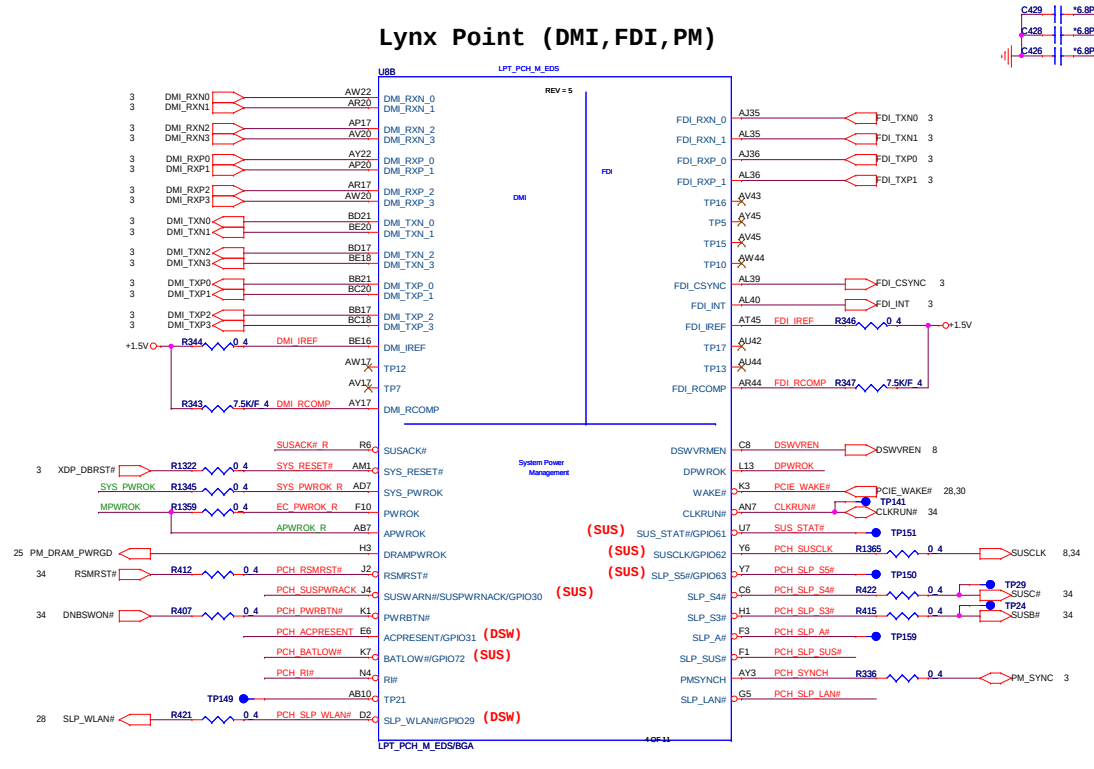
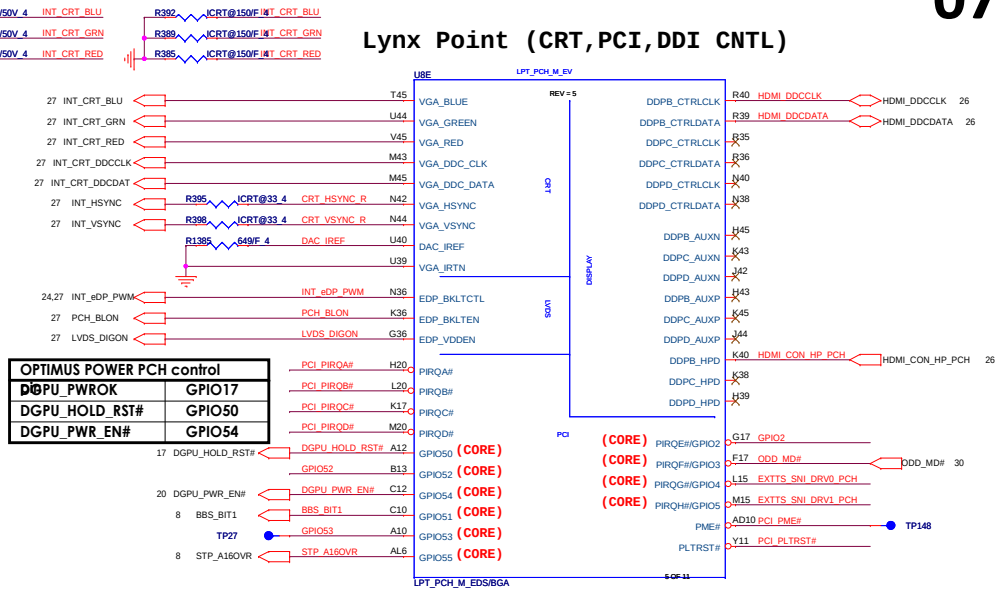
06

Lynx Point (DMI,FDI,PM)

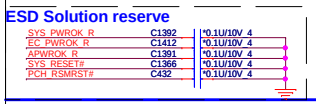


Lynx Point (CRT,PCI,DDI CNTL)

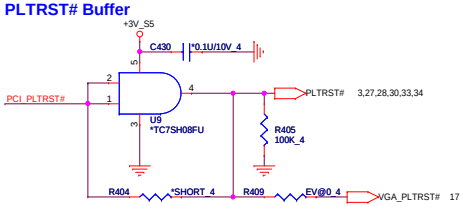


OPTIMUS POWER PCH control	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO50
DGPU_PWR_EN#	GPIO54

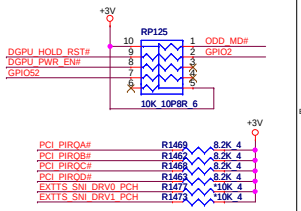
ESD Solution reserve



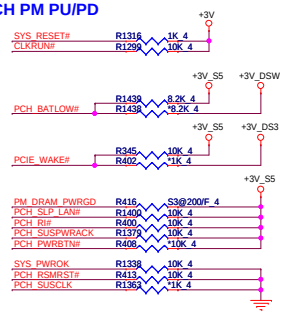
PLTRST# Buffer



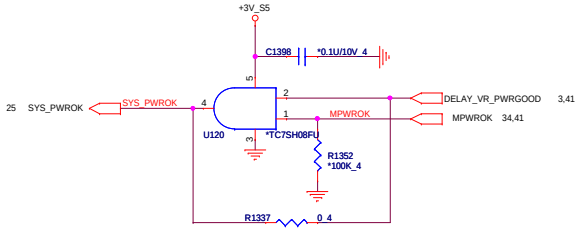
PCI PU



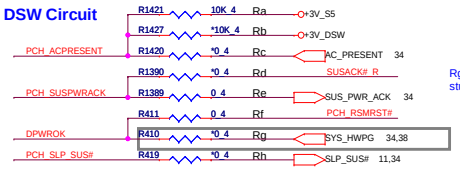
PCH PM PU/PD



SYSPWOK

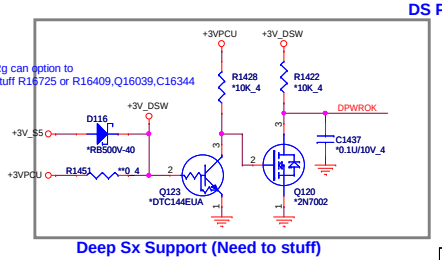


DSW Circuit



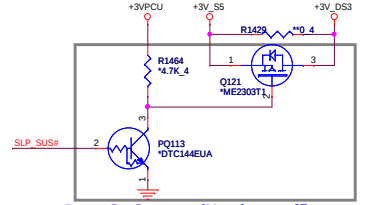
Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

Rg can option to stuff R16725 or R16409,Q16039,C16344



Deep Sx Support (Need to stuff)

DS Power



Deep Sx Support (Need to stuff)

Quanta Computer Inc.
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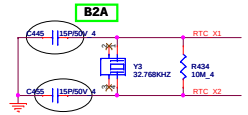
Lynx Point (RTC,THDA,SATA,JTAG)

Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)

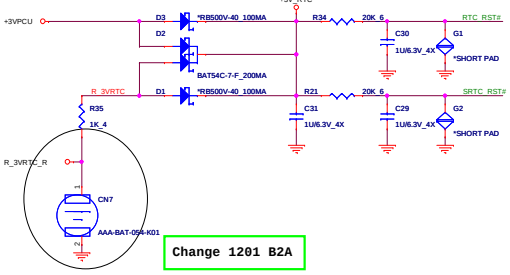
08

RTC Clock 32.768KHz (RTC)



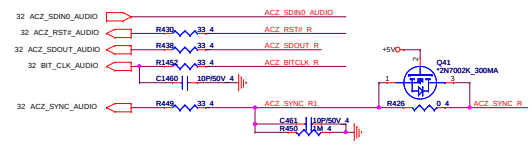
RTC Circuitry (RTC)

Trace = 30mils for power



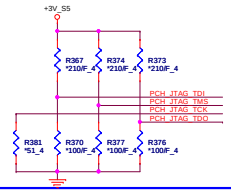
Change 1201 B2A

HDA

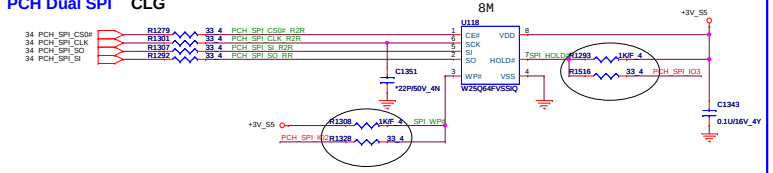


PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

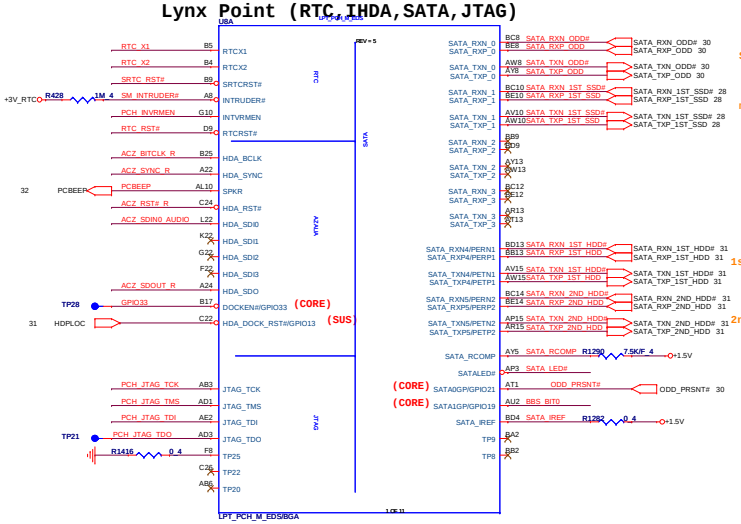


PCH Dual SPI CLG



EC (EC+BIOS):SPI_CS0# Change 11/27

Lynx Point (RTC,THDA,SATA,JTAG)



SATA ODD

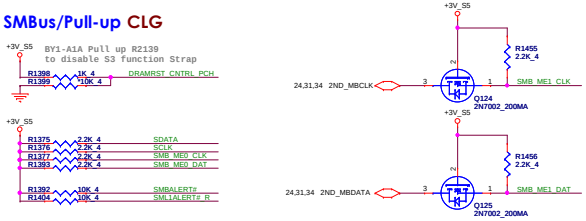
mSATA

1st SATA HDD

2nd SATA HDD

CLG

SMBus/Pull-up CLG



PCH STRAPING

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	PCBEEP R1424 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	7,34 SUSCLK R1364 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	7 STP_A16OVR R1332 *1K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R1430 330K_4 +3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 1 0 Resvered 1 1 SPI 0 0 LPC	7 BBS_BIT1 R1431 *1K_4 BBS_BIT0 R355 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	34 ACZ_SDOUT R ACZ_SDOUT R423 *1K_4 +VCC_HDA_IO
GPIO36	RSVD	PWROK	Internal PD	10 GPIO36 R357 *1K_4 +3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	10 FDI_OVRVLTG R368 *1K_4 +3V
GPIO8	RSVD	RSMRST#	Internal PU	10 GPIO8 R388 10K_4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	10 PLL_ODVR_EN R1356 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Disable 1 = Enable Must be PU to VCCRTC	7 DSWVREN R429 330K_4 R432 330K_4 +3V_RTC

Check list V1.0 Removed the GPIO28 signal information of PLL VR enable signal

Quanta Computer Inc.
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	LPT 2/6 (SATA/HDA/SPI)	1A

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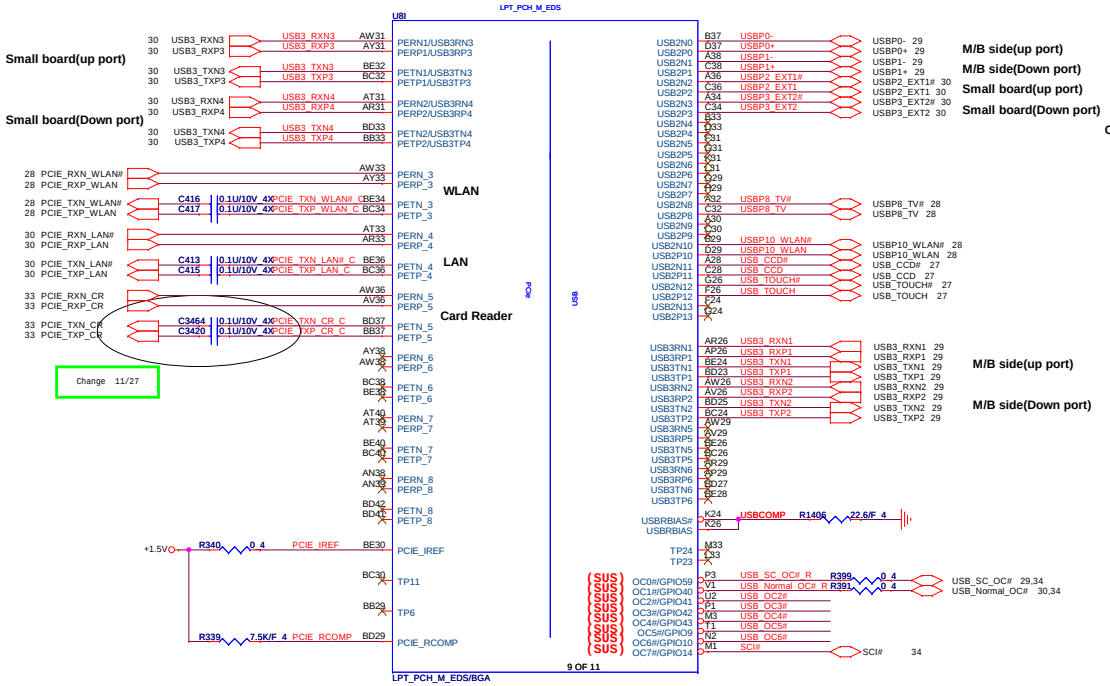
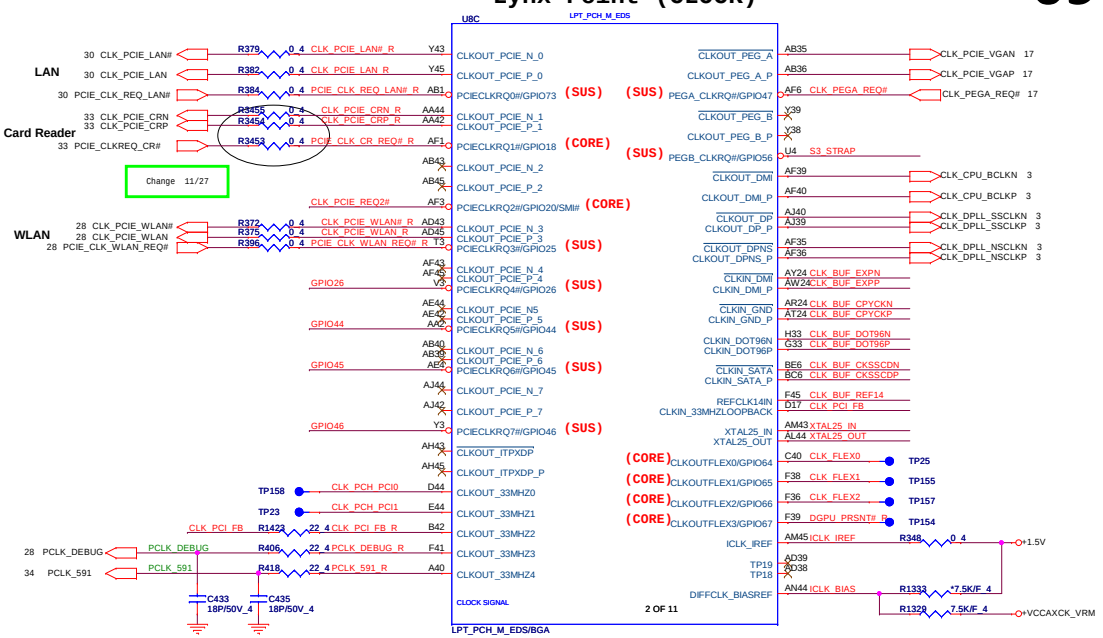
Lynx Point (PCIE,USB3.0,USB2.0)

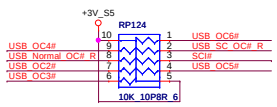
Lynx Point (CLOCK)

09

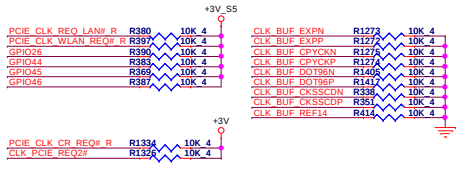


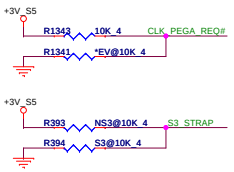


USB Overcurrent

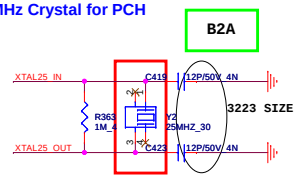


PCH Intenal Clock





25MHz Crystal for PCH



Quanta Computer Inc.			
PROJECT : BDBE			
Size	Document Number		Rev
	LPT 3/6 (PCIE/USB/CLK)		1A
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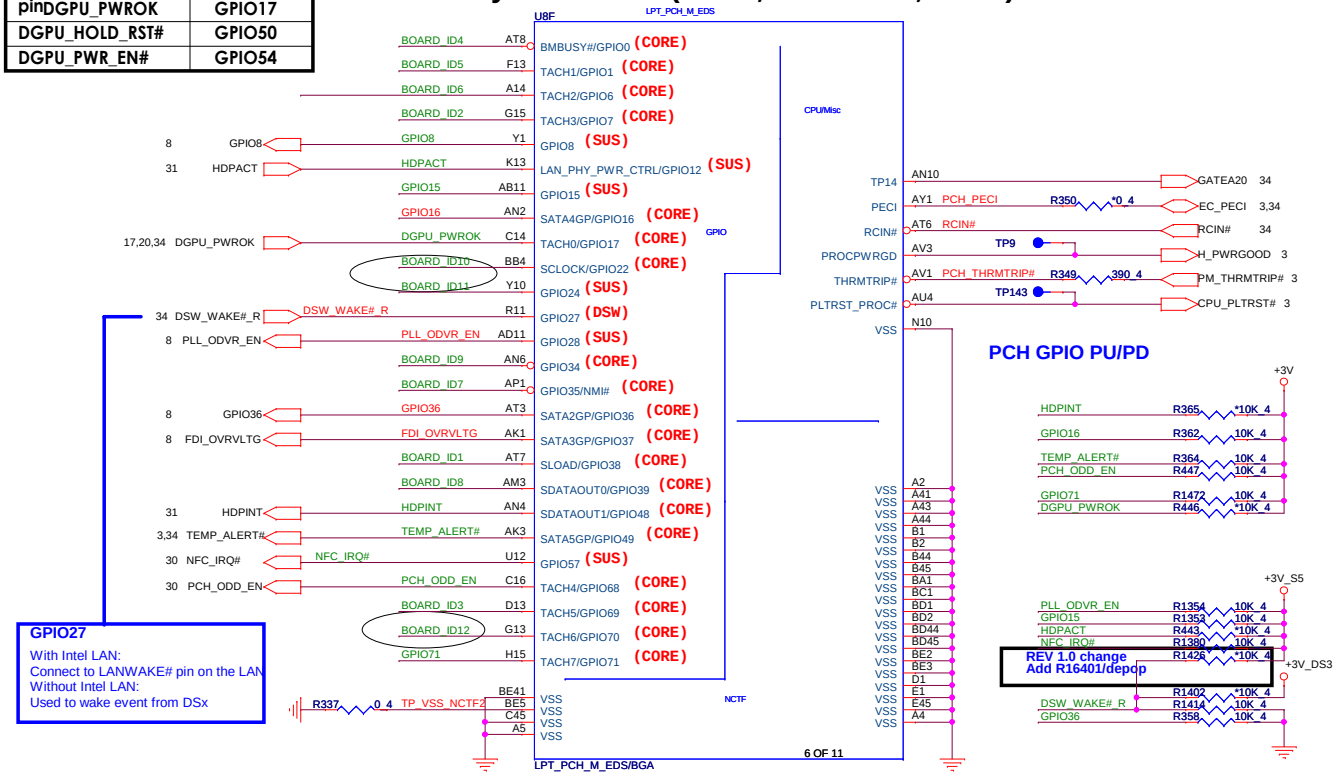
Lynx Point (GPIO,CPU/MISC,NCTF)

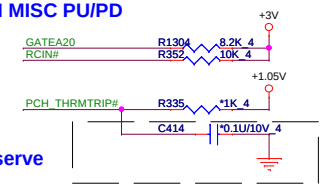
OPTIMUS POWER PCH control	
pinDGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO50
DGPU_PWR_EN#	GPIO54



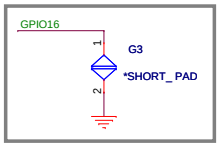
GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

PCH GPIO PU/PD

PCH MISC PU/PD



PU & Password Clear

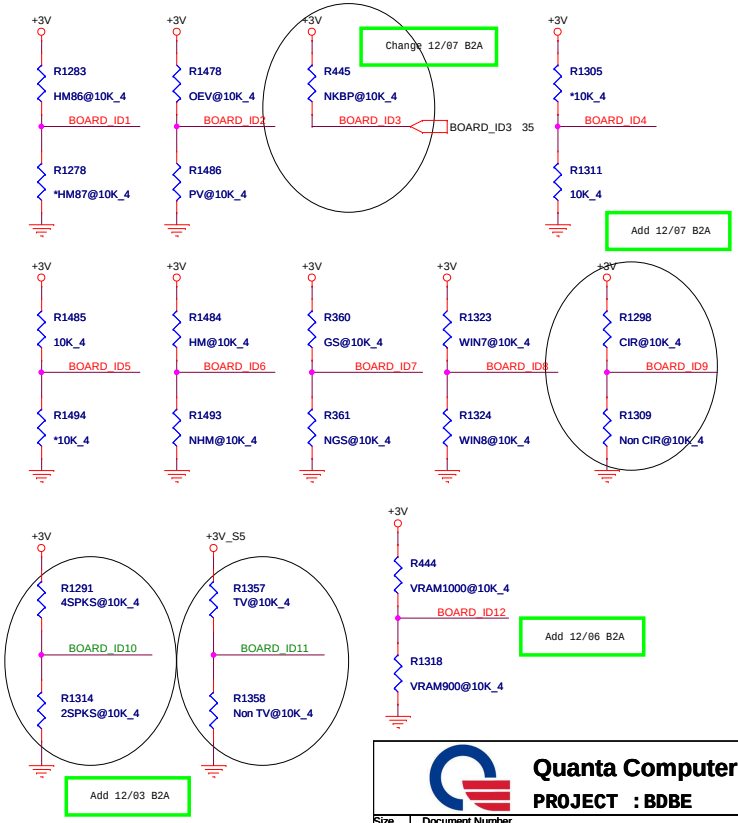


REV-B2A Add G3 for Clear CMOS password

ESD Solution Reserve

BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11	ID12
HM86 HM87	H L											
Only VGA OPTIMUS		H L										
W/O LED KB W/ LED KB			H L									
UMA Discrete				H L								
17" Premium 17" Gaming					H L							
W/ HDMI W/O HDMI						H L						
W/ G-sensor W/O G-sensor							H L					
WIN7 WIN8								H L				
W/ CIR W/O CIR									H L			
4 SPKS 2 SPKS										H L		
TV SKU SSD SKU											H L	
VRAM 1000 VRAM 900												H L



Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	1A
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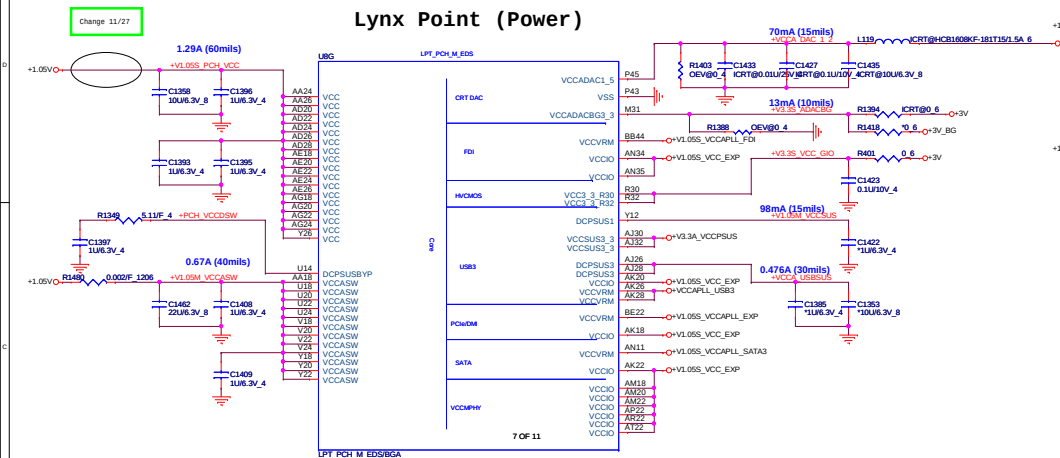
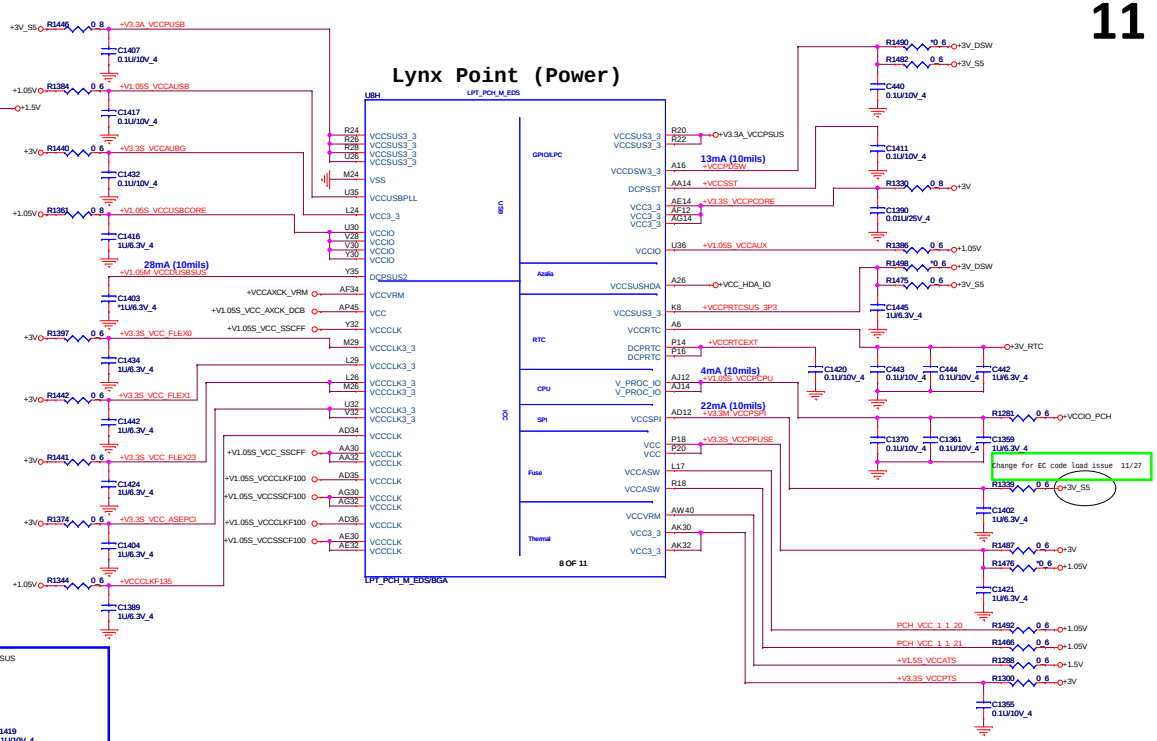
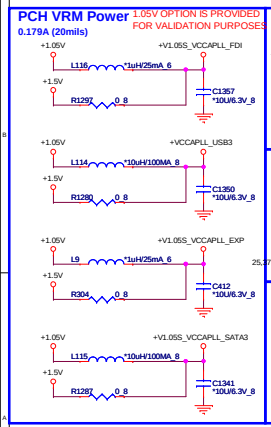
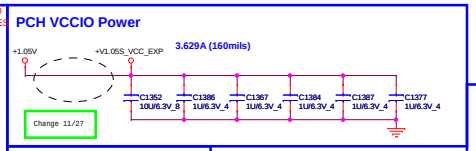
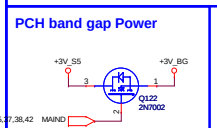
Lynx Point (Power)

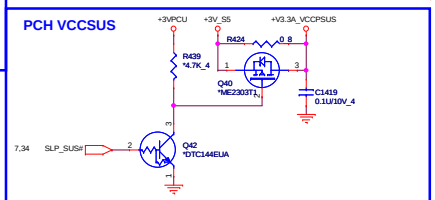




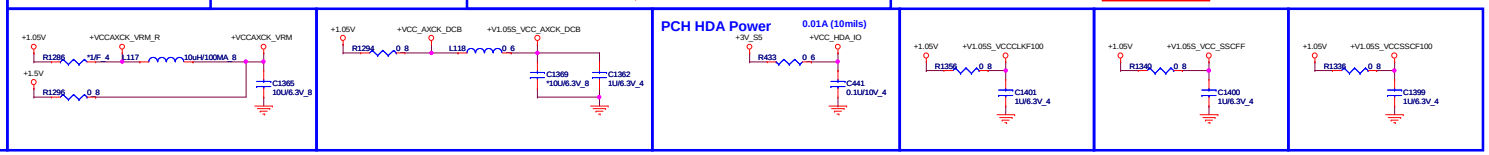








VCCCLK:
0.306A (20mils)



Quanta Computer Inc.		
PROJECT : BDBE		
Size	Document Number	Rev
	LPT 5/6 (POWER)	1A
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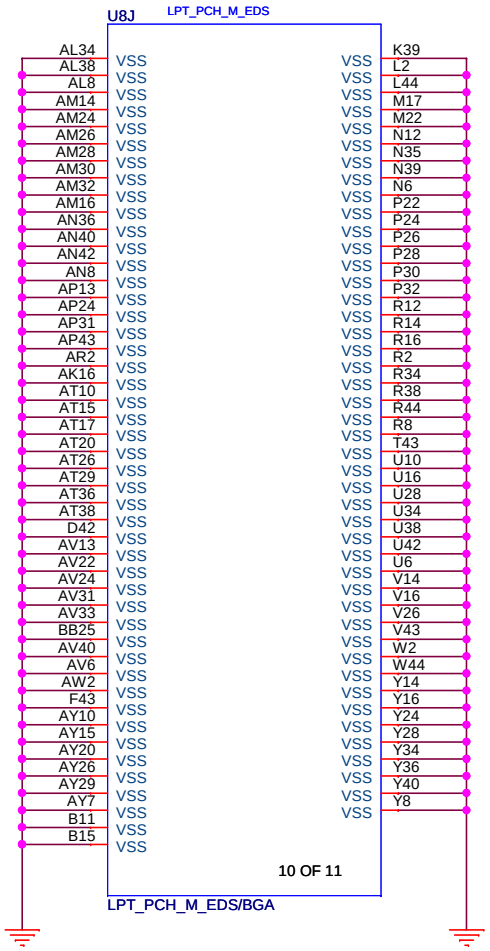
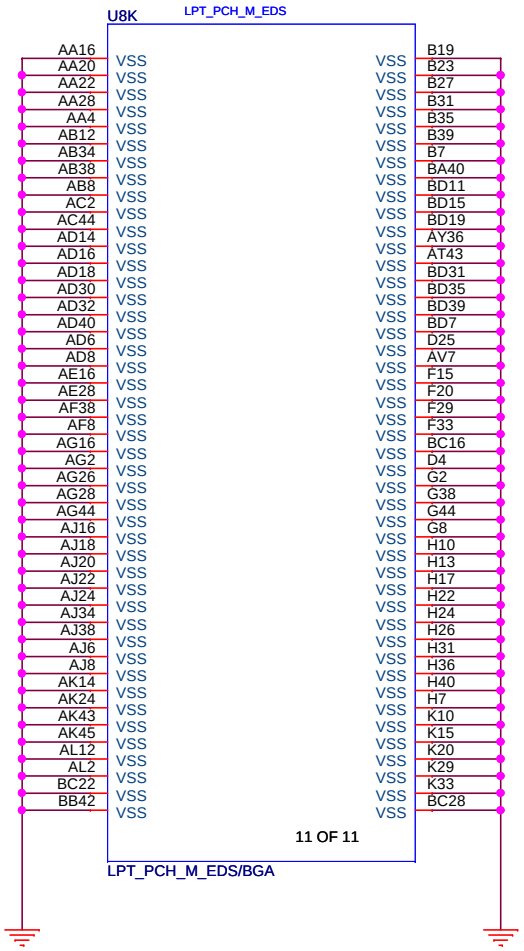
Lynx Point (GND)



Lynx Point (GND)



Quanta Computer Inc.

PROJECT : BDBE

Size	Document Number	Rev
	LPT 6/6 (GND)	1A

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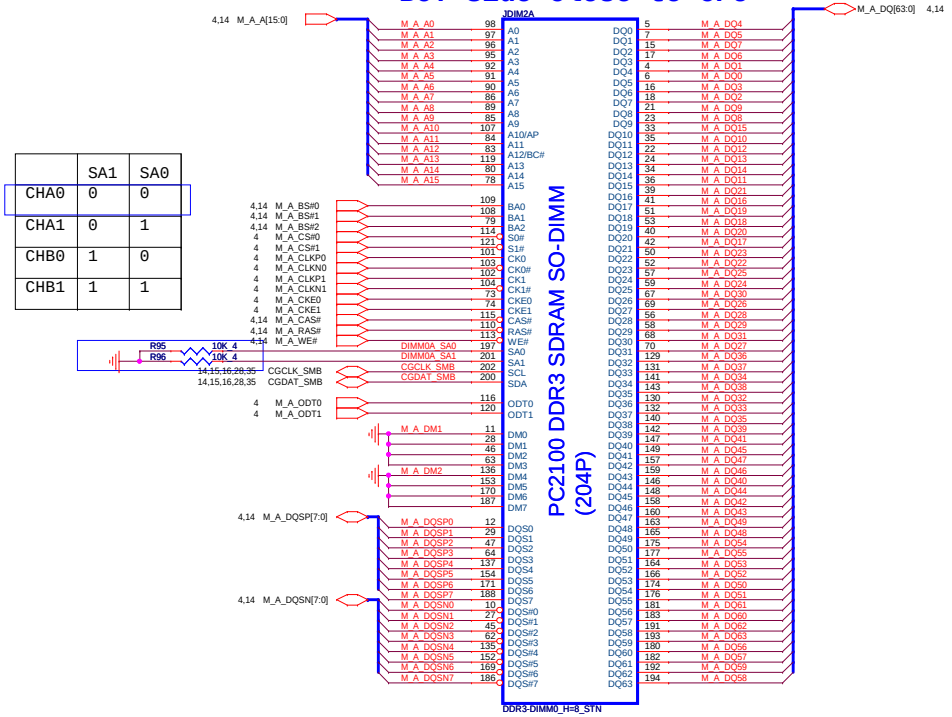
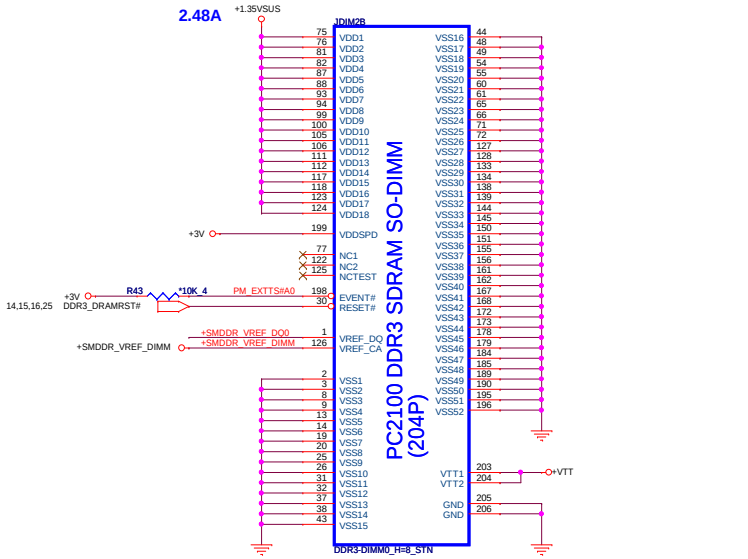
BOT Side Close to CPU

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



2.48A

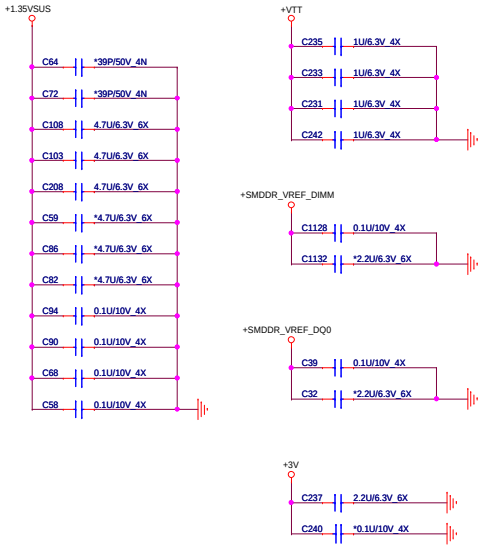


3,7,8,9,10,11,14,15,16,20,24,26,27,28,30,31,33,34,35,36,38,42 +3V

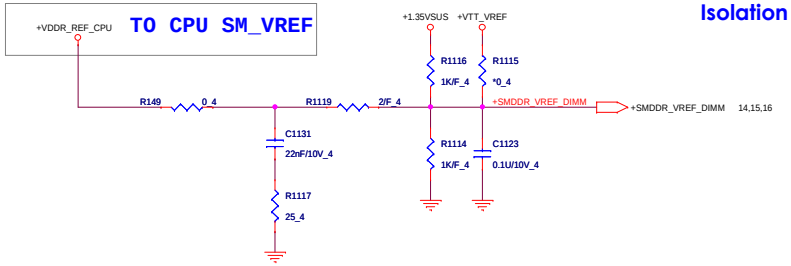
14,15,16,25,39 +VTT

14,15,16 +SMDDR_VREF_DIMM

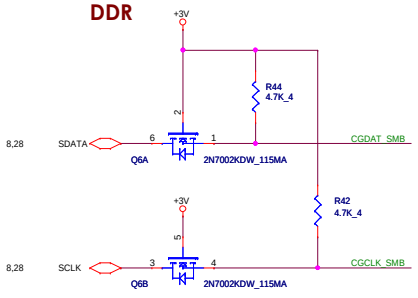
Place these Caps near So-Dimm0.



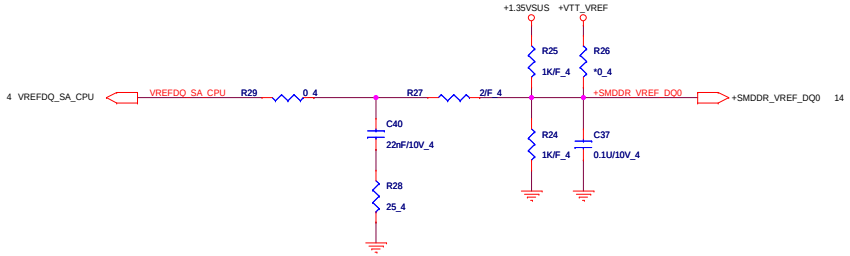
DDR3 VREF CA DDR



SMBus Isolation DDR



DDR3 VREF DQ0 (M1+M3) DDR



ESD Solution Reserve

Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	System Memory 1/2 (5.2H)	1A
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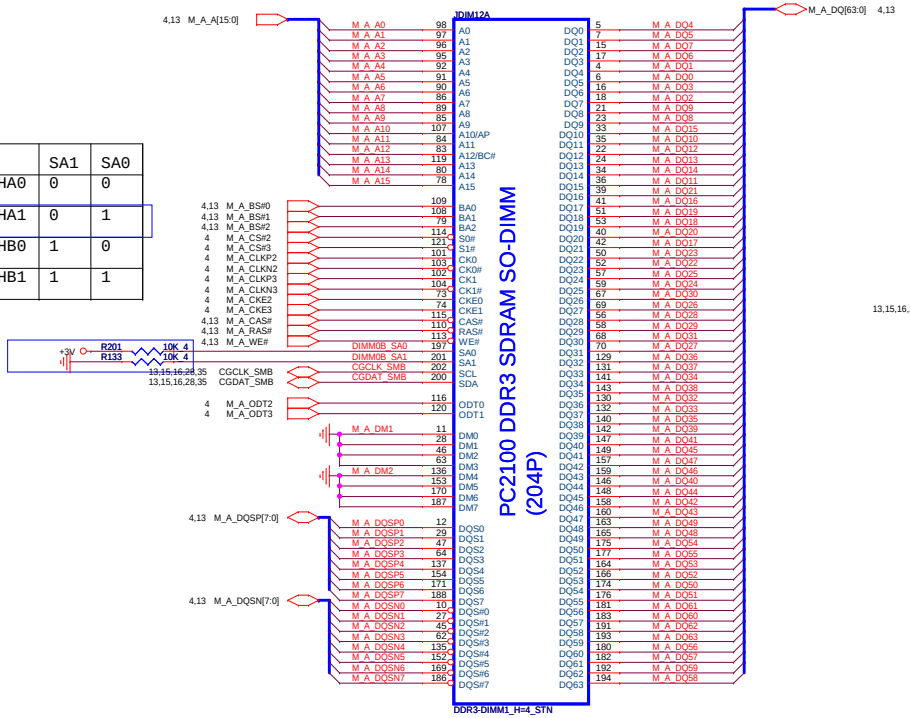
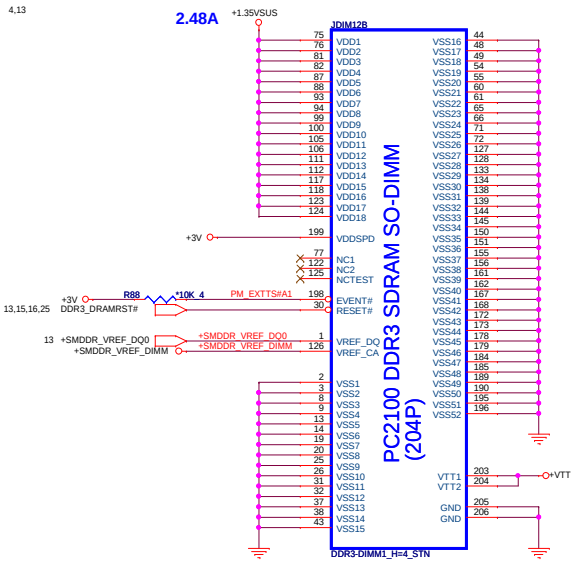
TOP Side Close to CPU

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



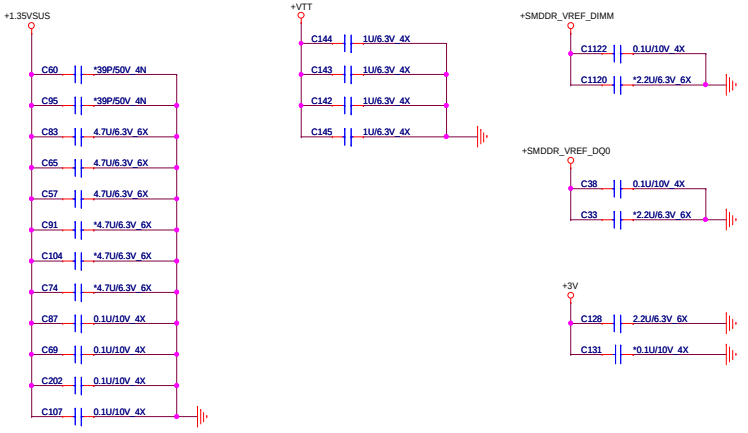


3,7,8,9,10,11,13,15,16,20,24,26,27,28,30,31,33,34,35,36,38,42 +3V

13,15,16,25,39 +VTT

13,15,16 +SMDDR_VREF_DIMM

Place these Caps near So-Dimm0.



ESD Solution Reserve

Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	CPU/PCH XDP	1A
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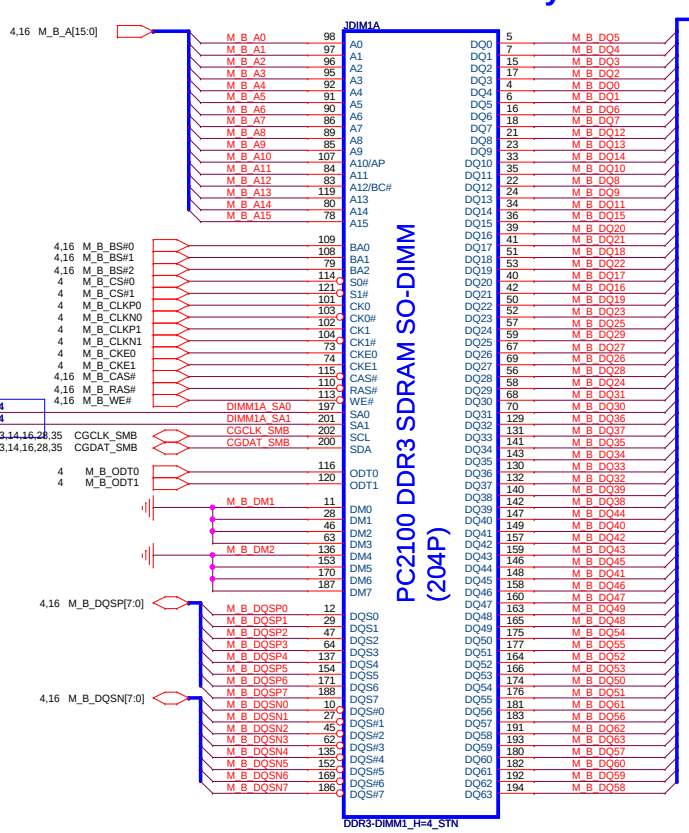
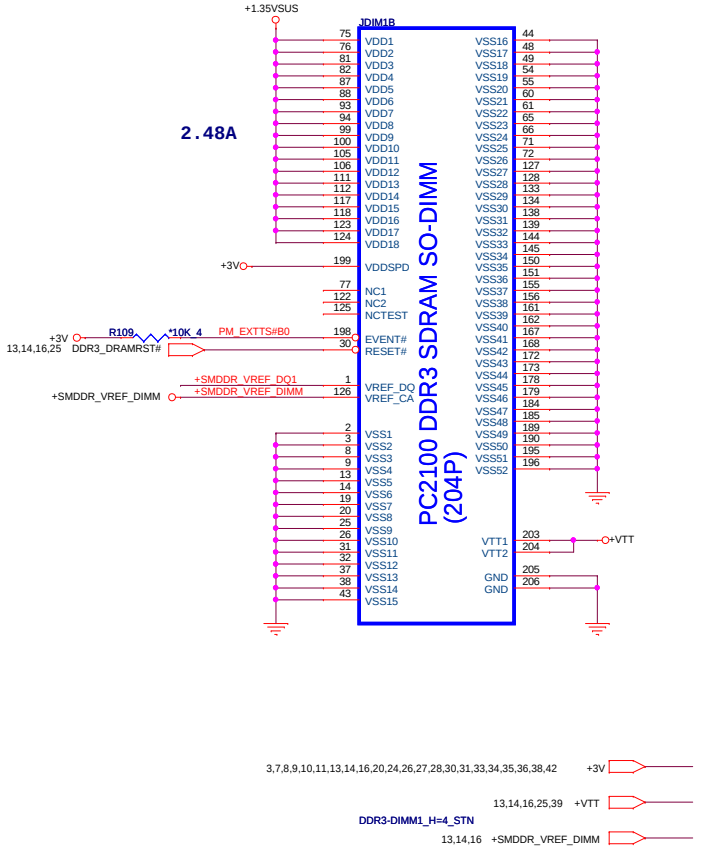
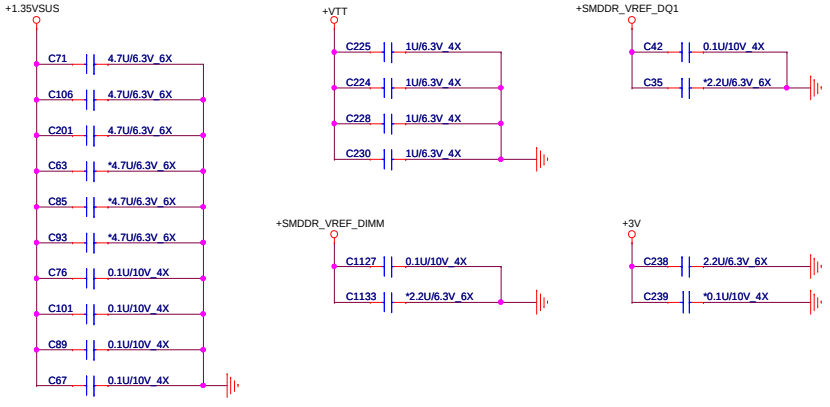
BOT Side Far away CPU

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

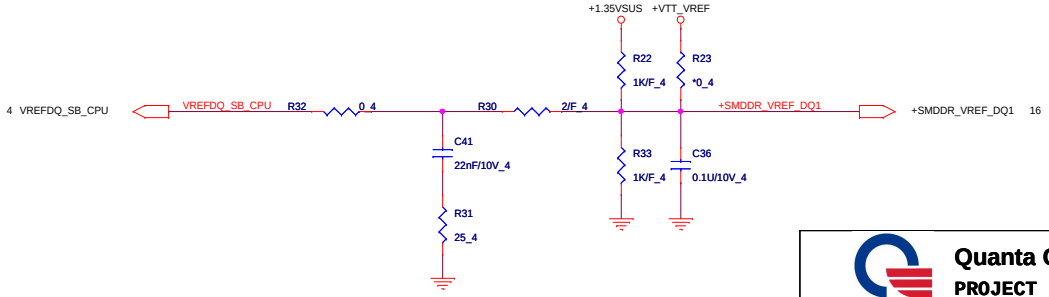




Place these Caps near So-Dimm1.



DDR3 VREF DQ1 (M1+M3) DDR



ESD Solution Reserve

Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	System Memory 2/2 (9.2H)	1A

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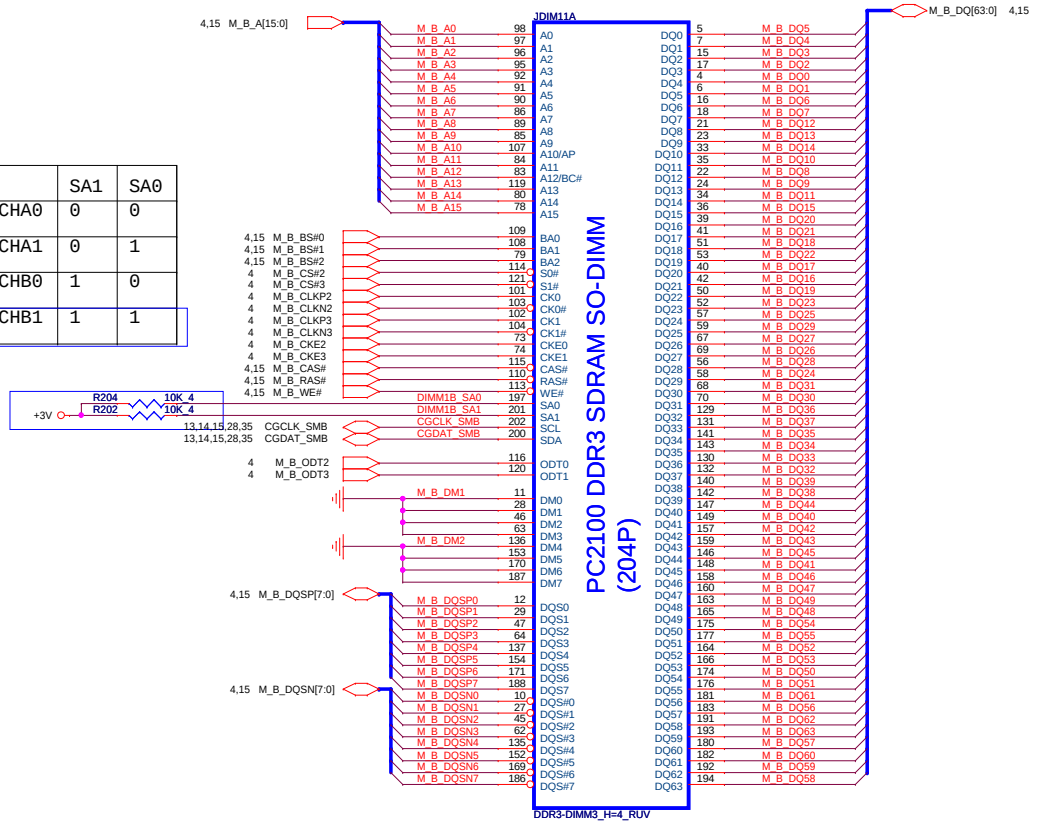
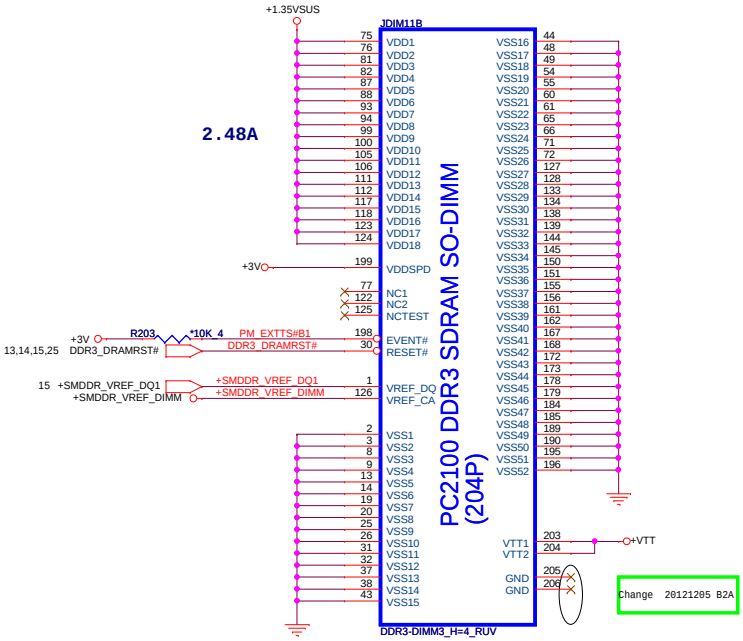
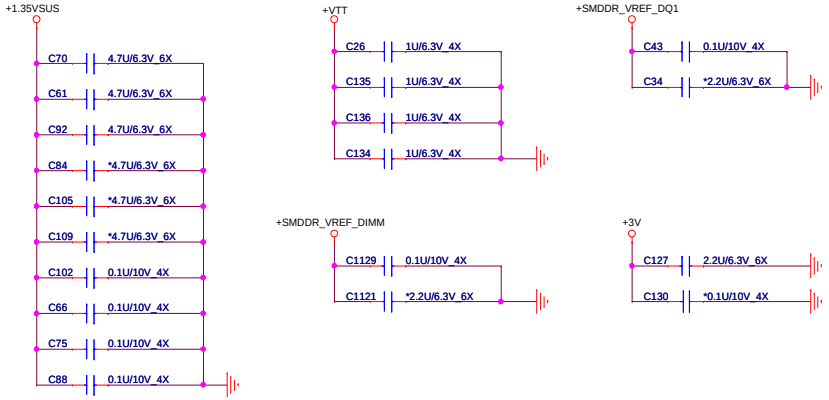
TOP Side Far away CPU

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1





Place these Caps near So-Dimm1.



ESD Solution Reserve

Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	02_Thames_M2/ GPIO_DP_CRT_I2C	1A

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U7A
EV@N14P-GS

[PEG Interface]

PEX_IOVDD/Q : 3300mA
+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C366 EV@22U/6.3VS_6
C367 EV@22U/6.3VS_6
C371 EV@22U/6.3VS_6
C373 EV@22U/6.3VS_6
C381 EV@10U/6.3VS_6
C378 EV@10U/6.3VS_6
C379 EV@10U/6.3VS_6
C382 EV@10U/6.3VS_6

PLACE NEAR BALLS

C1264 EV@1U/6.3V_4
C1253 EV@1U/6.3V_4
C1242 EV@1U/6.3V_4
C1260 EV@1U/6.3V_4

PLACE UNDER BGA

C1250 EV@4.7U/6.3V_6
C1245 EV@4.7U/6.3V_6

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6

AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

VDD33 : 85mA
+3V_GFX

J8 VDD33_1
K8 VDD33_2
L8 VDD33_3
M8 VDD33_4

PLACE CLOSE TO BGA

C1282 EV@4.7U/6.3V_6
C1323 EV@2.2U/6.3V_6

PLACE CLOSE TO GPU BALLS

C1333 EV@1U/6.3V_4
C1280 EV@0.1U/10V_4
C1279 EV@0.1U/10V_4
C1284 EV@0.1U/10V_4

PEX_RX0 AN12 PEG_TX0 3
PEX_RX0_N AM12 PEG_TX#0 3
PEX_RX1 AN14 PEG_TX1 3
PEX_RX1_N AM14 PEG_TX#1 3
PEX_RX2 AP14 PEG_TX2 3
PEX_RX2_N AP15 PEG_TX#2 3
PEX_RX3 AN15 PEG_TX3 3
PEX_RX3_N AM15 PEG_TX#3 3
PEX_RX4 AN17 PEG_TX4 3
PEX_RX4_N AM17 PEG_TX#4 3
PEX_RX5 AP17 PEG_TX5 3
PEX_RX5_N AP18 PEG_TX#5 3
PEX_RX6 AN18 PEG_TX6 3
PEX_RX6_N AM18 PEG_TX#6 3
PEX_RX7 AN20 PEG_TX7 3
PEX_RX7_N AM20 PEG_TX#7 3
PEX_RX8 AP20 PEG_TX8 3
PEX_RX8_N AP21 PEG_TX#8 3
PEX_RX9 AN21 PEG_TX9 3
PEX_RX9_N AM21 PEG_TX#9 3
PEX_RX10 AN23 PEG_TX10 3
PEX_RX10_N AM23 PEG_TX#10 3
PEX_RX11 AP23 PEG_TX11 3
PEX_RX11_N AP24 PEG_TX#11 3
PEX_RX12 AN24 PEG_TX12 3
PEX_RX12_N AM24 PEG_TX#12 3
PEX_RX13 AN26 PEG_TX13 3
PEX_RX13_N AM26 PEG_TX#13 3
PEX_RX14 AP26 PEG_TX14 3
PEX_RX14_N AP27 PEG_TX#14 3
PEX_RX15 AN27 PEG_TX15 3
PEX_RX15_N AM27 PEG_TX#15 3

PEX_TX0 AK14 C_PEG_RX0 C1203 EV@0.22U/10V_4 PEG_RX0 3
PEX_TX0_N AJ14 C_PEG_RX#0 C1206 EV@0.22U/10V_4 PEG_RX#0 3
PEX_TX1 AH14 C_PEG_RX1 C1219 EV@0.22U/10V_4 PEG_RX1 3
PEX_TX1_N AG14 C_PEG_RX#1 C1223 EV@0.22U/10V_4 PEG_RX#1 3
PEX_TX2 AK15 C_PEG_RX2 C1208 EV@0.22U/10V_4 PEG_RX2 3
PEX_TX2_N AJ15 C_PEG_RX#2 C1209 EV@0.22U/10V_4 PEG_RX#2 3
PEX_TX3 AL16 C_PEG_RX3 C1211 EV@0.22U/10V_4 PEG_RX3 3
PEX_TX3_N AK16 C_PEG_RX#3 C1213 EV@0.22U/10V_4 PEG_RX#3 3
PEX_TX4 AK17 C_PEG_RX4 C1200 EV@0.22U/10V_4 PEG_RX4 3
PEX_TX4_N AJ17 C_PEG_RX#4 C1201 EV@0.22U/10V_4 PEG_RX#4 3
PEX_TX5 AH17 C_PEG_RX5 C1197 EV@0.22U/10V_4 PEG_RX5 3
PEX_TX5_N AG17 C_PEG_RX#5 C1199 EV@0.22U/10V_4 PEG_RX#5 3
PEX_TX6 AK18 C_PEG_RX6 C1202 EV@0.22U/10V_4 PEG_RX6 3
PEX_TX6_N AJ18 C_PEG_RX#6 C1205 EV@0.22U/10V_4 PEG_RX#6 3
PEX_TX7 AL19 C_PEG_RX7 C1190 EV@0.22U/10V_4 PEG_RX7 3
PEX_TX7_N AK19 C_PEG_RX#7 C1193 EV@0.22U/10V_4 PEG_RX#7 3
PEX_TX8 AK20 C_PEG_RX8 C1195 EV@0.22U/10V_4 PEG_RX8 3
PEX_TX8_N AJ20 C_PEG_RX#8 C1194 EV@0.22U/10V_4 PEG_RX#8 3
PEX_TX9 AH20 C_PEG_RX9 C1188 EV@0.22U/10V_4 PEG_RX9 3
PEX_TX9_N AG20 C_PEG_RX#9 C1186 EV@0.22U/10V_4 PEG_RX#9 3
PEX_TX10 AK21 C_PEG_RX10 C1183 EV@0.22U/10V_4 PEG_RX10 3
PEX_TX10_N AJ21 C_PEG_RX#10 C1177 EV@0.22U/10V_4 PEG_RX#10 3
PEX_TX11 AL22 C_PEG_RX11 C1196 EV@0.22U/10V_4 PEG_RX11 3
PEX_TX11_N AK22 C_PEG_RX#11 C1198 EV@0.22U/10V_4 PEG_RX#11 3
PEX_TX12 AK23 C_PEG_RX12 C1192 EV@0.22U/10V_4 PEG_RX12 3
PEX_TX12_N AJ23 C_PEG_RX#12 C1189 EV@0.22U/10V_4 PEG_RX#12 3
PEX_TX13 AH23 C_PEG_RX13 C1182 EV@0.22U/10V_4 PEG_RX13 3
PEX_TX13_N AG23 C_PEG_RX#13 C1176 EV@0.22U/10V_4 PEG_RX#13 3
PEX_TX14 AK24 C_PEG_RX14 C1171 EV@0.22U/10V_4 PEG_RX14 3
PEX_TX14_N AJ24 C_PEG_RX#14 C1167 EV@0.22U/10V_4 PEG_RX#14 3
PEX_TX15 AL25 C_PEG_RX15 C1174 EV@0.22U/10V_4 PEG_RX15 3
PEX_TX15_N AK25 C_PEG_RX#15 C1172 EV@0.22U/10V_4 PEG_RX#15 3

PEX_REFCLK AL13 CLK_PCIE_VGAP 9
PEX_REFCLK_N AK13 CLK_PCIE_VGAN 9

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R261 *EV@200_4
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#

PEX_WAKE AJ11
PEX_RST_N AJ12 VGA_RST# R1234 *EV@0_4/S PEGX_RST#

PEX_CLKREQ_N AK12 PEX_CLKREQ# R1232 EV@10K_4 +3V_GFX

PEX_TERMP AP29 PEX_TERMP R259 EV@2.49K/F_4

TESTMODE AK11 TESTMODE R1233 EV@10K_4

PEX_PLLVDD AG26 PEX_PLLVDD PEX_PLLVDD : 150mA
+1.05V_GFX
R1209 *EV@0_6
L17 EV@PBY160808T-300Y-N
C1224 EV@4.7U/6.3V_6 PLACE NEAR BGA CLOSE TO CAPS
C1216 EV@1U/6.3V_4 PLACE UNDER BGA
C1215 EV@0.1U/10V_4 PLACE NEAR BALLS

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
PEX_SVDD_3V3 : 210mA
EV@0.1U/10V_4 C1272
EV@4.7U/6.3V_6 C1325
EV@4.7U/6.3V_6 C1281
+3V_GFX
PLACE NEAR BGA

3.3V_AUX_NC P8

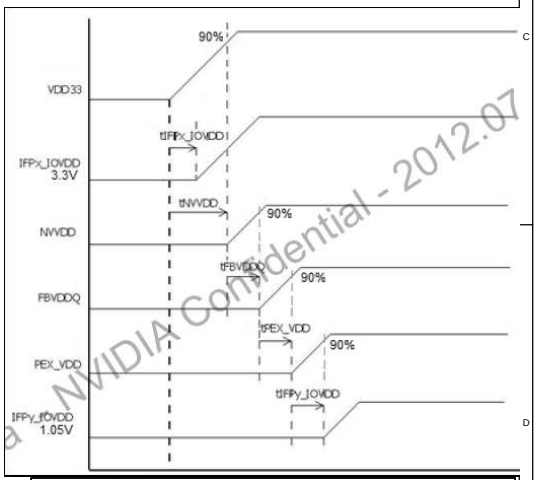
VDD_SENSE L4 VGA_VCCSENSE 43

GND_SENSE L5 VGA_VSSSENSE 43

+3V_GFX R278 EV@4.7K_4
10,20,34 DGPU_PWROK R283 *EV@0_4
Q30 EV@DTC144EUA
PEX_CLKREQ# 2
Q28 EV@DTC144EUA
+3V_GFX
Q27 *EV@2N7002
CLK_PEGA_REQ# 9

Change follow vendor advice 0913

+3V_GFX
U113 EV@MC74VHC1G08DFT2G
C1276 EV@0.1U/10V_4
7 VGA_PLTRST#
7 DGPU_HOLD_RST#
PEGX_RST# 20
R1236 EV@100K_4
R1235 *OEV@0_4



19,20,21,26,43,44 +3V_GFX
18,20,21,22,23,36,44 +1.5V_GFX
18,19,20,44 +1.05V_GFX
3,7,8,9,10,11,13,14,15,16,20,24,26,27,28,30,31,33,34,35,36,38,42 +3V

Quanta Computer Inc.
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Size	Document Number	Rev
	N14P-GS - 1/5 (PCIE)	1A
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U7B
EV@N14P-GS

[MEMORY I/F A]

U7C
EV@N14P-GS

MEMORY I/F C

PVBDDQ : 5000mA

PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO BGA

PLACE NEAR BGA CLOSE TO CAPS

PLACE CLOSE TO BALL

Need check 0911

Add 0911

CALIBRATION PIN	GDDR5
FB_CALx_PD_VDDQ	40
FB_CALx_PU_GND	42.2
FB_CALx_TERM_GND	51.1

Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	N14P-GS - 2/5 (Memory)	1A

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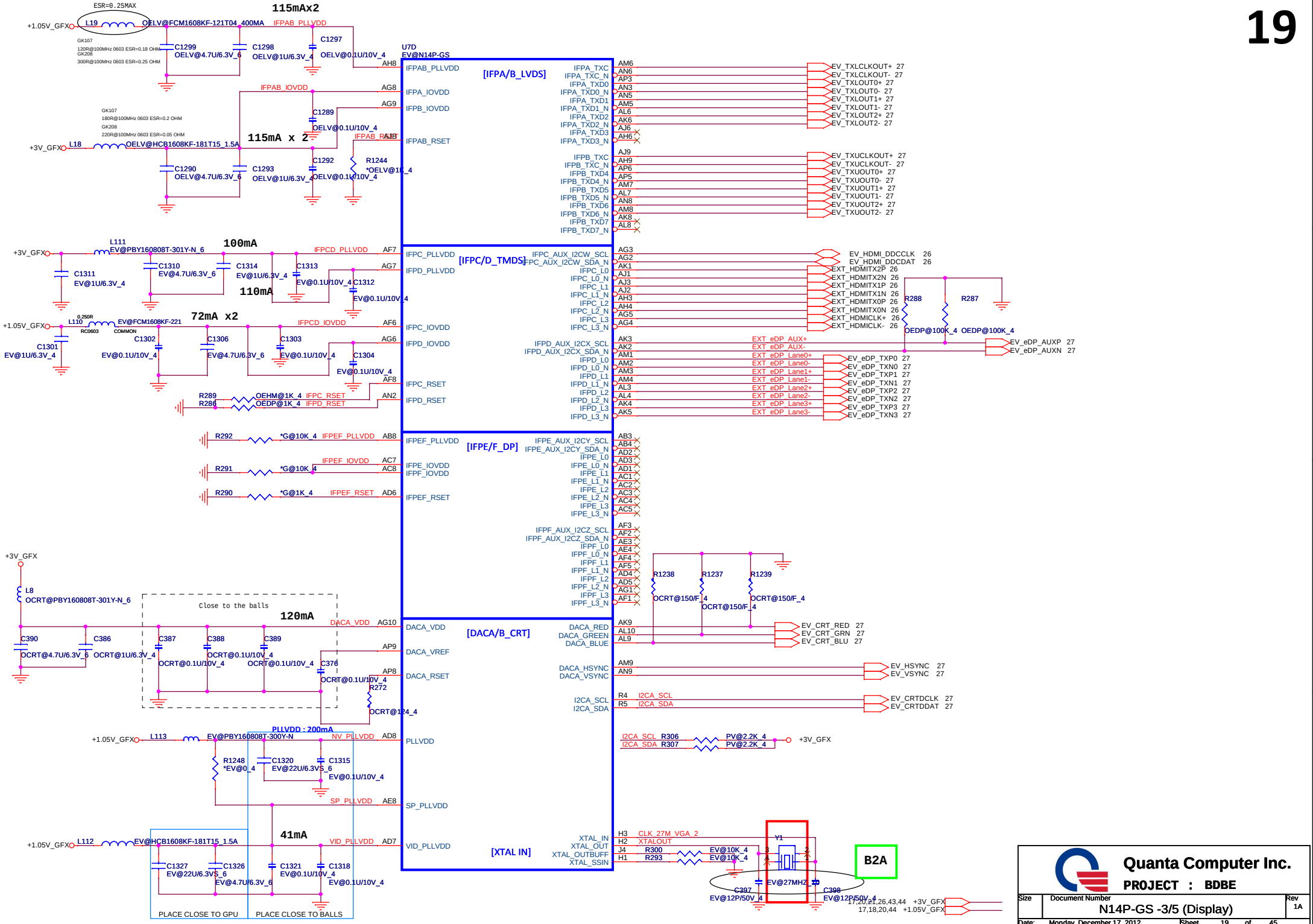

Quanta Computer Inc.
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Size	Document Number	Rev
	N14P-GS -3/5 (Display)	1A
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GPU	VRAM Vendor	Type	F8VDD/ F8VDDQ	Config	VRAM P/N	Max Speed CLK	D/C Mini	RAM_CFG	ROM_SI
N14M-GS/N14M-LP/N14P-GV2 N14P-GS/N14P-LP/N14P-GE	Samsung	DDR3	1.5 V/ 1.5 V	128Mx16	K4W2G1646E-BC1A	1000Mhz	1204	0x7	PD 45K
					K4W2G1646E-BC11	900Mhz			
	Micro	DDR3	1.5 V/ 1.5 V	128Mx16	MT41J128M16JT-093:G:K	1000Mhz	1105	0x5	PD 30K
					MT41J128M16JT-107:G:K	900Mhz			
	Hynix	DDR3	1.5 V/ 1.5 V	128Mx16	H5TQ2G63DFR-N0C	1000Mhz	NA	0x6	PD 35K
					H5TQ2G63DFR-11C	900Mhz			
	Samsung	DDR3	1.5 V/ 1.5 V	256Mx16	K4W4G1646B-HC11	900Mhz	NA	0x3	PD 20K
	Micro	DDR3	1.5 V/ 1.5 V	256Mx16	MT41K256M16HA-107:G:E	900Mhz	NA	0x1	PD 10K
	Samsung	DDR3L	1.35V/ 1.35V	128Mx16	K4W2G1646E-BY11	900Mhz	NA	0xA	PU 15K
	Micro	DDR3L	1.35V/ 1.35V	128Mx16	MT41K128M16JT-107:G:K	900Mhz	NA	0x8	PU 5K

Note:

Need change the VRAM strap if used other die VRAM which not include by attached RVL

VRAM (DDR3L / 900MHz) Configuration Table ROM_SI	
2G Samsung 128Mx16	15K PU
2G Micron 128Mx16	5K PU

Default: SAM 2G VRAM

VRAM (DDR3 / 1000MHz) Configuration Table ROM_SI	
2G Samsung 128Mx16	45.3K PD
2G Micron 128Mx16	30.1K PD
2G Hynix 128Mx16	35K PD
4G Samsung 256Mx16	20K PD
4G Micron 256Mx16	10K PD

N14P-GS ID:

Netname	N14P-GS
ROM_SO	OP 5K PU GS 10K PU
ROM_SCLK	15K PD
STRAP0	45K PD
STRAP1	5K PD
STRAP2	20K PD
STRAP3	GS:15K PD OP:5K PD
STRAP4	45K PD

4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)
10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
15K/F 4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)
34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +-1% (0402)
45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

Logical Strap Bit Mapping

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EH_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

GPIO ASSIGNMENTS

GPIO	Function
GPIO 0	Debug Service Header
GPIO 1	MEM_VDD_CTL/FAN_PWM
GPIO 2	LCD Brightness Control (BL PWM)
GPIO 3	LCD Power Enable (PPEN)
GPIO 4	LCD Backlight Enable (BLEN)
GPIO 5	NVVDD PWM_VID_BOOT_EN
GPIO 6	Remote Sensor Error Correction
GPIO 7	3D STEREO
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert/FAN_PWM
GPIO 10	FB Vref Control
GPIO 11	NVVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	NVVDD PSI
GPIO 14	FB_CLAMP_TGL_REG/HPD for IFP AB (not used)
GPIO 15	HPD for IFP C (DP)
GPIO 16	Fan PWM/MEM_VDD_CTL/NVVDD PSI/FRAME LOCK
GPIO 17	HPD for IFP D (eDP)
GPIO 18	HPD for IFP E (DP)
GPIO 19	HPD for IFP F (DP)
GPIO 20	<not used>
GPIO 21	<not used>

Add follow vendor advice 0913

GPU_PWROK

GFx SMBus Isolation

Quanta Computer Inc.
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Size | Document Number: N14P-GS - 4/5 (MISC) | Rev 1A
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VDD/XVDD : 25.72A

+VGPU_CORE

U7F
EV@N14P-GS

[GPU VDD]

AA12	VDD_001	XVDD_001	U1
AA14	VDD_002	XVDD_002	U2
AA16	VDD_003	XVDD_003	U3
AA19	VDD_004	XVDD_004	U4
AA21	VDD_005	XVDD_005	U5
AA23	VDD_006	XVDD_006	U6
AB13	VDD_007	XVDD_007	U7
AB15	VDD_008	XVDD_008	U8
AB17	VDD_009	XVDD_009	V1
AB18	VDD_010	XVDD_010	V2
AB20	VDD_011	XVDD_011	V3
AB22	VDD_012	XVDD_012	V4
AC12	VDD_013	XVDD_013	V5
AC14	VDD_014	XVDD_014	V6
AC16	VDD_015	XVDD_015	V7
AC19	VDD_016	XVDD_016	V8
AC21	VDD_017	XVDD_017	W2
AC23	VDD_018	XVDD_018	W3
M12	VDD_019	XVDD_019	W4
M14	VDD_020	XVDD_020	W5
M16	VDD_021	XVDD_021	W7
M19	VDD_022	XVDD_022	W8
M21	VDD_023	XVDD_023	Y1
M23	VDD_024	XVDD_024	Y2
N13	VDD_025	XVDD_025	Y3
N15	VDD_026	XVDD_026	Y4
N17	VDD_027	XVDD_027	Y5
N18	VDD_028	XVDD_028	Y6
N20	VDD_029	XVDD_029	Y7
N22	VDD_030	XVDD_030	Y8
P12	VDD_031	XVDD_031	AA1
P14	VDD_032	XVDD_032	AA2
P16	VDD_033	XVDD_033	AA3
P19	VDD_034	XVDD_034	AA4
P21	VDD_035	XVDD_035	AA5
P23	VDD_036	XVDD_036	AA6
R13	VDD_037	XVDD_037	AA7
R15	VDD_038	XVDD_038	AA8
R17	VDD_039		
R18	VDD_040		
R20	VDD_041		
R22	VDD_042		
T12	VDD_043		
T14	VDD_044		
T16	VDD_045		
T19	VDD_046		
T21	VDD_047		
T23	VDD_048		
U13	VDD_049		
U15	VDD_050		
U17	VDD_051		
U18	VDD_052		
U20	VDD_053		
U22	VDD_054		
V13	VDD_055		
V15	VDD_056		
V17	VDD_057		
V18	VDD_058		
V20	VDD_059		
V22	VDD_060		
W12	VDD_061		
W14	VDD_062		
W16	VDD_063		
W19	VDD_064		
W21	VDD_065		
W23	VDD_066		
Y13	VDD_067		
Y15	VDD_068		
Y18	VDD_069		
Y17	VDD_070		
Y20	VDD_071		
Y22	VDD_072		

U7G
EV@N14P-GS

[GPU GND]

A2	GND_1	GND_101	D2
AA17	GND_2	GND_102	D33
AA18	GND_3	GND_103	E10
AA20	GND_4	GND_104	E22
AA22	GND_5	GND_105	E25
AB12	GND_6	GND_106	E5
AB14	GND_7	GND_107	E7
AB16	GND_8	GND_108	F28
AB19	GND_9	GND_109	F7
AB2	GND_10	GND_110	G10
AB21	GND_11	GND_111	G13
A33	GND_12	GND_112	G16
AB23	GND_13	GND_113	G19
AB28	GND_14	GND_114	G2
AB30	GND_15	GND_115	G22
AB32	GND_16	GND_116	G25
AB5	GND_17	GND_117	G28
AB7	GND_18	GND_118	G3
AC13	GND_19	GND_119	G30
AC15	GND_20	GND_120	G32
AC17	GND_21	GND_121	G33
AC18	GND_22	GND_122	G5
AA13	GND_23	GND_123	G7
AC20	GND_24	GND_124	K2
AC22	GND_25	GND_125	K28
AE2	GND_26	GND_126	K30
AE28	GND_27	GND_127	K32
AE30	GND_28	GND_128	K33
AE32	GND_29	GND_129	K5
AE33	GND_30	GND_130	K7
AE5	GND_31	GND_131	M13
AE7	GND_32	GND_132	M15
AH10	GND_33	GND_133	M17
AA15	GND_34	GND_134	M18
AH13	GND_35	GND_135	M20
AH16	GND_36	GND_136	M22
AH19	GND_37	GND_137	N12
AH2	GND_38	GND_138	N14
AH22	GND_39	GND_139	N16
AH24	GND_40	GND_140	N19
AH28	GND_41	GND_141	N2
AH29	GND_42	GND_142	N21
AH30	GND_43	GND_143	N23
AH32	GND_44	GND_144	N28
AH33	GND_45	GND_145	N30
AH5	GND_46	GND_146	N32
AH7	GND_47	GND_147	N33
AJ7	GND_48	GND_148	N5
AK10	GND_49	GND_149	N7
AK7	GND_50	GND_150	P13
AL12	GND_51	GND_151	P15
AL14	GND_52	GND_152	P17
AL15	GND_53	GND_153	P18
AL17	GND_54	GND_154	P20
AL18	GND_55	GND_155	P22
AL2	GND_56	GND_156	R12
AL20	GND_57	GND_157	R14
AL21	GND_58	GND_158	R16
AL23	GND_59	GND_159	R19
AL24	GND_60	GND_160	R21
AL26	GND_61	GND_161	R23
AL28	GND_62	GND_162	T13
AL30	GND_63	GND_163	T15
AL32	GND_64	GND_164	T17
AL33	GND_65	GND_165	T18
AL5	GND_66	GND_166	T2
AM13	GND_67	GND_167	T20
AM16	GND_68	GND_168	T22
AM19	GND_69	GND_169	AG11
AM22	GND_70	GND_170	T28
AM25	GND_71	GND_171	T32
AN1	GND_72	GND_172	T5
AN10	GND_73	GND_173	T7
AN13	GND_74	GND_174	U12
AN16	GND_75	GND_175	U14
AN19	GND_76	GND_176	U16
AN22	GND_77	GND_177	U19
AN25	GND_78	GND_178	U21
AN30	GND_79	GND_179	U23
AN34	GND_80	GND_180	V12
AN4	GND_81	GND_181	V14
AN7	GND_82	GND_182	V16
AP2	GND_83	GND_183	V19
AP33	GND_84	GND_184	V21
B1	GND_85	GND_185	V23
B10	GND_86	GND_186	W13
B22	GND_87	GND_187	W15
B25	GND_88	GND_188	W17
B28	GND_89	GND_189	W18
B31	GND_90	GND_190	W20
B34	GND_91	GND_191	W22
B4	GND_92	GND_192	W28
B7	GND_93	GND_193	Y12
C10	GND_94	GND_194	Y14
C13	GND_95	GND_195	Y16
C19	GND_96	GND_196	Y19
C22	GND_97	GND_197	Y21
C25	GND_98	GND_198	Y23
C28	GND_99	GND_199	AH11
C7	GND_100	GND_200	
		GND_OPT_1	C16
		GND_OPT_2	W32

+VGPU_CORE

PLACE UNDER GPU

C1256	EV@1U/6.3V_4
C1257	EV@1U/6.3V_4
C1278	EV@1U/6.3V_4
C1230	EV@1U/6.3V_4
C1228	EV@1U/6.3V_4
C1274	EV@0.1U/10V_4
C1231	EV@0.1U/10V_4
C1233	EV@0.1U/10V_4
C1229	EV@0.1U/10V_4
C1246	EV@4.7U/6.3V_6
C1258	EV@4.7U/6.3V_6
C1259	EV@4.7U/6.3V_6
C1247	EV@4.7U/6.3V_6
C1285	EV@4.7U/6.3V_6
C1266	EV@4.7U/6.3V_6
C1235	EV@4.7U/6.3V_6
C1236	EV@4.7U/6.3V_6
C1240	EV@4.7U/6.3V_6
C1237	EV@4.7U/6.3V_6
C1239	EV@4.7U/6.3V_6
C1267	EV@4.7U/6.3V_6
C1268	EV@4.7U/6.3V_6
C1248	EV@4.7U/6.3V_6
C1265	EV@4.7U/6.3V_6

PLACE NEAR GPU

C1316	EV@4.7U/10V_6
C1328	EV@4.7U/10V_8
C401	EV@4.7U/10V_8
C403	EV@4.7U/10V_8
C1322	EV@4.7U/10V_8
C399	EV@22U/6.3VS_6
C1277	EV@47U/6.3V_6_S

C1252	EV@100U/6.3V_1206

PLACE TO GPU CENTER

for meet Power down sequence for +3V_GFX

+VGPU_CORE — D16 — EV@RB500V-40 — +3V_GFX

+1.5V_GFX — D17 — *EV@RB500V-40

B2A

120808 Del DGPU_PWROK circuit because all +1.05V_GFX/+1.5V_GFX power solution have PG connector to PCH

17,18,19,20,44	+VGACORE
18,20,22,23,36,44	+1.05V_GFX
17,19,20,26,43,44	+1.5V_GFX
3,7,8,9,10,11,13,14,15,16,20,24,26,27,28,30,31,33,34,35,36,38,42	+3V_GFX
	+3V

Quanta Computer Inc.

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	N14P-GS - 5/5 (Power)	1A

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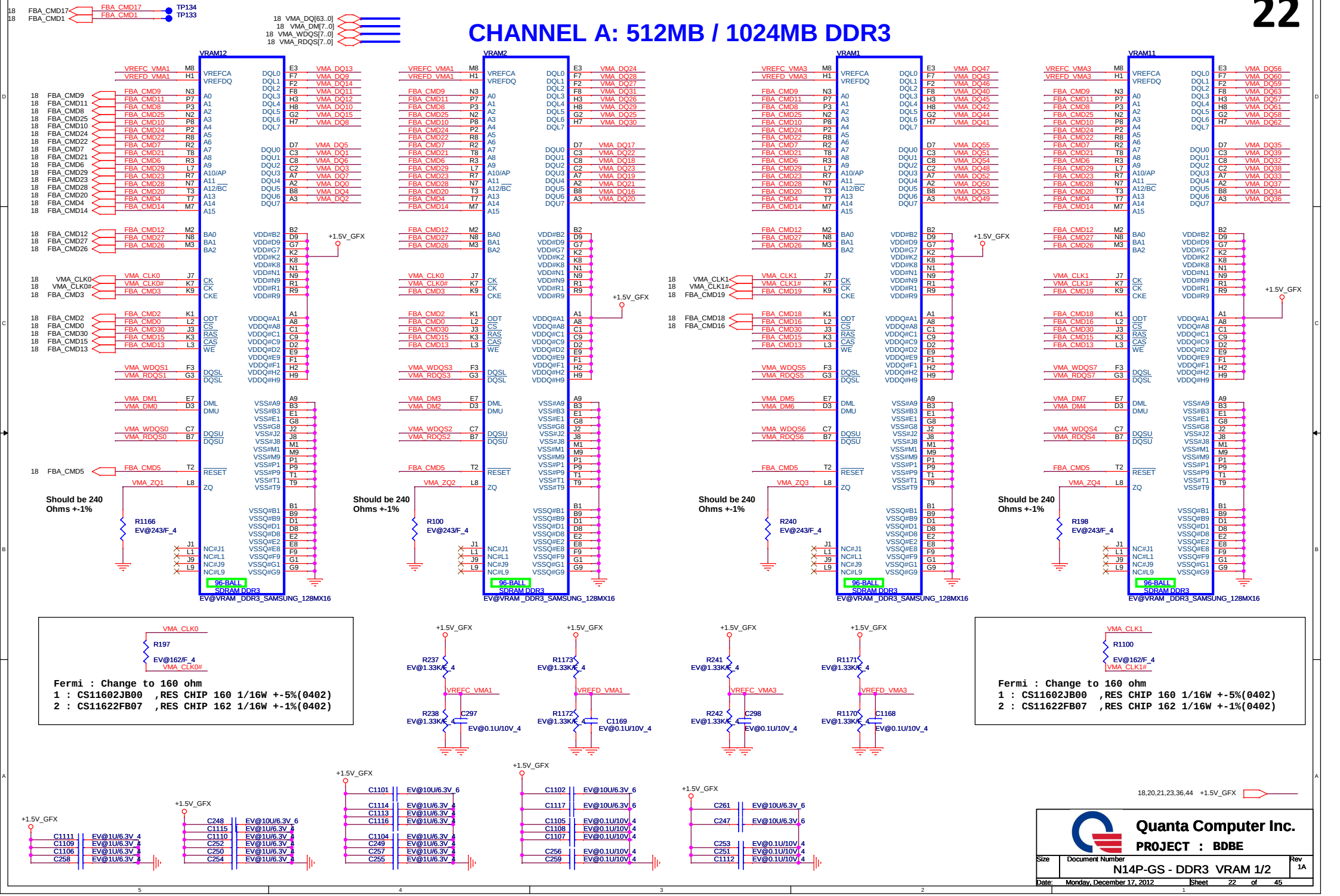
CHANNEL A: 512MB / 1024MB DDR3



Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	N14P-GS - DDR3 VRAM 1/2	1A
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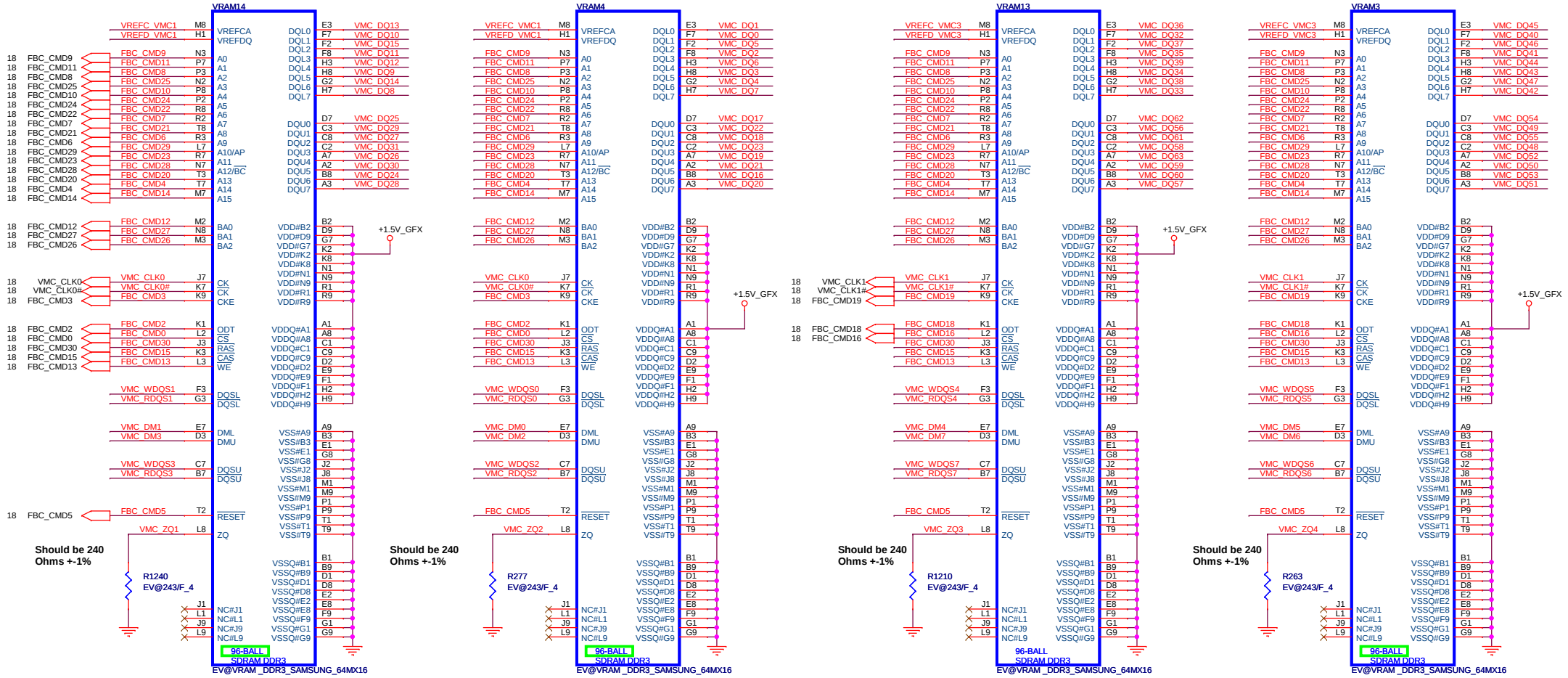
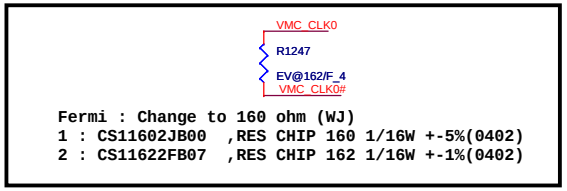
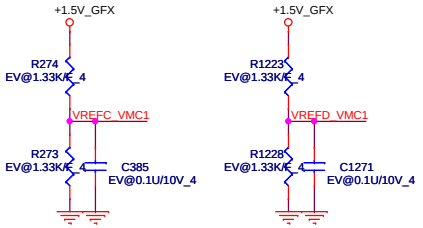
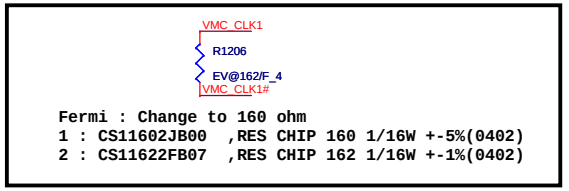
CHANNEL B: 256MB/512MB DDR3

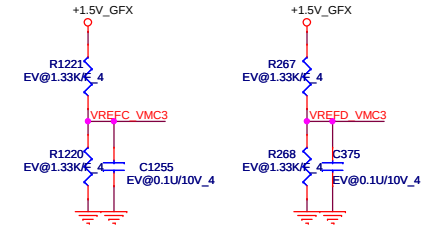
18 VMC_DQ[63..0]
18 VMC_DM[7..0]
18 VMC_WDQS[7..0]
18 VMC_RDQS[7..0]

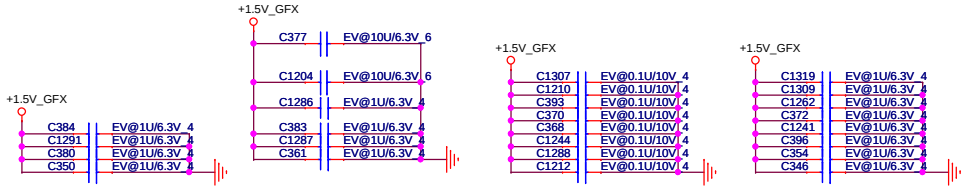












18 FBC_CMD17 — FBC_CMD17 — TP137
18 FBC_CMD1 — FBC_CMD1 — TP138

18,20,21,22,36,44 +1.5V_GFX

900MHz VRAM size:(WJ)
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

Quanta Computer Inc.
PROJECT : BDBE

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	N14P-GS - DDR3 VRAM 2/2	1A
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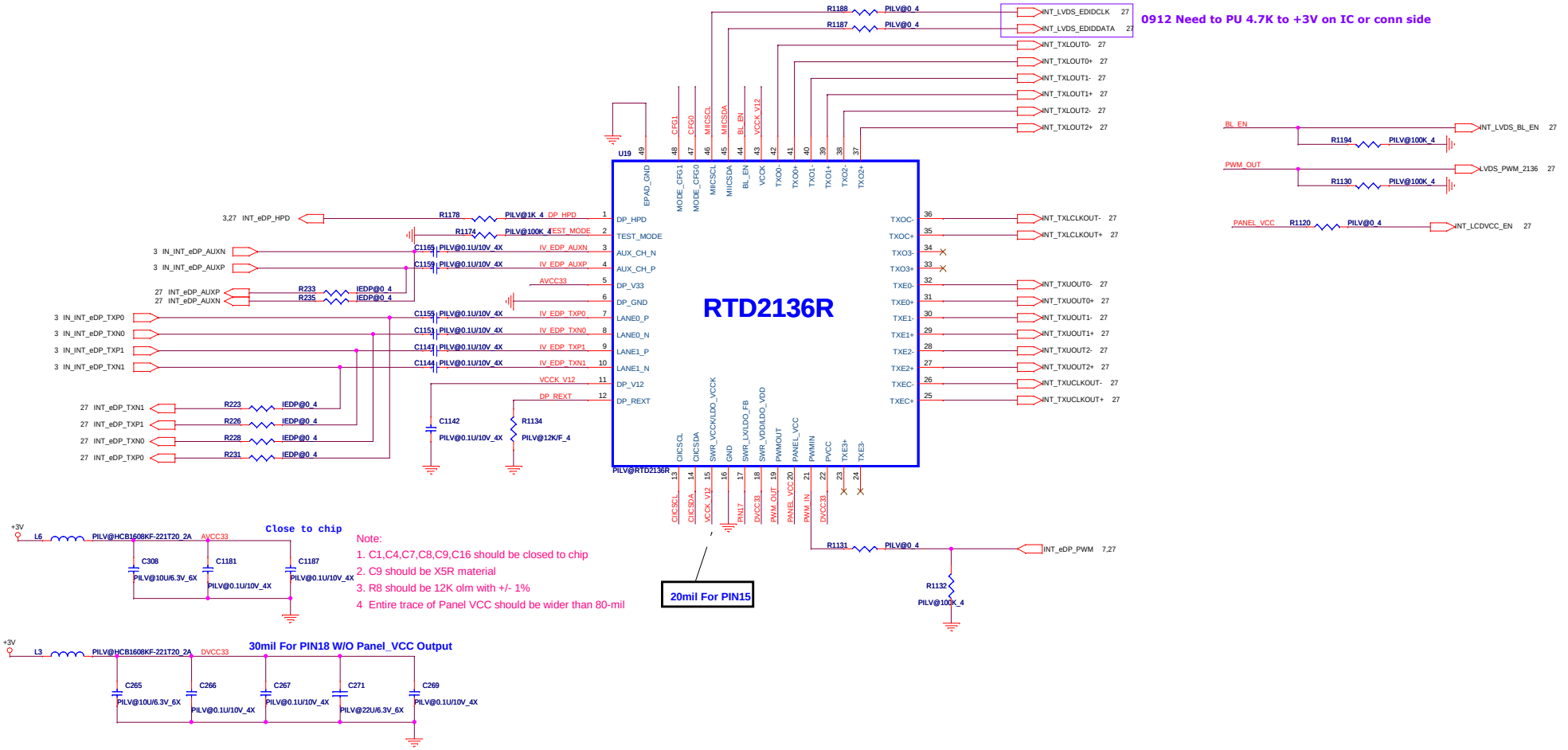
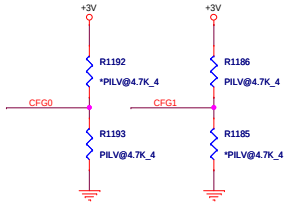


Note:
1. C1,C4,C7,C8,C9,C16 should be closed to chip
2. C9 should be X5R material
3. R8 should be 12K olm with +/- 1%
4 Entire trace of Panel VCC should be wider than 80-mil

Mode Configure Table(Power On Latch)

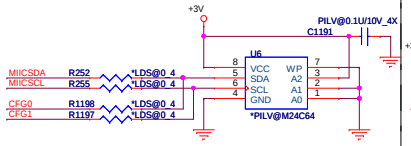
		CFG0	
		0	1
CFG1	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

ROM ONLY Mode : CFG0 4.7K pull low, CFG1 4.7K pull high
EP Mode : CFG0 4.7K pull high, CFG1 4.7K pull low
EEPROM Mode : CFG0 4.7K pull high, CFG1 4.7K pull high



EEPROM Mode
In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.

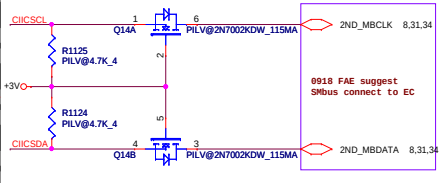
1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8



I2C address=0xA8

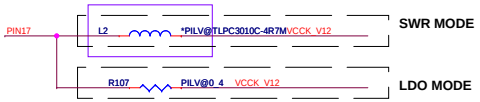
EP Mode
External device connect to DP2LVDS by Pin13/Pin14, I2C protocol is used

Address=0x94&0x6A

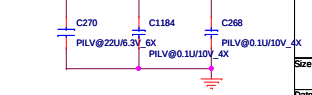


Dual Mode Regulator Configuration

	2.2-uH(L6)	0 Olm(R31)
SWR	Connect	NC
LDO	NC	Connect



1. C18 10-uF capacitor should be X5R material
2. Inductor should be withstand current >600-mA
3. Capacitors should be closed to PIN17



Quanta Computer Inc.
PROJECT : BDBE
Size | Document Number | Rev
Thames_M2/ Baco | 1A
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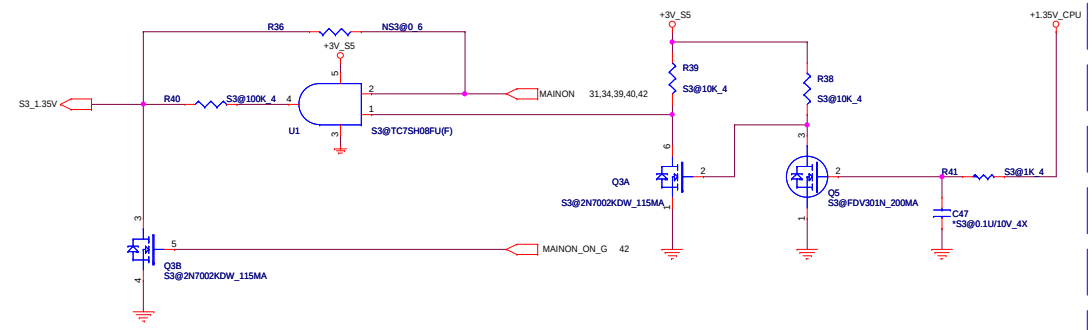
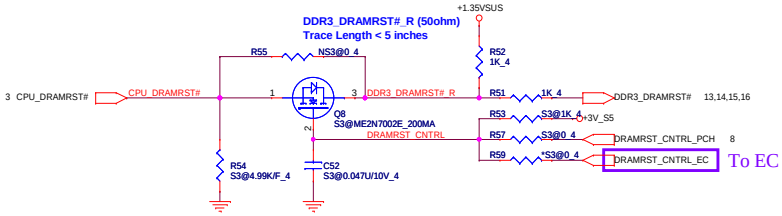
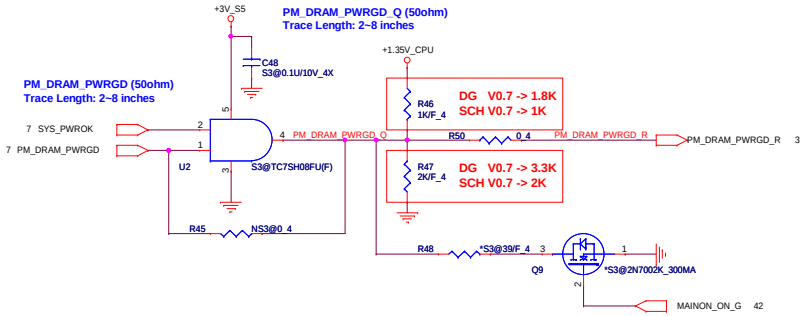
For S3 power Reduction Sequence S3P/NS3P/CPU



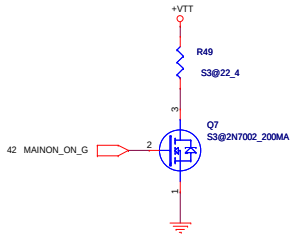
SM_DRAMRST# Topology S3P/NS3P/CPU



S3 power Reduction (SM_DRAMPWROK) S3P/NS3P/CPU

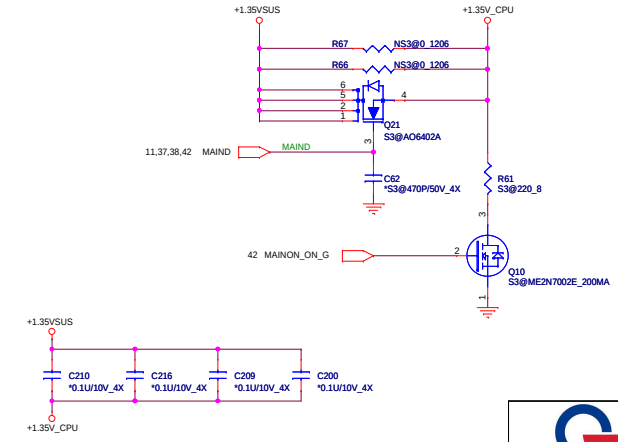


For S3 power Reduction VTT discharge S3P/NS3P/CPU



CPU SM_VREF S3P/NS3P/CPU

S3 power Reduction (CPU Power) S3P/NS3P/CPU



Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	1A
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HDMI Conn <HDM>

Close

from PCH / from NV

IV_HDMITX2	C277	PIHM@0.1U/10V_4X	HDMITX2_C_R		
IV_HDMITX2#	C280	PIHM@0.1U/10V_4X	HDMITX2#_C_R		
EXT_HDMITX2P	C1143	OEHM@0.1U/10V_4X			
EXT_HDMITX2N	C1145	OEHM@0.1U/10V_4X			
IV_HDMITX1	C290	PIHM@0.1U/10V_4X	HDMITX1_C_R		
IV_HDMITX1#	C291	PIHM@0.1U/10V_4X	HDMITX1#_C_R		
EXT_HDMITX1P	C1148	OEHM@0.1U/10V_4X			
EXT_HDMITX1N	C1152	OEHM@0.1U/10V_4X			
IV_HDMITX0	C292	PIHM@0.1U/10V_4X	HDMITX0_C_R		
IV_HDMITX0#	C293	PIHM@0.1U/10V_4X	HDMITX0#_C_R		
EXT_HDMITX0P	C1156	OEHM@0.1U/10V_4X			
EXT_HDMITX0N	C1164	OEHM@0.1U/10V_4X			
IV_HDMICLK	C295	PIHM@0.1U/10V_4X	HDMICLK_C_R		
IV_HDMICLK#	C299	PIHM@0.1U/10V_4X	HDMICLK#_C_R		
EXT_HDMICLK+	C1166	OEHM@0.1U/10V_4X			
EXT_HDMICLK-	C1170	OEHM@0.1U/10V_4X			

Change to correct diode (BC000220Z01)

+5V — R1203 0_6 — +DDC5V_F — F12 *SMD1206P110TFT — +DDC5V — D14 *B220LFA-13-F — +5V_HDMI

U111 HM@AP2331SA-7 (IN, OUT, GND) — C1214 HM@0.1U/16V_4Y — D15 *HM@AZ5125-01J — C1227 *HM@220P/50V_4X — C1207 HM@0.1U/16V_4Y

0.055A

Change 11/27

CN20 2HE1638-000111F

HDMITX2_R	1	D2+	SHELL1 20
HDMITX2#_R	2	D2 Shield	
HDMITX1_R	3	D2-	
	4	D1+	
HDMITX1#_R	5	D1 Shield	
HDMITX0_R	6	D1-	
	7	D0+	
HDMITX0#_R	8	D0 Shield	
HDMICLK_R	9	D0-	GND 23
	10	CK+	
HDMICLK#_R	11	CK Shield	GND 22
	12	CK-	
	13	CE Remote	
HDMI_CON_DDCCLK	14	NC	
HDMI_CON_DDCDATA	15	DDC CLK	
	16	DDC DATA	
	17	GND	
HDMI_CON_HP	18	+5V	
	19	HP DET	SHELL2 21

C1234 0.1U/16V_4Y

HDMI-passive level shift <HMP/HMG>

+3V — R1129 *HM@0_6 — +5V — R1136 *short_6 — Q15 N4K@2N7002K_300MA — R1123 N4K@100K_4

HDMITX0#_R1 / HDMITX0_R1	R1164	PIHM N4K@680_4	HDMITX0#_C_R_PAS / HDMITX0_C_R_PAS	
	R1160	PIHM N4K@680_R		
	R1163	OEHM N4K@499/F_4		
	R1161	OEHM N4K@499/F_4		
HDMITX1#_R1 / HDMITX1_R1	R1156	PIHM N4K@680_4	HDMITX1#_C_R_PAS / HDMITX1_C_R_PAS	
	R1153	PIHM N4K@680_R		
	R1157	OEHM N4K@499/F_4		
	R1152	OEHM N4K@499/F_4		
HDMITX2#_R1 / HDMITX2_R1	R1146	PIHM N4K@680_4	HDMITX2#_C_R_PAS / HDMITX2_C_R_PAS	
	R1141	PIHM N4K@680_R		
	R1147	OEHM N4K@499/F_4		
	R1140	OEHM N4K@499/F_4		
HDMICLK#_R1 / HDMICLK_R1	R1176	PIHM N4K@680_4	HDMICLK#_C_R_PAS / HDMICLK_C_R_PAS	
	R1167	PIHM N4K@680_R		
	R1175	OEHM N4K@499/F_4		
	R1168	OEHM N4K@499/F_4		

HDMI-HPD <HMP/HMG>

+3V — R1217 N4K@1M_4 — Q112 N4K@2N7002K_300MA

7 HDMI_CON_HP_PCH — R1215 PIHM@0_4 — HDMI_CON_HP_PCH_R — HDMI_CON_HP — R1211 PIHM_N4K@20K_4 — R1212 OEHM_N4K@100K_4

20 EXT_HDMI_HPD — R1214 OEHM@0_4

FOR EMI <EMC>

HDMITX2_R	R256 OEHM@120/F_4	HDMITX1_R	R260 OEHM@120/F_4
HDMITX2#_R		HDMITX1#_R	
HDMITX0_R	R265 OEHM@120/F_4	HDMICLK_R	R262 OEHM@120/F_4
HDMITX0#_R		HDMICLK#_R	

HDMI-SMBus <HDM>

+3V — R1205 PIHM@0_4 — +3V_HDMI

+3V_GFX — R1204 OEHM@0_4

+3V_HDMI, +5V — D12 RB500V-40_100MA — R1199 N4K@2.2K_4 — R1201 2.2K_4

7 HDMI_DDCCLK — HDMI_DDCCLK — R1196 PIHM@0_4 — HDMI_DDCCLK_ACT — Q110 N4K@FDV301N_200MA — HDMI_CON_DDCCLK

19 EV_HDMI_DDCCLK — EV_HDMI_DDCCLK — R253 OEHM@0_4

+3V_HDMI, +5V — D13 RB500V-40_100MA — R1202 N4K@2.2K_4 — R1200 2.2K_4

7 HDMI_DDCDATA — HDMI_DDCDATA — R1195 PIHM@0_4 — HDMI_DDCDATA_ACT — Q111 N4K@FDV301N_200MA — HDMI_CON_DDCDATA

19 EV_HDMI_DDCDAT — EV_HDMI_DDCDAT — R254 OEHM@0_4

Support 4K2K STUFF

U110 PIV4K@PS8401

HDMITX2_C_R	1	IN_D0+	OUT_D0+ 30 HDMITX2_R
HDMITX2#_C_R	2	IN_D0-	OUT_D0- 29 HDMITX2#_R
HDMITX1_C_R	4	IN_D1+	OUT_D1+ 27 HDMITX1_R
HDMITX1#_C_R	5	IN_D1-	OUT_D1- 26 HDMITX1#_R
HDMITX0_C_R	6	IN_D2+	OUT_D2+ 25 HDMITX0_R
HDMITX0#_C_R	7	IN_D2-	OUT_D2- 24 HDMITX0#_R
HDMICLK_C_R	9	IN_CLK+	OUT_CLK+ 22 HDMICLK_R
HDMICLK#_C_R	10	IN_CLK-	OUT_CLK- 21 HDMICLK#_R
HDMI_DDCCLK_ACT R1128	PIV4K@0_4	HDMI4K2K_SCL_SRC	38 SCL_SRC — SCL_SINK 32 HDMI_CON_DDCCLK
HDMI_DDCDATA_ACT R1127	PIV4K@0_4	HDMI4K2K_SDA_SRC	39 SDA_SRC — SDA_SINK 33 HDMI_CON_DDCDATA
HDMI_CON_HP_PCH_R	R220 PIV4K@0_4	HDMI_CON_HP_PCH_ACT	3 HPD_SRC — HPD_SINK 28 HDMI_CON_HP
+3V	R244 *PIV4K@4.7K_4		36 PD# — VCC33[1] 11 +3V
	HDMI4K2K_PRE		16 I2C_STL_EN — VCC33[2] 37 R1125 8401@0_4
	HDMI4K2K_ISET R208 8401@0_4		34 PRE — +1.5V
	HDMI4K2K_DDCBUF		14 ISET — VCCTX15[1] 20
	HDMI4K2K_EN		13 DDCBUF/SDA_CTL — VCCTX15[2] 31
	HDMI4K2K_EQ		17 DCIN_EN/SCL_STL — VCCRX15[1] 12 R1130 8401@0_4 460mA (30mils)
	HDMI4K2K_CFG		23 EQ/I2C_ADDR0 — VCCRX15[2] 40
R1183 PIV4K@4.99K/F_4			18 CFG/I2C_ADDR1 — VCCTA15[1] 19
			REXT — GND[1] 15 R247 8401@0_4
			GND[2] 35
			PAD(GND1) 41
			PAD(GND2) 42
			PAD(GND3) 43
			PAD(GND4) 44
			PAD(GND5) 45
			PAD(GND6) 46
			PAD(GND7) 47
			PAD(GND8) 48
			PAD(GND9) 49
			PAD(GND10) 50

Add 0ohms for compatible with PS8201A.
R2586 for NC.20121112

Close U2501

HDMITX0_C_R	R232	N4K@0_4	HDMITX0_C_R_PAS	R1162	N4K@0_4	HDMITX0_R	
HDMITX0#_C_R	R234	N4K@0_4	HDMITX0#_C_R_PAS	R1165	N4K@0_4	HDMITX0#_R	
HDMITX1_C_R	R227	N4K@0_4	HDMITX1_C_R_PAS	R1155	N4K@0_4	HDMITX1_R	
HDMITX1#_C_R	R229	N4K@0_4	HDMITX1#_C_R_PAS	R1158	N4K@0_4	HDMITX1#_R	
HDMITX2_C_R	R221	N4K@0_4	HDMITX2_C_R_PAS	R1142	N4K@0_4	HDMITX2_R	
HDMITX2#_C_R	R224	N4K@0_4	HDMITX2#_C_R_PAS	R1148	N4K@0_4	HDMITX2#_R	
HDMICLK_C_R	R236	N4K@0_4	HDMICLK_C_R_PAS	R1169	N4K@0_4	HDMICLK_R	
HDMICLK#_C_R	R243	N4K@0_4	HDMICLK#_C_R_PAS	R1177	N4K@0_4	HDMICLK#_R	

Close U2501

+3V — C1179 PIV4K@0.1U/10V_4X — C1180 PIV4K@0.01U/25V_4X

+1.5V — C1175 PIV4K@0.1U/10V_4X — C1135 PIV4K@0.1U/10V_4X — C1137 PIV4K@0.1U/10V_4X — C1138 PIV4K@0.1U/10V_4X — C1136 PIV4K@0.01U/25V_4X — C1185 PIV4K@0.01U/25V_4X

+3V — R250 *PIV4K@4.7K_4 — R210 *PIV4K@4.7K_4 — R1181 *PIV4K@4.7K_4 — R230 *PIV4K@4.7K_4 — R248 PIV4K@4.7K_4 — R245 *PIV4K@4.7K_4

HDMI4K2K_PRE
HDMI4K2K_ISET
HDMI4K2K_EQ
HDMI4K2K_CFG
HDMI4K2K_DDCBUF
HDMI4K2K_EN

R249 *PIV4K@4.7K_4 — R209 *PIV4K@4.7K_4 — R1182 *PIV4K@4.7K_4 — R246 *PIV4K@4.7K_4

	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC(Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default,AC coupling input
1(High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A

Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

Quanta Computer Inc.
PROJECT : BDBE
Size: — Document Number: HDMI CONN/CEC — Rev: 1A
Date: Monday, December 17, 2012 — Sheet 26 of 45

Panel backlight control LDS

3D Emitter

IR Module CONN

Change 1205 B2A

LCD POWER SWITCH

INT_LVDS PWR

80 mil

HALL Sensor HSR

TOUCH PANEL

Change 1205 B2A

CRT CRT/CRU/CRV

LCD Panel Module <LDS>

Lane 3

Lane 2

Lane 1

Lane 0

EDID DDC

CCD CCD

Change 20121204 B2A

Need change PN FT 28121812

Panel CNT

INT EDP 85ohm

EXT EDP 90ohm

INT EDP 85ohm

EXT LVDS 90ohm

RTS2136R

87ohm

90ohm

R1,C1 need to close Panel CNT

Stuff R1 for LVDS interface

Stuff C1 for EDP interface.

Quanta Computer Inc.

PROJECT : BDBE

Size: Document Number: LCD/LED Panel/CCD Rev: 1A

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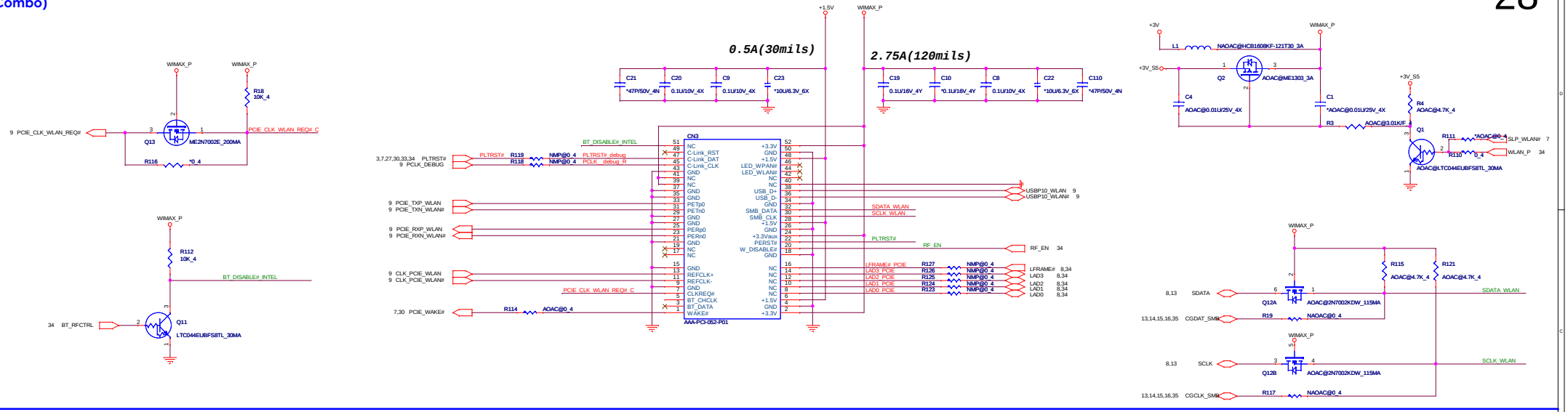
MINI Card Slot#1(WiFi / Wimax / Combo)

MNW/DEG

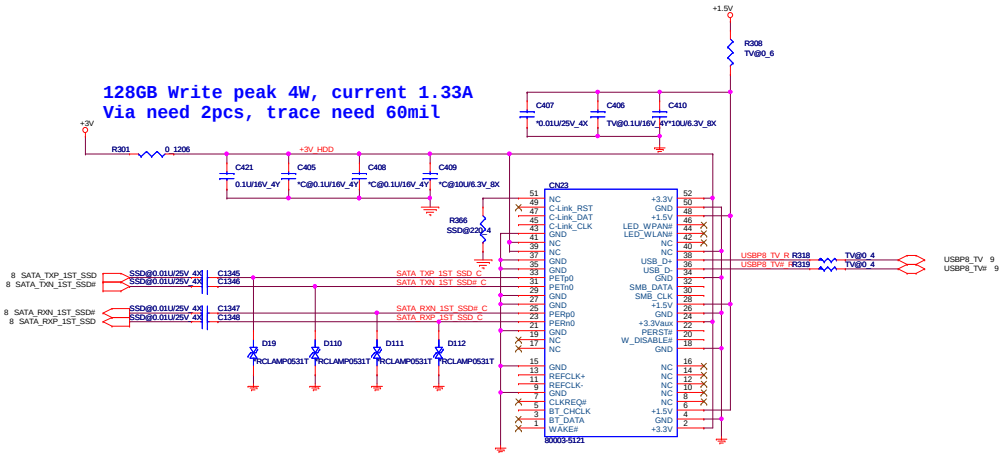


TV Tuner / MSATA

<SSD>

TV Tuner: 1.5V@240mA 3.3V@470mA

128GB Write peak 4W, current 1.33A
Via need 2pcs, trace need 60mil



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PROJECT : BDBE			
Size	Document Number		Rev
	MINI CARD(WLAN/3G/SIM Card)		1A
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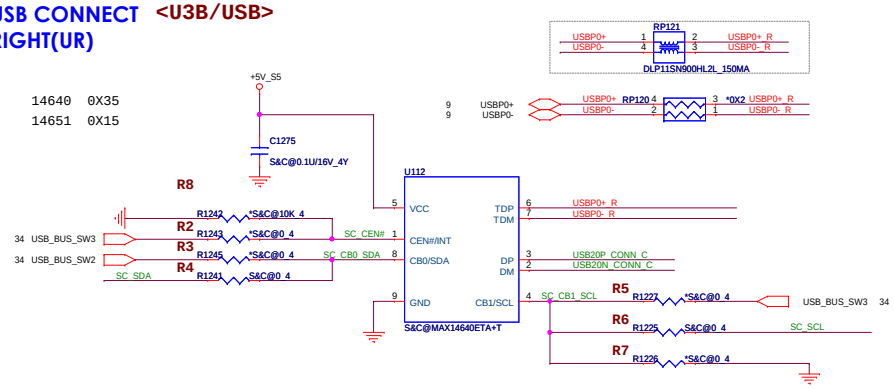
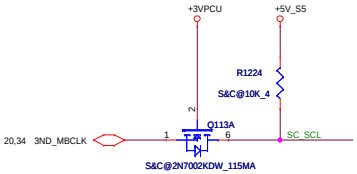
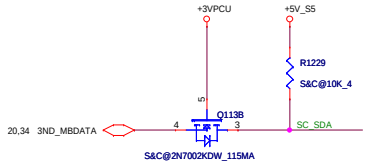
USB CONNECT RIGHT(UR) <U3B/USB>

14640 0X35
14651 0X15







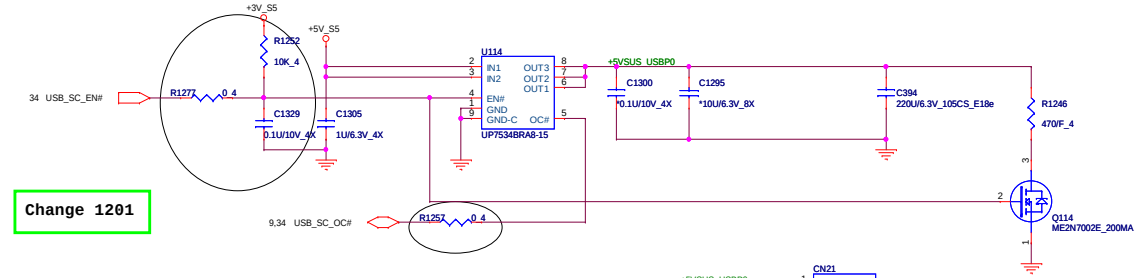
	R1	R2	R3	R4	R5	R6	R7	R8
14566		V	V				V	
14600			V		V			
14617(with CB2)	V		V		V			
14617(no CB2)			V		V			V
14641/42/44			V		V			
14640				V		V		

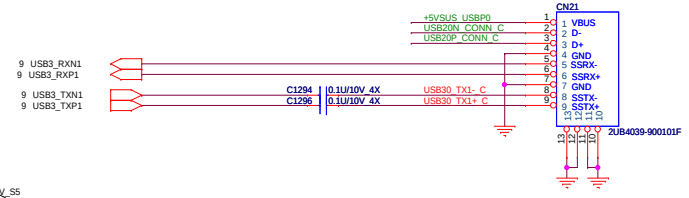
SW2	SW3	14600	
CB0	CB1	Status	
0	0	Auto mode	Charger / AM
0	1	Force dedicated charger mode	Charger / FM
1	0	Pass-Through(USB) mode	USB / PM
1	1	Pass-Through(USB) mode with CDP Emulation	USB / CM

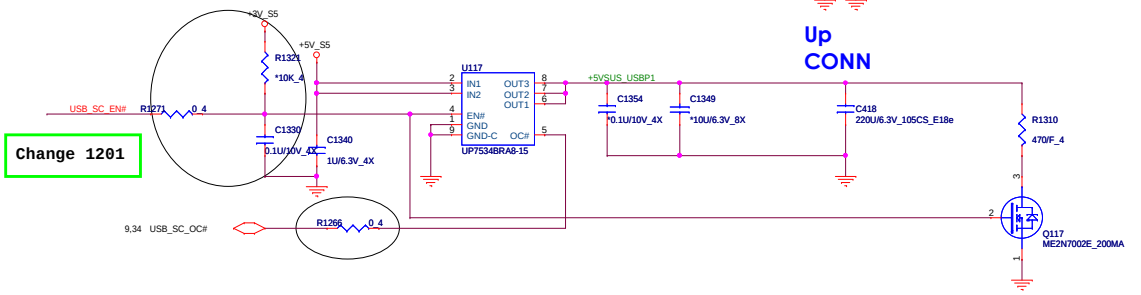
SW2	SW3	14644	
CB0	CB1	Status	
0	0	2A Auto mode for Apple Device	Charger / AM2
1	0	Force dedicated charger mode	Charger / FM
0	1	Pass-Through(USB) mode	USB / PM
1	1	Pass-Through(USB) mode with CDP Emulation	USB / CM

SW2	SW3	14641	
CB0	CB1	Status	
0	0	2A Auto mode for Apple Device	Charger / AM2
1	0	Force 1A for Apple Device	Charger / AP1
0	1	Pass-Through(USB) mode	USB / PM
1	1	Pass-Through(USB) mode with CDP Emulation	USB / CM

SW2	SW3	14642	
CB0	CB1	Status	
X	0	2A Auto mode for Apple Device	Charger / AM2
0	1	Pass-Through(USB) mode	USB / PM
1	1	Pass-Through(USB) mode with CDP Emulation	USB / CM

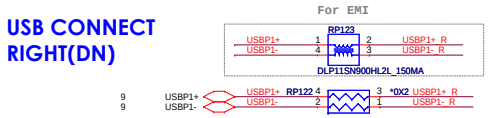


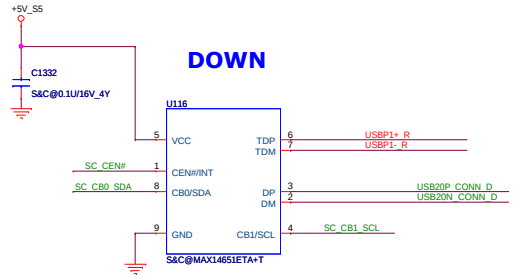


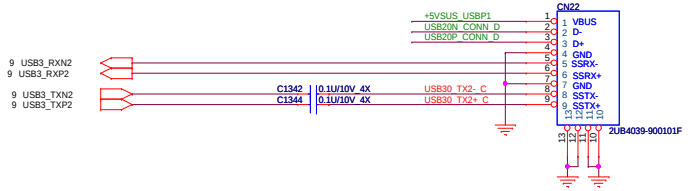


Up CONN

USB CONNECT RIGHT(DN)







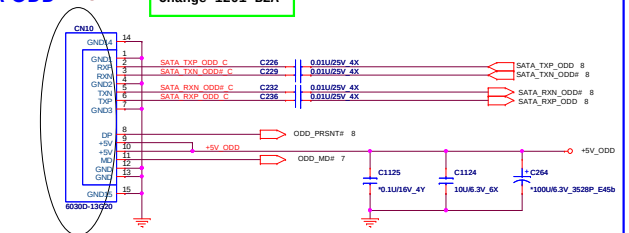
Down CONN

Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	USB3 Redriver/S&C(Right side)	1A
Date: Monday, December 17, 2012	Sheet 29 of 45	

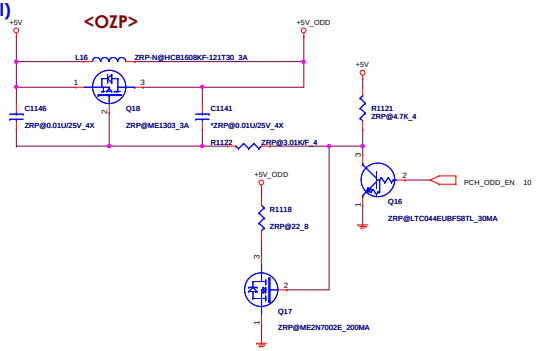
SATA ODD <ODD>

Change 1201 B2A



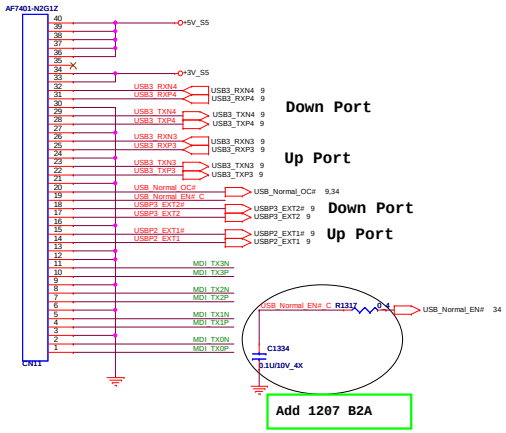
ODD Zero power .
(Only for Intel)

<OZP>



<LAN/LN1.LNG>

Atheros Lan/USB3 CONN



Down Port

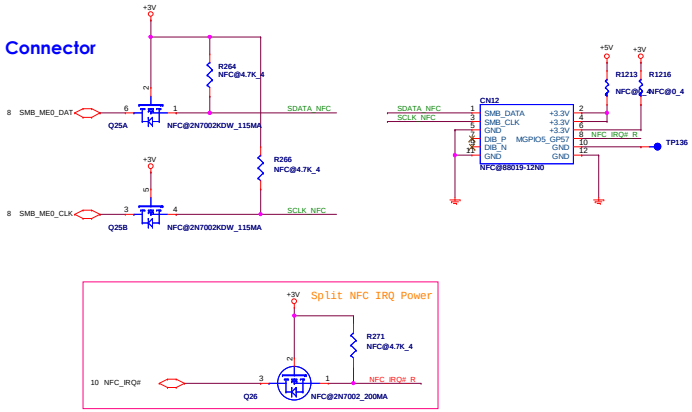
Up Port

Down Port

Up Port

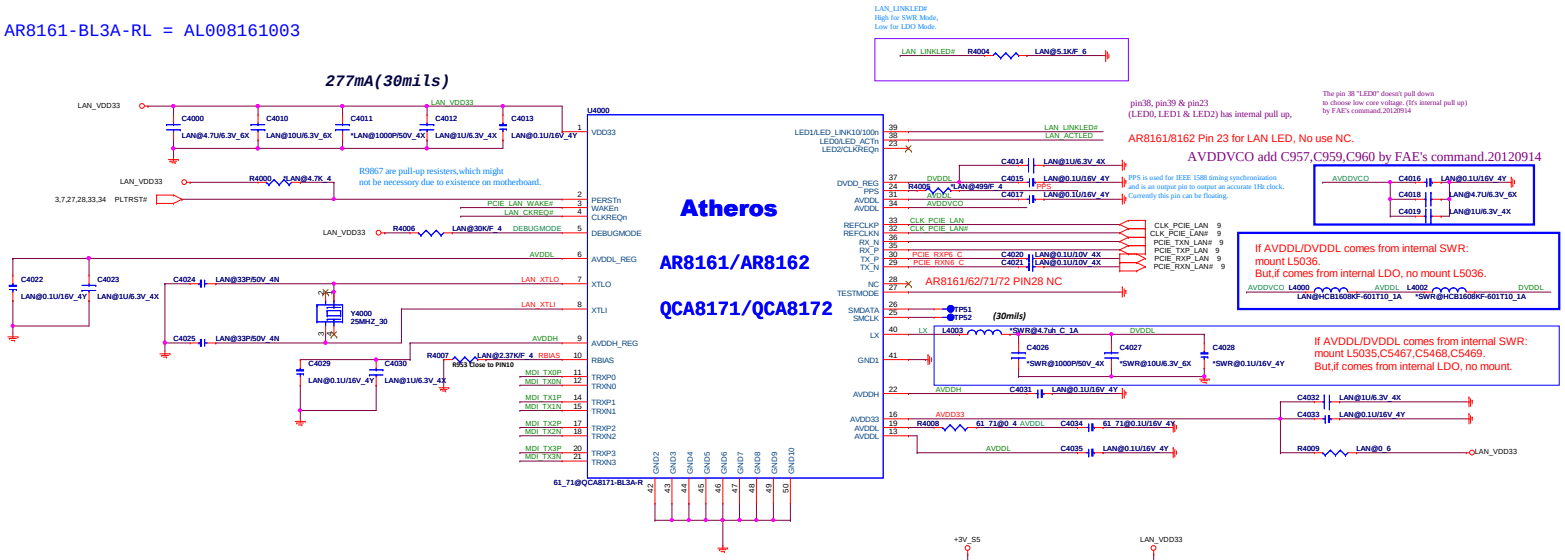
Add 1207 B2A

NFC Connector



AR8161-BL3A-RL = AL008161003

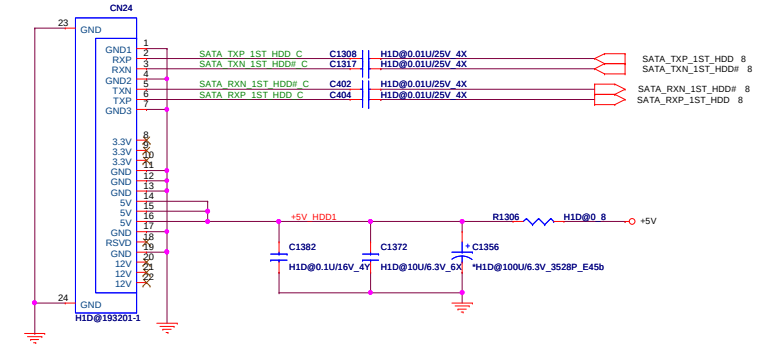
277mA(30mils)



Quanta Computer Inc.			
PROJECT : BDBE			
Size	Document Number		Rev
	USB3 Redriver/USB2_Left		1A
Date: Monday, December 17, 2012	Sheet 30 of 45		

SATA HDD1

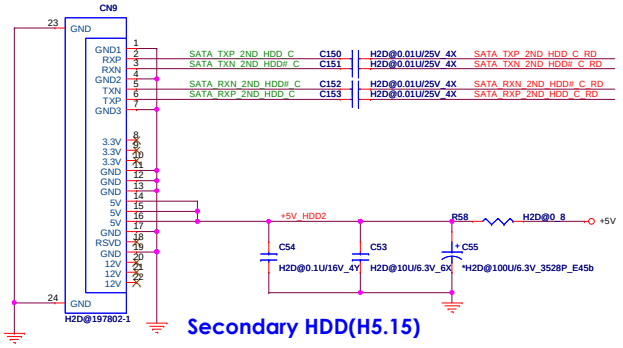
HDD1



Primary HDD(H2.75)

SATA HDD2

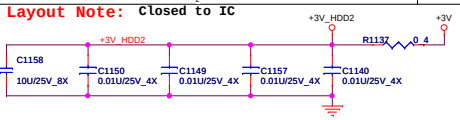
HDD2



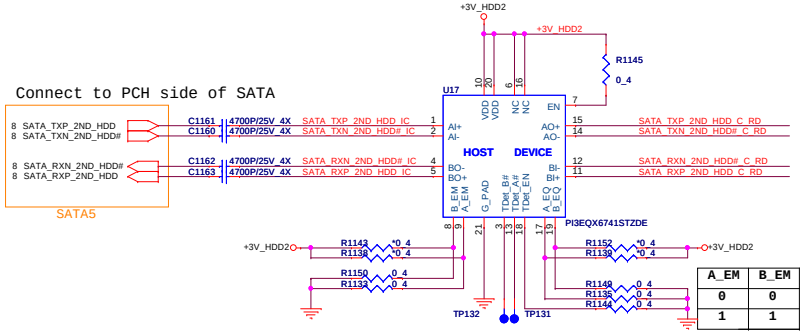
Secondary HDD(H5.15)

2nd HDD SATA Re-driver

Layout Note: Closed to IC



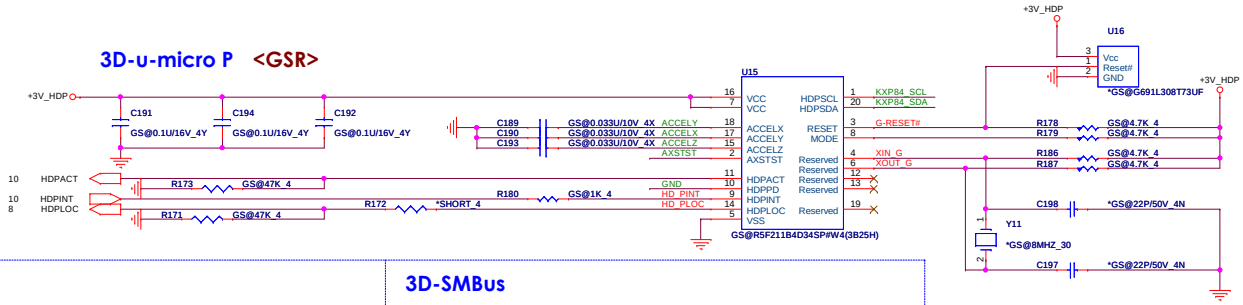
Connect to PCH side of SATA



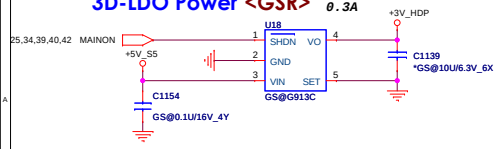
A_EQ	B_EQ	1.5 Gb/s	3 Gb/s	6 Gb/s
0	0	1 bB	2.5 bB	3 bB
1	1	4 bB	7.5 bB	9 bB
floating		2.5 bB	5 bB	6 bB

A_EM	B_EM	3 Gb/s	6 Gb/s
0	0	550mV pp	650mV pp
1	1	550mV pp+3dB Pre-emphasis	650mV pp+1.5dB Pre-emphasis

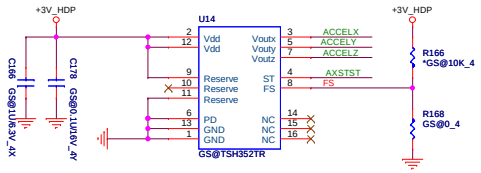
3D-u-micro P <GSR>



3D-LDO Power <GSR> 0.3A



3D-Sensor IC <GSR>



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

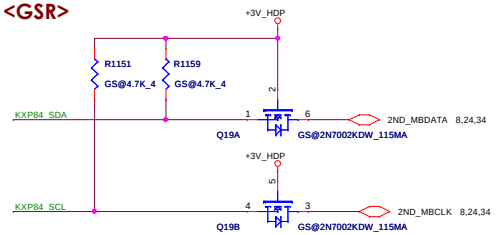
PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

HDPPD	0	1
	Normal Mode	Power-down mode

3D-SMBus <GSR>



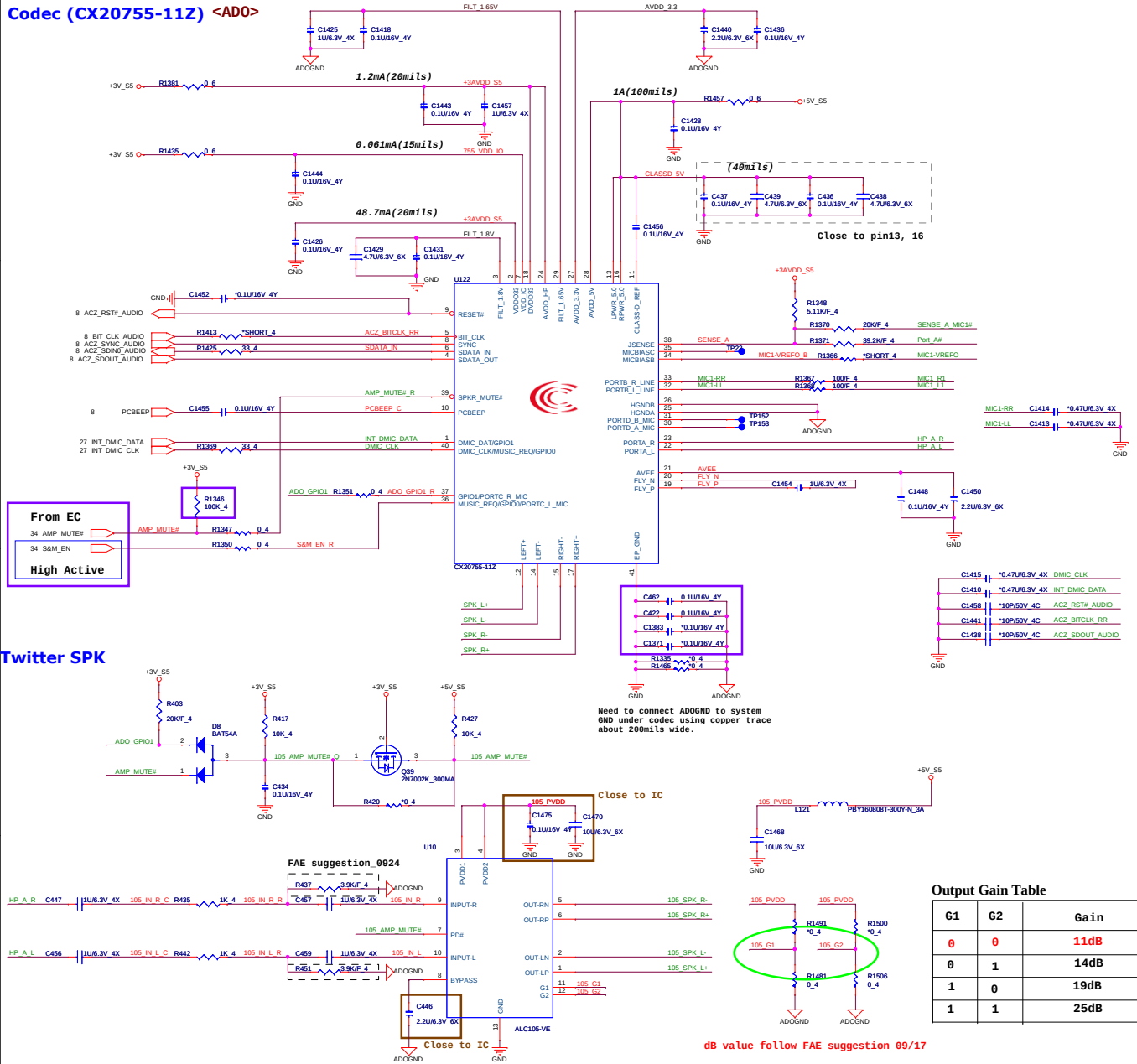
Quanta Computer Inc.

PROJECT : BDBE

Size	Document Number	Rev
	HDD/ODD	1A

Date: Monday, December 17, 2012 Sheet 31 of 45

Codec (CX20755-11Z) <ADO>



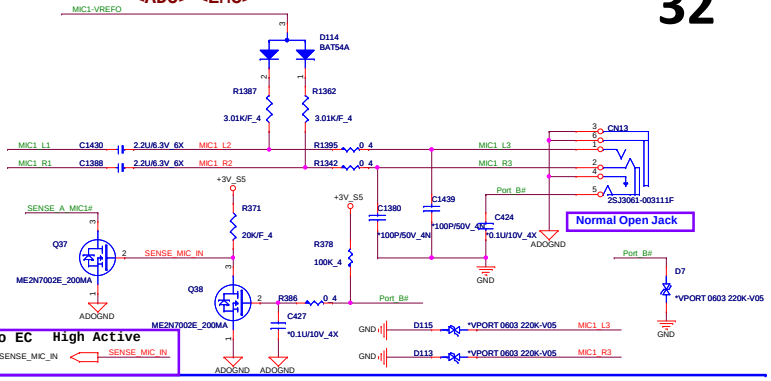
Twitter SPK

Output Gain Table

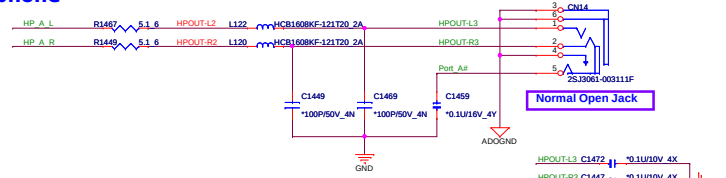
G1	G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

dB value follow FAE suggestion 09/17

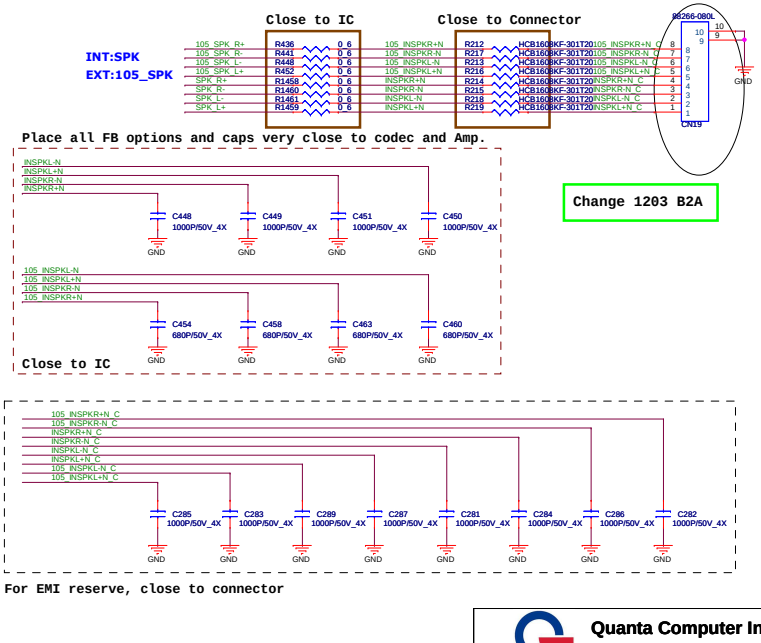
External MIC <ADO> <EMC>



Headphone <ADO>



4 Speakers <ADO>

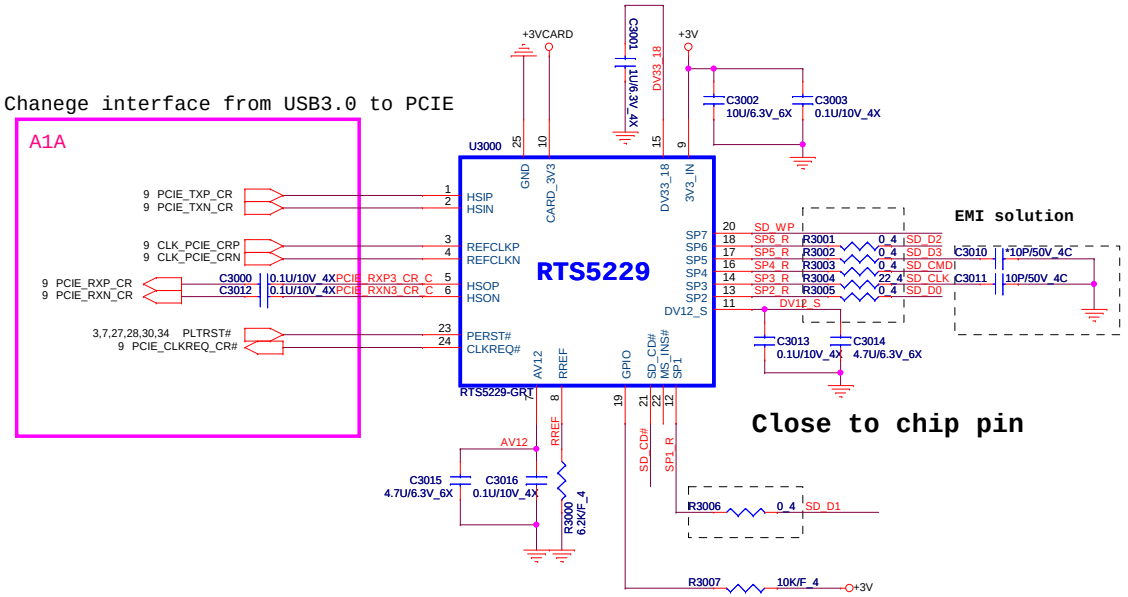


Quanta Computer Inc.
PROJECT : BDBE

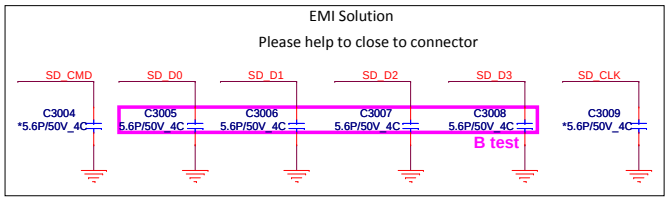
Size	Document Number	Rev
	Audio Codec (CX20755)	LA

Date: Monday, December 17, 2012 Sheet 32 of 45

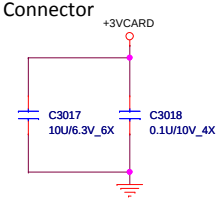
Card Reader (GL834L) <MMC>



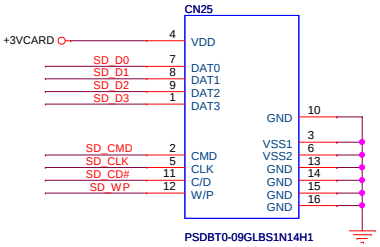
Share Pin



Place close to Connector



SD / MMC CARD READER



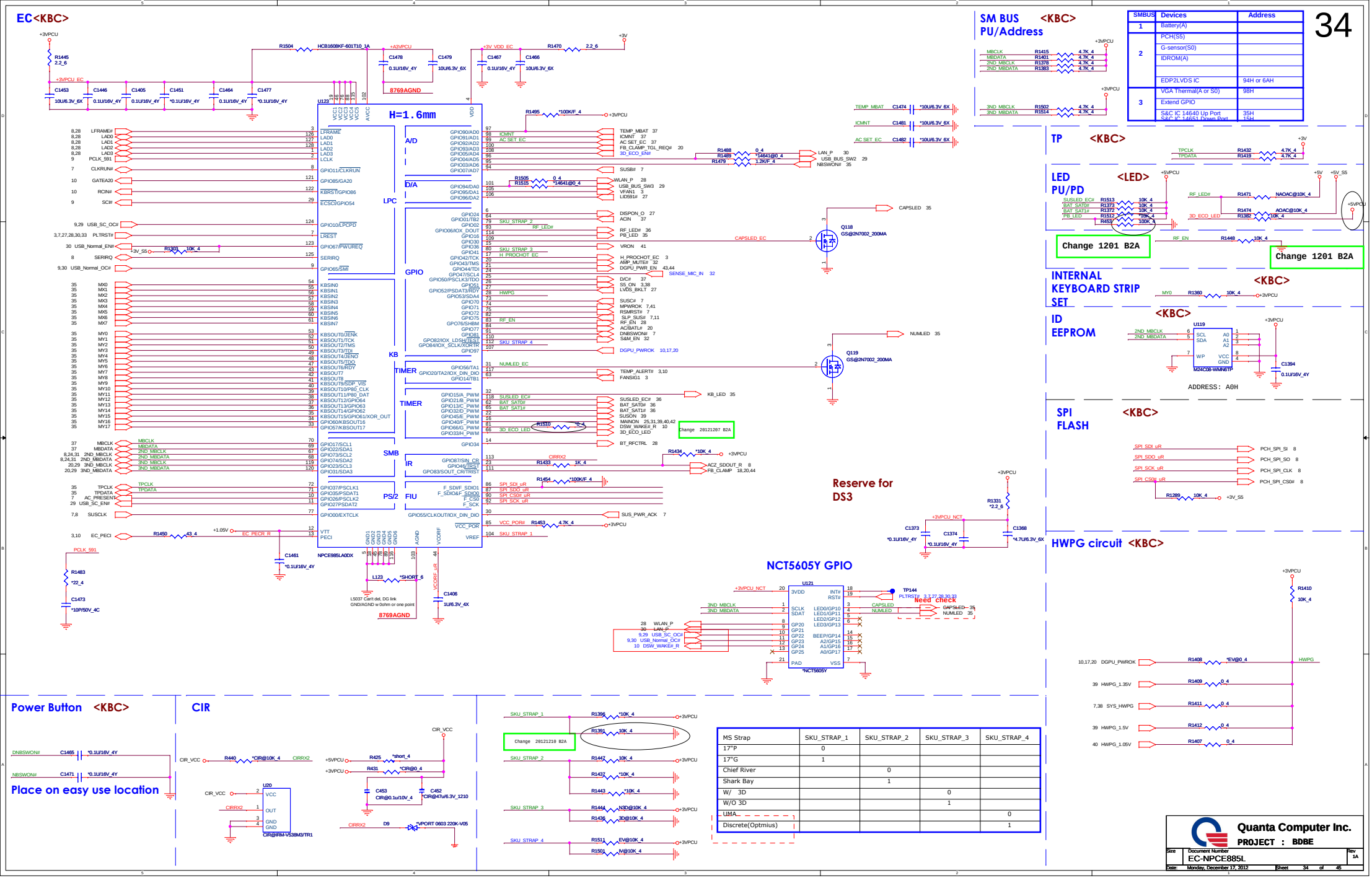
Quanta Computer Inc.

PROJECT : BDBE

Size	Document Number	Rev
	Card Reader(AU6437)	1A

Date: Monday, December 17, 2012 Sheet 33 of 45

EC<KBC>



SM BUS PU/Address <KBC>

SMBUS	Devices	Address
1	Battery(A)	
2	PCH(S5)	
	G-sensor(S0)	
	IDROM(A)	
	EDP2LVDS IC	94H or 6AH
3	VGA Thermal(A or S0)	98H
	Extend GPIO	
	S&C IC 14640 Up Port	35H
	S&C IC 14651 Down Port	15H

TP <KBC>

LED PU/PD <LED>

Change 1201 B2A

Change 1201 B2A

INTERNAL KEYBOARD STRIP SET <KBC>

ID EEPROM <KBC>

ADDRESS: A0H

SPI FLASH <KBC>

Reserve for DS3

HWPG circuit <KBC>

NCT5605Y GPIO

Power Button <KBC>

Place on easy use location

CIR

MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3	SKU_STRAP_4
17"P	0			
17"G	1			
Chief River		0		
Shark Bay		1		
W/ 3D			0	
W/O 3D			1	
UMA				0
Discrete(Optmius)				1

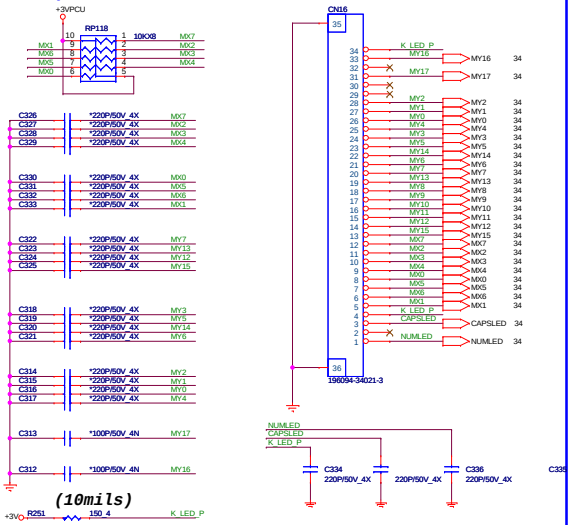
Quanta Computer Inc.

PROJECT : BDBE

Size	Document Number	Rev
	EC-NPCE885L	1A

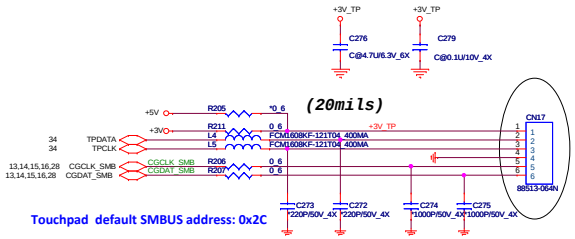
Date: Monday, December 17, 2012 Sheet 34 of 45

INT KeyBoard <KBC>



TP board <TPD>

Touch Pad Connector <TPD> <EMI>

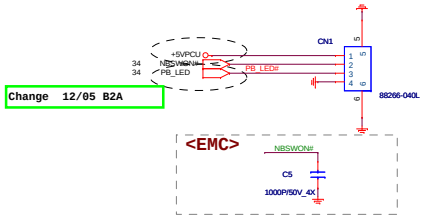


Touchpad default SMBUS address: 0x2C

Change 1201 B2A

Power board w LED <PSW>

Power Botton Connector <PSW>

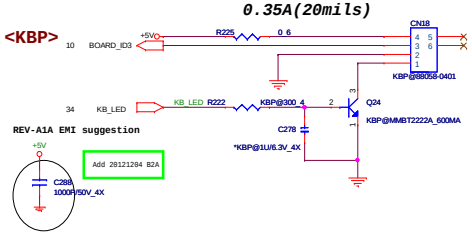


Change 12/05 B2A

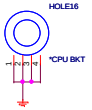
K/B LED power

0.35A(20mils)

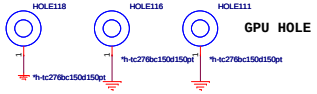
<KBP>



CPU BKT INTEL-CPU-BKT2



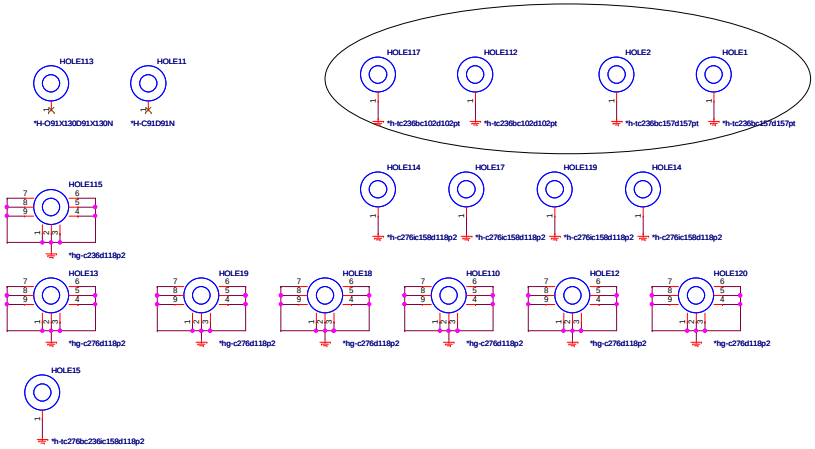
GPU



Control board w LED <PSW>

Del 1201 B2A

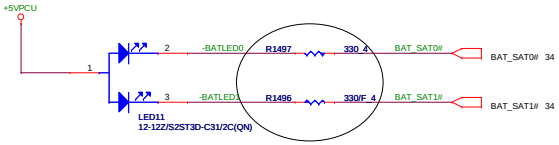
HOLE



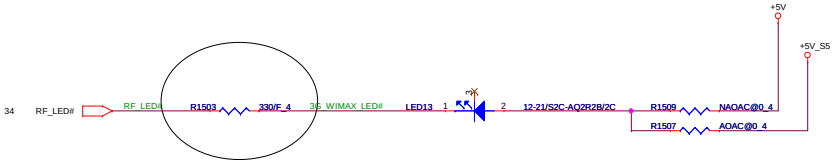
LED LED

BATERRY

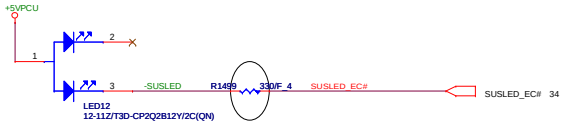
B2A



RF LED LED

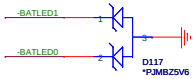


POWER LED

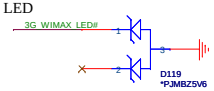


ESD Protect LED

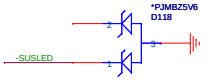
FOR BATTERY LED



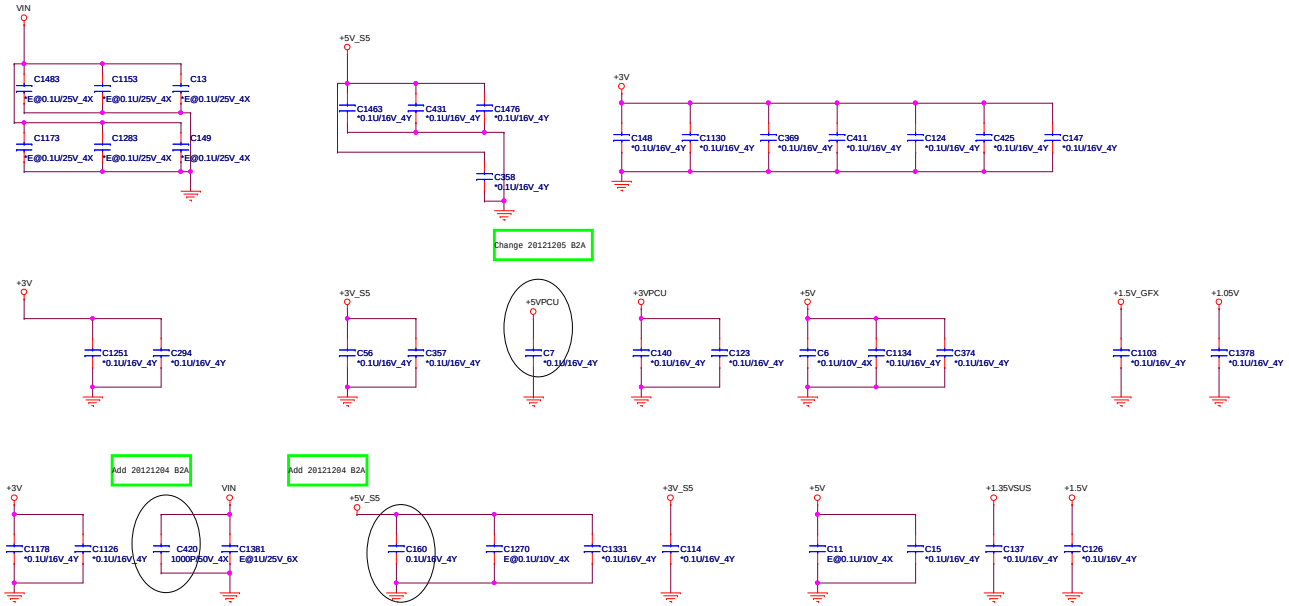
FOR W-LAN LED



FOR Power LED



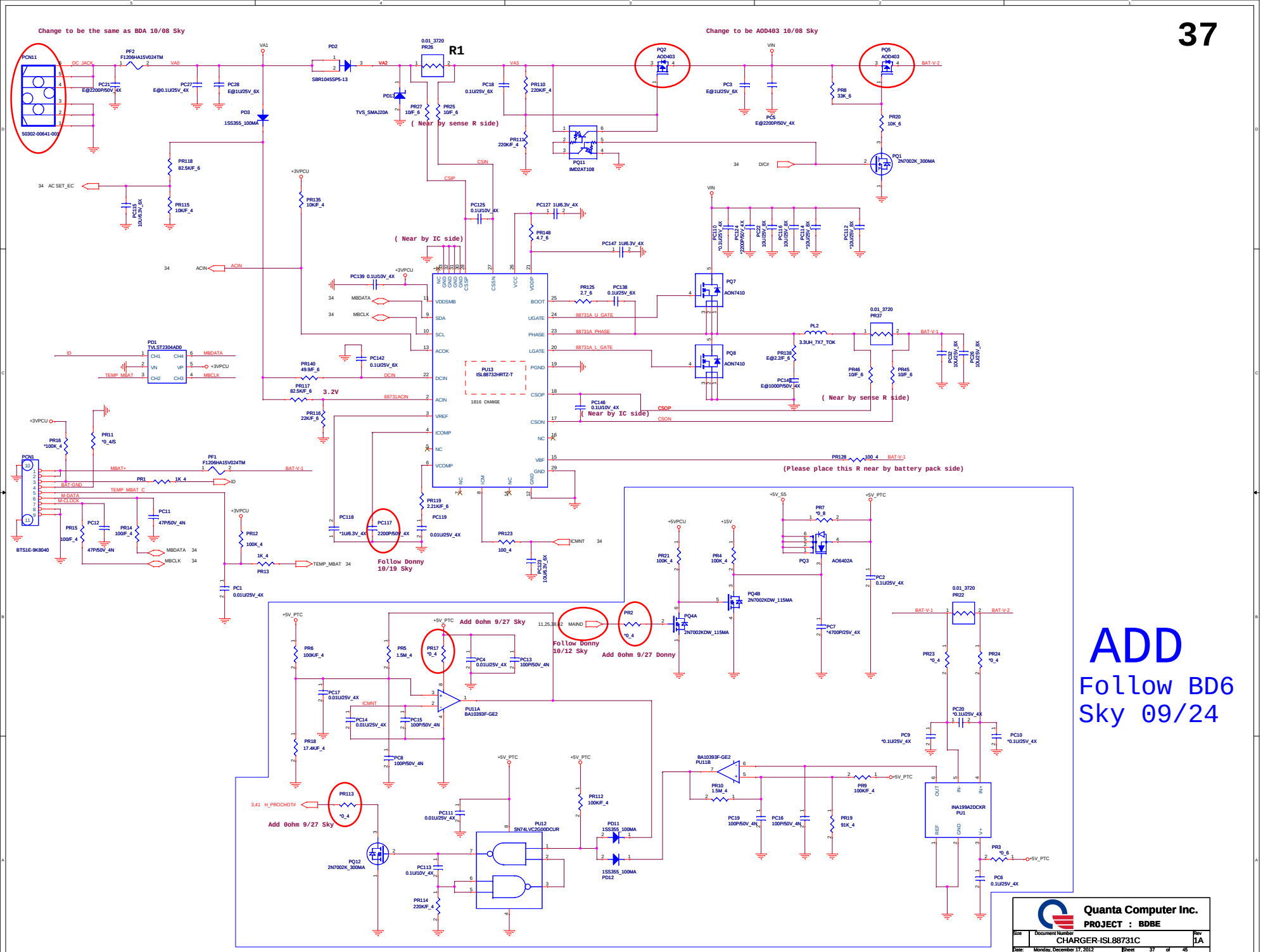
EMI EMI

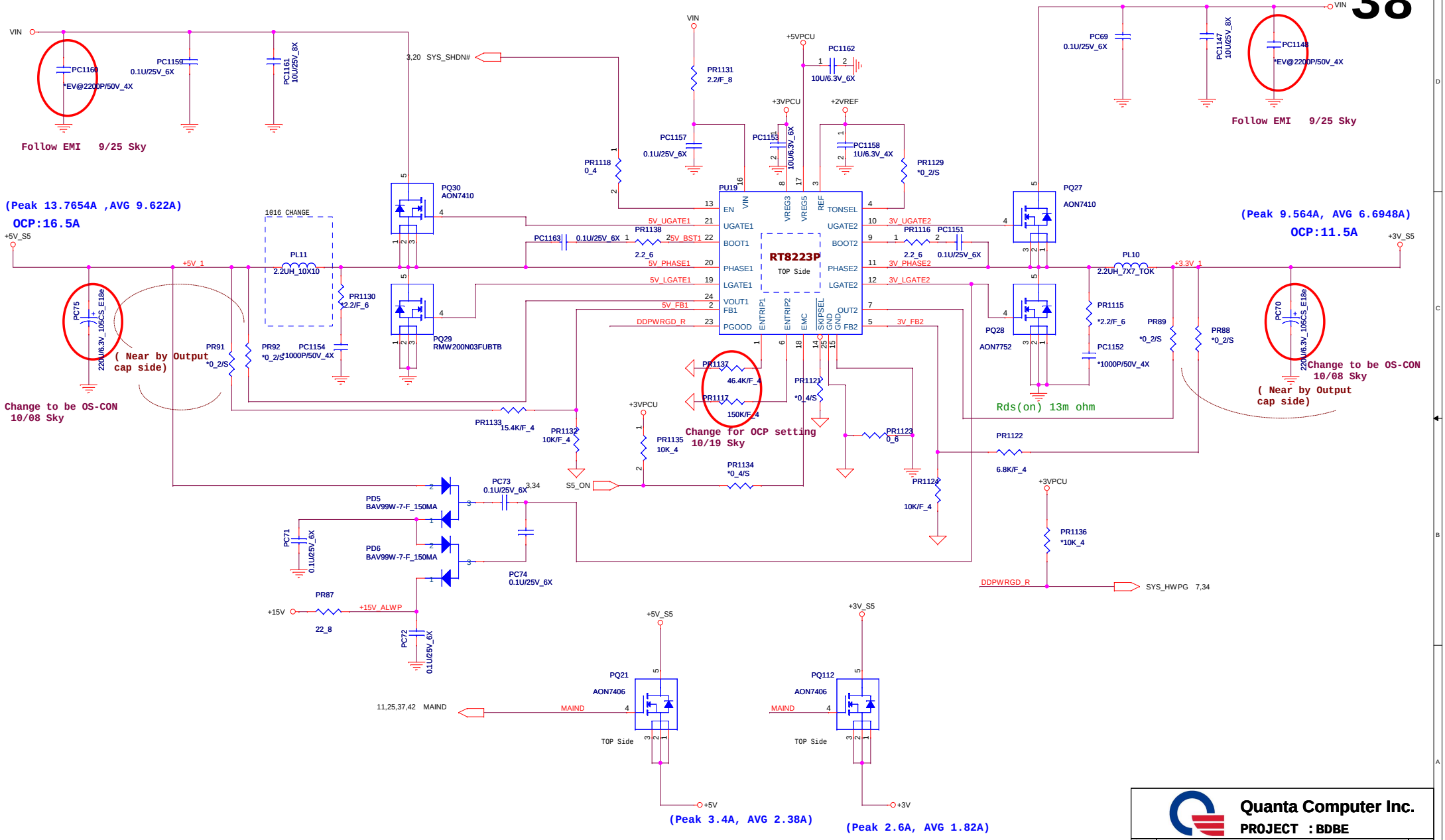


Quanta Computer Inc.
PROJECT : BDBE

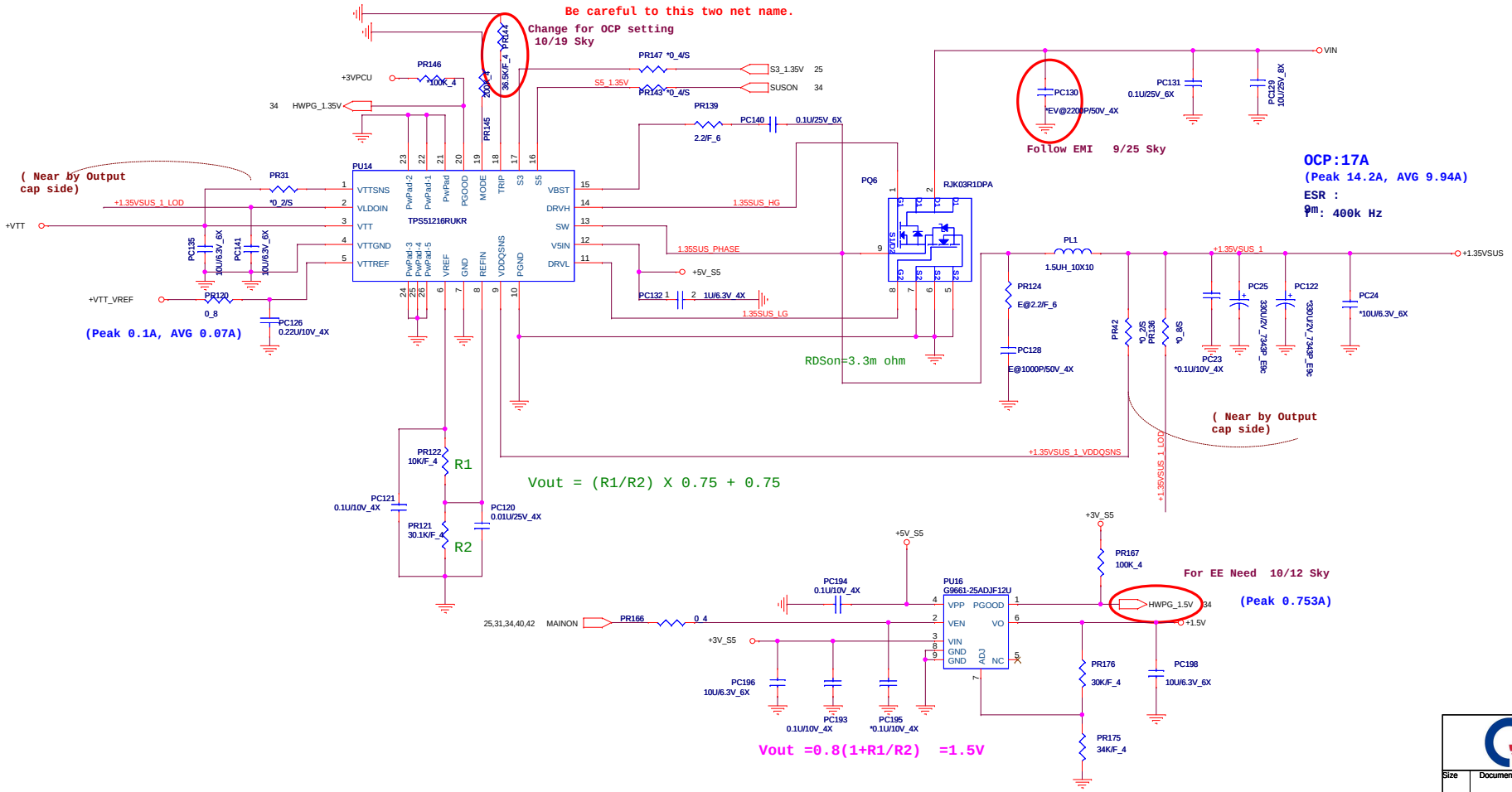
Size	Document Number	Rev
	LED/EMI/Green CLK	1A

Date: Monday, December 17, 2012 Sheet 36 of 45


Change to be the same as BDA 10/08 Sky
Change to be AOD403 10/08 Sky
R1
(Near by sense R side)
(Near by IC side)
(Near by sense R side)
(Near by IC side)
3.2V
1016 CHANGE
(Please place this R near by battery pack side)
Follow Donny 10/19 Sky
Follow Donny 10/12 Sky
Add 0ohm 9/27 Donny
Add 0ohm 9/27 Sky
Add 0ohm 9/27 Sky
ADD
Follow BD6 Sky 09/24
Quanta Computer Inc.
PROJECT : BDBE
CHARGER-ISL88731C
Rev 1A
Monday, December 17, 2012
Sheet 37 of 45



Quanta Computer Inc.		
PROJECT : BDBE		
Size	Document Number: System 3V/5V(TPS51123A)	Rev: 1A
Date: Monday, December 17, 2012	Sheet 38 of 45	

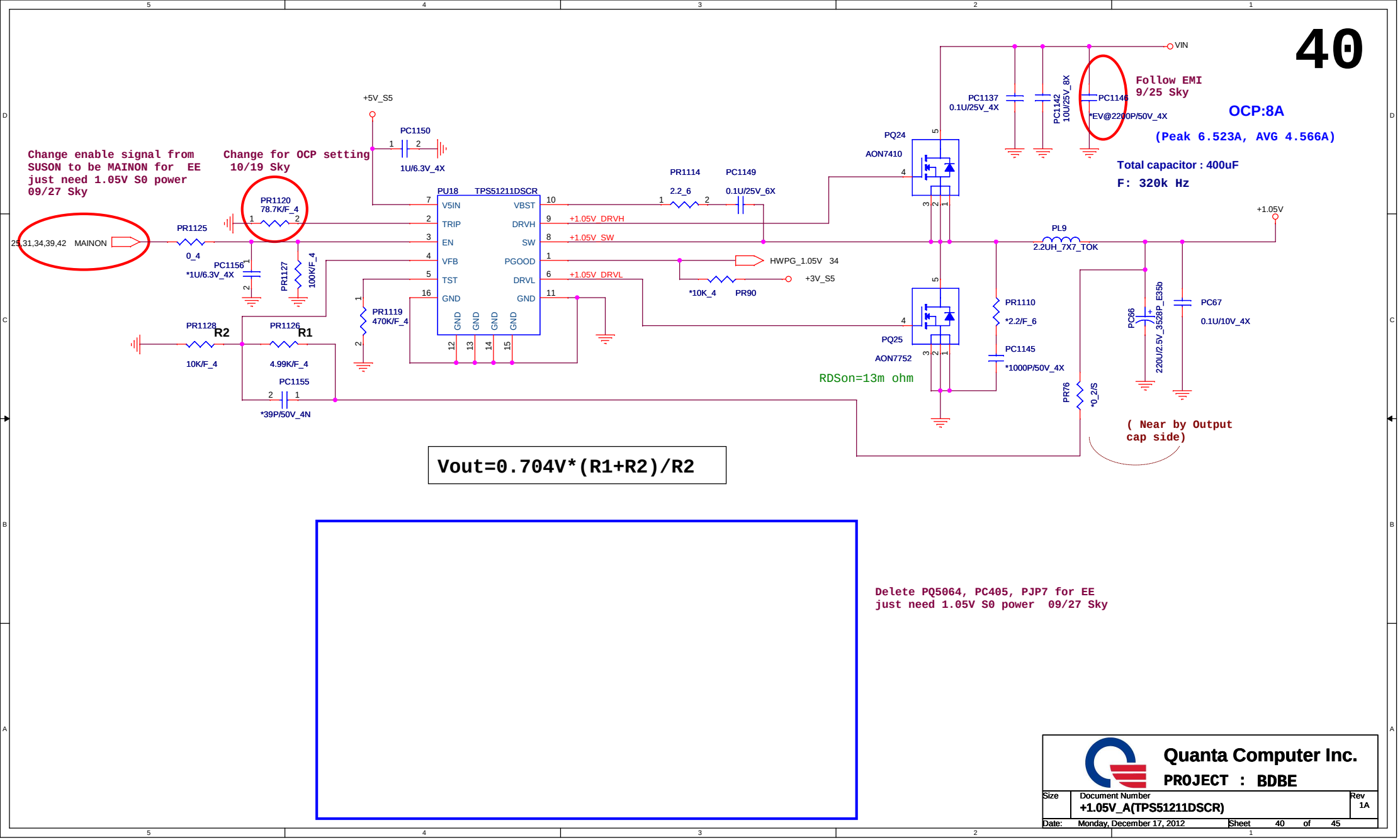


Quanta Computer Inc.

PROJECT : BDBE

Size	Document Number	Rev
	DDR1.5V	1A

Date: Monday, December 17, 2012 Sheet 39 of 45



Vout=0.704V*(R1+R2)/R2

Delete PQ5064, PC405, PJP7 for EE
just need 1.05V S0 power 09/27 Sky

Quanta Computer Inc. PROJECT : BDBE		
Size	Document Number +1.05V_A(TPS51211DSCR)	Rev 1A
Date: Monday, December 17, 2012	Sheet 40 of 45	

CPU Core : Loadline = -1.5mV/A
TDC = 33A
ICCMAX=85A

OCP=120A

CPU Core : Loadline = -1.5mV/A
TDC = 26A
ICCMAX=55A

OCP=66A

PU15
ISL95812HRZ-T

Follow FAE 9/27 Sky

Follow EMI 9/25 Sky

Add PC329 follow Donny 10/16 Sky

Max. DCR=1.1m

(Near by IC side)

(Near by MOS side)

Change VIN_VCC_IN to be VIN Sky 09/24

All Follow FAE 9/27 Sky

* PR135 PLACE NEAR PL8

(Near by Choke side)

PQ20 RJK03R1DPA

PQ9 RJK03R1DPA

PQ10 47W@RJK03R1DPA

PU2 47W@ISL6208BCRZ-T

PL4 0.22UH_7X7X4

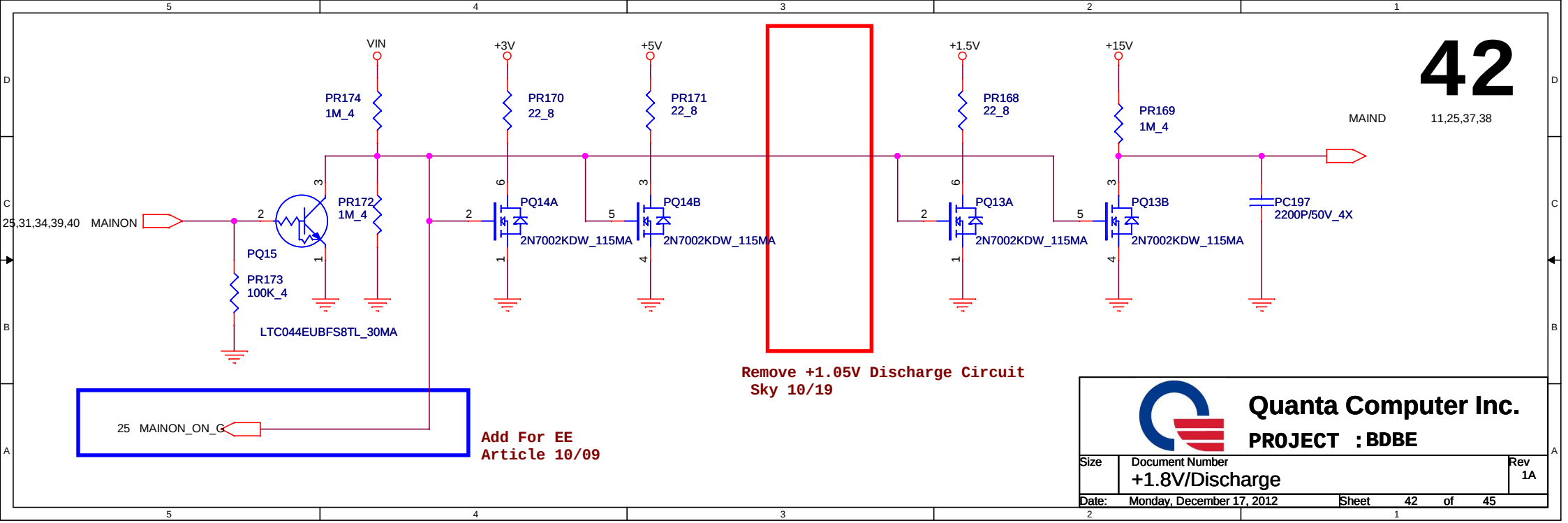
PL3 0.22UH_7X7X4

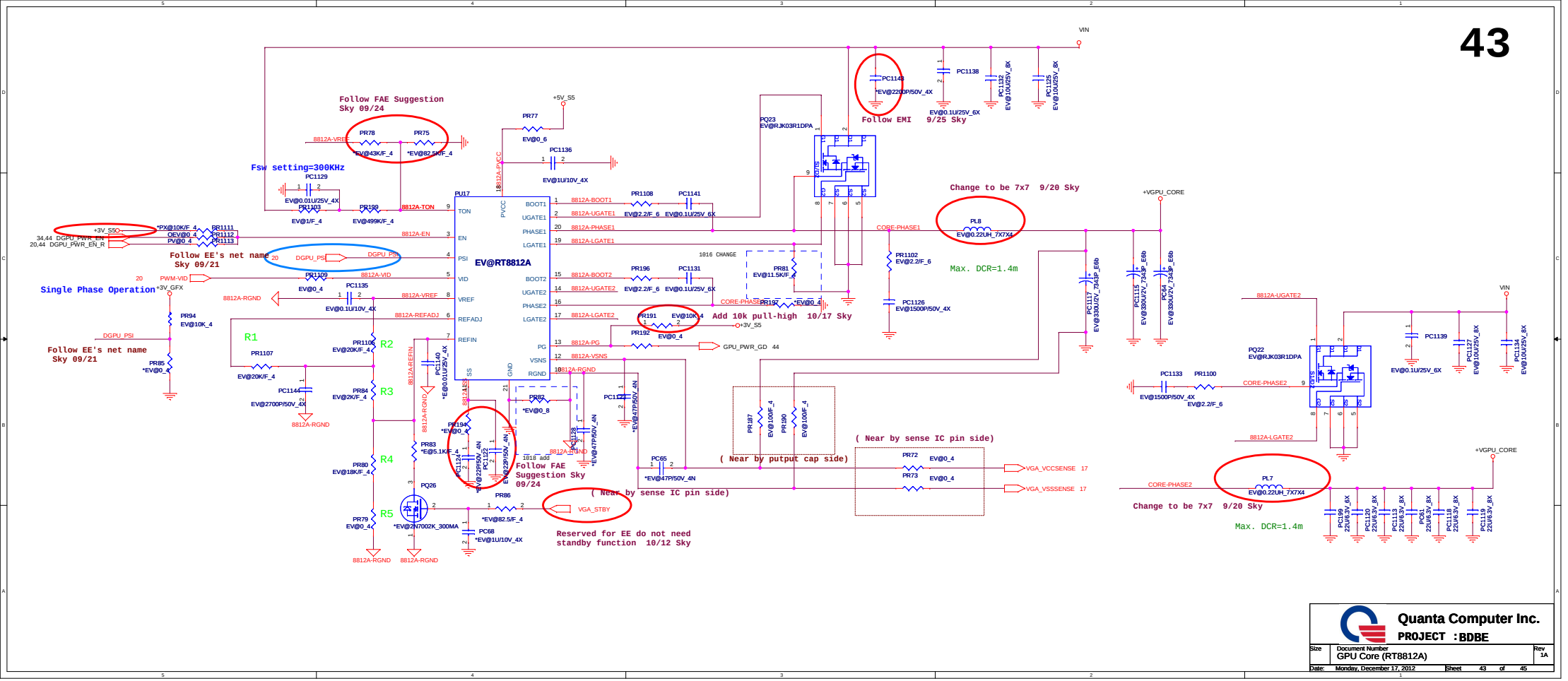
PL5 0.22UH_7X7X4

Quanta Computer Inc.
PROJECT : BDBE

Size	Document Number	Rev
	+VCCIN (ISL95812) 47/57W	1A

Date: Monday, December 17, 2012 Sheet 41 of 45

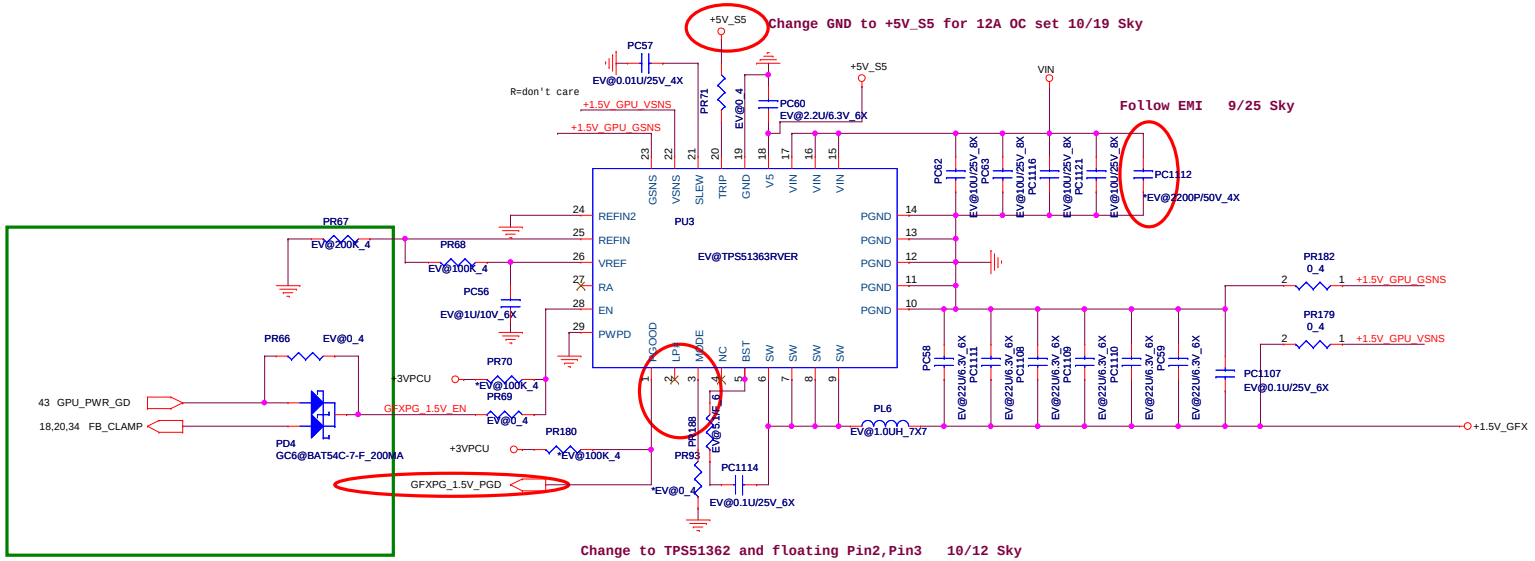

42
VIN
+3V
+5V
+1.5V
+15V
PR174
1M_4
PR170
22_8
PR171
22_8
PR168
22_8
PR169
1M_4
MAIND
11,25,37,38
25,31,34,39,40 MAINON
PR172
1M_4
PQ15
PR173
100K_4
LTC044EUBFS8TL_30MA
PQ14A
2N7002KDW_115MA
PQ14B
2N7002KDW_115MA
PQ13A
2N7002KDW_115MA
PQ13B
2N7002KDW_115MA
PC197
2200P/50V_4X
Remove +1.05V Discharge Circuit
Sky 10/19
25 MAINON_ON_G
Add For EE
Article 10/09
Quanta Computer Inc.
PROJECT : BDBE
Size
Document Number
+1.8V/Discharge
Rev
1A
Date: Monday, December 17, 2012
Sheet 42 of 45



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Change GND to +5V_S5 for 12A OC set 10/19 Sky

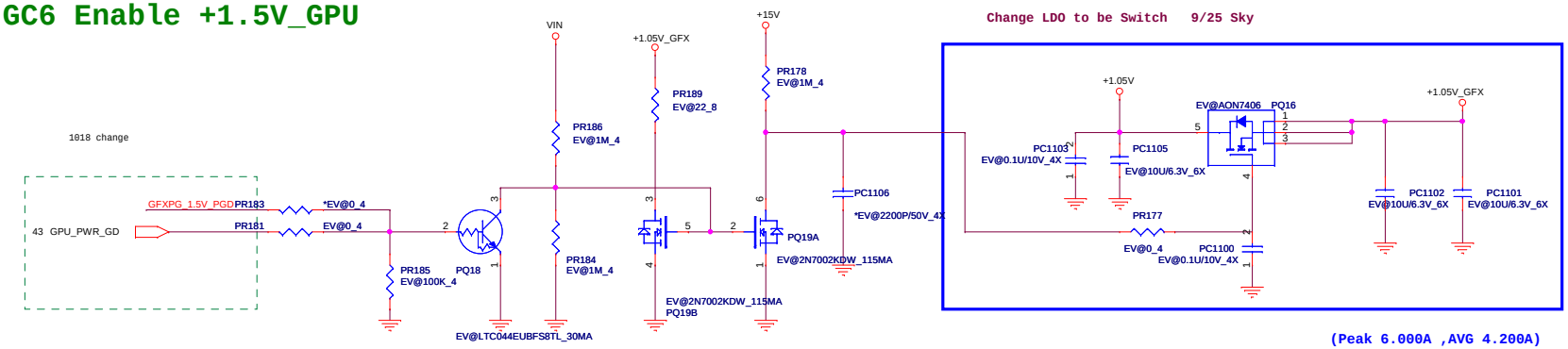
Follow EMI 9/25 Sky



GC6 Enable +1.5V_GPU

Change to TPS51362 and floating Pin2,Pin3 10/12 Sky

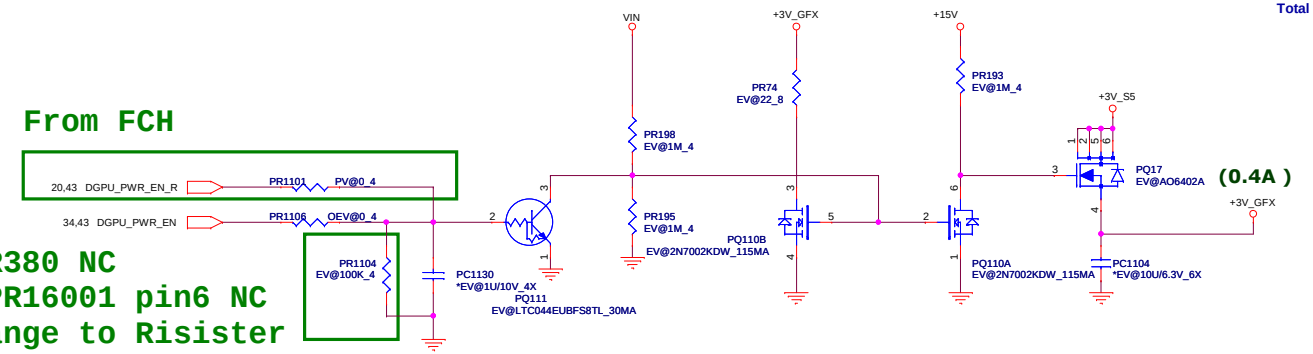
Change LDO to be Switch 9/25 Sky



(Peak 6.000A ,AVG 4.200A)

Total capacitor : 22uF

From FCH



BD5 : R380 NC
BD6 : PR16001 pin6 NC
and change to Risister
These is initial low,
for sure that dGPU power Off

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CHANGE LIST

Model	REV	
BDB	B2A	PAGE 8: C445,C455 Change to 15pf PAGE 8: CN7 Change to socket type PAGE 8: Add R1328 and R1516 for QUAD IO PAGE 9: Change C419, C423 to 12pf PAGE 10: Add board ID for SPK,CIR,TV PAGE 11: Change R1339 to +3v_s5 for EC code PAGE 19: Change C397,C398 to 12pf PAGE 30: Add LAN IC PAGE 32: Change R212,R213,R214,R215,R216,R217,R218,R219 to bead PAGE 33: Change Cardreader to RTS5229 PAGE 33: Add R453 for PB_LED change to high active PAGE 34: Remove R1408 for optimus PAGE 35: Change PWR/B LED PWR to +5VPCU for white LED PAGE 35: Change hole1,hole2,hole112 and hole117 for ID PAGE 36: Change R1496,R1497,R1499 and R1503 for LED brightness SPEC

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1	1A	
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24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

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	PART NUMBER:		DRAWING BY:		REVISON:	

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