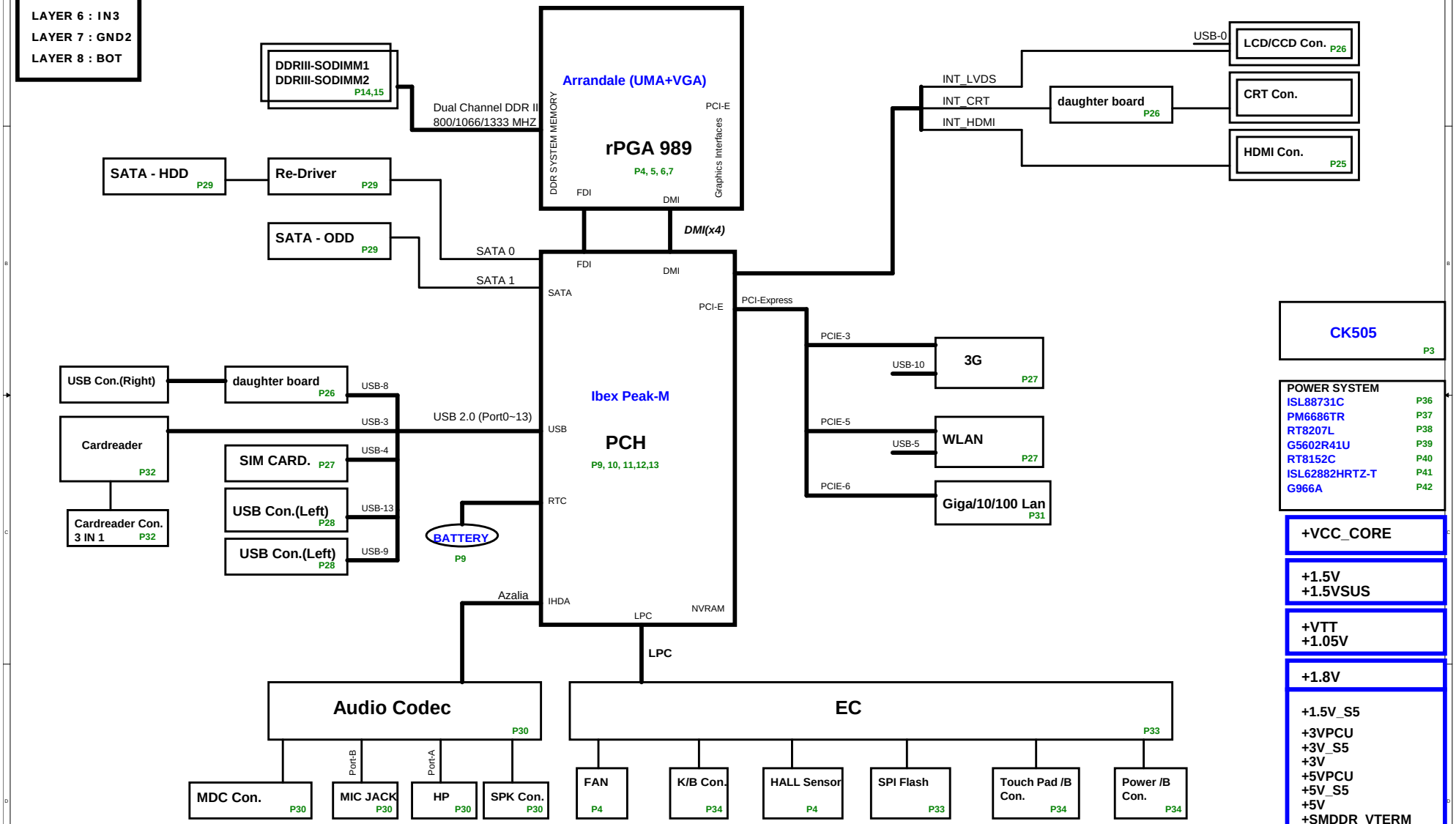
PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND2
- LAYER 8 : BOT

TE4 Block Diagram



Quanta Computer Inc.
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	Block Diagram	1A

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14-15	DDRIII SO-DIMM
25	HDMI comm part
26	LCD Panel
	CRT & CRT BUS SWITCH
	CCD
	HALL SENSOR&BACK LIGHT SWITCH
27	MINI Card (Wi-Fi & WIMAX)
	MINI Card 2nd
	MINI Card 3nd
28	USB 2.0
29	SATA ODD
	Main SATA HDD & 2nd SATA HDD
30	Codec (CX20587)
31	Atheros LAN
32	3 IN 1 Card reader
33	EC NPCE791L
34	INT KeyBoard & K/B LED Power
	TP board
	Power SW
	HOLE
35	LED / EMI
36	Charger (ISL88731C)
37	System 5V/3V (PM6686TR)
38	DDR1.5V(RT8207L)/1.05VSUS
39	+VTT/+1.05V (G5602R41U)
40	VAXG_CORE RT8152C FOR UMA
41	+VCC_CORE(ISL62882HRTZ-T)
42	+1.8V (G966A)/Discharge

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

GND PLANE	PAGE
8769AGND	33
Audio_GND	30
Shield_GND	30
GND	ALL
ISL95870A_AGND	30

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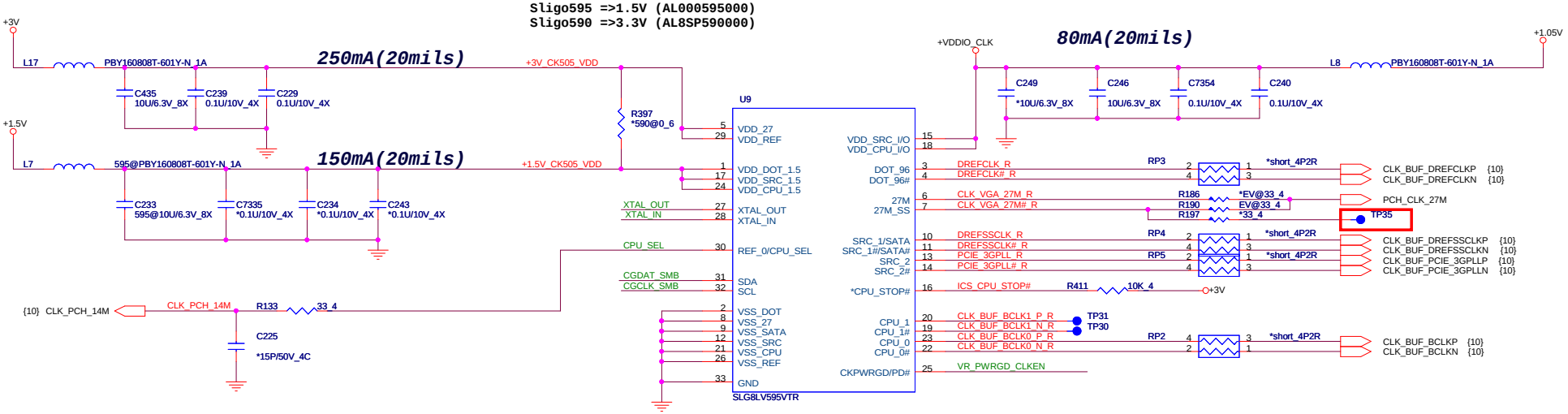
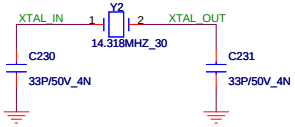
CLOCK Gen [CLK]

03

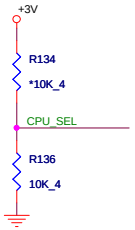
Pin1/17/24
Sligo595 =>1.5V (AL000595000)
Sligo590 =>3.3V (AL8SP590000)



CLK CRYSTAL

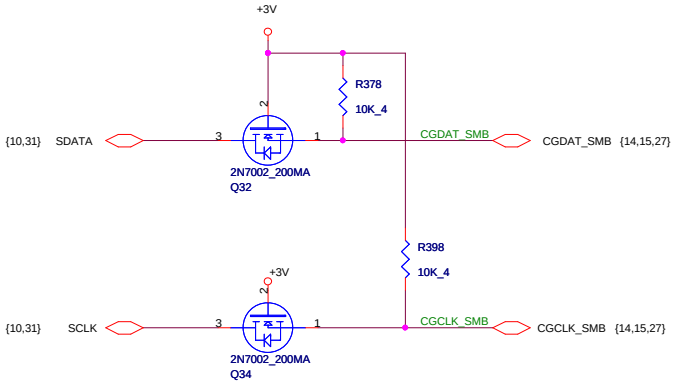


CLK CPU_SEL

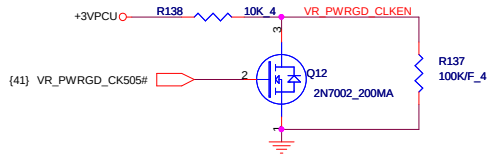


	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD



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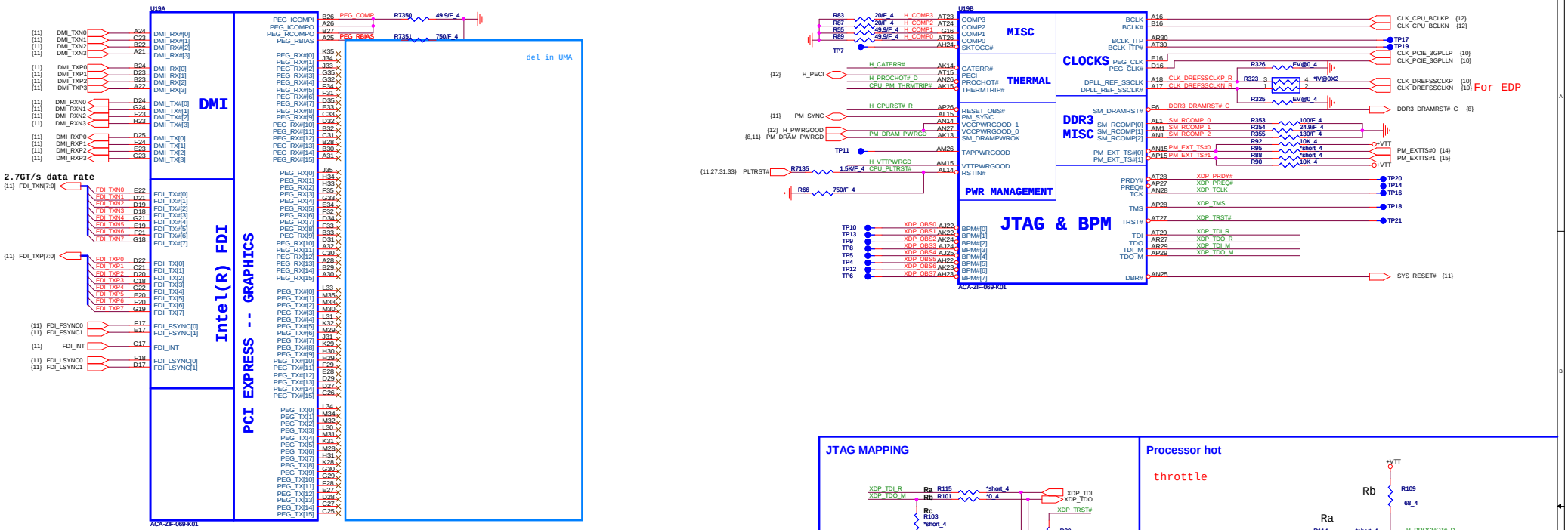


JTAG MAPPING

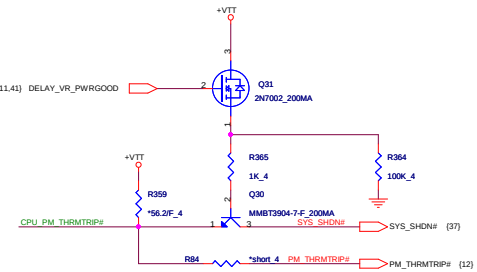
Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

Processor hot

throttle

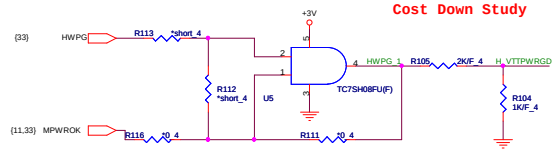
If Ra no stuff must change Rb to 50 ohm

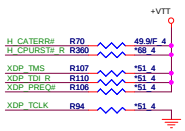
Thermal Trip



VTT Power Good

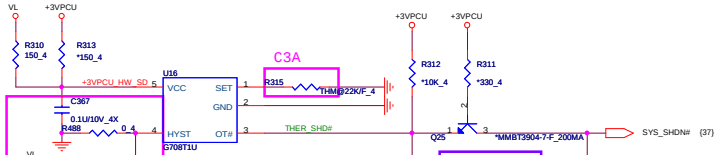
Cost Down Study





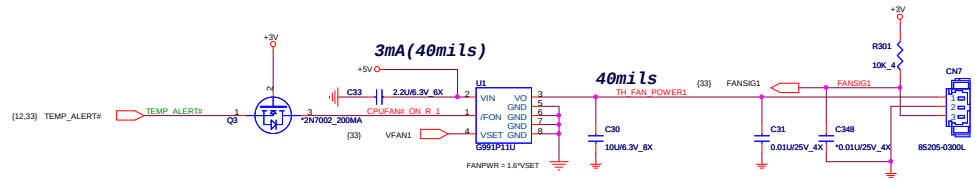
FDI Disable (Discrete only)

Local Temperature



C3A #Shut down on 86 degree# D3B

CPU FAN CTRL



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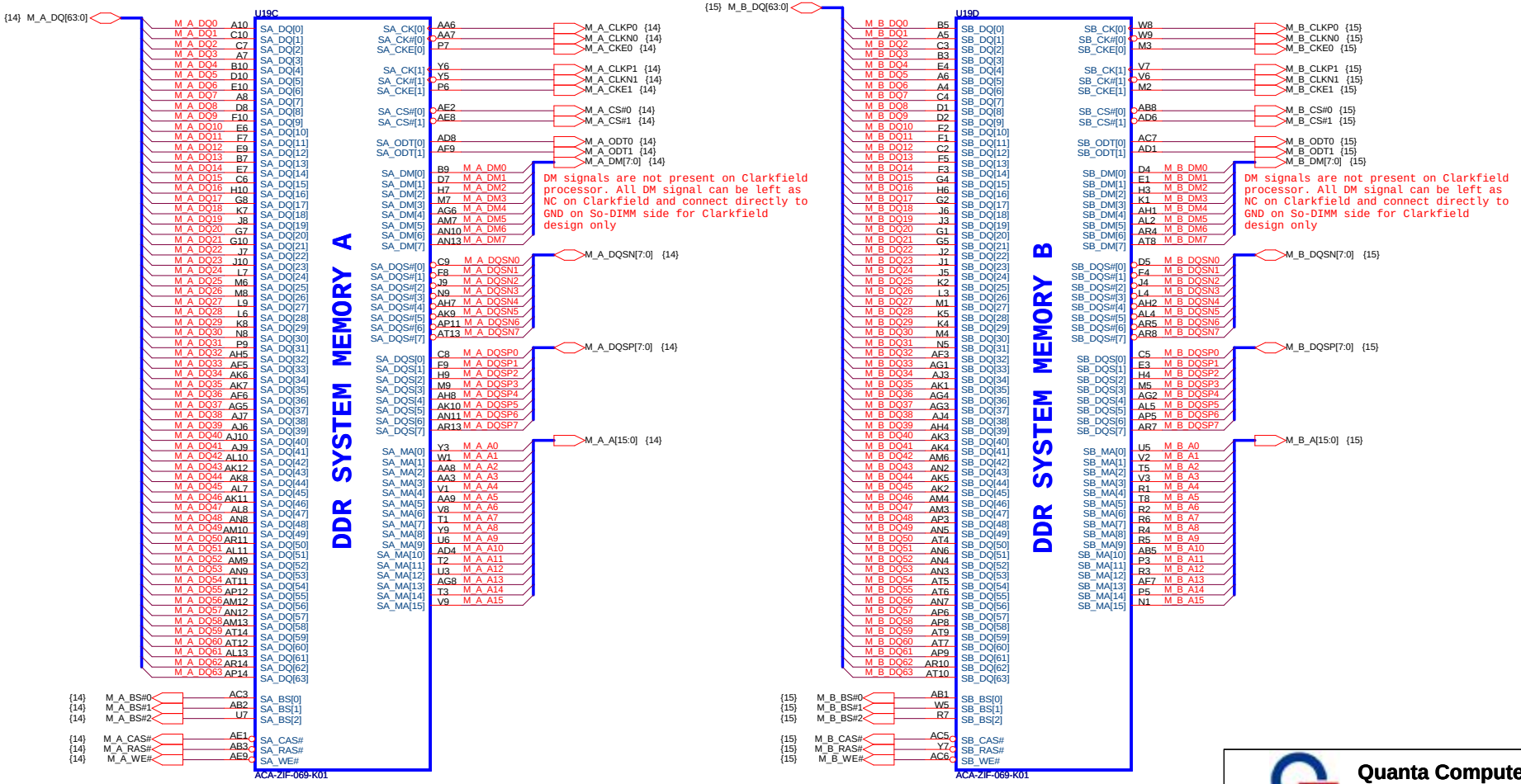
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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	PROCESSER 2/4(DDR)	A1A

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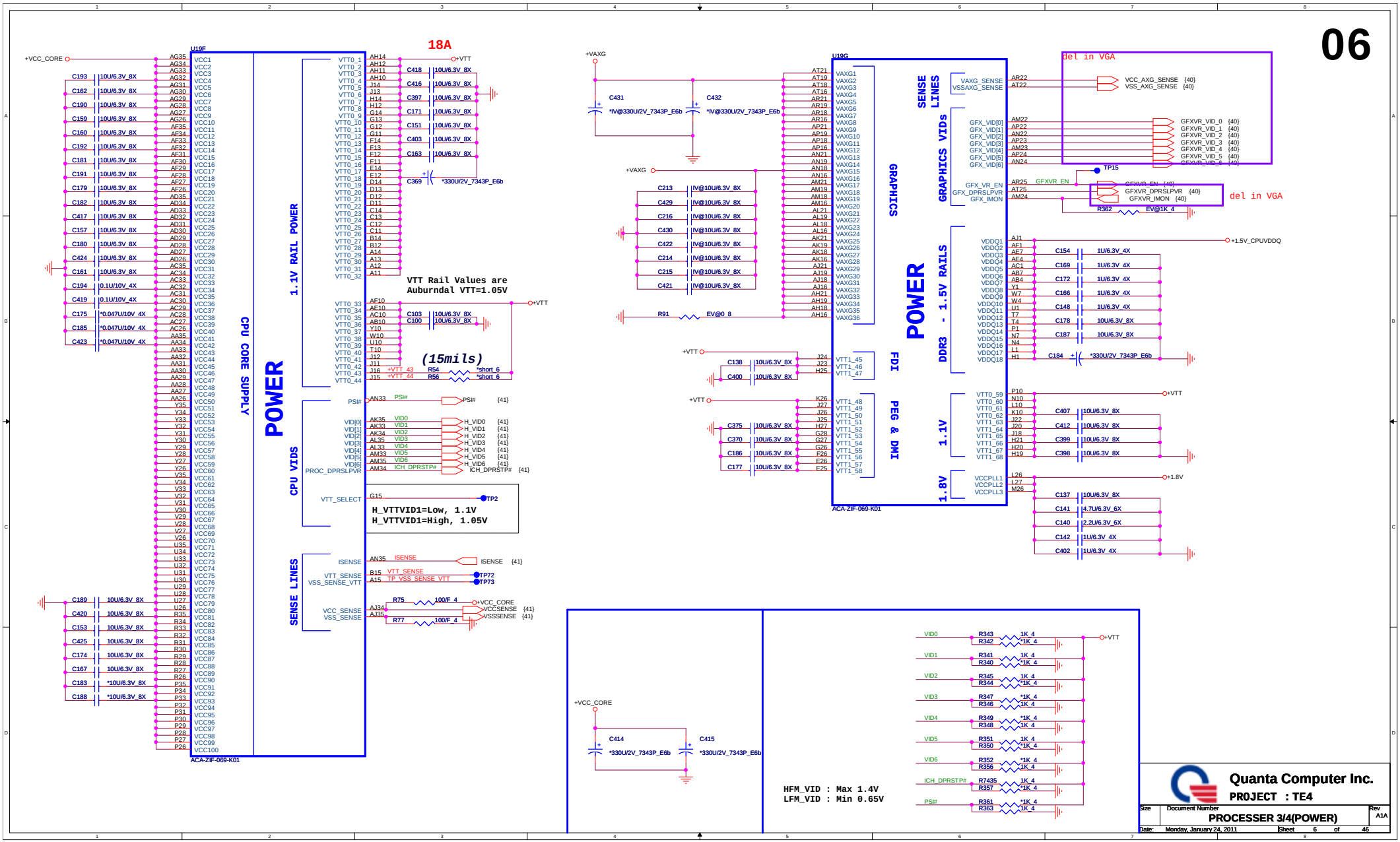
06
18A
U19F
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
ACA-ZIF-069-K01
VTT Rail Values are
Auburndal VTT=1.05V
(15mils)
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
U19G
POWER
GRAPHICS
FDI
PEG & DMI
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
1.1V
1.8V
del in VGA
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
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PROCESSER 3/4(POWER)
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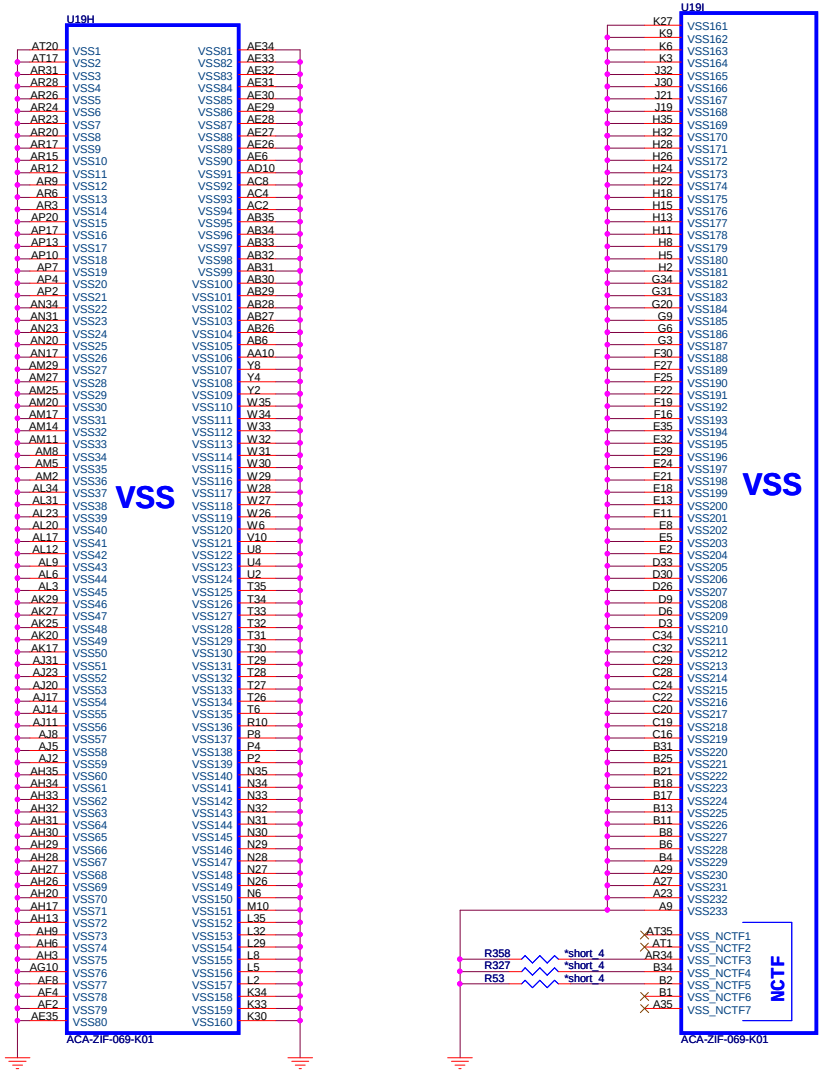
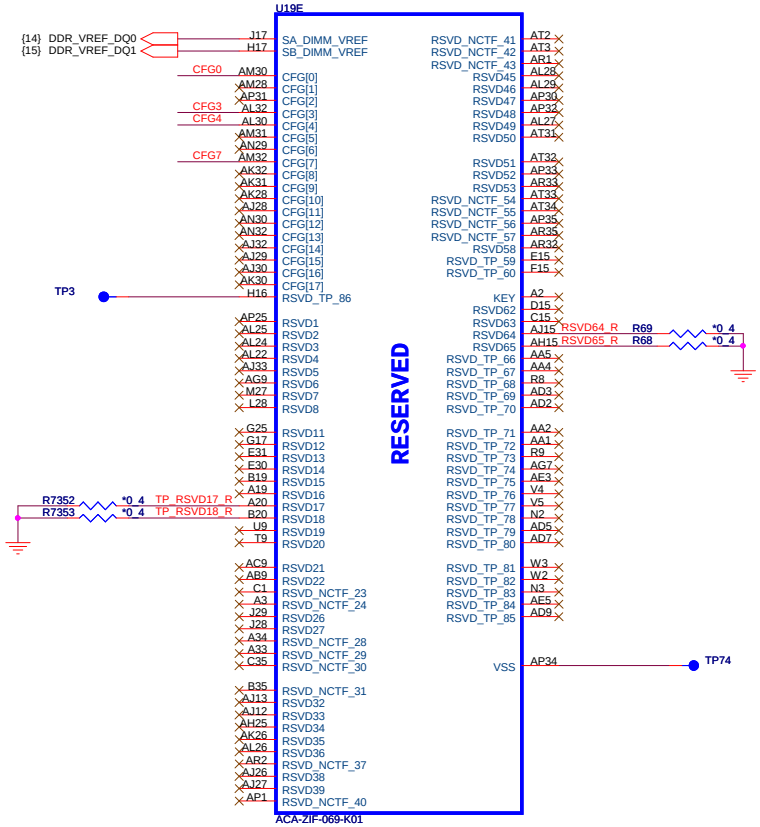
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

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	PROCESSER 4/4 (GND)	A1A
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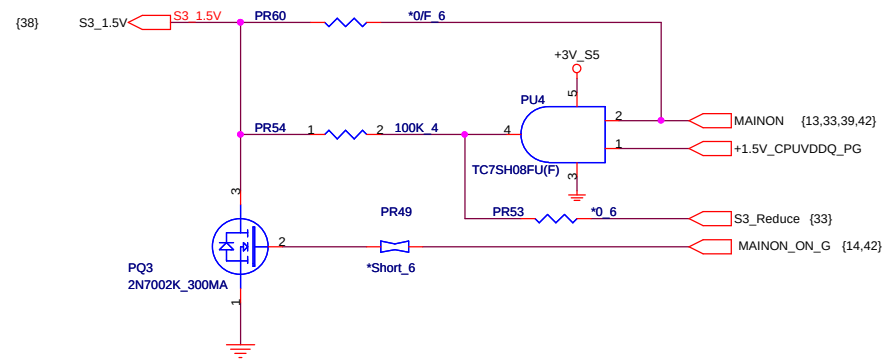
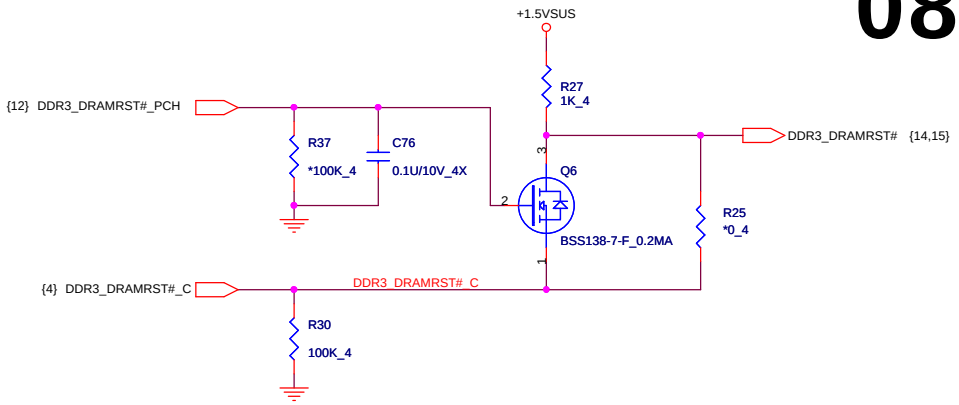
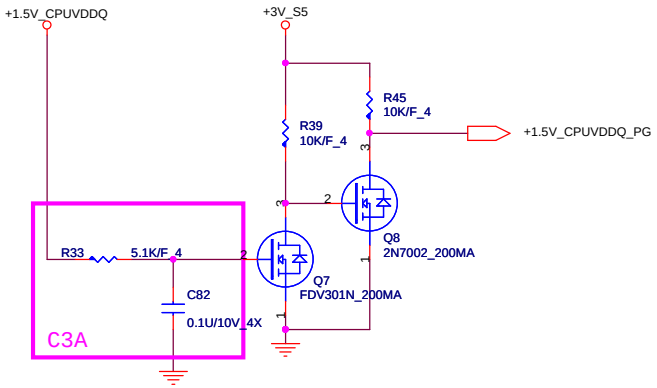
S3 Power Enable



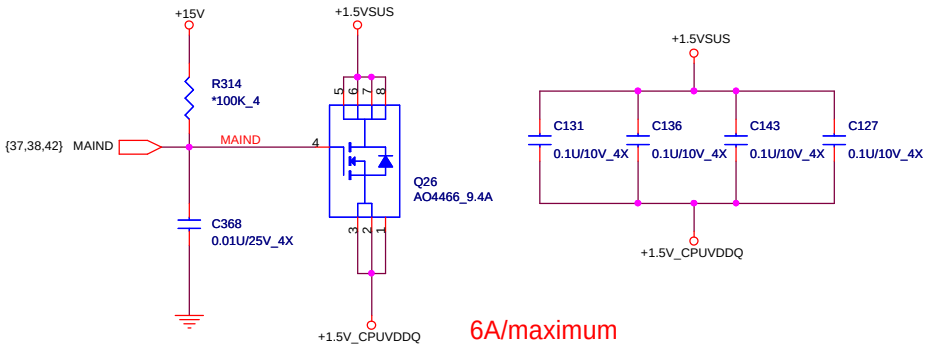
DRAM Reset



VDDQ Power Good



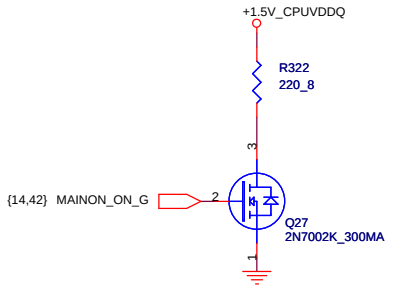
VDDQ Power Switch



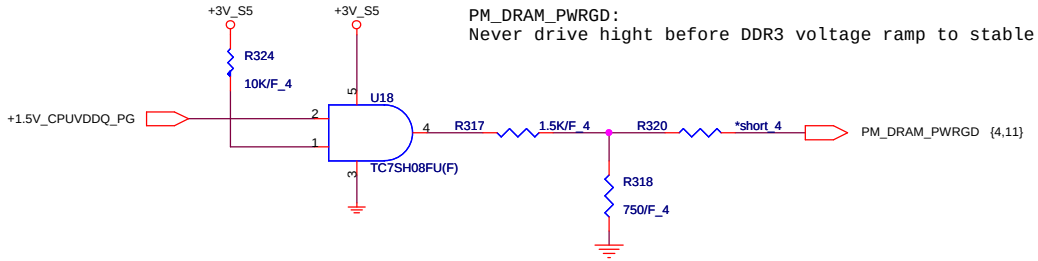
6A/maximum

Q7044可換AO6402A,cost down.

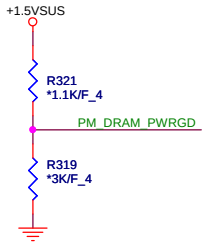
VDDQ Discharge



DRAM Power Good



PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable



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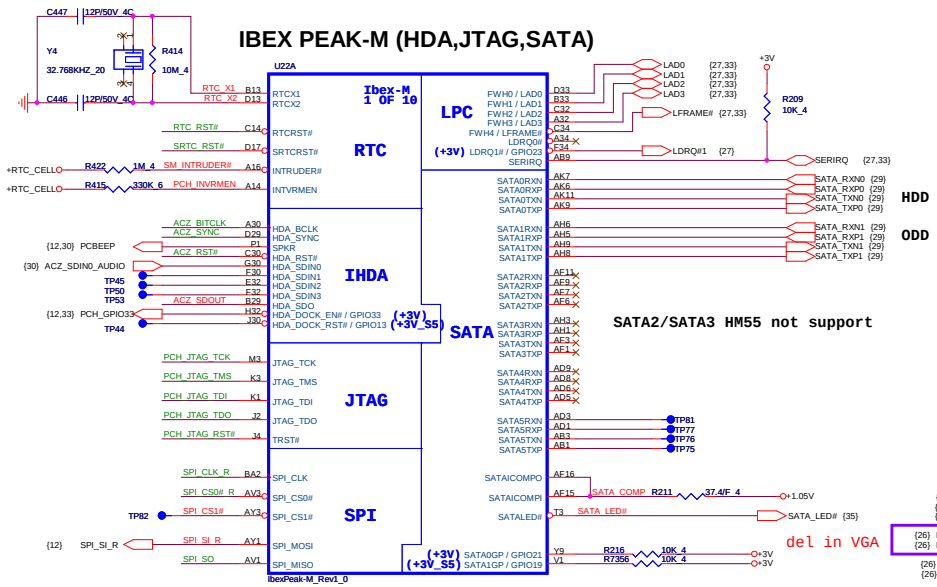
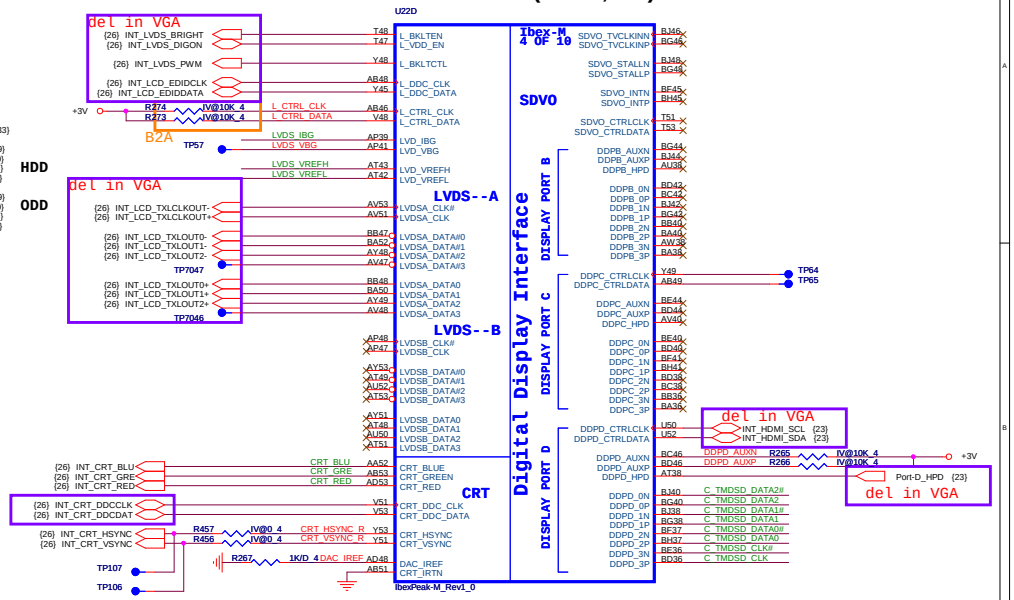
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

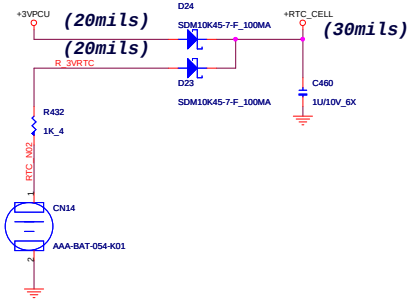


IBEX PEAK-M (LVDS,DDI)



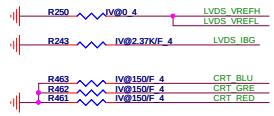
[RTC]

RTC BATTERY

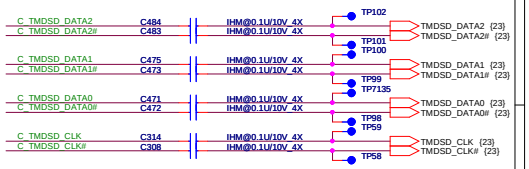


DDP Setting

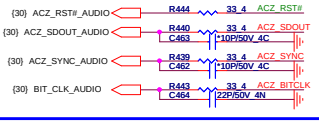
Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

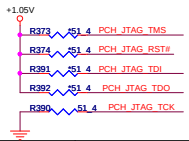


HDMI



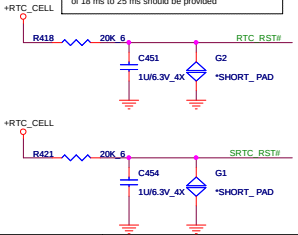
Alzia



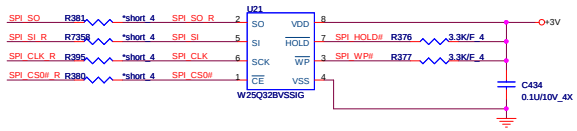


RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided



4M byte SPI ROM



PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

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	PCH 1/5 (SATA,HDA,LPC)	A1A
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IBEX PEAK-M (GND)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

10

U22I

IbexPeak-M_Rev1_0

U22B

IbexPeak-M_Rev1_0

SMBUS

CRYSTAL

Placement close

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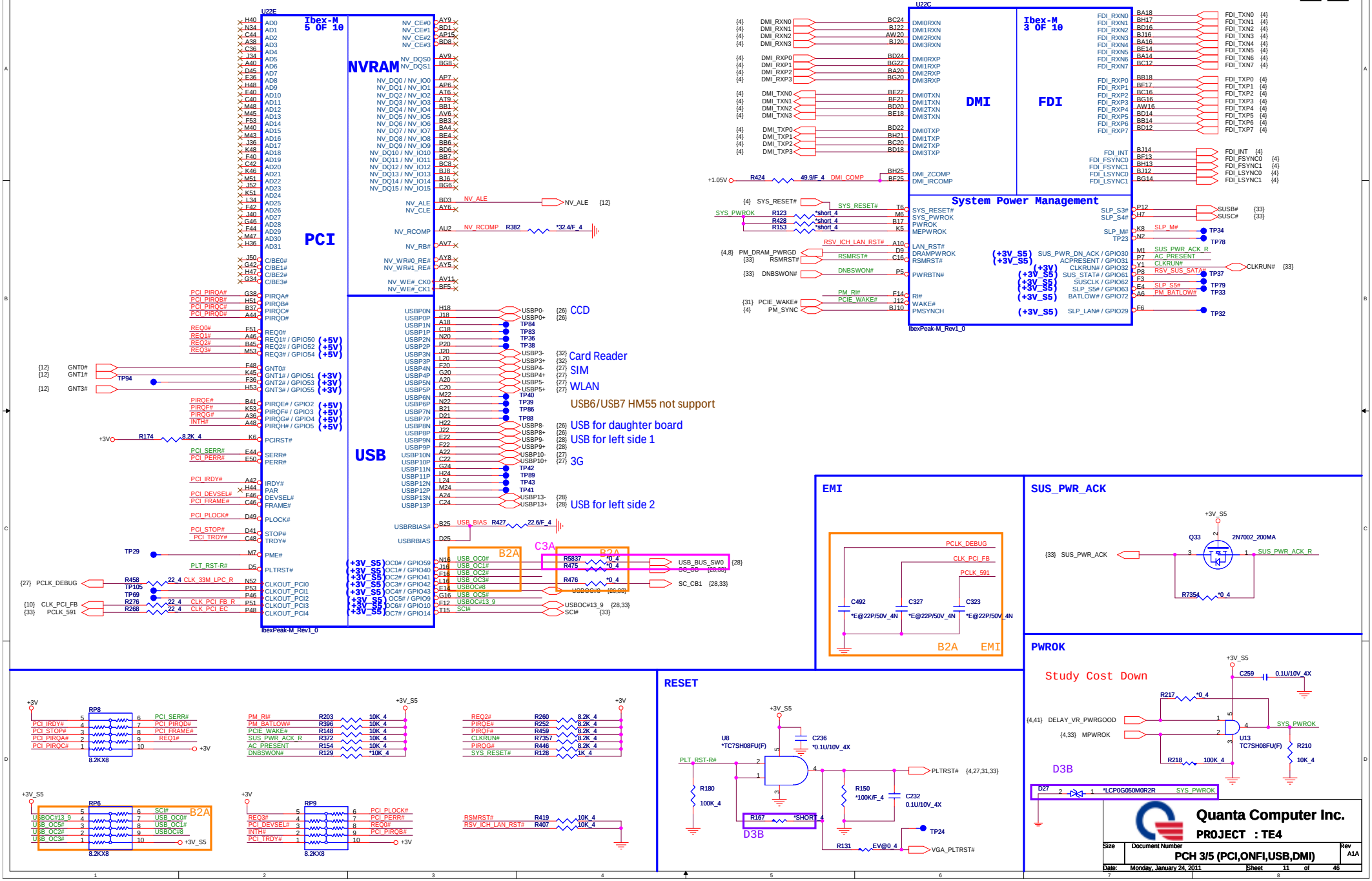
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)

11



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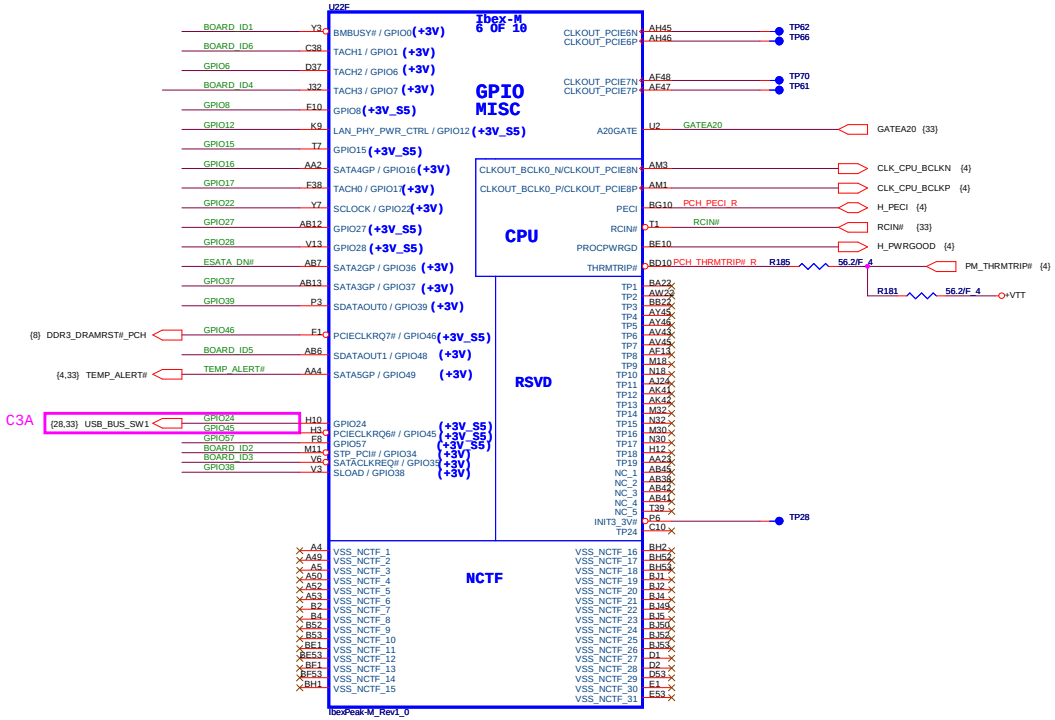
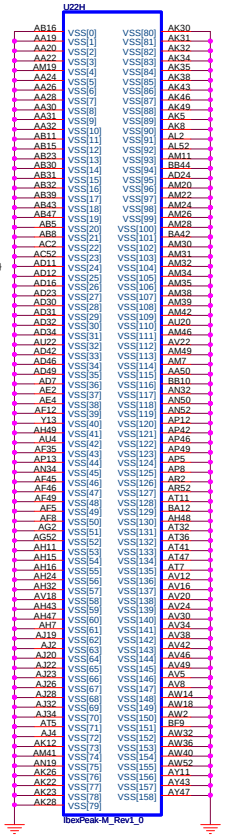
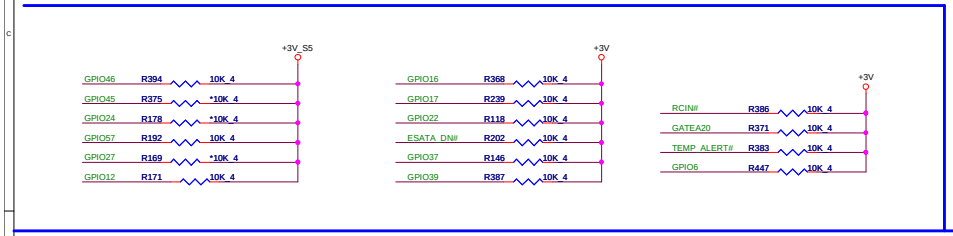
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



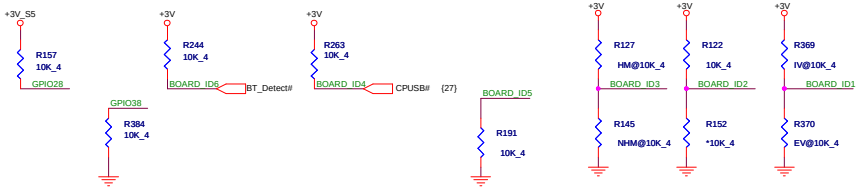
IBEX PEAK-M (GND)





BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	GPIO28	GPIO38
UMA SKU VGA SKU	H L							
W/ MDC W/O MDC		H L						
W/ HDMI W/O HDMI			H L					
W/O 3G W/ 3G				H L				
15" 14"					H L			
W/O BT W/ BT						H L		
14 or 15 13							H L	
Old HW(2010) New HW(2011)								H L



12

PCH Strap Pin Configuration Table

SPKR

{9,30} PCBEEP — *1K/F_4 — R388 — +3V

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/ GPIO55

{11} GNT3# — R460 — *10K/F_4

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

HDA_DOCK_EN #/GPIO33

{9,33} PCH_GPIO33 — R237 — 1K/F_4 — JP1 (2, 1) — *SHORT PAD

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

GNT0#, GNT1#

{11} GNT0# — GNT0# R270 *1K/F_4
{11} GNT1# — GNT1# R271 *1K/F_4

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

SPI_MOSI

{9} SPI_SI_R — R7355 — *1K_4 — +3V

NV_ALE

{11} NV_ALE — R403 — *10K_4 — +1.8V

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 — R149 — 10K_4 — +3V_S5

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 — R126 — 1K_4 — +3V_S5

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

GPIO27

GPIO27 — R182 — *10K_4

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	A1A
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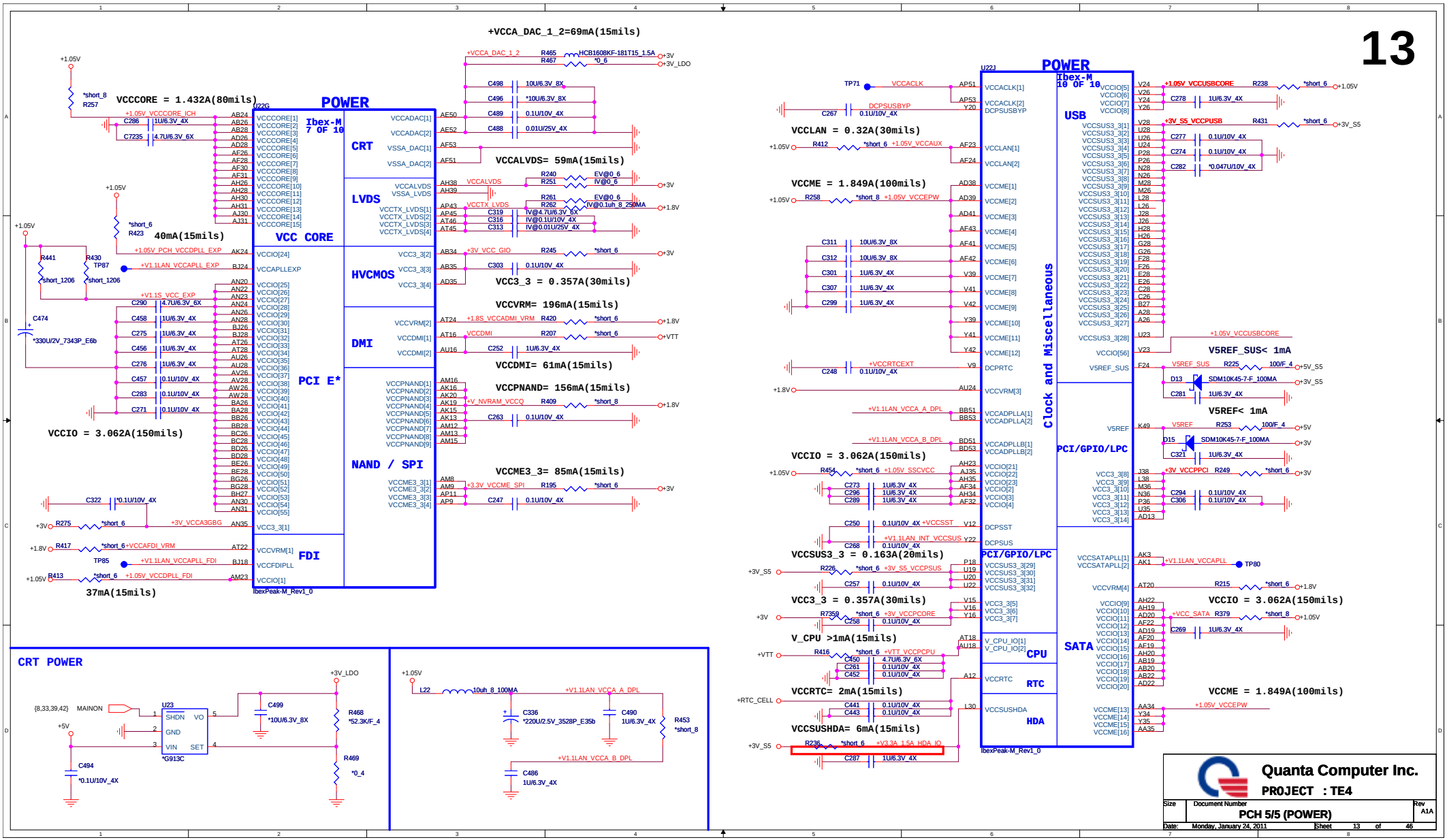
13
+VCCA_DAC_1_2=69mA(15mils)
VCCCORE = 1.432A(80mils)
40mA(15mils)
VCCIO = 3.062A(150mils)
37mA(15mils)
POWER
Ibex-M
7 OF 10
VCC CORE
PCI E*
CRT
LVDS
HVCMOS
DMI
NAND / SPI
FDI
VCCALVDS= 59mA(15mils)
VCC3_3 = 0.357A(30mils)
VCCVRM= 196mA(15mils)
VCCDMI= 61mA(15mils)
VCCPNAND= 156mA(15mils)
VCCME3_3= 85mA(15mils)
IbexPeak-M_Rev1_0
CRT POWER
VCCME = 1.849A(100mils)
VCCLAN = 0.32A(30mils)
VCCSUS3_3 = 0.163A(20mils)
V_CPU >1mA(15mils)
VCCRTC= 2mA(15mils)
VCCSUSHDA= 6mA(15mils)
POWER
Ibex-M
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
V5REF_SUS< 1mA
V5REF< 1mA
VCCIO = 3.062A(150mils)
VCCME = 1.849A(100mils)
Quanta Computer Inc.
PROJECT : TE4
PCH 5/5 (POWER)
Monday, January 24, 2011
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H=4

JDIM2A

{5} M_A_A[15:0]

M_A_A0 98, M_A_A1 97, M_A_A2 96, M_A_A3 95, M_A_A4 92, M_A_A5 91, M_A_A6 90, M_A_A7 86, M_A_A8 89, M_A_A9 85, M_A_A10 107, M_A_A11 84, M_A_A12 83, M_A_A13 119, M_A_A14 80, M_A_A15 78

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

{5} M_A_BS#0 109
{5} M_A_BS#1 108
{5} M_A_BS#2 79
{5} M_A_CS#0 114
{5} M_A_CS#1 121
{5} M_A_CLKP0 101
{5} M_A_CLKN0 103
{5} M_A_CLKP1 102
{5} M_A_CLKN1 104
{5} M_A_CKE0 73
{5} M_A_CKE1 74
{5} M_A_CAS# 115
{5} M_A_RAS# 110
{5} M_A_WE# 113

BA0 BA1 BA2 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#

R78 10K/F_4 DIMM0_SA0
R79 10K/F_4 DIMM0_SA1

{3,15,27} CGCLK_SMB 197
{3,15,27} CGDAT_SMB 201

SA0 SA1 SCL SDA

{5} M_A_ODT0 116
{5} M_A_ODT1 120

ODT0 ODT1

{5} M_A_DM[7:0]

M_A_DM0 11, M_A_DM1 28, M_A_DM2 46, M_A_DM3 63, M_A_DM4 136, M_A_DM5 153, M_A_DM6 170, M_A_DM7 187

DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

{5} M_A_DQSP[7:0]

M_A_DQSP0 12, M_A_DQSP1 29, M_A_DQSP2 47, M_A_DQSP3 64, M_A_DQSP4 137, M_A_DQSP5 154, M_A_DQSP6 171, M_A_DQSP7 188

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

{5} M_A_DQSN[7:0]

M_A_DQSN0 10, M_A_DQSN1 27, M_A_DQSN2 45, M_A_DQSN3 62, M_A_DQSN4 135, M_A_DQSN5 152, M_A_DQSN6 169, M_A_DQSN7 186

DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRSK-20401-TP4B

M_A_DQ[63:0] {5}

M_A_DQ0 5, M_A_DQ1 7, M_A_DQ2 15, M_A_DQ3 17, M_A_DQ4 4, M_A_DQ5 6, M_A_DQ6 16, M_A_DQ7 18, M_A_DQ8 21, M_A_DQ9 23, M_A_DQ10 33, M_A_DQ11 35, M_A_DQ12 22, M_A_DQ13 24, M_A_DQ14 34, M_A_DQ15 36, M_A_DQ16 39, M_A_DQ17 41, M_A_DQ18 51, M_A_DQ23 53, M_A_DQ21 40, M_A_DQ20 42, M_A_DQ22 50, M_A_DQ19 52, M_A_DQ28 57, M_A_DQ25 59, M_A_DQ26 67, M_A_DQ27 69, M_A_DQ29 56, M_A_DQ24 58, M_A_DQ30 68, M_A_DQ31 70, M_A_DQ36 129, M_A_DQ37 131, M_A_DQ35 141, M_A_DQ34 143, M_A_DQ32 130, M_A_DQ33 132, M_A_DQ39 140, M_A_DQ38 142, M_A_DQ45 147, M_A_DQ44 149, M_A_DQ47 157, M_A_DQ46 159, M_A_DQ40 146, M_A_DQ41 148, M_A_DQ42 158, M_A_DQ43 160, M_A_DQ48 163, M_A_DQ53 165, M_A_DQ55 175, M_A_DQ54 177, M_A_DQ52 164, M_A_DQ49 166, M_A_DQ51 174, M_A_DQ50 176, M_A_DQ61 181, M_A_DQ60 183, M_A_DQ58 191, M_A_DQ59 193, M_A_DQ57 180, M_A_DQ56 182, M_A_DQ62 192, M_A_DQ63 194

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ23 DQ21 DQ20 DQ22 DQ19 DQ28 DQ25 DQ26 DQ27 DQ29 DQ24 DQ30 DQ31 DQ36 DQ37 DQ35 DQ34 DQ32 DQ33 DQ39 DQ38 DQ45 DQ44 DQ47 DQ46 DQ40 DQ41 DQ42 DQ43 DQ48 DQ53 DQ55 DQ54 DQ52 DQ49 DQ51 DQ50 DQ61 DQ60 DQ58 DQ59 DQ57 DQ56 DQ62 DQ63

JDIM2B

+1.5VSUS

VDD1 75, VDD2 76, VDD3 81, VDD4 82, VDD5 87, VDD6 88, VDD7 93, VDD8 94, VDD9 99, VDD10 100, VDD11 105, VDD12 106, VDD13 111, VDD14 112, VDD15 117, VDD16 118, VDD17 123, VDD18 124

+3V 199 VDDSPD

NC1 77, NC2 122, NCTEST 125

{4} PM_EXTTS#0 198 EVENT#
{8,15} DDR3_DRAMRST# 30 RESET#
+1.5VSUS R41 *1K/F_4 PM_EXTTS#0

{7} DDR_VREF_DQ0 R26 *0_4 SMDDR_VREF_DQ0
SMDDR_VREF_DIMM 1 VREF_DQ, 126 VREF_CA

R22 *100K/F_4

B2A

VSS1 2, VSS2 3, VSS3 8, VSS4 9, VSS5 13, VSS6 14, VSS7 19, VSS8 20, VSS9 25, VSS10 26, VSS11 31, VSS12 32, VSS13 37, VSS14 38, VSS15 43

VSS16 44, VSS17 48, VSS18 49, VSS19 54, VSS20 55, VSS21 60, VSS22 61, VSS23 65, VSS24 66, VSS25 71, VSS26 72, VSS27 127, VSS28 128, VSS29 133, VSS30 134, VSS31 138, VSS32 139, VSS33 144, VSS34 145, VSS35 150, VSS36 151, VSS37 155, VSS38 156, VSS39 161, VSS40 162, VSS41 167, VSS42 168, VSS43 172, VSS44 173, VSS45 178, VSS46 179, VSS47 184, VSS48 185, VSS49 189, VSS50 190, VSS51 195, VSS52 196

VTT1 203, VTT2 204 +SMDDR_VTERM

GND 205, GND 206

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRSK-20401-TP4B

Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

+1.5VSUS
C116 4.7U/6.3V_6X
C115 4.7U/6.3V_6X
C132 4.7U/6.3V_6X
C110 4.7U/6.3V_6X
C128 4.7U/6.3V_6X
C149 4.7U/6.3V_6X
C124 0.1U/10V_4X
C125 0.1U/10V_4X
C123 0.1U/10V_4X
C114 0.1U/10V_4X
C139 0.1U/10V_4X
C120 *0.047U/10V_4X
C119 *0.047U/10V_4X

SMDDR_VREF_DQ0
C62 0.1U/10V_4X
C66 2.2U/6.3V_6X

SMDDR_VREF_DIMM
C152 0.1U/10V_4X
C158 2.2U/6.3V_6X
C155 *0.047U/10V_4X

+3V
C198 2.2U/6.3V_6X
C197 *0.1U/10V_4X
C196 *0.047U/10V_4X

+SMDDR_VTERM
C210 1U/6.3V_4X
C209 1U/6.3V_4X
C203 1U/6.3V_4X
C211 1U/6.3V_4X
C207 4.7U/6.3V_6X

C170 470P/50V_4X R62 *short_4 SMDDR_VREF_DIMM {15}
R60 *10K/F_4 R59 *10K/F_4 +1.5VSUS
+SMDDR_VREF

+1.5VSUS
R36 1K/F_4
SMDDR_VREF_DQ0
R32 1K/F_4 C70 0.1U/10V_4X C72 *0.047U/10V_4X

+1.5VSUS
+ C112 *330U/2.5V_7343P_E9a

+SMDDR_VTERM
R82 22_4
{8,42} MAINON_ON_G
Q11 2N7002_200MA

Quanta Computer Inc.
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	DDR3 DIMM-0	A1A
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H=8

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRSK-20401-TP8D

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRSK-20401-TP8D

B2A

Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603

It can cost down 30%

+1.5VSUS

C129 4.7U/6.3V_6X
C111 4.7U/6.3V_6X
C147 4.7U/6.3V_6X
C133 4.7U/6.3V_6X
C146 4.7U/6.3V_6X
C117 4.7U/6.3V_6X
C121 0.1U/10V_4X
C122 0.1U/10V_4X
C113 0.1U/10V_4X
C118 0.1U/10V_4X
C134 0.1U/10V_4X
C126 *0.047U/10V_4X
C130 *0.047U/10V_4X

SMDDR_VREF_DIMM

C164 0.1U/10V_4X
C168 2.2U/6.3V_6X
C156 *0.047U/10V_4X

SMDDR_VREF_DQ1

C60 0.1U/10V_4X
C57 2.2U/6.3V_6X

+3V

C199 2.2U/6.3V_6X
C202 *0.1U/10V_4X
C201 *0.047U/10V_4X

+SMDDR_VTERM

C204 1U/6.3V_4X
C205 1U/6.3V_4X
C208 1U/6.3V_4X
C206 1U/6.3V_4X
C212 4.7U/6.3V_6X

+1.5VSUS

R31 1K/F_4
SMDDR_VREF_DQ1
R7035 1K/F_4
C64 0.1U/10V_4X
C67 *0.047U/10V_4X

+1.5VSUS

C108 *330U/2.5V_7343P_E9a

Quanta Computer Inc.		
PROJECT : TE4		
Size	Document Number: DDR3 DIMM-1	Rev: A1A
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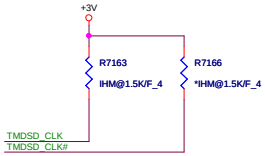
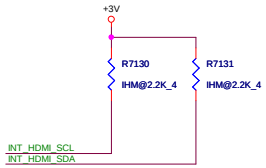
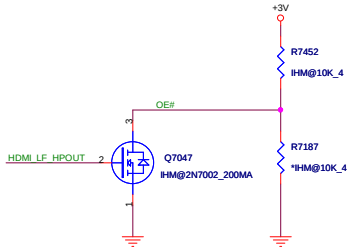
Display Port Enable [HDM]



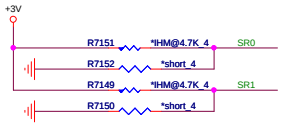
I2C PU

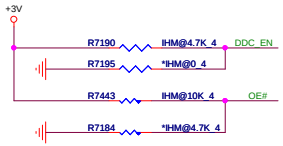


LEVEL SHIFT ENABLE



LEVEL SHIFT SETTING



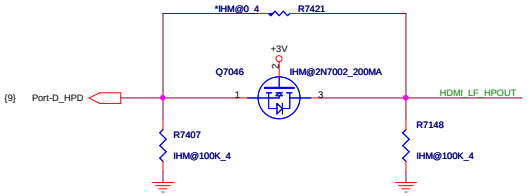


Slew Rate Control Function

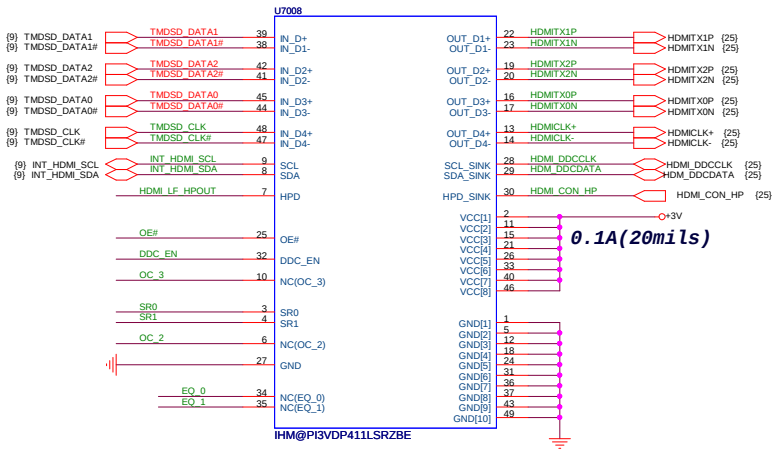
SR1	SR0	Rise/Fall Time
1	1	140ps
1	0	130ps
0	1	120ps
0	0	110ps

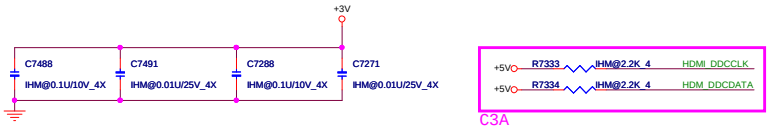
Reserve

Hot Plug Detector (UMA)



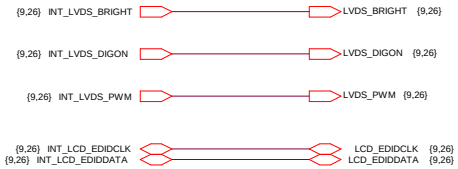
HDMI LEVEL SHIFT (UMA)

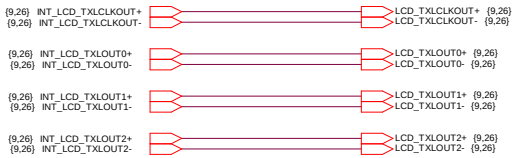




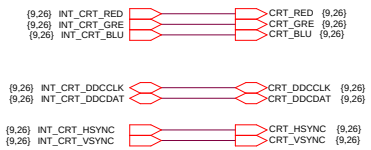
C3A

LVDS (UMA)





CRT (UMA)



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Quanta Computer Inc.
PROJECT : TE4

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HDMI Conn [HDM]

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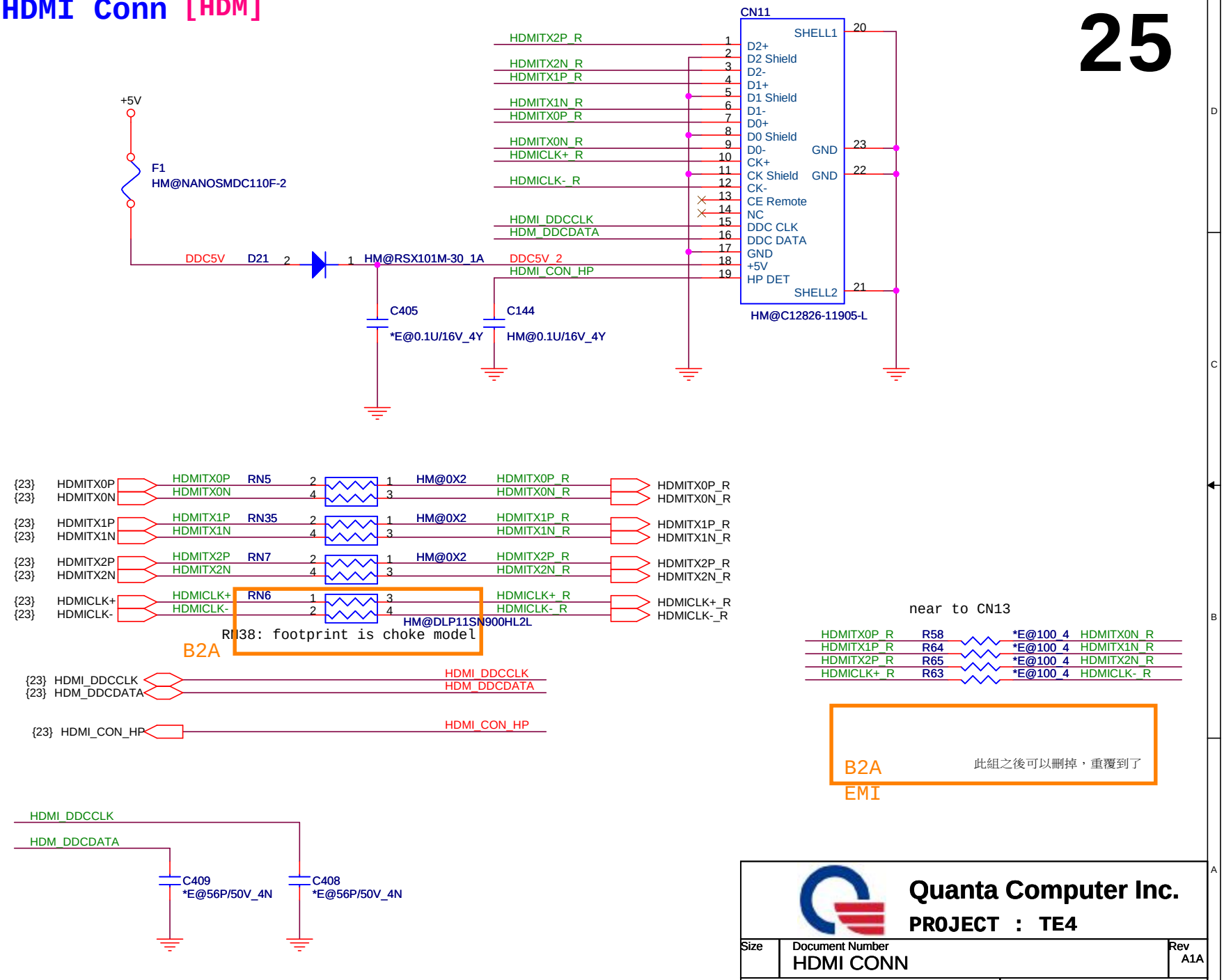

Quanta Computer Inc.		
PROJECT : TE4		
Size	Document Number: HDMI CONN	Rev: A1A
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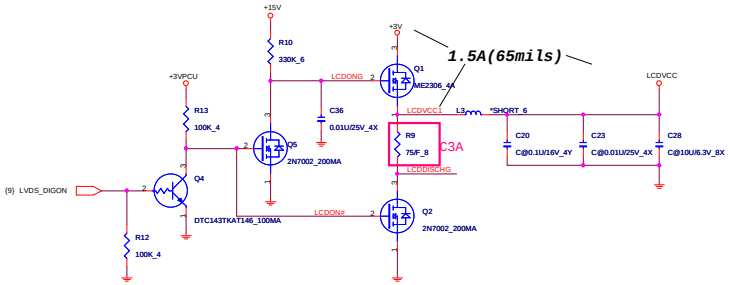
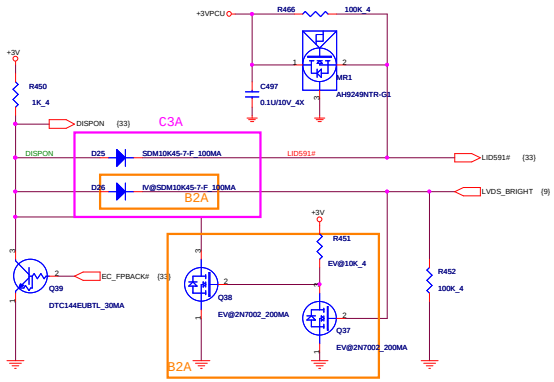
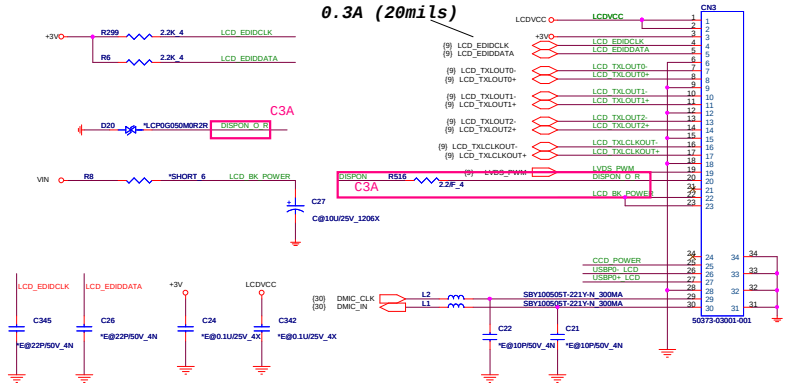
LCD POWER SWITCH
<LDS>



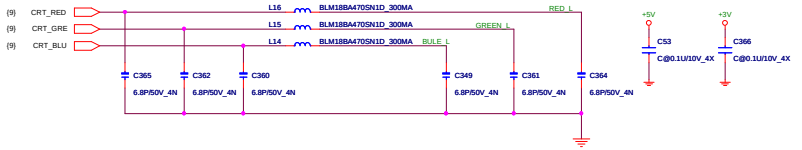
HALL Sensor
<HSR>



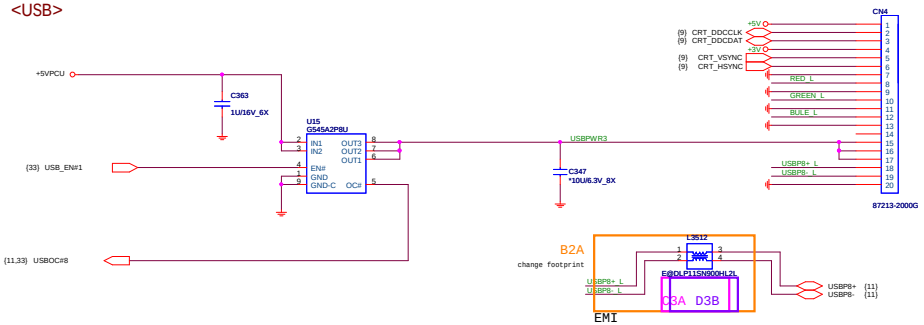
LCD Panel Module
[LDS]



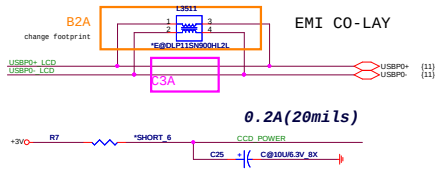
CRT
<CRT>



USB for CRT BOARD (Right) <USB>



CCD
[CCD]



Quanta Computer Inc.
PROJECT : TE4
Size
Document Number
LCD/LED Panel/CCD
Rev
A1A
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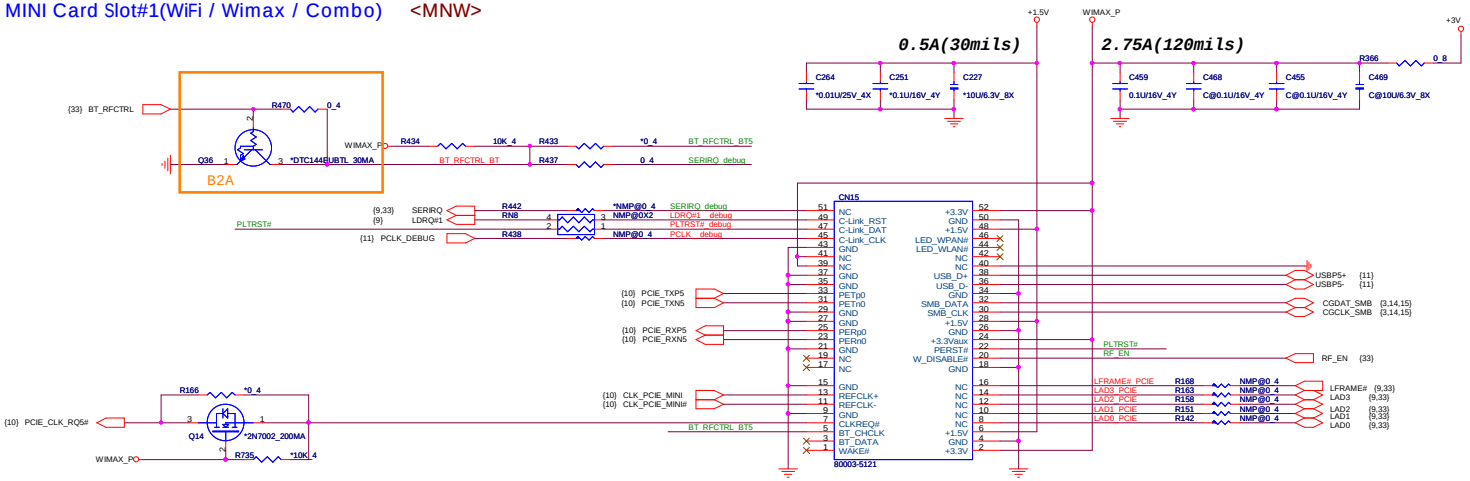
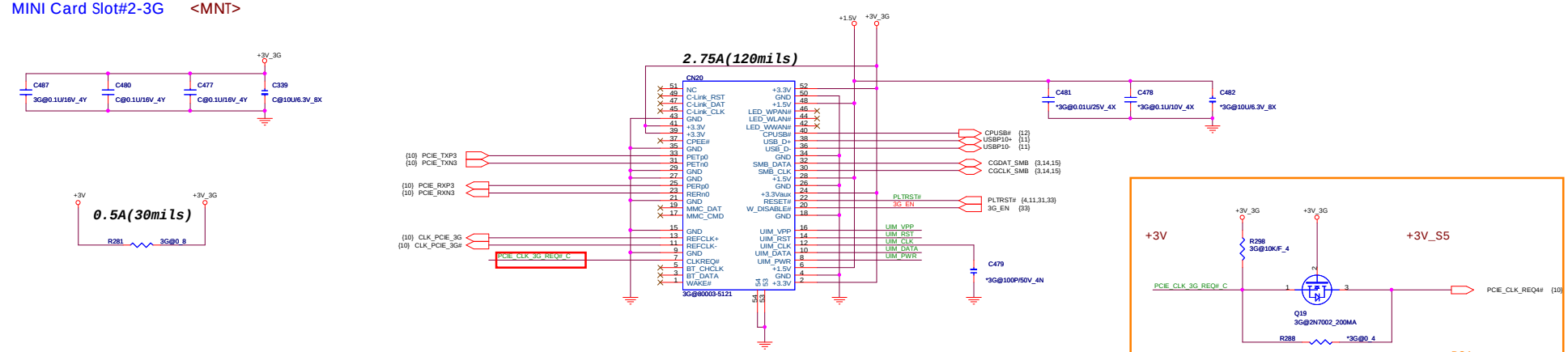
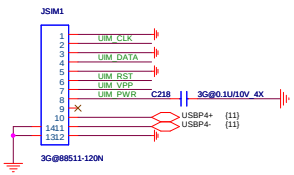
MINI Card Slot#1(WiFi / Wimax / Combo) <MNW>



MINI Card Slot#2-3G <MNT>



SIM CARD



Quanta Computer Inc.
PROJECT : TE4D
Size: Document Number: MINI CARD(WLAN/3G/SIM Card) Rev: A1A
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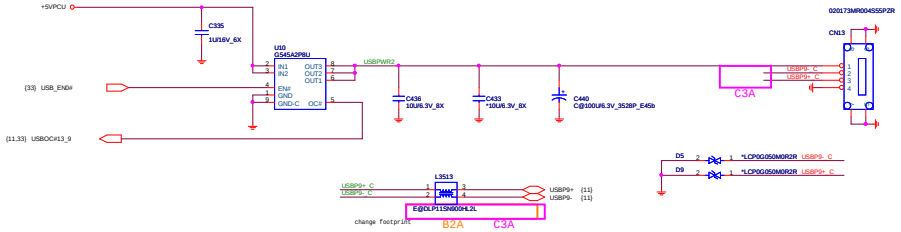
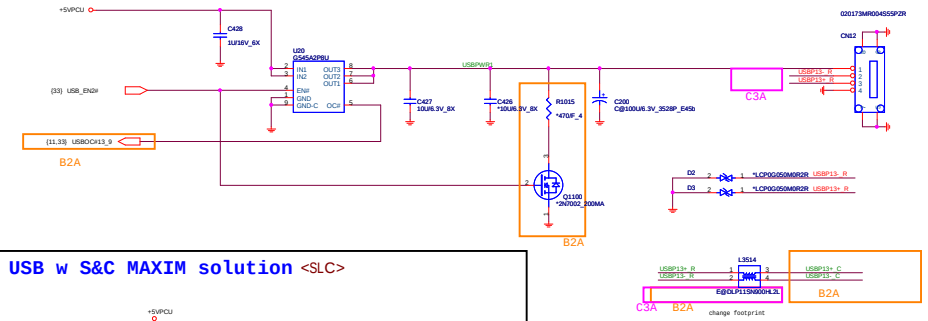
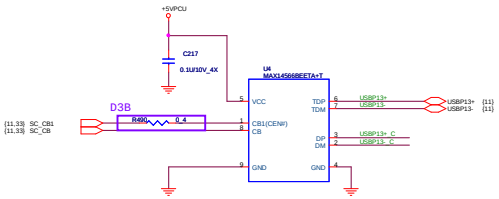
USB2.0 MB SIDE (Left) 1 <USB>



USB2.0 MB SIDE (Left) 2 <USB>

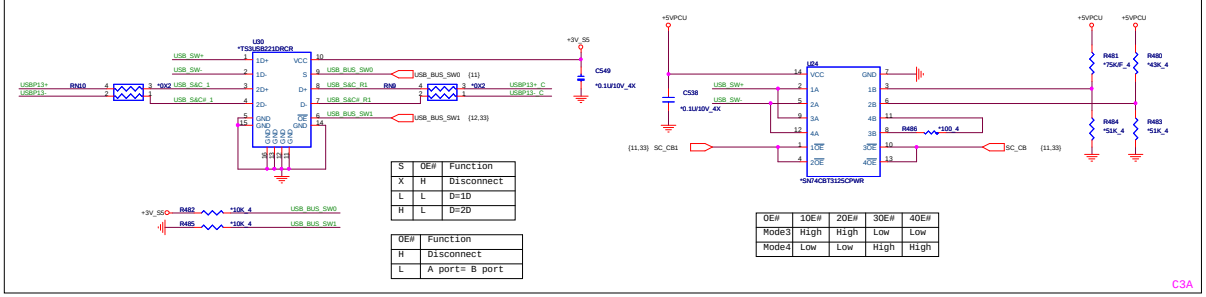


USB w S&C MAXIM solution <SLC>



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

USB w S&C TI solution <SLC>



S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

OE#	Function
H	Disconnect
L	A port= B port

OE#	1OE#	2OE#	3OE#	4OE#
Mode3	High	High	Low	Low
Mode4	Low	Low	High	High

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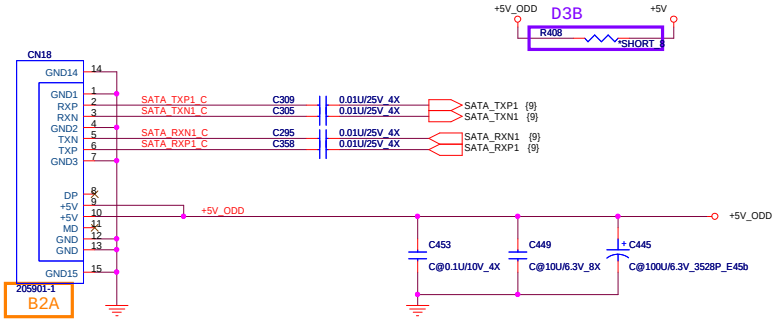
SATA ODD

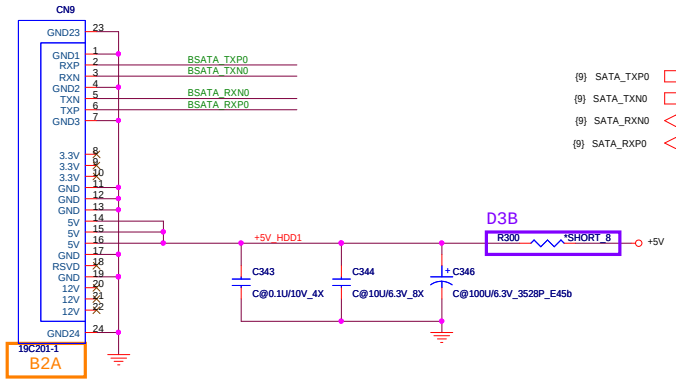
[ODD]

ODD Zero power . (Only for Intel)<OZP>

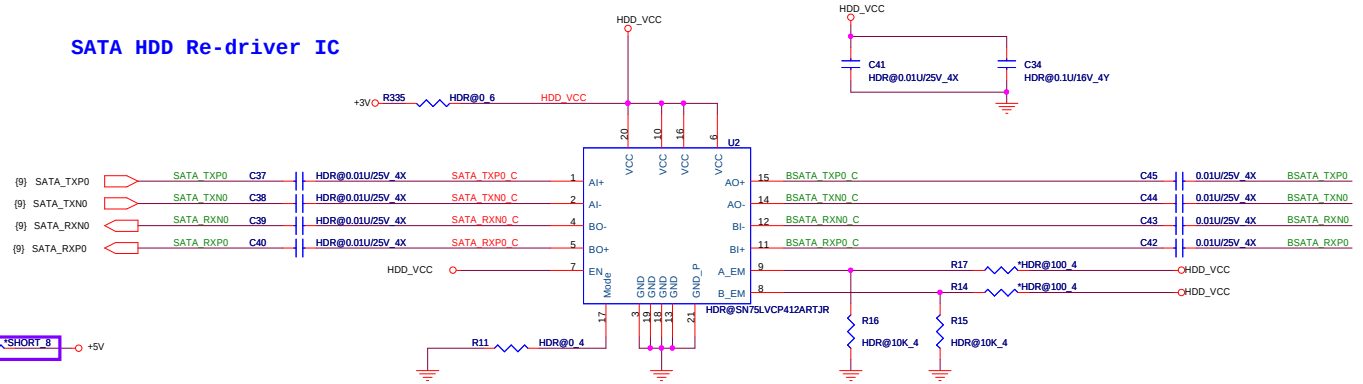


SATA HDD

[HDD]

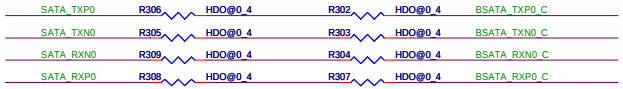


SATA HDD Re-driver IC



SATA Re-driver Bypass

Colay with Redriver IC



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Size	Document Number	Rev
	HDD/ODD/MDC	A1A

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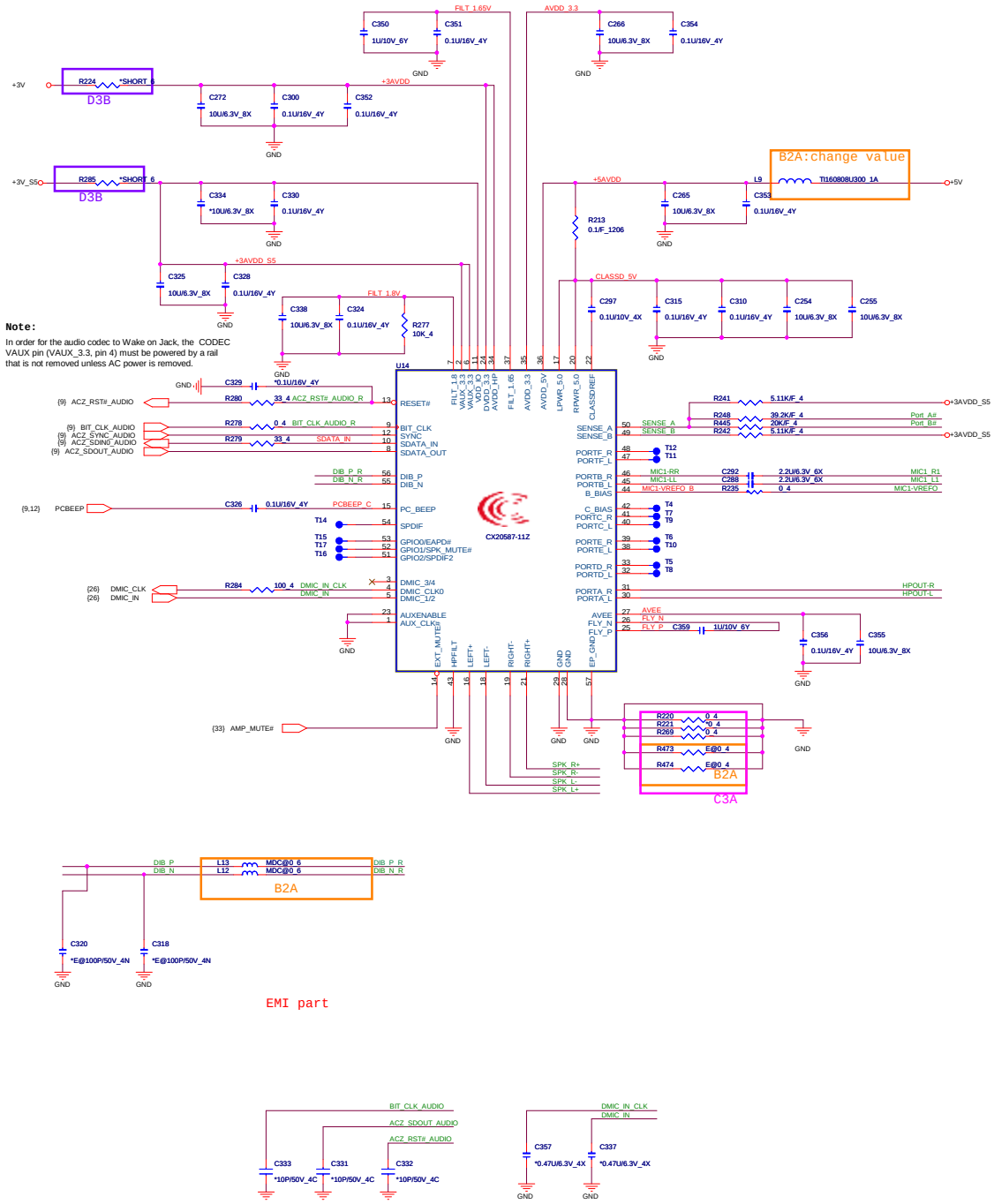
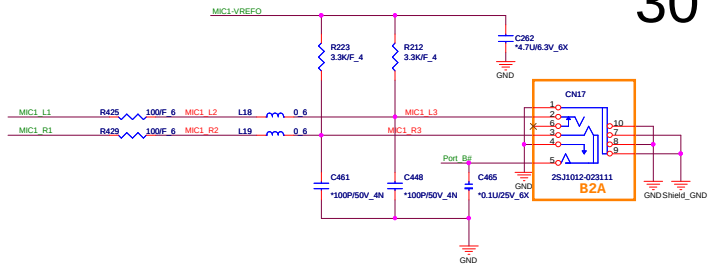
Codec(CX20587-11Z) <ADO/MDC/AMP>



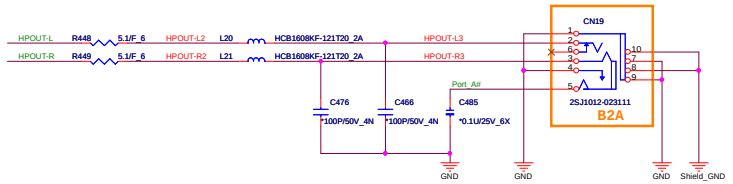
Note:

In order for the audio codec to Wake on Jack, the CODEC VAUX pin (VAUX_3.3, pin 4) must be powered by a rail that is not removed unless AC power is removed.

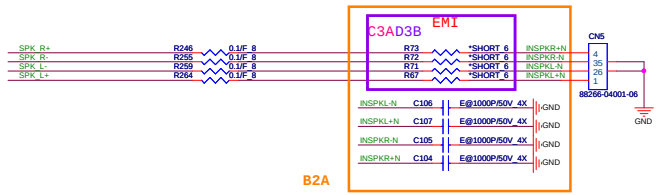
EXT MIC <ADO/AMP>



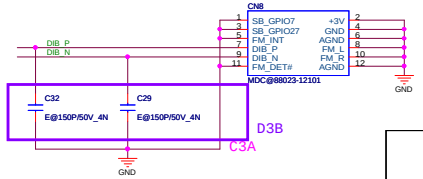
EXT H.P / Beats <ADO/AMP>



INT SPK <ADO/AMP>



MDC <MDC>



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	Codec (CX20587)	A1A
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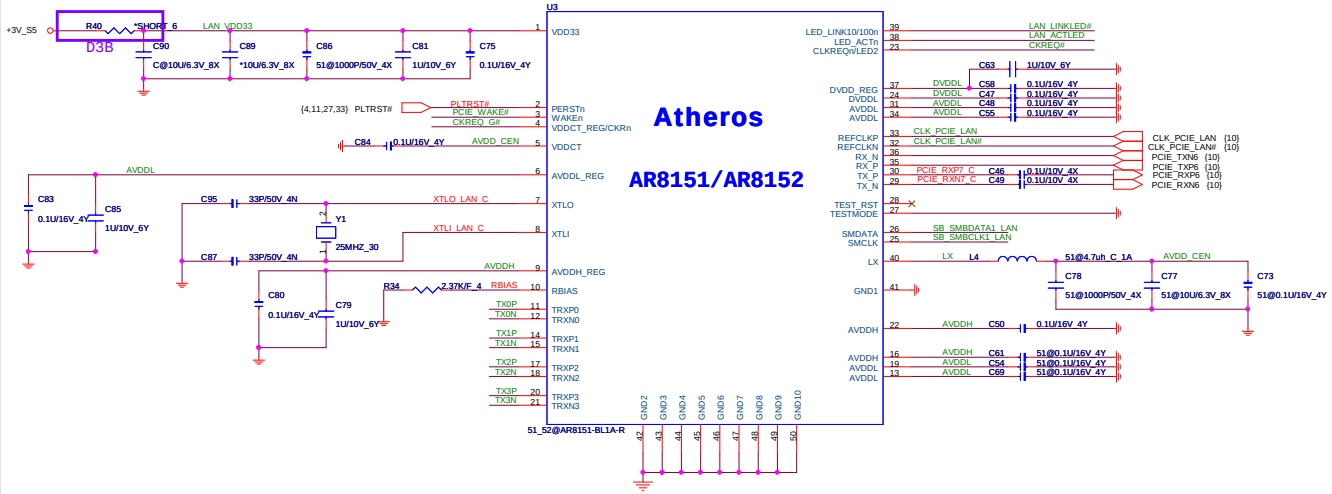
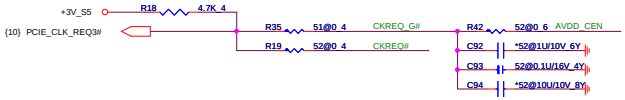
Atheros Lan <LAN/LN1/LNG>



GIGA:AR8151-BL1A-R = AL008151005

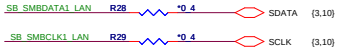
10/100:AR8152-BL1A-R = AL008152009

31



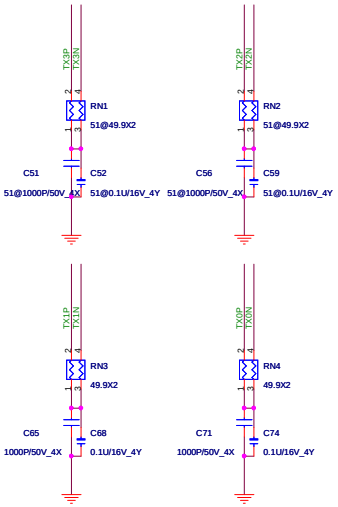
LAN-Wake up function<LAN>

LAN-SM-Bus <LAN>

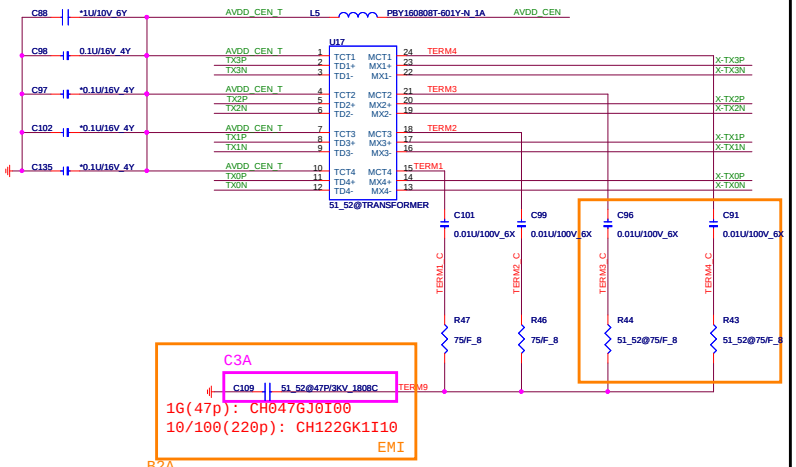


LAN-terminator<LAN/LN1/LNG>

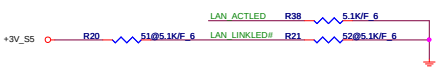
PLACE NEAR LAN IC SIDE



LAN-Transformer <LAN/LN1/LNG>

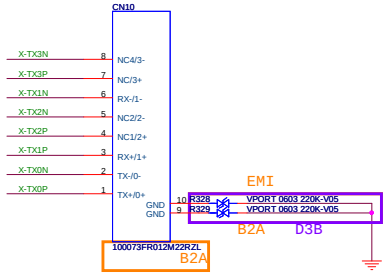


LAN-Strap function <LAN/LN1/LNG>



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

LAN(RJ45)-CONN Interface <LAN>



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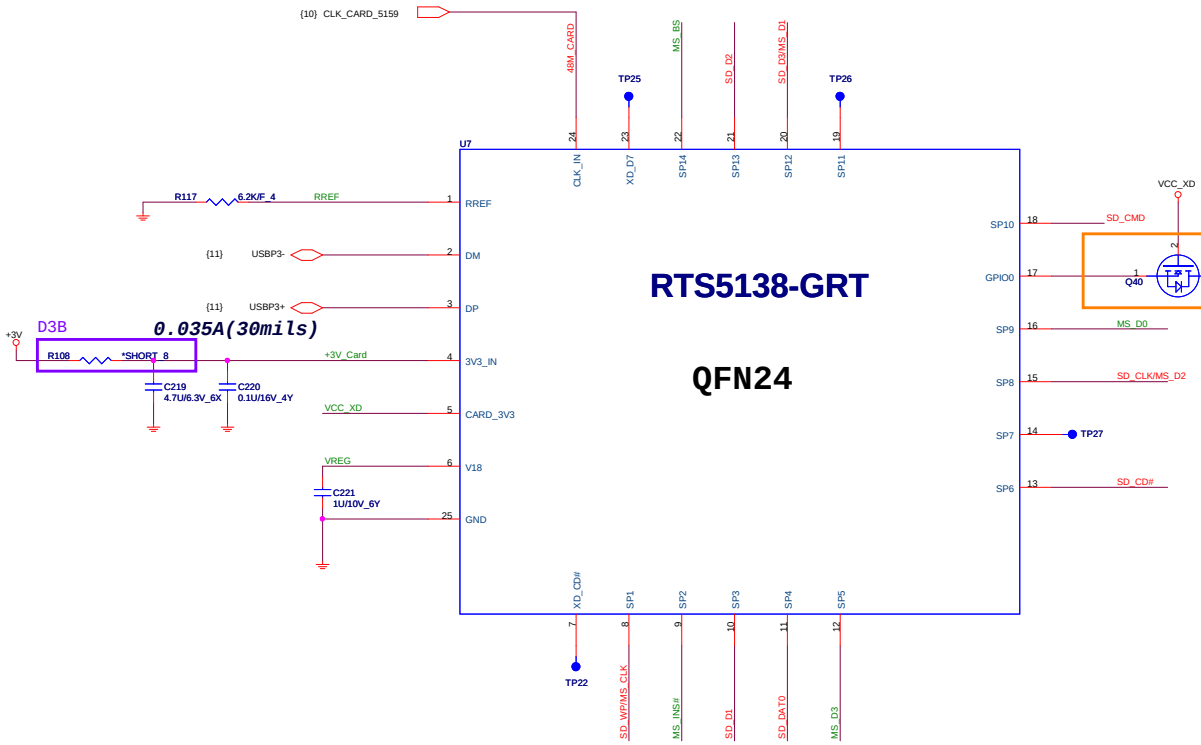
3 IN 1 CARD READER

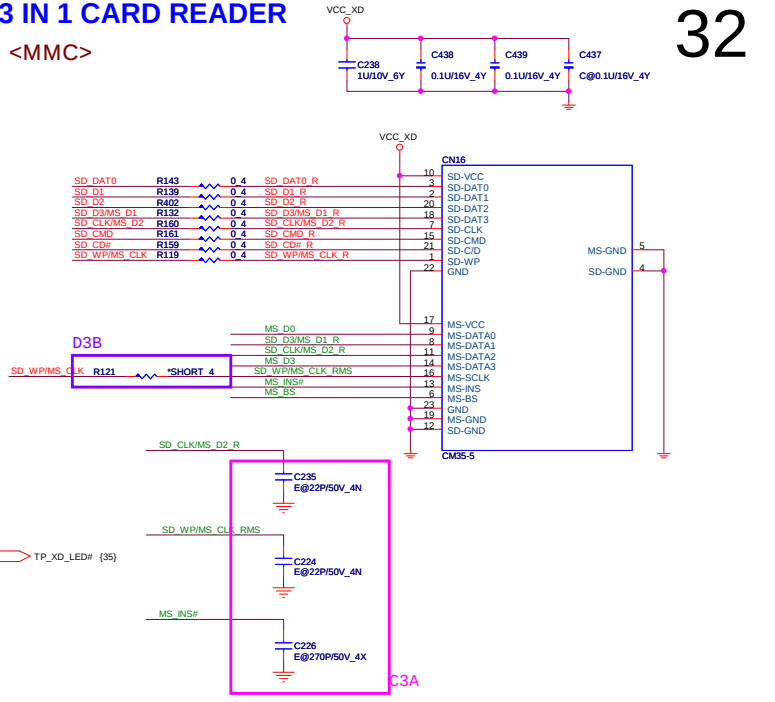
Card reader controller <MMC>



3 IN 1 CARD READER

<MMC>

32



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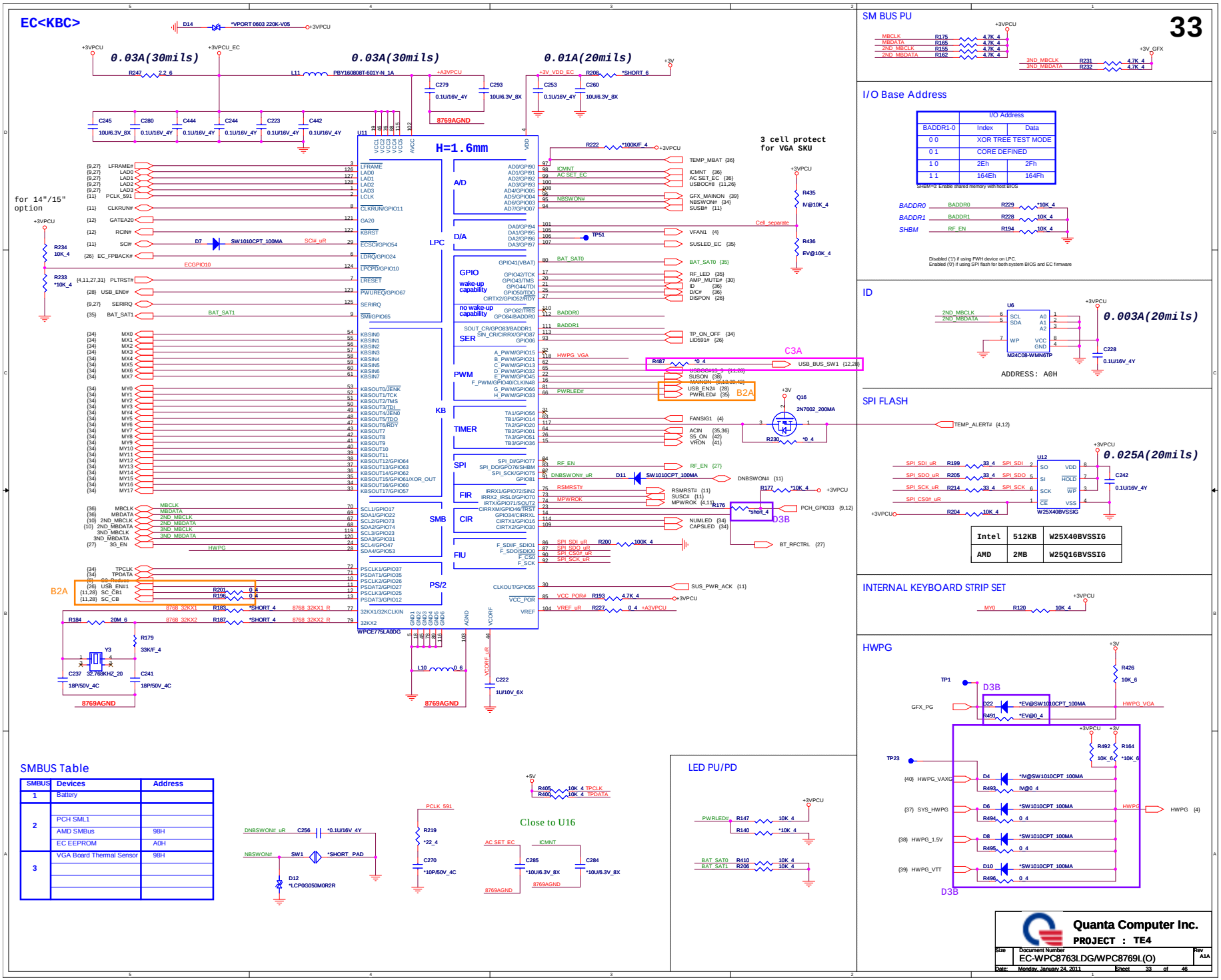

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	AMD SMBus	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

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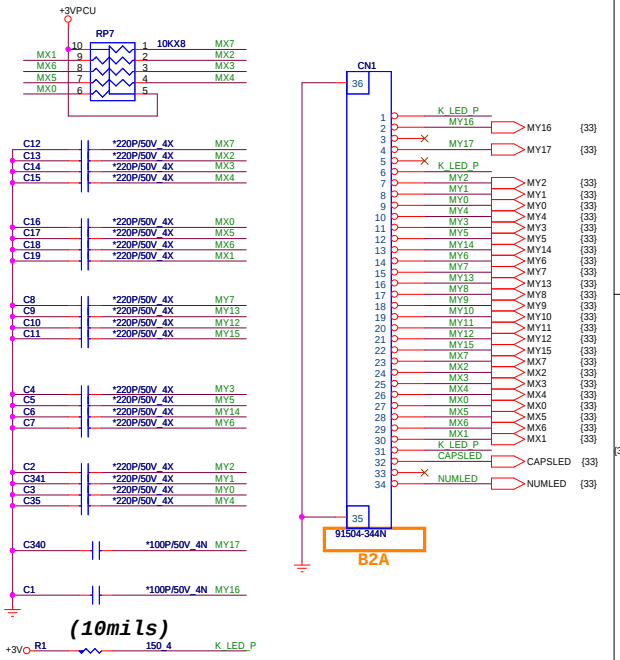
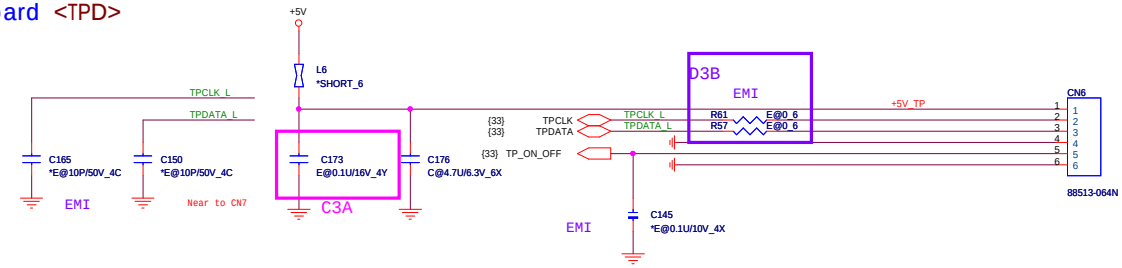
INT KeyBoard <KBC>



TP board <TPD>



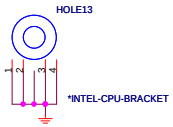
Power board <PSW>

K/B LED power <KBP>

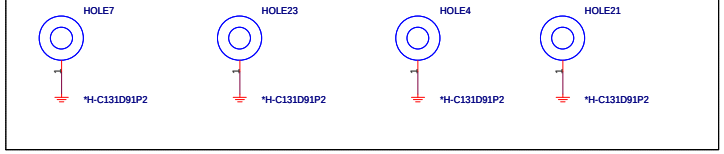
Only for Huron River

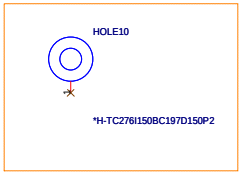
HOLE

CPU



HDD&ODD

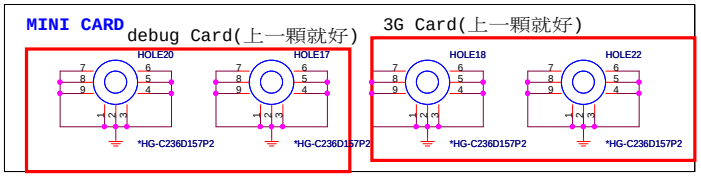




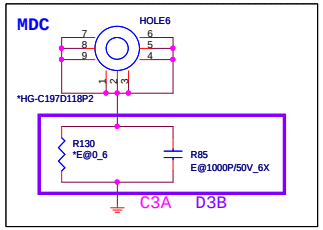
MINI CARD

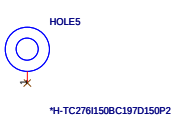
debug Card(上一顆就好)

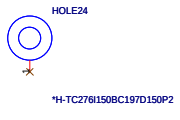
3G Card(上一顆就好)

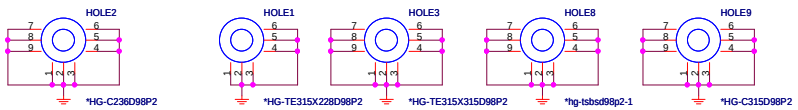


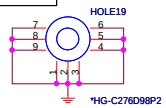
MDC

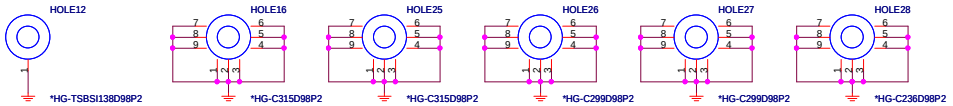


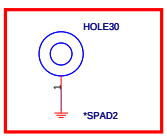


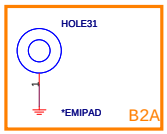












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	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	A1A
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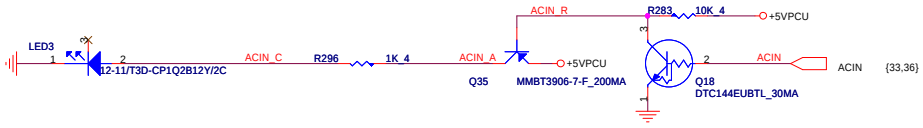
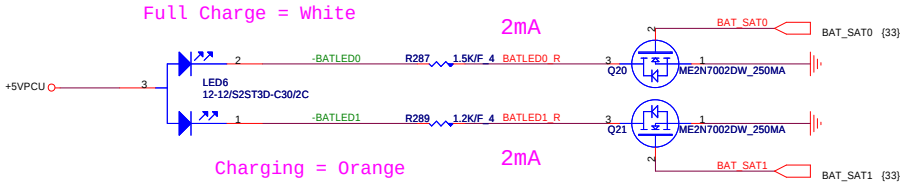
LED

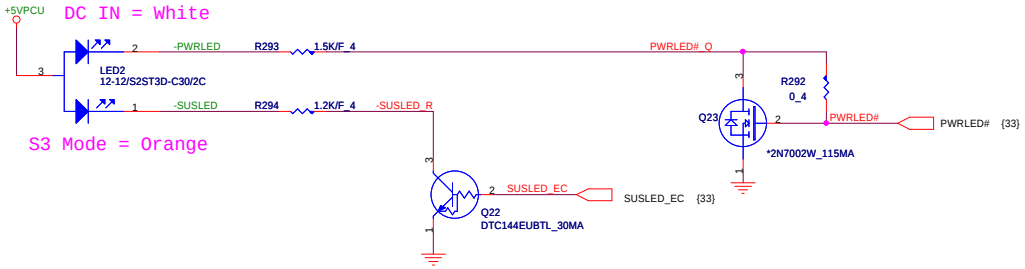
AC-IN



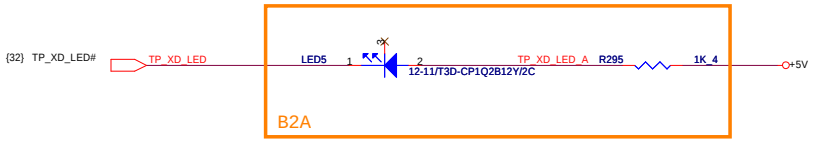
BATERRY



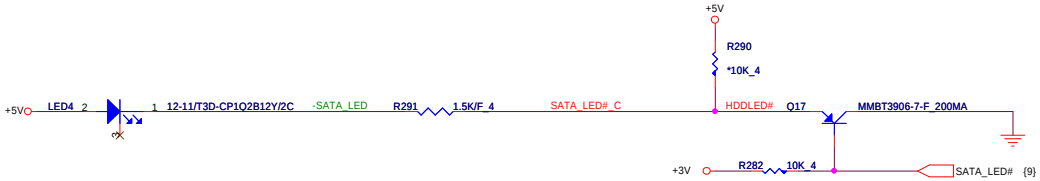
POWER



CARDREADER

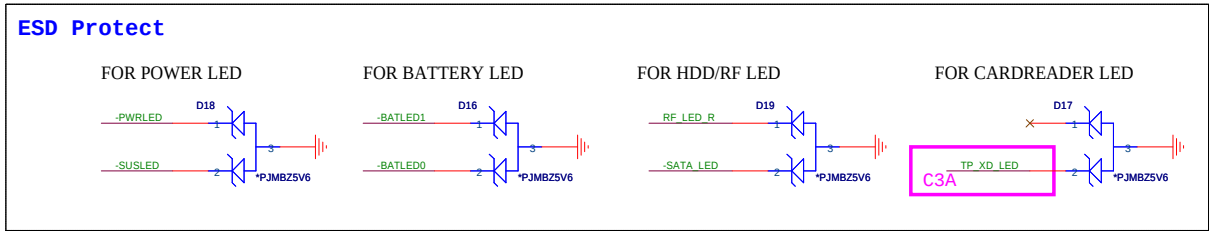


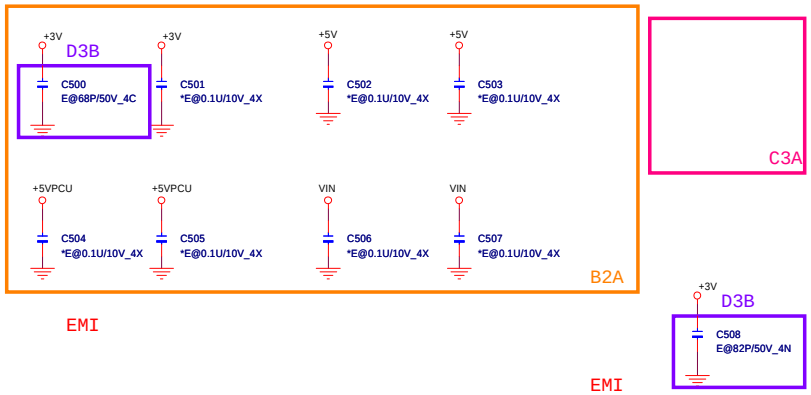
HDD/ODD



RF LED

ESD Protect





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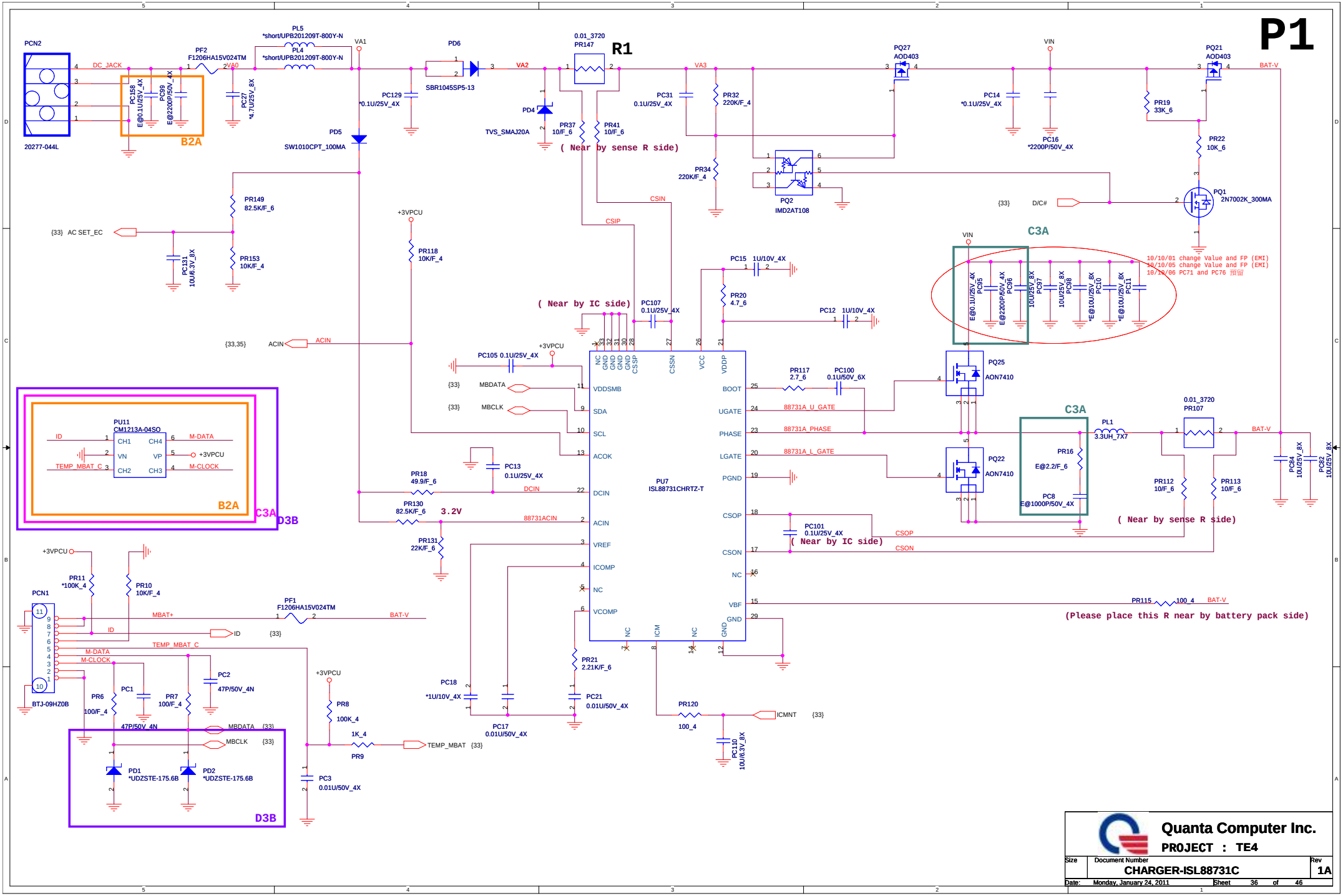
P1
PCN2
20277-044L
DC_JACK
PF2
F1206HA15V024TM
PL5
*short/UPB201209T-800Y-N
PL4
*short/UPB201209T-800Y-N
VA1
VA0
B2A
PC158
E@0.1U/25V_4X
PC99
E@220P/50V_4X
PC27
*4.7U/25V_8X
PD6
SBR1045SP5-13
VA2
PD4
TVS_SMAJ20A
PD5
SW1010CPT_100MA
PC129
*0.1U/25V_4X
0.01_3720
PR147
R1
PR37
10/F_6
PR41
10/F_6
(Near by sense R side)
VA3
PC31
0.1U/25V_4X
PR32
220K/F_4
PR34
220K/F_4
PQ2
IMD2AT108
PQ27
AOD403
VIN
PC14
*0.1U/25V_4X
PC16
*2200P/50V_4X
PQ21
AOD403
BAT-V
PR19
33K_6
PR22
10K_6
PQ1
2N7002K_300MA
{33} D/C#
PR149
82.5K/F_6
{33} AC SET_EC
PC131
10U/6.3V_8X
PR153
10K/F_4
+3VPCU
PR118
10K/F_4
CSIN
CSIP
(Near by IC side)
PC107
0.1U/25V_4X
PC15 1U/10V_4X
PR20
4.7_6
PC12 1U/10V_4X
C3A
VIN
E@0.1U/25V_4X
PC95
E@2200P/50V_4X
PC96
10U/25V_8X
PC97
10U/25V_8X
PC98
*E@10U/25V_8X
PC10
*E@10U/25V_8X
PC11
10/10/01 change Value and FP (EMI)
10/10/05 change Value and FP (EMI)
10/10/06 PC71 and PC76 預留
{33,35} ACIN
ACIN
PC105 0.1U/25V_4X
+3VPCU
{33} MBDATA
{33} MBCLK
PU7
ISL88731CHRTZ-T
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
NC
ICM
NC
GND
PR117
2.7_6
PC100
0.1U/50V_6X
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ25
AON7410
PQ22
AON7410
C3A
PL1
3.3UH_7X7
0.01_3720
PR107
BAT-V
PR16
E@2.2/F_6
PC8
E@1000P/50V_4X
PR112
10/F_6
PR113
10/F_6
PC84
10U/25V_8X
PC82
10U/25V_8X
(Near by sense R side)
PC13
0.1U/25V_4X
DCIN
PR18
49.9/F_6
PR130
82.5K/F_6
3.2V
88731ACIN
PR131
22K/F_6
PC101
0.1U/25V_4X
(Near by IC side)
CSOP
CSON
PR115
100_4
BAT-V
(Please place this R near by battery pack side)
PR21
2.21K/F_6
PC21
0.01U/50V_4X
PC18
*1U/10V_4X
PC17
0.01U/50V_4X
PR120
100_4
ICMNT {33}
PC110
10U/6.3V_8X
+3VPCU
PR11
*100K_4
PR10
10K/F_4
PCN1
BTJ-09HZ0B
MBAT+
PF1
F1206HA15V024TM
BAT-V
ID
{33}
TEMP_MBAT_C
M-DATA
M-CLOCK
PC2
47P/50V_4N
PR6
100/F_4
PC1
PR7
100/F_4
47P/50V_4N
MBDATA {33}
MBCLK {33}
PD1
*UDZSTE-175.6B
PD2
*UDZSTE-175.6B
D3B
+3VPCU
PR8
100K_4
1K_4
PR9
TEMP_MBAT {33}
PC3
0.01U/50V_4X
PU11
CM1213A-04SO
ID
TEMP_MBAT_C
CH1
VN
CH2
CH4
VP
CH3
M-DATA
+3VPCU
M-CLOCK
B2A
C3A
D3B
Quanta Computer Inc.
PROJECT : TE4
Size
Document Number
CHARGER-ISL88731C
Rev
1A
Date: Monday, January 24, 2011
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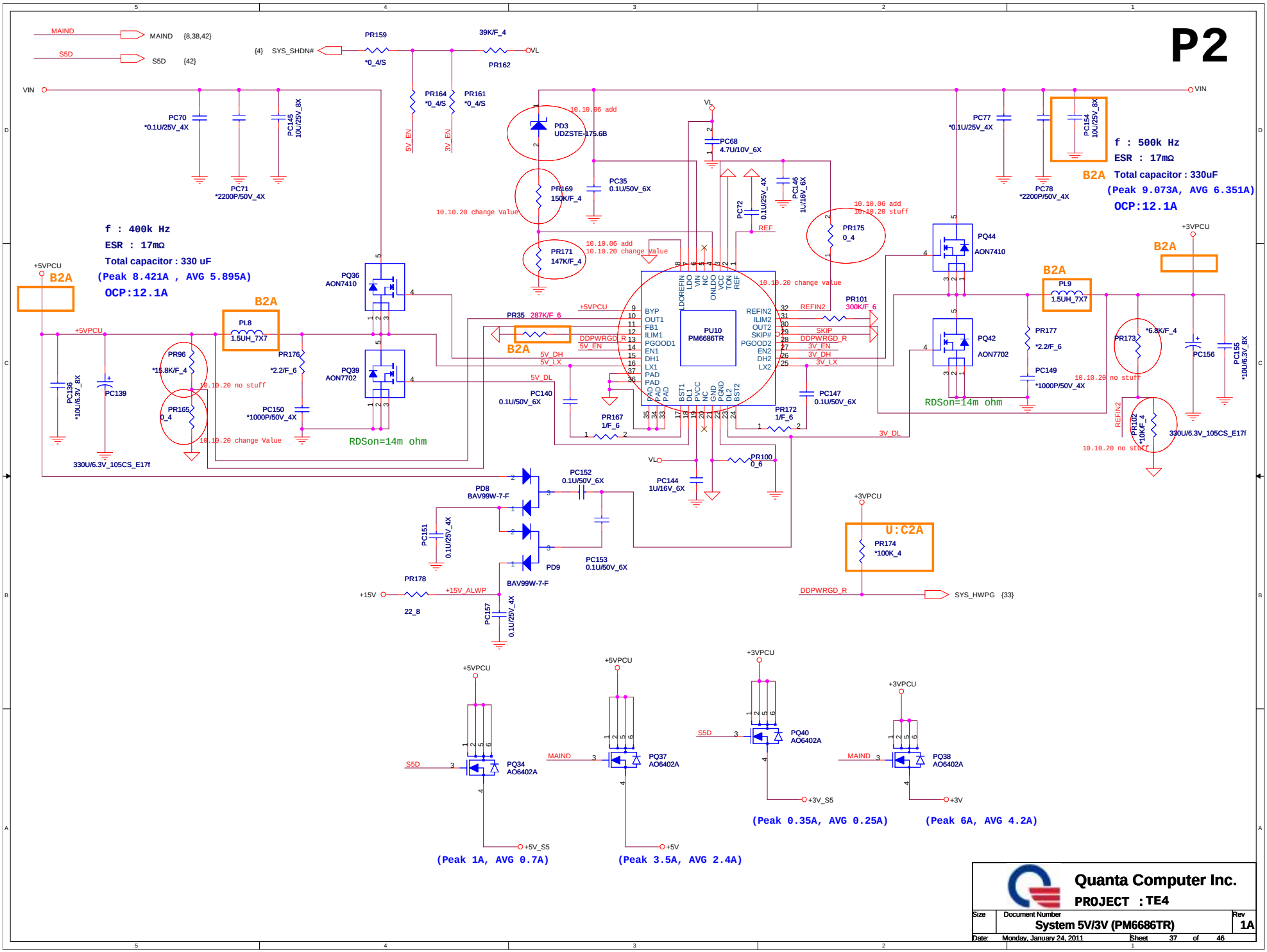
P2
MAIND {8,38,42}
S5D {42}
{4} SYS_SHDN#
PR159 *0_4/S
39K/F_4
PR162
VL
VIN
PC70 *0.1U/25V_4X
PC71 *2200P/50V_4X
PC145 10U/25V_8X
PR164 *0_4/S
PR161 *0_4/S
5V_EN
3V_EN
10.10.06 add
PD3 UDZSTE-175.6B
PC68 4.7U/10V_6X
PR169 150K/F_4
PC35 0.1U/50V_6X
10.10.20 change Value
PC72 0.1U/25V_4X
PC146 1U/16V_6X
REF
10.10.06 add
10.10.20 change Value
PR171 147K/F_4
10.10.06 add
10.10.20 stuff
PR175 0_4
PC77 *0.1U/25V_4X
PC78 *2200P/50V_4X
PC154 10U/25V_8X
f : 500k Hz
ESR : 17mΩ
B2A Total capacitor : 330uF
(Peak 9.073A, AVG 6.351A)
OCP:12.1A
f : 400k Hz
ESR : 17mΩ
Total capacitor : 330 uF
(Peak 8.421A , AVG 5.895A)
OCP:12.1A
+5VPCU
B2A
PL8 1.5UH_7X7
PQ36 AON7410
PQ39 AON7702
PR96 *15.8K/F_4
PR165 0_4
PR176 *2.2/F_6
10.10.20 no stuff
10.10.20 change Value
PC136 *10U/6.3V_8X
PC139
330U/6.3V_105CS_E17f
PC150 *1000P/50V_4X
RDSon=14m ohm
PR35 287K/F_6
DDPWRGD_R
5V_EN
5V_DH
5V_LX
5V_DL
PU10 PM6686TR
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
SKIP
3V_EN
3V_DH
3V_LX
PR101 300K/F_6
PC140 0.1U/50V_6X
PR167 1/F_6
PC147 0.1U/50V_6X
PR172 1/F_6
3V_DL
PR100 0_6
PC144 1U/16V_6X
PQ44 AON7410
PQ42 AON7702
PR177 *2.2/F_6
PC149 *1000P/50V_4X
PL9 1.5UH_7X7
PR173 *6.8K/F_4
PC156
PC155 *10U/6.3V_8X
330U/6.3V_105CS_E17f
PR102 *10K/F_4
PD8 BAV99W-7-F
PD9 BAV99W-7-F
PC152 0.1U/50V_6X
PC153 0.1U/50V_6X
PC151 0.1U/25V_4X
PR178 22_8
+15V
+15V_ALWP
PC157 0.1U/25V_4X
U:C2A
PR174 *100K_4
SYS_HWPG {33}
PQ34 AO6402A
PQ37 AO6402A
PQ40 AO6402A
PQ38 AO6402A
+5V_S5
+5V
+3V_S5
+3V
(Peak 1A, AVG 0.7A)
(Peak 3.5A, AVG 2.4A)
(Peak 0.35A, AVG 0.25A)
(Peak 6A, AVG 4.2A)
Quanta Computer Inc.
PROJECT : TE4
Size
Document Number
System 5V/3V (PM6686TR)
Rev 1A
Date: Monday, January 24, 2011
Sheet 37 of 46

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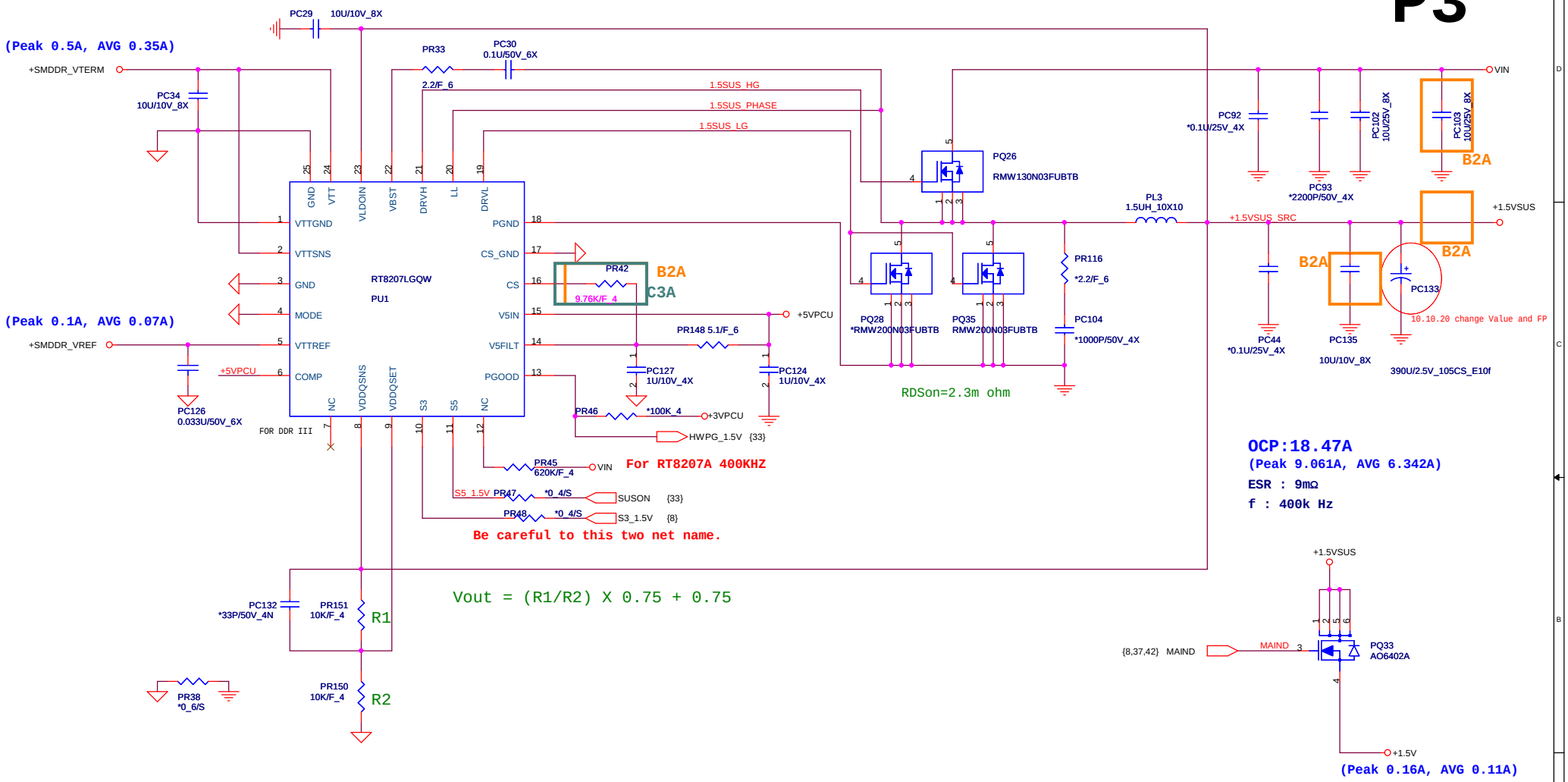
P3



Quanta Computer Inc.		
PROJECT : TE4		
Size	Document Number: DDR 1.5V(RT8207L)/1.05VSUS	Rev 1A
Date: Monday, January 24, 2011	Sheet 38 of 46	

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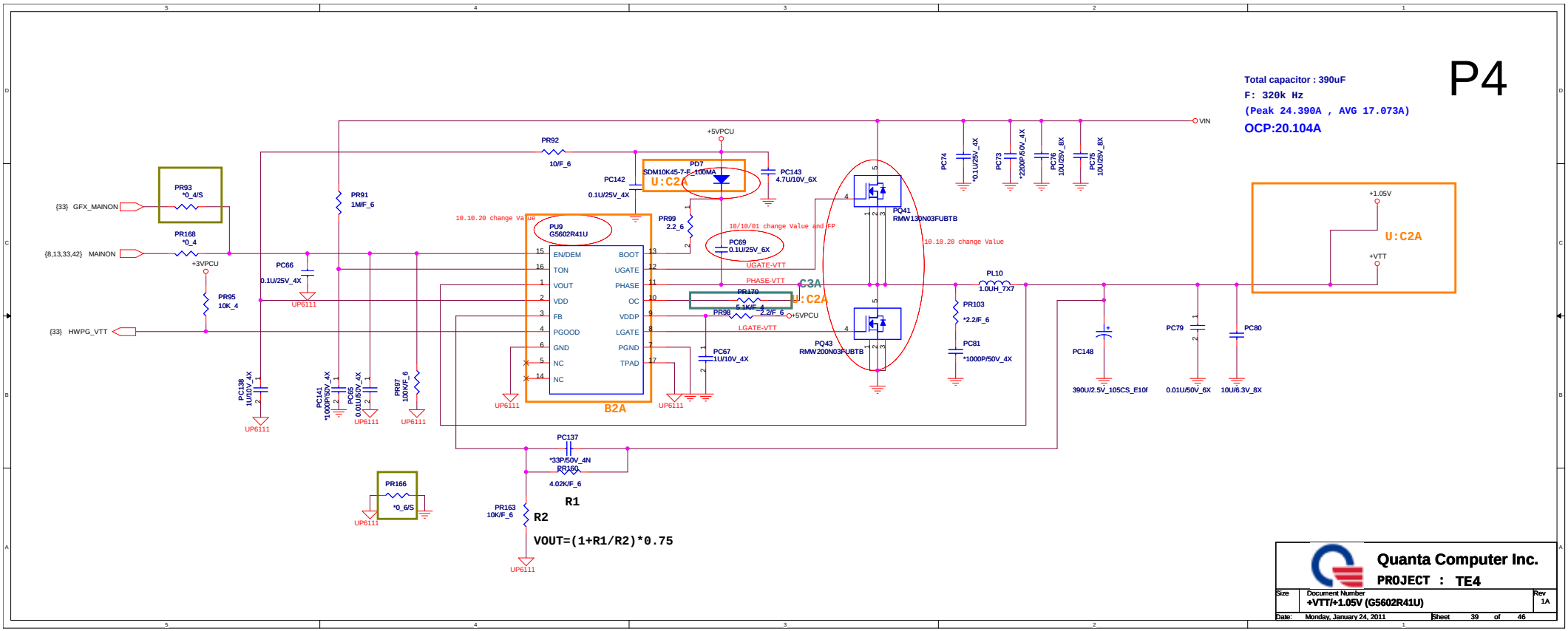
P4
Total capacitor : 390uF
F: 320k Hz
(Peak 24.390A , AVG 17.073A)
OCP:20.104A
VOUT=(1+R1/R2)*0.75
R1
R2
B2A
U:C2A
C3A
Quanta Computer Inc.
PROJECT : TE4
+VTT/+1.05V (G5602R41U)
Monday, January 24, 2011
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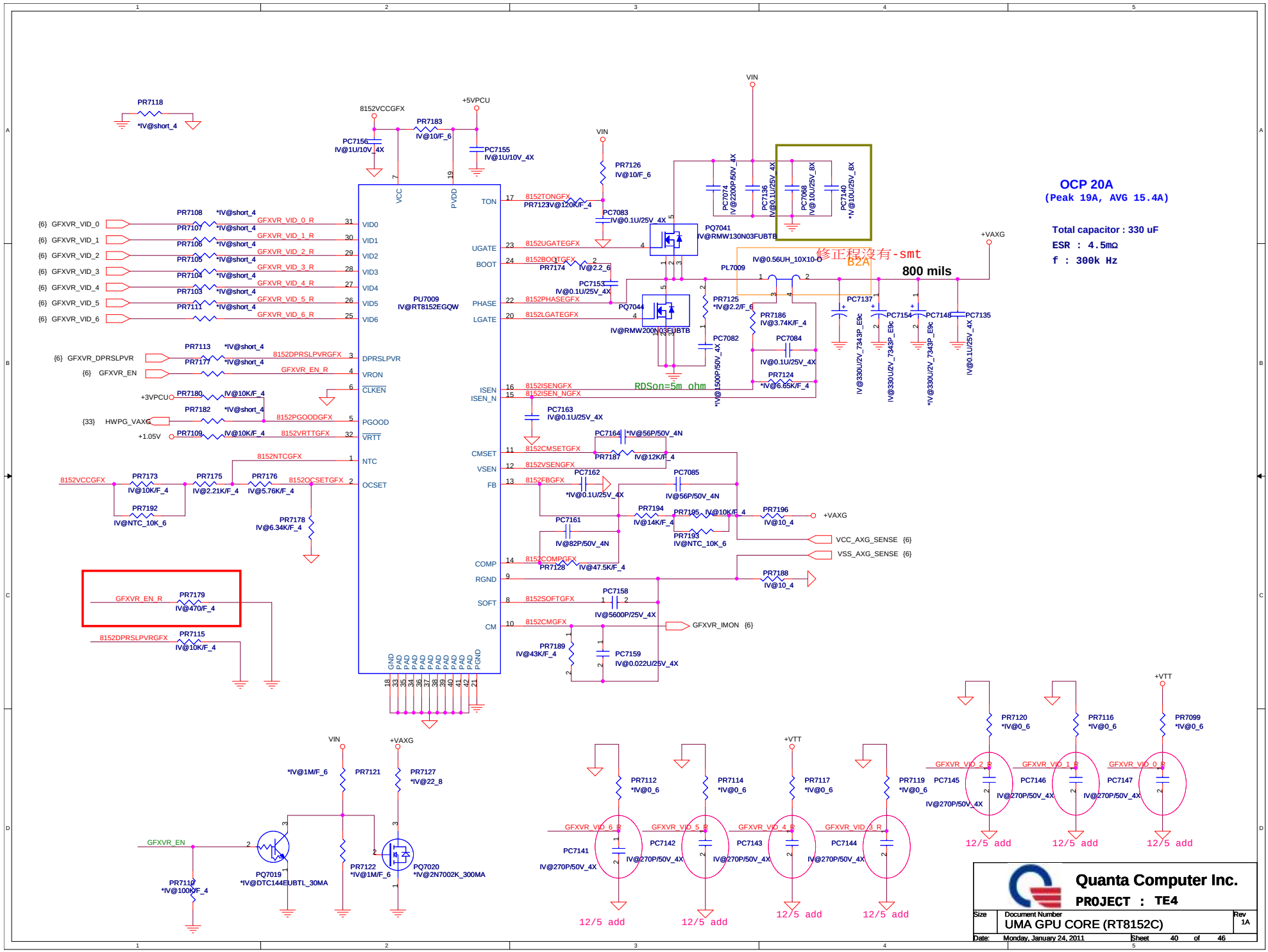
OCP 20A
(Peak 19A, AVG 15.4A)
Total capacitor : 330 uF
ESR : 4.5mΩ
f : 300k Hz
800 mils
修正程沒有-smt
B2A
RDSon=5m ohm
PU7009
IV@RT8152EGQW
PQ7041
IV@RMW130N03FUBTB
PQ7044
IV@RMW200N03FUBTB
PL7009
IV@0.56UH_10X10-D
PQ7019
*IV@DTC144EUBTL_30MA
PQ7020
*IV@2N7002K_300MA
12/5 add
Quanta Computer Inc.
PROJECT : TE4
Document Number
UMA GPU CORE (RT8152C)
Rev 1A
Date: Monday, January 24, 2011
Sheet 40 of 46

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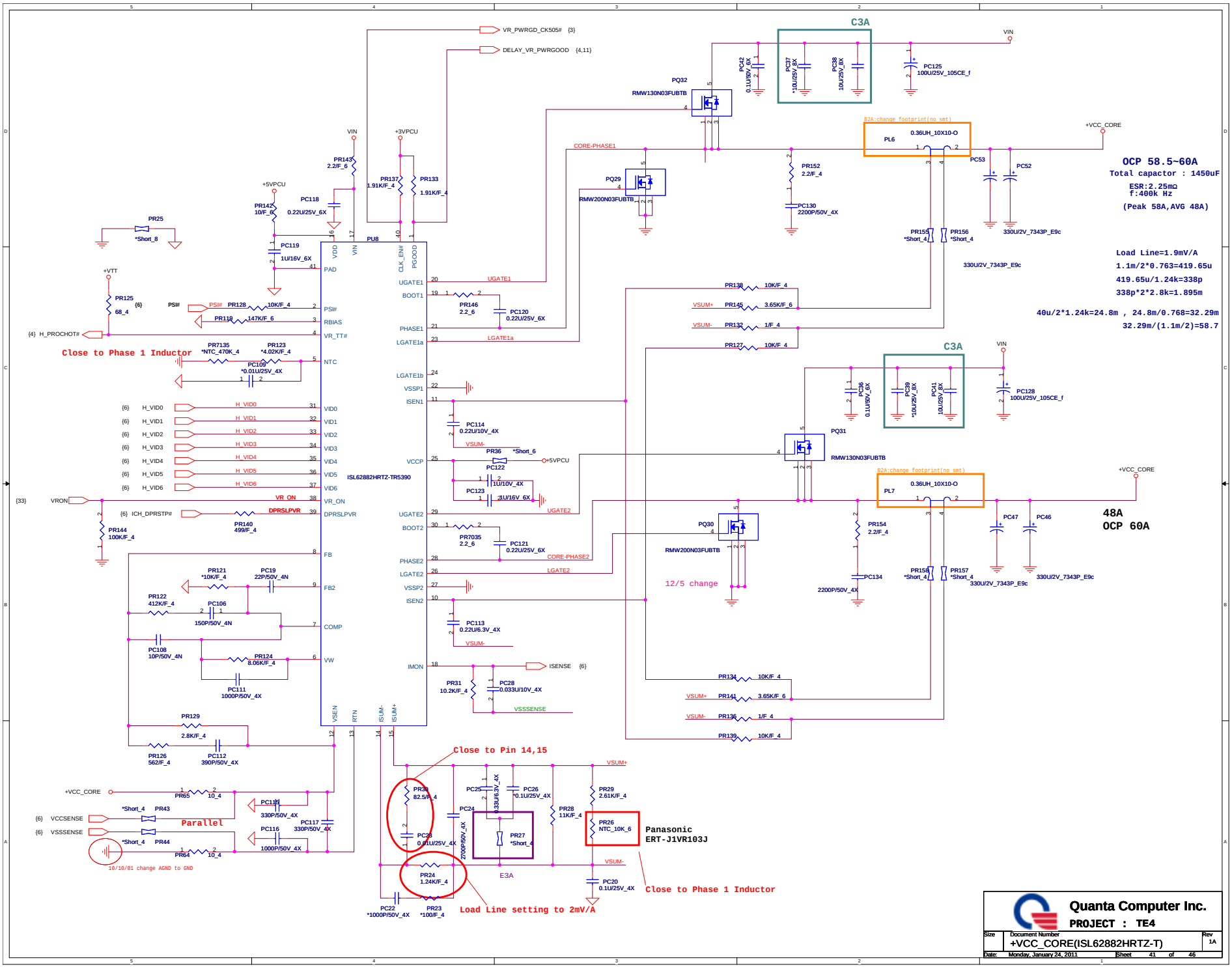
ISL62882HRTZ-TR5390
PU8
C3A
PQ32
RMW130N03FUBTB
PQ29
RMW200N03FUBTB
PQ31
PQ30
PL6
PL7
0.36UH_10X10-O
B2A:change footprint(no smt)
+VCC_CORE
VIN
+5VPCU
+3VPCU
+VTT
OCP 58.5~60A
Total capactor : 1450uF
ESR:2.25mΩ
f:400k Hz
(Peak 58A,AVG 48A)
Load Line=1.9mV/A
1.1m/2*0.763=419.65u
419.65u/1.24k=338p
338p*2*2.8k=1.895m
40u/2*1.24k=24.8m , 24.8m/0.768=32.29m
32.29m/(1.1m/2)=58.7
48A
OCP 60A
Close to Phase 1 Inductor
Close to Pin 14,15
Parallel
Panasonic
ERT-J1VR103J
Load Line setting to 2mV/A
12/5 change
E3A
10/10/01 change AGND to GND
Quanta Computer Inc.
PROJECT : TE4
+VCC_CORE(ISL62882HRTZ-T)
Monday, January 24, 2011
Sheet 41 of 46

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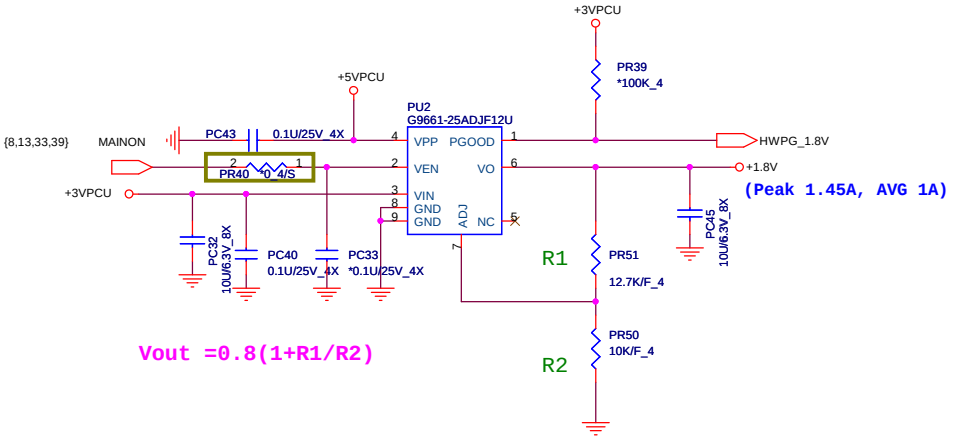
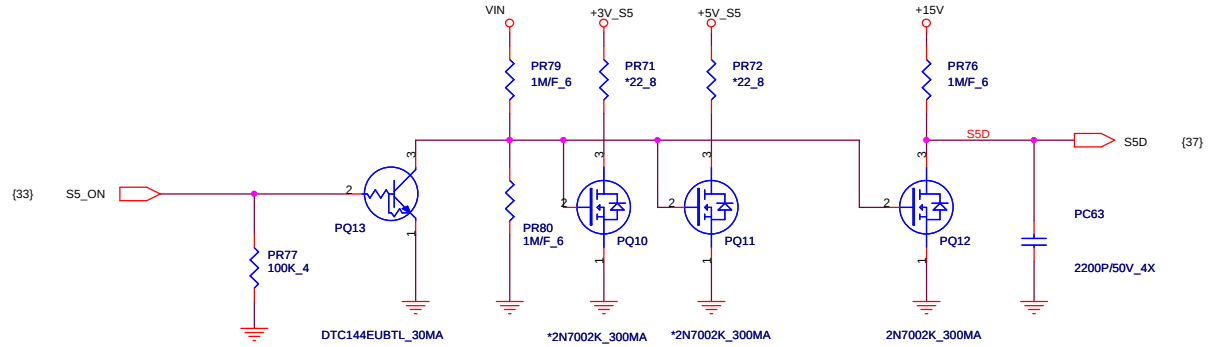
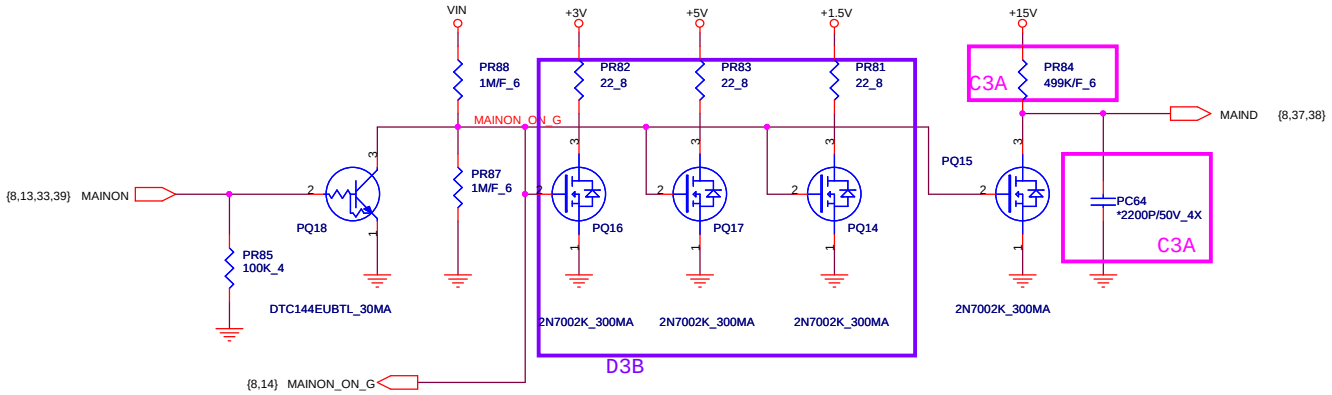
P7







Quanta Computer Inc.

PROJECT : TE4

Size	Document Number	Rev
	+1.8V (G966A)/Discharge	1A
Date: Monday, January 24, 2011	Sheet 42 of 46	

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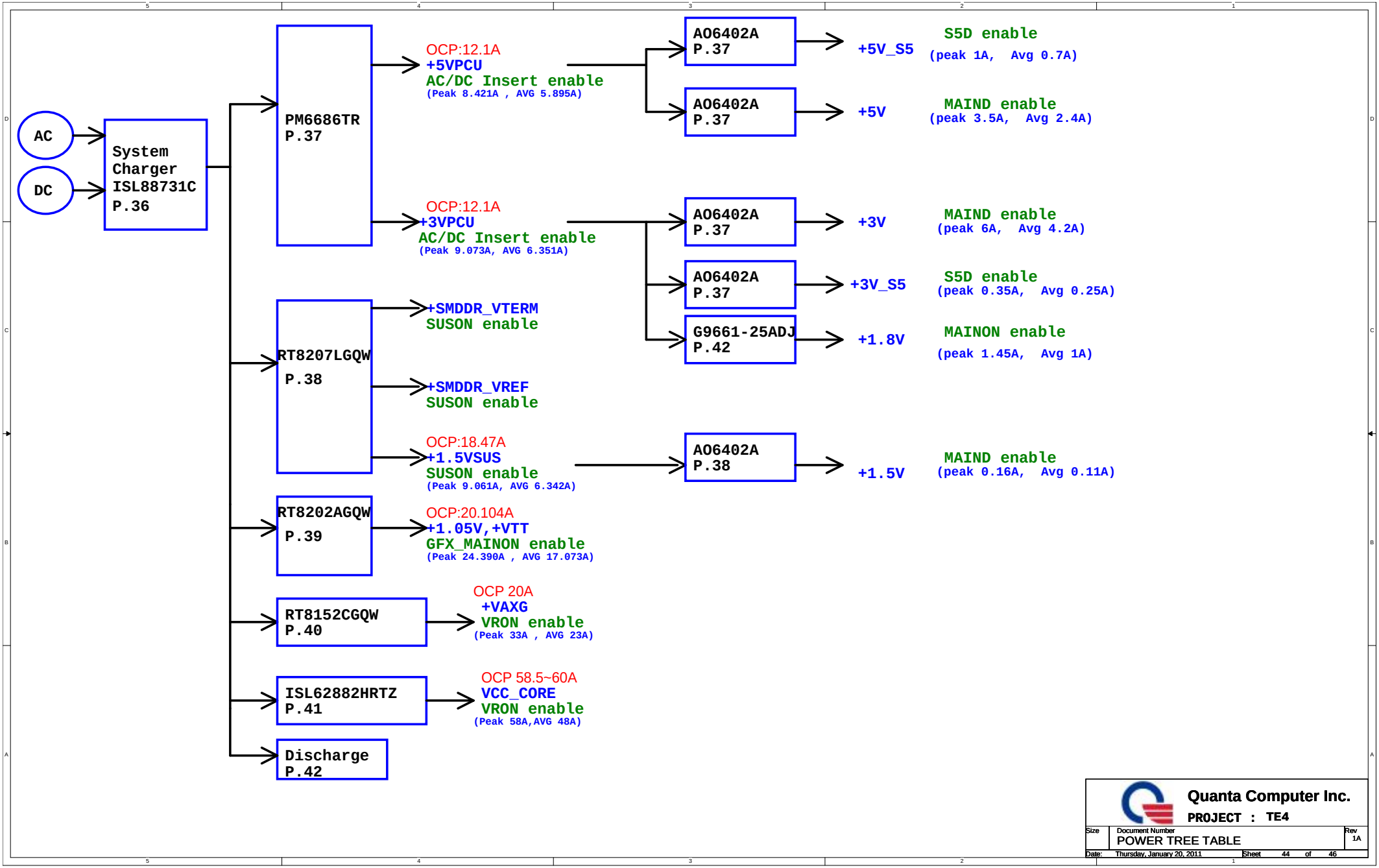
AC
DC
System Charger ISL88731C P.36
PM6686TR P.37
OCP:12.1A
+5VPCU
AC/DC Insert enable
(Peak 8.421A , AVG 5.895A)
AO6402A P.37
+5V_S5
S5D enable
(peak 1A, Avg 0.7A)
AO6402A P.37
+5V
MAIND enable
(peak 3.5A, Avg 2.4A)
OCP:12.1A
+3VPCU
AC/DC Insert enable
(Peak 9.073A, AVG 6.351A)
AO6402A P.37
+3V
MAIND enable
(peak 6A, Avg 4.2A)
AO6402A P.37
+3V_S5
S5D enable
(peak 0.35A, Avg 0.25A)
G9661-25ADJ P.42
+1.8V
MAINON enable
(peak 1.45A, Avg 1A)
RT8207LGQW P.38
+SMDDR_VTERM
SUSON enable
+SMDDR_VREF
SUSON enable
OCP:18.47A
+1.5VSUS
SUSON enable
(Peak 9.061A, AVG 6.342A)
AO6402A P.38
+1.5V
MAIND enable
(peak 0.16A, Avg 0.11A)
RT8202AGQW P.39
OCP:20.104A
+1.05V,+VTT
GFX_MAINON enable
(Peak 24.390A , AVG 17.073A)
RT8152CGQW P.40
OCP 20A
+VAXG
VRON enable
(Peak 33A , AVG 23A)
ISL62882HRTZ P.41
OCP 58.5~60A
VCC_CORE
VRON enable
(Peak 58A,AVG 48A)
Discharge P.42
Quanta Computer Inc.
PROJECT : TE4
Size
Document Number
POWER TREE TABLE
Rev 1A
Date: Thursday, January 20, 2011
Sheet 44 of 46

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Model	REV	CHANGE LIST
TE4 MB	2A	PAGE 14: R22 no stuff PAGE 15: R23 no stuff PAGE 27: add R470 PAGE 28: add Q1100/R1015 and no stuff PAGE 32: add Q40

MODEL	TE4	
PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204					
PROJECT MODEL :	TE4	APPROVED BY:	Kent Su	DATE:	2010/11/12
PART NUMBER:		DRAWING BY:	Kent Su	REVISON:	1A

Quanta Computer Inc.
PROJECT : TE4

Size	Document Number	Rev
	Block Diagram	1A

Date: Thursday, December 02, 2010 Sheet 45 of 46

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Model	REV	CHANGE LIST
TE4 MB	1A	PAGE 38: PC212 change value and FP to 0.1U/25V_6X ; add PD9 (10.10.06)
		PAGE 35: add PC71 and PC76 for EMI Sol. (10.10.06)
		PAGE 36: add PD12 , PR142 and PR139 (10.10.06)
		Rename
		PAGE 36: PR169 , PR171, PR165 , PU10 , PR101 change Value ; PR173 , PR102 , PR96 no stuff ; PR175 stuff (10.10.20)
		PAGE 37: PC133 change Value and FP (10.10.20)
		PAGE 38: PU9 , PQ41 , PQ43 change Value (10.10.20)
		PAGE 35: add PC158 and PC99 for EMI sol. (10.11.5)
		PAGE 35: add PU11 (10.11.5)
		PAGE 36: delete PJP5 , PJP6 (10.11.5)
		PAGE 36: change PL8 , PL9 , PR35 Value (10.11.5)
		PAGE 37: delete PJP4 , PC135 stuff , PR42 change Value (10.11.5)
		PAGE 38: PU9 change Value (10.11.5)

MODEL: TE2

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204					
PROJECT MODEL :	TE2	APPROVED BY:	Mosy Li	DATE:	2009/11/13
PART NUMBER:		DRAWING BY:	Mosy Li	REVISON:	1A

Quanta Computer Inc.
PROJECT : TE4
Size: | Document Number: GPU | Rev: 1A
Date: Thursday, December 02, 2010 | Sheet 46 of 46

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