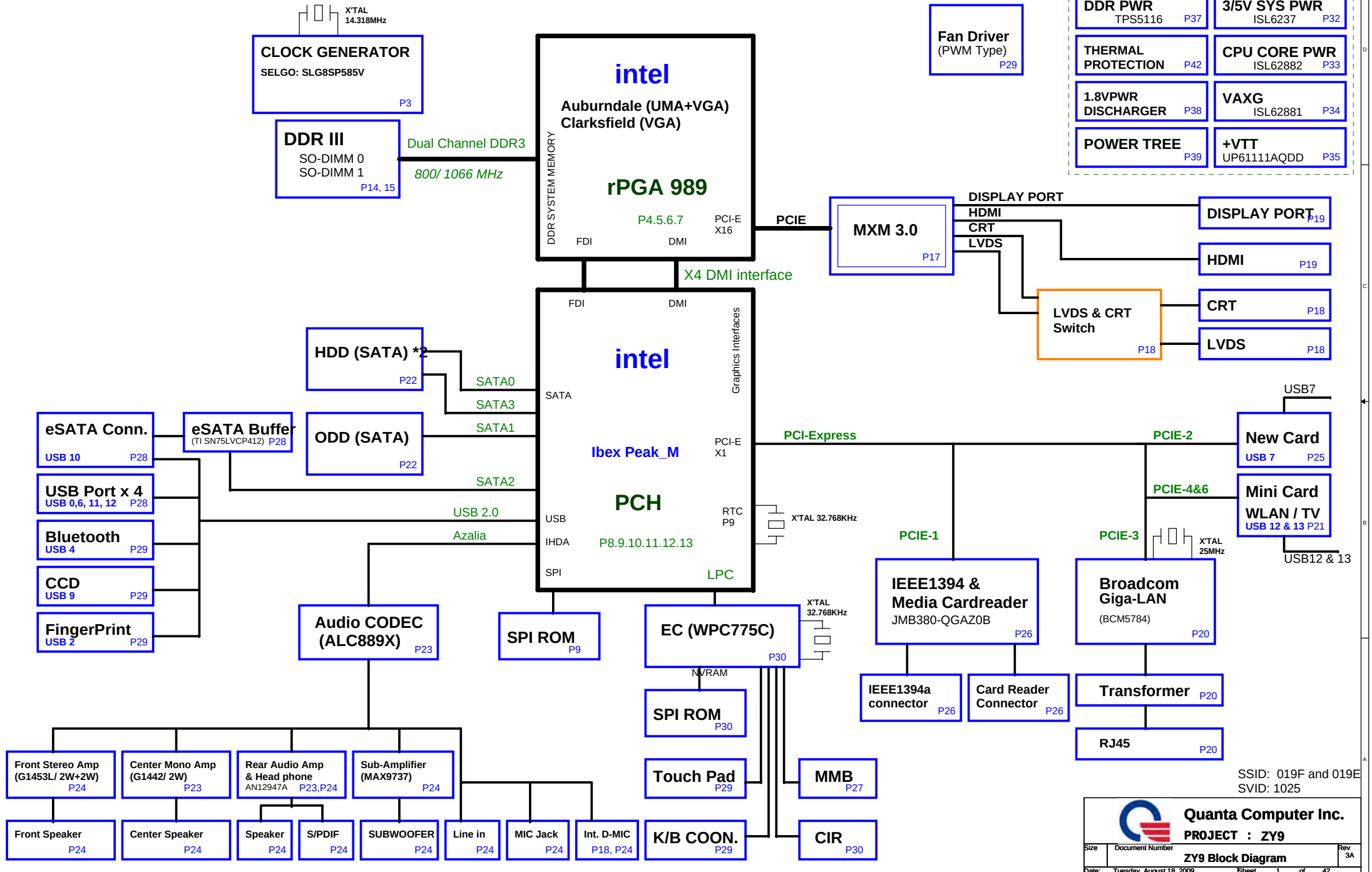
31ZY9MB0000
ZY9 MB ASSY(DC/GM/MXM)ASSY W/O CPU
31ZY9MB0010
ZY9 MB ASSY(QC/GM/MXM)ASSY W/O CPU

ZY9 SYSTEM BLOCK DIAGRAM



SSID: 019F and 019E
SVID: 1025

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PROJECT : ZY9

Size	Document Number	Rev
	ZY9 Block Diagram	3A

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Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5VSUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

GND PLANE	PAGE	DESCRIPTION
LANGND	20	
E775AGND	30	
ADOGND	23.24	
GND	ALL	

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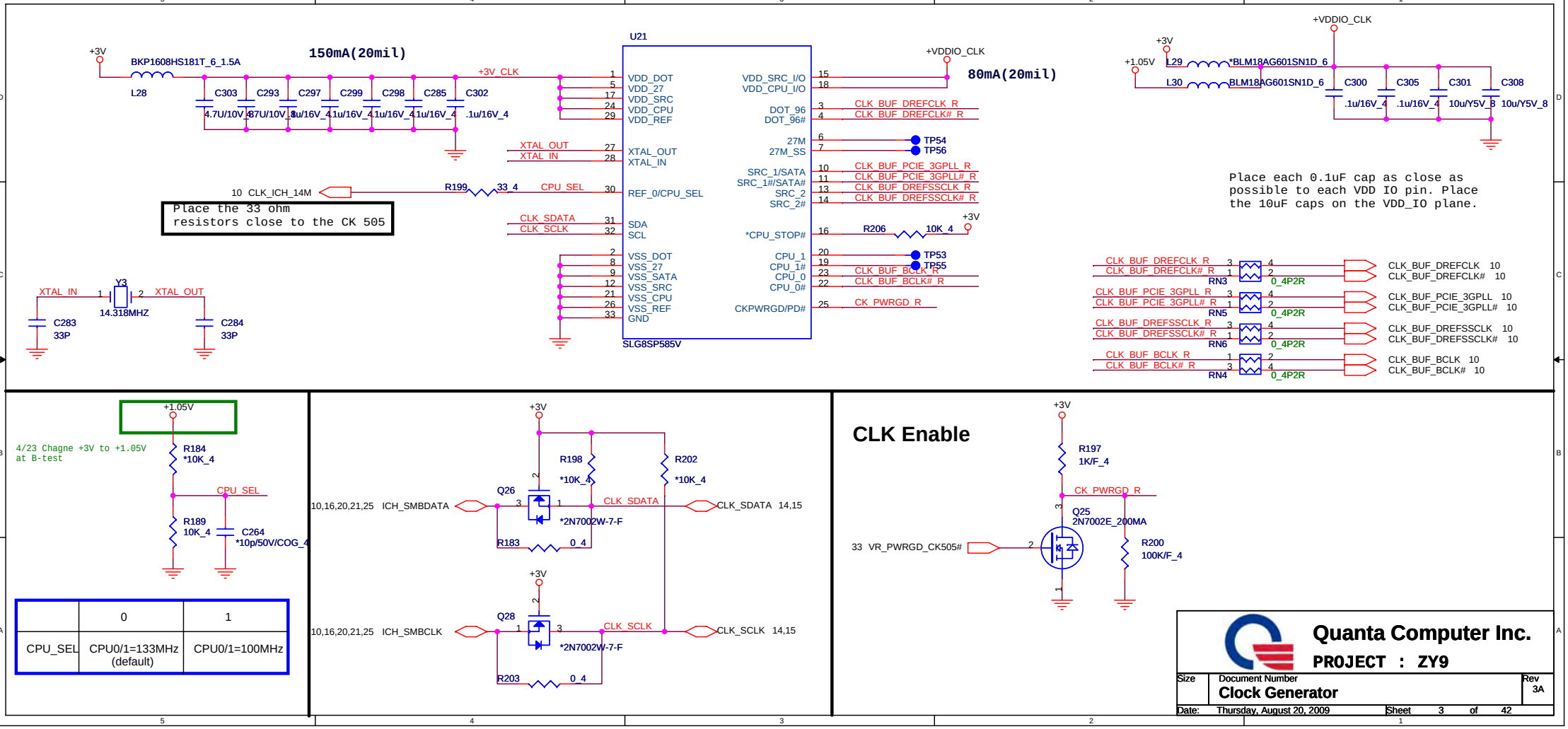

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

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Size	Document Number	Rev
	Clock Generator	3A

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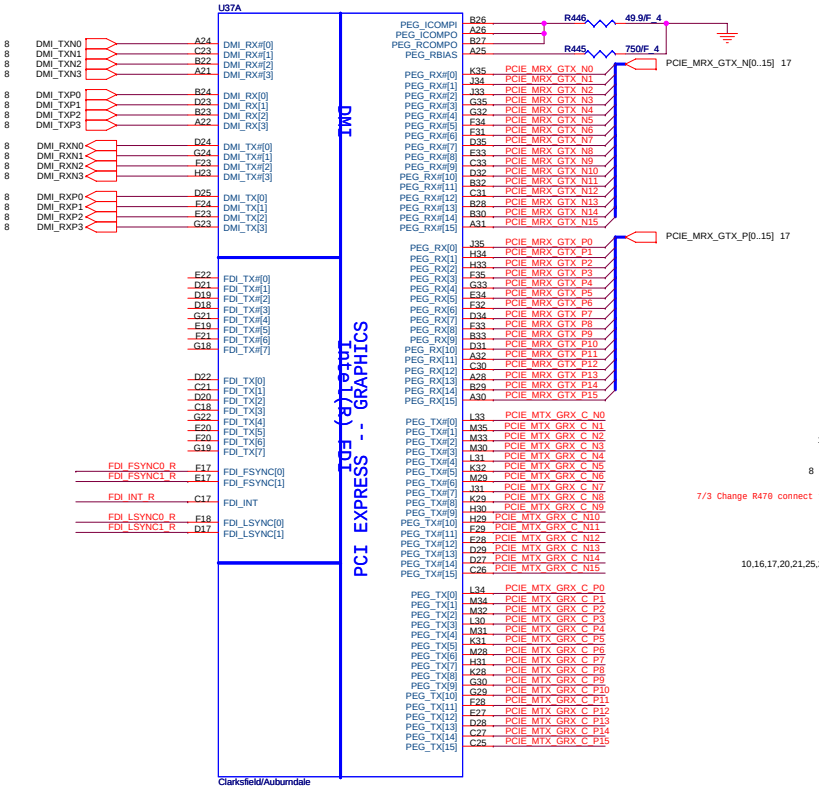
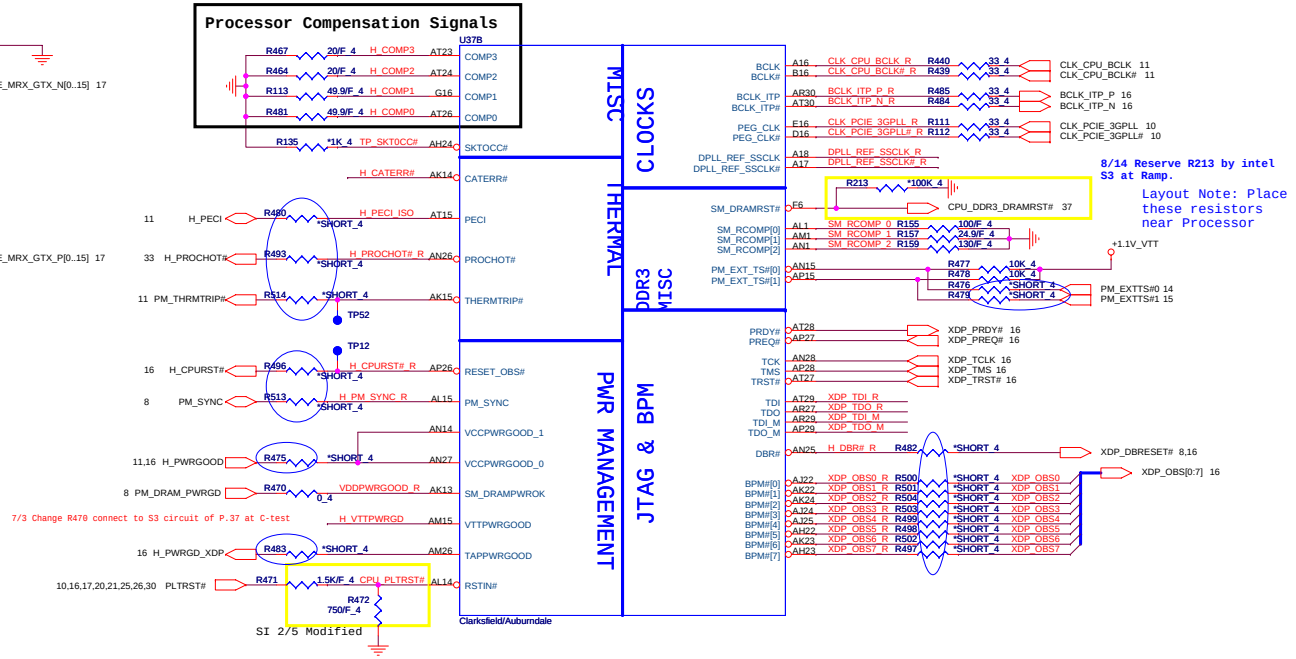
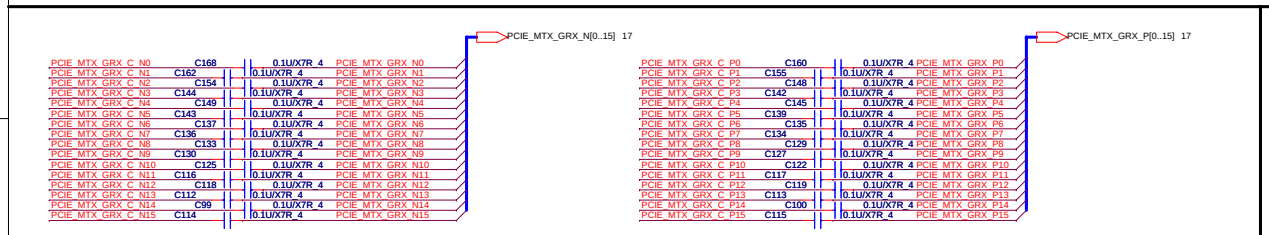
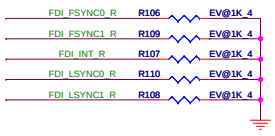
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



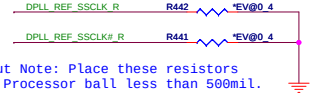




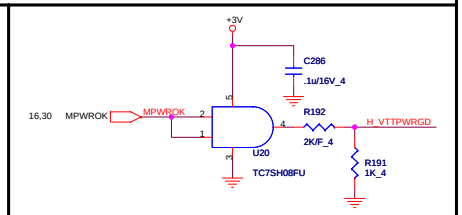
[VGA]



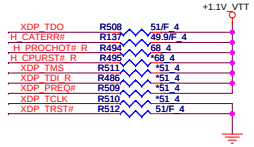
Auburndale Graphics Disabled Guideline
(Checklist 1.0 P52 Auburndale Graphics Disable Guidelines)



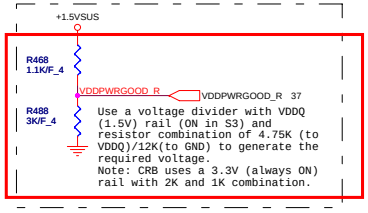
Layout Note: Place these resistors near Processor ball less than 500mil.



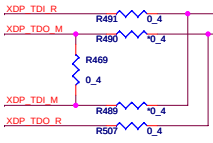
Processor Pullups



7/3 Reserve S3 circuit of P.37 connect to VDDPWRGOOD_R at C-test
4/9 REV:B MODIFY BY DG1.52



JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

Quanta Computer Inc.
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	AUBURNDA 1/4	3A
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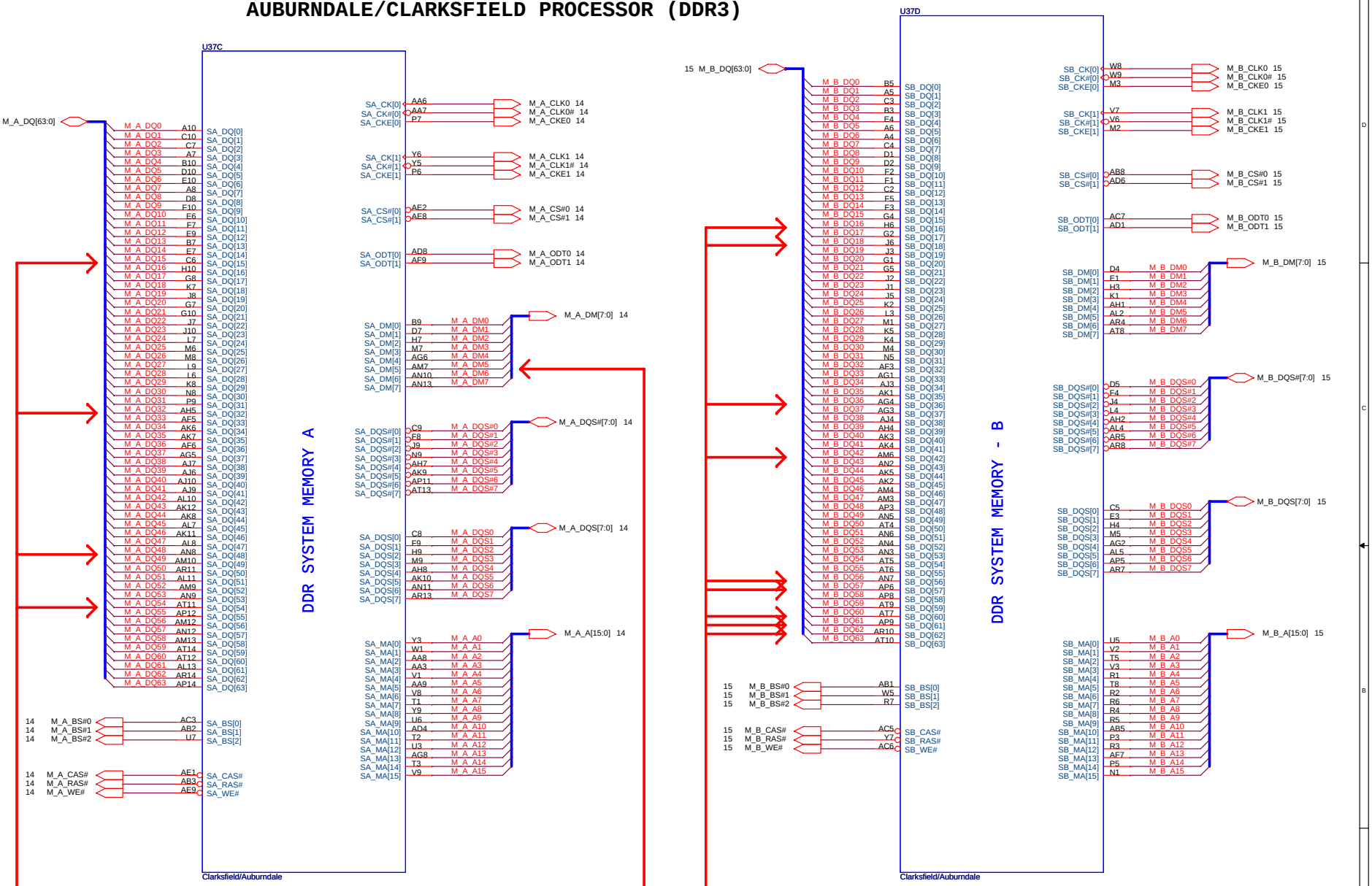
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.		
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AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

CPU Core Power

+VCC_CORE

U37F

48A

1.1V RAIL POWER

CPU CORE SUPPLY

18A

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

+1.1V_VTT

C501 10U_8
C506 10U_8
C525 10U_8
C531 10U_8
C519 10U_8
C523 10U_8
C504 10U_8
C214 22U_8
C205 22U_8
C511 22U_8
C500+ *330u/2V_7343

+1.1V_VTT

C223 22U_8
C237 22U_8
TP9
R122 *SHORT_4
R123 *SHORT_4
TP10
C98 1u/10V_4

(15mils)

For CRB use

POWER

CPU VIDS

PSI# AN33 H_PSI# 33

VID[0] AK35 H_VID0 H_VID0 33
VID[1] AK33 H_VID1 H_VID1 33
VID[2] AK34 H_VID2 H_VID2 33
VID[3] AL35 H_VID3 H_VID3 33
VID[4] AL33 H_VID4 H_VID4 33
VID[5] AM33 H_VID5 H_VID5 33
VID[6] AM35 H_VID6 H_VID6 33

PROC_DPRSLPVR AM34 ICH_DPRSLPVR 33

VTT_SELECT G15 H_VTTVID1 TP8

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

SENSE LINES

ISENSE AN35 I_MON 33

VCC_SENSE AJ34 R150 100_4 VCC_CORE VCCSENSE 33
VSS_SENSE AJ35 R146 100_4 VSSSENSE 33

VTT_SENSE B15 VTT_SENSE
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT TP6 TP7

Clarksfield/Auburndale

U37G

GRAPHICS

SENSE LINES

VAXG_SENSE AR22
VSSAXG_SENSE AT22

GRAPHICS VIDS

GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24

IMON R193 EV@1K_4

POWER

DDR3 - 1.5V RAILS

3A

+1.5V_CPUVDDQ

VDDQ1 AJ1
VDDQ2 AF1
VDDQ3 AE7
VDDQ4 AF4
VDDQ5 AC1
VDDQ6 AB7
VDDQ7 AB4
VDDQ8 W7
VDDQ9 W4
VDDQ10 U1
VDDQ11 T7
VDDQ12 T4
VDDQ13 P1
VDDQ14 N7
VDDQ15 N4
VDDQ16 L1
VDDQ17 H1
VDDQ18

C188 1u/10V_4
C194 1u/10V_4
C241 1u/10V_4
C228 1u/10V_4
C221 1u/10V_4

C203 22U_8
C213 22U_8
C163 *330u/2V_7343

7/2 Change CPU VDDQ from +1.5V_S3 to +1.5V_CPUVDDQ at C test.

6/5 No stuff at RevC by DG1.6

FDI

+1.1V_VTT

C180 22U_8
C509 22U_8

VTT1_45 J24
VTT1_46 J23
VTT1_47 H25

PEG & DMI

+1.1V_VTT

C181 22U_8
C182 22U_8
C197 22U_8
C517 22U_8

VTT1_48 K26
VTT1_49 J27
VTT1_50 J26
VTT1_51 J25
VTT1_52 H27
VTT1_53 G28
VTT1_54 G27
VTT1_55 G26
VTT1_56 F26
VTT1_57 E26
VTT1_58 E25

1.1V

+1.1V_VTT

VTT0_59 P10
VTT0_60 N10
VTT0_61 L10
VTT0_62 K10

C184 10u/6.3V_6
C176 10u/6.3V_6

VTT1_63 J22
VTT1_64 J20
VTT1_65 J18
VTT1_66 H21
VTT1_67 H20
VTT1_68 H19

C507 22U_8
C508 22U_8

1.8V

VCCPLL1 L26
VCCPLL2 L27
VCCPLL3 M26

+1.8V

C178 1u/10V_4
C179 1u/10V_4
C503 2.2U_6_H0.5
C502 4.7u_6
C505 22U_8

0.6A

Clarksfield/Auburndale

+1.1V_VTT

R448 1K_4
R450 1K_4
R452 1K_4
R454 *1K_4
R456 *1K_4
R459 1K_4
R461 *1K_4
R466 1K_4
R463 *1K_4

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
ICH_DPRSLPVR
H_PSI#

R447 *1K_4
R449 *1K_4
R451 *1K_4
R453 1K_4
R455 1K_4
R458 *1K_4
R460 1K_4
R465 *1K_4
R462 1K_4

Note:
For Validating IMVP VR R6451 should be STUFF and R2N1 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

+VCC_CORE

C199 22U_8
C530 22U_8
C526 22U_8
C512 22U_8
C222 22U_8
C238 22U_8
C174 22U_8
C191 22U_8

C183 22U_8
C226 22U_8
C529 22U_8
C243 22U_8
C236 22U_8
C190 22U_8
C527 22U_8
C528 22U_8

C198 10u/6.3V_6
C234 10u/6.3V_6
C520 10u/6.3V_6
C209 10u/6.3V_6
C516 10u/6.3V_6
C514 10u/6.3V_6
C195 10u/6.3V_6
C217 10u/6.3V_6

C515 10u/6.3V_6
C513 10u/6.3V_6
C521 10u/6.3V_6
C518 10u/6.3V_6
C510 10u/6.3V_6
C232 10u/6.3V_6
C524 10u/6.3V_6
C196 10u/6.3V_6

C498 *330u/2V_7343
C480 330u/2V_7343
C208 *330u/2V_7343
C522 330u/2V_7343

4,7,11,12,16,34,37 +1.1V_VTT
33 +VCC_CORE
11,12,37 +1.8V

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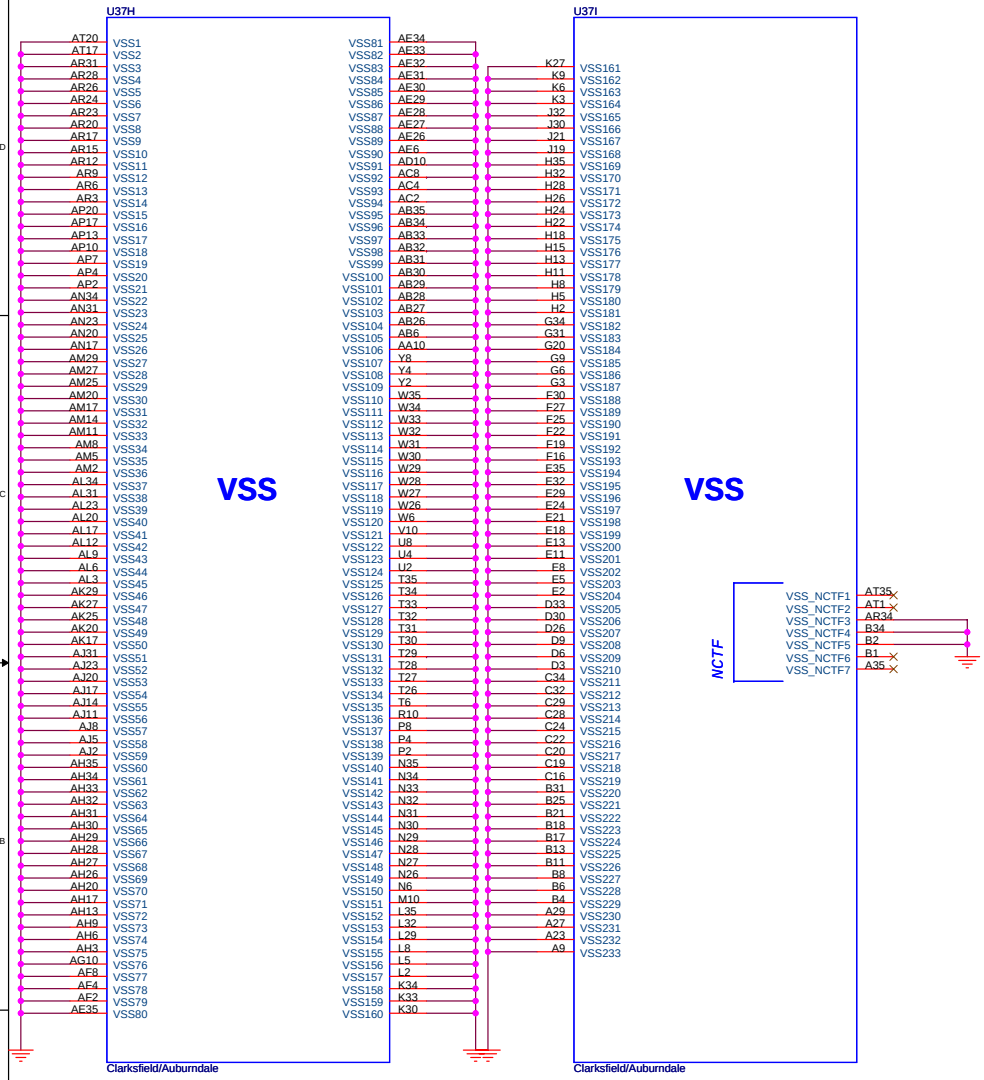
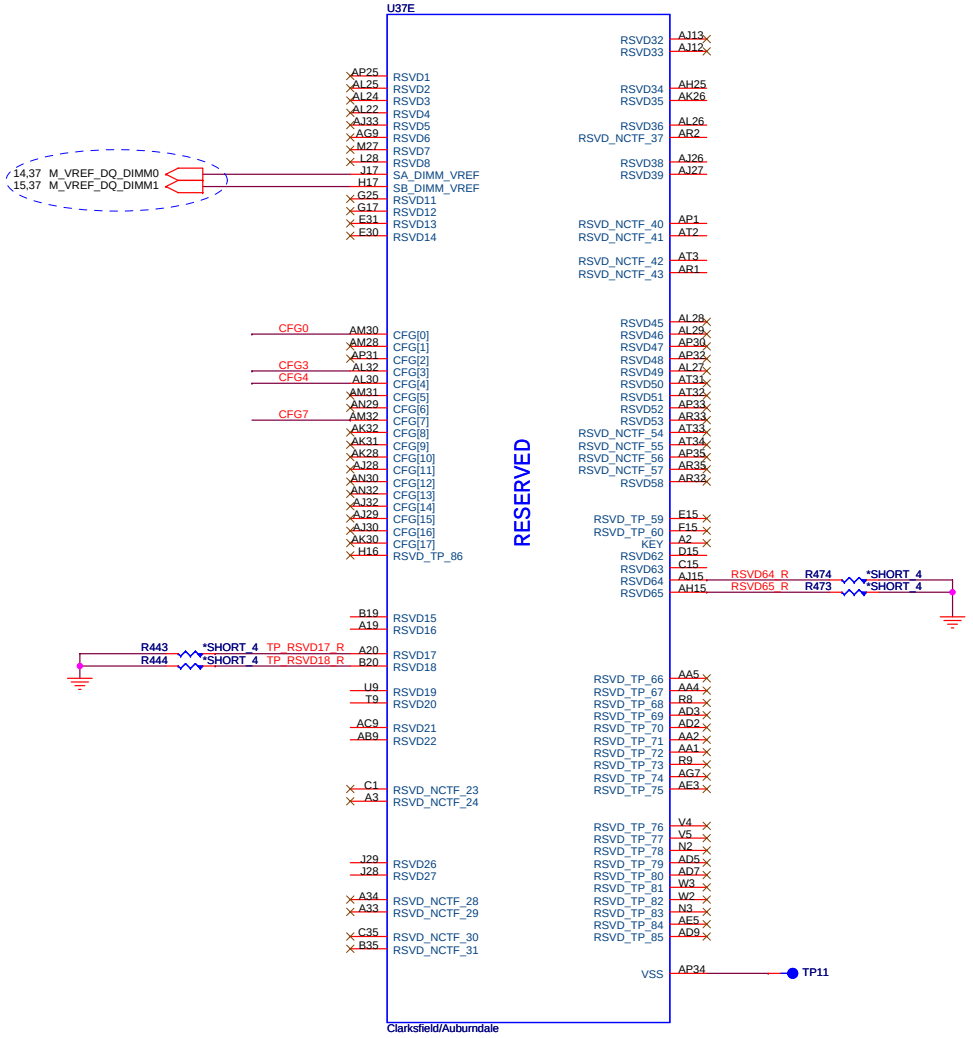
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

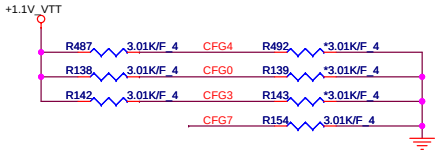
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

Quanta Computer Inc.
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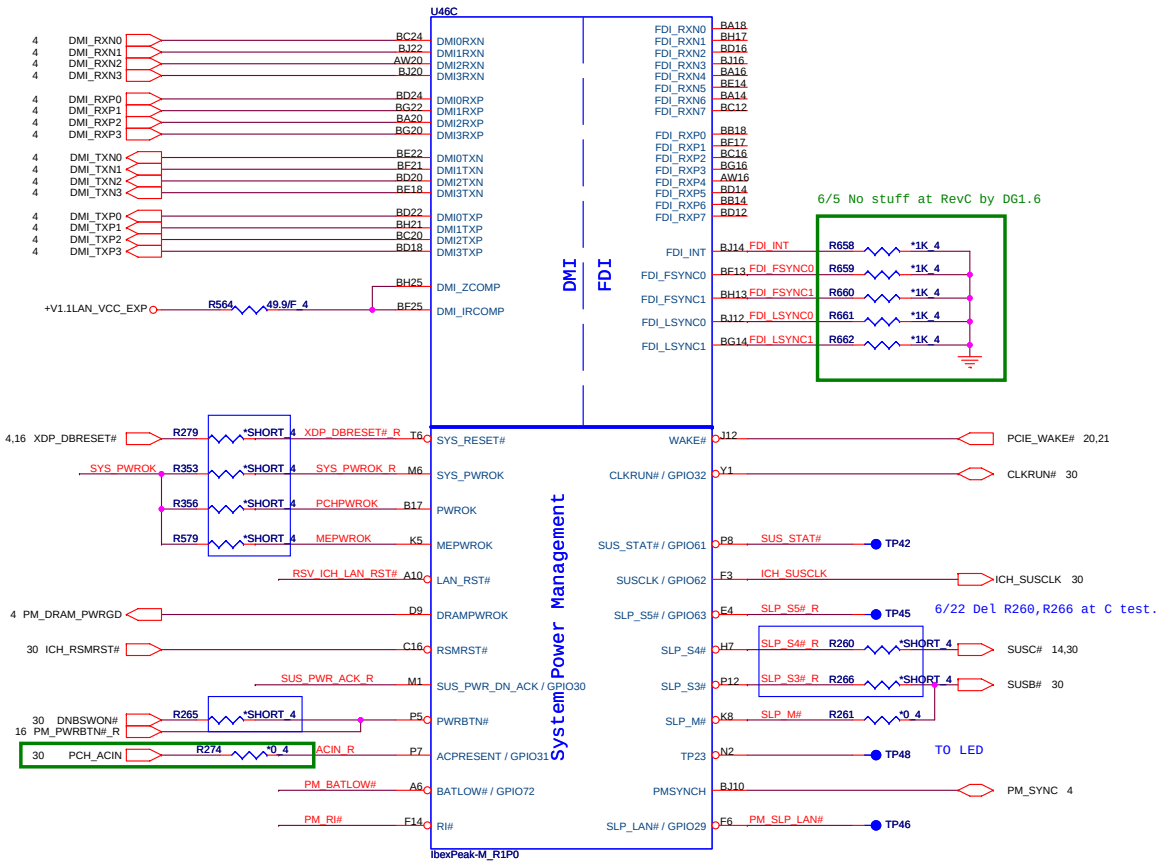
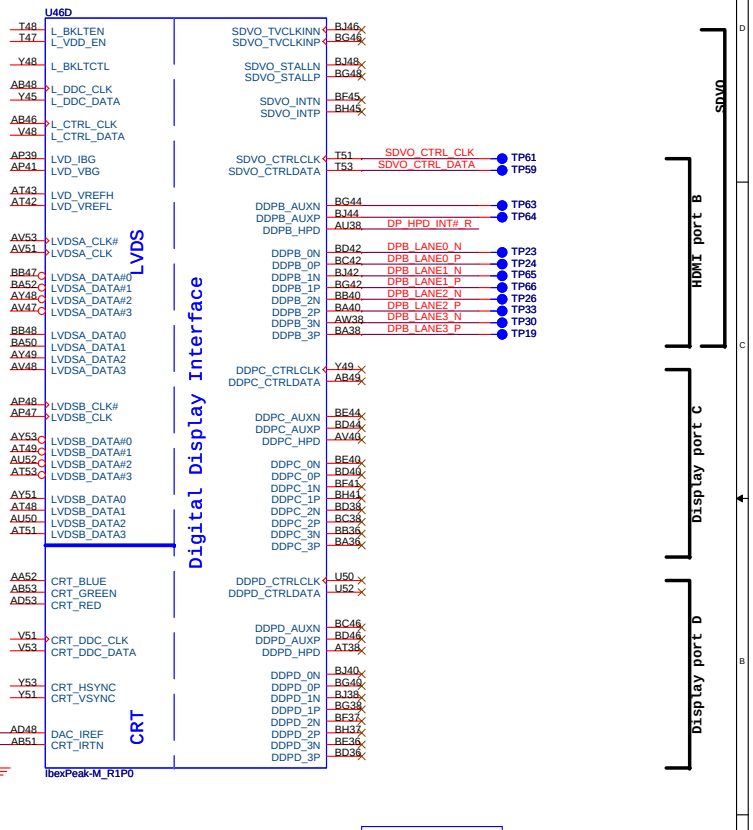
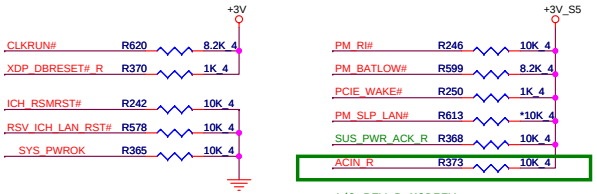
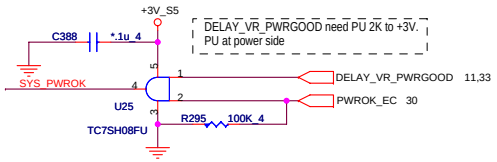
IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (LVDS,DDI)







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IBEX PEAK-M (HDA,JTAG,SATA)

RTC Circuitry

CMOS Settings	J5
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J4
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

Cap values depend on Xtal

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

7/1 change from +3V_S5 to +3V by intel.

6/21 Non stuff R233 by Intel at C-test.

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

For PCH 16Mbit (2M Byte), SPI/ 32Mbit (4M Byte), SPI

TPM Function	R591
Enable	Mount
Disable	NC (Default)

SATA HDD **SATA ODD** **E-SATA** **2ND SATA HDD**

Quanta Computer Inc.	
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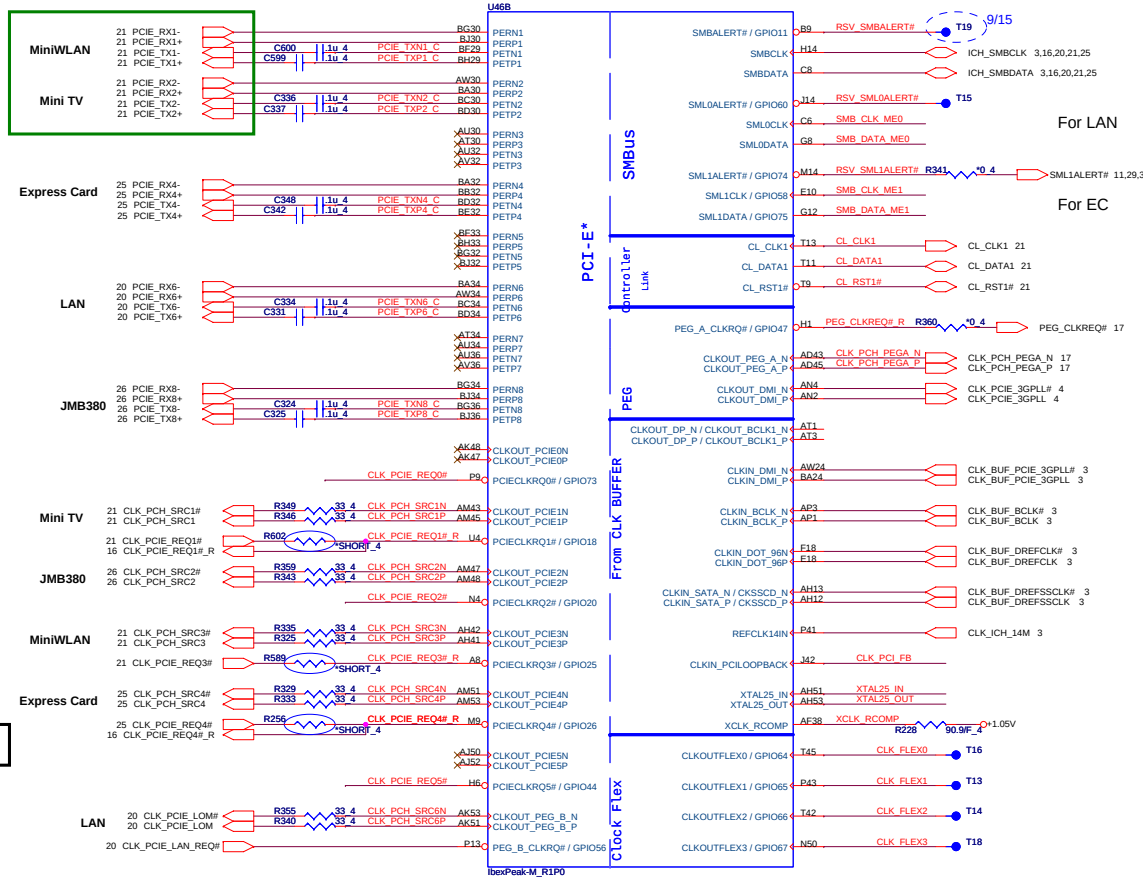
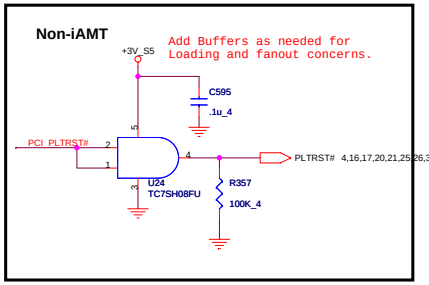
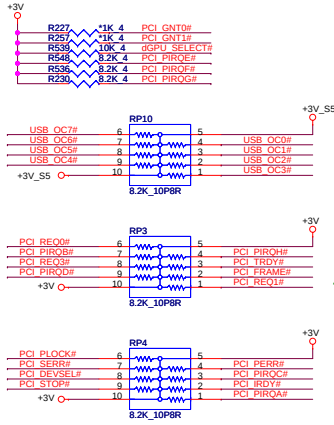
IBEX PEAK-M (PCI,USB,NVRAM)

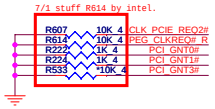
5/14 Change PCIE sequence beween CN21 and CN23 by BIOS at B-test.

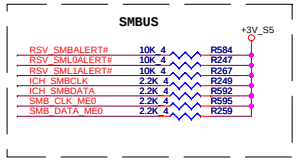
IBEX PEAK-M (PCI-E,SMBUS,CLK)

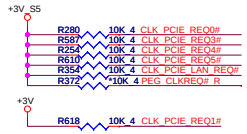


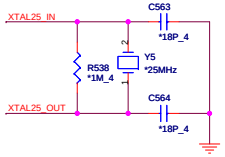


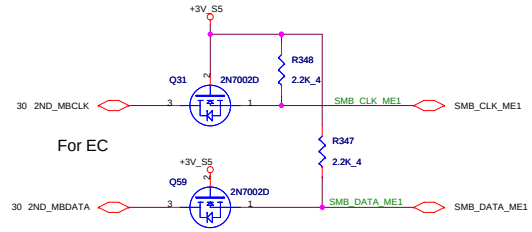


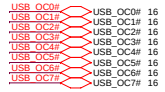












Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

No stuff XTAL25_IN and XTAL25_OUT circuitry until integrated CG becomes PCH POR.

Quanta Computer Inc.	
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IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

U46F

BMBUSY# / GPIO0
TACH1 / GPIO1
TACH2 / GPIO6
TACH3 / GPIO7
GPIO8
LAN_PHY_PWR_CTRL / GPIO12
GPIO15
SATA4GP / GPIO16
TACH0 / GPIO17
SCLOCK / GPIO22
GPIO24
GPIO27
GPIO28
STP_PCI# / GPIO34
SATACLKREQ# / GPIO35
SATA2GP / GPIO36
SATA3GP / GPIO37
SLOAD / GPIO38
SDATAOUT0 / GPIO39
PCIECLKRQ6# / GPIO45
PCIECLKRQ7# / GPIO46
SDATAOUT1 / GPIO48
SATA5GP / GPIO49
GPIO57

MISC
GPIO
CPU
NCTF
RSVD

16 BMBUSY# — BMBUSY# — Y3
30 SIO_EXT_SMI# — SIO_EXT_SMI# — C38
30 SIO_EXT_SCI# — SIO_EXT_SCI# — D37
BOARD_ID0 — J32
7/1 change board_id0 to GPIO7 at C-test
RSV_GPIO8 — F10
TP60 — LAN_DISABLE# — K9
26 CR_WAKE# — CR_WAKE# — T7
16,17 dGPU_HOLD_RST# — dGPU_HOLD_RST# — AA2
17 dGPU_RUNPWROK — R229 *SHORT_4 — dGPU_RUNPWROK_R — F38
GPIO22 — Y7
7/1 GPIO24 NC for Intel suggestion at C-test.
TP69 — GPIO24 — H10
TP58 — GPIO27 — AB12
16 TP_PCH_GPIO28 — V13
STP_PCI# — M11
28 SAVE_LED# — SAVE_LED# — V6
16 dGPU_PWR_EN# — dGPU_PWR_EN# — AB7
16,17 dGPU_PRSNT# — dGPU_PRSNT# — AB13
GPIO38 — V3
GPIO39 — P3
GPIO45 — H3
30,37 DDR3_DRAMRST#_EC — R428 *0_4 — GPIO46 — F1
SV_SET_UP — AB6
16 SATA5GP — SATA5GP — AA4
10,29,30 SML1ALERT# — R351 0_4 — GPIO57 — F8

8/8 Reserve R428 from GPIO46 by intel S3 suggestion at Ramp.

5/12 Reverse R351 connect to EC for Temp Alert at B-test

SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

CLKOUT_PCIE6N — AH45 — TP_PCH_PCIE6N — TP49
CLKOUT_PCIE6P — AH46 — TP_PCH_PCIE6P — TP50
CLKOUT_PCIE7N — AF48 — TP_PCH_PCIE7N — TP51
CLKOUT_PCIE7P — AF47 — TP_PCH_PCIE7P — TP44
A20GATE — U2 — SIO_A20GATE 30
CLKOUT_BCLK0_N / CLKOUT_PCIE8N — AM3 — CLK_CPU_BCLK# 4
CLKOUT_BCLK0_P / CLKOUT_PCIE8P — AM1 — CLK_CPU_BCLK 4
PECI — BG10 — PCH_PECI_R — R581 *SHORT_4 — H_PECI 4
RCIN# — T1 — SIO_RCIN# 30
PROCPWRGD — BE10 — H_PWRGOOD 4,16
THRMTRIP# — BD10 — PCH_THRMTRIP#_R — R252 56/F_4 — PM_THRMTRIP# 4
+1.1V_VTT — R251 56/F_4

TP1 — BA22 — TP1_PCH — TP41
TP2 — AW22 — TP2_PCH — TP40
TP3 — BB22
TP4 — AY45
TP5 — AY46
TP6 — AV43
TP7 — AV45
TP8 — AF13
TP9 — M18
TP10 — N18
TP11 — AJ24
TP12 — AK41
TP13 — AK42
TP14 — M32
TP15 — N32
TP16 — M30
TP17 — N30
TP18 — H12
TP19 — AA23
NC_1 — AB45
NC_2 — AB38
NC_3 — AB42
NC_4 — AB41
NC_5 — T39
INIT3_3V# — P6 — TP_INT3_3V — TP68
TP24 — C10

VSS_NCTF_1 — A4
VSS_NCTF_2 — A49
VSS_NCTF_3 — A5
VSS_NCTF_4 — A50
VSS_NCTF_5 — A52
VSS_NCTF_6 — A53
VSS_NCTF_7 — B2
VSS_NCTF_8 — B4
VSS_NCTF_9 — B52
VSS_NCTF_10 — B53
VSS_NCTF_11 — BE1
VSS_NCTF_12 — BE53
VSS_NCTF_13 — BF1
VSS_NCTF_14 — BF53
VSS_NCTF_15 — BH1
VSS_NCTF_16 — BH2
VSS_NCTF_17 — BH52
VSS_NCTF_18 — BH53
VSS_NCTF_19 — BJ1
VSS_NCTF_20 — BJ2
VSS_NCTF_21 — BJ4
VSS_NCTF_22 — BJ49
VSS_NCTF_23 — BJ5
VSS_NCTF_24 — BJ50
VSS_NCTF_25 — BJ52
VSS_NCTF_26 — BJ53
VSS_NCTF_27 — D1
VSS_NCTF_28 — D2
VSS_NCTF_29 — D53
VSS_NCTF_30 — E1
VSS_NCTF_31 — E53

IbexPeak-M_R1P0

Del R231 at C-test.

+3V_S5
CR_WAKE# — R275 — 1K_4
RSV_GPIO8 — R258 — 10K_4
TP_PCH_GPIO28 — R634 — 10K_4
GPIO45 — R625 — 10K_4
GPIO46 — R624 — 10K_4
GPIO57 — R621 — *10K_4
LAN_DISABLE# — R285 — 10K_4

+3V
SIO_EXT_SMI# — R551 — 10K_4
SIO_EXT_SCI# — R278 — 10K_4
dGPU_PWR_EN# — R631 — 10K_4
dGPU_RUNPWROK_R — R330 — 10K_4

+3V
SIO_RCIN# — R601 — 10K_4
SIO_A20GATE — R616 — 10K_4
dGPU_HOLD_RST# — R282 — 10K_4
SATA5GP — R605 — 10K_4
GPIO22 — R276 — 10K_4
dGPU_PRSNT# — R604 — 10K_4
SAVE_LED# — R277 — 10K_4
STP_PCI# — R623 — 10K_4
GPIO39 — R600 — 10K_4
GPIO38 — R603 — 10K_4

4,6,7,12,16,34,37 +1.1V_VTT
3,10,12,16,22,35,37 +1.05V
3,4,8,9,10,12,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37 +3V
8,9,10,12,14,15,16,20,25,27,29,30,32,37 +3V_S5
6,12,37 +1.8V

+3V_S5 — R641 *10K_4 — BOARD_ID0 — R640 10K_4
GPIO27 — R669 *10K_4
RSV_GPIO8 — R670 *1K_4
GPIO57 — R671 10K_4

4/9 Reserve GPIO8 by ww14 MoW
7/1 Add R671 for GPIO57 PD and not PU for Intel suggestion at C-test.

Integrated Clock Chip Enable	
RSV_GPIO8	High = Disable Low = Enable
BOARD_ID0	High = Touch Screen Low = Discrete

+1.8V
10 NV_ALE — R586 *1K_4
10 NV_CLE — R606 *1K_4

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

5/12 Reverse Q12,Q11 connect to t SYS_SHDN# at B-test

+1.1V_VTT
8,33 DELAY_VR_PWRGOOD — Q12 *2N7002D
PM_THRMTRIP# — Q11 *MMBT3904 — SYS_SHDN# 32,41

+3V
BMBUSY# — R371 — 8.2K_4
SV_SET_UP — R283 — 10K_4

SV_SET_UP	1-X High = Strong (Default)

Quanta Computer Inc.
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Size	Document Number	Rev
	IBEX PEAK-M 4/6	3A
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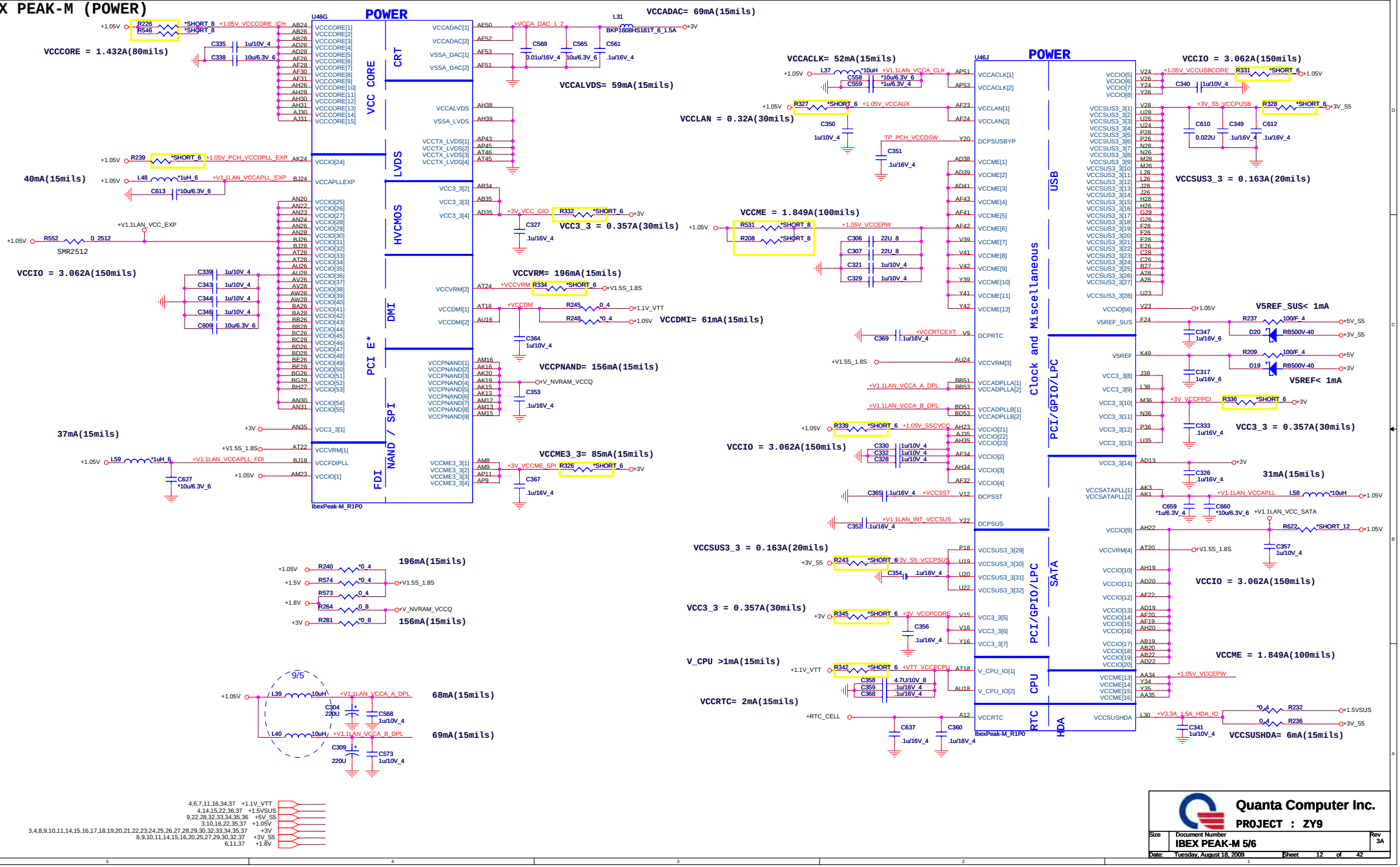
IBEX PEAK-M (POWER)



Quanta Computer Inc.
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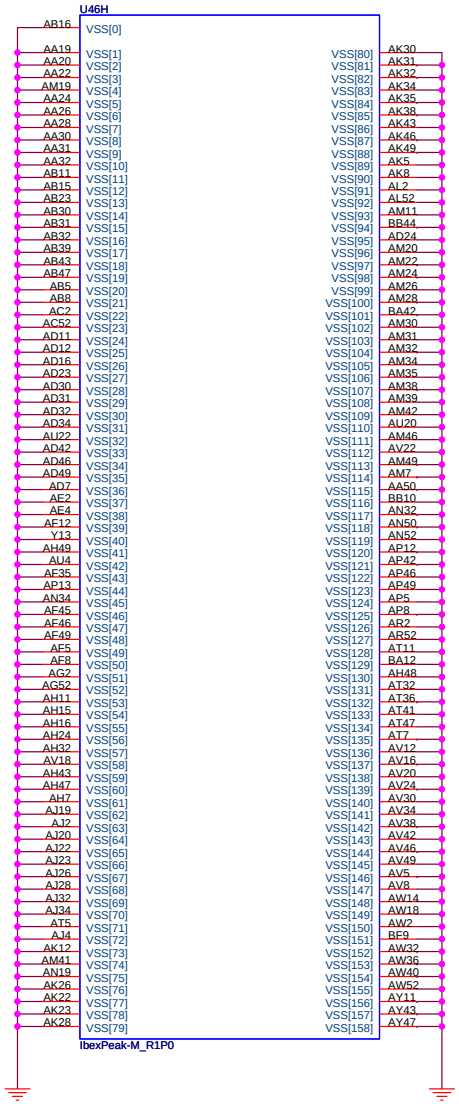
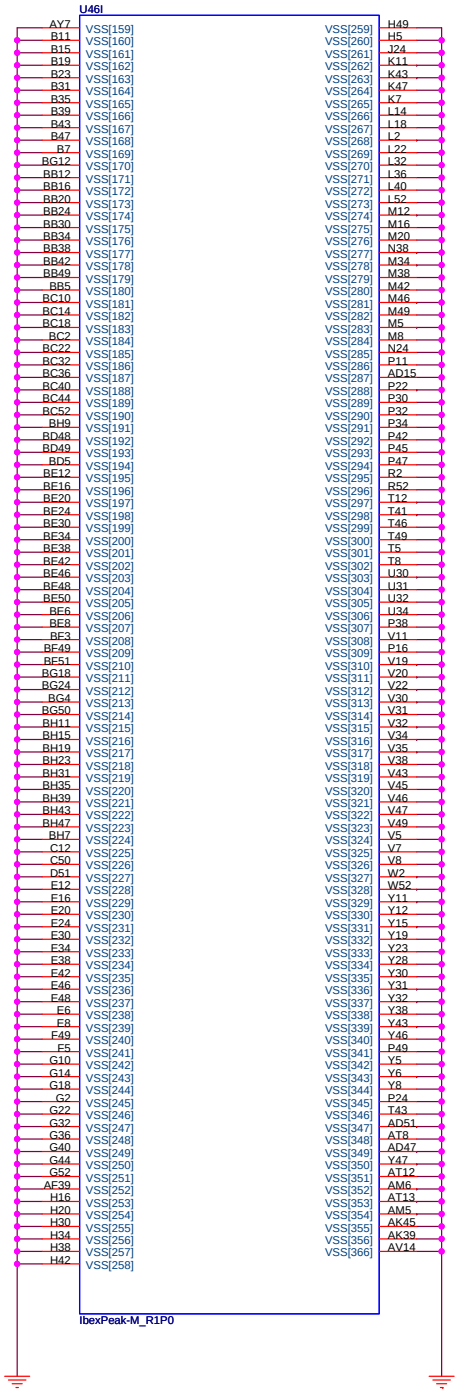
Size	Document Number	Rev
	IBEX PEAK-M 5/6	3A
Date: Tuesday, August 18, 2009	Sheet 12 of 42	

IBEX PEAK-M (GND)





Quanta Computer Inc.

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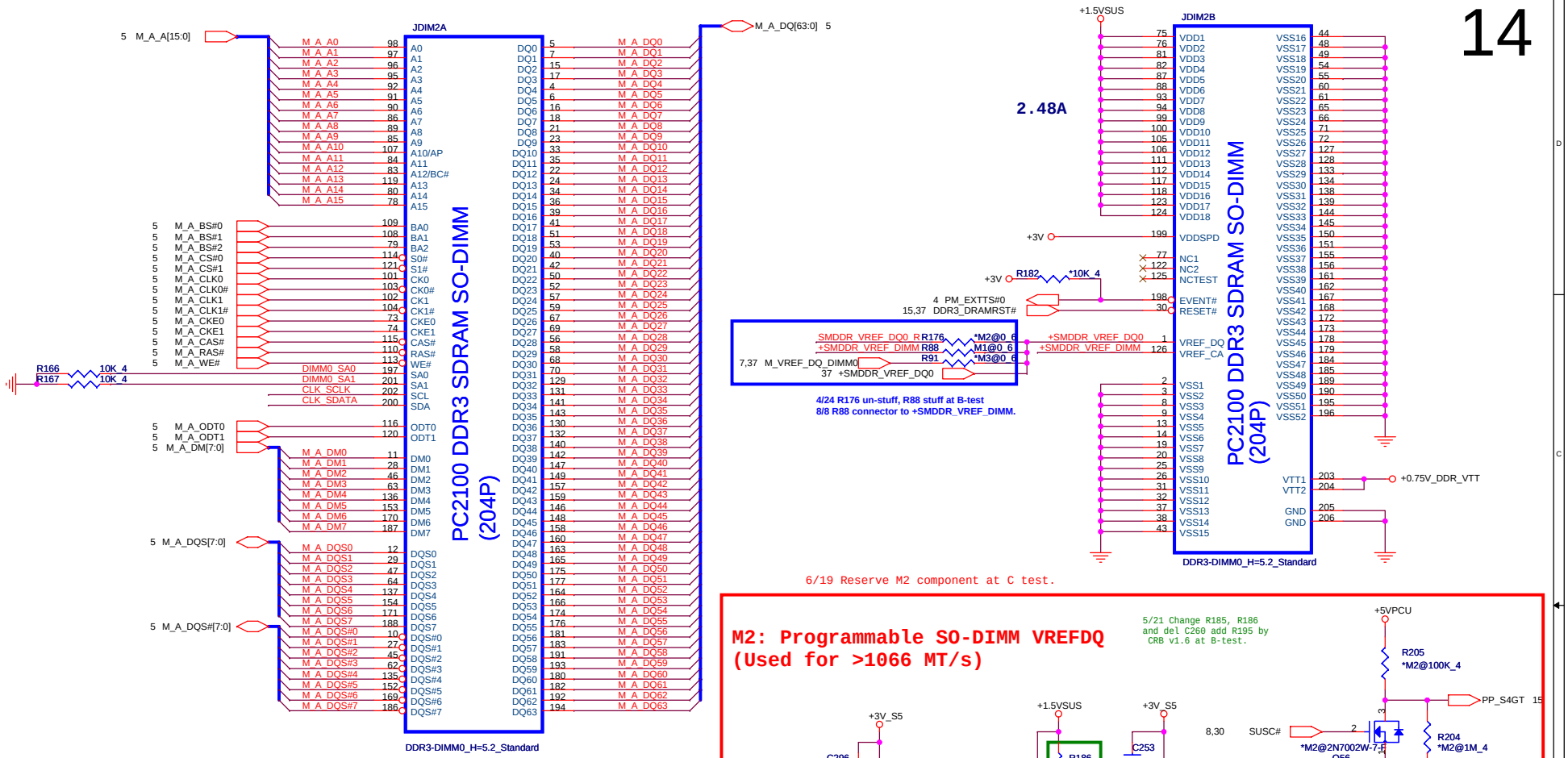
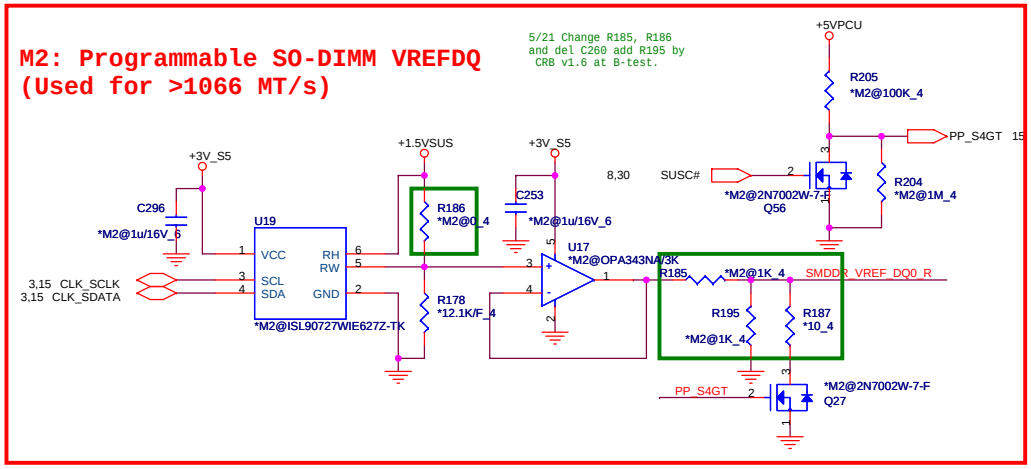
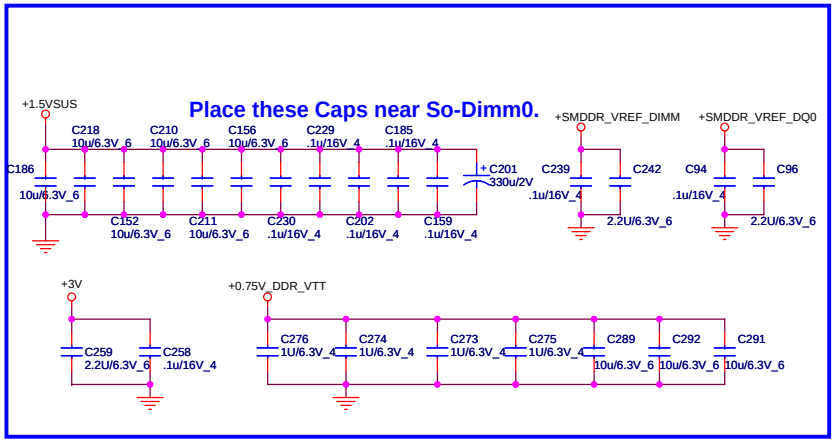
Size	Document Number	Rev
	IBEX PEAK-M 6/6	3A

Date: Tuesday, August 18, 2009 Sheet 13 of 42

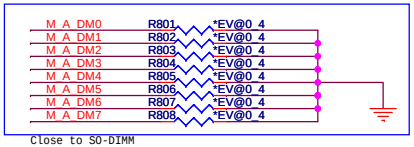


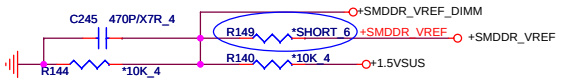
6/19 Reserve M2 component at C test.





6/22 Reserve R801~R808 at C test.





Quanta Computer Inc.

PROJECT : ZY9

Size	Document Number	Rev
	DDRIII SO-DIMM-0	3A
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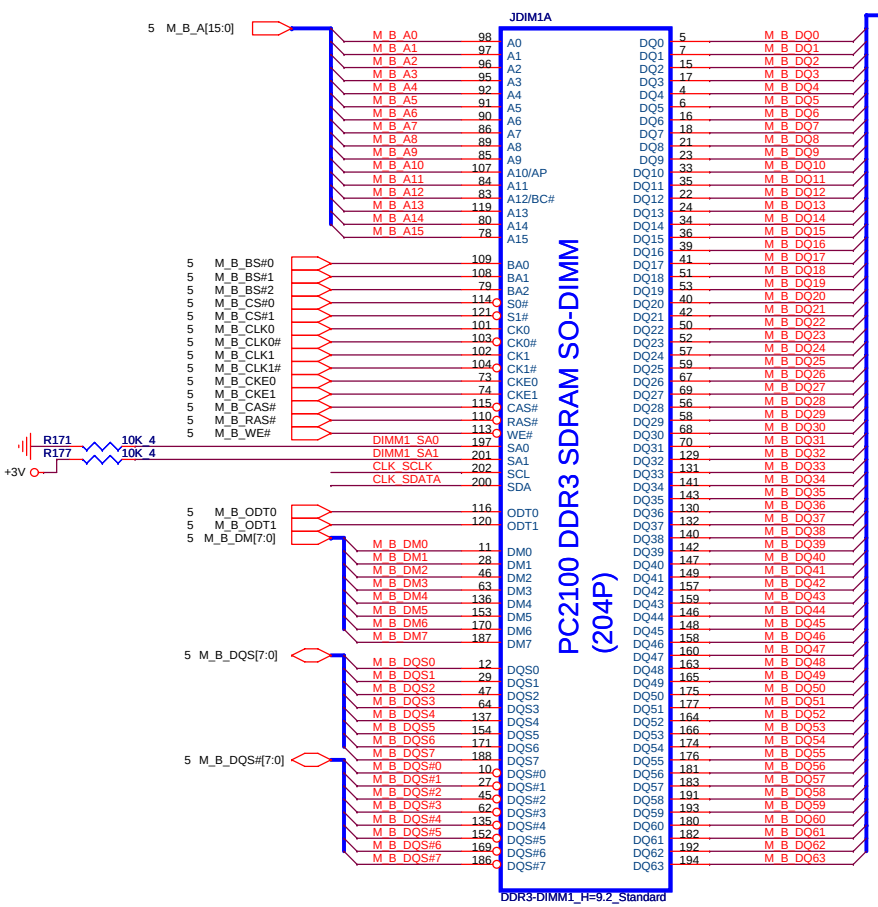
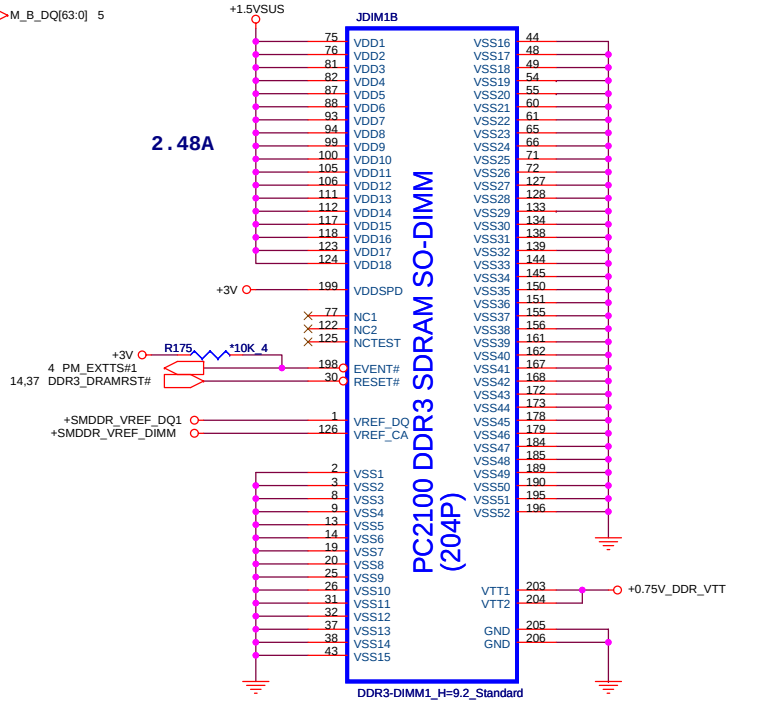
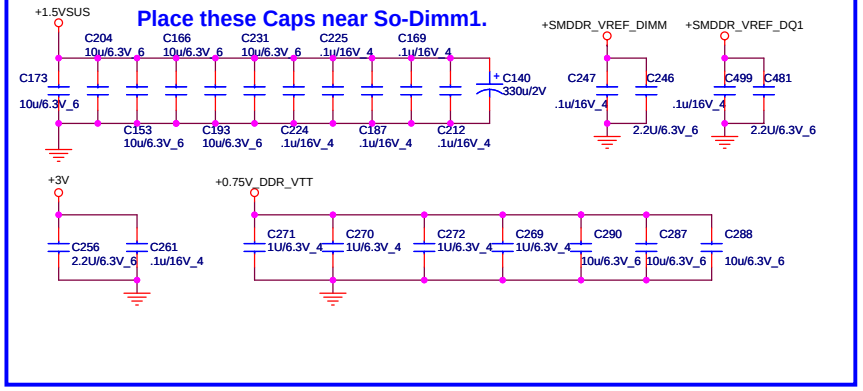
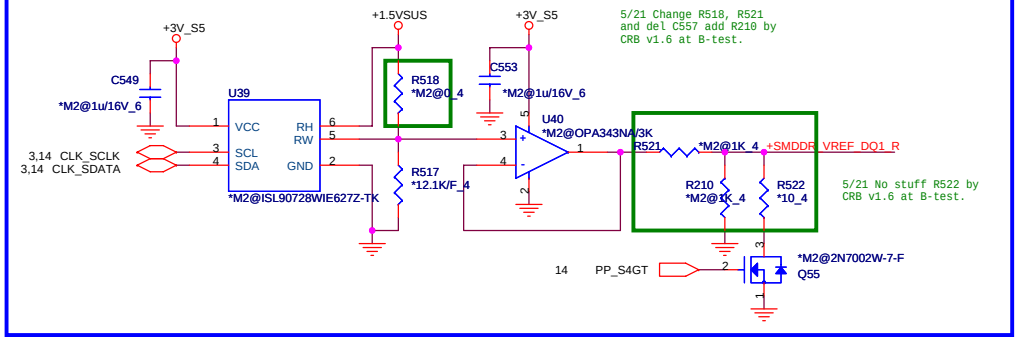




Place these Caps near So-Dimm1.

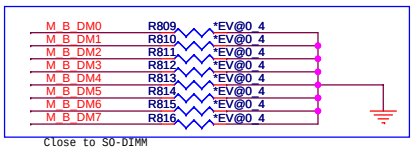


M2: Programmable SO-DIMM VREFDQ (Used for >1066 MT/s)



6/19 Reserve M2 component at C test.

6/22 Reserve R809~R816 at C test.



Quanta Computer Inc.

PROJECT : ZY9

Size	Document Number	Rev
	DDRIII SO-DIMM-1	3A

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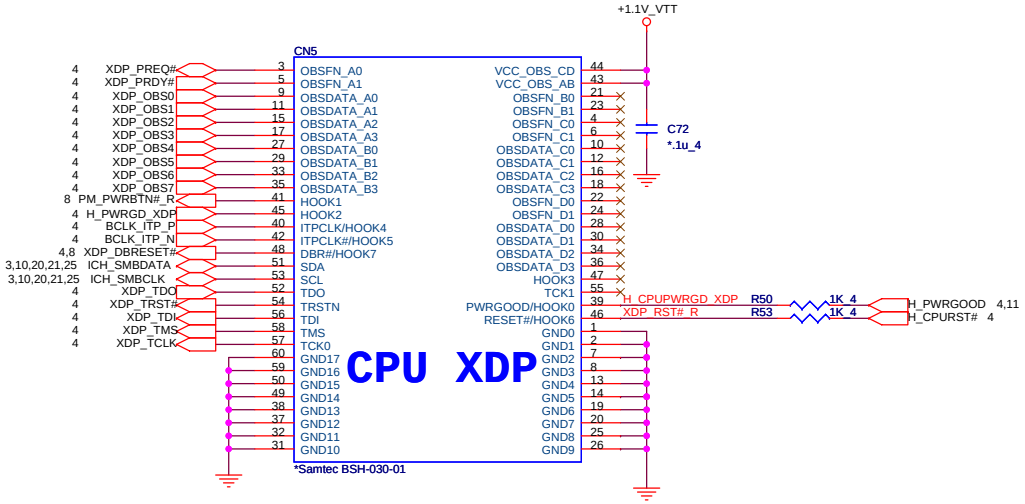

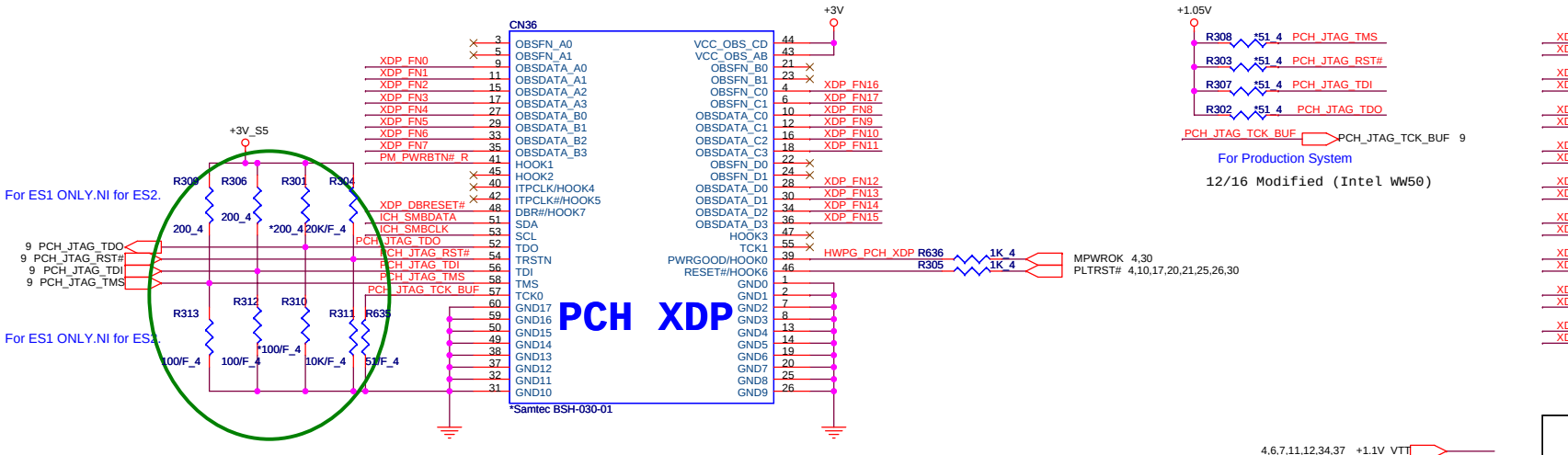

4/9 Modify JTAG table by change note ww15.3

4,6,7,11,12,34,37 +1.1V_VTT
3,10,12,22,35,37 +1.05V
3,4,8,9,10,11,12,14,15,17,18,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37 +3V
8,9,10,11,12,14,15,20,25,27,29,30,32,37 +3V_S5

Quanta Computer Inc.
PROJECT : ZY9

Size	Document Number	Rev
	XDP/BRAIDWOOD	3A

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MXM Module

6/25 Change CN22 pin define and footprint at C test.

At 11/21
update MXM footprint to mxm-mm70-314-310b1-1-270p

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM

MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	N/A	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

MXM3_2.0 CONNECTOR

MXM Reset

Thermo SMBus

Stuff isolate 2N7002 at C-test

change to 2N7002 at B-test

MXM VIN Power switch

MXM 3V/5V Power switch

At 11/14 Add it

Quanta Computer Inc.
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Size	Document Number	Rev
	MXM3.0	3A

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CRT

5/22 Change L9,L10,L13 to 75ohm by EMI at B test.

8/12 del R431~R437 at Ramp-test

17 EV_CRT_RED
17 EV_CRT_GRN
17 EV_CRT_BLU
17 EV_VSYNC
17 EV_HSYNC
17 EV_CRTDDAT
17 EV_CRTDCLK

1A/30V
D24
RSX101M-30
+5V
C423 .22u_4
CRTVDD5

EV_CRT_RED
EV_CRT_GRN
EV_CRT_BLU

L13 BLM18BA750SN1D
L10 BLM18BA750SN1D
L9 BLM18BA750SN1D

CRT_R1
CRT_G1
CRT_B1

R35 150/F_4
R30 150/F_4
R28 150/F_4
C48 10p/50V_4
C38 10p/50V_4
C28 10p/50V_4
C27 10p/50V_4
C30 10p/50V_4
C45 10p/50V_4

CN17
CRT
CRT_11
DDCDAT_1
CRTHSYNC
CRTVSYNC
DDCCLK_1

D3 MTW355
CRT_SENSE# 30
D4 *VPORT_6

+3V
C432 .1u_4
C425 22u/25V_6
CRT_BYP
C426 .1u_4

U29
VCC_SYNC SYNC_OUT2
SYNC_OUT1
VCC_DDC
BYP
VCC_VIDEO
SYNC_IN2
SYNC_IN1
VIDEO_1
VIDEO_2
VIDEO_3
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
GND
CM2009-02QR

CRT_VSYNC1
CRT_HSYNC1
EV_VSYNC
EV_HSYNC
EV_CRTDCLK
EV_CRTDDAT
DDCCLK_1
DDCDAT_1

R36 0_4
R29 0_4
R385 2.7K_4
R386 2.7K_4
R384 2.7K_4
R388 2.7K_4

C429 *.1u_4
C44 *10p/50V_4 CRTVSYNC
C31 *10p/50V_4 CRTHSYNC
C424 10p/50V_4 DDCCLK_1
C431 10p/50V_4 DDCDAT_1

LVDS

At 11/13 Modify

30 CONTRAST
17 EV_LVDS_BRIGHT
R401 0_4
R402 *0_4
LVDS_BRIGHT

3/11 NV request I2C pull-up 4.7K, and MXM module have 4.7K pull-up.

R397 4.7K_4
R398 4.7K_4

Remove R438, R639 at B-test

17 EV_LVDS_DDCDAT
17 EV_LVDS_DDCCLK
EV_LVDS_DDCDAT
EV_LVDS_DDCCLK

17 EV_LVDS_BLON
17 EV_LVDS_VDDEN
R656 *SHORT_4
R657 *SHORT_4
LVDS_BLON
LVDS_VDDEN

Reserve RV7,RV8 by ESD at B-test

RV7 *EGA-0402 DMIC_DAT
RV8 *EGA-0402 DMIC_CLK

+3V
C4 0.1u/50V_6
C2 1000p/50V_4
VIN
C3 4.7u/25V_8
C1 1000p/50V_4

0.8A
R3 *SHORT_8
R1 *SHORT_8
INVCC0
LCDVCC

CN1
GS12401-1011-40P-R-NH

EV_LVDS_DDCDAT
EV_LVDS_DDCCLK
LVDS_BRIGHT
BL_ON

23 DMIC_DAT
23 DMIC_CLK

17 EV_TXLCLKOUT+
17 EV_TXLCLKOUT-
EV_TXLCLKOUT+
EV_TXLCLKOUT-

17 EV_TXLOUT0+
17 EV_TXLOUT0-
EV_TXLOUT0+
EV_TXLOUT0-

17 EV_TXLOUT1+
17 EV_TXLOUT1-
EV_TXLOUT1+
EV_TXLOUT1-

17 EV_TXLOUT2+
17 EV_TXLOUT2-
EV_TXLOUT2+
EV_TXLOUT2-

17 EV_TXUCLKOUT+
17 EV_TXUCLKOUT-
EV_TXUCLKOUT+
EV_TXUCLKOUT-

17 EV_TXUOUT0+
17 EV_TXUOUT0-
EV_TXUOUT0+
EV_TXUOUT0-

17 EV_TXUOUT1+
17 EV_TXUOUT1-
EV_TXUOUT1+
EV_TXUOUT1-

17 EV_TXUOUT2+
17 EV_TXUOUT2-
EV_TXUOUT2+
EV_TXUOUT2-

10 USBP8+
10 USBP8-

LCD Power

+15V
R15 330K_6
+3VPCU
R11 100K_4
Q4 PDTC143TT
LVDS_VDDEN
R10 100K_4
LCDONG
C9 .01u/25V_4
Q7 2N7002D
+3V
65mil
Q6 AO3404
LCDVCC1
65mil
R9 22_8
LCDDISCHG
LCDON#
Q3 2N7002D
L2 *SHORT_6
L1 *SHORT_6
65mil
LCDVCC
C410 .1u/16V_4
C409 .01u/16V_4
C7 22U_8

Backlight Control

+3V
R2 10K_4
R14 10K_4
BL_ON
D2 BAS316
LID591# 29,30
BL#
Q2 2N7002D
Q1 DTC144EUA
EC_FPBACK# 30
LVDS_BLON
Q5 2N7002D
R13 100K_4

Quanta Computer Inc.
PROJECT : ZY9

Size	Document Number	Rev
	CRT/LVDS/LID	3A

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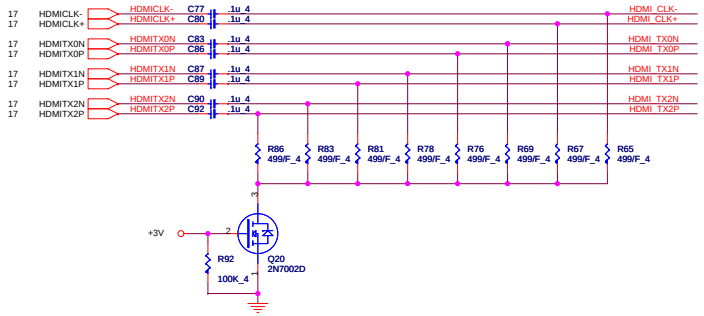
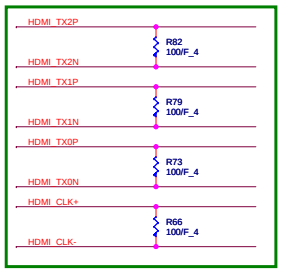
HDMI

TMDS (DC-coupled)
DP(AC-coupled)

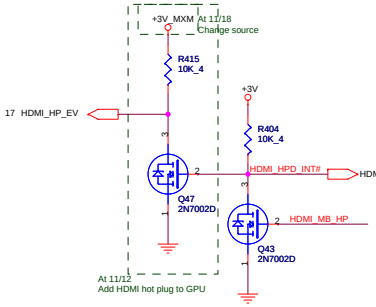


5/14 Stuff R82,R79,R73,R66 by EMI at B test.



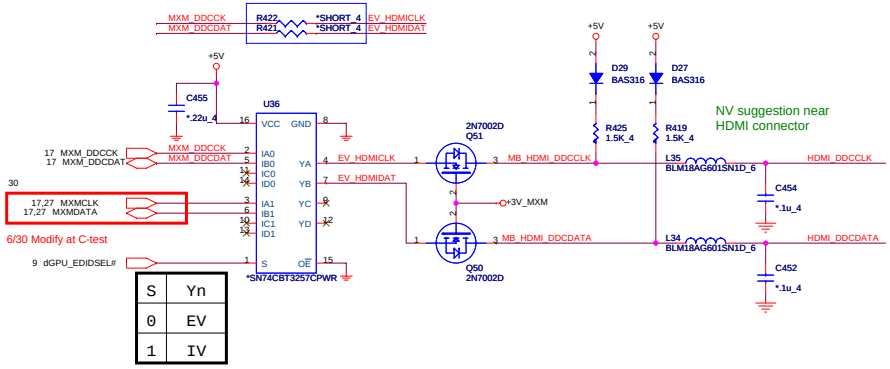
Close CN27

HDMI Hot-PLUG to SB and GPU



SDVO I2C Control

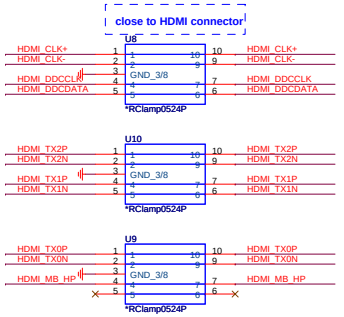
Bypass(default)



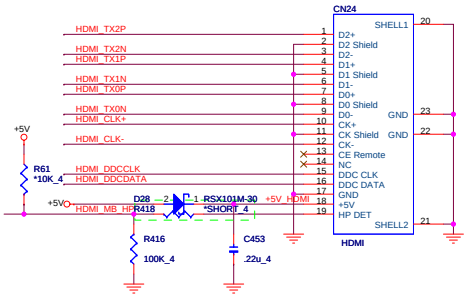
S	Yn
0	EV
1	IV

ESD Protect

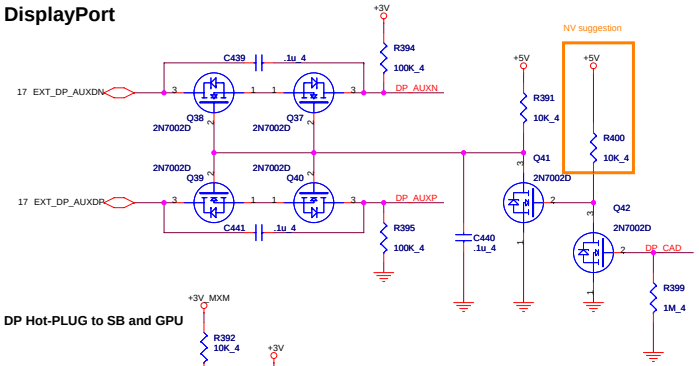
close to HDMI connector



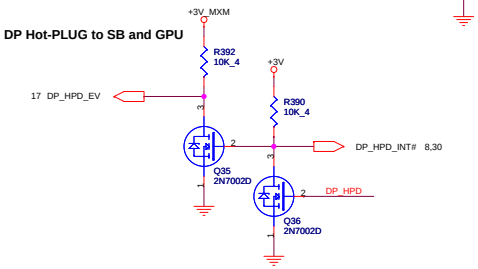
HDMI connector



DisplayPort



DP Hot-PLUG to SB and GPU

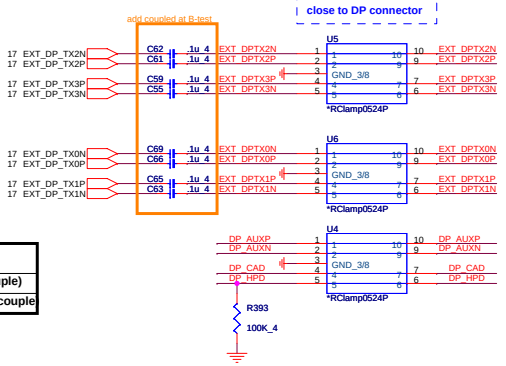


DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple

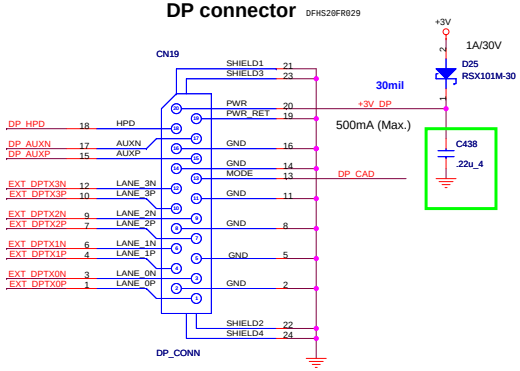
ESD Protect

close to DP connector

add coupled at B-test



DP connector DFHS20FR029



Quanta Computer Inc.
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HDMI/DP
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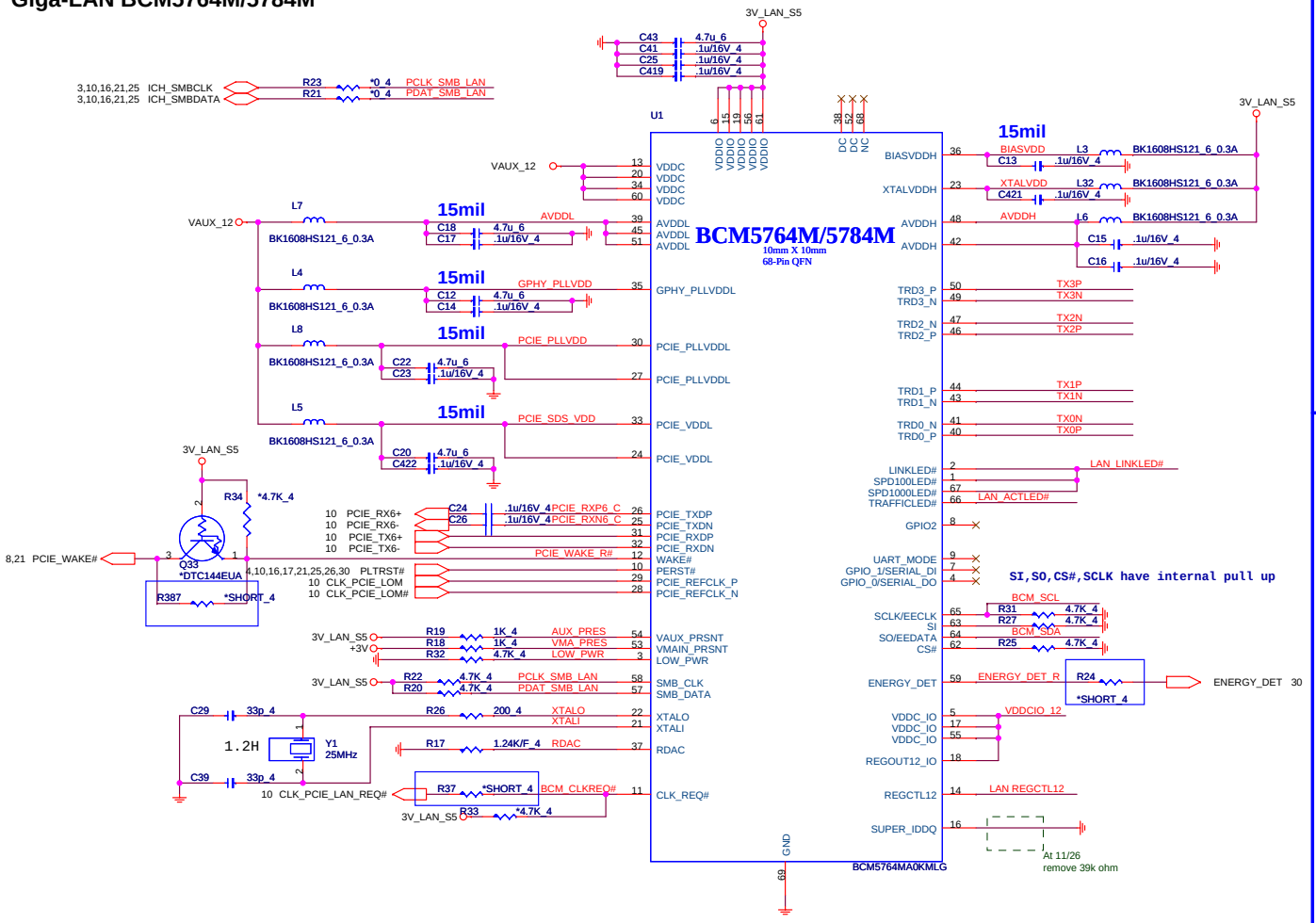
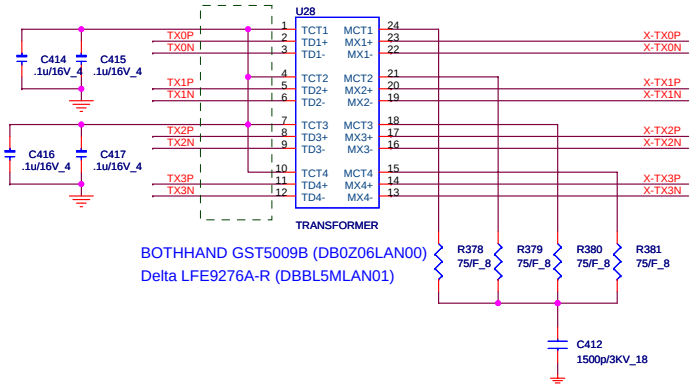
Giga-LAN BCM5764M/5784M

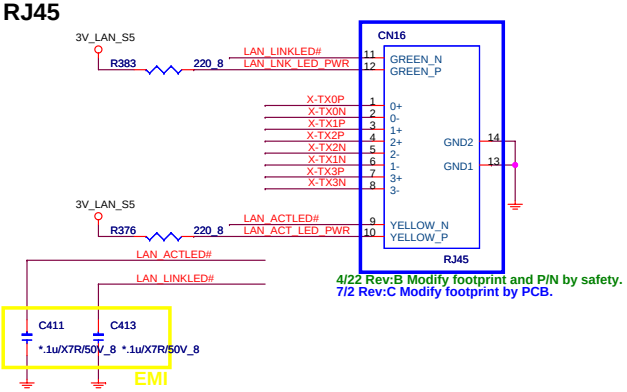


TRANSFORMER

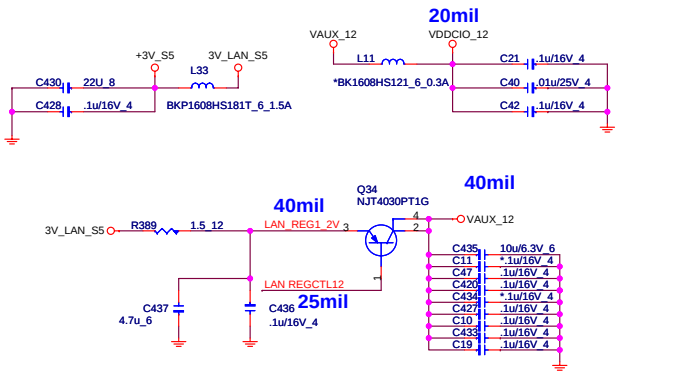
At 11/26
TCT1-4 pin connect toghter



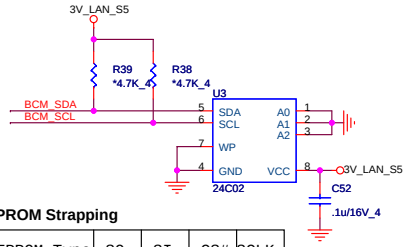
RJ45



LAN POWER



EEPROM



EEPROM Strapping

EEPROM Type	SO	SI	CS#	SCLK
24c02	1	0	0	0

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	LAN (BCM5764M/5784M)	3A

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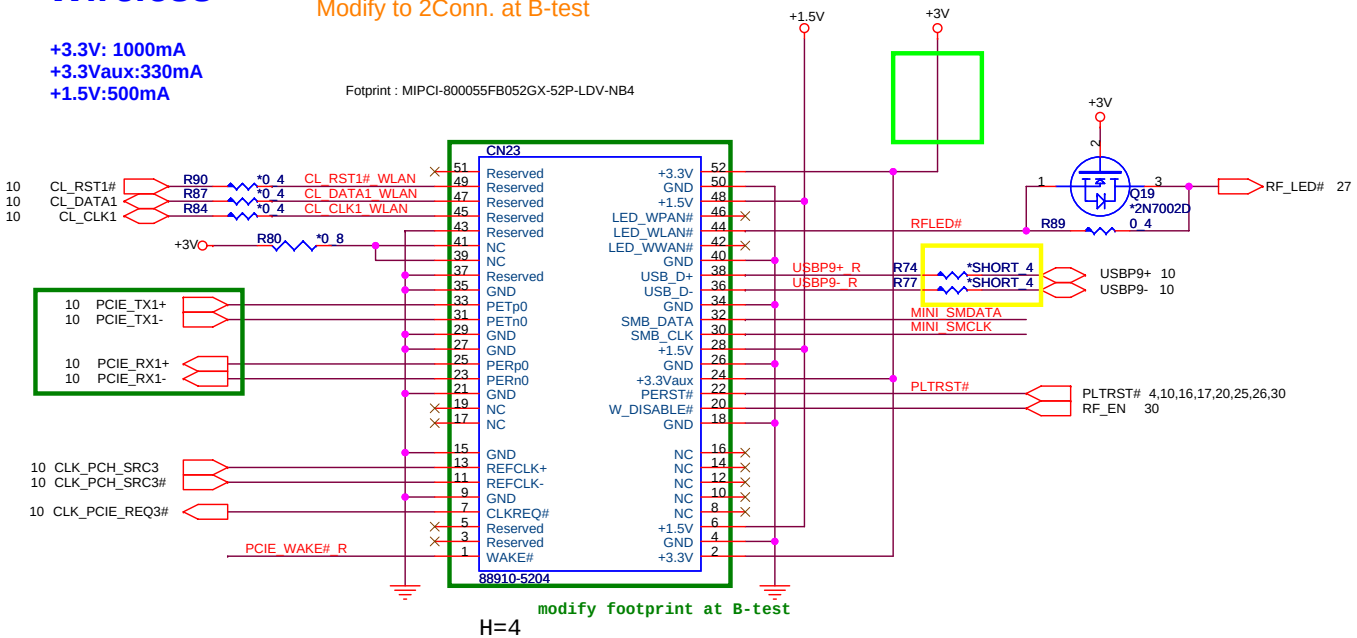
Wireless

Modify to 2Conn. at B-test

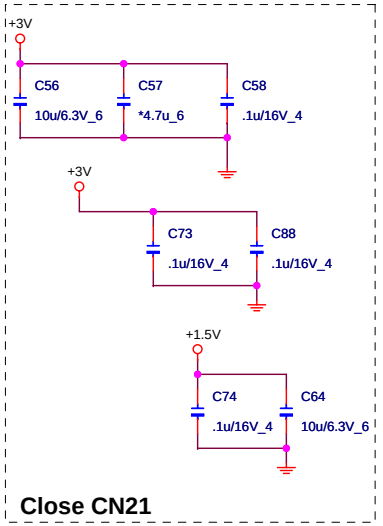
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

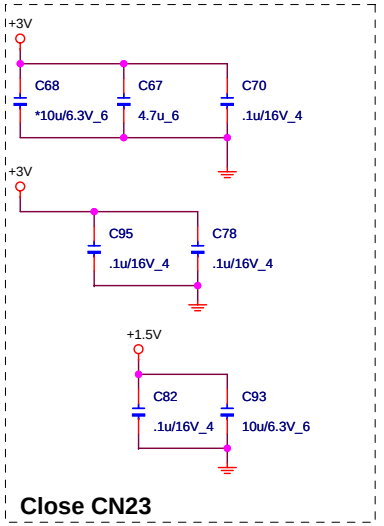
Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4



modify footprint at B-test

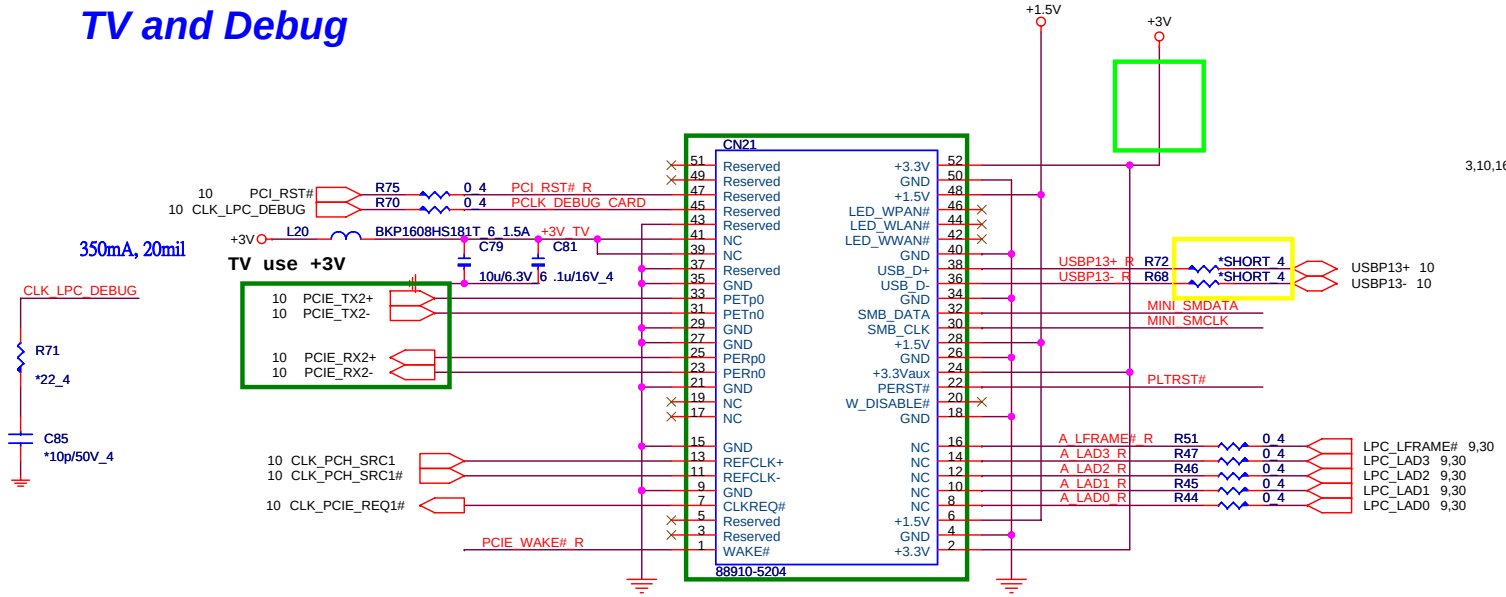
H=4





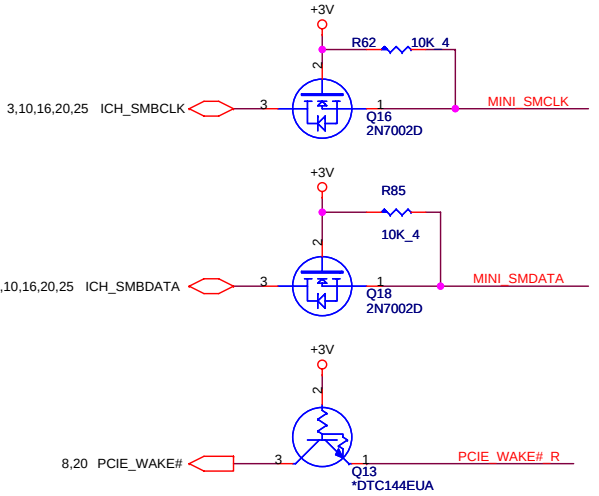
5/14 Change PCIE sequence beween CN21 and CN23 by BIOS at B-test.

TV and Debug



modify footprint at B-test

H=9



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	MINI PCI-E card/TV	3A
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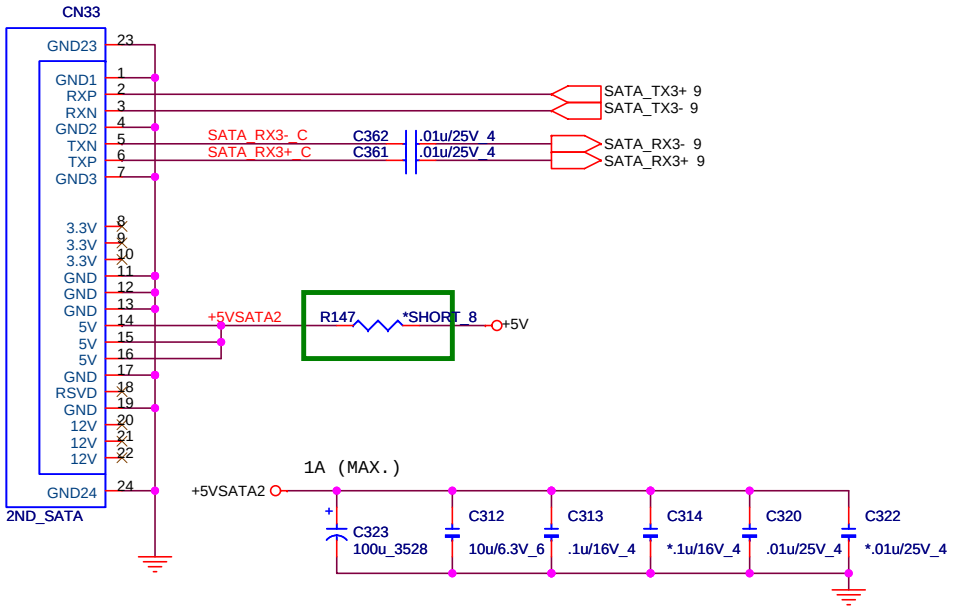
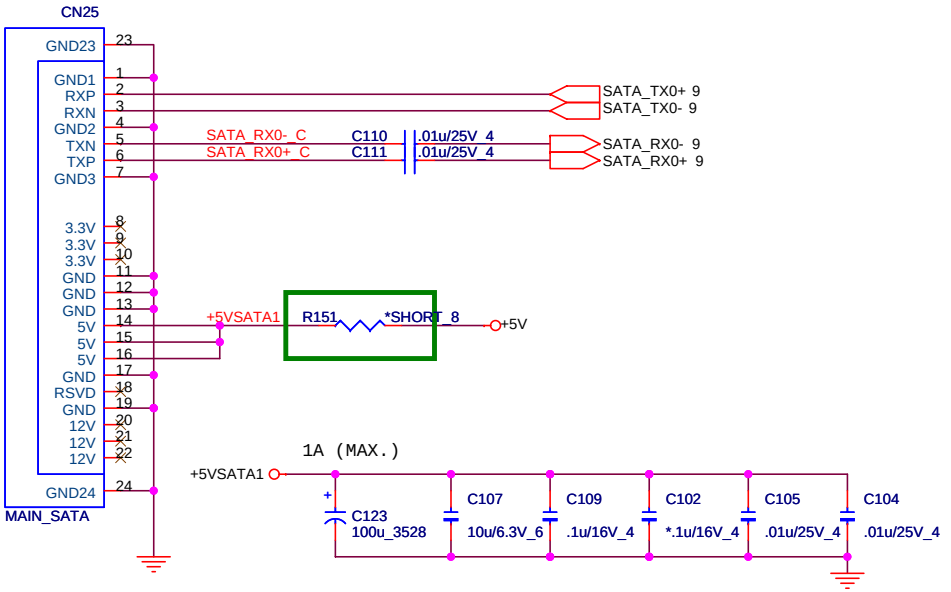
2nd SATA HDD (edge of board)

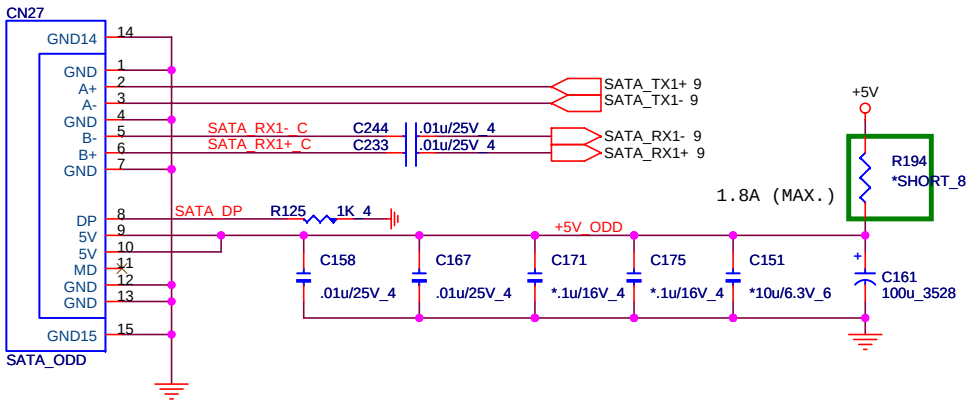


5/13 Add R147,R151,R197 for power consumption measure at B-test.

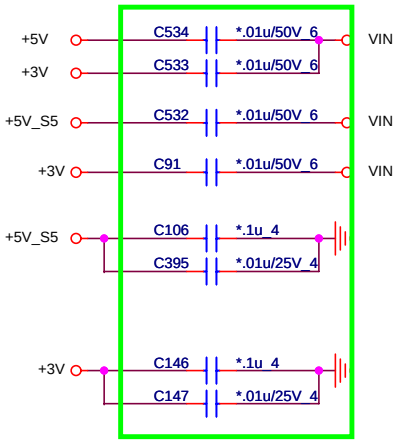
MAIN SATA HDD

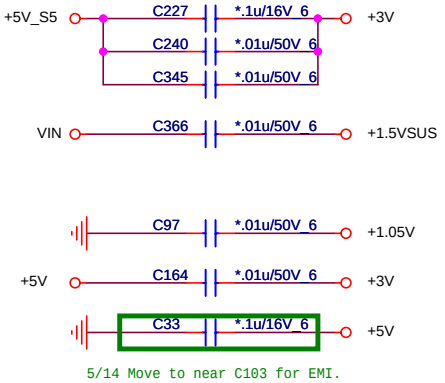


ODD (SATA)



EE RETURN-PATH CAPACITORS





5/14 Move to near C103 for EMI.

Quanta Computer Inc.

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	SATA-HDD/ODD	3A
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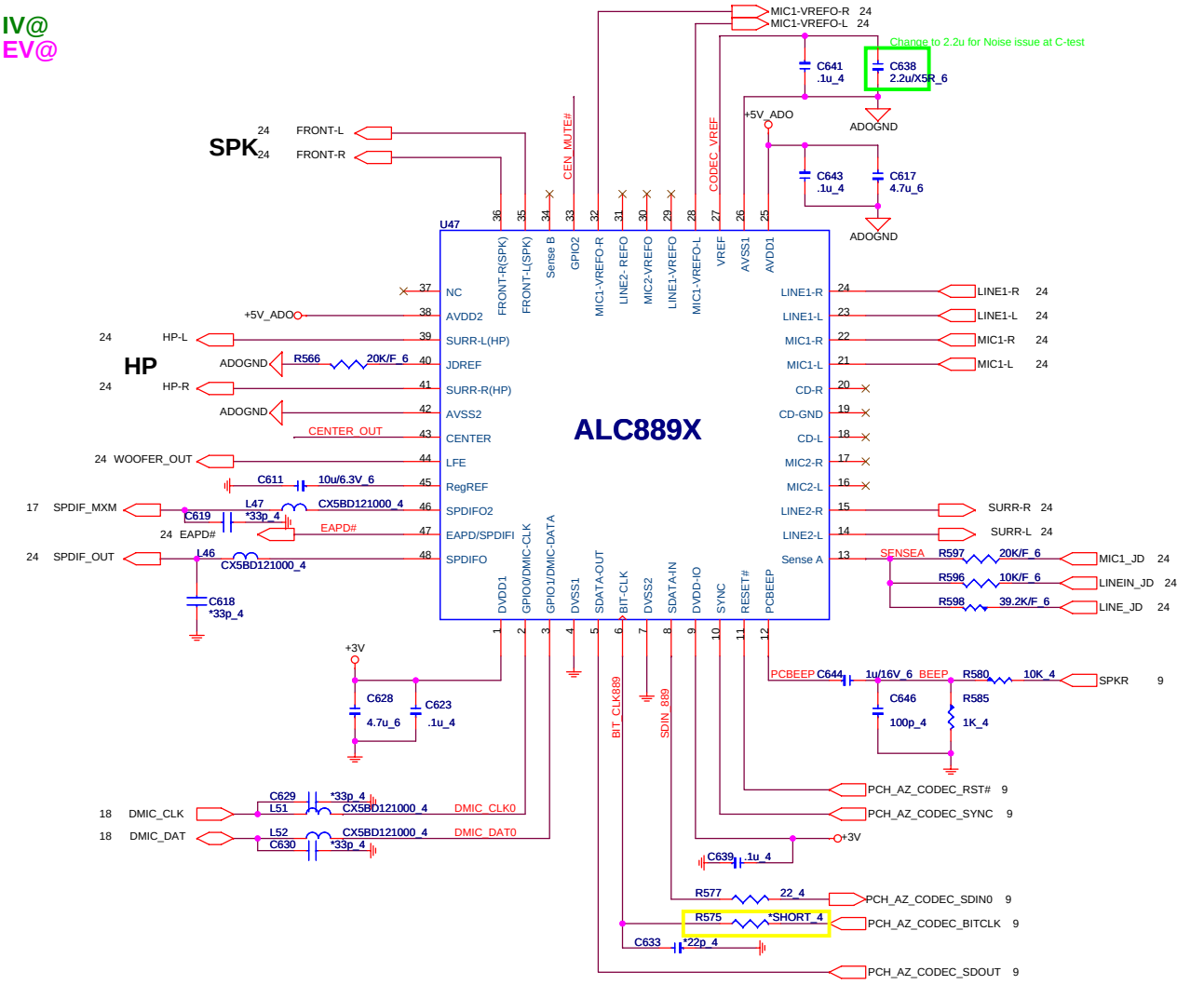
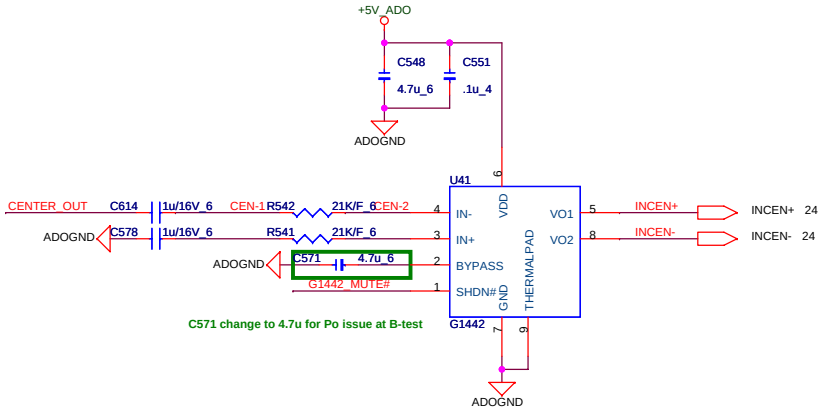
CODEC(ALC889X)

IV@
EV@

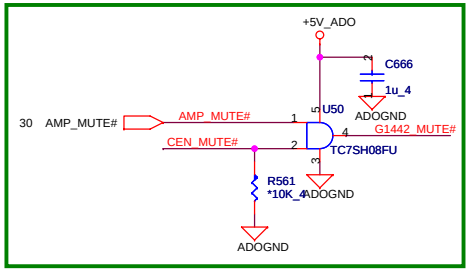


CENTER MONO

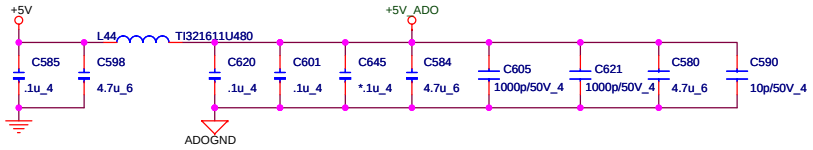


EAPD pin

5/11: Add U50, C666 and R561 for Po issue at B-test



CODEC/AMP Power



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Size	Document Number	Rev
	REALTEK ALC889X/MONO-AMP	3A
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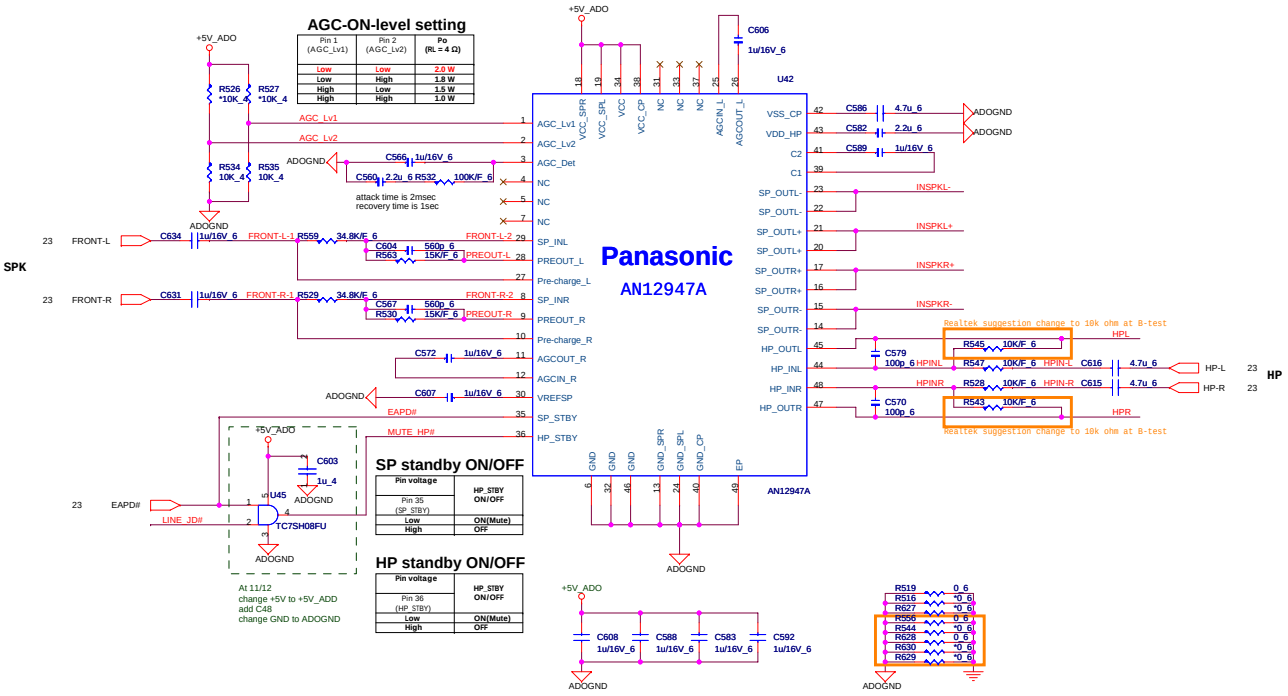
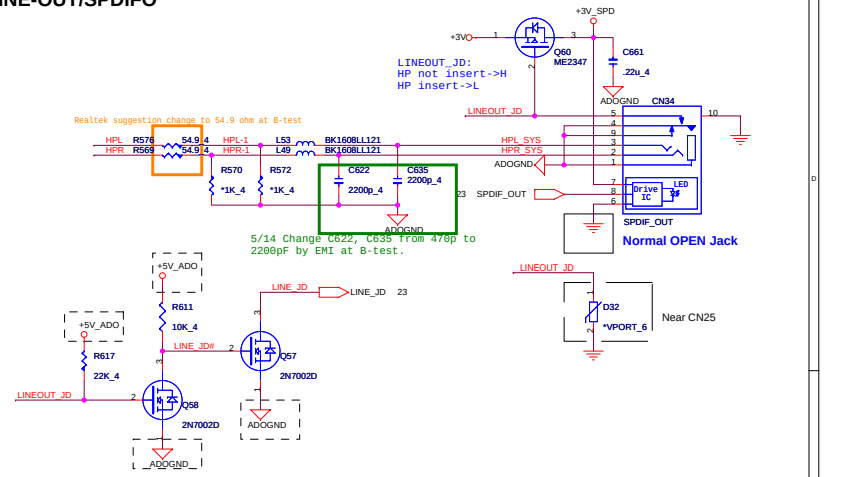
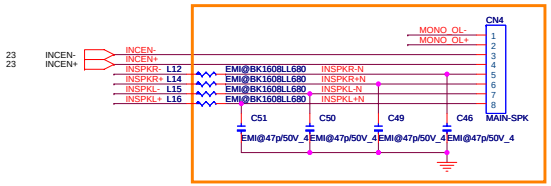
SPEAKER/HP AMP.



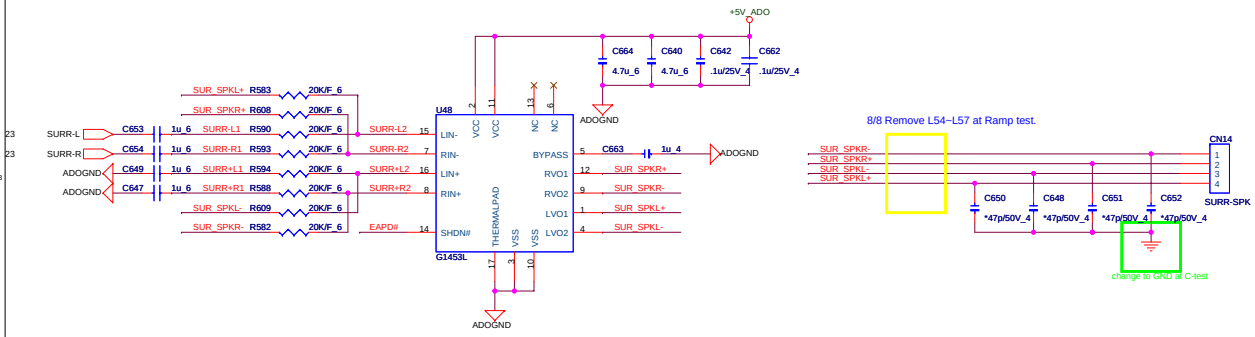
LINE-OUT/SPDIFO



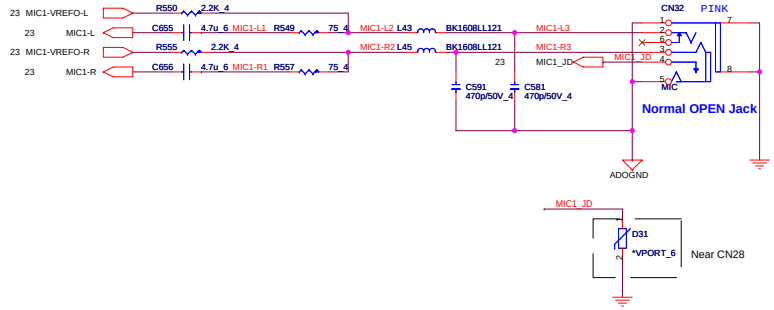
Main SPK/Center/Subwoofer EMI



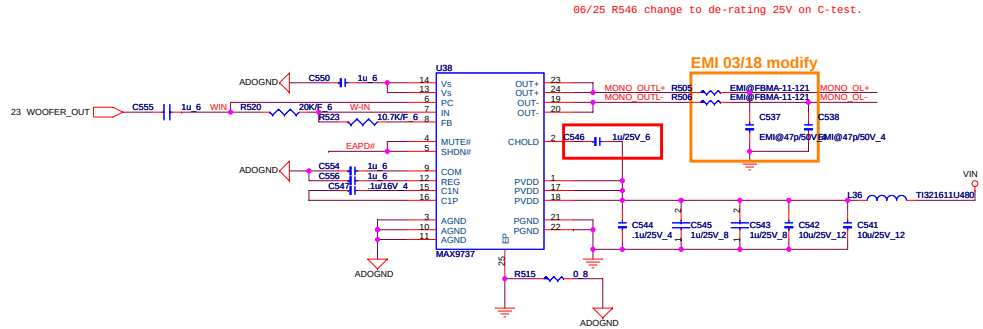
SURR-SPK



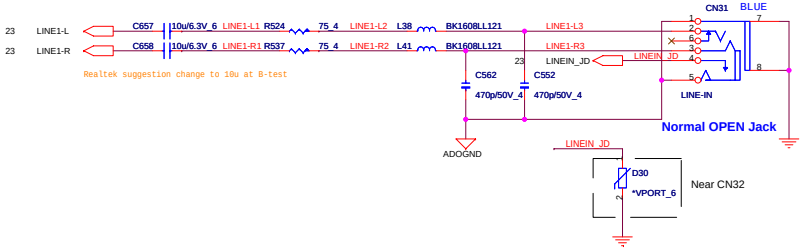
MIC



SUBWOOFER



LINE IN



Quanta Computer Inc.			
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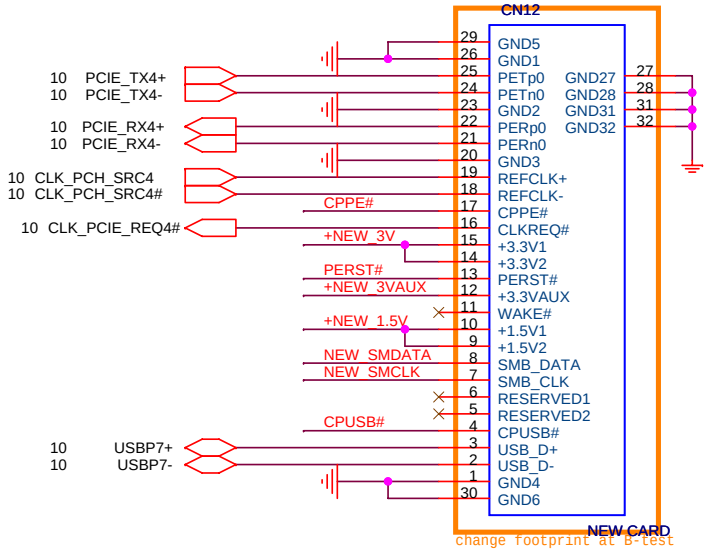
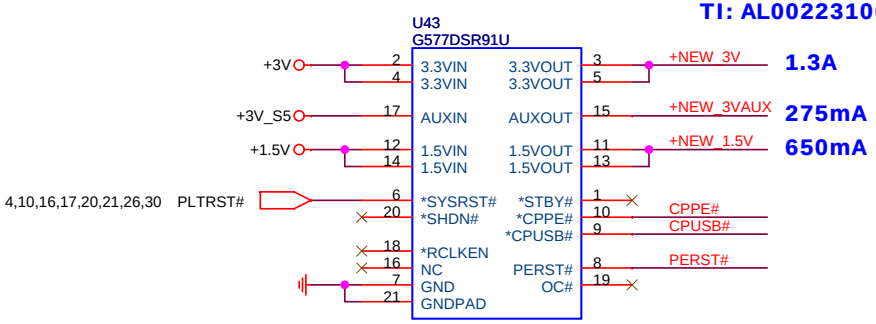
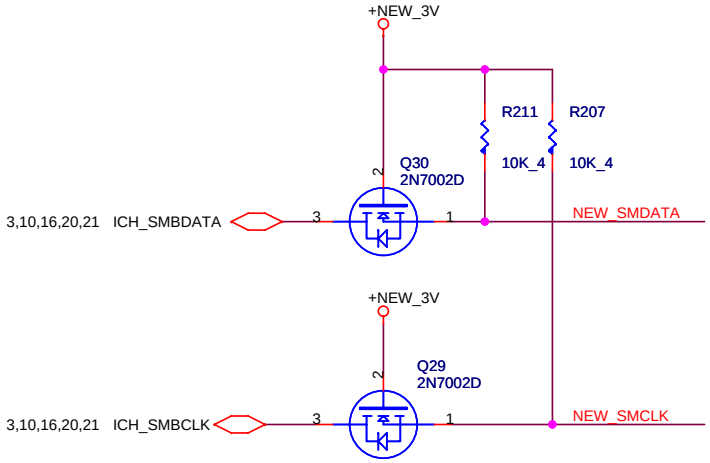
NEW CARD

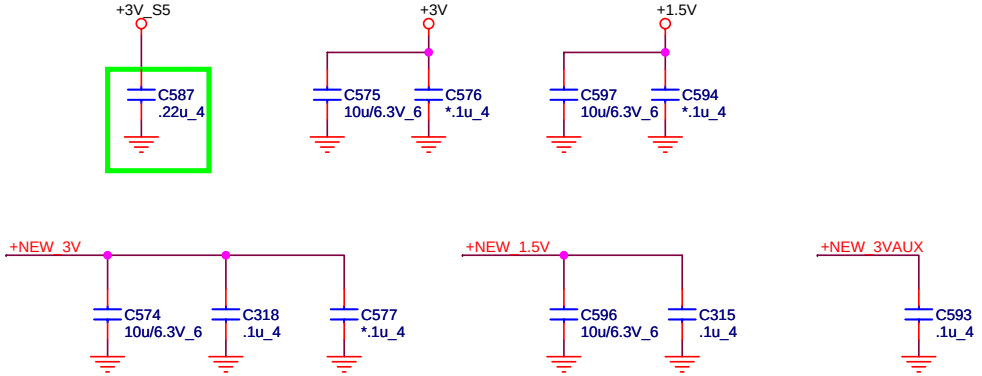


At 11/18
Change GMT cost down version.

NEW CARD'S POWER SWITCH **GMT: AL000577002** **TI: AL002231000**







Quanta Computer Inc.
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Size	Document Number	Rev
	NEW CARD	3A
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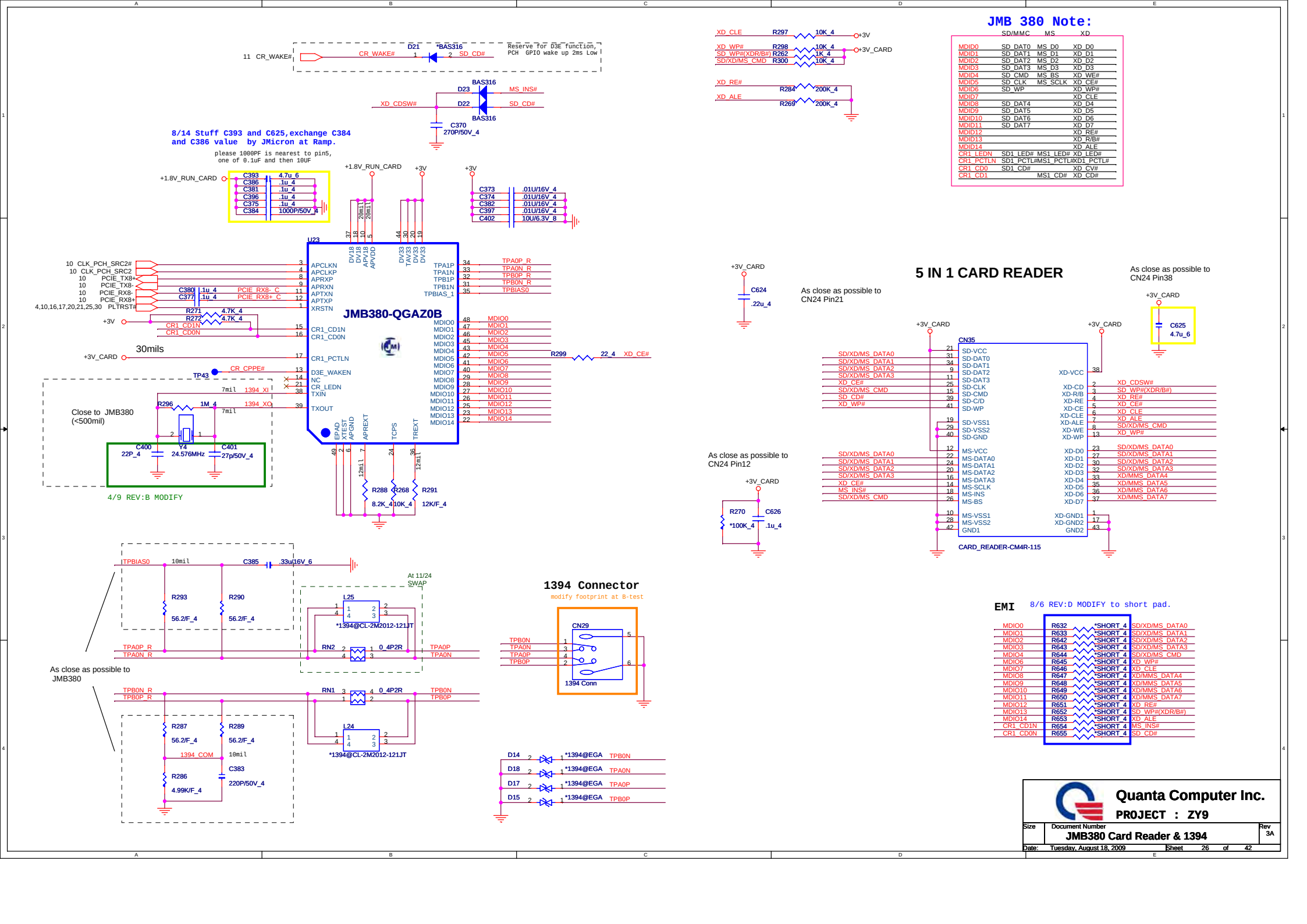
JMB 380 Note:
SD/MMC MS XD
MDID0 SD_DAT0 MS_D0 XD_D0
MDID1 SD_DAT1 MS_D1 XD_D1
MDID2 SD_DAT2 MS_D2 XD_D2
MDID3 SD_DAT3 MS_D3 XD_D3
MDID4 SD_CMD MS_BS XD_WE#
MDID5 SD_CLK MS_SCLK XD_CE#
MDID6 SD_WP XD_WP#
MDID7 XD_CLE
MDID8 SD_DAT4 XD_D4
MDID9 SD_DAT5 XD_D5
MDID10 SD_DAT6 XD_D6
MDID11 SD_DAT7 XD_D7
MDID12 XD_RE#
MDID13 XD_R/B#
MDID14 XD_ALE
CR1_LEDN SD1_LED# MS1_LED# XD_LED#
CR1_PCTLN SD1_PCTL# MS1_PCTL# XD1_PCTL#
CR1_CD0 SD1_CD# XD_CV#
CR1_CD1 MS1_CD# XD_CD#
XD_CLE R297 10K_4 +3V
XD_WP# R298 10K_4
SD_WP#(XDR/B#) R262 1K_4 +3V_CARD
SD/XD/MS_CMD R300 10K_4
XD_RE# R284 200K_4
XD_ALE R269 200K_4
11 CR_WAKE#
CR_WAKE# D21 *BAS316 SD_CD#
Reserve for D3E function, PCH GPIO wake up 2ms Low
D23 BAS316 MS_INS#
XD_CDSW# D22 SD_CD#
C370 270P/50V_4
8/14 Stuff C393 and C625,exchange C384 and C386 value by JMicron at Ramp.
please 1000PF is nearest to pin5, one of 0.1uF and then 10UF
+1.8V_RUN_CARD
C393 4.7u_6
C386 .1u_4
C381 .1u_4
C396 .1u_4
C375 .1u_4
C384 1000P/50V_4
+1.8V_RUN_CARD +3V +3V
C373 .01U/16V_4
C374 .01U/16V_4
C382 .01U/16V_4
C397 .01U/16V_4
C402 10U/6.3V_8
U23
JMB380-QGAZ0B
10 CLK_PCH_SRC2#
10 CLK_PCH_SRC2
10 PCIE_TX8+
10 PCIE_TX8-
10 PCIE_RX8-
10 PCIE_RX8+
4,10,16,17,20,21,25,30 PLTRST#
C380 .1u_4 PCIE_RX8- C
C377 .1u_4 PCIE_RX8+ C
R271 4.7K_4
R272 4.7K_4
+3V
CR1_CD1N
CR1_CD0N
30mils
+3V_CARD
CR_CPPE#
TP43
7mil 1394_XI
1394_XO
R296 1M_4
Close to JMB380 (<500mil)
C400 22P_4
Y4 24.576MHz
C401 27p/50V_4
4/9 REV:B MODIFY
TPA0P_R
TPA0N_R
TPB0P_R
TPB0N_R
TPBIAS0
MDIO0
MDIO1
MDIO2
MDIO3
MDIO4
MDIO5
MDIO6
MDIO7
MDIO8
MDIO9
MDIO10
MDIO11
MDIO12
MDIO13
MDIO14
R299 22_4 XD_CE#
R288 8.2K_4
R268 10K_4
R291 12K/F_4
+3V_CARD
C624 .22u_4
As close as possible to CN24 Pin21
5 IN 1 CARD READER
As close as possible to CN24 Pin38
+3V_CARD
C625 4.7u_6
CN35
SD/XD/MS_DATA0
SD/XD/MS_DATA1
SD/XD/MS_DATA2
SD/XD/MS_DATA3
XD_CE#
SD/XD/MS_CMD
SD_CD#
XD_WP#
SD-VCC SD-DAT0 SD-DAT1 SD-DAT2 SD-DAT3 SD-CLK SD-CMD SD-C/D SD-WP SD-VSS1 SD-VSS2 SD-GND
MS-VCC MS-DATA0 MS-DATA1 MS-DATA2 MS-DATA3 MS-SCLK MS-INS MS-BS MS-VSS1 MS-VSS2 GND1
XD-VCC XD-CD XD-R/B XD-RE XD-CE XD-CLE XD-ALE XD-WE XD-WP XD-D0 XD-D1 XD-D2 XD-D3 XD-D4 XD-D5 XD-D6 XD-D7 XD-GND1 XD-GND2 GND2
XD_CDSW#
SD_WP#(XDR/B#)
XD_RE#
XD_CE#
XD_CLE
XD_ALE
SD/XD/MS_CMD
XD_WP#
SD/XD/MS_DATA0
SD/XD/MS_DATA1
SD/XD/MS_DATA2
SD/XD/MS_DATA3
XD/MMS_DATA4
XD/MMS_DATA5
XD/MMS_DATA6
XD/MMS_DATA7
CARD_READER-CM4R-115
As close as possible to CN24 Pin12
+3V_CARD
R270 *100K_4
C626 .1u_4
TPBIAS0 10mil C385 .33u/16V_6
R293 56.2/F_4
R290 56.2/F_4
At 11/24 SWAP
L25
*1394@CL-2M2012-121JT
RN2 0_4P2R
TPA0P_R TPA0N_R TPA0P TPA0N
As close as possible to JMB380
TPB0N_R TPB0P_R
RN1 0_4P2R
L24
*1394@CL-2M2012-121JT
R287 56.2/F_4
R289 56.2/F_4
1394_COM 10mil C383 220P/50V_4
R286 4.99K/F_4
TPB0N TPA0N TPA0P TPB0P
1394 Connector
modify footprint at B-test
CN29
1394 Conn
D14 D18 D17 D15 *1394@EGA
EMI 8/6 REV:D MODIFY to short pad.
MDIO0 R632 *SHORT_4 SD/XD/MS_DATA0
MDIO1 R633 *SHORT_4 SD/XD/MS_DATA1
MDIO2 R642 *SHORT_4 SD/XD/MS_DATA2
MDIO3 R643 *SHORT_4 SD/XD/MS_DATA3
MDIO4 R644 *SHORT_4 SD/XD/MS_CMD
MDIO6 R645 *SHORT_4 XD_WP#
MDIO7 R646 *SHORT_4 XD_CLE
MDIO8 R647 *SHORT_4 XD/MMS_DATA4
MDIO9 R648 *SHORT_4 XD/MMS_DATA5
MDIO10 R649 *SHORT_4 XD/MMS_DATA6
MDIO11 R650 *SHORT_4 XD/MMS_DATA7
MDIO12 R651 *SHORT_4 XD_RE#
MDIO13 R652 *SHORT_4 SD_WP#(XDR/B#)
MDIO14 R653 *SHORT_4 XD_ALE
CR1_CD1N R654 *SHORT_4 MS_INS#
CR1_CD0N R655 *SHORT_4 SD_CD#
Quanta Computer Inc.
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JMB380 Card Reader & 1394
Rev 3A
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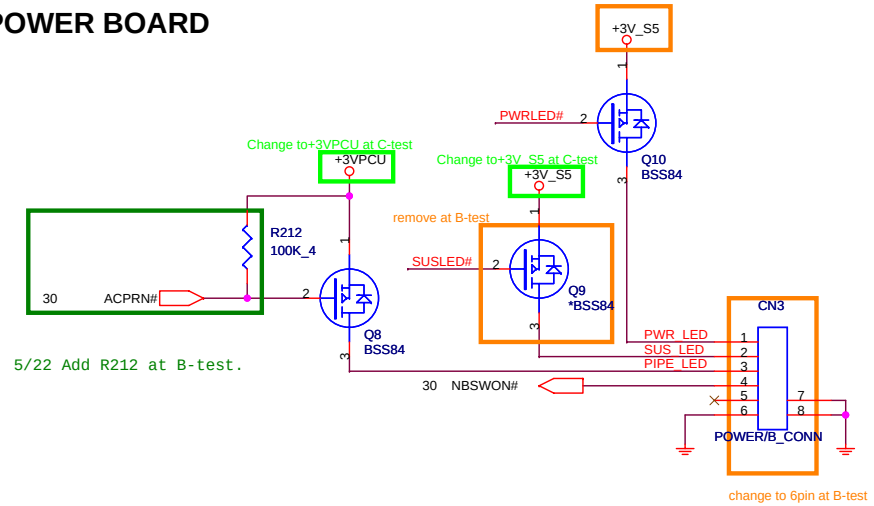
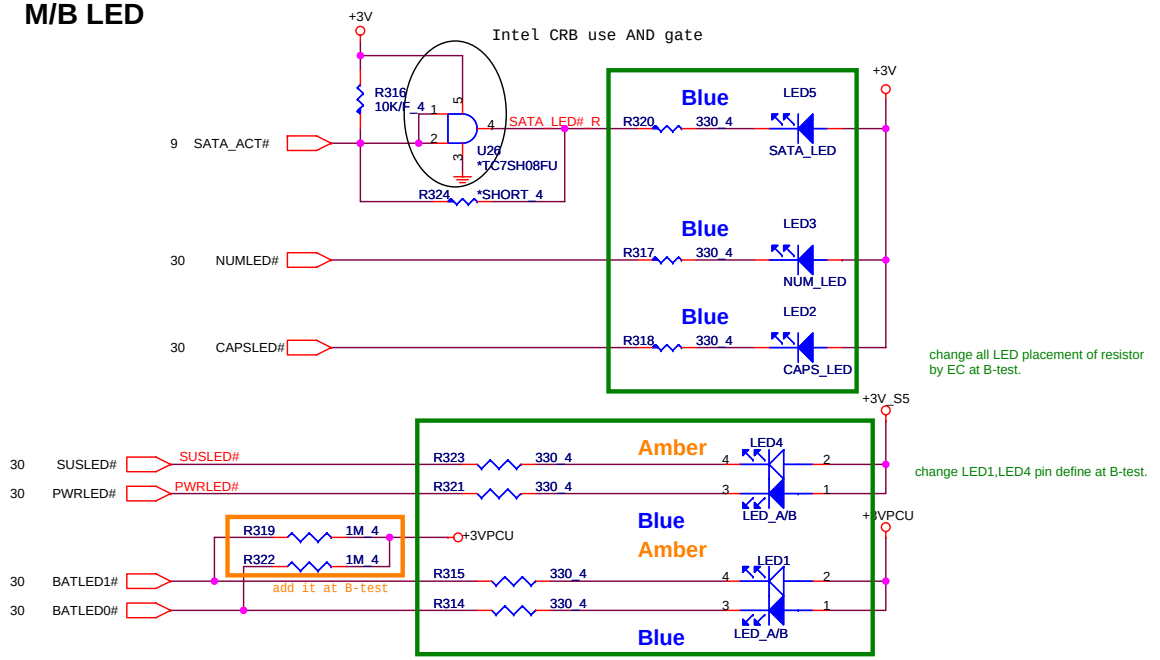
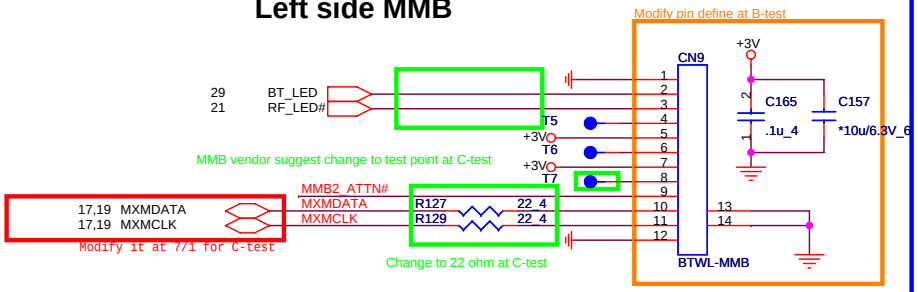
POWER BOARD



M/B LED

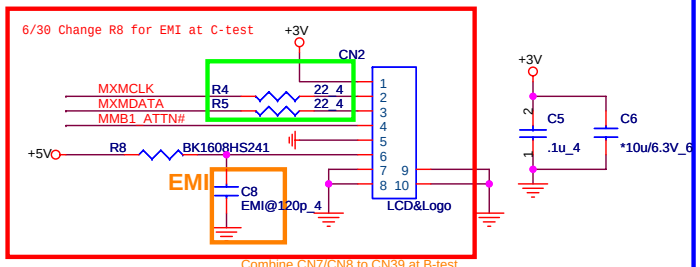


Left side MMB

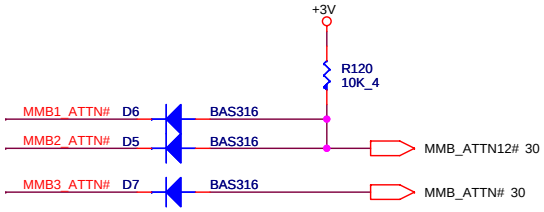


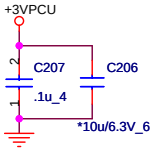
MXMCLK=MXM_SMCLK; MXMDATA=MXM_SMDATA12
MMB1 and MMB2 need add ISOLATE circuit where are on MXM page.

LCD BL_ON/OFF MMB & Backlight Logo LED

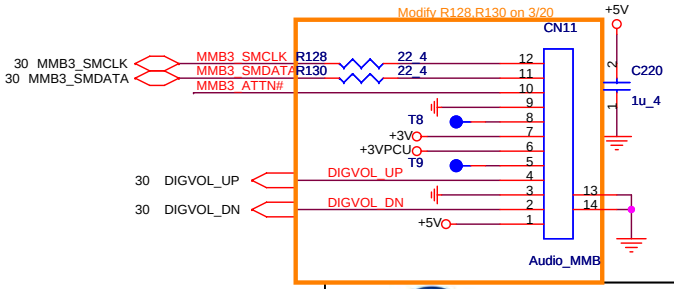


MMB Status





Right Side MMB



Quanta Computer Inc.
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	POWER/MMB/LAUNCH/LED	3A
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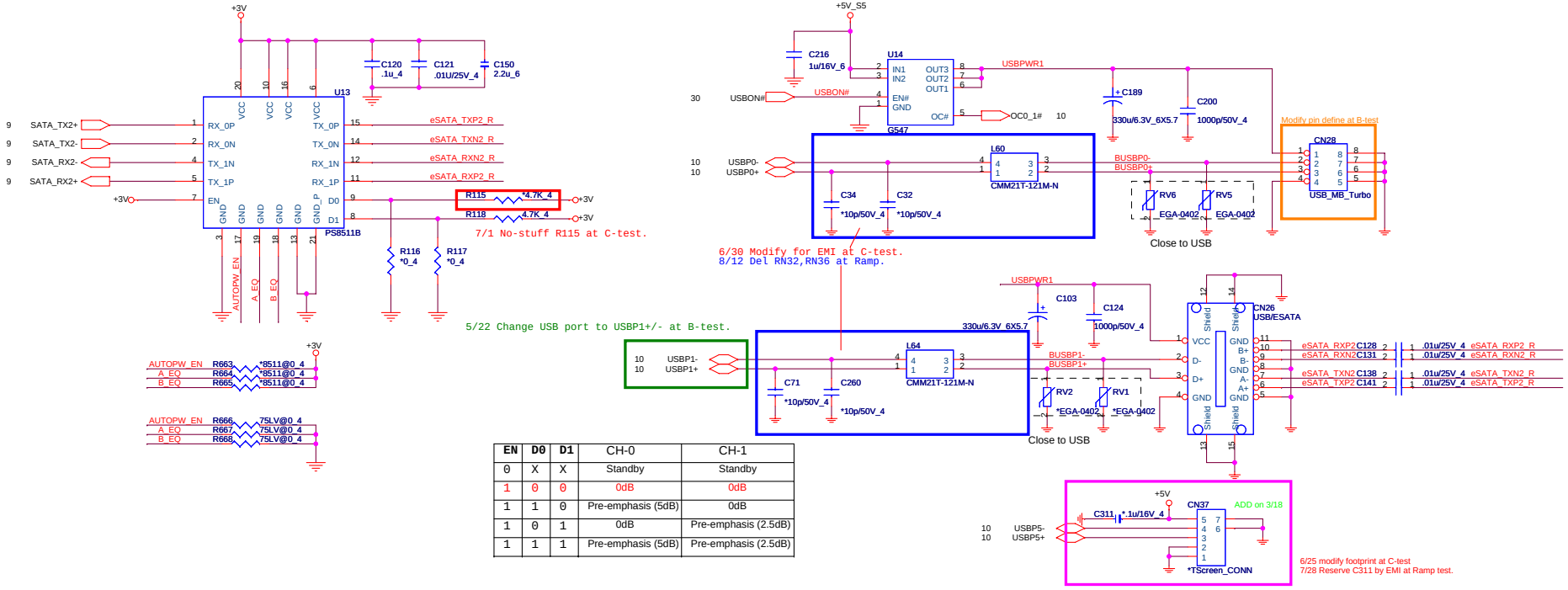
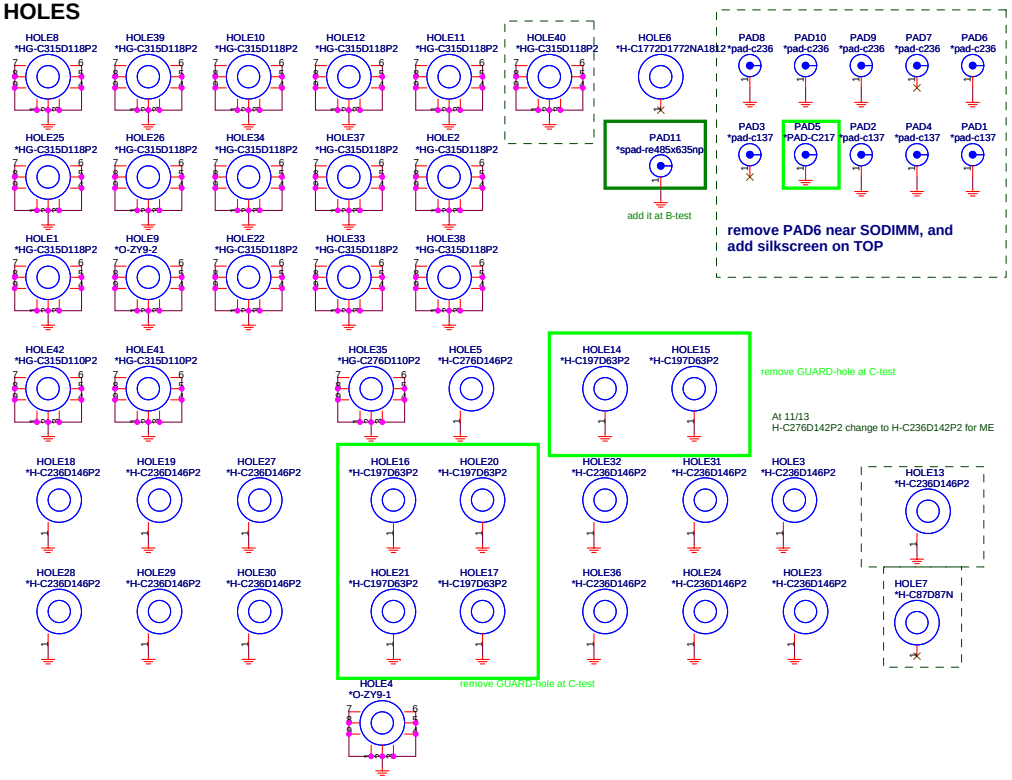
USB & ESATA

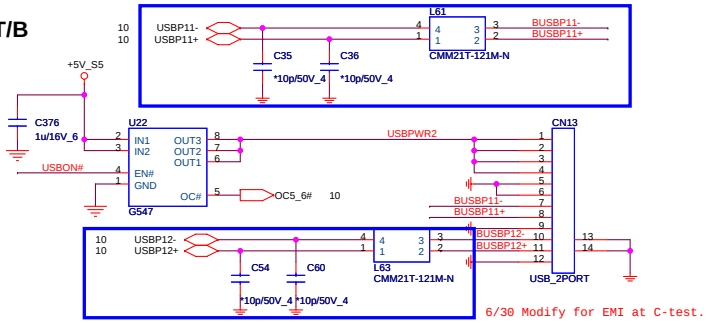


EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (2.5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (2.5dB)

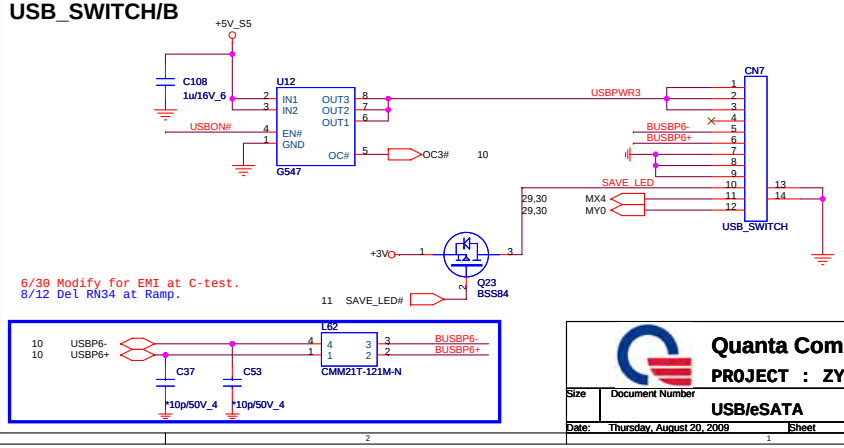
HOLES



USB_2PORT/B



USB_SWITCH/B



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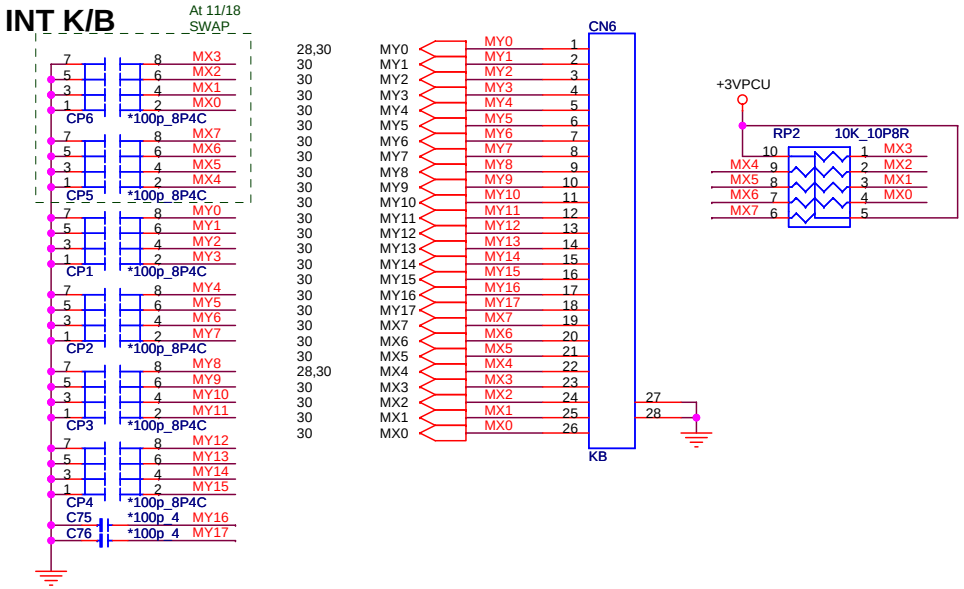
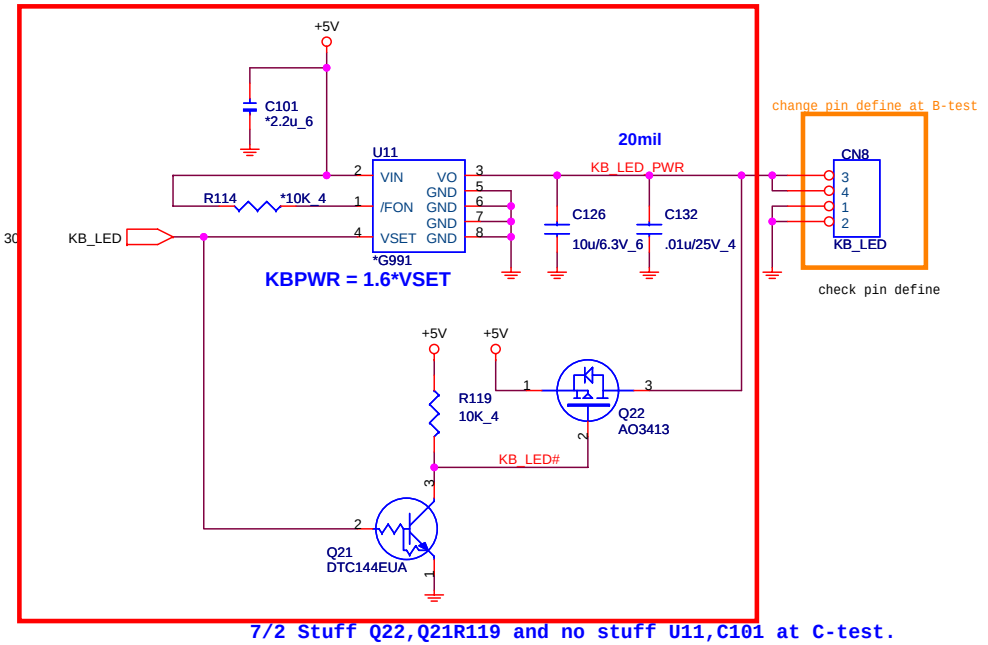
INT K/B

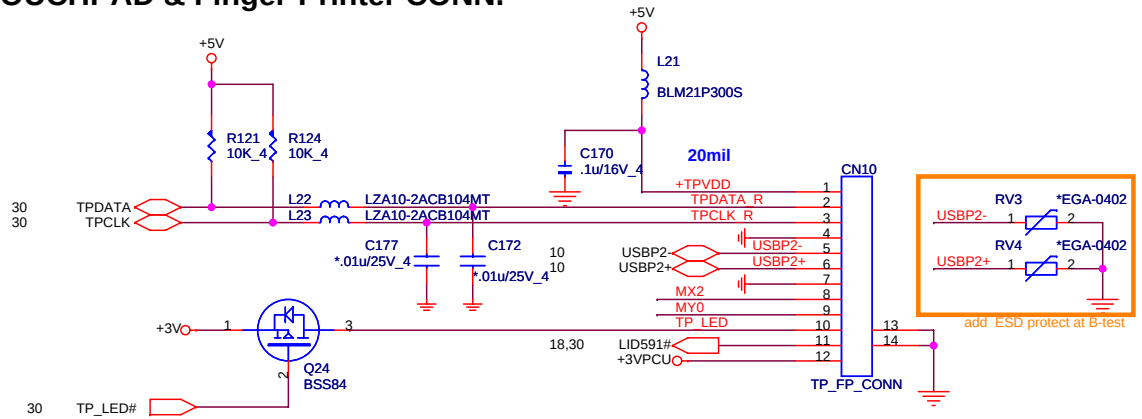


Keyboard LED control

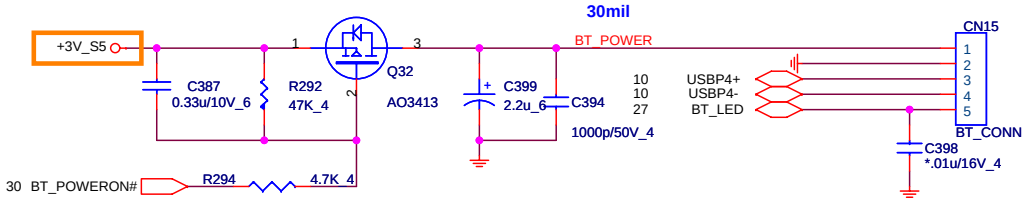


7/2 Stuff Q22,Q21R119 and no stuff U11,C101 at C-test.

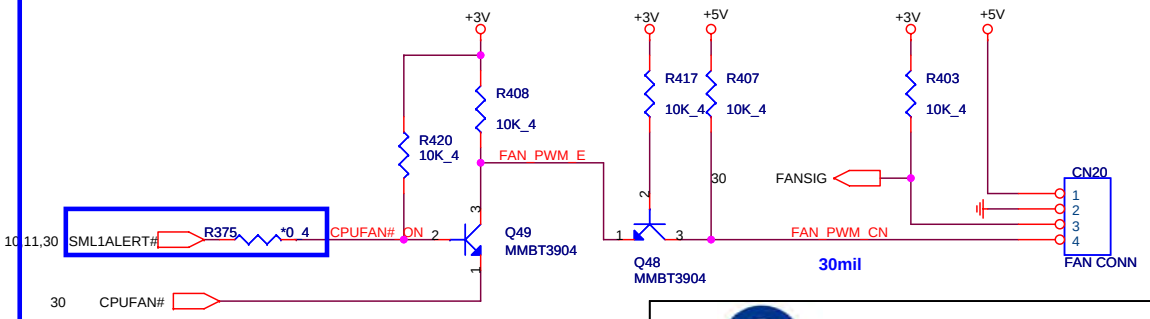
TOUCHPAD & Finger-Printer CONN.



BLUETOOTH CONNECTOR



CPU FAN



5/13 Reserve R375 by EC at B-test.
6/25 Stuff R375 by EC at C-test.
7/22 Un-stuff R375 by EC at Ramp.

Quanta Computer Inc.		
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EC

6/19 Change R196 to 2.2 by EC at C-test.

+3VPCU L27 BK1608HS220_6_1A 30mil C265 .1u/16V_4 C267 10u/6.3V_6 +A3VPCU

E775AGND

+3VPCU R196 2.2_6 +3VPCU_EC 0.03A(30mils) C235 4.7u_6 C295 .1u/16V_4 C268 *.1u/16V_4 C263 .1u/16V_4 C250 *.1u/16V_4 C215 .1u/16V_4

U16

VCC1 VCC2 VCC3 VCC4 VCC5 AVCC VDD

LFRAME LAD0 LAD1 LAD2 LAD3 LCLK

9,21 LPC_LFRAME# LPC_LFRAME# 3
9,21 LPC_LAD0 LPC_LAD0 126
9,21 LPC_LAD1 LPC_LAD1 127
9,21 LPC_LAD2 LPC_LAD2 128
9,21 LPC_LAD3 LPC_LAD3 1
10 CLK_PCI_775 CLK_PCI_775 2

CLK_PCI_775 R168 *22_4 C255 *10p/50V_4

8 CLKRUN# GPIO11/CLKRUN 8
11 SIO_A20GATE GA20 121
11 SIO_RCIN# KBRST 122
11 SIO_EXT_SCI# D13 BAS16 SCI#_uR ECSCI/GPIO54 29
18 EC_FPBACK# EC_FPBACK# GPIO24/LDRQ 6
37 +V1.1S1.5S_PWRGD +V1.1S1.5S_PWRGD GPIO10/LPCPD 124
4,10,16,17,20,21,25,26 PLTRST# PLTRST# LRESET 7
28 USBON# USBON# GPIO67/PWUREQ 123
9 IRQ_SERIRQ IRQ_SERIRQ SERIRQ 125
11 SIO_EXT_SMI# GPIO65/SMI 9

Del R190 at C-test

LPC

A/D: GPI90/AD0 GPI91/AD1 GPI92/AD2 GPI93/AD3 GPIO05/AD4 GPIO04/AD5

97 TEMP_MBAT 31
98 SML1ALERT# 10,11,29
99 TPD_TRIP
100 ICMNT 31
108 DIGVOL_UP DIGVOL_UP 27
96 DIGVOL_DN DIGVOL_DN 27

D/A: GPI94/DA0 GPI95/DA1 GPI96/DA2 GPI97/DA3

101 S5_DIS 32
105 KB_LED 29
106 TP_LED# 29
107 MAINON_DIS 37

5/19 Add D42 near JP1 at B-test.

GPIO: GPIO01/TB2 GPIO03/AD6 GPIO06 GPIO07/AD7 GPIO23/SCL3 GPIO30/CIRTX2 GPIO31/SDA3 GPIO32/D_PWM GPIO33/H_PWM GPIO36/TB3 GPIO40/F_PWM GPIO42/TCK GPIO43/TMS GPIO44/TDI GPIO45/E_PWM GPIO46/CIRRXM/TRST GPIO47/SCL4 GPIO50/TDO GPIO51/TA3 GPIO52/CIRTX2/RDY GPIO53/SDA4 GPIO81 GPO82/TRIS GPO84/BADDR0 GPIO41

64 NBSWON# R D42 BAS16
95 LID591#
93 ACIN 17,31
NBSWON# 27
LID591# 18,29
94 SUSB# 8
119 MMB3_SMCLK MMB3_SMCLK 27
109 ACPRN# 27
120 MMB3_SMDATA MMB3_SMDATA 27
65 BATLED0# BATLED0# 27
66 BATLED1# BATLED1# 27
15 VRON 33
16 SUSLED# SUSLED# 27
17 MXMPWR_EN 17
20 AMP_MUTE# 23
21 DDR3_DRAMRST#_EC DDR3_DRAMRST#_EC 11,37
22 CPUPWM 23
23 MMB_ATTN# 27
24 MXM_SMCLK12 17
25 D/C# 31
26 S5_ON 32,41
27 HDMI_HPD_INT# 19
28 MXM_SMDATA12 17
91 DNBSWON# 8
110 CL_RST_OUT T11
112 BADDR0_EC_R
80 DP_HPD_INT# 8,19

Modify Net name on 3/17

KB: KBSIN0 KBSIN1 KBSIN2 KBSIN3 KBSIN4 KBSIN5 KBSIN6 KBSIN7

29 MX0 MX0 54
29 MX1 MX1 55
29 MX2 MX2 56
29 MX3 MX3 57
28,29 MX4 MX4 58
29 MX5 MX5 59
29 MX6 MX6 60
29 MX7 MX7 61

KBSOUT0/JENK KBSOUT1/TCK KBSOUT2/TMS KBSOUT3/TDI KBSOUT4/JEN0 KBSOUT5/TDO KBSOUT6/RDY KBSOUT7 KBSOUT8 KBSOUT9 KBSOUT10 KBSOUT11 KBSOUT12/GPIO64 KBSOUT13/GPIO63 KBSOUT14/GPIO62 KBSOUT15/GPIO61/XOR_OUT GPIO60/KBSOUT16 GPIO57/KBSOUT17

28,29 MY0 MY0 53
29 MY1 MY1 52
29 MY2 MY2 51
29 MY3 MY3 50
29 MY4 MY4 49
29 MY5 MY5 48
29 MY6 MY6 47
29 MY7 MY7 43
29 MY8 MY8 42
29 MY9 MY9 41
29 MY10 MY10 40
29 MY11 MY11 39
29 MY12 MY12 38
29 MY13 MY13 37
29 MY14 MY14 36
29 MY15 MY15 35
29 MY16 MY16 34
29 MY17 MY17 33

TIMER: GPIO56/TA1 GPIO20/TA2 GPIO14/TB1

31 MMB_ATTN12# 27
117 SUSON 36
63 FANSIG 29

GPIO15/A_PWM GPIO21/B_PWM GPIO13/C_PWM GPIO66/G_PWM

32 CONTRAST 18
118 NUMLED# NUMLED# 27
62 PWRLED# PWRLED# 27
81 CAPSLED# CAPSLED# 27

SPI: GPIO77/SPI_DI GPO76/SPI_DO/SHBM GPIO75/SPI_SCK

84 CRT_SENSE# CRT_SENSE# 18
83 SHBM_R
82 ENERGY_DET 20

Modify Net name on 3/17

SMB: GPIO17/SCL1 GPIO22/SDA1 GPIO73/SCL2 GPIO74/SDA2

31 MBCLK MBCLK 70
31 MBDATA MBDATA 69
10 2ND_MBCLK 2ND_MBCLK 67
10 2ND_MBDATA 2ND_MBDATA 68

IR: GPIO72/IRRX1/SIN2 GPIO70/IRRX2_IRSL0 GPIO71/IRTX/SOUT2 GPIO87/CIRRXM/SIN_CR GPIO34/CIRRXL GPIO16/CIRTX GPO83/SOUT_CR/BADDR1

75 RSMRST#_uR R148 *SHORT_4 ICH_RSMRST# 8
73 SUSC# 8,14
74 PWROK_EC_uR R145 *SHORT_4 PWROK_EC 8
113 RF_EN 21
14 CIRR_X2
114 HWPG
111 BADDR1_EC_R

PS/2: GPIO37/PSCLK1 GPIO35/PSDAT1 GPIO26/PSCLK2 GPIO27/PSDAT2 GPIO25/PSCLK3 GPIO12/PSDAT3

29 TPCLK TPCLK 72
29 TPDATA TPDATA 71
8 PCH_ACIN PCH_ACIN 10
29 BT_POWERON# BT_POWERON# 11
34,35,36,37 MAINON 12
17 VGA_THERM# 13

FIU: F_SDI F_SDO F_CS0 F_SCK

86 SPI_SDI_uR
87 SPI_SDO_uR R163 22_4 SPI_SDO_uR
90 SPI_CS0#_uR
92 SPI_SCK_uR R169 22_4 SPI_SCK_uR

8 ICH_SUSCLK R457 *781@0_6 E775_32KX1 77

32KX1/32KCLKIN

GPIO55/CLKOUT 30 ECDB_CLOCK T10

VCC_POR 95 VCC_POR# R161 47K/F_4 +3VPCU

VREF 104 VREF_uR R172 *SHORT_4 A3VPCU

R156 20M_6 E775_32KX2 79

32KX2

R158 33K/F_4

Y2 32.768KHz

C248 15p_4 C251 15p_4

E775AGND

4/23 Add net PCH_ACIN connet to PCH at REV:B

GND1 GND2 GND3 GND4 GND5 GND6 AGND VCORF

WPCE775

C249 .1u/16V_4 C266 .1u/16V_4

L26 BK1608HS220_6_1A

E775AGND

VCORF_uR_44 C219 1u_4

change footprint to lqfp128-16x16-4-zy8 at C-test

+3V D16 BAS316 C254 4.7u_6 C252 .1u/16V_4

7/22 Reserve C282 near EC on top side.

ICMNT C282 *4.7u_6 E775AGND

7/22 Add C281 near EC on top side.

C281 0.01u/50V_6 E775AGND

Near TP on TOP side

+3V R179 47K_6 RT1 THERMISTOR_100K/1%(NTC) E775AGND

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU Thermal 1 (98h) and CPU Thermal 2 (9Ah)
SM Bus 3	MMB3 and EEPROM (+3VPCU)
SM Bus 4	MMB1, MMB2 and VGA Thermal (+3V)

I/O ADDRESS SETTING

BADDR1-0	I/O Address	
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 BADDR0_EC_R R188 10K_4
BADDR1 BADDR1_EC_R R181 *10K_4
SHBM SHBM_R R160 10K_4

7/1 Add R12 by EC at C-test. SPI_SDI_uR R12 100K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

+3VPCU

MBCLK R141 10K_4
MBDATA R136 10K_4
MMB3_SMCLK R173 10K_4
MMB3_SMDATA R174 10K_4

+3V

CRT_SENSE# R162 *10K_4
2ND_MBCLK R132 10K_4
2ND_MBDATA R133 10K_4
MXM_SMCLK12 R152 2.2K_4
MXM_SMDATA12 R153 2.2K_4

change to 10K ohm,
2nd MBCLK/MBDATA and MXM_SMCLK12/MXM_SMDATA12 PU to +3V at B-test

ACER ID

+3VPCU Change to PU +3VPCU at C-test

MMB3_SMCLK MMB3_SMDATA

U15 SCL SDA A0 A1 A2 WP VCC GND *24C02

C192 .1u/16V_4

5/14 Stuff C192 by EMI at B-test

SPI FLASH

+3VPCU

SPI_SDI_uR R164 22_4 SPI_SDI_uR_R
R16 100K_4
8/17 Add R16 by EC at Ramp
SPI_SDO_uR
SPI_SCK_uR
+3VPCU R165 10K_4 SPI_CS0#_uR

U18 SO SI SCK CE VDD HOLD WP VSS W25X16AVSSIG

C294 .1u/16V_4

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add
Winbond W25X16AVSSIG AKE38ZP0N01
MXIC MX25L1605AM2C-15G AKE37P0Z13
EON EN25F16-100HIP AKE38ZA0Q00
AMIC A25L016 AKE38ZN0800

HWPG

+3V R134 10K_4

37 HWPG_1.8V D11 BAS316
34,35,37 HWPG_1.05V D12 BAS316
36 HWPG_1.5V D10 *BAS316
32 SYS_HWPG D9 BAS316

HWPG R126 0_4 MPWROK 4,16

ESD Protection

D34 *VARISTOR ESD BT_POWERON#
D35 *VARISTOR ESD LID591# Near CN10.11
D36 *VARISTOR ESD NUMLED# Near R317
D37 *VARISTOR ESD PWRLED# Near R321
D38 *VARISTOR ESD SUSLED# Near R323
D39 *VARISTOR ESD CAPSLED# Near R318
D40 *VARISTOR ESD BATLED0# Near R319
D41 *VARISTOR ESD BATLED1# Near R320

5/12 Reserve ESD components by EC vendor at B-test

VR Cap.

+3V R170 *10K_4 R180 *10K_4

DIGVOL_UP DIGVOL_DN

C257 .1u/16V_4 C262 .1u/16V_4

Place two near EC

POWER-ON Switch

NBSWON# JP1 *SHORT PAD

CIR

+3VPCU +3V_S5 R637 *10K_4

C665 4.7U/10V_8

U49 VCC OUT GND GND

CIRR_X2 D33 *VPORT_6

CIR@IRM-V538-TR1

Change Footprint at C-test

INTERNAL KEYBOARD STRIP SET

+3VPCU MY0 R131 10K_4

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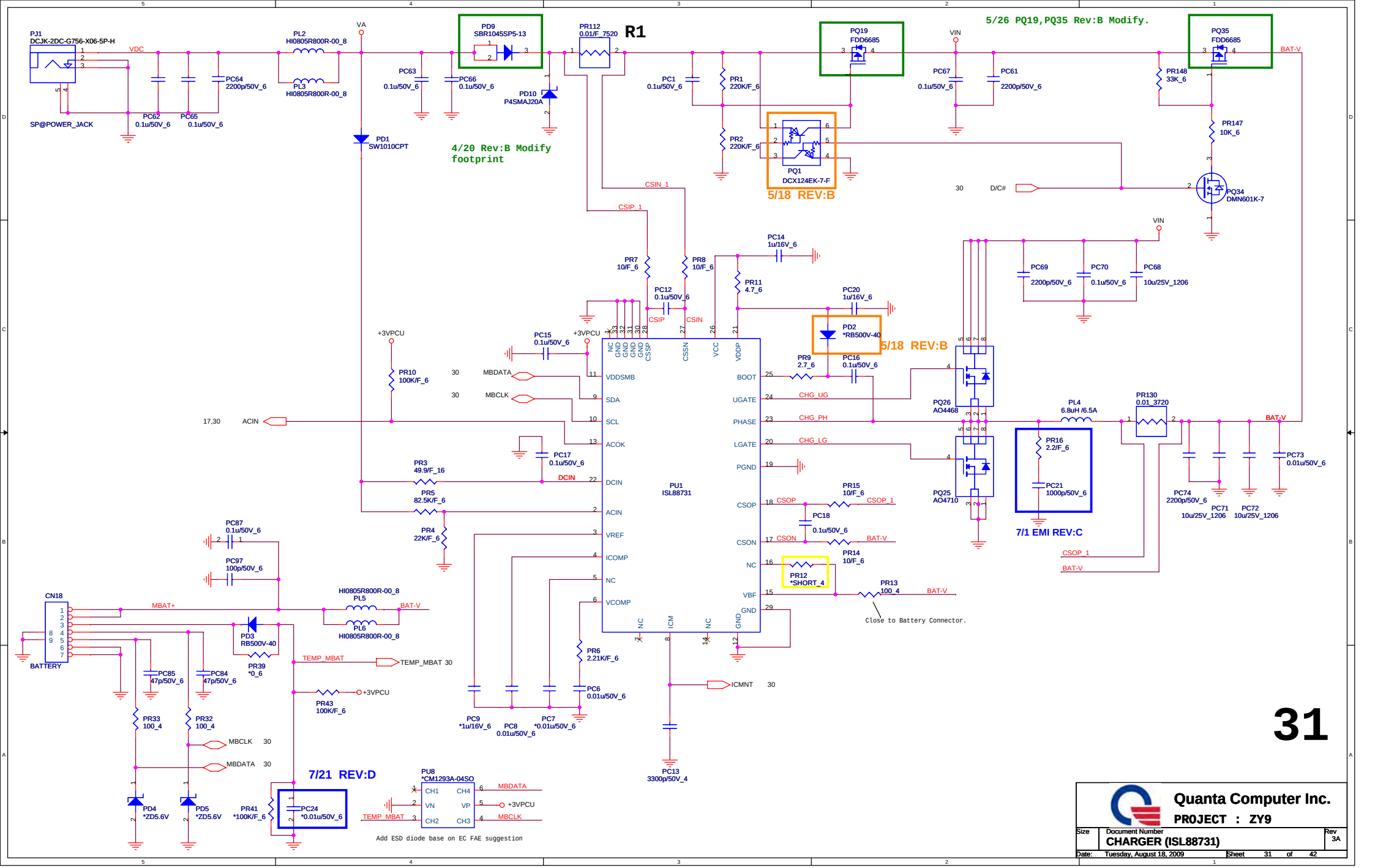

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[PWM] MAIND → MAIND 36,37

COMPLEX MARGIN TEST:

For ISL6237 ADJ
mount PR92 , PR80 , PR108 , PR95
No mount PR88 , PR83

For RT8206 ADJ
mount PR88 , PR83 , PR108 , PR95
No mount PR92 , PR80

For ISL6237 & RT8206 Fix
mount PR92 , PR108 , PR80
No mount PR88 , PR83

For TPS51427
PC40 mount 1u/6.3V_4

32

11,41 SYS_SHDN# — PS2 *SHORT_4 — PR84 39K/F_4 — VL

PS1 *SHORT_4 (5V_EN) — PS3 *SHORT_4 (3V_EN)

5/25 REV:B
Reduce ripple noise

VIN — 4/22 REV_B del JP — PC125 27u/25V_6.3X5.7 — PC51 0.1u/50V_6 — PC58 2200p/50V_6 — PC50 *10u/25V_1206

4/22 REV_B del JP — VIN — PC54 10u/25V/X6S_1206 — PC60 *10u/25V/X6S_1206

PC52 0.1u/50V_6 — PC59 2.2n/50V_4 — PC57 10u/25V/X6S_1206

6/29 REV:C
Acoustic issue

PD14 ZD5.6V — PC49 0.1u/50V_6 — PC53 1u/10V_4 — PR82 *0_6 — PR104 100K/F_4 — PC56 4.7u/10V_8 — PR79 0_4 — PC48 1u/16V_6 — PR80 0_4 — PR83 *0_4 — REF — PC47 0.1u/50V_6 — PR81 200K/F_4

13A

PQ6 AOL1448 — 5V_DH — PQ7 AOL1718 — 5V_DL — 5V_LX

PL1 1.5uH — PR107 *0_6 — PR86 0_6 — PR109 2.2/F_6 — PC164 1000p/50V_6

5/18 REV:B
EMI issue

PC122 330u/6.3V_105C — PC159 10u/25V/X6S_1206 — PC55 330u/6.3V_105C — PC169 0.1u/50V_6

+5VPCU

PU5 RT8206BGQW

5/18 REV:B
RT 2nd Source

LDOREFIN LDO VIN NC ONLIN VCC TON REF

BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD

REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2

BST1 DL1 PVCC NC GND PGND DL2 BST2

PR85 95.3K /F_6 — DDPWRGD_R — 5V_EN — REFIN2 — PR105 196K/F_6 — SKIP — 3V_EN

PC167 0.1u/50V_6 — PR87 1/F_6 — PC170 0.1u/50V_6 — PR89 1/F_6

PR103 *0_6 — VL — PR90 *SHORT_6 — PC171 1u/16V_6

PR88 *0_4 — PR92 0_4

3V_DH — PQ48 AO4468 — 3V_LX — PL13 2.2uH — 3V_DL — PQ47 AO4710

8.5A

PR106 2.2/F_6 — PC160 1000p/50V_6

5/18 REV:B
EMI issue

+3VPCU — PC162 0.1u/50V_6 — PC124 330u/6.3V_105C — PR108 0_6 — PR95 *0_6

AOL1718 Rds=3~4.3mOhm
+5VPCU OCP:4A 400K

L(ripple current)
=(19-5)*5/(1.5u*400kHz*19)
~6.14A

Iocp=14-(6.14/2)~10.93A
Vth=10.93A*4.3mOhm=46.999mV
R(Ilim)=(46.999mV*10)/5uA
=93.9~95.3K

PD13 CHN217UPT — PD12 CHN217UPT — PC172 0.1u/50V_6 — PC151 0.1u/50V_6 — PC161 0.1u/50V_6 — PR102 0_6

+15V — +15V_ALWP — PR98 22_8 — PC173 0.1u/50V_6

SKIP — PR101 *0_6 — REF — PR99 0_6

+3VPCU — PR91 *10K/F_6 — DDPWRGD_R — PS4 *SHORT_4 — SYS_HWPG 30

OCP:8A

L(ripple current)
=(19-3.3)*3.3/(2.2uH*0.5MHz*19)
~2.48A

Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K

VIN — PR111 *1M/F_6 — S5_DIS_G — PR159 *1M/F_6 — PQ12 *PDTC144EU — 5/18 REV:B

+3V_S5 — PR93 22_8 — PQ10 DMN601K-7

+5V_S5 — PR97 22_8 — PQ17 DMN601K-7

30 S5_DIS

VIN — PR100 1M/F_6 — S5_ON_G — PR96 1M/F_6 — PQ9 PDTC144EU — 5/18 REV:B

+15V — PR94 1M/F_6 — S5D — PQ8 DMN601K-7

30,41 S5_ON

+5VPCU — PQ11 AO6402A — +5V_S5

PR123 0_4 — S5_DIS_G — S5_ON_G

3.75A

+5VPCU — MAIND — PQ13 AO4468 — +5V — 8A

+3VPCU — MAIND — PQ14 AO4468 — +3V — 5A

+3VPCU — S5D — PQ15 AO6402A — +3V_S5 — 3A

5/25 stuff PR123, no stuff PQ12,PR111,PR159 at B test.

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	SYSTEM 5V/3V (ISL6237)	3A

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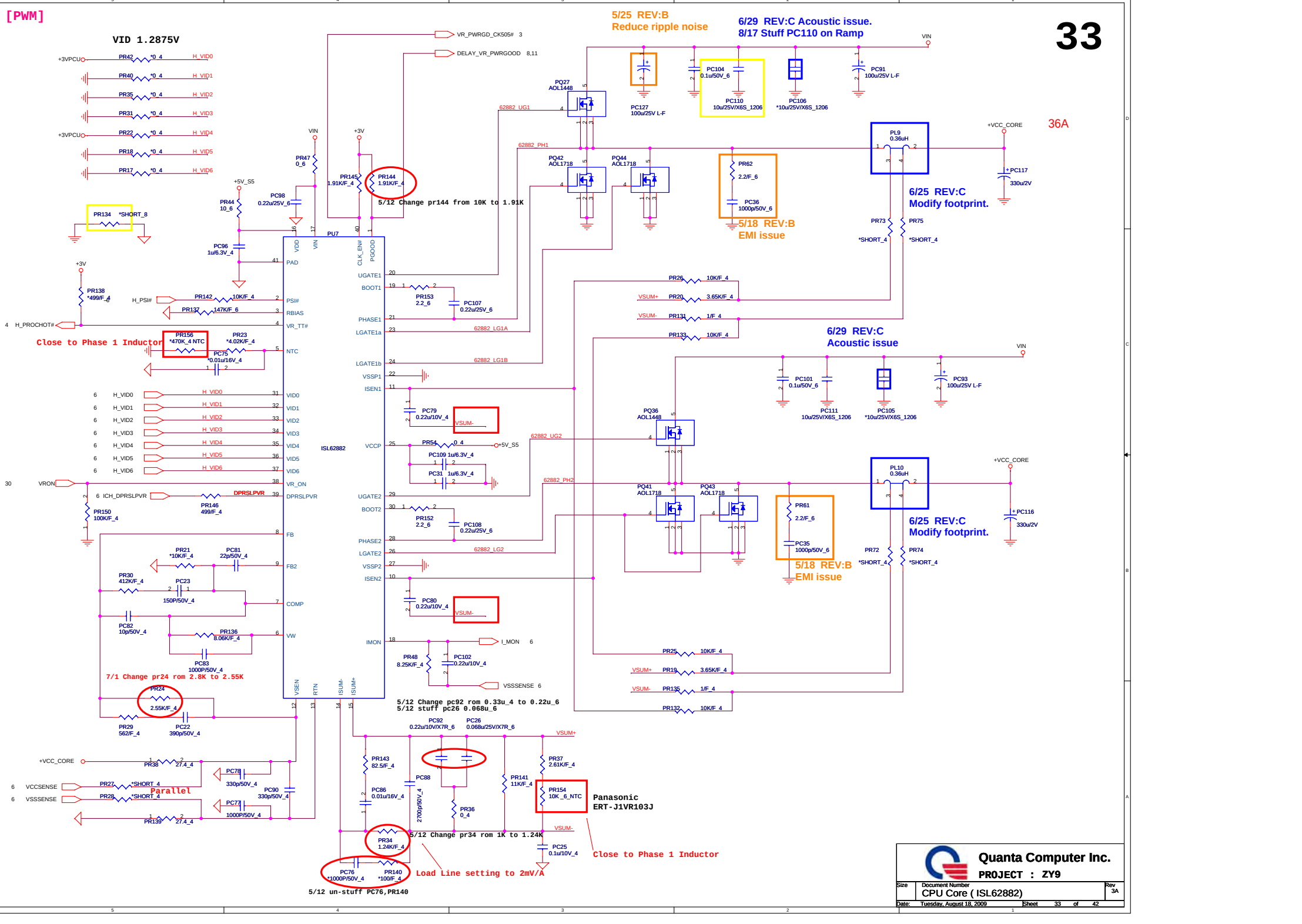
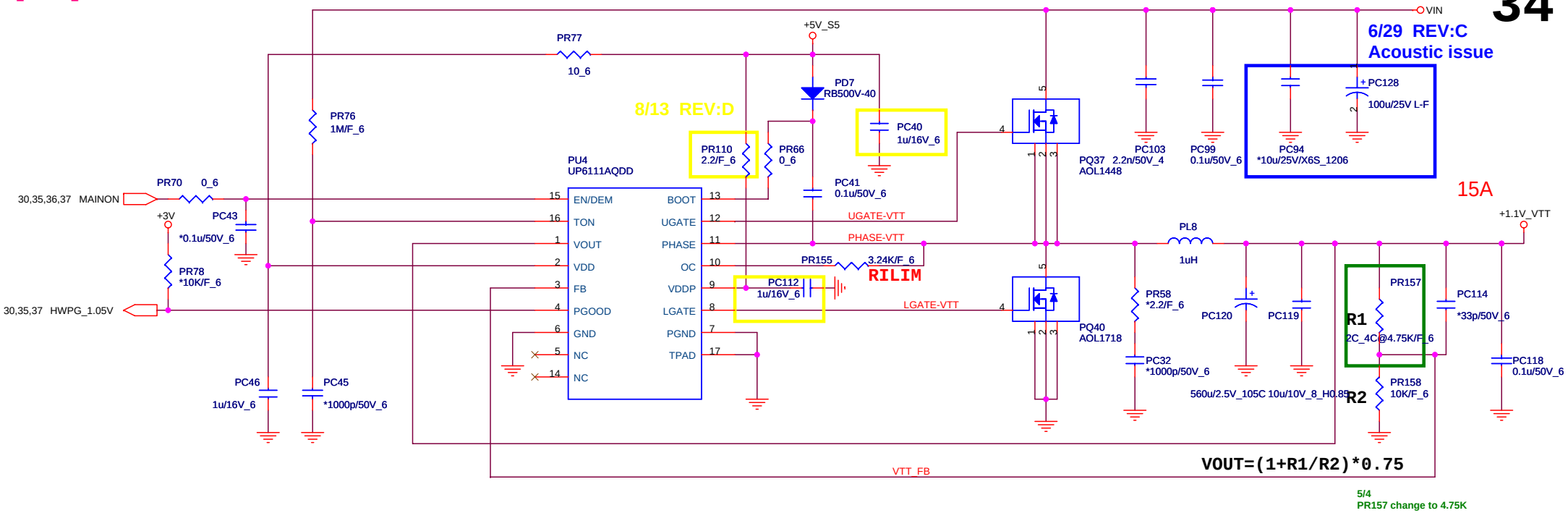

[PWM]
33
VID 1.2875V
5/25 REV:B
Reduce ripple noise
6/29 REV:C Acoustic issue.
8/17 Stuff PC110 on Ramp
36A
6/25 REV:C
Modify footprint.
5/18 REV:B
EMI issue
6/29 REV:C
Acoustic issue
5/12 Change pr144 from 10K to 1.91K
Close to Phase 1 Inductor
7/1 Change pr24 rom 2.8K to 2.55K
5/12 Change pc92 rom 0.33u_4 to 0.22u_6
5/12 stuff pc26 0.068u_6
Parallel
Panasonic
ERT-J1VR103J
5/12 Change pr34 rom 1K to 1.24K
Close to Phase 1 Inductor
Load Line setting to 2mV/A
5/12 un-stuff PC76,PR140
ISL62882
PU7
Quanta Computer Inc.
PROJECT : ZY9
CPU Core (ISL62882)
Tuesday, August 18, 2009



5/4
PR157 change to 4.75K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

4.3m*15=RILIM*20uA
RILIM=3.24K(3.22K)

Aurbundale (1.05V) R1 = 4.02K (CS24023F928)
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

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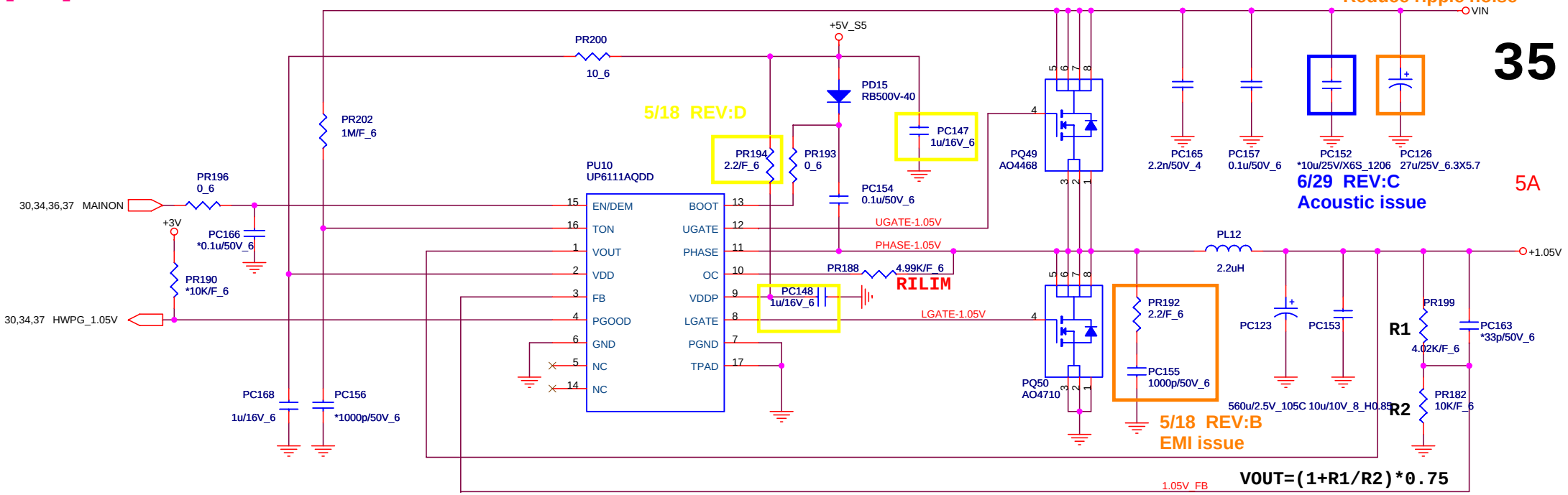
[PWM]

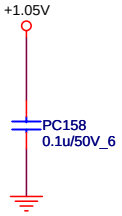
5/25 REV:B
Reduce ripple noise

35



AO4710 Rdson=11.8~14.2mOhm
OCP=7.2-0.8A
L(ripple current)
=(19-1.05)*1.05/(2.2u*272k*19)
~1.6577A

14.2m*7=RILIM*20uA
RILIM=4.99K(4.97K)



Quanta Computer Inc.
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Size	Document Number	Rev
	+1.05V(UP6111AQDD)	3A

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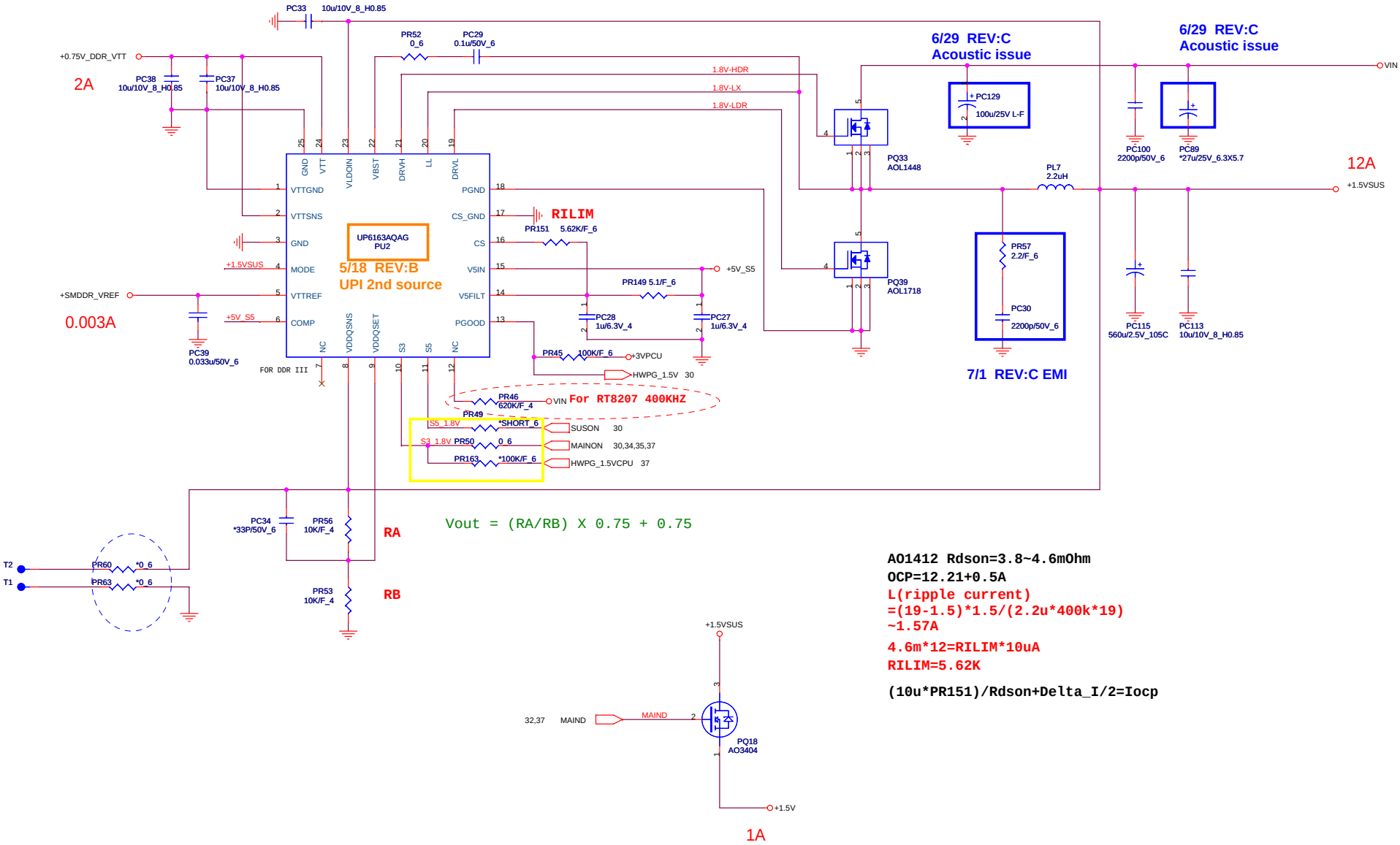

AO1412 Rdson=3.8~4.6mOhm
OCP=12.21+0.5A
L(ripple current)
=(19-1.5)*1.5/(2.2u*400k*19)
~1.57A

4.6m*12=RILIM*10uA
RILIM=5.62K

(10u*PR151)/Rdson+Delta_I/2=Iocp

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	DDR 1.5V(TPS51116)		3A
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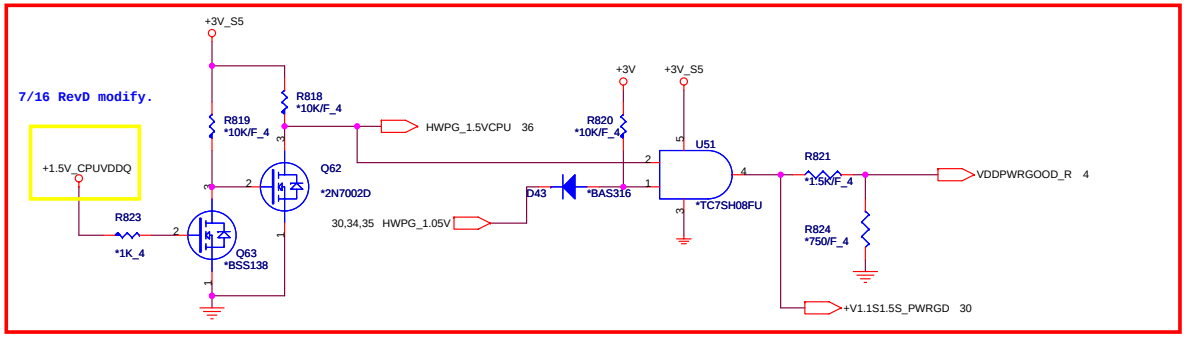
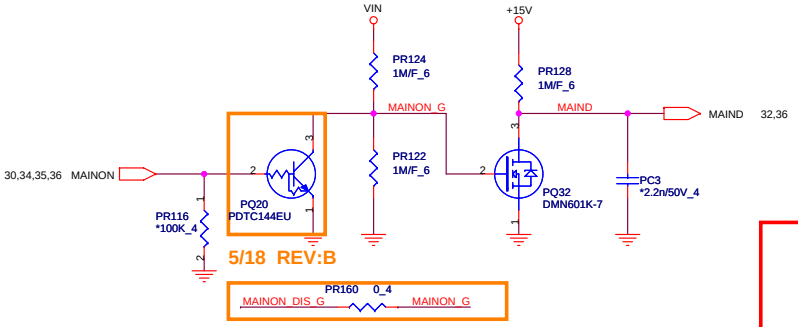
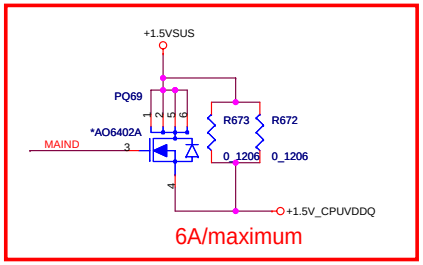
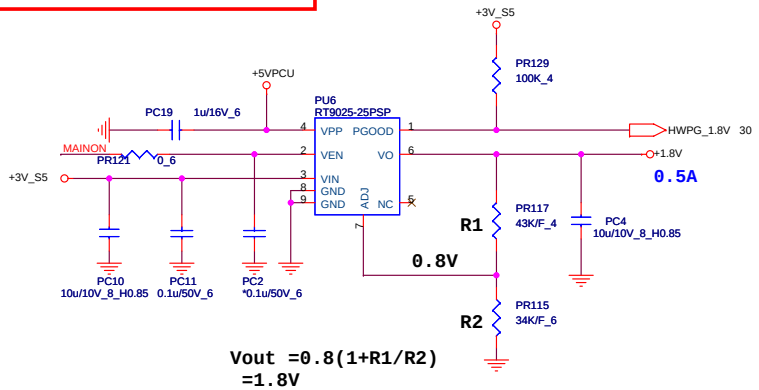




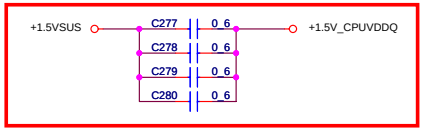
5/25 stuff PR160, no stuff PQ24,PR126,PR125 at B test.

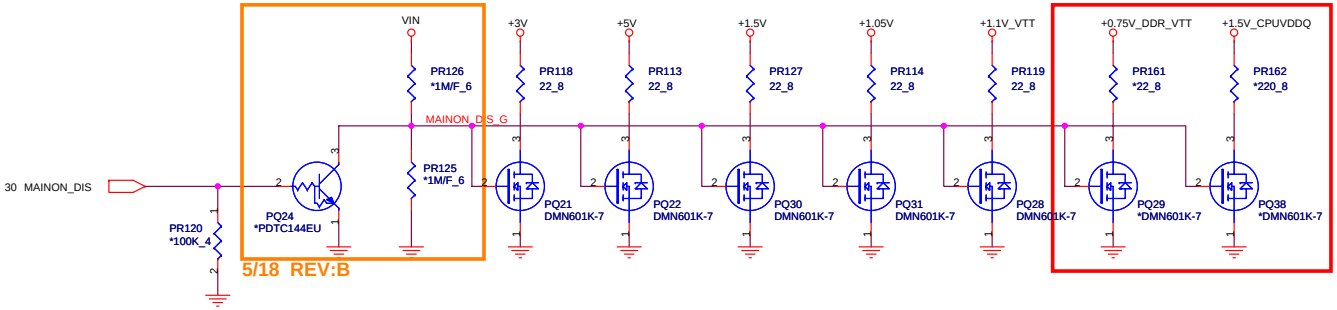


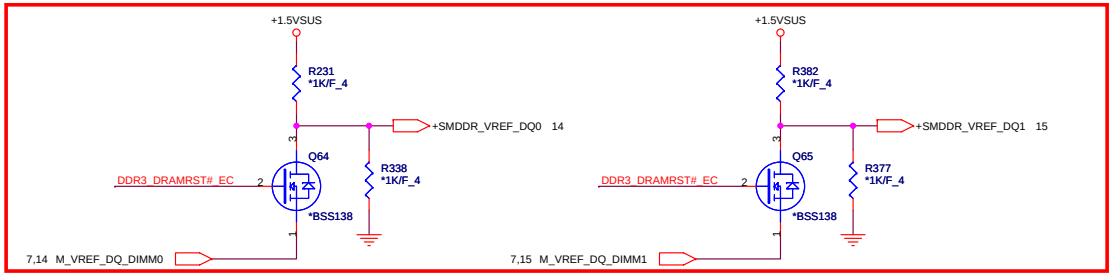


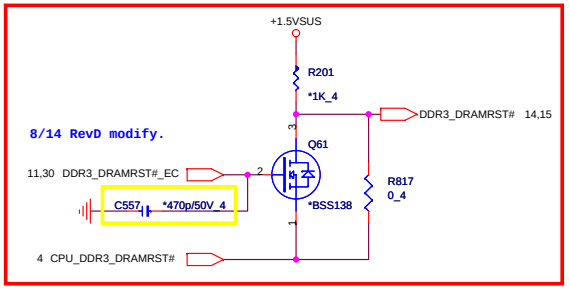
Vout =0.8(1+R1/R2)
=1.8V

S3 power solution: C277~C280 stuff 0.1uF cap;
Normal : Stuff 0ohm to short.









12,21,25,36 +1.5V

6 +1.5V_CPUVDDQ

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PROJECT : ZY9

Size	Document Number	Rev
	Discharge (1.5V_S5/1.8V)	3A
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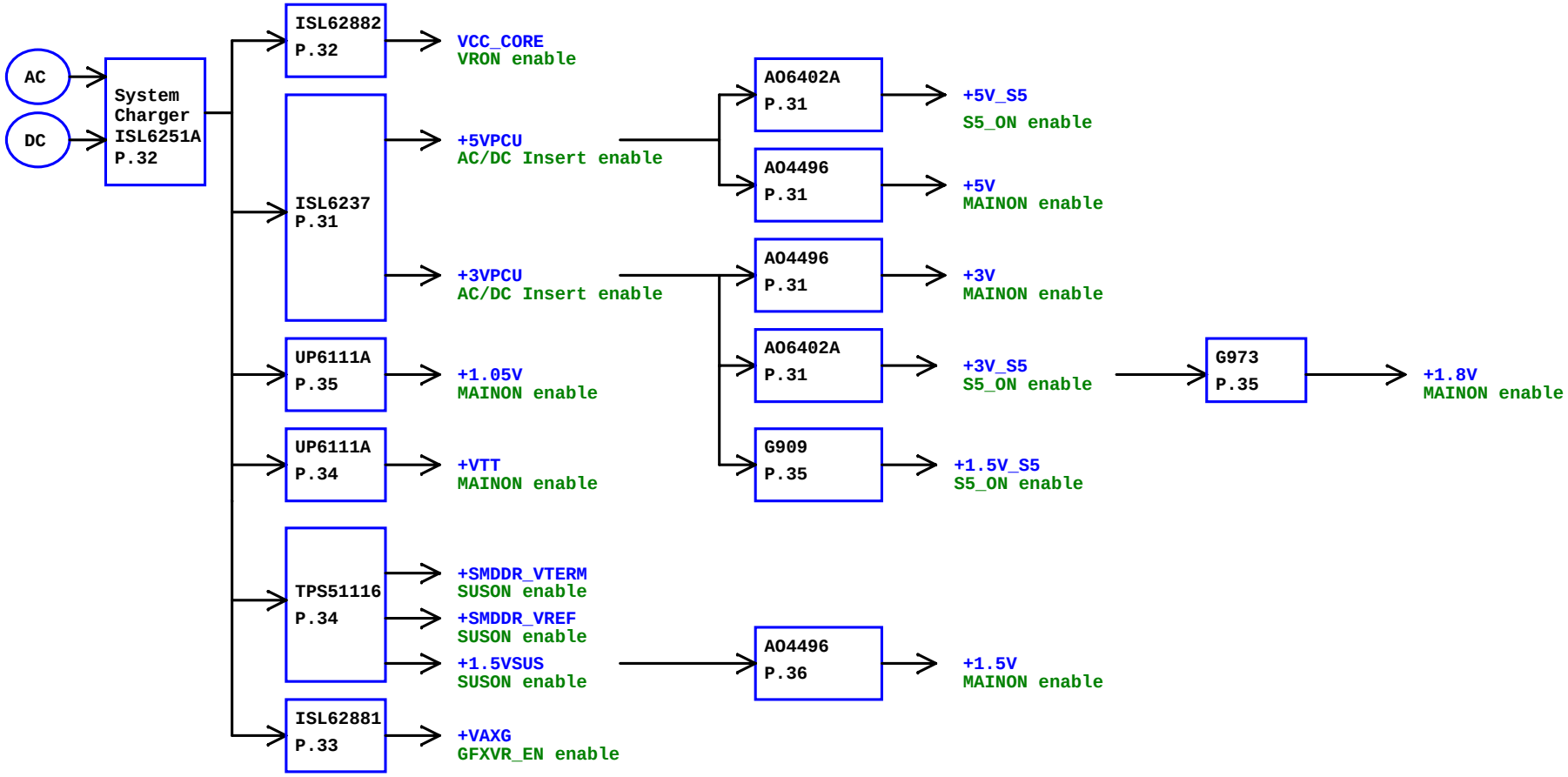

Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.5VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC, Cardreader (OZ129T)
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M

Quanta Computer Inc.
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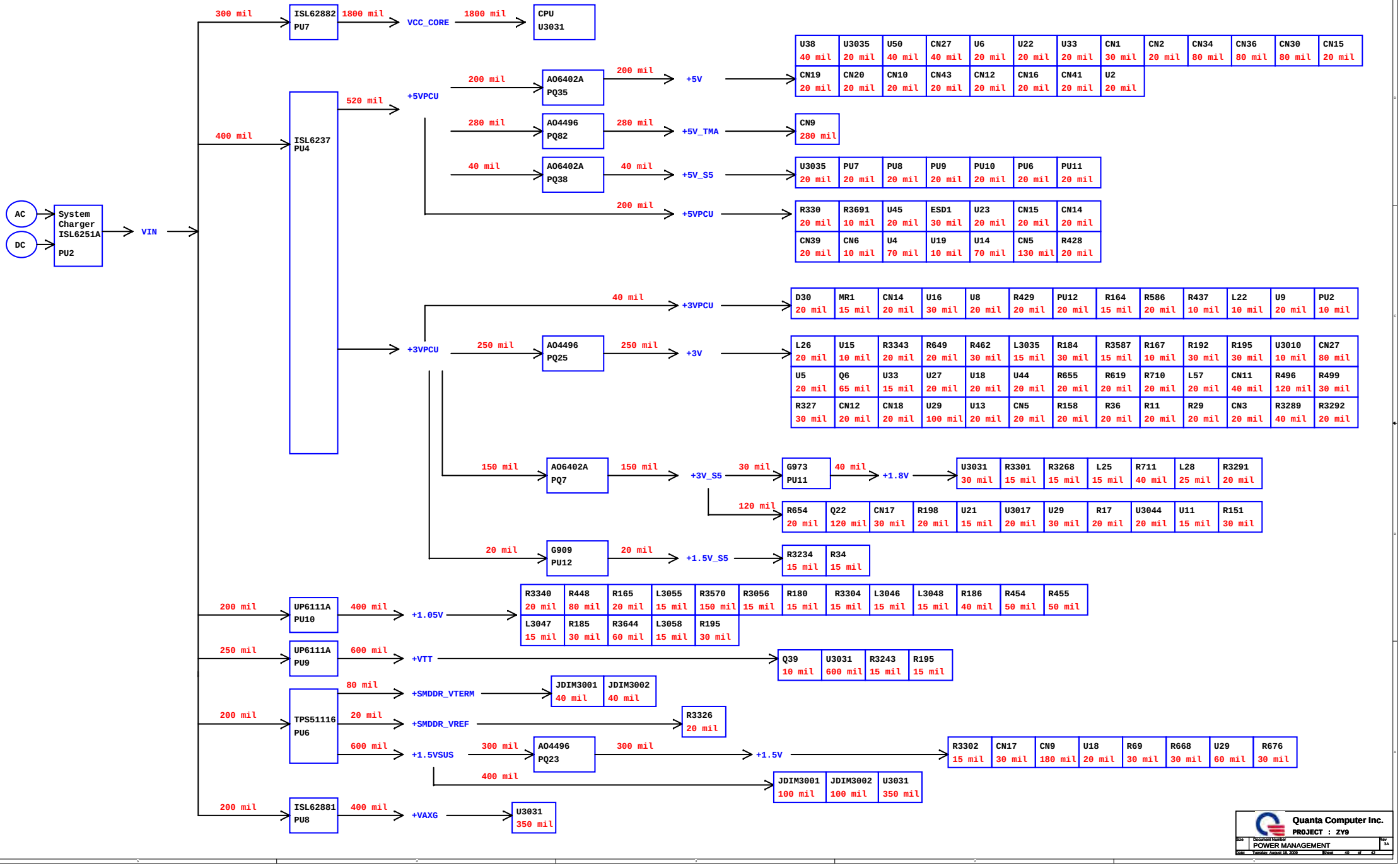
PCH POWER PLANE

LOGIC	SUPPLY	LEVEL	S0	S3	S4	S5
Fast Flash	VccpNAND	+1.8V/+3.3V	ON	OFF	OFF	OFF
Core	DcpSusByp	+1.05V	ON	OFF	OFF	OFF
CPU	V_CPU_IO	+VTT	ON	OFF	OFF	OFF
PCI	V5REF	+5V/+3V	ON	OFF	OFF	OFF
USB	V5REF_Sus	+5V_S5/+3V_S5	ON	ON	ON	ON
DisplayPort, SATA, PCI	VCC3_3	+3V	ON	OFF	OFF	OFF
Core	VccCore	+1.05V	ON	OFF	OFF	OFF
PCIE/DMI	VccDMI	+VTT/+1.05V	ON	OFF	OFF	OFF
Fast Flash	VccME3_3	+3V	ON	OFF	OFF	OFF
PCIE/DMI,SATA,USB	VccIO	+1.05V	ON	OFF	OFF	OFF
Core	VccLAN	+1.05V	ON	OFF	OFF	OFF
Core	VccME	+1.05V	ON	OFF	OFF	OFF
RTC	VccRTC	+VCCRTC	ON	ON	ON	ON
USB&PCI	VccSus3_3	+3V_S5	ON	ON	ON	ON
IntelR HD Audio	VccSusHDA	+1.5V_S5	ON	ON	ON	ON
Core	VccVRM	+V1.5S_1.8S	ON	OFF	OFF	OFF
CLK	VccAClk	+1.05V	ON	OFF	OFF	OFF
CRT	VccADAC	+3V	ON	OFF	OFF	OFF
DPLL	VccADPLLA	+1.05V	ON	OFF	OFF	OFF
DPLL	VccADPLLB	+1.05V	ON	OFF	OFF	OFF
PCIe/DMI	VccapllEXP	+1.05V	ON	OFF	OFF	OFF
IntelR FDI	VccFDIPLL	+1.05V	ON	OFF	OFF	OFF
SATA	VccSATAPLL	+1.05V	ON	OFF	OFF	OFF
Display	VccTX_LVDS	+1.8V	ON	OFF	OFF	OFF


AC
DC
System Charger ISL6251A PU2
VIN
300 mil
ISL62882 PU7
1800 mil
VCC_CORE
1800 mil
CPU U3031
400 mil
ISL6237 PU4
520 mil
+5VPCU
200 mil
AO6402A PQ35
200 mil
+5V
U38 40 mil | U3035 20 mil | U50 40 mil | CN27 40 mil | U6 20 mil | U22 20 mil | U33 20 mil | CN1 30 mil | CN2 20 mil | CN34 80 mil | CN36 80 mil | CN30 80 mil | CN15 20 mil
CN19 20 mil | CN20 20 mil | CN10 20 mil | CN43 20 mil | CN12 20 mil | CN16 20 mil | CN41 20 mil | U2 20 mil
280 mil
AO4496 PQ82
280 mil
+5V_TMA
CN9 280 mil
40 mil
AO6402A PQ38
40 mil
+5V_S5
U3035 20 mil | PU7 20 mil | PU8 20 mil | PU9 20 mil | PU10 20 mil | PU6 20 mil | PU11 20 mil
200 mil
+5VPCU
R330 20 mil | R3691 10 mil | U45 20 mil | ESD1 30 mil | U23 20 mil | CN15 20 mil | CN14 20 mil
CN39 20 mil | CN6 10 mil | U4 70 mil | U19 10 mil | U14 70 mil | CN5 130 mil | R428 20 mil
40 mil
+3VPCU
D30 20 mil | MR1 15 mil | CN14 20 mil | U16 30 mil | U8 20 mil | R429 20 mil | PU12 20 mil | R164 15 mil | R586 20 mil | R437 10 mil | L22 10 mil | U9 20 mil | PU2 10 mil
+3VPCU
250 mil
AO4496 PQ25
250 mil
+3V
L26 20 mil | U15 10 mil | R3343 20 mil | R649 20 mil | R462 30 mil | L3035 15 mil | R184 30 mil | R3587 15 mil | R167 10 mil | R192 30 mil | R195 30 mil | U3010 10 mil | CN27 80 mil
U5 20 mil | Q6 65 mil | U33 15 mil | U27 20 mil | U18 20 mil | U44 20 mil | R655 20 mil | R619 20 mil | R710 20 mil | L57 20 mil | CN11 40 mil | R496 120 mil | R499 30 mil
R327 30 mil | CN12 20 mil | CN18 20 mil | U29 100 mil | U13 20 mil | CN5 20 mil | R158 20 mil | R36 20 mil | R11 20 mil | R29 20 mil | CN3 20 mil | R3289 40 mil | R3292 20 mil
150 mil
AO6402A PQ7
150 mil
+3V_S5
30 mil
G973 PU11
40 mil
+1.8V
U3031 30 mil | R3301 15 mil | R3268 15 mil | L25 15 mil | R711 40 mil | L28 25 mil | R3291 20 mil
120 mil
R654 20 mil | Q22 120 mil | CN17 30 mil | R198 20 mil | U21 15 mil | U3017 20 mil | U29 30 mil | R17 20 mil | U3044 20 mil | U11 15 mil | R151 30 mil
20 mil
G909 PU12
20 mil
+1.5V_S5
R3234 15 mil | R34 15 mil
200 mil
UP6111A PU10
400 mil
+1.05V
R3340 20 mil | R448 80 mil | R165 20 mil | L3055 15 mil | R3570 150 mil | R3056 15 mil | R180 15 mil | R3304 15 mil | L3046 15 mil | L3048 15 mil | R186 40 mil | R454 50 mil | R455 50 mil
L3047 15 mil | R185 30 mil | R3644 60 mil | L3058 15 mil | R195 30 mil
250 mil
UP6111A PU9
600 mil
+VTT
Q39 10 mil | U3031 600 mil | R3243 15 mil | R195 15 mil
200 mil
TPS51116 PU6
80 mil
+SMDDR_VTERM
JDIM3001 40 mil | JDIM3002 40 mil
20 mil
+SMDDR_VREF
R3326 20 mil
600 mil
+1.5VSUS
300 mil
AO4496 PQ23
300 mil
+1.5V
R3302 15 mil | CN17 30 mil | CN9 180 mil | U18 20 mil | R69 30 mil | R668 30 mil | U29 60 mil | R676 30 mil
400 mil
JDIM3001 100 mil | JDIM3002 100 mil | U3031 350 mil
200 mil
ISL62881 PU8
400 mil
+VAXG
U3031 350 mil
Quanta Computer Inc.
PROJECT : ZY9
Size
Document Number
POWER MANAGEMENT
Rev
3A
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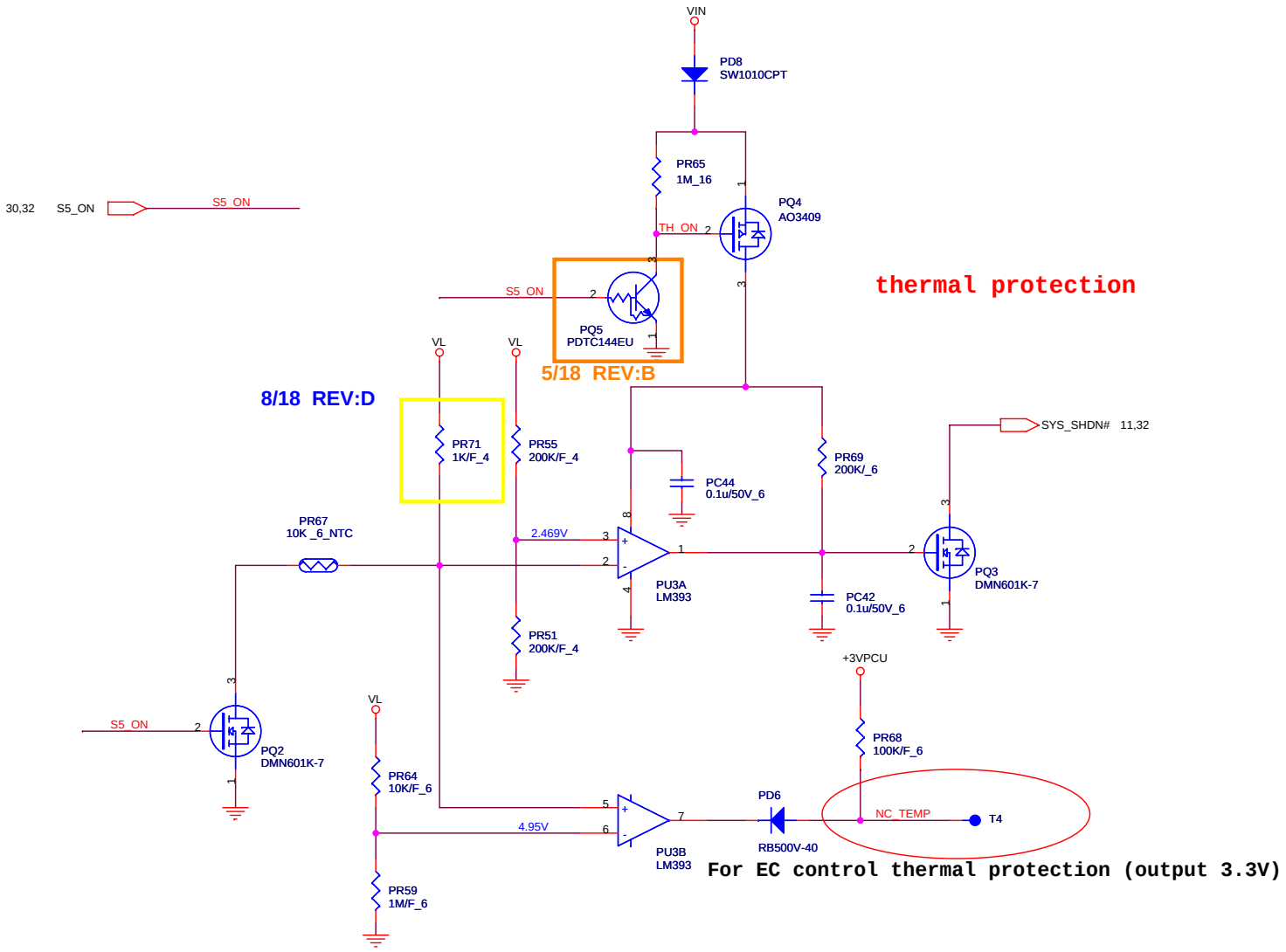

Quanta Computer Inc.		
PROJECT : ZY9		
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CHANGE LIST

Model: ZY9 MB

MODEL: ZY9

REV 1A

FIRST RELEASED: E20080?-???? (PCB: DA0ZY8MB6A0)

REV 2A

4/9 modify

- Page4 : R468 change from 4.75K to 1.1Kohm & R488 change from 12K to 3Kohm by DG1.52
- Page8 : Add R373 to pull up ACIN on PCH side, R274 net PCH_ACIN connector to EC pin10.
- Page10 : Stuff R227, R257; remove R222,R224
- Q2,Q5, Q15~Q20,Q29~Q31,Q35~Q43,Q45~Q47,Q50,Q51,Q57~Q59 : 2N7002E(BAM700200F6) change to 2N7002D(BAM700200H2) with ESD protection by SMT.
- Page21 : Modify LAN connector footprint and material by safety.
- Page21 : Modify CN21,CN23 footprint.
- Page28 : Add PAD11.
- Page31 :Chang PD9 footprint to power-6_5-1_84-3p by SMT.

4/23 modify

- Page37 : Stuff PQ28,PQ30,PQ31,PR114,PR119,PR127 by S3 discharge issue.
- Page3 : Chagne CPU_SEL PU +3V to +1.05V at B-test by SLG.
- Page14 : R176 un-stuff, R88 stuff at B-test.
- Page15 : R525 un-stuff, R429 stuff at B-test.
- Page23 : Change C571 to 4.7u for Po issue when boot at B-test
- Page26 : Chagne C400 to 22pF, C401 change to 27pF at B-test by HHC.
- Page32 : Del power net ISL6237_3V and all JP.
- Page33 : Stuff PR61,PR62,PC35,PC36 by EMI.

5/4 modify

- Page20 : Change CN16 footprint to rj45-jm36111-n2a22-7h-12p-h by safety test.
- Page34 : Change PR157 from 4.02K to 4.75K ohm for Clarksfield CPU.
- Page18 : Remove R438, R639 and Reserve RV7,RV8 by ESD at B-test.
- Page23 : Add U50, C666 and R561 for Po issue by Realtek at B-test.
- Page11 : Reverse R351 connect GPIO49 to EC for Temp Alert & Reverse Q12,Q11 connect to t SYS_SHDN# at B-test.
- Page30 : Add ESD components D34~D41 with EC signals ; Stuff C192 by EMI & Add D42 near JP1 at B-test.
- Page29 : Reserve R375 connect to Temp_Alert from PCH at B-test.

5/14 modify

- Page22 : Add R147,R151,R197 for power consumption measure & move C33 near C103 for EMI at B-test.
- Page21 : Change PCIE bus sequence beween CN21 and CN23 by BIOS at B-test.
- Page24 : Change C622, C635 to CH22206KB16 by EMI at B-test.

5/18 modify

- Page34 : Add PR110 at B-test.
- Page35 : Add PR194 at B-test.
- Page9 : 5/21 Change R233 to 1Kohm by Intel at B-test.

5/21 modify

- Page14: 5/21 No stuff R187 and change R185,R186; del C260 add R195 by CRB v1.6 at B-test.
- Page15: 5/21 No stuff R522 and change R518,R521; del C557 add R210 by CRB v1.6 at B-test.
- Page18: 5/21 change L9,L10,L13(CX8BA750006) from 47ohm to 75ohm by EMI at B-test.
- Page27: 5/22 Add R212 by pipe LED at B-test.
- Page10: 5/22 change ESATA USB port10 to port1 and rename OC0_1#, OC3#,OC5_6#; R565 connect to OC5_6# by BIOS at B-test.
- Page28: 5/22 change ESATA USB port10 to port1 and rename OC0_1#, OC3#,OC5_6# by BIOS at B-test.
- Page32: 5/25 stuff PR123, no stuff PQ12,PR111,PR159 at B test.
- Page37: 5/25 stuff PR160, no stuff PQ24,PR126,PR125 at B test.
- Page31: 5/25 Change PQ19, PQ35 to FDD6685 by power at B test.

REV 3A

- Page14: 6/19 Reserve M2 component and reserve R801~R808 DM connect to GND BY DG1.6 at C test.
- Page15: 6/19 Reserve M2 component and reserve R809~R816 DM connect to GND BY DG1.6 at C test.
- Page30: 6/19 Change R196 to 2.2 by EC at C-test.
- Page9 : 6/21 Non stuff R233 by Intel & R235 change to connect to +3V at C-test.
- Page17: 6/25 Delete R63 & Change CN22 pin define and footprint at C test.
- Page8: 6/25 Change some 0_4 to *short pad footprint; no stuff R366 at C-test.
- Page29 : 6/25 Stuff R375 by EC at C-test.
- Page11 : 7/1 Add R671 for GPIO57 PD and not PU; change board_id0 to GPIO7 by Intel suggestion at C-test.
- Page 29 : 7/2 Stuff Q22,Q2,1R119 & no stuff U11,C101 by cost down at C-test.
- Page37 : 7/2 Add Intel S3 power reduction circuit at C-test.
- Page28 : 7/2 no stuff R115 by Parade & add USB EMI chock at C-test.
- Page17 : 7/2 no stuff R406 R409 and stuff R411,R412,Q45,Q46 by S3 leakage at C-test.
- Page6 : 7/2 Change CPU VDDQ from +1.5V_S3 to +1.5V_CPUVDDQ by Intel at C test.
- Page33 : 7/5 Change PC79,PC80 connection from GND to VSUM- by ISL at C test.

REV 3B

- Page29: 7/22 Un-stuff R375 by EC at Ramp.
- Page30: 7/22 Add C281 and reserve C282 near EC on top side by battery LED abnormal & change RT1 connet form GND to AGND.
- Page33: 7/28 Change PU7 from AL062882000 to AL062882001 by Power shutdown issue and stuff PC110 by power on Ramp.
- Page28: 7/28 Reserve C311 and change L60~L64 by EMI at Ramp test.
- Page26: change resistor to short pad which MDIO0~14, CR1_CD0N,CR1_CD1N short to card reader connector at Ramp test.
- Page11: 8/8 Reserve R428 from GPIO46 by intel S3 suggestion at Ramp test.
- Page14: 8/8 R88 connector to +SMDDR_VREF_DIMM at Ramp test.
- Page24: 8/8 Remove L54~L57 at Ramp test.
- Page18: 8/12 del R431~R437 at Ramp-testt; change R29,R36 to 0 ohm.
- Page28: 8/12 del RN32~RN36 at Ramp-testt.
- Page34: 8/13 Replace and stuff PC112; change PC40 from 4.7uF to 1uF; PR110 from 0 to 2.2ohm by power at Ramp-testt.
- Page35: 8/13 Replace and stuff PC148; change PC147 from 4.7uF to 1uF; PR194 form 0 to 2.2ohm by power at Ramp-testt.
- Page26: 8/14 Stuff C393 and C625,exchange C384 and C386 value by JMicron at Ramp.
- Page4: 8/14 Reserve R213 by intel S3 at Ramp.
- Page37: 8/14 Reserve C557 connect to DDR3_DRAMRST#_EC by intel S3 at Ramp.
- Page36: 8/14 Reserve PR163 connect to S3_1.8V by intel S3 at Ramp.
- Page30: 8/17 SPI_SDI_uR add PD R16 by EC for saving S5 power at Ramp.
- Page41: 8/18 Change PR71 to 1K by power at Ramp.

REV 3C

ZY9

FROM	To
X	1A
X	1A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
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3A	3B
3A	3B
3A	3B
3A	3B
3A	3B
3A	3B

PROJECT MODEL :	ZY8	APPROVED BY:	
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