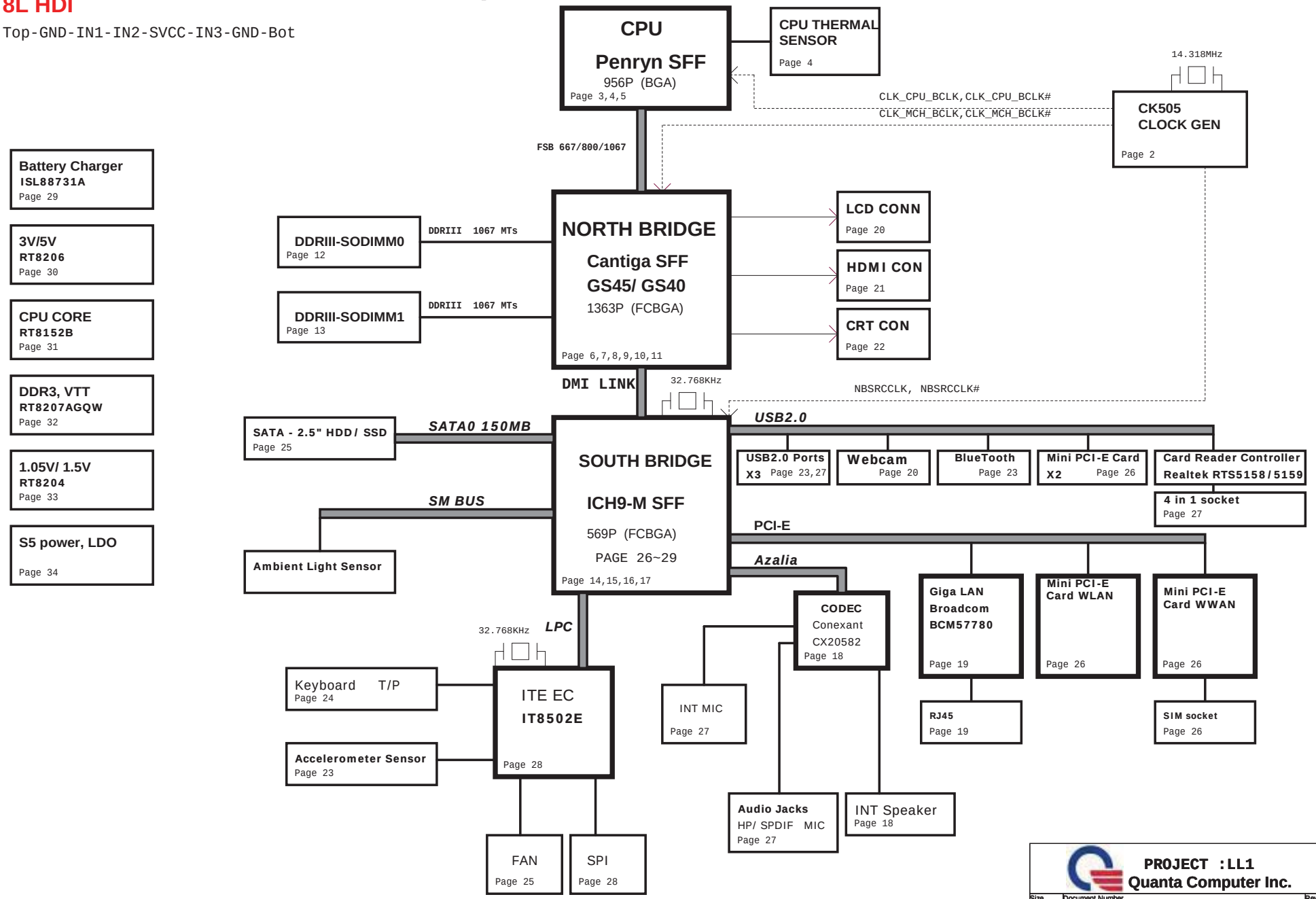
PCB STACK UP

8L HDI

Top-GND-IN1-IN2-SVCC-IN3-GND-Bot

Crimea, LL1 BLOCK DIAGRAM

01

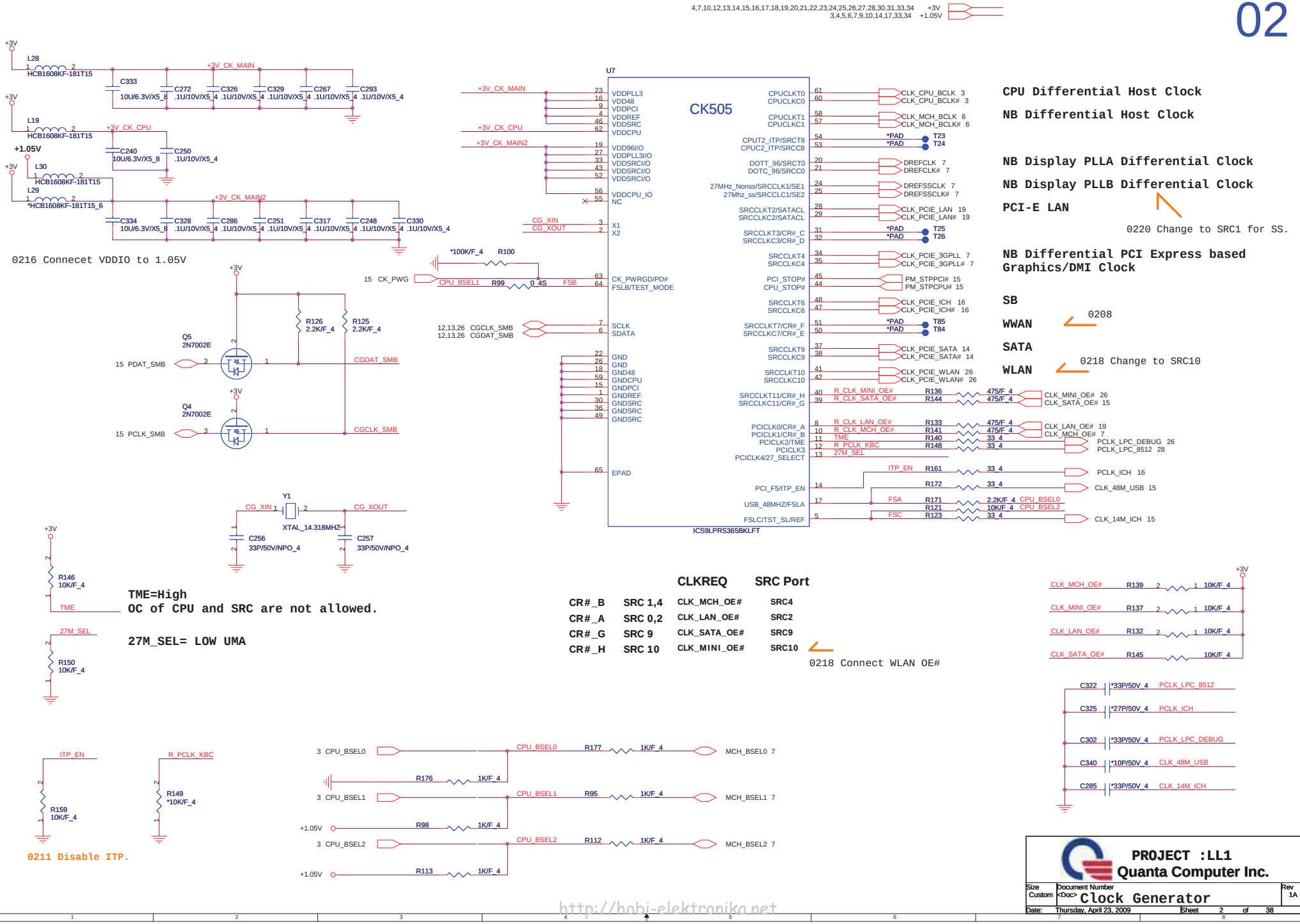


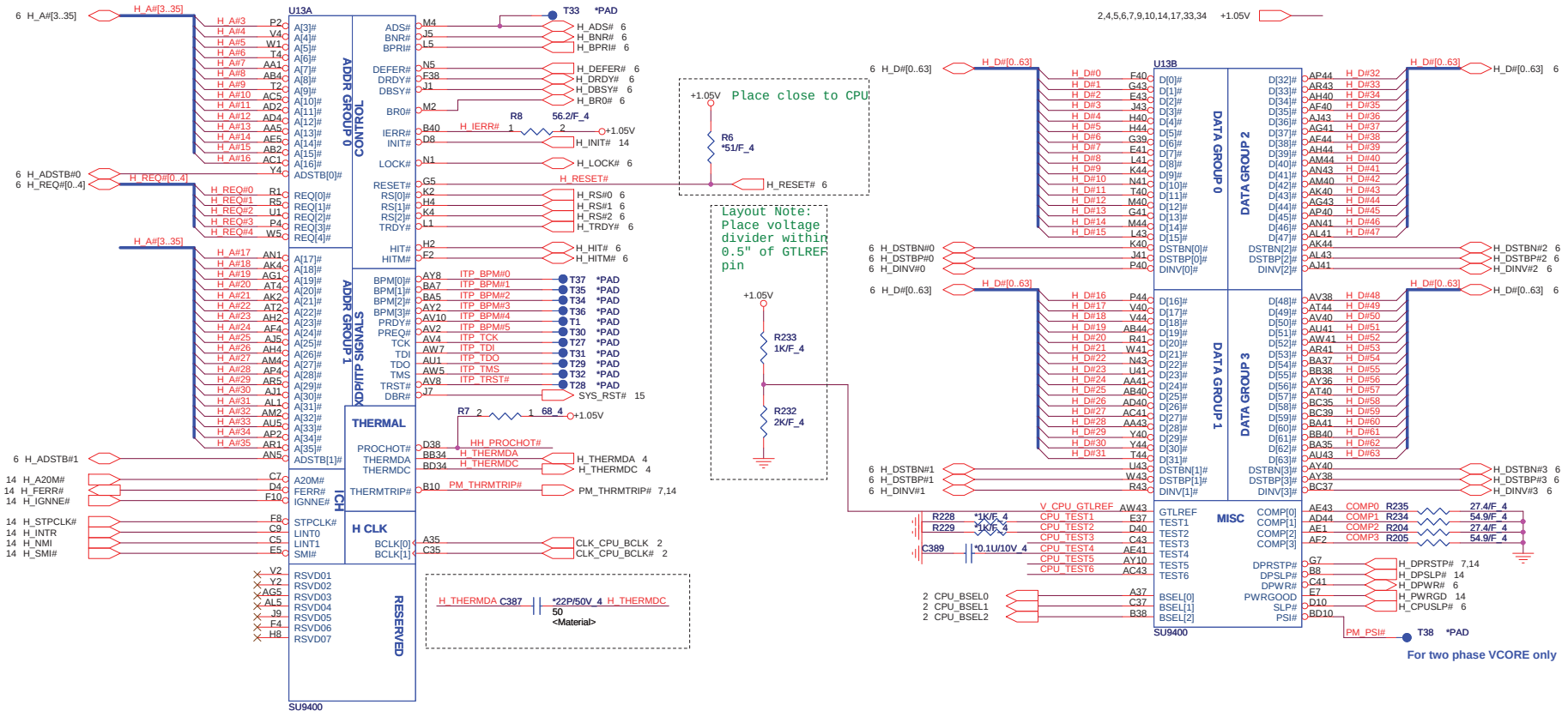
PROJECT : LL1

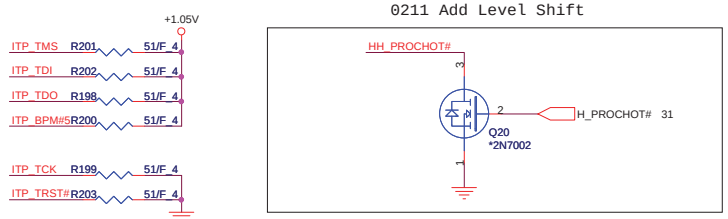
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Block Diagram	1A

Date: Thursday, April 23, 2009 Sheet 1 of 38


02
U7
CK505
ICS9LPRS365BKLFT
CPU Differential Host Clock
NB Differential Host Clock
NB Display PLLA Differential Clock
NB Display PLLB Differential Clock
PCI-E LAN
0220 Change to SRC1 for SS.
NB Differential PCI Express based Graphics/DMI Clock
SB
WWAN
0208
SATA
WLAN
0218 Change to SRC10
0216 Connecet VDDIO to 1.05V
TME=High
OC of CPU and SRC are not allowed.
27M_SEL= LOW UMA
CLKREQ SRC Port
CR#_B SRC 1,4 CLK_MCH_OE# SRC4
CR#_A SRC 0,2 CLK_LAN_OE# SRC2
CR#_G SRC 9 CLK_SATA_OE# SRC9
CR#_H SRC 10 CLK_MINI_OE# SRC10
0218 Connect WLAN OE#
0211 Disable ITP.
PROJECT : LL1
Quanta Computer Inc.
Clock Generator
Size Custom
Document Number <Doc>
Rev 1A
Date: Thursday, April 23, 2009
Sheet 2 of 38
http://hobi-elektronika.net





*PAD T42 CPU_TEST3
*PAD T39 CPU_TEST5
*PAD T43 CPU_TEST6

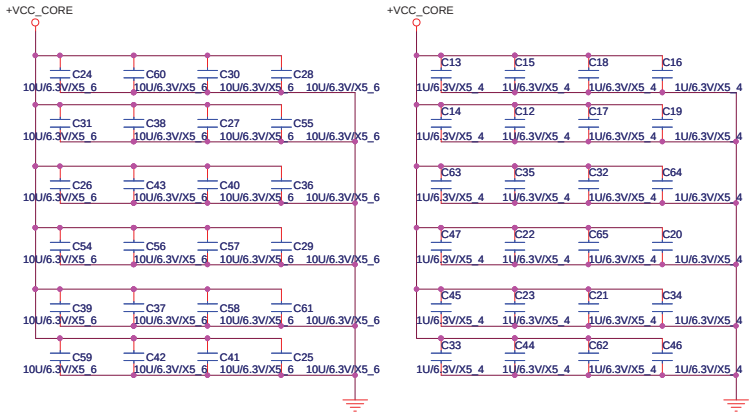
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

0209 Remove ITP connector

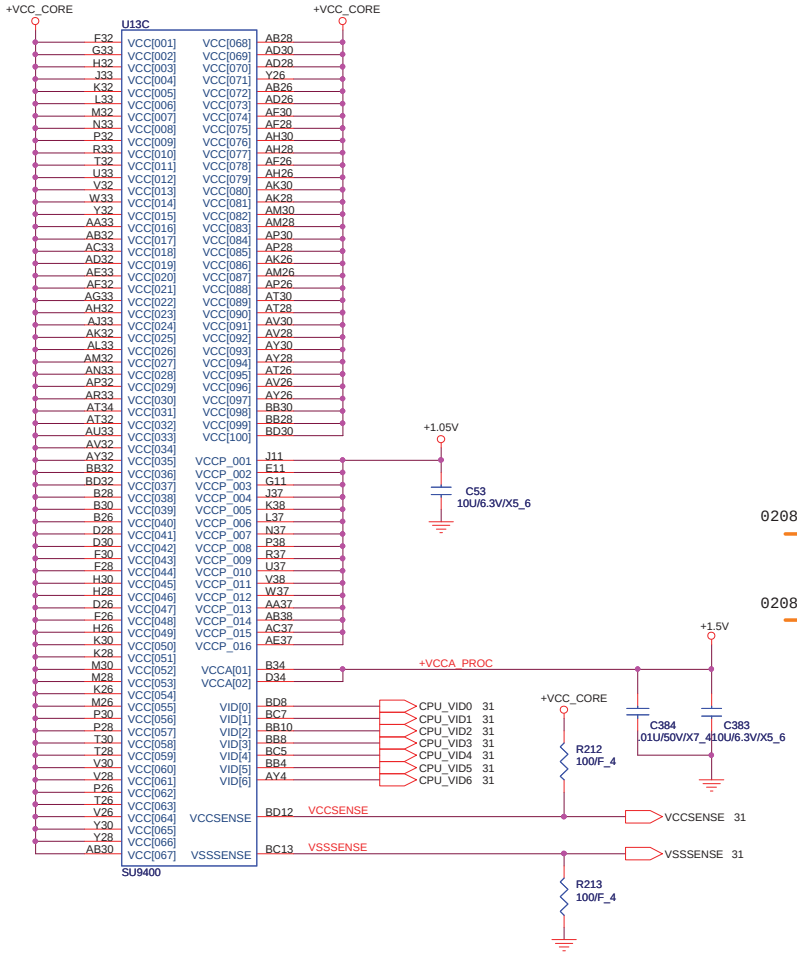
Signal	ITP disable guidelines		
TDI	Resistor Value		
TMS	150 ohm +/- 5%	Connect To	Resistor Placement
TRST#	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TCK	680 ohm +/- 5%	VTT	Within 2.0" of the ITP
TDO	27 ohm +/- 5%	Open GND	Within 2.0" of the ITP
ITP_EN		GND	Within 2.0" of the ITP
	R268 Depop	VTT	Within 2.0" of the ITP
		+3VRUN	Close to CK410M Pin8

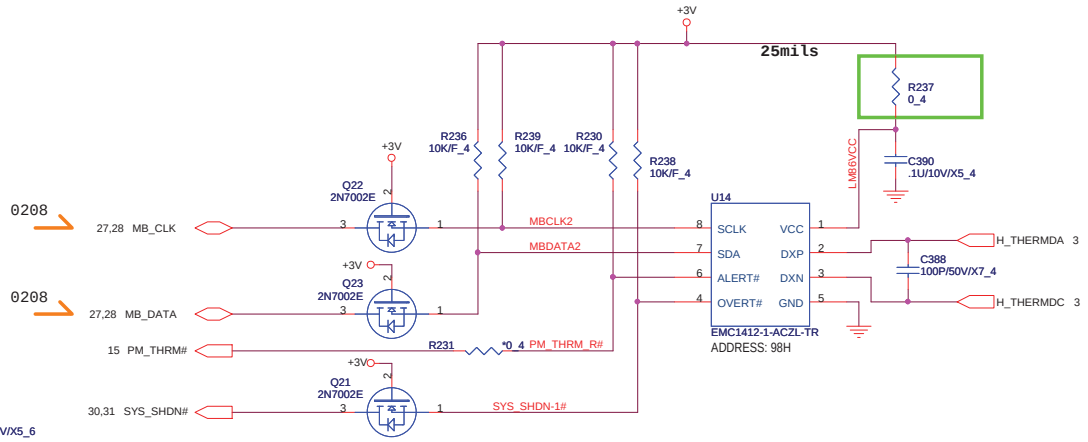
PROJECT : LL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Penryn (HOST BUS) 1/3	1A
Date: Thursday, April 23, 2009	Sheet 3 of 38	



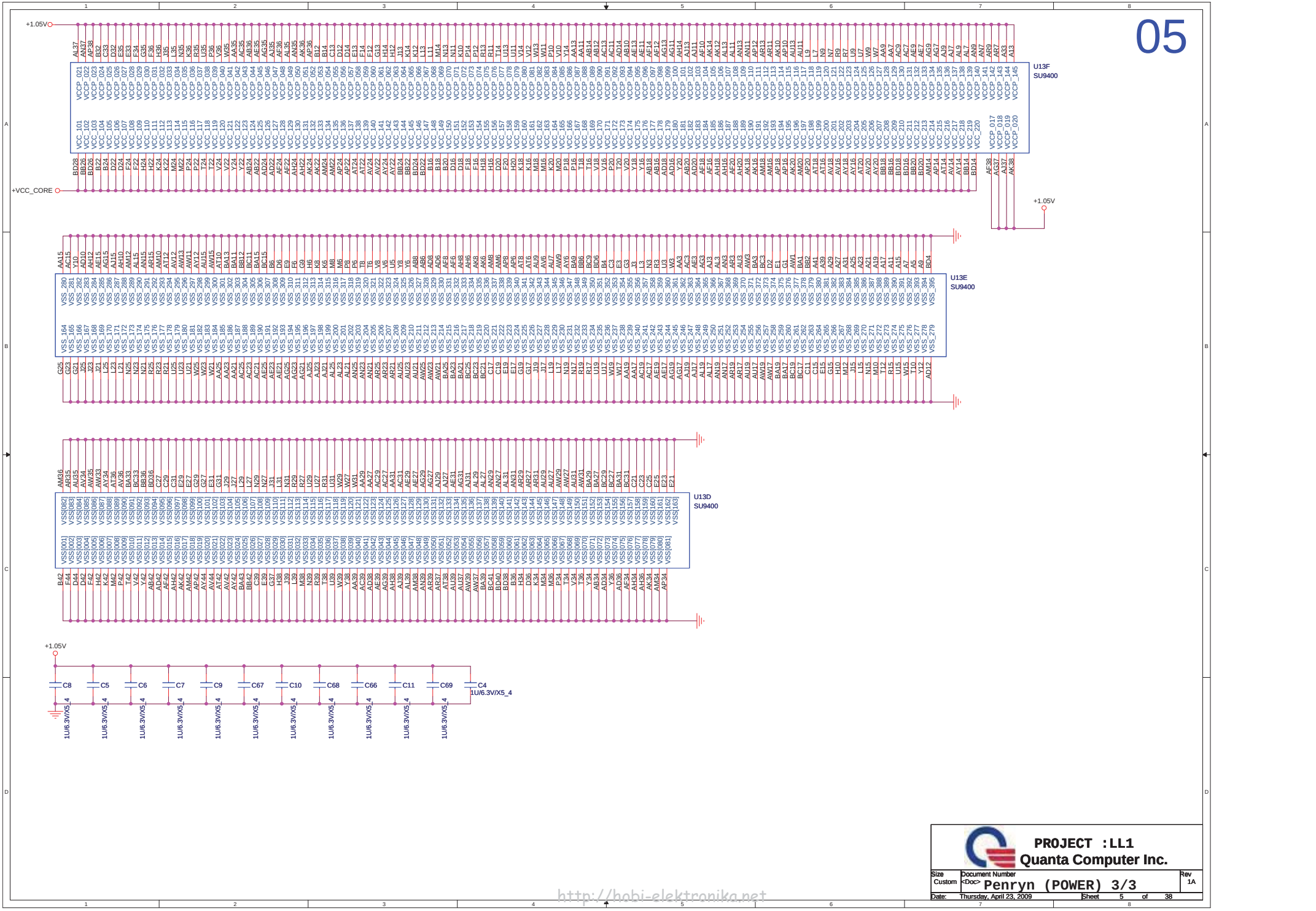
0217 del non-used part.





PROJECT : LL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Penryn (TH Monitor) 2/3	1A
Date: Thursday, April 23, 2009	Sheet 4 of 38	


05
+1.05V
+VCC_CORE
U13F
SU9400
U13E
SU9400
U13D
SU9400
C8
C5
C6
C7
C9
C67
C10
C68
C66
C11
C69
C4
1U/6.3V/X5_4
PROJECT : LL1
Quanta Computer Inc.
Size
Custom
Document Number
<Doc>
Penryn (POWER) 3/3
Rev
1A
Date:
Thursday, April 23, 2009
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5
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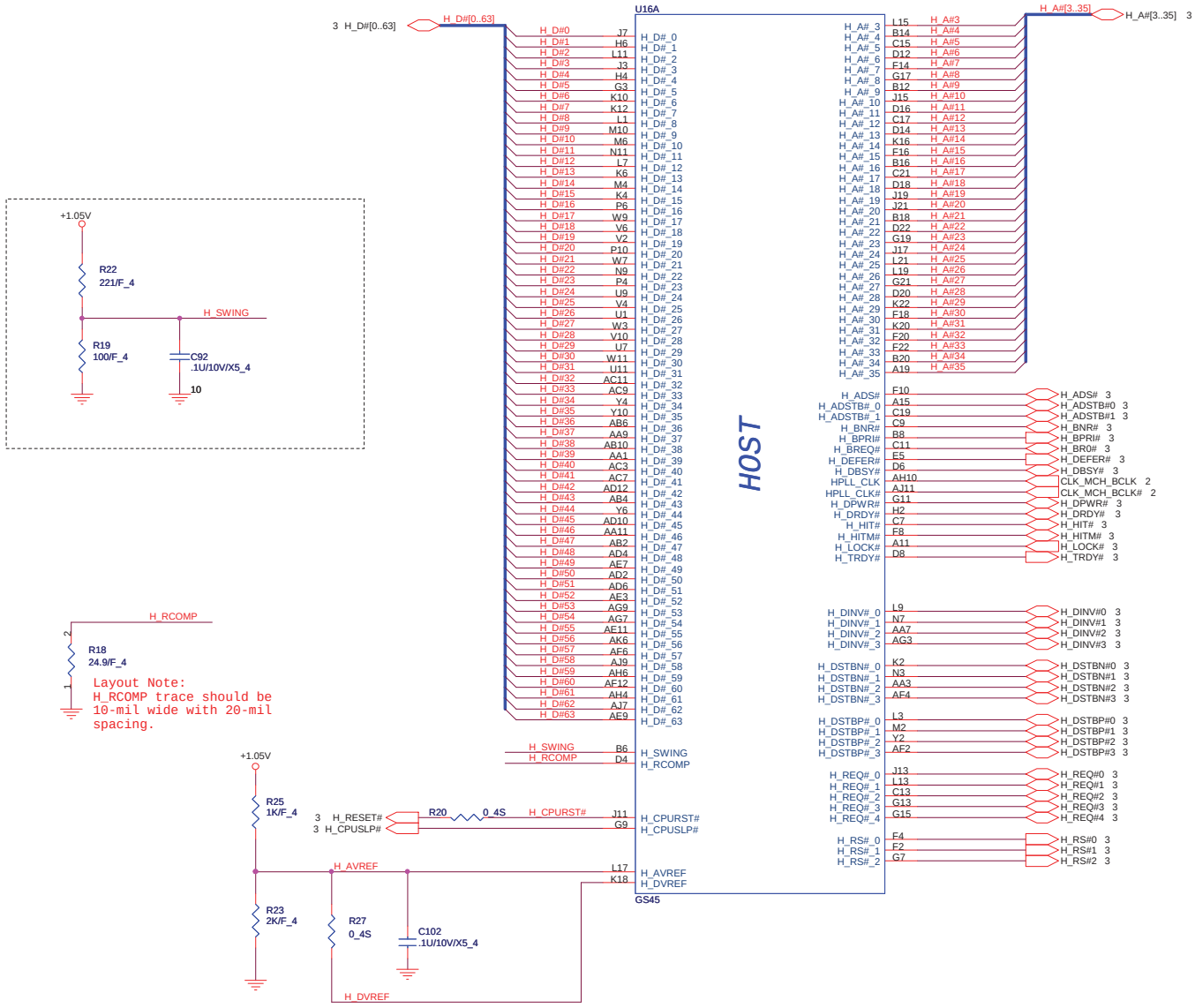
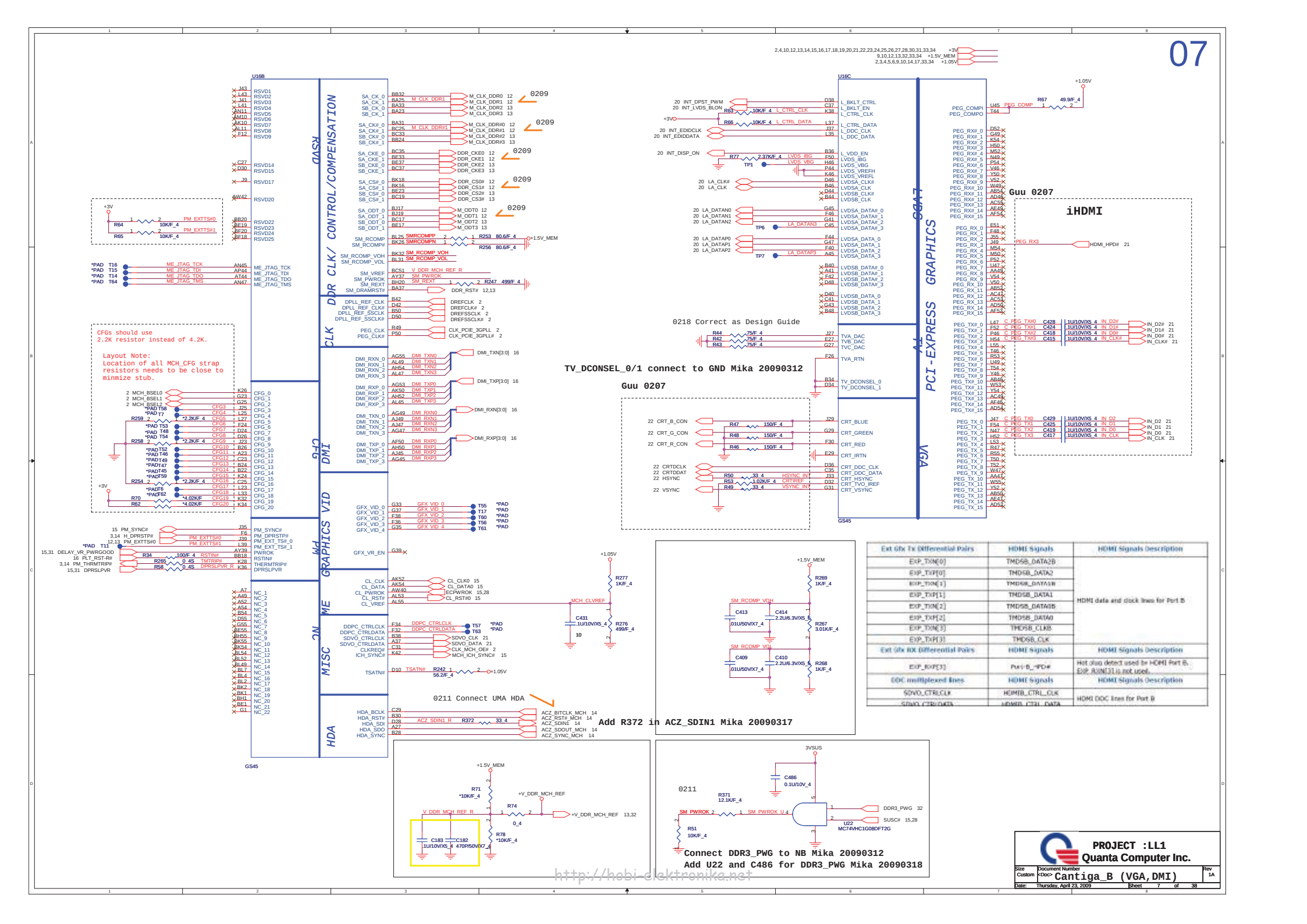


PROJECT : LL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Cantiga_A (HOST)	1A
Date: Thursday, April 23, 2009	Sheet 6 of 38	


U16B
RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
CFG
DMI
PM
GRAPHICS VID
MISC
NC
HDA
U16C
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
GS45
CFGs should use
2.2K resistor instead of 4.2K.
Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minmize stub.
0218 Correct as Design Guide
TV_DCONSEL_0/1 connect to GND Mika 20090312
Guu 0207
iHDMI
0211 Connect UMA HDA
Add R372 in ACZ_SDIN1 Mika 20090317
Connect DDR3_PWG to NB Mika 20090312
Add U22 and C486 for DDR3_PWG Mika 20090318
Ext Gfx Tx Differential Pairs
HDMI Signals
HDMI Signals Description
EXP_TXN[0]
EXP_TXP[0]
EXP_TXN[1]
EXP_TXP[1]
EXP_TXN[2]
EXP_TXP[2]
EXP_TXN[3]
EXP_TXP[3]
TMDSB_DATA2B
TMDSB_DATA2
TMDSB_DATA1B
TMDSB_DATA1
TMDSB_DATA0B
TMDSB_DATA0
TMDSB_CLKB
TMDSB_CLK
HDMI data and clock lines for Port B
Ext Gfx RX Differential Pairs
EXP_RXP[3]
Hot plug detect used for HDMI Port B.
EXP_RXN[3] is not used.
DDC multiplexed lines
SDVO_CTRLCLK
SDVO_CTRLDATA
HDMIB_CTRL_CLK
HDMIB_CTRL_DATA
HDMI DDC lines for Port B
PROJECT :LL1
Quanta Computer Inc.
Size: Custom
Document Number: <Doc> Cantiga_B (VGA, DMI)
Rev: 1A
Date: Thursday, April 23, 2009
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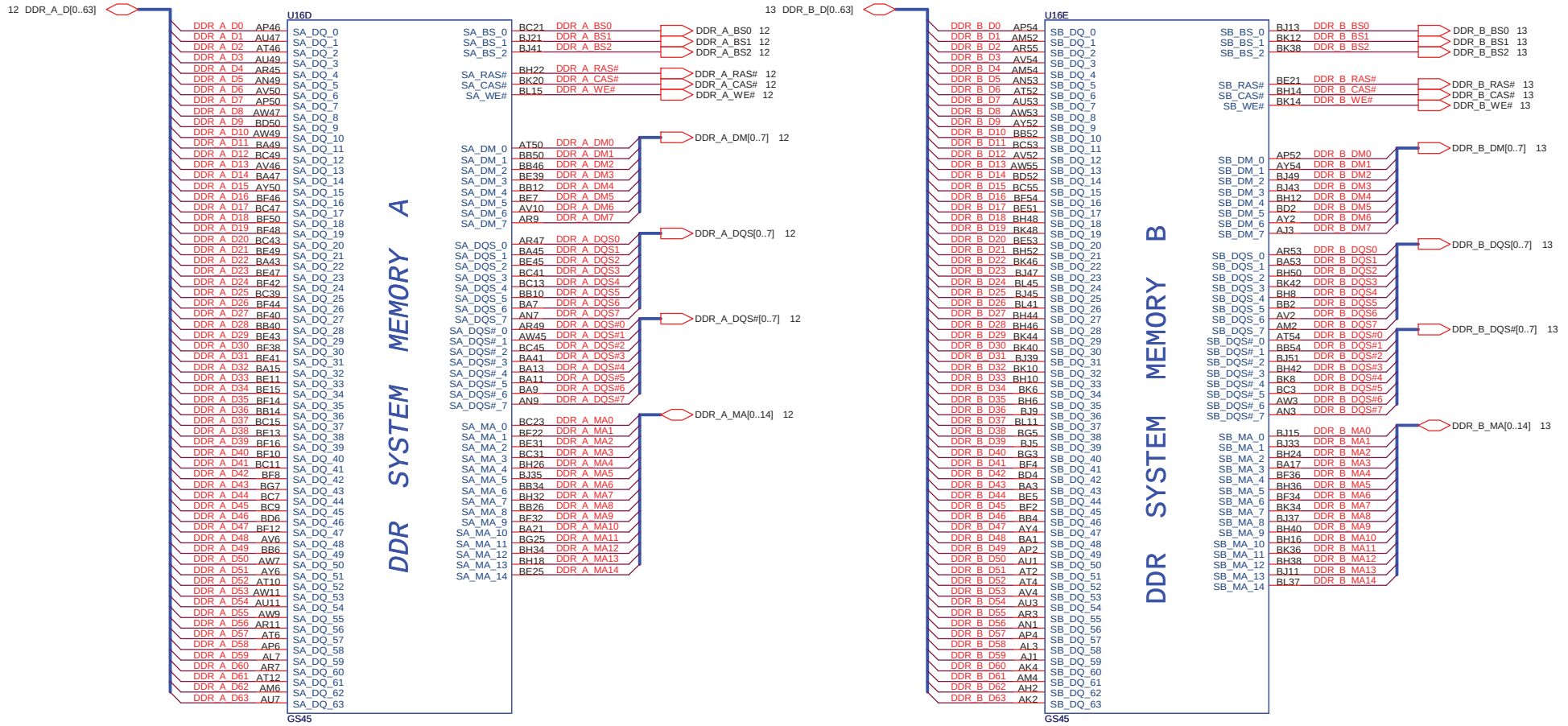
http://hobi-elektronika.net



PROJECT :	LL1
Quanta Computer Inc.	
Size: Custom	Document Number: <Doc> Cantiga_C (DDR interface)
Rev:	1A
Date: Thursday, April 23, 2009	Sheet 8 of 38

Ivcc_sm (DDR3,1.5V,1066MTs) -->4140mA

IVCC_AXG-->7700mA(GS45)

Layout Note:
370 mils from edge.

Layout Note:
Inside GMCH cavity.

Layout Note:
370 mils from edge.

U16G

U16F

VCC_SM POWER

VCC GFX_NCTF

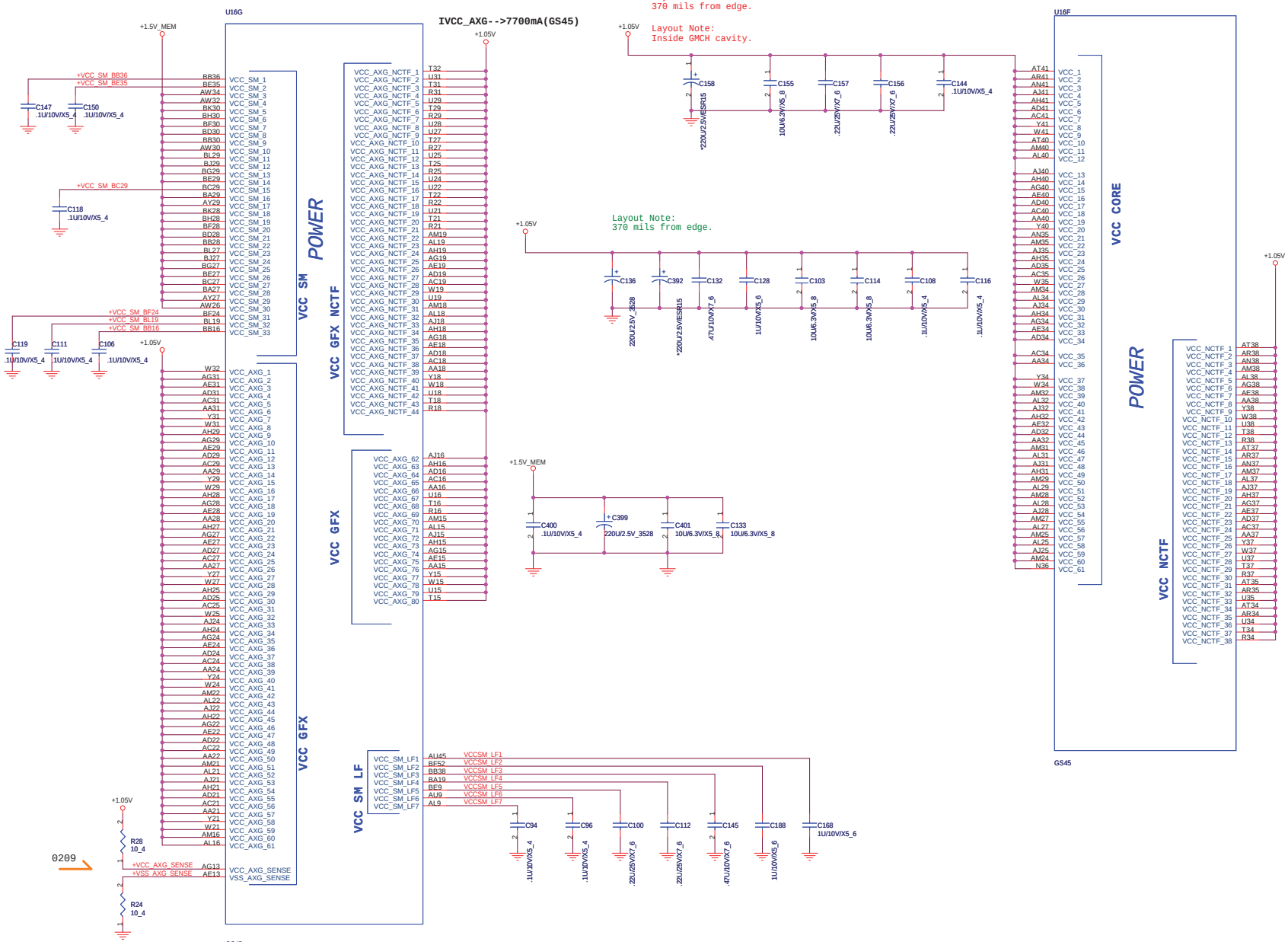
VCC GFX

VCC SM_LF

VCC CORE

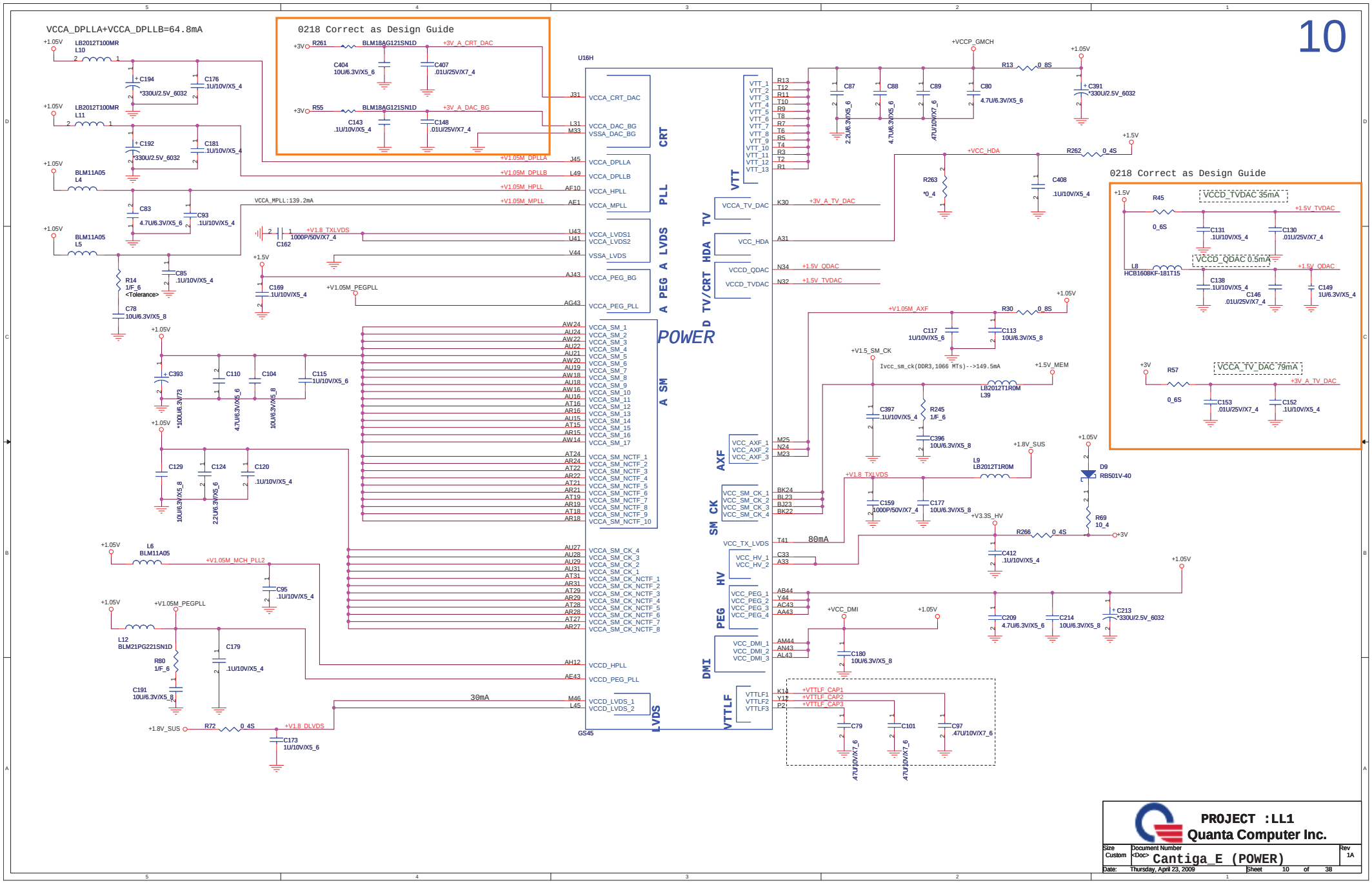
VCC NCTF POWER

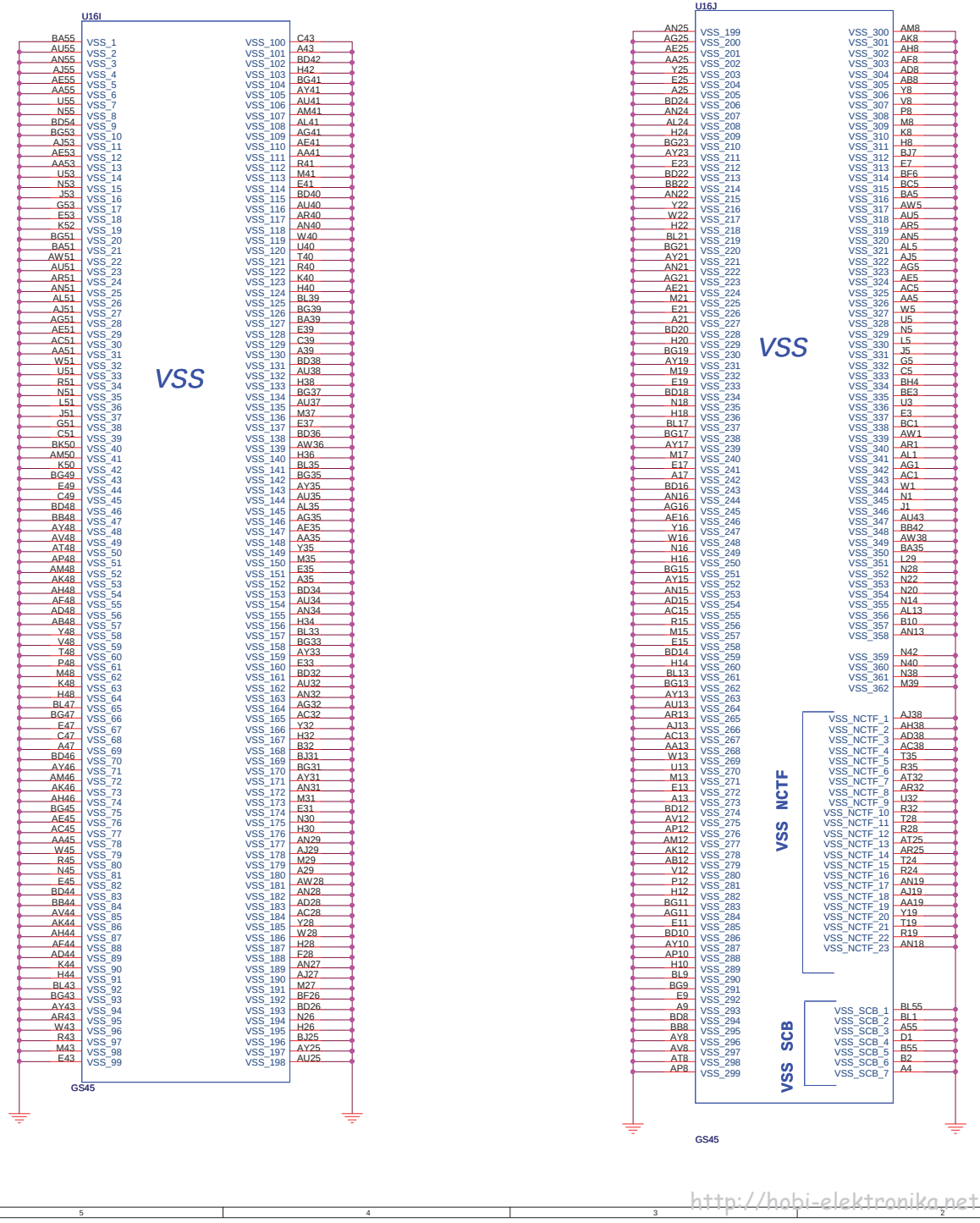
GS45



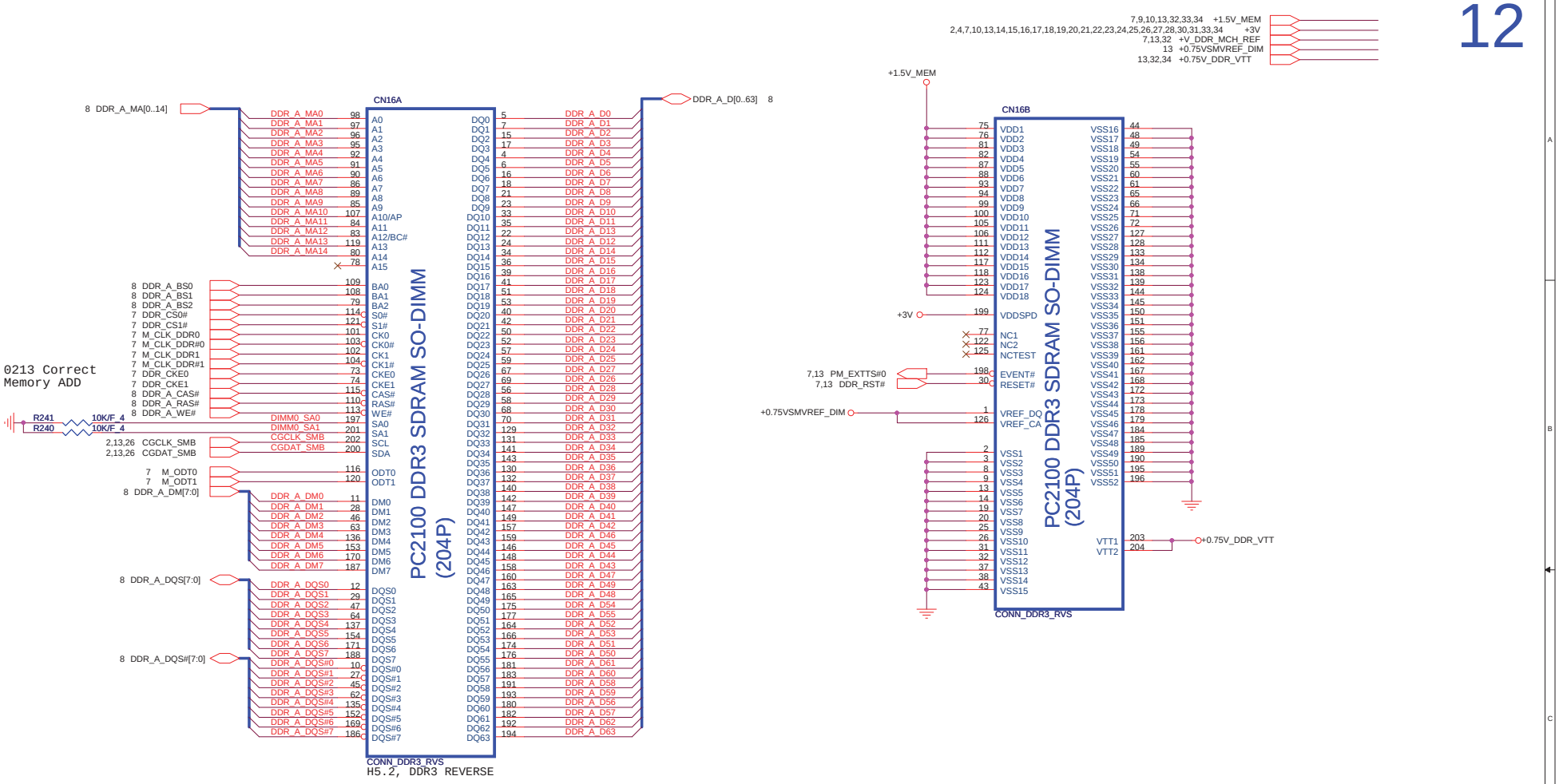
PROJECT :LL1
Quanta Computer Inc.

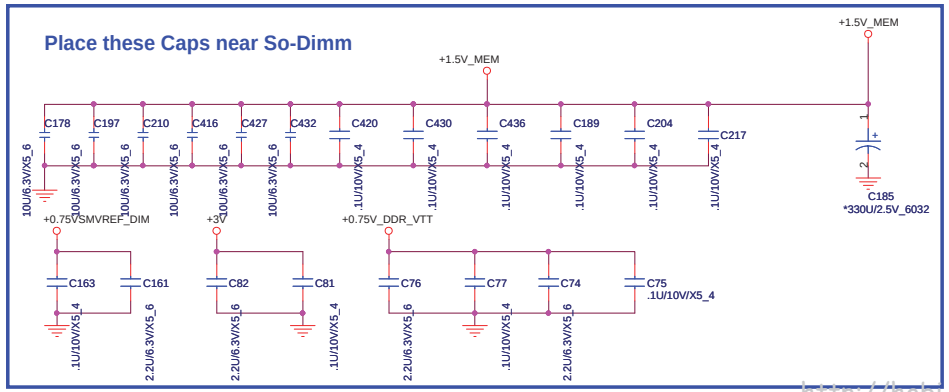
Size	Document Number	Rev
Custom	<Doc> Cantiga_D (VCC,NCTF)	1A
Date: Thursday, April 23, 2009	Sheet 9 of 38	





PROJECT : LL1	
Quanta Computer Inc.	
Size: Custom	Document Number: <Doc> Cantiga_F (VSS)
Rev: 1A	
Date: Thursday, April 23, 2009	Sheet 11 of 38

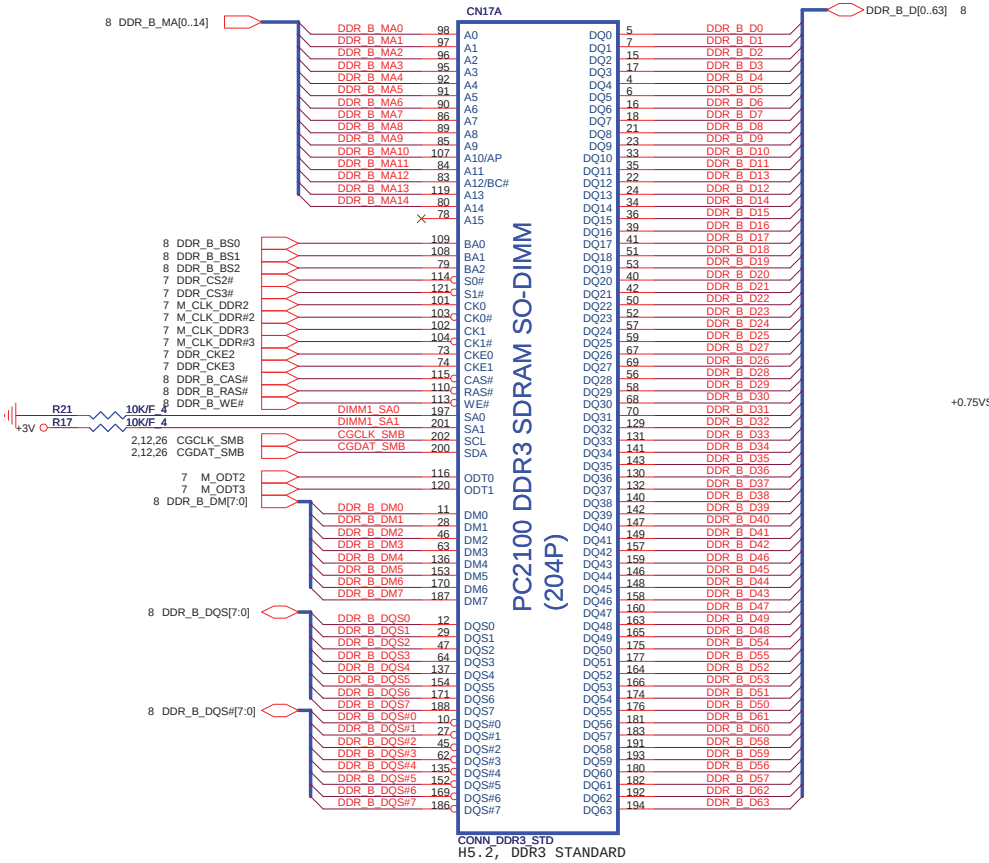


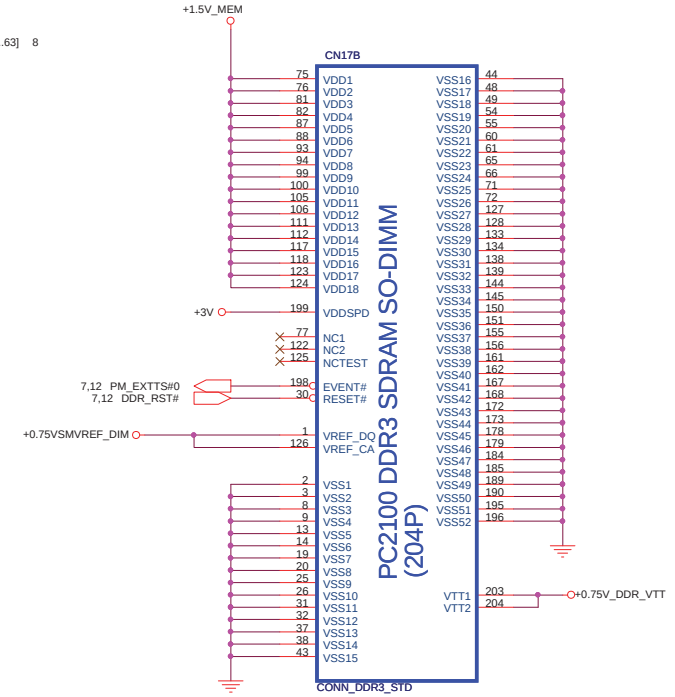


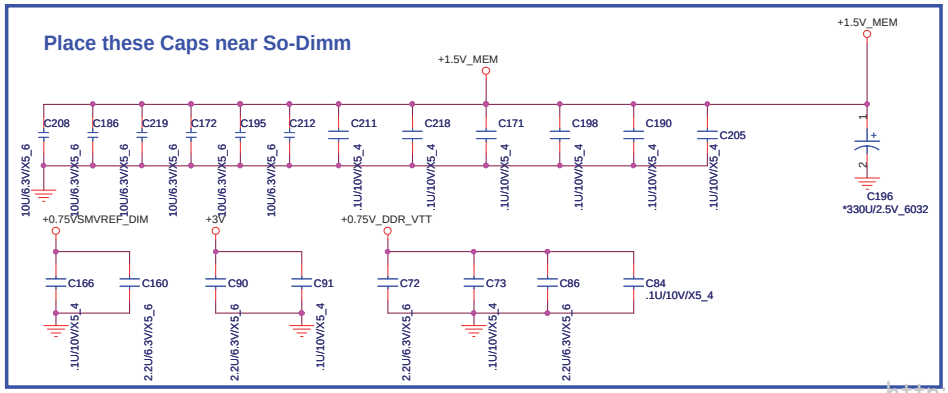
Size: Custom	Document Number: <Doc> DDR3 (A) SO-DIMM RVS		Rev: 1A
Date: Thursday, April 23, 2009		Sheet 12 of 38	

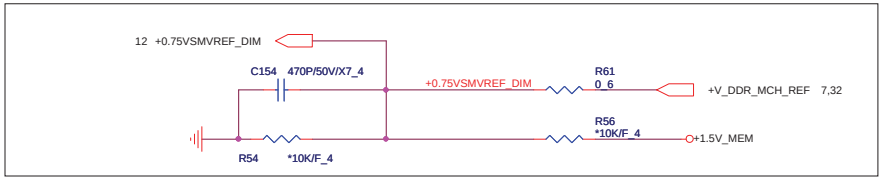
PROJECT : LL1
Quanta Computer Inc.

7,9,10,12,32,33,34 +1.5V_MEM
2,4,7,10,12,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,30,31,33,34 +3V
12,32,34 +0.75V_DDR_VTT
7,32 +V_DDR_MCH_REF



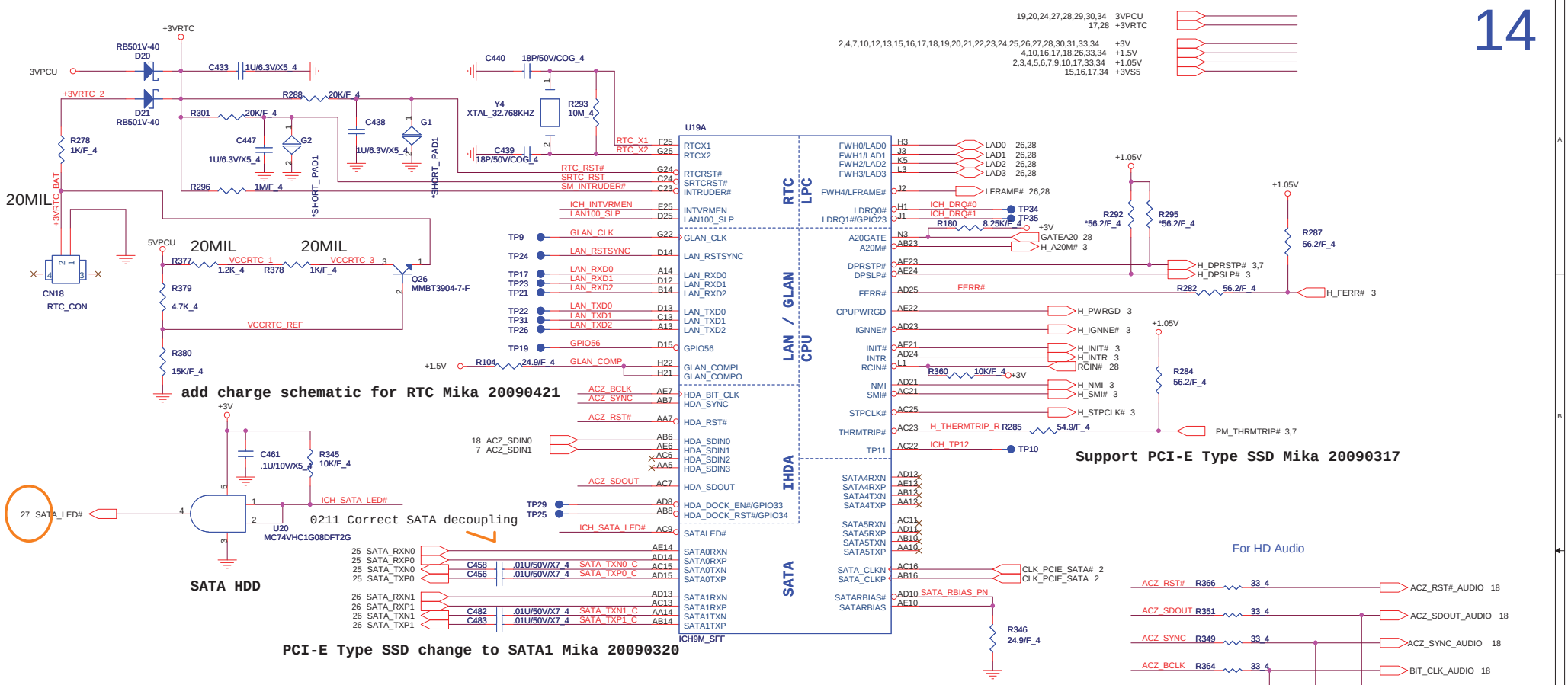






PROJECT : LL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> DDR3 (B) SO-DIMM STD	1A
Date: Thursday, April 23, 2009	Sheet 13 of 38	



SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

PROJECT : LL1 Quanta Computer Inc.			
Size: Custom	Document Number: <Doc> ICH9-M_A_(CPU,SATA,IDE)		Rev: 1A
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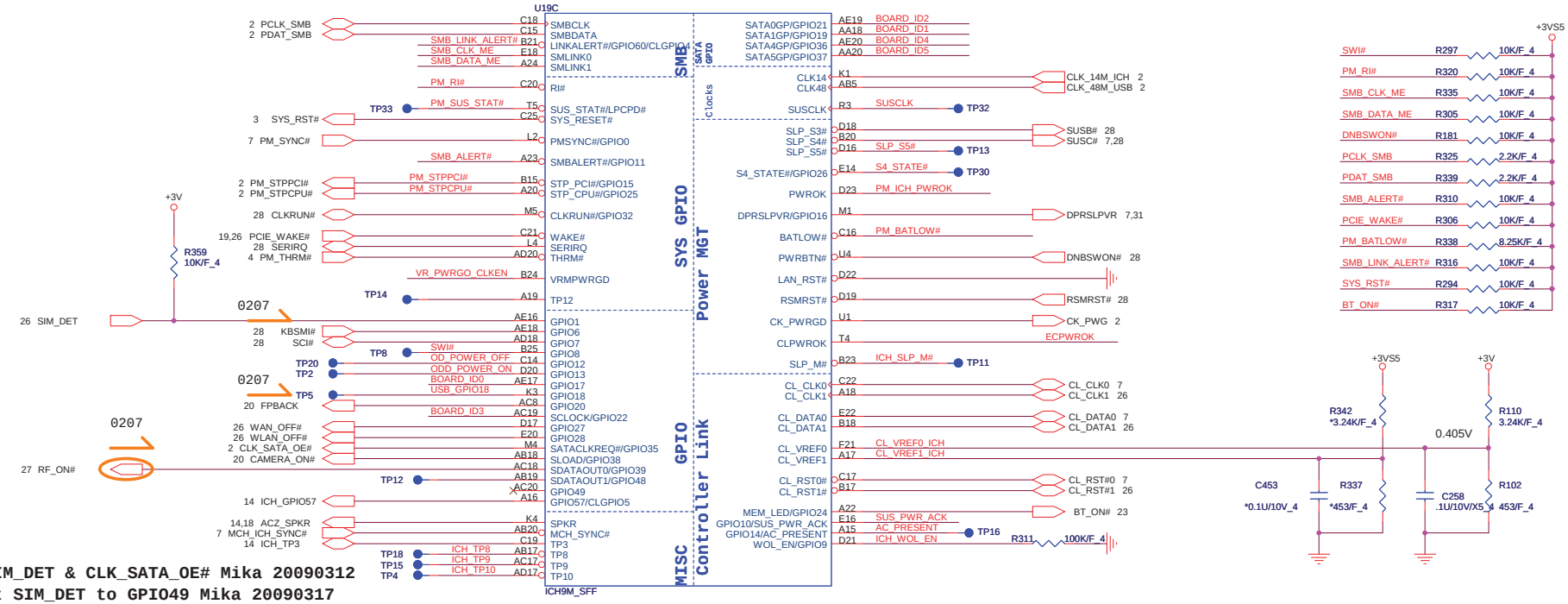
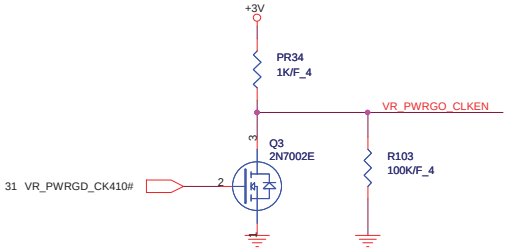
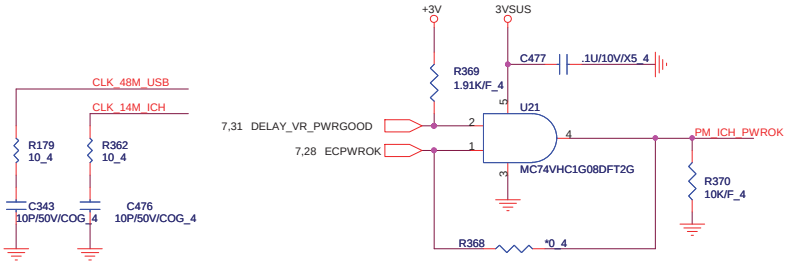
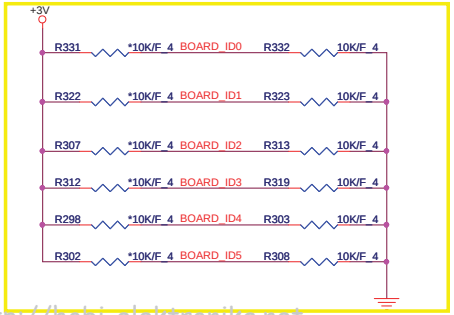


Swap SIM_DET & CLK_SATA_OE# Mika 20090312
Connect SIM_DET to GPIO49 Mika 20090317
Connect SIM_DET to GPIO1 Mika 20090319





RESERVED BOARD ID



PROJECT : LL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> ICH9-M_C_(PM,GPIO,SMB)	1A
Date: Thursday, April 23, 2009	Sheet 15 of 38	

Place TX DC blocking caps close ICH9.

WLAN

0207

WWAN

Del PCI-E interface (WWAN use USB type) Mika 20090317

Change WLAN to PCI-E-2 Mika 20090318

LAN

0219

0219 Swap per SW suggestion.

USB port	Assignment function
USB0	USB Connector onboard
USB1	USB Connector on function board
USB2	BLUETOOTH
USB3	X
USB4	Mini PCI E
USB5	Mini PCI E
USB6	USB Connector on function board
USB7	X
USB8	USB Card Reader on function board
USB9	X
USB10	CCD
USB11	X

PROJECT : LL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> ICH9-M_B_(USB,PCIE,DMI)	1A

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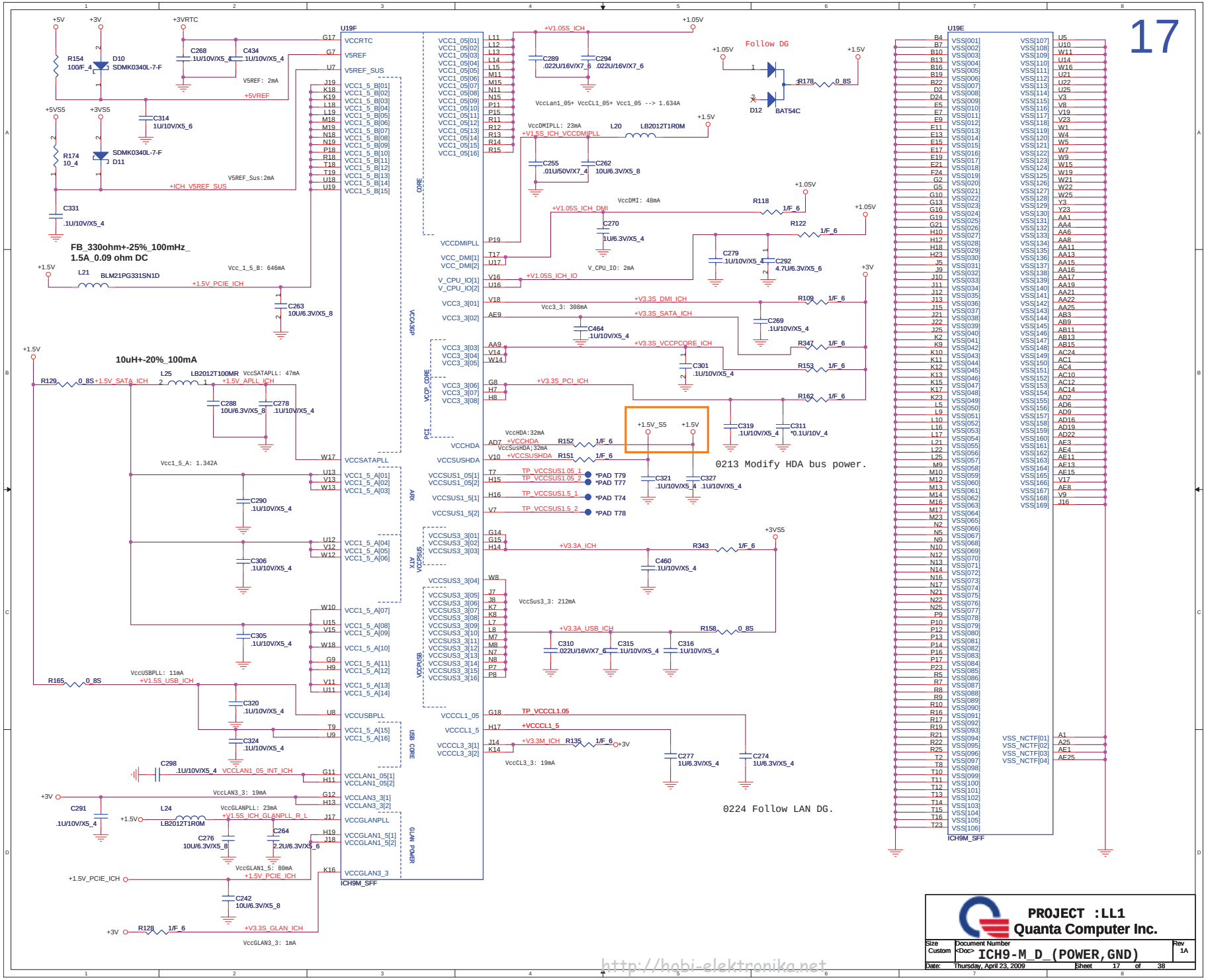
17
U19F
U19E
ICH9M_SFF
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
10uH+-20%_100mA
Follow DG
0213 Modify HDA bus power.
0224 Follow LAN DG.
PROJECT : LL1
Quanta Computer Inc.
ICH9-M_D_(POWER,GND)
Size Custom
Document Number
Rev 1A
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Add C480 and C481 Mika 20090316

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

0213 Modified(LC)

0226 change to 0805

Change R344 to 1206 size Mika 20090316

HD Audio Bus

Note:

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

0213 Modified(LC)

0224 Cnxt review to reserve for Beep Gain.

MIC Decoupling close to Codec

HP/ MIC jack Decoupling close to Connector

Change C235 to 0.1U Mika 20090316

0213 Modify Mute# to EXTMUTE#

EC_MUTE	HP_PLUG	AMP_SHDN#
0	0	1
0	1	0
1	0	0
1	1	0

Del R156 and Q8 then short Volmute# directly Mika 20090318

PC BEEP CONTROL

Close to codec

Change PC_BEEP voltage level to 1/10 Mika 20090319
Change PC_BEEP voltage level to 2/3 Mika 20090421

Connect to Function Board

HEADPHONE Normal Open

0211 Conexant review Audio page.
0213 Move Jack related to daughter board

MIC-IN JACK Normal Close

0211 Conexant review Audio page.
0213 Move Jack related to daughter board
By vendor suggestion "D22 and D23 close to codec"Mika 20090421

INT MIC

0213 Modified (LC)

0211 Conexant review Audio page.
0212 Change MIC conn. to daughter board
0224 Del decoupling Cap. and change Pull High.
0224 Change MIC_BIAS to Codec.
0209 Correct netname.

INT Speaker

Change R166~R169 to 0603 size Mika 20090316
Change R166~R169 from 0ohm to BK1608HS601 Mika 20090320

EMI Close to Pin out

HP Sense

MIC Sense

EXT_MIC_PLUG=H ---- EXTERNAL MIC
EXT_MIC_PLUG=L ---- INTERNAL MIC
MIC JACK DECT PIN IS NORMAL CLOSE TYPE

EMI Reserved

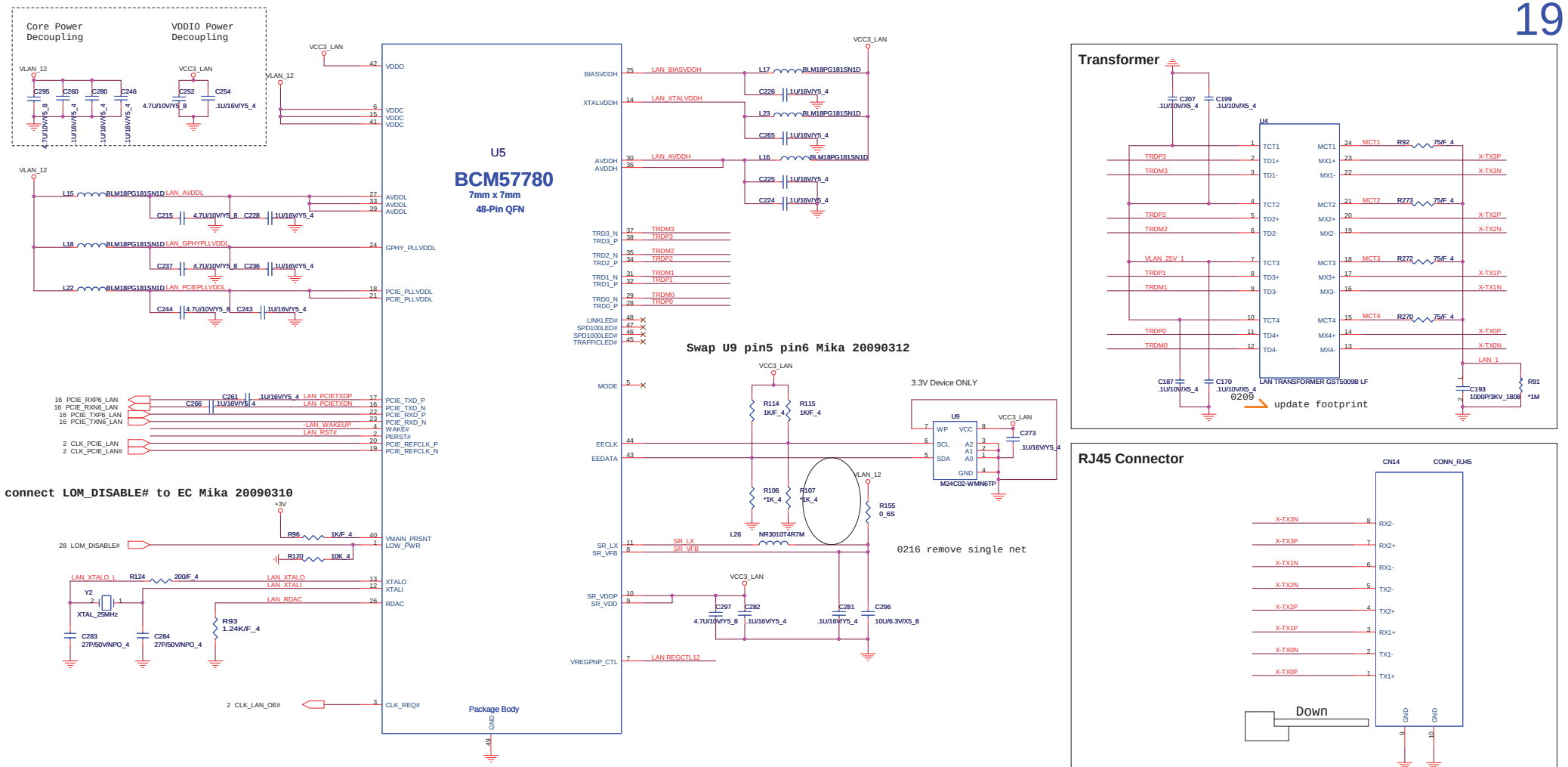
Del R94,R163 to short AGND and GND directly Mika 20090316

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

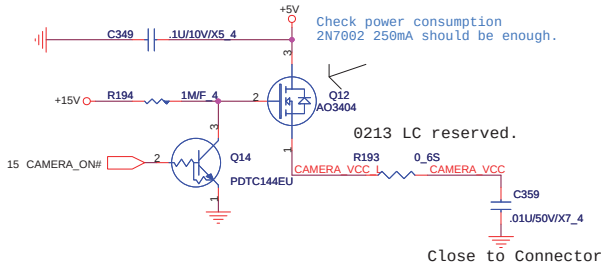
PROJECT : LL1
Quanta Computer Inc.

Size: Custom | Document Number: <Doc> AUDIO (CX20582, SPK) | Rev: 1A
Date: Thursday, April 23, 2009 | Sheet 18 of 38

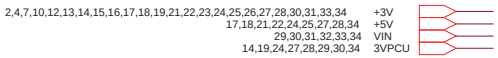


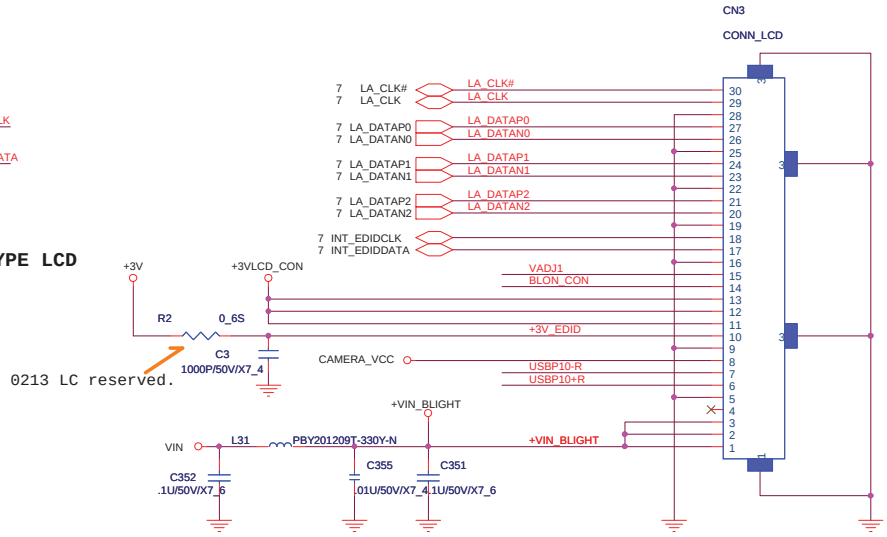
PROJECT :	LL1
Quanta Computer Inc.	
Size: Custom	Document Number: <Doc> LAN (BCM57780, RJ45) Rev: 1A
Date: Thursday, April 23, 2009	Sheet 19 of 38

CCD POWER CONTROL



SUPPORT 13.3" LED TYPE LCD



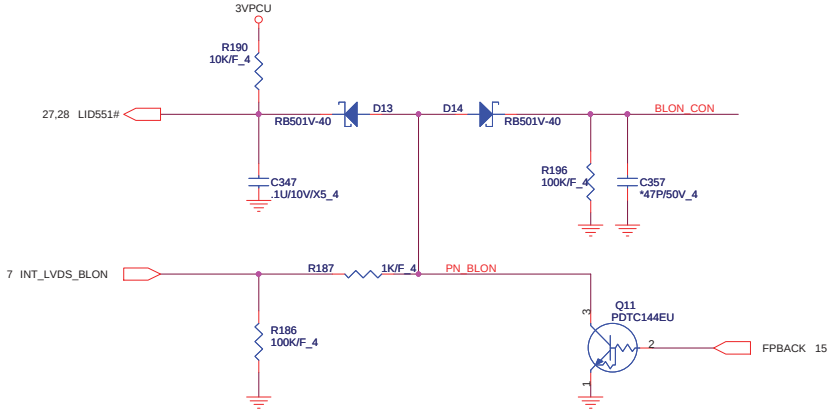


0213 LC reserved.

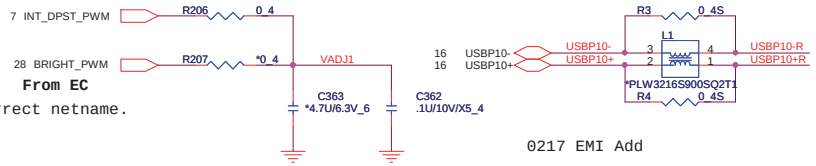
Close to LCD Connector

0212 Update footprint.

BACK LIGHT CONTROL



From NB

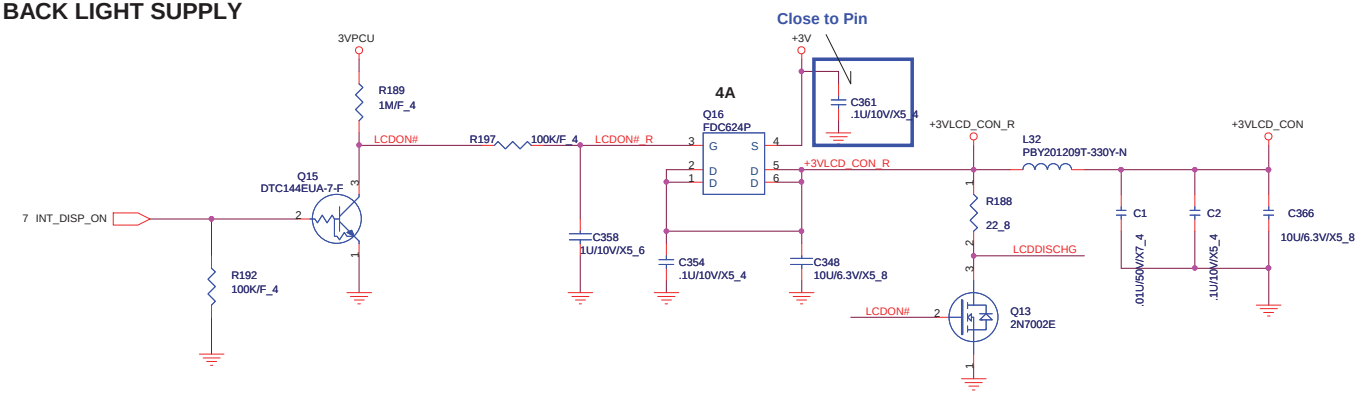


From EC

0209 Correct netname.

0217 EMI Add

BACK LIGHT SUPPLY



PROJECT : LL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> CONN (LVDS, CCD)	1A
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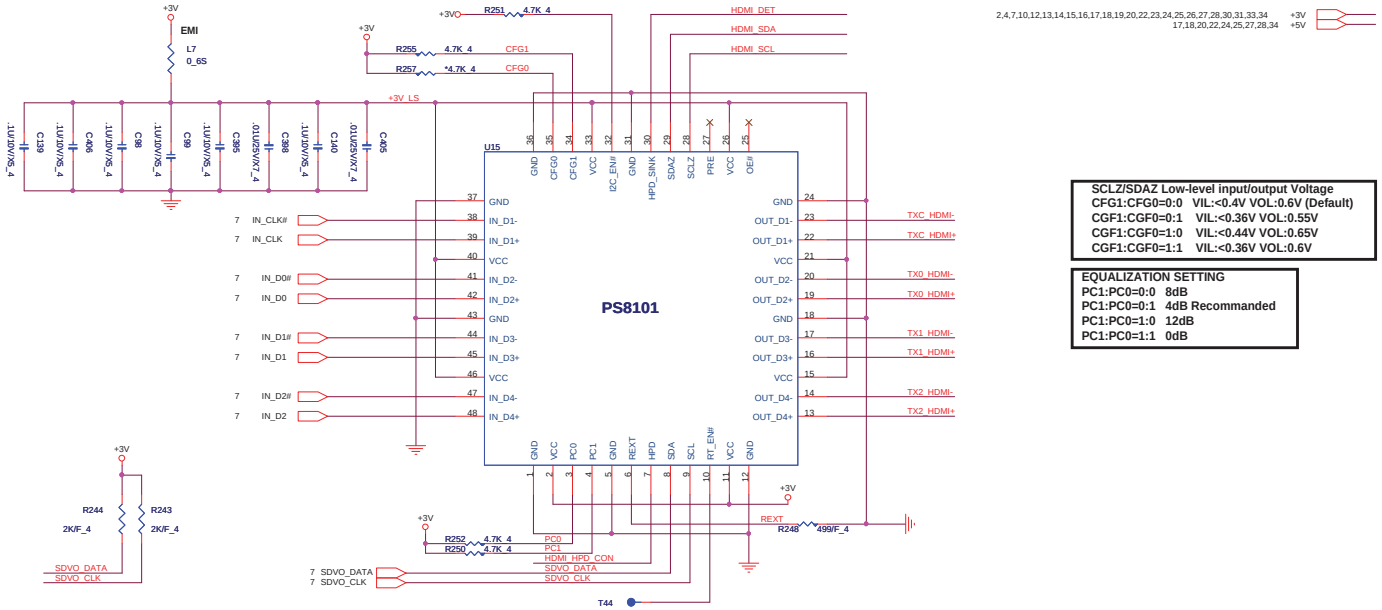
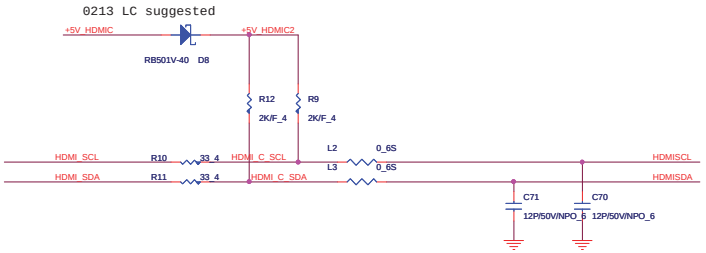


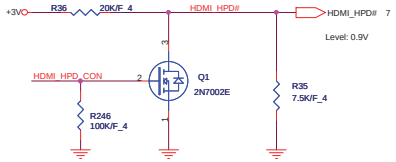
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

Reserve RP11~RP13 for EMI request Mika 20090422
Remove RP4~RP6 and add R373~R375 Mika 20090320
Change RP3 from 0ohm to WCM-2012-900T Mika 20090320

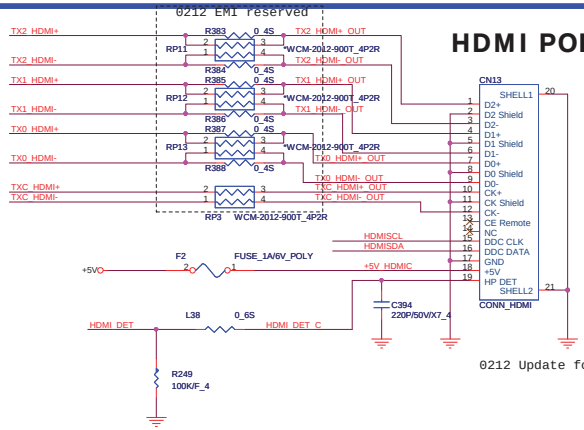
0213 LC suggested





HPD# Inverting Level Shifting Circuit

0212 EMI reserved



HDMI PORT

Down

0212 Update footprint.

PROJECT :LL1
Quanta Computer Inc.

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C	<Doc> CONN (HDMI, level Shift)	1A
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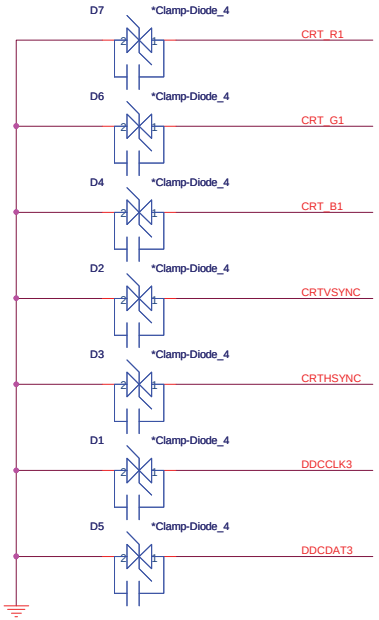
Swap CN5 Pin1,2,3,4,5 & Pin11,12,13,14,15 Mika 20090312
Change CN5 footprint Mika 20090318

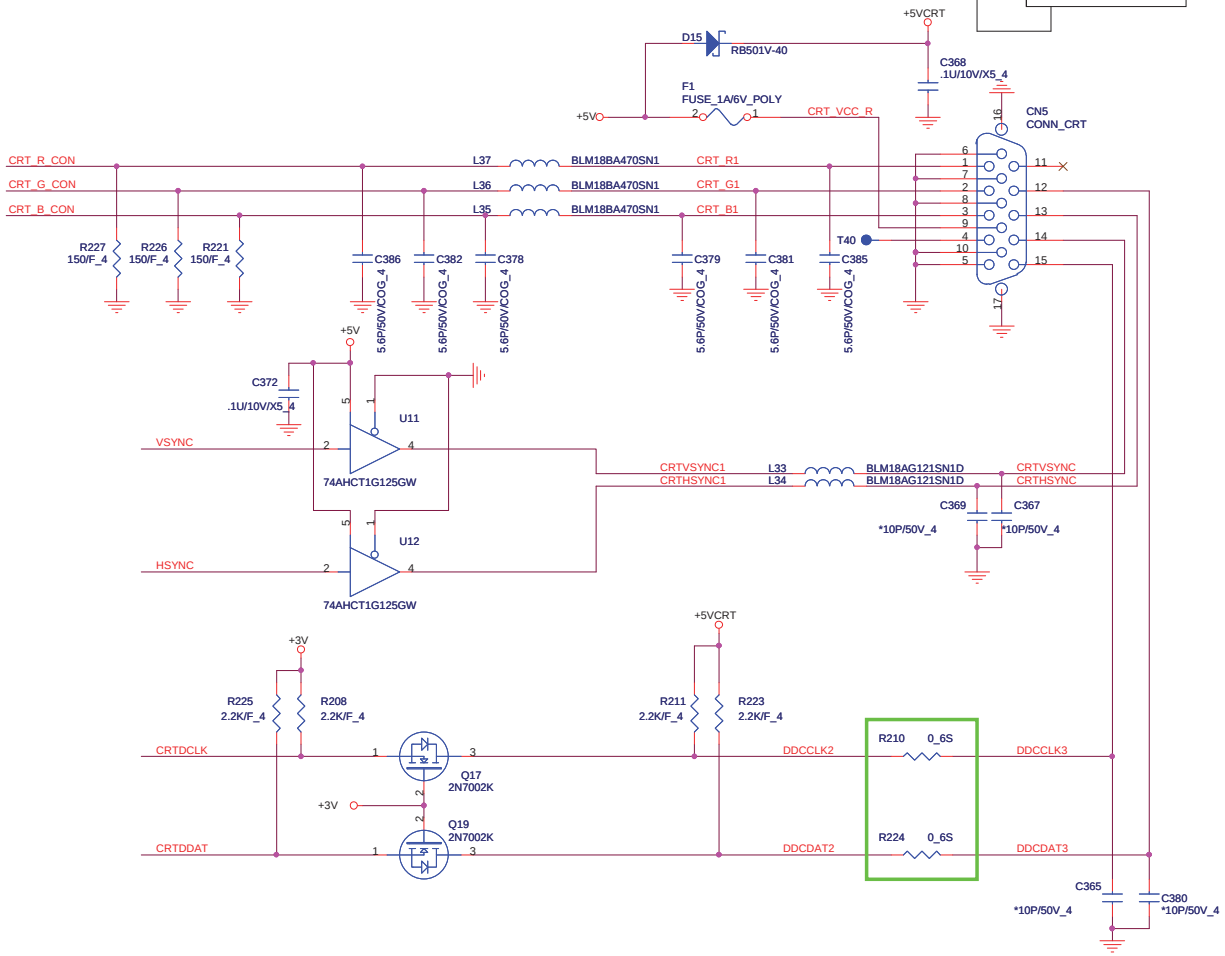
Down

CRT PORT

7 CRT_R_CON → CRT_R_CON
7 CRT_G_CON → CRT_G_CON
7 CRT_B_CON → CRT_B_CON
7 HSYNC → HSYNC
7 VSYNC → VSYNC
7 CRTDCLK → CRTDCLK
7 CRTDDAT → CRTDDAT



0218 Change by ESD suggestion



PROJECT : LL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> CONN (CRT)	1A
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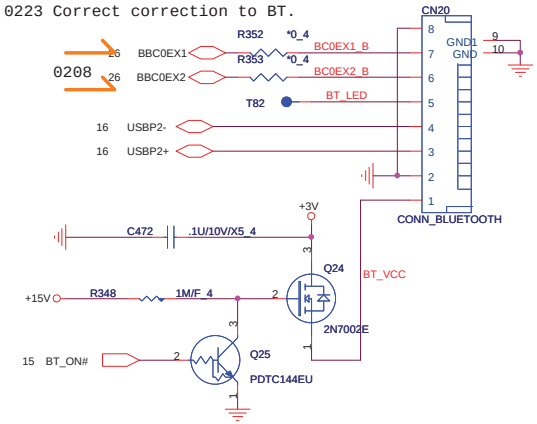
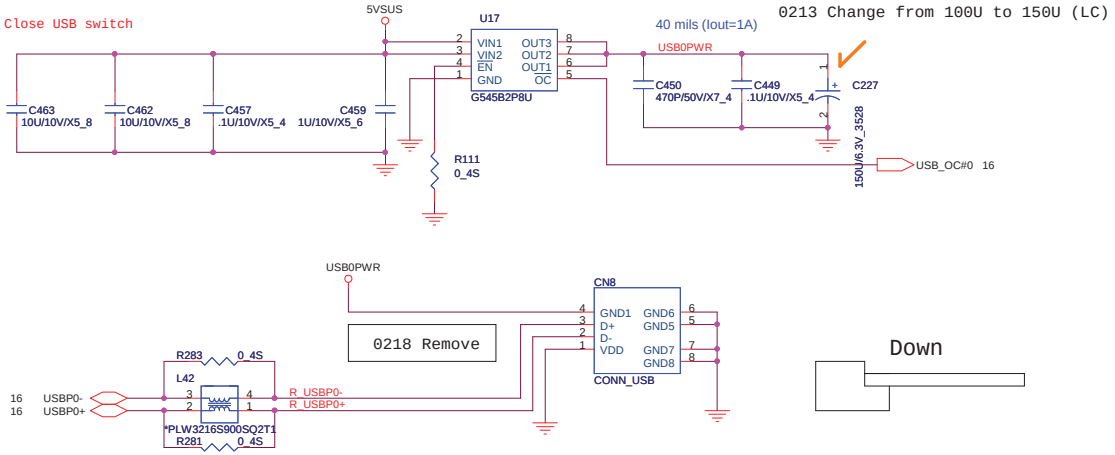
Blue Tooth control



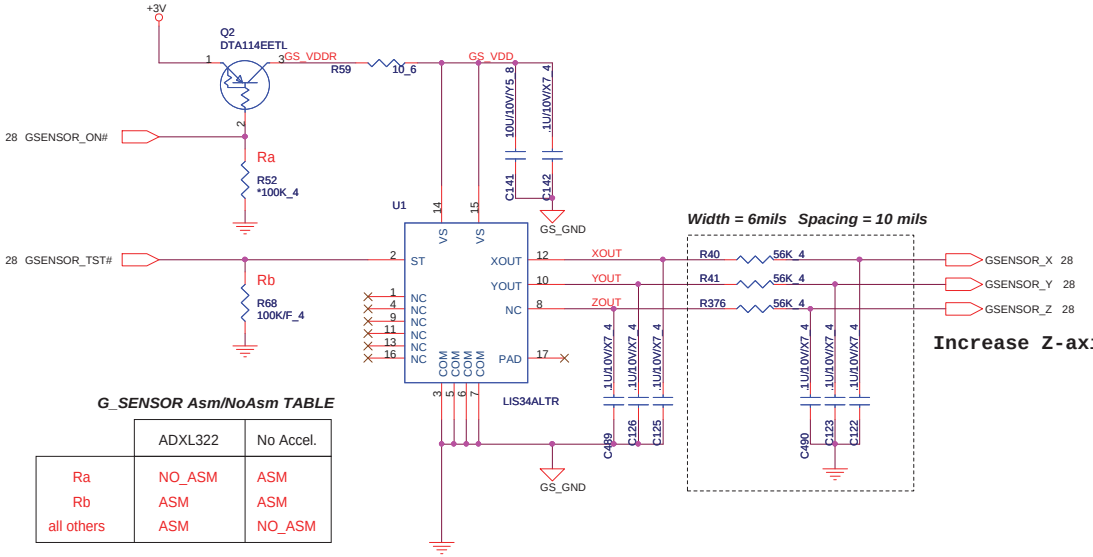
USB port X1



0207 update footprint.
0224 SWAP USB Net

Change USB CONN footprint Mika 20090305
Change USB CONN footprint Mika 20090318

Accelerometer Sensor



Increase Z-axis signal Mika 20090415

G_SENSOR Asm/NoAsm TABLE

	ADXL322	No Accel.
Ra	NO_ASM	ASM
Rb	ASM	ASM
all others	ASM	NO_ASM

0209 update footprint.
0213 Follow HengshanII (LE8)

PROJECT : LL1		
Quanta Computer Inc.		
Size: Custom	Document Number: <Doc> CONN (USB, BT, G sensor)	Rev: 1A
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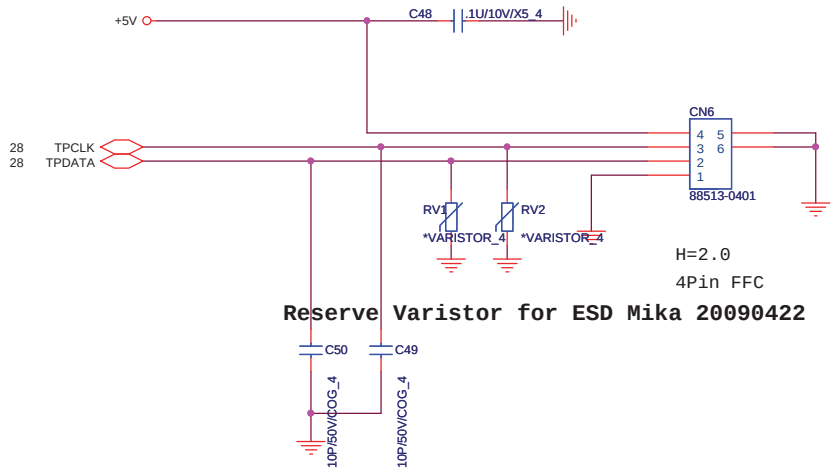
TOUCH PAD CONNECTOR



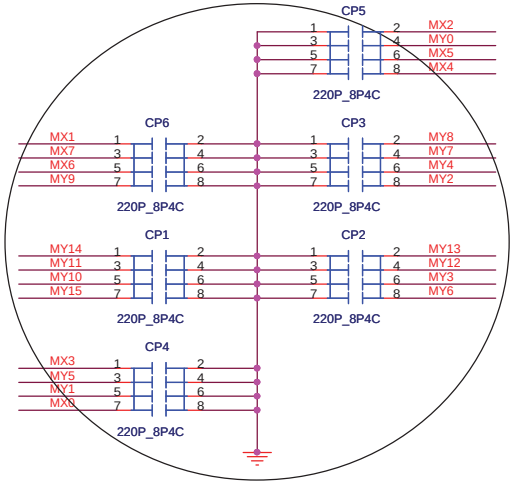
H=2.0
4Pin FFC

Reserve Varistor for ESD Mika 20090422

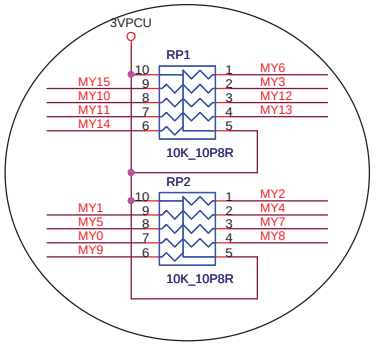
0212 Swap Pin definition
0216 Change TP conn. to 6P.

Change TP CONN to 4P Mika 20090305
Swap TP CONN Mika 20090312

KEYBOARD CONNECTOR

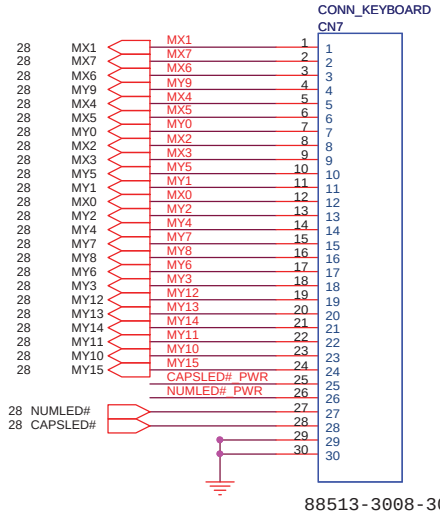


<-- Swap signal Mika 20090306



0223 Swap Keyboard Matrix for Routing

Swap pin definition Mika 20090305



88513-3008-30P-L

0212 Swap Pin definition

PROJECT : LL1 Quanta Computer Inc.		
Size: B	Document Number: <Doc> CONN (KB, TP)	Rev: 1A
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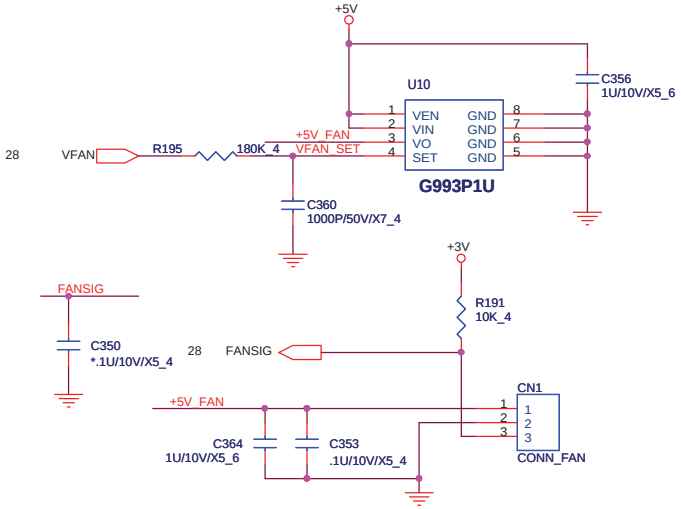
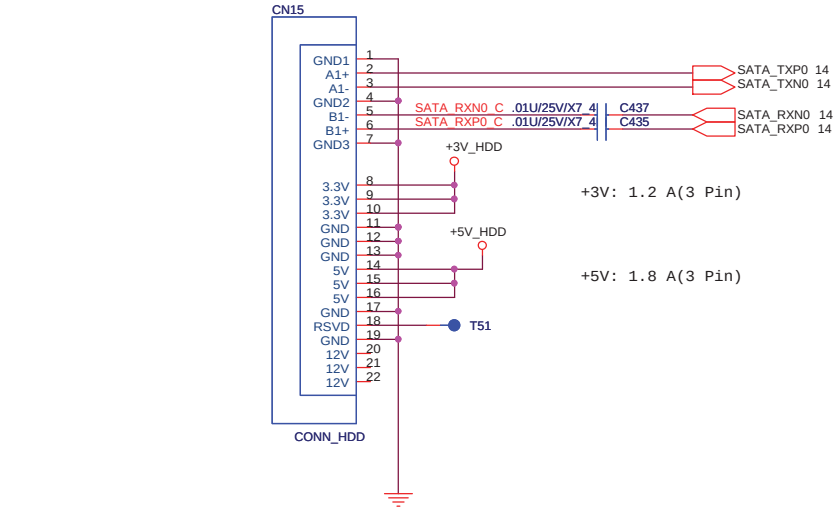
FAN CONTROL



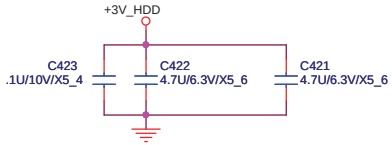
0210 Change Fan connector.
Follow KL1 Pin define.

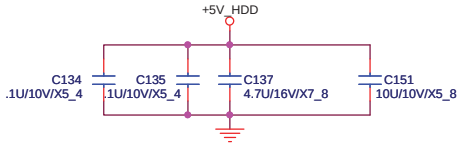
0217 change to right angle part.

SATA-HDD CONNECTOR



0213 Reserved for EMI, power consumption





PROJECT : LL1 Quanta Computer Inc.		
Size: B	Document Number: <Doc> CONN (HDD,FAN)	Rev: 1A
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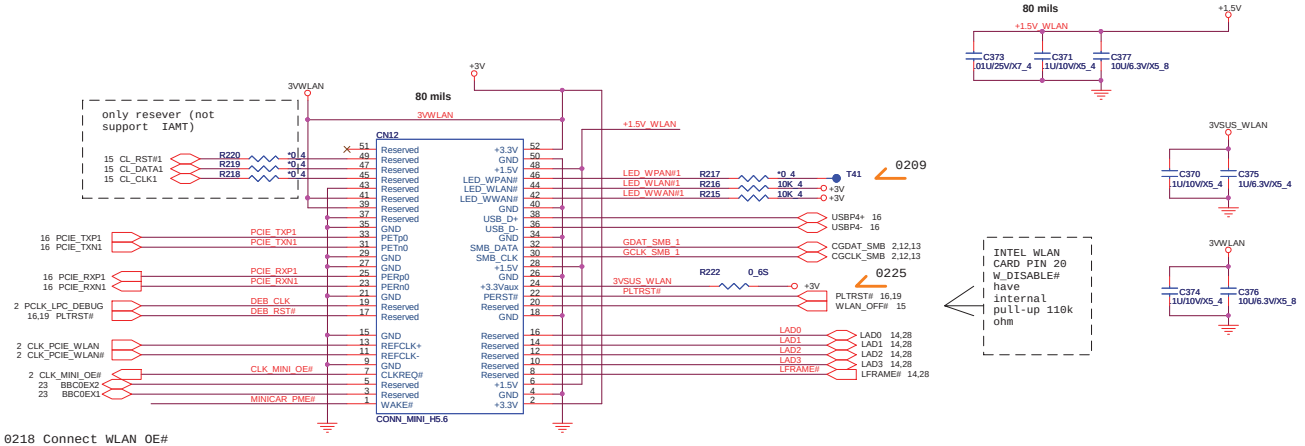
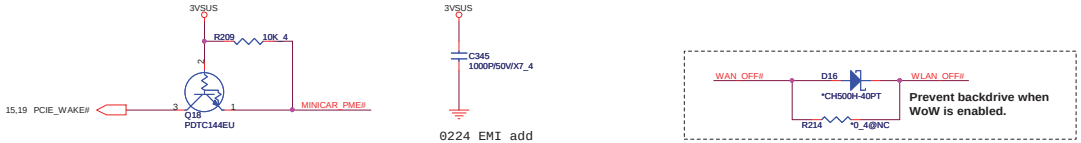
Mini PCI-E Card 1
WLAN



0218 Connect WLAN OE#

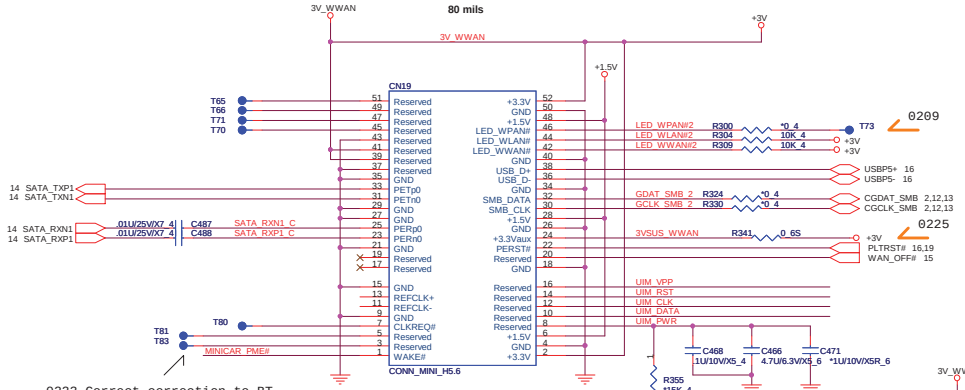
INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm



0224 EMI add

Mini PCI-E Card 2
WWAN(W/SIM)

R222 and R341 Connect to +3V Mika 20090318

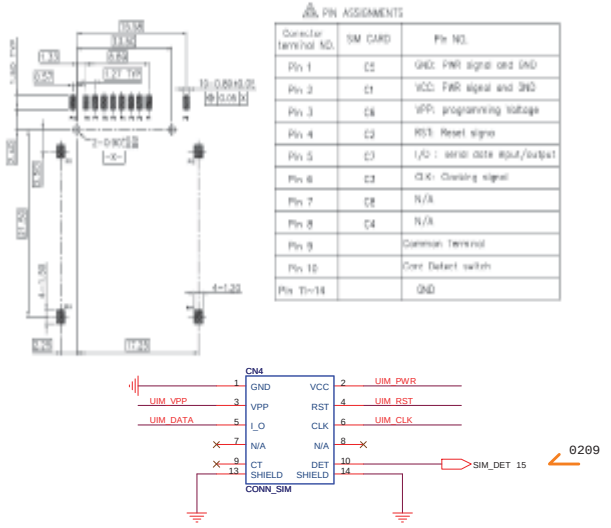


0223 Correct correction to BT.

Change PCI-E interface to SATA interface Mika 20090317

0211 Change footprint

SIM SOCKET



PROJECT :LL1
Quanta Computer Inc.

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C	<Doc> CONN (MINI PCI-E, SIM)	1A
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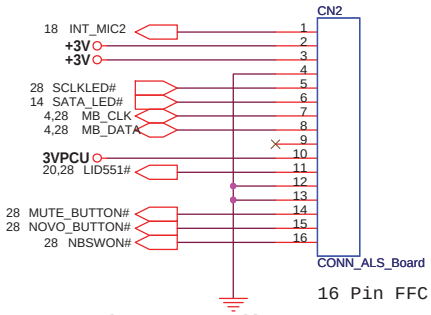
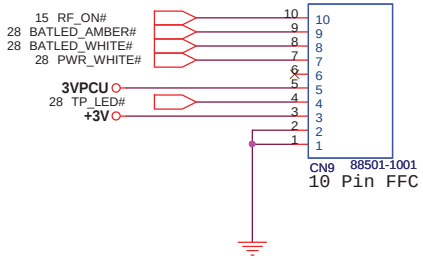
ALS/ Button Board



Change ALS smb to MB_CLK/MB_DATA Mika 20090421

Front LED indicator Board



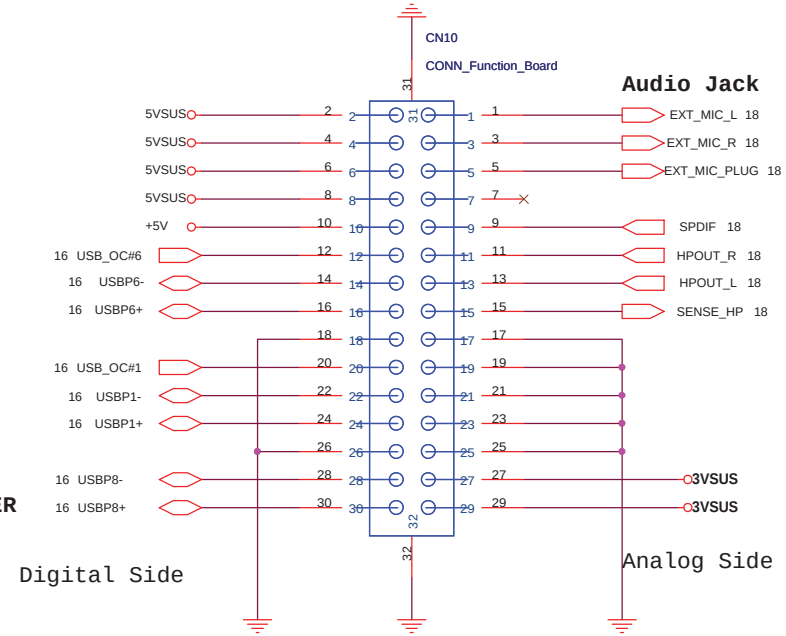
Change Front LED CONN to 10P Mika 20090306

Function Board

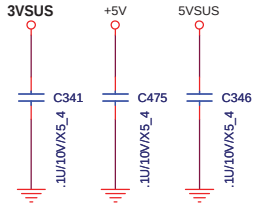
USB PORT

USB PORT

CARD READER



0217 EMI Add



PROJECT :LL1
Quanta Computer Inc.

Size	Document Number	Rev
B	<Doc> CONN (WIRE to BOARD, LED)	1A
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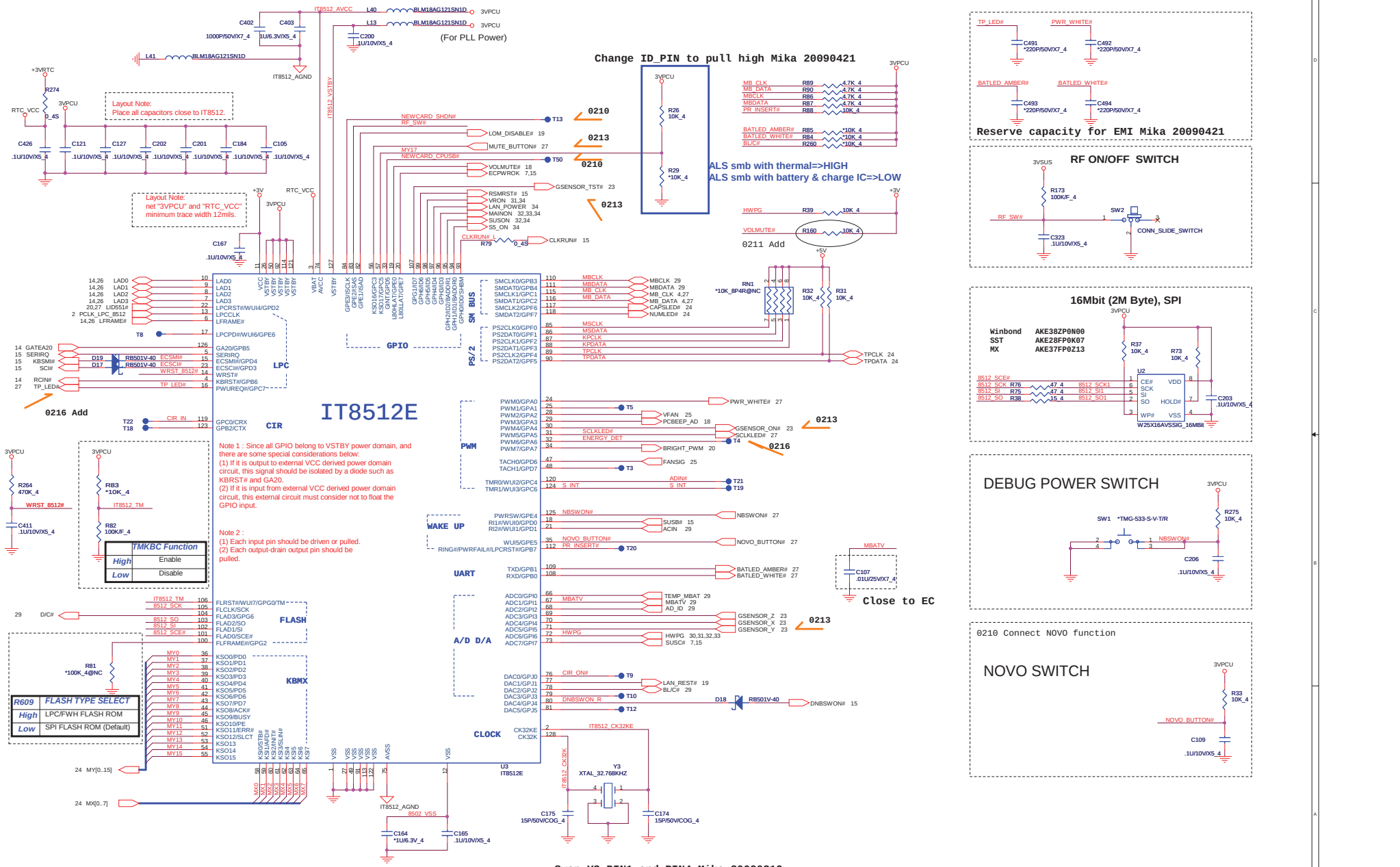

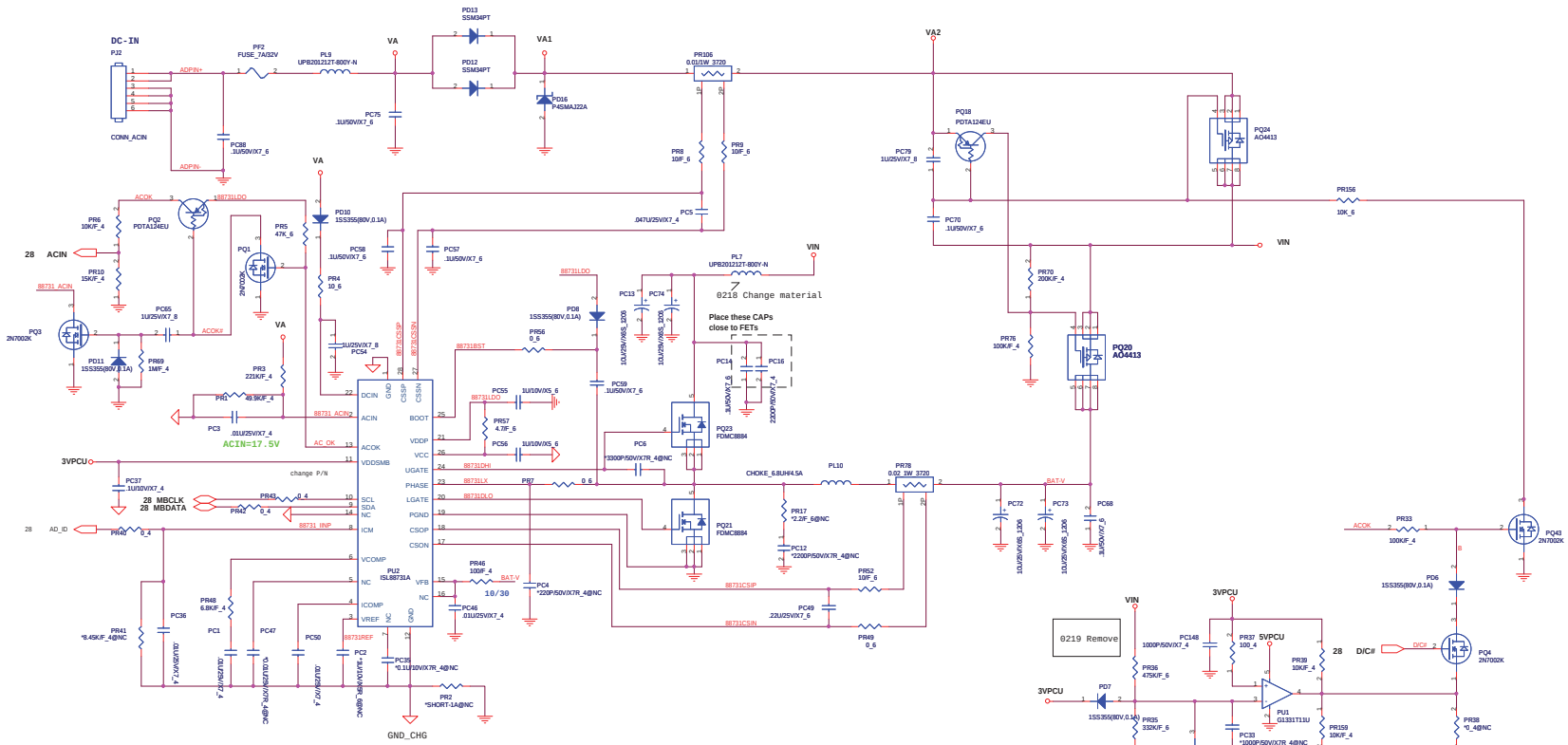

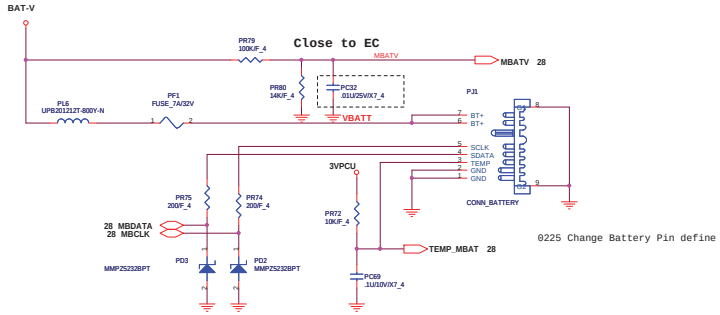

PROJECT :LL1
Quanta Computer Inc.
Size: Custom | Document Number: <Doc> POWER_Charger (ISL88731A) | Rev: 1A
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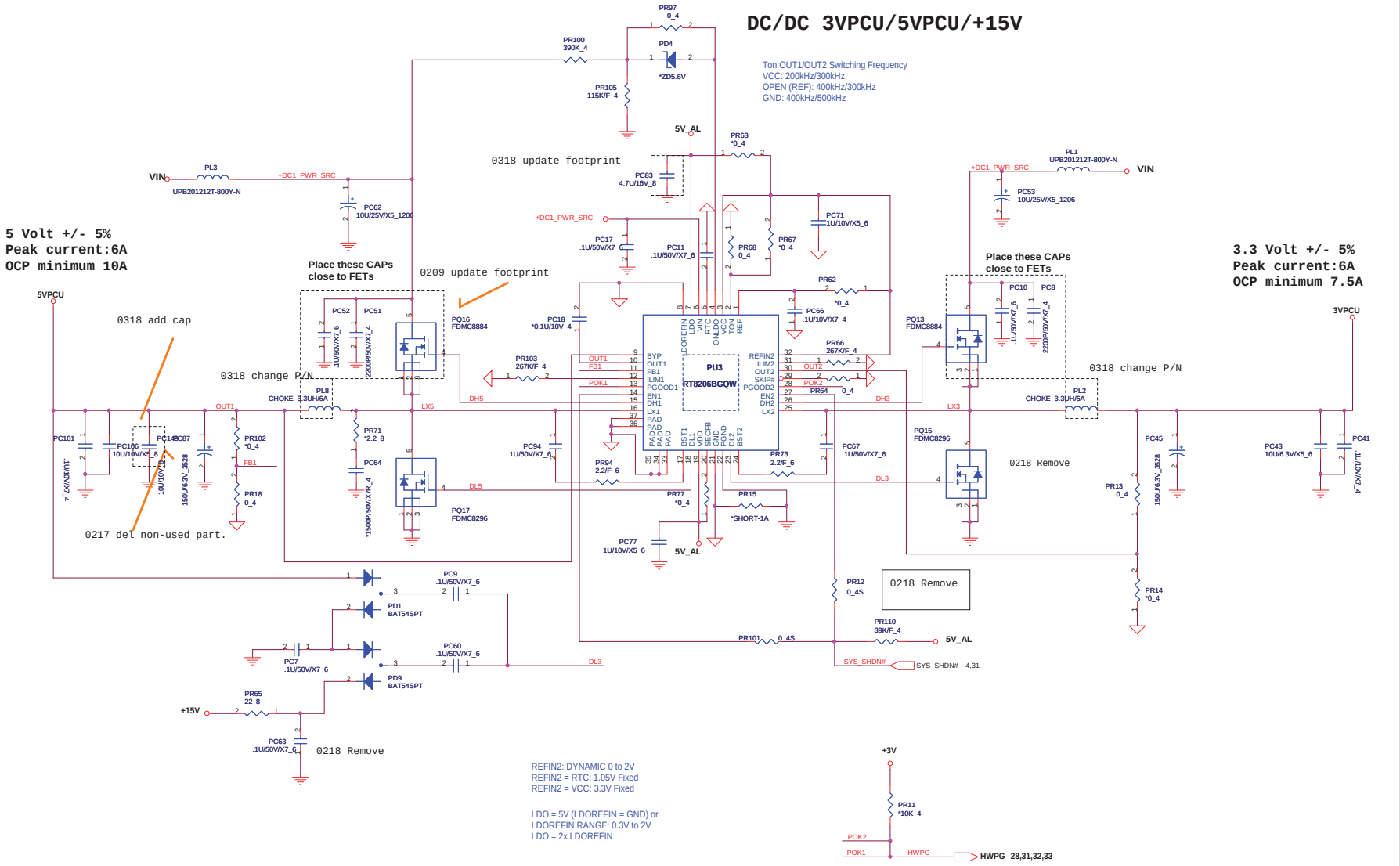
DC/DC 3VPCU/5VPCU/+15V



PROJECT :LL1 Quanta Computer Inc.		
Size: Custom	Document Number: <Doc> POWER_3V/5V (RT8206)	Rev: 1A
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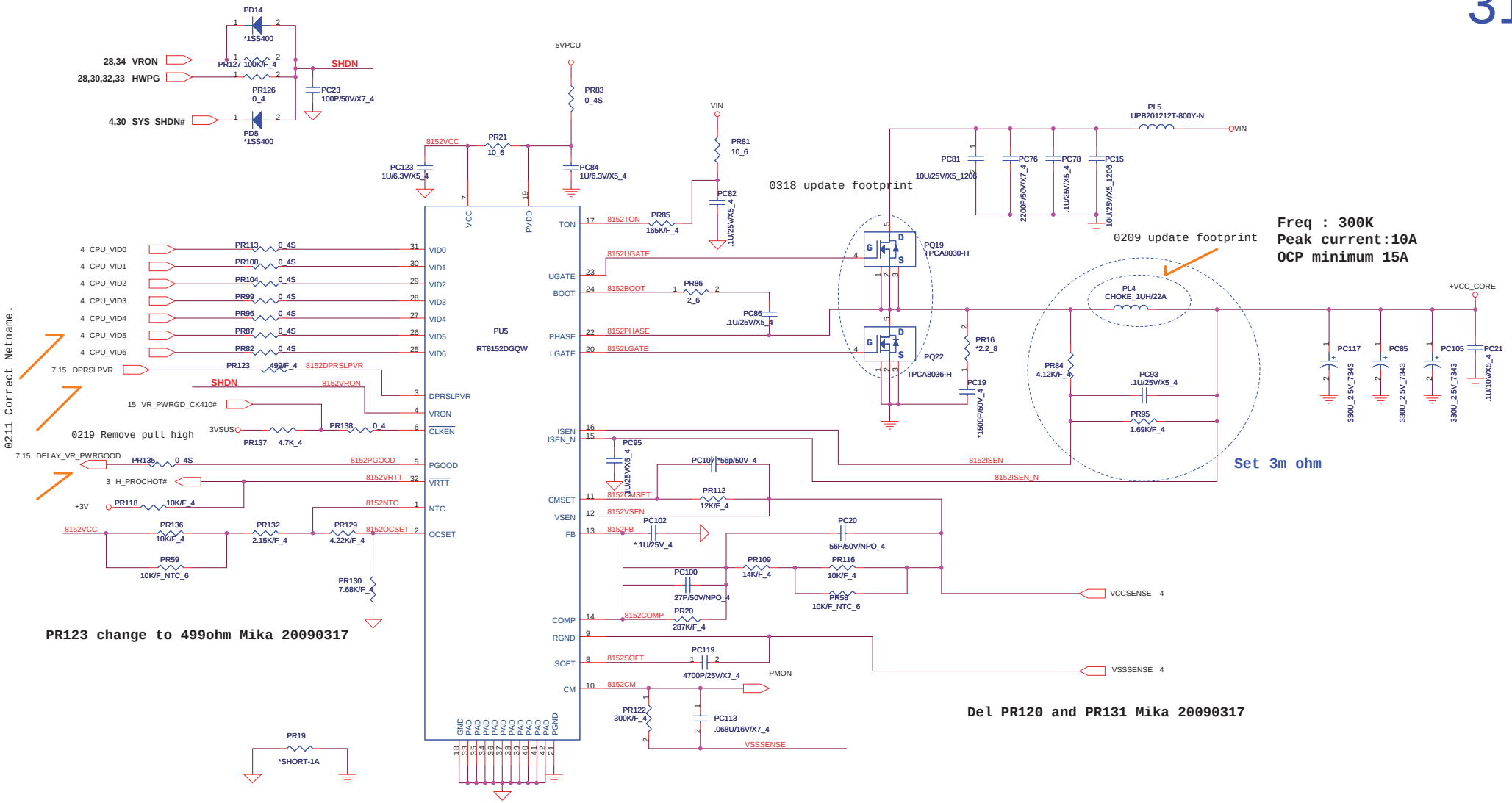

PROJECT : LL1			
Quanta Computer Inc.			
Size: Custom	Document Number: <Doc> POWER_CPU CORE (RT8152A)		Rev: 1A
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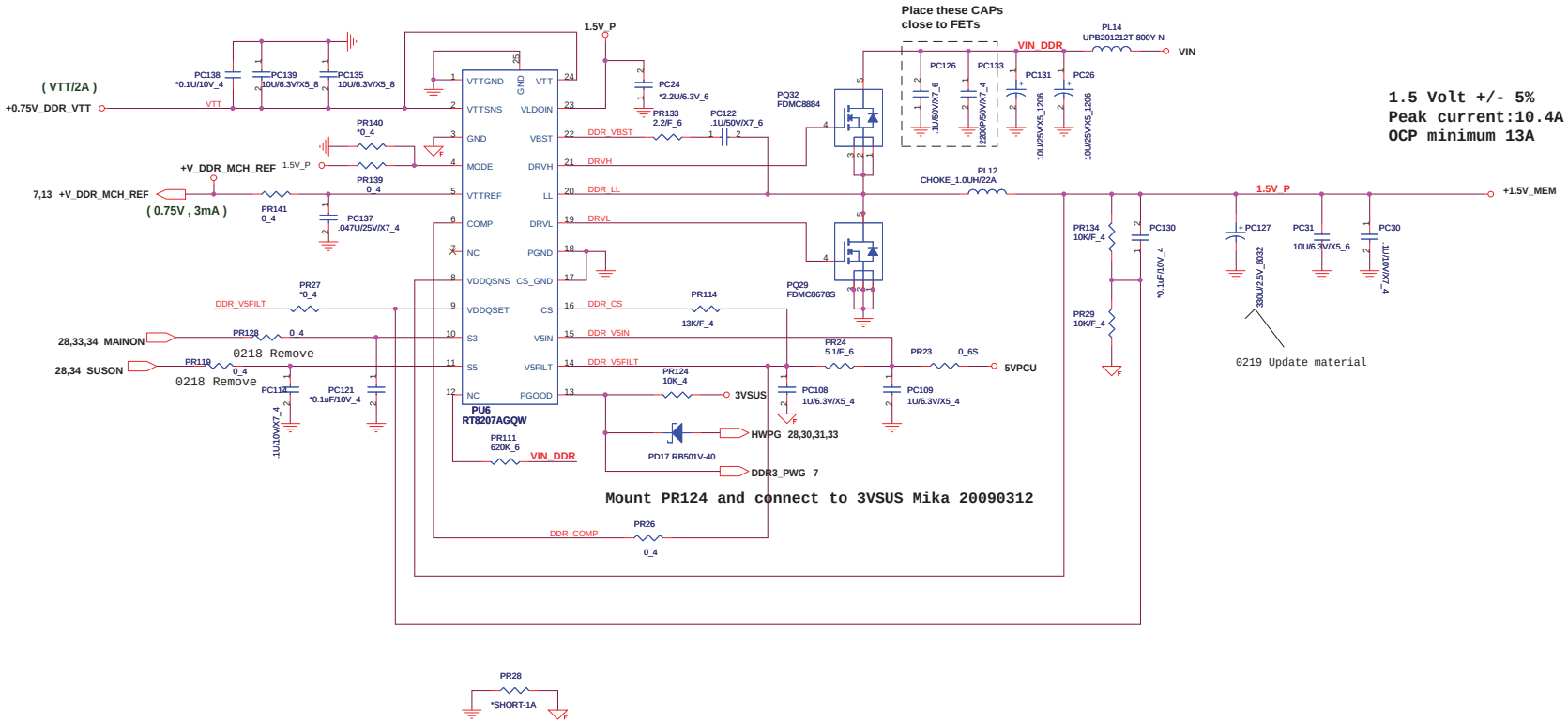

PROJECT :LL1 Quanta Computer Inc.			
Size: Custom	Document Number: <Doc> POWER_DDR3 (RT8207AGQW)		Rev: 1A
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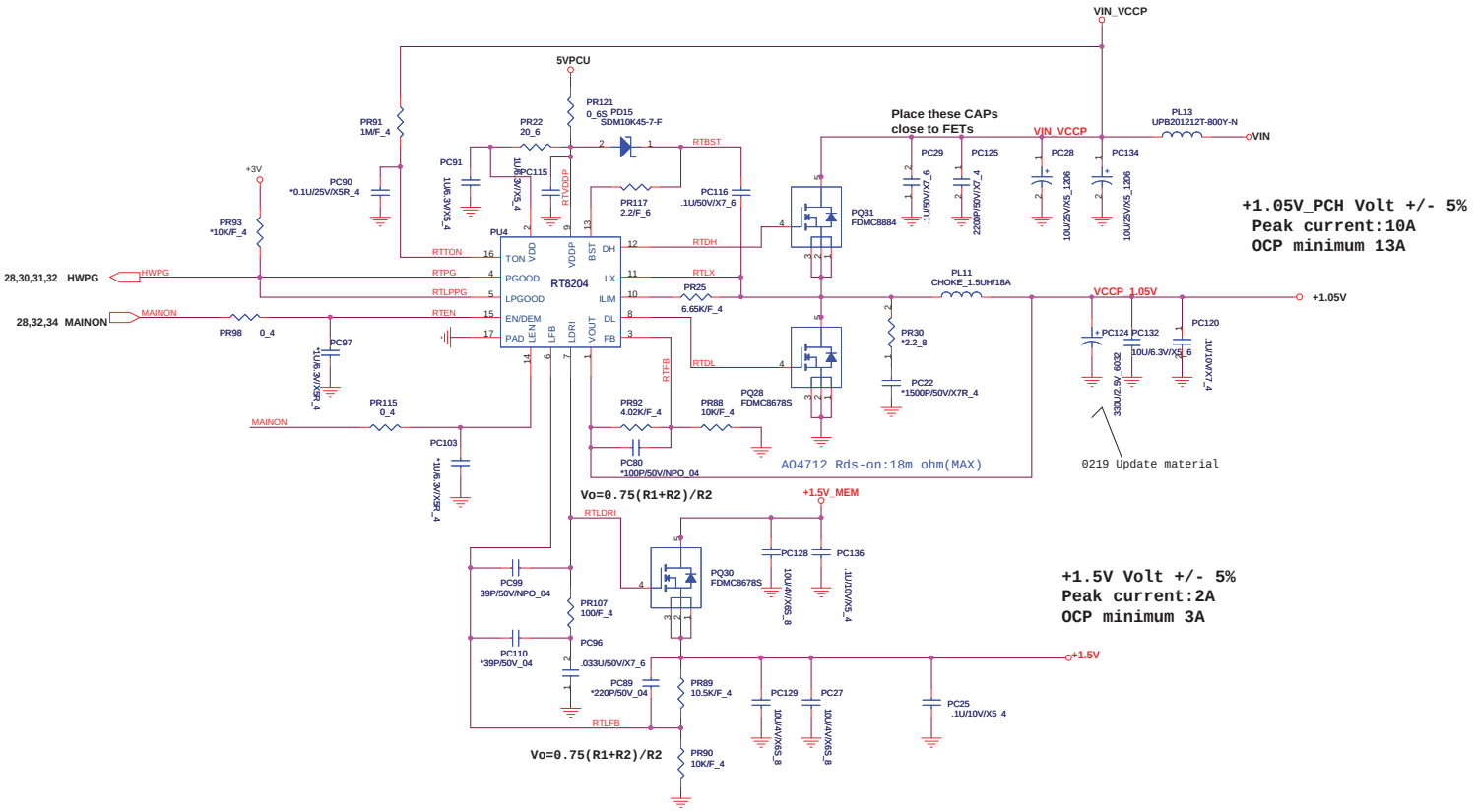

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Quanta Computer Inc.

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Custom	<Doc> POWER_1.05V/1.5V (RT8204)	1A
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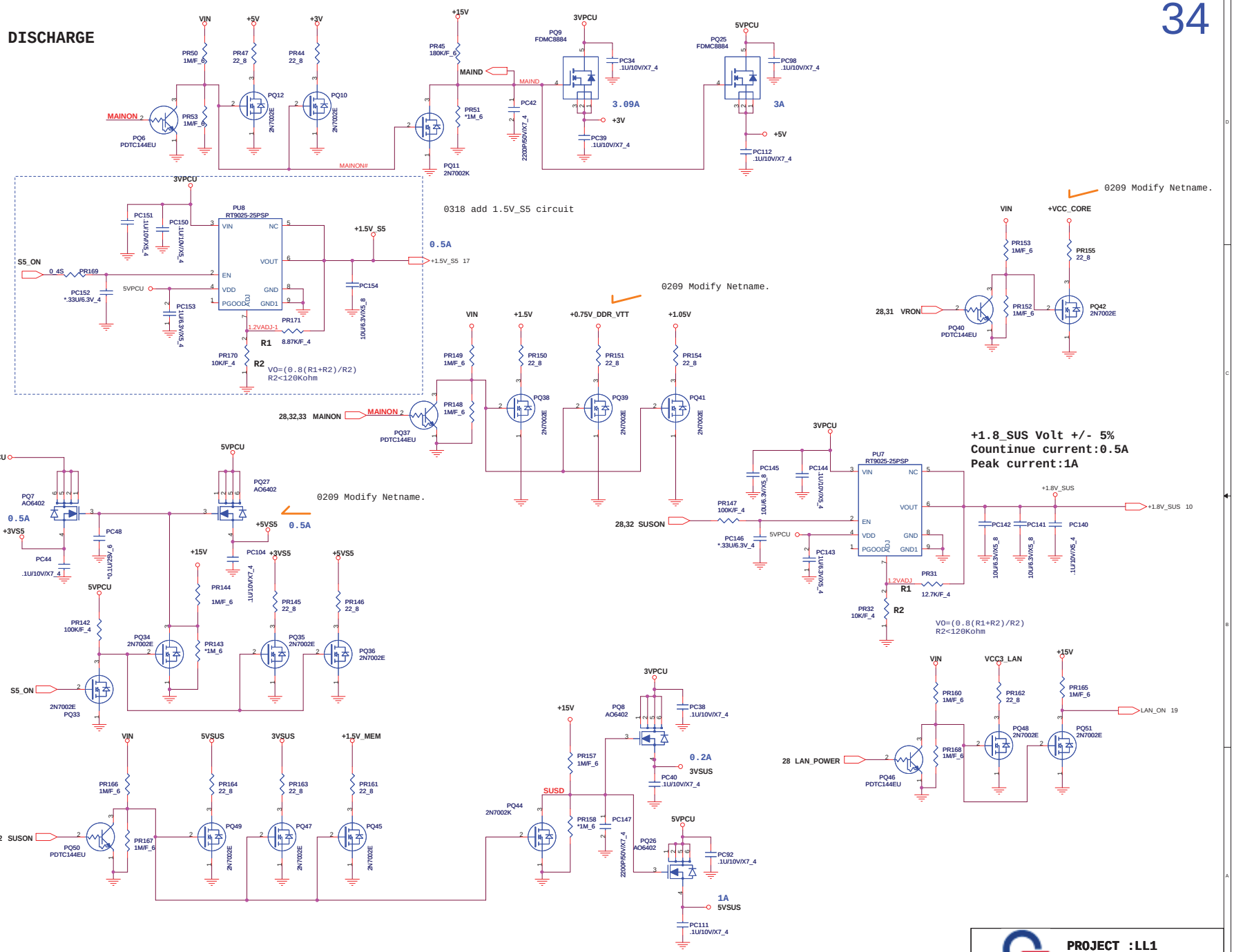
DISCHARGE



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Size: Custom	Document Number: <Doc> POWER_Discharge
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HOLE2
*h-c146d146n

HOLE7
*h-c146d146n

HOLE3
*h-c236d91p2

HOLE9
*h-c236d91p2

HOLE5
*h-c236d91p2

HOLE1
*h-c236d91p2

HOLE8
*h-c220d220n

HOLE11
h-c157d55p2

HOLE12
h-c157d55p2

WLAN NUT

PAD1
*ESD

PAD2
*ESD

PAD3
*ESD

HOLE10
*h-c78d78n

HOLE4
*h-c78d78n

HOLE13
h-c177d146p2

VGA NUT

HOLE14
h-c157d55p2

HOLE15
h-tc157bc75d55p2

WWAN NUT

Change Hole15 footprint Mika 20090316

PROJECT : LL1 Quanta Computer Inc.		
Size: B	Document Number: <Doc> HOLES, PAD, NUT	Rev: 1A
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02 -- Clock Generator
1) Disable ITP...0211
2) Connect VDD_IO to 1.05V...0216
3) Connect WLAN PCI-E to SRC10 contrlled by CR#_H...0218
4) Swap DREFFSSCLK pair to SRCCLK1 for spread spectrum...0220

03 -- Penryn (HOST BUS) 1/3
1) Del reserved ITP connector...0209
2) Disconnect ITP Clock...0209
3) Connect WLAN to SRC8, No clock request connect...0209
4) Add PROCHOT# level shift between 1.05V and +3V...0211

07 -- Cantiga_B (VGA,DMI)
1) Connect DDR3 CH.A (CKE1,ODT1,CS1,M_CLK_DDR1) signals...0209
2) Del SM_PWROK AND logic...0211
3) Del PM_EXTTS#1 connection due to no DDR thermal monitor...0211
4) Connect UMA HDA for HDMI support...0211
5) Correct TV DAC disable connection...0218

09 -- Cantiga_D (VCC,NCTF)
1) Mount VCC_AXG_SENSE, VSS_AXG_SENSE 10Ohm...0209

10 -- Cantiga_E (POWER)
1) Add CRT DAC power to enable CRT feature...0211
2) Add CRT Enable/ TV disable DAC power...0218

12 -- DDR3 (A) SO-DIMM RVS
1) Paste DDR3 socket module...0209
2) Update DDR3 conn. footprint...0211
3) Correct Dimm0 Address...0213

13 -- DDR3 (B) SO-DIMM STD
1) Del DDR thermal monitor...0209
2) Update DDR3 conn. footprint...0211

14 -- ICH9-M_A_(CPU,SATA,IDE)
1) Connect HDA to UMA for iHDMI support...0211
2) Correct SATA decoupling...0211

16 -- ICH9-M_B_(USB,PCIE,DMI)
1) Swap USB port for USB Host controller allocation...0219

17 -- ICH9-M_D_(POWER,GND)
1) Modfiy HDA BUS power plan to +1.5V(LC)...0213
2) Add decouping on VCCL_1_05 as Design Guide request...0224

18 -- AUDIO (CX20582, SPK)
1) Correct PCBEEP (EC) netname...0209
2) Update Conexant review result...0211
3) Move MIC conn. to daugter board due to ME concern...0212
4) Move Jack related components to daughter board...0213
5) Correct Mute function...0213
6) Modify MIC BIAS to net"AVDD_3.3V" (LC)...0213
7) Modify HDA BUs power to +1.5V(LC)...0213
8) Reserve PCBEEP Gain pull high for further experiment...0224.
9) Del MIC-IN decoupling Cap. and change Pull High to 2.2K...0224
10) Change MIC_IN VBIAS from Codec...0224.
11) Enlarge +5VA trace width...0226

19 -- LAN (BCM57780, RJ45)
1) Update Transformer footprint...0209
2) Update RJ45 footprint...0211
3) Reserve 0Ohm short in LANVCC (LC)...0213
4) Add 0Ohm short reserved for Energey_DET net(LC)...0213
5) Change LAN Chip to BCM57780...0216
6) Remove 1.6V single net...0216

20 -- CONN (LVDS, CCD)
1) Correct Backlight PWM netname from EC...0209
2) Update LCD conn. footprint...0212
3) Reserve LVDS +3V 0Ohm short for further experiment...0213
4) Reserve CAMERA VCC 0Ohm short for further experiment...0213
5) Reserve CCD USB port Common mode Choke...0217

21 -- CONN (HDMI, level Shift)
1) Add EMI reserved RP (0X2) in HDMI signals...0212
2) Update HDMI conn. footprint...0212
3) Add diode in +5V_HDMIC series(LC)...0213

22 -- CONN (CRT)
1) Update CRT conn. footprint...0211
2) Change ESD solution...0218

23 -- CONN (USB, BT, G sensor)
1) Update G-sensor footprint...0209
2) Change USB port bulk from 100U to 150U(LC)...0213
3) G-sensor follow HengshanII...0213
4) Del additioanl USB power Bulk and filter...0218
5) Correct BBCPEX1,2 connection...0223
6) Swap USB net for routing...0224

24 -- CONN (KB, TP)
1) Update TP connector footprint...0209
2) Swap TP pin definition...0212
3) Swap KB pin definitoin...0212
4) Swap Keyboard matrix for routing...0223

25 -- CONN (HDD,FAN)
1) Modify Fan connector and Pin define...0210
2) Update HDD conn. footprint...0211
3) Reserve HDD 3V/5V short jump for further EMI/power consumption check(LC)...0213
4) Change FAN conn. to right angle...0217

26 -- CONN (MINI PCI-E, SIM)
1) Connect SIM socket Detect...0209
2) Modify Mini Card LED indicator connection...0209
3) Modify WWAN 470u bulk reserved to 10u...0211
4) Connect WLAN OE#...0218
5) Correct BBCPEX1,2 connection...0223
6) EMI add 1000P filter in 3VSUS trace...0224
7) Remove +3V to +3.3VAUX connection, reserve only 3VSUS...0225

27 -- CONN (WIRE to BOARD, LED)
1) Connect USB/Audio/CR function connector...0210
2) Connect ALS/ Button connector...0210
3) Connect Front LED indicator connector...0210
4) Connecet MIC on ALS board...0212
5) Update 30Pin Wire to Board conn. footprint...0212
6) EMI add reserved filter for power trace...0217

28 -- EC (ITE8502E)
1) Connect NOVO function...0210
2) NC un-used GPIO as test points...0210
3) Connect G-sensor signals...0213
4) Connect TP_LED#...0216
5) Disconnect ENERGY_DET...0216

PROJECT : LL1
Quanta Computer Inc.

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C	<Doc> Pre A to A-test change list	1A

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07 -- Cantiga_B (VGA,DMI)
1) TV_DCONSEL_0/1 connect to GND ...0312
2) Connect DDR3_PWG to NB ...0312
3) Add R372 in ACZ_SDIN1 ...0317
4) Add U22 and C486 for DDR3_PWG ...0318

14 -- ICH9-M_A_(CPU,SATA,IDE)
1) Support PCI-E Type SSD ...0317
2) PCI-E Type SSD change to SATA1 ...0320

15 -- ICH9-M_C_(PM,GPIO,SMB)
1) Swap SIM_DET & CLK_SATA_OE# ...0312
2) Connect SIM_DET to GPIO49 ...0317
3) Connect SIM_DET to GPIO1 ...0319

16 -- ICH9-M_B_(USB,PCIE,DMI)
1) Del PCI-E interface (WWAN use USB type) ...0317
2) Change WLAN to PCI-E-2 ...0318

18 -- AUDIO (CX20582, SPK)
1) Del R94,R163 to short AGND and GND directly ...0316
2) Add C480 and C481 ...0316
3) Change R344 to 1206 size ...0316
4) Change C235 to 0.1U ...0316
5) Change R166~R169 to 0603 size ...0316
6) Del R156 and Q8 then short Volmute# directly ...0318
7) Change PC_BEEP voltage level to 1/10 ...0319
8)Change R166~R169 from 0ohm to BK1608HS601 ...0320

19 -- LAN (BCM57780, RJ45)
1) Change LAN CONN footprint ...0305
2) Connect LOM_DISABLE# to EC ...0310
3) Swap U9 pin5 pin6 ...0312

21 -- CONN (HDMI, level Shift)
1) Remove RP4~RP6 and add R373~R375 ...0320
2) Change RP3 from 0ohm to WCM-2012-900T ...0320

22 -- CONN (CRT)
1) Swap CN5 Pin1,2,3,4,5 & Pin11,12,13,14,15 ...0312
2) Change CN5 footprint ...0318

23 -- CONN (USB, BT, G sensor)
1) Change USB CONN footprint ...0305
1) Change USB CONN footprint ...0318

24 -- CONN (KB, TP)
1) Swap CN7 pin definition ...0305
2) Change TP conn to 4P ...0305
3) Swap KB bypass capacity and resistor ...0306
4) Swap TP CONN ...0312

26 -- CONN (MINI PCI-E, SIM)
1) Change PCI-E interface to SATA interface ...0317
2) R222 and R341 Connect to +3V ...0318

27 -- CONN (WIRE to BOARD, LED)
1) Change Front LED CONN to 10P ...0306

28 -- EC (ITE8502E)
1) Swap Y3 PIN1 and PIN4 ...0319

31 -- POWER_CPU CORE (RT8152B)
1) PR123 change to 499ohm ...0317
2) Del PR120 and PR131 ...0317

32 -- POWER_DDR3 (RT8207AGQW)
1) Mount PR124 and connect to 3VSUS ...0312

35 -- HOLES, PAD, NUT
1) Change Hole15 footprint ...0316

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14 -- ICH9-M_A_(CPU,SATA,IDE)
   1) Add charge schematic for RTC ...0421

18 -- AUDIO (CX20582, SPK)
   1) Change PC_BEEP voltage level to 2/3 ...0421
   2) By vendor suggestion "D22 and D23 close to codec" ...0421

21 -- CONN (HDMI, level Shift)
   1) Reserve RP11~RP13 for EMI request ...0422

23 -- CONN (USB, BT, G sensor)
   1) Increase Z-axis signal ...0415

24 -- CONN (KB, TP)
   1) Reserve Varistor for ESD ...0422

27 -- CONN (WIRE to BOARD, LED)
   1) Change ALS smb to MB_CLK/MB_DATA ...0421

28 -- EC (ITE8502E)
   1) Change ID_PIN to pull high ...0421
   2) Reserve capacity on LED signal for EMI ...0421

change 0 Ohm to short footprint:

P02: (1) Short connect R99.

P10: (1) Short connect R45, R57

P20: (1) Short connect R3, R4

P21: (1) Short connect L2, L3, L38

P22: (1) Short connect R210, R224

P23: (1) Short connect R111, R281, R283

P28: (1) Short connect R79, R274

P30: (1) Short connect PR12, PR101

P31: (1) Short connect PR82, PR83, PR87, PR96, PR99 PR104, PR108, PR113, PR135

P32: (1) Short connect PR23

P33: (1) Short connect PR121

P34: (1) Short connect PR169

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