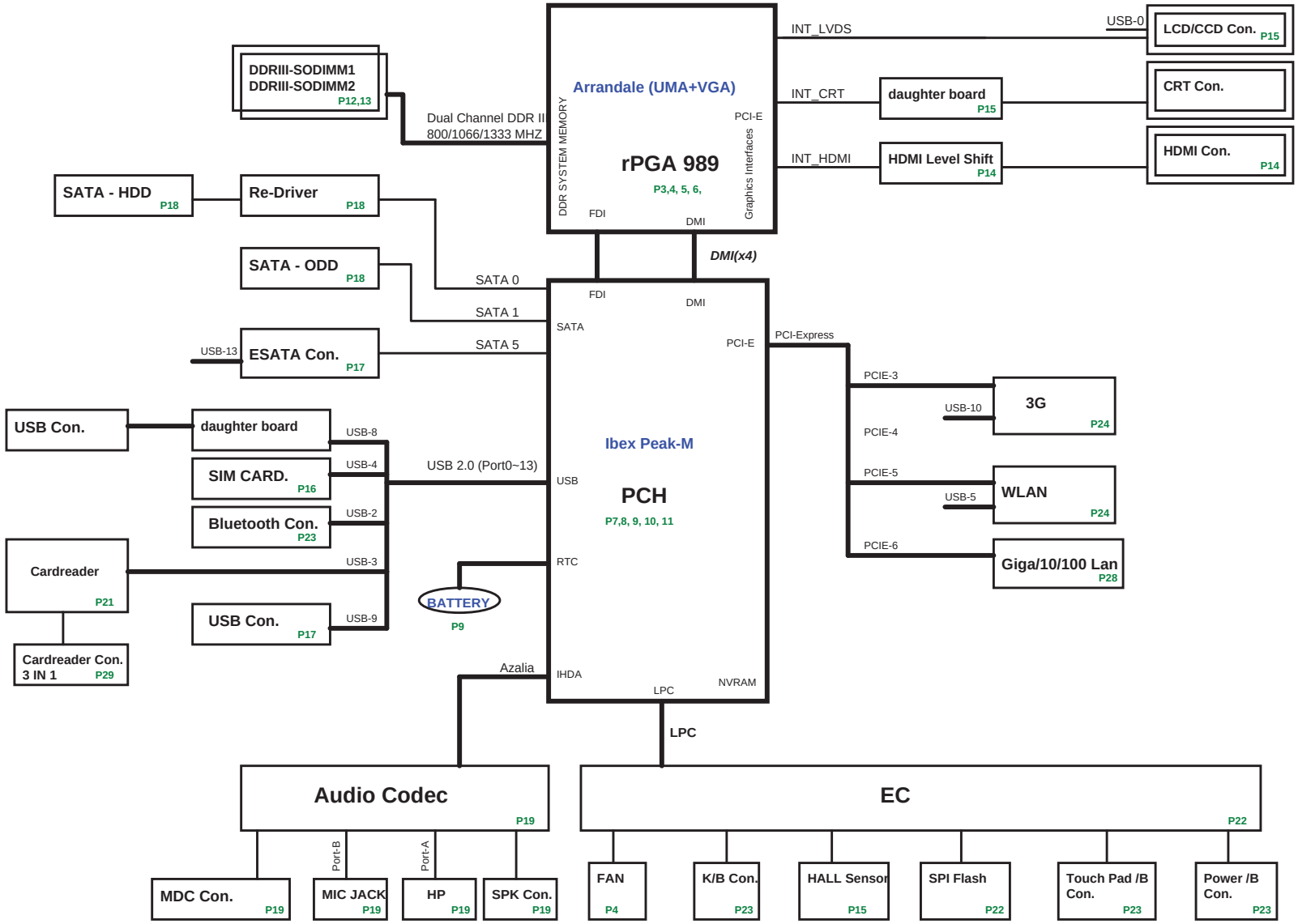
TE2 Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



CK505 P2

POWER SYSTEM

ISL88731A	P25
RT8210B	P26
UP6163	P27
UP6111A	P28
RT015A	P29
ISL62882C	P30
RT8152C	P32

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+1.5V_S5

+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

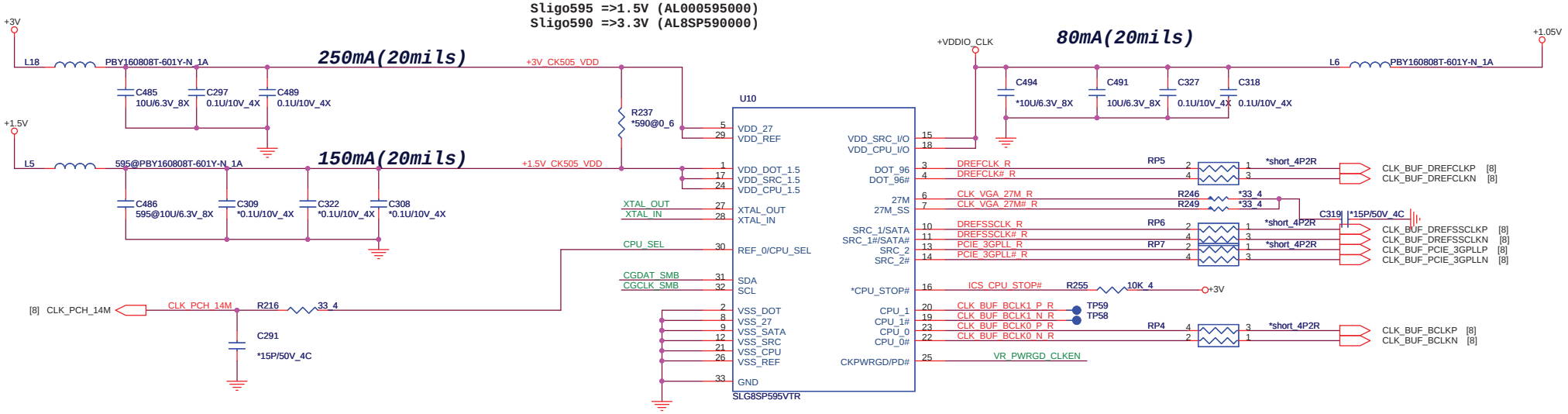
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Block Diagram	2A

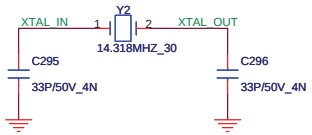
Date: Wednesday, March 10, 2010 Sheet 1 of 35

CLOCK Gen [CLK]

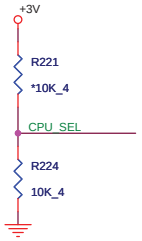
Pin1/17/24
Sligo595 =>1.5V (AL000595000)
Sligo590 =>3.3V (AL8SP590000)



CLK CRYSTAL

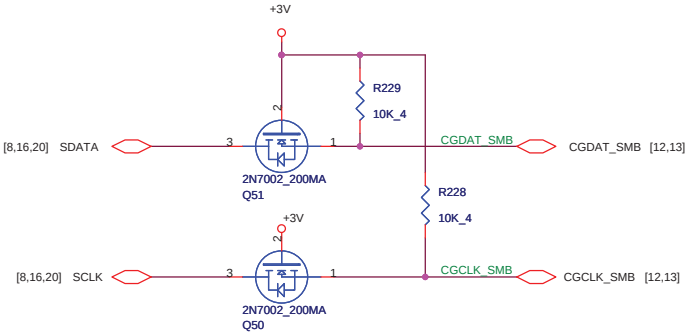


CLK CPU_SEL



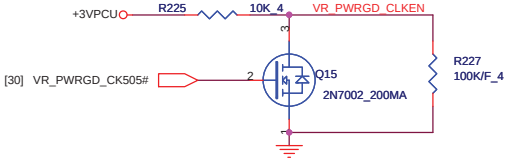
	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD

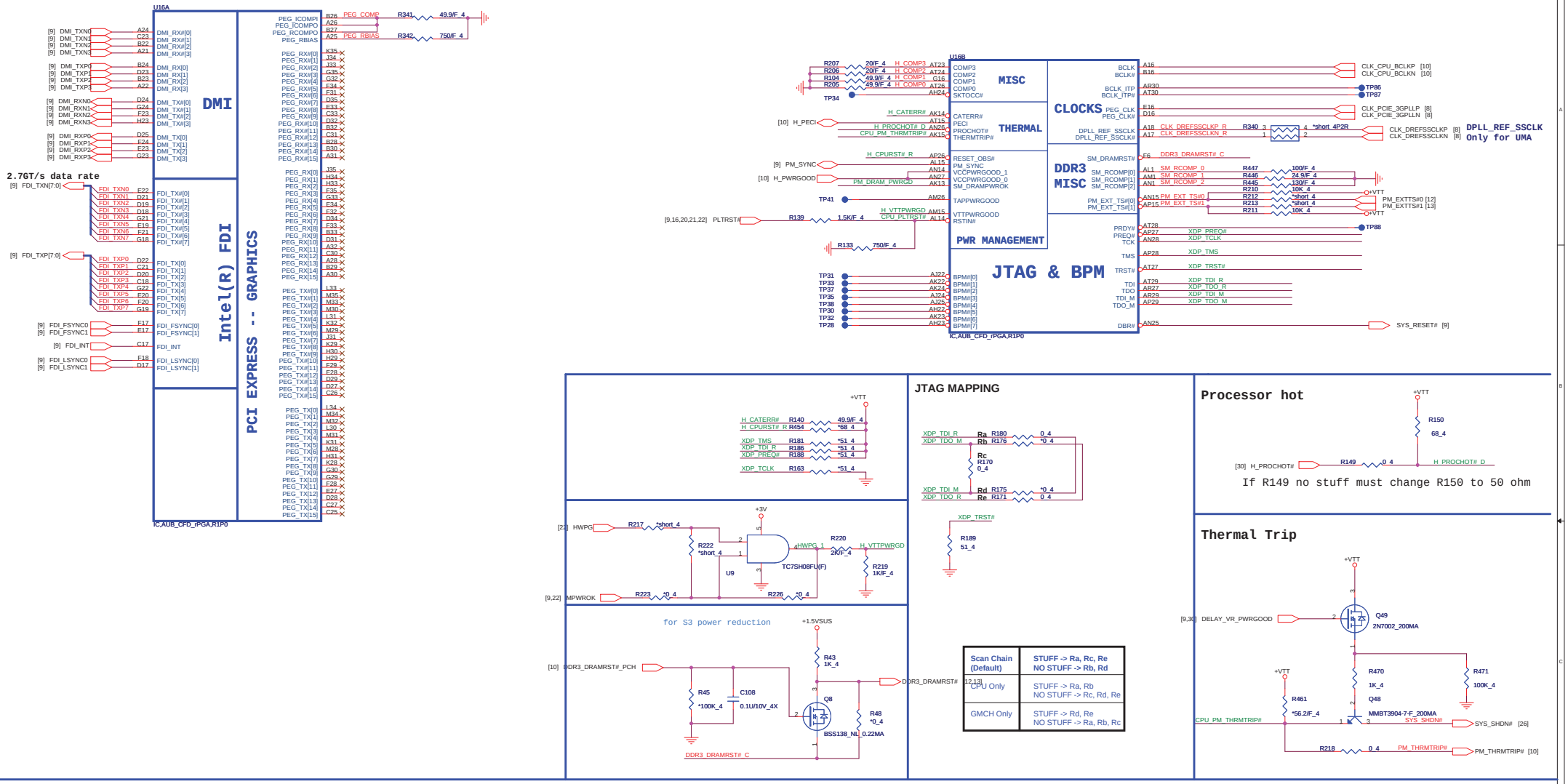
Change to +3VPCU
(follow CRB)



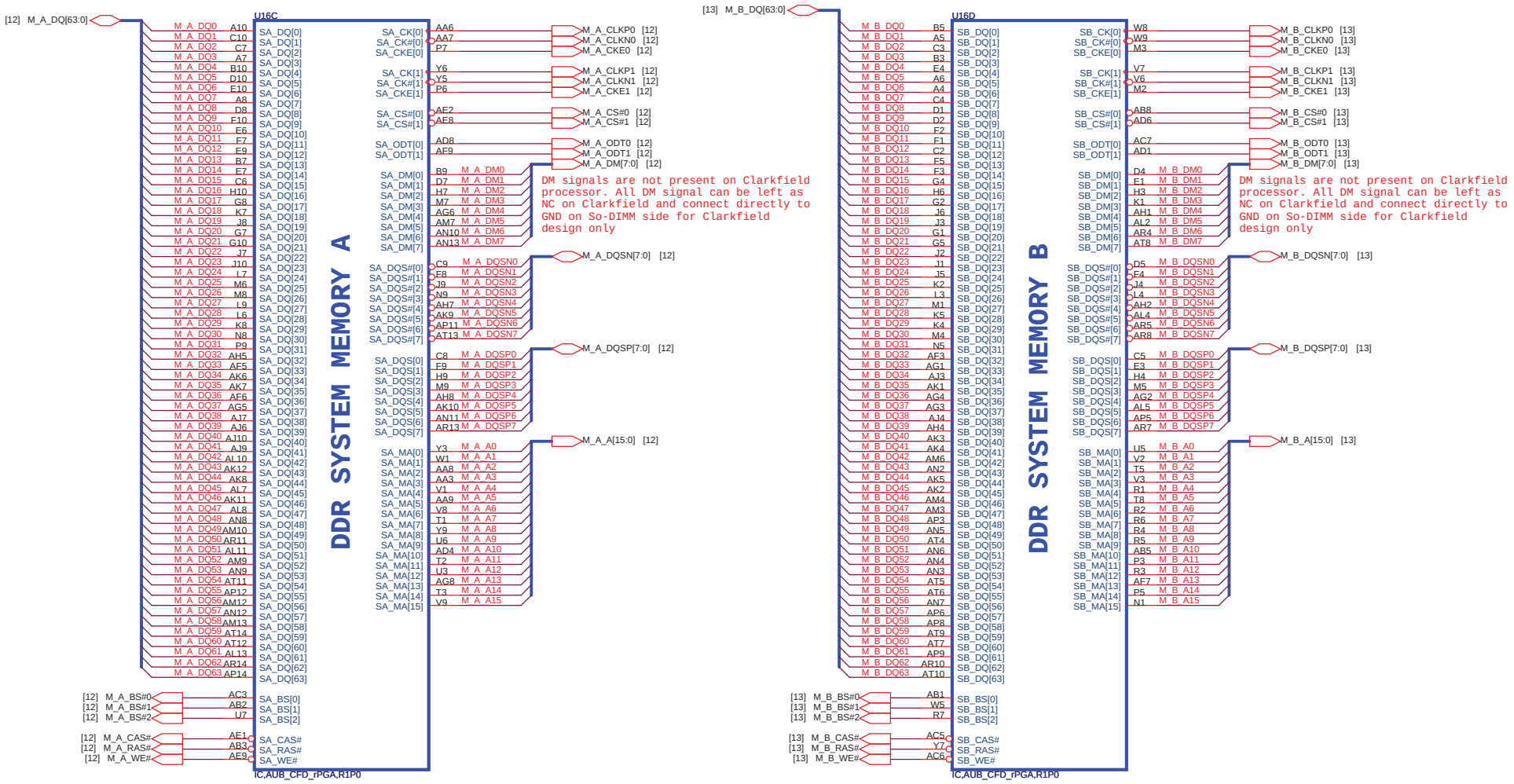
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	CLOCK GENERATOR	2A

Date: Friday, March 19, 2010 Sheet 2 of 35


U16A
DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
2.7GT/s data rate
IC,AUB_CFD_rPGA,R1P0
U16B
MISC
THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
IC,AUB_CFD_rPGA,R1P0
DPLL_REF_SSCLK
Only for UMA
JTAG MAPPING
Scan Chain (Default)
STUFF -> Ra, Rc, Re
NO STUFF -> Rb, Rd
CPU Only
STUFF -> Ra, Rb
NO STUFF -> Rc, Rd, Re
GMCH Only
STUFF -> Rd, Re
NO STUFF -> Ra, Rb, Rc
Processor hot
If R149 no stuff must change R150 to 50 ohm
Thermal Trip
for S3 power reduction
CPU FAN CTRL
3mA(40mils)
40mils
PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable
Quanta Computer Inc.
PROJECT :TE2
PROCESSER 1/4(HOST&PEX)
Size
Document Number
Rev 2A
Date: Tuesday, March 09, 2010
Sheet 3 of 35

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

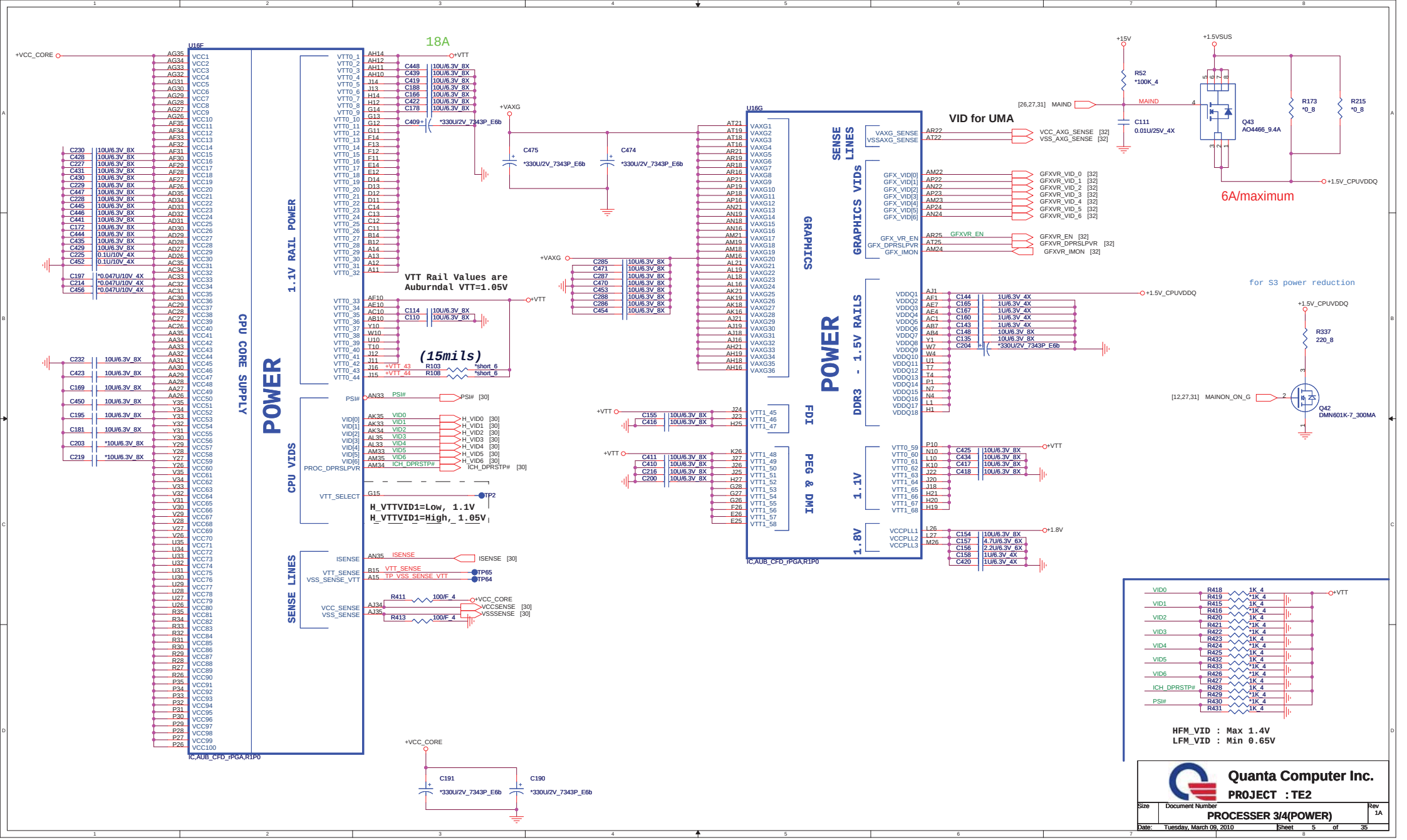


Quanta Computer Inc.

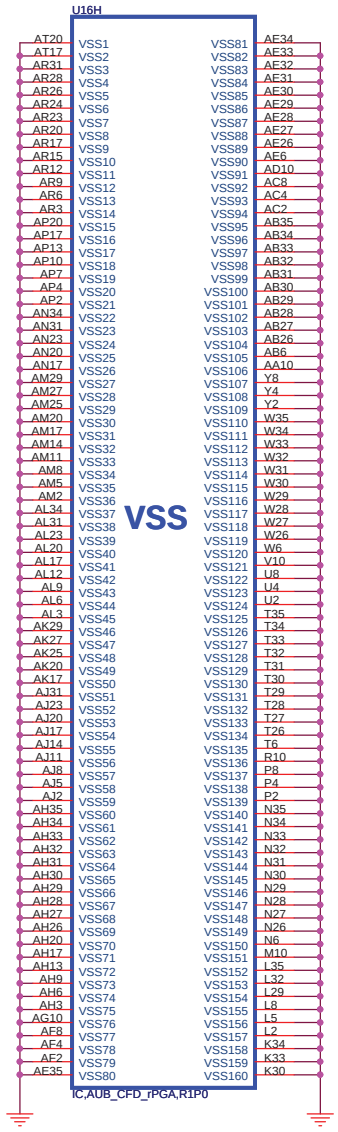
PROJECT : TE2

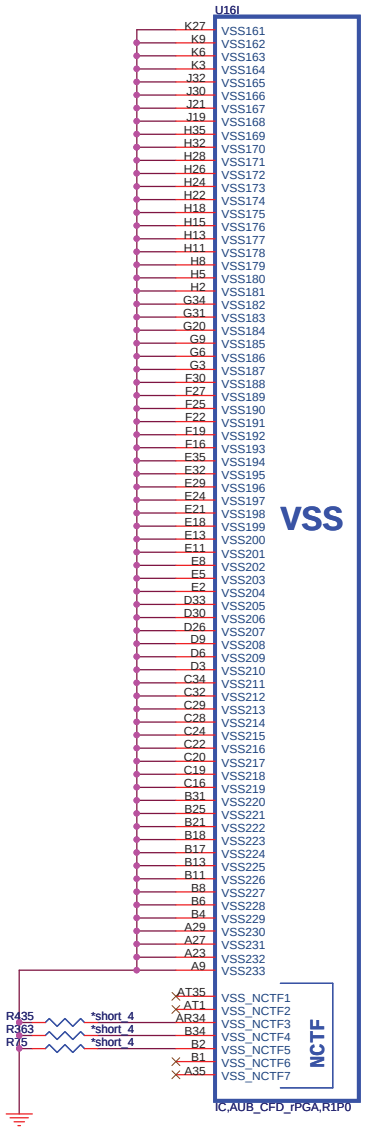
Size	Document Number	Rev
	PROCESSER 2/4(DDR)	2A

Date: Friday, February 26, 2010 Sheet 4 of 35

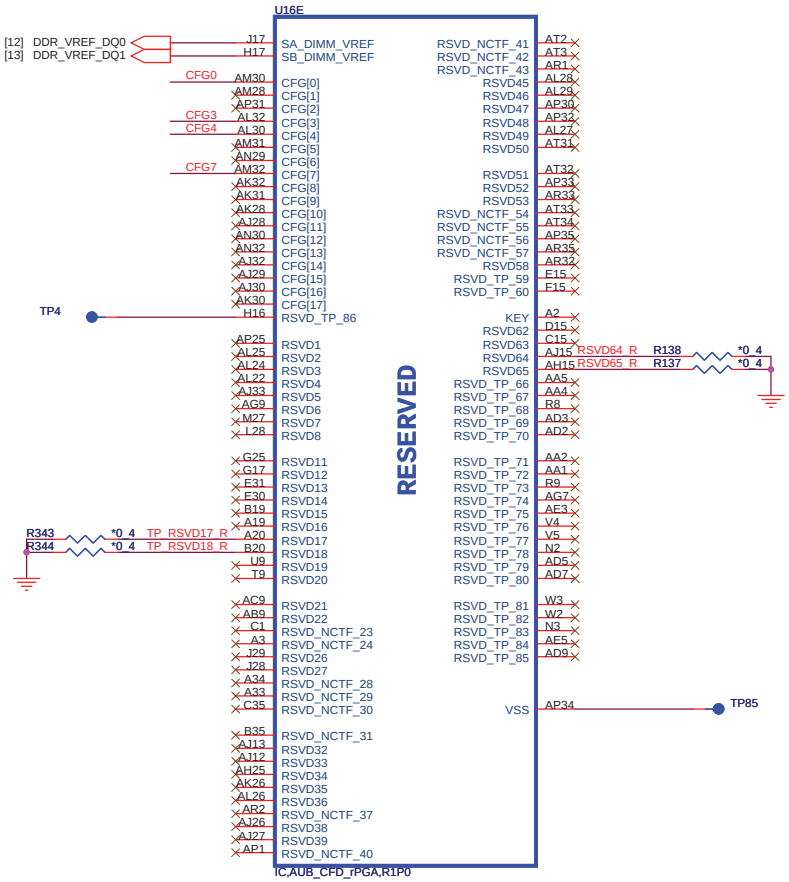

18A
U16F
U16G
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
GRAPHICS
GRAPHICS VIDs
DDR3 - 1.5V RAILS
FDI & PEG DMI
1.1V
1.8V
VID for UMA
VTT Rail Values are Auburndal VTT=1.05V
(15mils)
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
IC,AUB_CFD_rPGA,R1P0
6A/maximum
for S3 power reduction
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
Quanta Computer Inc.
PROJECT : TE2
PROCESSER 3/4(POWER)
Size
Document Number
Rev
1A
Date: Tuesday, March 09, 2010
Sheet 5 of 35

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)





AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only

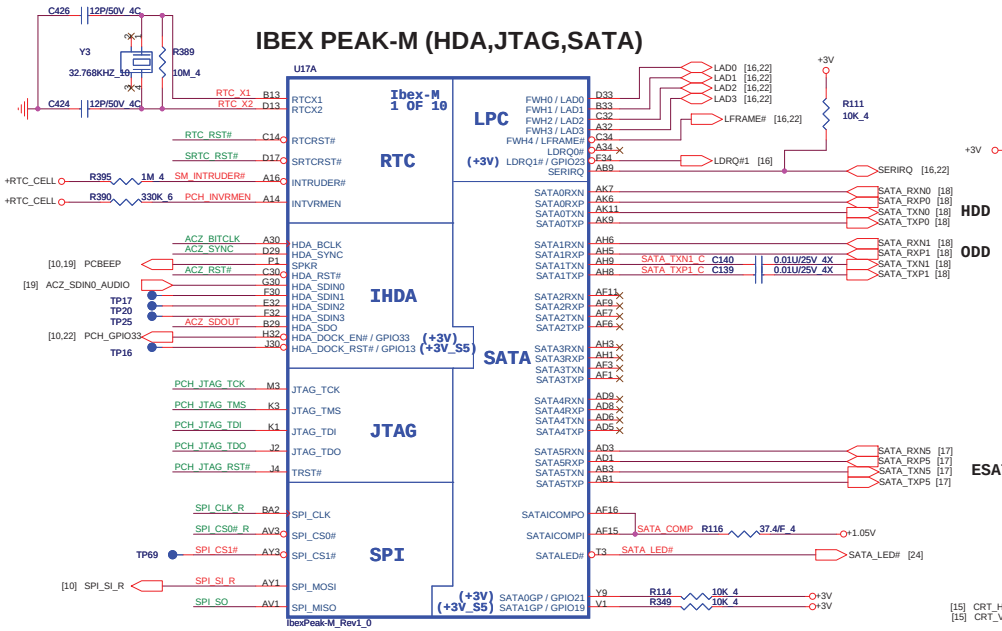
CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

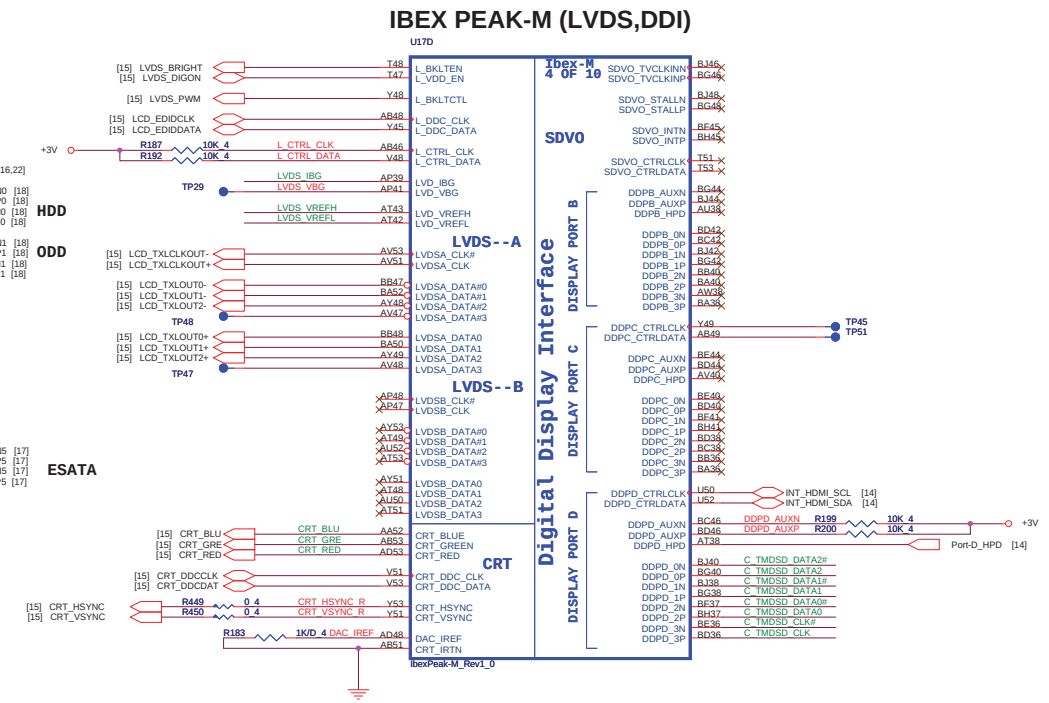
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	2A
Date: Tuesday, March 09, 2010	Sheet 6 of 35	

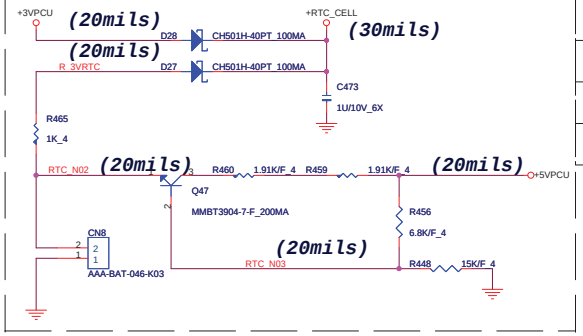
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs





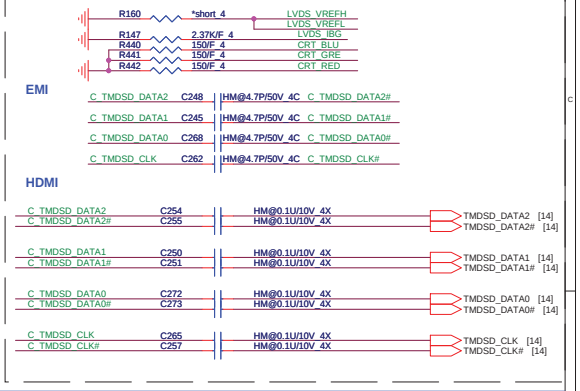
[RTC]

RTC BATTERY

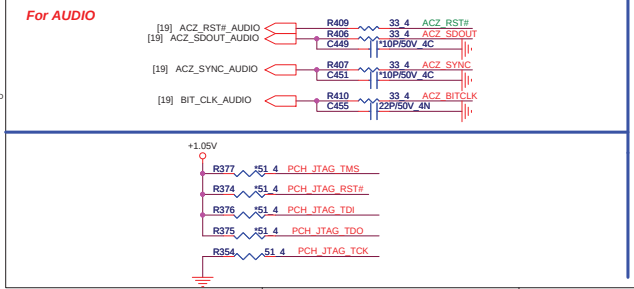


Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

[UMA]

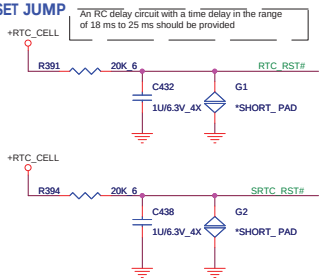


For AUDIO

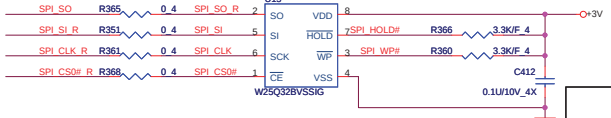


RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided



4M byte SPI ROM



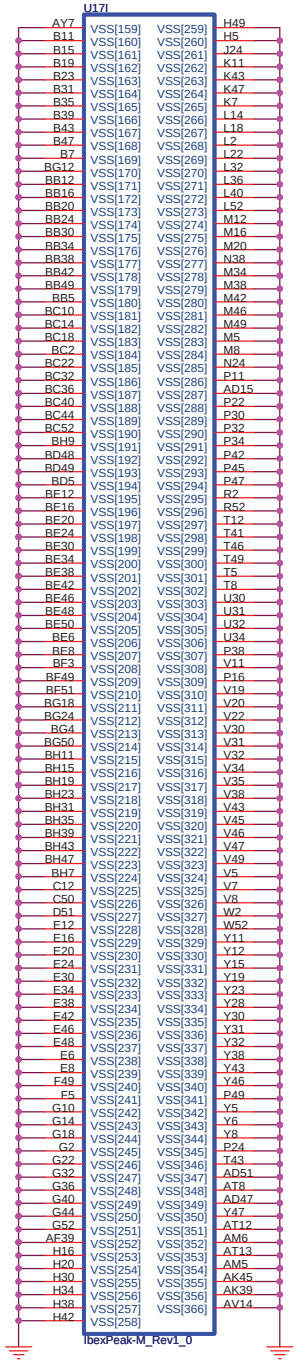
PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

Quanta Computer Inc.
PROJECT : TE2

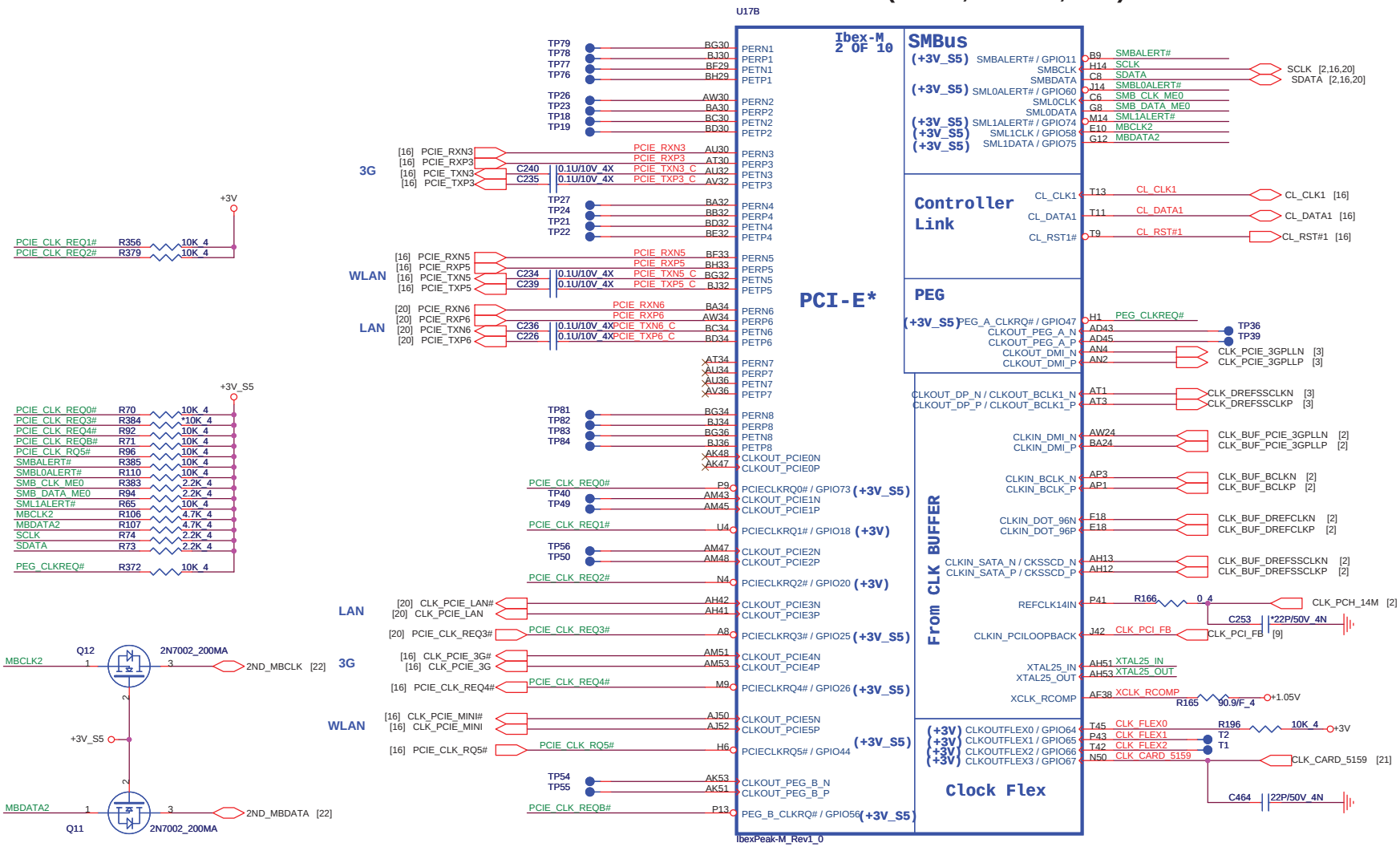
Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	2A

Date: Wednesday, March 10, 2010 Sheet 7 of 35

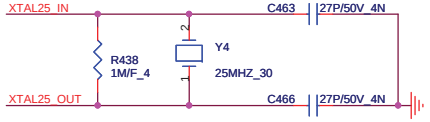
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)

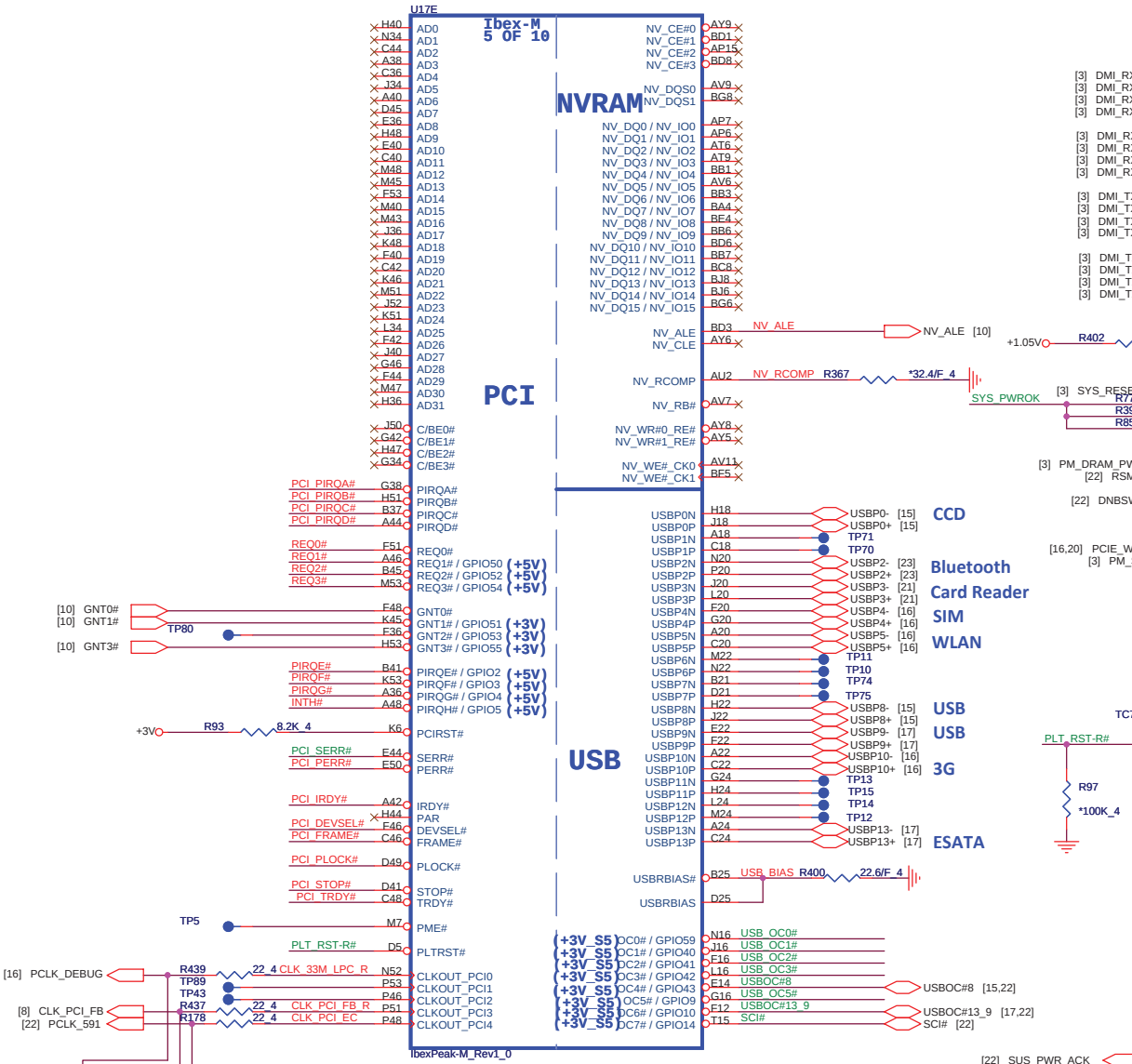


Placement close

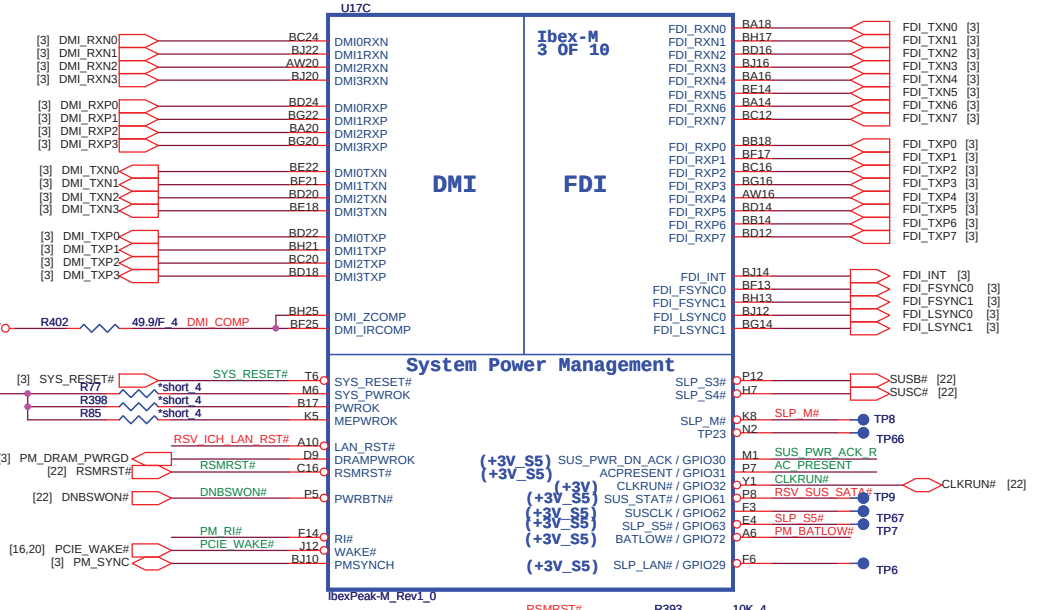


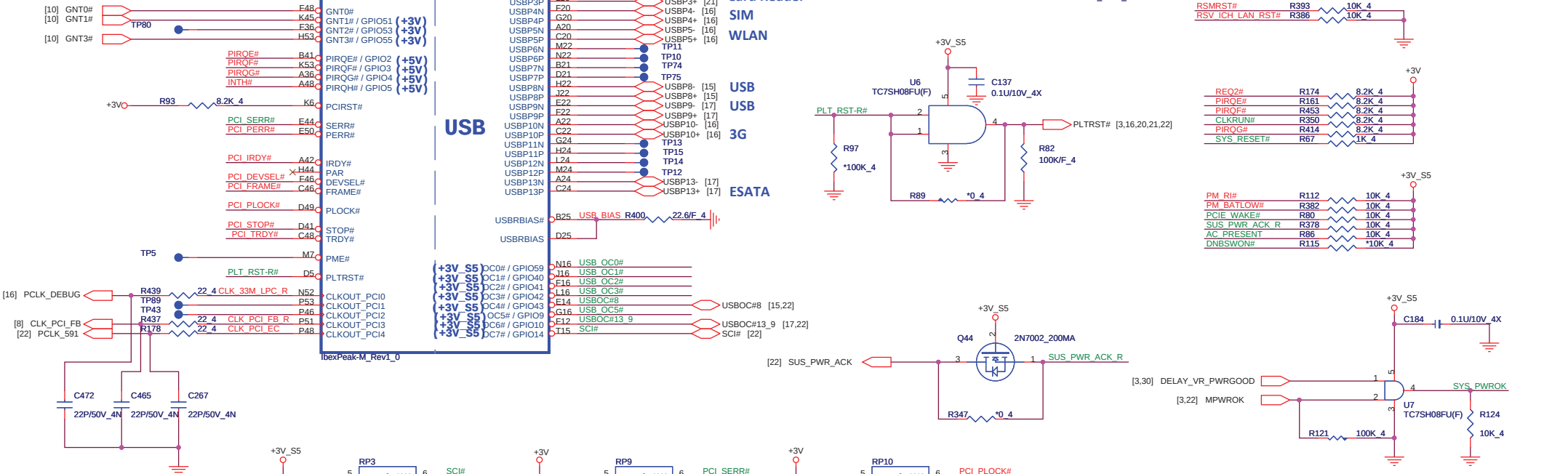
Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: PCH 2/5 (PCIE, SMBUS, CK)	Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 8 of 35	

IBEX PEAK-M (PCI,USB,NVRAM)



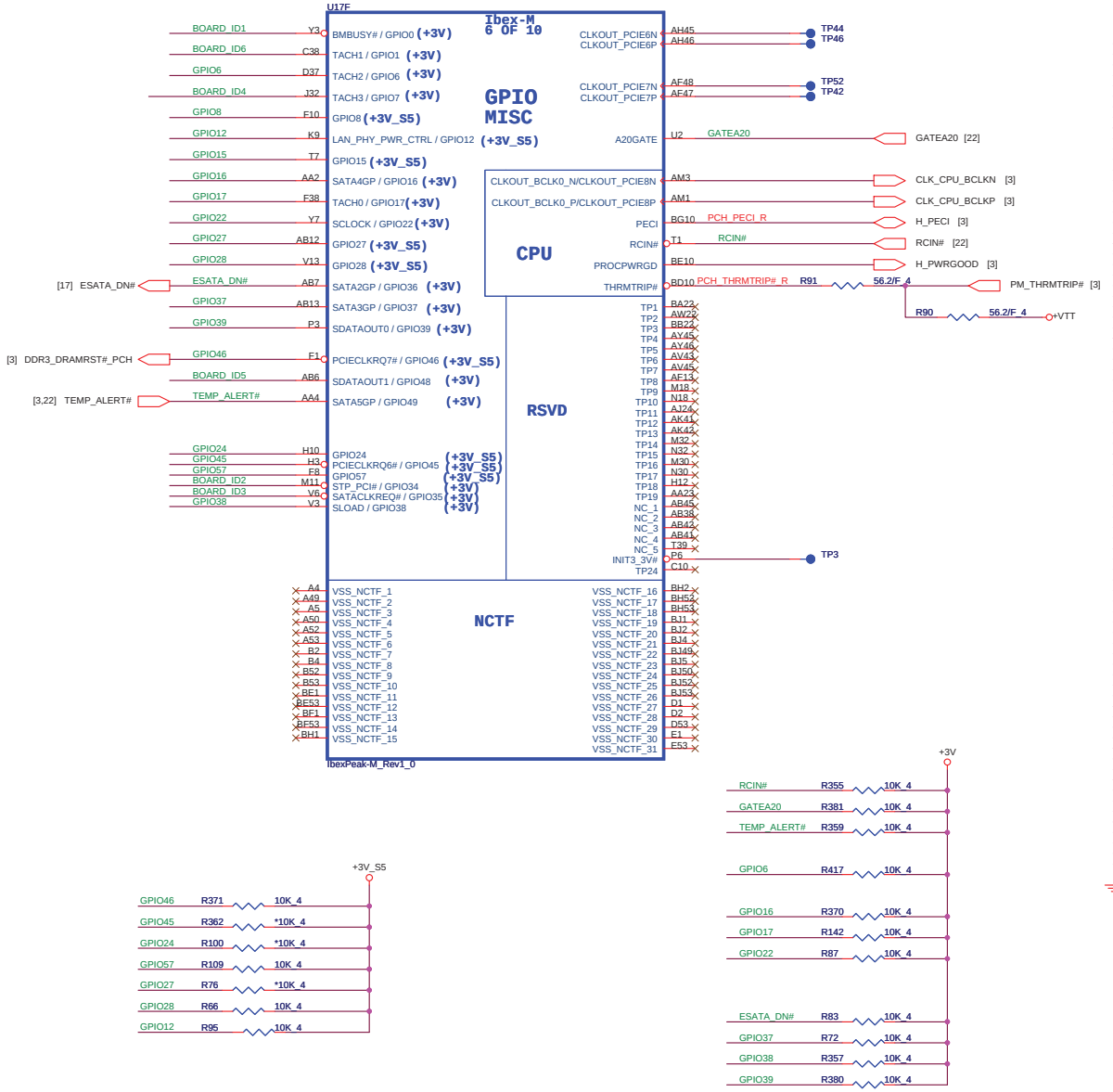
IBEX PEAK-M (DMI,FDI,GPIO)



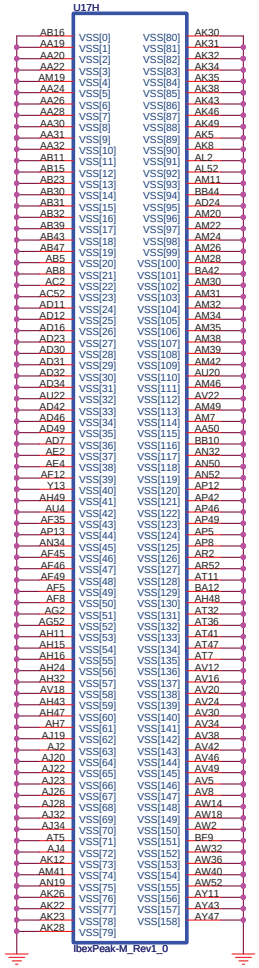


Quanta Computer Inc.			
PROJECT : TE2			
Size	Document Number		Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)		2A
Date:	Wednesday, March 10, 2010	Sheet 9 of 35	

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

SPKR

[7,19] PCBEEP — *1K/F_4 — R364 — +3V

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/ GPIO55

[9] GNT3# — R452 — *10K/F_4

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

HDA_DOCK_EN #/GPIO33

[7,22] PCH_GPIO33 — R136 — 10K_4 — JP1 (2, 1 *SHORT PAD)

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

GNT0#, GNT1#

[9] GNT0# — GNT0# R184 *1K/F_4
[9] GNT1# — GNT1# R185 *1K/F_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

SPI_MOSI

[7] SPI_SI_R — R348 — *1K_4 — +3V

NV_ALE

[9] NV_ALE — R98 — *10K_4 — +1.8V

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 — R81 — 10K_4 — +3V_S5

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 — R58 — 1K_4 — +3V_S5

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

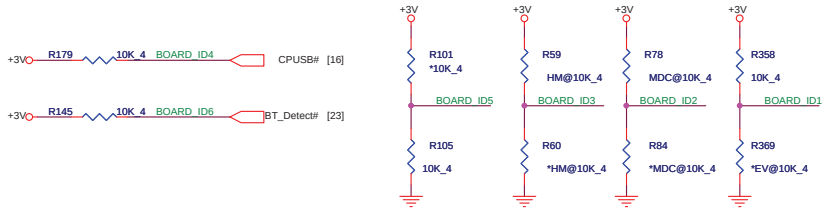
GPIO27

GPIO27 — R79 — *10K_4

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6
UMA SKU VGA SKU	H L					
W/ MDC W/O MDC		H L				
W/ HDMI W/O HDMI			H L			
W/O 3G W/ 3G				H L		
15" 14"					H L	
W/O BT W/ BT						H L



Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	2A
Date: Wednesday, March 10, 2010	Sheet 10 of 35	

+VCCA_DAC_1_2=69mA(15mils)

VCCCORE = 1.432A(80mils)

VCCALVDS= 59mA(15mils)

VCCLAN = 0.32A(30mils)

40mA(15mils)

VCCME = 1.849A(100mils)

VCC3_3 = 0.357A(30mils)

VCCVRM= 196mA(15mils)

VCCDMI= 31mA(15mils)

V5REF_SUS< 1mA

VCCPNAND= 156mA(15mils)

V5REF< 1mA

VCCIO = 3.062A(150mils)

68mA(15mils)

VCCME3_3= 85mA(15mils)

VCCIO = 3.062A(150mils)

37mA(15mils)

VCCSUS3_3 = 0.163A(20mils)

VCC3_3 = 0.357A(30mils)

Reserve for clear CRT Power

V_CPU >1mA(15mils)

VCCRTC= 2mA(15mils)

VCCIO = 3.062A(150mils)

VCCME = 1.849A(100mils)

VCCSUSHDA= 6mA(15mils)

U17G POWER Ibex-M 7 OF 10

CRT LVDS HVCMOS DMI PCI E* NAND / SPI VCC CORE FDI

IbexPeak-M_Rev1_0

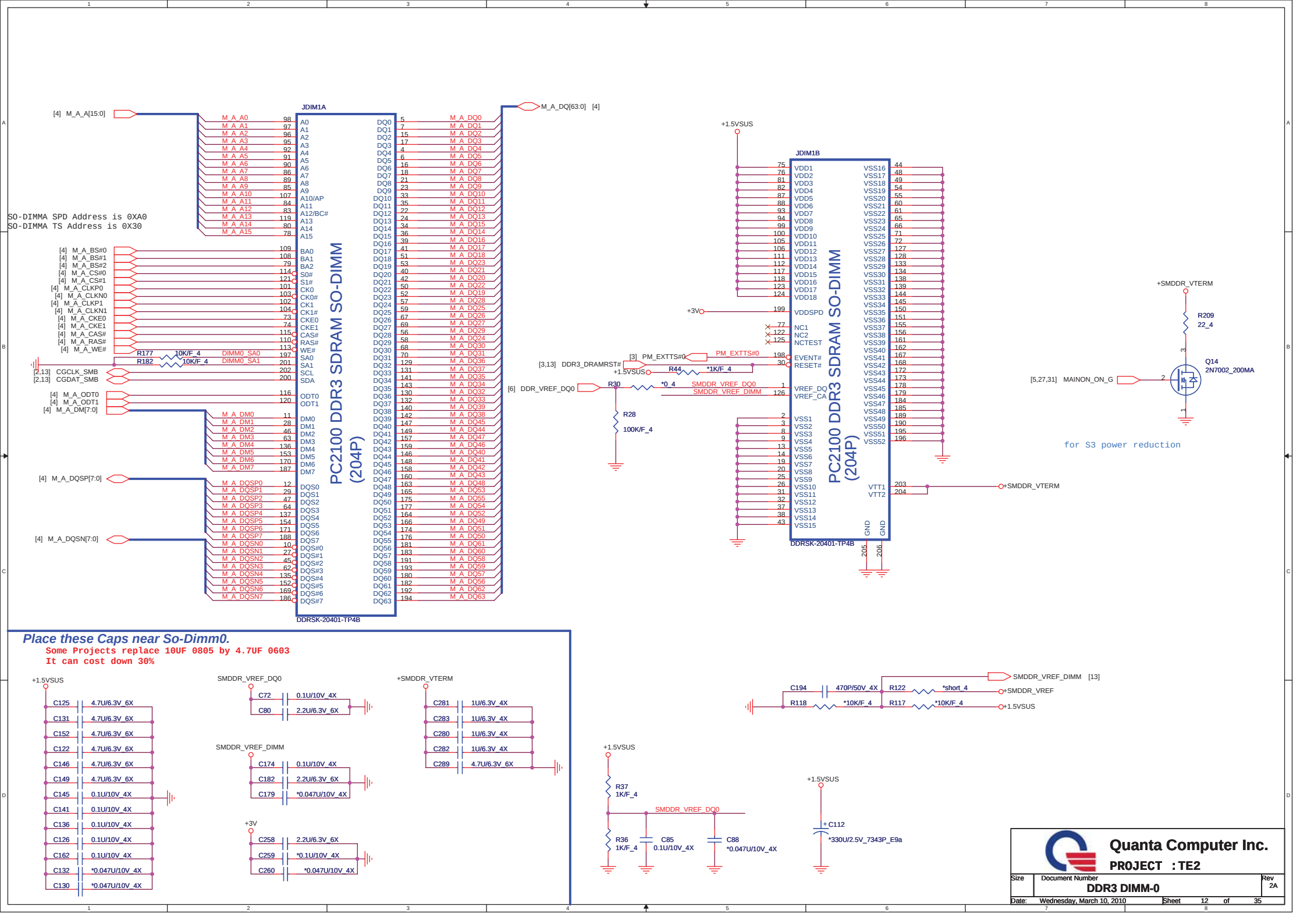
U17J POWER Ibex-M 10 OF 10

Clock and Miscellaneous PCI/GPIO/LPC CPU RTC HDA USB SATA

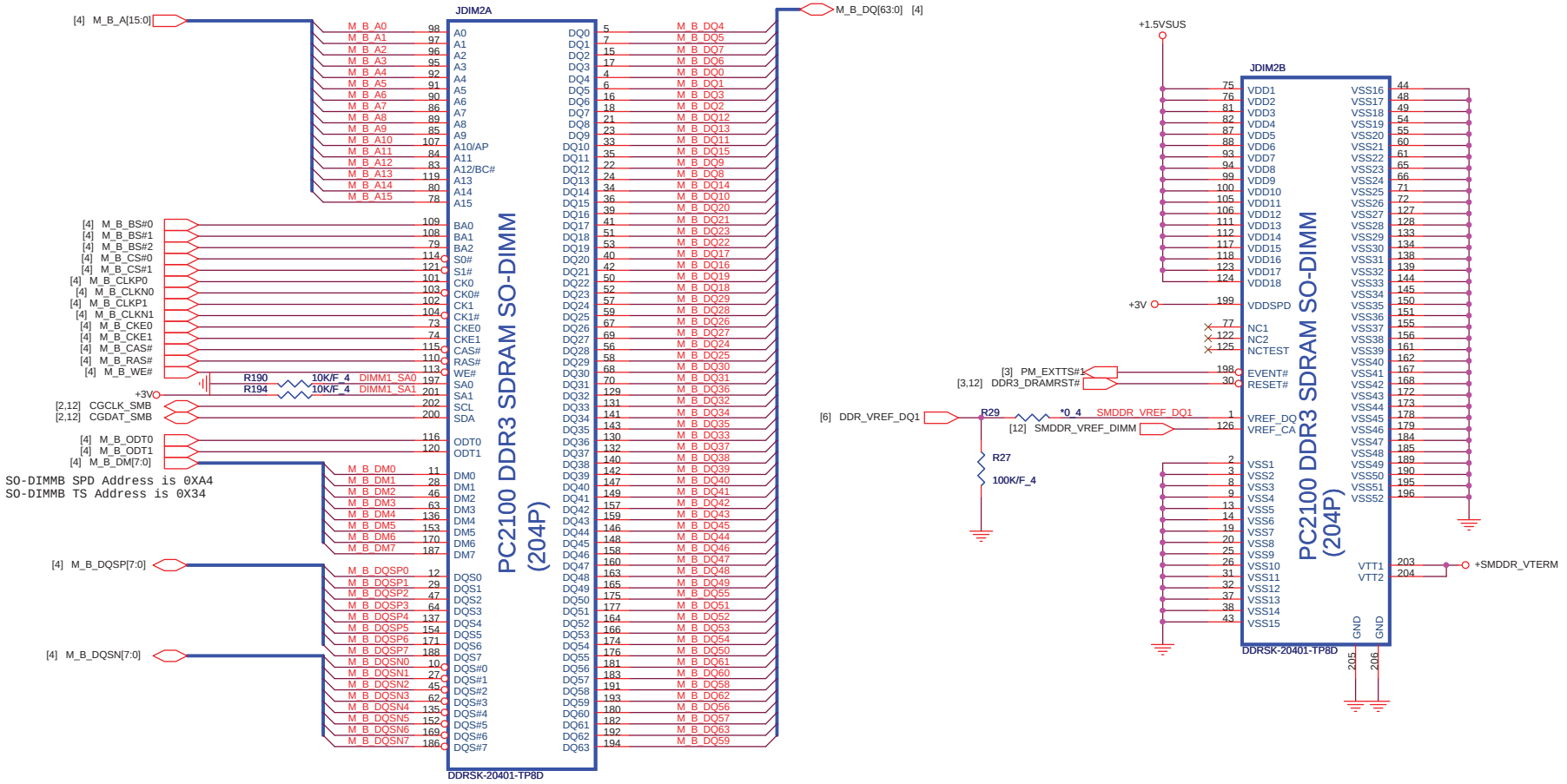
IbexPeak-M_Rev1_0

U19 *G913C

Quanta Computer Inc.			
PROJECT : TE2			
Size	Document Number: PCH 5/5 (POWER)		Rev: 2A
Date: Tuesday, March 09, 2010		Sheet 11 of 35	

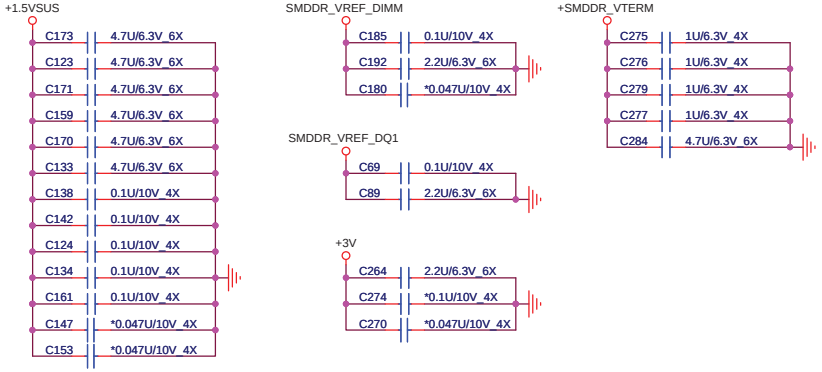


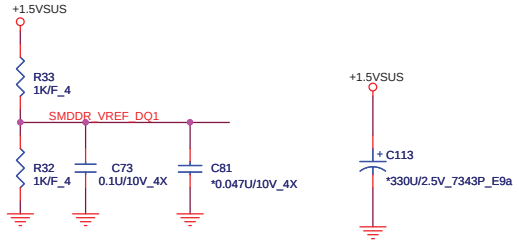
Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: DDR3 DIMM-0	Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 12 of 35	



Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





Quanta Computer Inc.
PROJECT : TE2

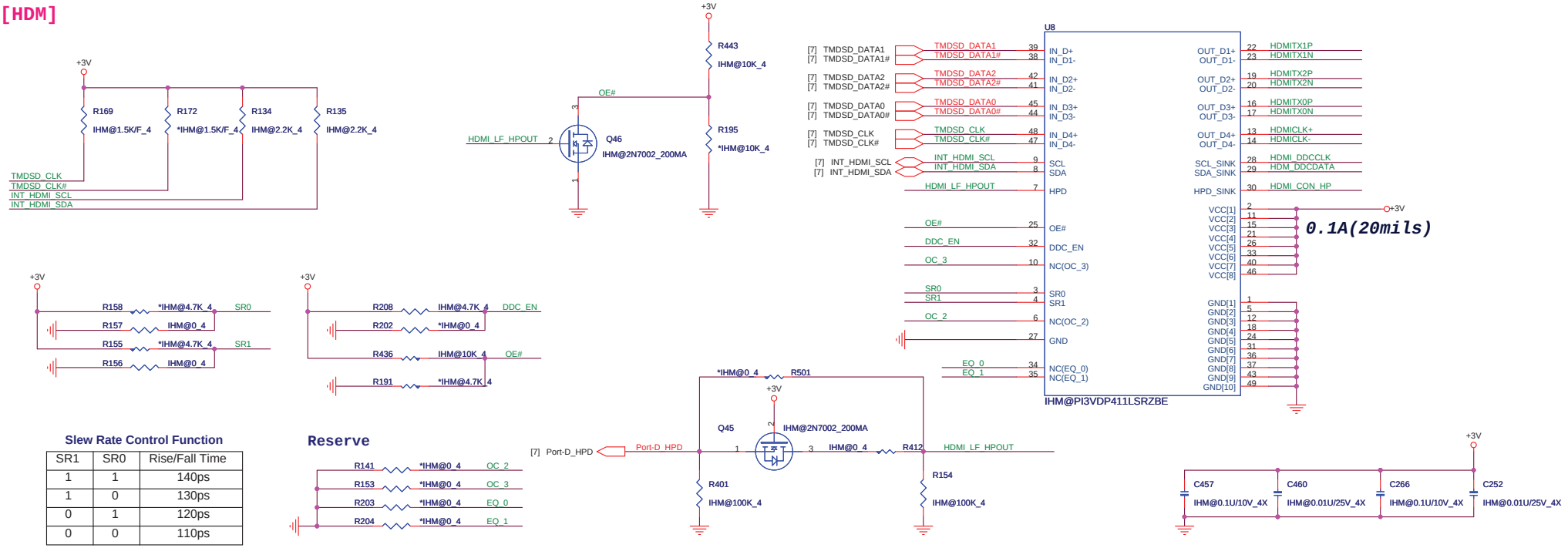
Size	Document Number	Rev
	DDR3 DIMM-1	2A

Date: Wednesday, March 10, 2010 Sheet 13 of 35

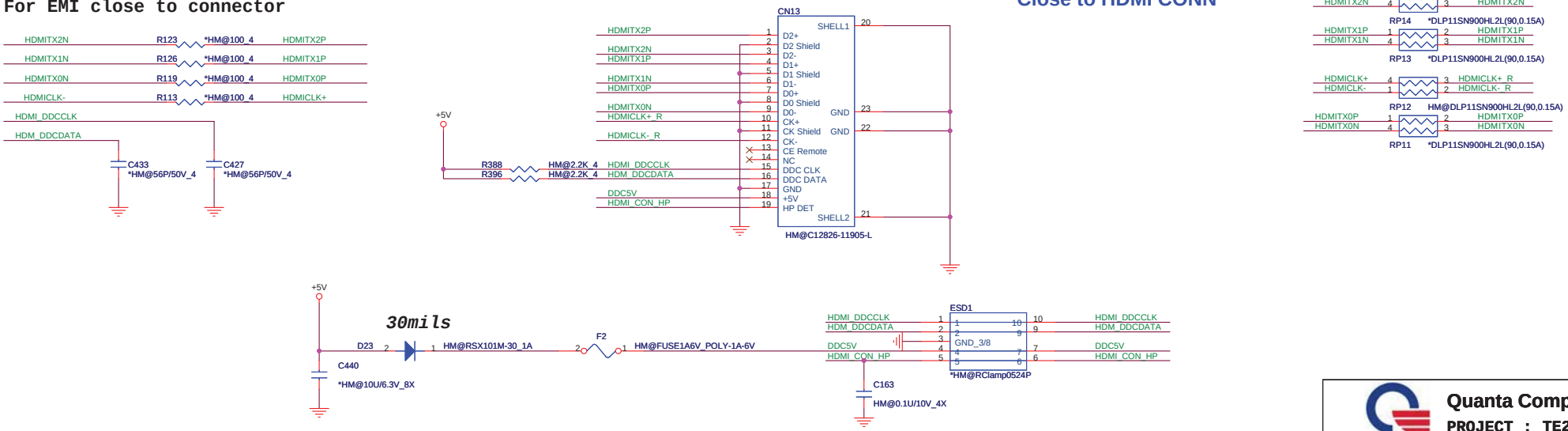
HDMI Conn

HDMI Level Shift UMA only

[HDM]



For EMI close to connector



Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	HDMI CONN	2A

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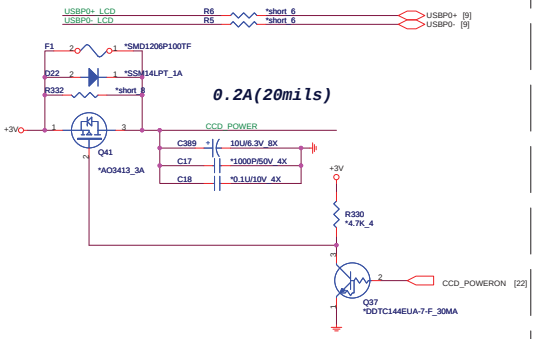
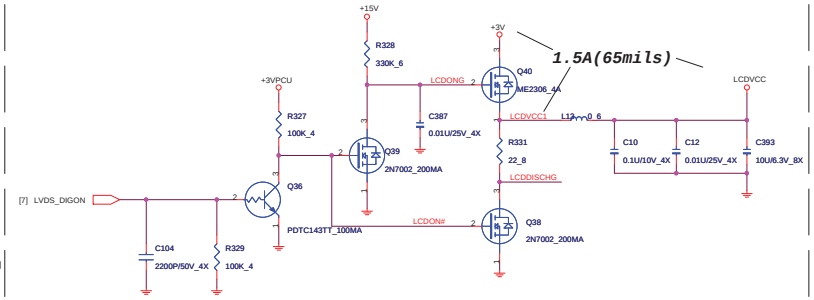
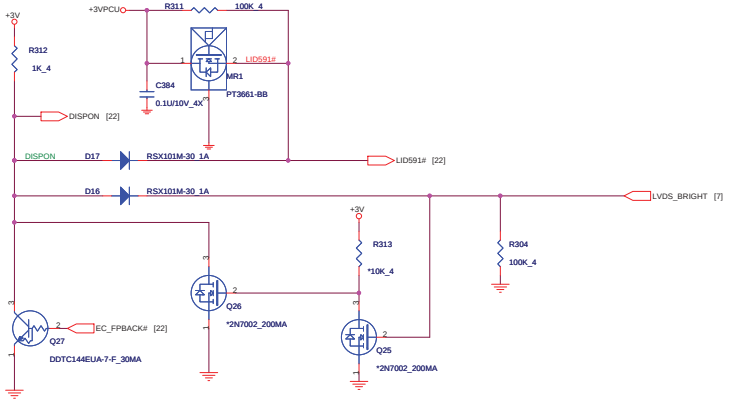
CCD [CCD]



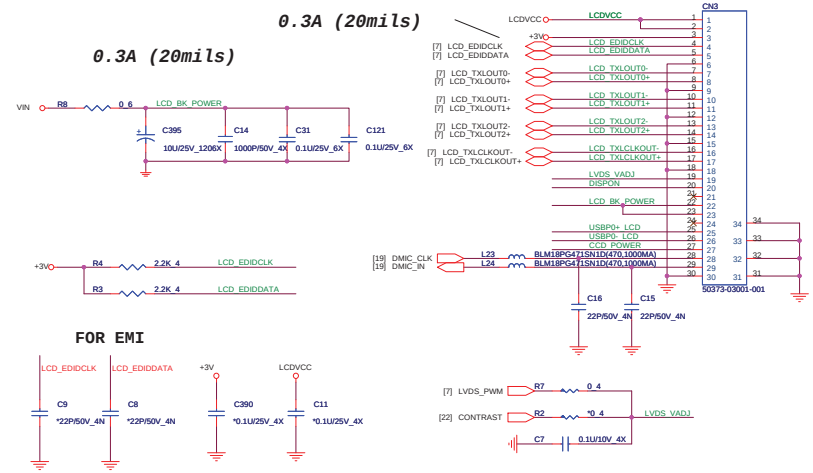
LCD POWER SWITCH [LDS]



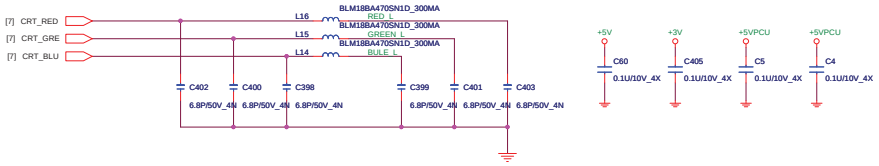
HALL SENSOR&BACK LIGHT SWITCH [HSR]



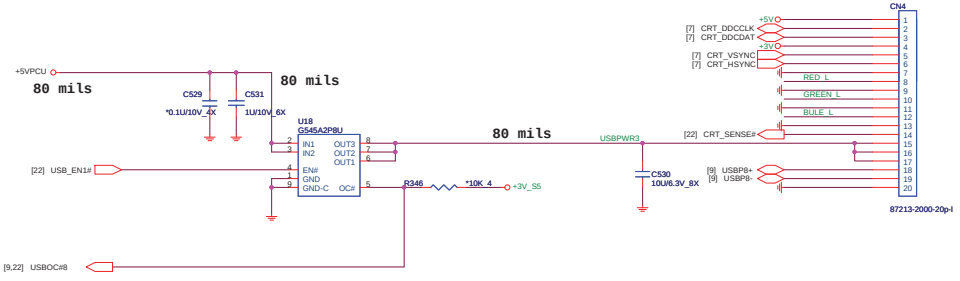
LCD Panel Module [LDS]



CRT [CRT]



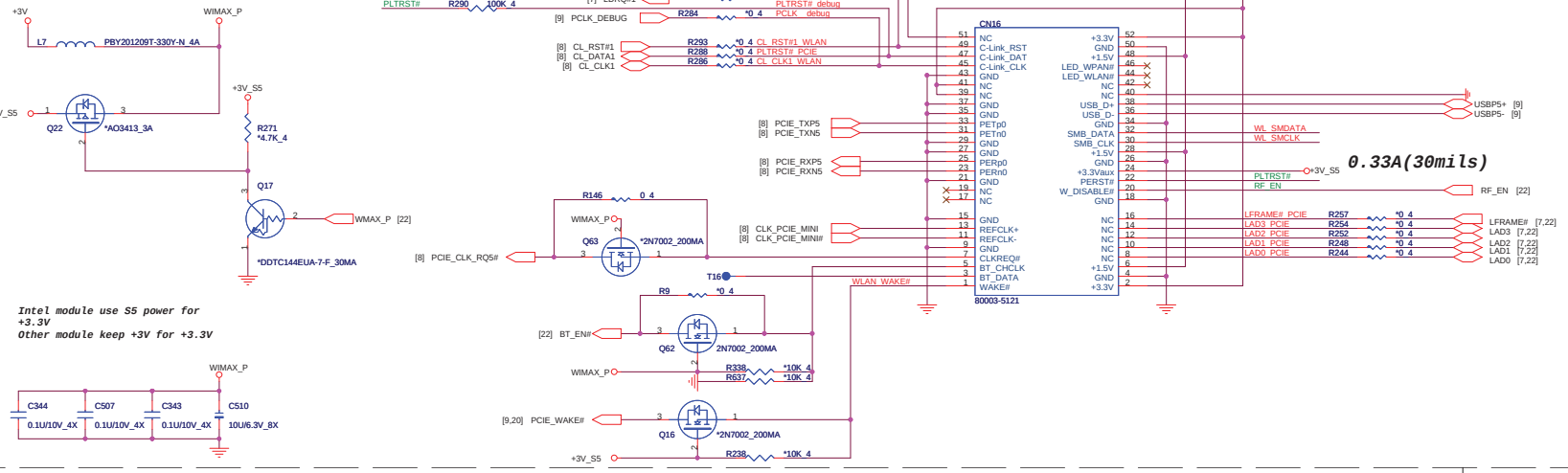
USB for CRT BOARD [USB]



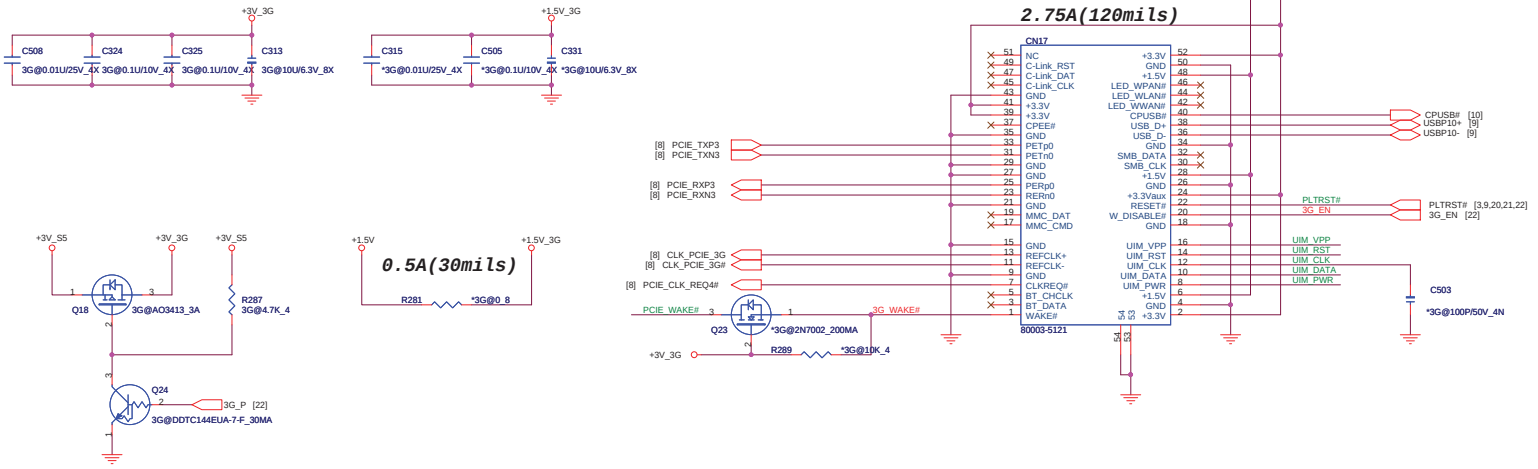
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	LCD/LED Panel/CCD	2A
Date: Tuesday, March 09, 2010	Sheet 15 of 35	

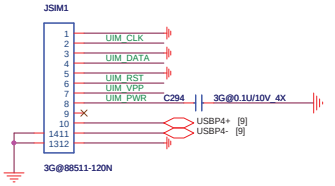
MINI Card Slot#1 (WiFi) [WLN]



MINI Card Slot#2 3G [M3G]



SIM CARD

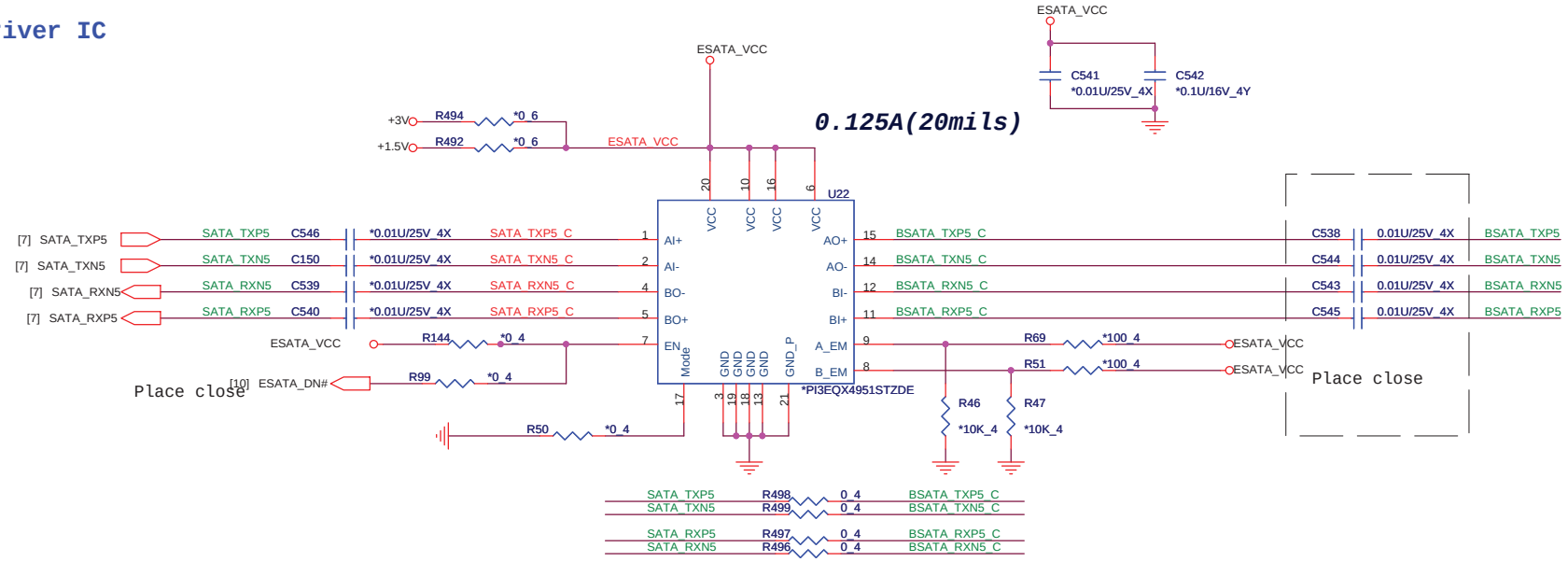


Quanta Computer Inc.
PROJECT : TE2

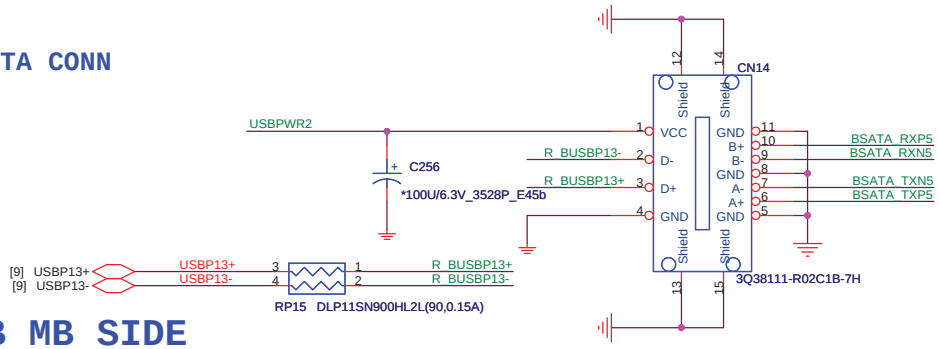
Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	2A
Date: Friday, March 19, 2010	Sheet 16 of 35	

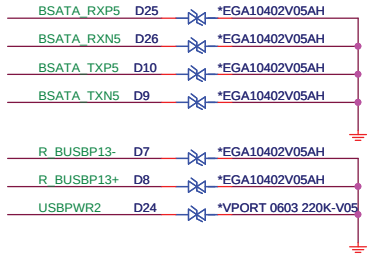
E-SATA [ESA]

SATA HDD Re-driver IC

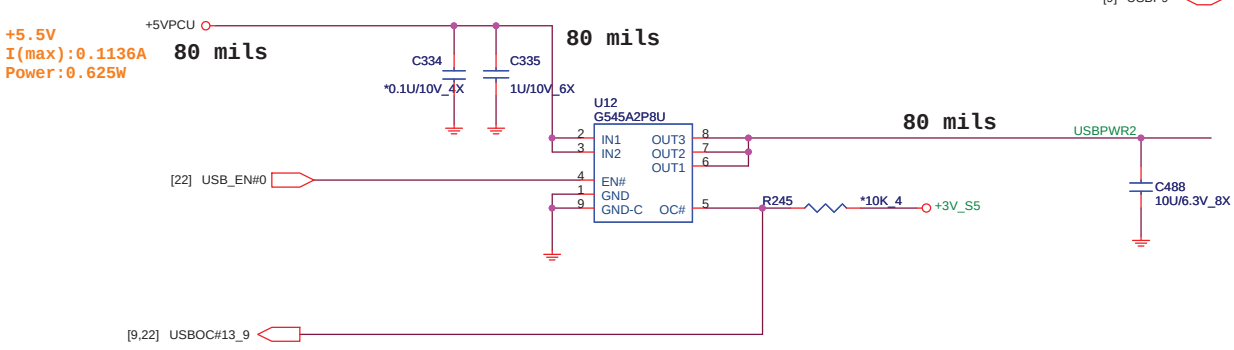


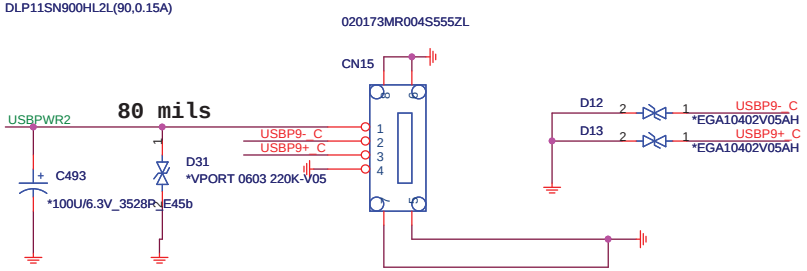
ESATA CONN





USB MB SIDE





Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	TP/SW/ESATA/USB+Audio/LED	2A

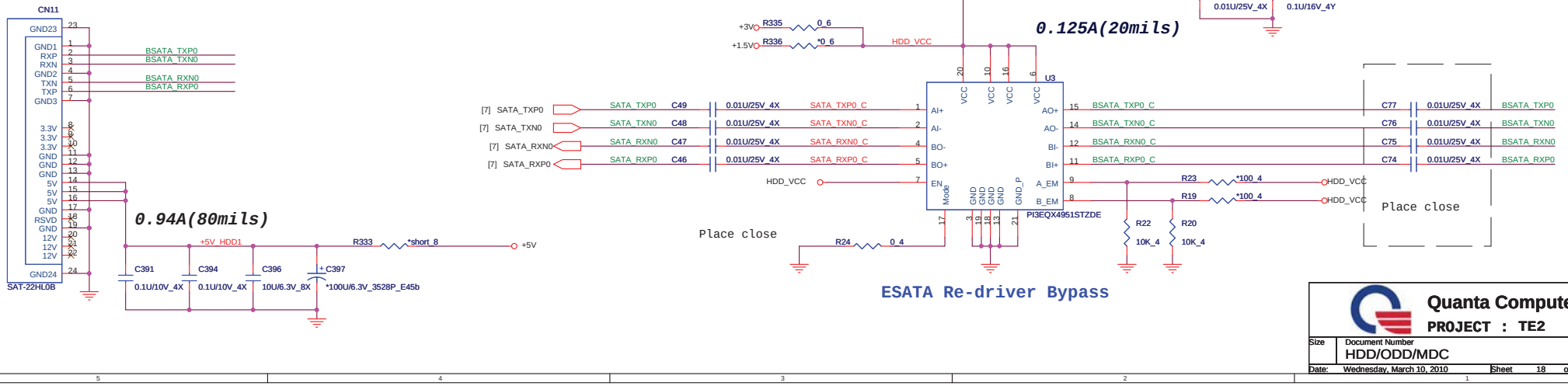
Date: Wednesday, March 10, 2010 Sheet 17 of 35

SATA ODD

[ODD]

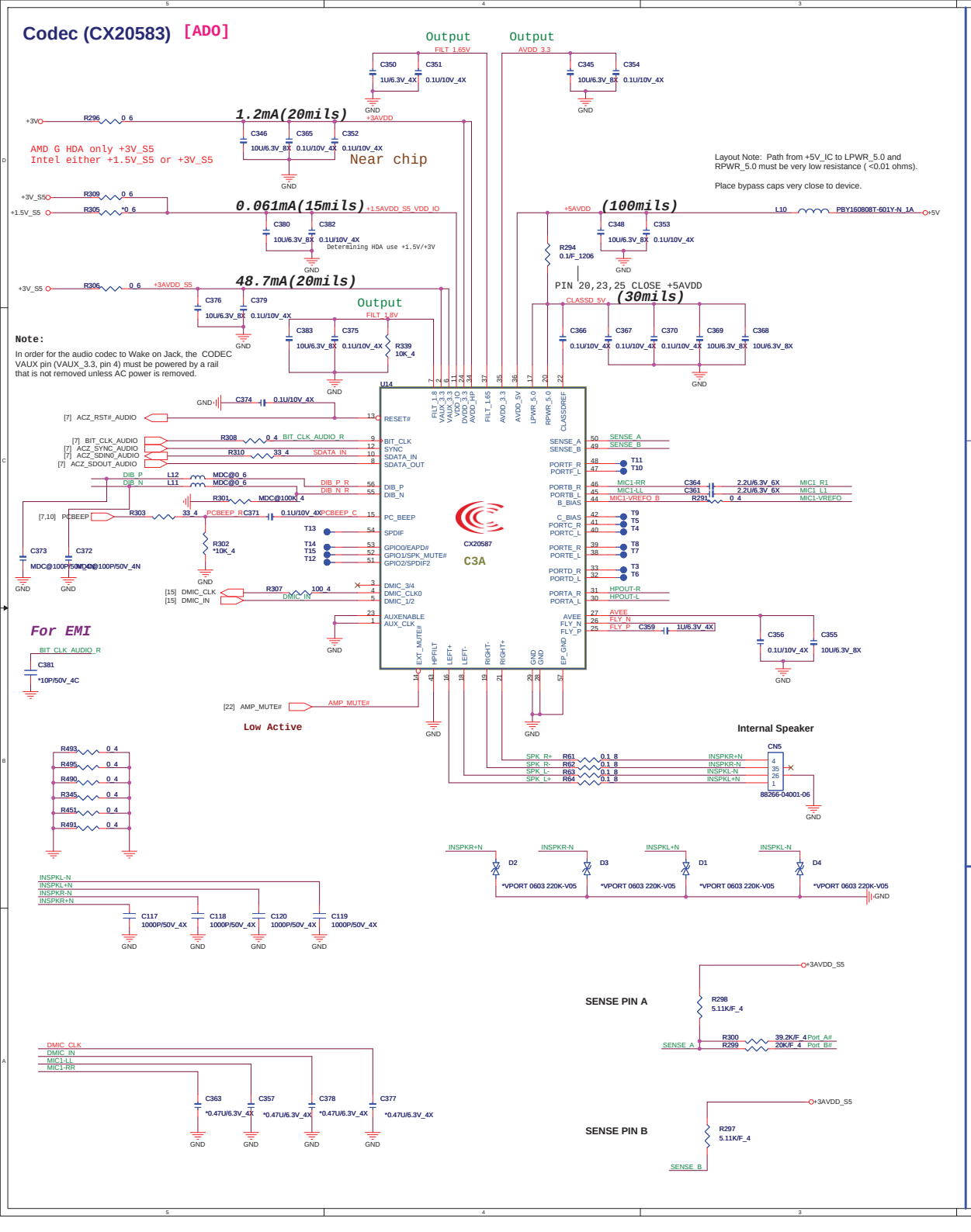
SATA HDD

[HDD]



Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: HDD/ODD/MDC	Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 18 of 35	

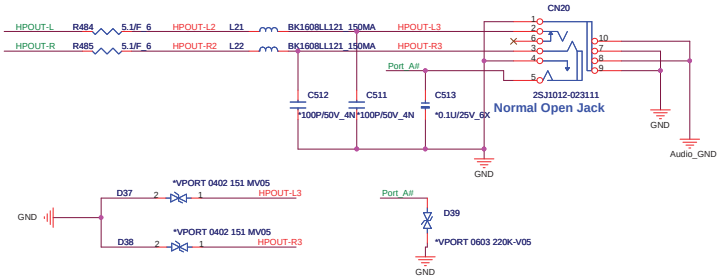
Codec (CX20583) [ADO]



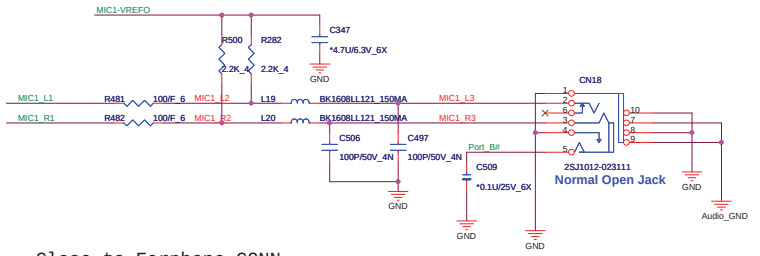
Layout Note: Path from +5V_IC to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

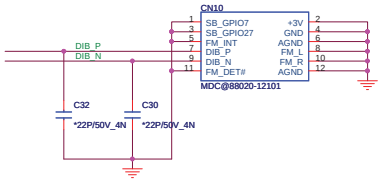
Earphone



External MIC

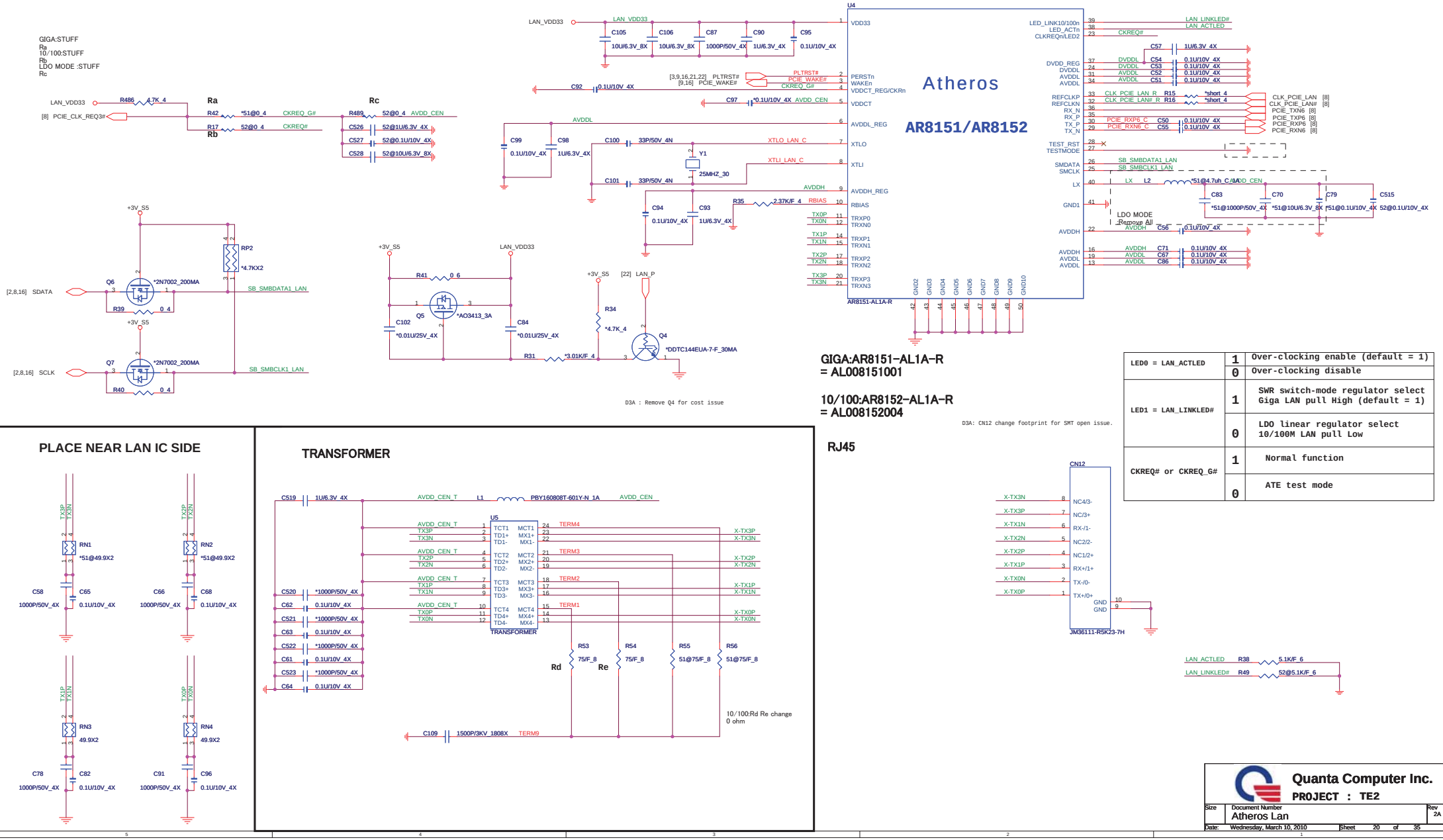


MDC



Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: Codec (CX20583)	Rev: 2A
Date: Friday, March 19, 2010	Sheet 19 of 35	

Atheros Lan



GIGA:AR8151-AL1A-R
= AL008151001

10/100:AR8152-AL1A-R
= AL008152004

RJ45

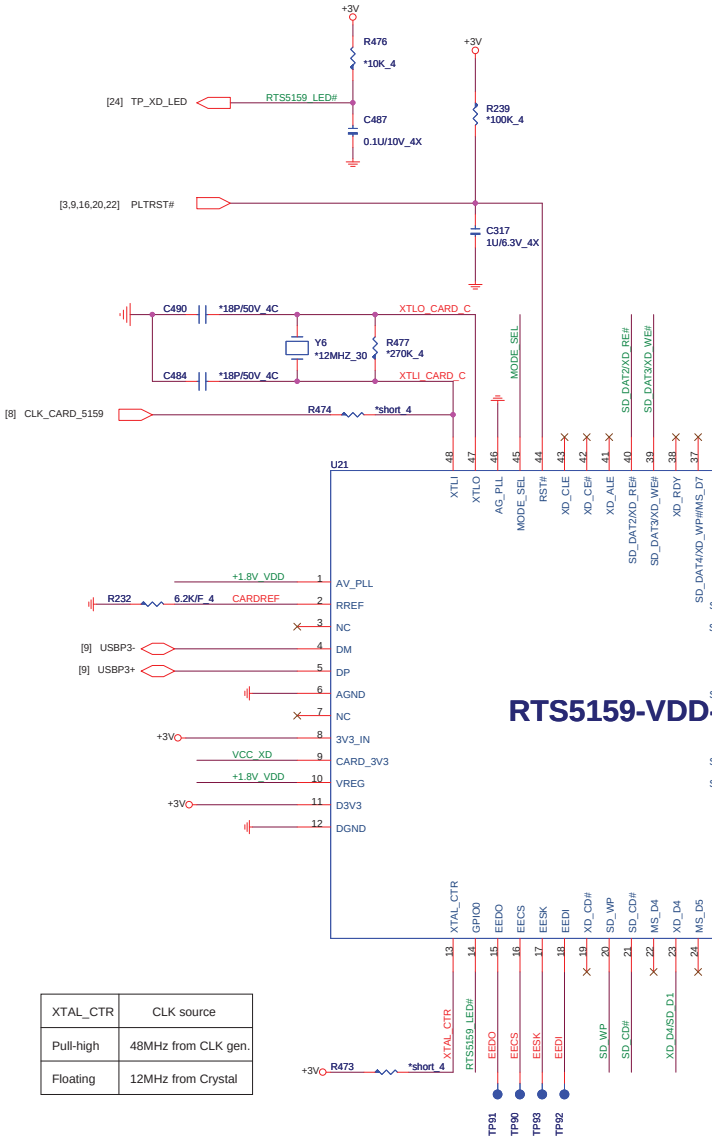
LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

PLACE NEAR LAN IC SIDE

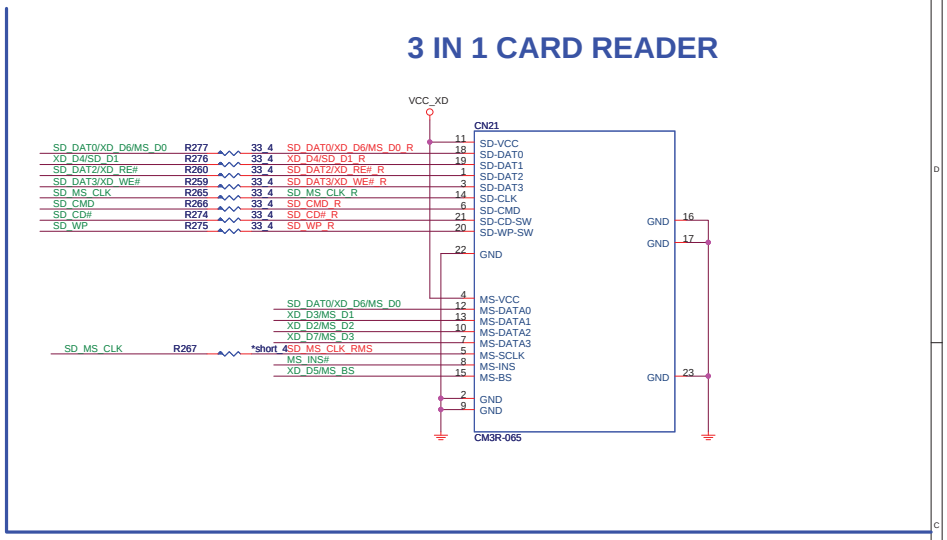
TRANSFORMER

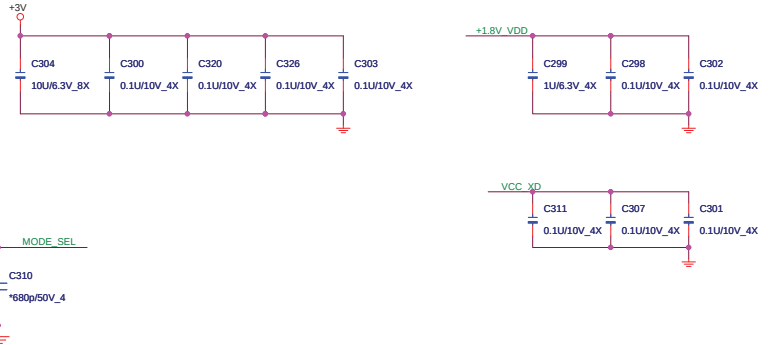
Quanta Computer Inc.	
PROJECT : TE2	
Size	Document Number: Atheros Lan — Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 20 of 35

3 IN 1 CARD READER



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal





MODE_SEL (Please refer to Realtek Application Notes for more detail description)

	R49	C73	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

Quanta Computer Inc.
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Size	Document Number	Rev
	RTS5159 (Card Reader)	2A
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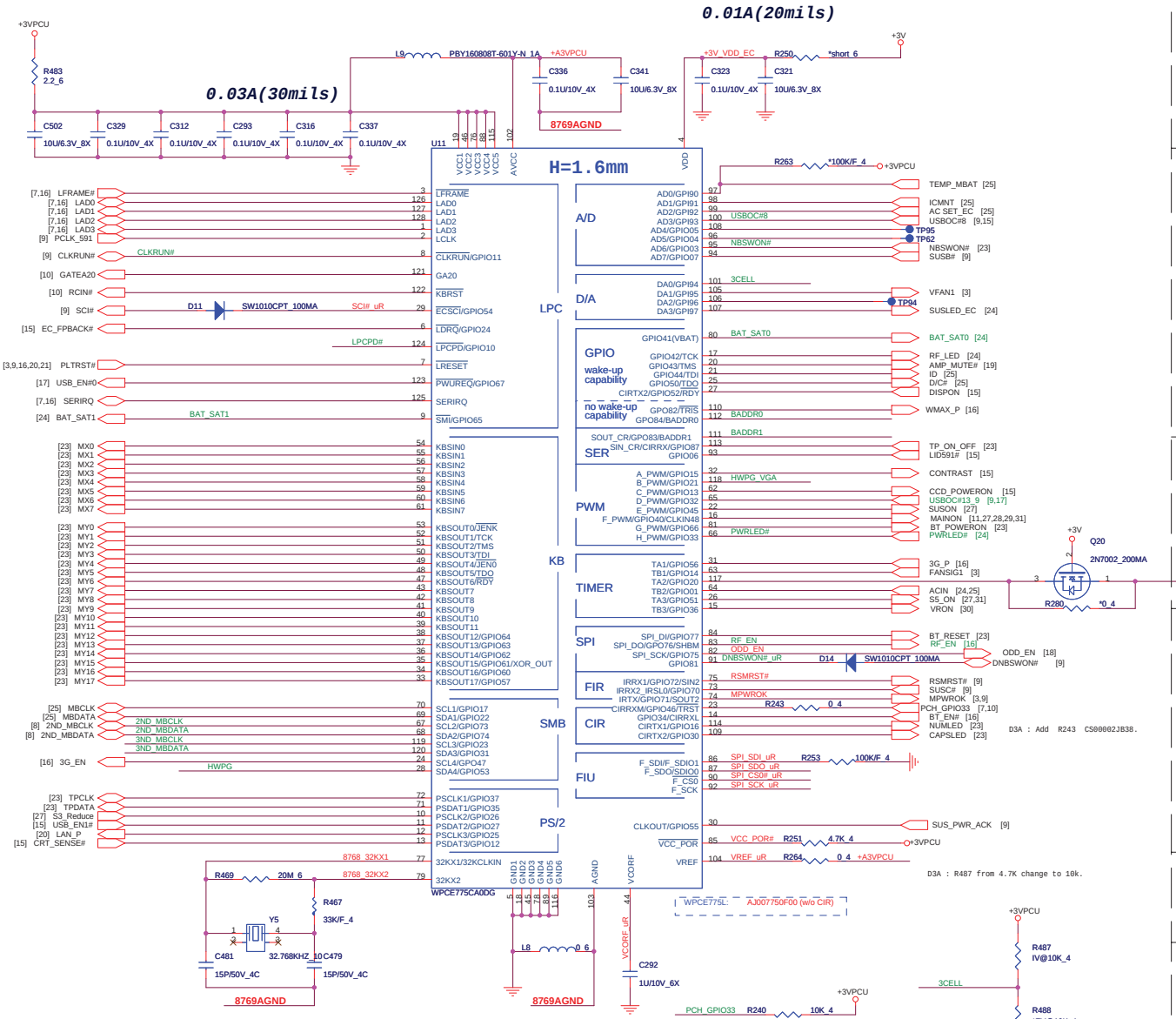
EC [KBC]



SM BUS PU

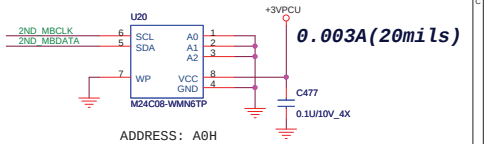
I/O Base Address

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

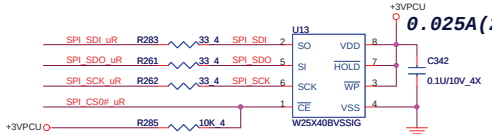
SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID



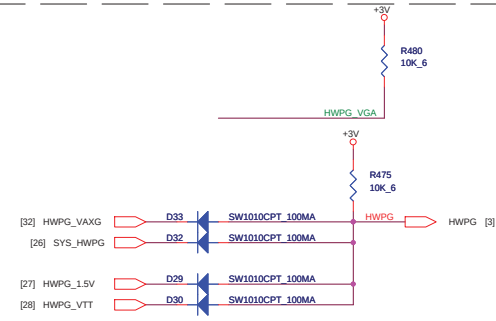
SPI FLASH



Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

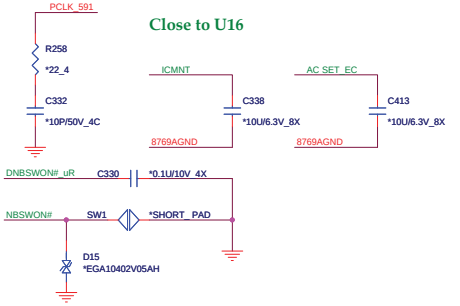
INTERNAL KEYBOARD STRIP SET

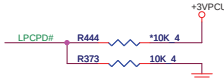
HWPG



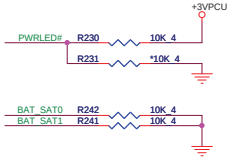
SMBUS Table

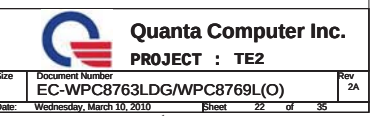
SMBUS	Devices	Address
1	Battery	12H
2	CPU Board Thermal Sensor	
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H



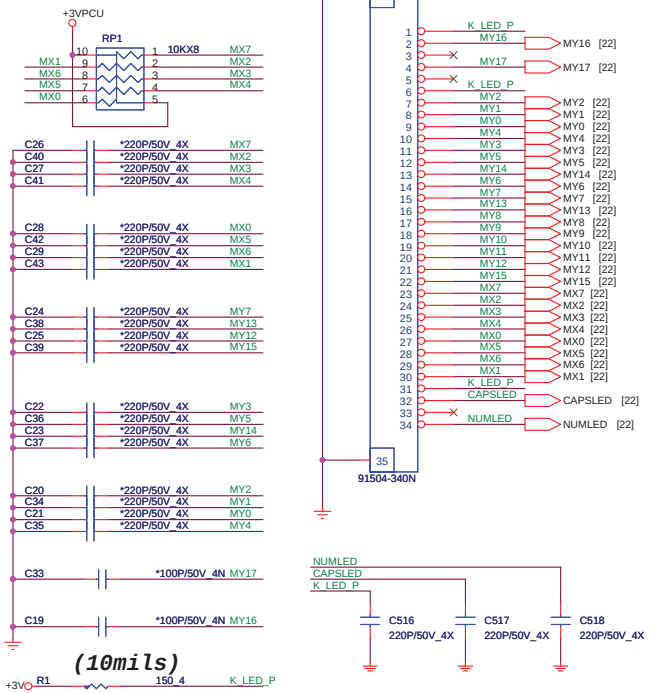


LED PU/PD

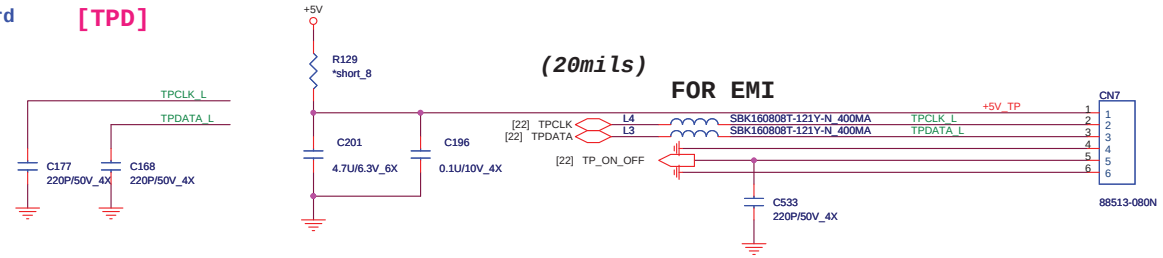




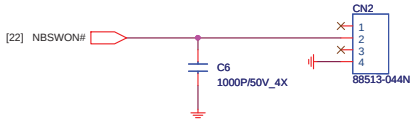
INT KeyBoard [KBC]



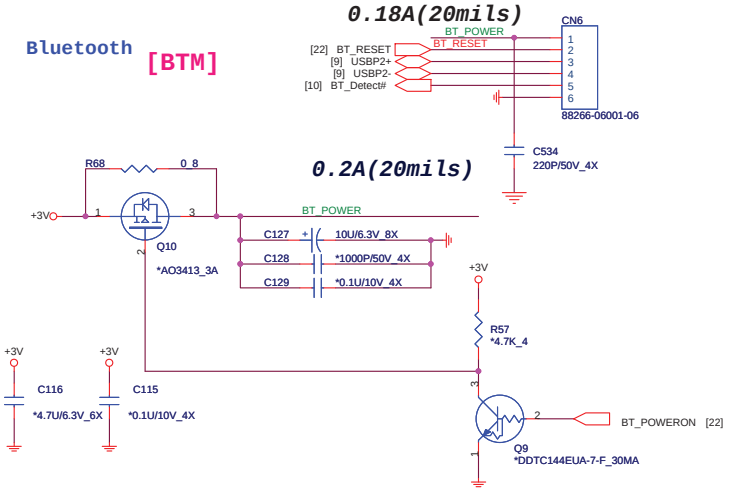
TP board [TPD]



Power board [PSW]

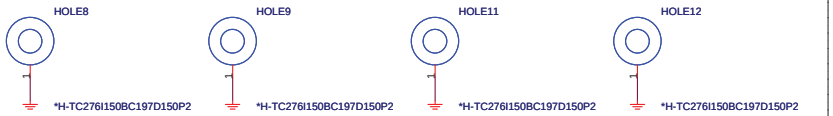


Bluetooth [BTM]

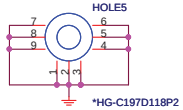


HOLE

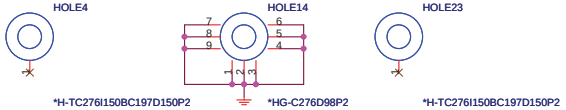
CPU



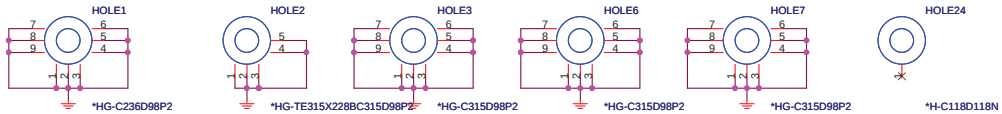
MDC

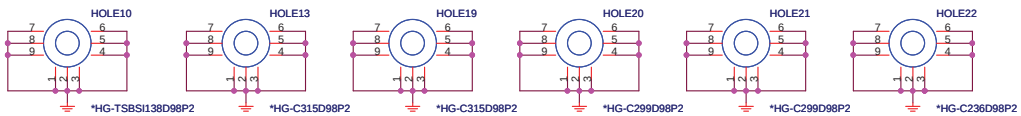


MINI CARD



HDD&ODD





Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	2A

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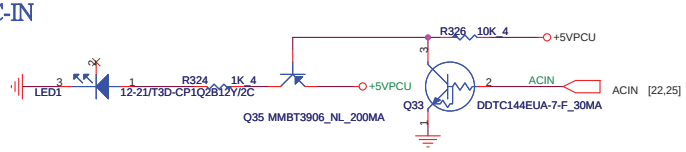
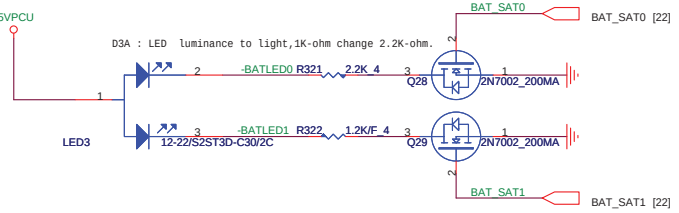
LED [LED]

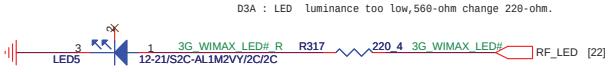
AC-IN



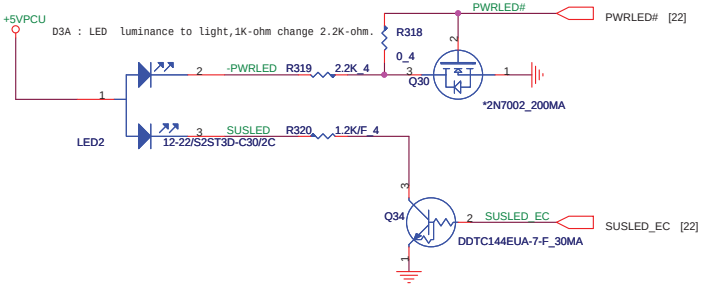
BATERRY



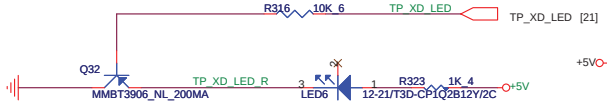
RF LED



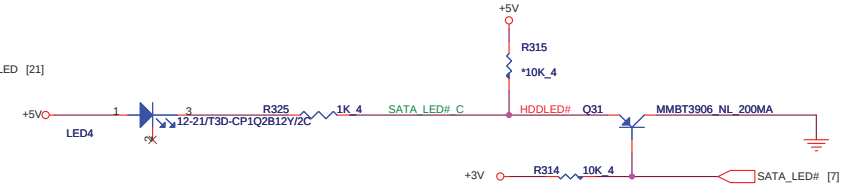
POWER



CARDREADER

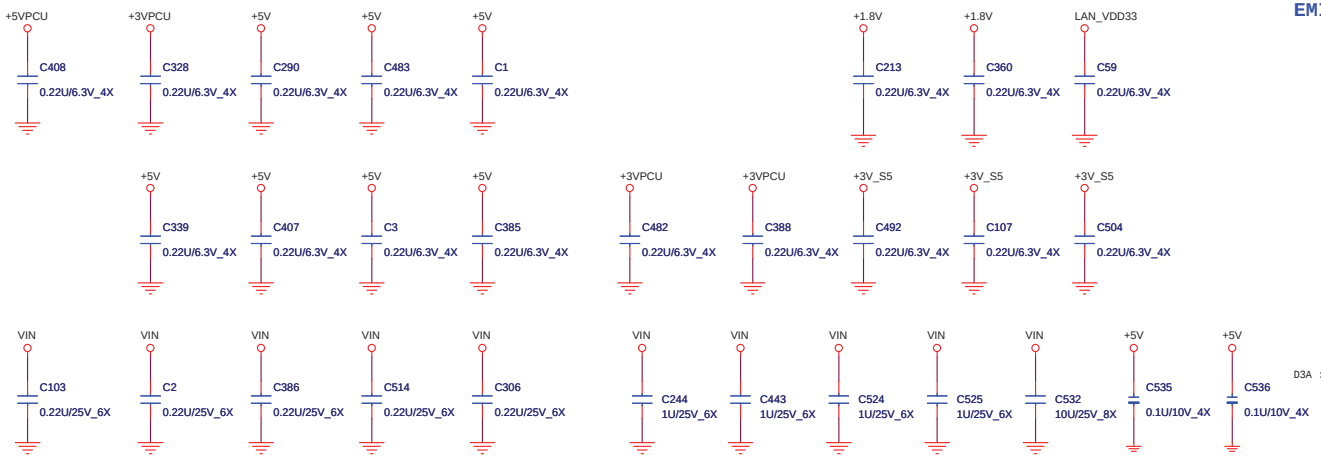


HDD/ODD

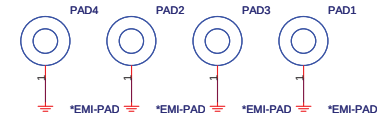


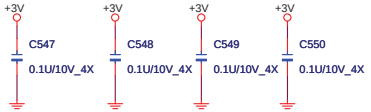
ESD Protect

EMI



EMI PAD





D3A : Add C547,C548,C549,C550 0.1u Cap for EMI issue.

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	LED/HOLE	2A

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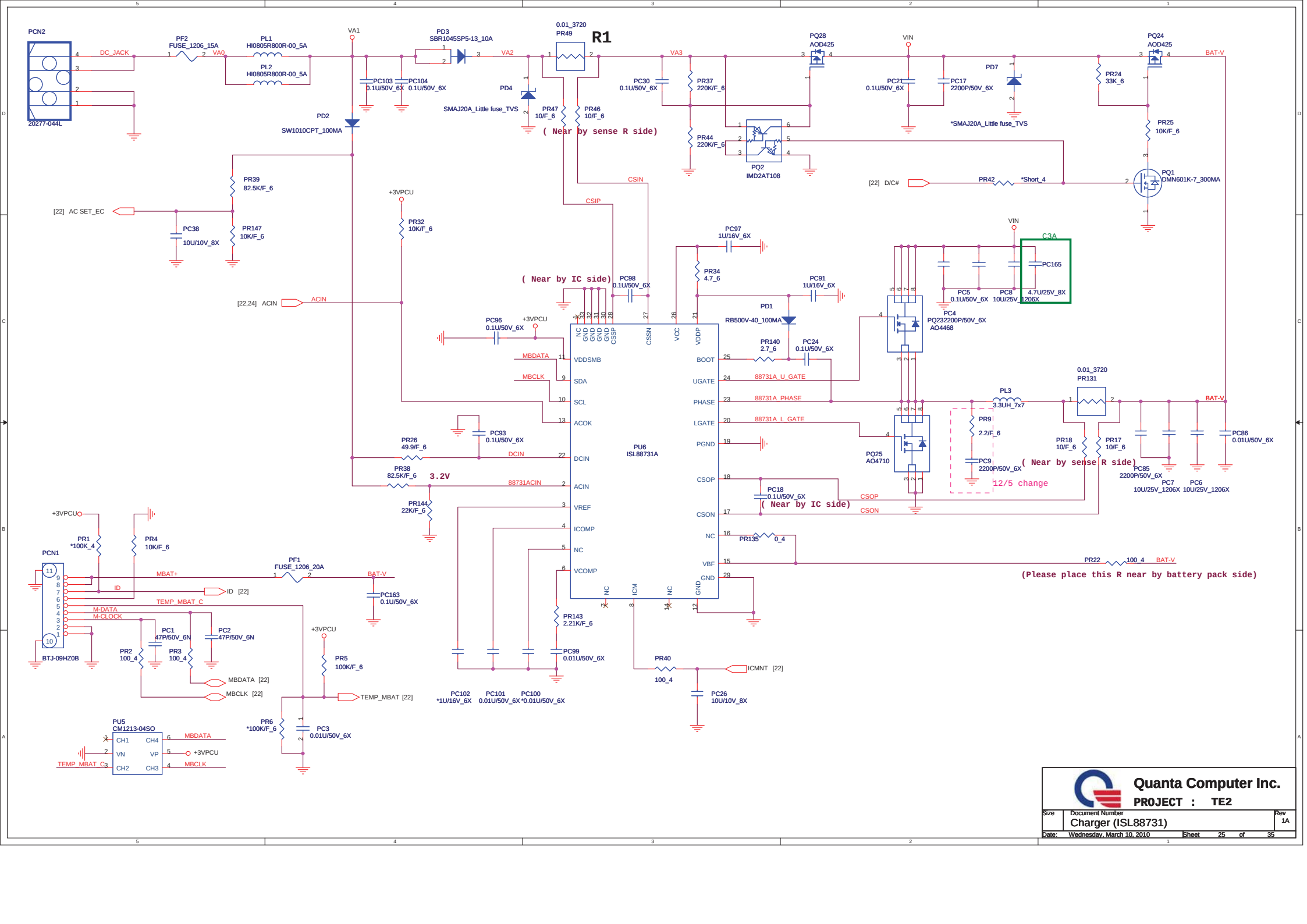
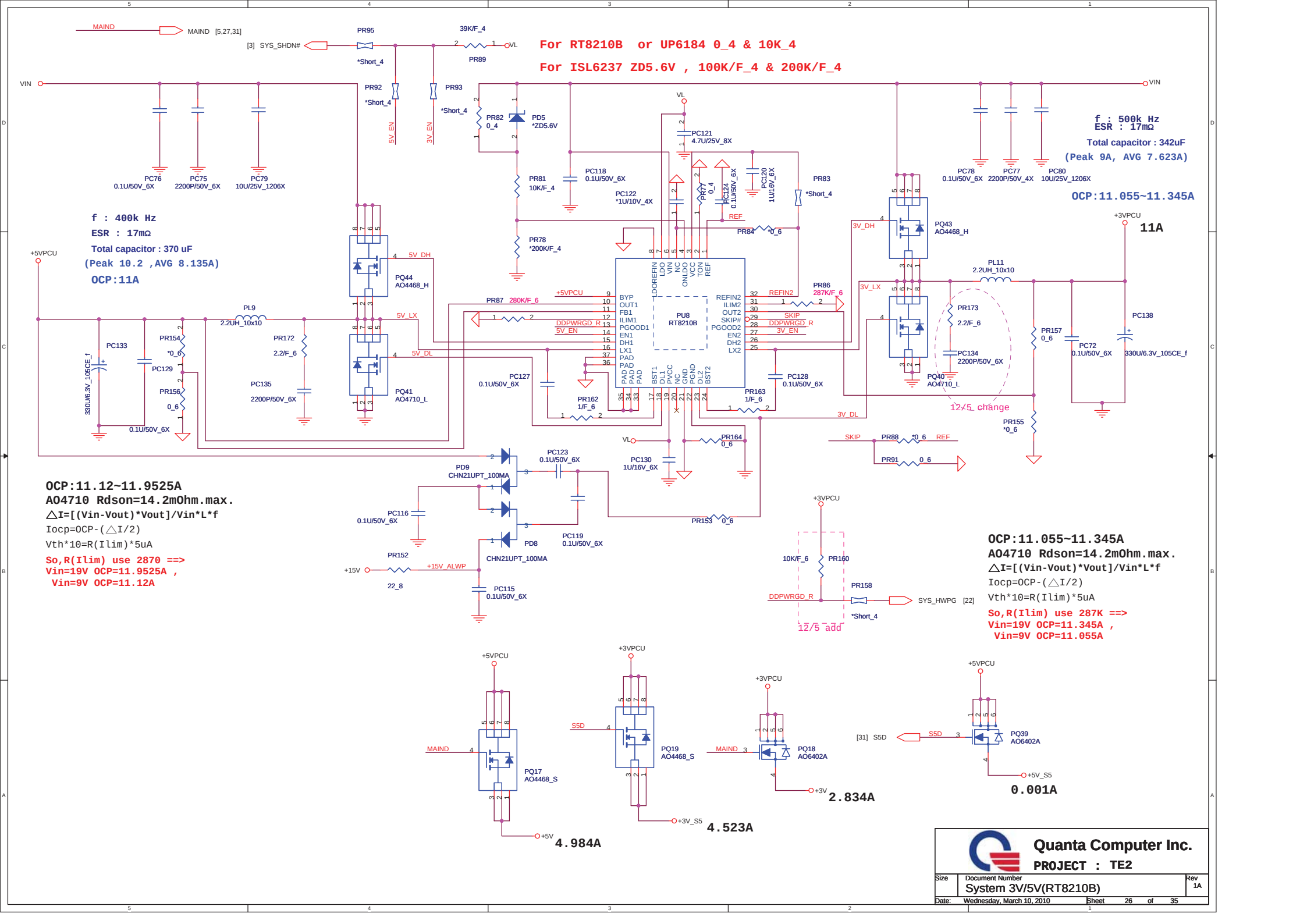


Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: Charger (ISL88731)	Rev: 1A
Date: Wednesday, March 10, 2010	Sheet 25 of 35	


For RT8210B or UP6184 0_4 & 10K_4
For ISL6237 ZD5.6V , 100K/F_4 & 200K/F_4
f : 500k Hz
ESR : 17mΩ
Total capacitor : 342uF
(Peak 9A, AVG 7.623A)
OCP:11.055~11.345A
11A
f : 400k Hz
ESR : 17mΩ
Total capacitor : 370 uF
(Peak 10.2 ,AVG 8.135A)
OCP:11A
PU8 RT8210B
PQ44 AO4468_H
PQ41 AO4710_L
PQ43 AO4468_H
PQ40 AO4710_L
PD5 *ZD5.6V
PD9 CHN21UPT_100MA
PD8 CHN21UPT_100MA
PL9 2.2UH_10x10
PL11 2.2UH_10x10
PR81 10K/F_4
PR78 *200K/F_4
PR82 0_4
PR83 *Short_4
PR84 *0_6
PR86 287K/F_6
PR87 280K/F_6
PR162 1/F_6
PR163 1/F_6
PR164 0_6
PR153 0_6
PR154 *0_6
PR156 0_6
PR172 2.2/F_6
PR173 2.2/F_6
PR155 *0_6
PR157 0_6
PR88 *0_6
PR91 0_6
PR152 22_8
PR158 *Short_4
PR160 10K/F_6
PC133 330U/6.3V_105CE_f
PC129 0.1U/50V_6X
PC135 2200P/50V_6X
PC134 2200P/50V_6X
PC138 330U/6.3V_105CE_f
PC72 0.1U/50V_6X
PC76 0.1U/50V_6X
PC75 2200P/50V_6X
PC79 10U/25V_1206X
PC78 0.1U/50V_6X
PC77 2200P/50V_4X
PC80 10U/25V_1206X
PC118 0.1U/50V_6X
PC122 *1U/10V_4X
PC121 4.7U/25V_8X
PC124 0.1U/50V_6X
PC120 1U/16V_6X
PC127 0.1U/50V_6X
PC128 0.1U/50V_6X
PC130 1U/16V_6X
PC123 0.1U/50V_6X
PC116 0.1U/50V_6X
PC119 0.1U/50V_6X
PC115 0.1U/50V_6X
PQ17 AO4468_S
PQ19 AO4468_S
PQ18 AO6402A
PQ39 AO6402A
4.984A
4.523A
2.834A
0.001A
OCP:11.12~11.9525A
AO4710 Rdson=14.2mOhm.max.
△I=[(Vin-Vout)*Vout]/Vin*L*f
Iocp=OCP-(△I/2)
Vth*10=R(Ilim)*5uA
So,R(Ilim) use 2870 ==>
Vin=19V OCP=11.9525A ,
Vin=9V OCP=11.12A
OCP:11.055~11.345A
AO4710 Rdson=14.2mOhm.max.
△I=[(Vin-Vout)*Vout]/Vin*L*f
Iocp=OCP-(△I/2)
Vth*10=R(Ilim)*5uA
So,R(Ilim) use 287K ==>
Vin=19V OCP=11.345A ,
Vin=9V OCP=11.055A
12/5 change
12/5 add
Quanta Computer Inc.
PROJECT : TE2
System 3V/5V(RT8210B)
Size
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Date: Wednesday, March 10, 2010
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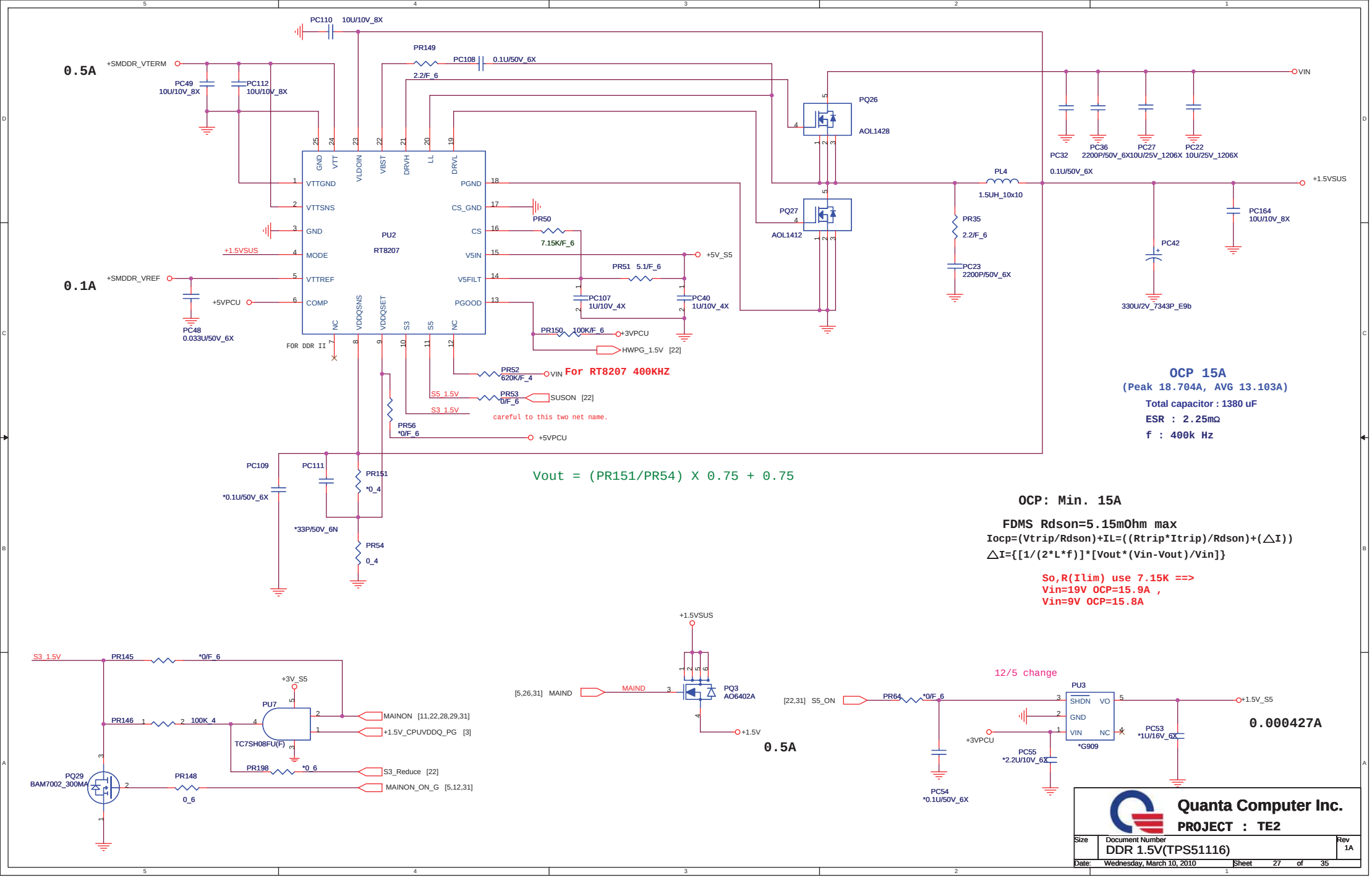
0.5A
0.1A
PU2
RT8207
FOR DDR II
For RT8207 400KHZ
OCP 15A
(Peak 18.704A, AVG 13.103A)
Total capacitor : 1380 uF
ESR : 2.25mΩ
f : 400k Hz
Vout = (PR151/PR54) X 0.75 + 0.75
OCP: Min. 15A
FDMS Rdson=5.15mOhm max
Iocp=(Vtrip/Rdson)+IL=((Rtrip*Itrip)/Rdson)+(△I))
△I={[1/(2*L*f)]*[Vout*(Vin-Vout)/Vin]}
So,R(Ilim) use 7.15K ==>
Vin=19V OCP=15.9A ,
Vin=9V OCP=15.8A
careful to this two net name.
12/5 change
0.000427A
0.5A
PQ26
AOL1428
PQ27
AOL1412
PQ3
AO6402A
PQ29
BAM7002_300MA
PU7
TC7SH08FU(F)
PU3
*G909
PL4
1.5UH_10x10
330U/2V_7343P_E9b
Quanta Computer Inc.
PROJECT : TE2
DDR 1.5V(TPS51116)
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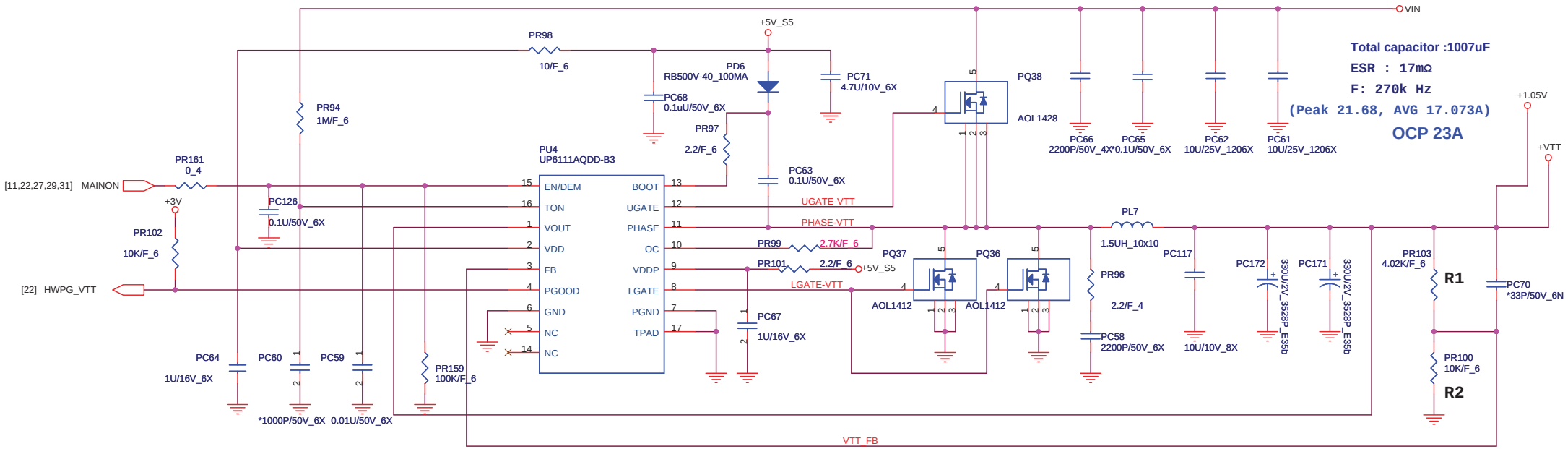
PC63 X V



VOUT=(1+R1/R2)*0.75

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

OCP:23.18~23.27A

FDMS0310 Rdson=5.15mOhm max

Iocp=(Vtrip/Rdson)+IL=((Rtrip*Itrip)/Rdson)+(△I))

△I={[1/(2*L*f)]*[Vout*(Vin-Vout)/Vin]}

Rdson*OCP=RIlim*20uA

So,R(Ilim) use 2.7K ==>

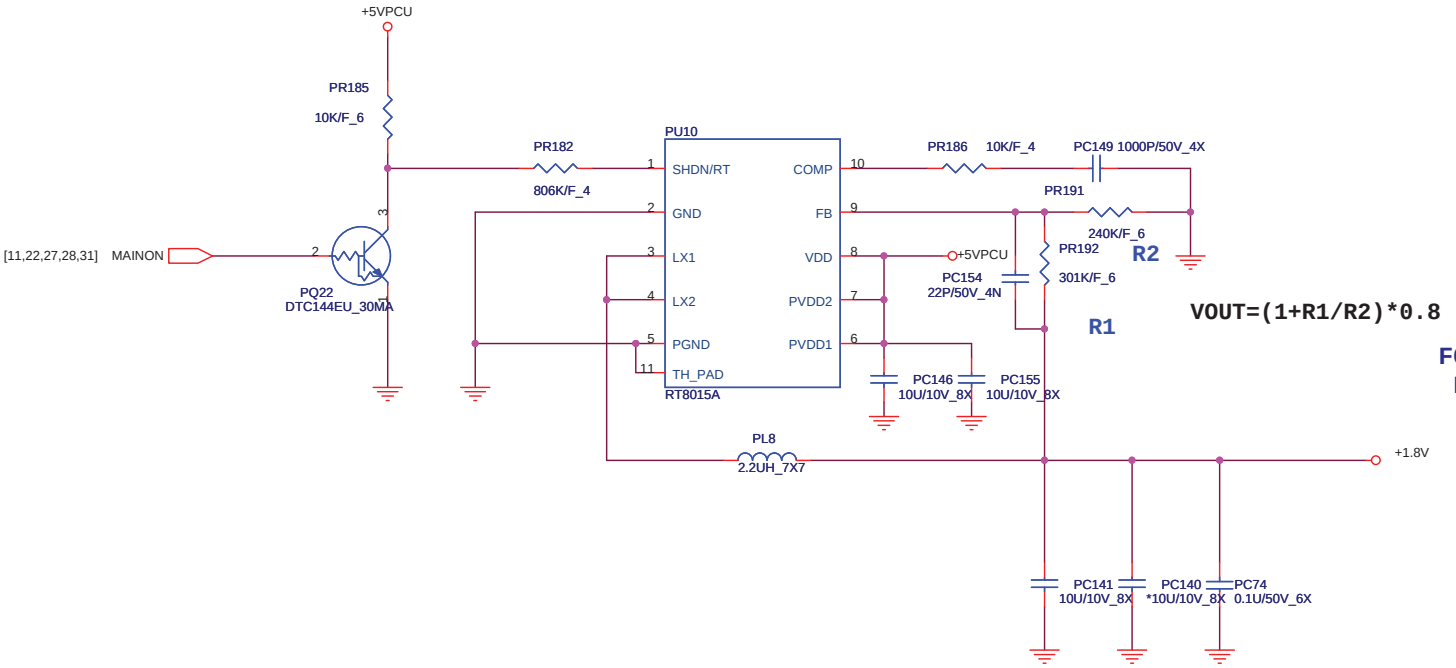
Vin=19V OCP=23.18A ,

Vin=9V OCP=23.27A

Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date: Wednesday, March 10, 2010	Sheet 28 of 35	

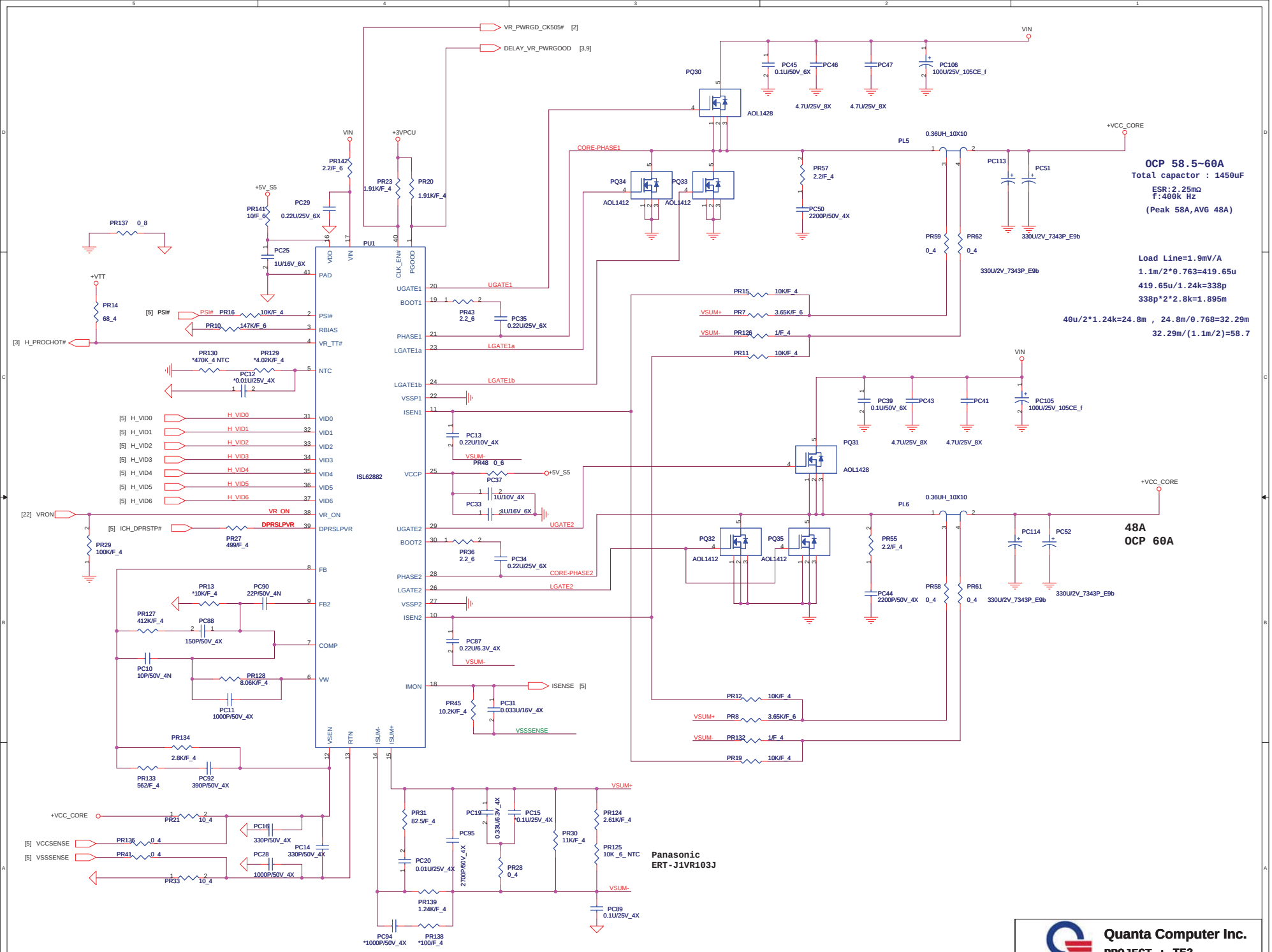


VOUT=(1+R1/R2)*0.8

OCP Fellow IC spec~3.7A

FOR UMA 0.194A
For VGA 1.345A

Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: +1.8V (RT8015A)	Rev: 1A
Date: Tuesday, March 09, 2010	Sheet 29 of 35	



Quanta Computer Inc.			
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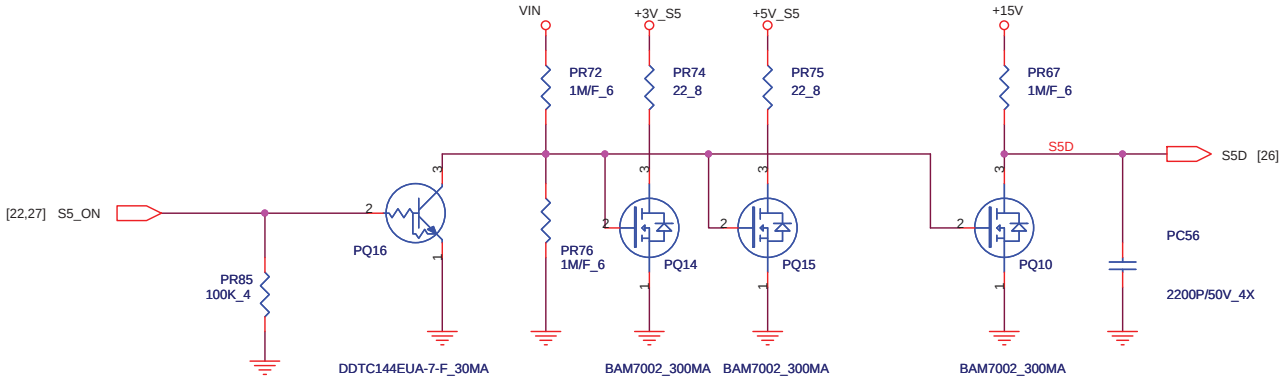
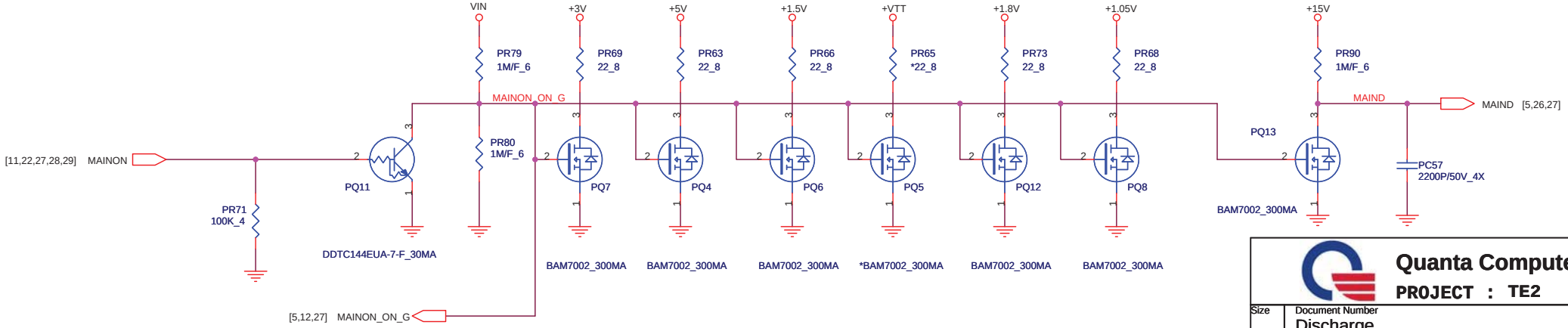
Size	Document Number		Rev
	CPU Core (ISL62882)		1A
Date:	Wednesday, March 10, 2010	Sheet 30 of 35	





Quanta Computer Inc.

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Size	Document Number	Rev
	Discharge	1A

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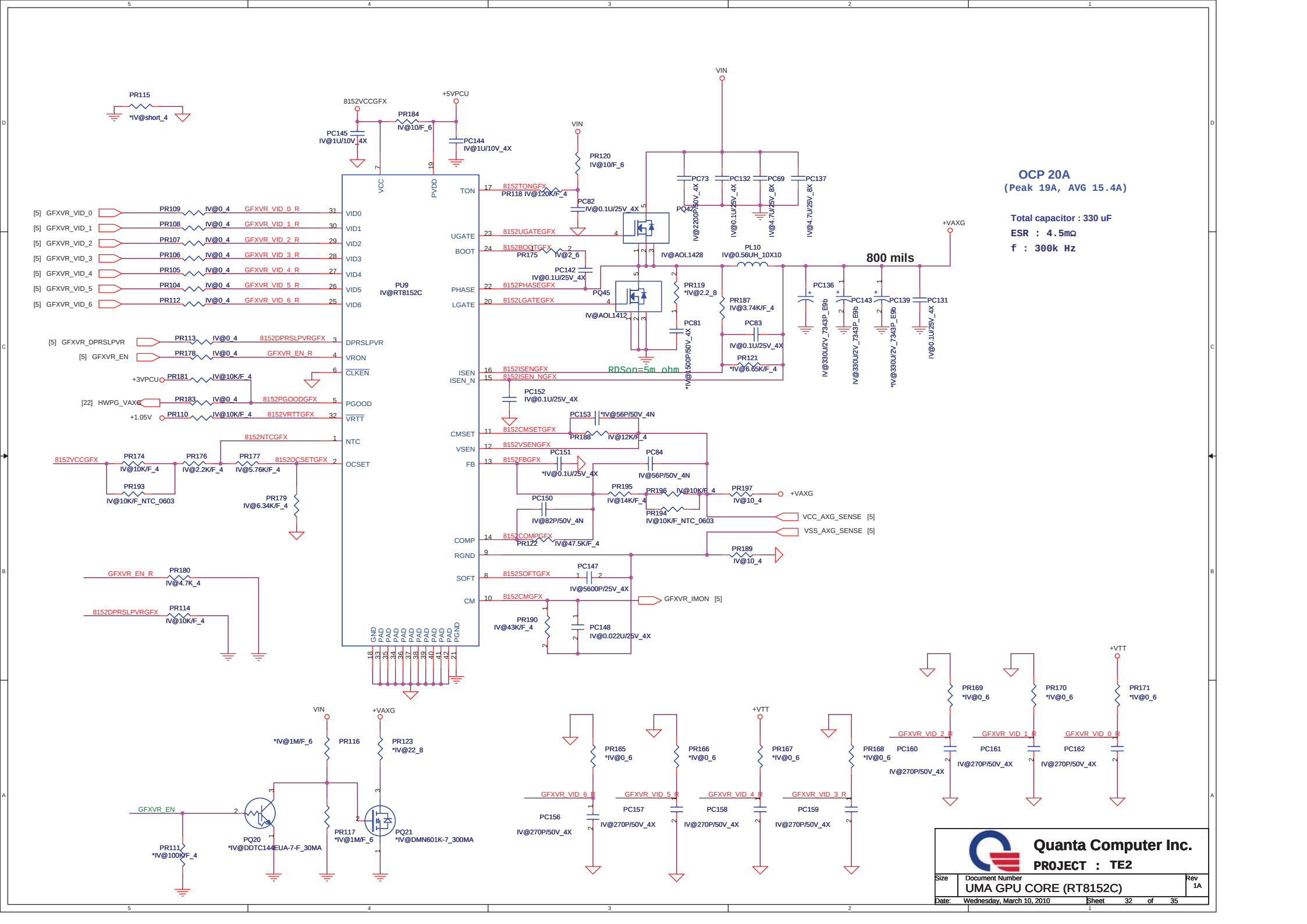
OCP 20A
(Peak 19A, AVG 15.4A)
Total capacitor : 330 uF
ESR : 4.5mΩ
f : 300k Hz
800 mils
RDSon=5m ohm
PU9
IV@RT8152C
Quanta Computer Inc.
PROJECT : TE2
Size
Document Number
UMA GPU CORE (RT8152C)
Rev
1A
Date: Wednesday, March 10, 2010
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Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
GND_SIGNAL	32
CARD_GND	21
AGND_DC/DC	31
GND	ALL

Quanta Computer Inc.

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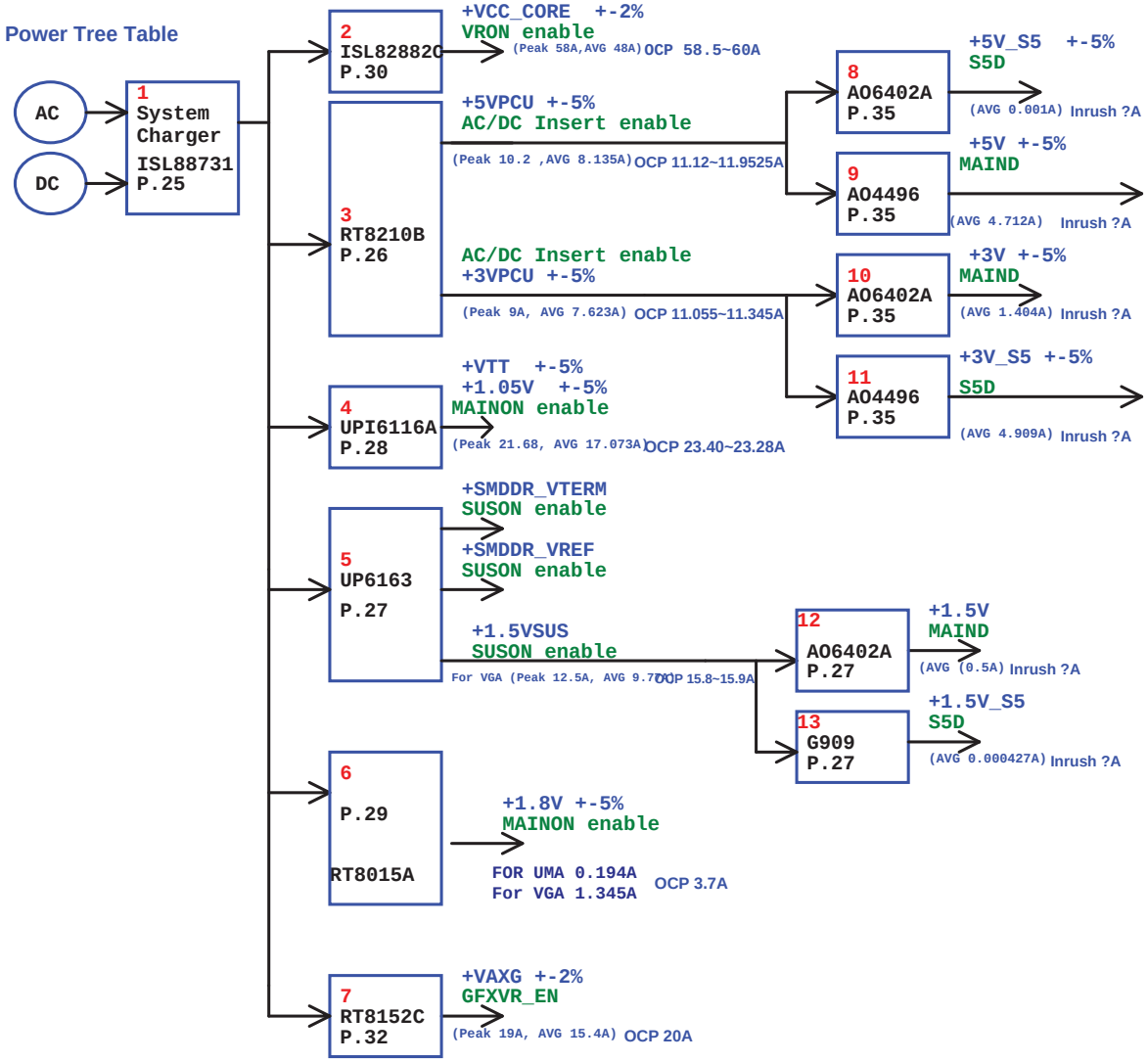
Size	Document Number	Rev
	POWER STAGE AND BOI-FUNCTION	2A

Date: Friday, February 26, 2010 Sheet 33 of 35

Power Tree Table



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Power Tree Table	2A

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Model	REV	CHANGE LIST
TE2 MB	B2A	PAGE(16) : Add BT_EN# for combo RF control for BT
		PAGE(27) : Change DDR S3_1.5V ON circuit.
	C3A	PAGE(07) : Add ESATA re-driver IC
	D3A	PAGE(24) : LED luminance to light,R321、R319 1K-ohm change 2.2K-ohm.
		PAGE(24) : LED luminance too low,R317 560-ohm change 220-ohm.
		PAGE(19) : Add R61,R62,R63,R64 0.1-ohm to avoid speaker burn.
		PAGE(16) : Add Q62 to avoid leakage current.

MODEL TE2

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204					
PROJECT MODEL :	TE2	APPROVED BY:	Mosy Li	DATE:	2009/11/13
PART NUMBER:		DRAWING BY:	Mosy Li	REVISON:	1A

Quanta Computer Inc.
PROJECT : TE2
Size | Document Number: Change list | Rev 2A
Date: Friday, March 19, 2010 Sheet 31 of 35