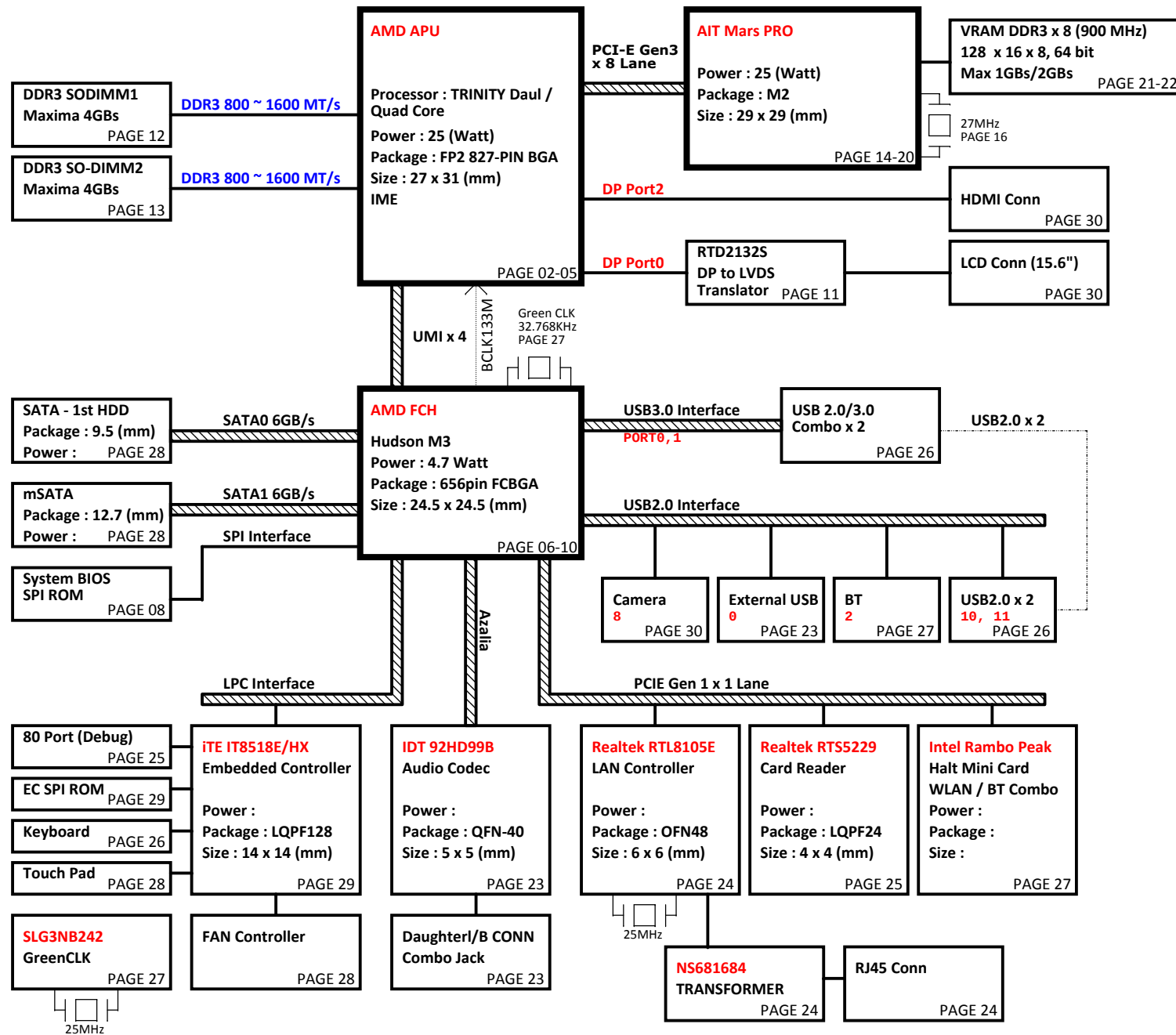


Volks_AMD Comal DIS/UMA (14") Ultra/Slim

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728

System Charge Power (+BATCHG)

G5934RZ1U

System Discharge Power
(+1.5V/+3V/+5V)
(+3VSUSV/+3VLANVCC/+1.1V)

Ricktek RT8223PZ

System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

SL6277/RT8228AZ/AP3407A/ISL6208BCRZ

Processor Power (+VCC_CORE/
+1.2V/+2.5V/+VDDNB_CORE)

Richtek RT8207L

System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

Richtek RT8228AZ

PCH Power (+1.1VS5)

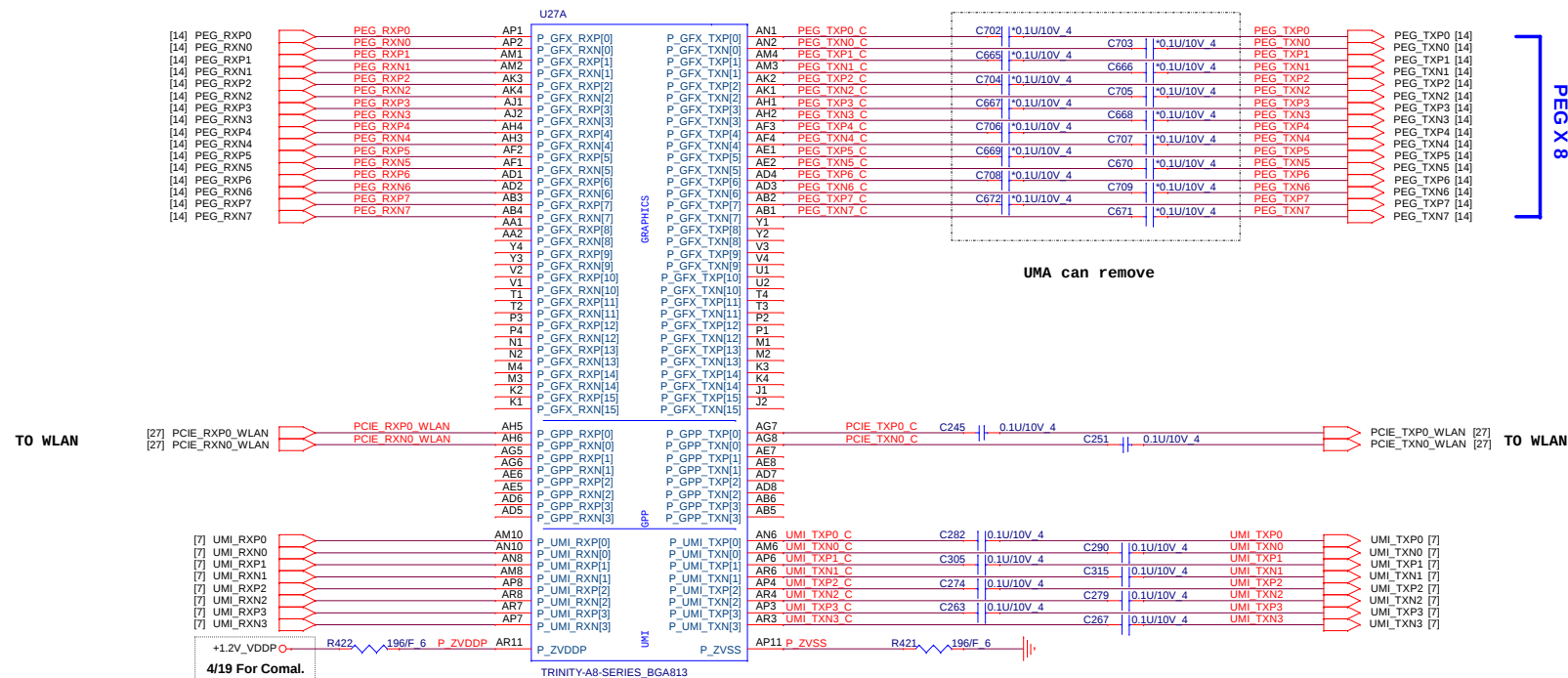
RT8152E/G5193/G5193R41U/NB650

DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/
+1.5V_VGA/+1.8V_VGA/+VDDCI)

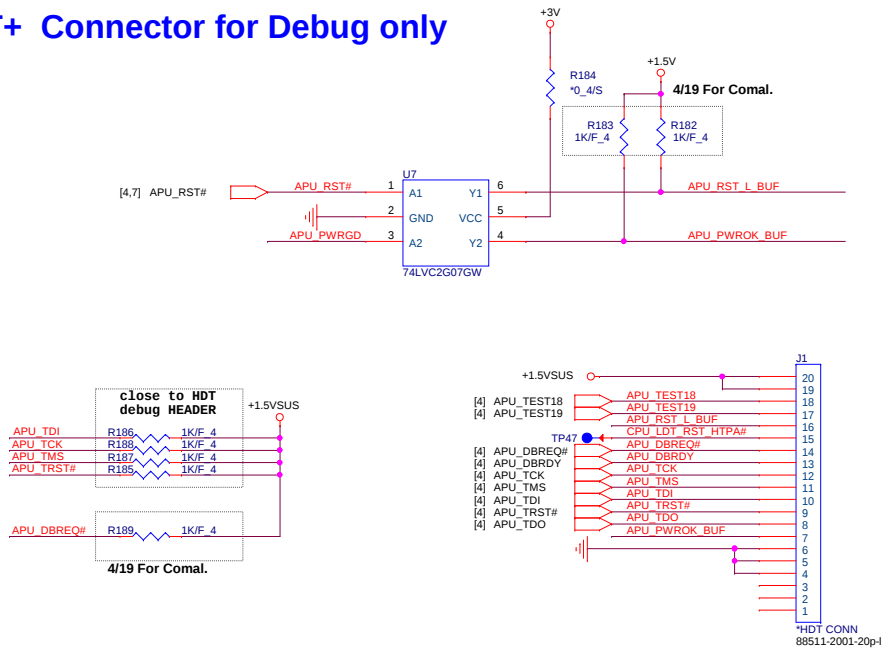


PROJECT : VOLKS_Coma1 14"
Quanta Computer Inc.

Size A3	Document Number Block Diagram	Rev 1A
Date: Thursday, September 20, 2012 Sheet		1 of 42

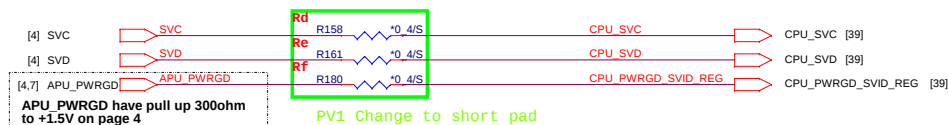


HDT+ Connector for Debug only

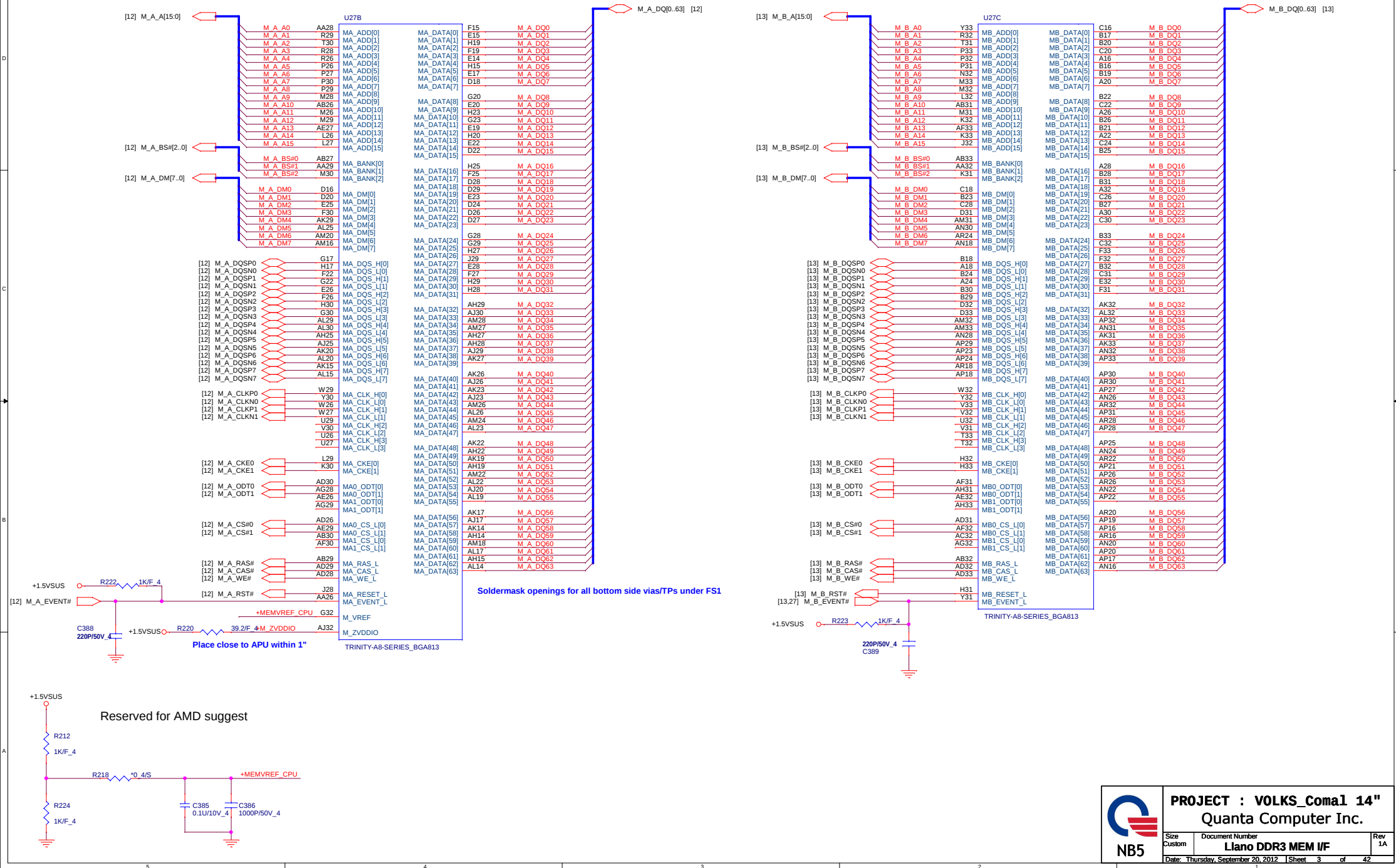


VID Override Circuit

Note:
To override VID, Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.



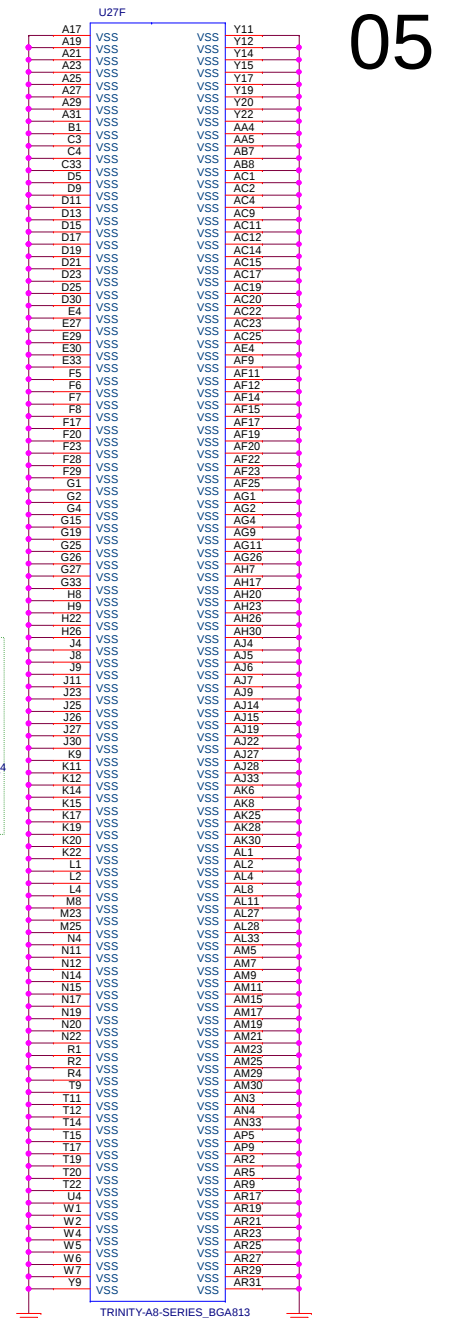
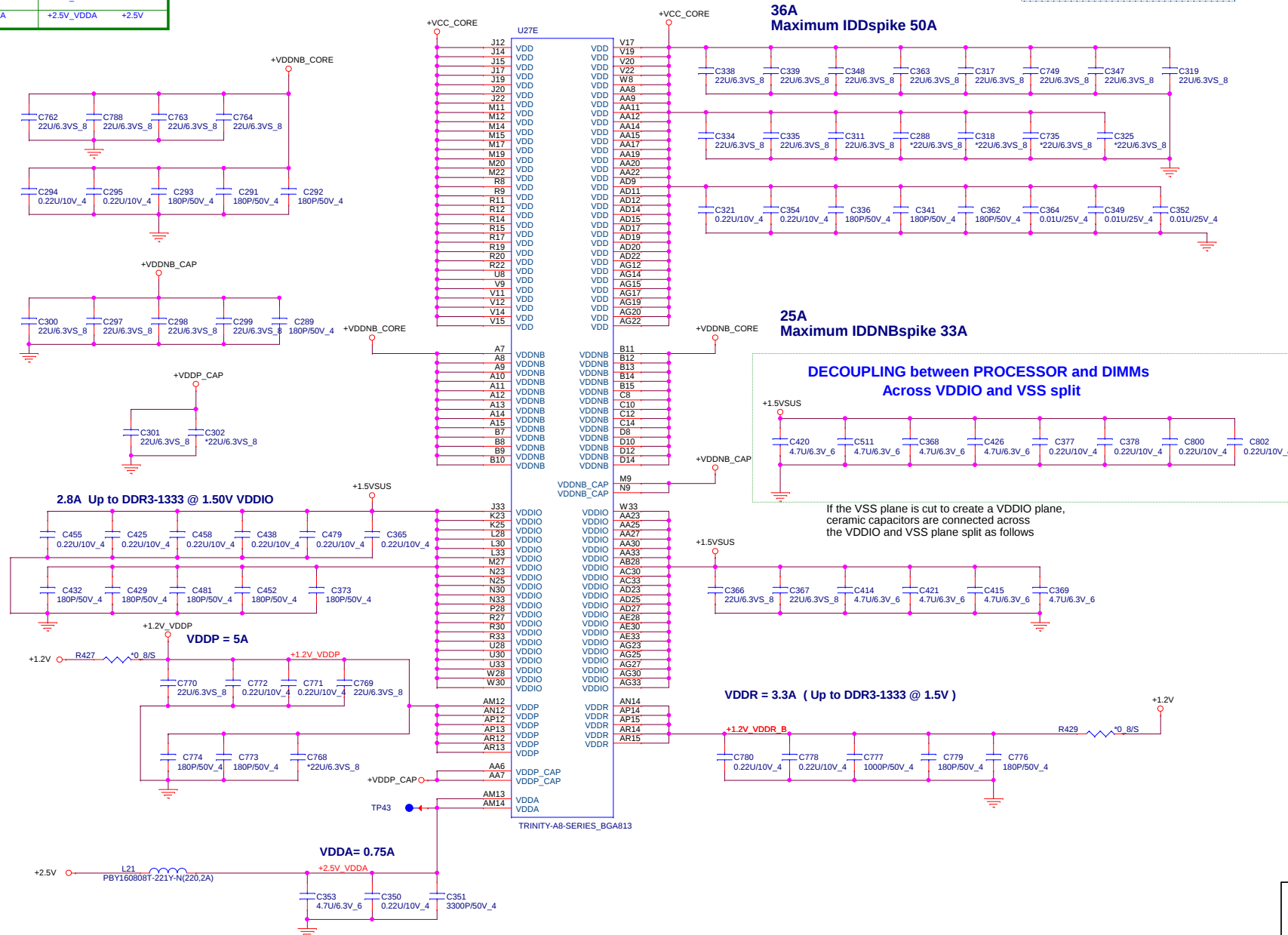
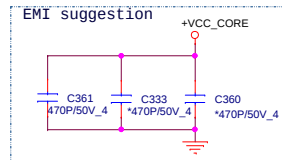
BOOT VOLTAGE			
SVC	SVD	VFIX_+VDD =VCC/6ND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



Rev
14

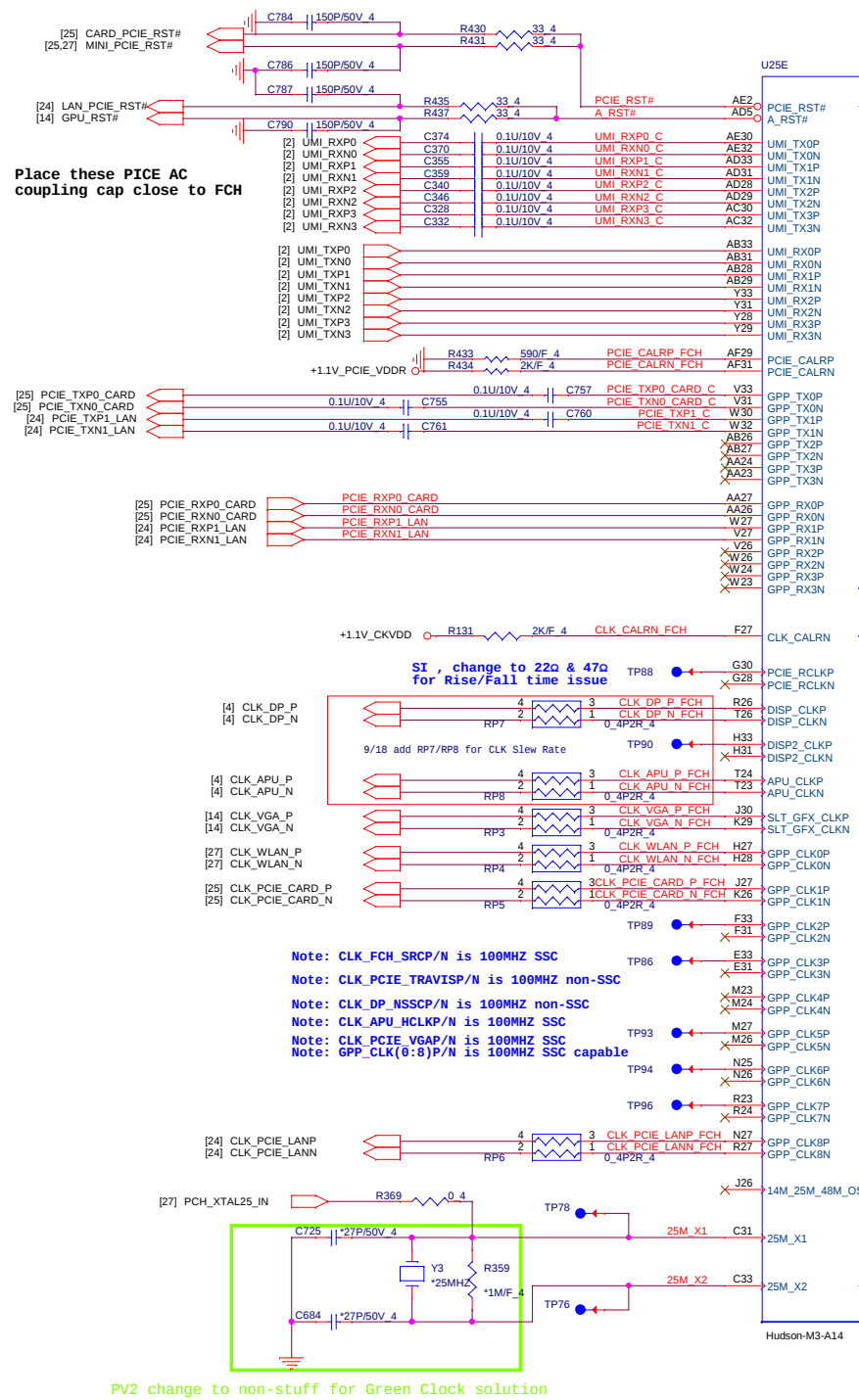
APU POWER TABLE

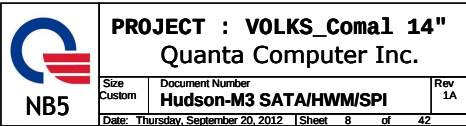
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V





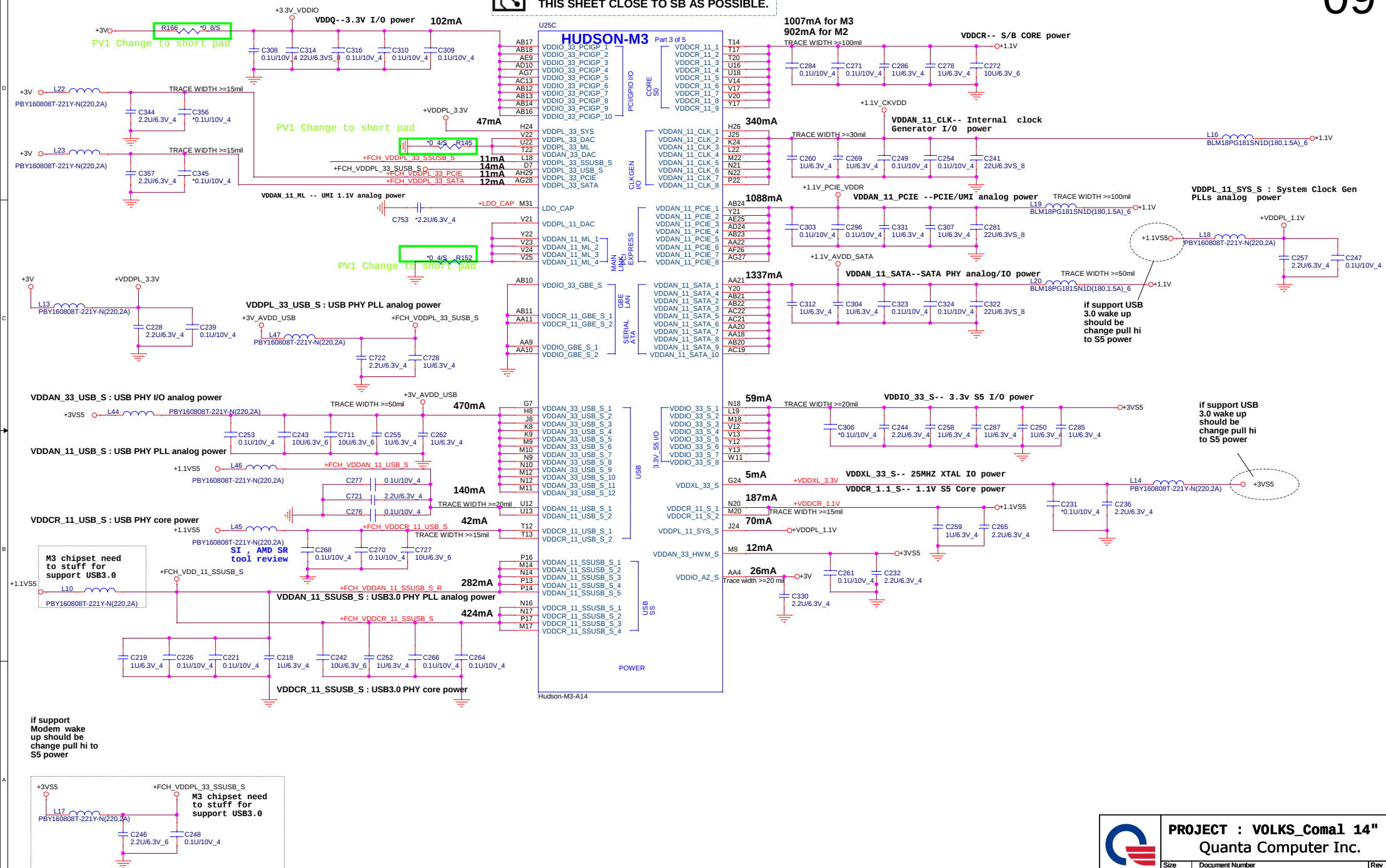
Place these PICE AC coupling cap close to FCH





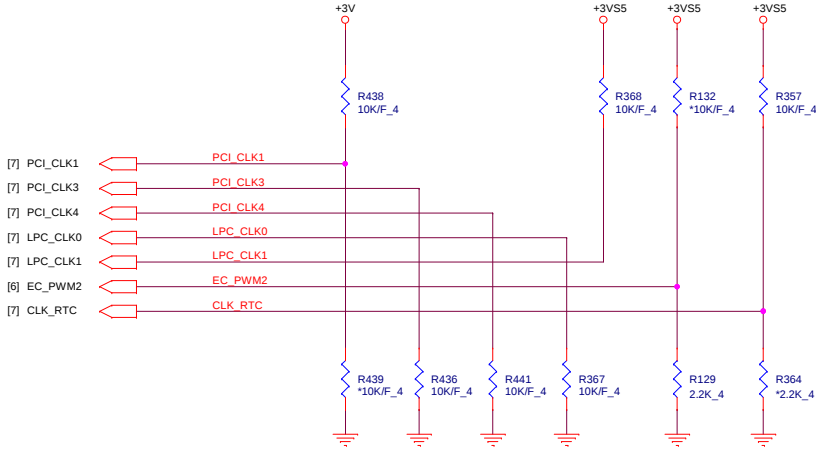


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

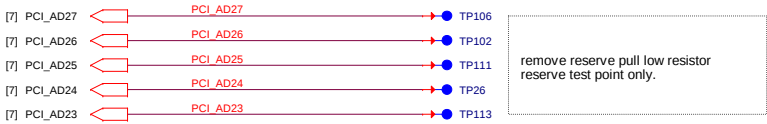


REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

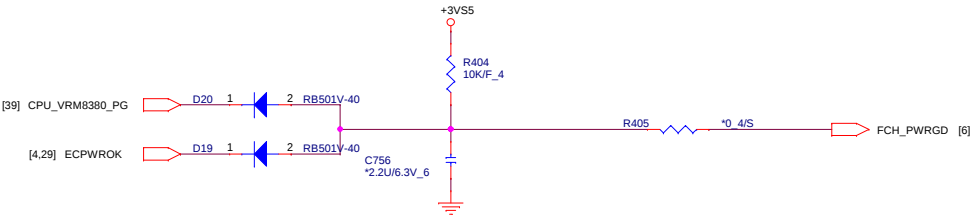
DEBUG STRAPS

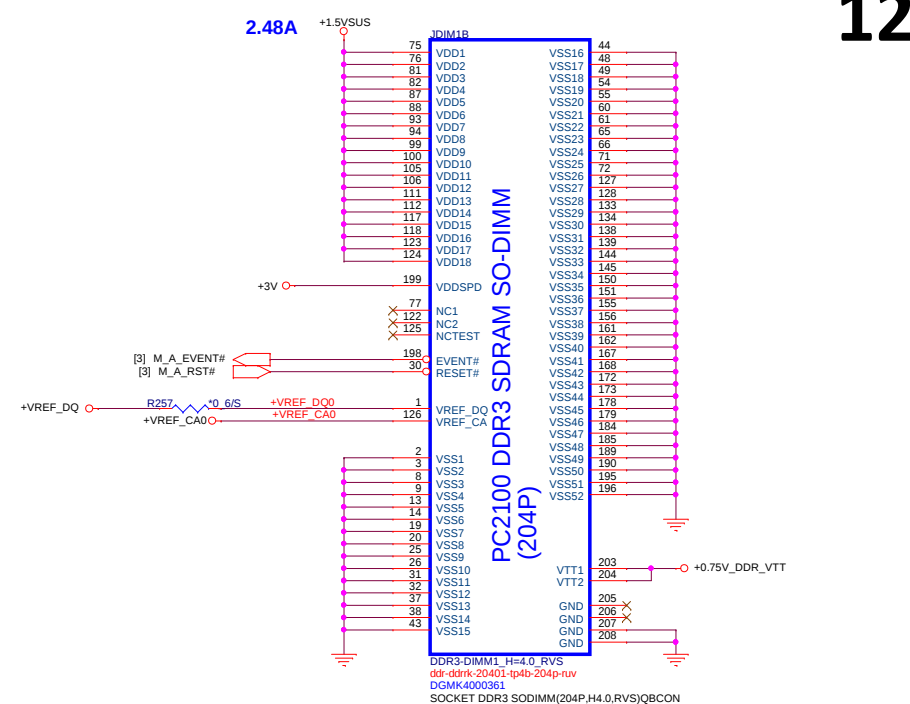
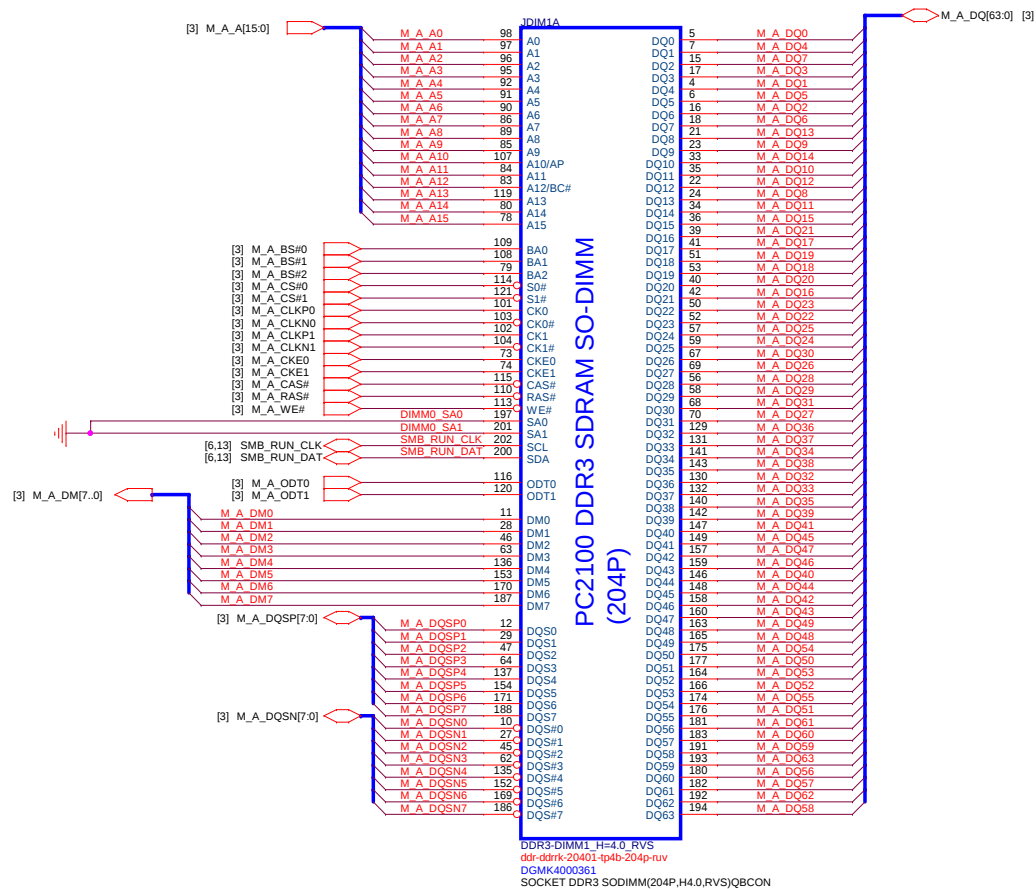
FCH has 15K Internal Pull Up for PCI_AD[27:23]



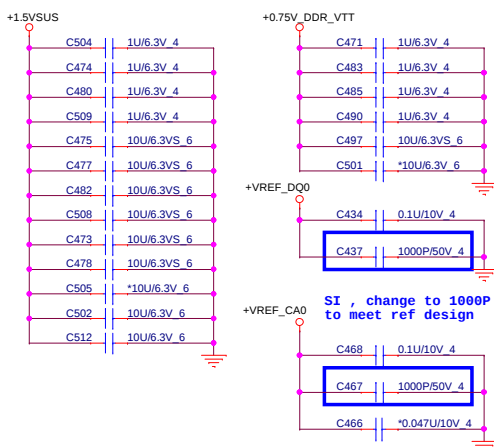
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH_PWRGD

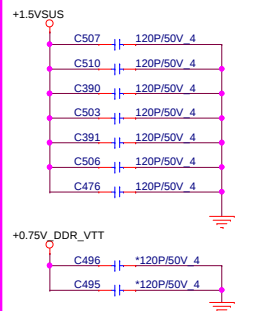




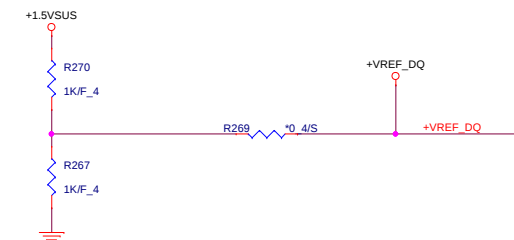
Place these Caps near So-Dimm0.

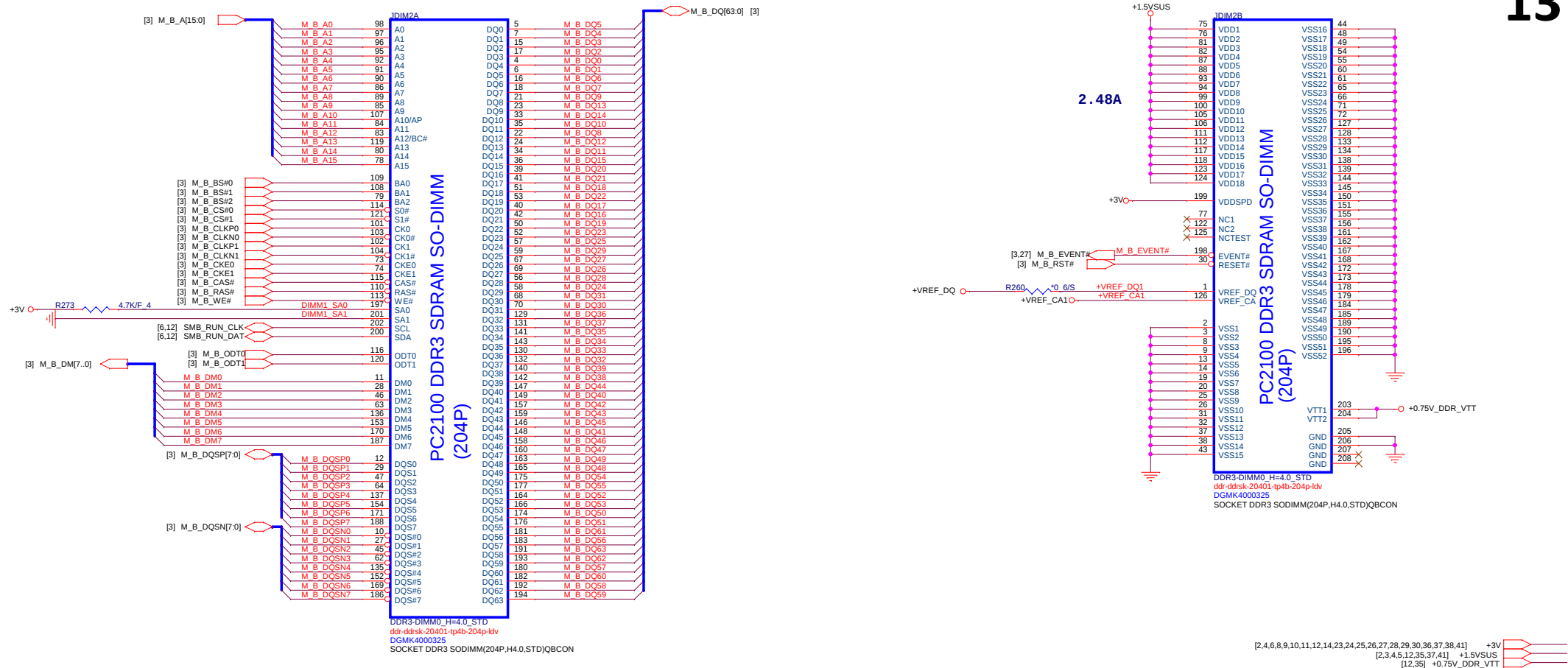


For EMI RESERVE



Reserved for AMD suggest

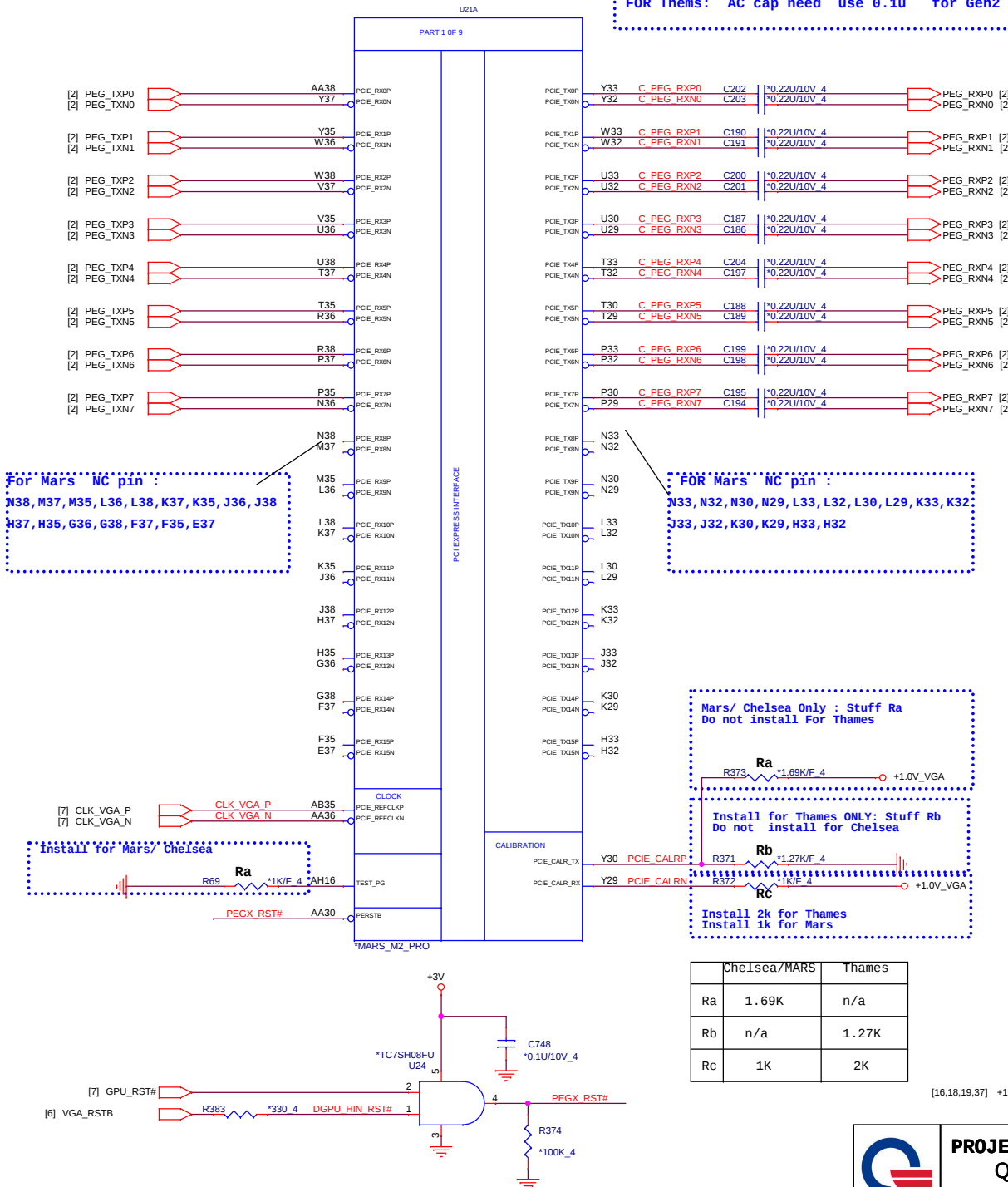




Place these Caps near So-Dimm1.

For EMI

FOR Mars support Gne3: AC cap nees use 0.22u
FOR Them: AC cap need use 0.1u for Gen2

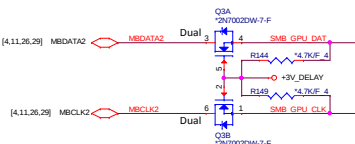
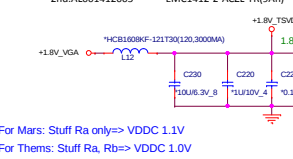


PROJECT : VOLKS_Coma1 14"
Quanta Computer Inc.

Size Custom Document Number Mars_PCIE_interface Rev 1A
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GPI030 GPI012 GPI016 GPI020 GPI015 Thames XT

The schematic diagram illustrates the +3V_DELAY supply rail. It begins with a +3V_DELAY source connected to a series of resistors: RS3, RS2, R79, RB9, RB8, RI04, and RB1. Each resistor is labeled with a value of 10KΩ. The rail then branches out to various components: GPID_23_CLKREQ, DGPU_PRODCHOTF, GPCOR_R70, DGPU_TBSTB, DGPU_TDR, DGPU_TMS, and DGPU_TCK. A ground symbol is shown at the bottom right.

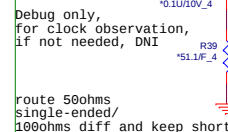
[illegible]

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: FOR ThemS: La, LB: :
 : CX8PG471000/BLM18PG471\$N1D/1A_6

For Thems: La, Lb:

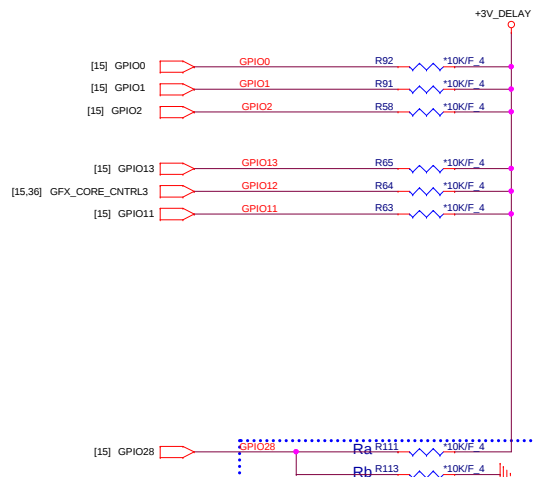
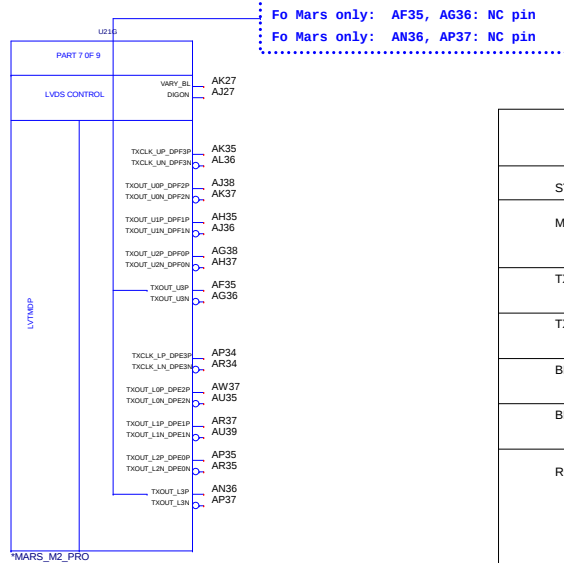
CX8PG471000/BLM18



The diagram shows two input signals, CLKTESTA and CLKTESTB, connected to a clock divider circuit. The circuit consists of two parallel branches. The first branch contains a resistor R39 (51.1F_4) in series with a capacitor C62 (0.1U/10V_4). The second branch contains a resistor R45 (51.1F_4) in series with a capacitor C69 (0.1U/10V_4). Both branches are connected to ground. The output of the circuit is labeled 'Debug only, for clock observation, if not needed, DNI'.

route 50ohms
single-ended/
100ohms diff and keep short





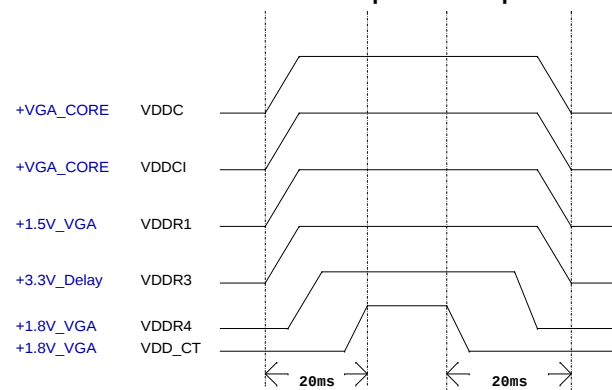
Memory Aperture size:

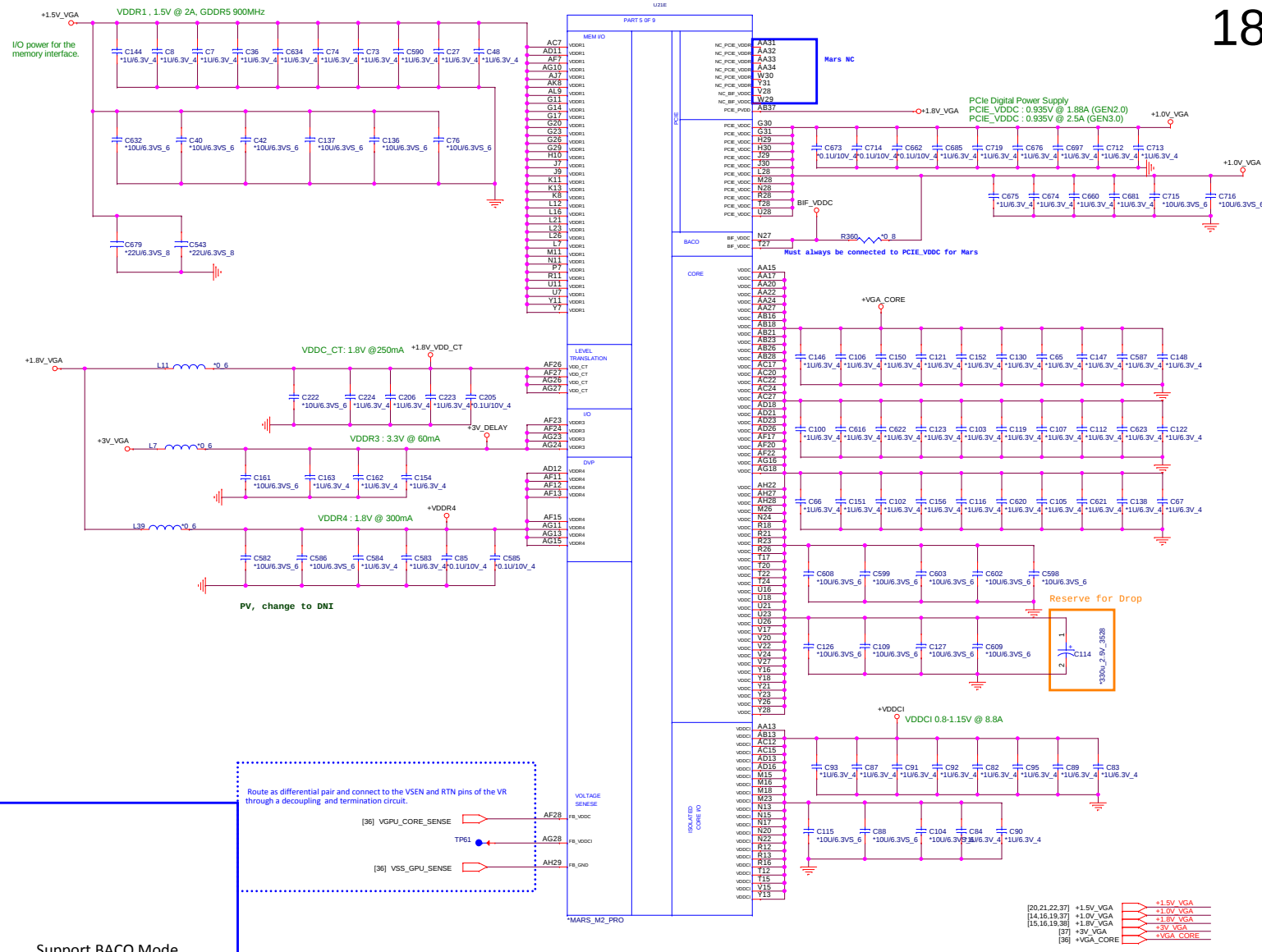
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS -- SEE EACH DATABASE FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (SD) 101 - 1Mbit M25P10A (SD) 101 - 2Mbit M25P20 (SD) 101 - 4Mbit M25P40 (SD) 101 - 8Mbit M25P80 (ST) 101 - 512Kbit Fm25LV512 (Chingis) 101 - 1Mbit Fm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, it is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] PS_3[4] PS_0[5]	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Power Up/Down Sequence

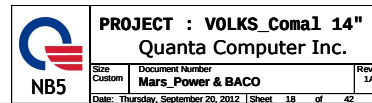


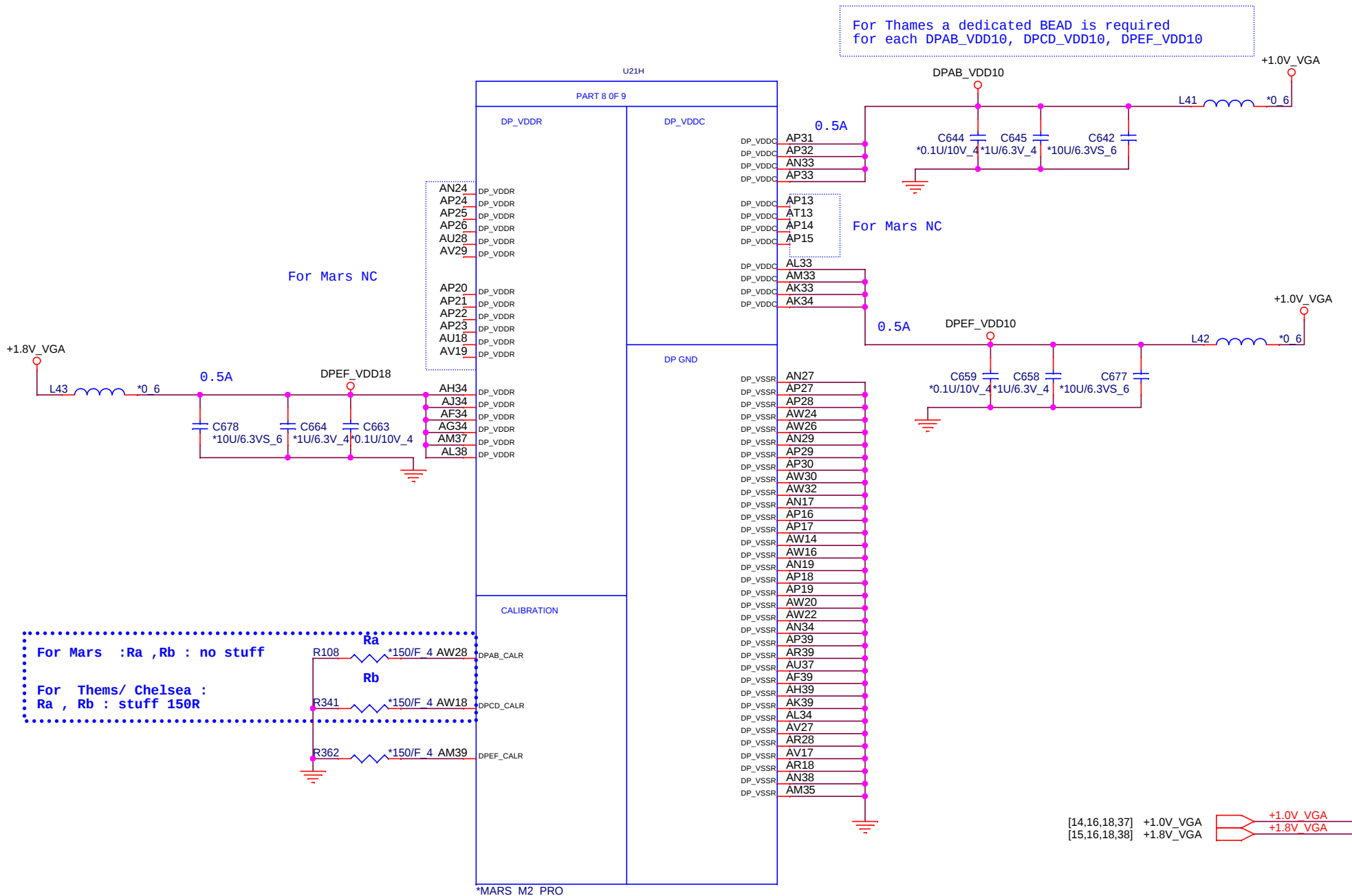


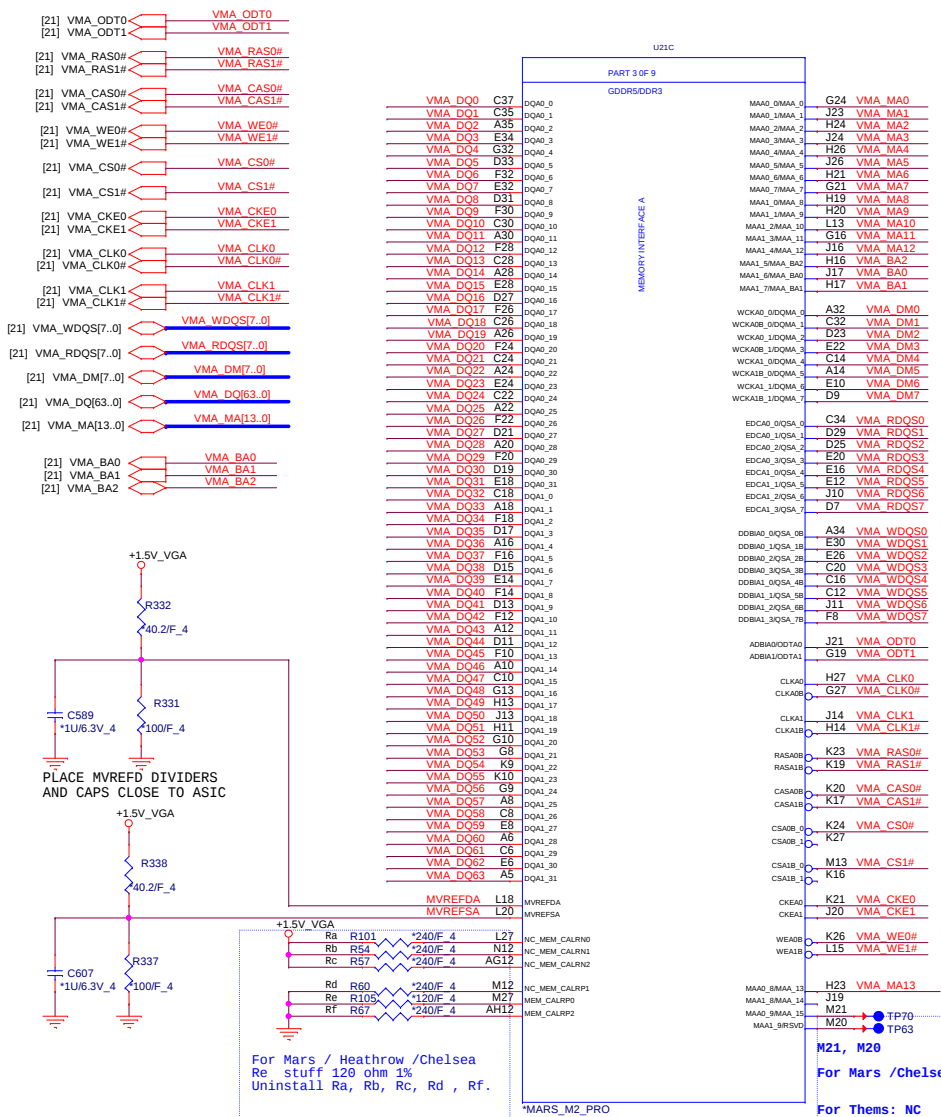
Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

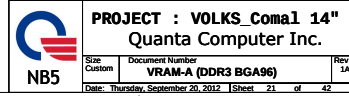
2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE



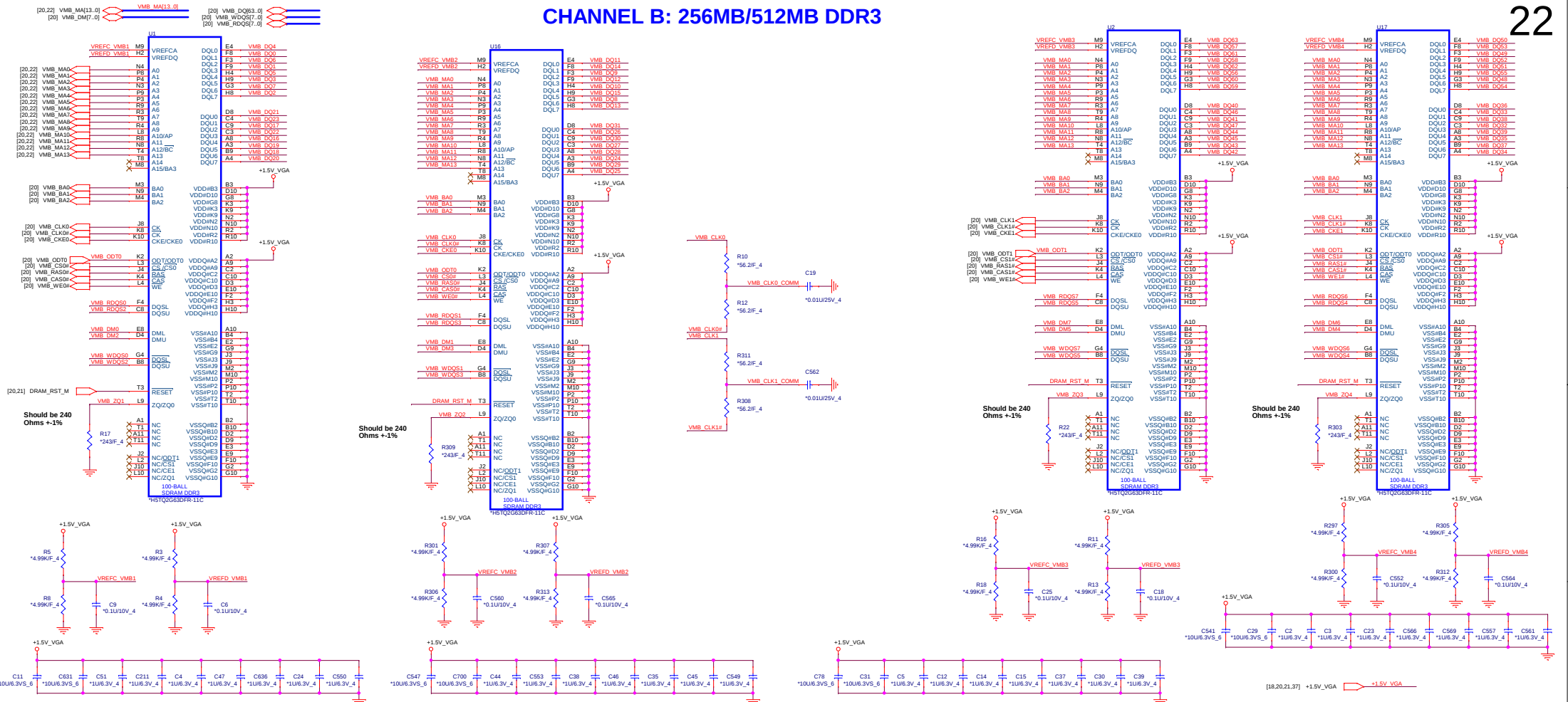


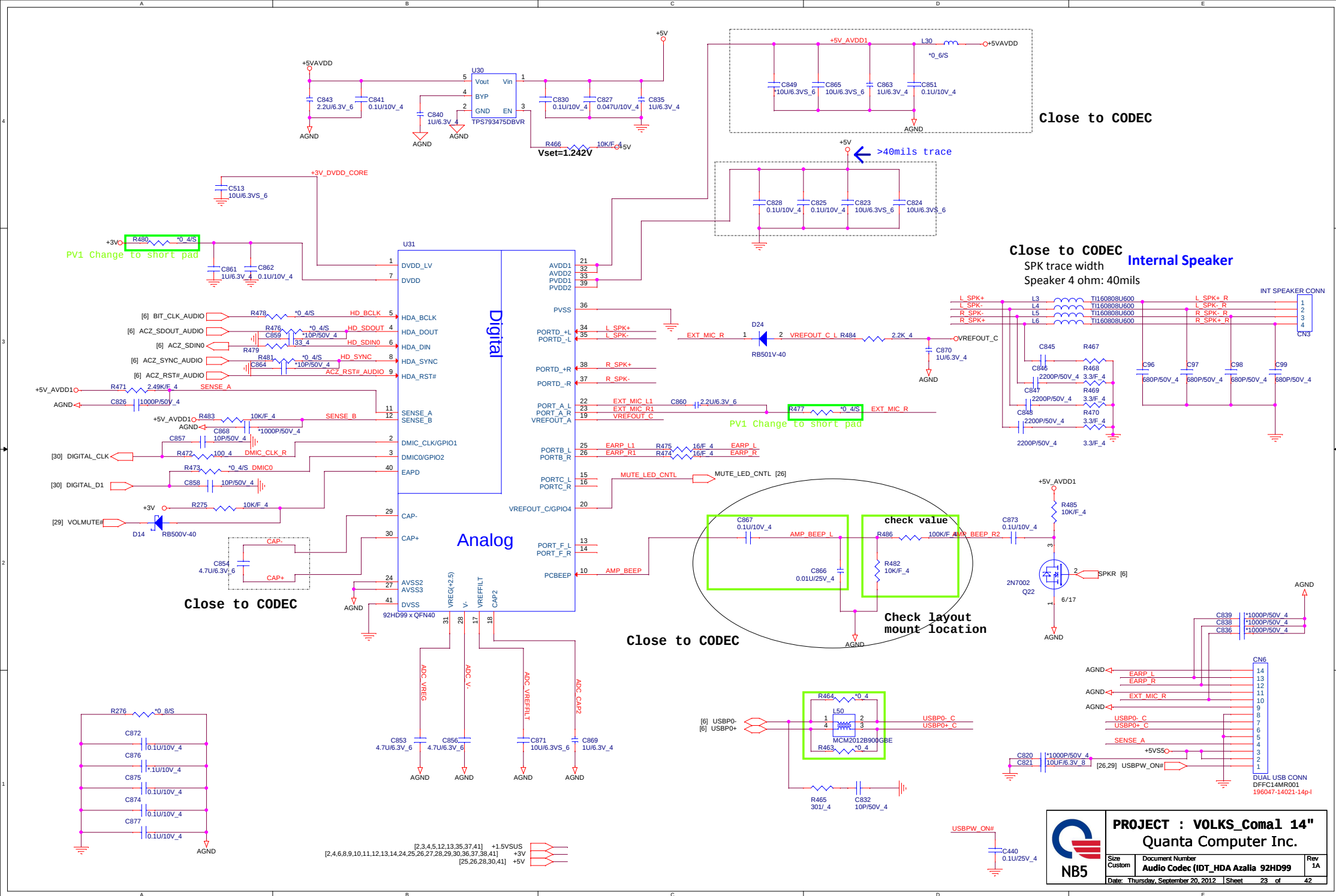


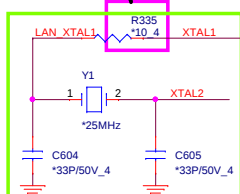


CHANNEL B: 256MB/512MB DDR3

22





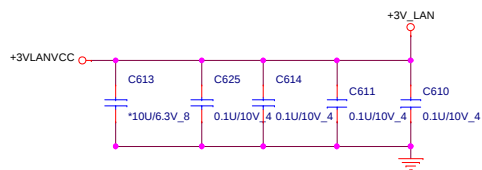
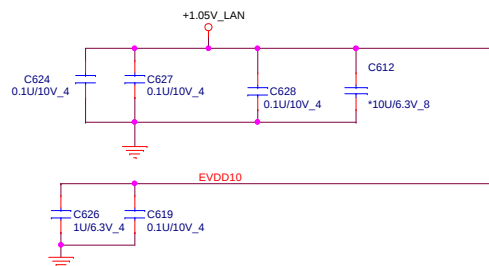
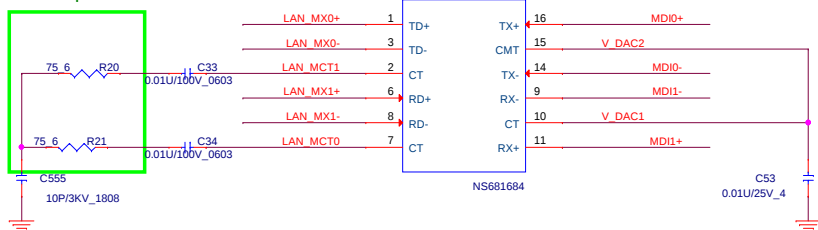
For EMI $\theta \sim 22 \text{ ohm}$ 

PV2 change to non-stuff for Green Clock solution

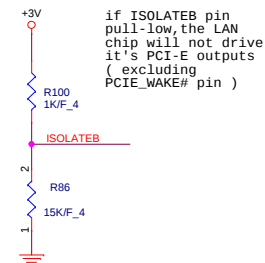
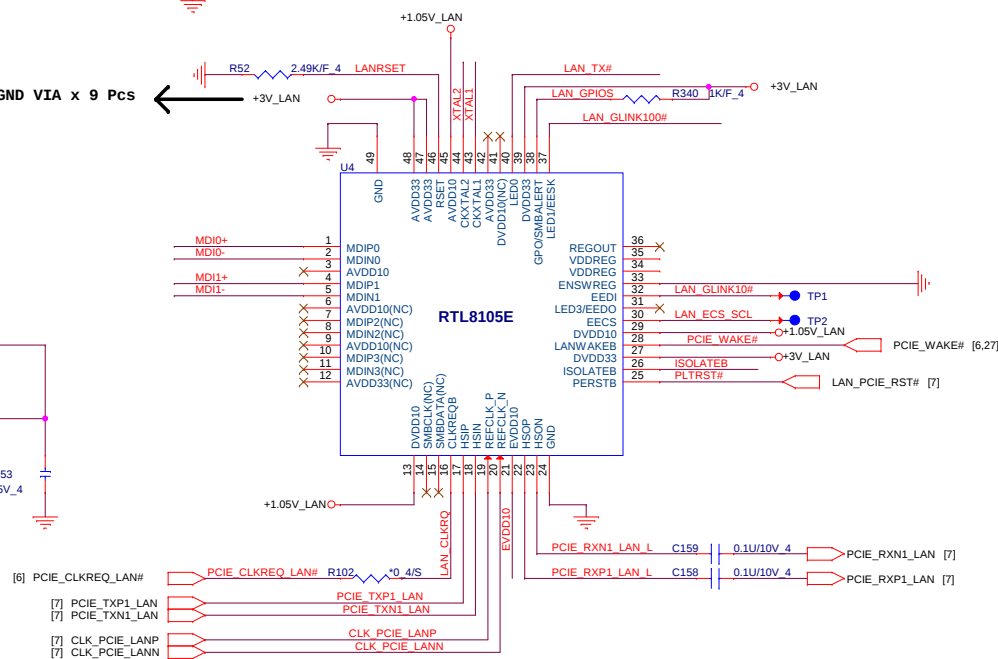
Green Clk

[27] LAN_XTAL25_IN R336 510/F_4 XTAL2
PV2 change to stuff for Green Clock solution

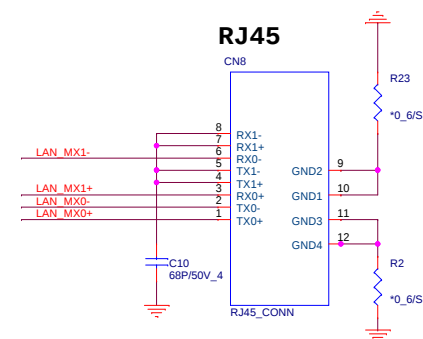
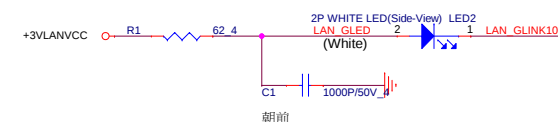
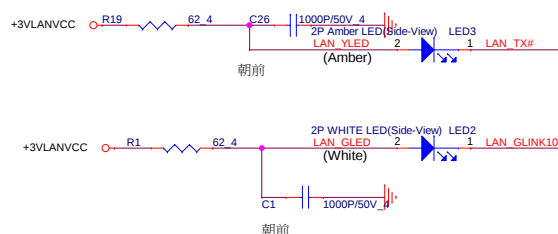
Change to 0603 size for EMI request



GND VIA x 9 Pcs

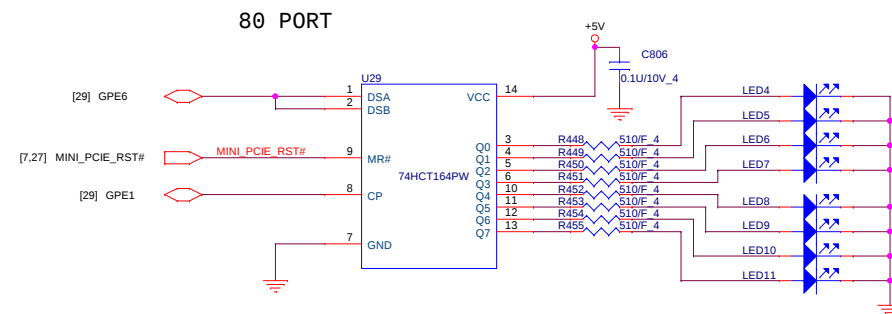
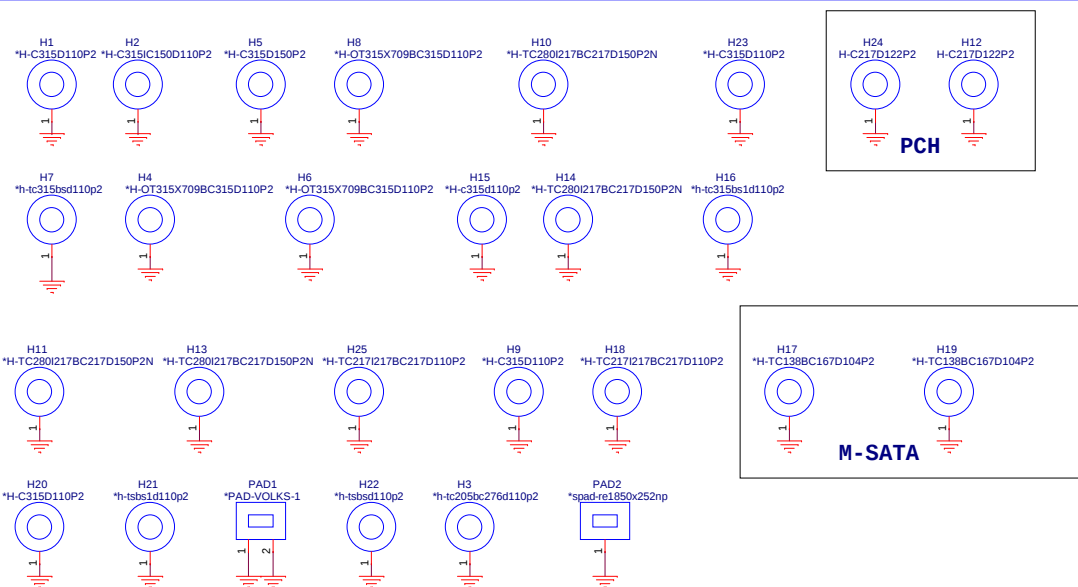
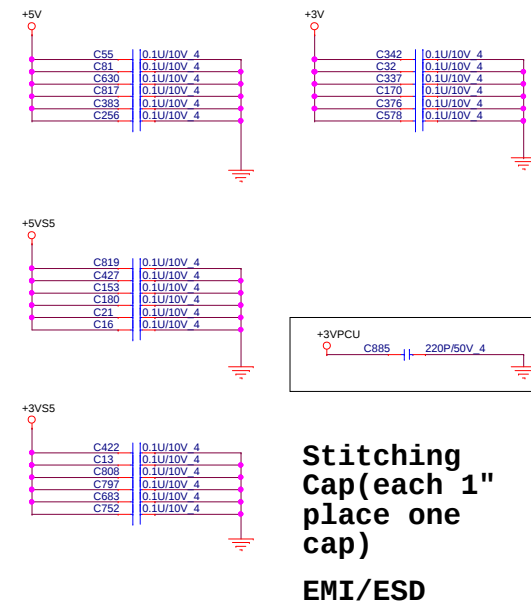
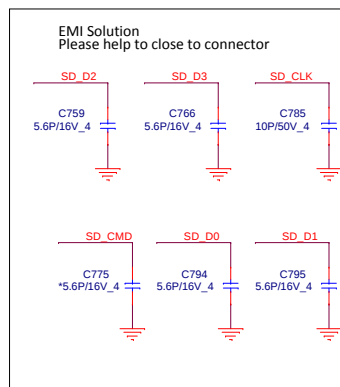
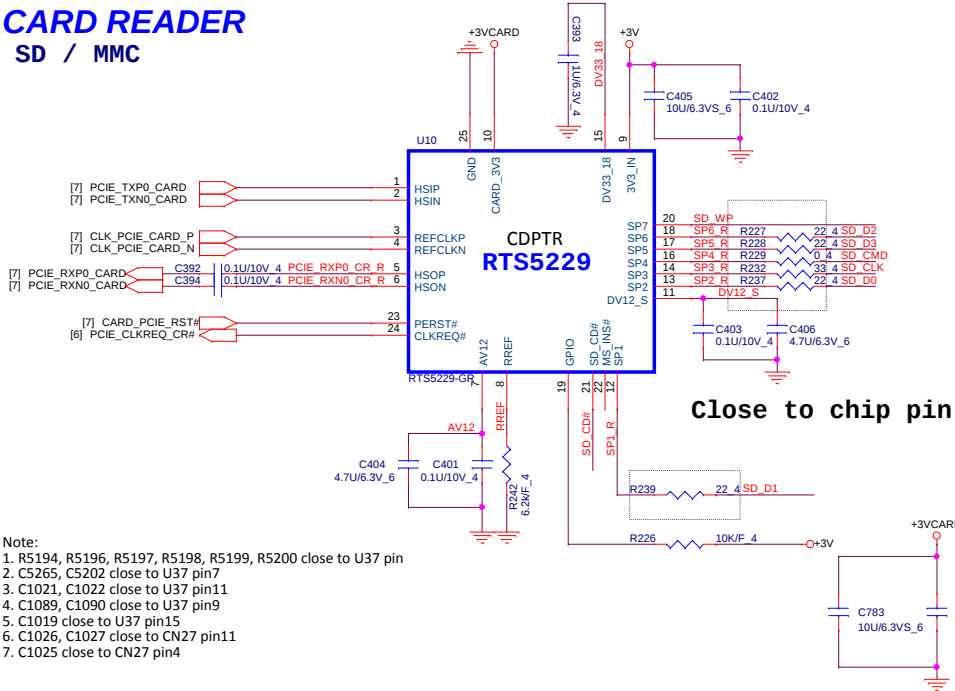


if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)



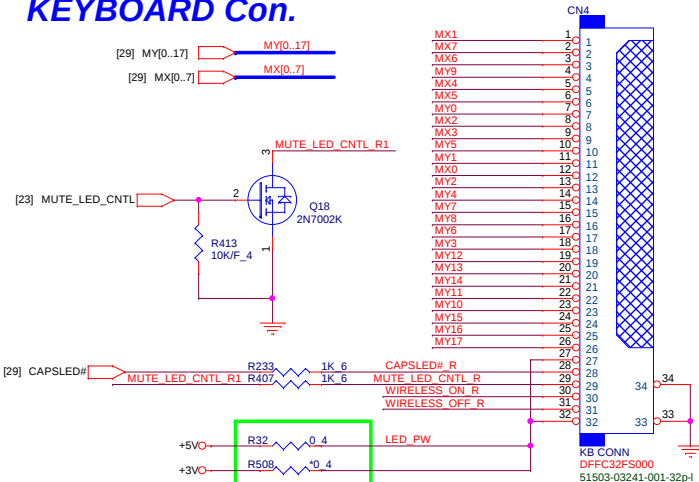
CARD READER

SD / MMC



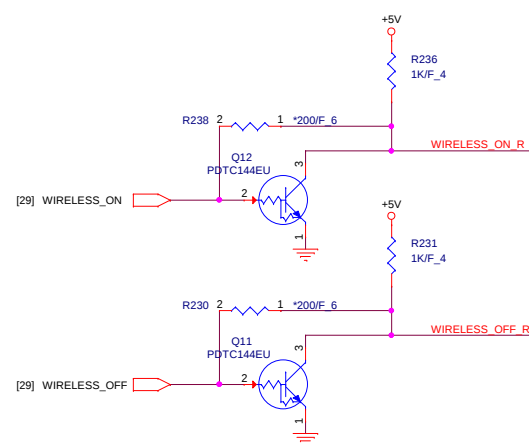
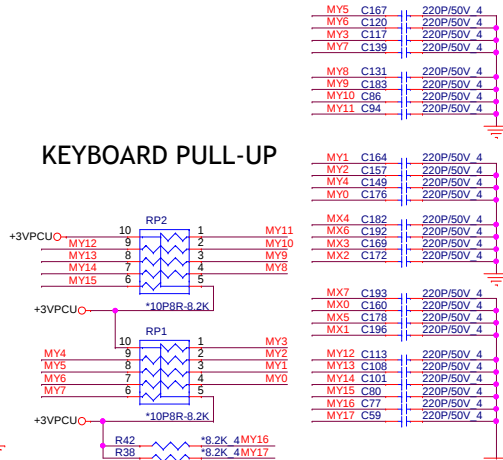
KEYBOARD Con.

26

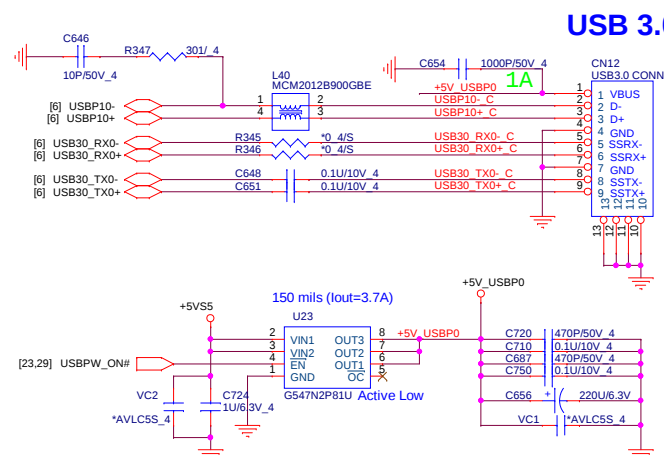
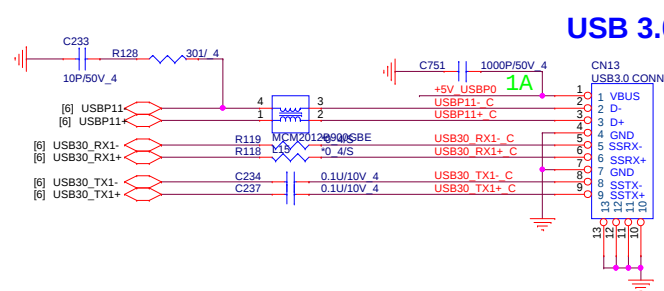
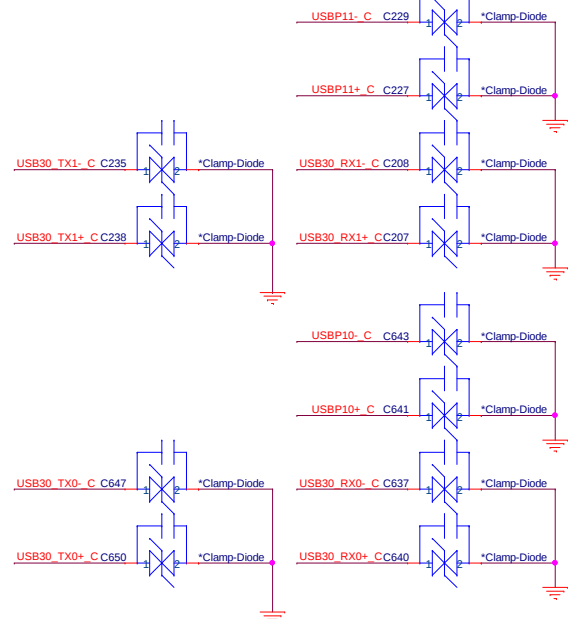


PV2 Change solution to same as U52

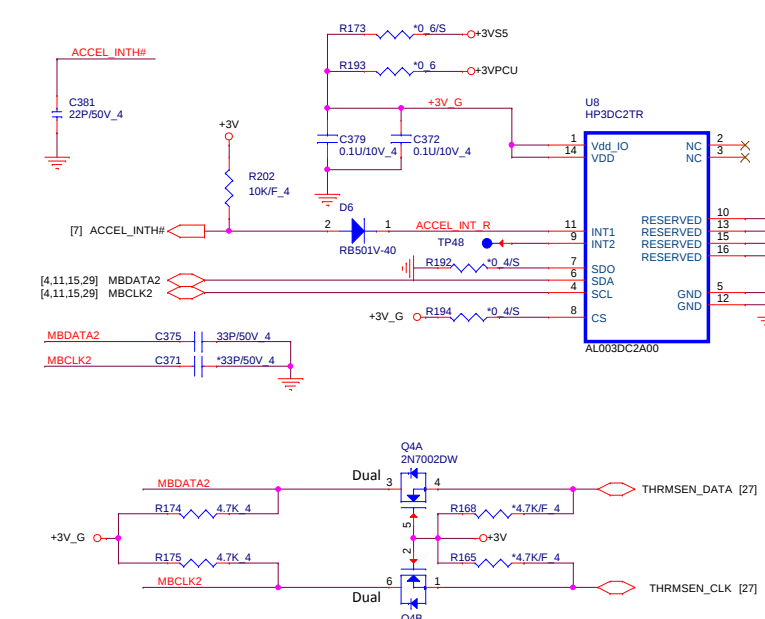
KEYBOARD PULL-UP



USB 2.0/3.0 Combo



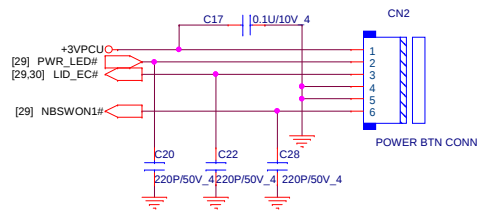
Accelerometer Sensor



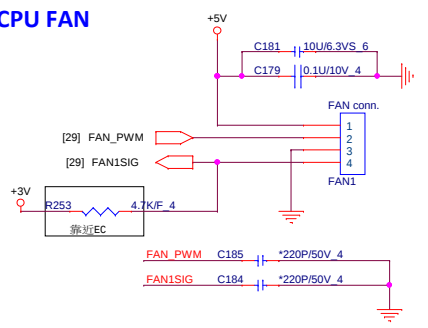
			PROJECT : VOLKS_Coma1 14" Quanta Computer Inc.		
Size	Document Number	Rev			
Custom	USB 3.0/KB/Green CLK	1A			
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Power Button Connector

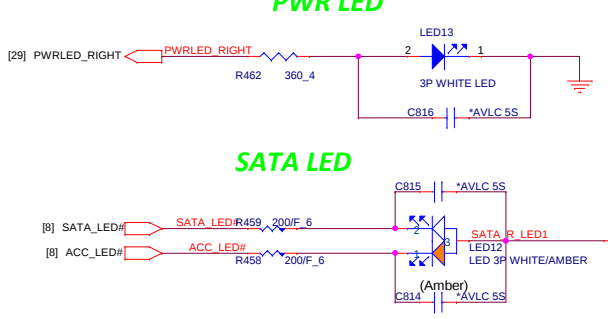
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



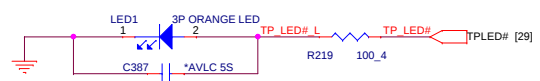
CPU FAN



LED Status

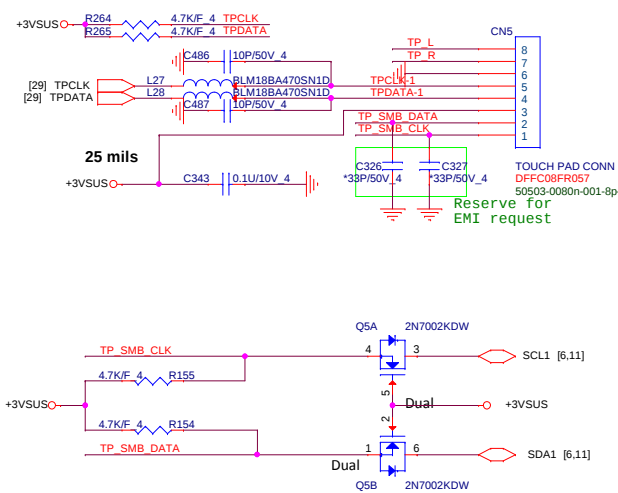
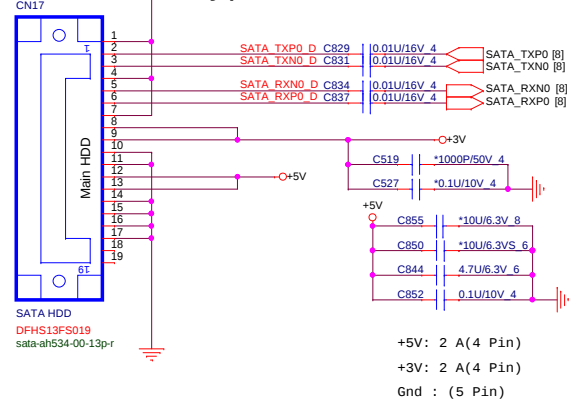


14 "TP LED

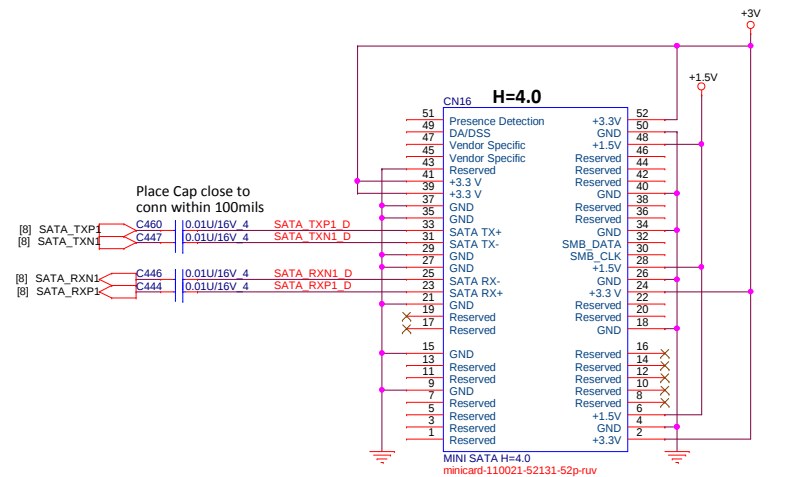


SATA HDD Connector(Cable type)

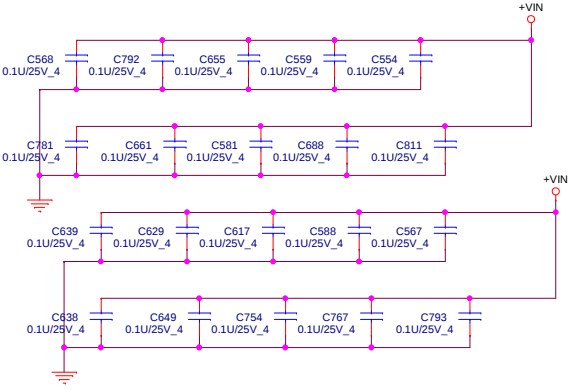
Bypass CAP close conn



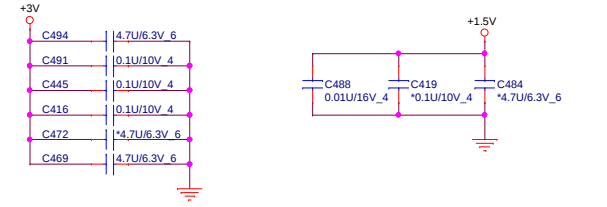
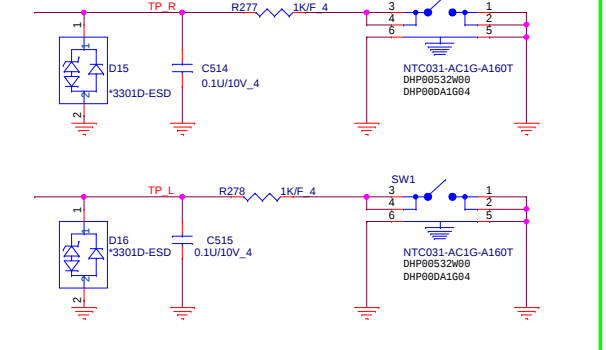
Mini PCI-E Card 2- Full size mSATA



+VIN Cap



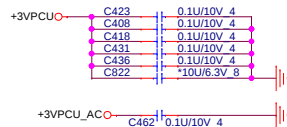
TP for 14"



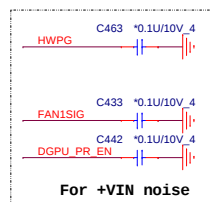
PROJECT : VOLKS Coma1 14"
Quanta Computer Inc.

Size Custom	Document Number SATA HDD/ODD/MSATA CONN	Rev 1A
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default
it
mode



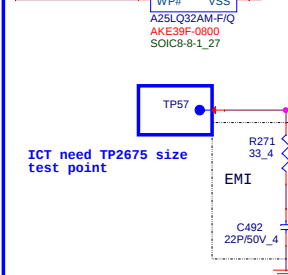
+3VPCU CAP close to EC pin



For +VIN noise

Vender	Size	P/N
PME	4M	AKE39ZN0500
GGD	4M	AKE39GN0Q00
AMC	4M	AKE39F-0800
Socket		DFHS08FS023

U13	
BIOS_CS#	1
BIOS_SPI_CLK I	6
BIOS_WR#	5
BIOS_RD#	2
SPI_3P	3
CE#	VDD
SCK	
SI	
SO	HOLD#
WP#	VSS



ICT need T
test point

For GPU thermal
for Battery
charge/discharge
for CPU thermal

from power button

[illegible]

lay for
request

lay for
request

0424 Fix PWR_LED

Adapter select

+3V/PCU

R268 10K/F 4 GPIO42 R263 10K/F 4

Hi ==> DIS/SG
Low ==> UMA

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

Hi ==> DIS/S
Low ==>UMA

Platform model	GPI042	adapter
SG/DIS	High	90W
UMA	Low	65W

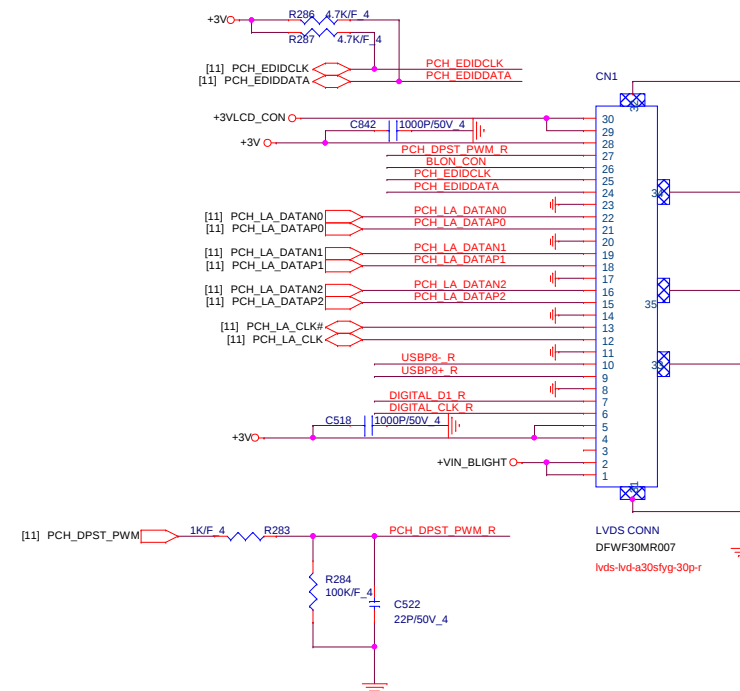
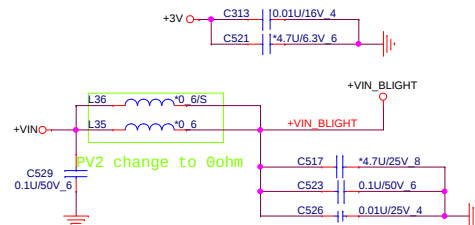
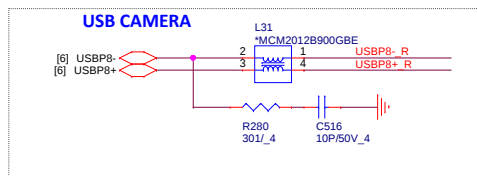
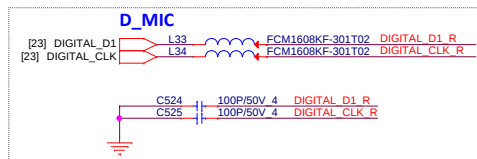
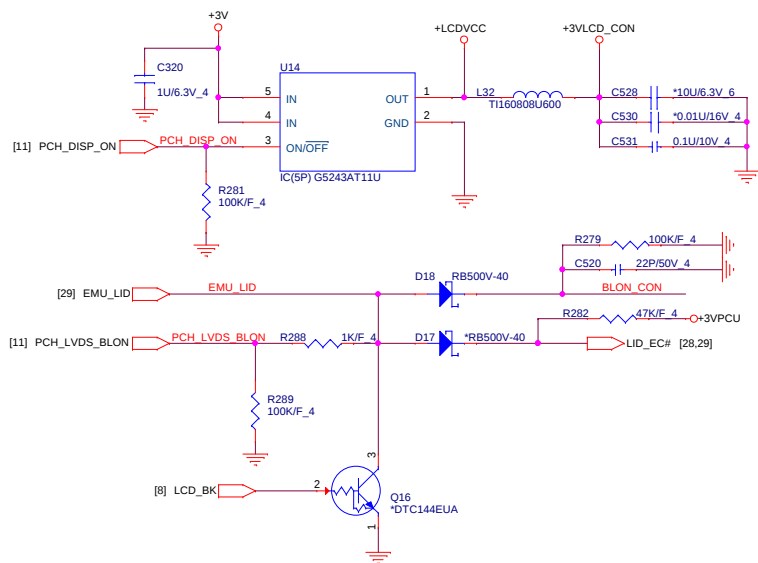
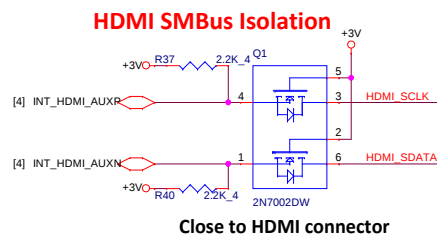


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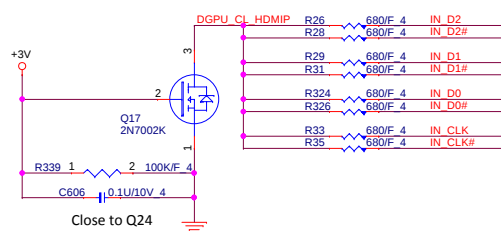
Size Custom	Document Number EC (KB3926)/ROM	Re
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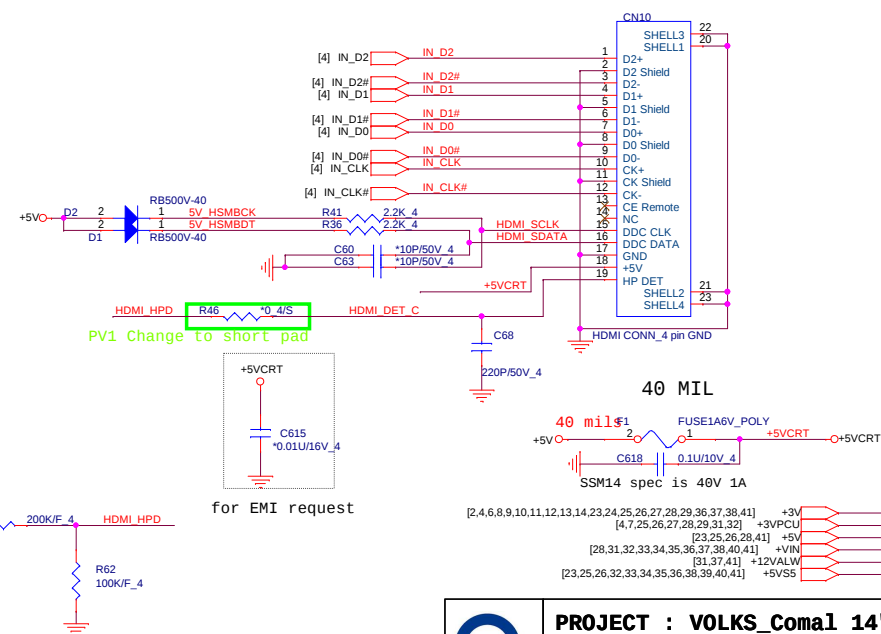
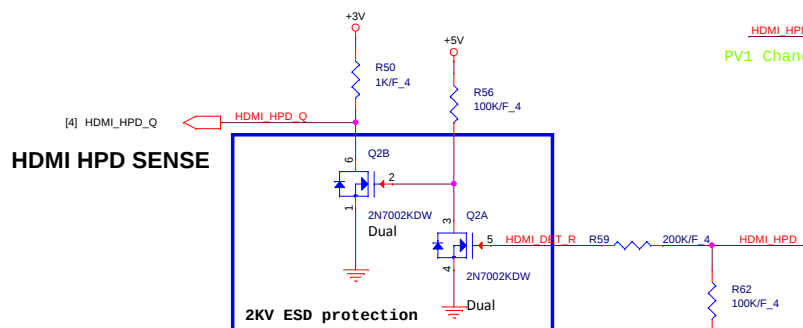
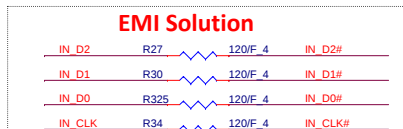
LVDS Conn.

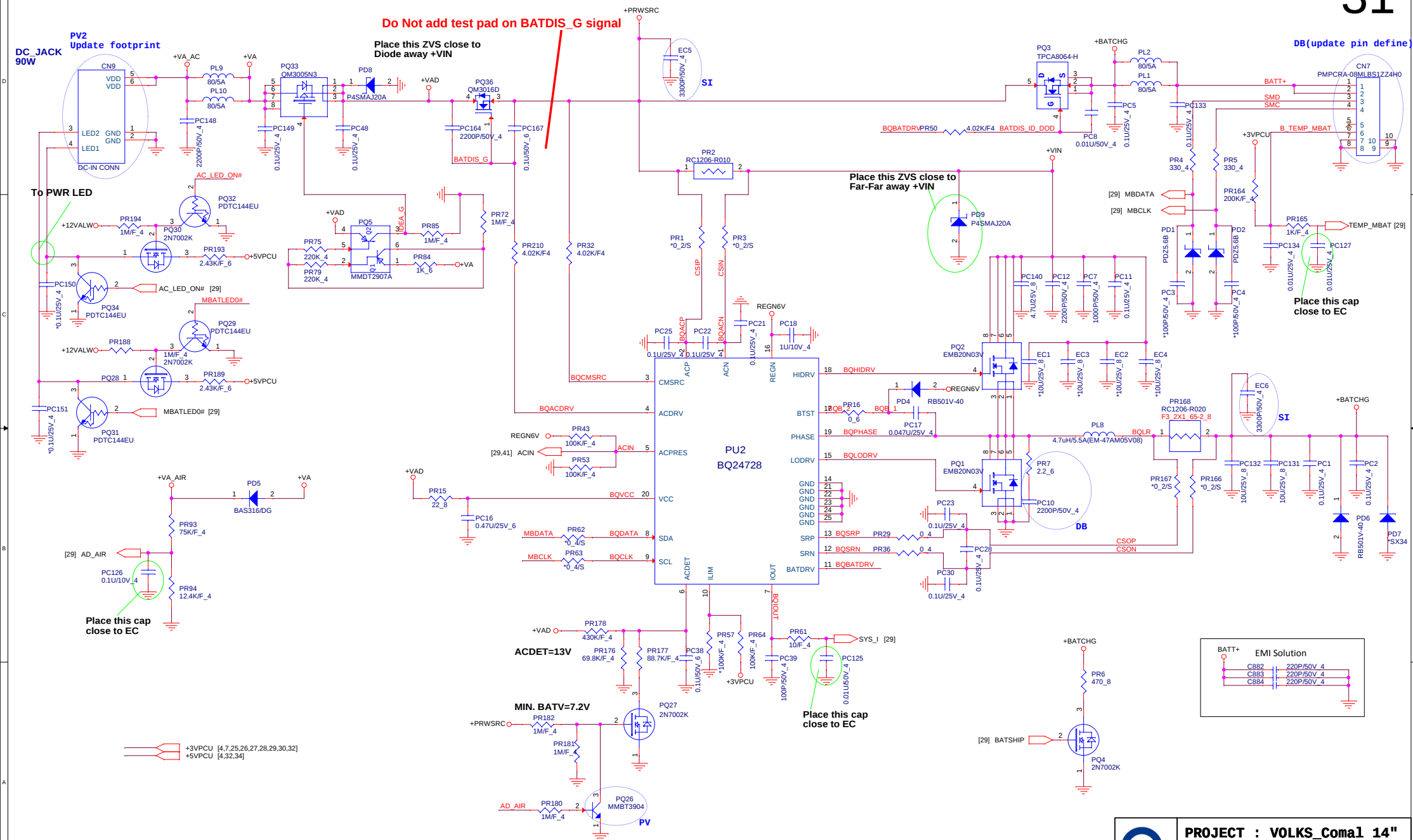
**HDMI Conn.**

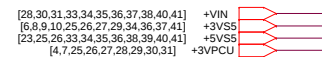
Close to HDMI connector

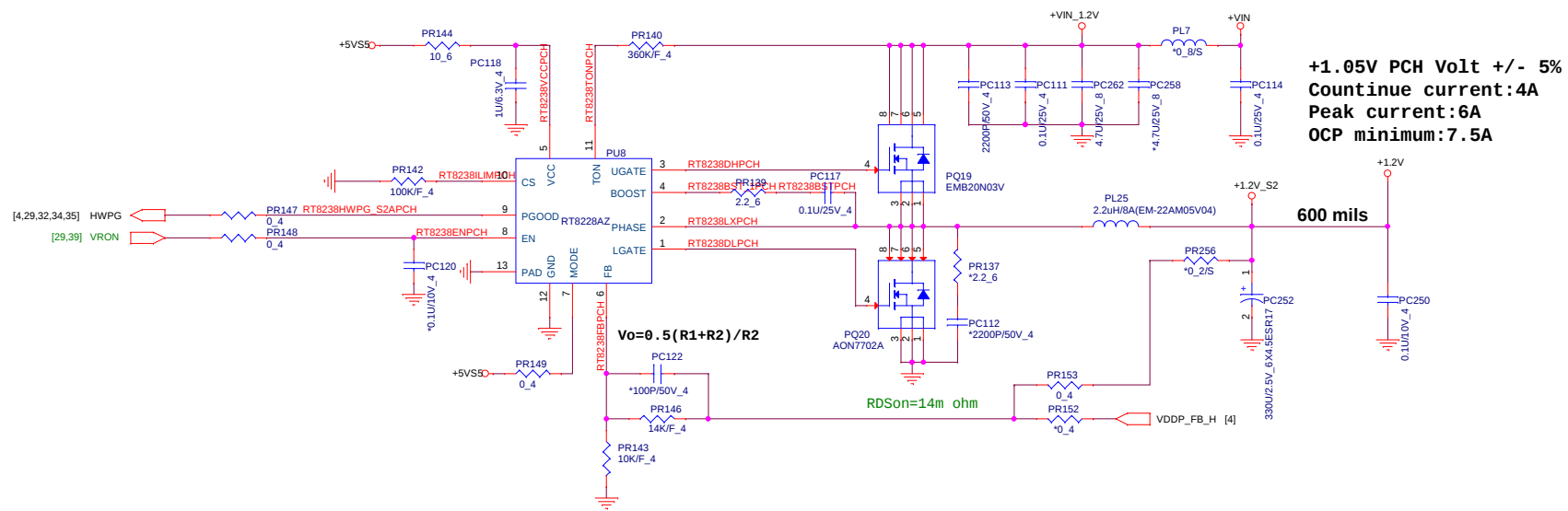


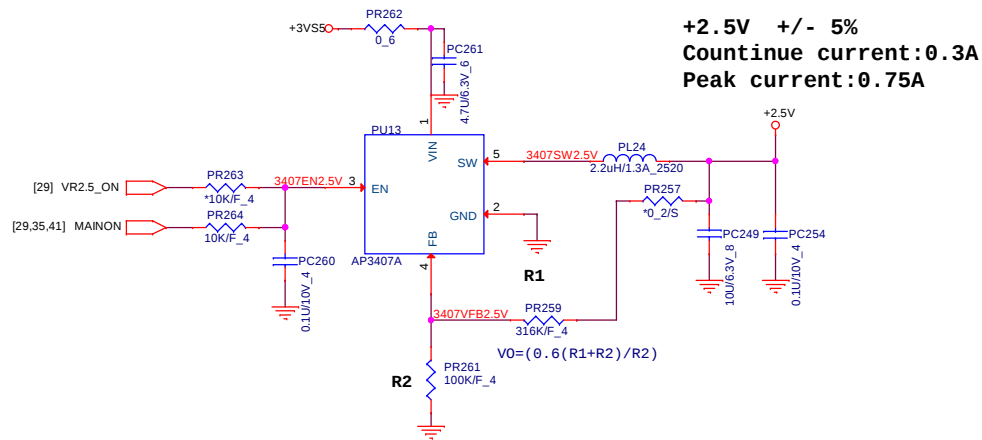
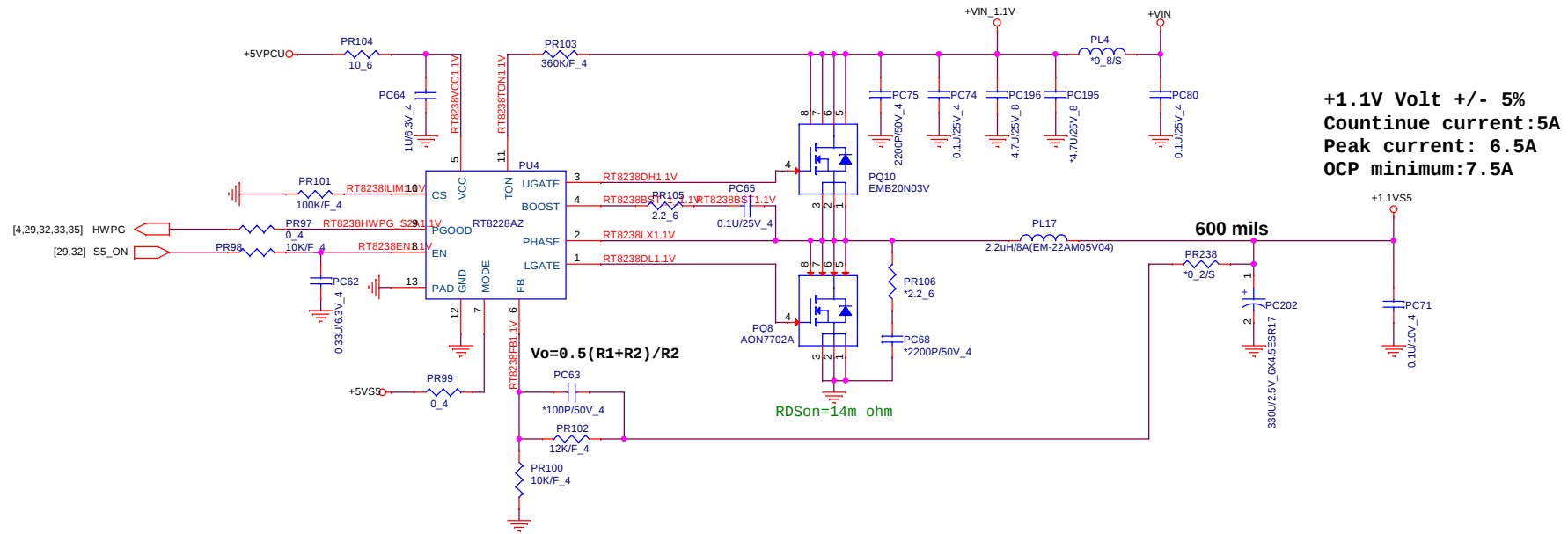
Close to Q24

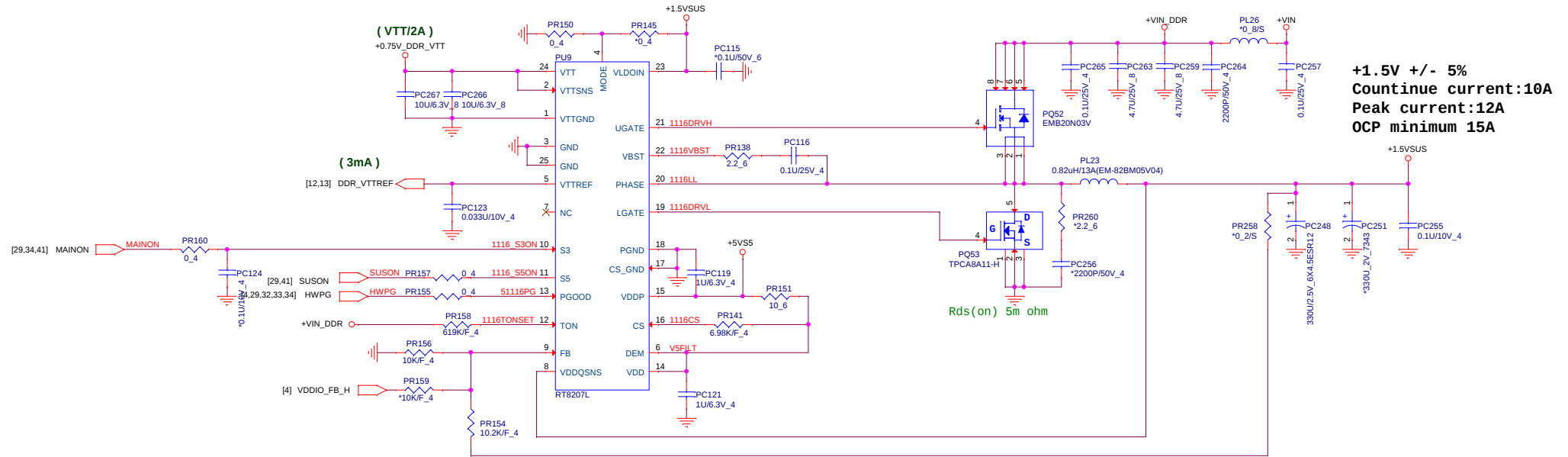






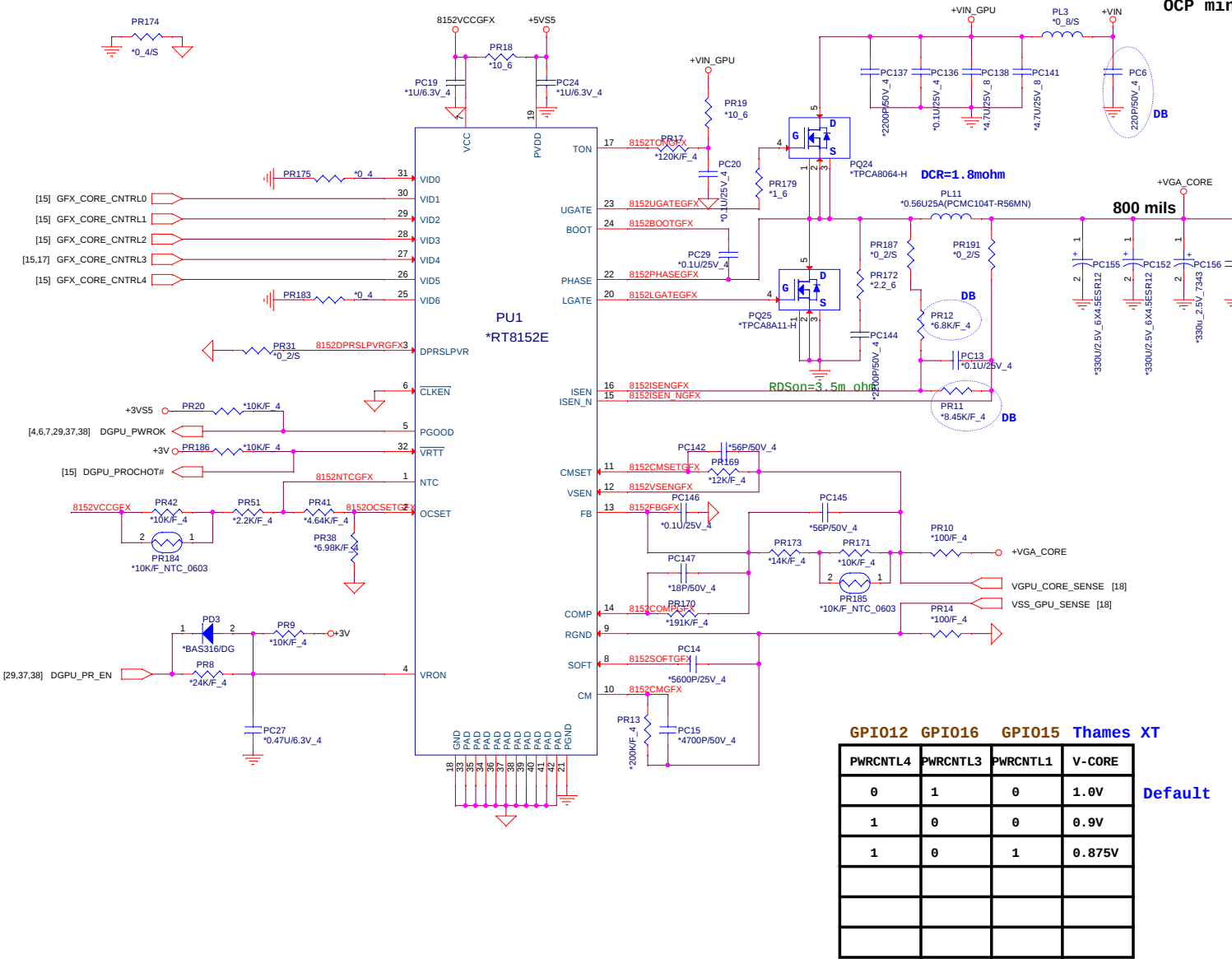






VGA Core

+VGA_UMA +/- 5%
Countinue current:18A
Peak current:22A
OCP minimum 25A



GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

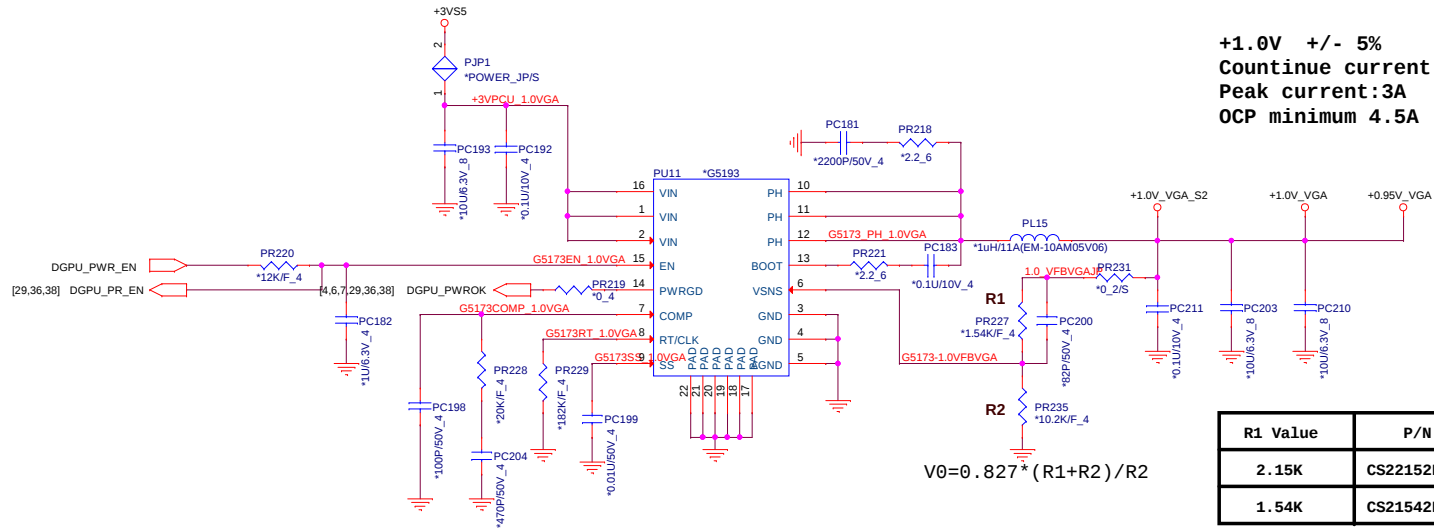
Default

PV

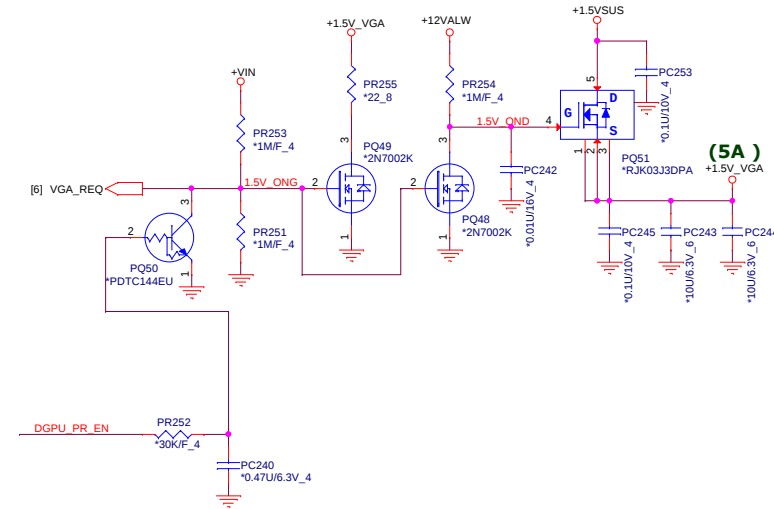
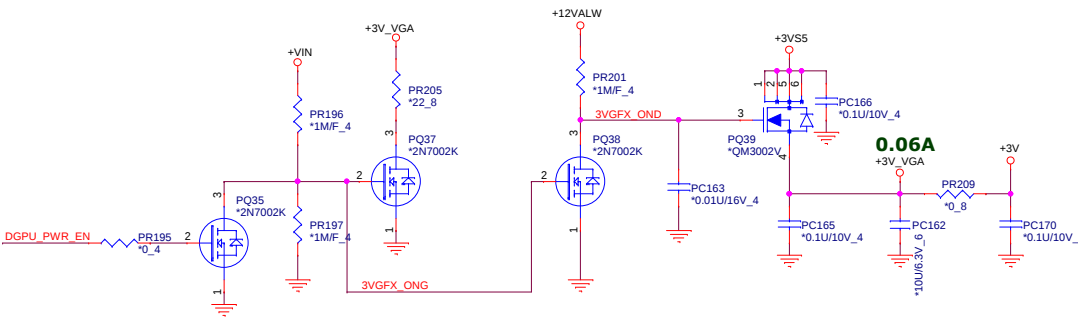
GPIO12 GPIO16 GPIO15 Thames XT

PWRCNTL4	PWRCNTL3	PWRCNTL1	V-CORE
0	1	0	1.0V
1	0	0	0.9V
1	0	1	0.875V

Default

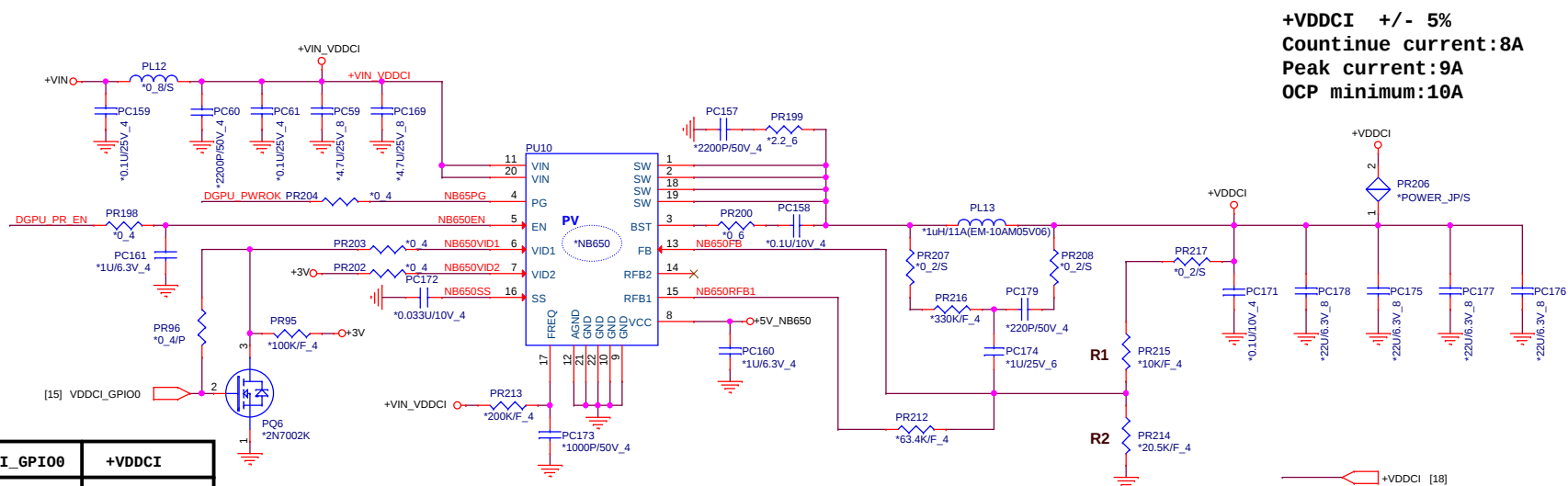
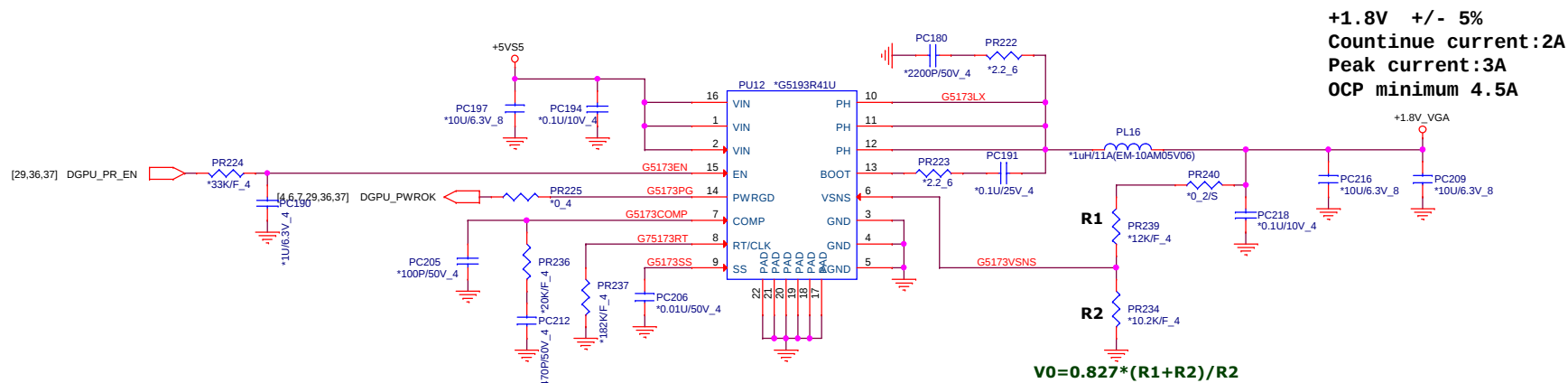


- +3V [2,4,6,8,9,10,11,12,13,14,23,24,25,26,27,28,29,30,36,38,41]
- +VIN [28,30,31,32,33,34,35,36,38,40,41]
- +3VSS [6,8,9,10,25,26,27,29,32,34,36,41]
- +5VSS [23,25,26,32,33,34,35,36,38,39,40,41]
- +3V_VGA [18]
- +12VALW [31,41]
- +1.5VSUS [2,3,4,5,12,13,35,41]
- +1.5V_VGA [18,20,21,22]
- +1.8V_VGA [15,16,18,19,38]
- +3V_DELAY [15,17,18]
- +VGA_CORE [18,36]



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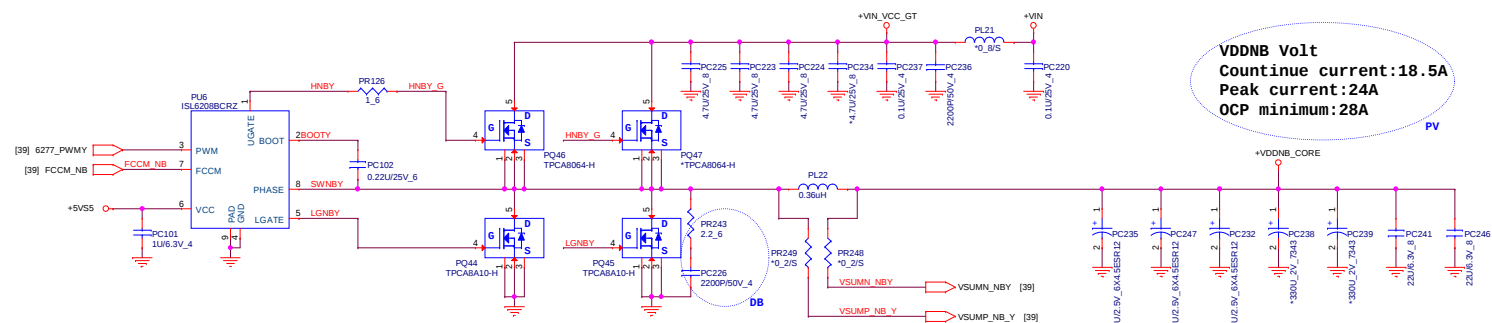
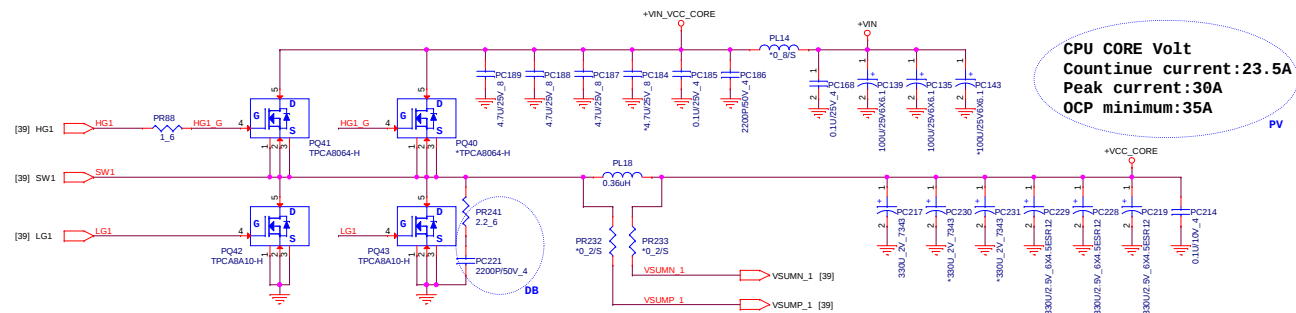


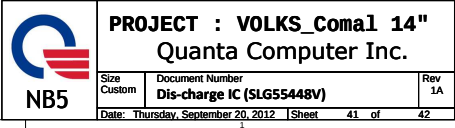
VDDCI_GPI01	VDDCI_GPI00	+VDDCI
X	0	1.0V
X	1	0.9V
X	X	X
X	X	X



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5	4	3	2	1
D				D
C				C
B				B
A				A
S	4	3	2	



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Size C	Document Number History	Rev 1A
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