ZRA SYSTEM DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

DDR3-SODIMM1 PAGE 7 — DDR3 channel A
DDR3-SODIMM2 PAGE 8 — DDR3 channel B

AMD Champlain
35mm X 35mm
S1G4 Processor
638P (PGA)45W/35W
PAGE 4,5,6

CPU THERMAL SENSOR PAGE 6

From SB Option

14.318MHz
CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP628VTR-->HP
RTM880N-796 -->HP
PAGE 3

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

HT3

PCI-E

NORTH BRIDGE
RS880
A12
21mm X 21mm, 528pin BGA
PAGE 9,10,11,12

PCI-Express 16X

ATI
Madison LP
128-bit M2 Pkg
29mm X 29mm
PAGE 18,19,20,21,22,23

800MHz
VRAM DDR3
64MX16X8,128bit
128MX16X8,128 bit
PAGE 24,25

VGA
Madison/Park

X1 Port 0
LAN
BCM 57760
PCIE-LAN
(10/100/1000)
PAGE 27

X1 Port 2
Mini PCI-E Card
(Wireless LAN)
PAGE 28

1 to 2 Switch

Lan_PCIE1
Lan_PCIE2

Docking

RJ45
PAGE 27

ALINK X4

DVI
LVDS
CRT

MUXs (S.G)

1 to 2 Switch

On board LVDS
On board CRT

Docking
PAGE 36

CRT connector
DVI connector
USB connector x 3
RJ45 connector
MIC
Line out
Line in

USB2.0 x 1
Lan_PCIE1
MIC to Docking
Line out to Docking
Line in from Docking

SOUTH BRIDGE
SB820
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 13,14,15,16,17

USB2.0
Finger print PAGE 32
BT PAGE 32

SATA - HDD1 PAGE 29 — SATA0 150MB
SATA - CD-ROM PAGE 29 — SATA1 150MB

USB2.0 Ports X1 PAGE 32
Webcam PAGE 26
CardReader AU6437 PAGE 31
WLAN conn PAGE 28

USB BOARD
USB2.0 Ports x3
PAGE 32

Power BOARD
PAGE 33

TPM PAGE 28

LPC
Azalia

Winbond KBC
NPCE781L
PAGE 35

Codec CX20672-11Z
PAGE 30

MIC to Docking
Line out to Docking
Line in from Docking

MDC
PAGE 30

Keyboard PAGE 34
Touch Pad PAGE 32

CPU FAN PAGE 34

SPI PAGE 35

Digital MIC PAGE 30

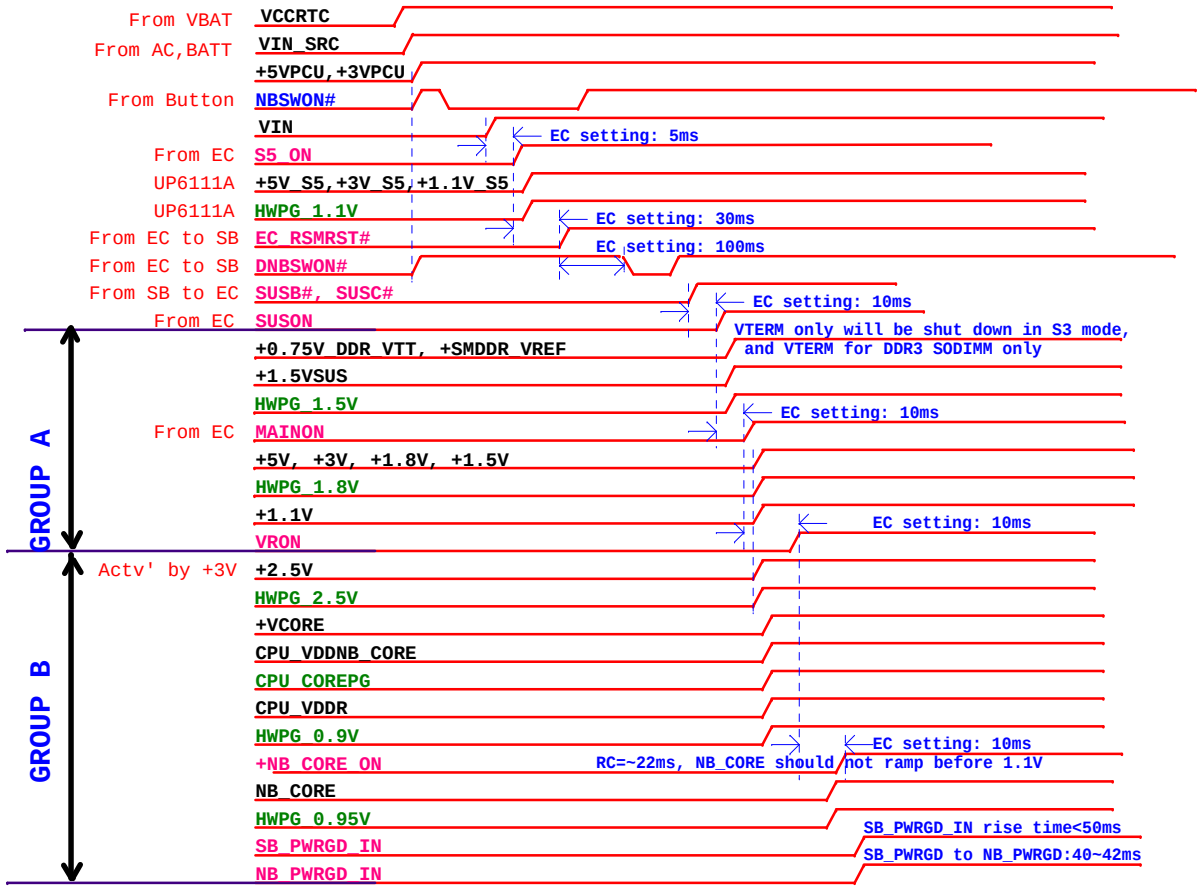
AUDIO CONN (Phone/ MIC) PAGE 30

Speaker PAGE 30

AMD CPU CORE (ISL6265) PAGE 39
NB_CORE (UP6111AQDD) PAGE 41
+VGPU_CORE (MAX8792ETD) PAGE 43
1.1V (UP6111AQDD) PAGE 40
1.8V/GPU_Power/+2.5V PAGE 44
DDR 1.5V(RT8207) PAGE 42
SYSTEM 5V/3V (RT8206) PAGE 38
1V/CPU_VDDR/Discharage PAGE 45
Charger (ISL88731) PAGE 37

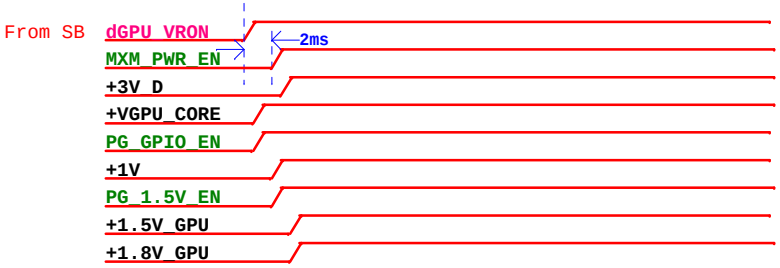
Quanta Computer Inc.
PROJECT : ZRA
Size | Document Number: Block Diagram | Rev 1A
Date: Monday, March 29, 2010 | Sheet 1 of 48

Danube Power On Sequence



Notice:
1.CPU_LDT_RST# msut be asserted a minimum of 1ms prior to the assertion of CPU_PWRGD
2.CPU_CLKP/N must be within specification a minimum of 1ms prior to the assertion of CPU_PWRGD
3.CPU_PWRGD remains deasserted at least 1ms after both CPU_CLKP/N and all voltages to the processor are within specification for operation
4.all NB power rails(1.8V/1.2V/1.1V) valid before NB_PWRGD at least 1ms
5.stable input clocks from CLKGEN(HT_REFCLKP/N) to NB before NB_PWRGD at least 1ms

Danube GPU Power Sequence



Power on sequence required:

SB800:
1.+3.3V_S5 ramp before +1.1_S5
2.+3.3V ramp before +1.8V
3.+1.8V ramp before +1.1V
4.+3.3V ramp before +1.1V
5.+3.3V_S5 ramping down time>300us
6.All power rails rise time >= 50us, except +3.3V_S5<=40ms
7.100us<=+3.3V_S5 rise time<=40ms
9.VBAT (VCCRTC) must ramp at least 5 seconds before the S5 rails to allow start time for the internal RTC

(only in SB820M NB_PWRGD signal)
40ms <= SB PWRGOOD to NB_PWRGD delay <= 42ms

RS880:
1.0<(+3.3V)-(+1.8V)<2.1
2.+1.8V ramp before +1.1V
3.+1.1V ramp before CPU_VDDNB_CORE

BOM naming rule

Items	Function	Name	Description
1	Internal CLK GEN	SGN@	
2	External CLK GEN	GN@	
3	iGPU	IV@	
4	dGPU	SW@	
5	iGPU & dGPU notice	SP@	

SB SMBUS Table

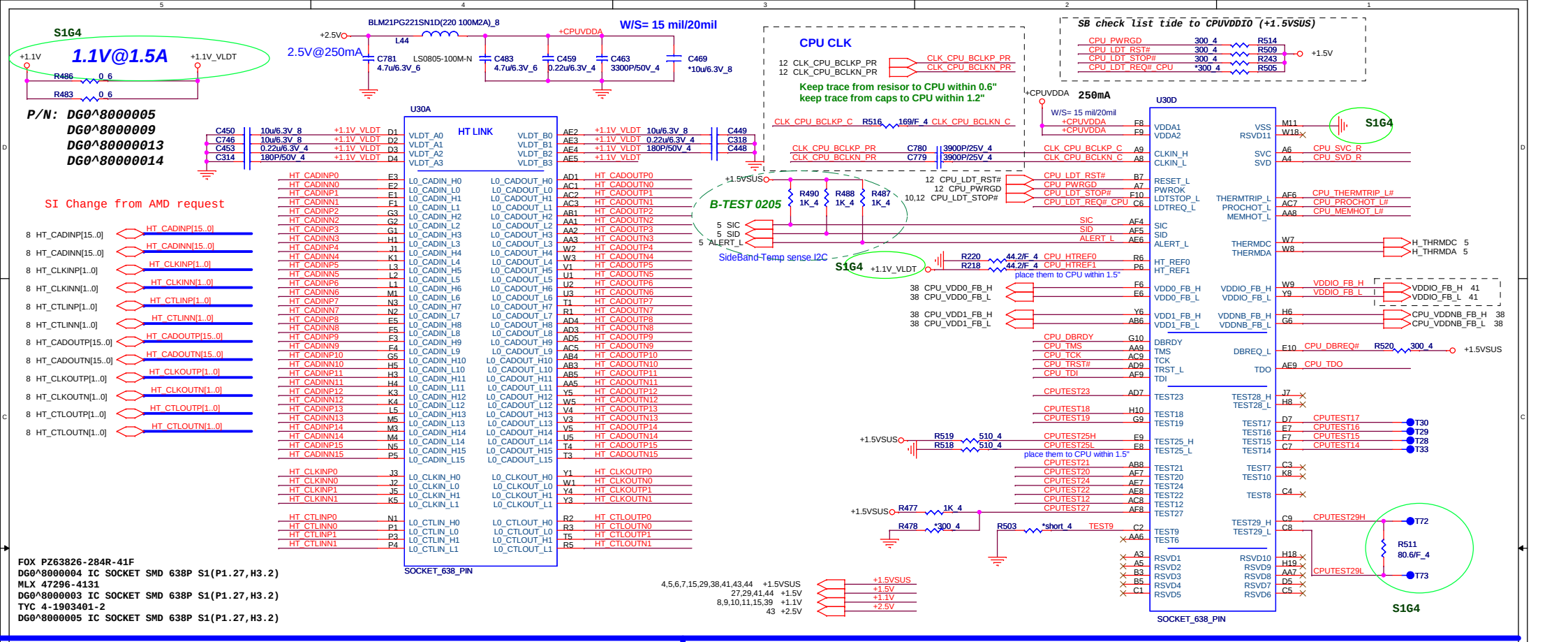
	CLK GEN	RAM	Mini Card (WLAN)
(SB_DA0)/(SB_CL0) (+3V)	V	V	V
Power Plane	+3V	+3V	+3V
MOS CKT (Level shift)	X	X	X*

*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor
EC775 SDA1 / SCL1 (+3VPCU)	V	
EC775 SDA2 / SCL2 (+3V)		V
EC775 SDA3 / SCL3 ()		
Power Plane	+3VPCU	+3V
MOS CKT (Level shift)	X	X

Quanta Computer Inc.
PROJECT : ZRA
Size | Document Number | Power Sequence | Rev 1A
Date: Monday, March 29, 2010 | Sheet 2 of 48


S1G4
1.1V@1.5A
+1.1V
+1.1V_VLDT
R486 0_6
R483 0_6
P/N: DG0^8000005
DG0^8000009
DG0^80000013
DG0^80000014
SI Change from AMD request
BLM21PG221SN1D(220 100M2A)_8
L44
+2.5V
2.5V@250mA
C781 4.7u/6.3V_6
LS0805-100M-N
+CPUVDDA
W/S= 15 mil/20mil
C483 4.7u/6.3V_6
C459 0.22u/6.3V_4
C463 3300P/50V_4
C469 *10u/6.3V_8
CPU CLK
12 CLK_CPU_BCLKP_PR
12 CLK_CPU_BCLKN_PR
CLK_CPU_BCLKP_PR
CLK_CPU_BCLKN_PR
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
SB check list tide to CPUVDDIO (+1.5VSUS)
CPU_PWRGD 300_4 R514
CPU_LDT_RST# 300_4 R509
CPU_LDT_STOP# 300_4 R243
CPU_LDT_REQ#_CPU *300_4 R505
+1.5V
+CPUVDDA 250mA
W/S= 15 mil/20mil
U30A
HT LINK
SOCKET_638_PIN
U30D
SOCKET_638_PIN
C450 10u/6.3V_8 +1.1V_VLDT
C746 10u/6.3V_8 +1.1V_VLDT
C453 0.22u/6.3V_4 +1.1V_VLDT
C314 180P/50V_4 +1.1V_VLDT
C449 10u/6.3V_8
C318 0.22u/6.3V_4
C448 180P/50V_4
+1.1V_VLDT
B-TEST 0205
R490 1K_4
R488 1K_4
R487 1K_4
+1.5VSUS
5 SIC
5 SID
5 ALERT_L
SideBand-Temp sense I2C
R220 44.2/F_4 CPU_HTREF0
R218 44.2/F_4 CPU_HTREF1
place them to CPU within 1.5"
38 CPU_VDD0_FB_H
38 CPU_VDD0_FB_L
38 CPU_VDD1_FB_H
38 CPU_VDD1_FB_L
CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
CPU_TDO
CPU_DBREQ#
R520 300_4
CPUTEST23
CPUTEST18
CPUTEST19
CPUTEST25H
CPUTEST25L
R519 510_4
R518 510_4
CPUTEST21
CPUTEST20
CPUTEST24
CPUTEST22
CPUTEST12
CPUTEST27
R477 1K_4
R478 *300_4
R503 *short_4
TEST9
CPUTEST29H
CPUTEST29L
R511 80.6/F_4
T30
T29
T28
T33
T72
T73
VDDIO_FB_H 41
VDDIO_FB_L 41
CPU_VDDNB_FB_H 38
CPU_VDDNB_FB_L 38
H_THRMDC 5
H_THRMDA 5
CPU_SVC_R
CPU_SVD_R
CPU_THERMTRIP_L#
CPU_PROCHOT_L#
CPU_MEMHOT_L#
4,5,6,7,15,29,38,41,43,44 +1.5VSUS
27,29,41,44 +1.5V
8,9,10,11,15,39 +1.1V
43 +2.5V
+1.5VSUS
+1.5V
+1.1V
+2.5V
FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)
B-TEST 0205
CNTR_VREF
C778 0.1u/10V_4
R524 20K/F_4
R529 34.8K/F_4
Q35 *BSS138_NL/SOT23
CPU_LDT_REQ# CPU
CPU_LDT_REQ# 10
R508 *0_4
CPU_LDT_RST#
R532 4.7K_4
Q36 BSS138_NL/SOT23
CPU_LDT_RST_HTPA#
G2 *SHORT_PAD1
for debug only
The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP
of the Northbridge is no longer required.
Q33 FDV301N
16,38,39 CPU_COREPG
R459 *10K_4
D25 *BAS316
R460 100K_6
R461 10K_4
R467 1K_4
R455 0_4
SYS_SHDN# 18,37,44
Q31 MMBT3904
CPU_THERMTRIP_L#
R456 *0_4
CPU_THERMTRIP# 13
R466 *10K_4
R472 300_4
Q30 *MMBT3904
CPU_PROCHOT_L#
R458 0_4
CPU_PROCHOT# 12,14
R457 *10K_4
R464 *1K_4
Q32 *MMBT3904
CPU_MEMHOT_L#
CPU_MEMHOT# 6,7,12
S1g4 does not support MEMHOT#
Serial VID
SI Change from AMD request
R530 1K_4
R526 *1K_4
R531 1K_4
R527 *1K_4
CPU_SVC_R R513 *short_4
CPU_SVD_R R512 *short_4
CPU_PWRGD R515 *short_4
R523 *220_4
R522 *220_4
R525 *220_4
CPU_SVC 38
CPU_SVD 38
CPU_PWRGD_SVID_REG 38
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.1V
0 1 1.0V
1 0 0.9V
1 1 0.8V
HDT Connector
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
C484 *0.1u/10V_4
CPU_LDT_RST_HTPA#
KEY
*HDT_CONN
CN7
CPUTEST24 R475 1K_4
CPUTEST23 R473 *1K_4
CPUTEST20 R474 1K_4
CPUTEST22 R476 1K_4
CPUTEST12 R184 1K_4
CPUTEST15 R229 1K_4
CPUTEST14 R534 1K_4
CPUTEST19 R533 1K_4
CPUTEST18 R236 1K_4
CPUTEST21 R159 1K_4
Quanta Computer Inc.
PROJECT : ZRA
Size
Document Number
S1G4 HT,CTL I/F 1/3
Rev 1A
Date: Monday, March 29, 2010
Sheet 3 of 48

Processor Memory Interface

VDDR=> 0.9V support 1066 / 800 DDR
VDDR= >1.05V support 1333 / 1066 / 800 DDR

CPU_VDDR VDDR=>1.75A

PLACE THEM CLOSE TO CPU WITHIN 1"

U30B — MEM:CMD/CTRL/CLK — SOCKET_638_PIN

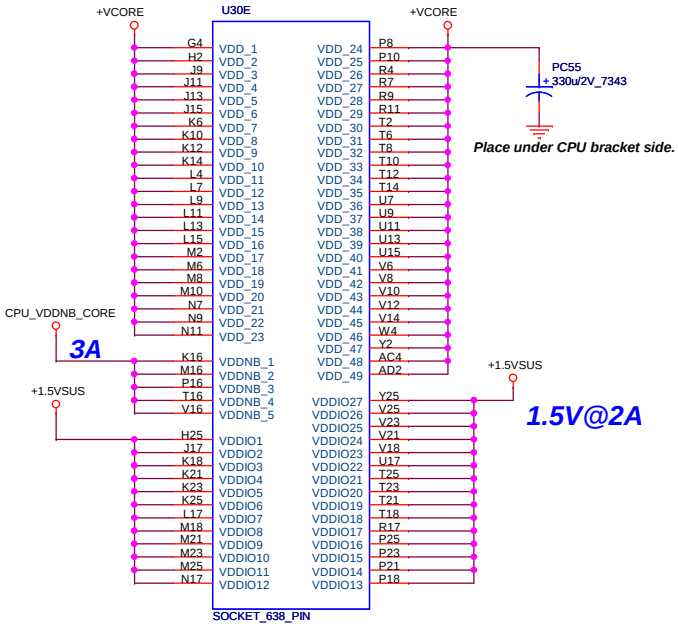
U30C — MEM:DATA — SOCKET_638_PIN

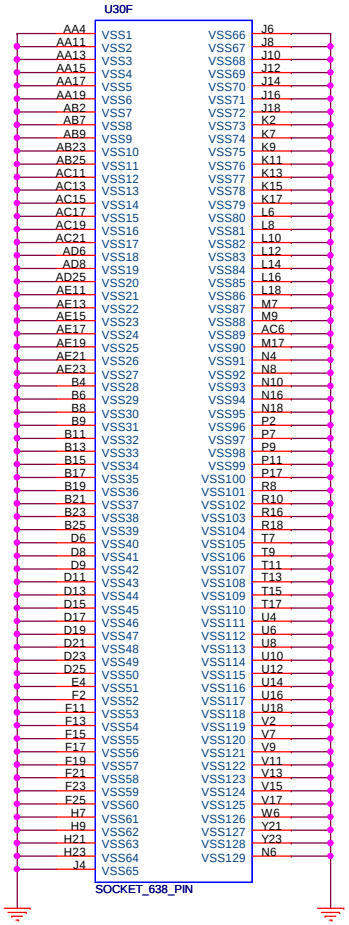
Place close to socket

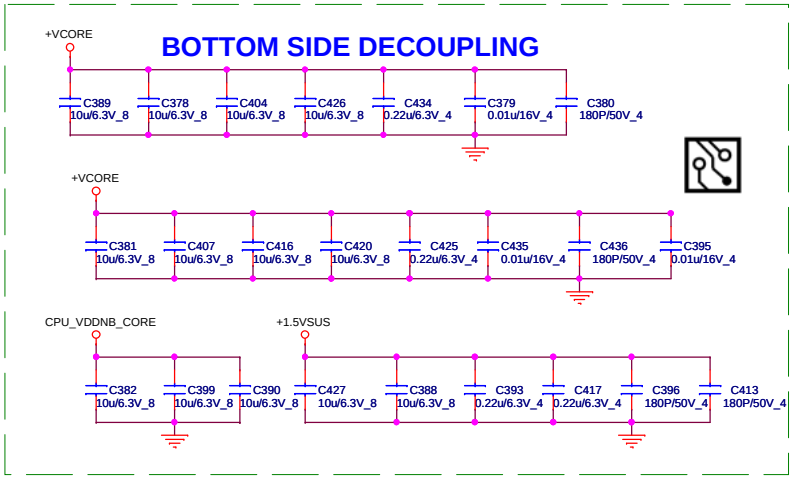
Reserved for AMD suggest

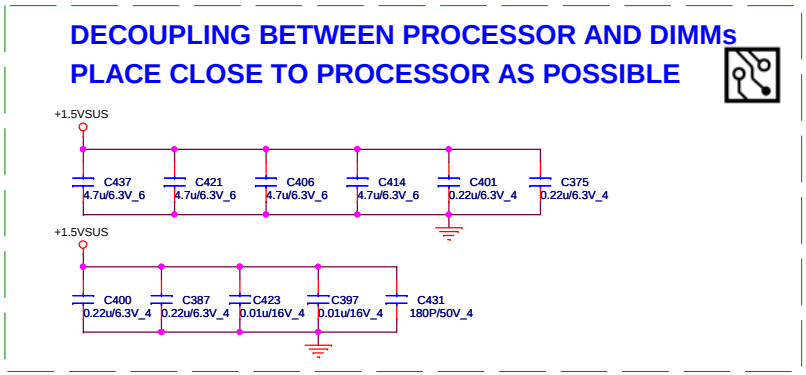
Quanta Computer Inc.	PROJECT : ZRA
Size	Document Number: S1G4 DDRIII MEMORY I/F 2/3 — Rev: 1A
Date: Monday, March 29, 2010	Sheet 4 of 48

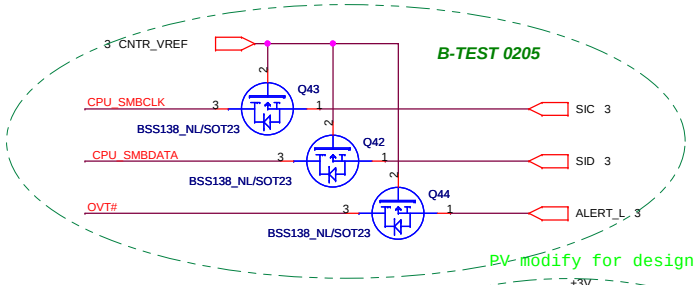
PROCESSOR POWER AND GROUND



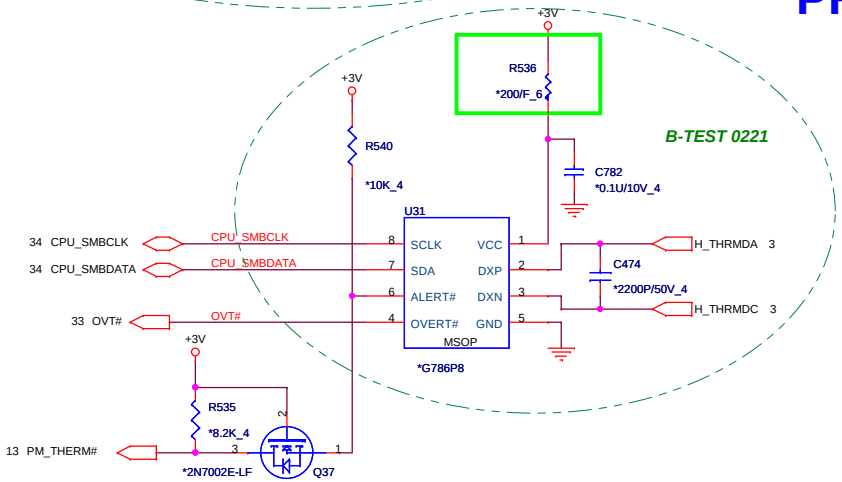








PV modify for design

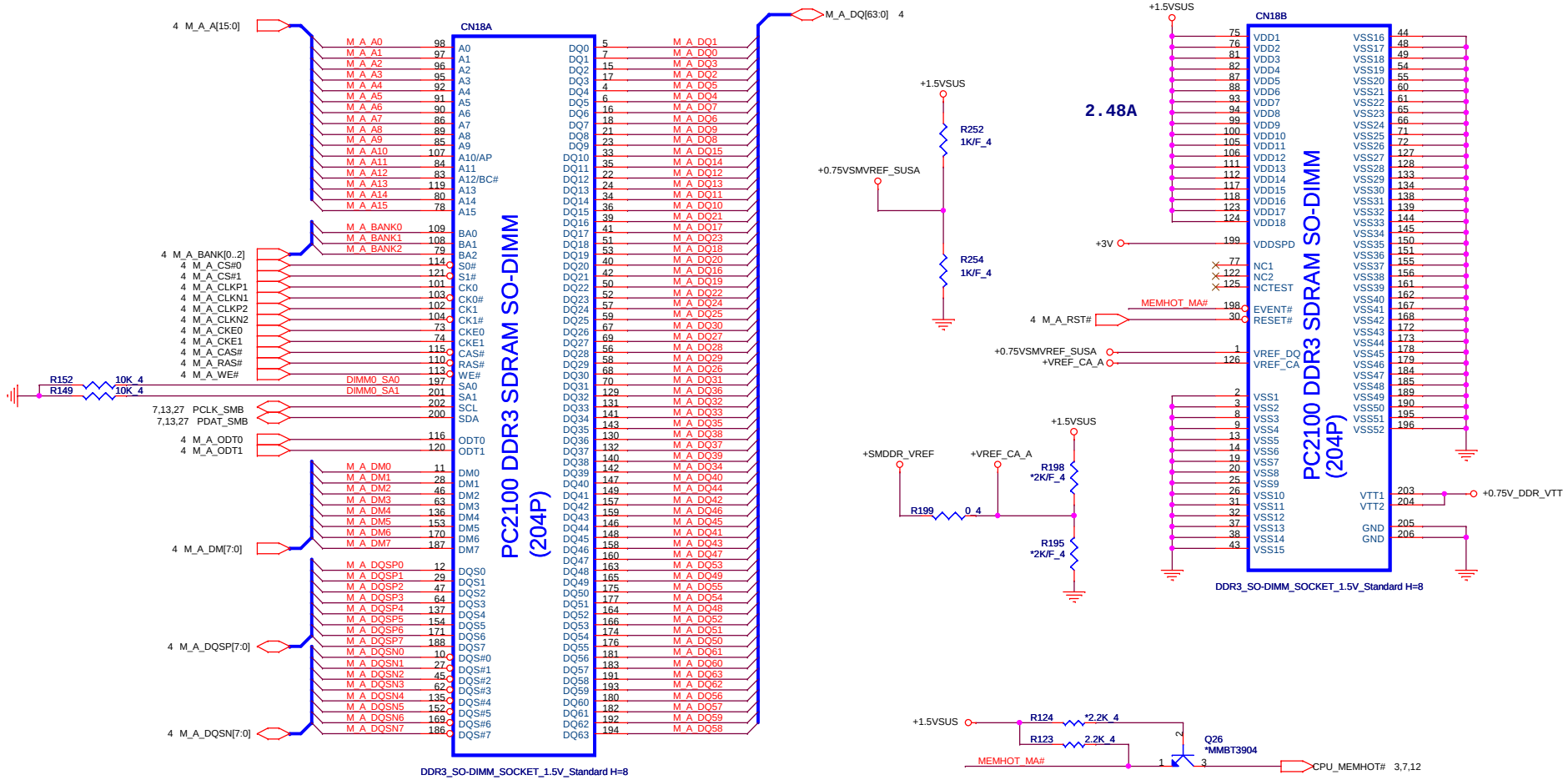


3,4,6,7,15,29,38,41,43,44 +1.5VSUS
38 CPU_VDDNB_CORE
38 +VCORE
12,13,15,16,26,27,29,32,35,37 +3V_S5
3,6,7,10,11,12,13,14,15,16,18,20,25,26,27,29,30,32,33,34,35,37,38,39,40,41,42,43,44 +3V

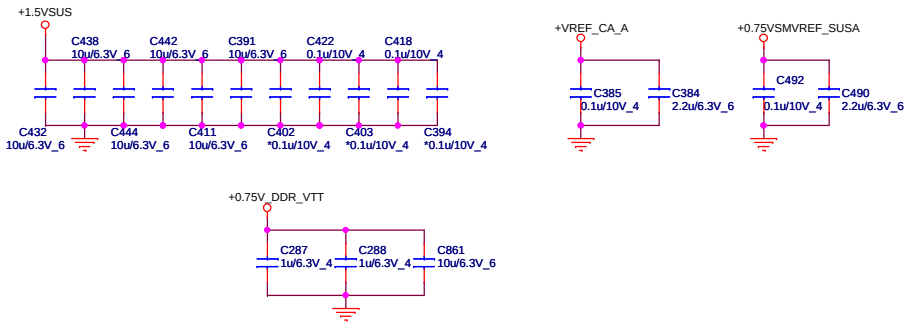
+1.5VSUS
CPU_VDDNB_CORE
+VCORE
+3V_S5
+3V

Quanta Computer Inc.
PROJECT : ZRA

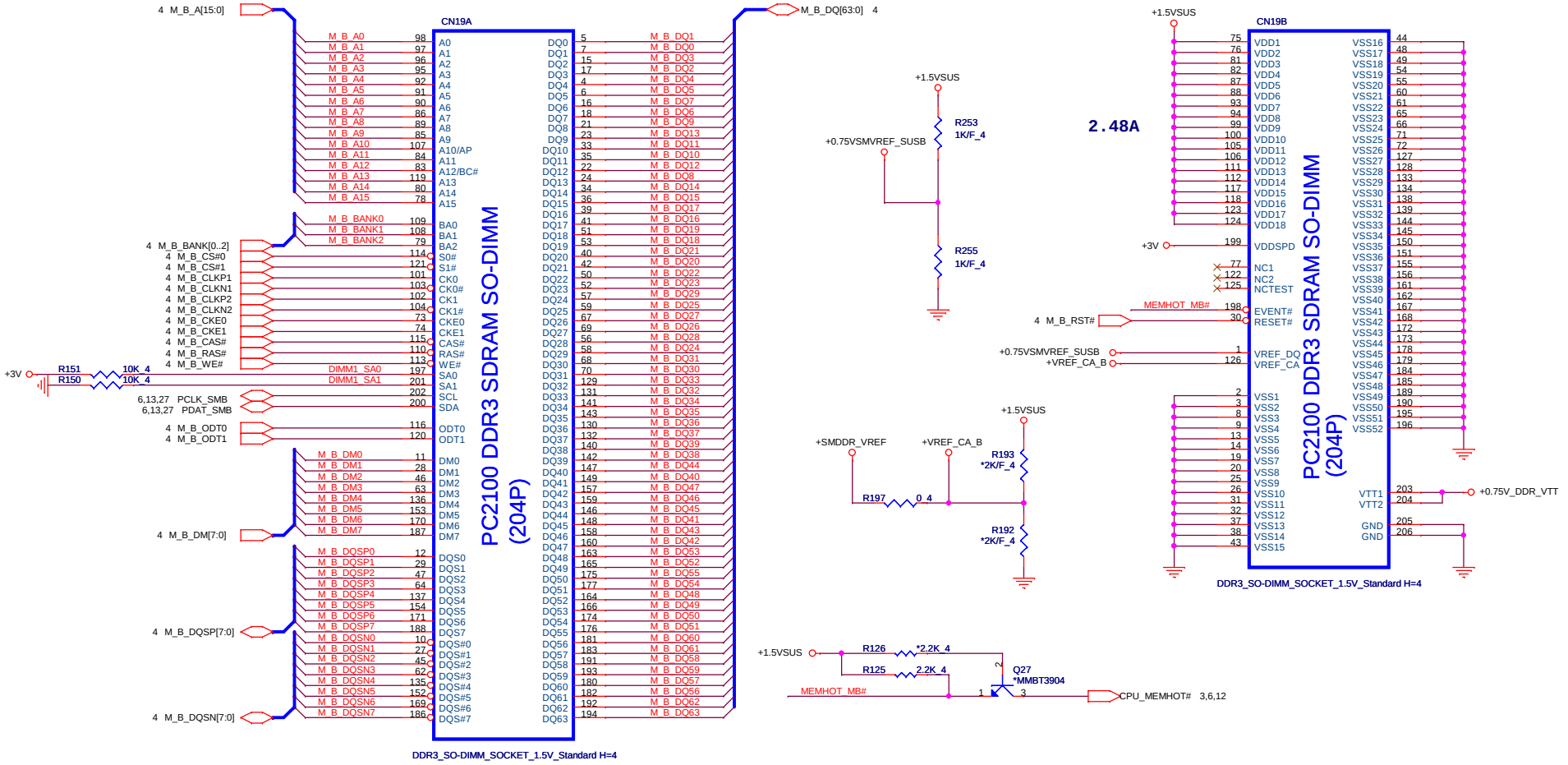
Size	Document Number	Rev
	S1G4 PWR & GND 3/3	1A
Date: Monday, March 29, 2010	Sheet 5 of 48	



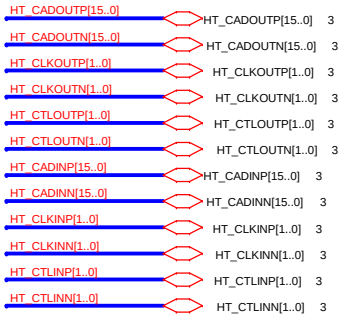
Place these Caps near So-Dimm0.



Quanta Computer Inc.			
PROJECT : ZRA			
Size	Document Number		Rev
	DDR3 DIMMA-STD		1A
Date: Monday, March 29, 2010		Sheet 6 of 48	



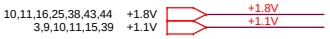
Quanta Computer Inc.			
PROJECT : ZRA			
Size	Document Number		Rev
	DDR3 DIMMB-STD		1A
Date: Monday, March 29, 2010		Sheet 7 of 48	

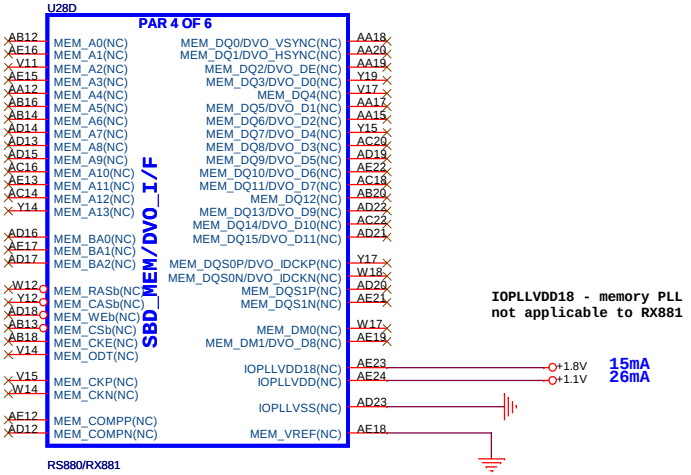


signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

This block is for UMA only , Discrete can remove all component

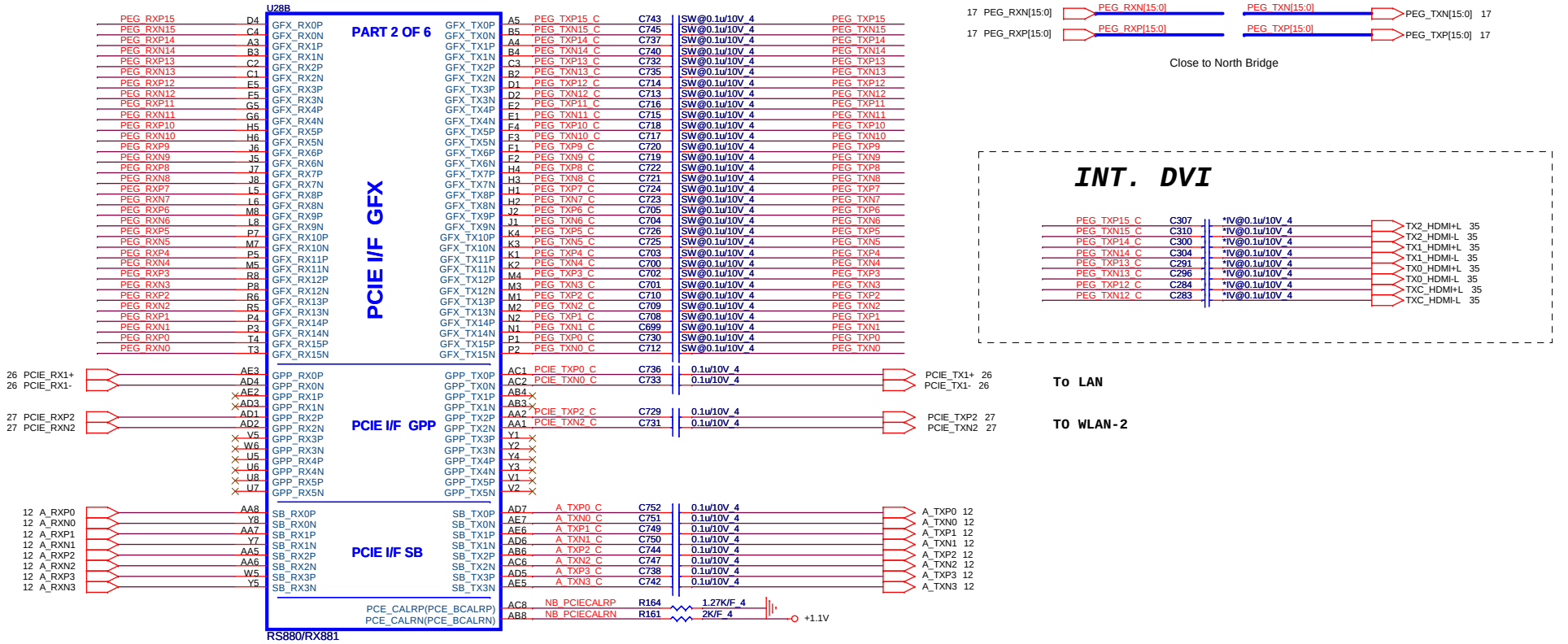




IOPLLVDD18 - memory PLL
not applicable to RX881

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
Date: Monday, March 29, 2010	Sheet 8 of 48	



RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Quanta Computer Inc.

PROJECT : ZRA

Size	Document Number	Rev
	RS880M-PCIE I/F 2/4	1A

Date: Monday, March 29, 2010 Sheet 9 of 48

All RS880 variants do not support analog TV-out functionality. As such, Y, C_Pr, and COMP_Pb

110mA
20mA
4mA

U28C — RS880/RX881 — PART 3 OF 6

CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.

Only for UMA
VGA (Not applicable to RX881)

For Check list JTAG

For A11 version

B-TEST 0128

Reference clock input for the RS880M.

B-TEST 0128

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M
1 Disable
0 Enable

RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

For extrnal EEPROM Debug only

RS780/RX780/RS880

Display Port interface from PCIeGraphics (RS880/rs880M only)

RS880M --- ADD

AVDD-DAC Analog not applicable to RX780

PLLVDD - Graphics PLL not applicable to RX780

change R175 0ohm to bead(CX8PG221003) and C339 from 0.1uF to 2.2uF(CH52201K991), for monitor noise issue.

C-TEST 0322

AVDDI-DAC Digital not applicable to RX780

AVDDQ-DAC Bandgap Reference not applicable to RX780

PLLVDD18 - Graphics PLL not applicable to RX780

VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

20mils width

VDDA18PCIEPLL -PCIE PLL

20mils width

VDDA18HTPLL -HT LINK PLL

DDR3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor on the Northbridge side.

B-TEST 0225
2.2K => 300R，Accord with LDT riss time SPEC

The RS880 family does not support CLMC architecture The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	RS880M-SYSTEM I/F 3/4	1A
Date: Monday, March 29, 2010	Sheet 10 of 48	

U28F

PART 6/6

GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLT18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	NC	NC

+1.1V 2A for RS880M
+1.1V 1.3A for RX881

+1.1V

0.6A L29 0_8 +1.1V_VDDHT

C343 4.7u/6.3V_6 C345 0.1u/10V_4 C346 0.1u/10V_4 C347 0.1u/10V_4

0.7A L42 0_8 +1.1V_VDDHTRX

C392 4.7u/6.3V_6 C359 0.1u/10V_4 C366 0.1u/10V_4 C357 0.1u/10V_4

+1.1V 2A for RS880M
+1.2V 0.4A for Rx881

+1.1V L34 0_6 **0.4A** +1.1V_VDDHTTX

C356 4.7u/6.3V_6 C354 0.1u/10V_4 C360 0.1u/10V_4 C355 0.1u/10V_4 C364 0.1u/10V_4

+1.8V 1A for RS780M+SB700
+1.8V 1A for RX881

+1.8V L27 BLM21PG221SN1D(220 100M2A)_8 **0.7A** +1.8V_VDDA18PCIE

C325 4.7u/6.3V_6 C324 4.7u/6.3V_6 C320 0.1u/10V_4 C323 0.1u/10V_4 C316 0.1u/10V_4 C326 0.1u/10V_4

+1.8V R157 0_6 **25mA** +1.8V_VDDG18_NB

VDD18-RS880 I/O Transform

C315 1u/6.3V_4

U28E

PART 5/6

POWER

RS880/RX881

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7 — J17 K16 L16 M16 P16 R16 T16

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7 — H18 G19 F20 E21 D22 B23 A23

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13 — AE25 AD24 AC23 AB22 AA21 Y20 W19 V18 U17 T17 R17 P17 M17

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15 — J10 P10 K10 M10 L10 W9 H9 T10 R10 Y9 AA9 AB9 AD9 AE9 U10

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2) VDD18_MEM1(NC) VDD18_MEM2(NC) — F9 G9 AE11 AD11

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17 — A6 B6 C6 D6 E6 F6 G7 H8 J9 K9 M9 L9 P9 R9 T9 V9 U9

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22 — K12 J14 U16 J11 K15 M12 L14 L11 M13 M15 N12 N14 P11 P13 P14 R12 R15 T11 T15 U12 T14 J16

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC) — AE10 AA11 Y11 AD10 AB10 AC10

VDDG33_1(NC) VDDG33_2(NC) — H11 H12

+1.1V_VDD_PCIE **2.5A** VDDPCIE - PCIE-E Main power

C297 0.1u/10V_4 C319 0.1u/10V_4 C321 1u/6.3V_4 C322 1u/6.3V_4 C317 4.7u/6.3V_6

R143 0_8 +1.1V

0.95~1.1V 10A

VDDC - Core Logic power

C341 0.1u/10V_4 C338 0.1u/10V_4 C337 0.1u/10V_4 C333 0.1u/10V_4 C340 10u/6.3V_8

NB_CORE

C342 0.1u/10V_4 C334 0.1u/10V_4 C332 0.1u/10V_4 C329 10u/6.3V_8

VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

+3V_VDDG33 R172 0_4 **60mA** +3V

C327 0.1u/10V_4 C328 0.1u/10V_4

VDD33 - 3.3V I/O
Not applicable to RX780

+1.1V
+1.8V
NB_CORE

+1.1V 3,8,9,10,15,39
+1.8V 8,10,16,25,38,43,44
NB_CORE 33,40

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	RS880M-POWER 4/4	1A
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MINI-PCIE,Card reader
NB & EC

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO SB820

SB800 Part 1 of 5

RTC(RTC)

Board ID

	BOARD_ID4 GPIO14	BOARD_ID3 GPIO13	BOARD_ID2 GPIO12	BOARD_ID1 GPIO11	BOARD_ID0 GPIO10
0	N/A	BAP50	WO/Sideport	UMA	14"
1	N/A	BXP50	W/Sideport	Discrete	15.6"

B-TEST 0226
B-TEST 0226
B-TEST 0226
不分BAP/BXP

B-TEST 0128
B-TEST 0128
B-TEST 0128

C-TEST 0323
add R638 for CRT 預留

B-TEST 0129
B-TEST 0201
B-TEST 0129

For VDDR 1.05 control
VDDR_1.05_EN:
1 : VDDR =1.05V
0 : VDDR = 0.9V (Default)

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

for EMI suggestion

Quanta Computer Inc.			
PROJECT : ZRA			
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NC only ,Can't be install

+3V_S5
R376 *2.2K_4 SB_TEST0
R373 *2.2K_4 SB_TEST1
R358 *2.2K_4 SB_TEST2

+3V
SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R276 2.2K_4 PCLK_SMB
R275 2.2K_4 PDAT_SMB
Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

+3V_S5
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R278 2.2K_4 SB_SCLK2
R270 2.2K_4 SB_SDATA2

+3V
R329 4.7K_4 SUS_STAT#

dGPU_VRON
2ms
MXM_PWR_EN
20 MXM_PWREN
12,42,43 dGPU_VRON
+3V
R289 SW@10K_4
B-TEST 0128
D13 SW@RB501V-40
D14 *SW@RB501V-40
C564 SW@0.1u/10V_4
>1mS delay is required between all MXM power rail stable and MXM_PWREN(enables the module internal power)

12,15,16,26,27,29,32,35,37 +3V_S5
3,5,6,7,10,11,12,14,15,16,18,20,25,26,27,29,30,32,33,34,35,37,38,39,40,41,42,43,44 +3V
+3V_S5
+3V

USBCLK/41M_25M_48M_OSC pin is CLK input
pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

change R301 footprint from 0402 to 0603
P/N from CS00002JB38 to CX08T600102

C-TEST 0324
B-TEST 0223
CLK source change from exterior to SB

EMI
CLK_48M_USB
C-TEST 0324
del R300, stuff C581 for EMI
C581 10p/50V_4

U36D
SB800
Part 4 of 5

34 SUSB#
34 SUSC#
34 DNBSWON#
16,27 SB_PWRGD_IN
10 SUS_STAT#
SB_TEST0
SB_TEST1
SB_TEST2
34 SIO_A20GATE
34 SIO_RCIN#
LANLINK_STATE#
34 SIO_EXT_SMI#
34 SIO_EXT_SCI#
R551 0_4
R378 0_4
SIO_EXT_SMI#_R
SIO_EXT_SCI#_R
SYS_RST#
26 PCIE_WAKE#
PCIE_WAKE#
IR_RX1
3 CPU_THERMTRIP#
16 NB_PWRGD_SB
34 ICH_RSMRST#
T99
T98
T59

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS

USBCLK/14M_25M_48M_OSC
USB_RCOMP
A10 CLK_48M_USB
R301 S8K160808T-600Y-N_6
CR_CLK 30
G19 USB_RCOMP_SB
R283 11.8K/F_6
USB 1.1 USB MISC

USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
J10
H11
H9 USB_FDS12P
J8 USB_FSD12N
T51
T53

USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USB 2.0

USBP5+ 30
USBP5- 30
USBP12+ 31
USBP12- 31
USBP11+ 31
USBP11- 31
USBP10+ 31
USBP10- 31
USBP9+ 32
USBP9- 32
USBP8+ 25
USBP8- 25
USBP7+ 31
USBP7- 31
USBP4+ 27
USBP4- 27
USBP1+ 35
USBP1- 35
USBP0+ 31
USBP0- 31

USB card reader
USB board
USB board
USB board
BLUETOOTH
USB CAMERA
Finger Print
WLAN MINI CARD
DOCKING
On board USB connect
Only USB Port0 can be configured as debug port.

12 SB_GPIO_PCIE_RST#
26 CLK_PCIE_LAN_REQ#
MXM_PWR_EN
T45 SB_GPIO59
29 SPKR
6,7,27 PCLK_SMB
6,7,27 PDAT_SMB
26 SB_SMBCLK1
26 SB_SMBDATA1
27 CLK_PCIE_2_REQ#
T47 CRD_CLKREQ#
18 SB_CLKREQG# R272 *SW@0_4 CLKREQG#

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN
GPIO

31 OC_7# R377 0_4
31 OC_6#
5 PM_THERM#
31 OC_4# R315 0_4
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
USB OC

HD audio interface is +3VS5 voltage

16 ACZ_SDOUT
R622 *10K_4 ACZ_BCLK
ACZ_SDOUT
R328 *10K_4 ACZ_SDIN0
R327 *10K_4 ACZ_SDIN1
R630 *10K_4 ACZ_SDIN2
R317 *10K_4 ACZ_SDIN3
ACZ_SYNC
ACZ_RST#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
SB_SCLK2
SB_SDATA2
SB_GPIO195
SB_GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
GPIO199 16
GPIO200 16

+3V_S5
R619 10K_4 GBE_COL
R314 10K_4 GBE_CRS
R614 10K_4 GBE_MDIO
ZR8
R350 10K_4 GBE_RXERR
R351 10K_4 GBE_PHY_INTR

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
GBE LAN

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226
EMBEDDED CTRL

T40 ADP_PRES0
PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
EMBEDDED CTRL

SB820M_A12

Azalia to AUDIO and MDC
ADD C873 C874 C875,L43 for EMI
C-TEST 0324

ACZ_SDOUT
C875 *10p/50V_4
R341 33_4 ACZ_SDOUT_MDC 29
R629 33_4 ACZ_SDOUT_AUDIO 29
C611 *10p/50V_4
ACZ_SYNC
C874 *10p/50V_4
R631 33_4 ACZ_SYNC_MDC 29
R618 33_4 ACZ_SYNC_AUDIO 29
C857 *10p/50V_4
BLM15AG121SS1_4 L43
C873 *10p/50V_4
ACZ_BCLK
R627 33_4 ACZ_BITCLK_MDC 29
R628 33_4 ACZ_BITCLK_AUDIO 29
C614 *10p/50V_4
ACZ_RST#
R621 33_4 ACZ_RST#_MDC 29
R620 33_4 ACZ_RST#_AUDIO 29
ACZ_SDIN0 ACZ_SDIN0 29 AUDIO CODE
ACZ_SDIN1 ACZ_SDIN1 29 MDC
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

CN12
+3V_S5
C615 *10p/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W_JTAG_DEBUG
SB JTAG

Check list
SB_GPIO195 R563 10K_4
SB_GPIO196 R549 10K_4

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SATA PORT 0,1,2,3
can support AHCI
mode

SATA HDD

SATA ODD

U36B

SB800
Part 2 of 5

28 SATA_TX0+ — C850 0.01u/16V_4 — SATA_TX0+_C — AH9 SATA_TX0P
28 SATA_TX0- — C849 0.01u/16V_4 — SATA_TX0-_C — AJ9 SATA_TX0N
28 SATA_RX0- — AJ8 SATA_RX0N
28 SATA_RX0+ — AH8 SATA_RX0P
28 SATA_TX1+ — C848 0.01u/16V_4 — SATA_TX1+_C — AH10 SATA_TX1P
28 SATA_TX1- — C847 0.01u/16V_4 — SATA_TX1-_C — AJ10 SATA_TX1N
28 SATA_RX1- — AG10 SATA_RX1N
28 SATA_RX1+ — AF10 SATA_RX1P
AG12 SATA_TX2P
AF12 SATA_TX2N
AJ12 SATA_RX2N
AH12 SATA_RX2P
AH14 SATA_TX3P
AJ14 SATA_TX3N
AG14 SATA_RX3N
AF14 SATA_RX3P
AG17 SATA_TX4P
AF17 SATA_TX4N
AJ17 SATA_RX4N
AH17 SATA_RX4P
AJ18 SATA_TX5P
AH18 SATA_TX5N
AH19 SATA_RX5N
AJ19 SATA_RX5P

SERIAL ATA

+1.1V_AVDD_SATA
R295 1K/F_4 — SATA_CALRP — AB14 SATA_CALRP
R290 931/F_4 — SATA_CALRN — AA14 SATA_CALRN

32 SATA_ACT# — AD11 SATA_ACT#/GPIO67

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

*22P/50V_4 C845 — SATA_X1 — AD16 SATA_X1
Y7 *25MHZ
R587 *1M_4
C841 *22P/50V_4 — SATA_X2 — AC16 SATA_X2

T56 SB_GPIO164 — J5 SPI_DI/GPIO164
T61 SB_GPIO163 — E2 SPI_DO/GPIO163
T58 SB_GPIO162 — K4 SPI_CLK/GPIO162
T50 SB_GPIO165 — K9 SPI_CS1#/GPIO165
T60 SB_GPIO161 — G2 ROM_RST#/GPIO161

SPI ROM

SB820M_A12

15 +1.1V_AVDD_SATA — +1.1V_AVDD_SATA
12,13,15,16,26,27,29,32,35,37 +3V_S5 — +3V_S5

FC_CLK AH28 — T80
FC_FBCLKOUT AG28 — T78
FC_FBCLKIN AF26 — T86
FC_OE#/GPIOD145 AF28 — T77
FC_AVD#/GPIOD146 AG29 — T76
FC_WE#/GPIOD148 AG26 — T87
FC_CE1#/GPIOD149 AF27 — T81
FC_CE2#/GPIOD150 AE29 — T74
FC_INT1/GPIOD144 AF29 — T75
FC_INT2/GPIOD147 AH27 — T83
FC_ADQ0/GPIOD128 AJ27 — T82
FC_ADQ1/GPIOD129 AJ26 — T37
FC_ADQ2/GPIOD130 AH25 — T85
FC_ADQ3/GPIOD131 AH24 — T91
FC_ADQ4/GPIOD132 AG23 — T90
FC_ADQ5/GPIOD133 AH23 — T93
FC_ADQ6/GPIOD134 AJ22 — T95
FC_ADQ7/GPIOD135 AG21 — T96
FC_ADQ8/GPIOD136 AF21 — T97
FC_ADQ9/GPIOD137 AH22 — T94
FC_ADQ10/GPIOD138 AJ23 — T89
FC_ADQ11/GPIOD139 AF23 — T42
FC_ADQ12/GPIOD140 AJ24 — T92
FC_ADQ13/GPIOD141 AJ25 — T88
FC_ADQ14/GPIOD142 AG25 — T84
FC_ADQ15/GPIOD143 AH26 — T79

FLASH

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

FANOUT0/GPIO52 W5
FANOUT1/GPIO53 W6
FANOUT2/GPIO54 Y9 — SB_PROCHOT#_C
FANIN0/GPIO56 W7 — WWAN_DET# — T55
FANIN1/GPIO57 V9 — CPPE_NC1# — T52
FANIN2/GPIO58 W8 — CRD_REQ1# — T57
TEMPIN0/GPIO171 B6 — TEMPIN0
TEMPIN1/GPIO172 A6 — TEMPIN1
TEMPIN2/GPIO173 A5 — MB_THRMDA_SB
TEMPIN3/TALERT#/GPIO174 B5 — SB_GPIO174
TEMP_COMM C7 — TEMP_COMM
VIN0/GPIO175 A3 — SB_GPIO175
VIN1/GPIO176 B4 — SB_GPIO176
VIN2/GPIO177 A4 — SIDE_PORT_ID0
VIN3/GPIO178 C5 — SIDE_PORT_ID1
VIN4/GPIO179 A7 — MEM_1V5 12
VIN5/GPIO180 B7 — SB_GPIO180
VIN6/GBE_STAT3/GPIO181 B8 — SB_GPIO181
VIN7/GBE_LED3/GPIO182 A8 — SB_GPIO182

HW MONITOR

NC1 G27
NC2 Y2

+3V
R316 *10K_4
R306 *10K_4
Q23 *MMBT3904
3,12 CPU_PROCHOT# — SB_PROCHOT#_C

Check list

TEMPIN0	R597	10K_4
TEMPIN1	R598	10K_4
MB_THRMDA_SB	R601	10K_4
SB_GPIO174	R600	10K_4
SB_GPIO175	R606	10K_4
SB_GPIO176	R605	10K_4
SIDE_PORT_ID0	R603	10K_4
SIDE_PORT_ID1	R604	10K_4
SB_GPIO180	R596	10K_4
SB_GPIO181	R594	*10K_4
SB_GPIO182	R592	10K_4

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PROJECT : ZRA

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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power

VDD-- S/B CORE power

U36C

SB800

Part 3 of 5

POWER

SB820M_A12

SB820 without GBE: Connected to GND plane.

U36E

SB800

GROUND

Part 5 of 5

SB820M_A12

If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

For support USB wakeup-->3V_S5

B-TEST 0202

Quanta Computer Inc.

PROJECT : ZRA

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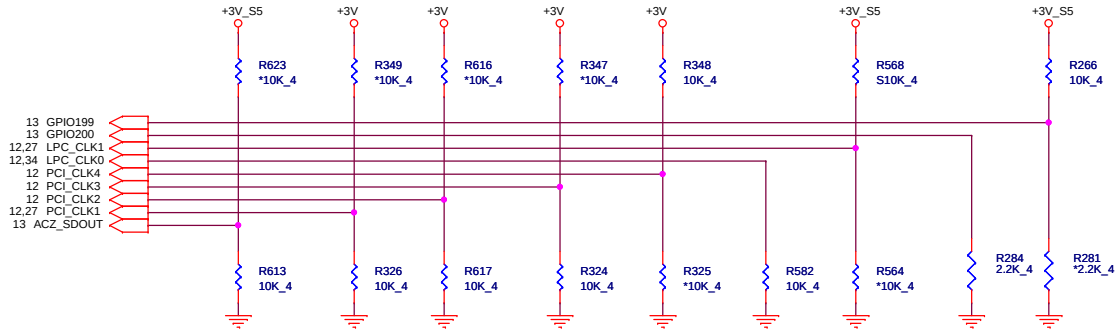
REQUIRED STRAPS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

SB820M is supported Gen1 mode only.

For internal clock GEN.



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L,H=LPC ROM DEFAULT L, L=FWH ROM

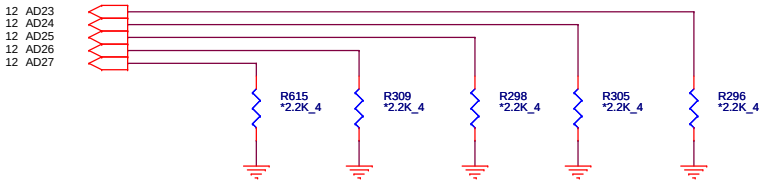
internal have pull Hi 10K

12,13,15,26,27,29,32,35,37 +3V_S5
8,10,11,25,38,43,44 +1.8V

+3V_S5
+1.8V

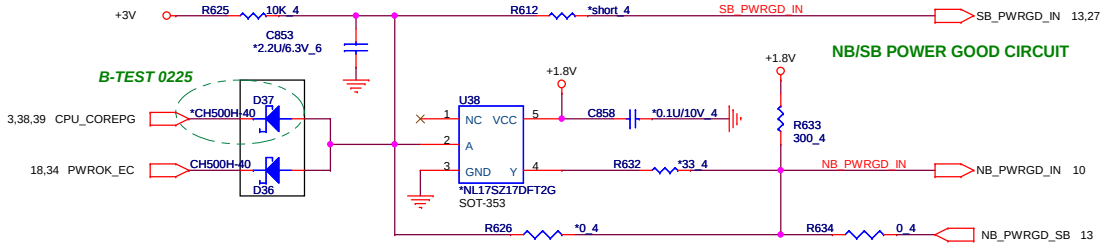
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

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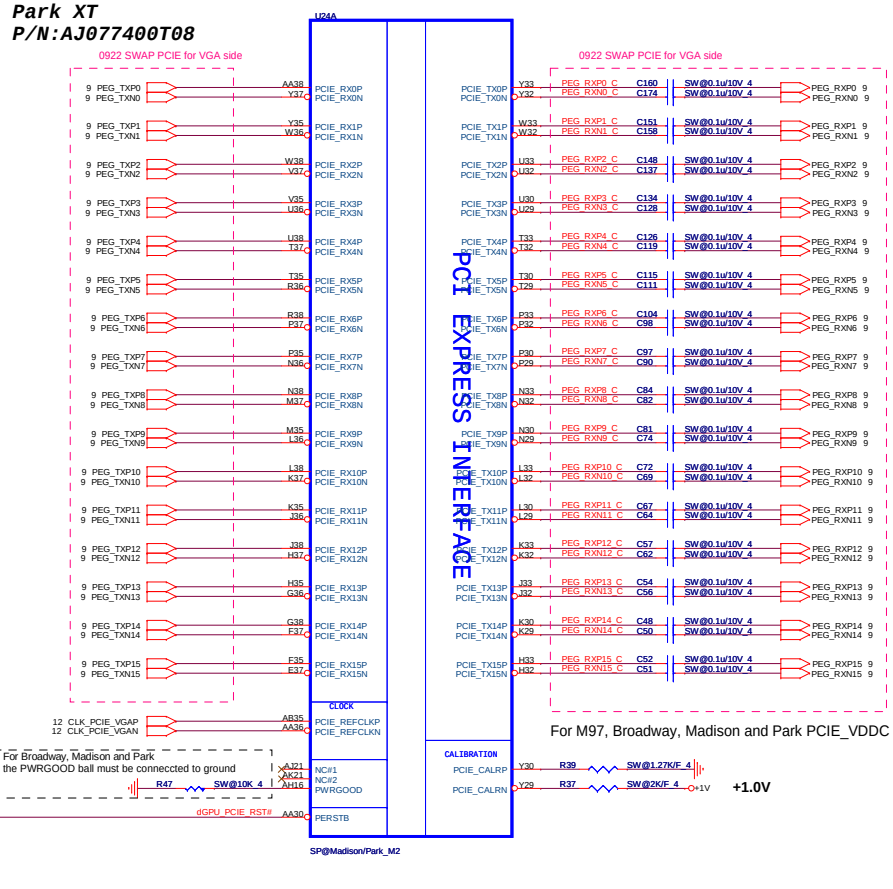
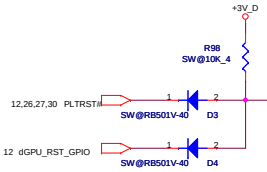
Park XT
P/N:AJ077400T08





For Broadway, Madison and Park the PWRGOOD ball must be connecctd to ground

R47 SW@10K_4

dGPU_PCIE_RST#

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

R39 SW@1.27K/F_4

R37 SW@2K/F_4 +1V

+1.0V

+3V_D
+1V

+3V_D 18,20,22,25,35
+1V 18,20,21,44

B-TEST 0201

18 GPIO24_TRSTB R76 *SW@10K_4
18 GPIO27_TMS R83 *SW@10K_4 +3V_D
18 GPIO26_TCK R91 *SW@0_4 SB_CLK_VGA 12
19 TESTEN R45 *SW@10K_4 +3V_D

JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBUG)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
TESTEN	"1" (PU)	"1" (PU)

Quanta Computer Inc.
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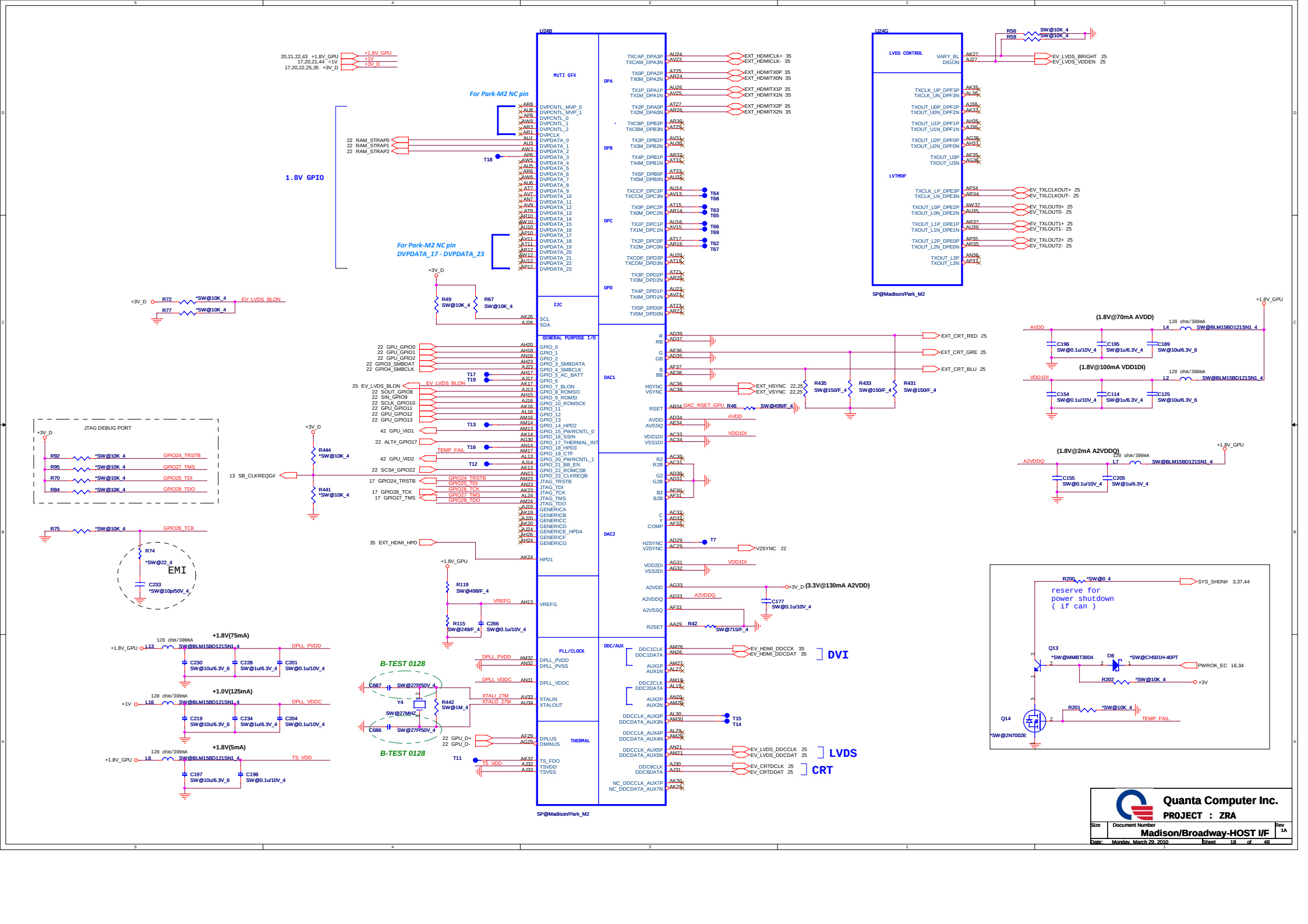
U24B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
PLL/CLOCK
DDC/AUX
THERMAL
SP@Madison/Park_M2
U24G
LVDS CONTROL
LVTMDP
SP@Madison/Park_M2
For Park-M2 NC pin
DVPDATA_17 - DVPDATA_23
1.8V GPIO
JTAG DEBUG PORT
EMI
B-TEST 0128
B-TEST 0128
+1.8V(75mA)
+1.0V(125mA)
+1.8V(5mA)
(1.8V@70mA AVDD)
(1.8V@100mA VDD1DI)
(1.8V@2mA A2VDDQ)
(3.3V@130mA A2VDD)
reserve for
power shutdown
(if can)
DVI
LVDS
CRT
Quanta Computer Inc.
PROJECT : ZRA
Madison/Broadway-HOST I/F
Rev 1A
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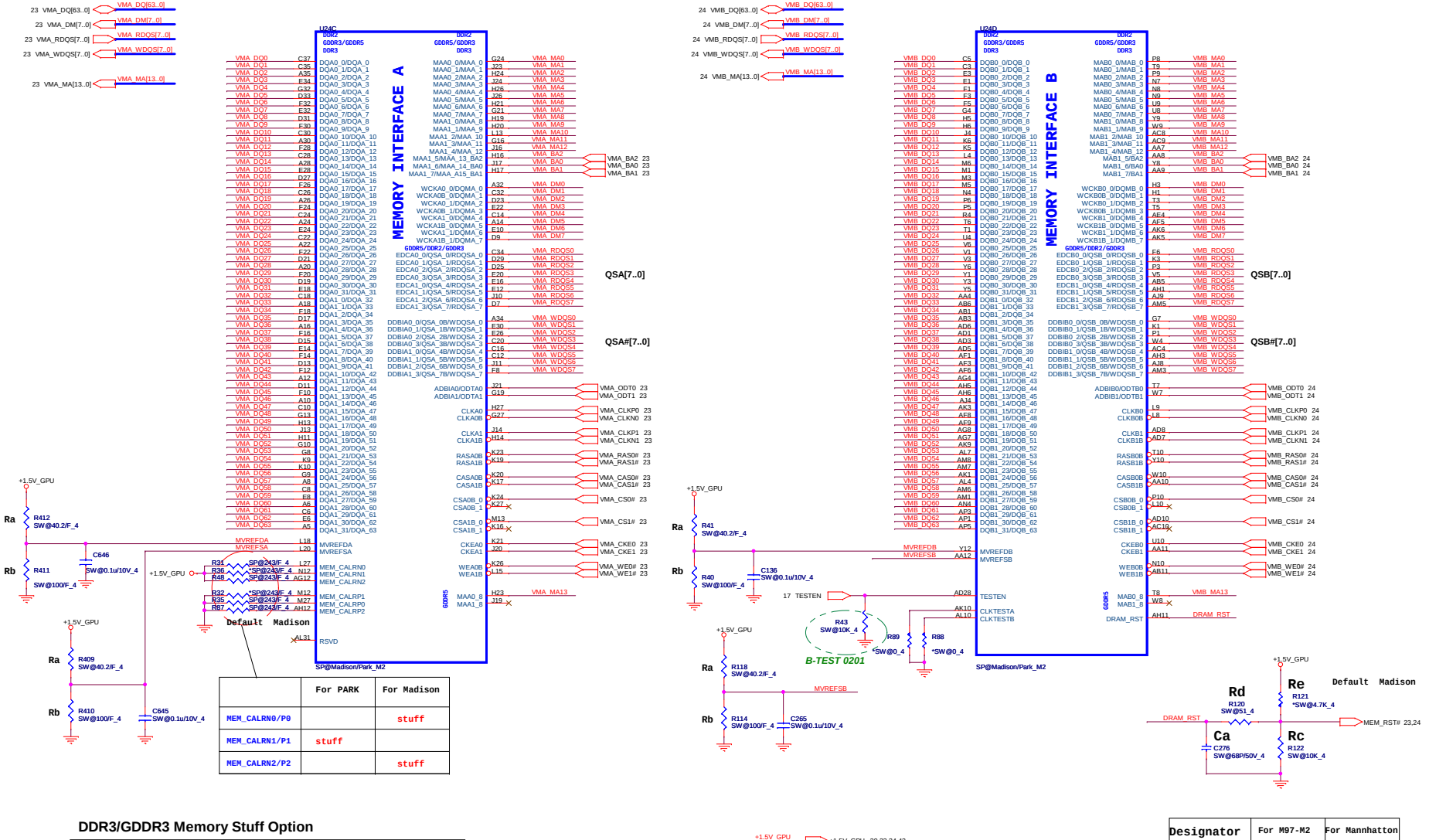

	For PARK	For Madison
MEM_CALRN0/P0		stuff
MEM_CALRN1/P1	stuff	
MEM_CALRN2/P2		stuff

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3(Default)
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

Designator	For M97-M2	For Mannhatton
Rc	10K	10K
Rd	0R/Short	51R
Re	DNI	DNI
Ca	2.2nF	68pF

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+1.5V_GPU
+1.8V_GPU
+1V
+VGPU_CORE
+VGPU_CORE
+3V

+1.5V_GPU 19,23,24,43
+1.8V_GPU 18,21,22,43
+1V 17,18,21,44
+VGPU_CORE 42
+VGPU_CORE 42
+3V 3,5,6,7,10,11,12,13,14,15,16,18,25,26,27,29,30,32,33,34,35,37,38,39,40,41,42,43,44

For DDR3, MVDDQ = 1.5V (7.5A)

+1.5V_GPU

C659 SW@10u/6.3V_6 C80 SW@10u/6.3V_6 C658 SW@10u/6.3V_6 C662 SW@10u/6.3V_6 C660 SW@10u/6.3V_6

C70 SW@1u/6.3V_4 C63 SW@1u/6.3V_4 C76 SW@1u/6.3V_4 C183 SW@1u/6.3V_4 C176 SW@1u/6.3V_4 C71 SW@1u/6.3V_4

C68 SW@1u/6.3V_4 C167 SW@1u/6.3V_4 C169 SW@1u/6.3V_4 C38 SW@1u/6.3V_4 C78 SW@1u/6.3V_4 C77 SW@1u/6.3V_4

C156 SW@1u/6.3V_4 C65 SW@0.1u/10V_4 C37 SW@0.1u/10V_4 C95 SW@0.1u/10V_4 C61 SW@0.1u/10V_4

U24E

MEM I/O

VDDR1#1 AC7
VDDR1#2 AD11
VDDR1#3 AE7
VDDR1#4 AG10
VDDR1#5 AJ7
VDDR1#6 AK8
VDDR1#7 AL9
VDDR1#8 G11
VDDR1#9 G14
VDDR1#10 G17
VDDR1#11 G20
VDDR1#12 G23
VDDR1#13 G26
VDDR1#14 G29
VDDR1#15 H10
VDDR1#16 J7
VDDR1#17 J9
VDDR1#18 K11
VDDR1#19 K13
VDDR1#20 K8
VDDR1#21 L12
VDDR1#22 L16
VDDR1#23 L21
VDDR1#24 L23
VDDR1#25 L26
VDDR1#26 L7
VDDR1#27 M11
VDDR1#28 N11
VDDR1#29 P7
VDDR1#30 R11
VDDR1#31 U11
VDDR1#32 U7
VDDR1#33 Y11
VDDR1#34 Y7

LEVEL TRANSLATION

VDD_CT#1 AF26
VDD_CT#2 AF27
VDD_CT#3 AG26
VDD_CT#4 AG27

I/O

VDDR3#1 AF23
VDDR3#2 AF24
VDDR3#3 AG23
VDDR3#4 AG24

VDDR4#4 AE13
VDDR4#5 AE15
VDDR4#7 AG13
VDDR4#8 AG15

VDDR4#1 AD12
VDDR4#2 AF11
VDDR4#3 AF12
VDDR4#6 AG11

NC_VDDRHA M20
NC_VSSRHA M21
NC_VDDRHB V12
NC_VSSRHB U12

PLL

PCIE_PVDD AB37
MPV18#1 H7
MPV18#2 H8
SPV18 AM10
SPV10 AN9
SPVSS AN10

VOLTAGE SENESE

FB_VDDC AF28
FB_VDDCI AG28
FB_GND AH29

SP@Madison/Park_M2

PCIE

PCIE_VDDR#1 AA31
PCIE_VDDR#2 AA32
PCIE_VDDR#3 AA33
PCIE_VDDR#4 AA34
PCIE_VDDR#5 V28
PCIE_VDDR#6 W29
PCIE_VDDR#7 W30
PCIE_VDDR#8 Y31

PCIE_VDDC#1 G30
PCIE_VDDC#2 G31
PCIE_VDDC#3 H29
PCIE_VDDC#4 H30
PCIE_VDDC#5 J29
PCIE_VDDC#6 J30
PCIE_VDDC#7 L28
PCIE_VDDC#8 M28
PCIE_VDDC#9 N28
PCIE_VDDC#10 R28
PCIE_VDDC#11 T28
PCIE_VDDC#12 U28

CORE

VDDC#1 AA15
VDDC#2 AA17
VDDC#3 AA20
VDDC#4 AA22
VDDC#5 AA24
VDDC#6 AA27
VDDC#7 AB16
VDDC#8 AB18
VDDC#9 AB21
VDDC#10 AB23
VDDC#11 AB26
VDDC#12 AB28
VDDC#13 AC17
VDDC#14 AC20
VDDC#15 AC22
VDDC#16 AC24
VDDC#17 AC27
VDDC#18 AD18
VDDC#19 AD21
VDDC#20 AD23
VDDC#21 AD26
VDDC#22 AF17
VDDC#23 AF20
VDDC#24 AF22
VDDC#25 AG16
VDDC#26 AG18
VDDC#27 AG21
VDDC#28 AH22
VDDC#29 AH27
VDDC#30 AH28
VDDC#31 M26
VDDC#32 N24
VDDC#33 N27
VDDC#34 R18
VDDC#35 R21
VDDC#36 R23
VDDC#37 R26
VDDC#38 T17
VDDC#39 T20
VDDC#40 T22
VDDC#41 T24
VDDC#42 T27
VDDC#43 U16
VDDC#44 U18
VDDC#45 U21
VDDC#46 U23
VDDC#47 U26
VDDC#48 V17
VDDC#49 V20
VDDC#50 V22
VDDC#51 V24
VDDC#52 V27
VDDC#53 Y16
VDDC#54 Y18
VDDC#55 Y21
VDDC#56 Y23
VDDC#57 Y26
VDDC#58 Y28

ISOLATED CORE I/O

VDDC#1 AA13
VDDC#2 AB13
VDDC#3 AC12
VDDC#4 AC15
VDDC#5 AD13
VDDC#6 AD16
VDDC#7 M15
VDDC#8 M16
VDDC#9 M18
VDDC#10 M23
VDDC#11 N13
VDDC#12 N15
VDDC#13 N17
VDDC#14 N20
VDDC#15 N22
VDDC#16 R12
VDDC#17 R13
VDDC#18 R16
VDDC#19 T12
VDDC#20 T15
VDDC#21 V15
VDDC#22 Y13

POWER

SP@Madison/Park_M2

+1.8V_GPU

L3 SW@HCB1608KF-181T15_6 180 ohm/1.5A

(1.8V@400mA PCIE_VDDR)

PCIE_VDDR

C139 SW@0.1u/10V_4 C138 SW@0.1u/10V_4 C129 SW@1u/6.3V_4 C124 SW@1u/6.3V_4 C153 SW@1u/6.3V_4 C130 SW@1u/6.3V_4 C150 SW@1u/6.3V_4 C157 SW@10u/6.3V_6

+1V

(1.0V@1.1A PCIE_VDDC)

C99 SW@1u/6.3V_4 C218 SW@1u/6.3V_4 C79 SW@1u/6.3V_4 C241 SW@1u/6.3V_4 C112 SW@1u/6.3V_4 C73 SW@1u/6.3V_4 C94 SW@1u/6.3V_4 C229 SW@10u/6.3V_6

+VGPU_CORE

(30A or more)

C102 SW@1u/6.3V_4 C106 SW@1u/6.3V_4 C131 SW@1u/6.3V_4 C133 SW@1u/6.3V_4 C103 SW@1u/6.3V_4 C172 SW@1u/6.3V_4 C159 SW@1u/6.3V_4 C100 SW@1u/6.3V_4 C101 SW@1u/6.3V_4 C147 SW@1u/6.3V_4

C194 SW@1u/6.3V_4 C193 SW@1u/6.3V_4 C161 SW@1u/6.3V_4 C141 SW@1u/6.3V_4 C187 SW@1u/6.3V_4 C180 SW@1u/6.3V_4 C166 SW@1u/6.3V_4 C117 SW@1u/6.3V_4 C165 SW@1u/6.3V_4 C181 SW@1u/6.3V_4

C152 SW@1u/6.3V_4 C170 SW@1u/6.3V_4 C143 SW@1u/6.3V_4 C188 SW@1u/6.3V_4 C164 SW@1u/6.3V_4 C120 SW@1u/6.3V_4 C116 SW@1u/6.3V_4 C146 SW@1u/6.3V_4 C127 SW@1u/6.3V_4 C110 SW@1u/6.3V_4

C144 SW@10u/6.3V_6 C121 SW@10u/6.3V_6 C142 SW@10u/6.3V_6 C122 SW@10u/6.3V_6 C91 SW@10u/6.3V_6 C123 SW@10u/6.3V_6

BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
(Separate Core power for PCIe bus macros
Connector to VDDCin non-ower-Xpress desingns ZR8

PIN different between Broadway and Madison		
Pin	Broadway	Madison
VDDC#32 / BIF_VDDC (N27)	VDDC	BIF_VDDC
VDDC#42 / BIF_VDDC (T27)	VDDC	BIF_VDDC
GND#61 / PX_EN (AL21)	GND	PX_EN
(AL31)	TS_A	NC_TS_A

+VGPU_CORE

(DDR3 1.12V@4A VDDCI) or more

C93 SW@1u/6.3V_4 C132 SW@1u/6.3V_4 C109 SW@1u/6.3V_4 C85 SW@1u/6.3V_4 C162 SW@1u/6.3V_4 C92 SW@1u/6.3V_4

C171 SW@10u/6.3V_6 C135 SW@10u/6.3V_6 C149 SW@10u/6.3V_6 C87 SW@1u/6.3V_4 C108 SW@1u/6.3V_4 C89 SW@1u/6.3V_4 C86 SW@1u/6.3V_4

+1.8V_GPU

L23 SW@BLM15BD121SN1_4 120 ohm/300mA

(1.8V@110mA VDD_CT)

VDDC_CT

C698 SW@10u/6.3_6 C184 SW@1u/6.3V_4 C173 SW@0.1u/10V_4

+3V_D

(3.3V@60mA))

C235 SW@10u/6.3V_6 C182 SW@1u/6.3V_4 C212 SW@1u/6.3V_4 C255 SW@1u/6.3V_4

+1.8V_GPU

L23 SW@BLM15BD121SN1_4 120 ohm/300mA

VDDR4

C274 SW@1u/6.3V_4 C273 SW@0.1u/10V_4

+1.8V_GPU

L69 SW@BLM15BD121SN1_4 120 ohm/300mA

(1.8V@40mA PCIE_PVDD)

PCIE_PVDD

C676 SW@10u/6.3V_6 C675 SW@1u/6.3V_4 C673 SW@0.1u/10V_4

+1.8V_GPU

L1 SW@BLM15BD121SN1_4 120 ohm/300mA

(1.8V@150mA MPV18)

MPV18

SPV18

SPV10

C58 SW@10u/6.3V_6 C66 SW@1u/6.3V_4 C60 SW@0.1u/10V_4

+1.8V_GPU

L19 SW@BLM15BD121SN1_4 120 ohm/300mA

(1.8V@75mA SPV18)

C261 SW@10u/6.3V_6 C249 SW@0.1u/10V_4

+1V

L20 SW@BLM15BD121SN1_4 120 ohm/300mA

(1.0V@120mA SPV10)

C262 SW@10u/6.3V_6 C250 SW@0.1u/10V_4

T4 T3 T6 T5 T9 T8 T10

U24F

AB39	PCIE_VSS#1	GND#1	A3
E39	PCIE_VSS#2	GND#2	A37
F34	PCIE_VSS#3	GND#3	AA16
F39	PCIE_VSS#4	GND#4	AA18
G33	PCIE_VSS#5	GND#5	AA2
G34	PCIE_VSS#6	GND#6	AA21
H31	PCIE_VSS#7	GND#7	AA23
H34	PCIE_VSS#8	GND#8	AA26
H39	PCIE_VSS#9	GND#9	AA28
J31	PCIE_VSS#10	GND#10	AA6
J34	PCIE_VSS#11	GND#11	AB12
K31	PCIE_VSS#12	GND#12	AB15
K34	PCIE_VSS#13	GND#13	AB17
K39	PCIE_VSS#14	GND#14	AB20
L31	PCIE_VSS#15	GND#15	AB22
L34	PCIE_VSS#16	GND#16	AB24
M34	PCIE_VSS#17	GND#17	AB27
M39	PCIE_VSS#18	GND#18	AC11
N31	PCIE_VSS#19	GND#19	AC13
N34	PCIE_VSS#20	GND#20	AC16
P31	PCIE_VSS#21	GND#21	AC18
P34	PCIE_VSS#22	GND#22	AC2
P39	PCIE_VSS#23	GND#23	AC21
R34	PCIE_VSS#24	GND#24	AC23
T31	PCIE_VSS#25	GND#25	AC26
T34	PCIE_VSS#26	GND#26	AC28
T39	PCIE_VSS#27	GND#27	AC6
U31	PCIE_VSS#28	GND#28	AD15
U34	PCIE_VSS#29	GND#29	AD17
V34	PCIE_VSS#30	GND#30	AD20
V39	PCIE_VSS#31	GND#31	AD22
W31	PCIE_VSS#32	GND#32	AD24
W34	PCIE_VSS#33	GND#33	AD27
Y34	PCIE_VSS#34	GND#34	AD9
Y39	PCIE_VSS#35	GND#35	AE2
		GND#36	AE6
		GND#37	AE10
		GND#38	AE16
		GND#39	AE18
		GND#40	AE21
		GND#41	AG17
		GND#42	AG2
		GND#43	AG20
		GND#44	AG22
		GND#45	AG6
		GND#46	AG9
		GND#47	AH21
		GND#48	AJ10
		GND#49	AJ11
		GND#50	AJ12
		GND#51	AJ28
		GND#52	AJ6
		GND#53	AK11
		GND#54	AK31
		GND#55	AK7
		GND#56	AL11
		GND#57	AL14
		GND#58	AL17
		GND#59	AL2
		GND#60	AL20
		GND#61	AL21
		GND#62	AL23
		GND#63	AL26
		GND#64	AL32
		GND#65	AL6
		GND#66	AL8
		GND#67	AM11
		GND#68	AM31
		GND#69	AM9
		GND#70	AN11
		GND#71	AN2
		GND#72	AN30
		GND#73	AN6
		GND#74	AN8
		GND#75	AP11
		GND#76	AP7
		GND#77	AP9
		GND#78	AR5
		GND#79	AW34
		GND#80	B11
		GND#81	B13
		GND#82	B15
		GND#83	B17
		GND#84	B19
		GND#85	B21
		GND#86	B23
		GND#87	B25
		GND#88	B27
		GND#89	B29
		GND#90	B31
		GND#91	B33
		GND#92	B7
		GND#93	B9
		GND#94	C1
		GND#95	C39
		GND#96	E35
		GND#97	E5
		GND#98	F11
		GND#99	F13

GND

VSS_MECH#1 A39
VSS_MECH#2 AW1
VSS_MECH#3 AW36

SP@Madison/Park_M2

GND#61/ PX_EN
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high '3.3V' will turn the regulators OFF. An output low '0V' will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.

R71 *SW@4.7K_4

B-TEST 0223

Pin AL21 to Ground for Broadway

GPU all PWROK

+3V

R112 SW@10K_4

R107 SW@10K_4

dGPU_PWROK 12

Q6 SW@2N7002K

+1.8V_GPU

Q4 SW@DTC144EUA

GPU +3V power

13 MXM_PWREN

R128 SW@0_4

+1.5V_GPU

R129 *SW@0_4

C279 *SW@1u/6.3V_4

R454 SW@4.7K_4

Q9 SW@ME2N7002E

B-TEST 0128

C-TEST 0323

Q0 change footprint from UMT_213-3-1_3 to SOT23_213-3_3-2

Q28 SW@AO3413

R449 *SW@0_6

C697 SW@10u/6.3V_6 C694 SW@1u/6.3V_4 C696 SW@0.1u/10V_4

0.5A

+3V_D

Q29 SP@AO3413

R453 *SP@0_6

R450 *SP@0_6

C727 SP@10u/6.3V_6 C711 SP@1u/6.3V_4 C728 SP@0.1u/10V_4

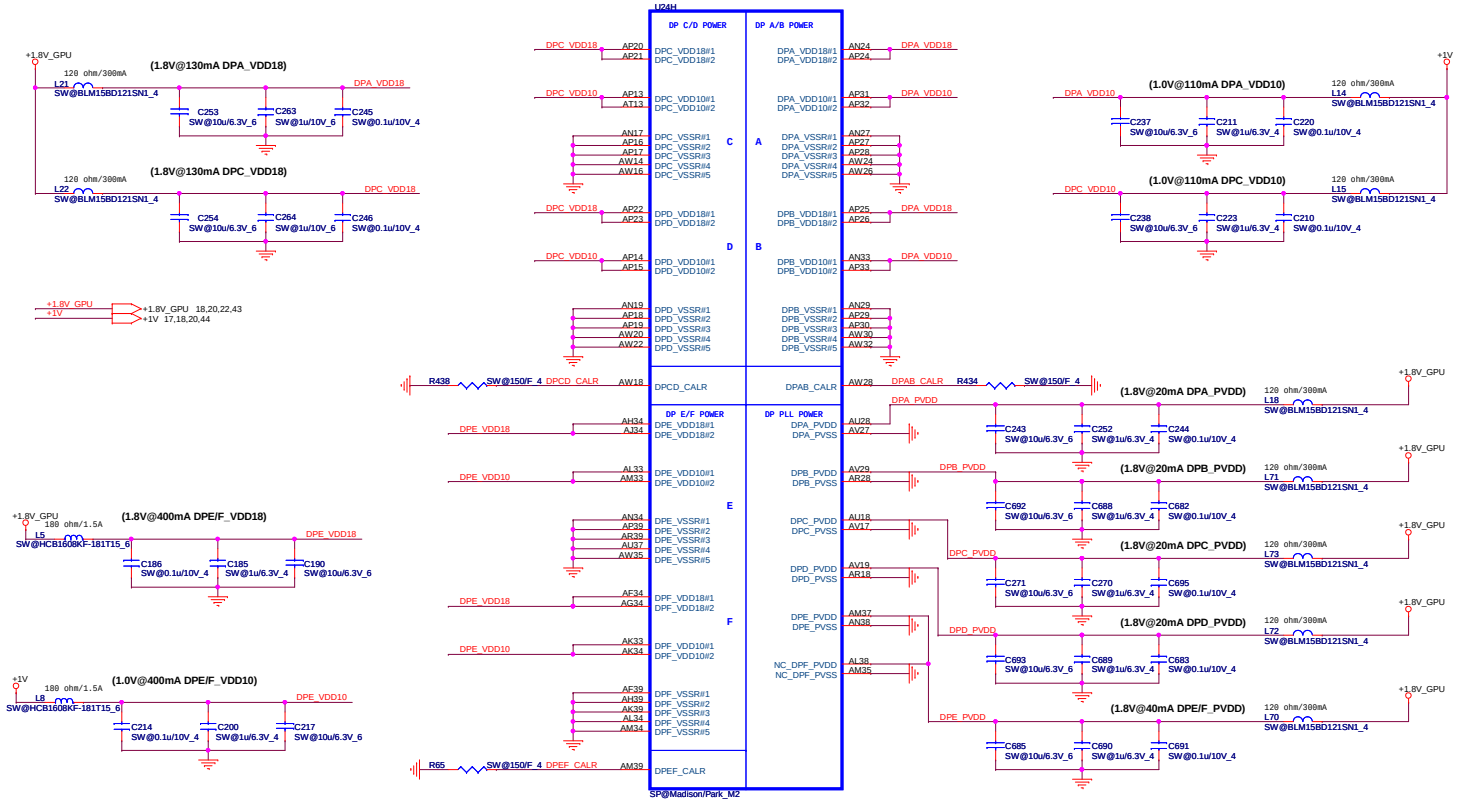
0.5A

+3V_D_EXT

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	Madison/Broadway PWR_GND	1A

Date: Monday, March 29, 2010 Sheet 20 of 48


U24H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
SP@Madison/Park_M2
+1.8V_GPU
(1.8V@130mA DPA_VDD18)
(1.8V@130mA DPC_VDD18)
(1.8V@400mA DPE/F_VDD18)
(1.0V@400mA DPE/F_VDD10)
(1.0V@110mA DPA_VDD10)
(1.0V@110mA DPC_VDD10)
(1.8V@20mA DPA_PVDD)
(1.8V@20mA DPB_PVDD)
(1.8V@20mA DPC_PVDD)
(1.8V@20mA DPD_PVDD)
(1.8V@40mA DPE/F_PVDD)
+1V
+1.8V_GPU 18,20,22,43
+1V 17,18,20,44
Quanta Computer Inc.
PROJECT : ZRA
Madison/Broadway DPPW_GND
Rev 1A
Date: Monday, March 29, 2010
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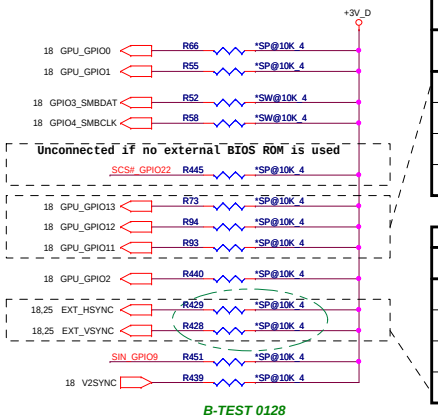
PIN STRAPS



B-TEST 0128

Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

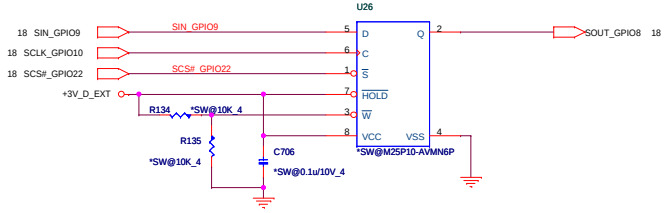
Function Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	(Recommended setting as 5.0 GT/s capability will be controlled by software.)
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable 1 = VGA controller capacity disenable (The device will not be recognized as the system's VGA controller.)	0	
VIP_DEVICE_STRAP_DIS	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET. 1 = DRIVER would use the value sample on VHAD_0 during RESET.	0	

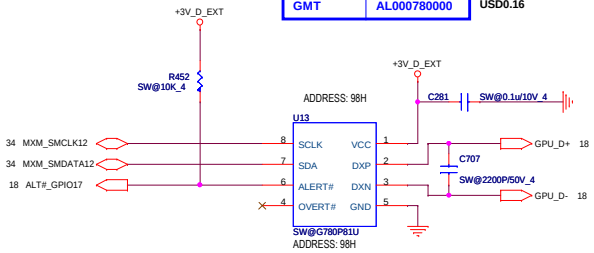
SERIAL ROM *Default don't put*



Thermal Sensor

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

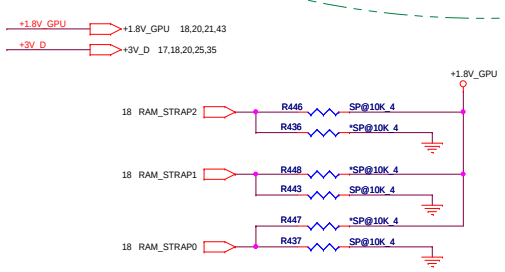
USD0.16



DDR3 Memory Aperture size

DDR3 Memory Aperture size						
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C		512Mb			
		AKD5LZGTW04 (64M*16)	1Gb	1	0	0
			2Gb			
Samsung	K4W1G1646E-HC12		512Mb			
		AKD5LGGT506 (64M*16)	1Gb	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2Gb			
AMD	23EY2387MA12-SZ	AKD5LGGT700	1Gb	0	1	0

B-TEST 0128



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	Memory strip/Thermal/HDCP	1A
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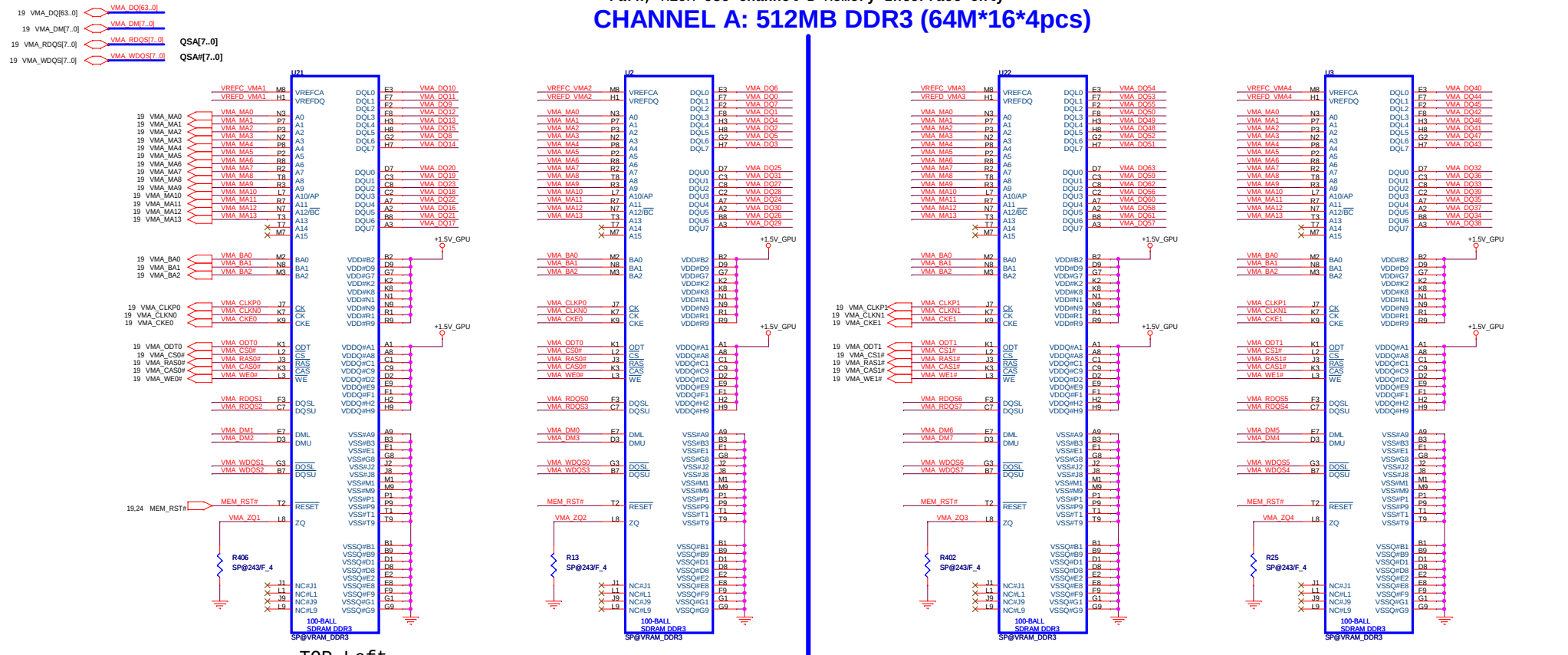
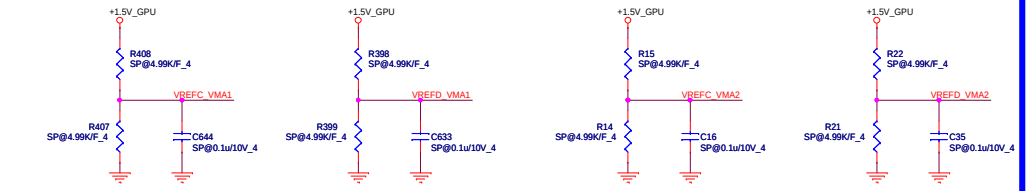
Park, M29M Use Channel B Memory Interface Only

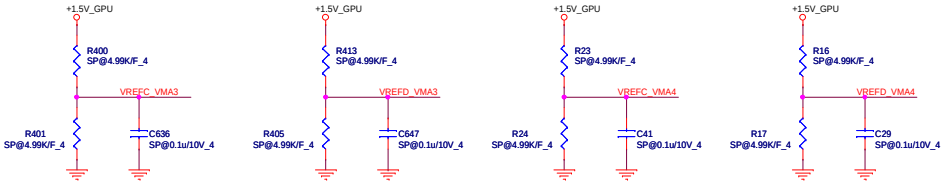
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



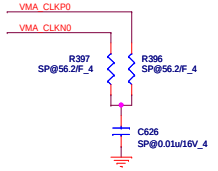
Group-A0 VREF



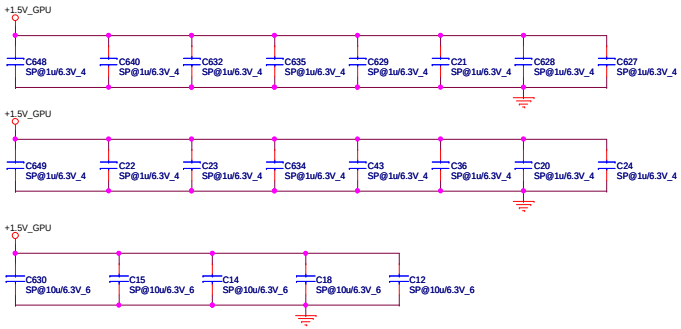
Group-A1 VREF



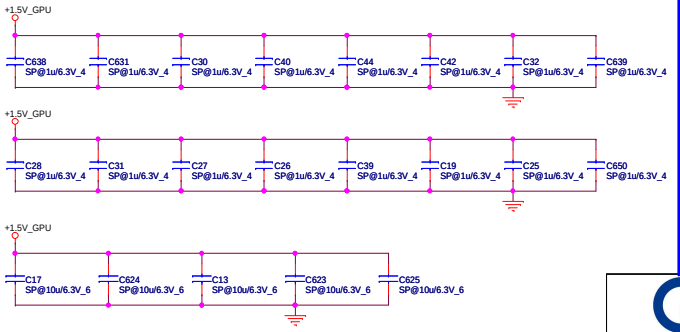
MEM_A0 CLK



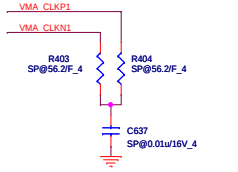
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



Quanta Computer Inc.

PROJECT : ZRA

Size	Document Number	Rev
	VRAM_A: DDR3-64M*16*4PCS	1A

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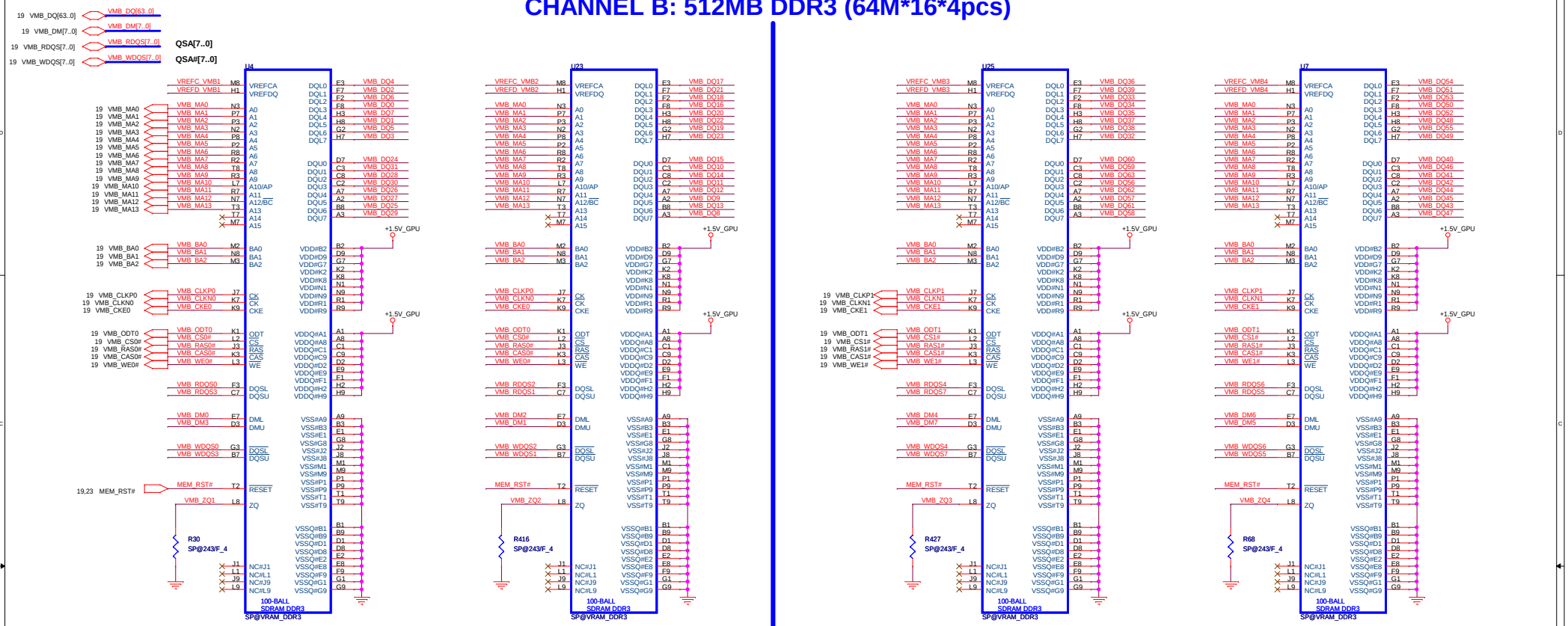
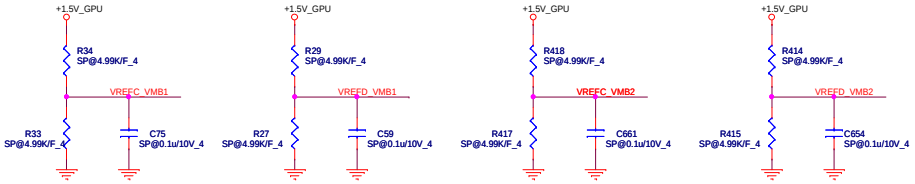
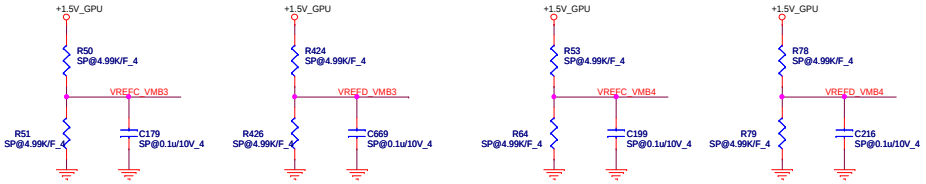
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



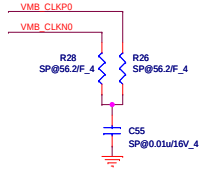
Group-B0 VREF



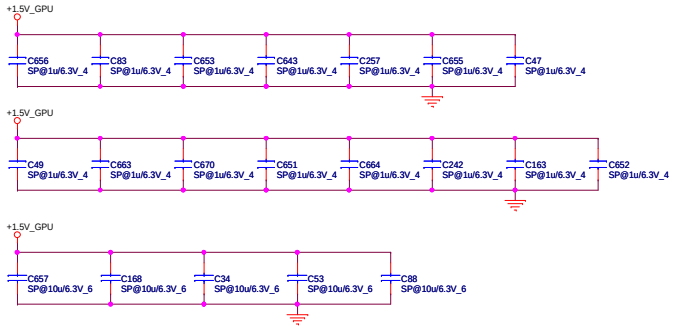
Group-B1 VREF



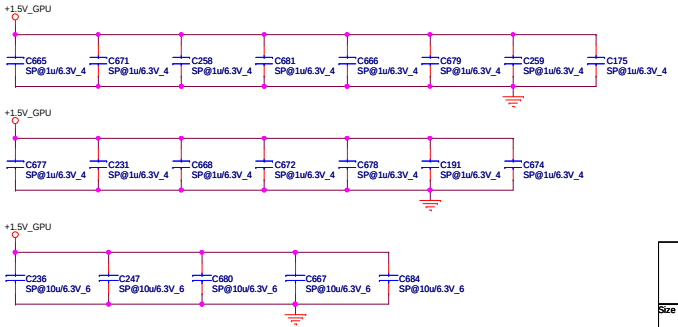
MEM_B0 CLK



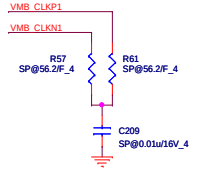
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	VRAM_B: DDR3-64M*16*4PCS	1A
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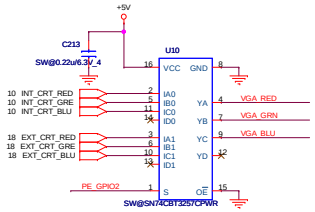
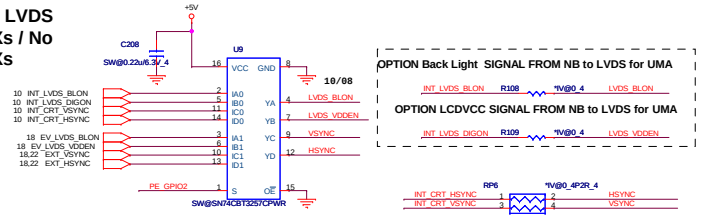
CRT MUXs / No MUXs



S	Yn
0	IV
1	SW(EV)

OPTION SIGNAL FROM NB to CRT for UMA

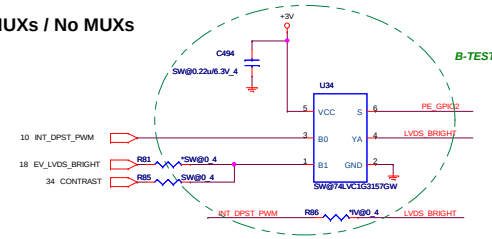
CRT LVDS MUXs / No MUXs



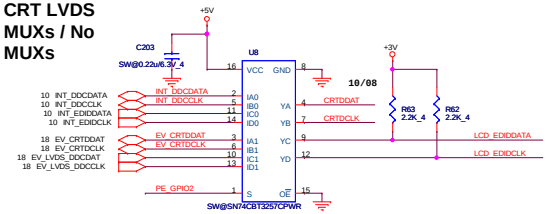
OPTION Back Light SIGNAL FROM NB to LVDS for UMA

OPTION LCDVCC SIGNAL FROM NB to LVDS for UMA

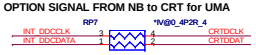
LVDS MUXs / No MUXs



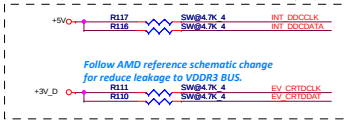
CRT LVDS MUXs / No MUXs



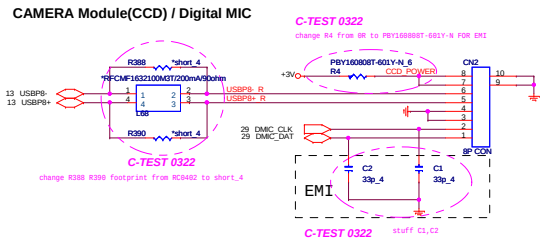
OPTION SIGNAL FROM NB to CRT for UMA



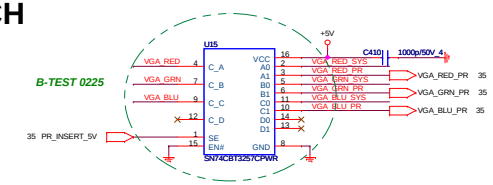
A-test 確認 R7467 R7468 R7295 R7469是否可以不上件



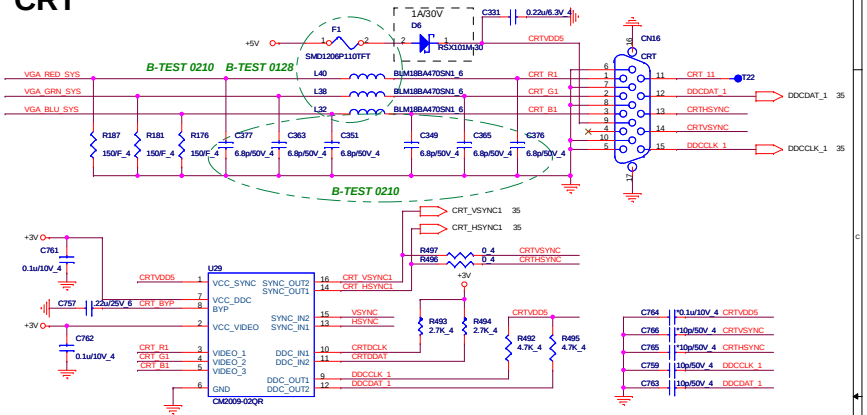
CAMERA Module(CCD) / Digital MIC



CRT SWITCH



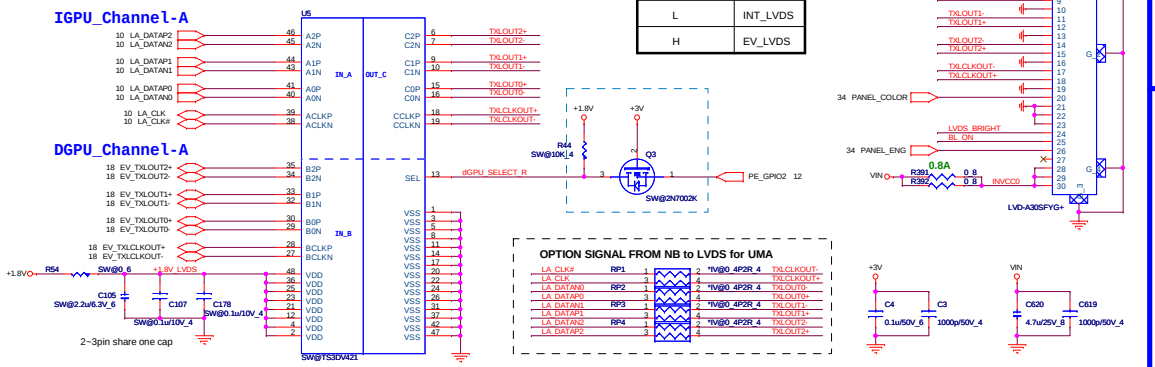
CRT



LVDS MUXs / No MUXs

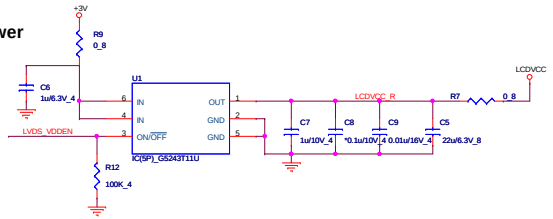
TI	AL3DV421V00
Pericom	AL000412W00

PE_GPIO2	Output
L	INT_LVDS
H	EV_LVDS

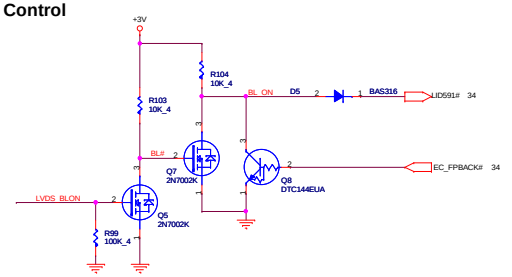


OPTION SIGNAL FROM NB to LVDS for UMA

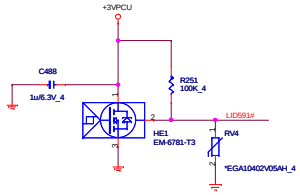
LCD Power



Backlight Control



Lid Switch (HSR)



AL006781000 no need pull high R. USD 0.053
AL003661003 need pull high 100K. USD 0.05
AL002648034 need pull high 100K. USD 0.048

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	CRT/LVDS/CCD/DIG MIC	1A

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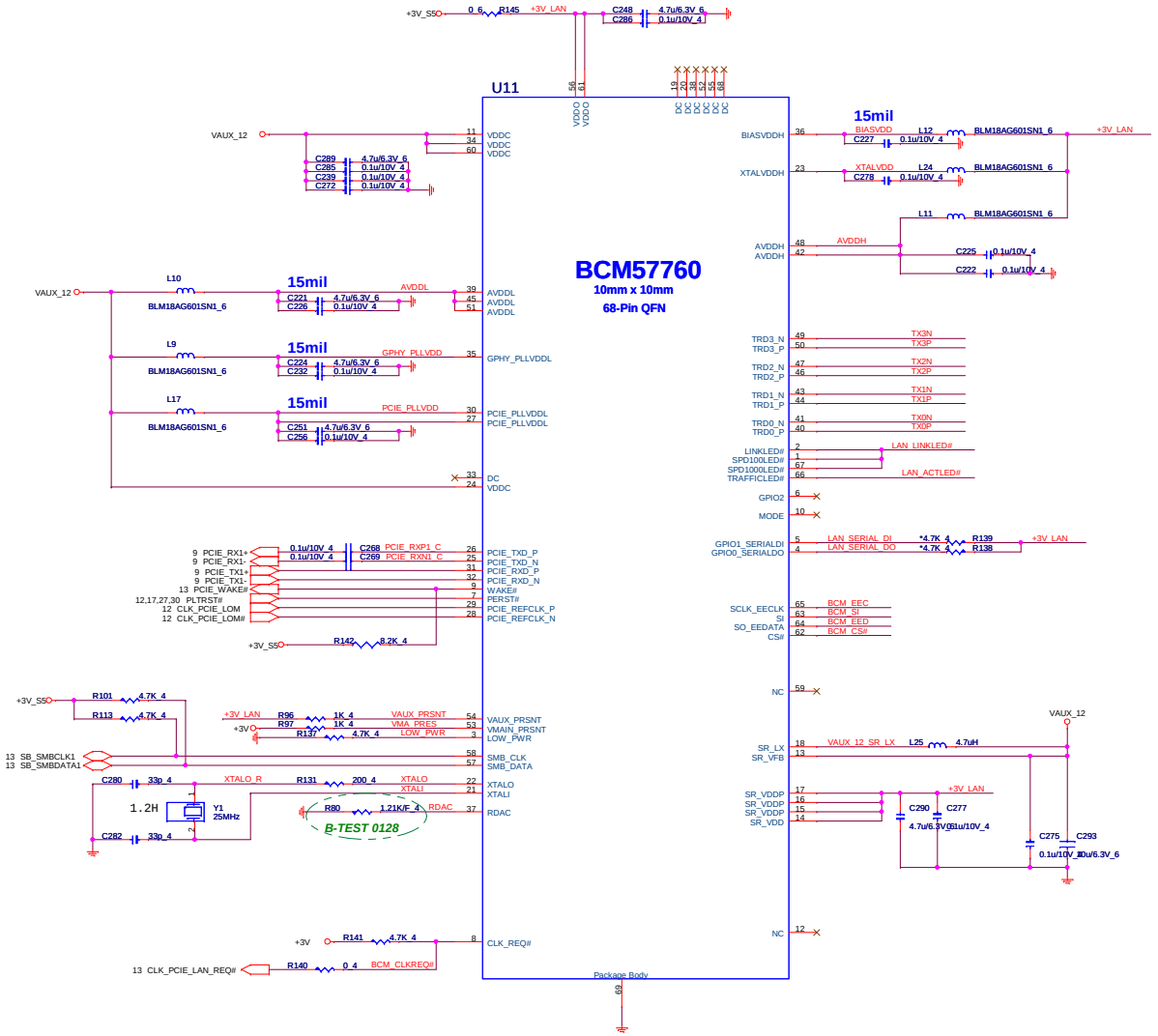
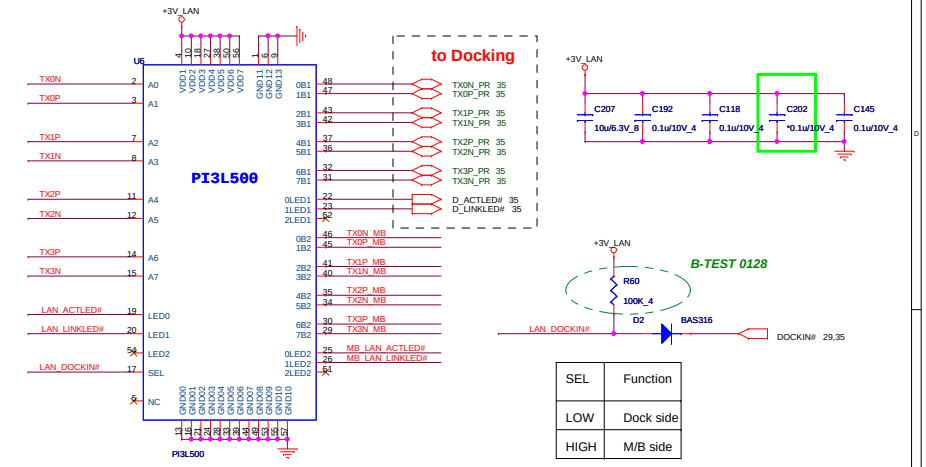
Giga-LAN BCM57760(LAN)

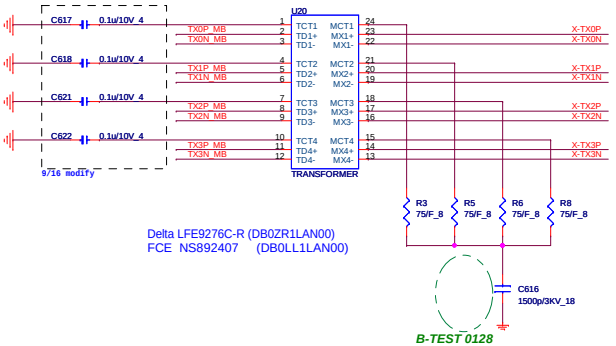


LAN SWITCH



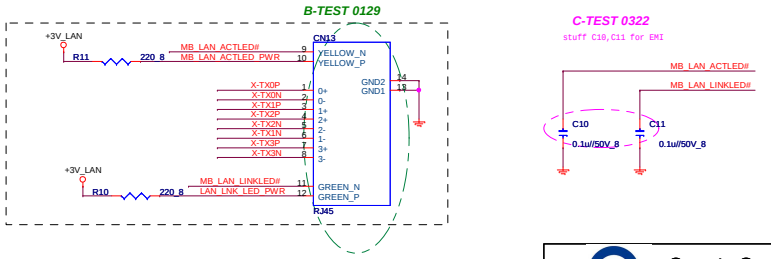
SEL	Function
LOW	Dock side
HIGH	M/B side

TRANSFORMER

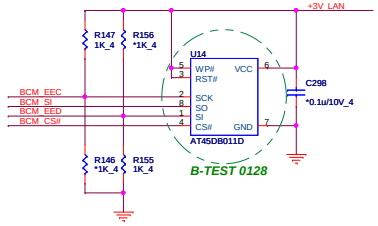


Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)

RJ45(LAN)



Flash (1M) for ASF2.0



Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	LAN (BCM57760)	1A

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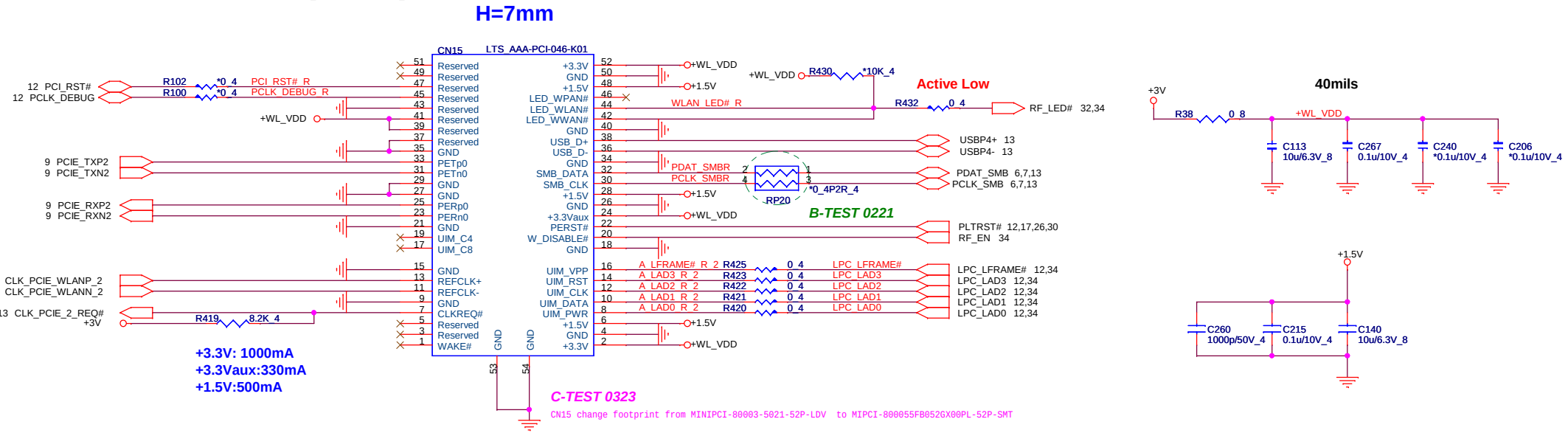
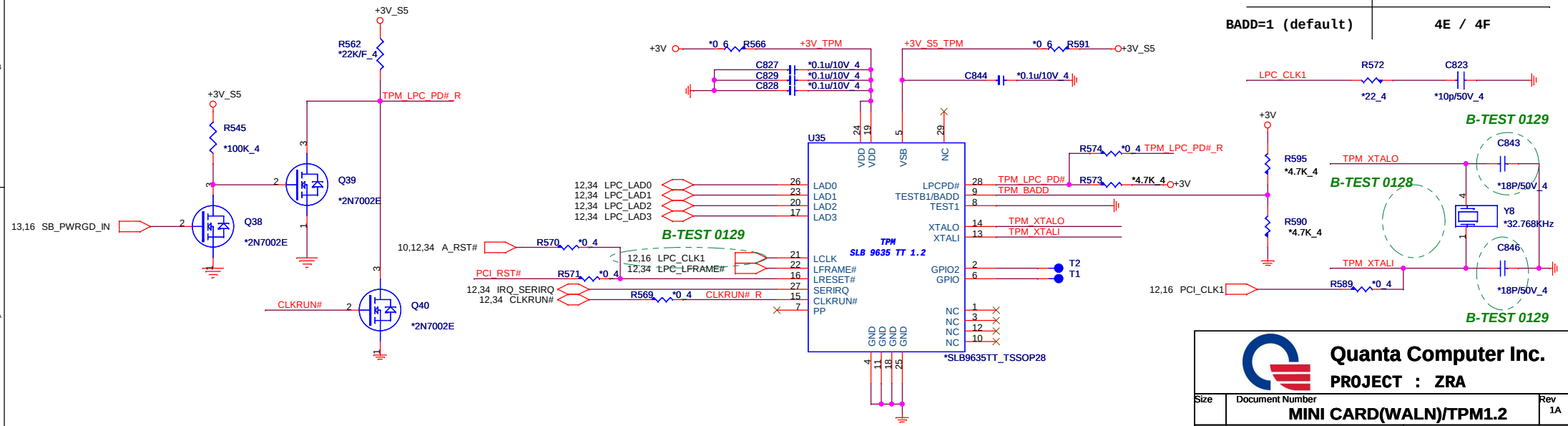
MINI-CARD WLAN(MPC)



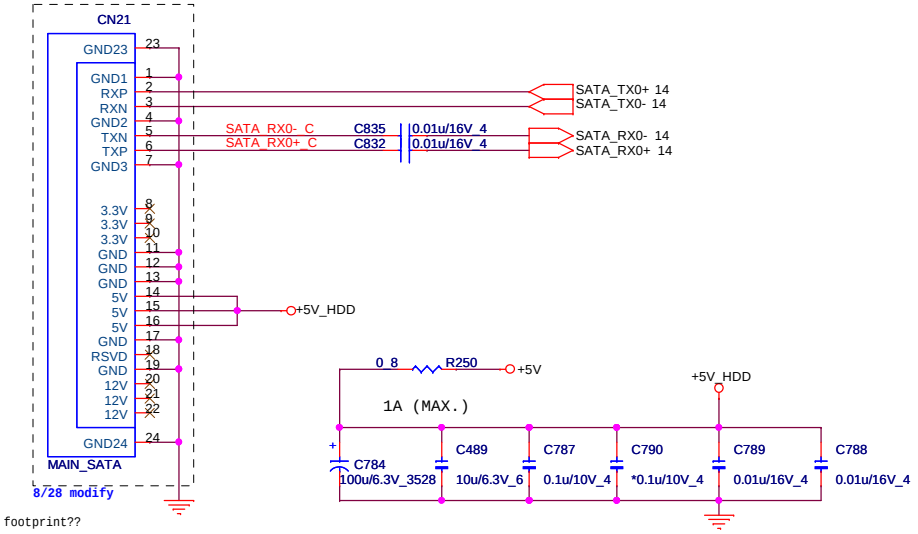
TPM

Resiger Base Address	
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F

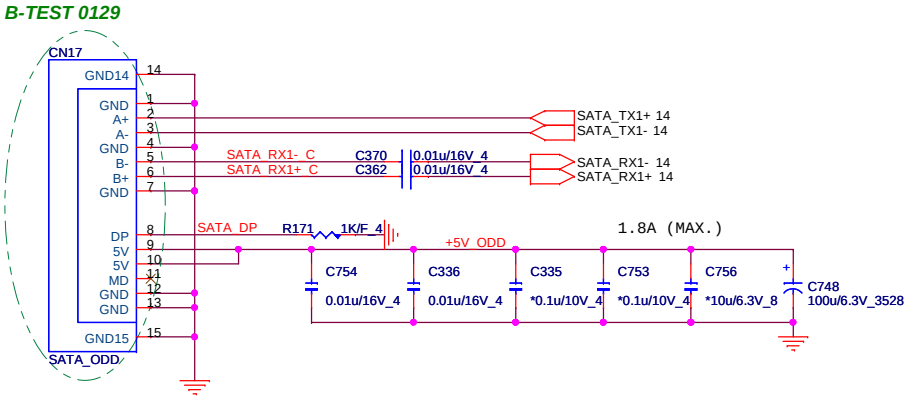


Quanta Computer Inc.			
PROJECT : ZRA			
Size	Document Number		Rev
	MINI CARD(WALN)/TPM1.2		1A
Date: Monday, March 29, 2010		Sheet 27 of 48	

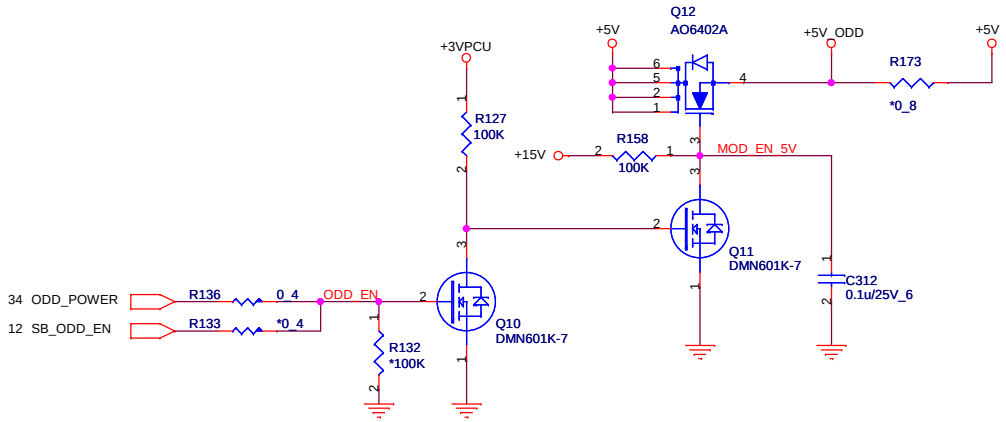
SATA HDD(HDD)



SATA ODD (ODD)



ODD POWER(ODD)



Quanta Computer Inc.		
PROJECT : ZRA		
Size	Document Number: SATA-HDD/ODD	Rev: 1A
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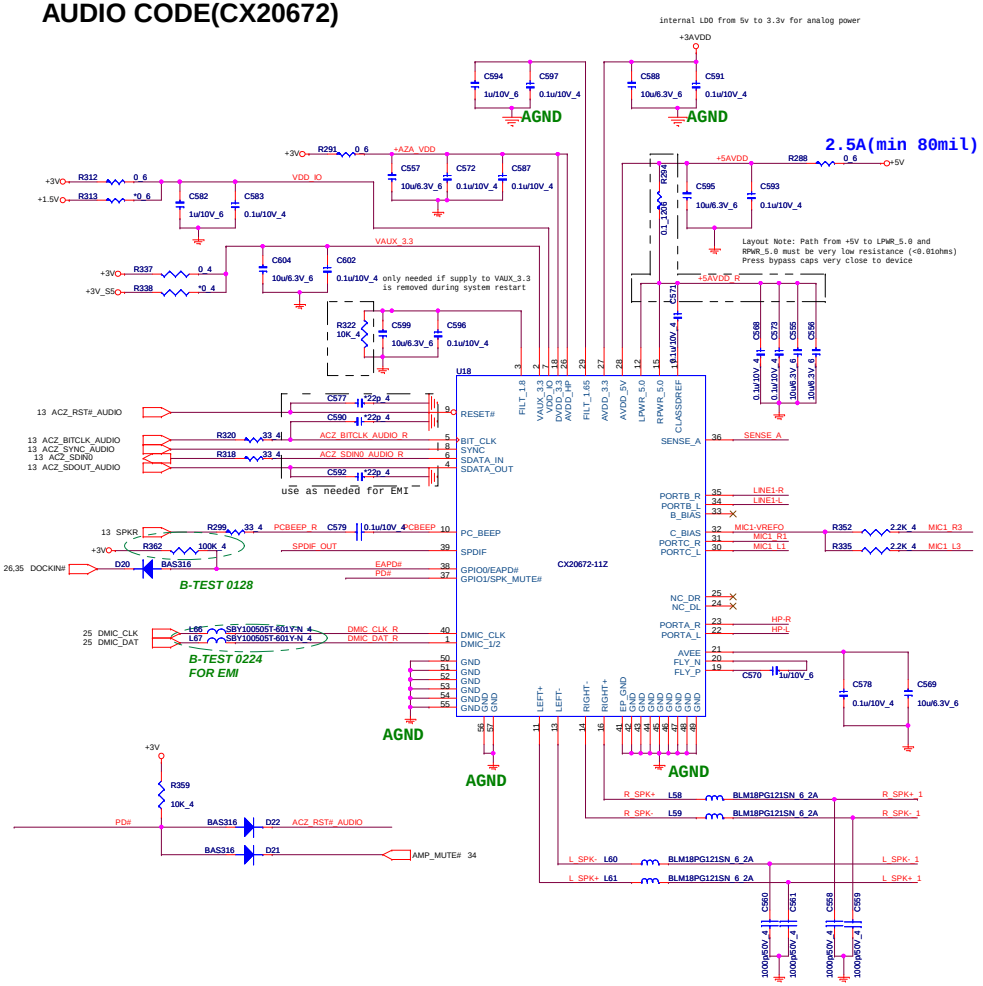
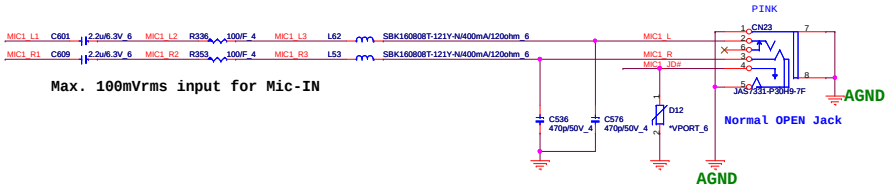
AUDIO CODE(CX20672)

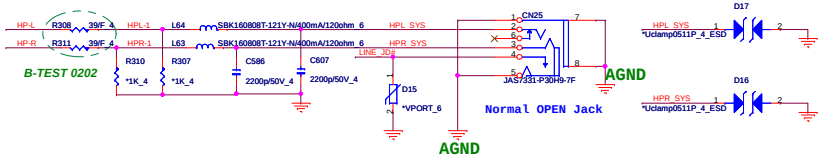


EXTERNAL MIC

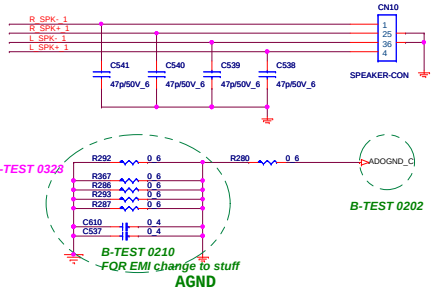


Max. 100mVrms input for Mic-IN

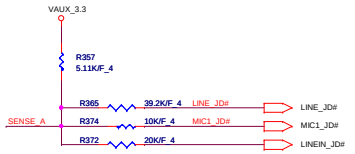
LINE-OUT/SPDIFO(AMP)



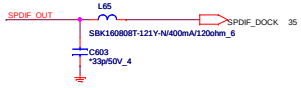
INT SPEAKER CONN

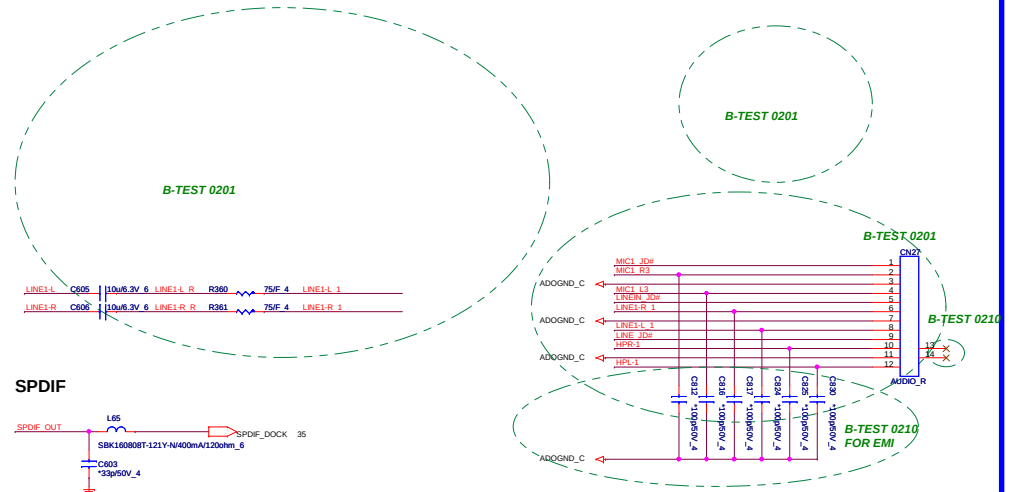


Jack Detect Resistor

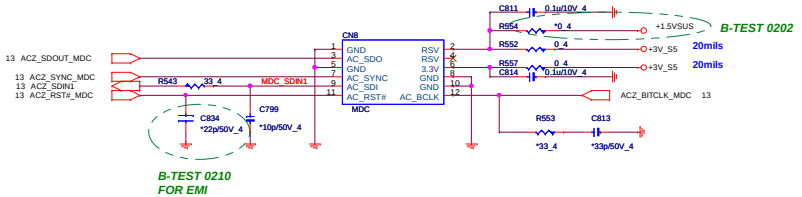


SPDIF





MDC Module



Quanta Computer Inc.

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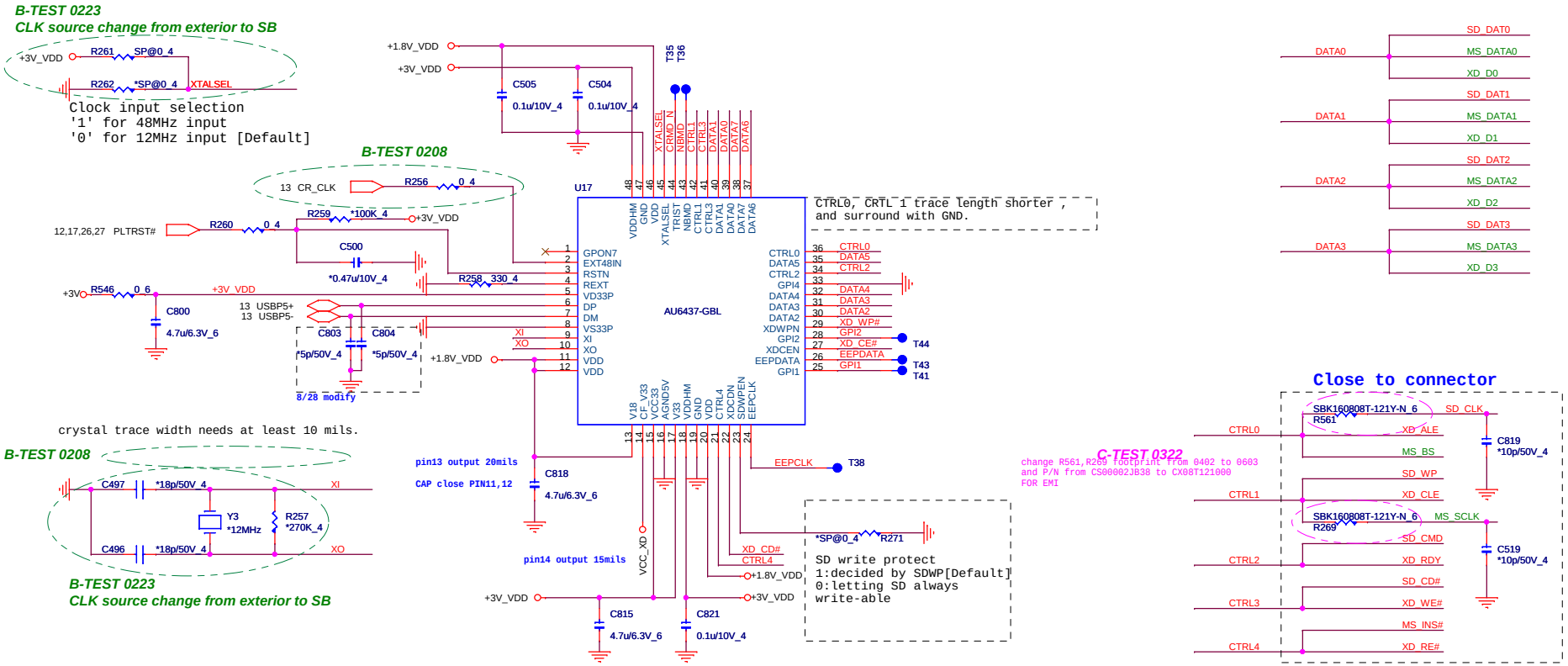
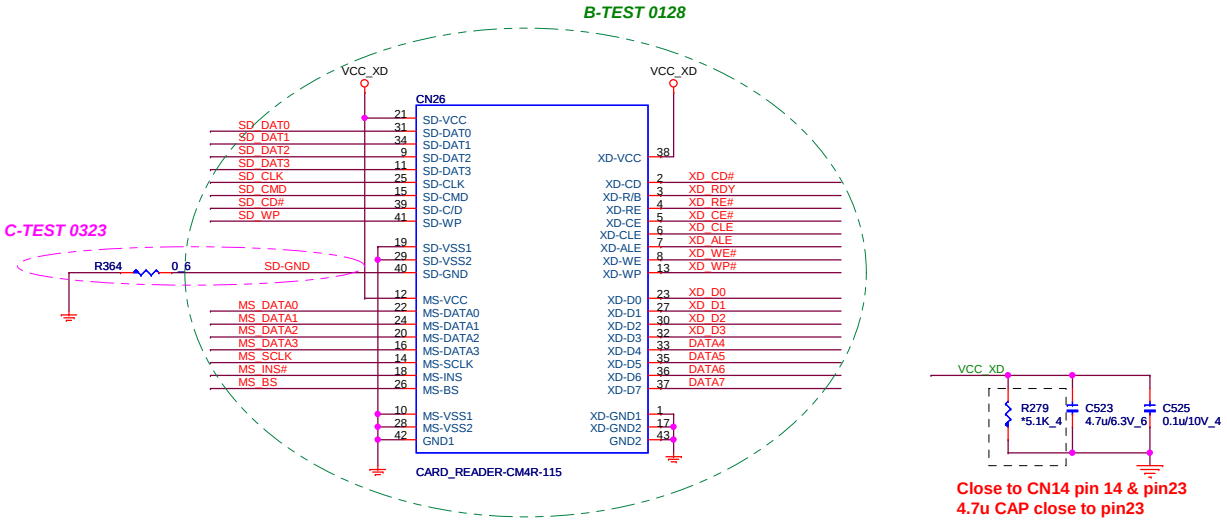
CARD READER (AU6437)



4 IN 1 CARD READER (MMC)



Quanta Computer Inc.		
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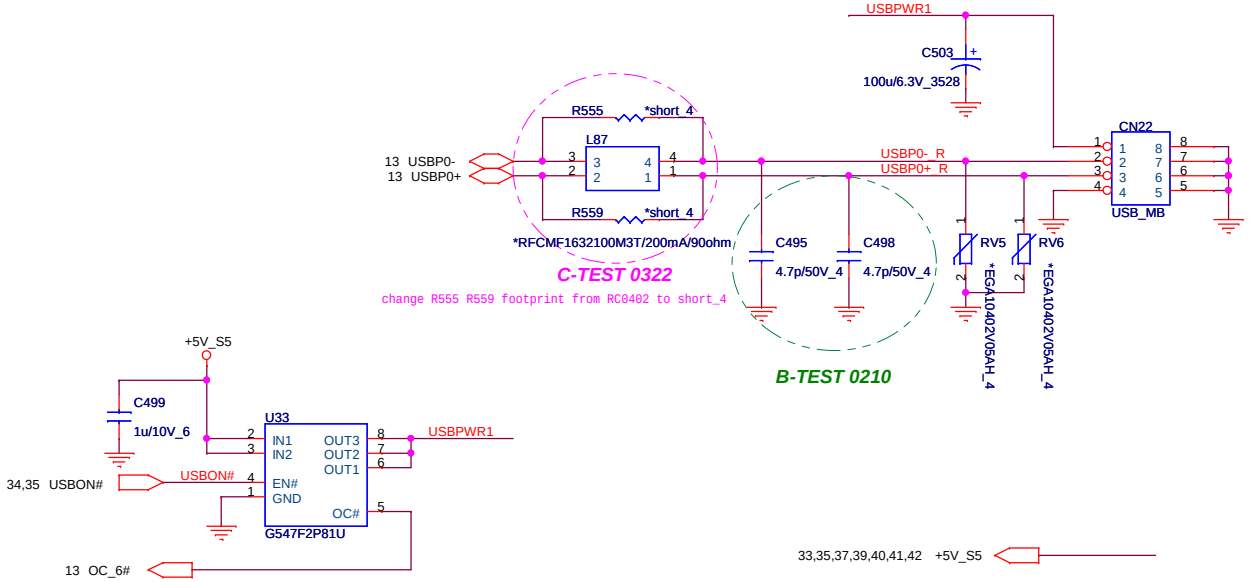
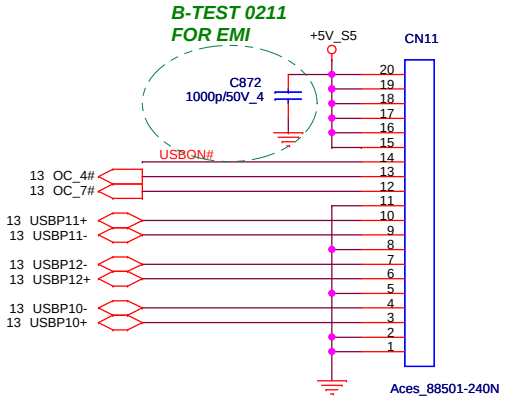
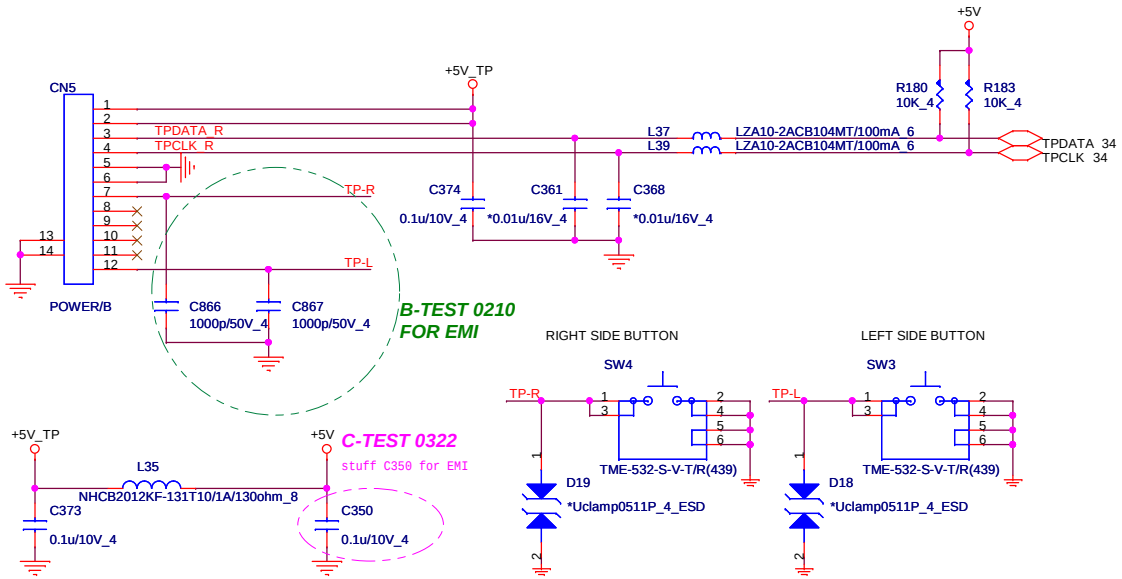
USB PORT(USB)



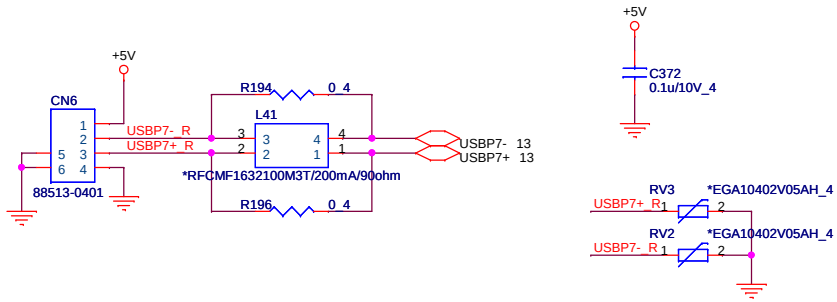
USB BOARD CONN(USB)



Touch Pad



Finger Print



Quanta Computer Inc.

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Size	Document Number	Rev
	USB/USB DB/TP/FP	1A

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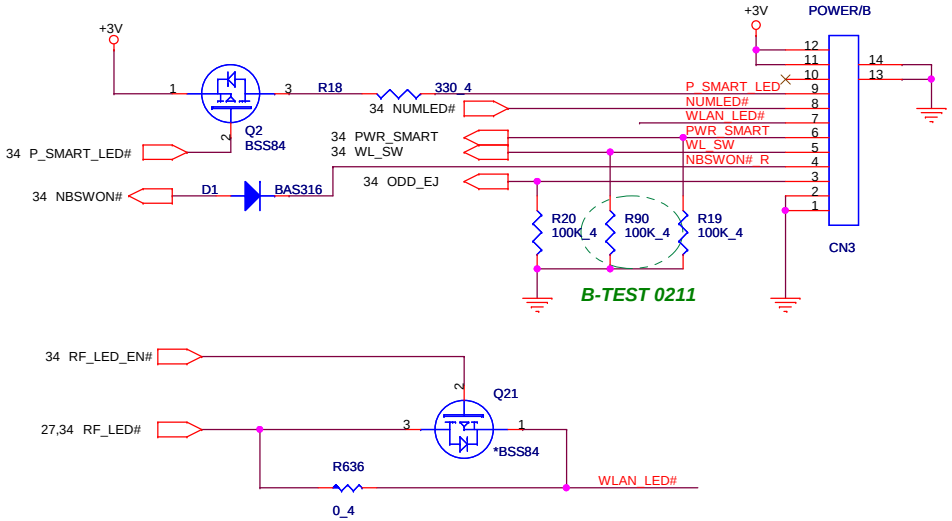
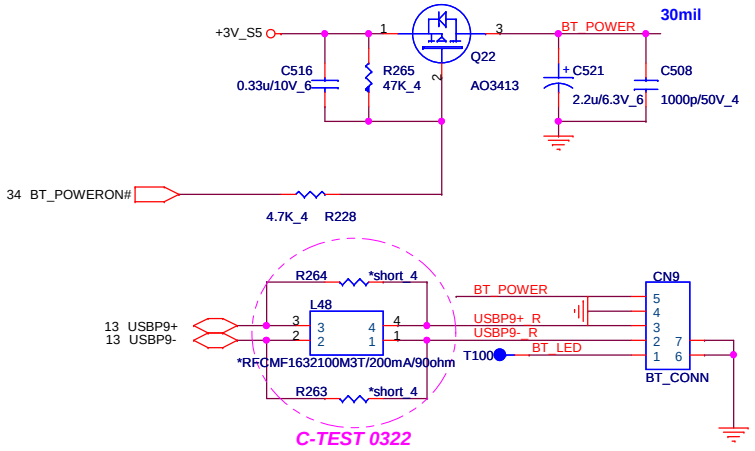
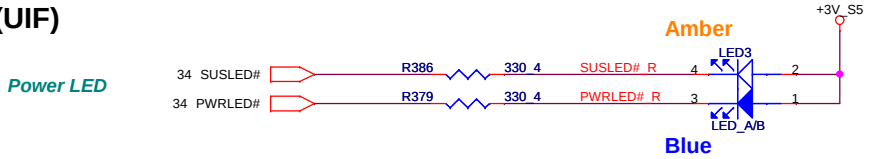
POWER DB CONN(UIF)

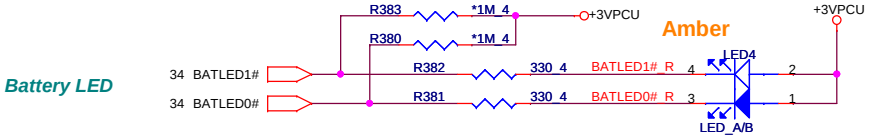


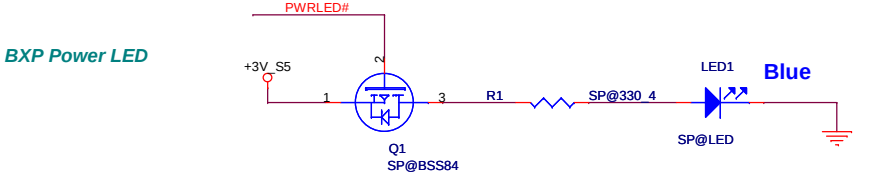
BLUETOOTH CONN(BTM)

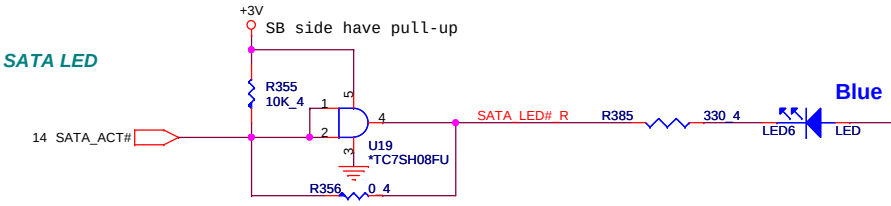


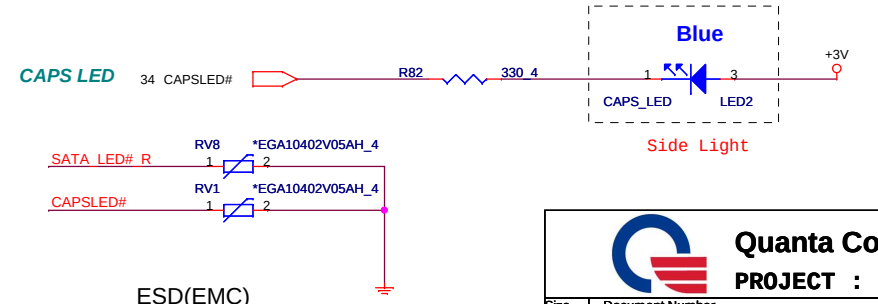
LED(UIF)











ESD(EMC)

Quanta Computer Inc.

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	PWR DB/BT/LED	1A
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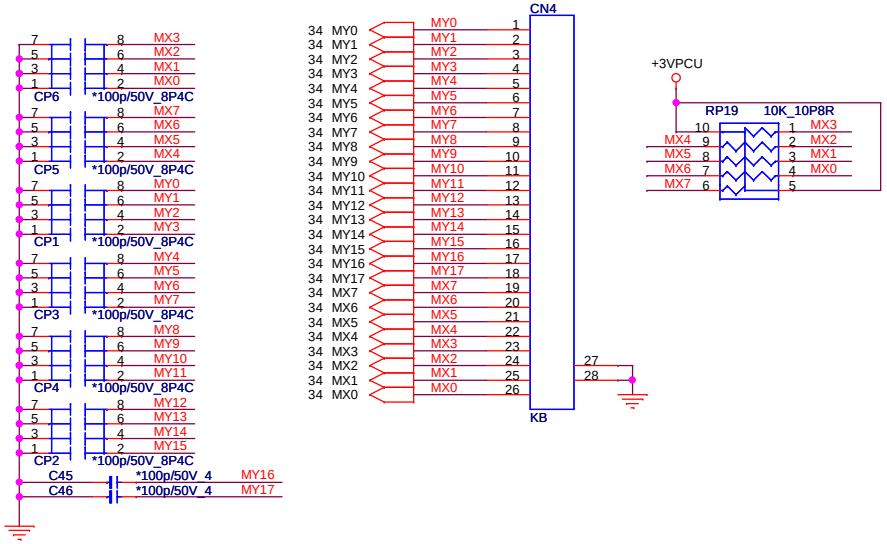
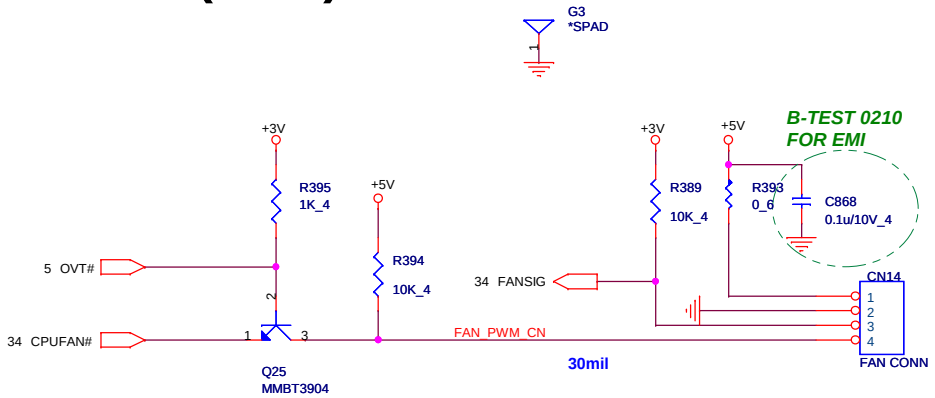
K/B(KBC)

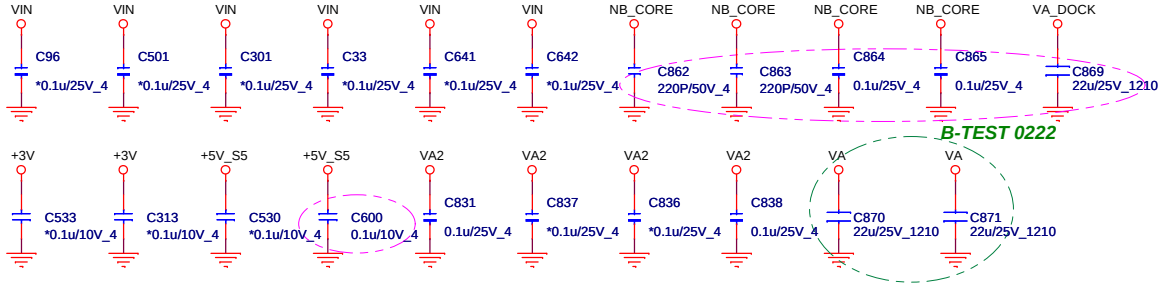


CPU FAN(THM)

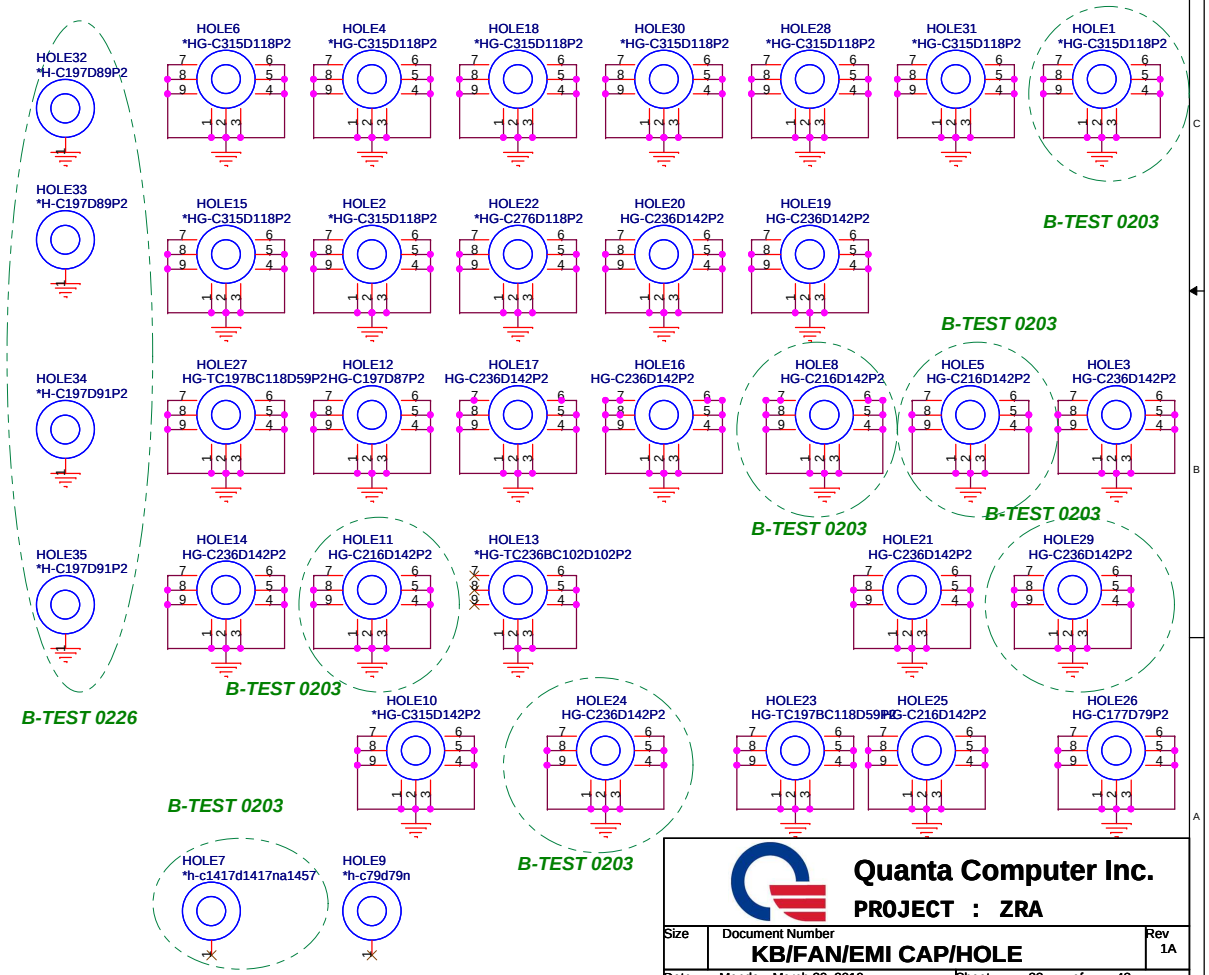


EMI CAP

C-TEST 0322 stuff C862,C863,C864,C865,C600,C869,C831,C838



HOLE(OTH)



Quanta Computer Inc.		
PROJECT : ZRA		
Size	Document Number	Rev
	KB/FAN/EMI CAP/HOLE	1A
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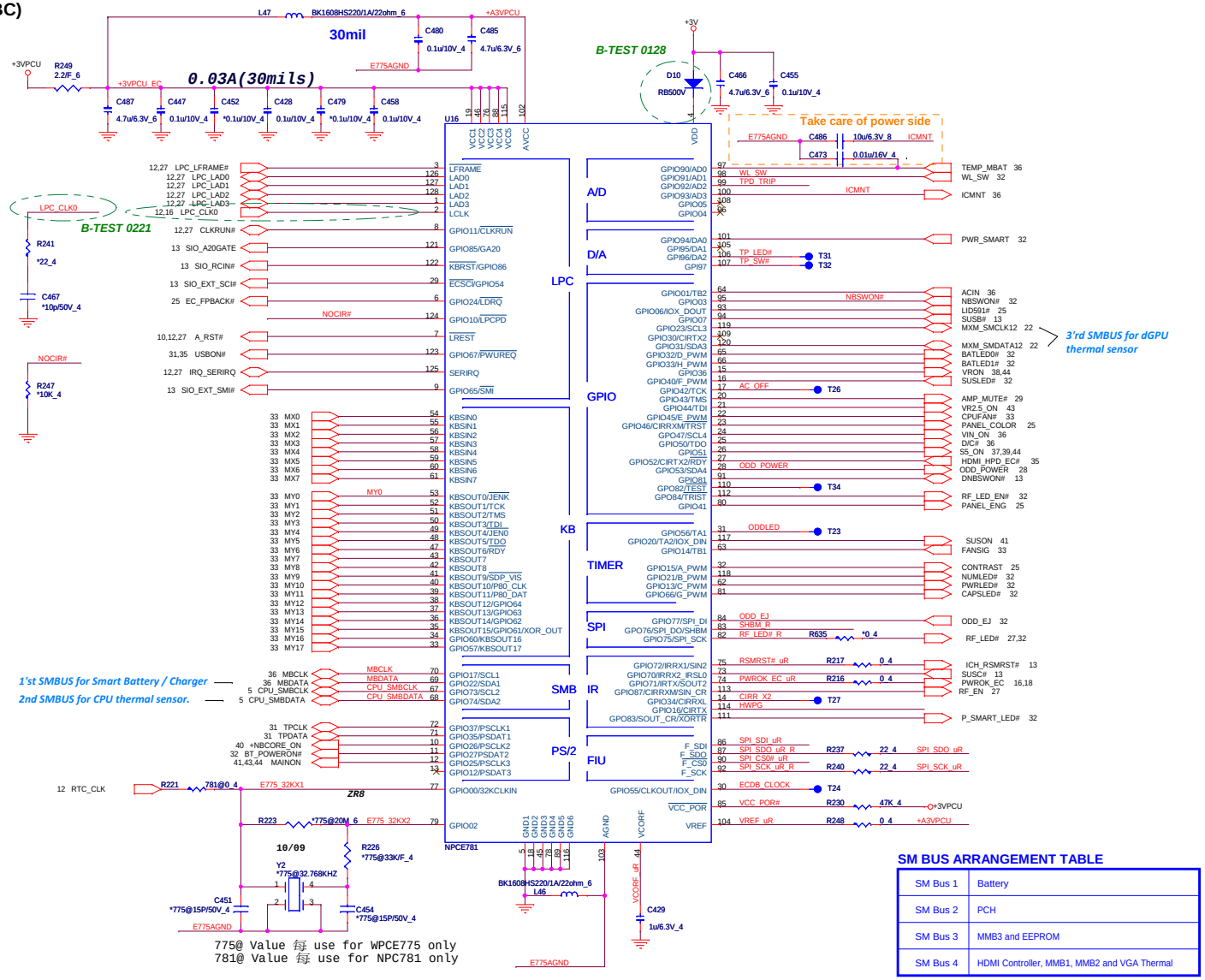
EC(KBC)



SM BUS ARRANGEMENT TABLE

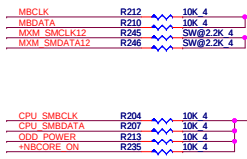
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal

I/O ADDRESS SETTING(KBC)

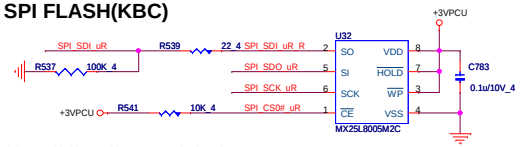
SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

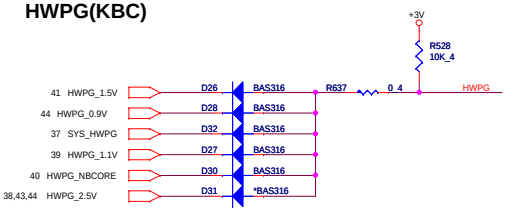


SPI FLASH(KBC)

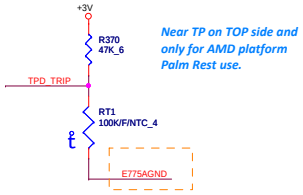


If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG(KBC)

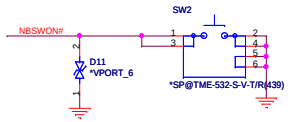


Palm Rest Thermal Sensor(THM)



Near TP on TOP side and only for AMD platform Palm Rest use.

POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.
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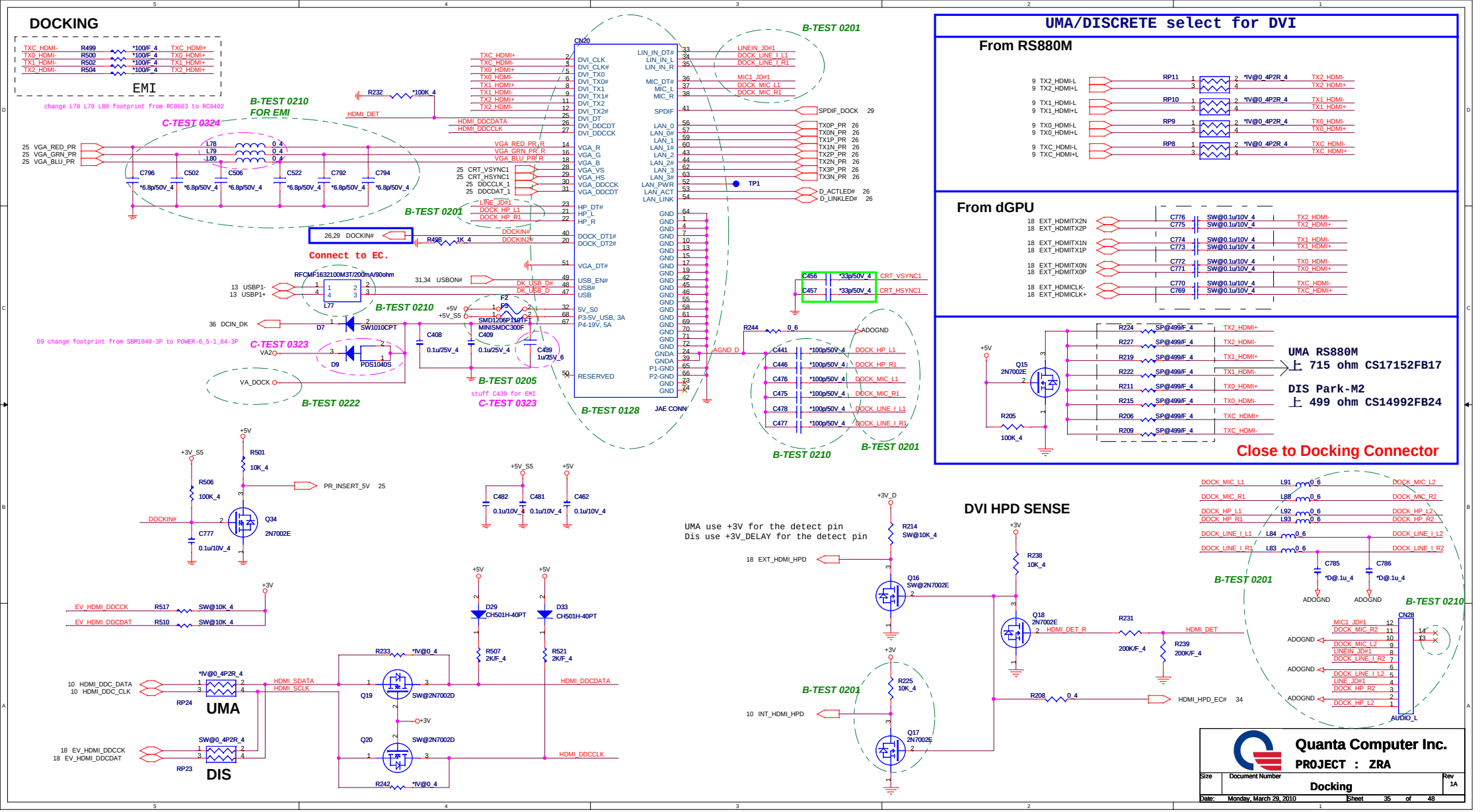
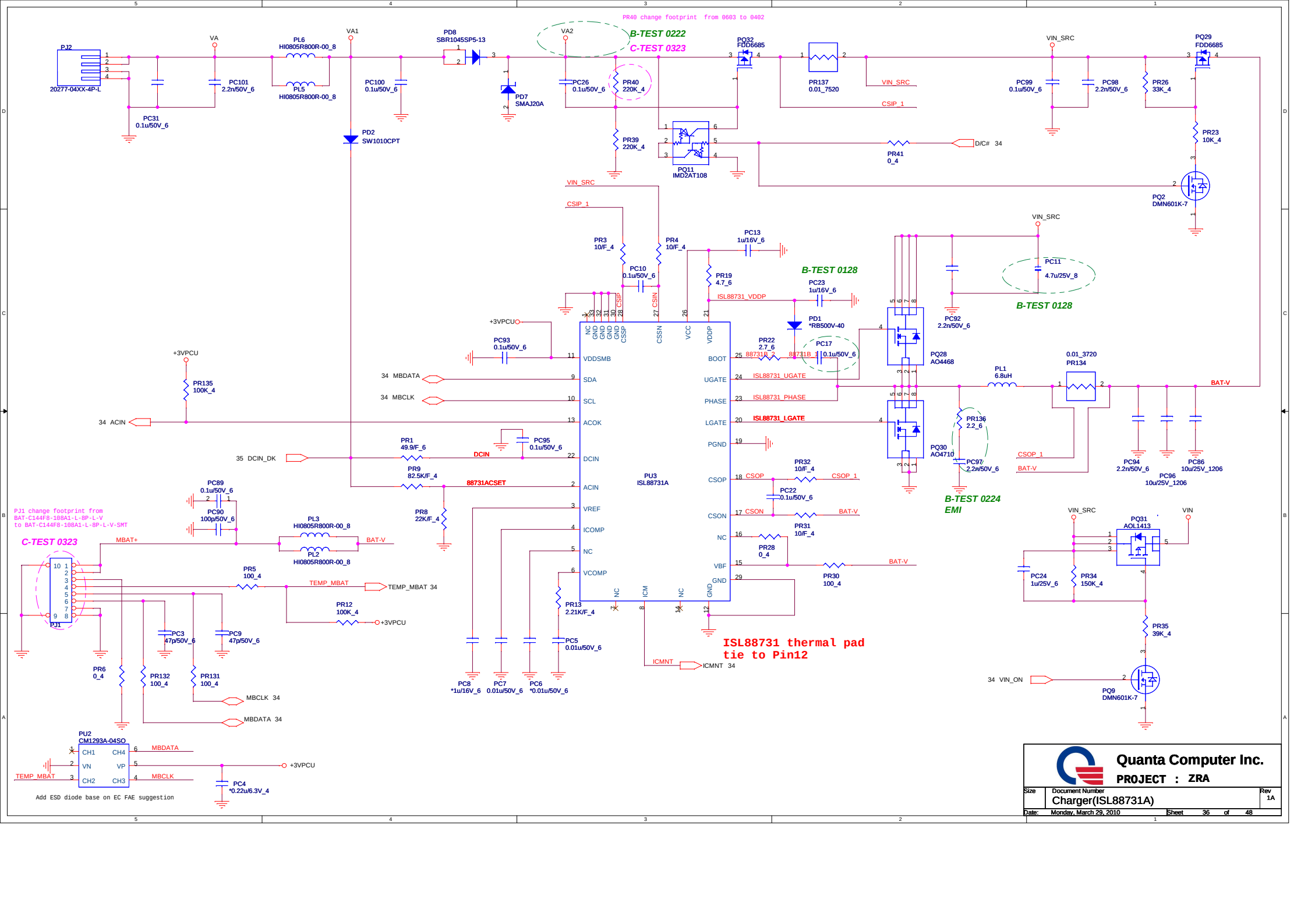

DOCKING
EMI
B-TEST 0210
FOR EMI
C-TEST 0324
B-TEST 0201
B-TEST 0210
C-TEST 0323
B-TEST 0205
B-TEST 0222
B-TEST 0128
JAE CONN
Connect to EC.
UMA/DISCRETE select for DVI
From RS880M
From dGPU
UMA RS880M
上 715 ohm CS17152FB17
DIS Park-M2
上 499 ohm CS14992FB24
Close to Docking Connector
DVI HPD SENSE
UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin
UMA
DIS
Quanta Computer Inc.
PROJECT : ZRA
Docking
Monday, March 29, 2010


PR40 change footprint from 0603 to 0402
B-TEST 0222
C-TEST 0323
B-TEST 0128
B-TEST 0224
EMI
PJ1 change footprint from BAT-C144F8-108A1-L-8P-L-V to BAT-C144F8-108A1-L-8P-L-V-SMT
ISL88731 thermal pad tie to Pin12
Add ESD diode base on EC FAE suggestion
PU3 ISL88731A
Quanta Computer Inc.
PROJECT : ZRA
Charger(ISL88731A)
Monday, March 29, 2010
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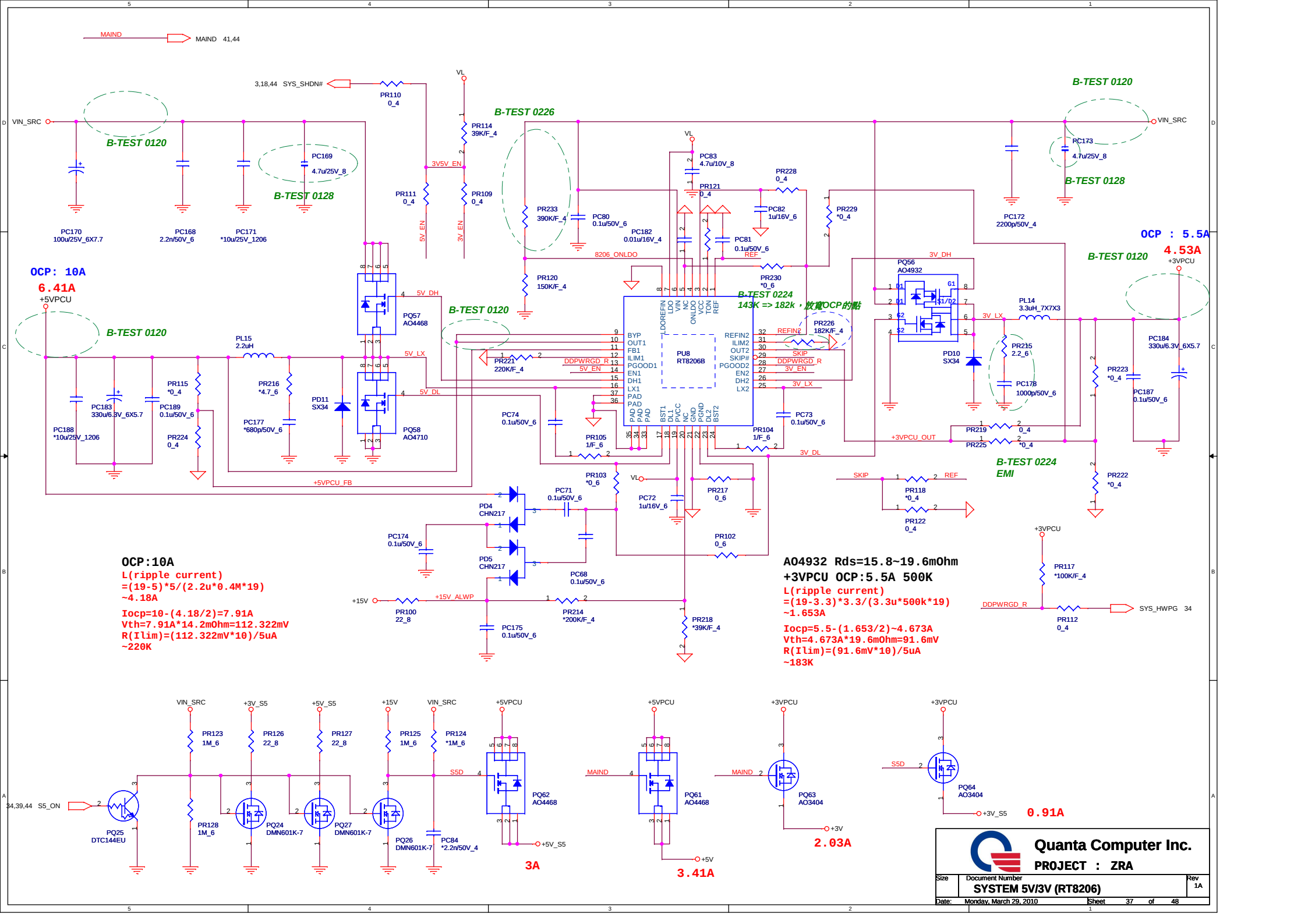

Quanta Computer Inc.		
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Size	Document Number: SYSTEM 5V/3V (RT8206)	Rev: 1A
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OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

3A

15A

15A

PU13
ISL6265A

Pin 49 is GND Pin

Close to CPU socket

Close to CPU socket

Parallel

B-TEST 0120

B-TEST 0128

B-TEST 0224 EMI

B-TEST 0225

Quanta Computer Inc. PROJECT : ZRA			
Size	Document Number: CPU Core (ISL6265)		Rev: 1A
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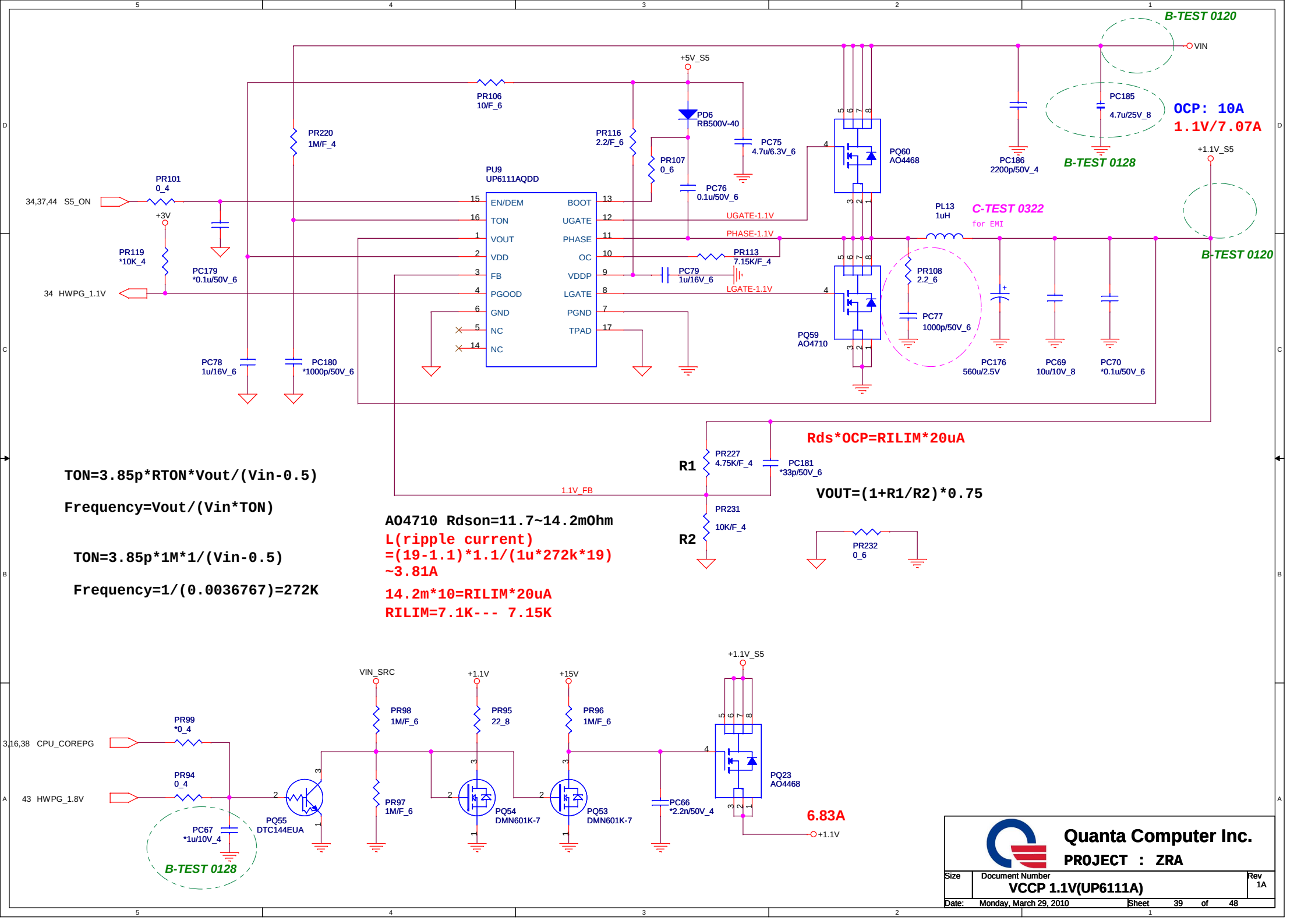
B-TEST 0120
VIN
+5V_S5
PR106
10/F_6
PD6
RB500V-40
PR220
1M/F_4
PR116
2.2/F_6
PC75
4.7u/6.3V_6
PQ60
AO4468
PC185
4.7u/25V_8
OCP: 10A
1.1V/7.07A
PC186
2200p/50V_4
B-TEST 0128
+1.1V_S5
PR107
0_6
PC76
0.1u/50V_6
PU9
UP6111AQDD
PR101
0_4
34,37,44 S5_ON
+3V
PR119
*10K_4
PC179
*0.1u/50V_6
34 HWPG_1.1V
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-1.1V
PHASE-1.1V
LGATE-1.1V
PR113
7.15K/F_4
PC79
1u/16V_6
PL13
1uH
C-TEST 0322
for EMI
B-TEST 0120
PR108
2.2_6
PC77
1000p/50V_6
PQ59
AO4710
PC78
1u/16V_6
PC180
*1000p/50V_6
PC176
560u/2.5V
PC69
10u/10V_8
PC70
*0.1u/50V_6
Rds*OCP=RILIM*20uA
R1
PR227
4.75K/F_4
PC181
*33p/50V_6
1.1V_FB
VOUT=(1+R1/R2)*0.75
PR231
10K/F_4
R2
PR232
0_6
TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K
AO4710 Rdson=11.7~14.2mOhm
L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A
14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K
VIN_SRC
+1.1V
+15V
+1.1V_S5
PR99
*0_4
3,16,38 CPU_COREPG
PR94
0_4
43 HWPG_1.8V
PR98
1M/F_6
PR95
22_8
PR96
1M/F_6
PQ55
DTC144EUA
PR97
1M/F_6
PQ54
DMN601K-7
PQ53
DMN601K-7
PC66
*2.2n/50V_4
PQ23
AO4468
PC67
*1u/10V_4
B-TEST 0128
6.83A
+1.1V
Quanta Computer Inc.
PROJECT : ZRA
Size
Document Number
VCCP 1.1V(UP6111A)
Rev
1A
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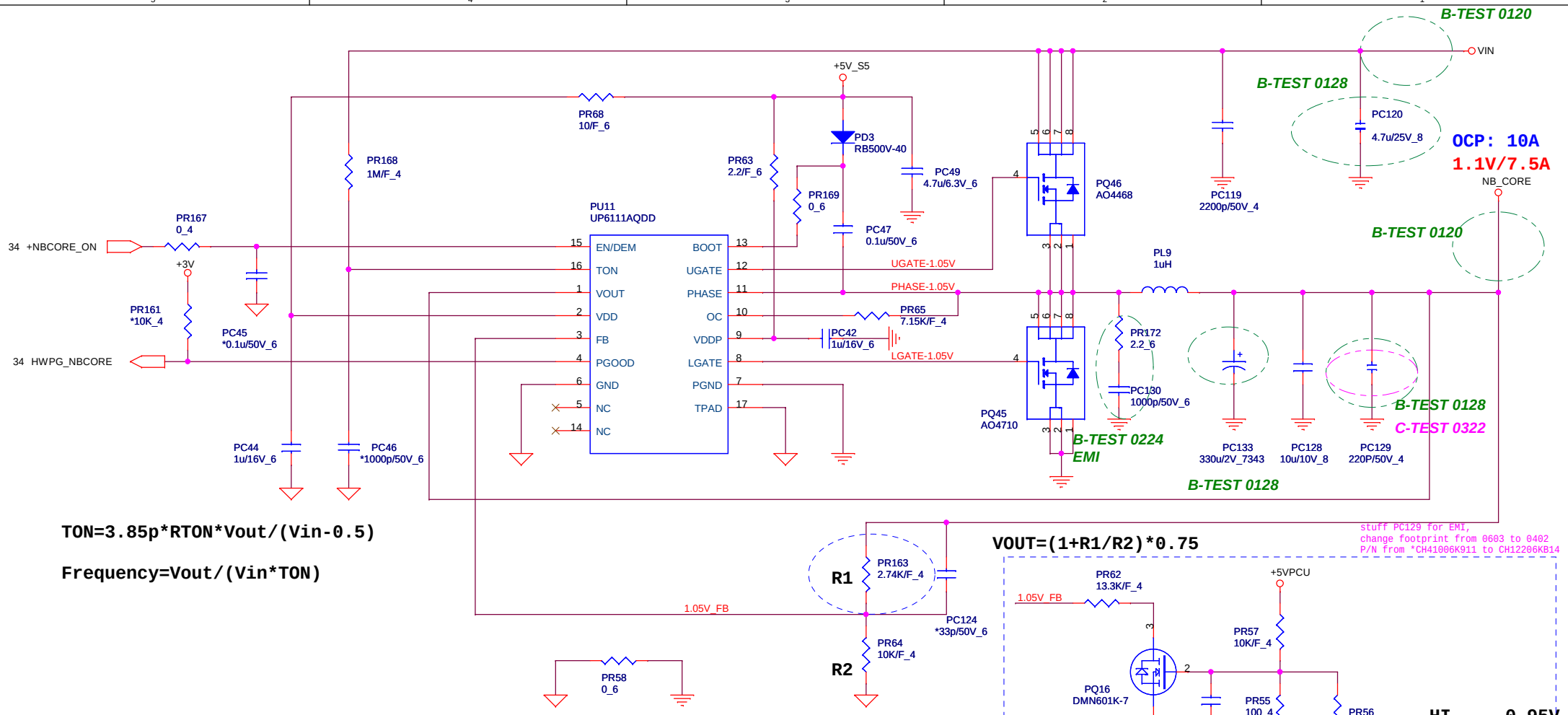

Quanta Computer Inc.		
PROJECT : ZRA		
Size	Document Number: NB_CORE(UP6111A)	Rev: 1A
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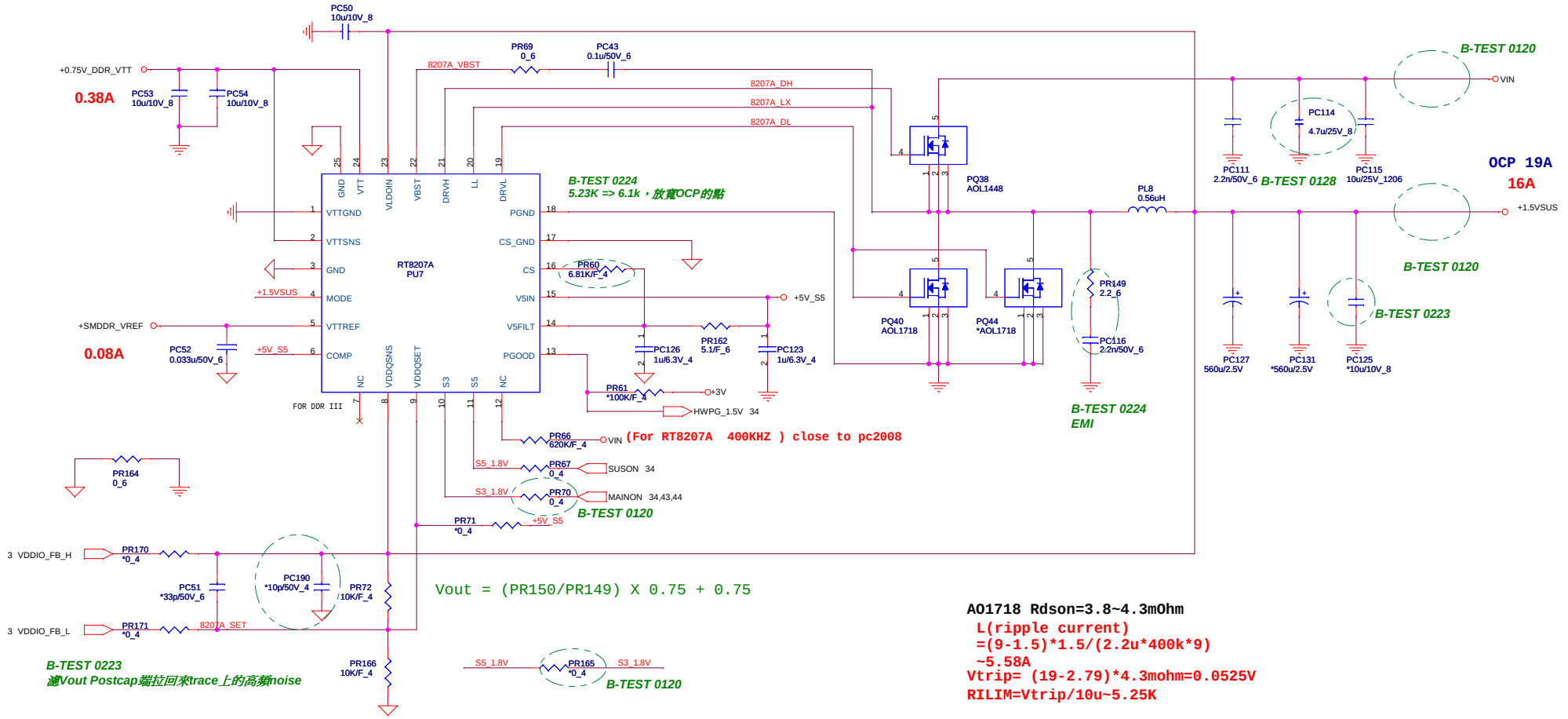
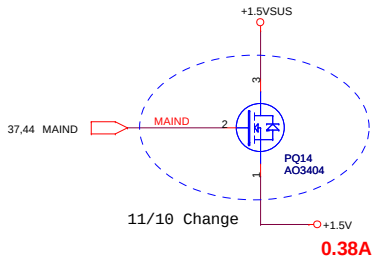
[PWM]





	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZRA

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

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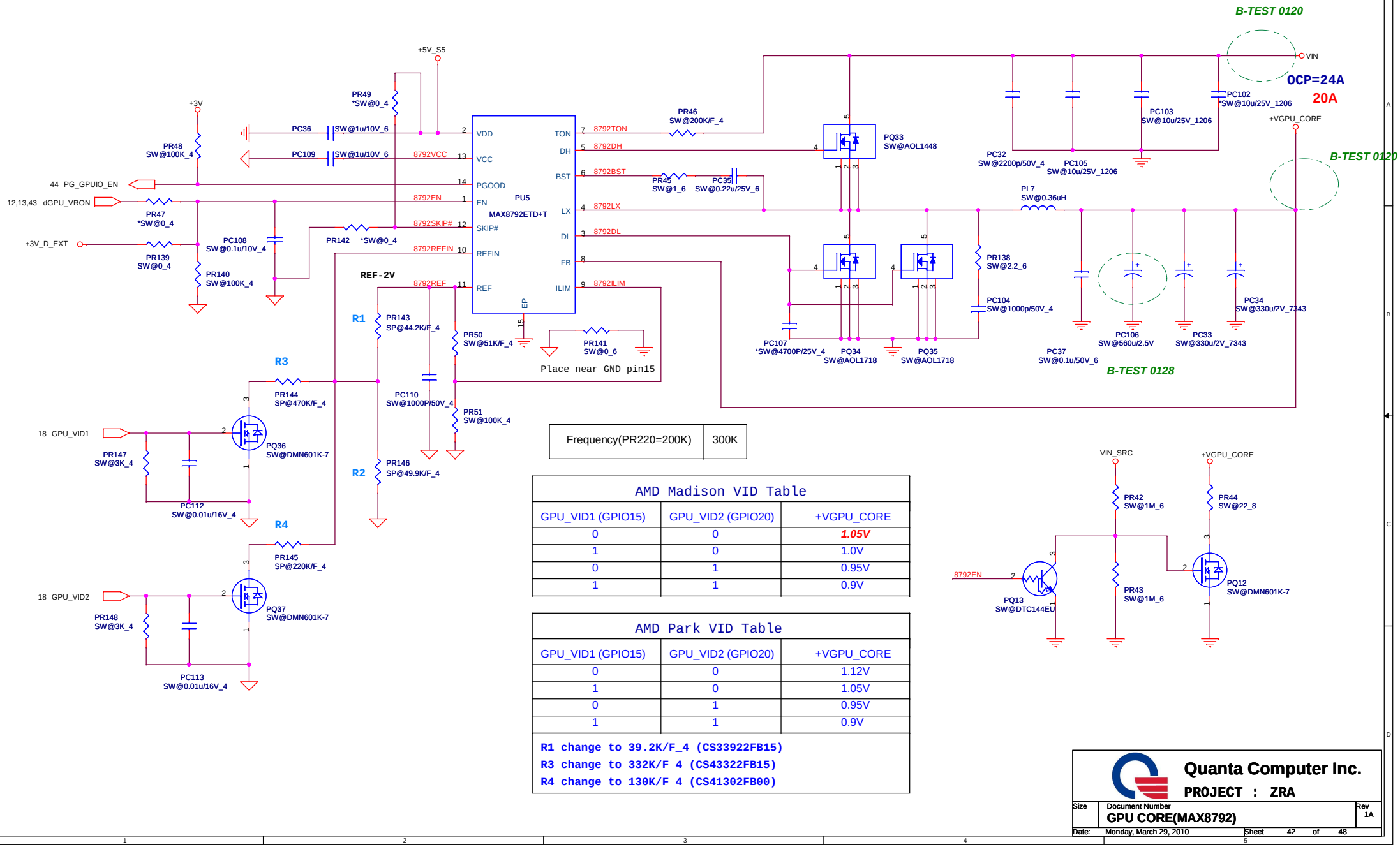

Frequency(PR220=200K)	300K

AMD Madison VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	***1.05V***
1	0	1.0V
0	1	0.95V
1	1	0.9V

AMD Park VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

R1 change to 39.2K/F_4 (CS33922FB15)
R3 change to 332K/F_4 (CS43322FB15)
R4 change to 130K/F_4 (CS41302FB00)

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Size	Document Number	Rev
	GPU CORE(MAX8792)	1A
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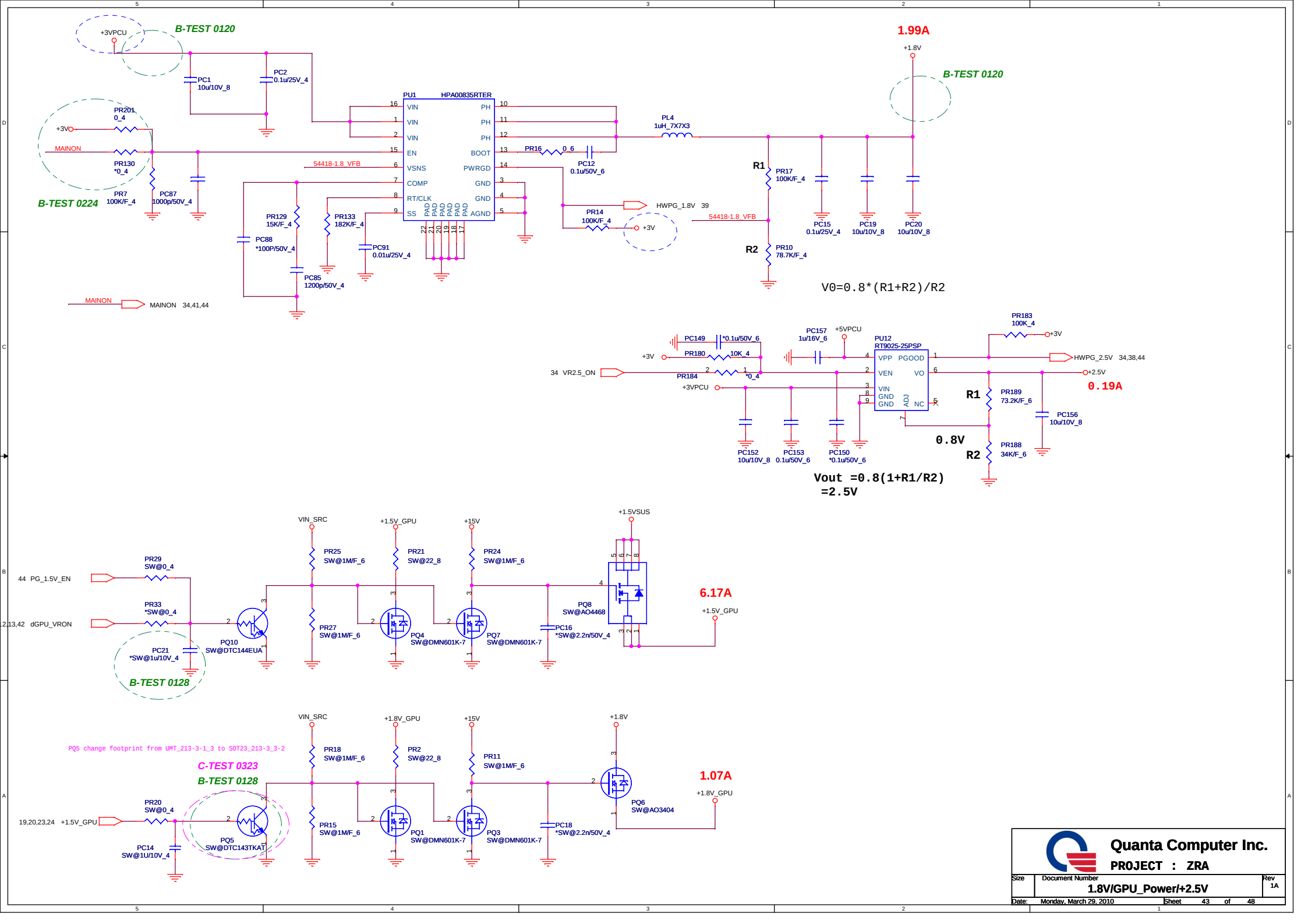

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	1.8V/GPU_Power/+2.5V	1A
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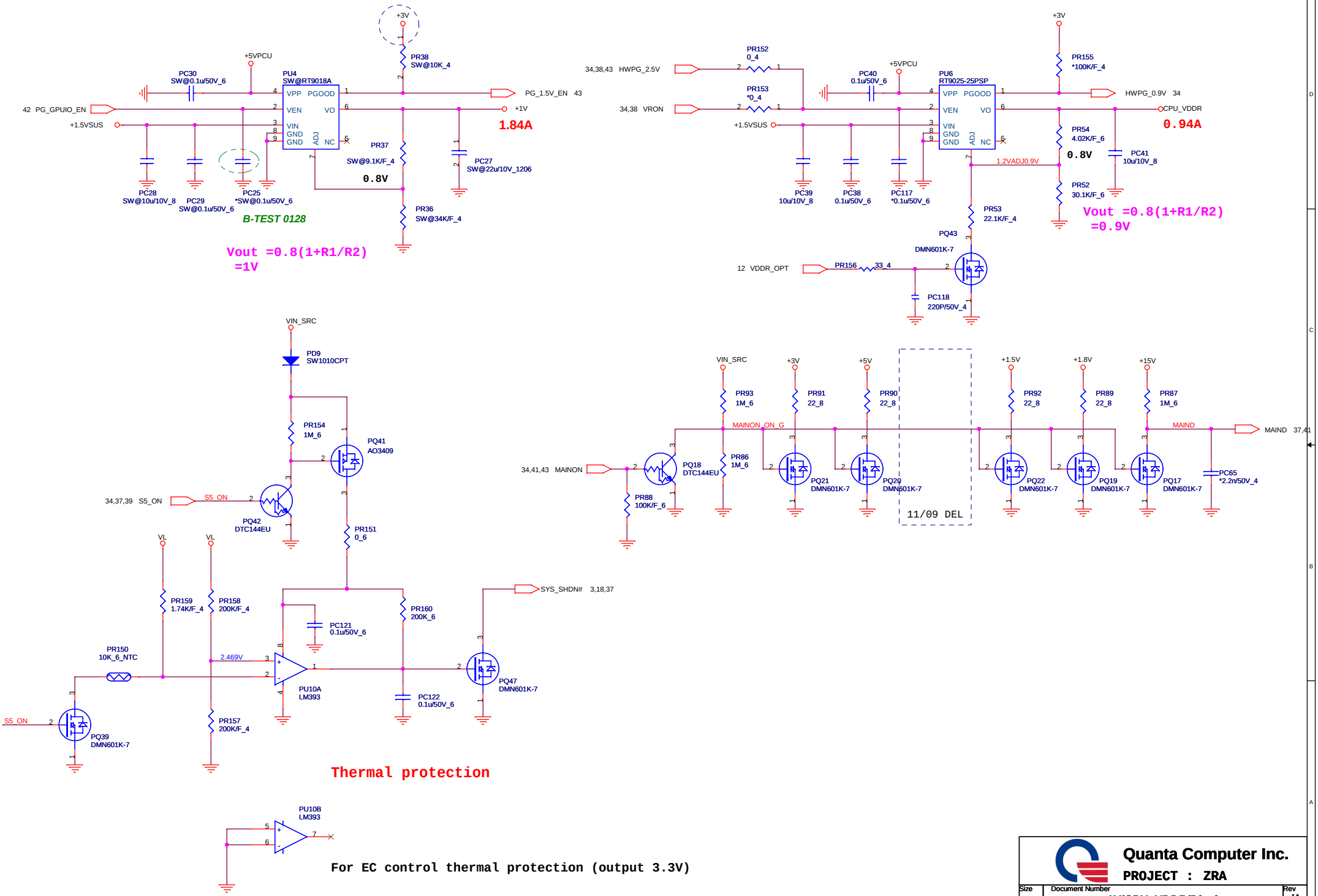
+3V
+5VPCU
PC30
SW@0.1u/50V_6
PU4
SW@RT9018A
VPP PGOOD
VEN VO
VIN
GND
GND ADJ NC
PR38
SW@10K_4
PG_1.5V_EN 43
42 PG_GPUIO_EN
+1V
1.84A
+1.5VSUS
PR37
SW@9.1K/F_4
0.8V
PC27
SW@22u/10V_1206
PC28
SW@10u/10V_8
PC29
SW@0.1u/50V_6
PC25
*SW@0.1u/50V_6
PR36
SW@34K/F_4
B-TEST 0128
Vout =0.8(1+R1/R2)
=1V
34,38,43 HWPG_2.5V
PR152
0_4
34,38 VRON
PR153
*0_4
PC40
0.1u/50V_6
PU6
RT9025-25PSP
PR155
*100K/F_4
HWPG_0.9V 34
CPU_VDDR
0.94A
PR54
4.02K/F_6
0.8V
PC41
10u/10V_8
1.2VADJ0.9V
PR52
30.1K/F_6
PC39
10u/10V_8
PC38
0.1u/50V_6
PC117
*0.1u/50V_6
PR53
22.1K/F_4
Vout =0.8(1+R1/R2)
=0.9V
PQ43
DMN601K-7
12 VDDR_OPT
PR156
33_4
PC118
220P/50V_4
VIN_SRC
PD9
SW1010CPT
PR154
1M_6
PQ41
AO3409
34,37,39 S5_ON
S5_ON
PQ42
DTC144EU
PR151
0_6
VL
VL
PR159
1.74K/F_4
PR158
200K/F_4
PR150
10K_6_NTC
2.469V
PC121
0.1u/50V_6
PR160
200K_6
SYS_SHDN# 3,18,37
PU10A
LM393
PC122
0.1u/50V_6
PQ47
DMN601K-7
S5_ON
PQ39
DMN601K-7
Thermal protection
PU10B
LM393
For EC control thermal protection (output 3.3V)
VIN_SRC
+3V
+5V
+1.5V
+1.8V
+15V
PR93
1M_6
PR91
22_8
PR90
22_8
PR92
22_8
PR89
22_8
PR87
1M_6
MAINON_ON_G
MAIND
MAIND 37,41
34,41,43 MAINON
PQ18
DTC144EU
PR86
1M_6
PR88
100K/F_6
PQ21
DMN601K-7
PQ20
DMN601K-7
PQ22
DMN601K-7
PQ19
DMN601K-7
PQ17
DMN601K-7
PC65
*2.2n/50V_4
11/09 DEL
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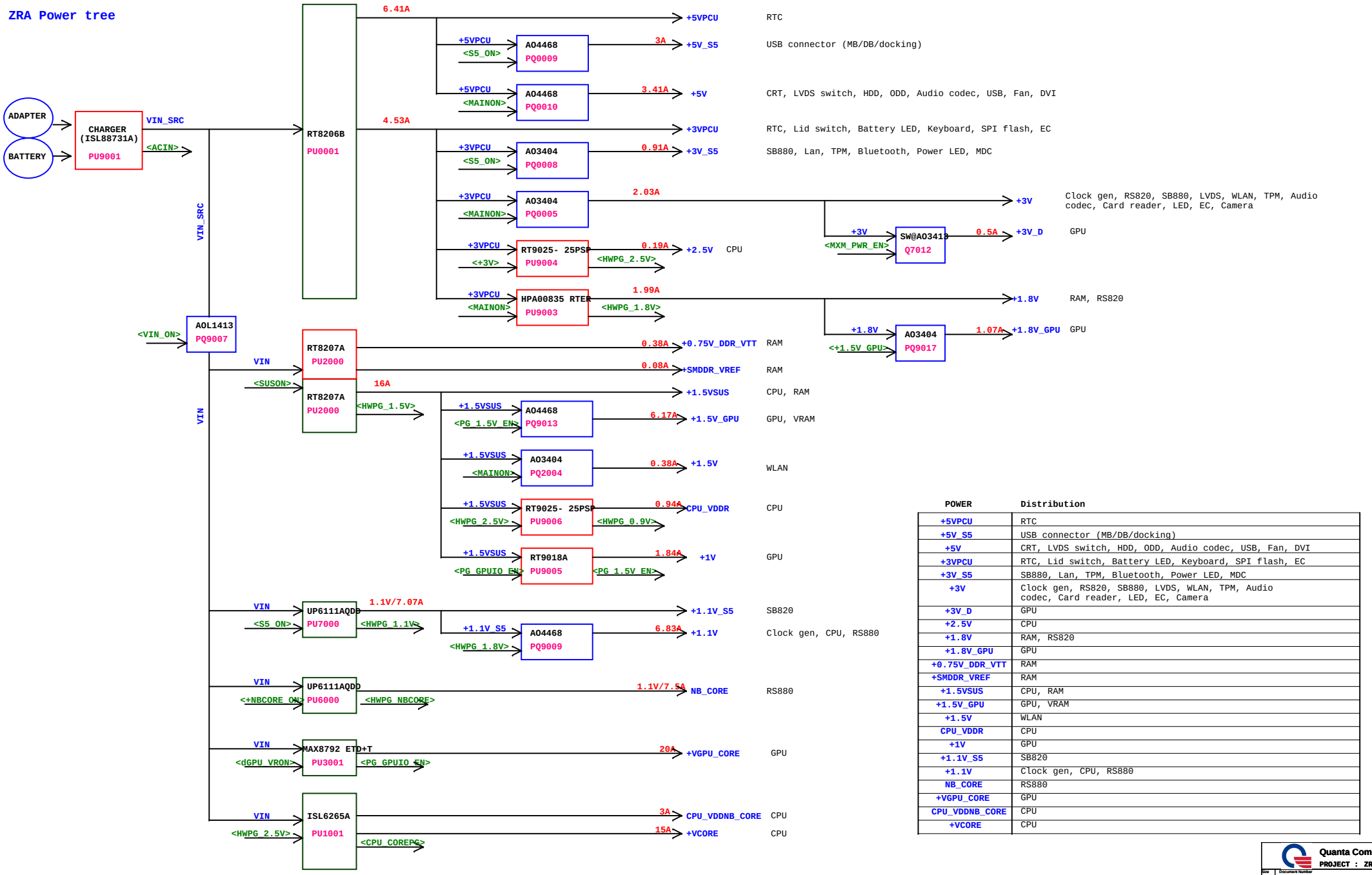
ZRA Power tree



POWER	Distribution
+5VPCU	RTC
+5V_S5	USB connector (MB/DB/docking)
+5V	CRT, LVDS switch, HDD, ODD, Audio codec, USB, Fan, DVI
+3VPCU	RTC, Lid switch, Battery LED, Keyboard, SPI flash, EC
+3V_S5	SB880, Lan, TPM, Bluetooth, Power LED, MDC
+3V	Clock gen, RS820, SB880, LVDS, WLAN, TPM, Audio codec, Card reader, LED, EC, Camera
+3V_D	GPU
+2.5V	CPU
+1.8V	RAM, RS820
+1.8V_GPU	GPU
+0.75V_DDR_VTT	RAM
+SMDDR_VREF	RAM
+1.5VSUS	CPU, RAM
+1.5V_GPU	GPU, VRAM
+1.5V	WLAN
CPU_VDDR	CPU
+1V	GPU
+1.1V_S5	SB820
+1.1V	Clock gen, CPU, RS880
NB_CORE	RS880
+VGPU_CORE	GPU
CPU_VDDNB_CORE	CPU
+VCORE	CPU

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ZRA	A1A	11/24	1.Change Hole31___P29(unguard hole) 2.Change CN9009___P32(ME modify T/B connector from 6pin to12 pin) 3.Del R7528、R7529___P28(for all acer project in 2010=>short the WLAN_LED and WWAN_LED)	ECN Release
		11/25	1.Add power tree___P46 2.Change CN7019 footprint___P29(NEW=>sata-c166h2-12204-l-22p-r) 3.Change PC9064、PR9021、PR9025 P/N___P37(PC9064=>CH5104K1900、PR9021=>CS41502JB10、PR9025=>CS33902JB01) 4.Stuff R7118、R7115___P11 (for NB REV:11 use) 5.Exchange R7105、C7228___P20(refence AMD design) 6.Del U7033A PINAA4 funcyion___P13(refence AMD design) 7.Rename U7033A PINAJ6 net name___P13(refence AMD design, change from PG_GPUIO_ENA to dGPU_PWROK)	
		11/26	1.Change R7029___P20(AMD suggest change from 1k to 10k) 2.no stuff R7060___P19 3.Change R7061、R7070、R7032___P18(AMD suggest change from 1k to 10k) 4.Change R7108、R9038___P18(AMD suggest change from 1k to 0R) 5.no stuff R7029___P20 6.Change GPU_VID1 net___P19(change from U7022B PIN AK14 to AM13) 7.Change GPU_VID2 net___P19(change from U7022B PIN AM13 to AL13) 8.Modify Board ID schematic___P13、P15(follow ZR8_B) 9.Add LED4、R9252、RV5___P33(SATA LED movie from DB to MB)	
		11/27	1.Change R9629 footprint___P28(from 0603 to 0402) 2.Change CN7022 H___P28(from H=5.6 to H=7) 3.Change PJ2 battery footprint___P37(new => bat-bhp-08afeb-8p-l-v) 4.Change PR3013、PR3017、PR3010 value___P43	
		12/01	1.Change L7031、L7060、L7026、L7035、L7032、L7061、L7021、L7033 value___P28(change to PBY160808T-221Y-N) 2.Modify Power tree	
		12/03	1.Change L9000 footprint___P27(from 0806 to 0805) 2.Change CN9007 P/N___P30(from DFHD12MS788 to DFHD12MS621)	
		12/08	1.Change C7343 value_P6(from 1000P to 2200P) 2.Change C9098、C9119、C9120、C9121、C9122、C9123 value_P34(from 0.1u/10V to 0.1u/25V) 3.Change R7437 value_P11(from 140 ohm to 133ohm ==> AMD suggest use docking need matching 133 ohm)	
		12/09	1.Change C7063 value_P21(from SPE@ to SW@) 2.Change C7404 value_P23(from SPE@ to SP@) 2.Add R9253 _P33	
		12/11	1.rename 2.Change PC24 P/N _P37(from CH5104K1900 to CH5104K9906) 3.Change PC55、PC56、PC57、PC58、PC139、PC140 P/N _P6/P39(from CH733RM8802 to CH733RY8802) 4.Change PL11 P/N _P39(from DC+18V0MZ04 to CV+18V0MZ04) 5.Change LED2 footprint _P33(change to ledltst-s326kgjskt-3p-nb4)	
		12/15	1.Change CN6 P/N _P32(from DFFC04FR014 to DFFC04FR018) 2.DEL R384、LED6、RV7 _P33(DEL BLUETOOTH LED function) 3.Add T100 _P33	
		12/16	1.Add Hole NUT P/N _P32 2.DEL CN20 PIN73/PIN74 _P36(change from GND to NA)	
	B1A	12/28	1.Modify power sequence_P2 2.Modify power tree_P46	
		01/20	1.Del JP15、JP16、JP20、JP21__P37 2.Del JP14、JP13、JP12、RP201、RP213、RP209、RP210__P38 3.no stuff PC141___P38 4.Change PL12 P/N to CV-2280MZ05、footprint to CHOKE-PCMC063T-3R3MN-smt___P38 5.Change PC154 and PC138 P/N to CC71004MZ01 and Value from 27uF to 100uF___P38 6.Del JP19、JP17、JP18__P39 7.Del JP7、JP8、JP10__P40 8.Del JP6、JP9、JP11__P41 9.no stuff PR165___P41 10.stuff PR70___P41 11.Del JP3、JP4、JP5__P42 12.Del JP2、JP1__P43	

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ZRA	B1A	01/28	1.Change Q9 P/N to BAM700200F6___P20 2.Change PC17 footprint to 0603 ___P36 3.Change PC11 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P36 4.Change PC169、PC173 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P37 5.Change PC158、PC62、PC142、PC143、PC135、PC136 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P38 6.Change PC185 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P39 7.no stuff PC67___P39 8.Change PC120 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P40 9.no stuff PC129___P40 10.Change PC114 Value from 10uF to 4.7uF，footprint form 1206 to 0805，P/N from CH61004M291 to CH5474KEA06 ___P41 11.no stuff PC21___P43 12.no stuff PC25___P44 13.Change PQ5 P/N from BA144EUAZ04 to BA001430Z31___P43 14.Change PC133 Value from 560uF to 330uF，footprint form ECAP6_3X6_1-7_2 to CC7343，P/N from CC7560JMZ15 to CH733RY8802 ___P40 15.Change PC106 Value from 560uF to 330uF，footprint form ECAP6_3X6_1-7_2 to CC7343，P/N from CC7560JMZ15 to CH733RY8802 ___P42 16.no stuff R148、R144___P10 17.Del Clock Generator ___P3 18.Del R166、R163、R162、R165、RP21 ___P10 19.Del RP26、RP14、RP13、RP27、RP33、RP30、RP29 ___P12 20.Del R274、R297 ___P13 21.Change R289 from 100K to 10K ___P13 22.Change C687、C686 from 18P to 27P ___P18 23.no stuff R428、R429___P22 24.Modify DDR3 Memory Aperture size table___P22 25.Add F1___P25 26.Change L32、L38、L40 from BLM18BA470SN1 to BLM18BA220SN1D ___P25 27.Change R80 from 1.24K to 1.21K ___P26 28.Change U14 footprint to soic8-8-1_27-at45db011d___P26 29.Change R60 from 100K to 10K ___P26 30.Del R2 ___P26 31.Del R593 ___P27 32.Modify CN16 schematic ___P30 33.Change D10 P/N to BCRB500VZ29___P34 34.Change CN20 footprint to DOCK-SP07-10207-19-64P-H-SMT___P35	ECN Release
		01/29	1.Change C797、C798 from 22P to 27P ___P12 2.Change CN13 footprint to rj45-130452-g-12p-v，P/N to DFTJ12FR154___P26 3.Change C843、C846 from 12P to 18P ___P27 4.Change U35 PIN21 netname to LPC_CLK0___P27	
		02/01	1.Add R162___P12 2.Del R90 ___P17 3.no stuff R76、R83、R91、R45___P17 4.Add C494、U34___P25 5.Add CN27___P29 6.Del L43、L45、L81、L82、L66、L67___P29 7.stuff R225、Q17 (Del IV)___P35 8.Add CN28、L91、L92、L93、L83、L84、L88、C785、C786___P35 9.Modify CN20 netname___P35 10.stuff R43___P17	
		02/02	1.Add R384___P15 2.Add R554___P29	
		02/05	1.Add Q43、Q42、Q44___P5 2.Add F2、F3___P35	
		02/08	1.Modify R256 schematic to U17 PIN2___P30	
		02/10	1.change L77 P/N to CX163210007，foot print to CHOKE-WCM3216-4P___P35 2.Add C495、C498___P31 3.no stuff C441、C446、C476、C475、C478、C477___P35 4.change CN28 PIN13、PIN14 from GND to NC___P35 5.change CN27 PIN13、PIN14 from GND to NC___P29 6.Change L32、L38、L40 P/N from BLM18BA220SN1D to BLM18BA470SN1___P25 7.Change C377、C363、C351、C349、C365、C376 value from 10p to 6.8p，P/N to CH-6806TB01___P25 8.add C796、C502、C506、C522、C792、C794___P35 9.change L78、L79、L80 P/N to CX8BA470003___P35	

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ZRA	B1A	02/10	10.Add C812、C816、C817、C824、C825、C830___P29 11.Add C834___P29 12.Add C831、C837、C836、C838、C862、C863、C864、C865、C869、C870、C871___P33 13.Add C866、C867___P31 14.Change R292,R364,R367,R286,R293,R287,C610,C537 footprint to short pad__P29 15.Add C868___P33	ECN Release
		02/11	1.Add C872___P31 2.Add R90___P32	
		02/21	1.Change netname LPC_CLK1 to LPC_CLK0___P34 2.no stuff R540、R536、C782、C474、U31___P3 3.no stuff RP20___P27	
		02/23	1.Change R308、R311 from 5.1R to 39R___P29 2.Change R71 from 0 ohm to 4.7k ohm and not stuff R71___P20 3.Change L78、L79、L80 from BEAD 47R TO 0R___P35 4.Change L91、L88、L92、L93、L84、L83 from BEAD 120R TO 0R___P35 5.No stuff R262、R257、Y3、C496、C497，and stuff R261、R256___P30 6.stuff R292、R364、R367、R286、R293、R287、C610、C537 to 0R___P29 7.ADD PC190 10pF___P41 8.No stuff PC125___P41 9.change PR226 from 143K => 182k，放寬OCP的點___P37 10.change PR60 from 5.23K => 6.1k，放寬OCP的點___P41 11.change R339、R340 to L66、L67，and change value from 0R to BEAD___P29	
		02/25	1.No stuff PR178___P41 2.change R130 from 2.2K => 300R， Accord with LDT riss time SPEC___P10 3.change U15 P/N from AL003257K28 to ALBT3257K18___P25	
		02/26	1.NO stuff R331（不分BAP/BXP）___P12	
		03/22	1.change R175 0ohm to bead(CX8PG221003) and C339 from 0.1uF to 2.2uF(CH52201K991), for monitor noise issue.___P10	

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