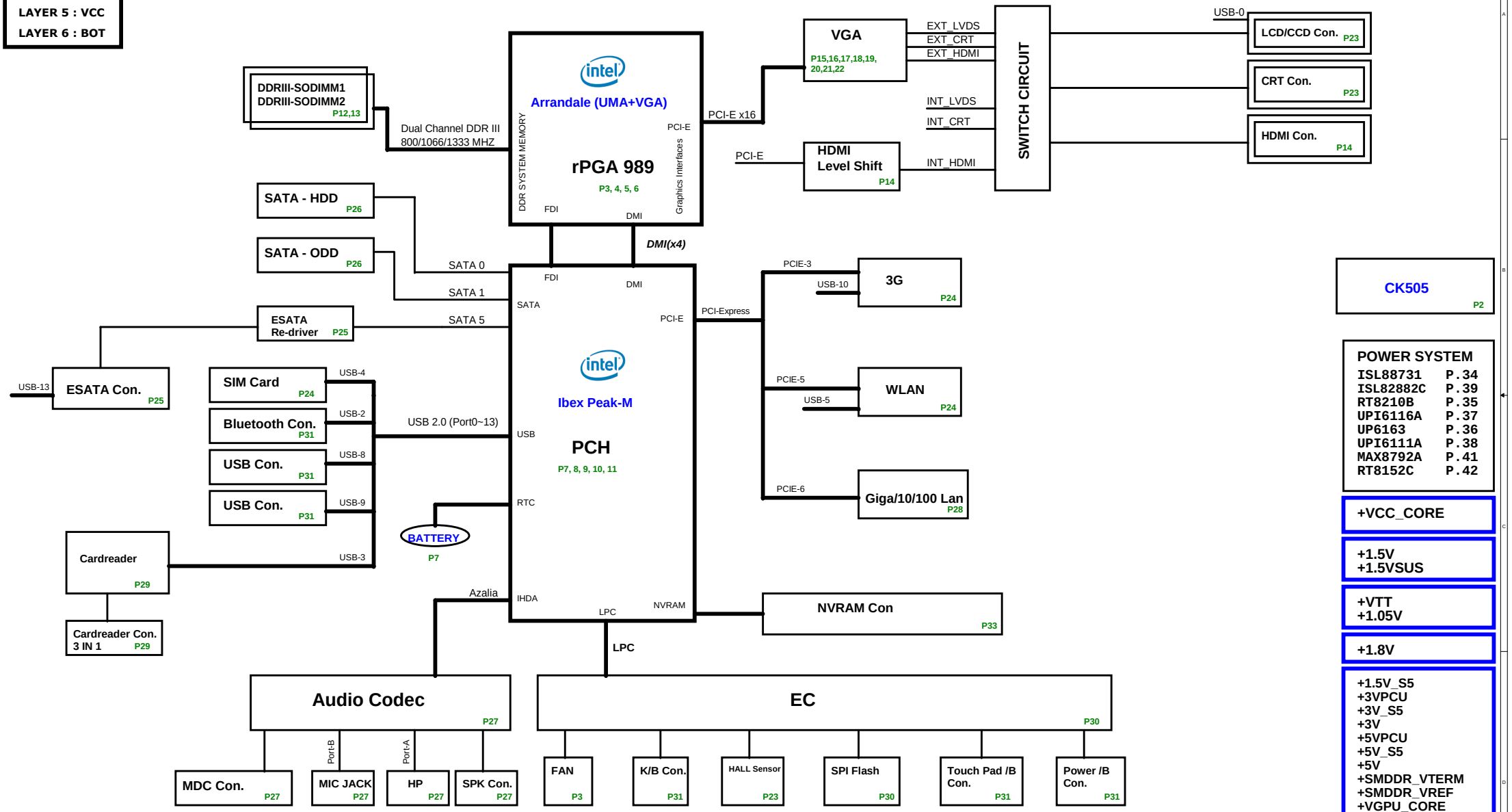
# BL6 Block Diagram

**PCB STACK UP**

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT




**POWER SYSTEM**

| | |
|---|---|
| ISL88731 | P.34 |
| ISL82882C | P.39 |
| RT8210B | P.35 |
| UPI6116A | P.37 |
| UP6163 | P.36 |
| UPI6111A | P.38 |
| MAX8792A | P.41 |
| RT8152C | P.42 |

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

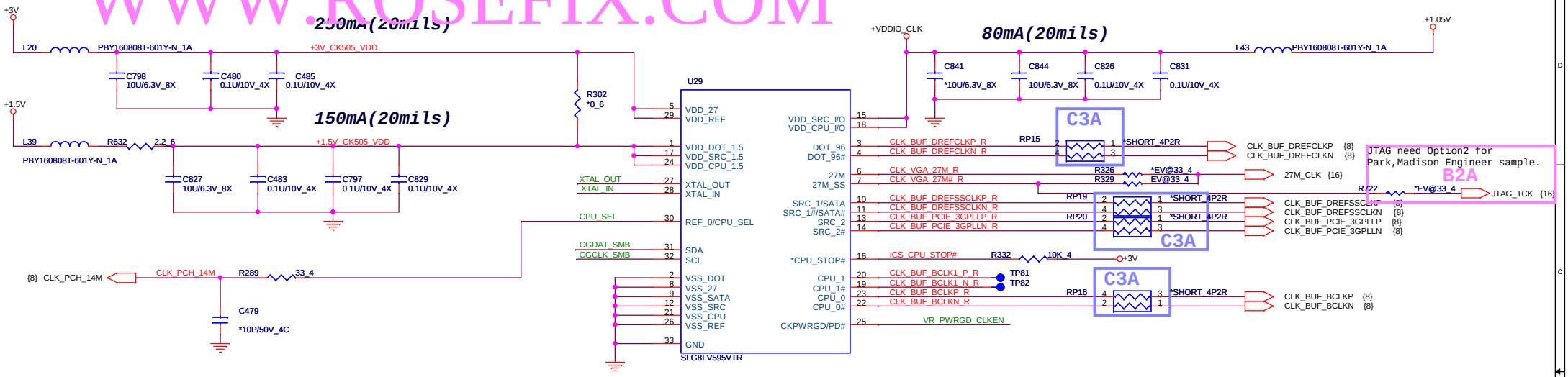
+1.5V_S5
+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF
+VGPU_CORE
+VAXG

Quanta Computer Inc.
PROJECT : BL6

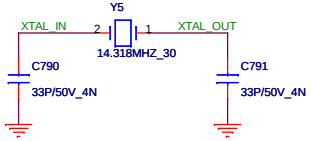
| Size | Document Number | Rev |
|---|---|---|
| | Block Diagram | A1A |

Date: Wednesday, April 07, 2010 Sheet 1 of 45

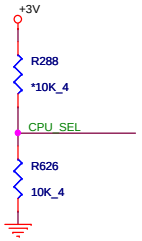
# CLOCK Gen




## CLK CRYSTAL

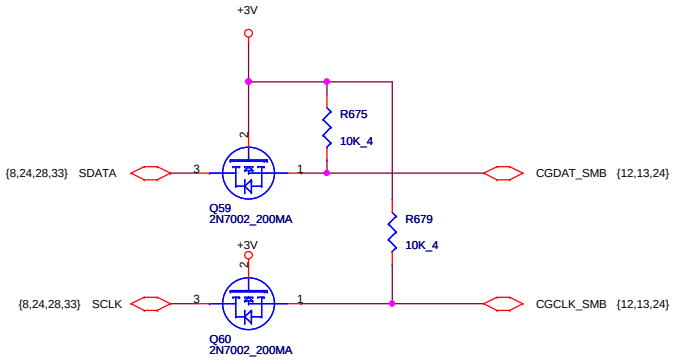



## CLK CPU_SEL



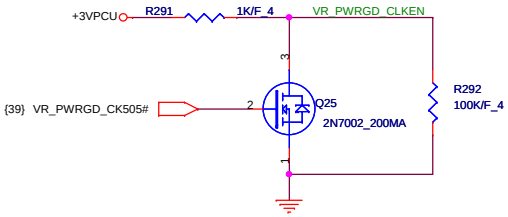

| | 0 | 1 |
|---|---|---|
| CPU_SEL | CPU =133MHz (default) | CPU=100MHz |

## CLK I2C




## CLK POWERGOOD

Change to +3VPCU
(follow CRB)

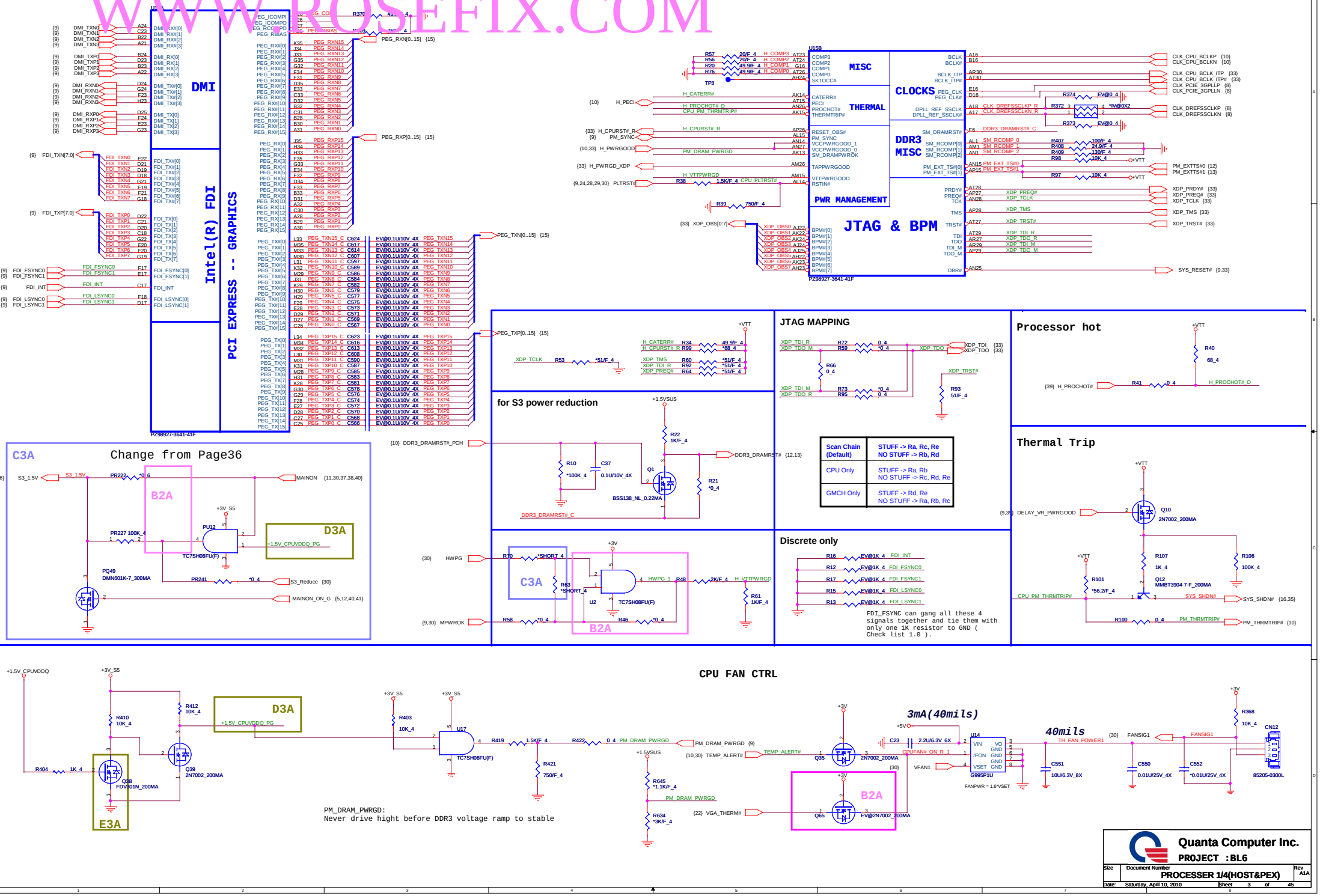



Quanta Computer Inc.

PROJECT : BL6

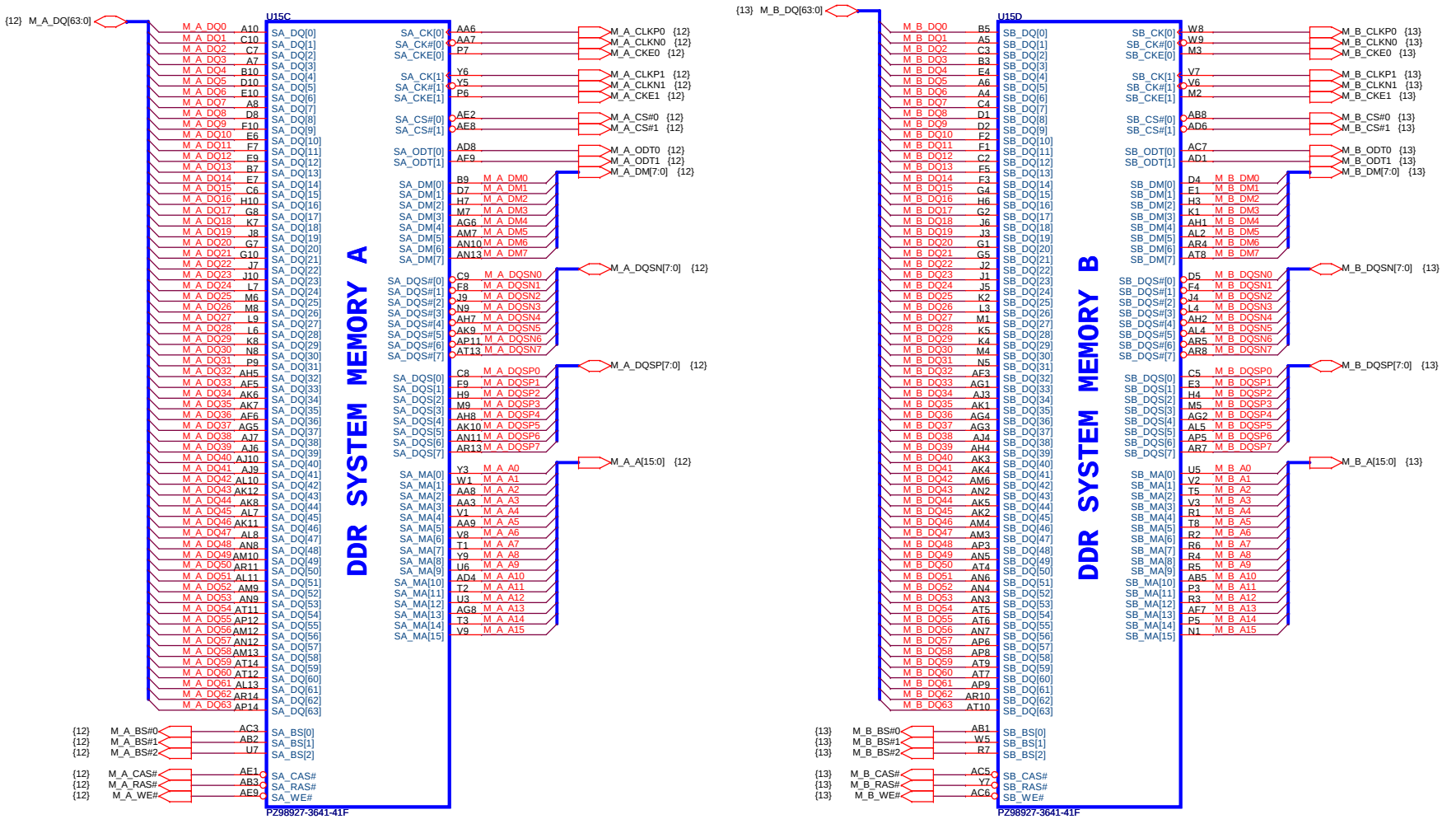
| Size | Document Number | Rev |
|---|---|---|
| | CLOCK GENERATOR | A1A |

Date: Thursday, April 08, 2010 Sheet 2 of 45




Quanta Computer Inc.
PROJECT : BL6
Size | Document Number: PROCESSER 1/4(HOST&PEX) | Rev: A1A
Date: Saturday, April 10, 2010 | Sheet 3 of 45

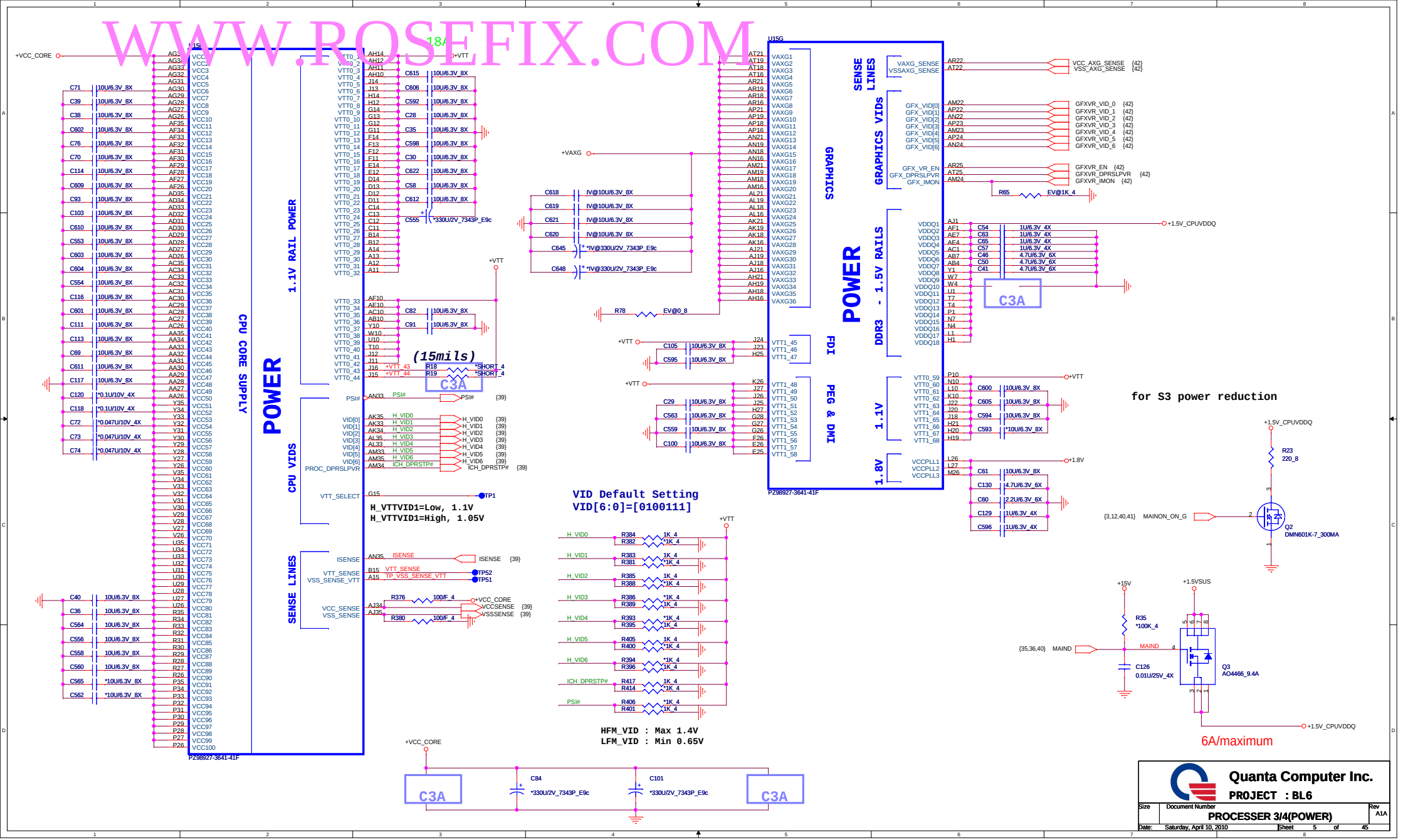
# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)




Quanta Computer Inc.

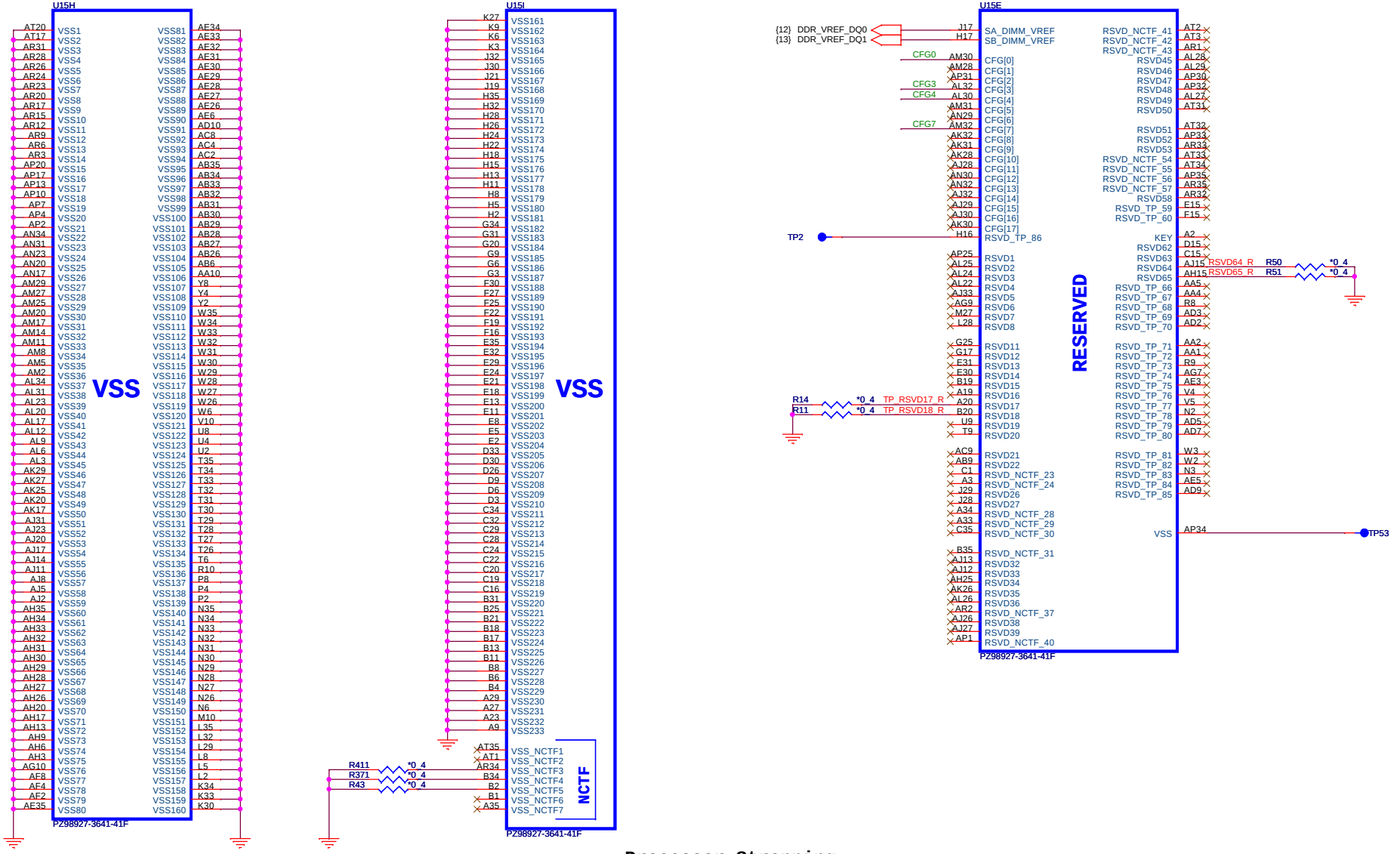
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | PROCESSER 2/4(DDR) | A1A |
| Date: Saturday, April 10, 2010 | Sheet 4 of 45 | |



# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

# AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)




## Processor Strapping

| | 1 | 0 |
|---|---|---|
| CFG4 (Display Port Presence) | Disabled; No Physical Display Port attached to Embedded Diplay Port | Enabled; An external Display port device is connected to the Embedded Display port |
| CFG0 (PCI-Epress Configuration Select) | Single PEG | Bifurcation enabled |
| **CFG3 (PCI-Epress Static Lane Reversal)** | Normal Operation | **Lane Numbers Reversed 15 -> 0 , 14 -> 1** |

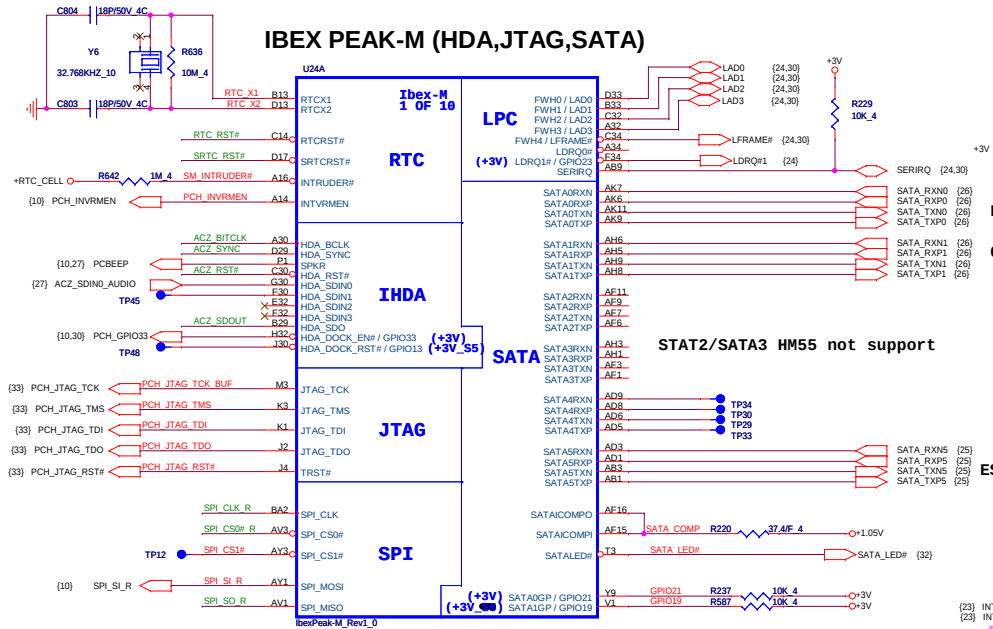

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

Quanta Computer Inc.
PROJECT : BL6

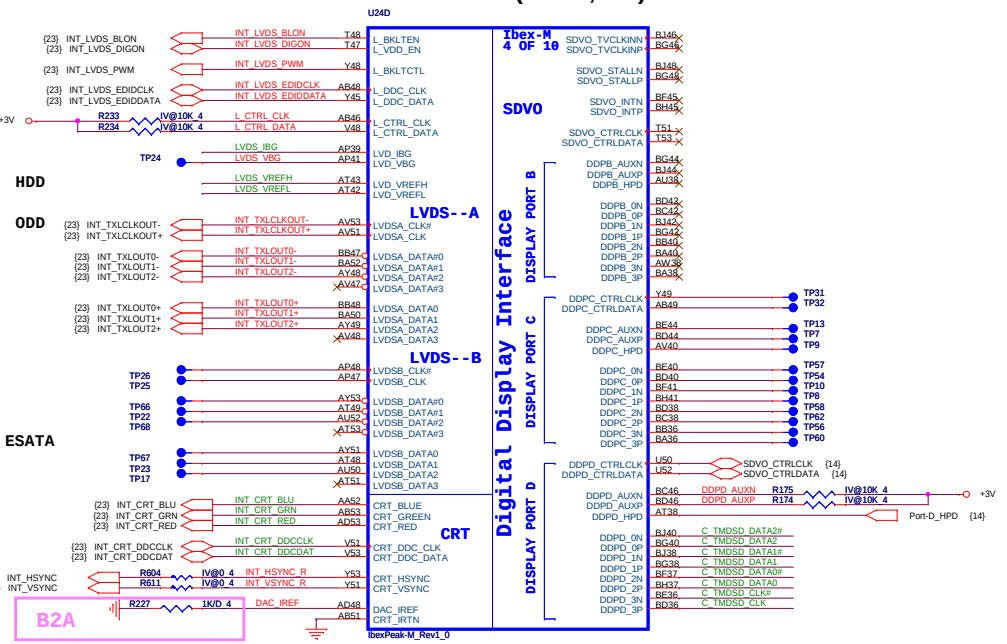
| Size | Document Number | Rev |
|---|---|---|
| | PROCESSER 4/4 (GND) | 1A |

Date: Saturday, April 10, 2010 Sheet 6 of 45

## IBEX PEAK-M (HDA,JTAG,SATA)

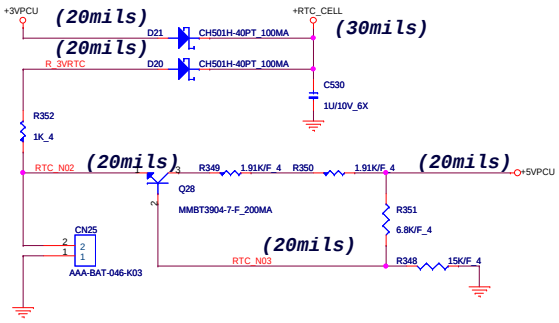


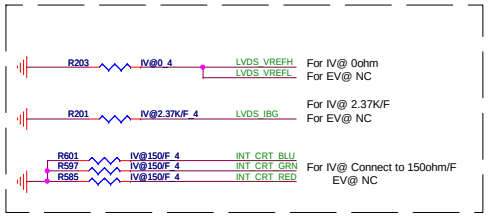

## IBEX PEAK-M (LVDS,DDI)

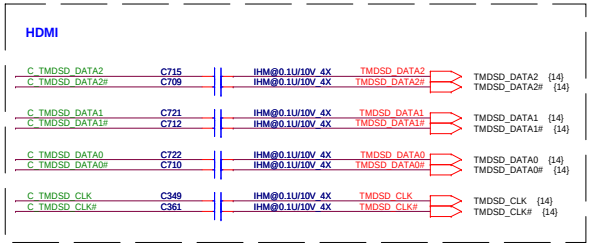



| Port | Strap | How to enable Port? | How to disable Port? |
|---|---|---|---|
| LVDS | L_DDC_DATA | PU to 3.3V with 2.2k+/- 5% | NC |
| Port B | SDVO_CTRLDATA | PU to 3.3V with 2.2k+/- 5% | NC |
| Port C | DDPC_CTRLDATA | PU to 3.3V with 2.2k+/- 5% | NC |
| Port D | DDPD_CTRLDATA | PU to 3.3V with 2.2k+/- 5% | NC |
| eDP | CFG[4] | PD to GND directly | NC |

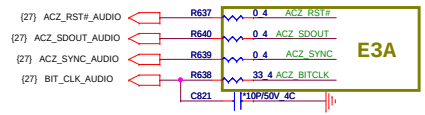
## RTC BATTERY

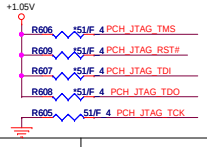


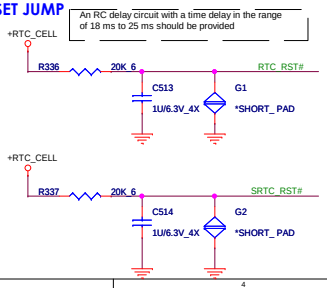

## For AUDIO



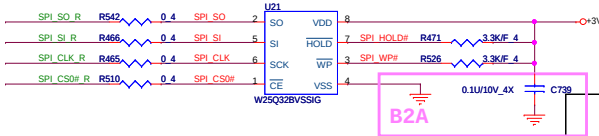




## RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided




## 4M byte SPI ROM




| PCH | 2MB | 4MB | 8MB |
|---|---|---|---|
| PM55 | ● | | |
| HM55 | | ● | |
| HM57/PM57 | | ● | ● |
| QM57/QS57 | | | ● |

Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | PCH 1/5 (SATA,HDA,LPC) | A1A |
| Date: Saturday, April 10, 2010 | Sheet 7 of 45 | |

# IBEX PEAK-M (GND)

U24I

| | | | |
|---|---|---|---|
| AY7 | VSS[159] | VSS[259] | H49 |
| B11 | VSS[160] | VSS[260] | H5 |
| B15 | VSS[161] | VSS[261] | J24 |
| B19 | VSS[162] | VSS[262] | K11 |
| B23 | VSS[163] | VSS[263] | K43 |
| B31 | VSS[164] | VSS[264] | K47 |
| B35 | VSS[165] | VSS[265] | K7 |
| B39 | VSS[166] | VSS[266] | L14 |
| B43 | VSS[167] | VSS[267] | L18 |
| B47 | VSS[168] | VSS[268] | L2 |
| B7 | VSS[169] | VSS[269] | L22 |
| BG12 | VSS[170] | VSS[270] | L32 |
| BB12 | VSS[171] | VSS[271] | L36 |
| BB16 | VSS[172] | VSS[272] | L40 |
| BB20 | VSS[173] | VSS[273] | L52 |
| BB24 | VSS[174] | VSS[274] | M12 |
| BB30 | VSS[175] | VSS[275] | M16 |
| BB34 | VSS[176] | VSS[276] | M20 |
| BB38 | VSS[177] | VSS[277] | M34 |
| BB42 | VSS[178] | VSS[278] | M38 |
| BB49 | VSS[179] | VSS[279] | M42 |
| BB5 | VSS[180] | VSS[280] | M46 |
| BC10 | VSS[181] | VSS[281] | M49 |
| BC14 | VSS[182] | VSS[282] | M5 |
| BC18 | VSS[183] | VSS[283] | M8 |
| BC2 | VSS[184] | VSS[284] | N24 |
| BC22 | VSS[185] | VSS[285] | P11 |
| BC32 | VSS[186] | VSS[286] | AD15 |
| BC36 | VSS[187] | VSS[287] | P22 |
| BC40 | VSS[188] | VSS[288] | P30 |
| BC44 | VSS[189] | VSS[289] | P32 |
| BC52 | VSS[190] | VSS[290] | P34 |
| BH9 | VSS[191] | VSS[291] | P42 |
| BD48 | VSS[192] | VSS[292] | P45 |
| BD49 | VSS[193] | VSS[293] | P47 |
| BD5 | VSS[194] | VSS[294] | R2 |
| BE12 | VSS[195] | VSS[295] | R52 |
| BE16 | VSS[196] | VSS[296] | T12 |
| BE20 | VSS[197] | VSS[297] | T41 |
| BE24 | VSS[198] | VSS[298] | T46 |
| BE30 | VSS[199] | VSS[299] | T49 |
| BE34 | VSS[200] | VSS[300] | T5 |
| BE38 | VSS[201] | VSS[301] | T8 |
| BE42 | VSS[202] | VSS[302] | U30 |
| BE46 | VSS[203] | VSS[303] | U31 |
| BE48 | VSS[204] | VSS[304] | U32 |
| BE50 | VSS[205] | VSS[305] | U34 |
| BF6 | VSS[206] | VSS[306] | P38 |
| BF8 | VSS[207] | VSS[307] | V11 |
| BF3 | VSS[208] | VSS[308] | P16 |
| BF49 | VSS[209] | VSS[309] | V19 |
| BF51 | VSS[210] | VSS[310] | V20 |
| BG18 | VSS[211] | VSS[311] | V22 |
| BG24 | VSS[212] | VSS[312] | V30 |
| BG4 | VSS[213] | VSS[313] | V31 |
| BG50 | VSS[214] | VSS[314] | V32 |
| BH11 | VSS[215] | VSS[315] | V34 |
| BH15 | VSS[216] | VSS[316] | V35 |
| BH19 | VSS[217] | VSS[317] | V38 |
| BH23 | VSS[218] | VSS[318] | V43 |
| BH31 | VSS[219] | VSS[319] | V45 |
| BH35 | VSS[220] | VSS[320] | V46 |
| BH39 | VSS[221] | VSS[321] | V47 |
| BH43 | VSS[222] | VSS[322] | V49 |
| BH47 | VSS[223] | VSS[323] | V5 |
| BH7 | VSS[224] | VSS[324] | V7 |
| C12 | VSS[225] | VSS[325] | V8 |
| C50 | VSS[226] | VSS[326] | W2 |
| D51 | VSS[227] | VSS[327] | W52 |
| E12 | VSS[228] | VSS[328] | Y11 |
| E16 | VSS[229] | VSS[329] | Y12 |
| E20 | VSS[230] | VSS[330] | Y15 |
| E24 | VSS[231] | VSS[331] | Y19 |
| E30 | VSS[232] | VSS[332] | Y23 |
| E34 | VSS[233] | VSS[333] | Y28 |
| E38 | VSS[234] | VSS[334] | Y30 |
| E42 | VSS[235] | VSS[335] | Y31 |
| E46 | VSS[236] | VSS[336] | Y32 |
| E48 | VSS[237] | VSS[337] | Y38 |
| E6 | VSS[238] | VSS[338] | Y43 |
| E8 | VSS[239] | VSS[339] | Y46 |
| F49 | VSS[240] | VSS[340] | P49 |
| F5 | VSS[241] | VSS[341] | Y5 |
| G10 | VSS[242] | VSS[342] | Y6 |
| G14 | VSS[243] | VSS[343] | Y8 |
| G18 | VSS[244] | VSS[344] | P24 |
| G2 | VSS[245] | VSS[345] | T43 |
| G22 | VSS[246] | VSS[346] | AD51 |
| G32 | VSS[247] | VSS[347] | AT8 |
| G36 | VSS[248] | VSS[348] | AD47 |
| G40 | VSS[249] | VSS[349] | Y47 |
| G44 | VSS[250] | VSS[350] | AT12 |
| G52 | VSS[251] | VSS[351] | AM6 |
| AF39 | VSS[252] | VSS[352] | AT13 |
| H16 | VSS[253] | VSS[353] | AM5 |
| H20 | VSS[254] | VSS[354] | AK45 |
| H30 | VSS[255] | VSS[355] | AK39 |
| H34 | VSS[256] | VSS[356] | AV14 |
| H38 | VSS[257] | VSS[366] | |
| H42 | VSS[258] | | |

IbexPeak-M_Rev1_0

# IBEX PEAK-M (PCI-E,SMBUS,CLK)

U24B

Ibex-M 2 OF 10

PCI-E*

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

TP63 TP61 TP55 TP59 → BG30 BJ30 BF29 BH29
TP19 TP16 TP14 TP11 → AW30 BA30 BC30 BD30

3G: {24} PCIE_RXN3 / {24} PCIE_RXP3 / {24} PCIE_TXN3 / {24} PCIE_TXP3 → PCIE_RXN3 AU30, PCIE_RXP3 AT30, PCIE_TXN3_C AU32, PCIE_TXP3_C AV32
C364 *3G@0.1U/10V_4X, C365 *3G@0.1U/10V_4X
B2A

BA32 BB32 BD32 BE32

WLAN: {24} PCIE_RXN5 / {24} PCIE_RXP5 / {24} PCIE_TXN5 / {24} PCIE_TXP5 → PCIE_RXN5 BF33, PCIE_RXP5 BH33, PCIE_TXN5_C BG32, PCIE_TXP5_C BJ32
C343 0.1U/10V_4X, C342 0.1U/10V_4X

LAN: {28} PCIE_RXN6 / {28} PCIE_RXP6 / {28} PCIE_TXN6 / {28} PCIE_TXP6 → PCIE_RXN6 BA34, PCIE_RXP6 AW34, PCIE_TXN6_C BC34, PCIE_TXP6_C BD34
C379 0.1U/10V_4X, C378 0.1U/10V_4X

AT34 AU34 AU36 AV36

PCIE7/PCIE8 HM55 not support

BG34 BJ34 BG36 BJ36 AK48 AK47

B2A: TP74 TP87 → CLKOUT_PCIE0N / CLKOUT_PCIE0P

PCIE_CLK_REQ0# → P9 PCIECLKRQ0# / GPIO73 (+3V_S5)
TP21 TP27 → AM43 AM45 CLKOUT_PCIE1N / CLKOUT_PCIE1P
PCIE_CLK_REQ1# → U4 PCIECLKRQ1# / GPIO18 (+3V)
TP28 TP20 → AM47 AM48 CLKOUT_PCIE2N / CLKOUT_PCIE2P
PCIE_CLK_REQ2# → N4 PCIECLKRQ2# / GPIO20 (+3V)

LAN: {28} CLK_PCIE_LAN# / {28} CLK_PCIE_LAN → AH42 AH41 CLKOUT_PCIE3N / CLKOUT_PCIE3P
{28} PCIE_CLK_REQ3# → PCIE_CLK_REQ3# A8 PCIECLKRQ3# / GPIO25 (+3V_S5)

3G: {24} CLK_PCIE_3G# / {24} CLK_PCIE_3G → AM51 AM53 CLKOUT_PCIE4N / CLKOUT_PCIE4P
{24} PCIE_CLK_REQ4# → PCIE_CLK_REQ4# M9 PCIECLKRQ4# / GPIO26 (+3V_S5)

WLAN: {24} CLK_PCIE_MINI# / {24} CLK_PCIE_MINI → AJ50 AJ52 CLKOUT_PCIE5N / CLKOUT_PCIE5P
{24} PCIE_CLK_RQ5# → PCIE_CLK_RQ5# H6 PCIECLKRQ5# / GPIO44 (+3V_S5)

TP70 TP71 → AK53 AK51 CLKOUT_PEG_B_N / CLKOUT_PEG_B_P
PCIE_CLK_REQB# → P13 PEG_B_CLKRQ# / GPIO56 (+3V_S5)

IbexPeak-M_Rev1_0

## SMBus

(+3V_S5) SMBALERT# / GPIO11 → B9 SMBALERT#
SMBCLK → H14 SCLK → SCLK {2,24,28,33}
SMBDATA → C8 SDATA → SDATA {2,24,28,33}
(+3V_S5) SML0ALERT# / GPIO60 → J14 SMBL0ALERT#
SML0CLK → C6 SMB_CLK_ME0
SML0DATA → G8 SMB_DATA_ME0
(+3V_S5) SML1ALERT# / GPIO74 → M14 SML1ALERT#
(+3V_S5) SML1CLK / GPIO58 → E10 MBCLK2
(+3V_S5) SML1DATA / GPIO75 → G12 MBDATA2

## Controller Link

CL_CLK1 → T13 CL_CLK1 → CL_CLK1 {24}
CL_DATA1 → T11 CL_DATA1 → CL_DATA1 {24}
CL_RST1# → T9 CL_RST#1 → CL_RST#1 {24}

## PEG

(+3V_S5) PEG_A_CLKRQ# / GPIO47 → H1 PEG_CLKREQ#
CLKOUT_PEG_A_N → AD43 → CLK_PCIE_VGA# {15}
CLKOUT_PEG_A_P → AD45 → CLK_PCIE_VGA {15}
CLKOUT_DMI_N → AN4 → CLK_PCIE_3GPLLN {3}
CLKOUT_DMI_P → AN2 → CLK_PCIE_3GPLLP {3}

## From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N → AT1 → CLK_DREFSSCLKN {3}
CLKOUT_DP_P / CLKOUT_BCLK1_P → AT3 → CLK_DREFSSCLKP {3}
CLKIN_DMI_N → AW24 → CLK_BUF_PCIE_3GPLLN {2}
CLKIN_DMI_P → BA24 → CLK_BUF_PCIE_3GPLLP {2}
CLKIN_BCLK_N → AP3 → CLK_BUF_BCLKN {2}
CLKIN_BCLK_P → AP1 → CLK_BUF_BCLKP {2}
CLKIN_DOT_96N → F18 → CLK_BUF_DREFCLKN {2}
CLKIN_DOT_96P → E18 → CLK_BUF_DREFCLKP {2}
CLKIN_SATA_N / CKSSCD_N → AH13 → CLK_BUF_DREFSSCLKN {2}
CLKIN_SATA_P / CKSSCD_P → AH12 → CLK_BUF_DREFSSCLKP {2}
REFCLK14IN → P41 → CLK_PCH_14M {2}
CLKIN_PCILOOPBACK → J42 CLK_PCI_FB → CLK_PCI_FB {9}
XTAL25_IN → AH51 XTAL25_IN
XTAL25_OUT → AH53 XTAL25_OUT
XCLK_RCOMP → AF38 XCLK_RCOMP
R226 90.9/F_4 → +1.05V

## Clock Flex

(+3V) CLKOUTFLEX0 / GPIO64 → T45 CLK_FLEX0
(+3V) CLKOUTFLEX1 / GPIO65 → P43 CLK_FLEX1 → T34
(+3V) CLKOUTFLEX2 / GPIO66 → T42 CLK_FLEX2 → T33
(+3V) CLKOUTFLEX3 / GPIO67 → N50 CLK_FLEX3 → R257 22_4 → 48M_CARD {29}
R235 10K_4 → +3V

48M_Card Reserve for cardreader 48MHZ

## C3A

+3V_S5
MBDATA2 → 1 Q15 2N7002_200MA 3 → 2ND_MBDATA {30}
+3V_S5
MBCLK2 → 1 Q13 2N7002_200MA 3 → 2ND_MBCLK {30}

## +3V

PCIE_CLK_REQ1# R588 10K_4
PCIE_CLK_REQ2# R600 10K_4

## +3V_S5

| | | |
|---|---|---|
| SMBALERT# | R650 | 10K_4 |
| SCLK | R311 | 2.2K_4 |
| SDATA | R654 | 2.2K_4 |
| SMBL0ALERT# | R300 | 10K_4 |
| SMB_CLK_ME0 | R631 | 2.2K_4 |
| SMB_DATA_ME0 | R623 | 2.2K_4 |
| SML1ALERT# | R310 | 10K_4 |
| MBCLK2 | R299 | 2.2K_4 |
| MBDATA2 | R313 | 2.2K_4 |

## +3V_S5

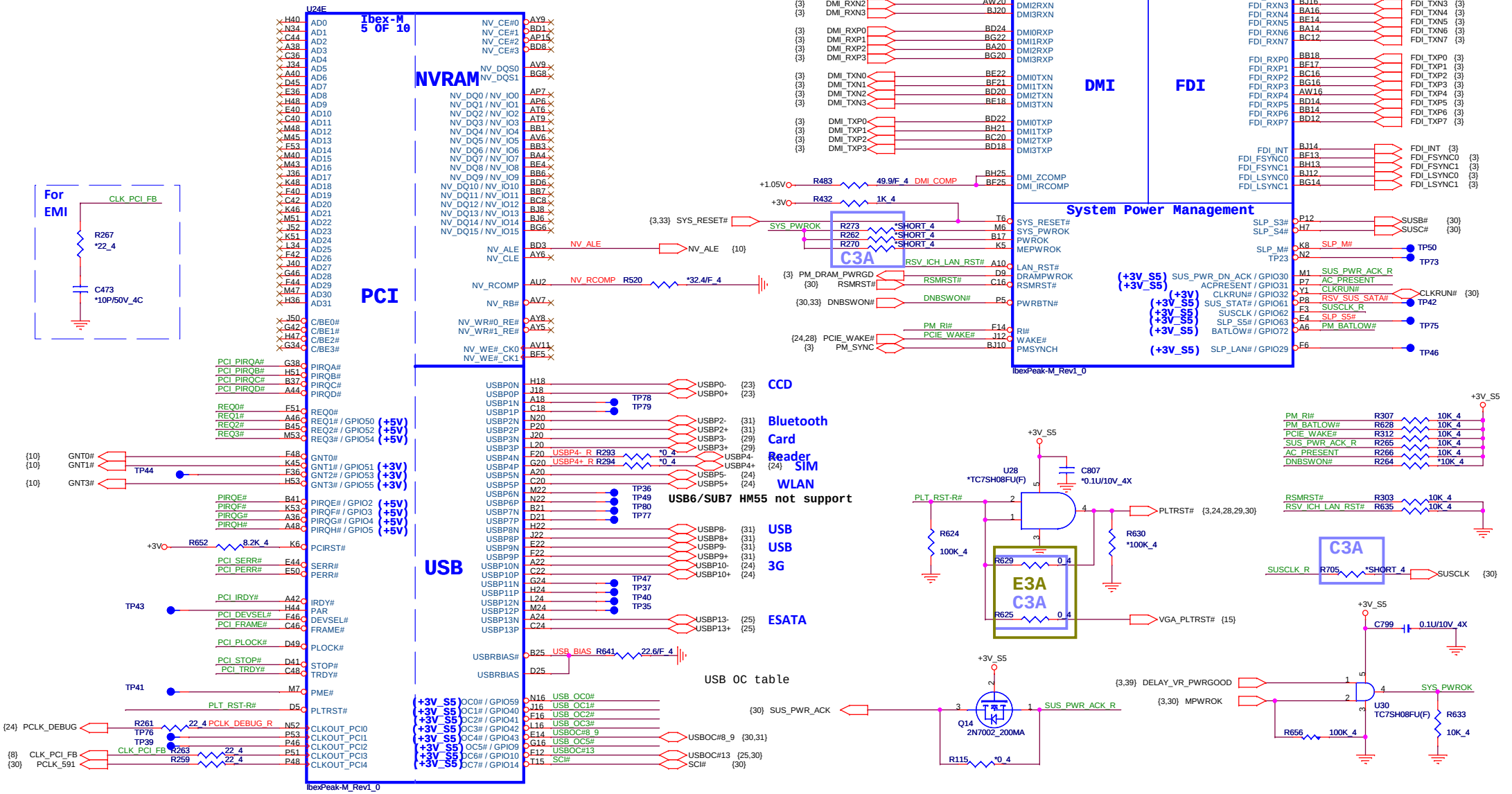
PCIE_CLK_REQ0# R309 10K_4
B2A
PCIE_CLK_REQ3# R653 *10K_4
PCIE_CLK_REQ4# R276 10K_4
PCIE_CLK_REQB# R301 10K_4
PCIE_CLK_RQ5# R619 10K_4
PEG_CLKREQ# R615 IV@10K_4
PEG_CLKREQ# R610 EV@10K_4

## Placement close

R560 EV@0_4
XTAL25_IN — C749 IV@27P/50V_4N
R552 IV@1M/F_4
Y4 IV@25MHZ_30
XTAL25_OUT — C747 IV@27P/50V_4N
B2A

| | | |
|---|---|---|
| Quanta Computer Inc. | PROJECT : BL6 | |
| Size | Document Number: PCH 2/5 (PCIE, SMBUS, CK) | Rev A1A |
| Date: Saturday, April 10, 2010 | Sheet 8 of 45 | |

# IBEX PEAK-M (PCI,USB,NVRAM)




# IBEX PEAK-M (DMI,FDI,GPIO)





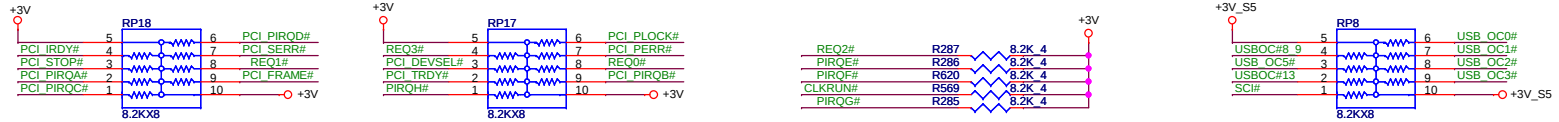








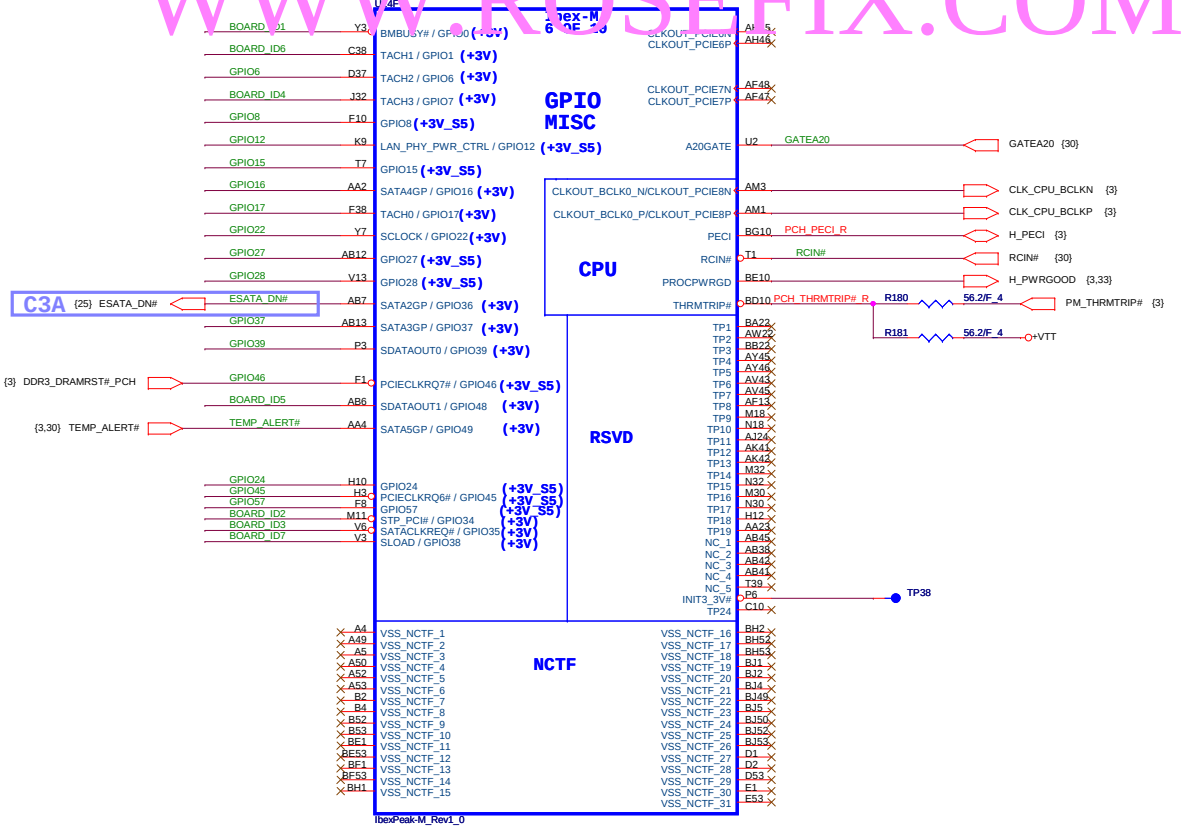


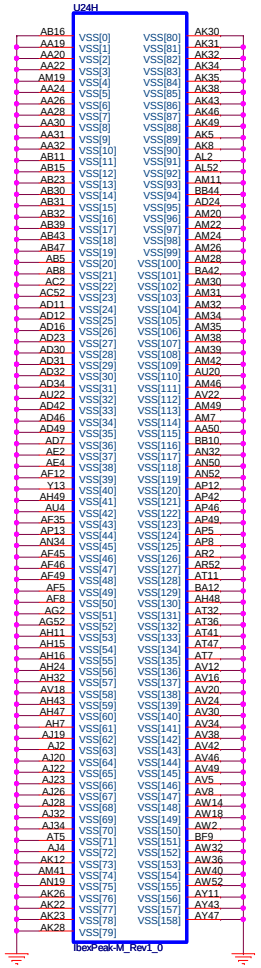

Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | PCH 3/5 (PCI,ONFI,USB,DMI) | A1A |
| Date: Saturday, April 10, 2010 | Sheet 9 of 45 | |

# IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)




# IBEX PEAK-M (GND)




## PCH Strap Pin Configuration Table

### SPKR

{7,27} PCBEEP — R592 *1K_4 — +3V

Reboot option at power-up

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

### GNT3# / GPIO55

{9} GNT3# — R622 *10K_4

Top-Block Swap Override

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

### HDA_DOCK_EN #/GPIO33

{7,30} PCH_GPIO33 — R282 1K_4 — E3A — JP1 2 — *SHORT PAD 1

Flash Descriptor Security Override

0 = Flash Descriptor Security will be overridden
1 = Security measure defined in the Flash Descriptor will be enabled.

### GNT0#, GNT1#

{9} GNT0# — R272 *1K_4
{9} GNT1# — R621 *1K_4

| Boot BIOS Strap | | |
|---|---|---|
| PCI_GNT0# | GNT#1 | Boot BIOS Location |
| 0 | 0 | LPC |
| 0 | 1 | PCI |
| 1 | 0 | Reserved (NAND) |
| 1 | 1 | SPI |

### SPI_MOSI

{7} SPI_SI_R — R504 *1K_4 — +3V

TPM Functionality Disable

1 = Enabled
0 = Disable

### NV_ALE

{9} NV_ALE — R496 *10K_4 — +1.8V

IntelR Anti-Theft Technology
HDD Data Protection
(Intel AT-d) Enable

1 = Enabled
0 = Disabled (Default)

### GPIO8

GPIO8 — R298 10K_4 — +3V_S5

Reserved

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

### GPIO15

GPIO15 — R248 1K_4 — +3V_S5

Reserved

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

### GPIO27

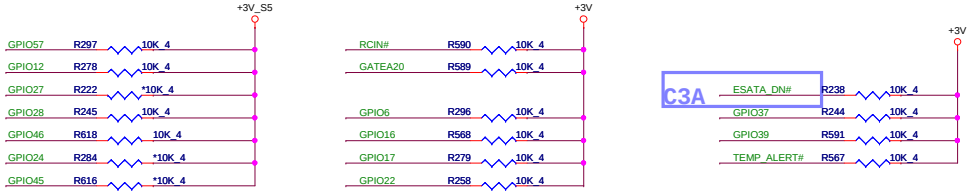
GPIO27 — R232 *10K_4

On-Die PLL Voltage Regulator

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

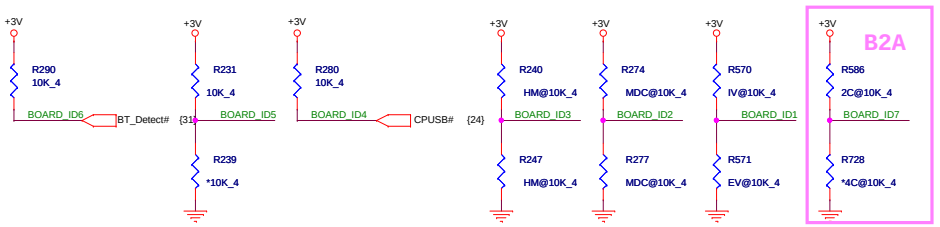
+RTC_CELL — R644 330K_6 — PCH_INVRMEN — {7}

```
INTVRMEN - Integrated 5US 1.1V VRM Enable
High - Enable Internal VRs
```



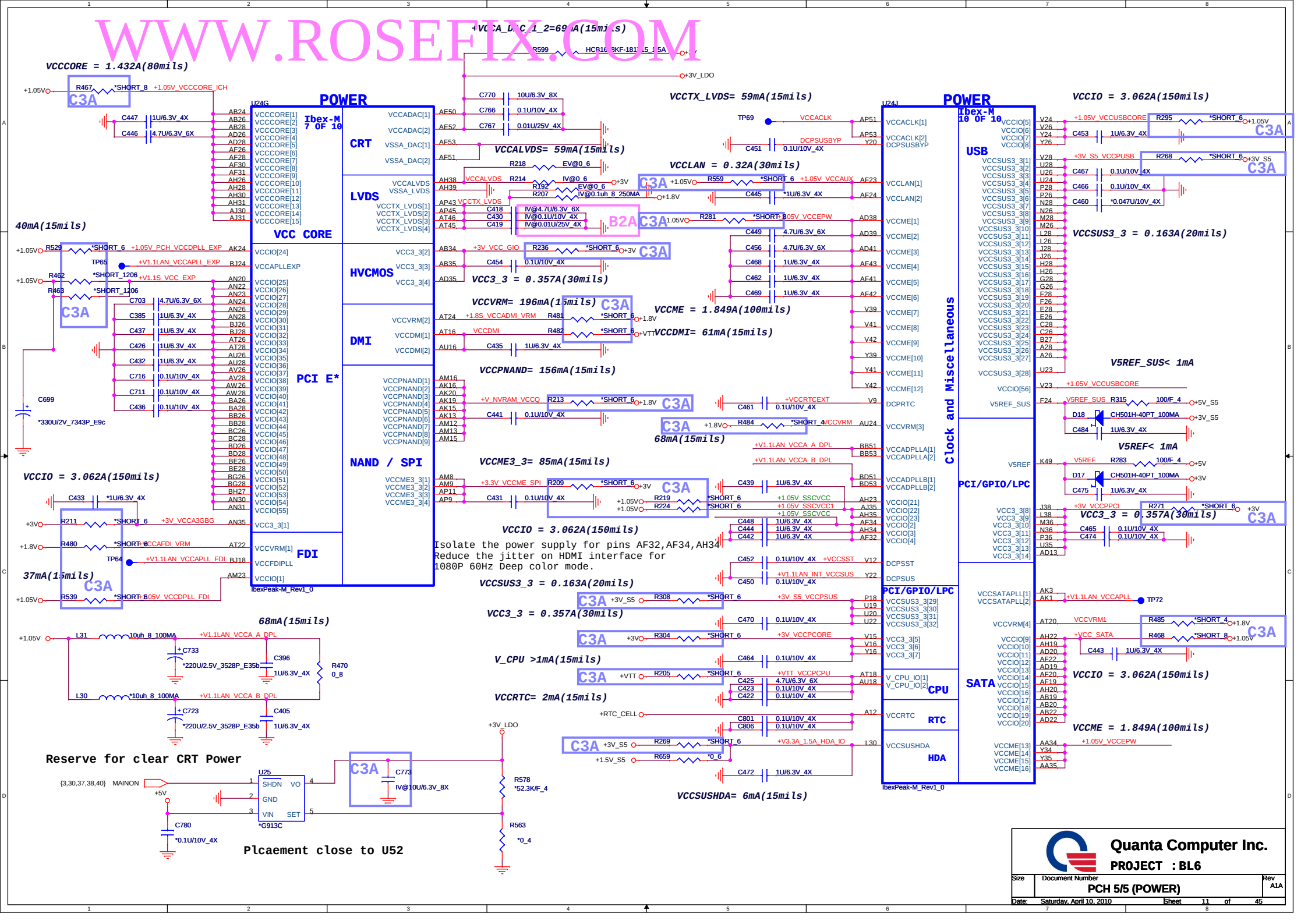

## BOARD ID SETTING

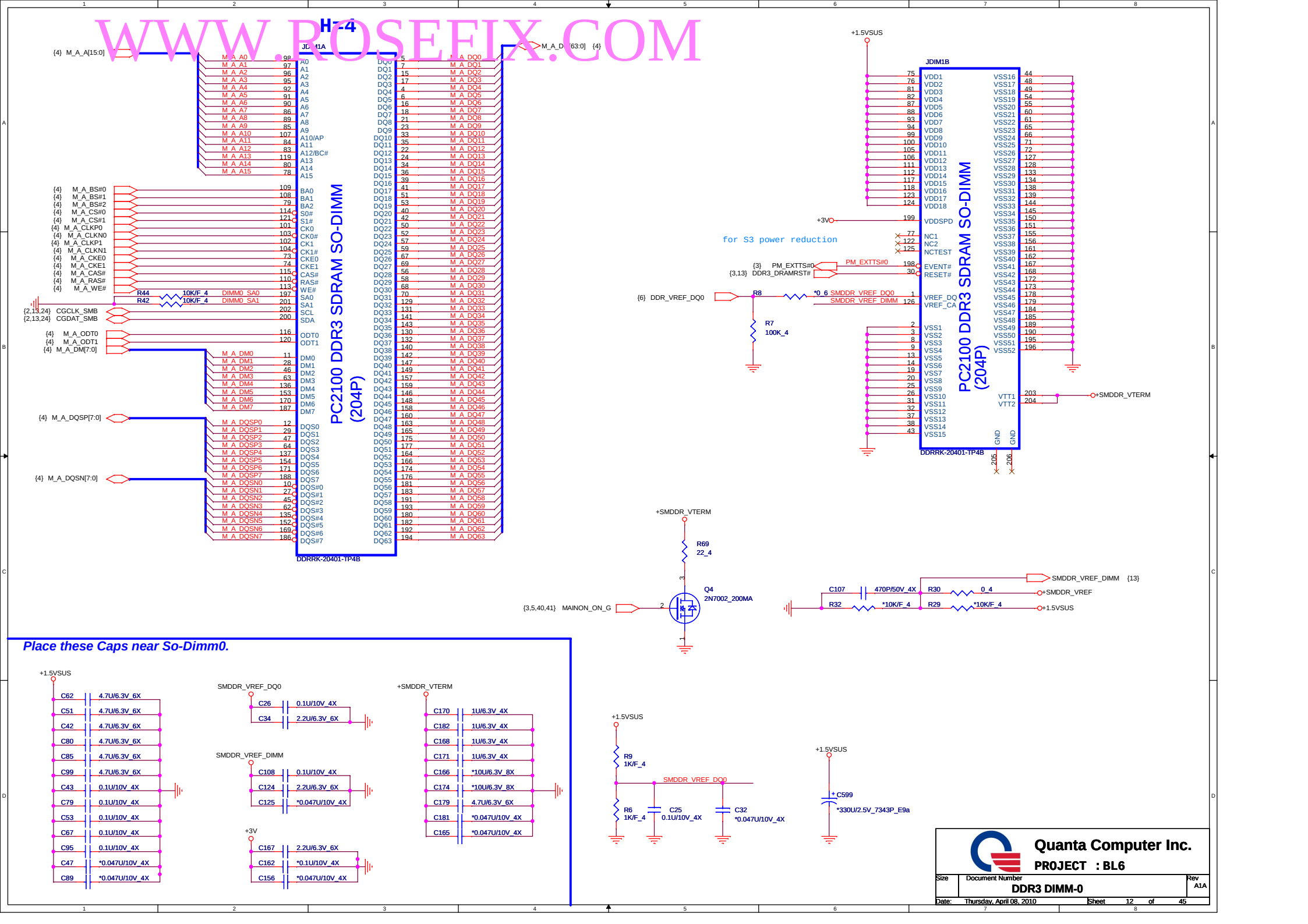
| Board ID | ID1 | ID2 | ID3 | ID4 | ID5 | ID6 | ID7 |
|---|---|---|---|---|---|---|---|
| UMA SKU<br>VGA SKU | H<br>L | | | | | | |
| W/ MDC<br>W/O MDC | | H<br>L | | | | | |
| W/ HDMI<br>W/O HDMI | | | H<br>L | | | | |
| W/O 3G<br>W/ 3G | | | | H<br>L | | | |
| 15"<br>14" | | | | | H<br>L | | |
| W/O BT<br>W/ BT | | | | | | H<br>L | |
| 2 Core<br>4 Core | | | | | | | H<br>L |



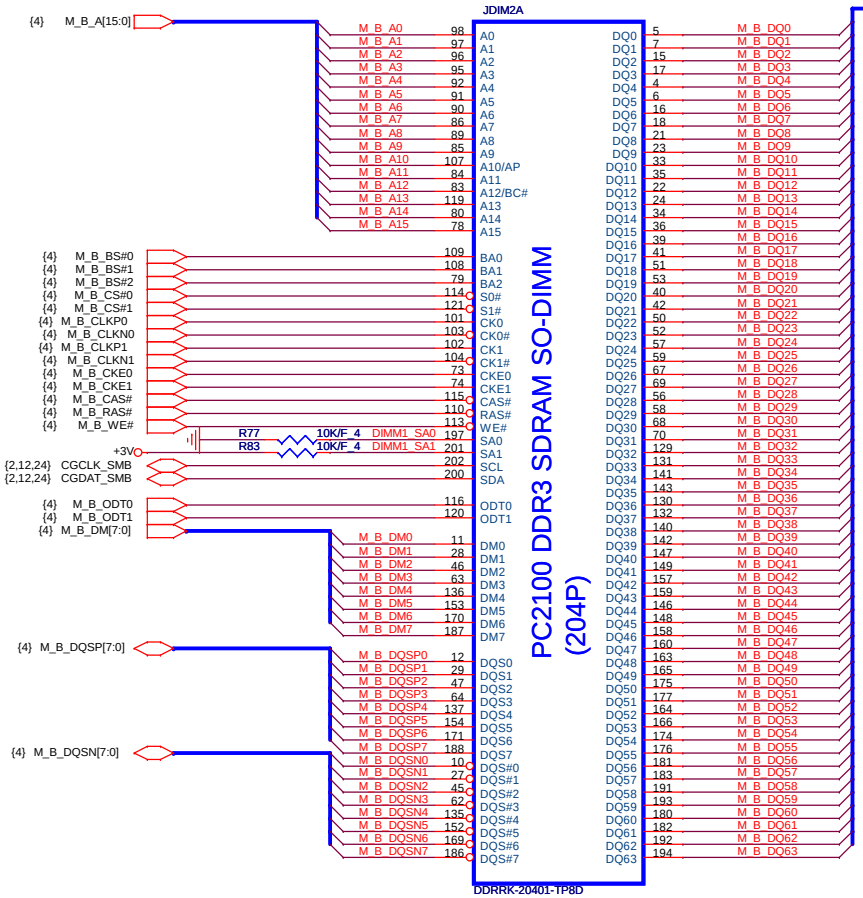

Quanta Computer Inc.
PROJECT : BL6

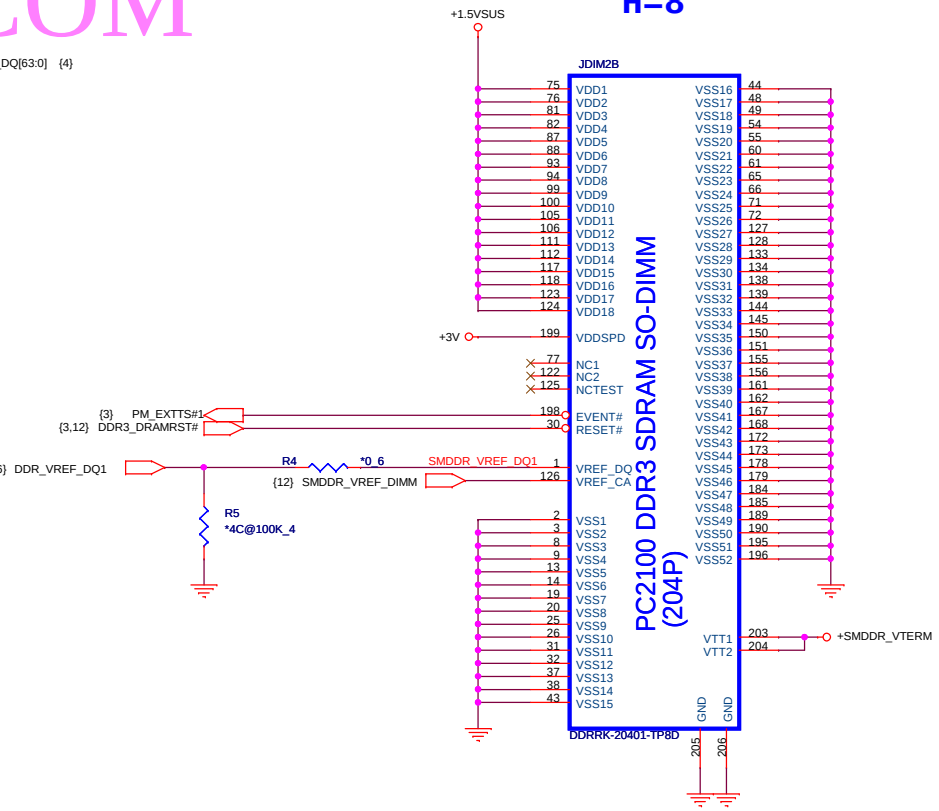
| Size | Document Number | Rev |
|---|---|---|
| | PCH 4/5 (GPIO & Strap) | A1A |
| Date: Saturday, April 10, 2010 | Sheet 10 of 45 | |



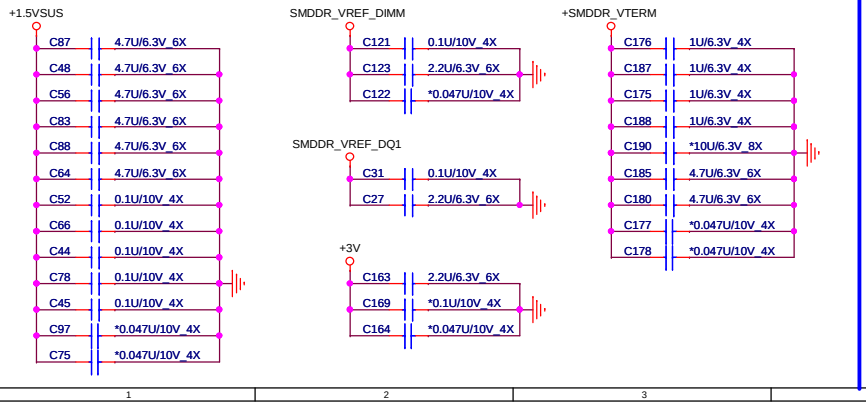


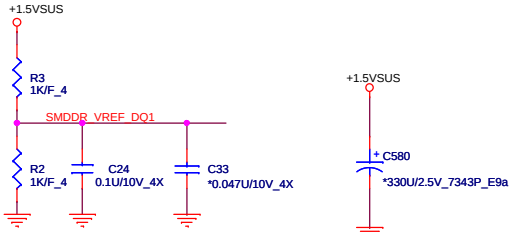
H=8




## Place these Caps near So-Dimm1.



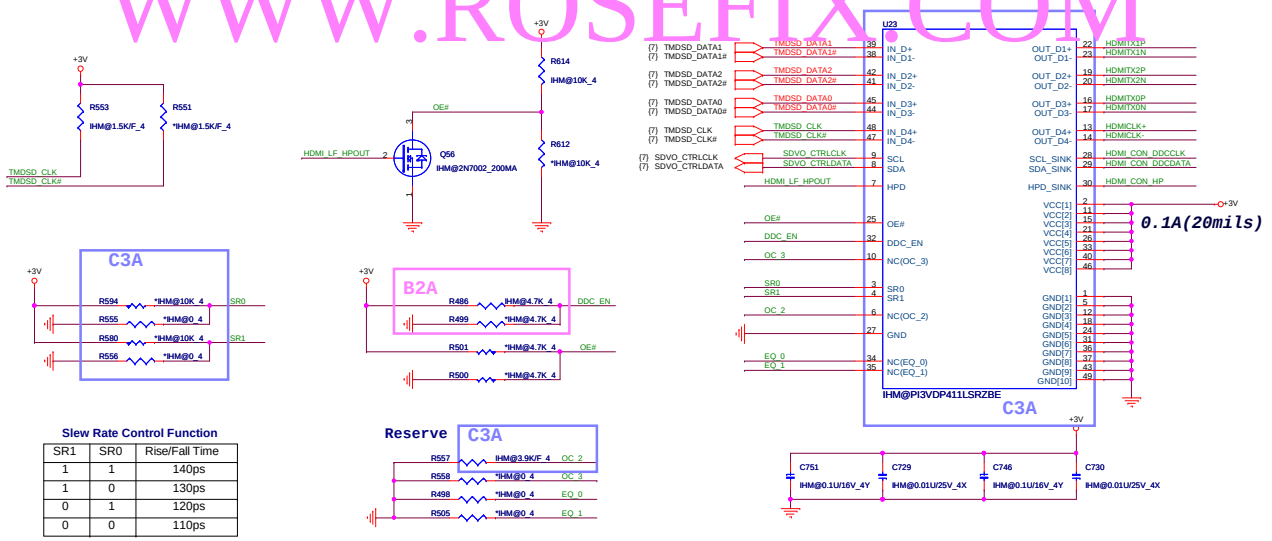

Quanta Computer Inc.

PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | DDR3 DIMM-1 | A1A |

Date: Thursday, April 08, 2010 Sheet 13 of 45

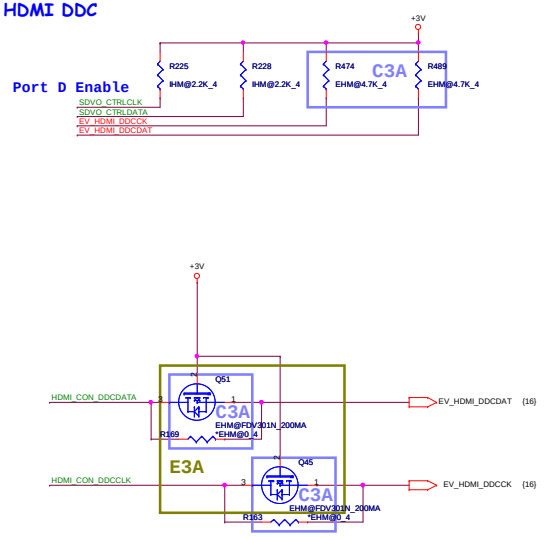
## HDMI Level Shift



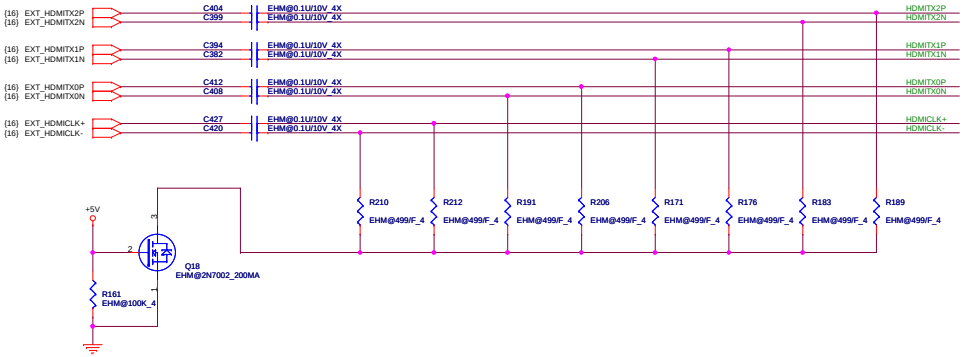

**Slew Rate Control Function**

| SR1 | SR0 | Rise/Fall Time |
|---|---|---|
| 1 | 1 | 140ps |
| 1 | 0 | 130ps |
| 0 | 1 | 120ps |
| 0 | 0 | 110ps |

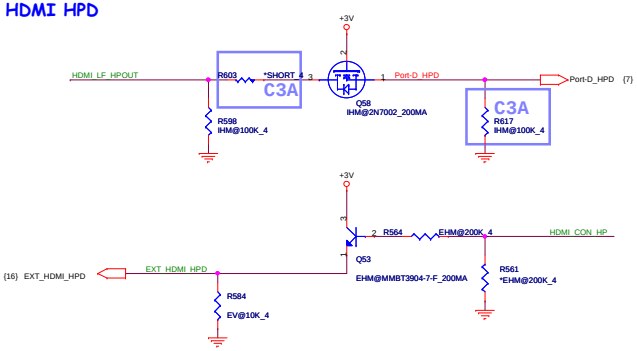
## HDMI DDC

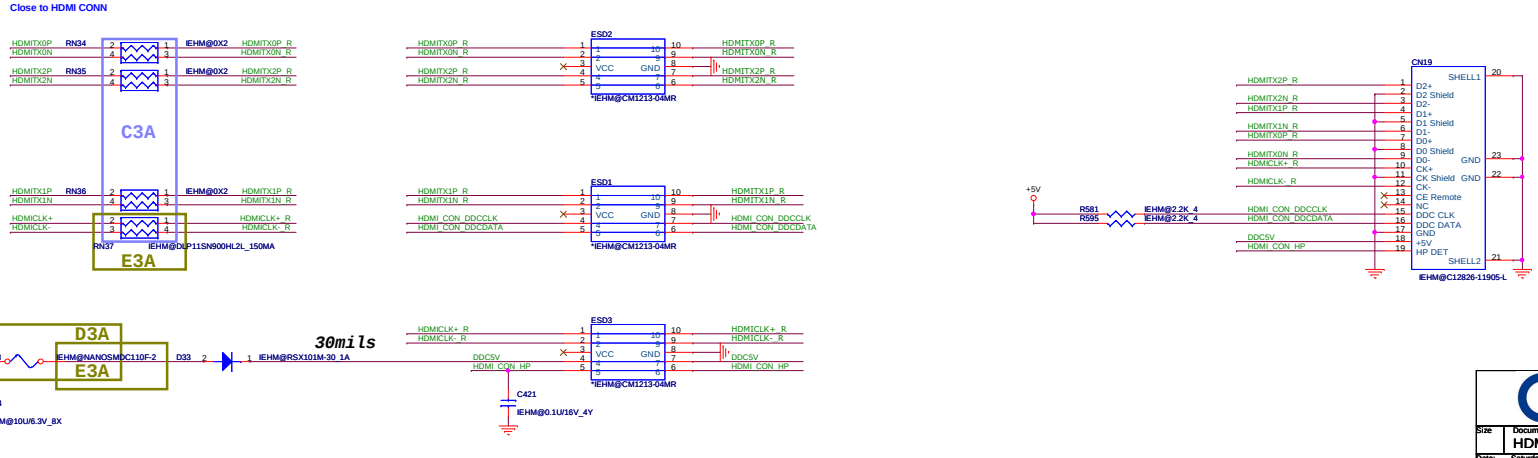



## Discrete HDMI




## HDMI HPD

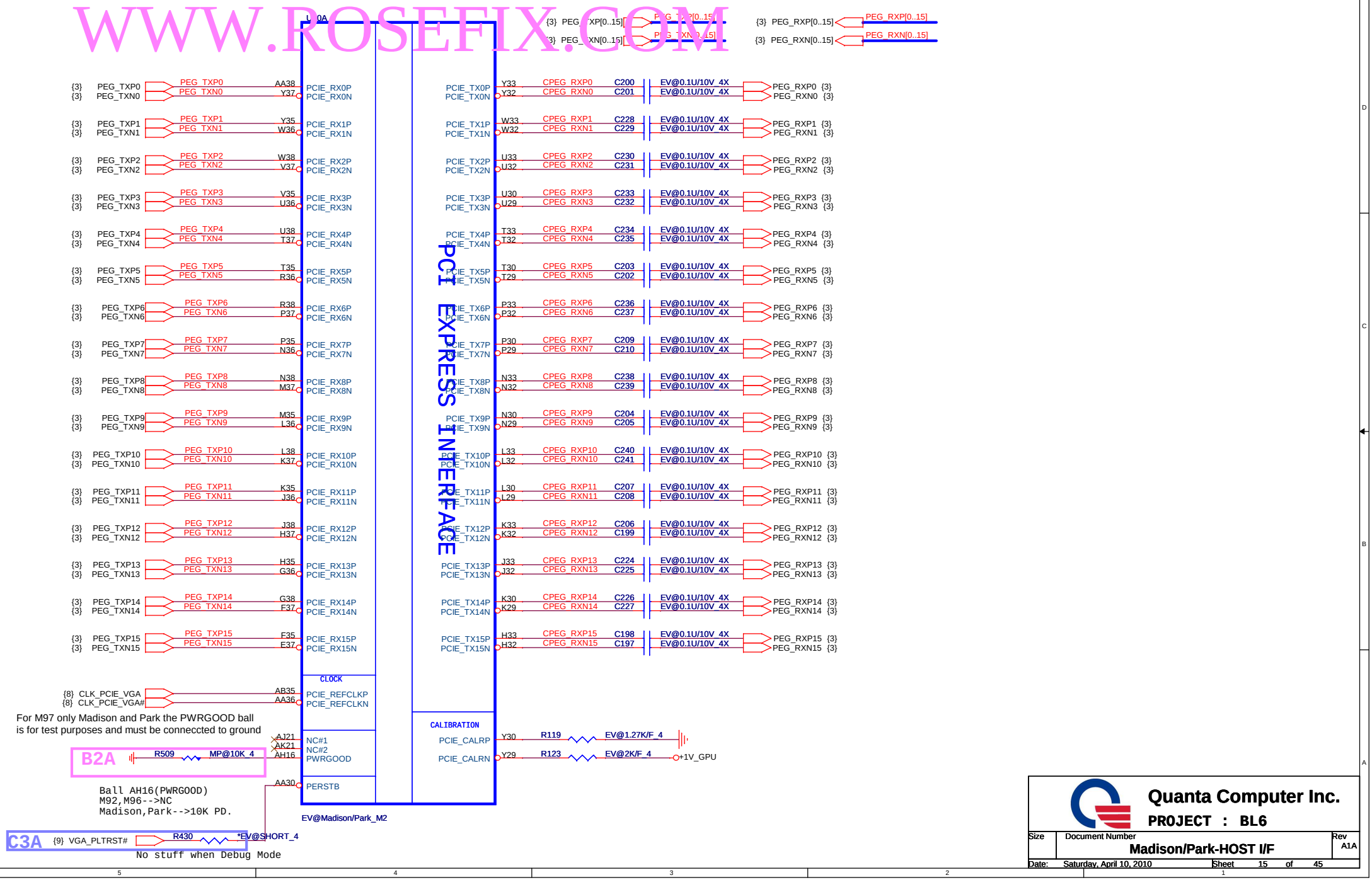



Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | HDMI CONN | A1A |

Date: Saturday, April 10, 2010 Sheet 14 of 45




Quanta Computer Inc.

PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | Madison/Park-HOST I/F | A1A |
| Date: Saturday, April 10, 2010 | Sheet 15 of 45 | |

B2A

JTAG SIGNAL STUFF OPTION FOR OPTION2

| SIGNALS | NORMAL MODE | JTAG MODE (DEBU |
|---|---|---|
| TESTEN | "1" (PU) | "1" (PU) |
| GPIO24_TRSTB | "0" (PD) | "1" (PU) |
| GPIO26_TCK | CLK | "1" (PU) |
| GPIO27_TMS | "1" (PU) | "1" (PU) |

1.8V GPIO

B2A
NC on Park
M92,M96,Madison support

B2A
NC on Park
M92,M96,Madison support

SCL must be tied high if not used

B2A
Park Channel D-->No support
M92 Channel C&D-->No support

HDMI

LVDS

EV@Madison/Park_M2

TjMax = 110
change by VBIOS

B2A
M92,M96 GPIO_21 pin control BB function.Park,Madison no suport.

B2A
M96,Madison-->support
Ball AH26-->HPD5
Ball AH24-->HPD6
M92,Park-->No support

JTAG need Option2 for Park,Madison Engineer sample

Place close to Chip

+1.8V(20mA)
5mA (5mils)

B2A
Madison,Park-->125mA (10mils)
M92,M96-->300mA(20mils)

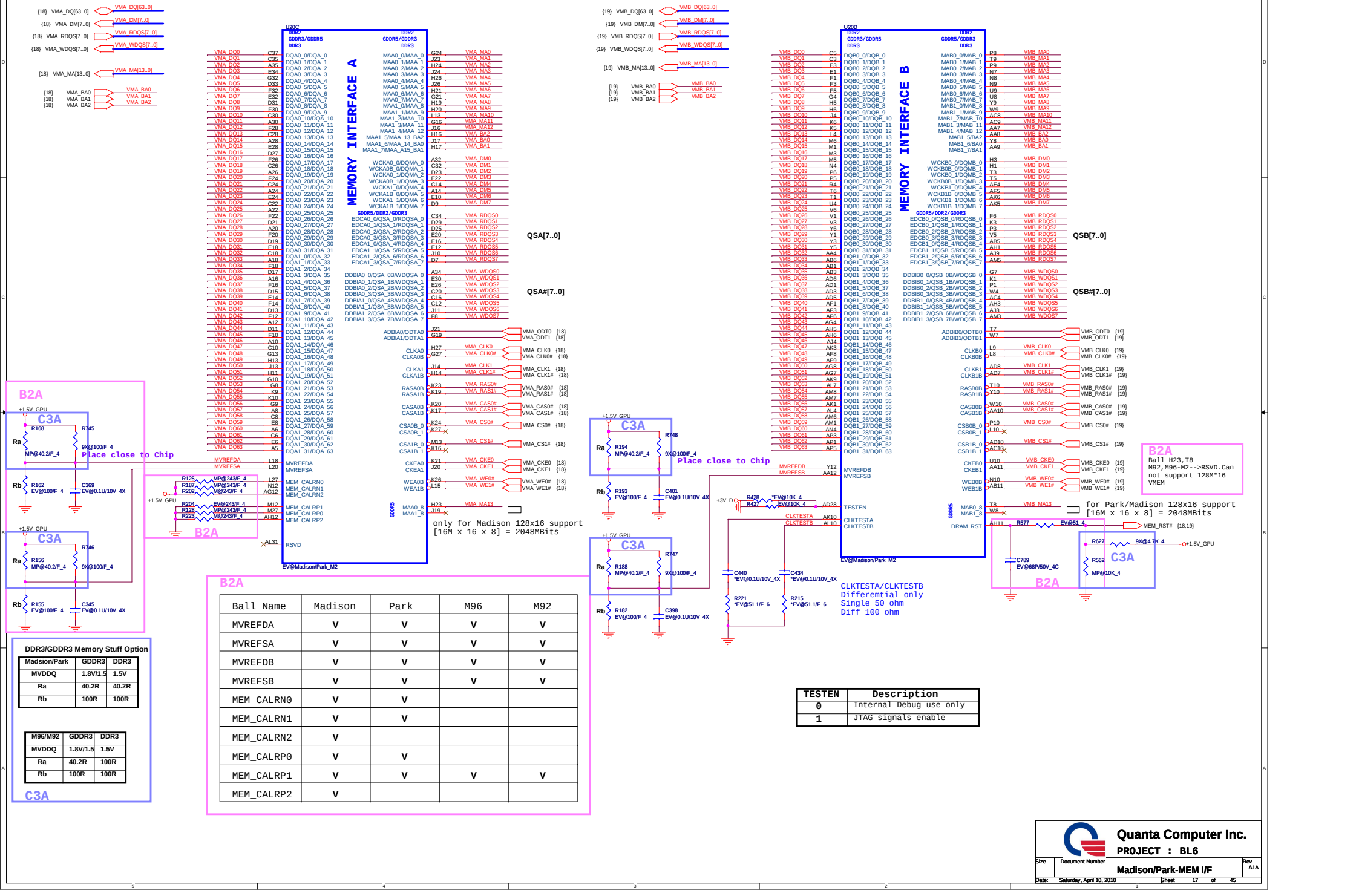
B2A
Port 3
M96,Madison,Park-->support
M92-->No support
Port 4
M96,Madison-->support
M92,Park-->No support

B2A
Port7
Madison-->support
M92,M96,Park-->No support

(1.8V@70mA AVDD)
(1.8V@45mA VDD1DI/ 50mA VFF2D)
(1.8V@1.5mA A2VDDQ)
(3.3V@130mA A2VDD)

Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | Madison/Park-HOST I/F | A1A |
| Date: Saturday, April 10, 2010 | Sheet 16 of 45 | |




DDR3/GDDR3 Memory Stuff Option

| Madsion/Park | GDDR3 | DDR3 |
|---|---|---|
| MVDDQ | 1.8V/1.5 | 1.5V |
| Ra | 40.2R | 40.2R |
| Rb | 100R | 100R |

| M96/M92 | GDDR3 | DDR3 |
|---|---|---|
| MVDDQ | 1.8V/1.5 | 1.5V |
| Ra | 40.2R | 100R |
| Rb | 100R | 100R |

| Ball Name | Madison | Park | M96 | M92 |
|---|---|---|---|---|
| MVREFDA | V | V | V | V |
| MVREFSA | V | V | V | V |
| MVREFDB | V | V | V | V |
| MVREFSB | V | V | V | V |
| MEM_CALRN0 | V | V | | |
| MEM_CALRN1 | V | V | | |
| MEM_CALRN2 | V | | | |
| MEM_CALRP0 | V | V | | |
| MEM_CALRP1 | V | V | V | V |
| MEM_CALRP2 | V | | | |

| TESTEN | Description |
|---|---|
| 0 | Internal Debug use only |
| 1 | JTAG signals enable |

Quanta Computer Inc.
PROJECT : BL6
Size | Document Number: Madison/Park-MEM I/F | Rev A1A
Date: Saturday, April 10, 2010 | Sheet 17 of 45

# CHANNEL A: 512MB DDR3 (64M*16*4pcs)

{17} VMA_DQ[63..0]
{17} VMA_DM[7..0]
{17} VMA_RDQS[7..0]
{17} VMA_WDQS[7..0]
{17} VMA_MA[13..0]

QSA_[7..0]
QSA_[7..0]

U6 — TOP Left

U19 — BOT Left

U9 — BOT Right

U22 — TOP Right

100-BALL SDRAM DDR3
MEV@VRAM _DDR3

+1.5V_GPU

{17,19} MEM_RST#

R113 MEV@243/F_4
R472 MEV@243/F_4
R151 MEV@243/F_4
R516 EV@243/F_4

## Group-A0 VREF

R124 MEV@4.99K/F_4
R120 MEV@4.99K/F_4
C286 MEV@0.1U/10V_4X
VREFC_VMA1

R138 MEV@4.99K/F_4
R147 MEV@4.99K/F_4
C314 MEV@0.1U/10V_4X
VREFD_VMA1

R477 MEV@4.99K/F_4
R475 MEV@4.99K/F_4
C700 MEV@0.1U/10V_4X
VREFC_VMA2

R452 MEV@4.99K/F_4
R450 MEV@4.99K/F_4
C683 MEV@0.1U/10V_4X
VREFD_VMA2

## Group-A1 VREF

R166 MEV@4.99K/F_4
R154 MEV@4.99K/F_4
C351 MEV@0.1U/10V_4X
VREFC_VMA3

R179 MEV@4.99K/F_4
R186 MEV@4.99K/F_4
C406 MEV@0.1U/10V_4X
VREFD_VMA3

R497 MEV@4.99K/F_4
R503 MEV@4.99K/F_4
C734 MEV@0.1U/10V_4X
VREFC_VMA4

R507 MEV@4.99K/F_4
R506 MEV@4.99K/F_4
C732 MEV@0.1U/10V_4X
VREFD_VMA4

## MEM_A0 CLK

VMA_CLK0
VMA_CLK0#
R112 MEV@56.2/F_4
R110 MEV@56.2/F_4
C266 MEV@0.01U/25V_4X

## Group-A0 decoupling CAP

C674 C260 C262 C665 C671 C664 C695 C686 MEV@1U/6.3V_4X
C303 C687 C685 C254 C251 C257 C667 C681 MEV@1U/6.3V_4X
C309 C675 C252 C676 C689 MEV@10U/6.3V_8X

## Group-A1 decoupling CAP

C249 C350 C253 C706 C327 C407 C748 C741 MEV@1U/6.3V_4X
C737 C717 C714 C334 C750 C745 C753 C381 MEV@1U/6.3V_4X
C778 C367 C713 C438 C701 MEV@10U/6.3V_8X

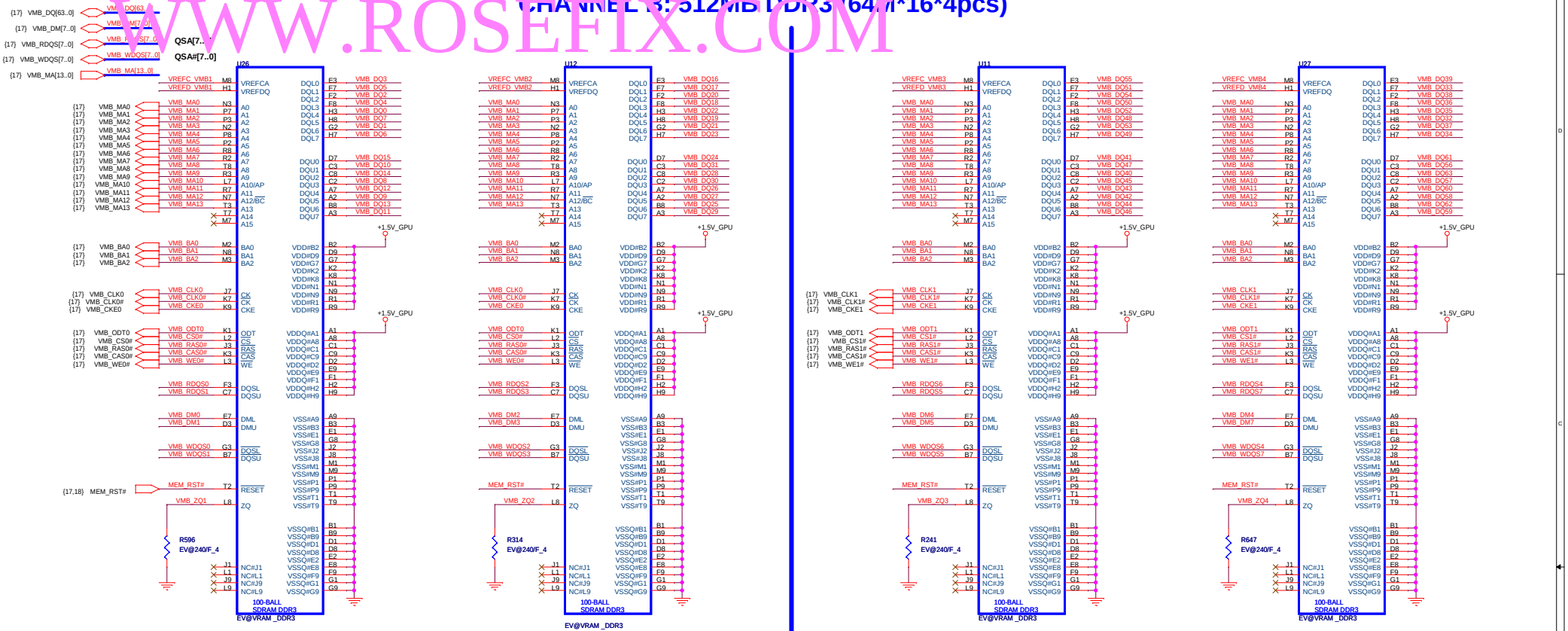
## MEM_A1 CLK

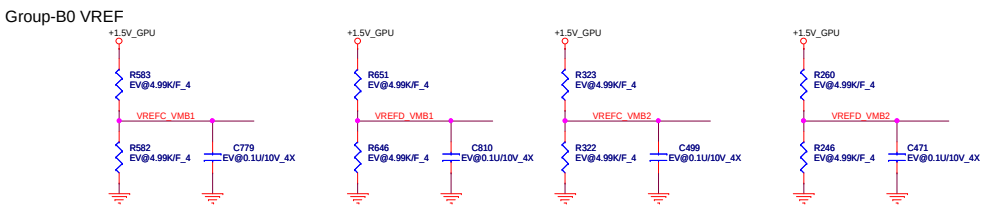
VMA_CLK1
VMA_CLK1#
R195 MEV@56.2/F_4
R208 MEV@56.2/F_4
C429 MEV@0.01U/25V_4X

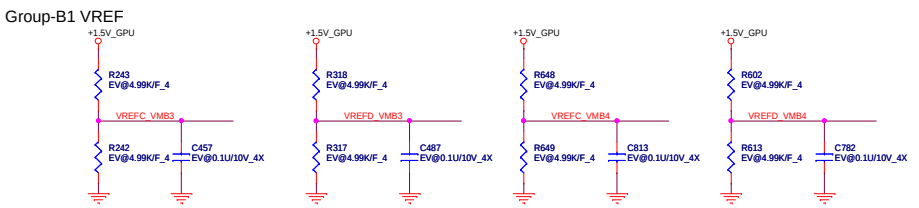
Quanta Computer Inc.
PROJECT : BL6

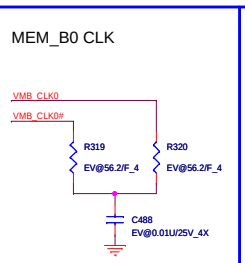
| Size | Document Number | Rev |
|---|---|---|
| | VRAM_A: DDR3-64M*16*4PCS | A1A |
| Date: Saturday, April 10, 2010 | Sheet 18 of 45 | |

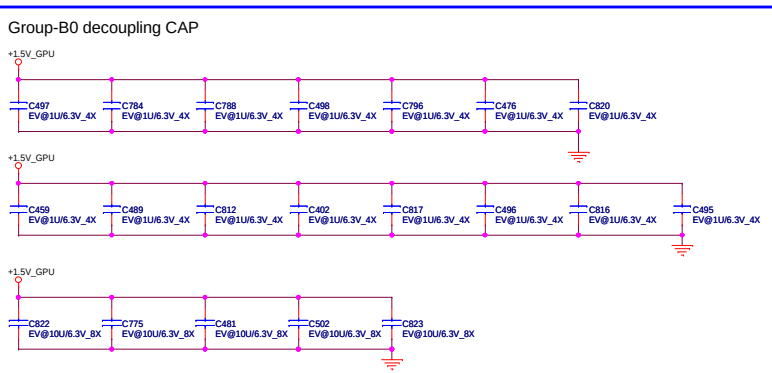
# CHANNEL B: 512MB DDR3 (64M*16*4pcs)

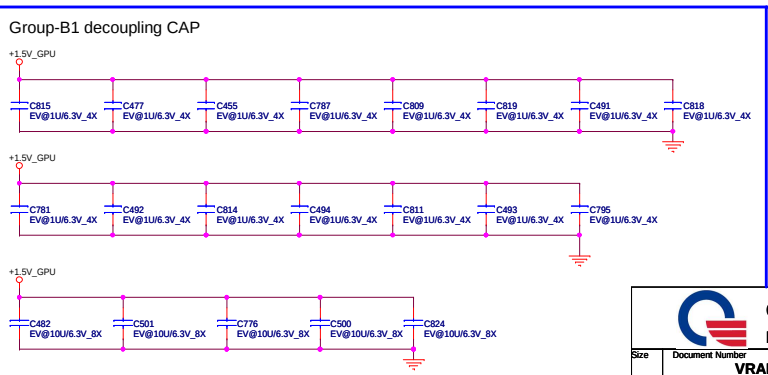


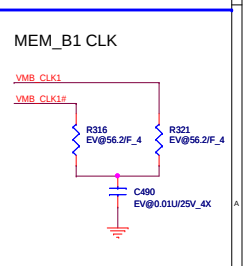




Quanta Computer Inc.

PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | VRAM_B: DDR3-64M*16*4PCS | A1A |
| Date: Saturday, April 10, 2010 | Sheet 19 of 45 | |

For Madison / and Park, VDDCI and VDDC can share one common regulator

VDD/VDDQ =1.5V at 1333
VDD/VDDQ =1.8V at 1600 and 1800

(1.5V@3.4A_VDDR1)

(1.8V@17mA VDD_CT)

(3.3V@60mA)

(1.8V@170mA)

(1.8V@40mA PCIE_PVDD)

(1.8V@150mA MPV18)

(1.8V@50mA SPV18)

(1.0V@100mA SPV10)

(1.8V@40mA PCIE_VDDR)

(1.0V@2A PCIE_VDDC)

(30A or more)

(DDR3 1.12V@4A VDDCI) or more

VDDCI:33.6A

GND

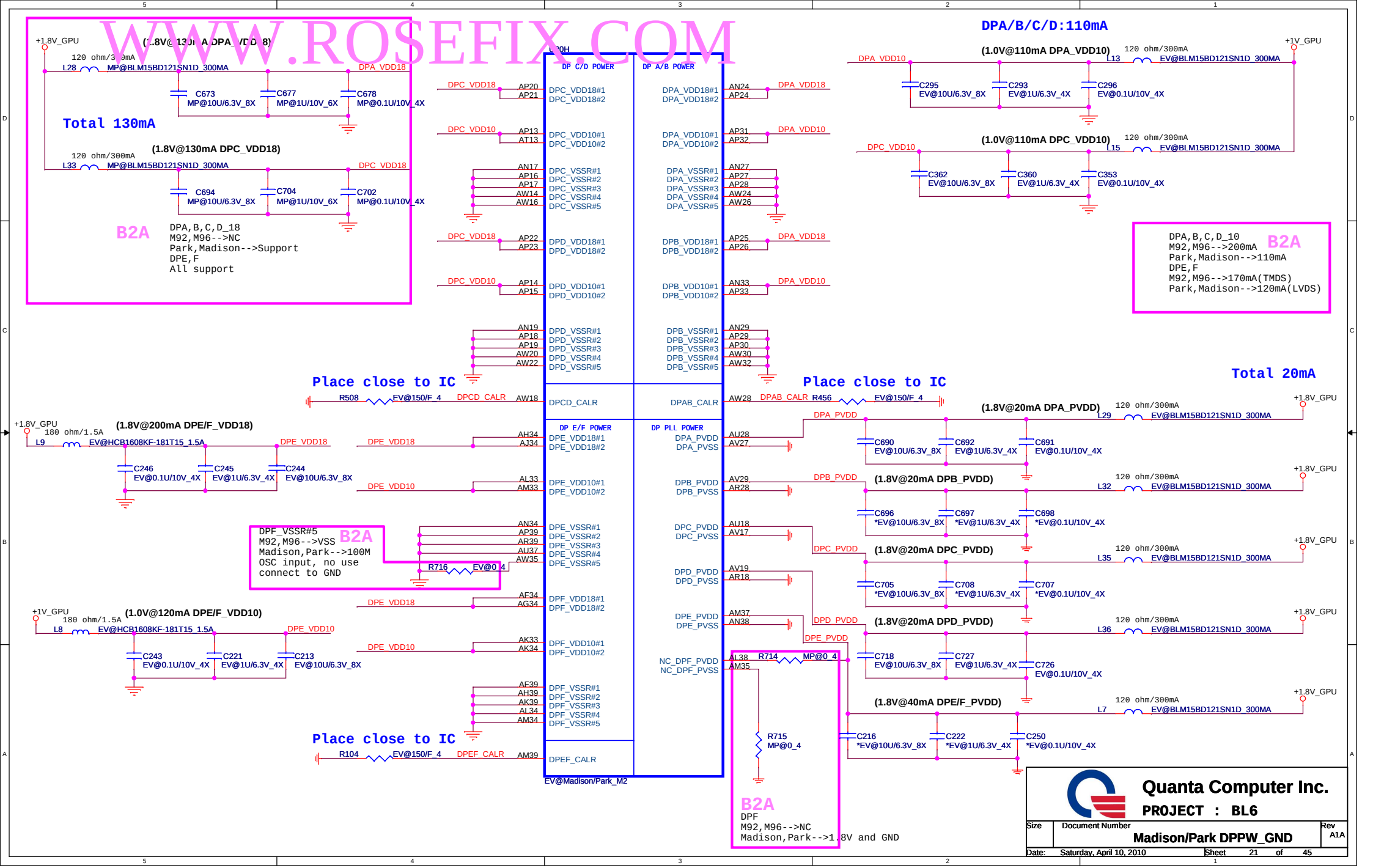
GPU +3V power
0.5A

Route as differential Pair

B2A

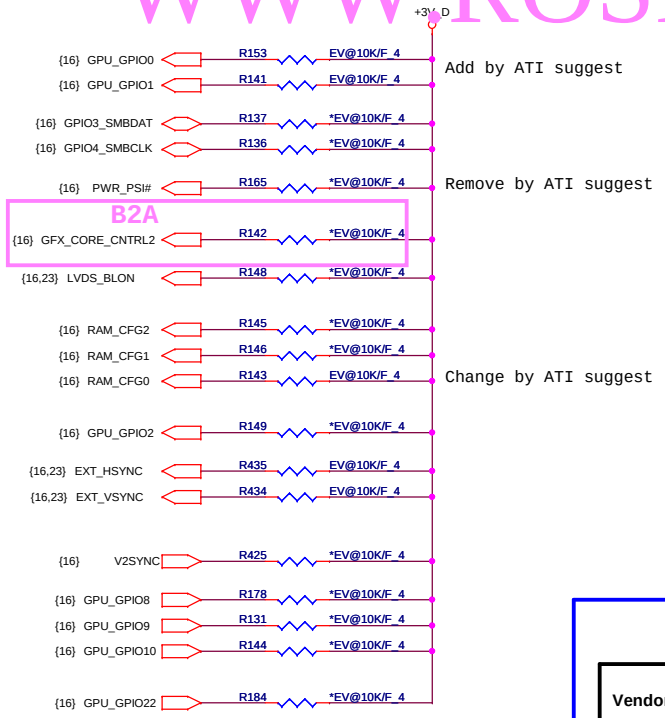
| | M92 | M96 | Park | Madison |
|---|---|---|---|---|
| VDDRHA | NC | VDDR1 | NC | NC |
| VDDRHB | VDDR1 | VDDR1 | NC | NC |
| VSSRHA | NC | VSS | NC | NC |
| VSSRHB | VSS | VSS | NC | NC |

Quanta Computer Inc.
PROJECT : BL6
Size: Document Number: Madison/Park PWR_GND Rev: A1A
Date: Saturday, April 10, 2010 Sheet 20 of 45




| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : BL6 | | | |
| Size | Document Number | | Rev |
| | Madison/Park DPPW_GND | | A1A |
| Date: Saturday, April 10, 2010 | | Sheet 21 of 45 | |

## PIN STRAPS




| Memory Aperture size | |
|---|---|
| RAM_CFG[2:0] | Size |
| 000 | 128MB |
| 001 | 256MB |
| 010 | 64MB |
| 011 | 32MB |

| ROM Table | | |
|---|---|---|
| EXT_HSYNC | EXT_VSYNC | Discription |
| 0 | 0 | No Audio |
| 0 | 1 | Any one by dectec |
| 1 | 0 | DP only |
| 1 | 1 | Both DP & HDMI |

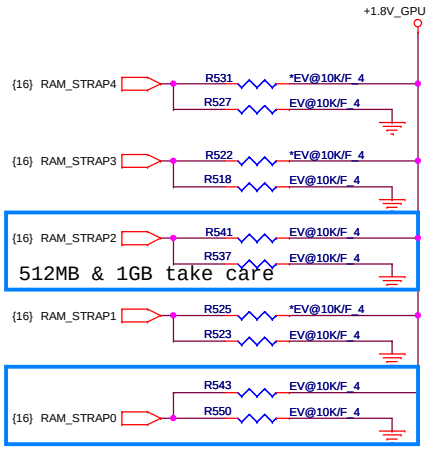
## CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

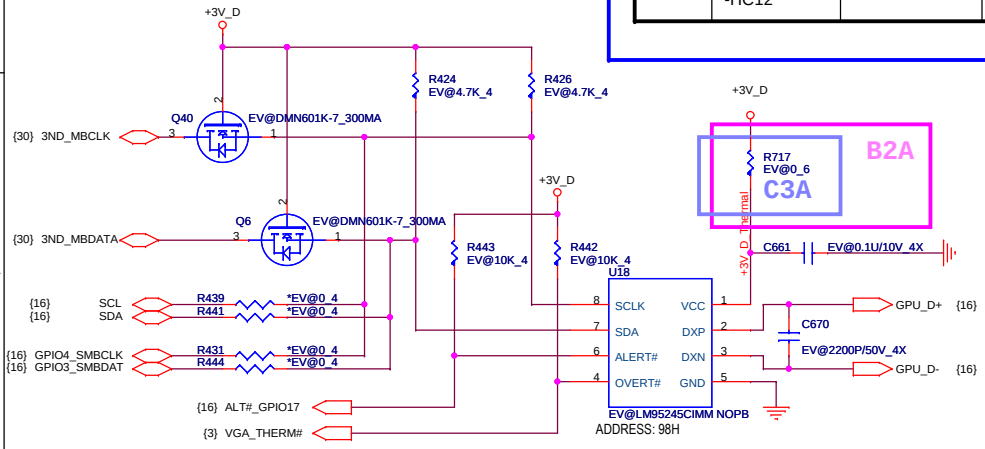
| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | DEFAULT | REMARK |
|---|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | 0 = 50% TX OUTPUT SWING<br>1 = FULL TX OUTPUT SWING | 0 | |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS ENABLED<br>0 = TX DE-EMPHASIS DISABLED<br>1 = TX DE-EMPHASIS ENABLED | 0 | |
| BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM (Only for GDDR5)<br>0 = DISABLE<br>1 = ENABLE | 0 | |
| ROMIDCFG(2:0) | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT<br>NUMONYX M25P10A : 101 | 000 | See ROM table |
| BIF_GEN2_EN_A | GPIO2 | 0 = PCIE DEVICE AS 2.5GT/S CAPABLE<br>1 = PCIE DEVICE AS 5GT/S CAPABLE | 0 | |
| GPIO_8_ROMSO<br>H2SYNC<br>GPIO_21_BB_EN | GPIO8<br>H2SYNC<br>GPIO21 | Reserved Only | 0 | |
| AUD[1]<br>AUD[0] | HSYNC<br>VSYNC | AUD[1:0]<br>00: NO AUDIO FUNCTION.<br>01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED.<br>10: AUDIO FOR DISPLAYPORT ONLY.<br>11: AUDIO FOR BOTH DISPLAYPORT AND HDMI. | 11 | See Audio table |
| GPIO_9_ROMSI | GPIO9 | 0 = VGA controller capacity enable | 0 | |
| VIP_DEVICE_STRAP_ENA<br>VIP: Video Capture Port Interface | V2SYNC | 0 = DRIVER would ignore the value sample on VHAD_0 during RESET. | 0 | |

## DDR3 Memory TYPE

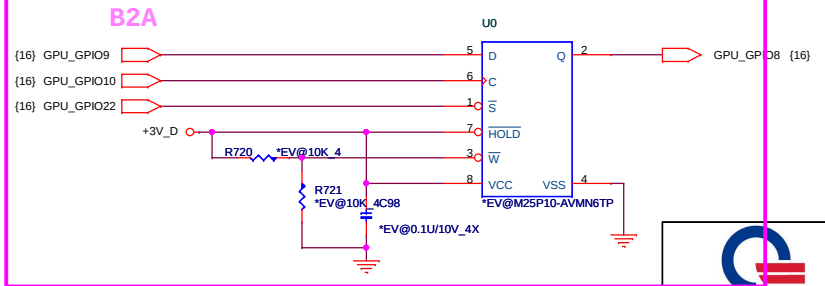
| Vendor | Vendor P/N | STN B/S P/N | Size | RAM_STRAP3 DVPDATA_3 | RAM_STRAP2 DVPDATA_2 | RAM_STRAP1 DVPDATA_1 | RAM_STRAP0 DVPDATA_0 | RAM_STRAP4 15" | RAM_STRAP4 14" |
|---|---|---|---|---|---|---|---|---|---|
| Hynix | H5TQ1G63BFR -12C | AKD5LZGTW00 (64M*16) | 512MB | 0 | 1 | 0 | 0 | 0 | 1 |
| | | | 1GB | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | 2GB | 0 | 0 | 1 | 0 | 0 | 1 |
| Samsung | K4W1G1646E -HC12 | AKD5LGGT502 (64M*16) | 512MB | 0 | 1 | 0 | 1 | 0 | 1 |
| | | | 1GB | 0 | 0 | 0 | 1 | 0 | 1 |
| | K4W2G1646B -HC12 | AKD5MGGT501 | 2GB | 0 | 0 | 1 | 1 | 0 | 1 |




## Thermal Sensor




## EEPROM

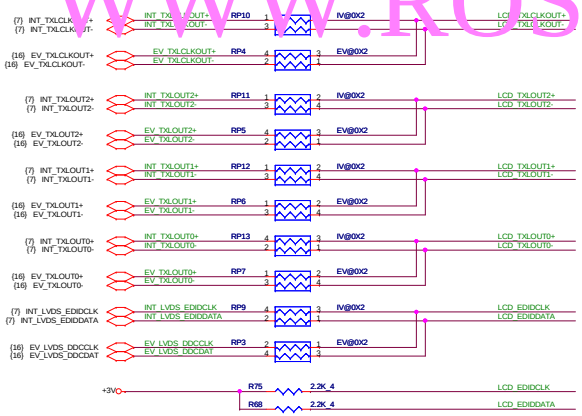



Quanta Computer Inc.

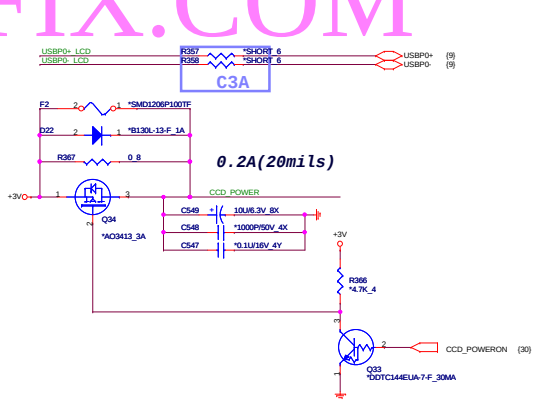
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | Memory strip/Thermal/HDCP | A1A |
| Date: Saturday, April 10, 2010 | Sheet 22 of 45 | |

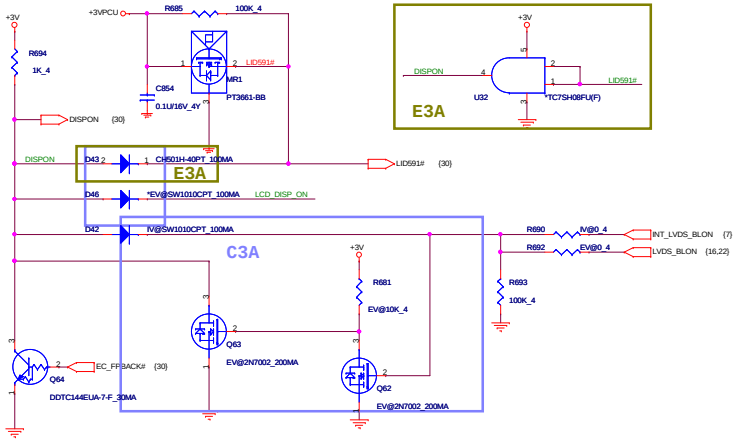
## LVDS Signals



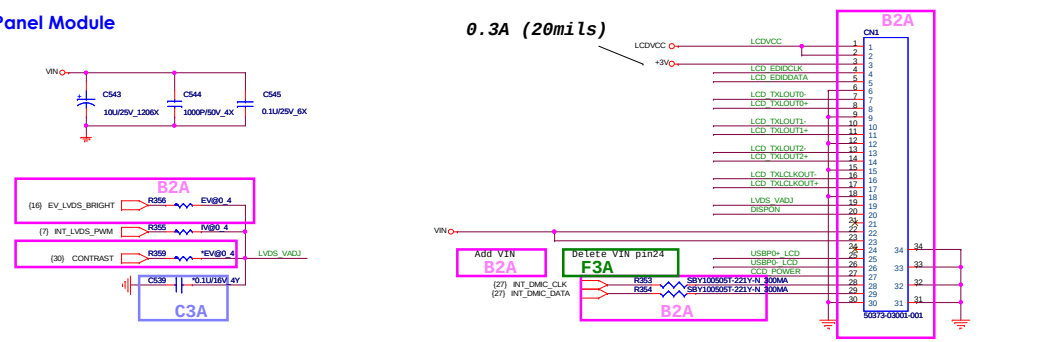

## CCD



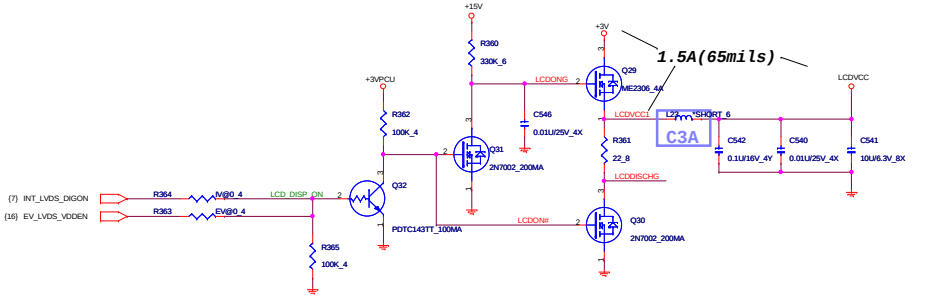

## HALL SENSOR&BACK LIGHT SWITCH



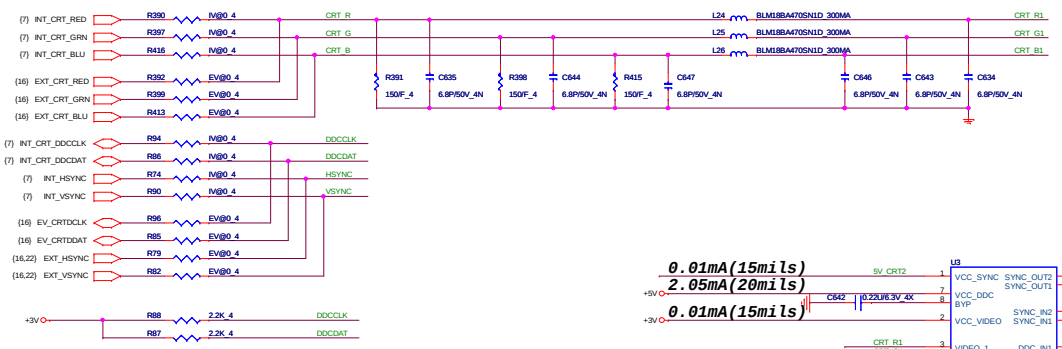

## LCD Panel Module

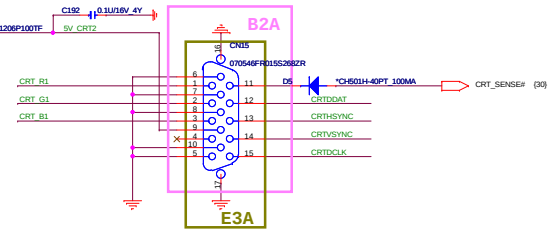


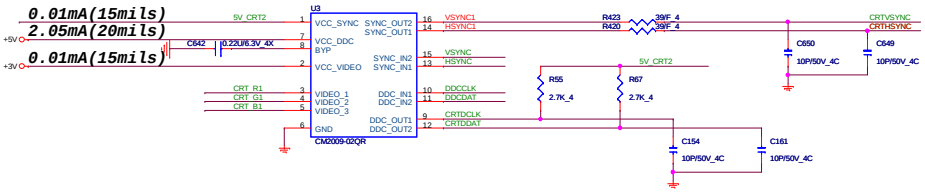

## LCD POWER SWITCH




## CRT




Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | LCD/LED Panel/CCD | XLA |
| Date: Saturday, April 10, 2010 | Sheet 23 of 45 | |

## MINI Card Slot#1 (WiFi)

Before RAMP must to remove debug card component

2.75A(120mils)

0.33A(30mils)

CN18 — 80003-5121

Intel module use S5 power for +3.3V
Other module keep +3V for +3.3V

## MINI Card Slot#2 3G

2.75A(120mils)

0.5A(30mils)

CN21 — *3G@80003-5121

## SIM CARD board to board

CN11 — *3G@88020-12101

## 3G CONN

Close to 3G MINI Card

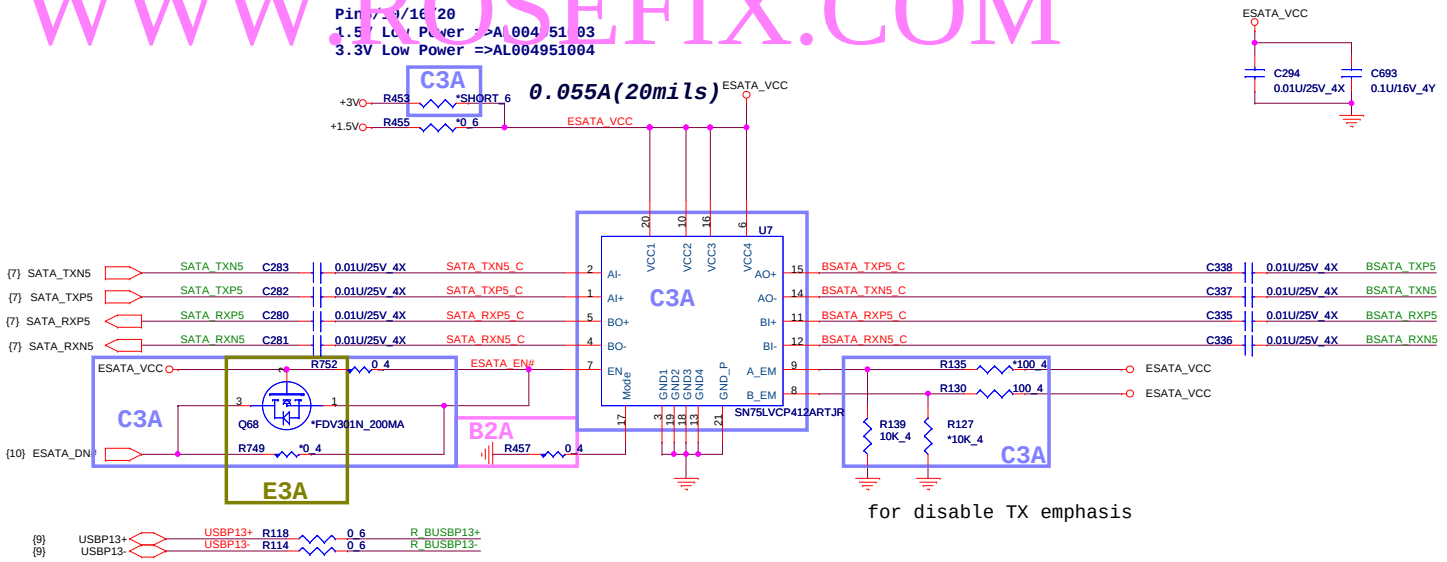
CN5 — *3G@88511-120N

CN8 — *3G@88511-120N

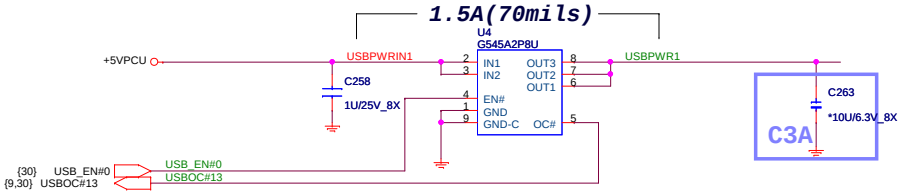
| | |
|---|---|
| Quanta Computer Inc. | PROJECT : BL6 |
| Size | Document Number: MINI CARD(WLAN/3G/SIM Card) |
| Rev | A1A |
| Date: Saturday, April 10, 2010 | Sheet 24 of 45 |

## ESATA Re-driver IC

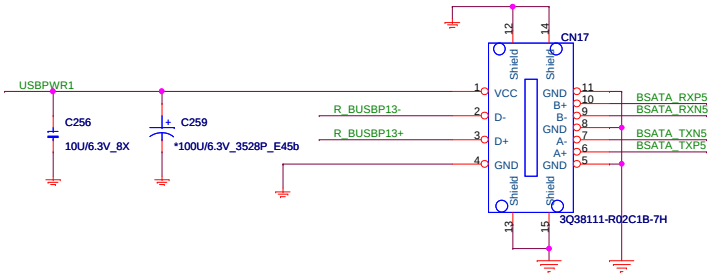
Pin 7/9/16/20
1.5V Low Power =>AL004951003
3.3V Low Power =>AL004951004



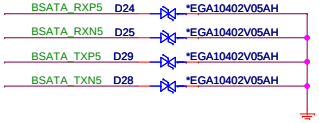

for disable TX emphasis




## ESATA CONN

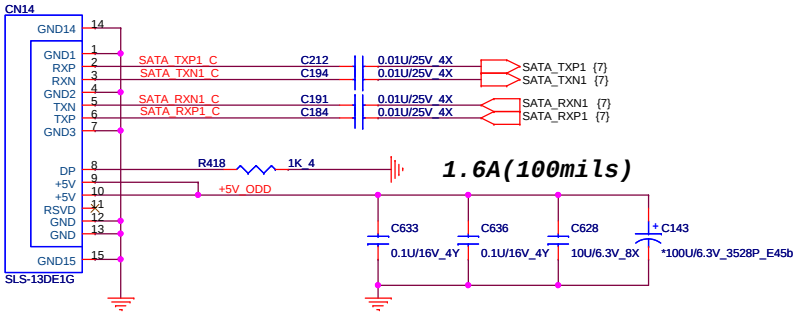


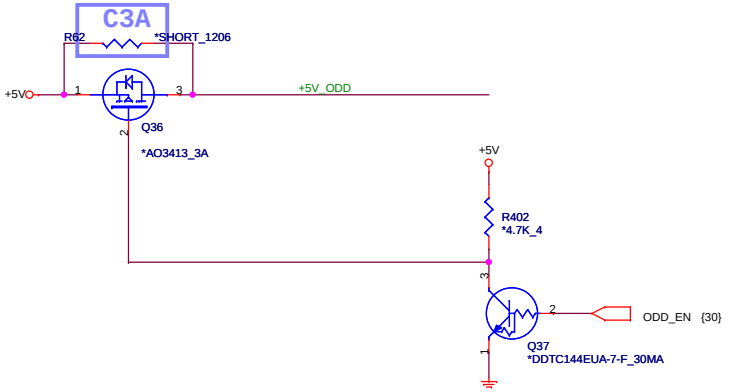




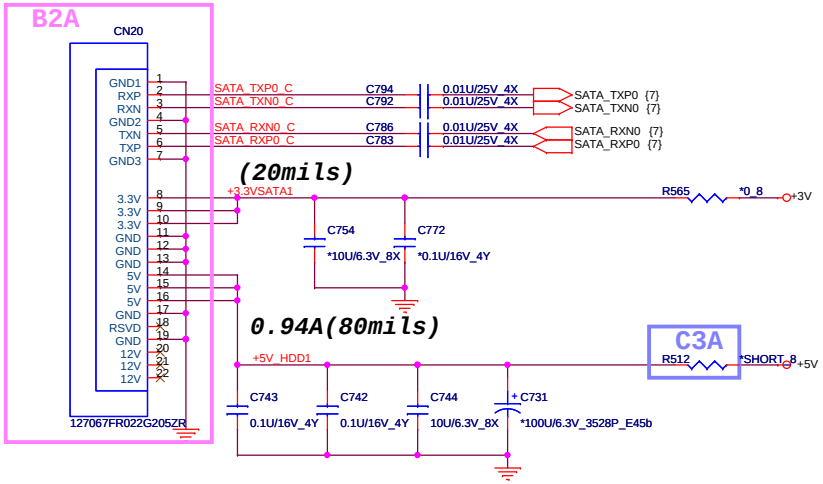

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BL6 | | |
| Size | Document Number: TP/SW/ESATA/USB+Audio/LED | Rev: A1A |
| Date: Saturday, April 10, 2010 | Sheet 25 of 45 | |

## SATA ODD

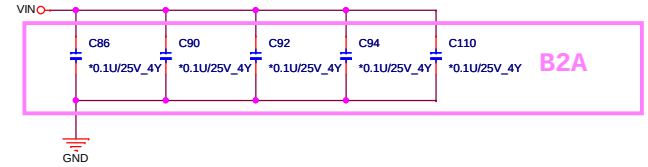


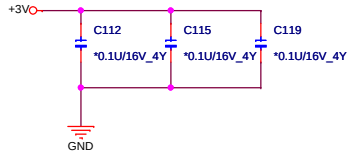




## SATA HDD




## EMI



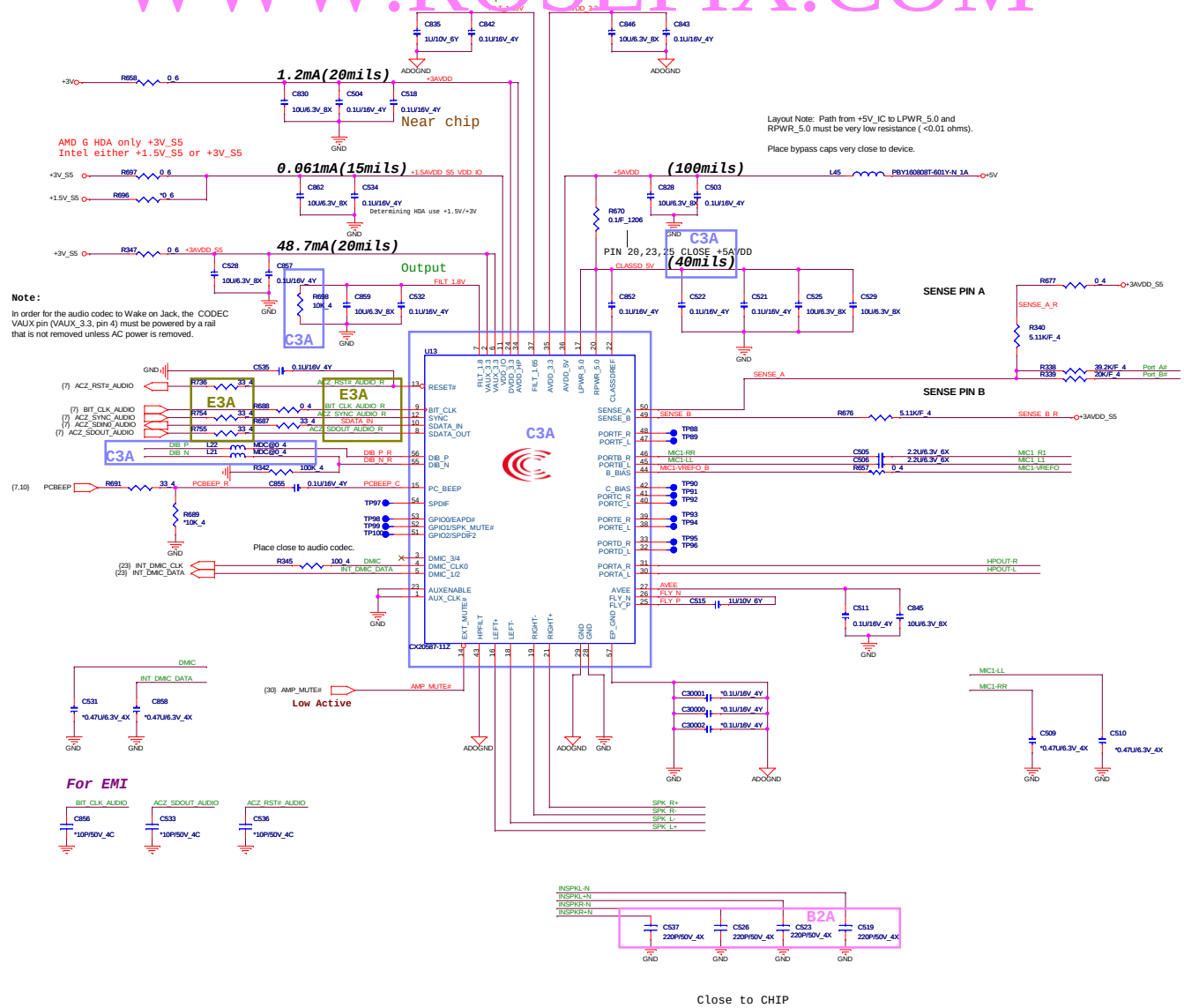

Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | HDD/ODD/EMI | A1A |

Date: Saturday, April 10, 2010 Sheet 26 of 45

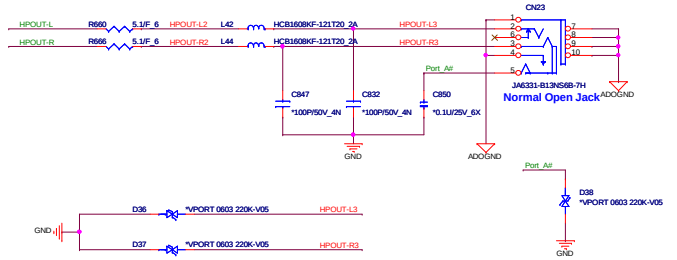
# Codec (CX20583)



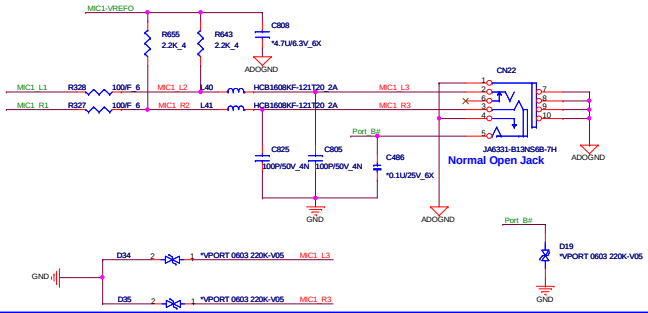



## AUDIO JACKS

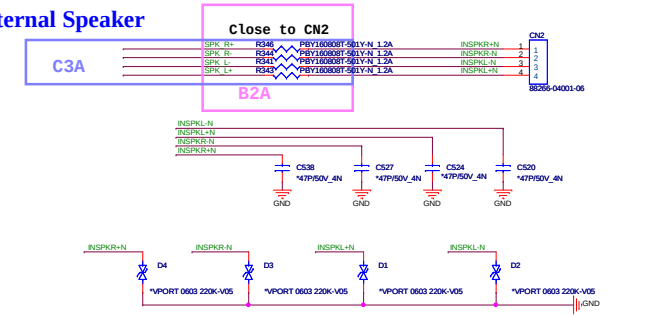
### Earphone



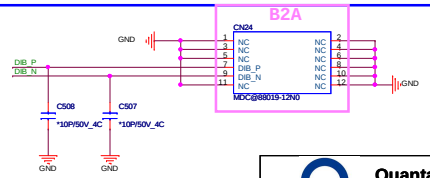

### External MIC




### Internal Speaker




### MDC




Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | Audio Codec (CX20583) | A1A |
| Date: Saturday, April 10, 2010 | Sheet 27 of 45 | |

# Atheros Lan



0.163A(20mils)

AMD mount Q66, NO mount R727
INTEL mount R727, No mount Q66

Atheros
AR8151/AR8152

PLACE NEAR LAN IC SIDE

TRANSFORMER

R27,R28
GIGA = 75 ohm
10/100 = 0 ohm

Close to LED

Power on Strapping pin

| | | |
|---|---|---|
| LED0 = LAN_ACTLED | 1 | Over-clocking enable (default = 1) |
| | 0 | Over-clocking disable |
| LED1 = LAN_LINKLED# | 1 | SWR switch-mode regulator select<br>Giga LAN pull High (default = 1) |
| | 0 | LDO linear regulator select<br>10/100M LAN pull Low |
| CKREQ# or CKREQ_G# | 1 | Normal function |
| | 0 | ATE test mode |

GIGA/A1:0A0R:81R51-5A2L-1AAL-1RA-=RA=L0A0L8010505810100210004

Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | Atheros Lan | A1A |

Date: Saturday, April 10, 2010 Sheet 28 of 45

# 5 IN 1 CARD READER

+3V_Card 0.043A(20mils)

C839 10U/6.3V_8X
C860 *0.1U/16V_4Y
C838 0.1U/16V_4Y
C861 0.1U/16V_4Y
C836 0.1U/16V_4Y

+3V → R662 *SHORT_8 → +3V_Card

C3A

+3V_Card → R686 *100K_4

{3,9,24,28,30} PLTRST#

C853 1U/10V_6Y

Y7 Close to U31 Please close

C848 *18P/50V_4C — XTLO — R668 *0_4
Y7 *12MHZ_30
R665 *270K_4
C840 *18P/50V_4C — XTLI — R664 *0_4

{8} 48M_CARD → R663 *SHORT_4

C3A

(10mils)

+1.8V_VDD
C834 1U/10V_6Y
C837 0.1U/16V_4Y
C833 0.1U/16V_4Y

## U31 RTS5159-VDD-GR

| | | | |
|---|---|---|---|
| 1 | AV_PLL | | |
| 2 | RREF | R661 6.2K/F_4 | CARDREF |
| 3 | NC | | |
| 4 | DM | {9} | USBP3- |
| 5 | DP | {9} | USBP3+ |
| 6 | AGND | | |
| 7 | NC | | |
| 8 | 3V3_IN | +3V_Card | |
| 9 | CARD_3V3 | VCC_XD | |
| 10 | VREG | +1.8V_VDD | |
| 11 | D3V3 | +3V_Card | |
| 12 | DGND | | |
| 13 | XTAL_CTR | | |
| 14 | GPIO0 | | |
| 15 | EEDO | | |
| 16 | EECS | | |
| 17 | EESK | | |
| 18 | EEDI | | |
| 19 | XD_CD# | | |
| 20 | SD_WP | | |
| 21 | SD_CD# | | |
| 22 | MS_D4 | | |
| 23 | XD_D4 | | |
| 24 | MS_D5 | | |
| 25 | XD_D5/MS_BS | | |
| 26 | XD_D3/MS_D1 | | |
| 27 | SD_DAT0/XD_D6/MS_D0 | | |
| 28 | XD_D2/MS_D2 | | |
| 29 | MS_INS# | | |
| 30 | NC | | |
| 31 | XD_D7/MS_D3 | | |
| 32 | DGND | | |
| 33 | D3V3 | +3V_Card | |
| 34 | XD_D1 | R325 *SHORT_4 | SD_MS_CLK |
| 35 | SD_DAT5/XD_D0/MS_D6 | | |
| 36 | SD_CMD | | |
| 37 | SD_DAT4/XD_WP#/MS_D7 | | |
| 38 | XD_RDY | | |
| 39 | SD_DAT3/XD_WE# | | |
| 40 | SD_DAT2/XD_RE# | | |
| 41 | XD_ALE | | |
| 42 | XD_CE# | | |
| 43 | XD_CLE | | |
| 44 | RST# | | |
| 45 | MODE_SEL | | |
| 46 | AG_PLL | | |
| 47 | XTLO | | |
| 48 | XTLI | | |

C3A

R678 *0_4 — MODE_SEL — C851 *680P/50V_4X

B2A

MODE_SEL (Please refer to Realtek Application Notes for more detail description)

| | R678 | C851 | Power mode |
|---|---|---|---|
| RTS 5159 | 0-ohm | NC | USB Auto De-link mode: |

B2A
{32} TP_XD_LED# → RTSS159_LED# → R669 *10K_4 → +3V_Card
C849 0.1U/16V_4Y

+3V_Card → R667 10K_4 → XTAL_CTR

TP83 RTS5159_LED#
TP84 EEDO
TP85 EECS
TP86 EESK
EEDI
SD_WP
SD_CD#
XD_D4/SD_D1

| XTAL_CTR | CLK source |
|---|---|
| Pull-high | 48MHz from CLK gen. |
| Floating | 12MHz from Crystal |

# 3 IN 1 CARD READER

VCC_XD 30mils
C517 0.1U/16V_4Y
C512 0.1U/16V_4Y
C516 0.1U/16V_4Y

VCC_XD

| | | | | |
|---|---|---|---|---|
| SD_DAT0/XD_D6/MS_D0 | R252 | 33_4 | SD_DAT0/XD_D6/MS_D0_R | CN26 11 SD-VCC |
| XD_D4/SD_D1 | R251 | 33_4 | XD_D4/SD_D1_R | 18 SD-DAT0 |
| SD_DAT2/XD_RE# | R256 | 33_4 | SD_DAT2/XD_RE#_R | 19 SD-DAT1 |
| SD_DAT3/XD_WE# | R255 | 33_4 | SD_DAT3/XD_WE#_R | 1 SD-DAT2 |
| SD_MS_CLK | R253 | 33_4 | SD_MS_CLK_R | 3 SD-DAT3 |
| SD_CMD | R254 | 33_4 | SD_CMD_R | 14 SD-CLK |
| SD_CD# | R250 | 33_4 | SD_CD#_R | 6 SD-CMD |
| SD_WP | R249 | 33_4 | SD_WP_R | 21 SD-C/D |
| | | | | 20 SD-WP |
| | | | | 22 GND |
| | | | | 4 MS-VCC |
| SD_DAT0/XD_D6/MS_D0 | | | | 12 MS-DATA0 |
| XD_D3/MS_D1 | | | | 13 MS-DATA1 |
| XD_D2/MS_D2 | | | | 10 MS-DATA2 |
| XD_D7/MS_D3 | | | | 7 MS-DATA3 |
| SD_MS_CLK | R230 | 33_4 | SD_MS_CLK_RMS | 5 MS-SCLK |
| MS_INS# | | | | 8 MS-INS |
| XD_D5/MS_BS | | | | 15 MS-BS |
| | | | | 2 MS-GND |
| | | | | 9 SD-GND |

MS-GND 16
SD-GND 17
GND 23

CM3R-065

SD_MS_CLK_R → C463 *10P/50V_4C

B2A

Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | RTS5159 (Card Reader) | A1A |

Date: Thursday, April 08, 2010 Sheet 29 of 45

# EC

0.03A(30mils) 0.03A(30mils) 0.01A(20mils)

U8 WPCE775LA0DG H=1.6mm

LPC: LFRAME, LAD0, LAD1, LAD2, LAD3, PCLK_591, CLKRUN#, GATEA20, RCIN#, SCI#, EC_FPBACK#, PLTRST#, USB_EN#0, SERIRQ, BAT_SAT1

KB: KBSIN0–KBSIN7, KBSOUT0–KBSOUT17

SMB: MBCLK, MBDATA, 2ND_MBCLK, 2ND_MBDATA, 3RD_MBCLK, 3RD_MBDATA, 3G_EN

PS/2: TPCLK, TPDATA, USB_EN#1, LAN_P, CRT_SENSE#

A/D: AD0/GPI90, AD1/GPI91, AD2/GPI92, AD3/GPI93, AD4/GPIO05, AD5/GPIO04, AD6/GPIO03, AD7/GPIO07

D/A: DA0/GPI94, DA1/GPI95, DA2/GPI96, DA3/GPI97

GPIO: GPIO41(VBAT), GPIO42/TCK, GPIO43/TMS, GPIO44/TDI, GPIO50/TDO, CIRTX2/GPIO52/RDY

wake-up capability

no wake-up capability: GPO82/TRIS, GPO84/BADDR0

SER: SOUT_CR/GPO83/BADDR1, SIN_CR/CIRRX/GPIO87, GPIO06

PWM: A_PWM/GPIO15, B_PWM/GPIO21, C_PWM/GPIO13, D_PWM/GPIO32, E_PWM/GPIO45, F_PWM/GPIO40/CLKIN48, G_PWM/GPIO66, H_PWM/GPIO33

TIMER: TA1/GPIO56, TB1/GPIO14, TA2/GPIO20, TB2/GPIO01, TA3/GPIO51, TB3/GPIO36

SPI: SPI_DI/GPIO77, SPI_DO/GPO76/SHBM, SPI_SCK/GPIO75, GPIO81

FIR: IRRX1/GPIO72/SIN2, IRRX2_IRSL0/GPIO70, IRTX/GPIO71/SOUT2, CIRRXM/GPIO46/TRST

CIR: GPIO34/CIRRXL, CIRTX1/GPIO16, CIRTX2/GPIO30

FIU: F_SDI/F_SDIO1, F_SDO/SDIO0, F_CS0, F_SCK

CLKOUT/GPIO55, VCC_POR, VREF

32KX1/32KCLKIN, 32KX2

Y2 32.768KHZ_10 C326 18P/50V_4C C344 18P/50V_4C R150 20M_6 R152 33K/F_4 R703 *SHORT_4 R702 *SHORT_4 R704 *0_4 C3A

L37 0_6 C269 1U/10V_6X VCORF_uR

8769AGND

3 cell protect for VGA SKU

B2A: R718 IV@10K_4, R719 EV@10K_4, Cell_separate

for 14"/15" option: R751 10K_4, R753 *10K_4, C3A

D7 SW1010CPT_100MA SCI#_uR ECGPIO10 E3A

BAT_SAT1

R513 *100K/F_4 +3VPCU

TEMP_MBAT {34}

ICMNT {34}, AC_SET_EC {34}, USBOC#8_9 {9,31}, GPU_VRON {20,41}, GPU_MAINON {41}, NBSWON# {31}, SUSB# {9}

TP6 C3A VFAN1 {3}, SUSLED_EC {32}

BAT_SAT0 {32}

RF_LED {32}, AMP_MUTE# {27}, ID {34}, D/C# {34}, DISPON {23}

WMAX_P {24} For Intel

BADDR0, BADDR1

TP_ON_OFF {31}, LID591# {23}

CONTRAST {23}

CCD_POWERON {23}, USBOC#13 {9,25}, SUSON {36}, MAINON {3,11,37,38,40}, BT_POWERON {31}, PWRLED# {32}

Q19 2N7002_200MA R196 *0_4

3G_P {24}, FANSIG1 {3}

ACIN {32,34}, S5_ON {36,40}, VRON {39}

BT_RESET {31}, RF_EN {24}, ODD_EN {26}, DNBSWON# {9,33}

D14 SW1010CPT_100MA E3A R726 *10K_4 C3A R753 0_4 PCH_GPIO33 {7,10}

RSMRST# {9}, SUSC# {9}, MPWROK {3,9}

NUMLED {31}, CAPSLED {31}

BT_RFCTRL {24} B2A E3A For Intel

SPI_SDI_uR R167 100K_4

SPI_SDO_uR, SPI_SCK_uR, SPI_CS0_uR

TP4 SUS_PWR_ACK {9}

VCC_POR# R158 4.7K_4 +3VPCU

VREF_uR R190 0_4 +A3VPCU

For Intel: S3_Reduce 2.5V_EN {3}

For AMD: CRT_SENSE# {23}

SUSCLK {9}

8768_32KX1, 8768_32KX2, 8768_32KX1_R, 8768_32KX2_R

# SM BUS PU

MBCLK R134 4.7K_4 +3VPCU

MBDATA R129 4.7K_4

2ND_MBCLK R122 4.7K_4

2ND_MBDATA R126 4.7K_4

3ND_MBCLK R199 4.7K_4

3ND_MBDATA R200 4.7K_4

# I/O Base Address

| BADDR1-0 | I/O Address | |
|---|---|---|
| | Index | Data |
| 0 0 | XOR TREE TEST MODE | |
| 0 1 | CORE DEFINED | |
| 1 0 | 2Eh | 2Fh |
| 1 1 | 164Eh | 164Fh |

SHBM=0: Enable shared memory with host BIOS

BADDR0 R197 *10K_4

BADDR1 R519 10K_4

SHBM RF_EN R487 10K_4

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

# ID

U5 M24C08-WMN6TP C3A ADDRESS: A0H

2ND_MBCLK, 2ND_MBDATA

0.003A(20mils)

C270 0.1U/16V_4Y

# SPI FLASH

For Intel: TEMP_ALERT# {3,10}

0.025A(20mils)

U10 W25X40BVSSIG

SPI_SDI_uR R170 33_4 SPI_SDI

SPI_SDO_uR R216 33_4 SPI_SDO

SPI_SCK_uR R217 33_4 SPI_SCK

SPI_CS0# uR

R177 10K_4

C428 0.1U/16V_4Y

| | | |
|---|---|---|
| Intel | 512KB | W25X40BVSSIG |
| AMD | 2MB | W25Q16BVSSIG |

# INTERNAL KEYBOARD STRIP SET

MY0 R111 10K_4 +3VPCU

# HWPG

B2A: {41} VGPU_IO_PG D32 *EV@SW1010CPT_100MA; {20} +1.8V_GPU_PWGD D45 *EV@SW1010CPT_100MA

R198 10K_6 HWPG_VGA

R132 10K_6

Intel {42} HWPG_VAXG D13 IV@SW1010CPT_100MA

Intel {35} SYS_HWPG D9 SW1010CPT_100MA

Intel B2A AMD {38} HWPG_1.05V, {38} HWPG_NB_CORE D10 *4C@SW1010CPT_100MA

Intel {36} HWPG_1.5V D8 SW1010CPT_100MA

Intel {37} HWPG_VTT D11 SW1010CPT_100MA

AMD {37} +1.1V_HWPG

HWPG {3}

# SMBUS Table

| SMBUS | Devices | Address |
|---|---|---|
| 1 | Battery | |
| 2 | PCH SML1 | |
| | AMD SMBus | 98H |
| | EC EEPROM | A0H |
| 3 | VGA Board Thermal Sensor | 98H |
| | | |
| | | |
| | | |

DNBSWON#_uR C388 *0.1U/16V_4Y

NBSWON# SW1 *SHORT_PAD

D15 *EGA10402V05AH

PCLK_591 R185 *22_4 C403 *10P/50V_4C

R464 10K_4 TPCLK, R461 10K_4 TPDATA

Close to U16

AC_SET_EC C740 *10U/6.3V_8X 8769AGND

ICMNT C413 *10U/6.3V_8X 8769AGND

# LED PU/PD

PWRLED# R116 10K_4 R117 *10K_4

BAT_SAT0 R476 10K_4

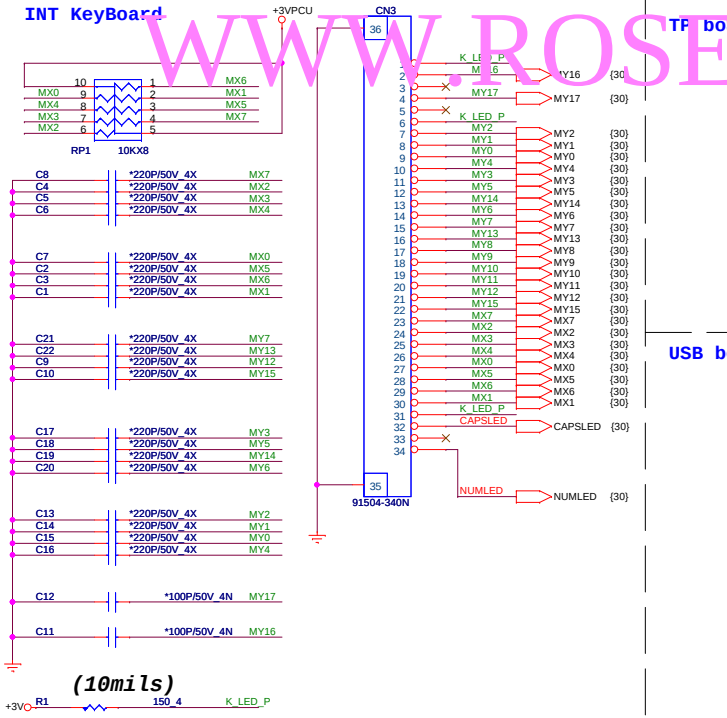
BAT_SAT1 R495 10K_4

Quanta Computer Inc.
PROJECT : BL6

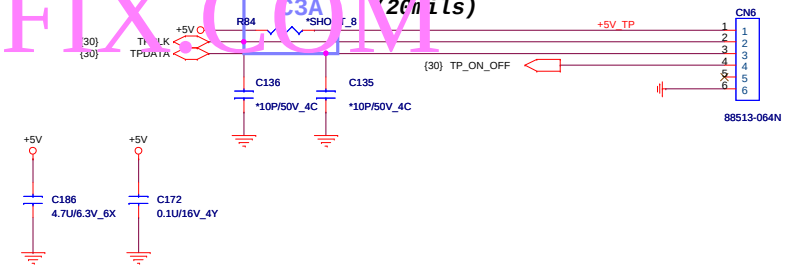
| Size | Document Number | Rev |
|---|---|---|
| | EC-WPC8763LDG/WPC8769L(O) | A1A |

Date: Saturday, April 10, 2010 Sheet 30 of 45

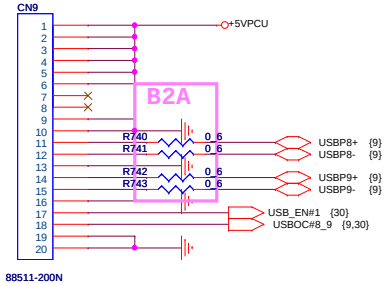
## INT KeyBoard



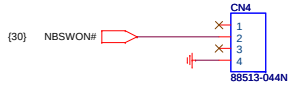

## TP board (20mils)



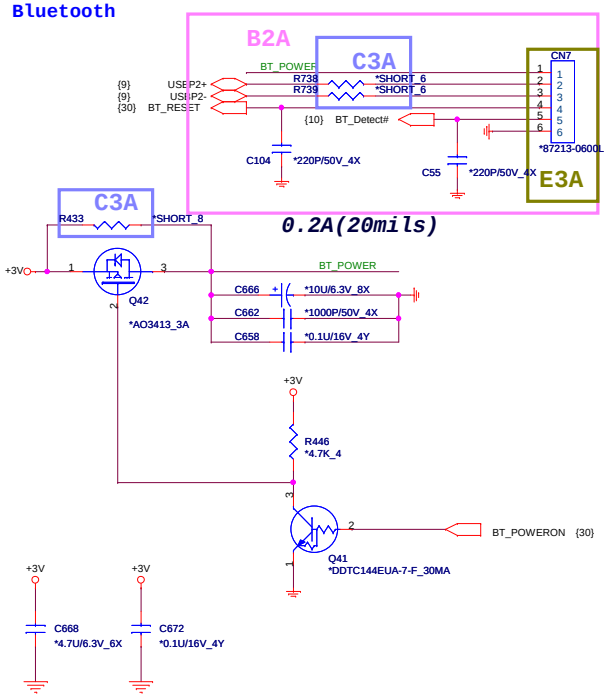

## USB board



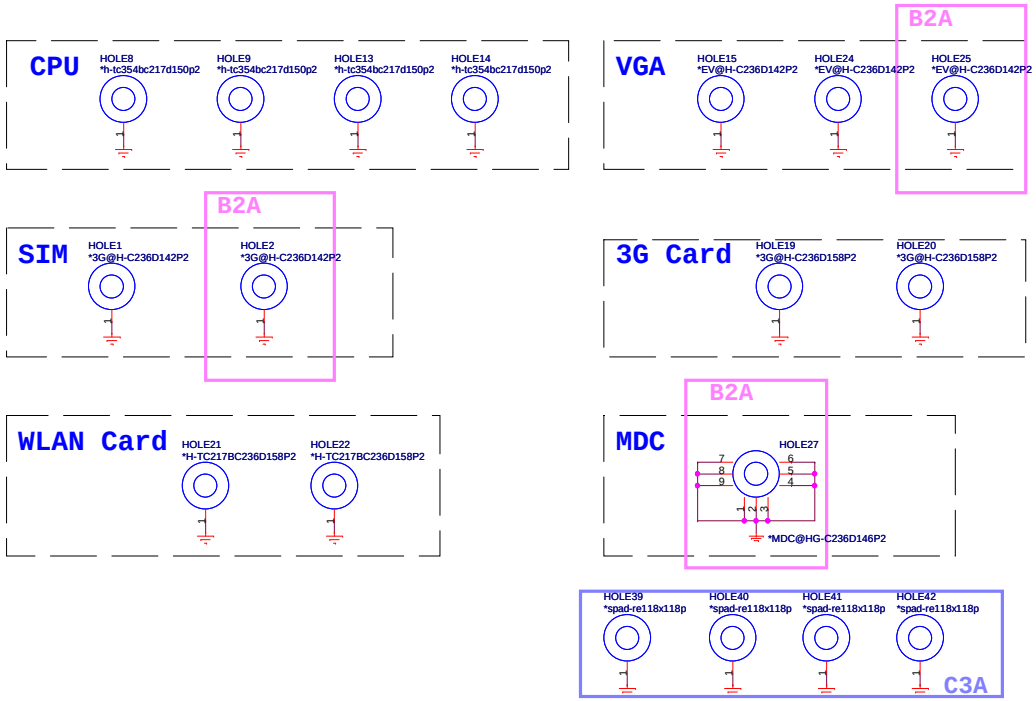

## Power board



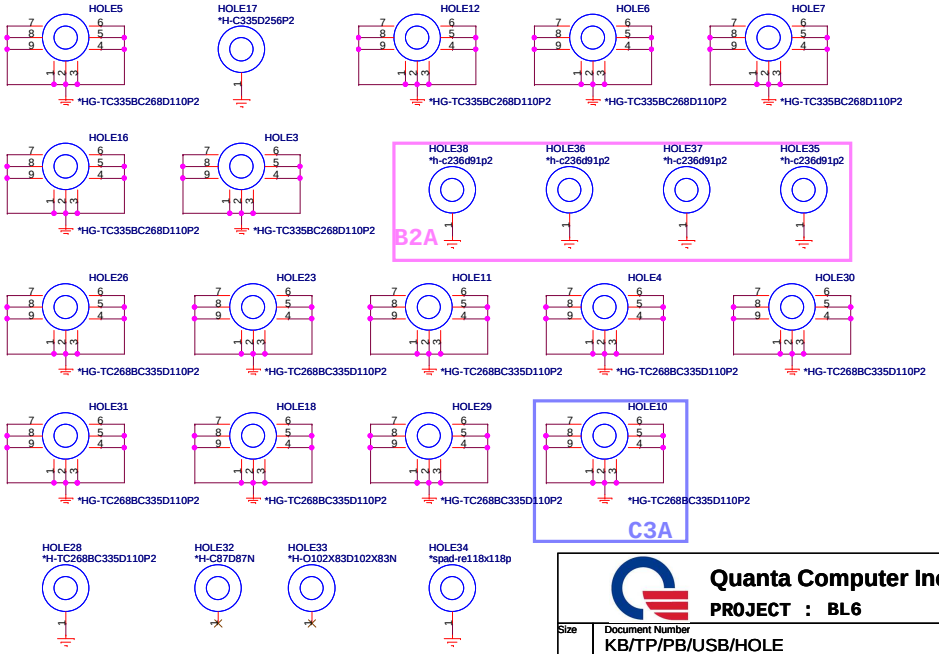

## Bluetooth




## NUT




## HOLE

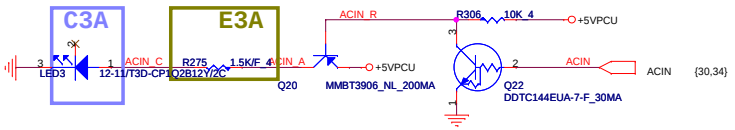



Quanta Computer Inc.
PROJECT : BL6

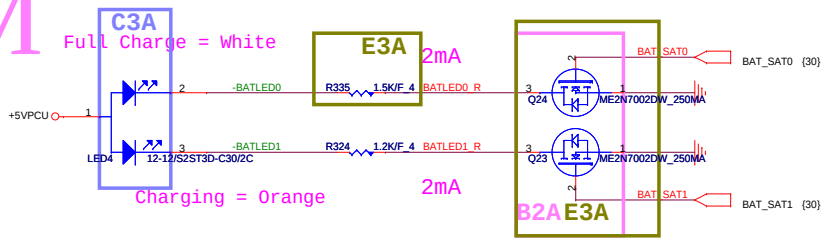
| Size | Document Number | Rev |
|---|---|---|
| | KB/TP/PB/USB/HOLE | A1A |
| Date: Saturday, April 10, 2010 | Sheet 31 of 45 | |

# LED

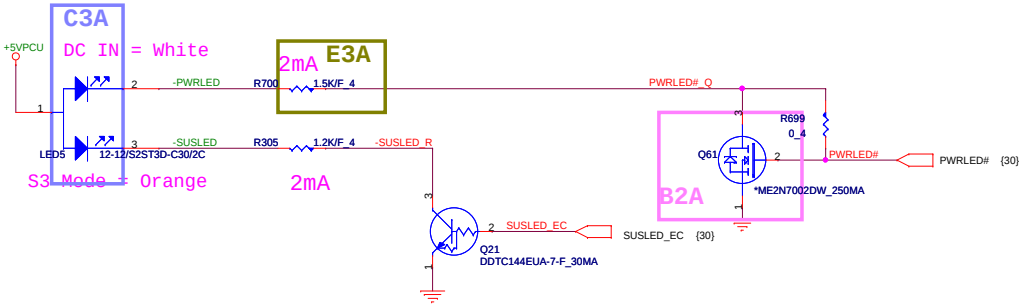
## AC-IN



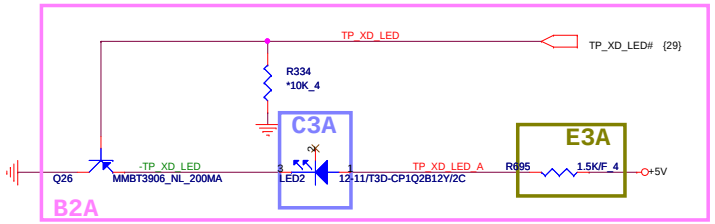

## BATTERY




## POWER

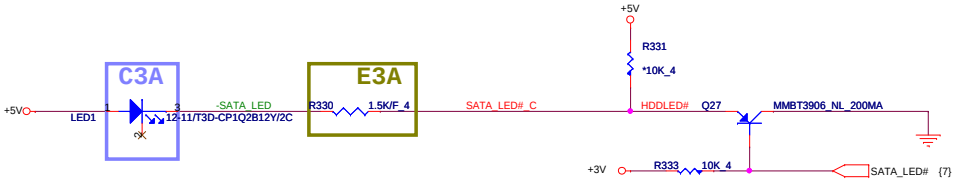



## CARDREADER

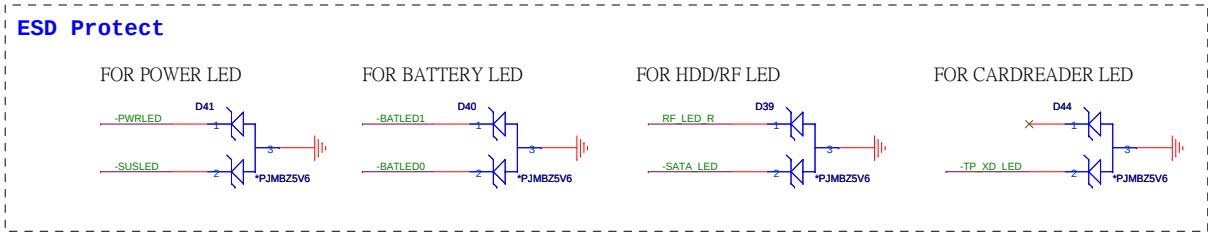



## RF LED


## HDD/ODD

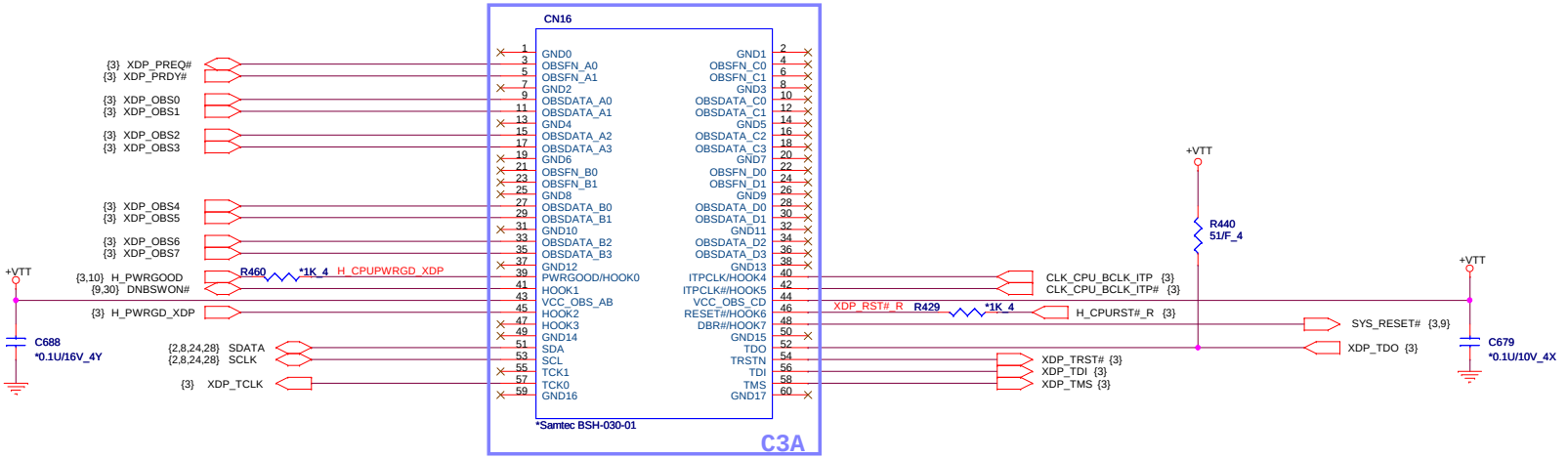



## ESD Protect




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BL6 | | |
| Size | Document Number: LED | Rev: A1A |
| Date: Thursday, April 08, 2010 | Sheet 32 of 45 | |

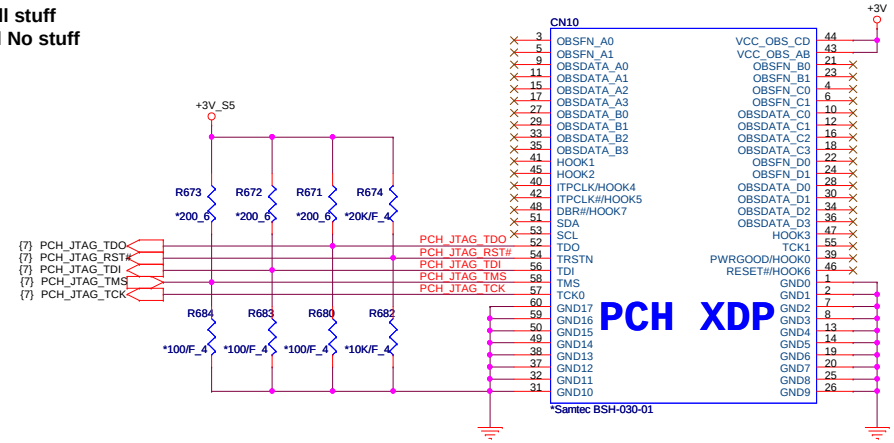
## CPU XDP




| Feature Set | SKU Name (S) | | | | |
|---|---|---|---|---|---|
| | Q57 | H57 | H55 | P55 | P57 |
| BraidWood | Y | Y | N | N | Y |

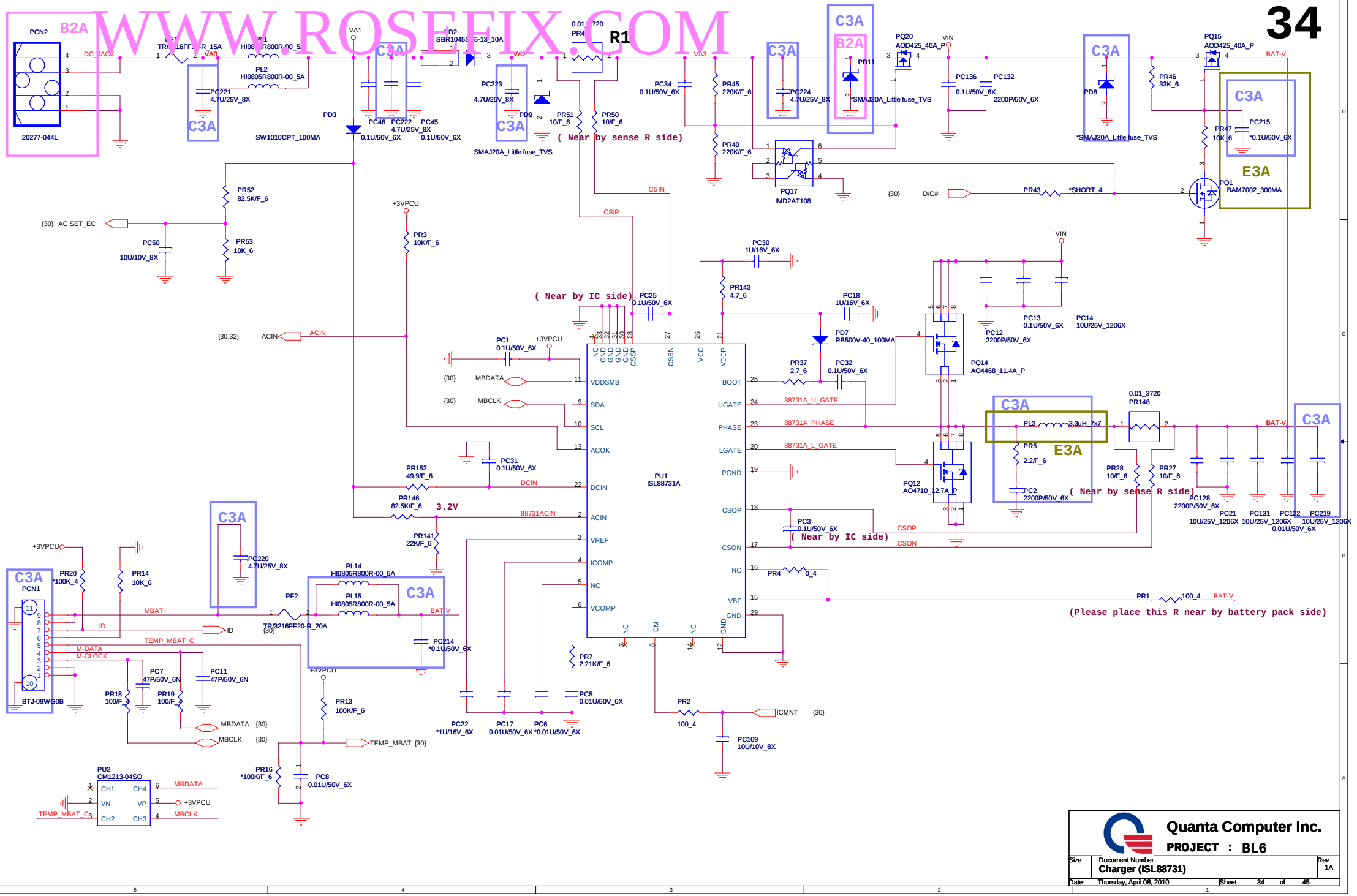
## PCH XDP

**Note: For ES1/ES2 version all stuff**
**Production version all No stuff**




Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | NVRAM Connector | A1A |
| Date: Wednesday, April 07, 2010 | Sheet 33 of 45 | |




| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : BL6 | | | |
| Size | Document Number: Charger (ISL88731) | | Rev: 1A |
| Date: Thursday, April 08, 2010 | | Sheet 34 of 45 | |

For RT8210B 0_4 & 10K_4
For ISL6237 ZD5.6V , 100K/F_4 & 200K/F_4

(Peak 10.2 ,AVG 8.135A)
f : 400k Hz
OCP:11A

f : 500k Hz
(Peak 9A, AVG 7.623A)
OCP:11A

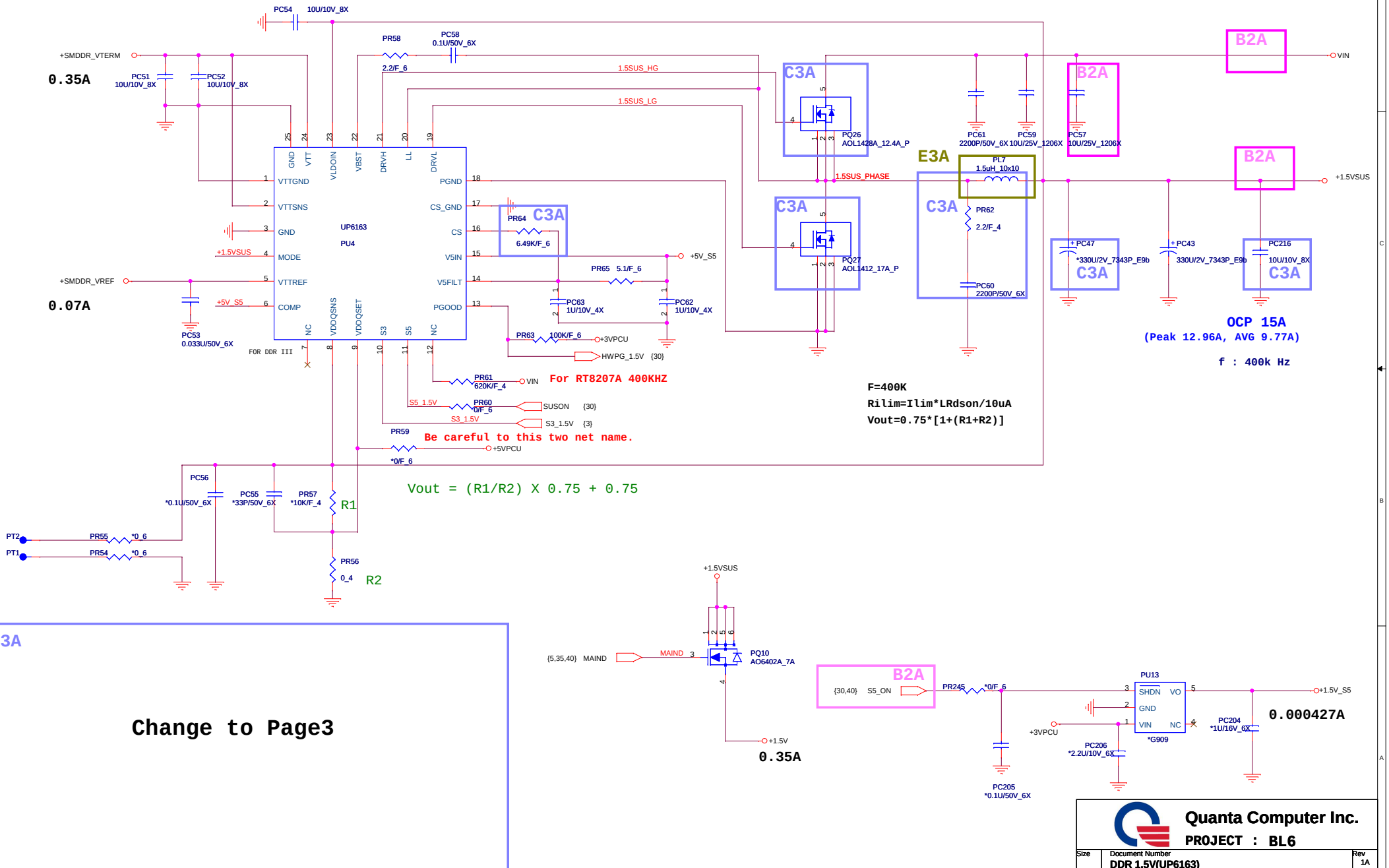
6A
7A

PU5 RT8210B
PQ29 AO4468_11.4A_P
PQ33 AO4468_11.4A_P
PQ30 AO4710_12.7A_P
PQ32 AO4710_12.7A_P
PQ3 AO4496_10A
PQ2 AO6402A_7A
PQ4 AO4496_10A
PQ59 AO6402A_7A
PD5 CHN21UPT_100MA
PD4 CHN21UPT_100MA
PD6 *ZD5.6V

4.253A
1.984A
2.744A~4.984A
0.001A

Quanta Computer Inc.
PROJECT : BL6

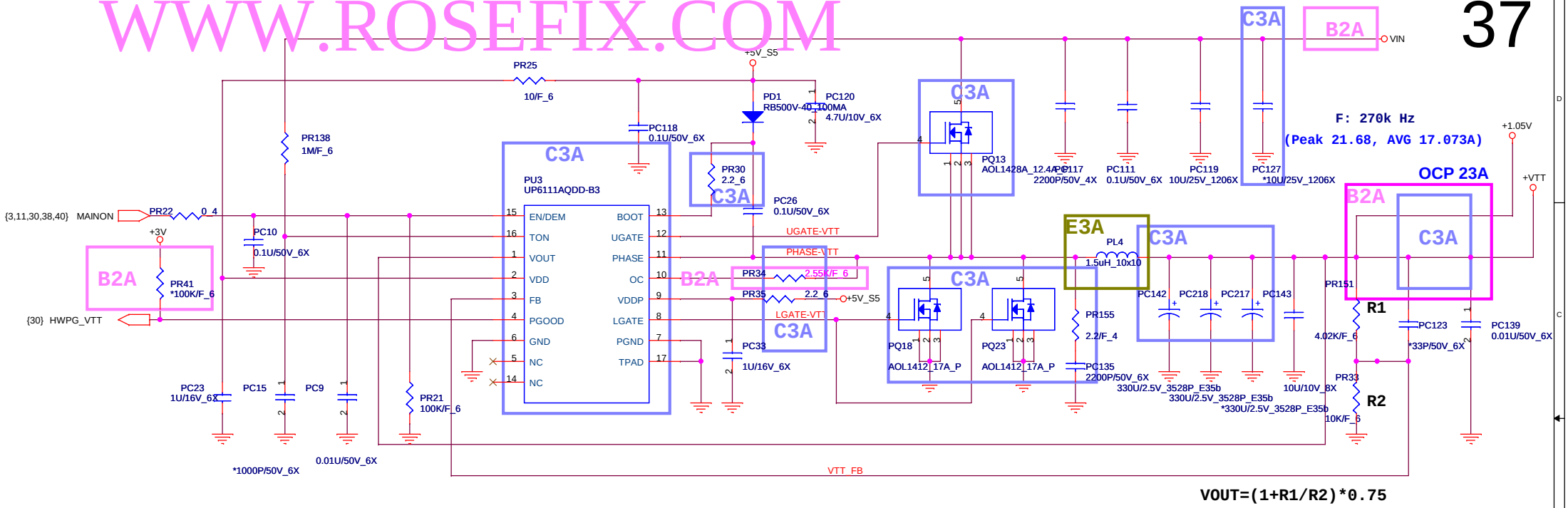
| Size | Document Number | Rev |
|---|---|---|
| | System 5V/3V (ISL6237) | 1A |
| Date: Wednesday, April 07, 2010 | Sheet 35 of 45 | |




Quanta Computer Inc.

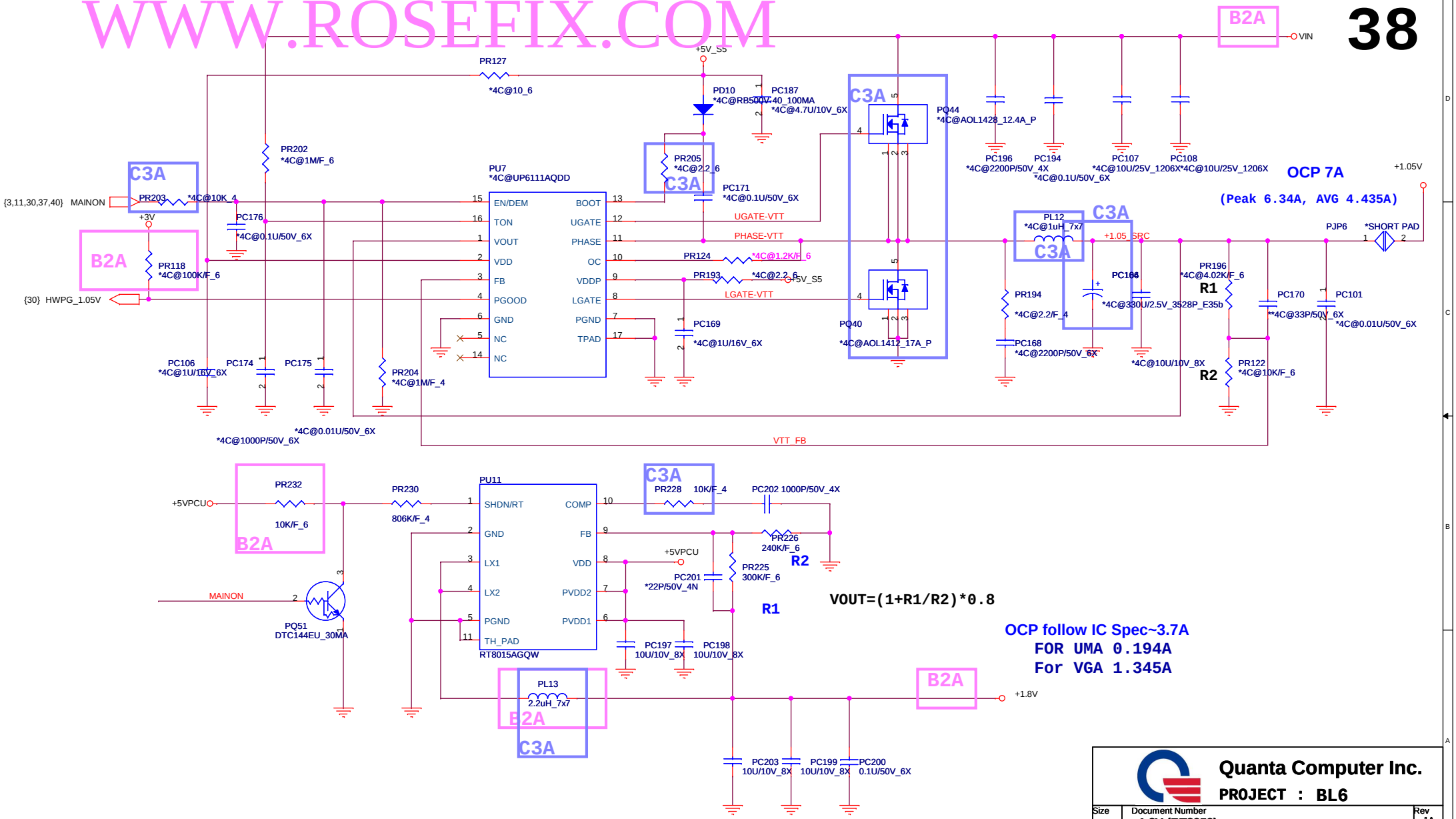
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | DDR 1.5V(UP6163) | 1A |
| Date: Wednesday, April 07, 2010 | Sheet 36 of 45 | |

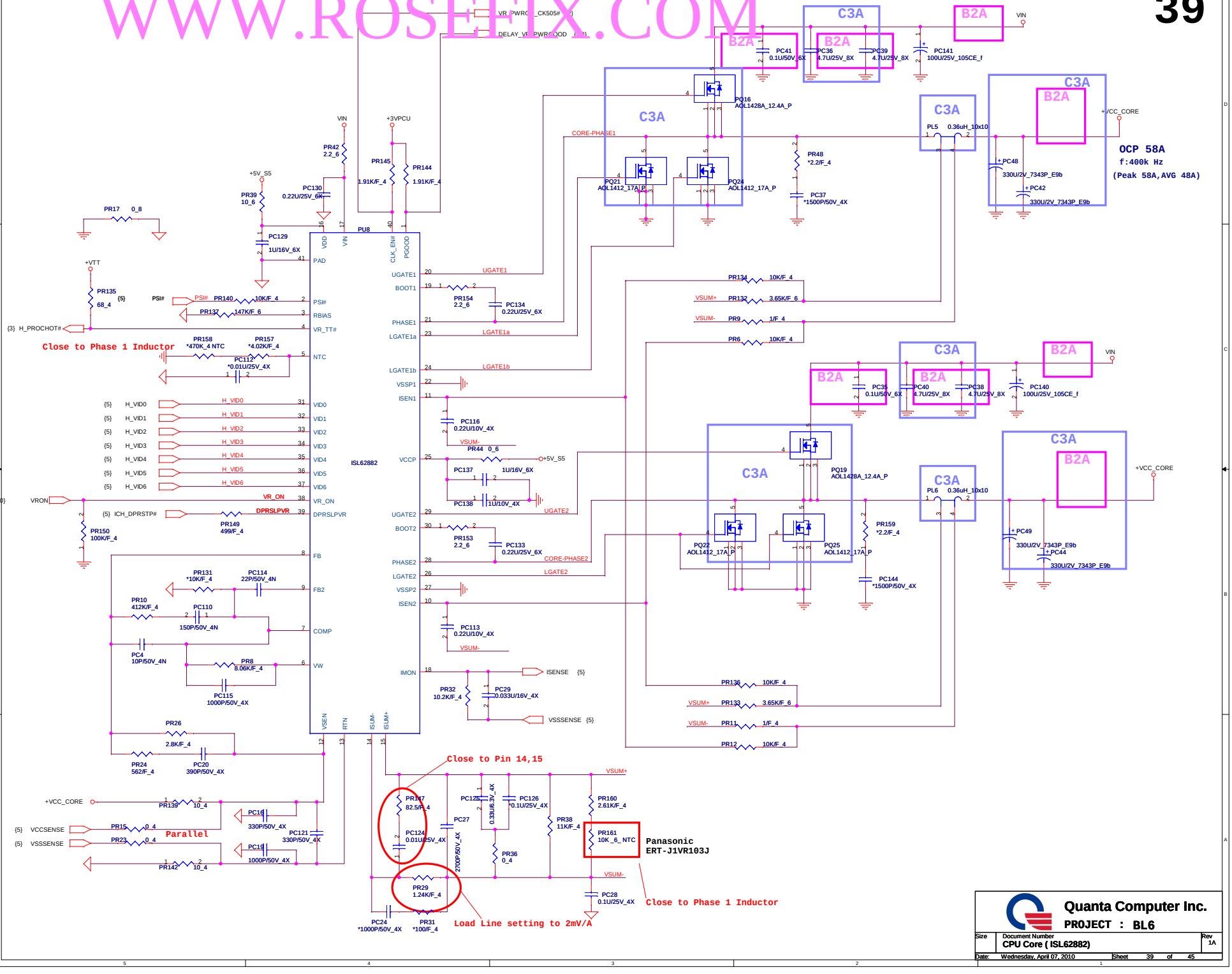



$$VOUT=(1+R1/R2)*0.75$$

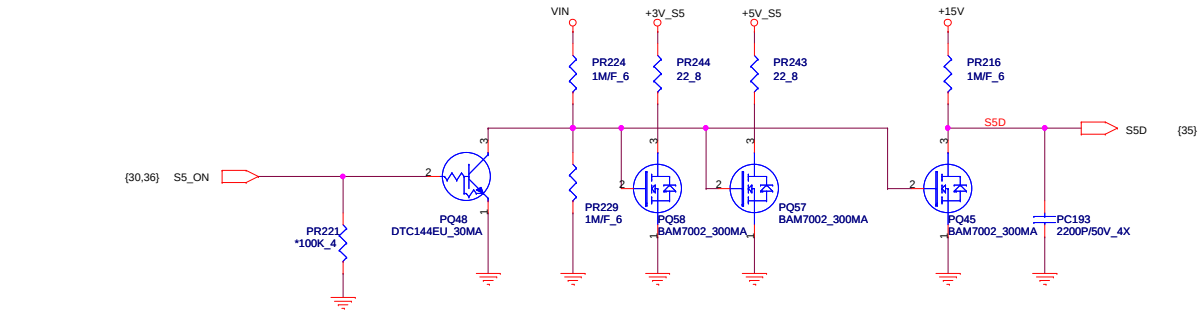
| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BL6 | | |
| Size | Document Number: +VTT (UP6111A) | Rev: 1A |
| Date: Wednesday, April 07, 2010 | Sheet 37 of 45 | |

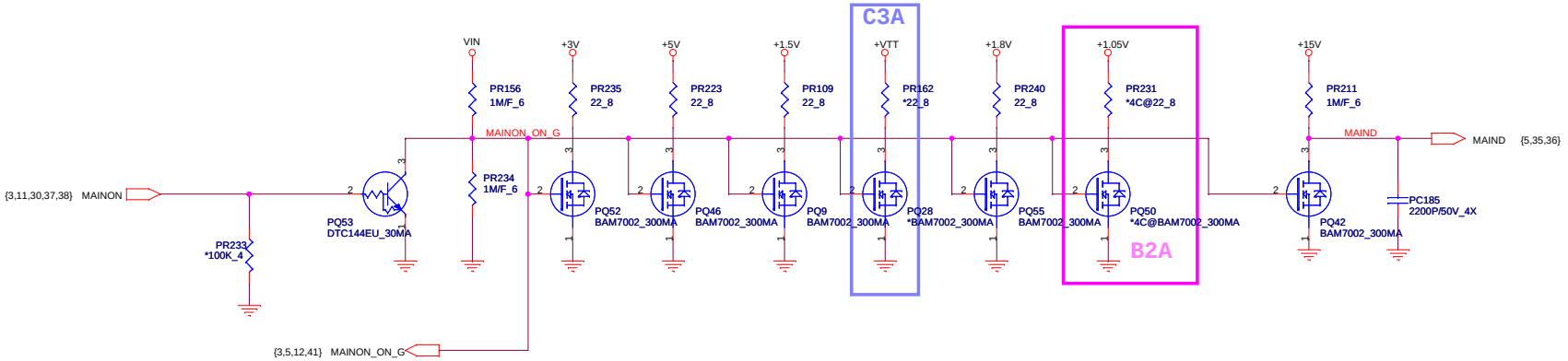



| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BL6 | | |
| Size | Document Number: +1.8V (RT8253) | Rev: 1A |
| Date: Wednesday, April 07, 2010 | Sheet 38 of 45 | |




| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : BL6 | | | |
| Size | Document Number: CPU Core ( ISL62882) | | Rev: 1A |
| Date: Wednesday, April 07, 2010 | | Sheet 39 of 45 | |




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BL6 | | |
| Size | Document Number: Discharge (1.5V_S5/1.8V) | Rev: 1A |
| Date: Wednesday, April 07, 2010 | Sheet 40 of 45 | |

OCP:30A
(Peak 28A, AVG 23.1A)
F: 297k Hz

| GFX_CORE_CNTRL1 | GFX_CORE_CNTRL0 | Madison/Park | Madison/Park Resistor | M92 | M92 Resistor | M96 | M96 Resistor |
|---|---|---|---|---|---|---|---|
| LOW | LOW | 0.9V | R1=39.2K CS33922FB15 | 0.9V | R1=39.2K CS33922FB15 | 0.9V | R1=39.2K CS33922FB15 |
| LOW | HIGH | 0.95V | R2=60.4K CS36042FB10 | 0.95V | R2=60.4K CS36042FB10 | 0.95V | R2=49.9K CS34992FB10 |
| HIGH | LOW | 1.12V | R3=309K CS43092FB16 | 1.1V | R3=270K CS42702FB10 | 1V | R3=249K CS42492FB18 |
| HIGH | HIGH | NA | R4=88.7K CS38872FB18 | 1.2V | R4=93.1K CS39312FB15 | 1.1V | R4=140K CS41402FB14 |

0.996A

1.791A

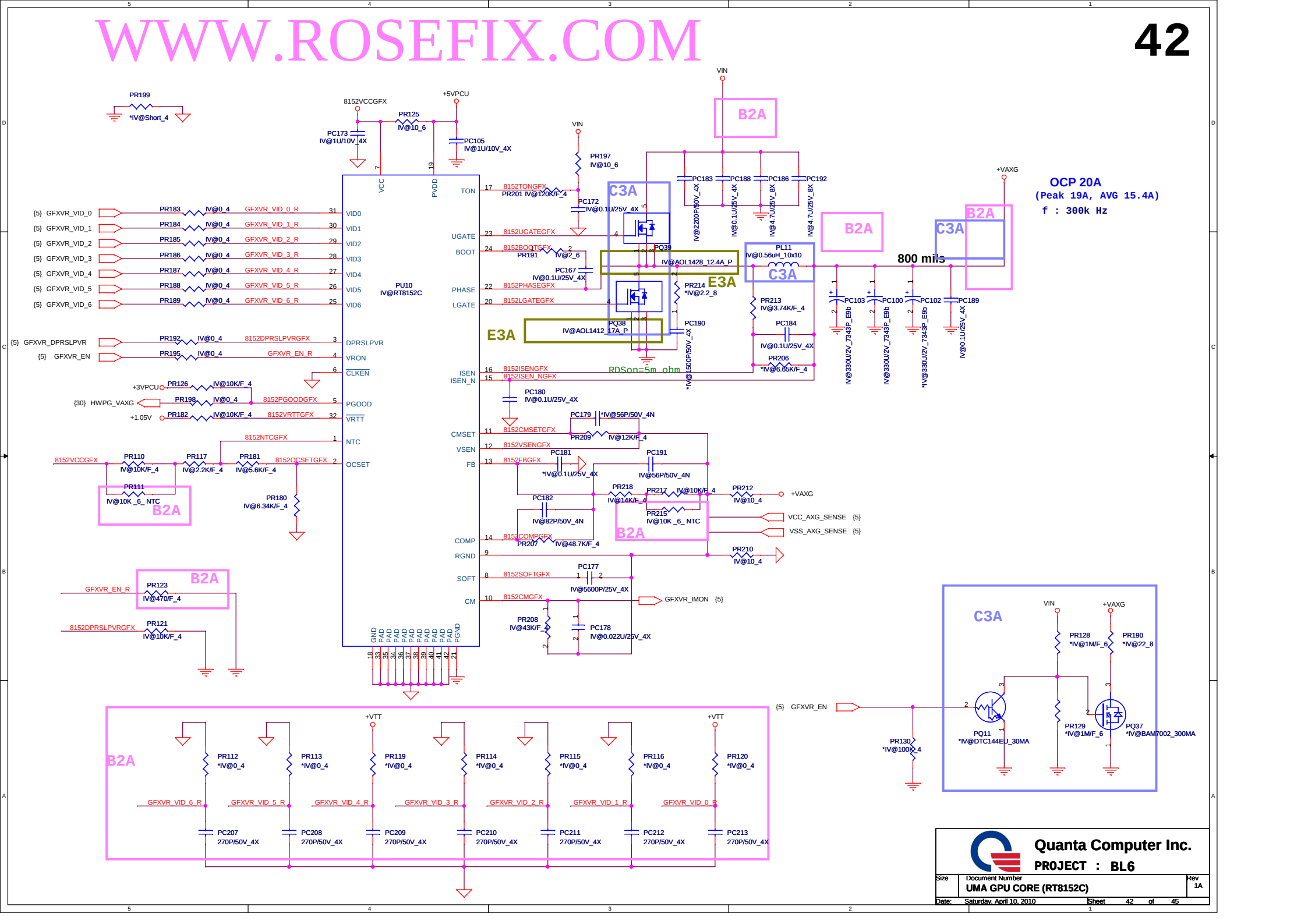
VO=(0.8(R1+R2)/R2)
R2<120Kohm

PCIE_VDDC
M92,M96-->1.1V
Madison,Park-->1.0V

| | Madison,Park | M92,M96 |
|---|---|---|
| PR163 = R1 | 25.5K/F_4 CS32552FB11 | 38.3K/F_4 CS33832FB08 |
| PR166 = R2 | 100K/F_4 CS41002FB28 | 100K/F_4 CS41002FB28 |

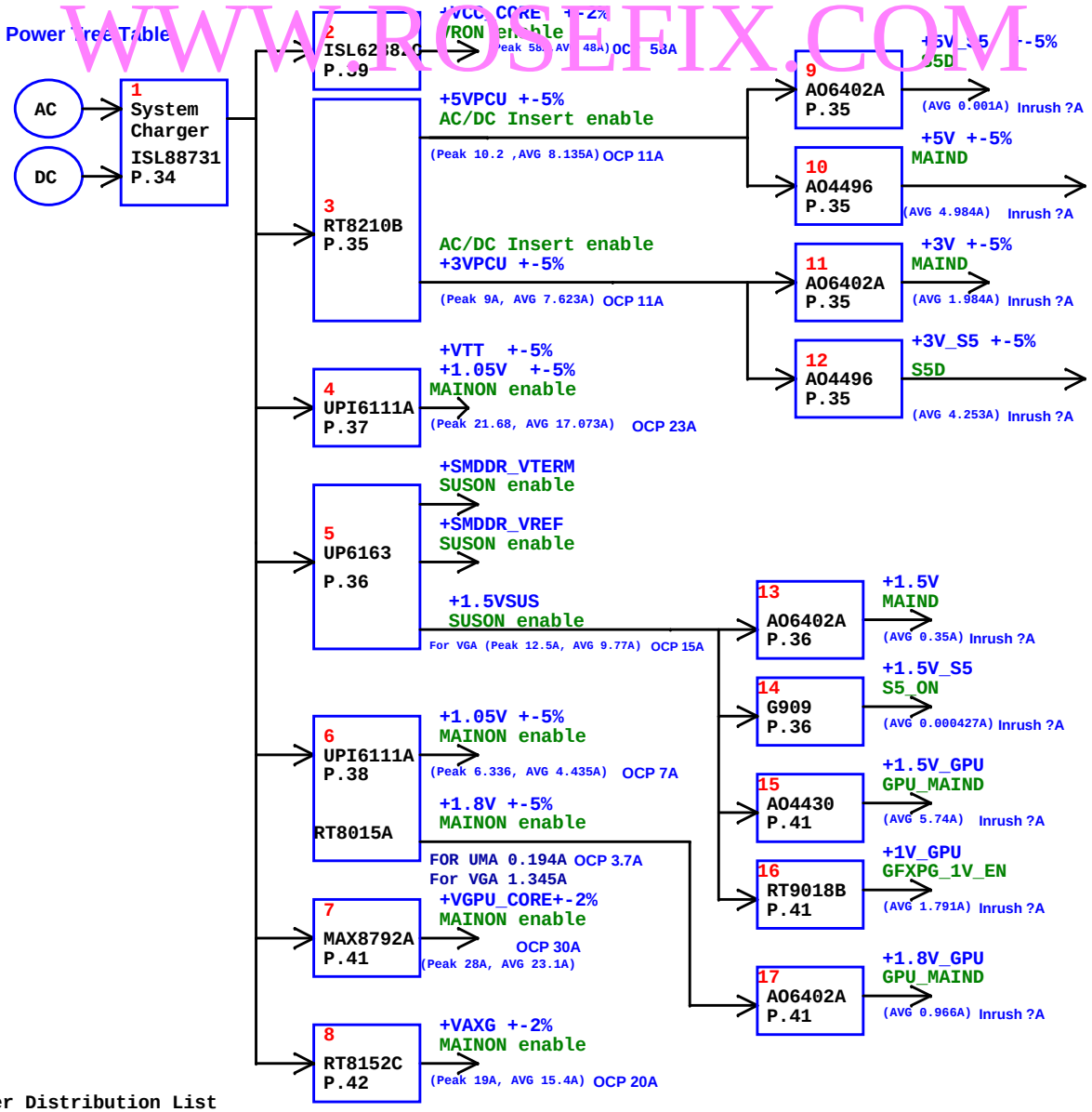
5.74A

Quanta Computer Inc.
PROJECT : BL6
Size | Document Number: +VGPU_CORE (MAX8792) | Rev 1A
Date: Saturday, April 10, 2010 | Sheet 41 of 45




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : BL6 | | |
| Size | Document Number: UMA GPU CORE (RT8152C) | Rev: 1A |
| Date: Saturday, April 10, 2010 | Sheet 42 of 45 | |

Power Tree Table




Power Distribution List

| Power | Distribution |
|---|---|
| | |
| | |
| | |
| | |
| | |
| | |
| | |

Quanta Computer Inc.
PROJECT : BL6

| Size | Document Number | Rev |
|---|---|---|
| | Power Tree Table | 1A |

Date: Wednesday, April 07, 2010 Sheet 43 of 45