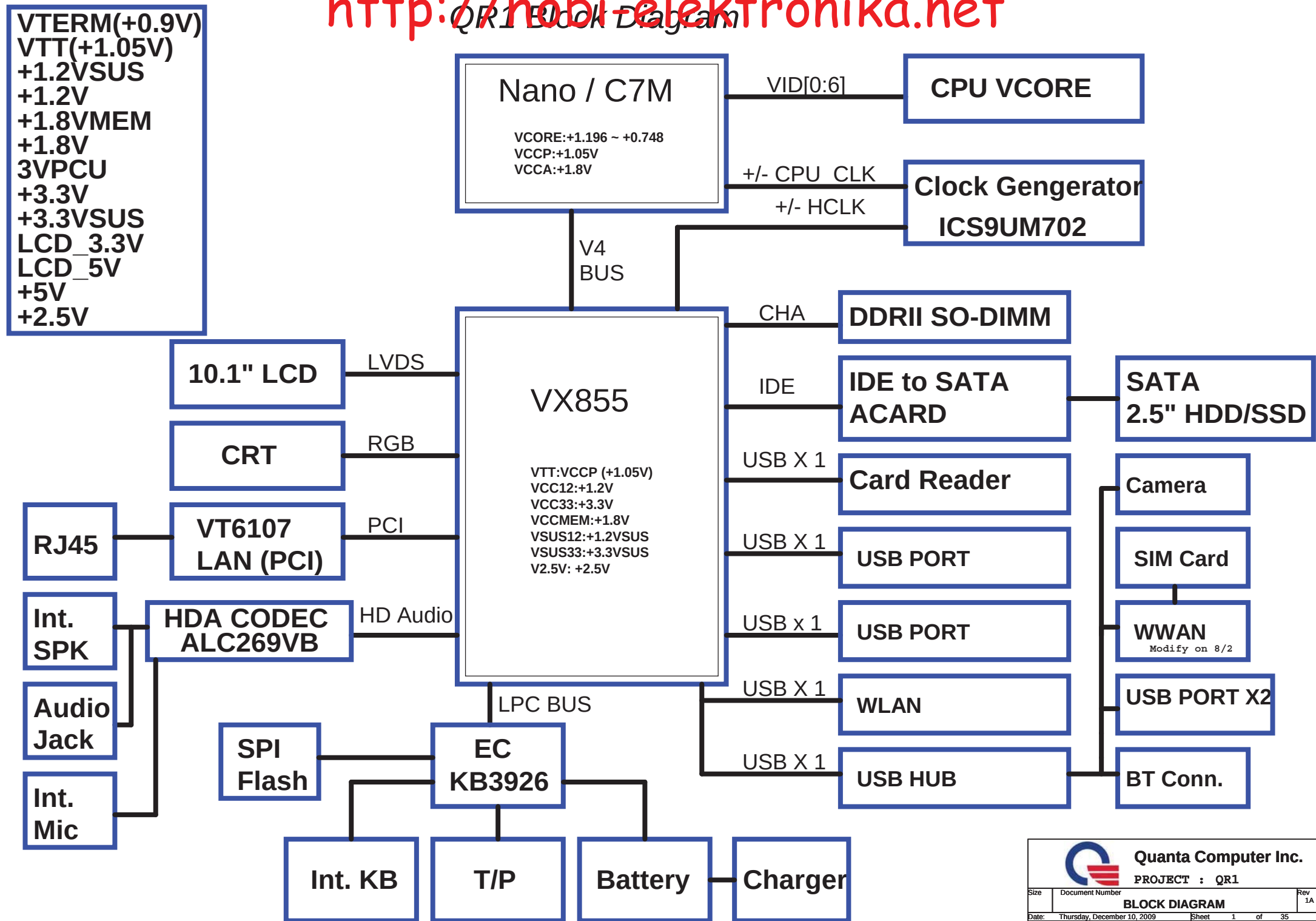
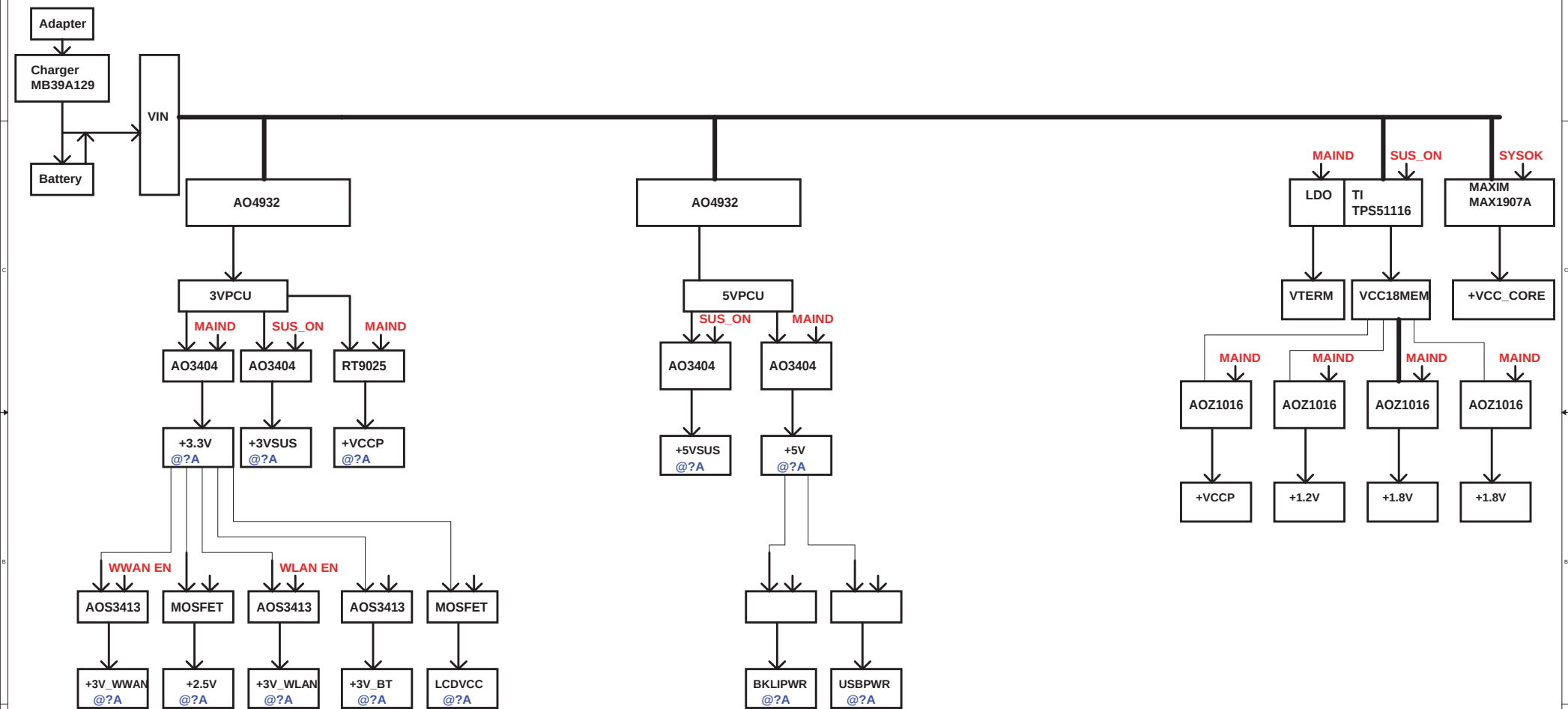
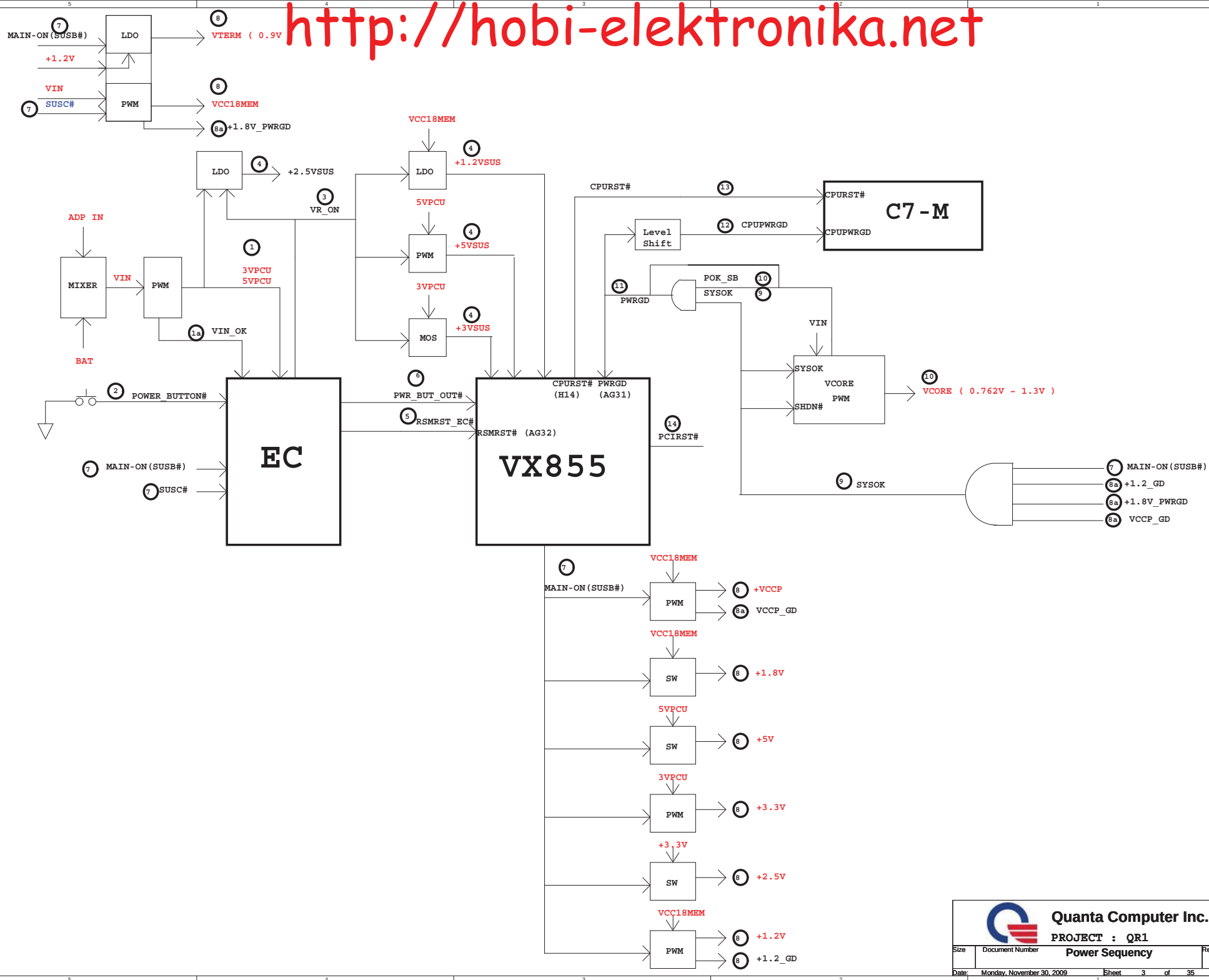
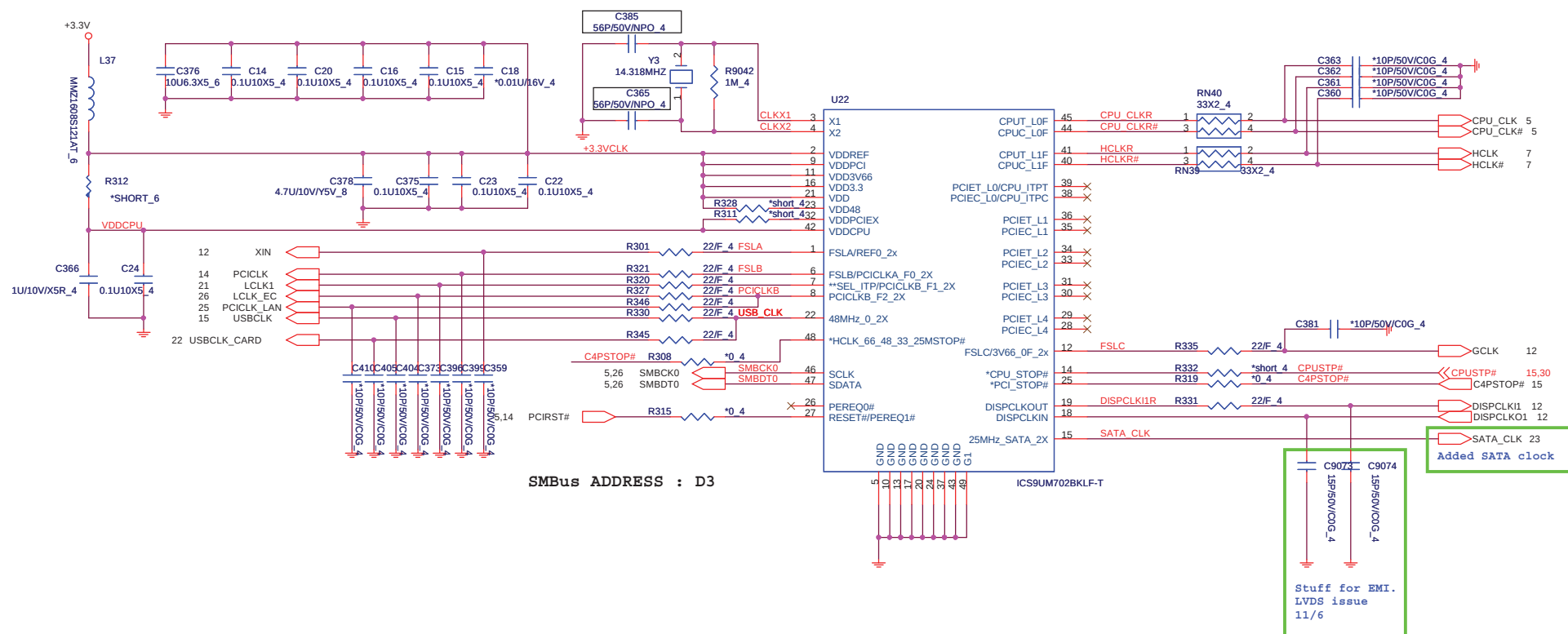






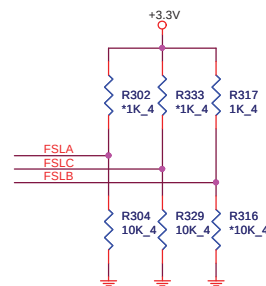


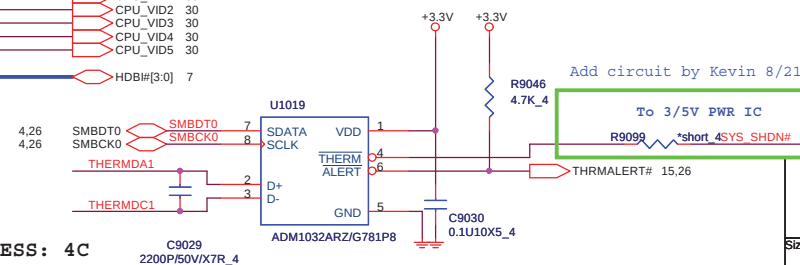
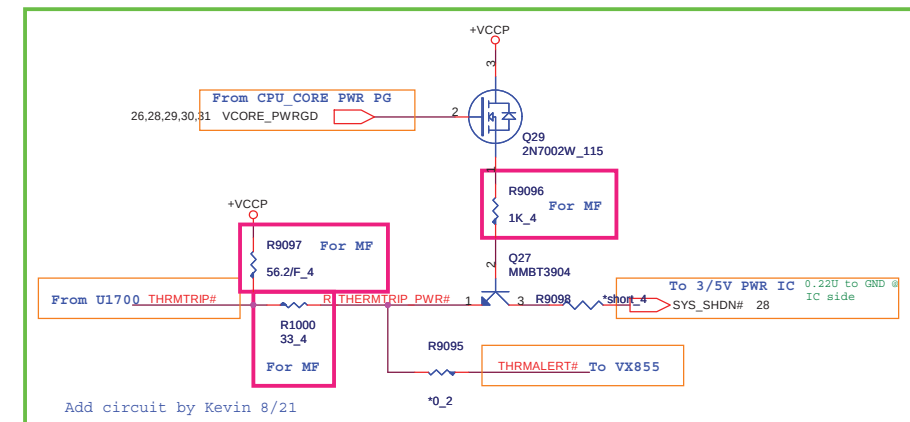
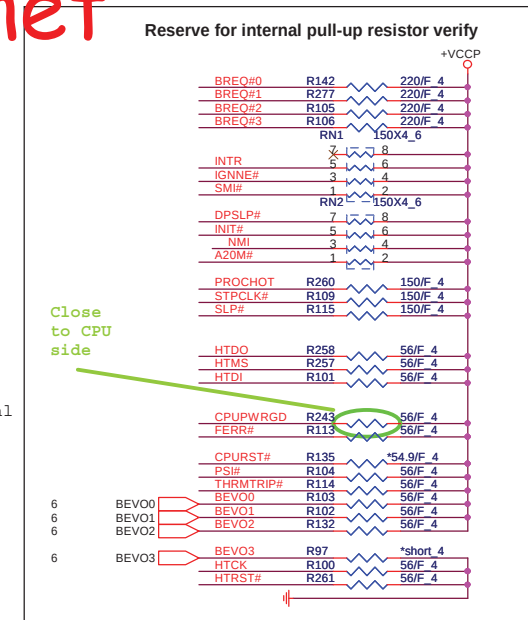
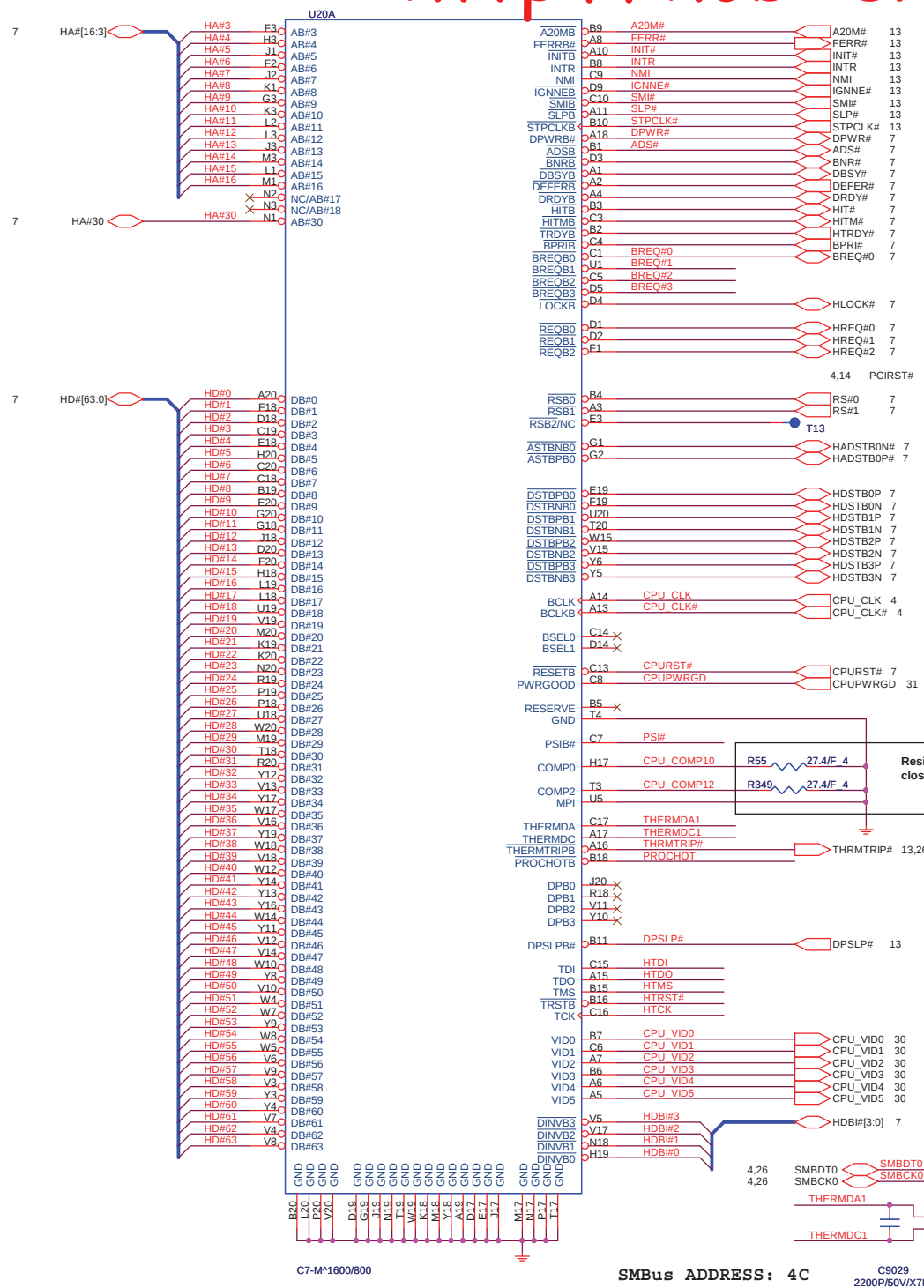


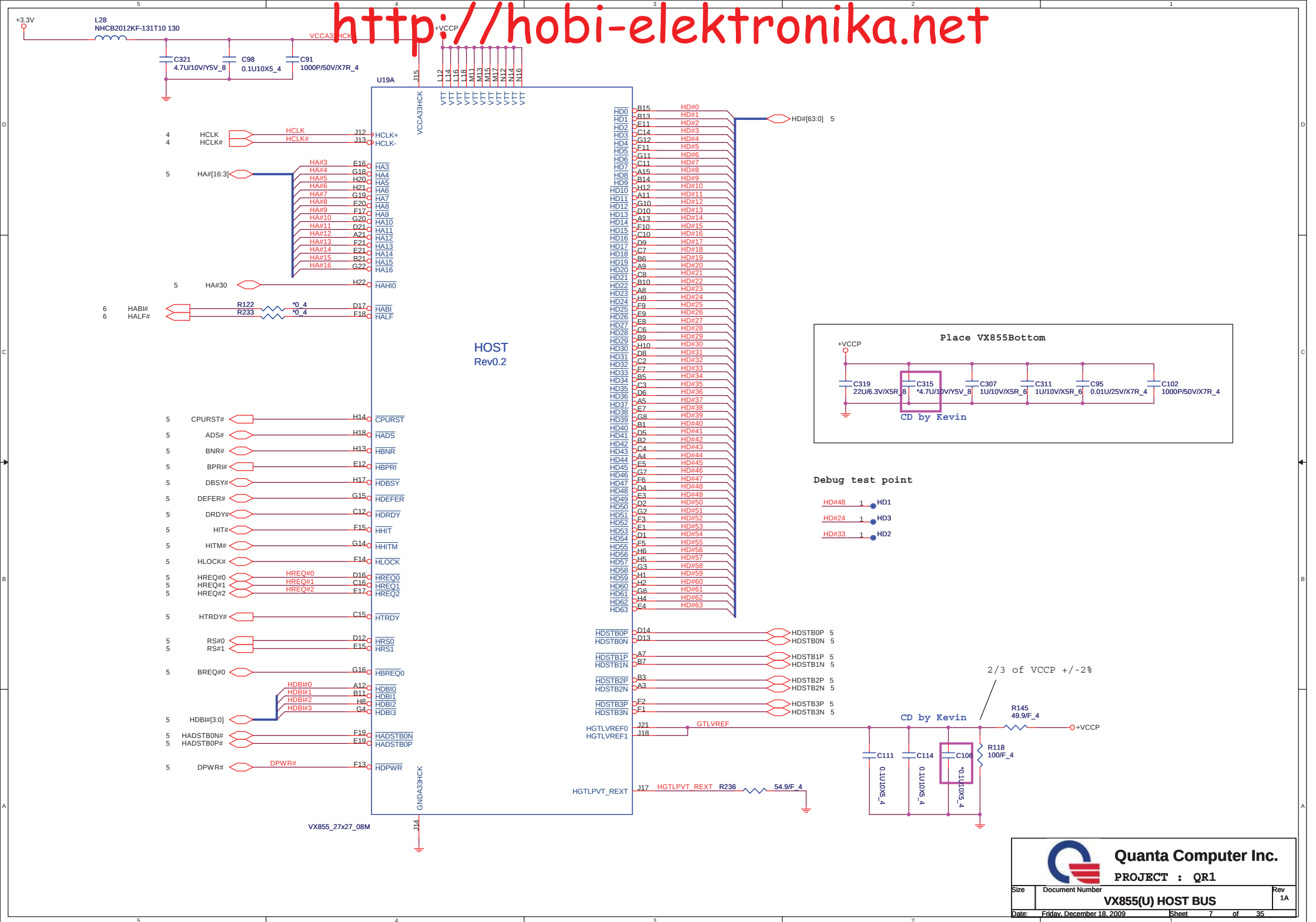
SMBus ADDRESS : D3

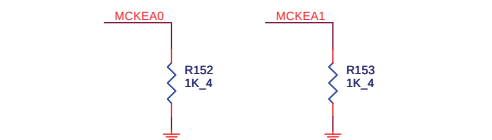
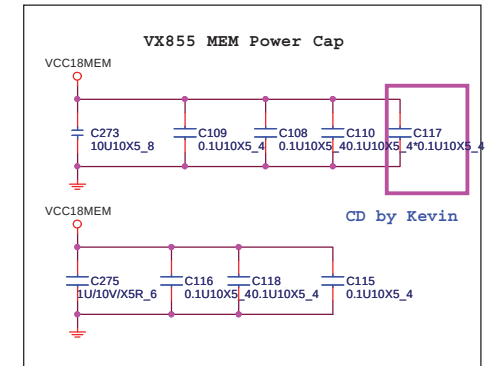
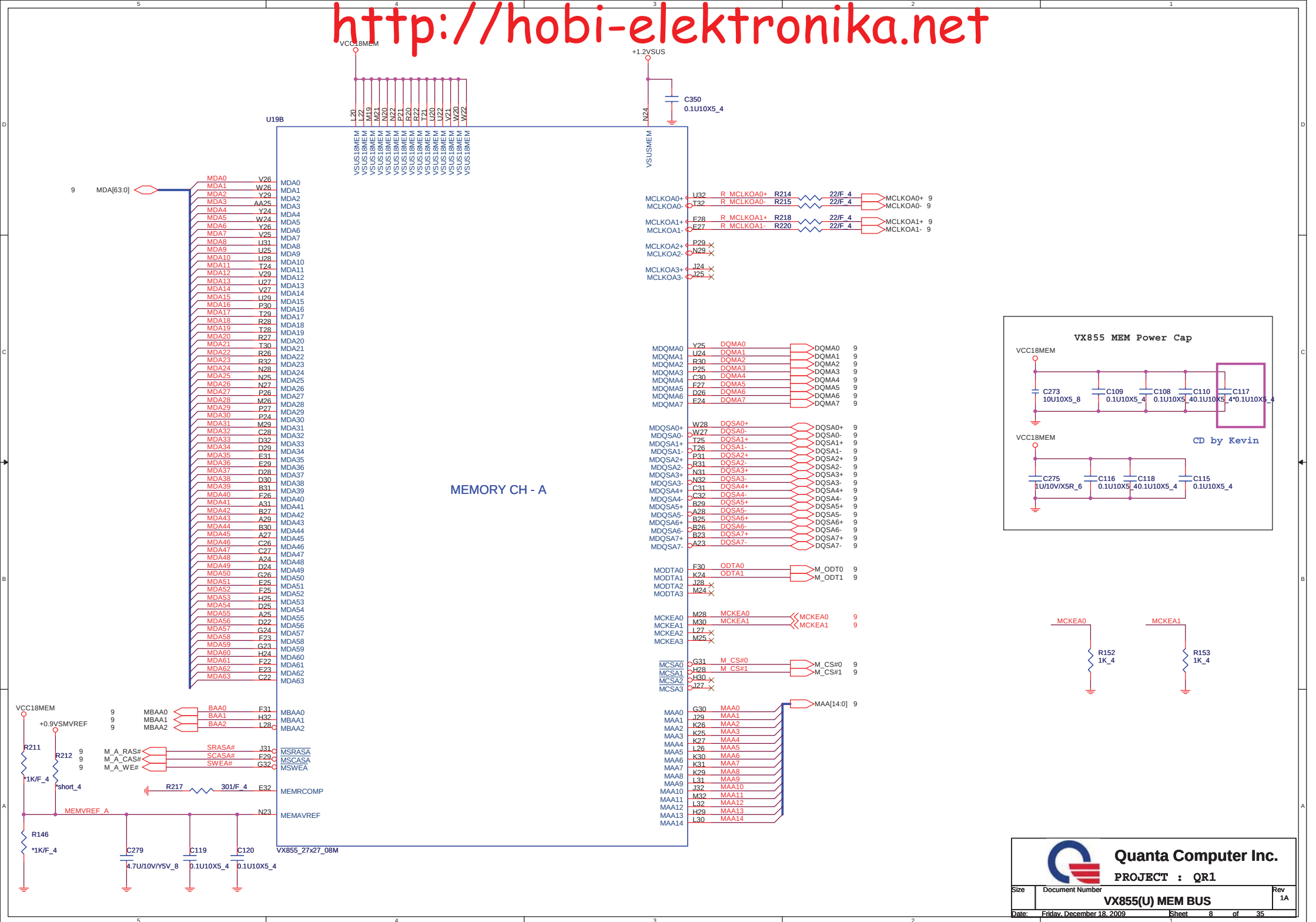
ICS9UM701 ON : 0 OFF : 1

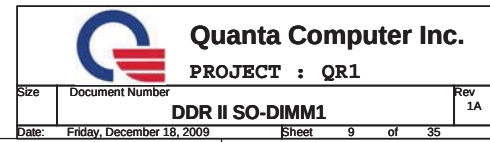
3	2	1		
FSLA	FSLC	FSLB	CPU	PCI
0	0	0	266.66	33
1	0	0	133.33	33
0	0	1	200	33
1	0	1	166.66	33
0	1	0	333.33	33
1	1	0	100	33
0	1	1	400	33
1	1	1	200	33







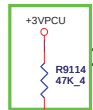




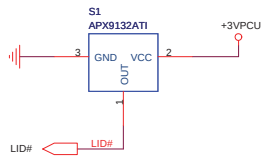
SCREW HOLE

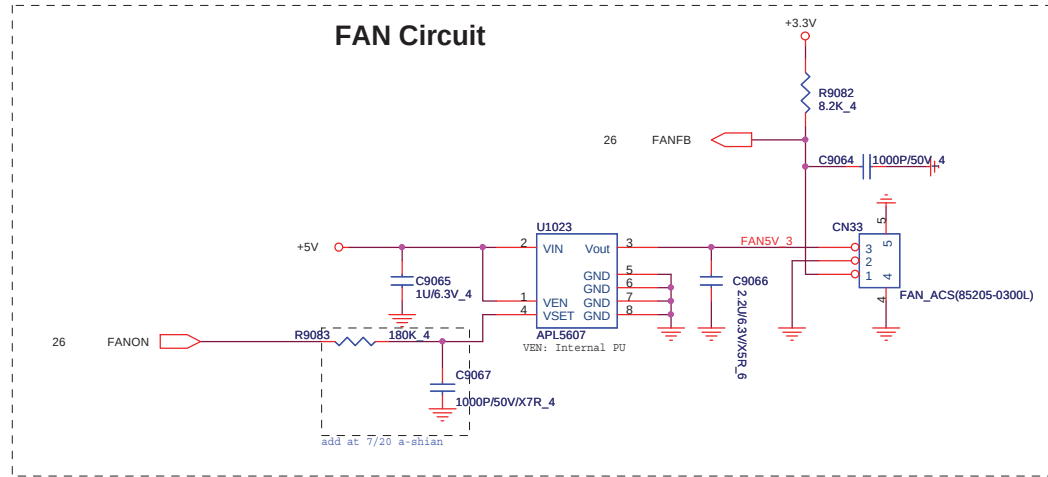
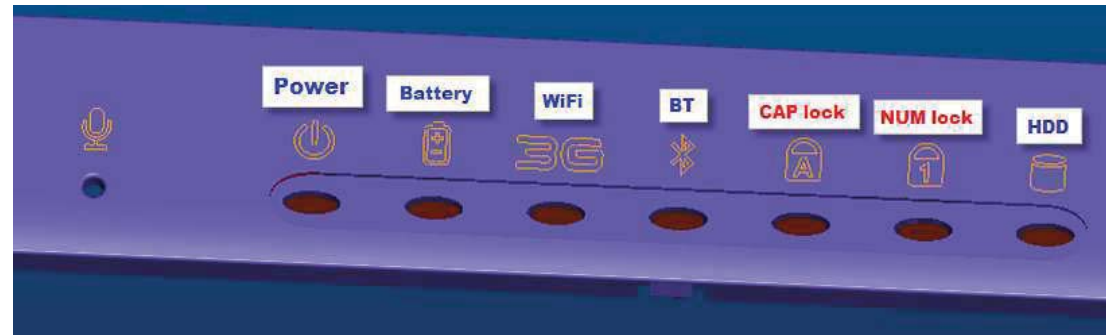
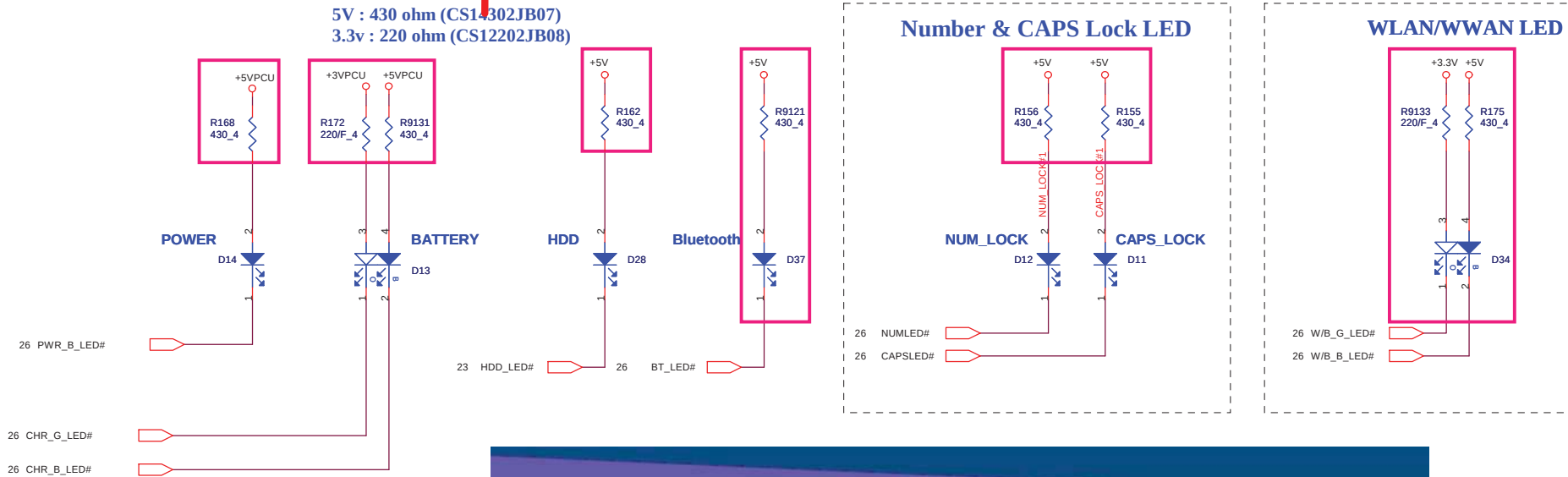
Power Button

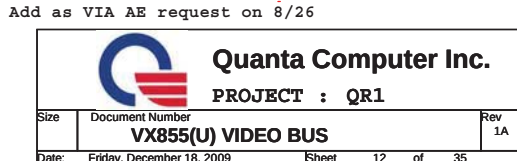
Added PWRBUT pull high 47KR

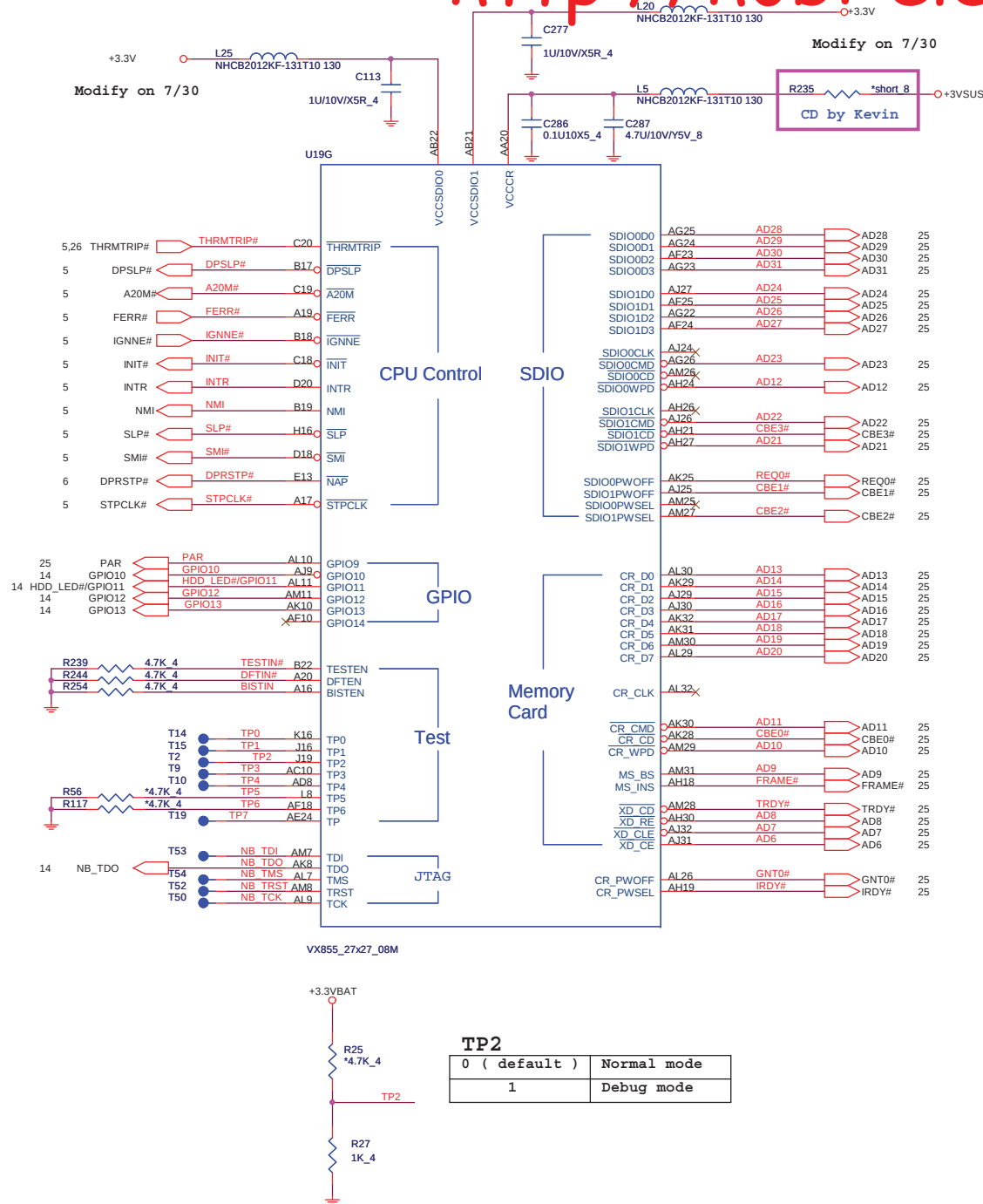


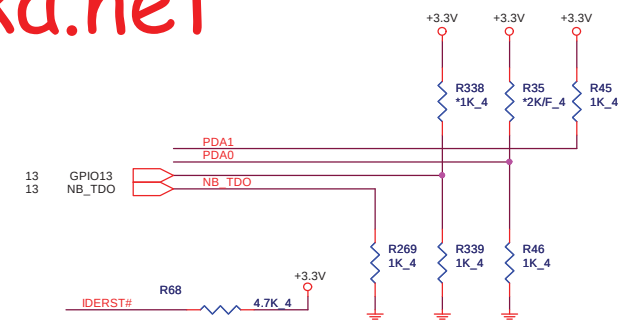
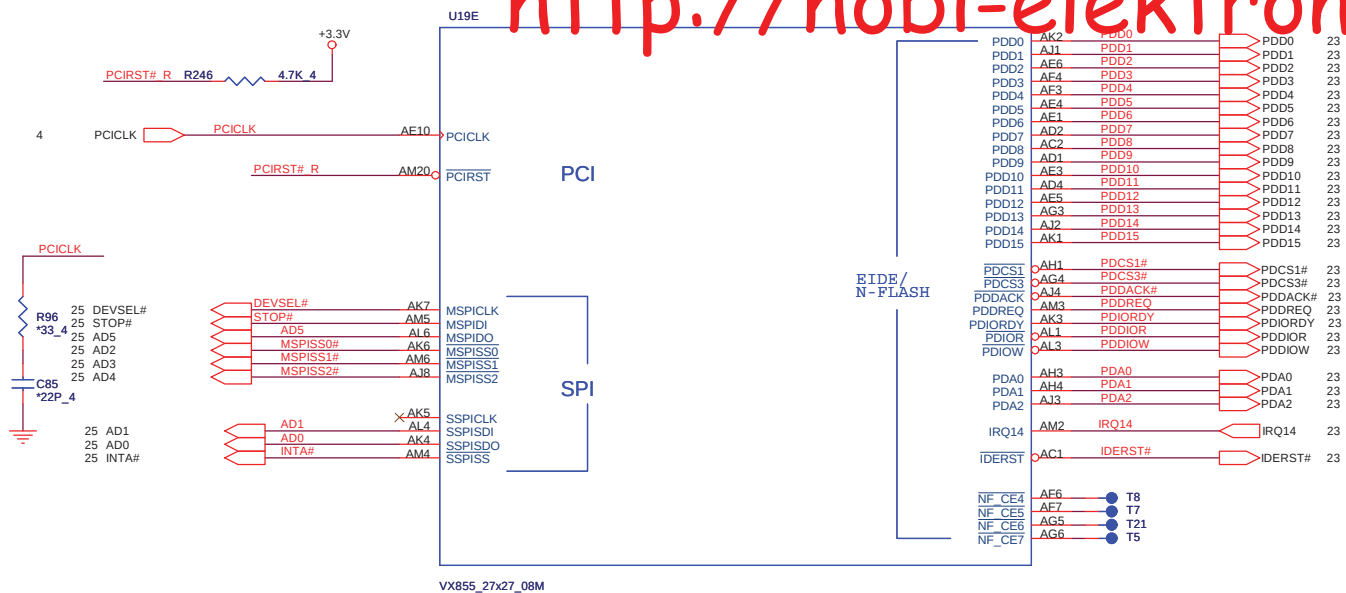
MR Sensor





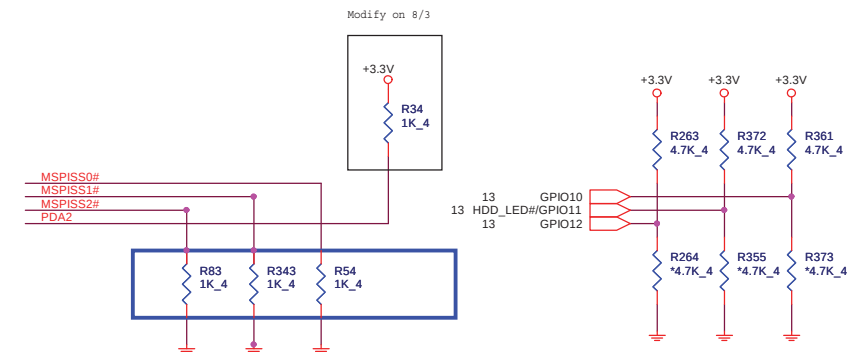






NB Strapping

Pin	Function	Pull Low	Pull High
PDA1	PLL OK source select	from NB PLL	from SB Logic*
PDA0	IOQ depth	12 *	1
GPIO13	GTL pull up	Enable *	Disable
NB_TDO	Debug Link enable	XD Mode*	Debug Link



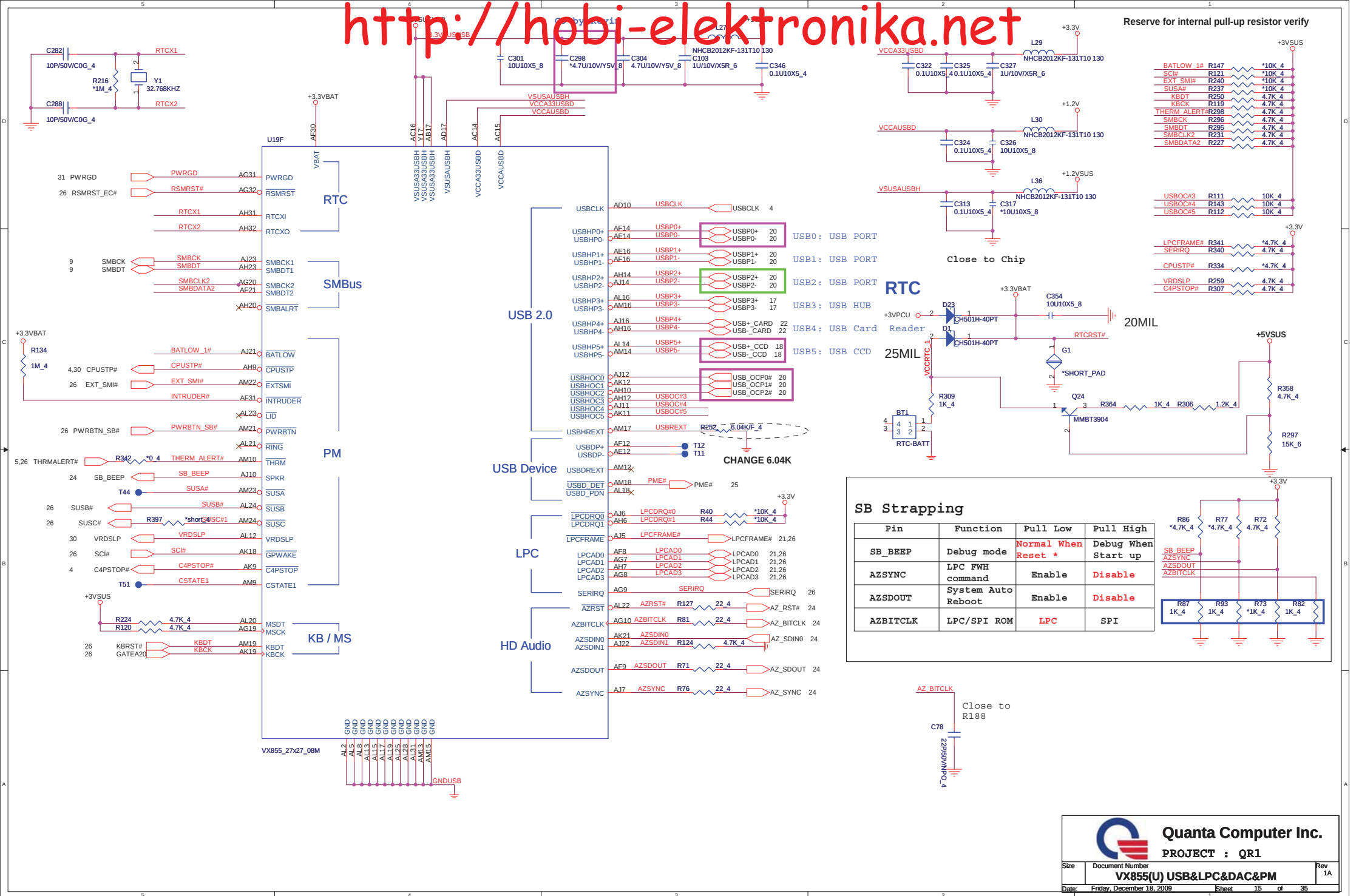
SB Strapping

Pin	0:Low 1:High	Function
MSPISS1/ MSPISS0	00 *	IDE
	01	NFC
	10	CE ATA
MSPISS2	0: SPI/LPC *	NFC ROM Select
	1: NFC ROM	
PDA2	0: Disable	PCI Master Mode Enable
	1: Enable	

NB Strapping

Pin	0:Low 1:High	FSB Freq.
GPIO12/ GPIO11/ GPIO10	000	100Mhz
	001	133Mhz
	010	200Mhz
	011	266Mhz
	111 *	Auto Mode



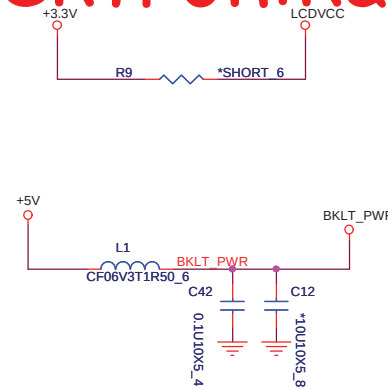
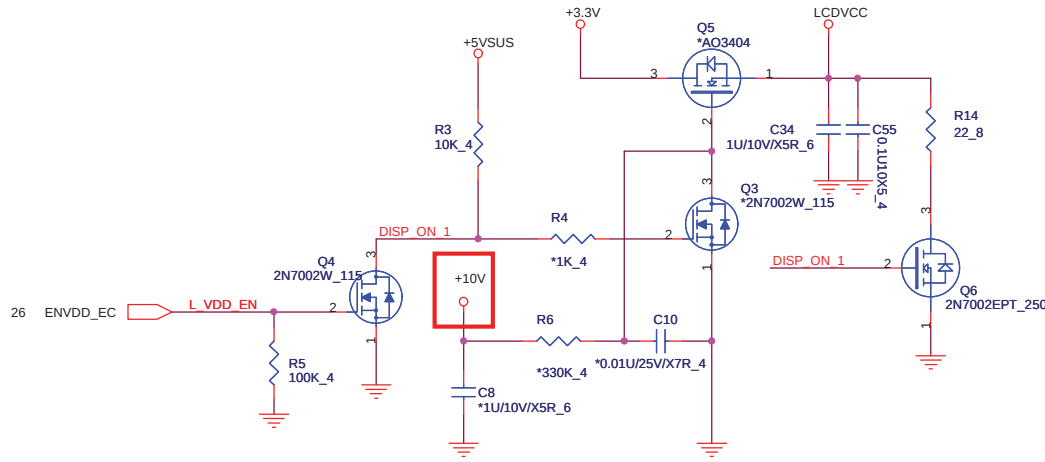




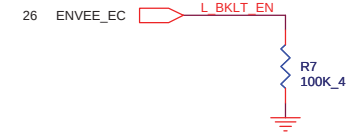
LVDS

<http://hobi-elektronika.net>

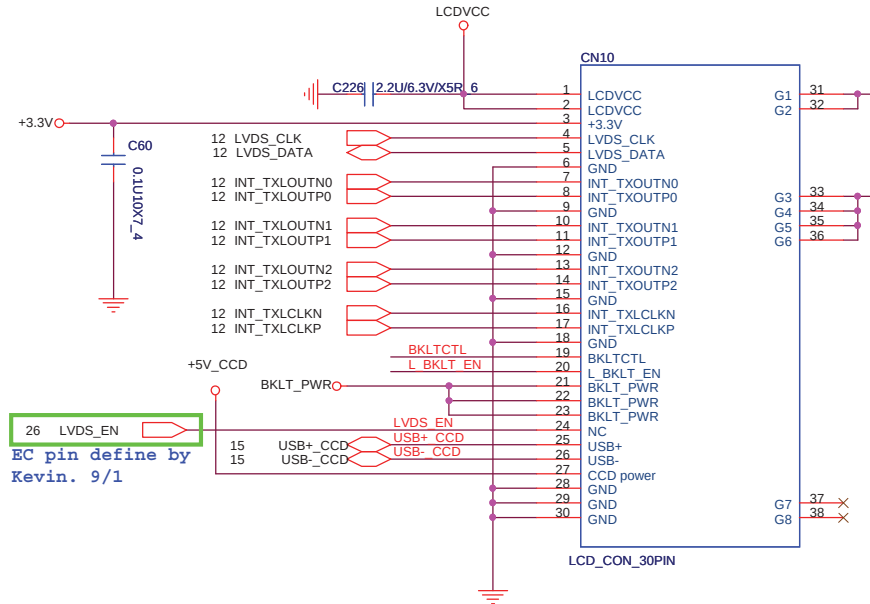
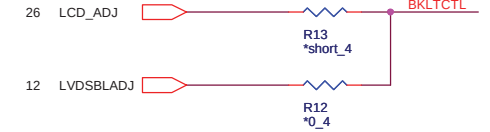
LVDS Enable



Display On



Backlight Control



LVDS (10.1")
(1024x600,
1366x768)

26 LVDS_EN
EC pin define by
Kevin. 9/1

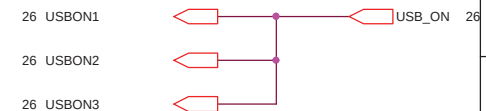
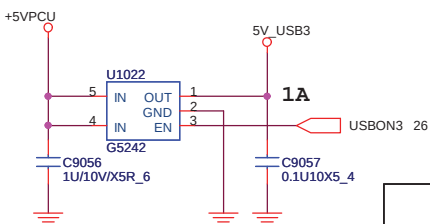
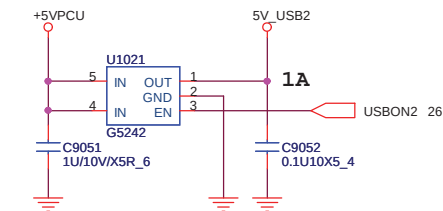
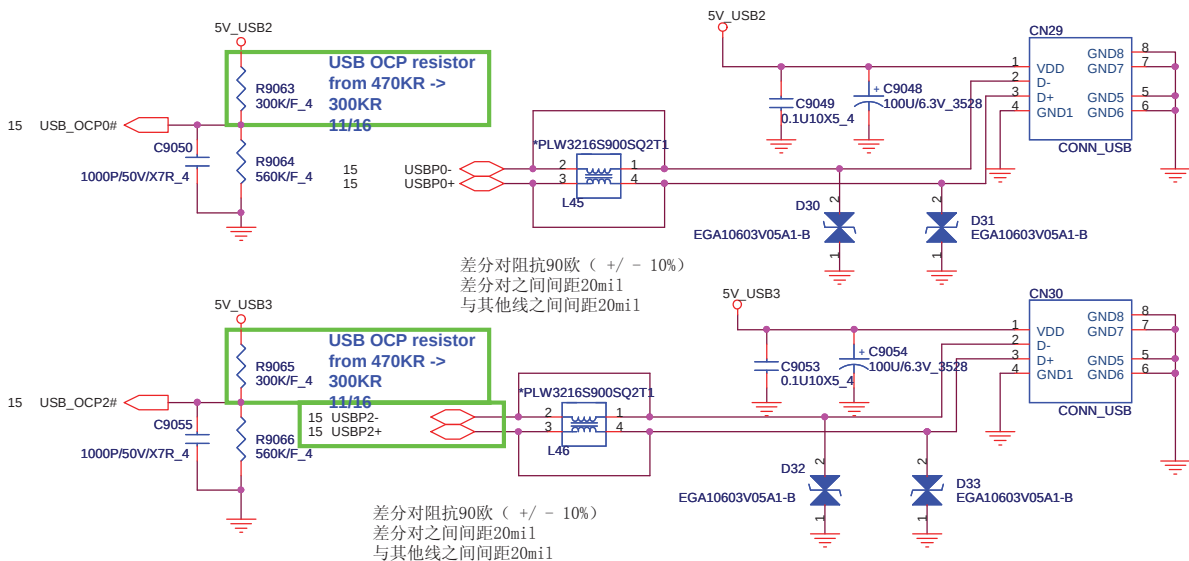
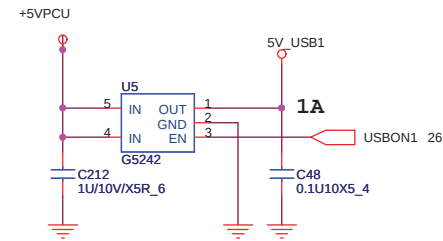
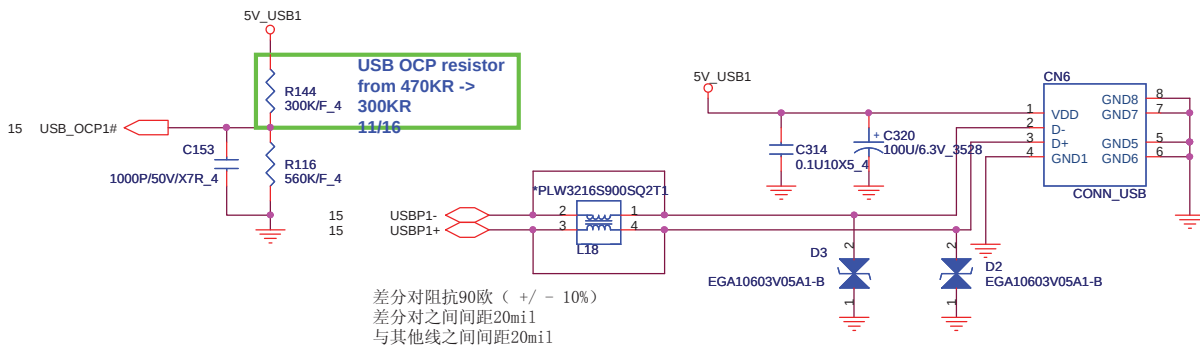
Modify on 8/21

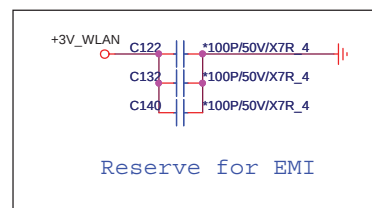
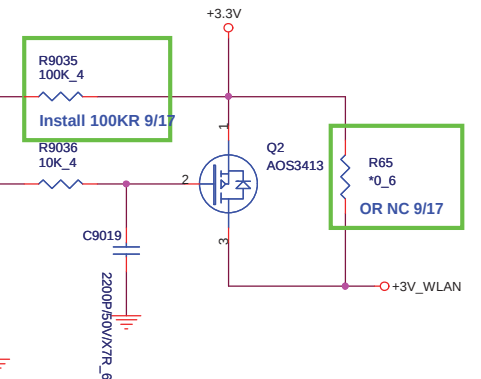


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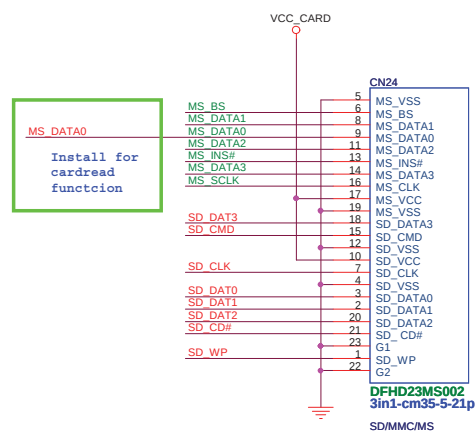
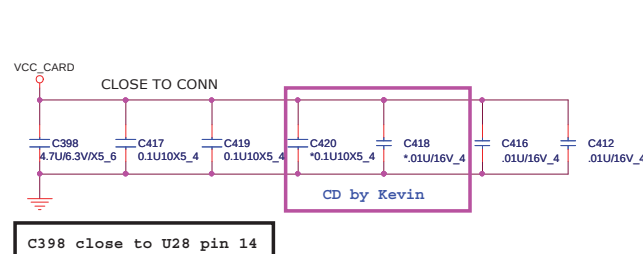
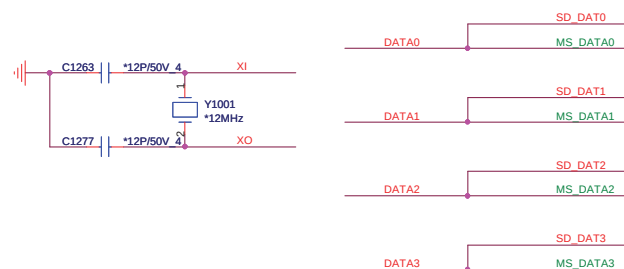
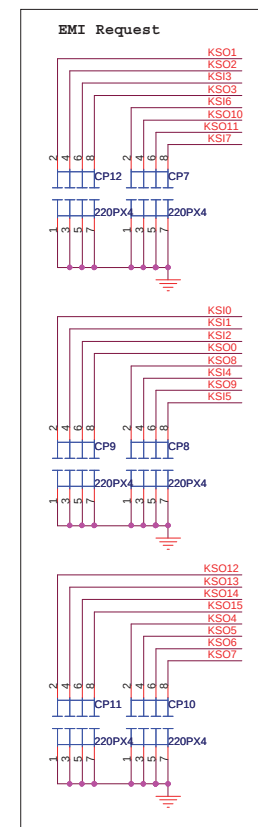
PROJECT : QR1

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	LVDS	1A
Date:	Friday, December 18, 2009	Sheet 18 of 35

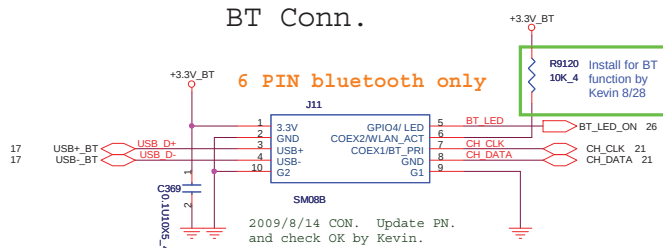




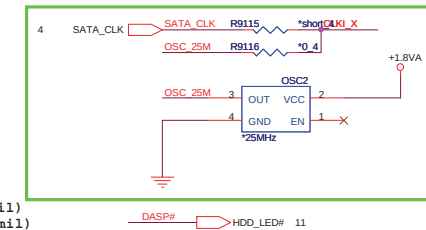
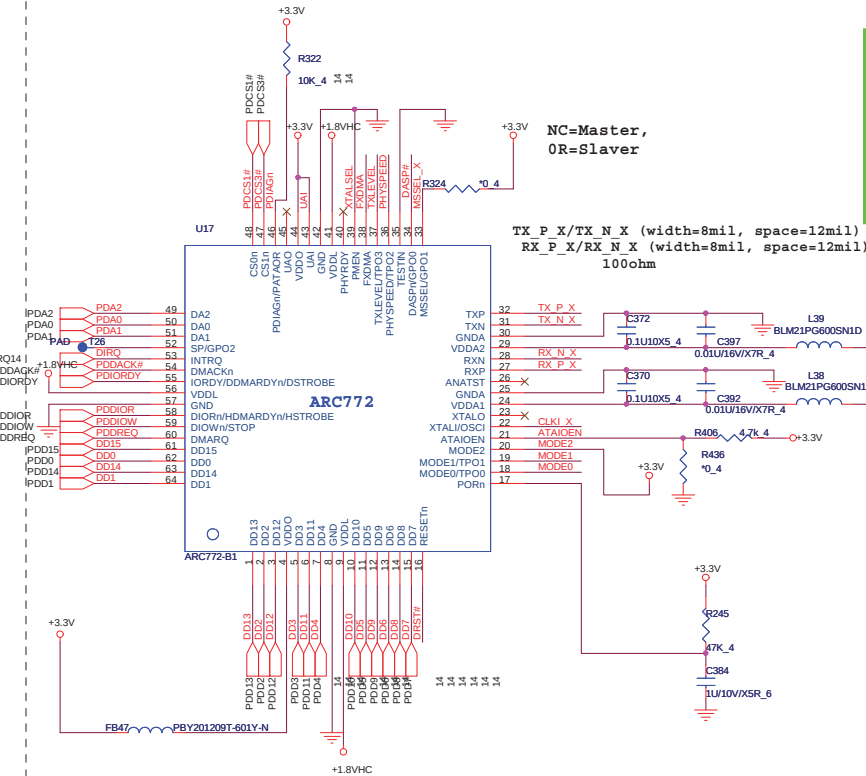
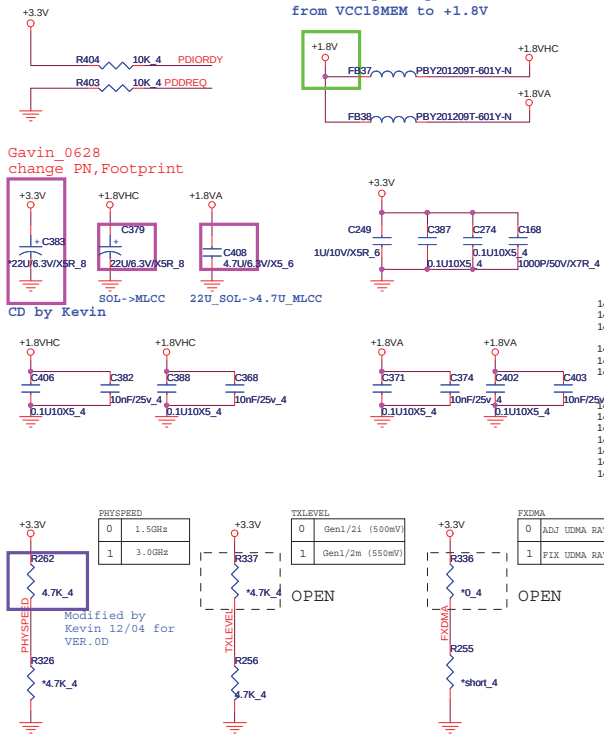
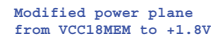
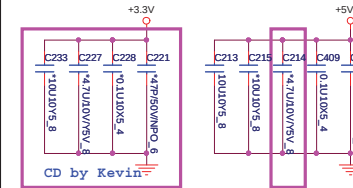
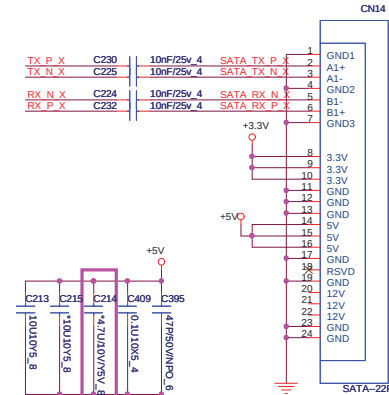
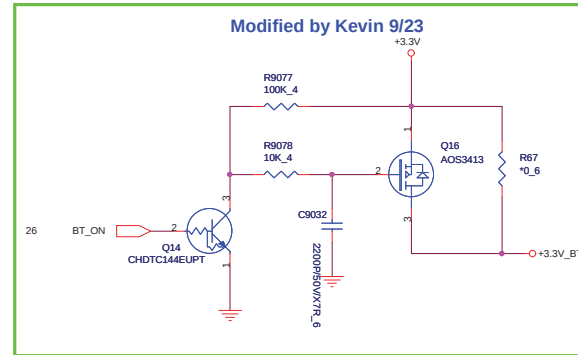
Reserve for EMI



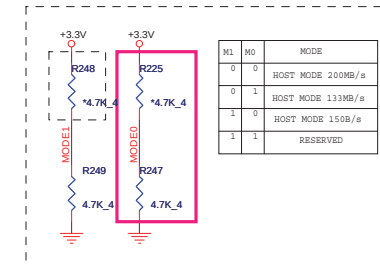
BT Conn.



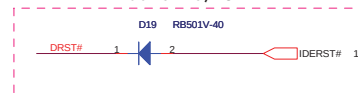
Modified by Kevin 9/23

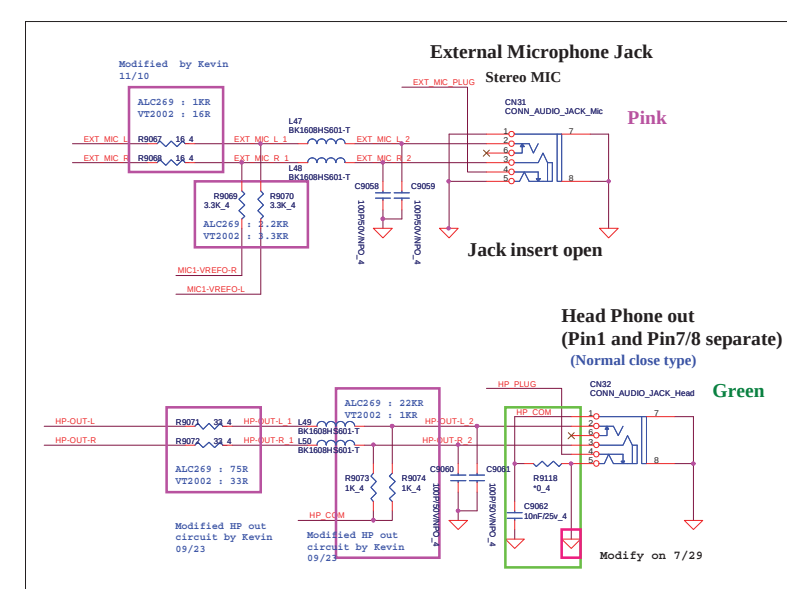
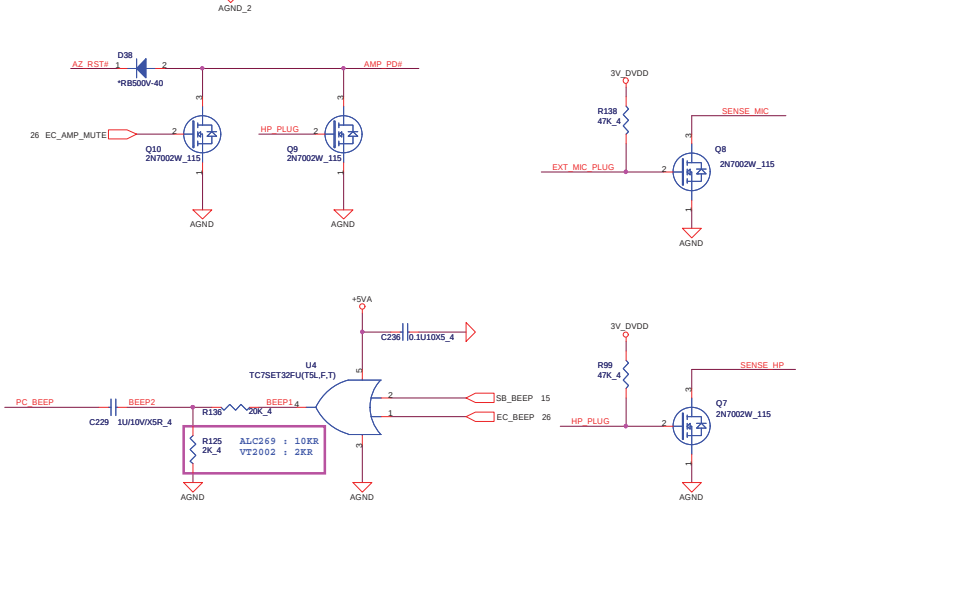
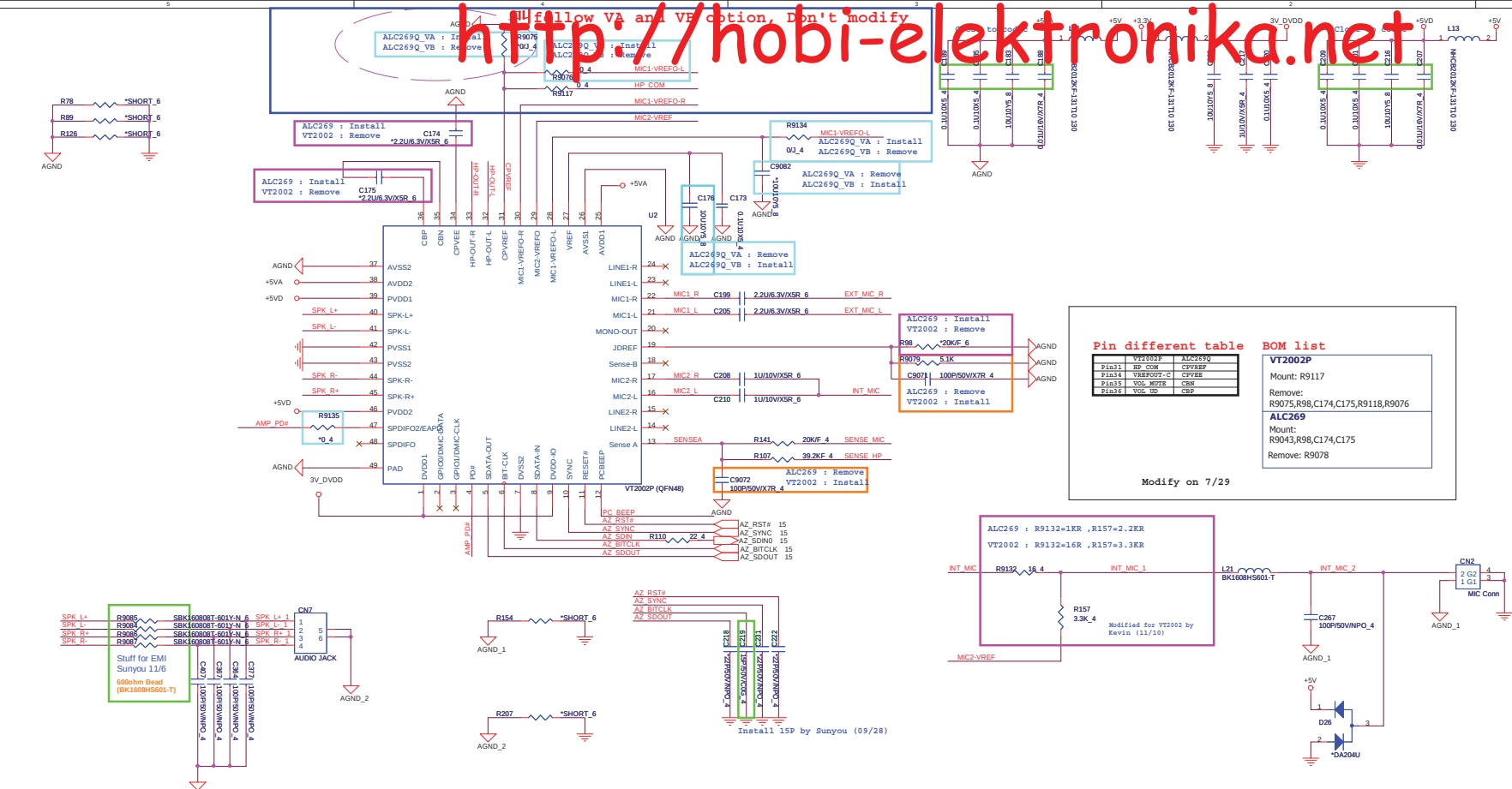


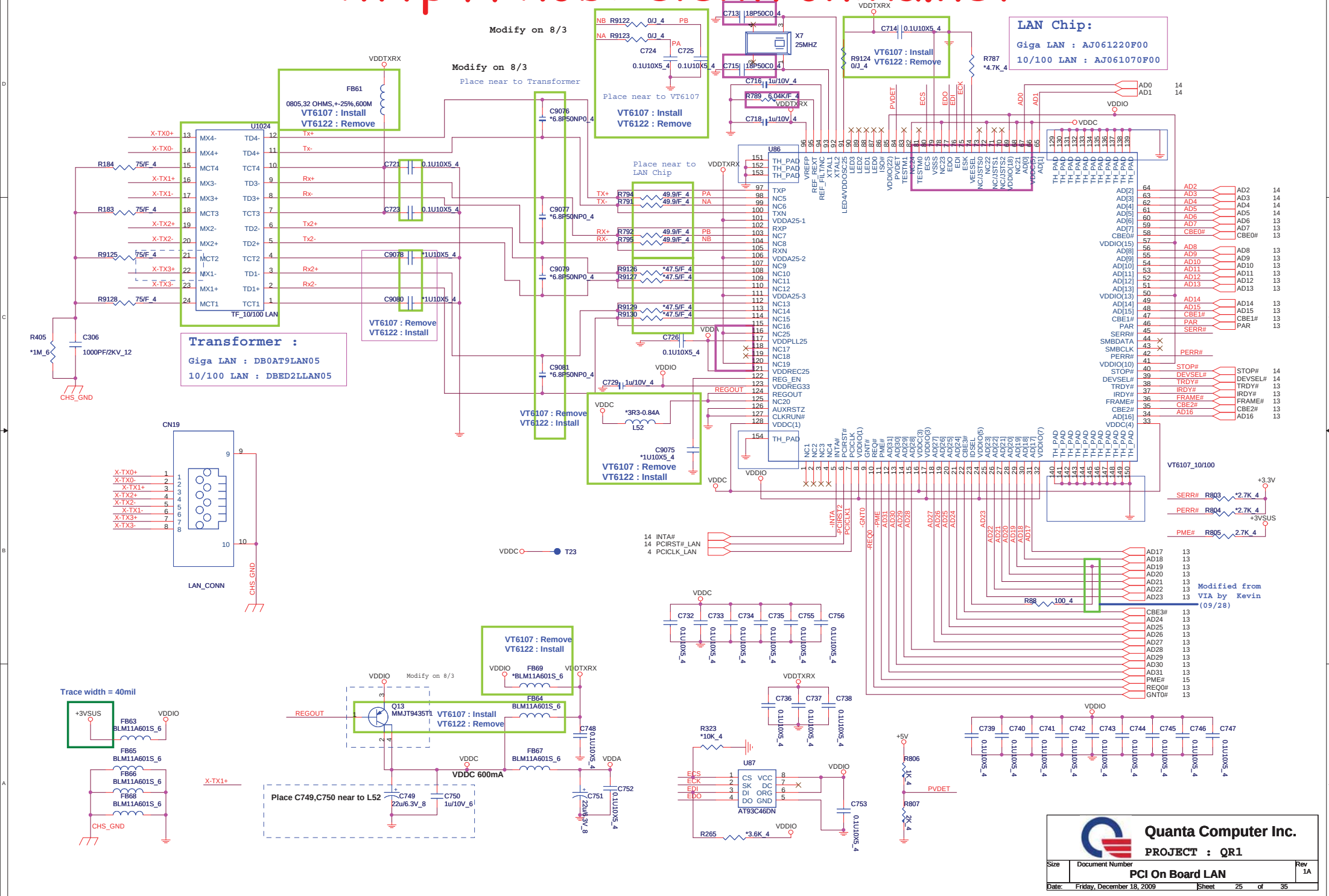
for DATA	MODE2	20	DRL	Operation Mode (MODE2, MODE1, MODE0)
	MODE3/TPO1	19	DROH	First output port (TPO0, TPO1)
+1.5VA	MODE0/TPO0	18	DROL	
		8 mA		
GN1D				(MODE2, MODE1, MODE0) (with POR0 low)
				Configure host/clients and Ultra DMA speed
				0.0 Device Mode at 200MB/s
				0.1 Device Mode at 133MB/s
				0.2 Device Mode at 150MB/s (default)
				0.3 Reserved
				1.0.0 Host Mode at 200MB/s
				1.0.1 Host Mode at 133MB/s
				1.0.2 Host Mode at 150MB/s
				1.1 Reserved

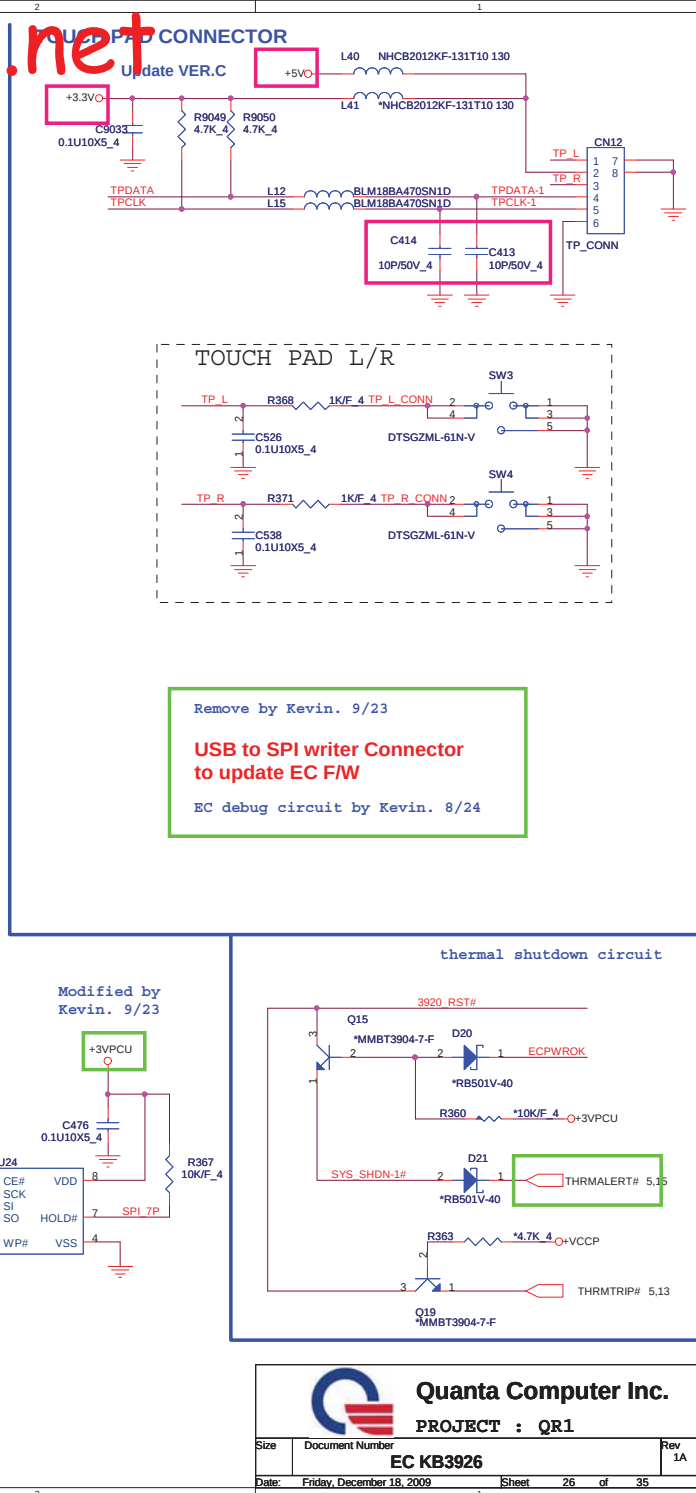
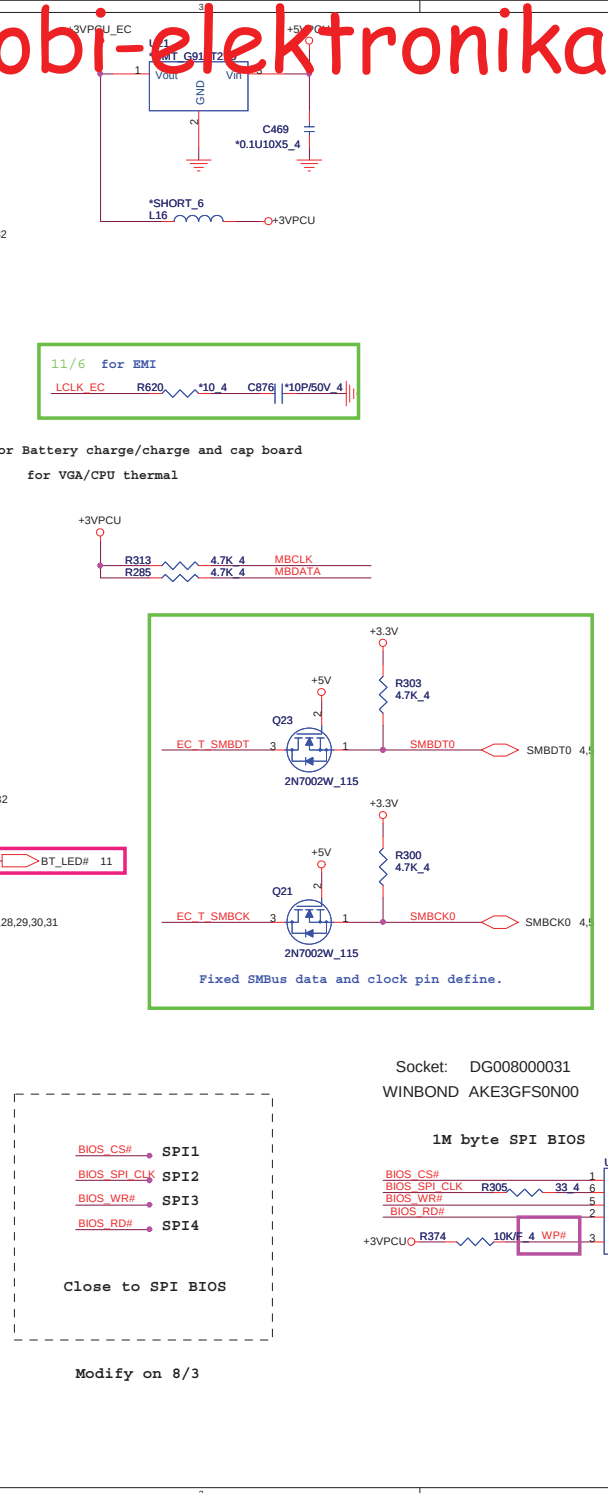


Add on 8/19









5 Volt +/- 5%
Fs=400K
TDC :4.5A (Imax)
OCP minimum 6A

10/14 PC141 BOM Change to 4.7uF by Howard

11/3 Del PJP21 by Howard

12/9 Added for 3G issue by Kevin

AO4932 Rds=15.8~19.6mOhm

+5VPCU OCP:4.3A 400K

L(ripple current)

= (19-5) * 5 / (3.3u*400k*19)

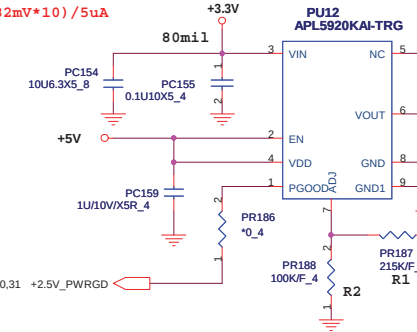
= 2.791A

Iocp=4.3 - (2.791/2) ~ 2.9045A

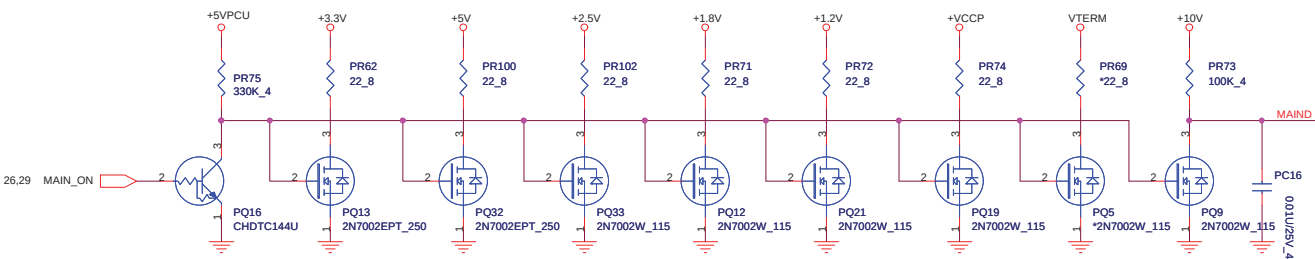
Vth=2.9045A*19.6mOhm=56.9282mV

R(Ilim) = (56.9282mV*10) / 5uA

= 113.8K=118K



Discharge



Iocp=4.5 - (1.653/2) ~ 3.6735A
Vth=3.6735A*19.6mOhm=72mV
R(Ilim) = (72mV*10) / 5uA
= 144K=143K

TDC : 0.5A (Imax)

11/3 Del PJP23 by Howard

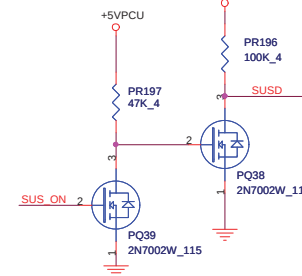
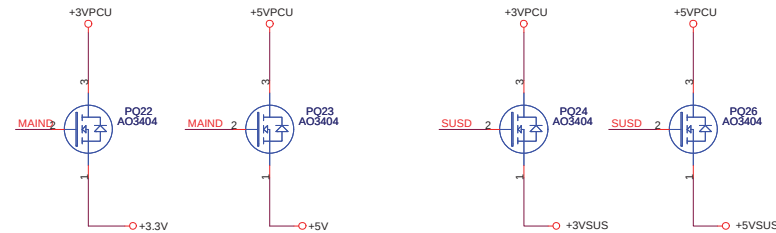
AO4932 Rds=15.8~19.6mOhm

+3VPCU OCP:4.5A 500K

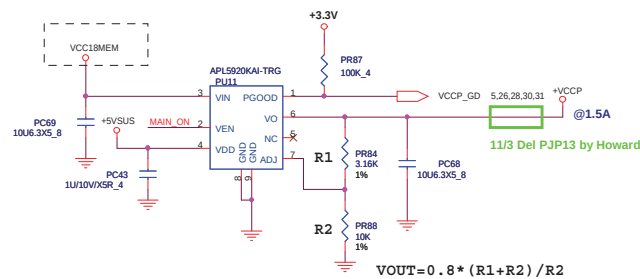
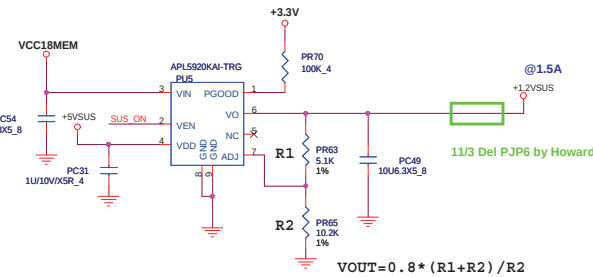
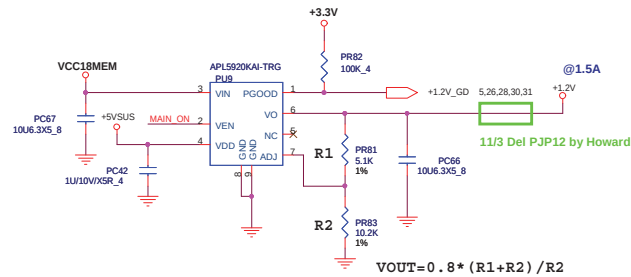
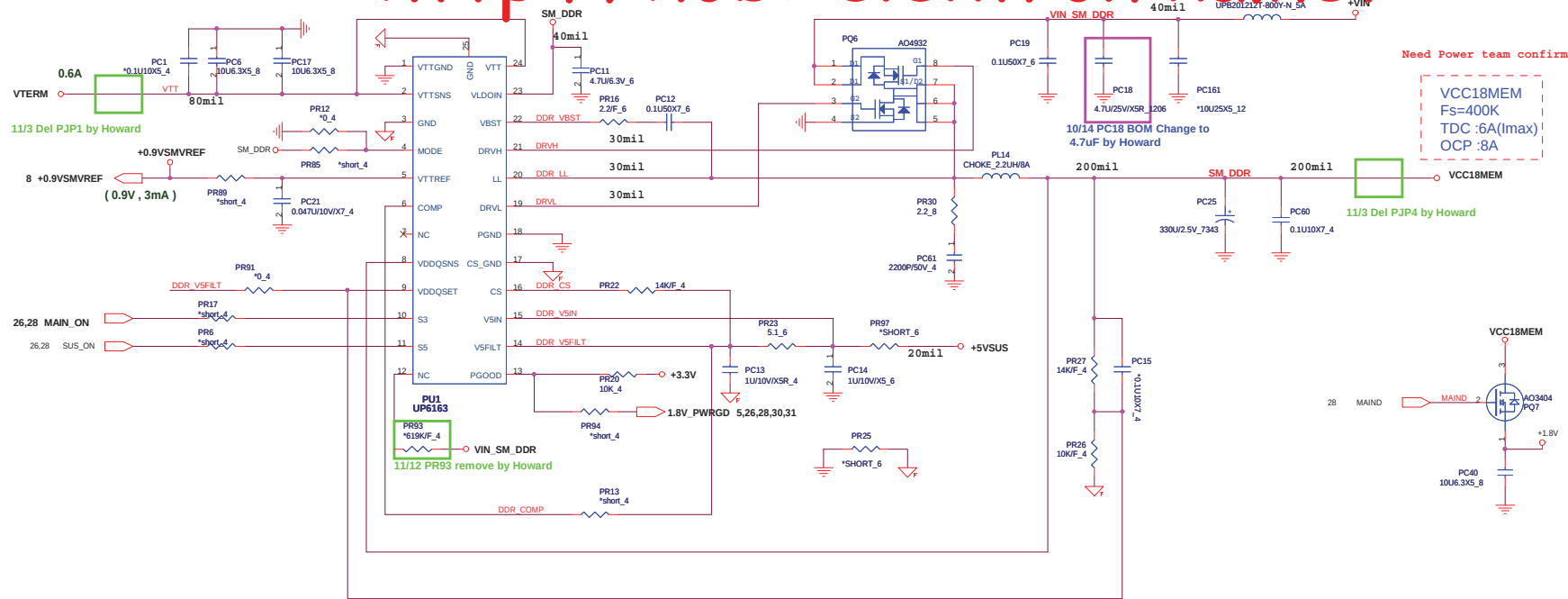
L(ripple current)

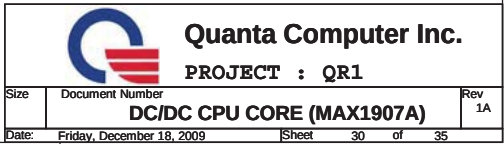
= (19-3.3) * 3.3 / (3.3u*500k*19)

= 1.653A



3.3 Volt +/- 5%
Fs=500K
TDC :4.6A (Imax)
OCP minimum 6A

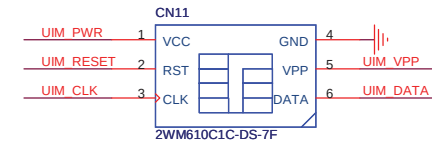




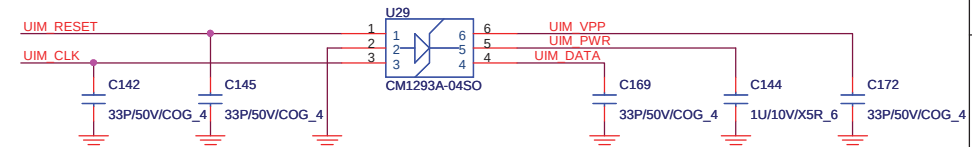


PROJECT : QR1

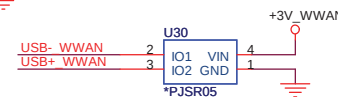
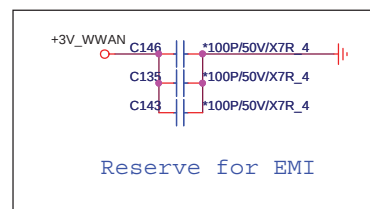
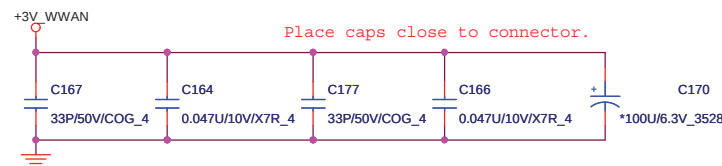
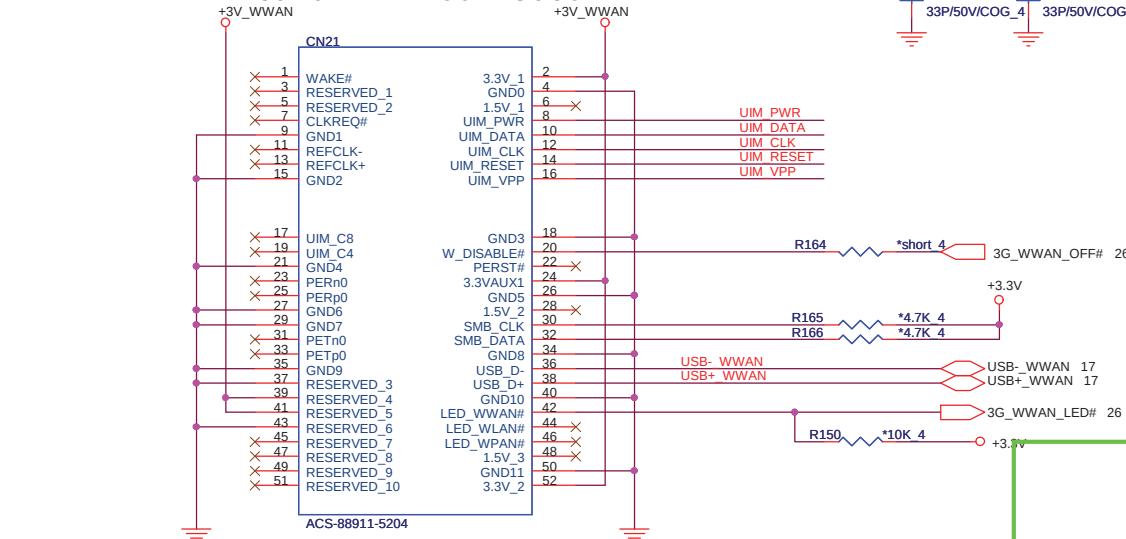
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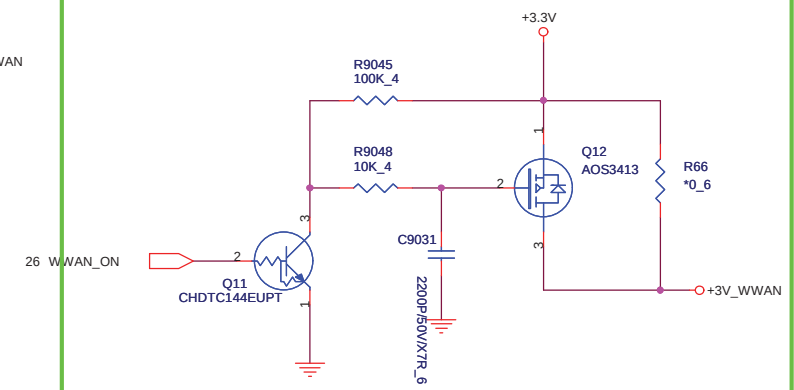
Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible



MiniCard WWAN connector



Modified by Kevin 9/23

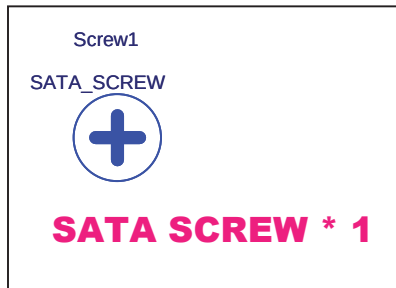
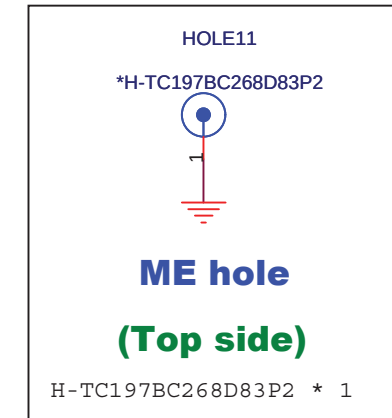
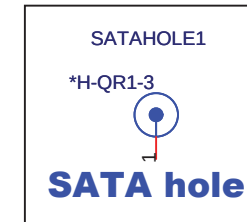
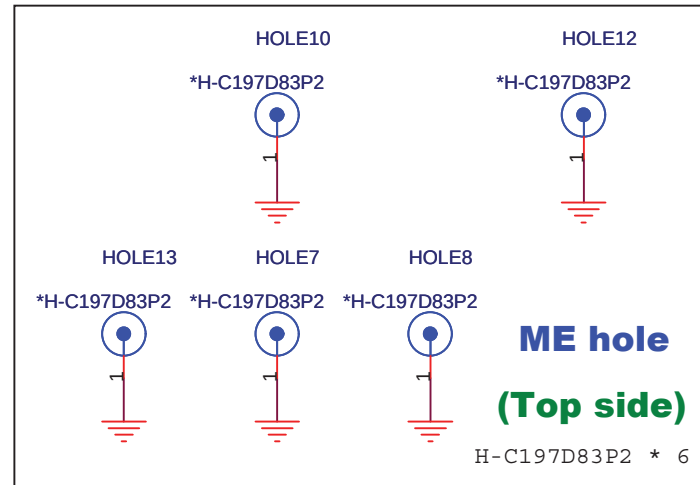
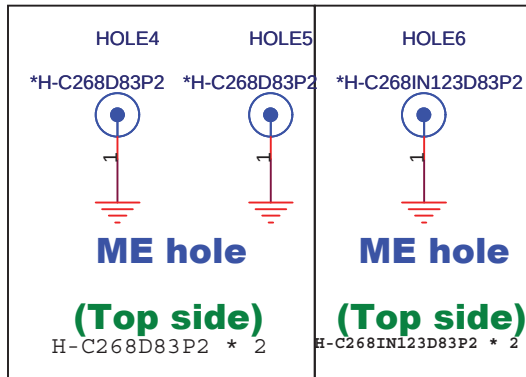
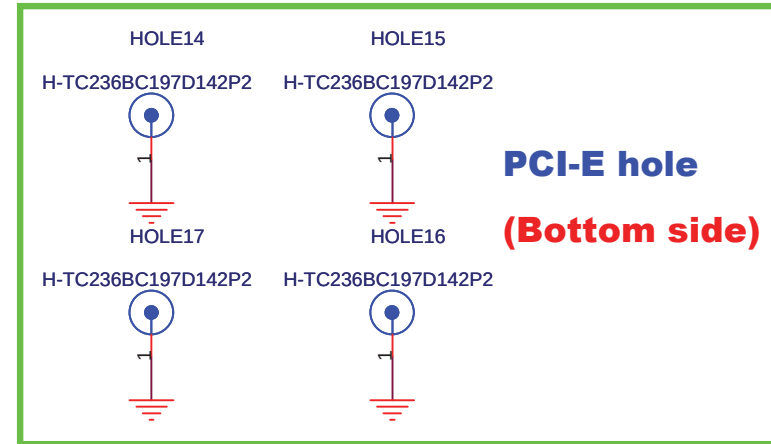
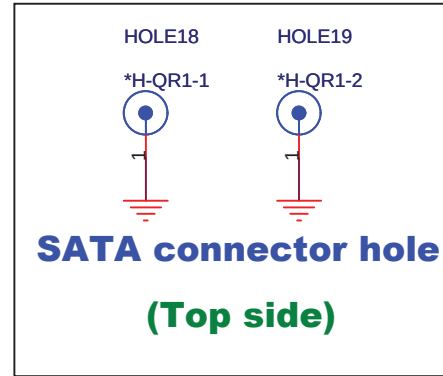
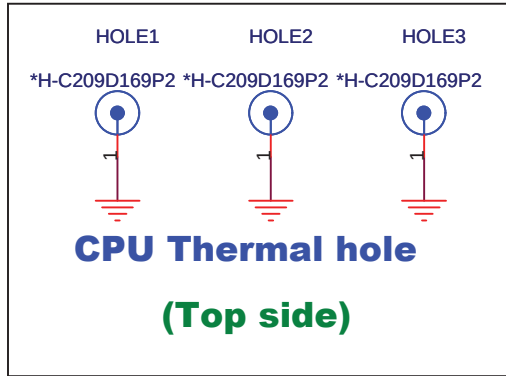


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PROJECT : QR1

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Screw Hole



Title		
<Title>		
Size A	Document Number Screw hole / EMI	Rev 1A
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1. Modified MAIND circuit (to separate MAIN_ON) -P28
2. Modified SUS_ON to SUSD circuit. - p28
3. Added PWRBUT pull high 47KR - p28
4. From 10KR to 100KR for battery internal pull low 5KR issue.
5. Modified WLAN ON/OFF circuit.
R9035 install 100KR, R65 N/C
6. Remove R17,R19,R16 and U7 for USB Hub issue.(Modified USB Hub only 2 port be workable) -P17
7. Modified power plane from VCC18MEM to +1.8V(Modified 築築issue) -P23
8. Remove R90 R74 for LVDS back light on -P12
9. Fixed SMBus data and clock pin define. - P26
10. Audio net: SENSEA added 100pf for VT2002 by Kevin (09/21) - P24
11. Audio JDREF added 100pf for VT2002 by Kevin (09/21) - P24
12. Update USB port setting for wake up function (09/23) - P
13. Install for cardread functcion - P22
14. DPRSTP# added pull high for C4 CPU VID function -P6
15. Remove resistor for Over Current Pin by Kevin 10/2 - P17

Update bug for VER.C.

1. ENE "AGATE20" and "kb_reset" added diode for electric leakage by Kevin 10/16 - P26



Quanta Computer Inc.

PROJECT : QR1

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