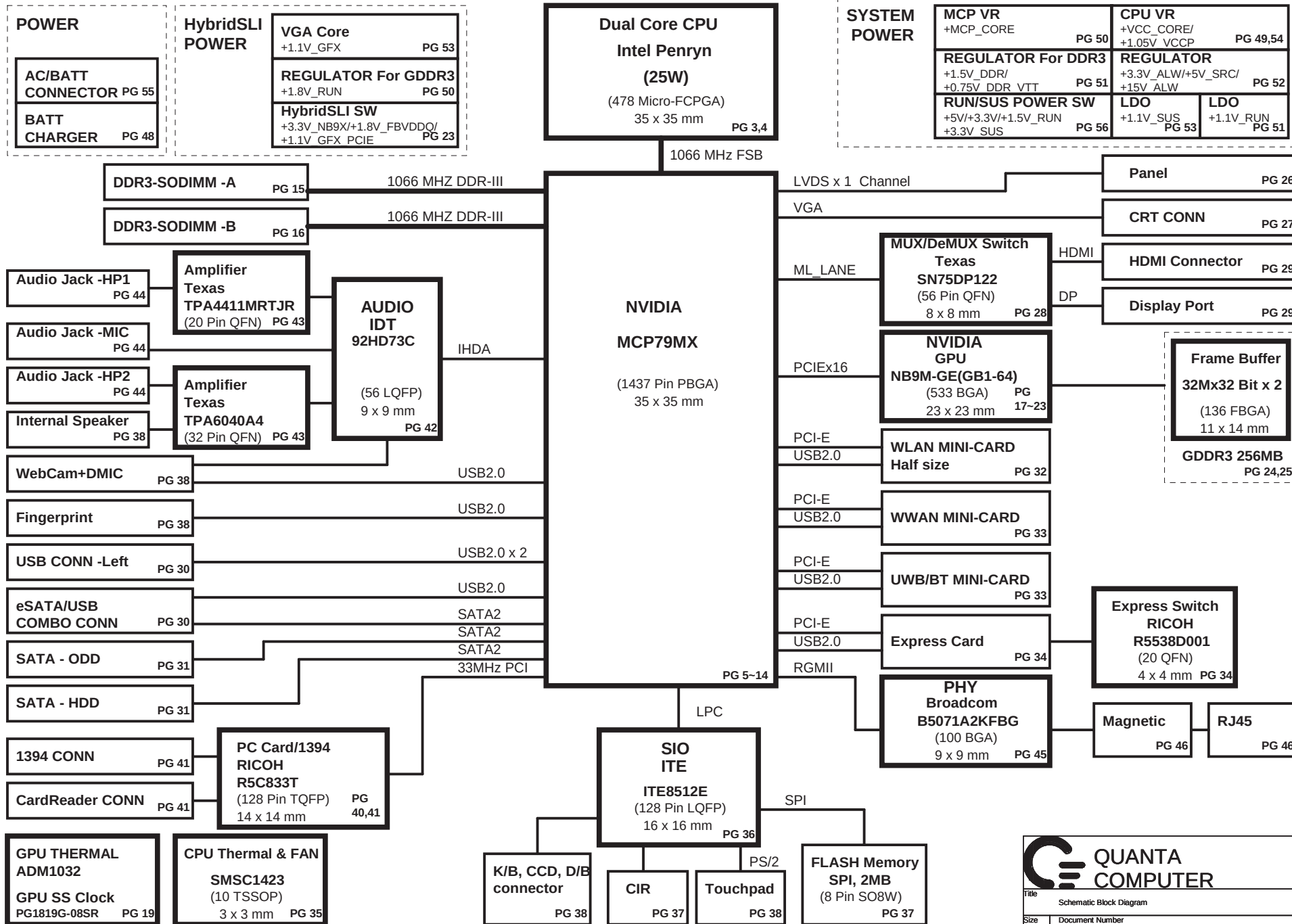


IM3/IM3B M/B PCB REV:G

<http://hobi-elektronika.net>

IM3 (Jolie) Discrete 256M & UMA Block Diagram

VER : 3A

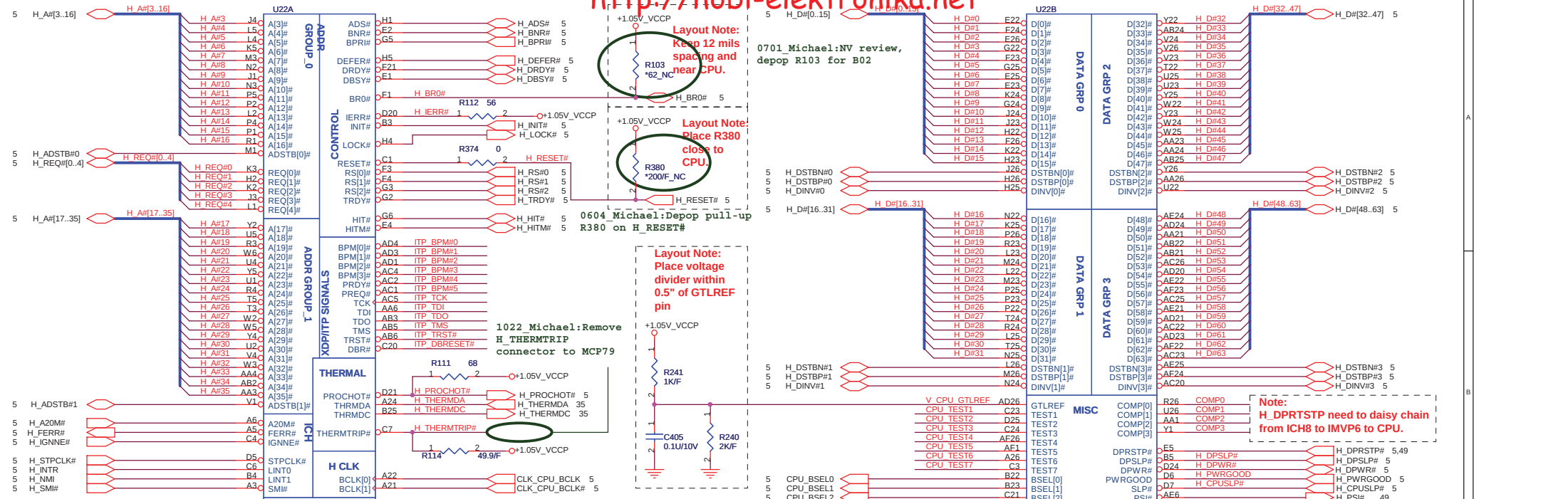


QUANTA
COMPUTER

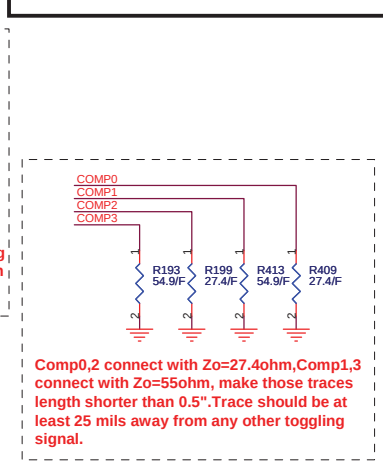
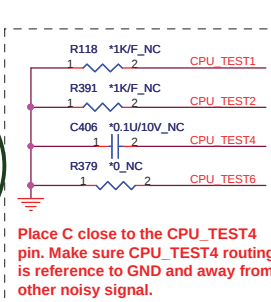
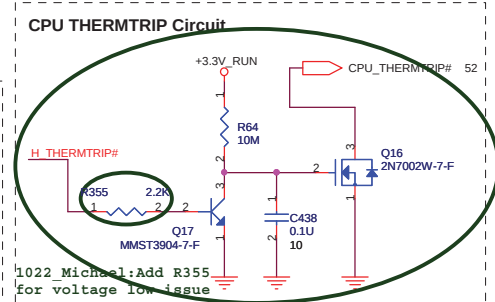
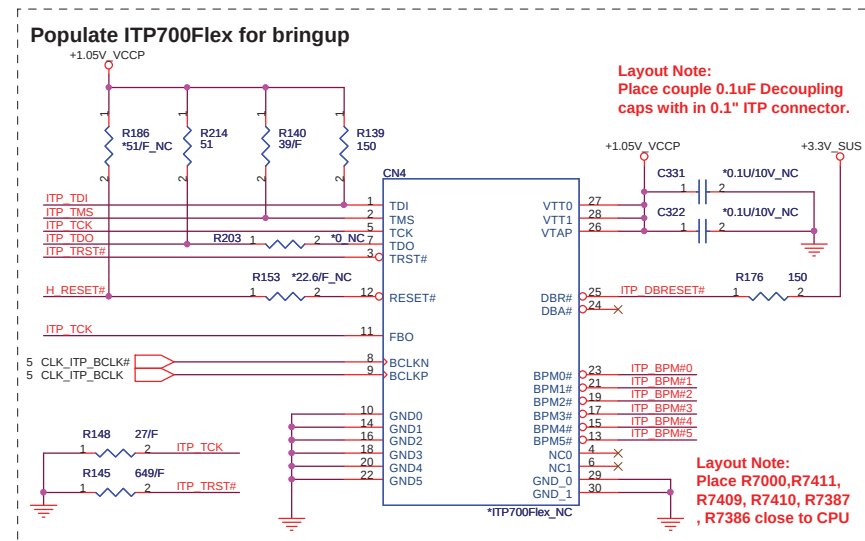
INDEX

Page#	Description
1	Block Diagram
2	Front Page
3-4	Penryn (CPU)
5-14	MCP79 (NB+SB+CKG)
15-16	DDRIII SO-DIMM(204P)
17-25	VGA (NB9M)
26	LCD CONN
27	CRT CONN
28	DeMux SW (SN75DP122)
29	HDMI & DP CONN
30	USB & eSATA & TV
31	HDD & ODD (SATA)
32	MINI-CARD (WLAN)
33	MINI-CARD (WPAN,WWAN)
34	Express Card
35	FAN & Thermal
36	SIO (ITE8512)
37	Flash ROM/ RTC/ CIR
38	KB/ CCD/ User Interface
39	LED
40-41	Card Reader & 1394
42-43	Audio CODEC(92HD73C)/ AMP/ Jack/ Subwoofer
45-46	LAN PHY (B5071)/ RJ45/ Transformer
47	System Reset Circuit
48	CHARGER (MAX8731)
49	CPU Core (ISL6266)
50	MCP79 CORE/ 1.05V (MAX17007)
51	DDR 1.5V/ 1.1V (TPS51116)
52	SYS 5V/ 3V(MAX17020)
53	NB9 Core (MAX8632)
54	GRAM_1.8V (TPS51117)
55	DCIN,Batt
56	RUN POWER SW
57	Debug Port (Mini PCI)
58	PAD & SCREW

Power Rail	Control Signal	S0	S3	S4	S5	G3
+PWR_SRC	N/A	V	V	V	V	
+0.75V_DDR_VTT	RUN_ON	V				
+1.05V_VCCP	CPUVDD_EN	V				
+1.1V_GFX	+3.3V_NB9X	V				
+1.1V_GFX_PCIE	MXM_PWR_EN	V				
+1.1V_RMGT	SLP_RMGT#	V	V			
+1.1V_RUN	RUN_ON	V				
+1.1V_SUS	+3.3V_SUS	V	V			
+1.5V_RUN	RUN_ON	V				
+1.5V_DDR	SIO_SLP_S5#	V	V			
+1.8V_FBVDDQ	NB9_CORE_PWRGD	V				
+1.8V_RUN	RUN_ON	V				
+15V_ALW	+5V_ALW	V	V			
+3.3V_ALW	+5V_ALW2	V	V	V	V	
+3.3V_NB9X	MXM_PWR_EN	V				
+3.3V_RMGT	SLP_RMGT#	V	V			
+3.3V_RUN	RUN_ON	V				
+3.3V_SUS	SUS_ON	V	V			
+5V_ALW	5V_ALW_ON	V	V			
+5V_ALW2	+PWR_SRC	V	V	V	V	
+5V_HDD	HDDC_EN	V				
+5V_MOD	MODC_EN	V				
+5V_RUN	RUN_ON	V				
+GFX_PWR_SRC	RUN_ON	V				
+LCDVCC	EN_LCDVCC	V				
+MCP_CORE	RUN_ON	V				
+NB9_CORE	+3.3V_NB9X	V				
+RTC_CELL	N/A	V	V	V	V	V
+VCC_CORE	1.05V_VCCP_PWRGD	V				
+USB_RIGHT_PWR	USB_SIDE_EN#	V	V			
+USB_LEFT_PWR	USB_BACK_EN#	V	V			

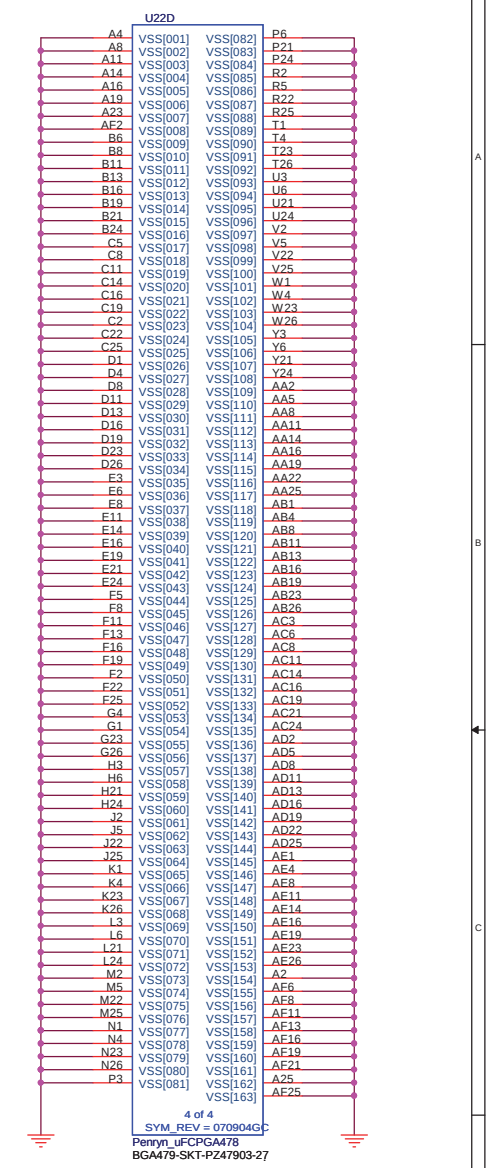
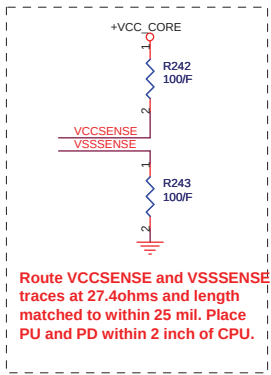
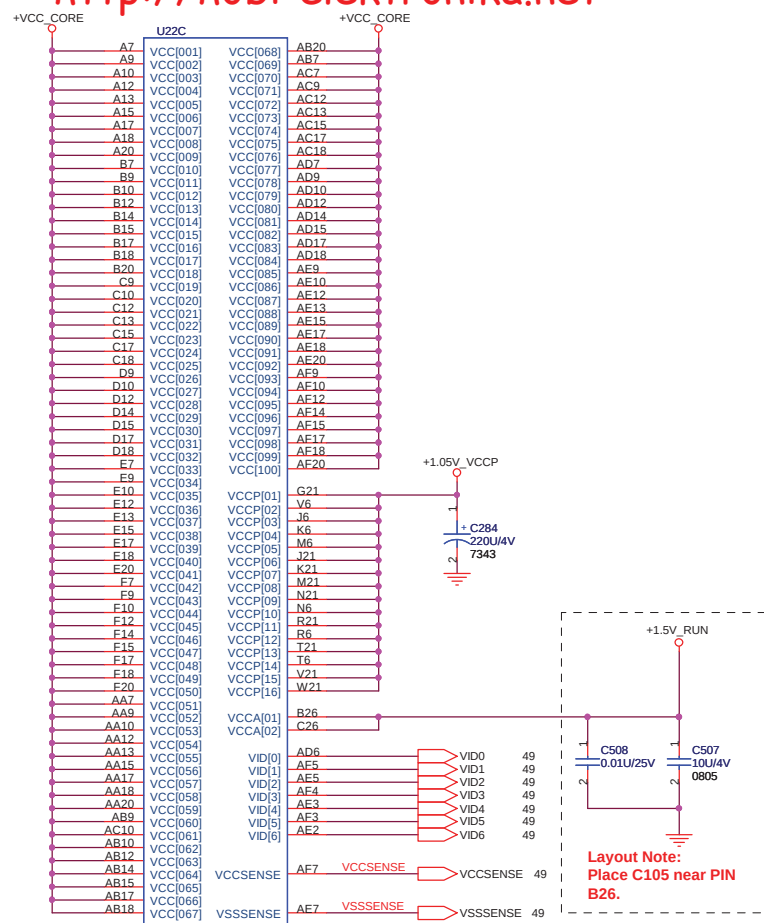
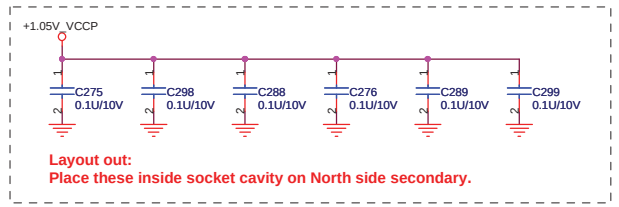
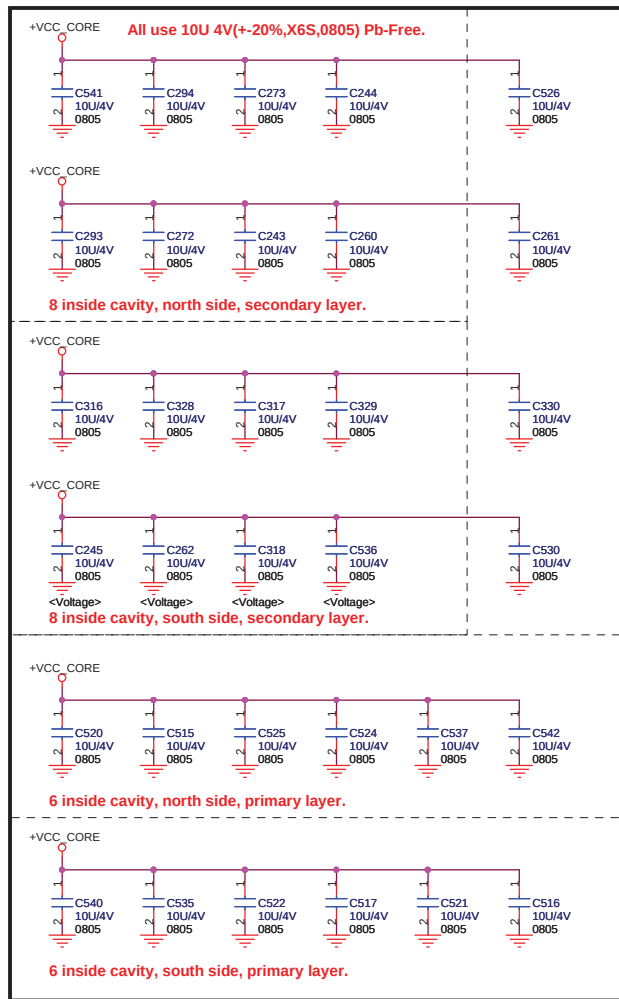


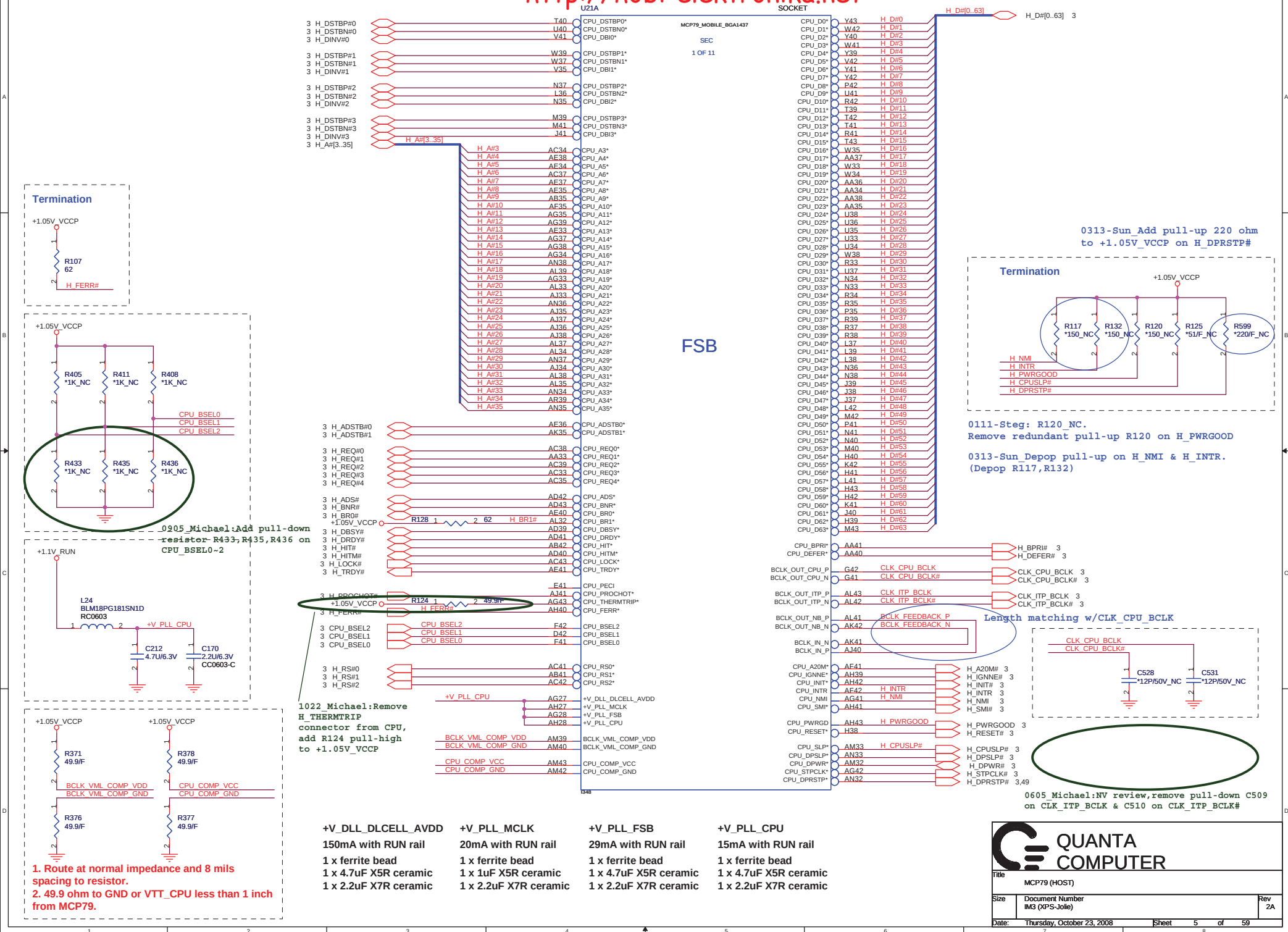
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

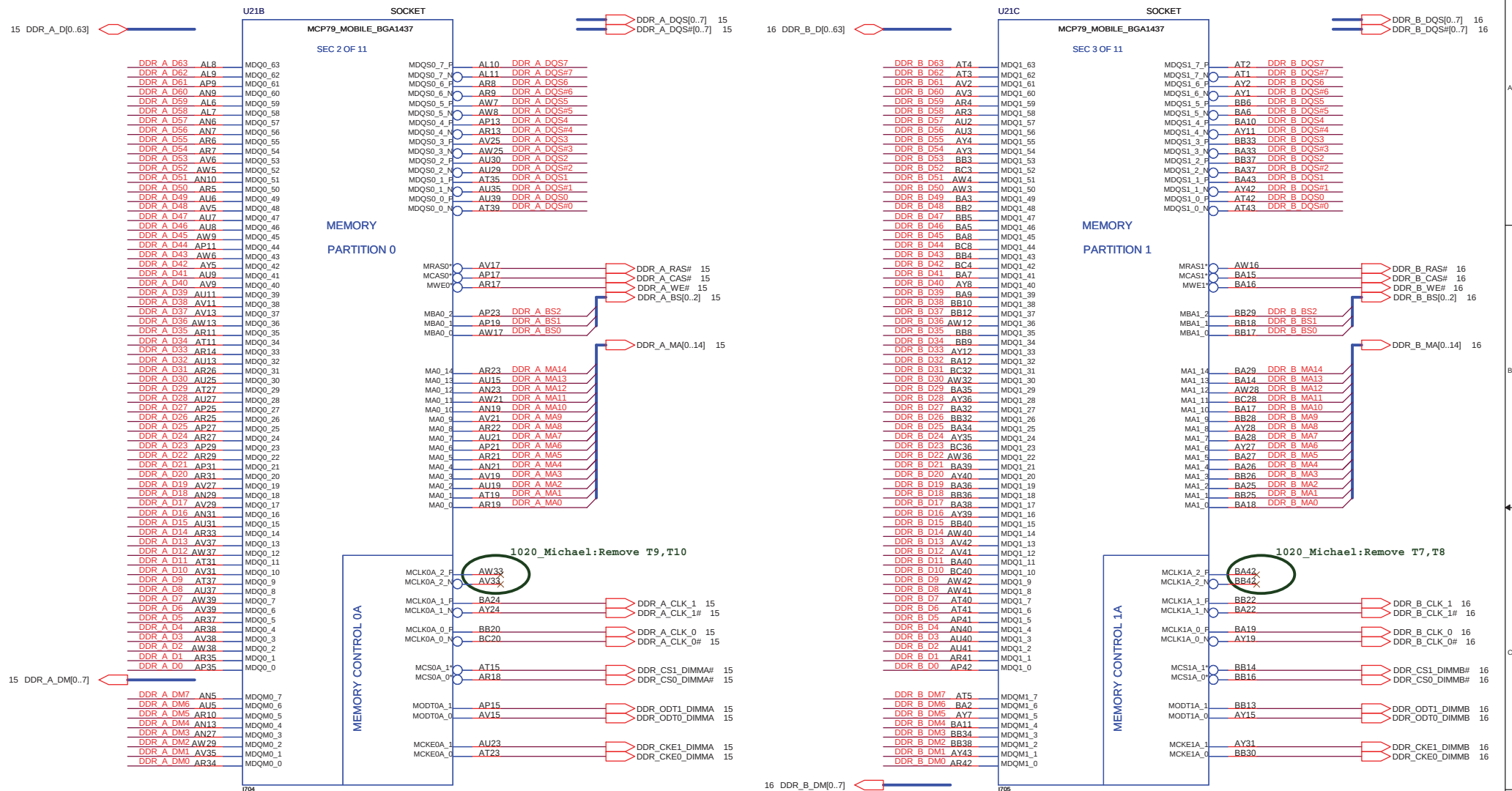


ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of
TMS	39 ohm +/- 5%	VTT	Within 2.0" of
TRST#	680 ohm +/- 5%	GND	Within 2.0" of
TCK	27 ohm +/- 5%	GND	Within 2.0" of
TDO	Open	VTT	Within 2.0" of
ITP_EN	R268 Depop	+3VRUN	Close to CK410M

 QUANTA COMPUTER	
Title: Penryn Processor (HOST BUS)	
Size	Document Number IM3 (XPS-Jolie)
Date: Thursday, October 23, 2008	Sheet 3 of 59
Rev 2A	







Layout Notice:
Memory Data Signal Group
MCP79 BGA Breakout (<175ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout: Route at 40 ohm impedance and 4x(Microstrip) or 3x(Stripline) dielectric spacing.
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

Memory Data Strobes
Route strobes differentially at 66 ohm impedance (42 ohm SE) and 5x dielectric height spacing to other signals.

Memory Clock Signal Group
MCP79 BGA Breakout (<90ps): Route at 50 ohm SE / 100 ohm differential impedance.
After Breakout: Route at 40 ohm SE / 66 ohm differential impedance and 5x dielectric height spacing to other signals.

Memory Address/Command/Control Signal Group
MCP79 BGA Breakout (<90ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout: Route at 40 ohm impedance and 2x dielectric height to other signals and 3x dielectric spacing to other non-associated signals.
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

+V_VPLL
39mA with RUN rail

+V_PLL_XREF_XS
17mA with RUN rail

+V_PLL_CORE
19mA with RUN rail

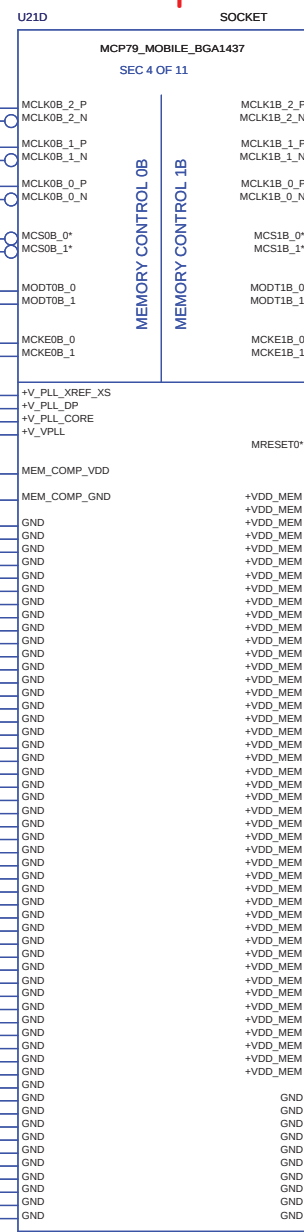
+V_PLL_DP
12mA with RUN rail

1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

0910 Michael:Follow NV check list
add 4.7U C738

0102-Sun_Change MEM_COMP_VDD &
MEM_COMP_GND setting
MEM_COMP_VDD from +1.5V_RUN to GND &
MEM_COMP_GND from GND to +1.5V_RUN

Layout Notice:
1. 40.2 +/-1% ohm to +1.5V_SUS less than 1 inch
from MCP79 for DDR3.
2. Route with 7 mils trace width and 8 mils
spacing to termination resistor.



0605_Michael:Remove 0ohm R93

4.3A with ALW rail for S0
318mA for S0 Idle
1 x 2.2uF ceramic
12 x 0.1uF X7R ceramic

0918 Michael:Follow NV checklist
change value from 4.7U to 2.2U

1217- AC Stitch Cap

17 PCIE_MRX_GTX_P[0..15]
17 PCIE_MRX_GTX_N[0..15]

PCIE Layout Notice:
MCP79 BGA Breakout (<27ps):
Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout:
Route at 50 Signal end and 90 ohm differential.
Inter-pair spacing 4x (Microstrip) dielectric height spacing 3x (Stripline) dielectric height spacing.

0605 Michael:Remove 0ohm
R185 on MXM_ON#
R433,R435,168 pull-down to GND
R177 on PE_RESET_MXM#
R458 on PCIE_WAKE#

Express Card

WLAN

UWB/BT

WWAN

34 CARD_CLK_REQ#

34,36 EXPRCDR_PWREN#

32 MINICLK_REQ#

33 MINI2CLK_REQ#

33 MINI3CLK_REQ#

17 PE_RESET_MXM#

38 KB_LED_DET

32,33,34 PCIE_WAKE#

34 PCIE_RX0_P

34 PCIE_RX0_N

32 PCIE_RX1_P

32 PCIE_RX1_N

33 PCIE_RX2_P

33 PCIE_RX2_N

33 PCIE_RX3_P

33 PCIE_RX3_N

34 PCIE_TX0_P

34 PCIE_TX0_N

32 PCIE_TX1_P

32 PCIE_TX1_N

33 PCIE_TX2_P

33 PCIE_TX2_N

33 PCIE_TX3_P

33 PCIE_TX3_N

34 PCIE_TX4_P

34 PCIE_TX4_N

32 PCIE_TX5_P

32 PCIE_TX5_N

33 PCIE_TX6_P

33 PCIE_TX6_N

33 PCIE_TX7_P

33 PCIE_TX7_N

33 PCIE_TX8_P

33 PCIE_TX8_N

33 PCIE_TX9_P

33 PCIE_TX9_N

33 PCIE_TX10_P

33 PCIE_TX10_N

32 PCIE_TX11_P

32 PCIE_TX11_N

33 PCIE_TX12_P

33 PCIE_TX12_N

33 PCIE_TX13_P

33 PCIE_TX13_N

33 PCIE_TX14_P

33 PCIE_TX14_N

33 PCIE_TX15_P

33 PCIE_TX15_N

34 PCIE_TX16_P

34 PCIE_TX16_N

32 PCIE_TX17_P

32 PCIE_TX17_N

33 PCIE_TX18_P

33 PCIE_TX18_N

33 PCIE_TX19_P

33 PCIE_TX19_N

33 PCIE_TX20_P

33 PCIE_TX20_N

33 PCIE_TX21_P

33 PCIE_TX21_N

33 PCIE_TX22_P

33 PCIE_TX22_N

33 PCIE_TX23_P

33 PCIE_TX23_N

33 PCIE_TX24_P

33 PCIE_TX24_N

33 PCIE_TX25_P

33 PCIE_TX25_N

33 PCIE_TX26_P

33 PCIE_TX26_N

33 PCIE_TX27_P

33 PCIE_TX27_N

33 PCIE_TX28_P

33 PCIE_TX28_N

33 PCIE_TX29_P

33 PCIE_TX29_N

33 PCIE_TX30_P

33 PCIE_TX30_N

33 PCIE_TX31_P

33 PCIE_TX31_N

33 PCIE_TX32_P

33 PCIE_TX32_N

33 PCIE_TX33_P

33 PCIE_TX33_N

33 PCIE_TX34_P

33 PCIE_TX34_N

33 PCIE_TX35_P

33 PCIE_TX35_N

33 PCIE_TX36_P

33 PCIE_TX36_N

33 PCIE_TX37_P

33 PCIE_TX37_N

33 PCIE_TX38_P

33 PCIE_TX38_N

33 PCIE_TX39_P

33 PCIE_TX39_N

33 PCIE_TX40_P

33 PCIE_TX40_N

33 PCIE_TX41_P

33 PCIE_TX41_N

33 PCIE_TX42_P

33 PCIE_TX42_N

33 PCIE_TX43_P

33 PCIE_TX43_N

33 PCIE_TX44_P

33 PCIE_TX44_N

33 PCIE_TX45_P

33 PCIE_TX45_N

33 PCIE_TX46_P

33 PCIE_TX46_N

33 PCIE_TX47_P

33 PCIE_TX47_N

33 PCIE_TX48_P

33 PCIE_TX48_N

33 PCIE_TX49_P

33 PCIE_TX49_N

33 PCIE_TX50_P

33 PCIE_TX50_N

33 PCIE_TX51_P

33 PCIE_TX51_N

33 PCIE_TX52_P

33 PCIE_TX52_N

33 PCIE_TX53_P

33 PCIE_TX53_N

33 PCIE_TX54_P

33 PCIE_TX54_N

33 PCIE_TX55_P

33 PCIE_TX55_N

33 PCIE_TX56_P

33 PCIE_TX56_N

33 PCIE_TX57_P

33 PCIE_TX57_N

33 PCIE_TX58_P

33 PCIE_TX58_N

33 PCIE_TX59_P

33 PCIE_TX59_N

33 PCIE_TX60_P

33 PCIE_TX60_N

33 PCIE_TX61_P

33 PCIE_TX61_N

33 PCIE_TX62_P

33 PCIE_TX62_N

33 PCIE_TX63_P

33 PCIE_TX63_N

33 PCIE_TX64_P

33 PCIE_TX64_N

33 PCIE_TX65_P

33 PCIE_TX65_N

33 PCIE_TX66_P

33 PCIE_TX66_N

33 PCIE_TX67_P

33 PCIE_TX67_N

33 PCIE_TX68_P

33 PCIE_TX68_N

33 PCIE_TX69_P

33 PCIE_TX69_N

33 PCIE_TX70_P

33 PCIE_TX70_N

33 PCIE_TX71_P

33 PCIE_TX71_N

33 PCIE_TX72_P

33 PCIE_TX72_N

33 PCIE_TX73_P

33 PCIE_TX73_N

33 PCIE_TX74_P

33 PCIE_TX74_N

33 PCIE_TX75_P

33 PCIE_TX75_N

33 PCIE_TX76_P

33 PCIE_TX76_N

33 PCIE_TX77_P

33 PCIE_TX77_N

33 PCIE_TX78_P

33 PCIE_TX78_N

33 PCIE_TX79_P

33 PCIE_TX79_N

33 PCIE_TX80_P

33 PCIE_TX80_N

33 PCIE_TX81_P

33 PCIE_TX81_N

33 PCIE_TX82_P

33 PCIE_TX82_N

33 PCIE_TX83_P

33 PCIE_TX83_N

33 PCIE_TX84_P

33 PCIE_TX84_N

33 PCIE_TX85_P

33 PCIE_TX85_N

33 PCIE_TX86_P

33 PCIE_TX86_N

33 PCIE_TX87_P

33 PCIE_TX87_N

33 PCIE_TX88_P

33 PCIE_TX88_N

33 PCIE_TX89_P

33 PCIE_TX89_N

33 PCIE_TX90_P

33 PCIE_TX90_N

33 PCIE_TX91_P

33 PCIE_TX91_N

33 PCIE_TX92_P

33 PCIE_TX92_N

33 PCIE_TX93_P

33 PCIE_TX93_N

33 PCIE_TX94_P

33 PCIE_TX94_N

33 PCIE_TX95_P

33 PCIE_TX95_N

33 PCIE_TX96_P

33 PCIE_TX96_N

33 PCIE_TX97_P

33 PCIE_TX97_N

33 PCIE_TX98_P

33 PCIE_TX98_N

33 PCIE_TX99_P

33 PCIE_TX99_N

33 PCIE_TX100_P

33 PCIE_TX100_N

33 PCIE_TX101_P

33 PCIE_TX101_N

33 PCIE_TX102_P

33 PCIE_TX102_N

33 PCIE_TX103_P

33 PCIE_TX103_N

33 PCIE_TX104_P

33 PCIE_TX104_N

33 PCIE_TX105_P

33 PCIE_TX105_N

33 PCIE_TX106_P

33 PCIE_TX106_N

33 PCIE_TX107_P

33 PCIE_TX107_N

33 PCIE_TX108_P

33 PCIE_TX108_N

33 PCIE_TX109_P

33 PCIE_TX109_N

33 PCIE_TX110_P

33 PCIE_TX110_N

33 PCIE_TX111_P

33 PCIE_TX111_N

33 PCIE_TX112_P

33 PCIE_TX112_N

33 PCIE_TX113_P

33 PCIE_TX113_N

33 PCIE_TX114_P

33 PCIE_TX114_N

33 PCIE_TX115_P

33 PCIE_TX115_N

33 PCIE_TX116_P

33 PCIE_TX116_N

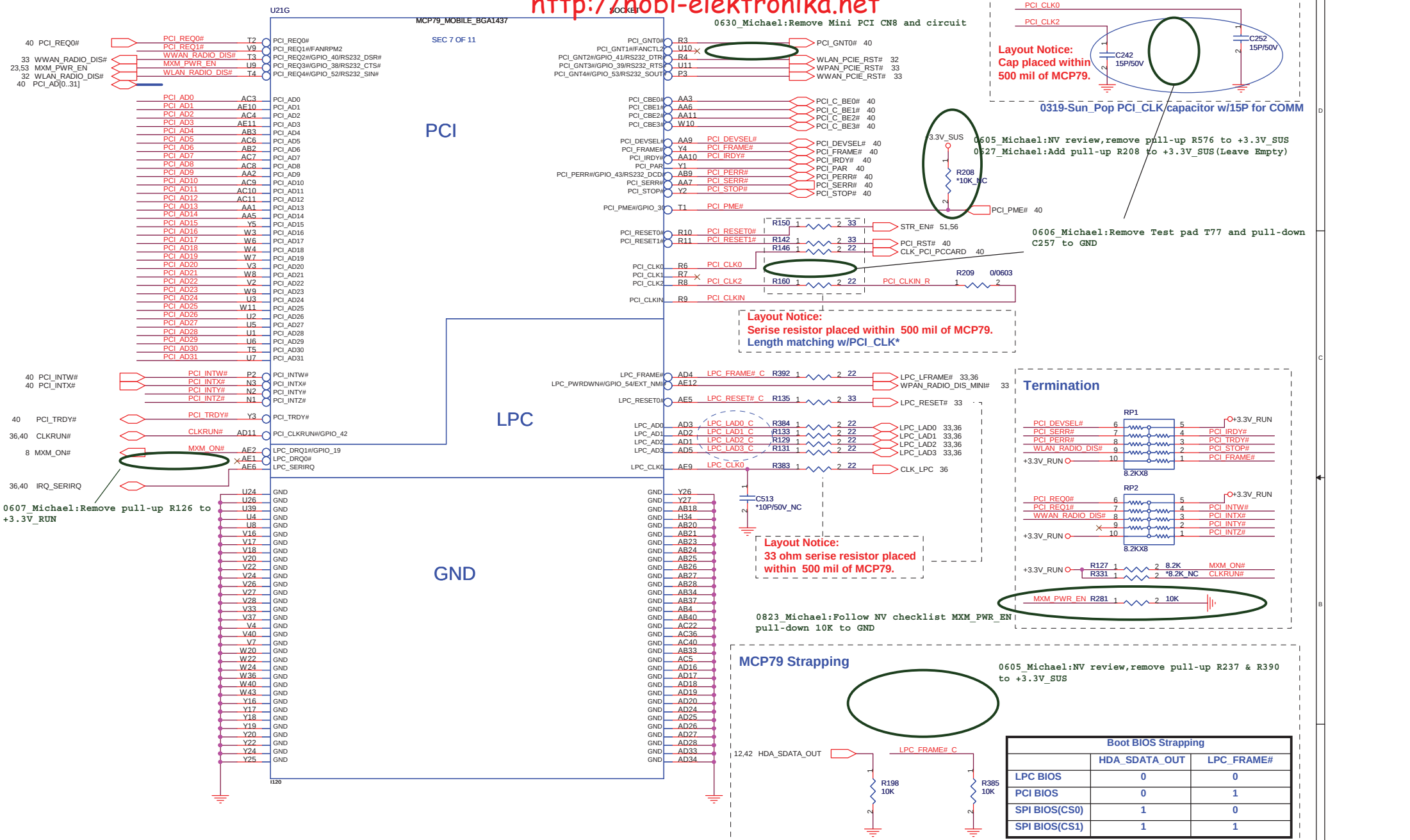
33 PCIE_TX117_P

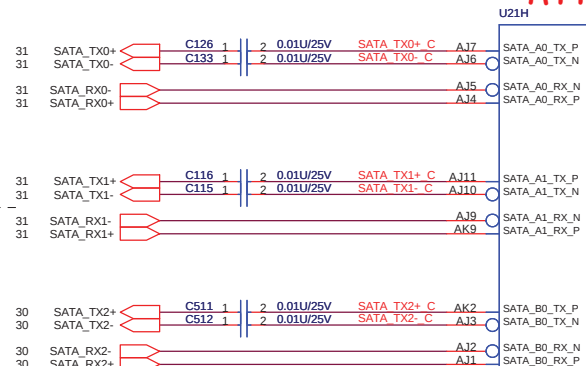
33 PCIE_TX117_N

33 PCIE_TX118_P

</



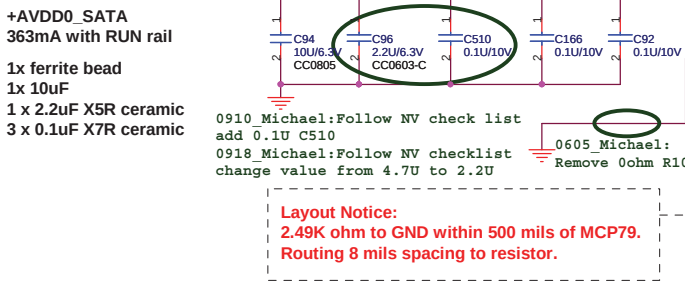
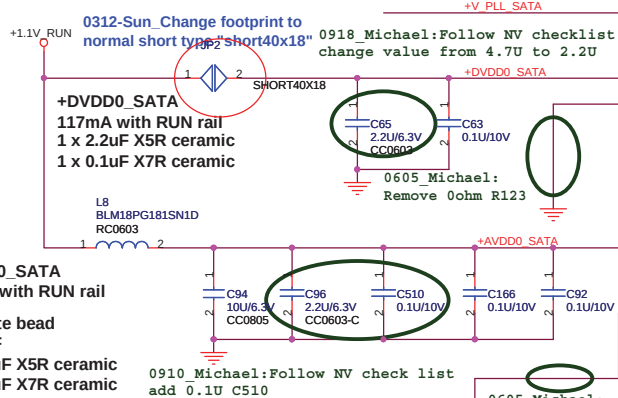
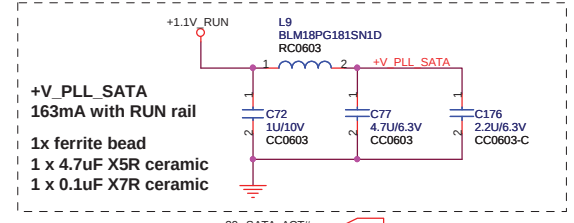




SATA

USB

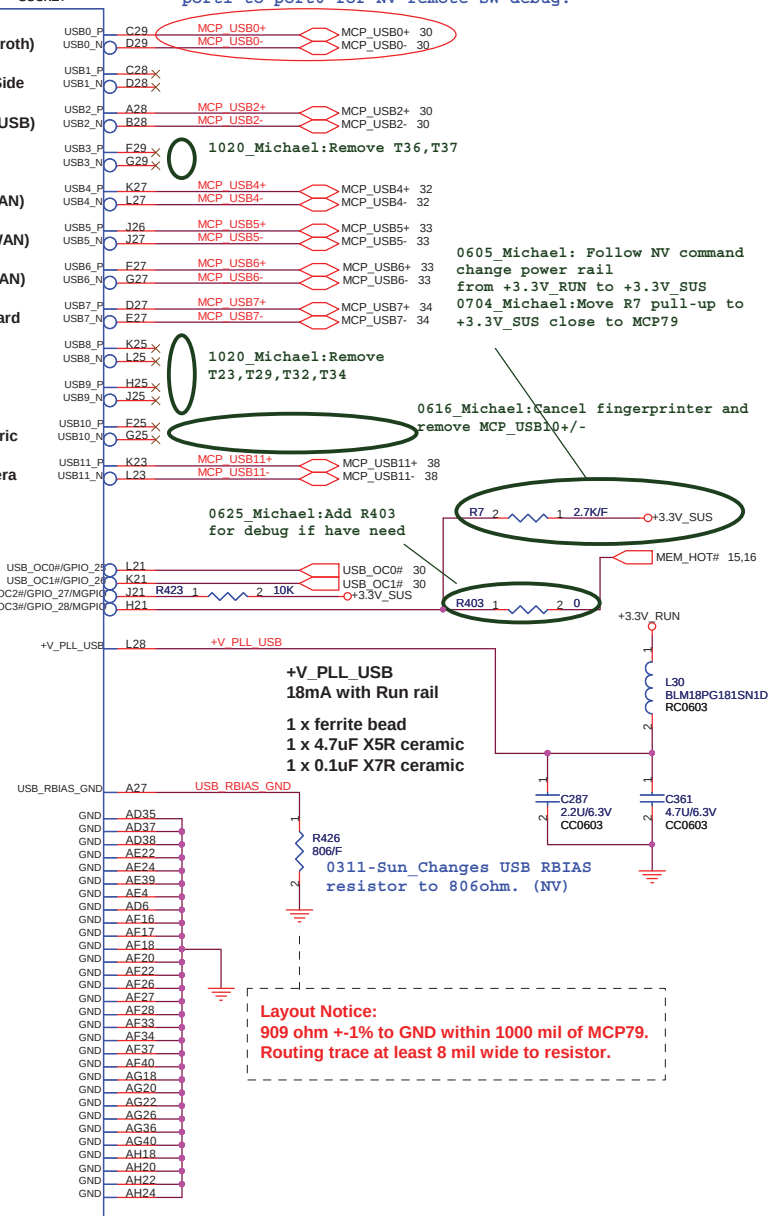
SATA Layout Notice:
BGA Breakout:
Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum brackout distance is 400 mils of MCP79.
BGA Fan-out:
Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA brackout plus Fan-out distance is 500 mils.
After Brackout:
Route at 100 ohm differential impedance (50 ohm SE) and 3x dielectric height spacing to other signals.
TX and RX intra-pair skew for a differential pair is 5 mils.



Layout Notice:
2.49K ohm to GND within 500 mils of MCP79.
Routing 8 mils spacing to resistor.

USB Layout Notice:
BGA Breakout:
Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum brackout distance is 300 mils of MCP79.
BGA Fan-out:
Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA brackout plus Fan-out distance is 400 mils.
After Brackout:
Route at 100 ohm differential impedance (50 ohm SE) and 4x dielectric height spacing (Microstrip) or 2x dielectric height spacing (Stripline) to other signals. Each USB pair must be length matched to within 50 mil.

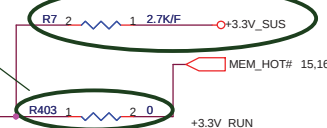
- Left Side (froth)
- Left Side
- Combo (eSATA/USB)
- Mini Card (WLAN)
- Mini Card (WWAN)
- Mini Card (WPAN)
- Express Card
- Biometric
- Camera



0605 Michael: Follow NV command change power rail from +3.3V RUN to +3.3V SUS

0616 Michael: Cancel fingerprinter and remove MCP_USB10+/-

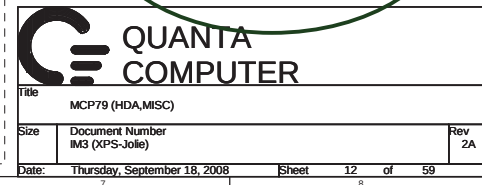
0625 Michael: Add R403 for debug if have need



+V_PLL_USB
18mA with Run rail
1x ferrite bead
1x 4.7uF X5R ceramic
1x 0.1uF X7R ceramic

0311-Sun_Changes USB RBIAS resistor to 806ohm. (NV)

Layout Notice:
909 ohm +-1% to GND within 1000 mil of MCP79.
Routing trace at least 8 mil wide to resistor.



1 x 10uF ceramic
2 x 2.2uF X5R ceramic
3 x 1uF X5R ceramic
3 x 0.22uF X5R ceramic
12 x 0.1uF X7R ceramic

17.756A with RUN rail for S0
2850mA for S0 Idle

+VTT_CPU
1139mA for ALW rail
+VTT_CPUCLK
43mA for ALW rail

1 x 10uF ceramic
1 x 2.2uF X5R ceramic
3 x 0.1uF X7R ceramic

0918 Michael: Follow NV checklist
change value from 10U to 2.2U

0918 Michael: Follow NV checklist
change value from 10U to 2.2U

POWER

0312-Sun_Change footprint to
normal short type "short40x18"

+3.3V_RUN_MCP
450mA with RUN rail

1 x 4.7uF X5R ceramic
4 x 0.1uF X7R ceramic

0312-Sun_Change footprint to
normal short type "short40x18"

+3.3V_DUAL
16mA with ALW rail

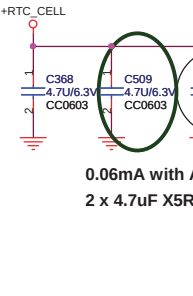
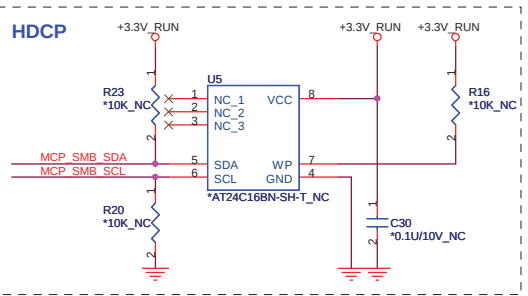
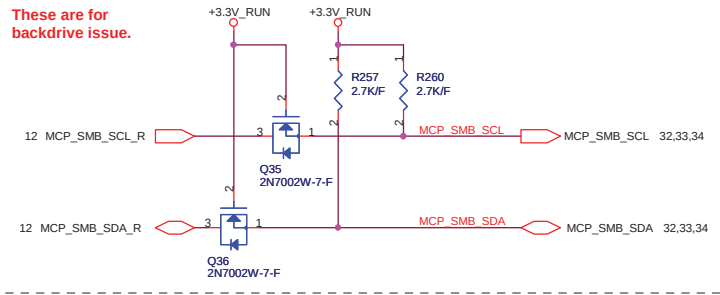
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

+3.3V_DUAL_USB
450mA with ALW rail

1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

+VDD_AUXC
105mA with ALW rail

2 x 0.1uF X7R ceramic

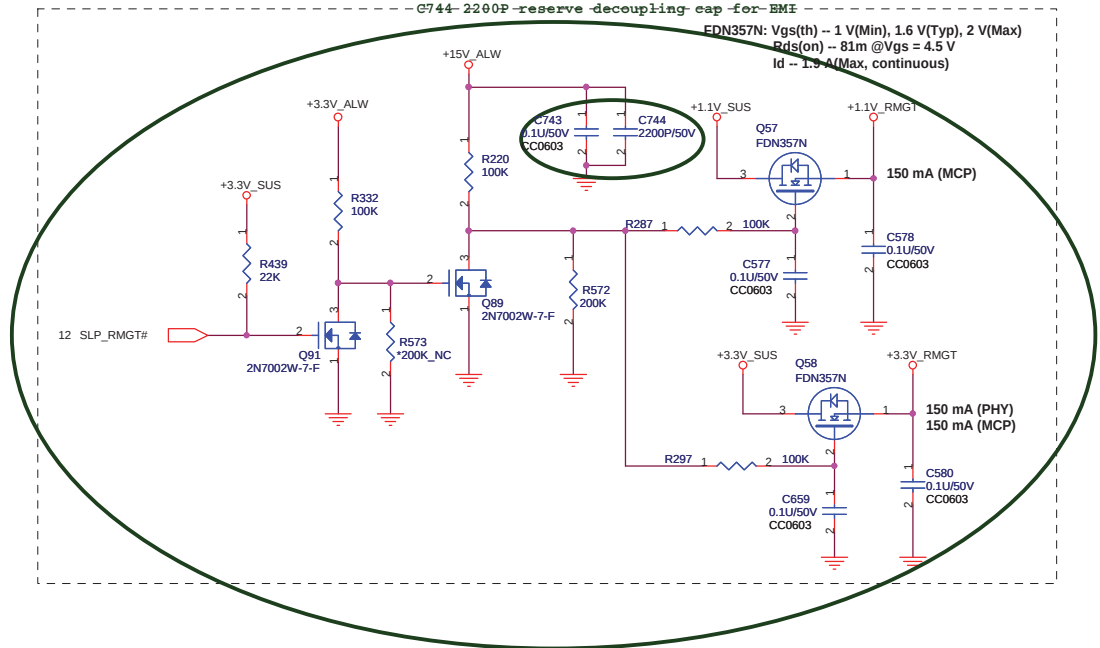
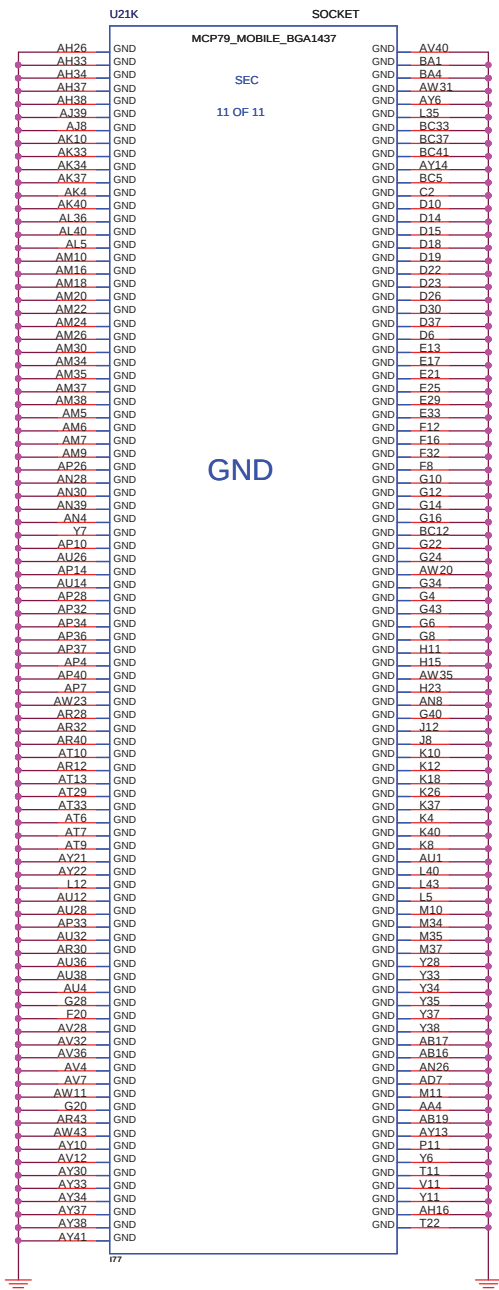


0229-Sun_Add C713 with 0.1U on +VBAT of MCP79
0829 Michael: Follow NV new DG add C509 on +RTC_CELL of MCP79

0.06mA with ALW rail for S0
2 x 4.7uF X5R ceramic



Title		MCP79 (POWER)	
Size	Document Number IM3 (XPS-Jolie)		Rev 2A
Date:	Friday, September 19, 2008	Sheet 13 of 59	



0229-Sun 1.1V_RMGT & +3.3V_RMGT MOSFET Vgs aren't enough issue, modify circuit reference NV CRB (Del JP11,JP12)

Change Q57 from SI2304BDS-T1-E3 to FDN357N, Q58 from SI2304BDS-T1-E3 to SI2301BDS-T1-E3 Add Q89 with 2N7002,R591 with 10K)

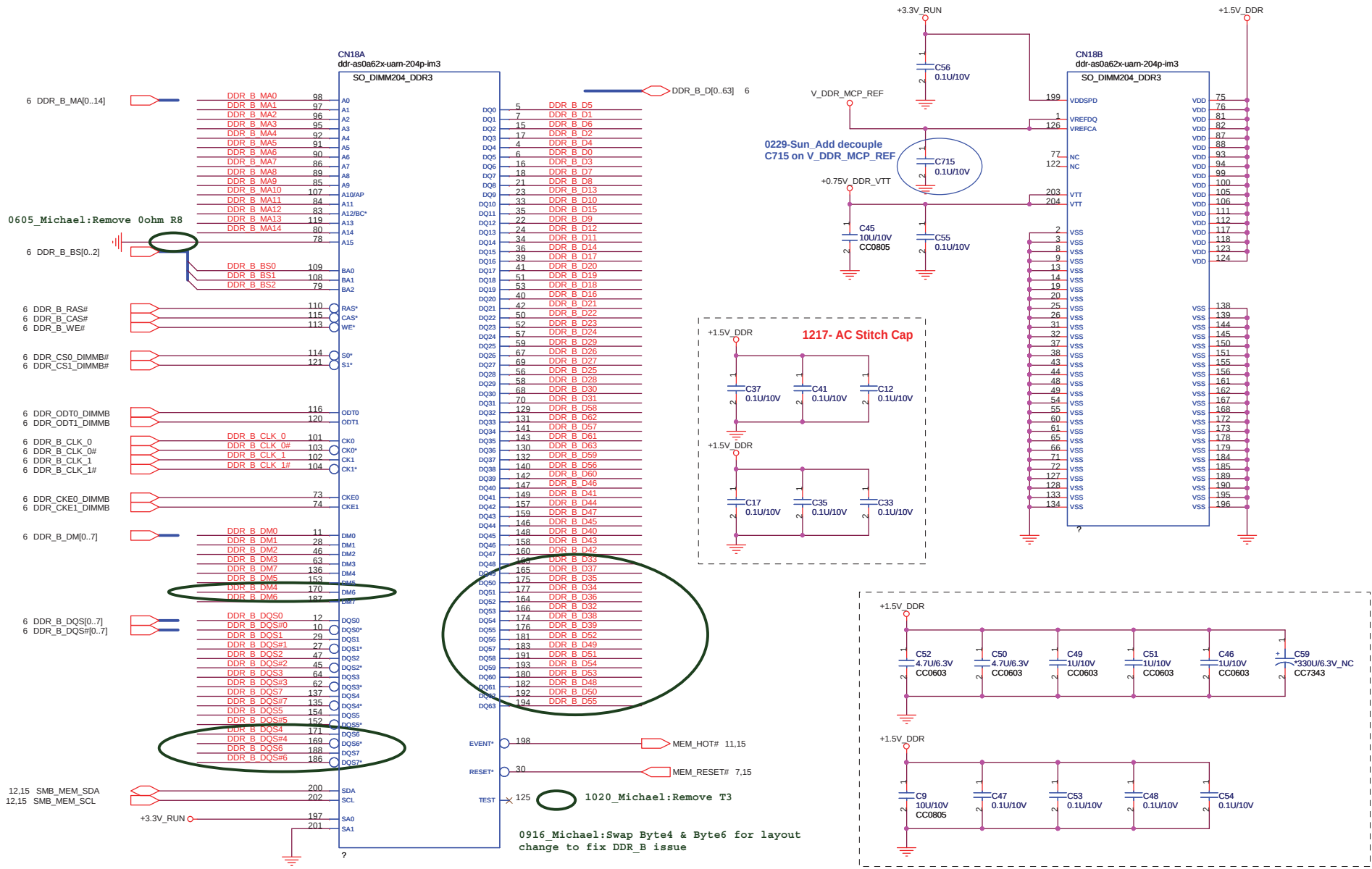
0825 Michael: Change Q58 type from SI2301BDS to FDN357N and add MOS 2N7002W-7-F,R&C for +1.1V_RMGT and +3.3V_RMGT power low issue



Title			MCP79 (GND)
Size	Document Number	Rev	
	IM3 (XP'S-Jolie)	2A	
Date:	Tuesday, October 26, 2008	Sheet	14 of 59



Title			
DDR3 SO-DIMM (204P)			
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	2A	
Date:	Monday, October 20, 2008	Sheet	15 of 59



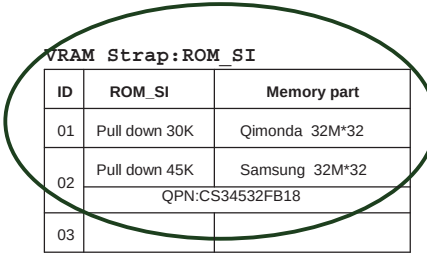
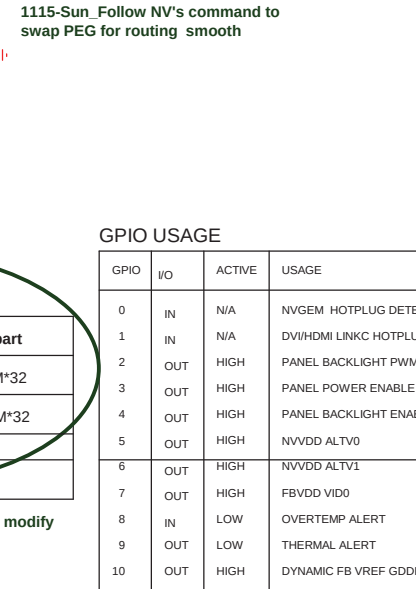
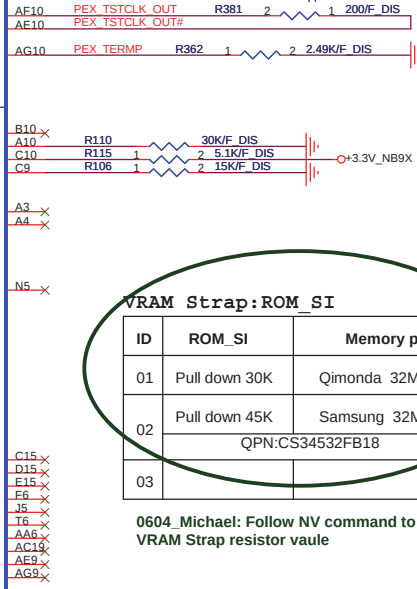
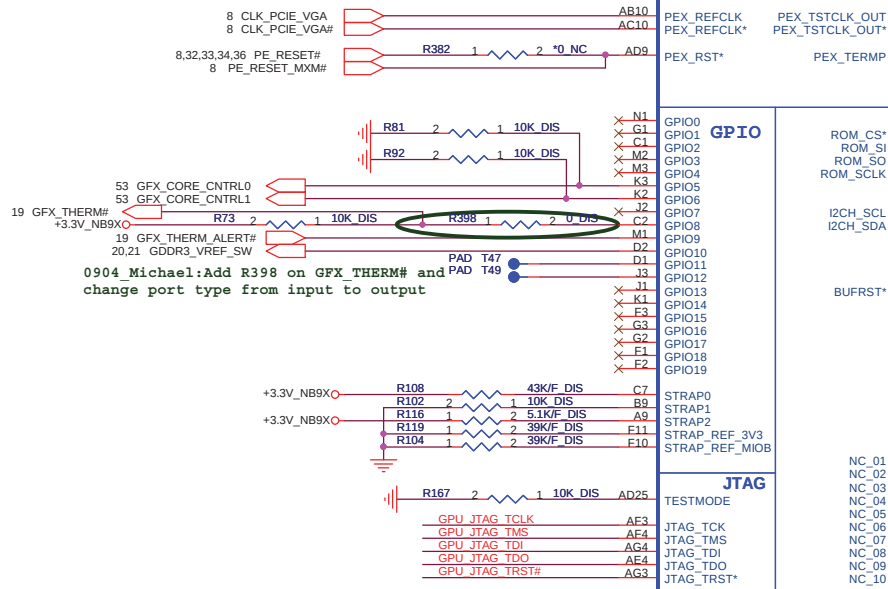
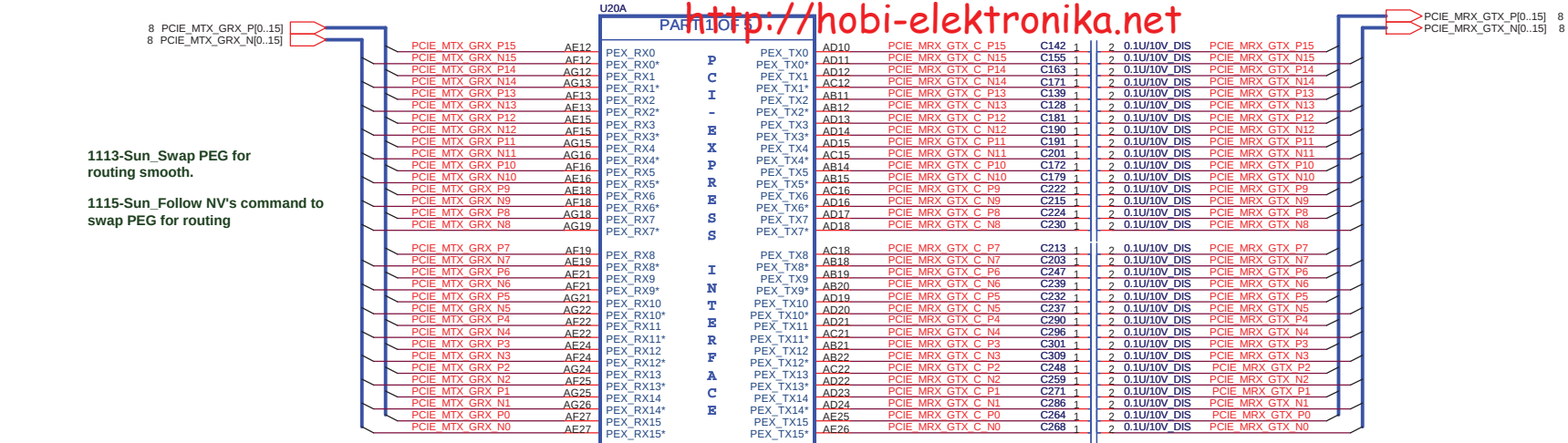
For EMI Reserved

DDR_B_CLK_1	R9	1	2	*200/F NC	DDR_B_CLK_1#
DDR_B_CLK_0	R11	1	2	*200/F NC	DDR_B_CLK_0#



1113-Sun_Swap PEG for routing smooth.

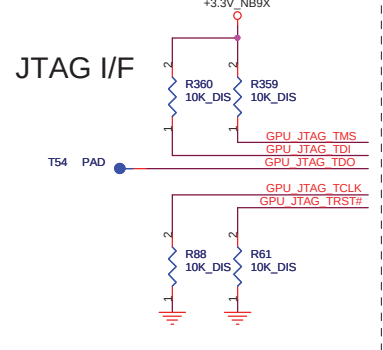
1115-Sun_Follow NV's command to swap PEG for routing



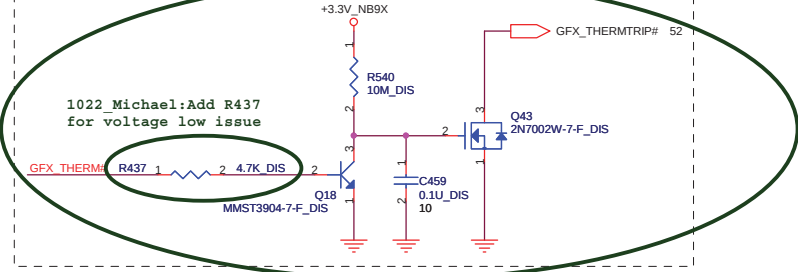
GPIO USAGE

GPIO	I/O	ACTIVE	USAGE	Used
0	IN	N/A	NVGEM HOTPLUG DETECT	
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT	
2	OUT	HIGH	PANEL BACKLIGHT PWM	
3	OUT	HIGH	PANEL POWER ENABLE	
4	OUT	HIGH	PANEL BACKLIGHT ENABLE	
5	OUT	HIGH	NVDD ALT0	
6	OUT	HIGH	NVDD ALT1	
7	OUT	HIGH	FBVDD VIDO	
8	IN	LOW	OVERTEMP ALERT	
9	OUT	LOW	THERMAL ALERT	
10	OUT	HIGH	DYNAMIC FB VREF GDDR3 (not used for DDR2)	
11	OUT	HIGH	SLI SYNC0 (not used for GB1-64)	
12	IN	N/A	AC DETECT	
13	OUT	LOW	POWER SUPPLY CONTROL0	
14	OUT	HIGH	POWER SUPPLY CONTROL1	
15	IN	N/A	HPD_E	
16	IN	N/A	DVI_E	No
17	IN	N/A	HDMI_E	No
18	IN	N/A	DVI_F (not used)	No
19	IN	N/A	HDMI_F (not used)	No

Place together.

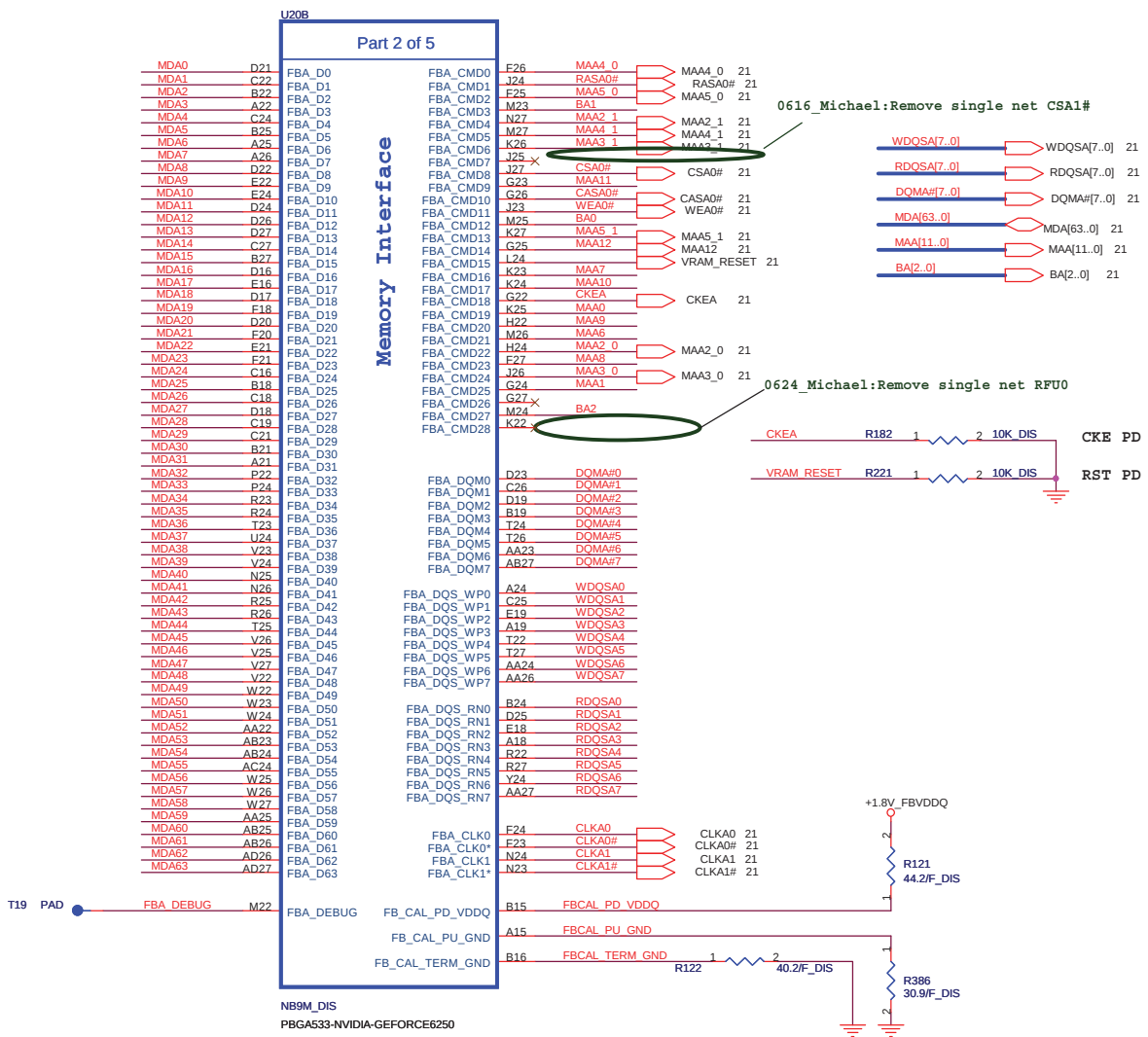


GPU THERMTRIP Circuit



0825 Michael:Modify THERMTRIP circuit,add MOS and CAP





Update as "PUN-03303-001_V01".

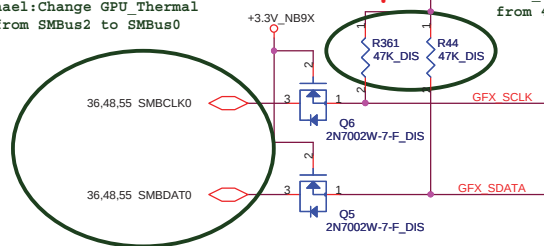
GPU Driver Calibration			
Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ
DDR2	1.8V	30.1	30.1
GDDR3	1.8V	30.9	44.2
GDDR3 DVS	1.8V/1.5V	30.9	44.2

Note: Use only 1% resistors for driver calibration



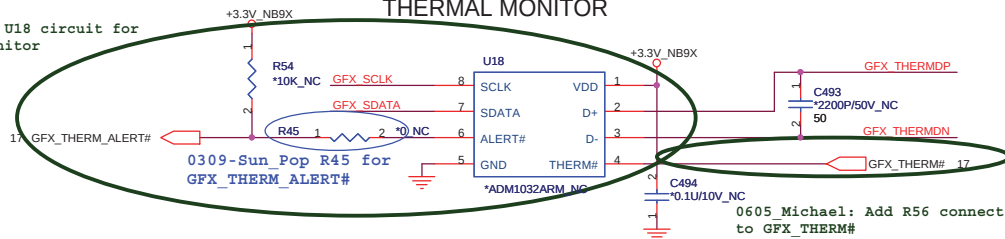

```
0627_Michael:Change GPU_Thermal
control from SMBus2 to SMBus0
```

0807_Change R361, R44
from 4.7k to 47k for battery issue



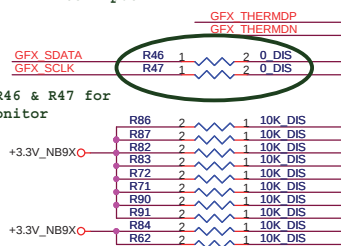
THERMAL MONITOR

0708_Michael:Depop U18 circuit for
nternal thermal monitor

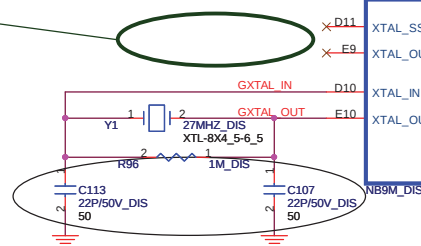


```
0605_Michael: Add R56 connect
to GFX_THERM#
0904_Michael: Remove R56 and
change port type from output
to input
```

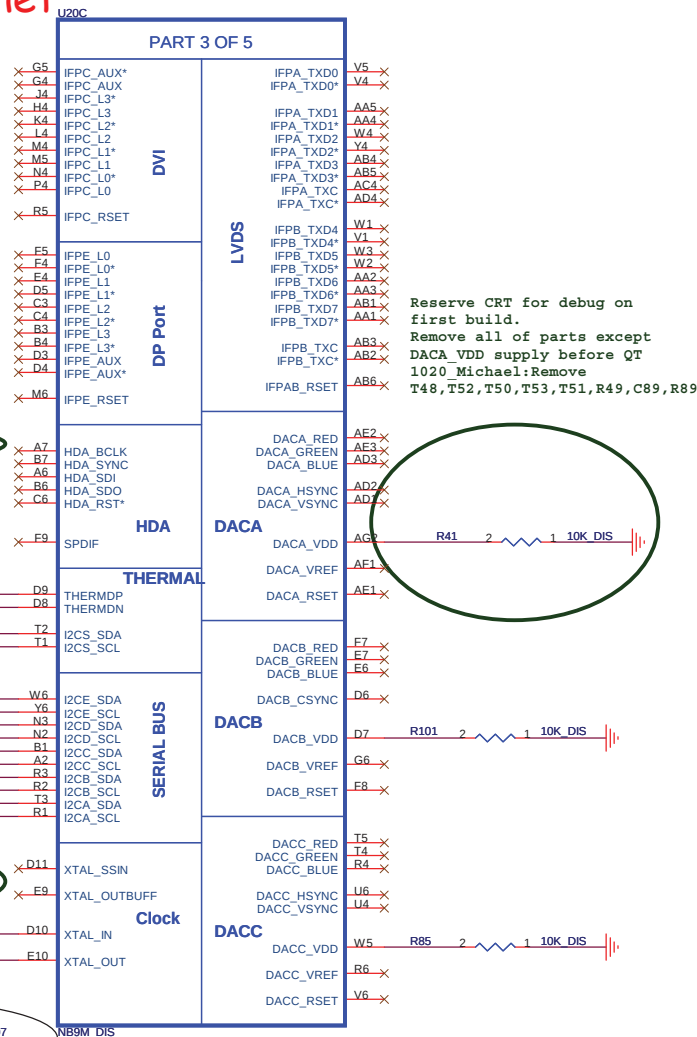
0708_Michael:Pop R46 & R47 for
internal thermal monitor



0701 Michael:Remove SPREAD SPECTRUM circuit



0709-Steg: Change CAP Value from 18p to 22p

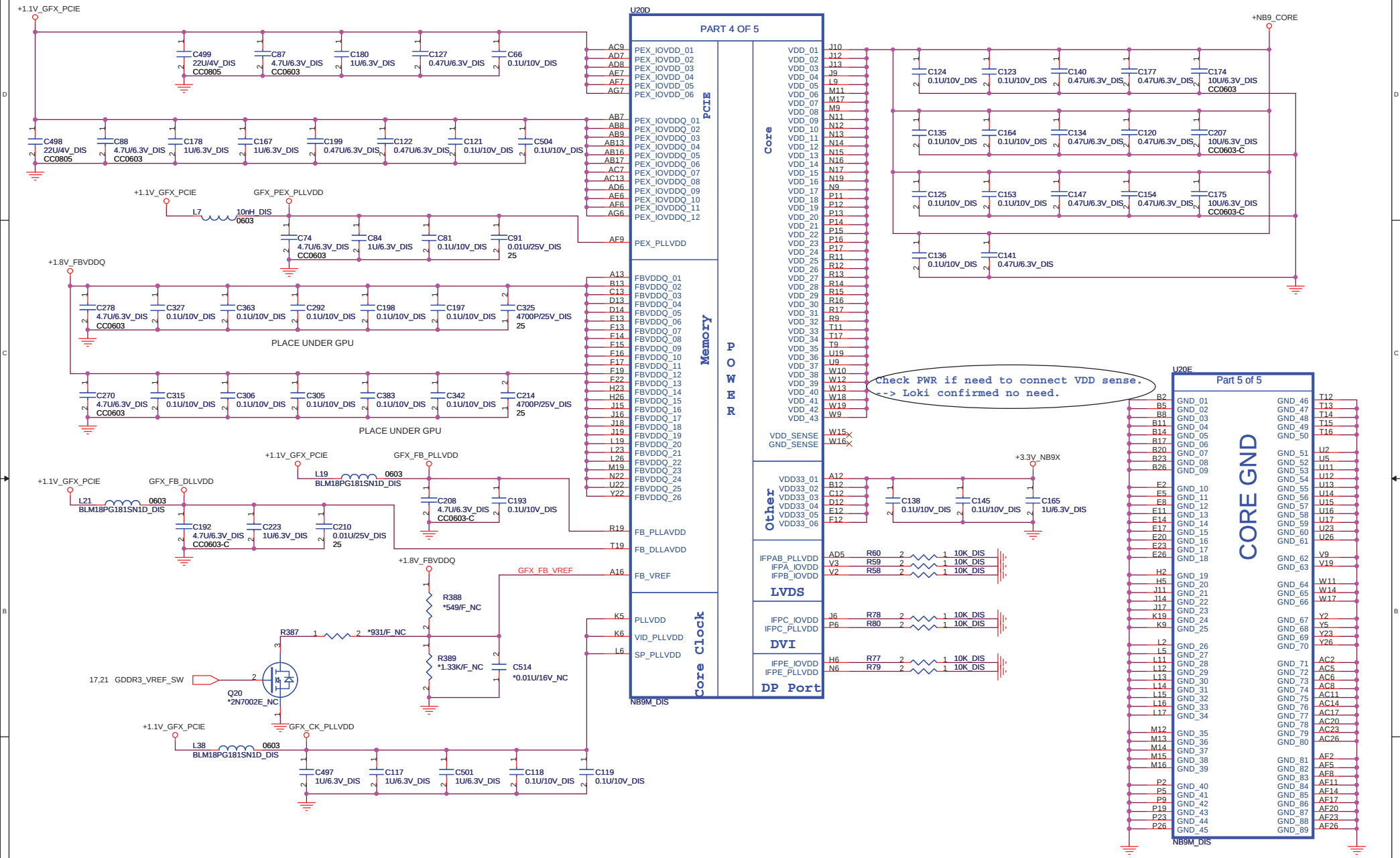


Title	VGA-NB9X GB1-64 (OUTPUT)
-------	--------------------------

Size	Document Number IM3 (XPS-Jolie)
------	------------------------------------

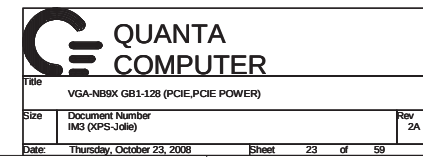
Rev
2A

Date: Monday, October 20, 2008 Sheet 19 of 59



**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number IM3 (XP'S-Jolie)	Rev 2A
Date:	Friday, September 05, 2008	Sheet 22 of 59

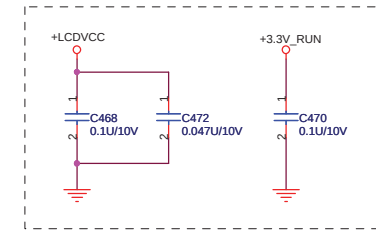
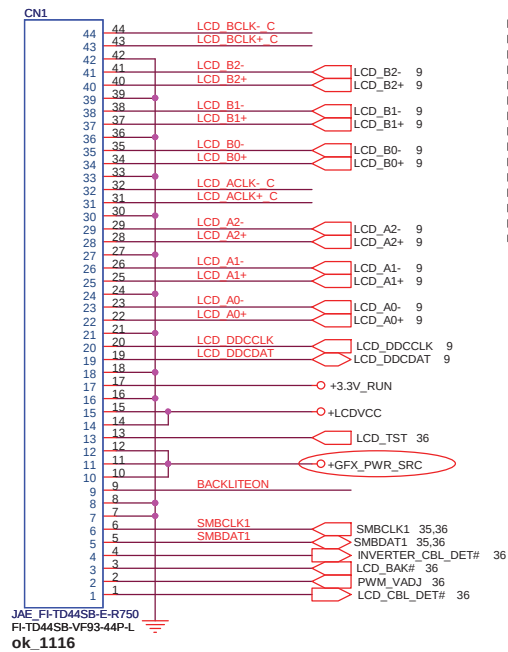
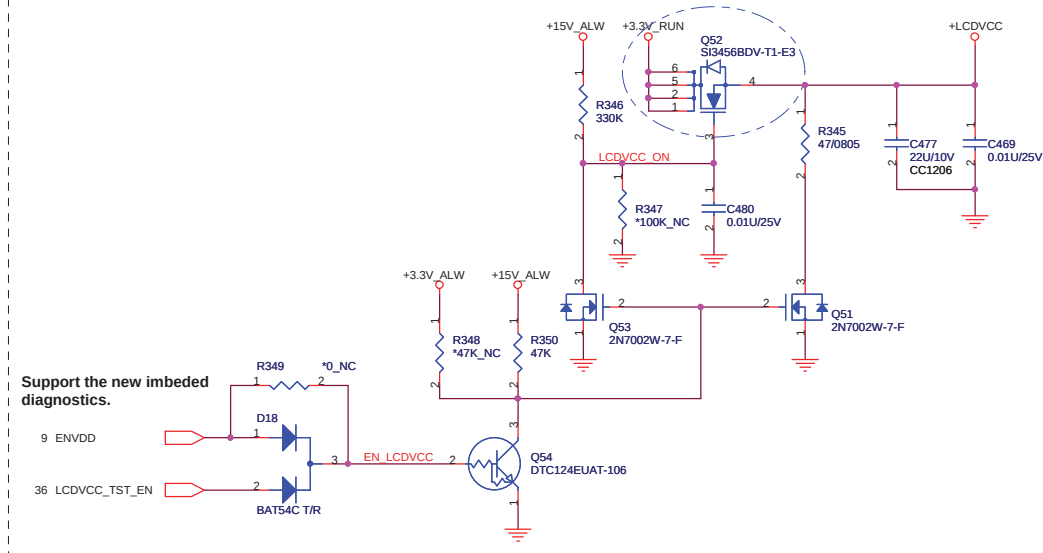


BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE

 QUANTA COMPUTER		
Title		
Size	Document Number IM3 (XP'S-Jolie)	Rev 2A
Date:	Friday, September 05, 2008	Sheet 24 of 59

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

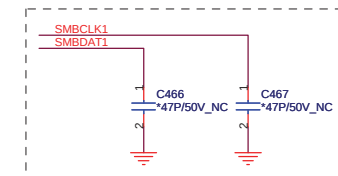
0112-Stanley: Change BOM for EOL issue (SI3456BDV).



WXGA 1280*800=>70 MHz
WXGA+ 1440*900=>108 MHz
WSXGA+ 1680*1050=>120MHz
WUXGA 1920*1200=>166 MHz

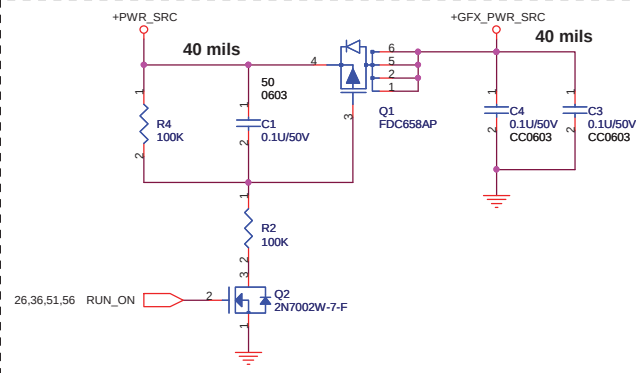
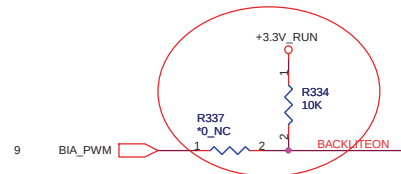
Address : A9H --Contrast
AAH --Backlight

MBRAI specification of antenna gain is 10dBi@474MHz, -7dBi@698MHz, -5dBi@858MHz.



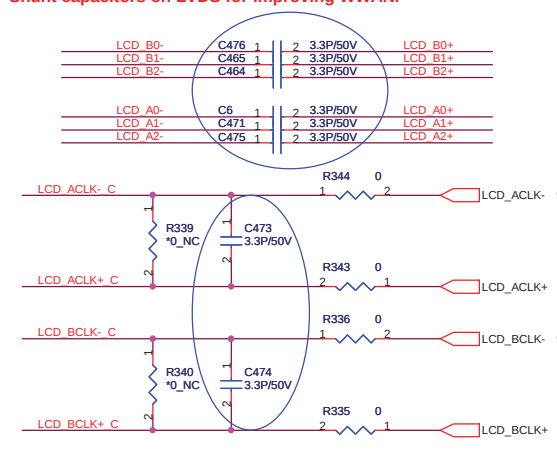
Populate R65 for DPST implementation only.

Populate R341 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.

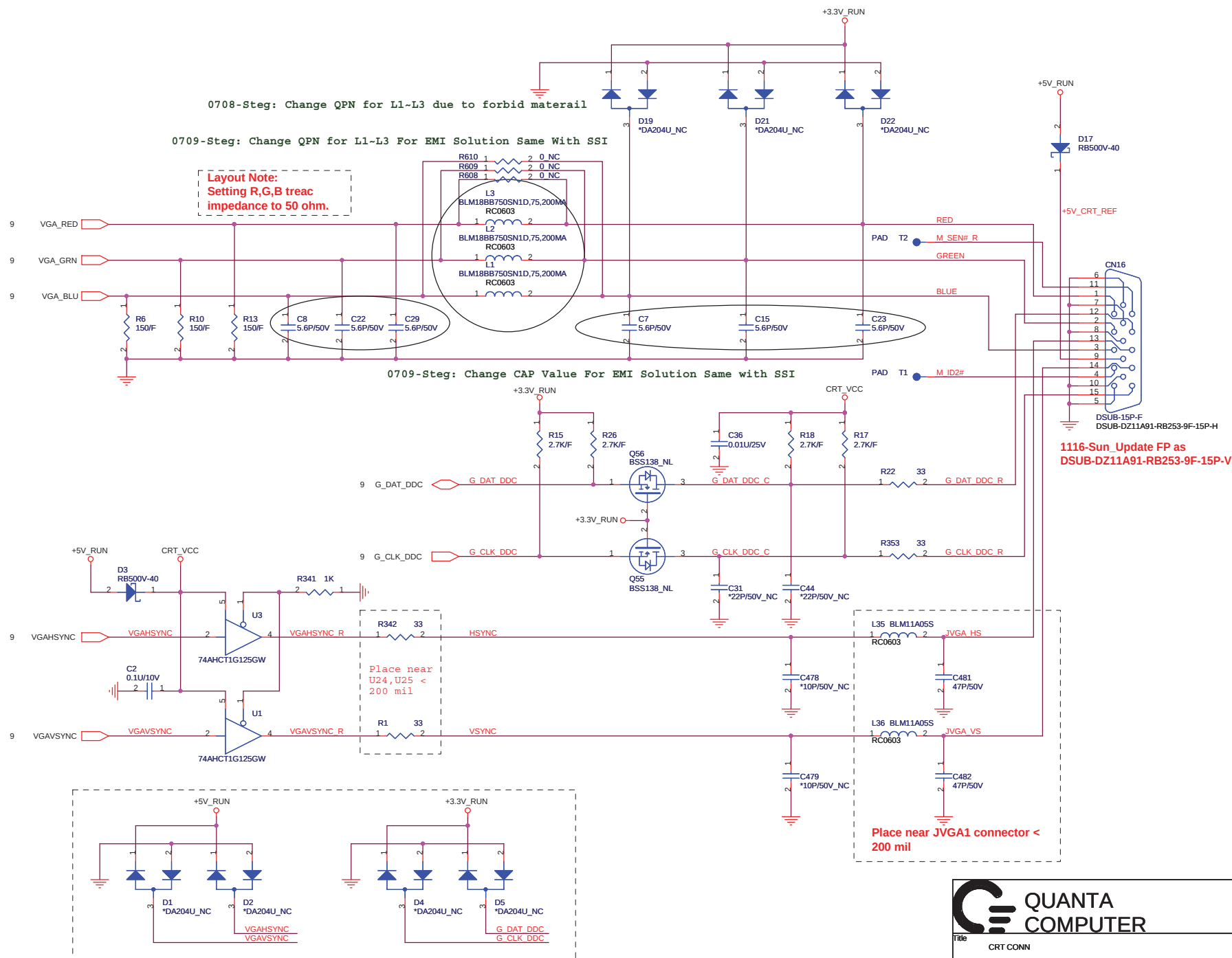


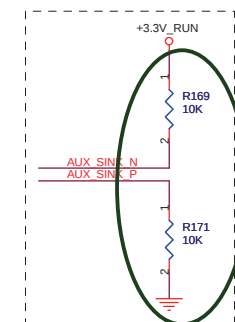
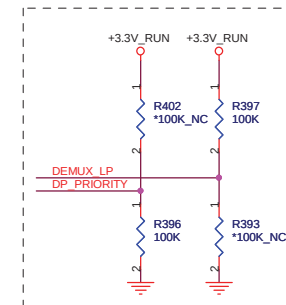
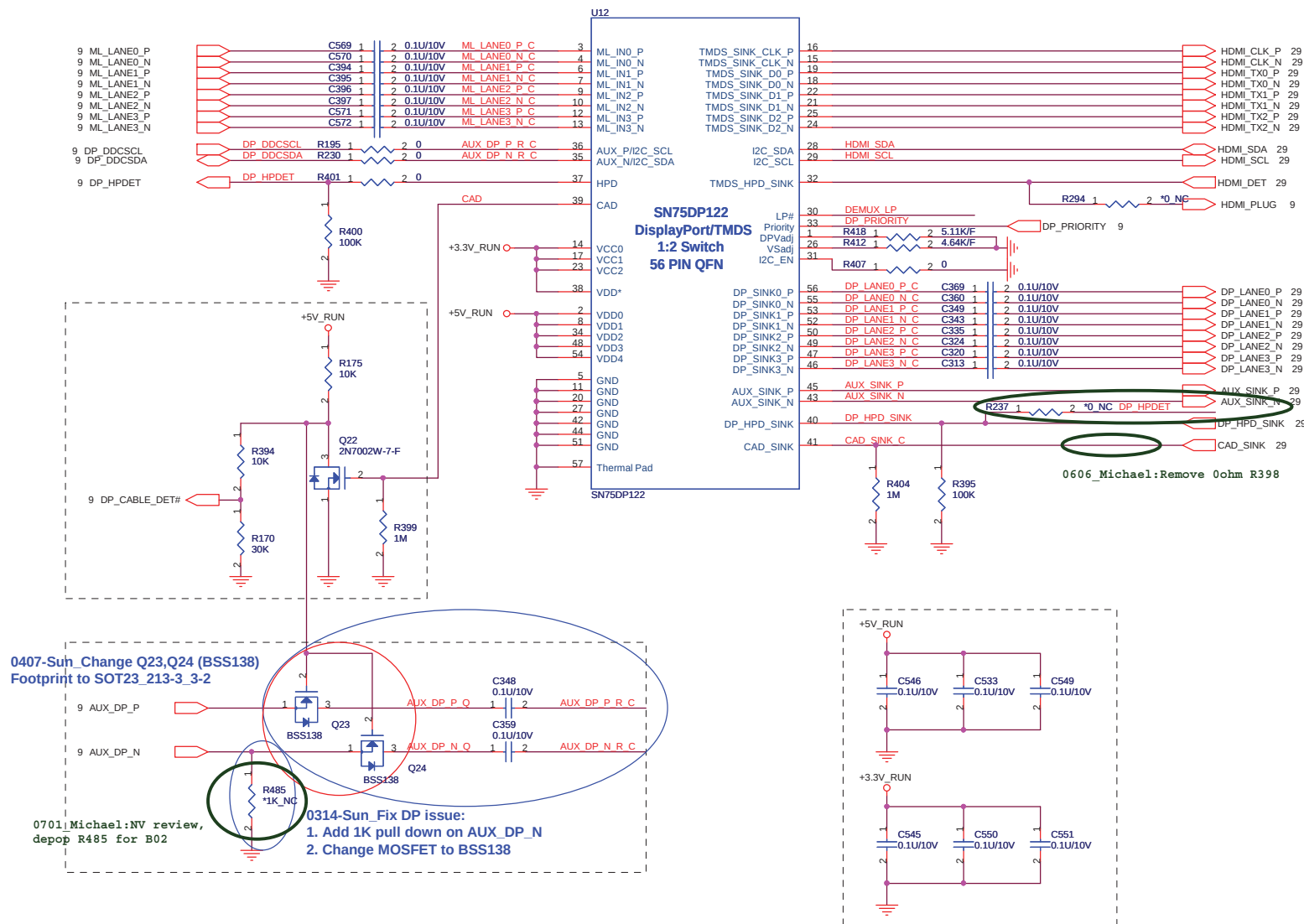
0319-Sun_Pop 3.3P on LVDS bus for COMM team demand

Shunt capacitors on LVDS for improving WWAN.



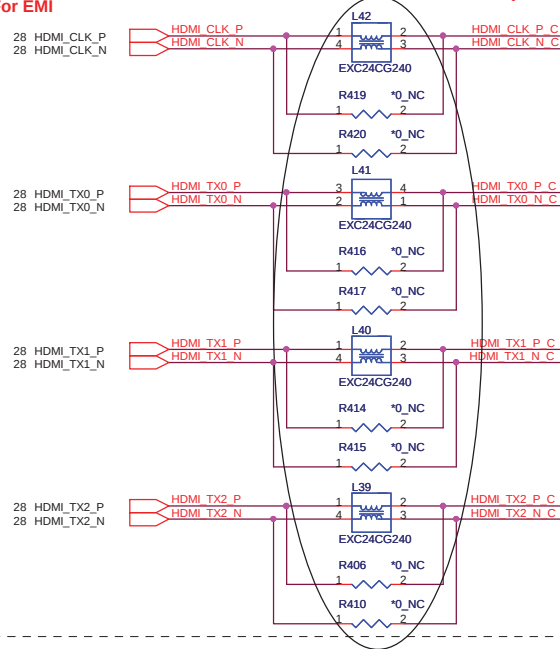
Title			
LCD CONN			
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	2A	
Date:	Friday, September 05, 2008	Sheet	26 of 59



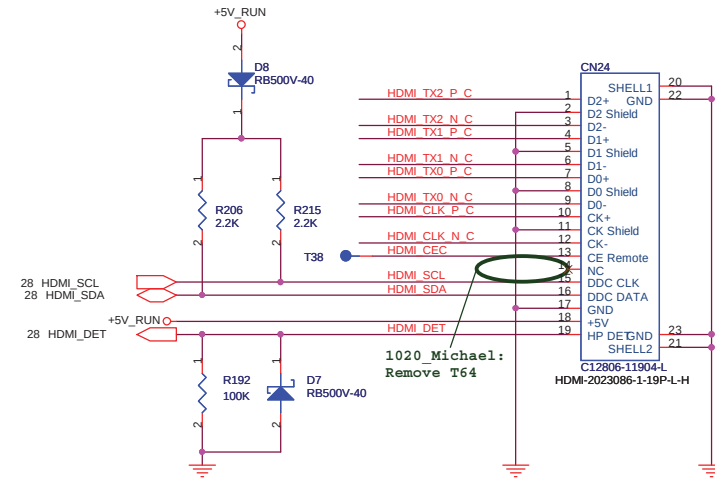


0705-Michael:Change R169 & R171 vaule from 100K to 10K for DP SPEC

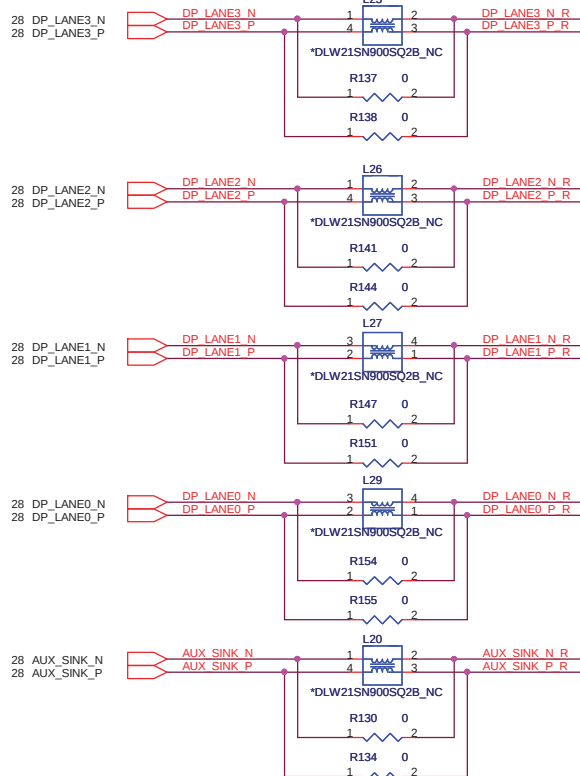
Reserve For EMI



HDMI CONNECTOR

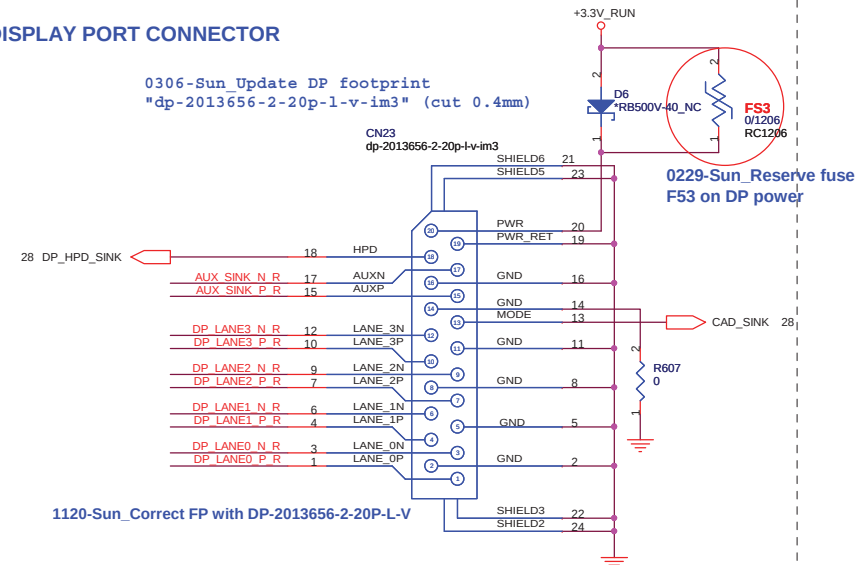


Reserve For EMI



DISPLAY PORT CONNECTOR

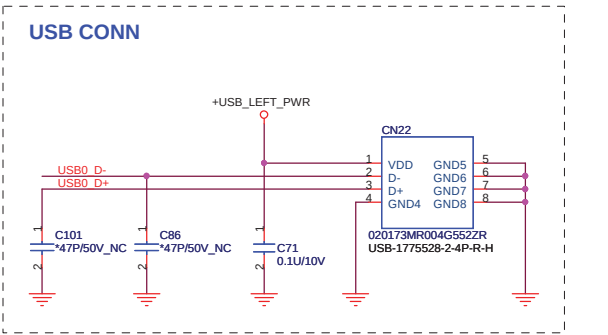
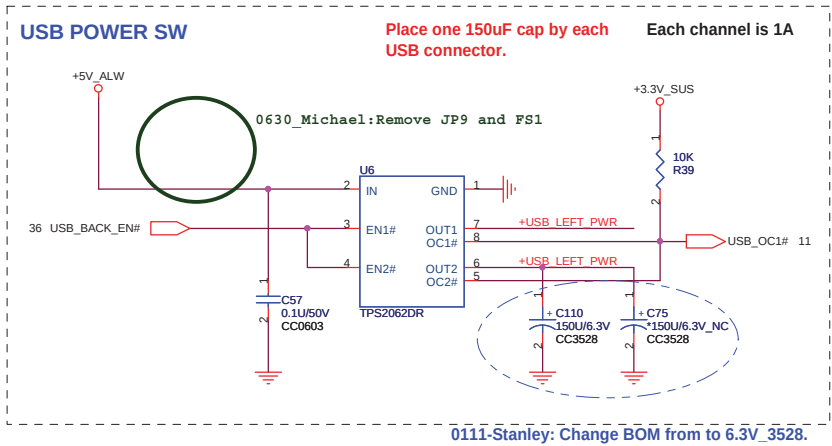
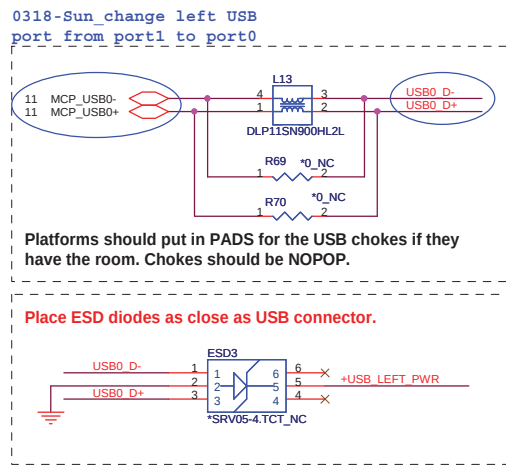
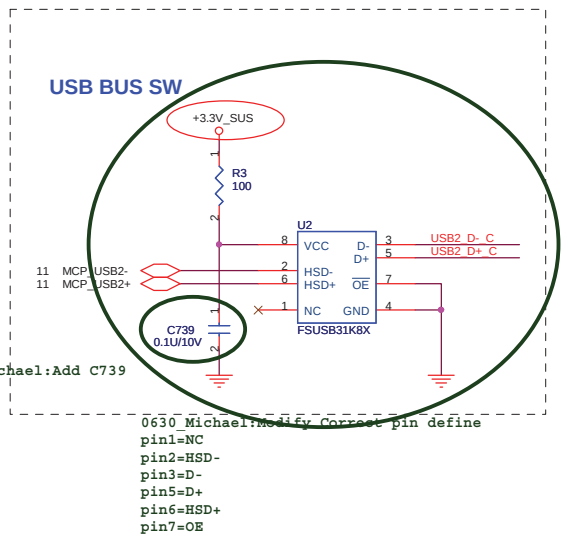
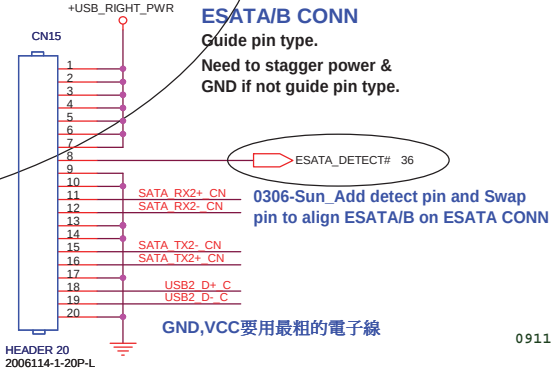
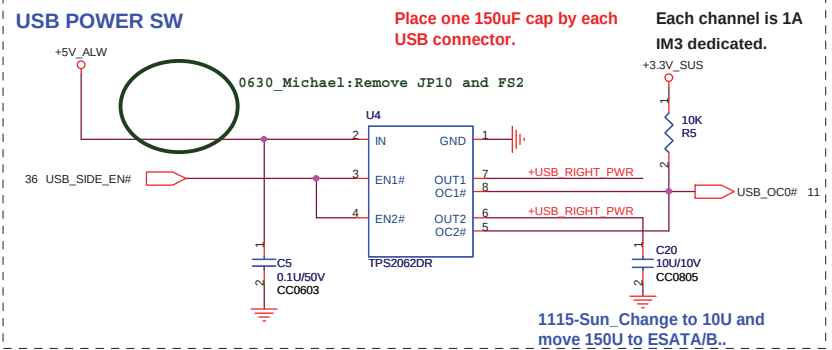
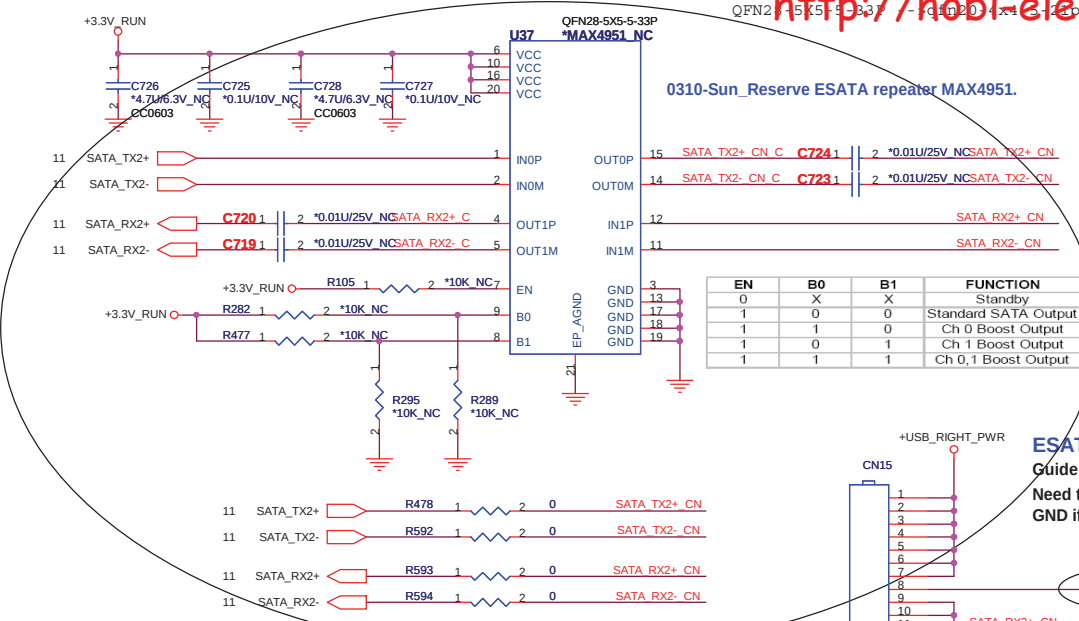
0306-Sun Update DP footprint
"dp-2013656-2-20p-1-v-im3" (cut 0.4mm)



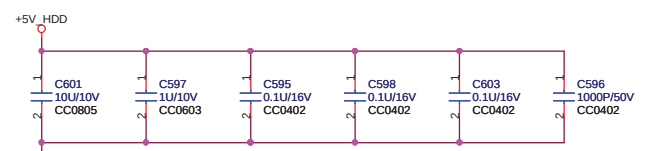
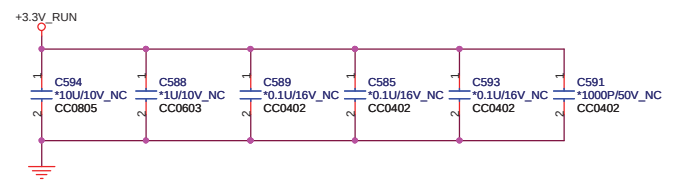
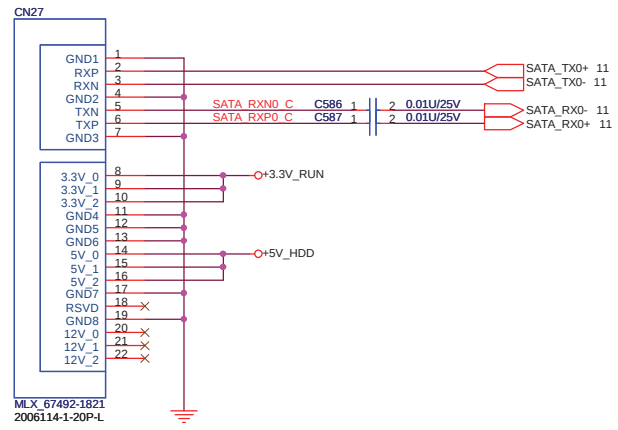
1120-Sun_Correct FP with DP-2013656-2-20P-L-V



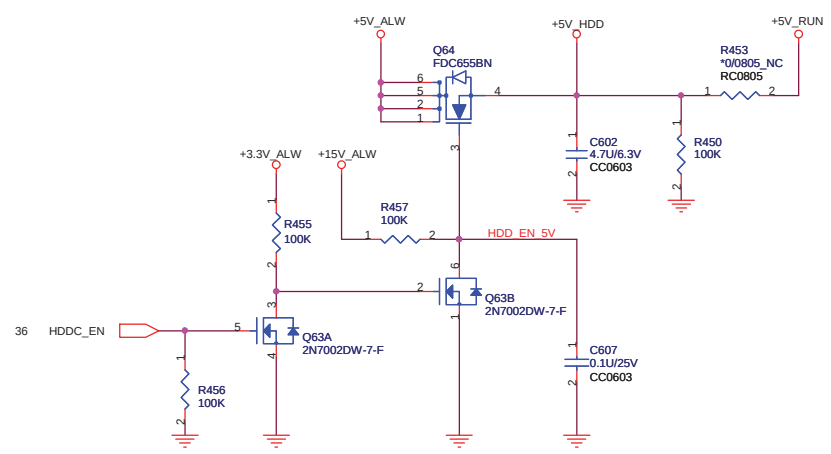
Title		
HDMI & DP CONN		
Size	Document Number	Rev
	IM3 (XPS-Jolie)	2A
Date:	Monday, October 20, 2008	Sheet 29 of 59



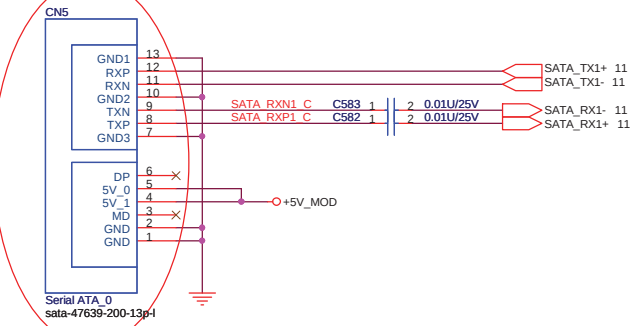
SATA HDD Connector



Place caps close to connector.

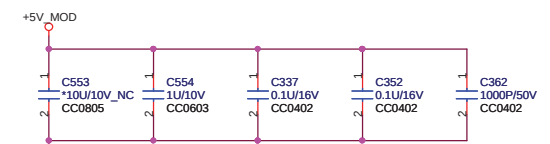


SATA ODD Connector

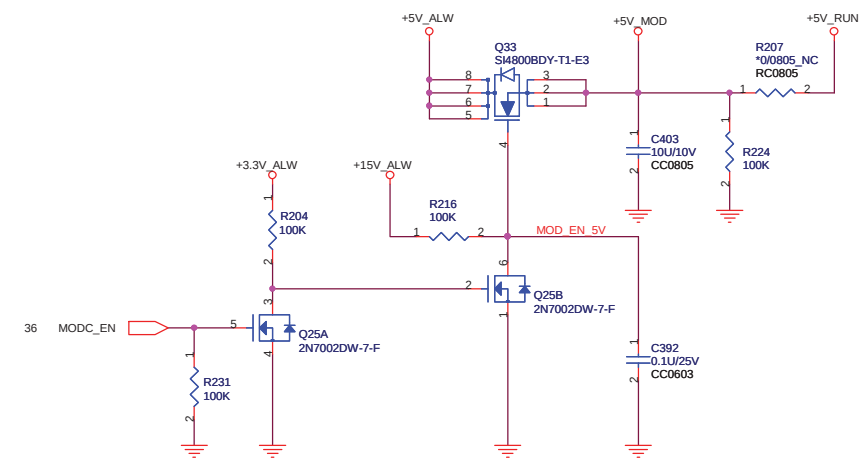


0306-Sun_Change to new footprint_sata-47639-200-13p-I

0407-Sun_Swap pin assignment due to pin direction is reversed

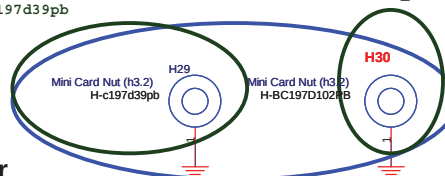


Place caps close to connector.



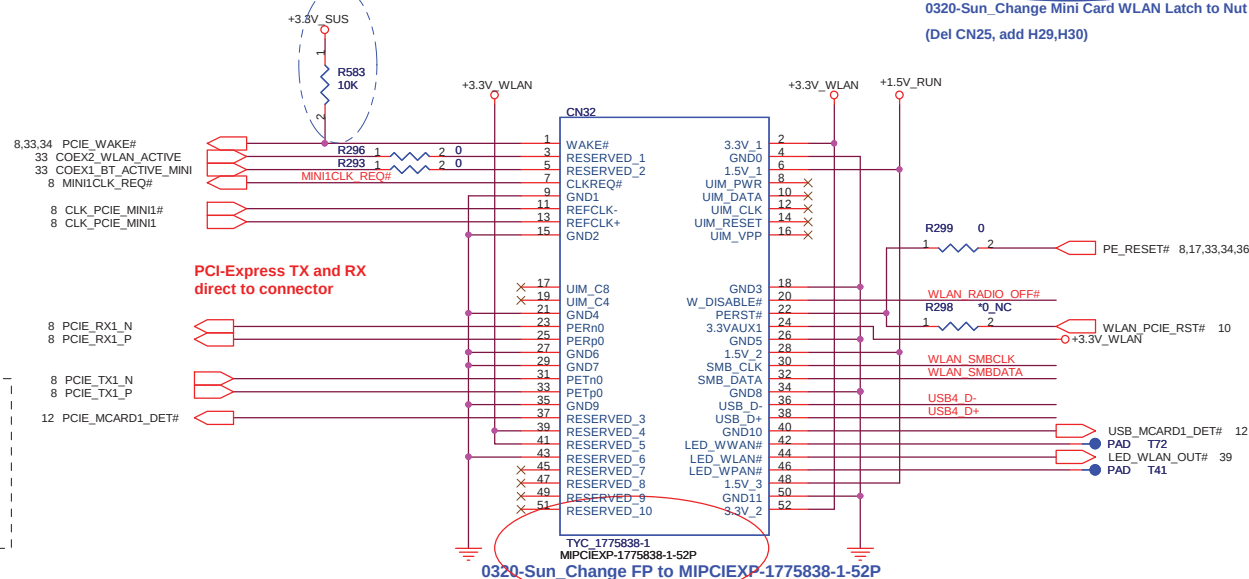
0829_Michael:Change Footprint from H-C197PB to H-c197d39pb

0616_Michael:Change footprint

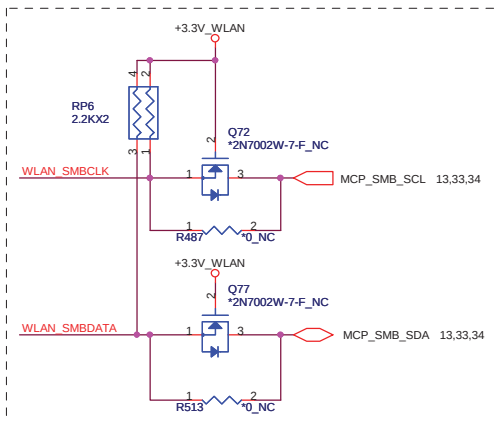
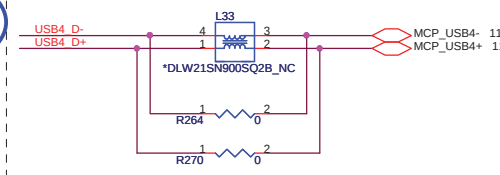


0320-Sun_Change Mini Card WLAN Latch to Nut
(Del CN25, add H29,H30)

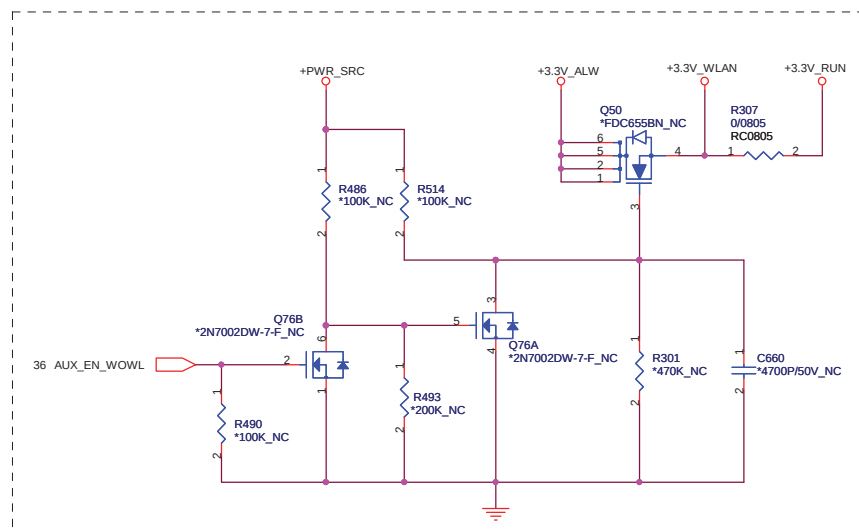
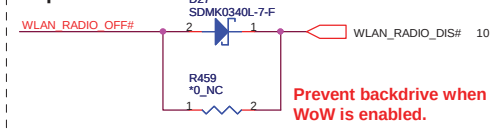
MiniCard WLAN Connector



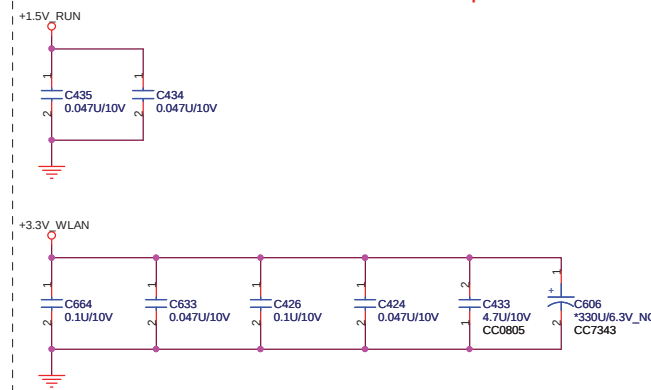
Reserved PAD for EMI



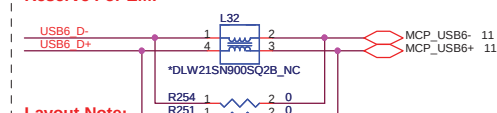
Support for WoW



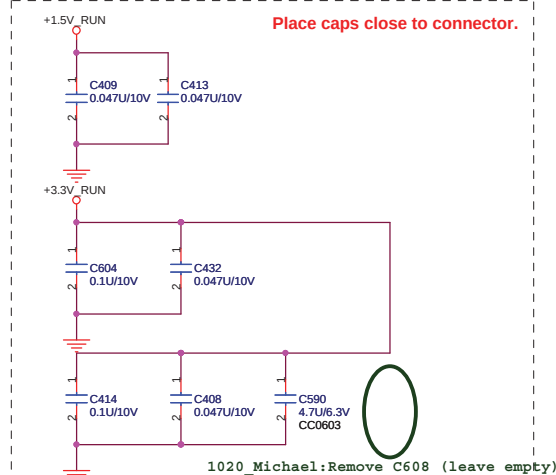
Place caps close to connector.



QUANTA
COMPUTER

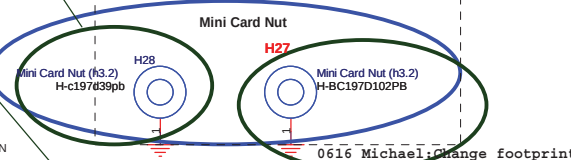


Layout Note: R240 and R244 close to choke as possible to minimize stubs.

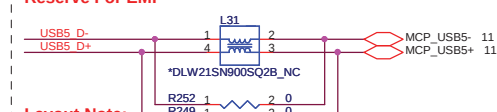


Place caps close to connector.

1020 Michael:Remove C608 (leave empty)

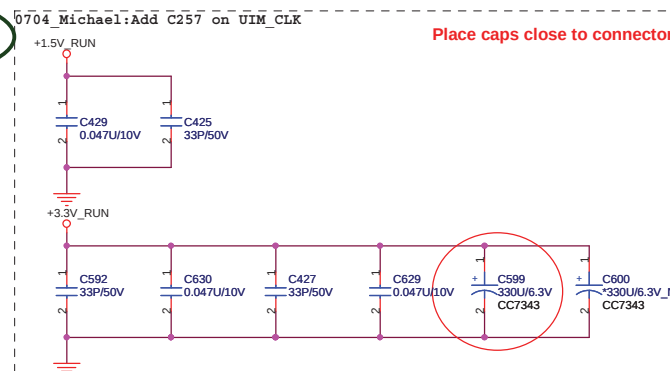
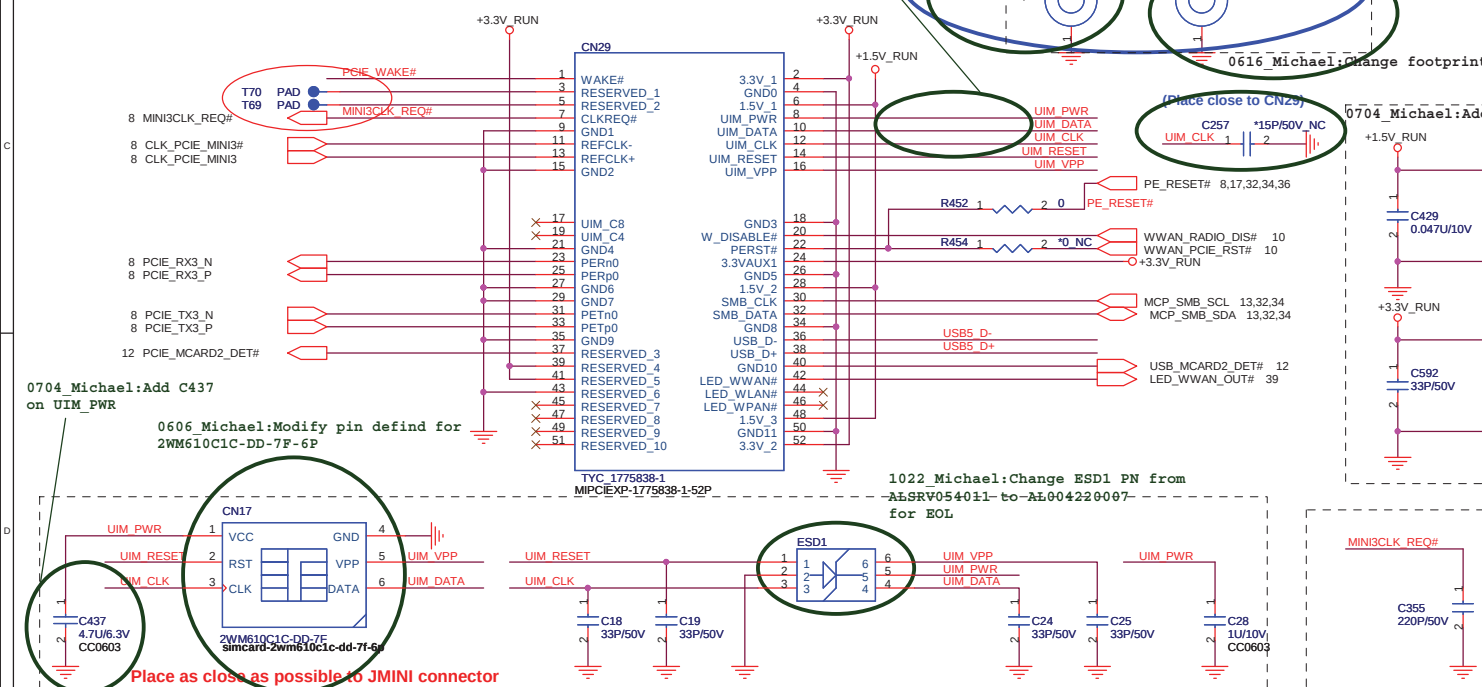


Reserve For EMI



Layout Note: R240 and R244 close to choke as possible to minimize stubs.

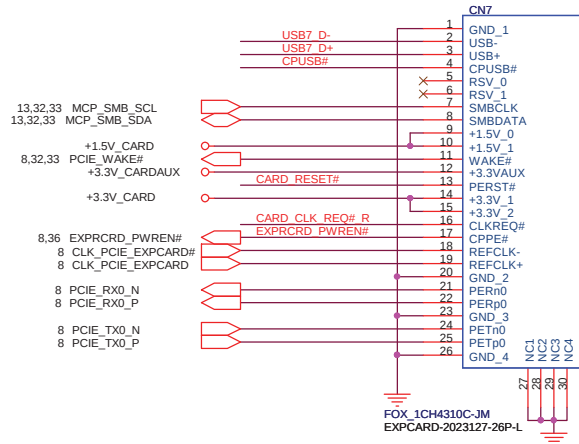
Place caps close to connector.



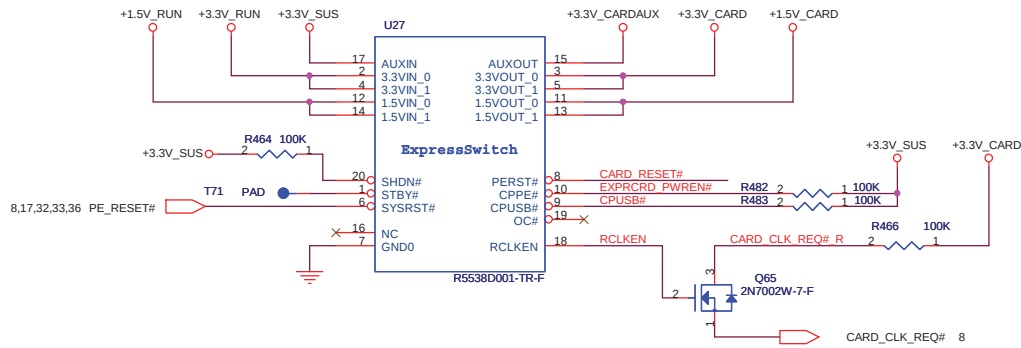
QUANTA
COMPUTER

Title			
MINI-CARD (WWAN,WPAN)			
Size	Document Number		Rev
	IM3 (XPS-Jolie)		2/
Date:	Thursday, October 23, 2008	Sheet	33 of 59

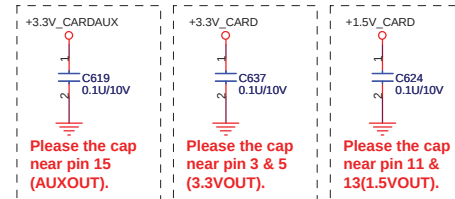
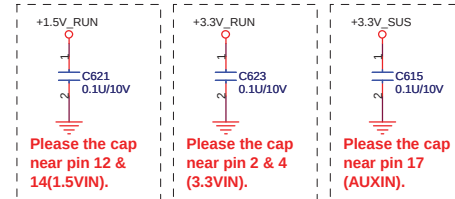
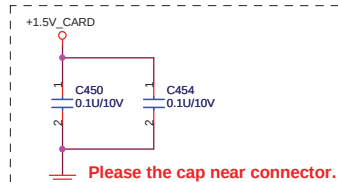
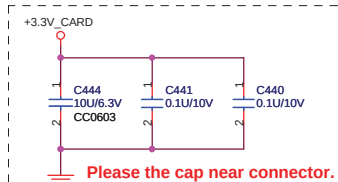
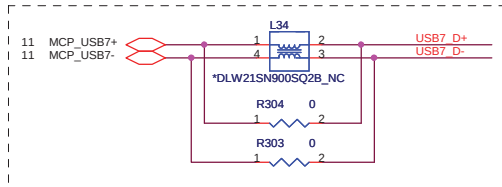
Express Card

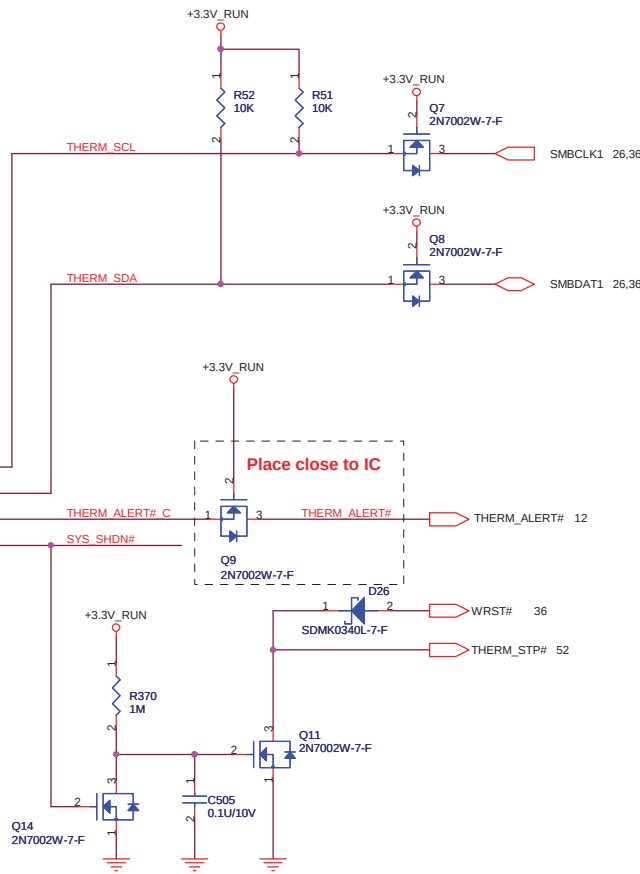
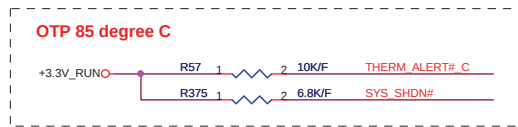
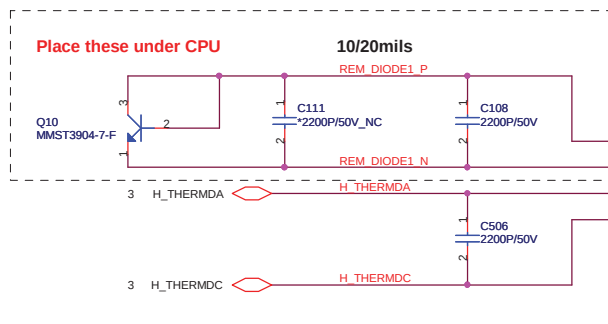
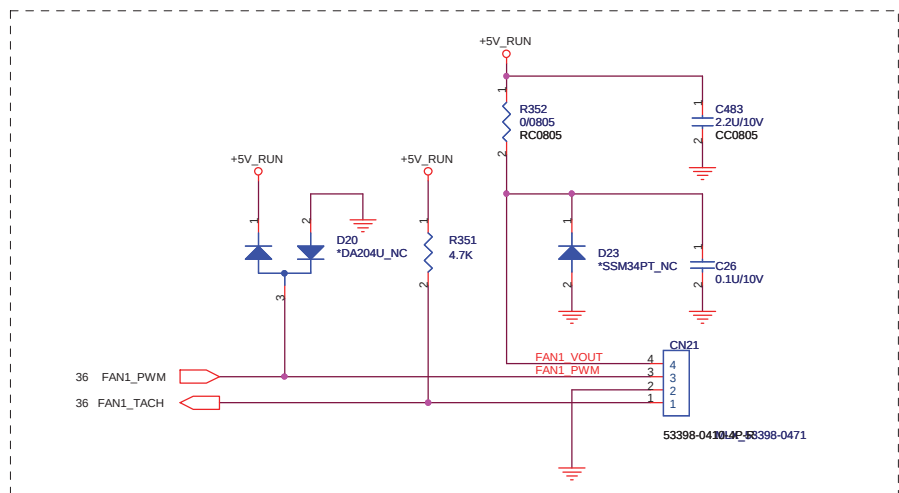


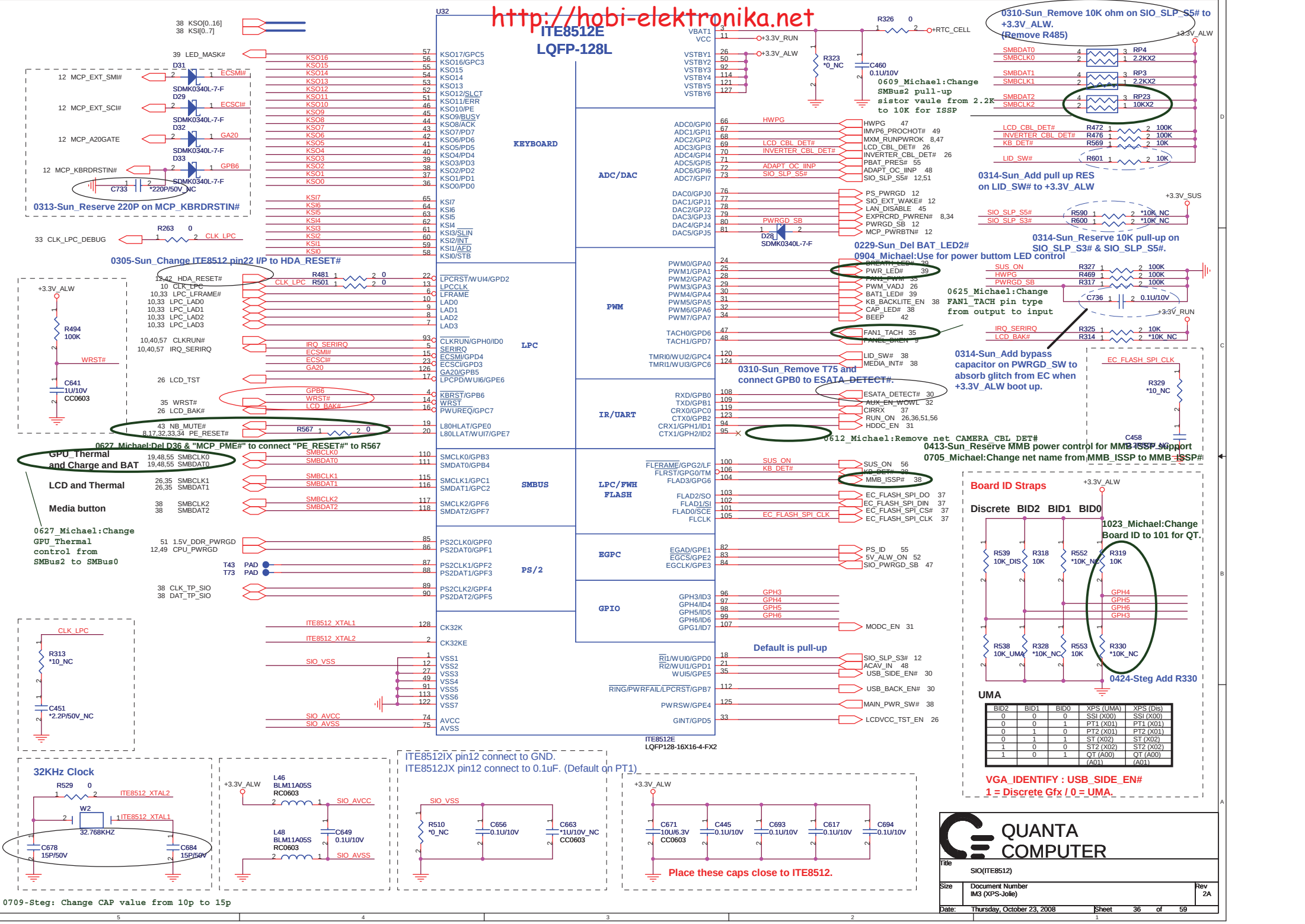
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



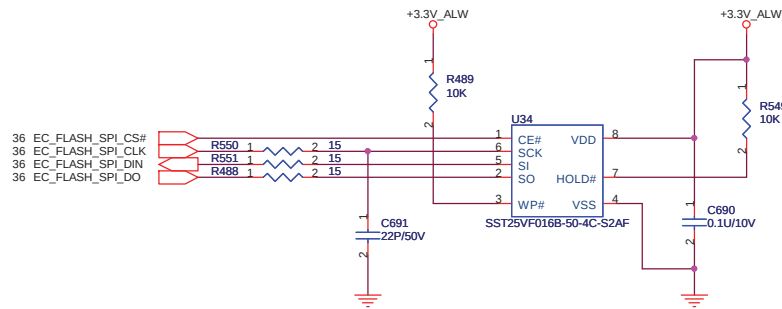
PCI-Express TX and RX direct to connector.



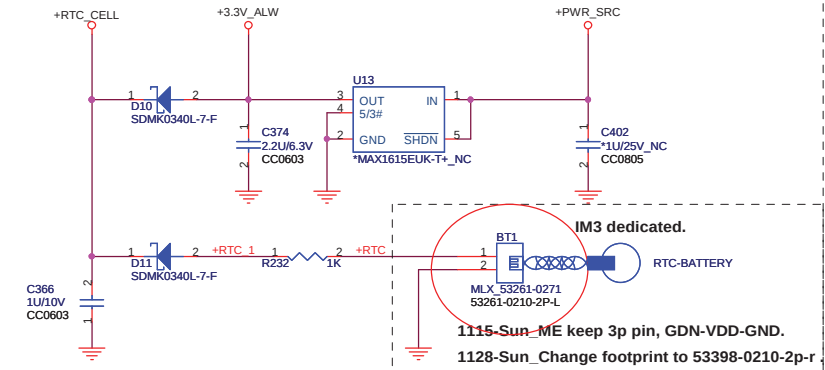




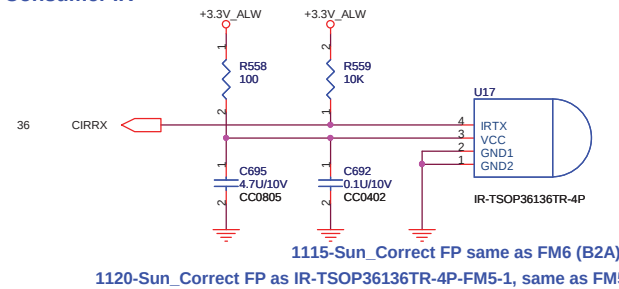
16Mbit (2M Byte), SPI



RTC BATTERY

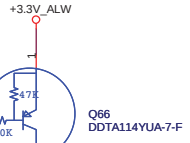


Consumer IR



Battery status

0313-Sun_Change battery LED to Amber (3.3V drive) (Remove Q68, R462, R460)



0606_Michael:Add R462 connect to CN2 on BAT1_LED



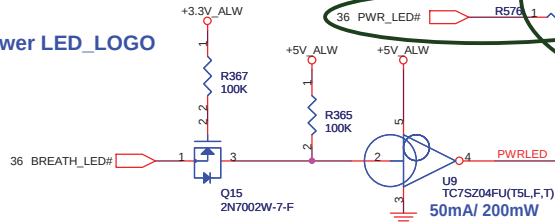
0922_Michael:Remove BAT1_AMB_LED function

0229-Sun_Del BAT_LED2
[Del R295,Q48,Q43 (2N7002) and Q46,Q47 (DDTA114YUA)]

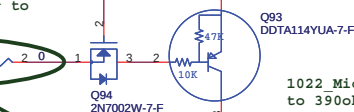
0229-Sun_Change PWRLED_SW control same as PWRLED_LOGO
[Del U10 (TC7S204F), Q16 (2N7002)]

0904_Michael:Add R576 and connector to PWR_LED# from ITE8512

Power LED_LOGO



0618_Michael:Follow DELL command modify circuit to change the LED behavior of Power button



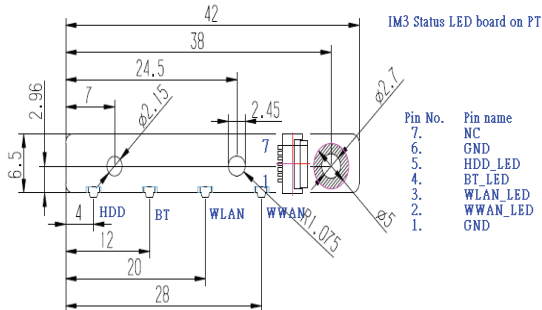
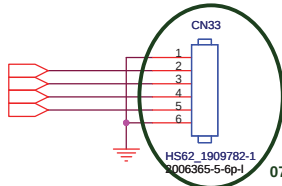
1022_Michael:Change R390 from 1K to 390ohm for LED brightness



1022_Michael:Change R366 from 220ohm to 100ohm for LED brightness

0229-Sun_Remove LED control by LID_SW#
(Del R478,R477,Q75)

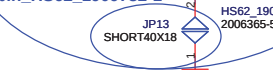
0704_Michael:Change CN33 pin number from 7pin to 6pin and also change type from HEADER7 to HS62_1909782-1 for cost down



Logo LED/B connector

PWRLED_LOGO
BAT1_LED

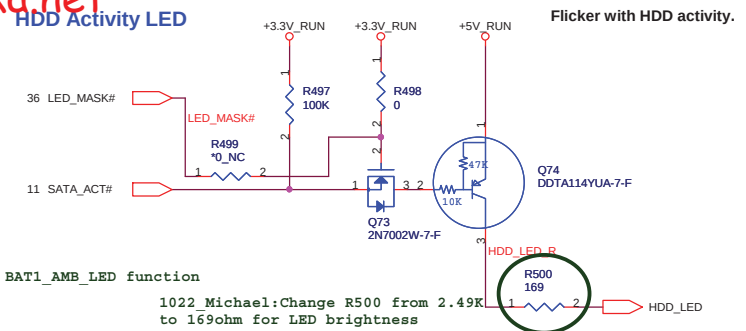
0306-Sun_Change Logo LED as BAT & PWR LED and change connector to 6pin_HS62_1909782-1



0314-Sun_Add short pad on GND of Logo LED/B connector for EMI request.

HDD Activity LED

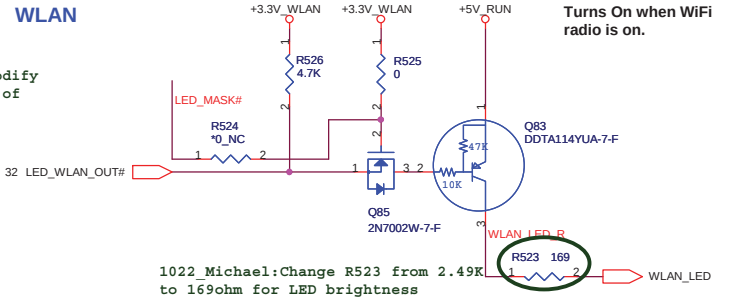
Flicker with HDD activity.



1022_Michael:Change R500 from 2.49K to 169ohm for LED brightness

WLAN

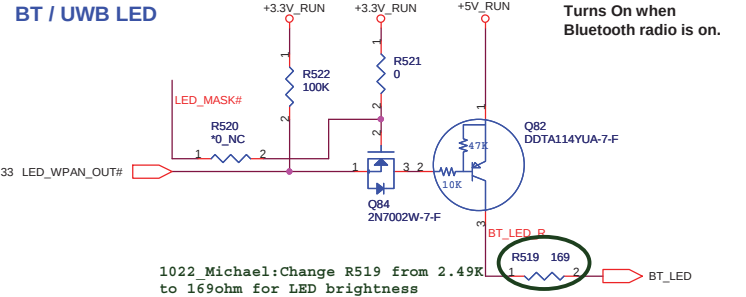
Turns On when WiFi radio is on.



1022_Michael:Change R523 from 2.49K to 169ohm for LED brightness

BT / UWB LED

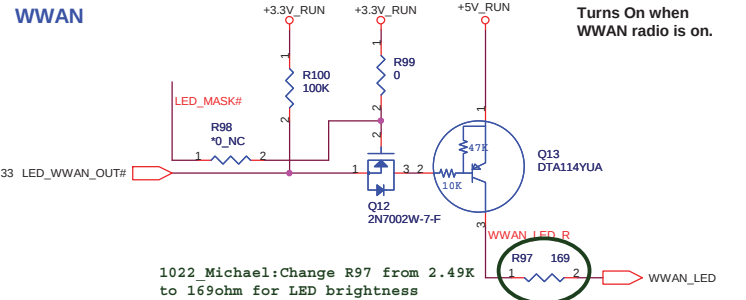
Turns On when Bluetooth radio is on.



1022_Michael:Change R519 from 2.49K to 169ohm for LED brightness

WWAN

Turns On when WWAN radio is on.

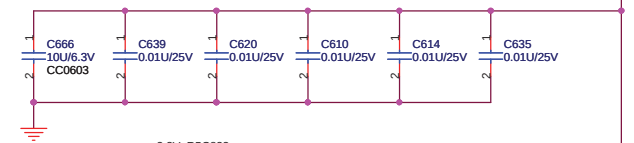


1022_Michael:Change R97 from 2.49K to 169ohm for LED brightness

QUANTA COMPUTER

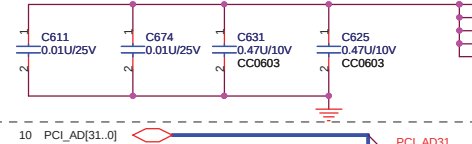
Title	LED	Rev	2A
Size	Document Number IM3 (XPS-Jolie)	Date:	Wednesday, October 22, 2008
Sheet	39	of	59

Place the power caps close to the relation pins.



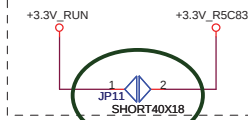
+3.3V_R5C833

Please place capacitors for VCC_ROUTx as close to R5C833 as possible.



10 PCI_AD[31..0]

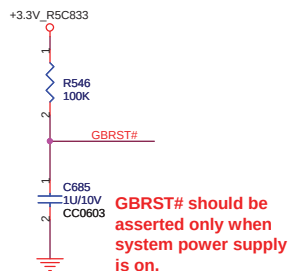
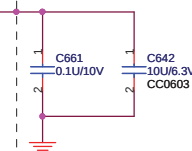
U298
VCC_PCI1
VCC_PCI2
VCC_PCI3
VCC_PCI4
VCC_PCI5
VCC_PCI6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5



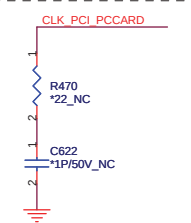
0606_Michael:Change footprint from 0ohm R468 to normal short type JP11 (short40x18)

+3.3V_R5C833

Place the power caps close to the relation pins.



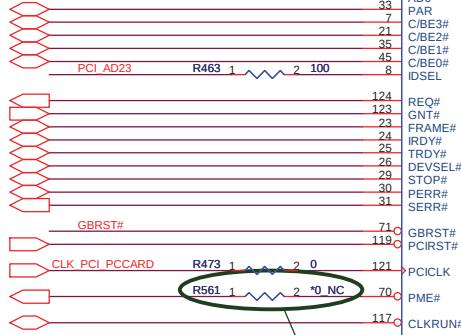
GBRST# should be asserted only when system power supply is on.



10 PCI_PAR
10 PCI_C_BE3#
10 PCI_C_BE2#
10 PCI_C_BE1#
10 PCI_C_BE0#

10 PCI_REQ0#
10 PCI_GNT0#
10 PCI_FRAME#
10 PCI_IRDY#
10 PCI_TRDY#
10 PCI_DEVSEL#
10 PCI_STOP#
10 PCI_PERR#
10 PCI_SERR#

10 PCI_RST#
10 CLK_PCI_PCCARD
10 PCI_PME#
10,36 CLKRUN#



0707_Michael:Depop R561 for leakage issue

0630_Michael:Remove Mini PCI CN8 and circuit

PCI / OTHER

GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10

AGND1
AGND2
AGND3
AGND4
AGND5

HWSNPDR#
MSEN
XDEN
UDIOS
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#

INTA#
INTB#

TEST

1394 Interrupt
Media card Interrupt

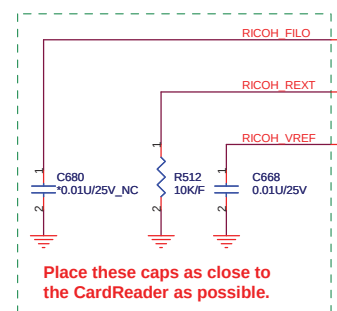
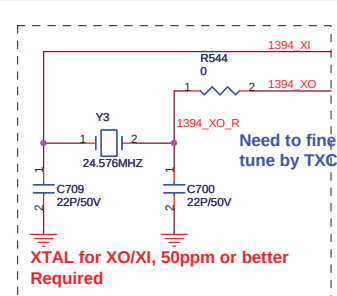
PCI_INTW#
PCI_INTX#

PME#
CLKRUN#

R5C833T_V00

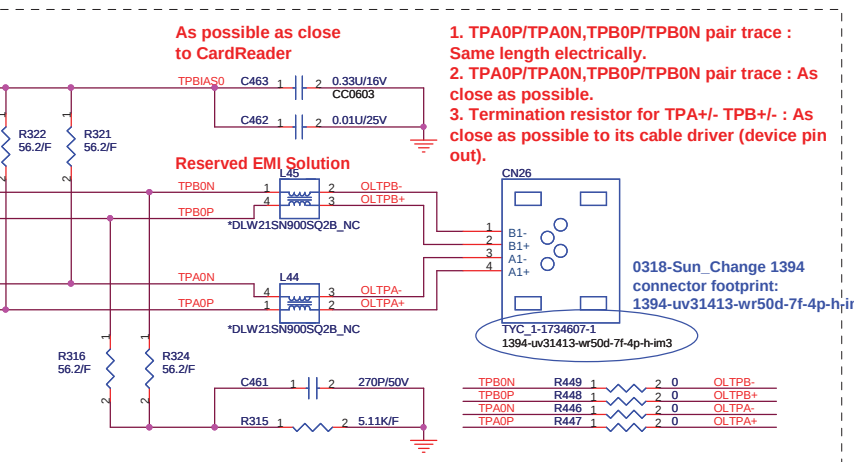
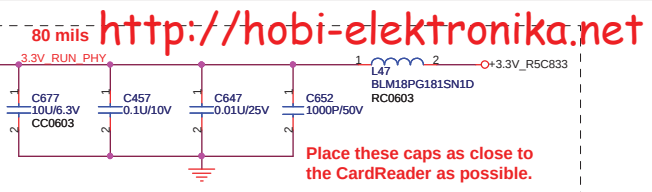
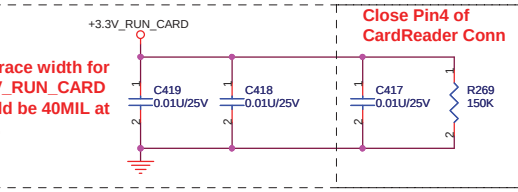
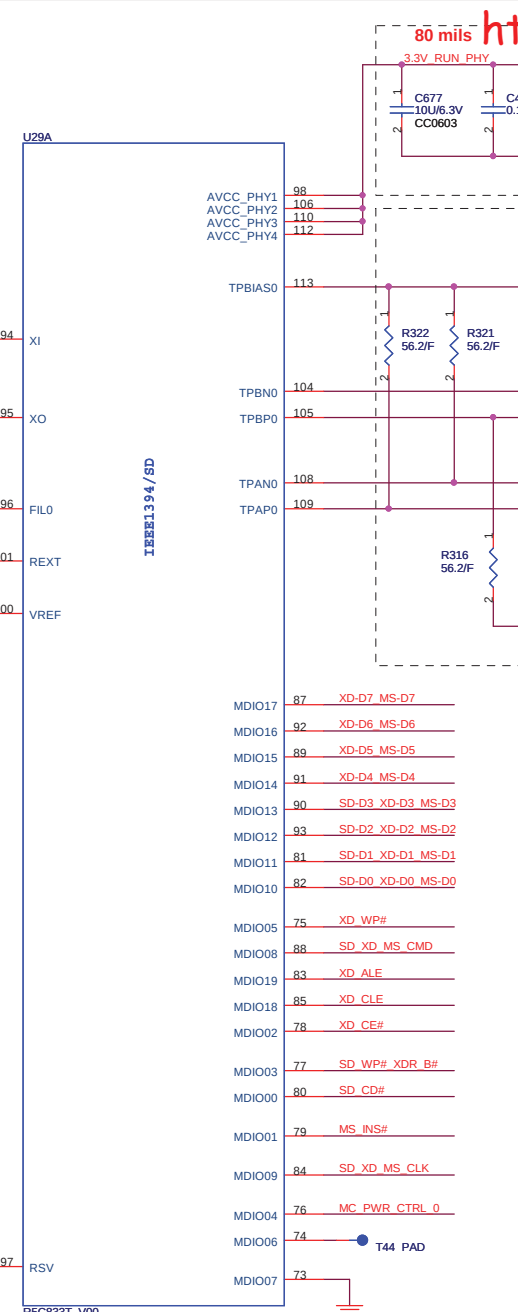
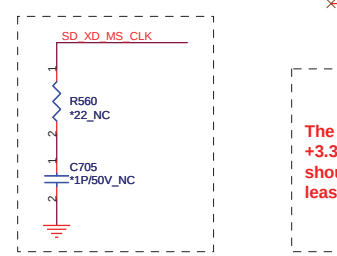
R563 100K





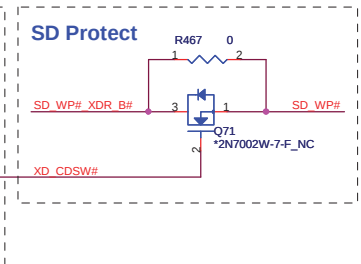
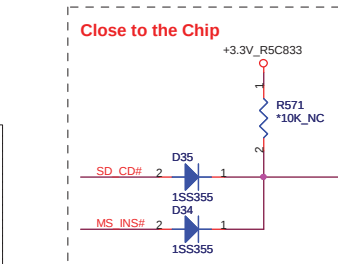
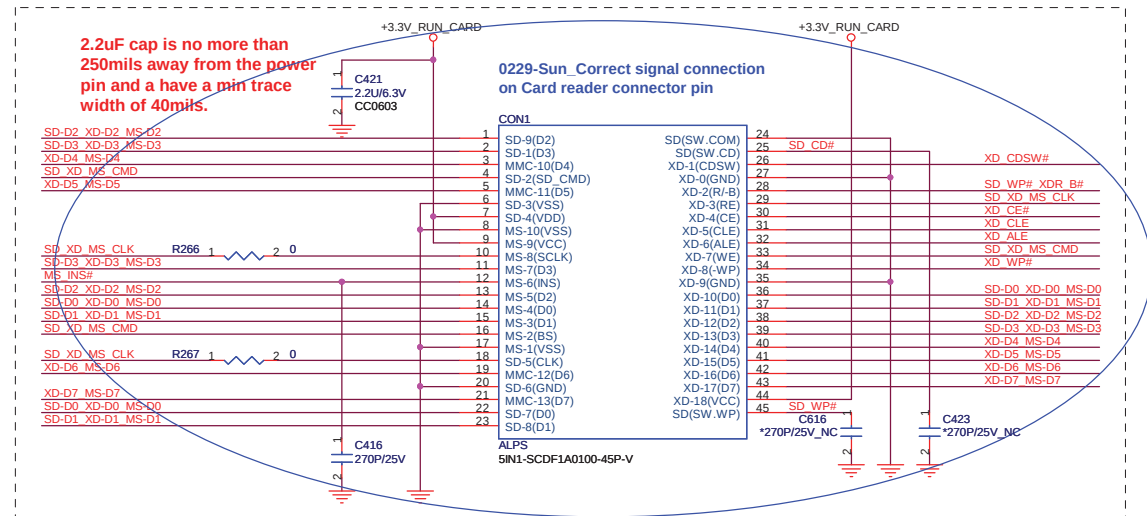
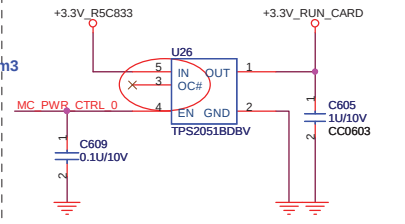
Card Reader interface signal mapping

PIN	SD	MMC	MS	XD
MDIO00	SD_CD#	MMC_CD#	MS_CD#	XD_CD#
MDIO01				XD_CD1#
MDIO02	SD_WP#	MMC_PWR	MS_PWR	XD_E/B#
MDIO04	SD_PWR0	MMC_PWR	MS_PWR	XD_WP#
MDIO05	SD_PWR1	MMC_PWR	MS_PWR	XD_WP#
MDIO06	SD_LED#	MMC_LED#	MS_LED#	XD_LED#
MDIO07	MTST			
MDIO08	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO09	SD_CLK	MMC_CLK	MS_CLK	XD_RE#
MDIO10	SD_D0	MMC_D0	MS_D0	XD_D0
MDIO11	SD_D1	MMC_D1	MS_D1	XD_D1
MDIO12	SD_D2	MMC_D2	MS_D2	XD_D2
MDIO13	SD_D3	MMC_D3	MS_D3	XD_D3
MDIO14	MMC_D4			XD_D4
MDIO15	MMC_D5			XD_D5
MDIO16	MMC_D6			XD_D6
MDIO17	MMC_D7			XD_D7
MDIO18				XD_CLE
MDIO19				XD_ALE

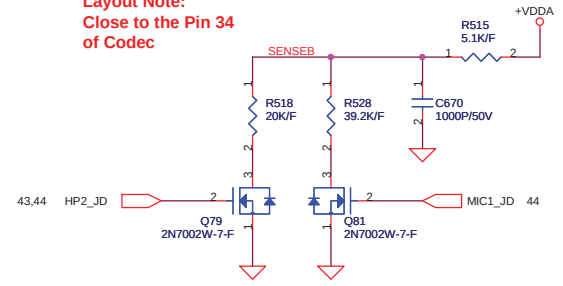


Layout Note:

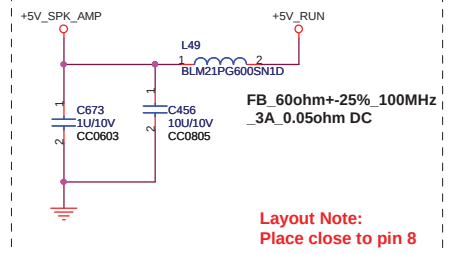
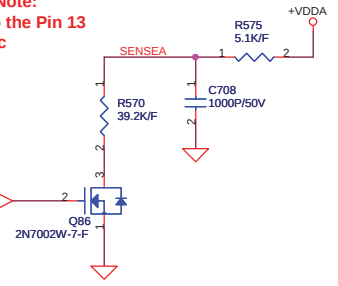
- 1). The distance between Media Card Power Switch and Media Socket should be less than 2-inches.
- 2). The trace width for +3.3V_RUN_CARD should be 40MIL at least.
- 3). The GND trace for Media Card Socket should be 40MIL at least.



Layout Note:
Close to the Pin 34
of Codec

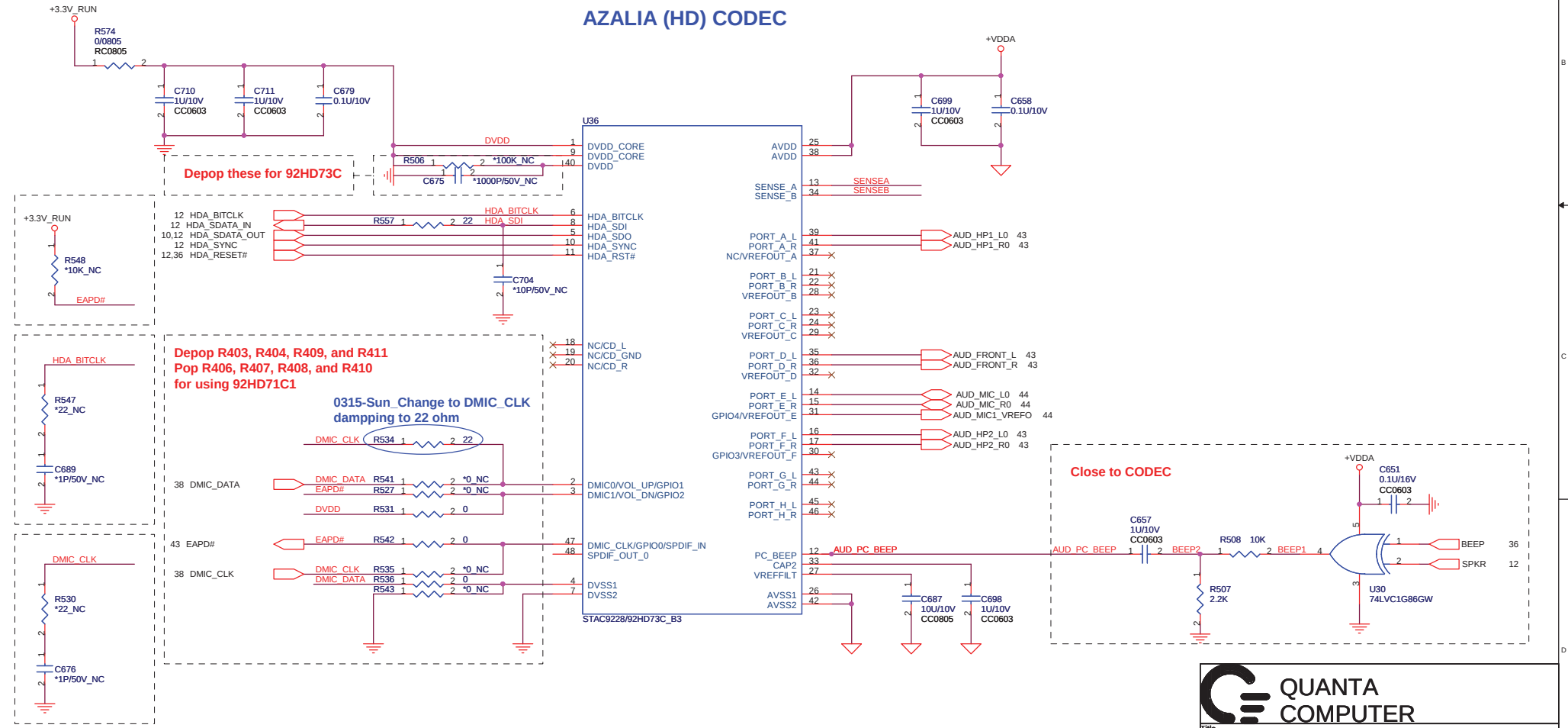


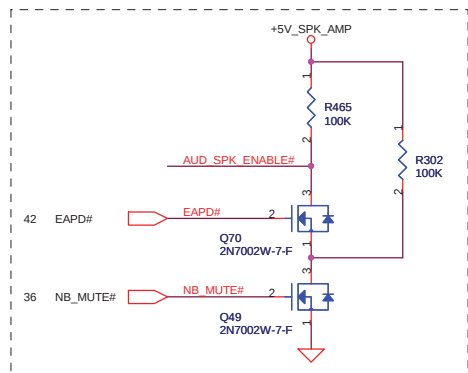
Layout Note:
Close to the Pin 13
of Codec



Layout Note:
Place close to pin 8

AZALIA (HD) CODEC





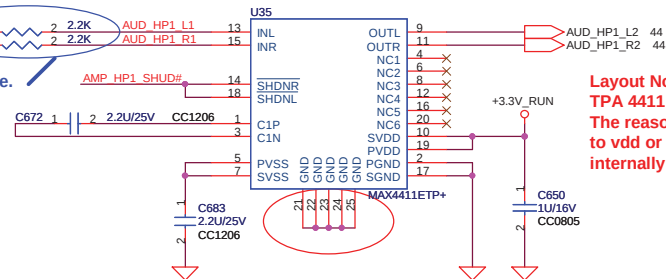
0315-Sun_Improve Dynamic Range.
0320-StegChange AC coupling to 10U/10V



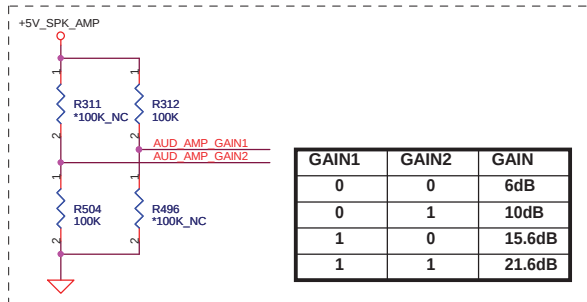
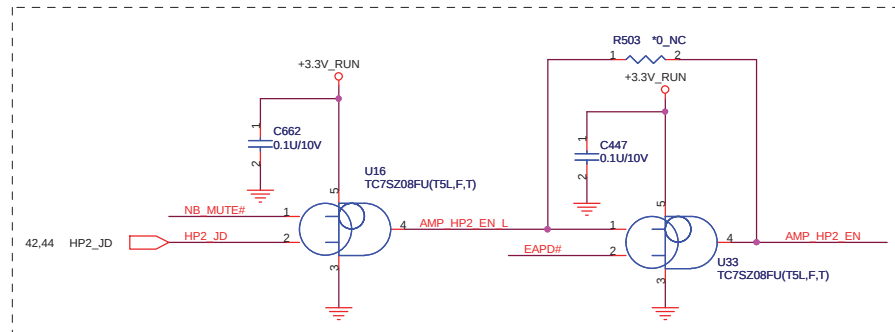
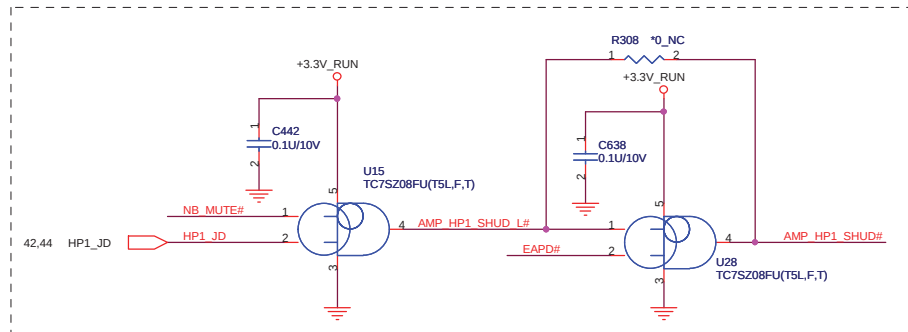
0310-Sun_Improve Dynamic Range.
Add R597,R598 w/2.2K



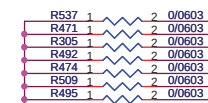
0315-Sun_Improve Dynamic Range.
Pop C452,C455 to 330P



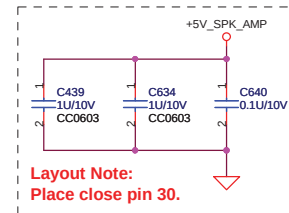
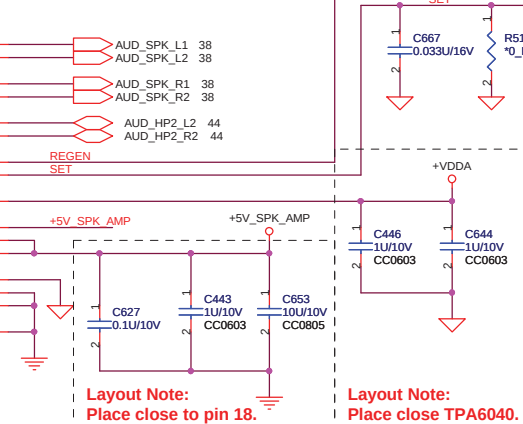
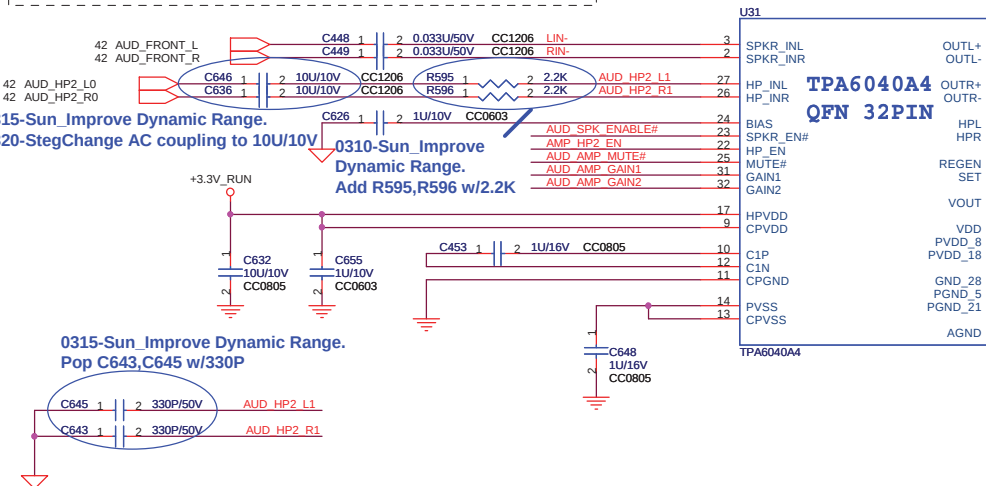
Layout Note:
TPA 4411 : cannot connect EP to GND.
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.



EMI Reserved



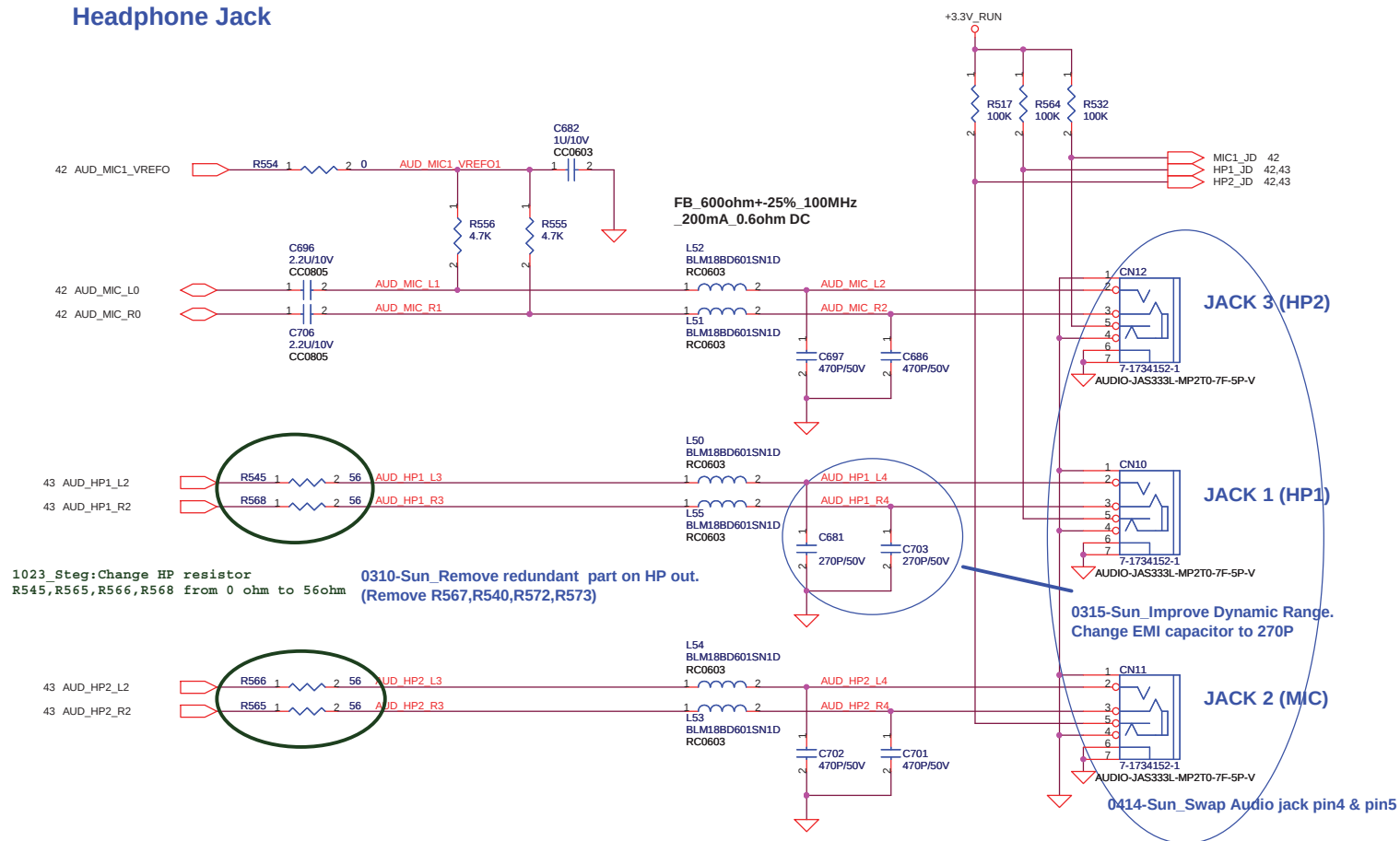
Layout Note:
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.
TPA 4411 : cannot connect EP to GND.
MAX 4411: can connect EP to GND.



Layout Note:
Place close pin 30.

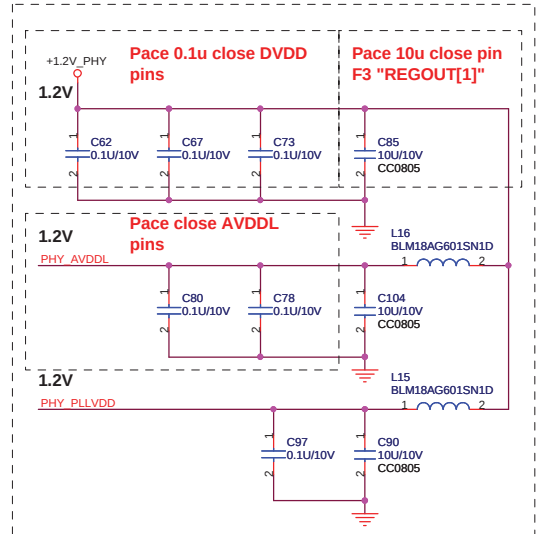
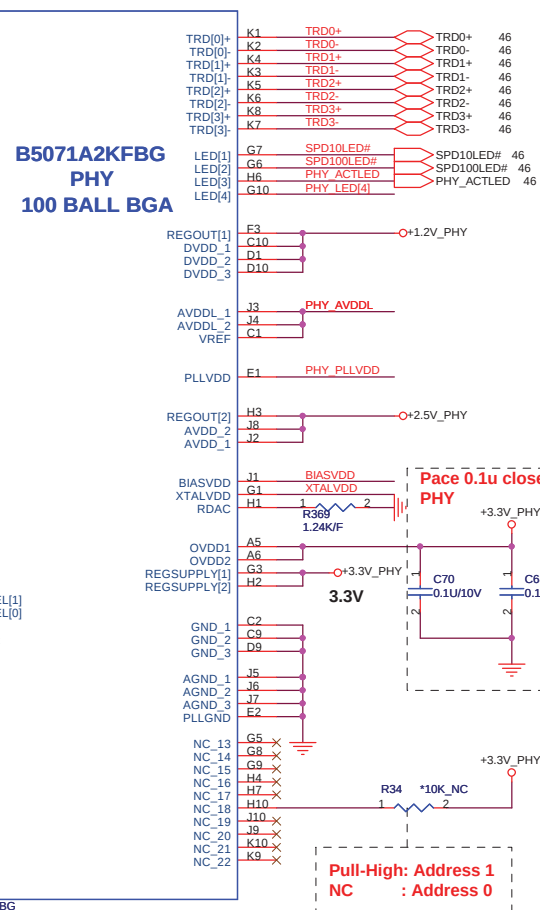
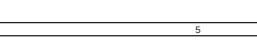
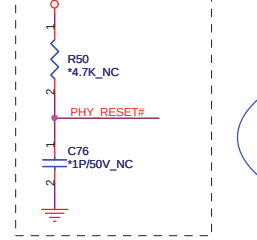
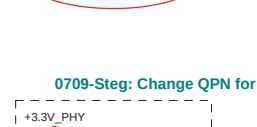
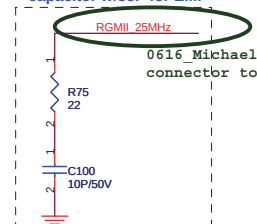
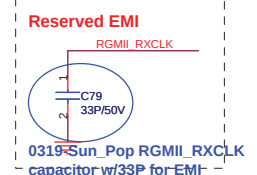
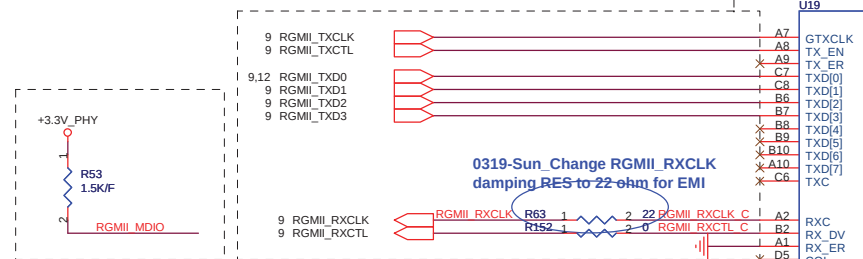
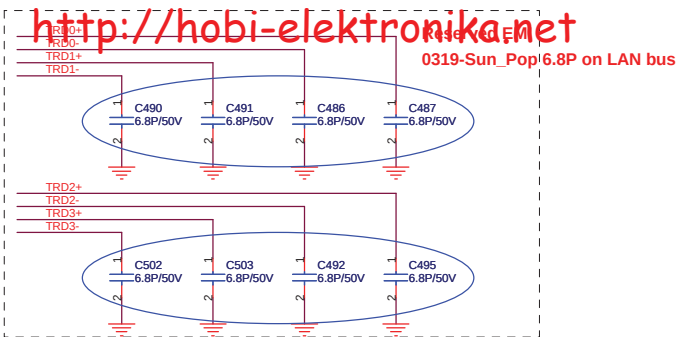


Headphone Jack

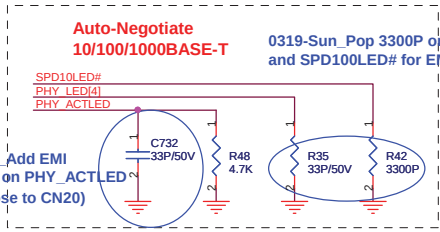
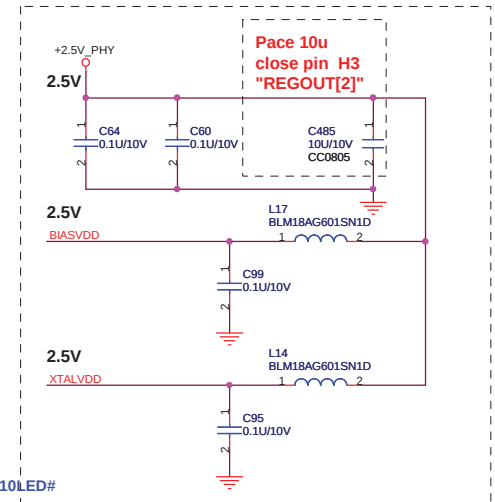


Layout Note:

1. Use 50 ohm impedance for all trace.
2. Trace length matched to a tolerance of 9.8mm in order to keep the skew between signals less than 0.07ns.
3. The receive and transmit signals kept away from each other and other analog and clock signals to reduce crosstalk.



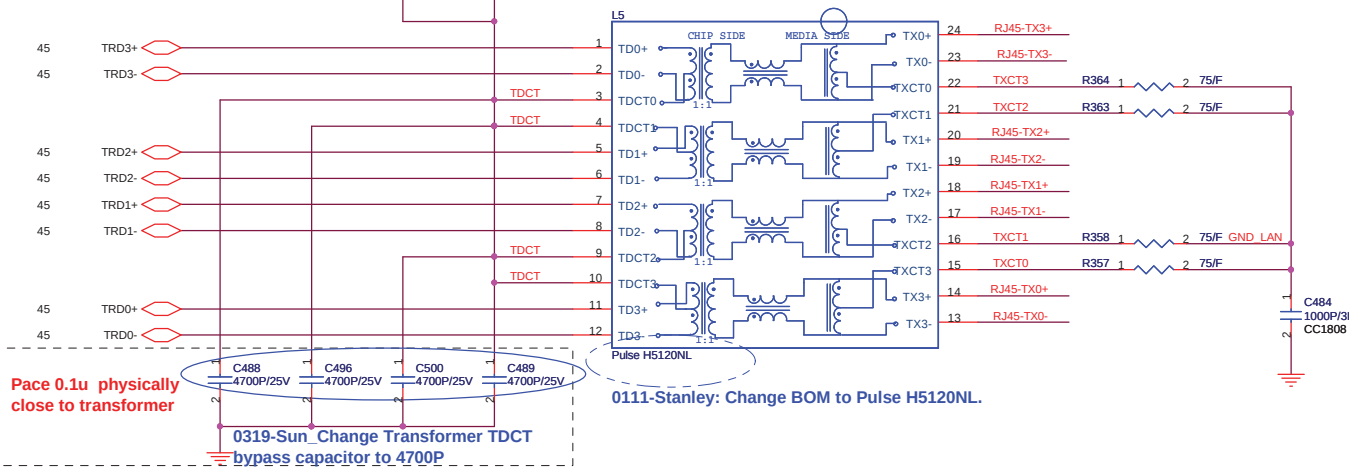
Layout Note:
Locate the RDAC resistor as close to the RDAC pin as possible and keep the trace between the pin and resistor and short and wide as possible.



0311-Sun_Add EMI capacitor on PHY_ACTLED# (Place close to CN20)

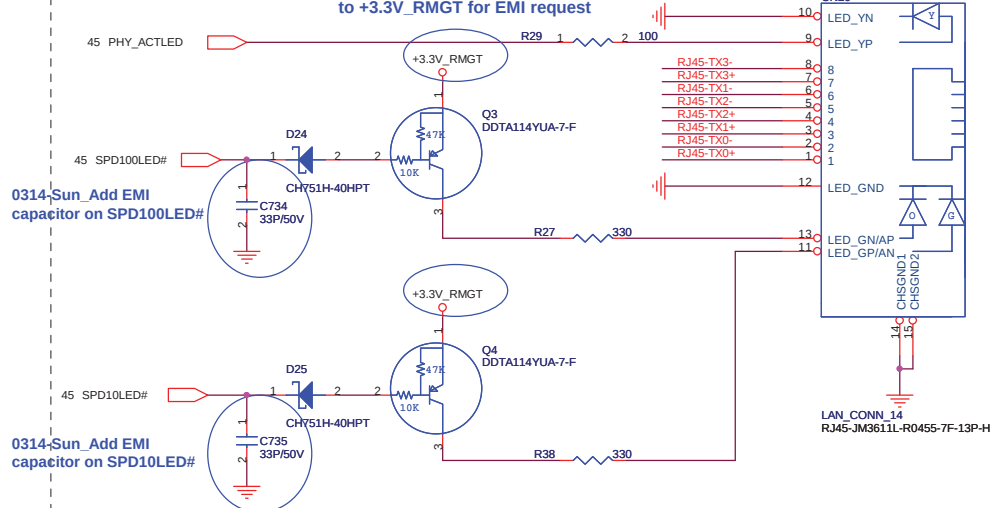
TRANSFORMER

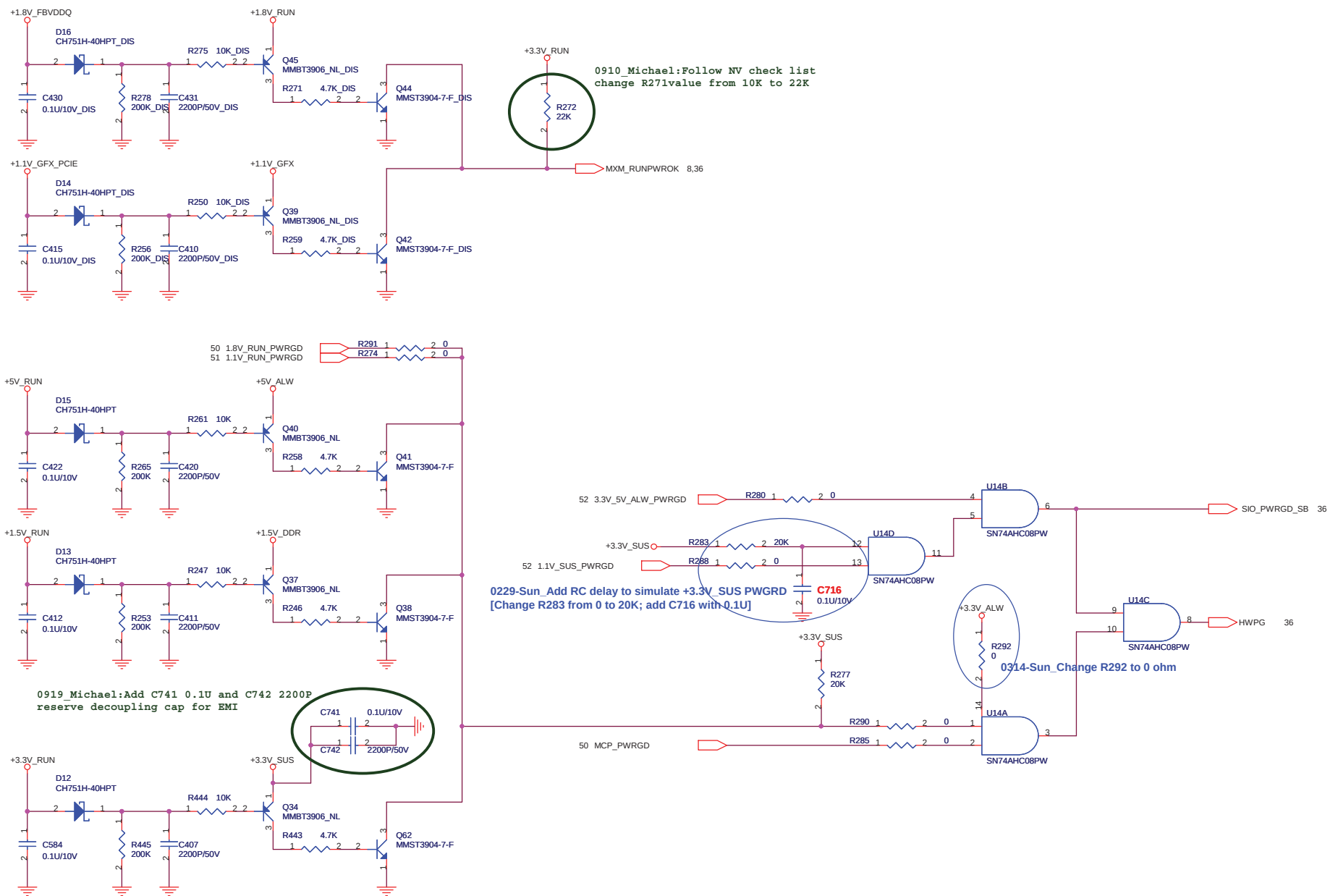
Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.



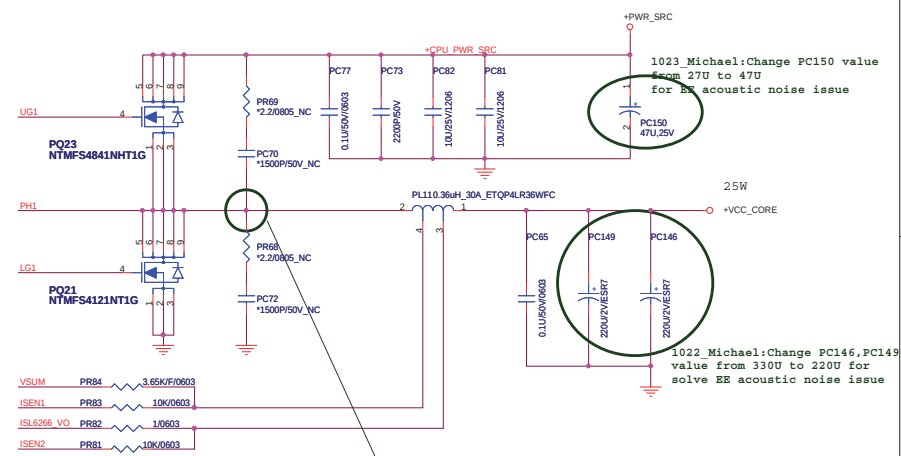
RJ-45 Connector

0314-Sun_Change RJ45 LED power to +3.3V_RMGT for EMI request

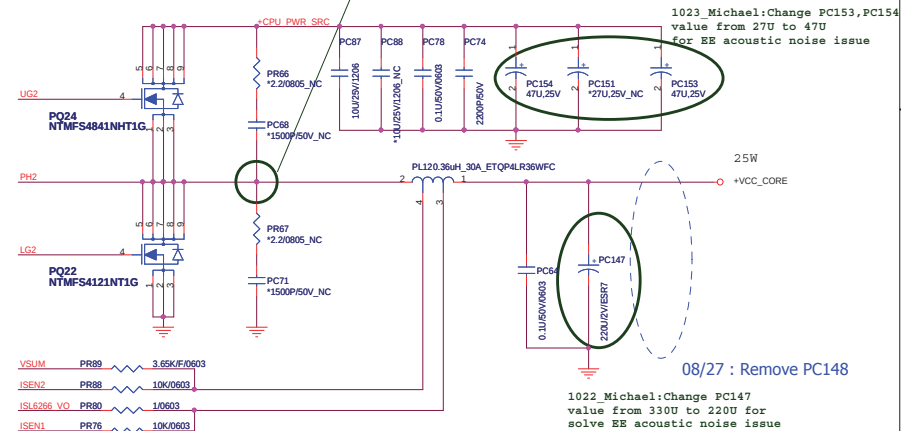








0916 Rick:Change connector from GND to PH for wrong circuit

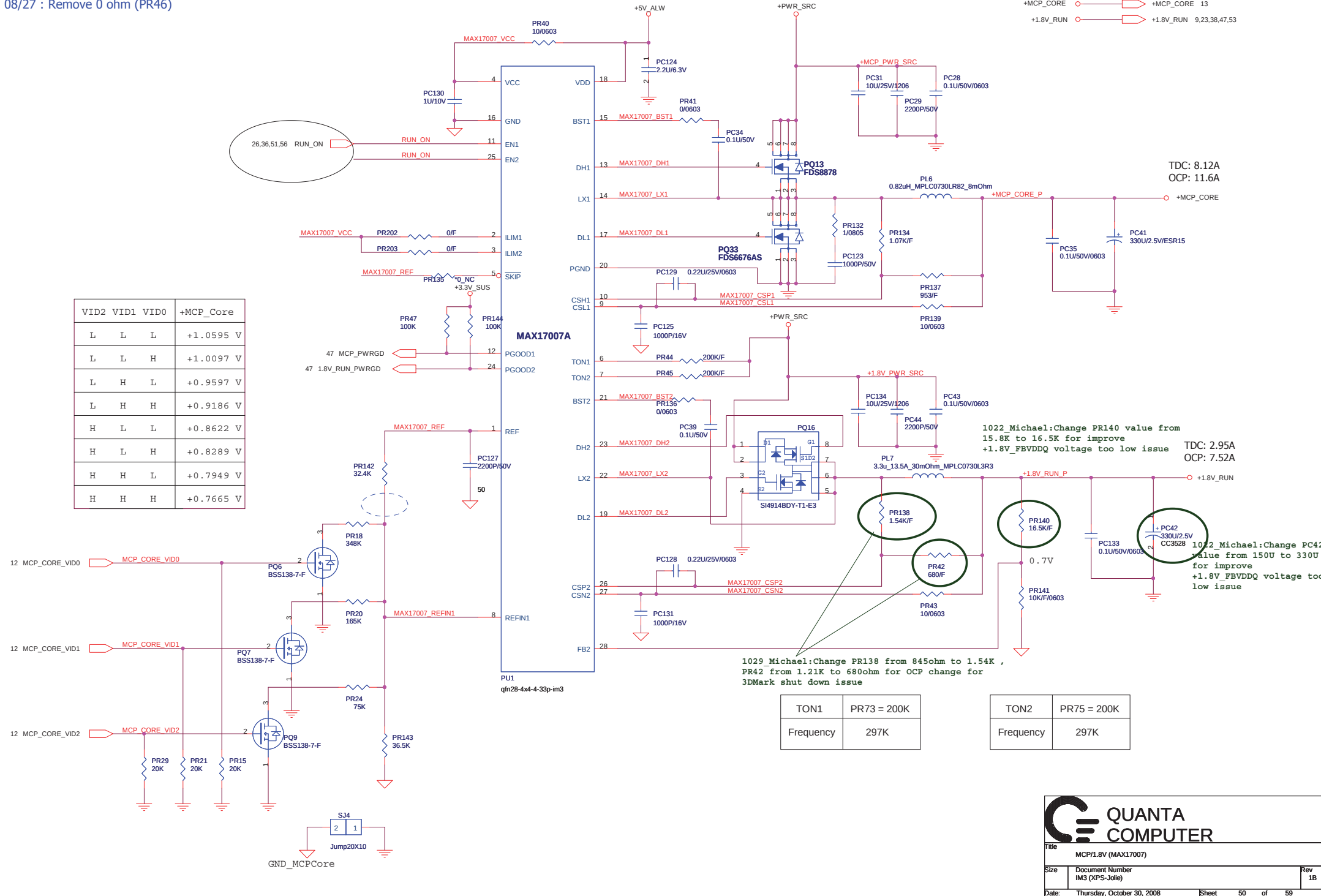


VW	PR37
Frequency	270KHZ@0A / 310KHZ@44A

0904_Rick:Change PC111 value
form 0.022uF to 0.068uF for transient change
1020_Rick:Change PC111 type from
0.068uF 0402 to 0.15uF 0603

Close to Phase 1 Inductor

08/27 : Remove 0 ohm (PR46)



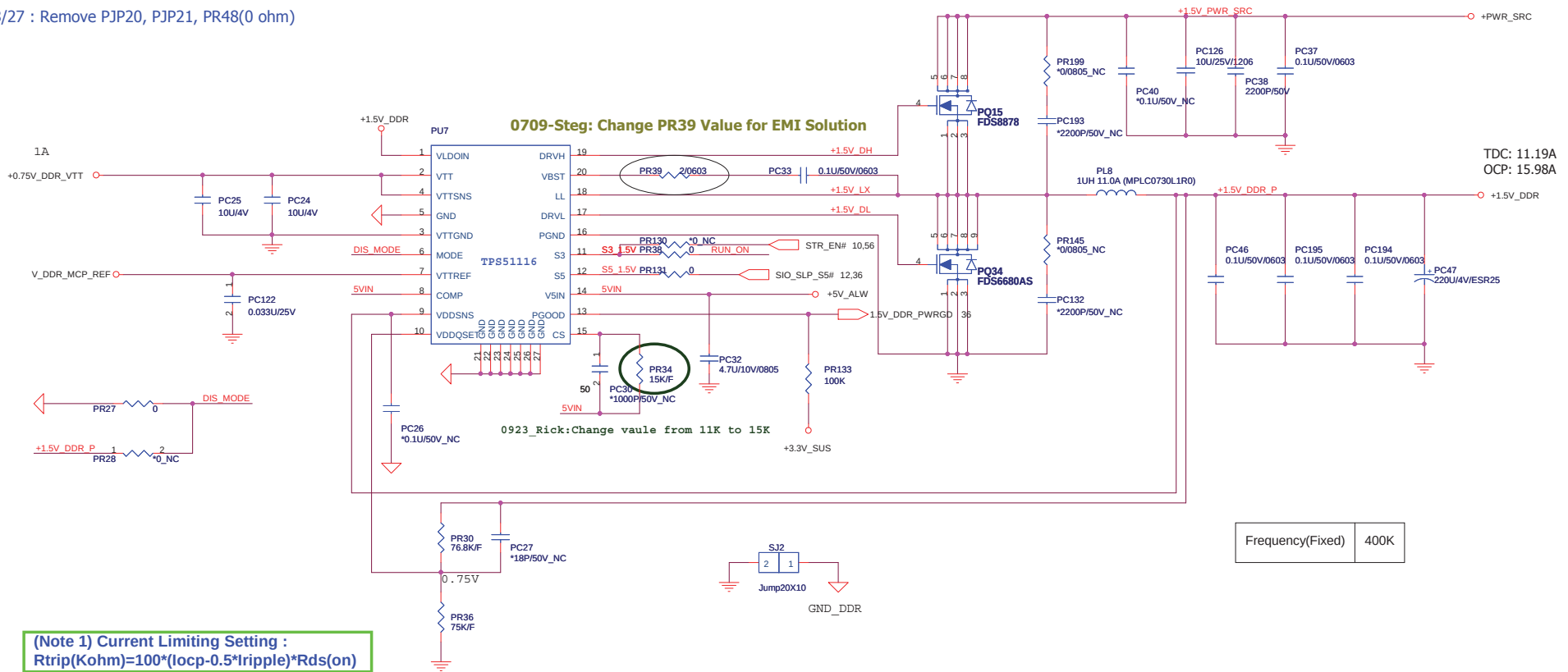
VID2	VID1	VID0	+MCP_Core
L	L	L	+1.0595 V
L	L	H	+1.0097 V
L	H	L	+0.9597 V
L	H	H	+0.9186 V
H	L	L	+0.8622 V
H	L	H	+0.8289 V
H	H	L	+0.7949 V
H	H	H	+0.7665 V

TON1	PR73 = 200K
Frequency	297K

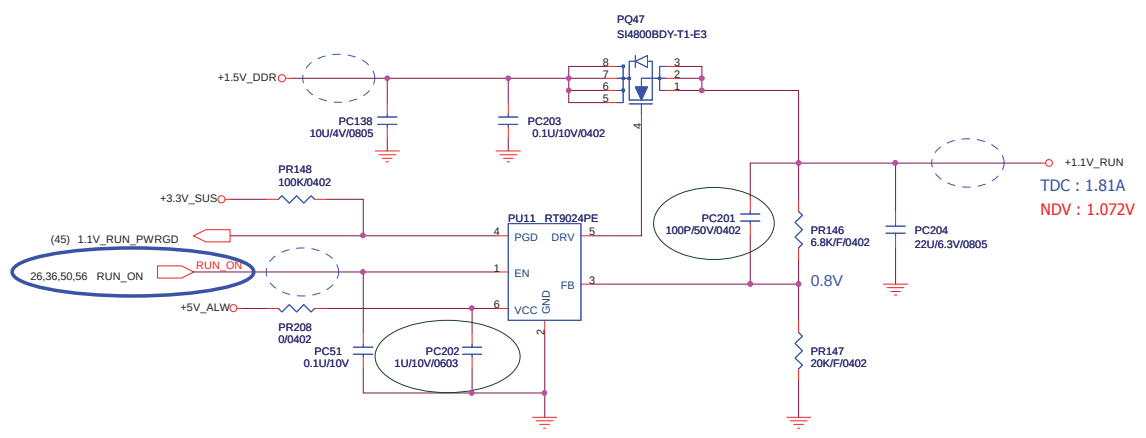
TON2	PR75 = 200K
Frequency	297K

+1.5V_DDR ○ → +1.5V_DDR 15,16,47,56
 +0.75V_DDR_VTT ○ → +0.75V_DDR_VTT 15,16,56
 +1.1V_RUN ○ → +1.1V_RUN 5,7,8,9,11,12
 V_DDR_MCP_REF ○ → V_DDR_MCP_REF 15,16

08/27 : Remove PJP20, PJP21, PR48(0 ohm)

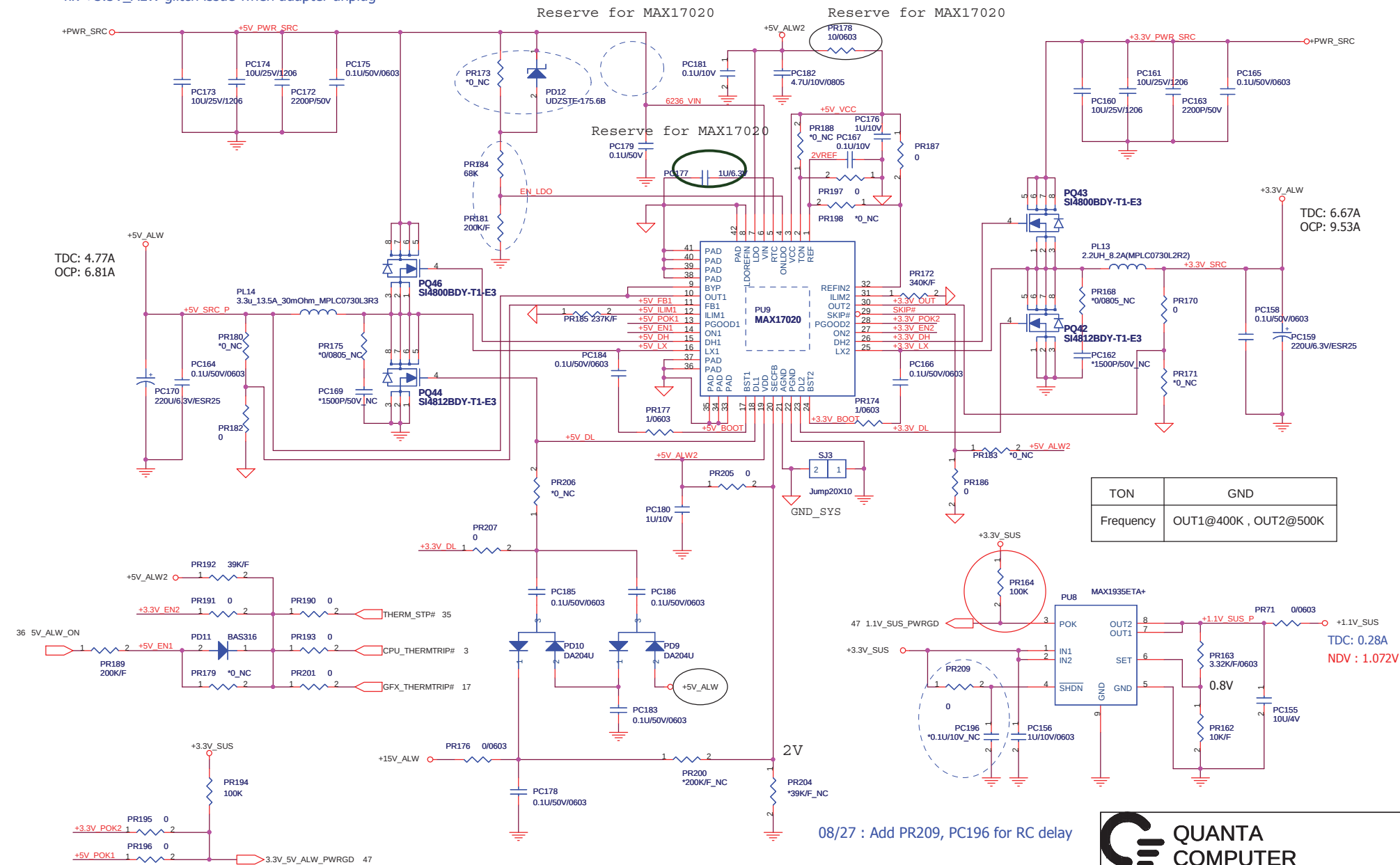


(Note 1) Current Limiting Setting :
 $R_{trip(Kohm)} = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$



0916 Rick:Change PC177 value from 0.1U to 1U

08/27 : Add Zener Diode (PD12), PR173 and change PR184=68K, PR181=200K to fix +3.3V_ALW glitch issue when adapter unplug



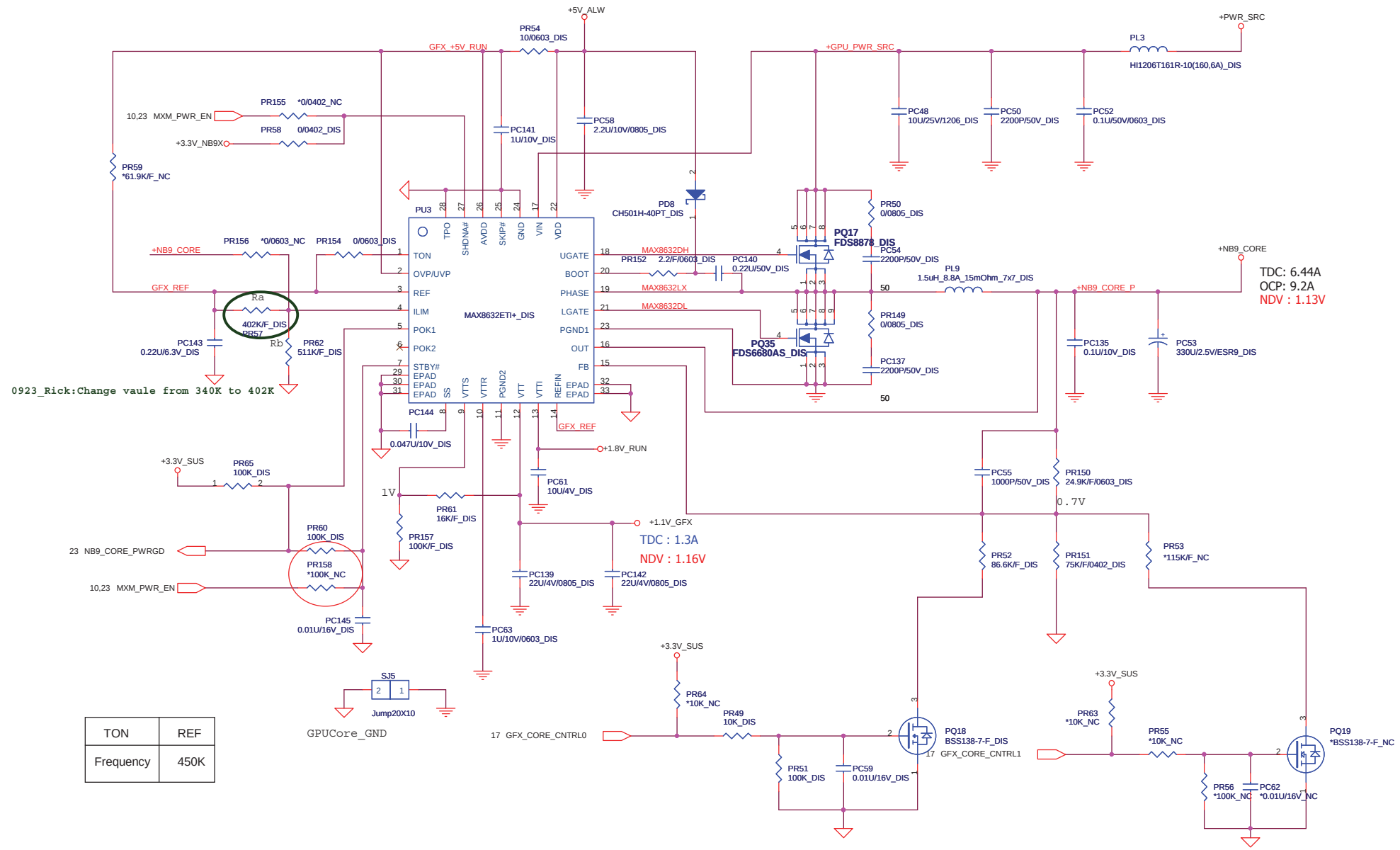
08/27 : Add PR209, PC196 for RC delay



QUANTA
COMPUTER

Title				SYS 5V/3V(MAX17020)			
Size	Document Number						Rev
	IM3 (XPS-Jolie)						1/
Date:	Thursday, October 30, 2008			Sheet	52	of	59

+NB9_CORE 20
+1.1V_GFX 23,47



TDC: 6.44A
OCP: 9.2A
NDV: 1.13V

TDC: 1.3A
NDV: 1.16V

TON	REF
Frequency	450K

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+NB9_CORE
LOW	LOW	0.9
HIGH	LOW	0.9
HIGH	HIGH	1.1V

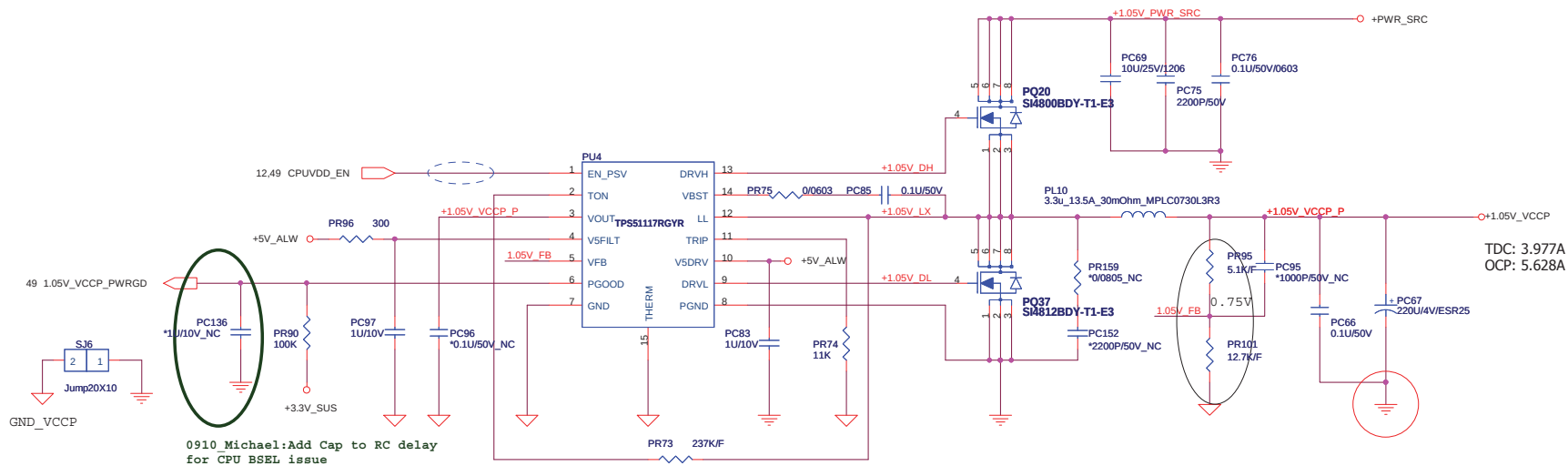
ILIM	$I_{ovp} = (2 * (R_b / (R_a + R_b)) * 0.1 * (1 / R_{DS(on)}) + (I_{\Delta} / 2)$
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVF	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

**QUANTA
COMPUTER**

Title		VGA DC/DC
Size	Document Number	Rev
	IM3 (XPS-Jolie)	1A
Date:	Tuesday, October 26, 2008	Sheet 53 of 59

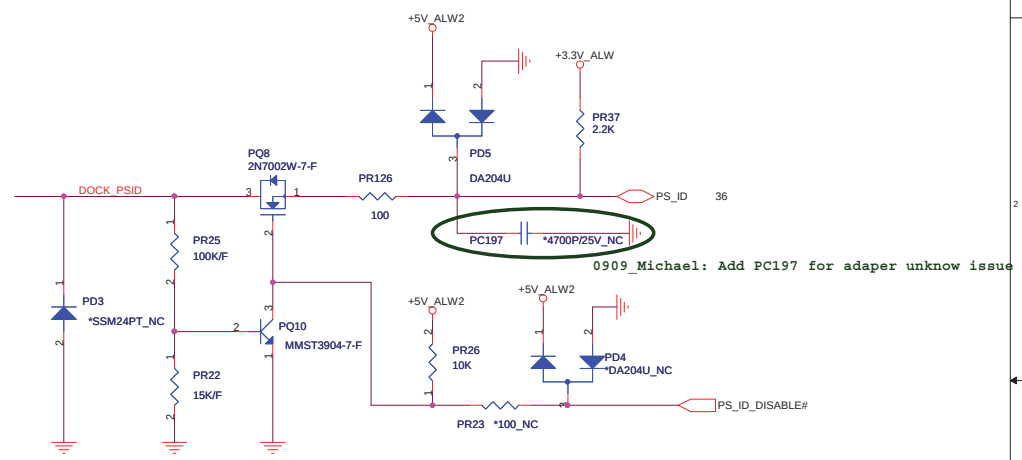
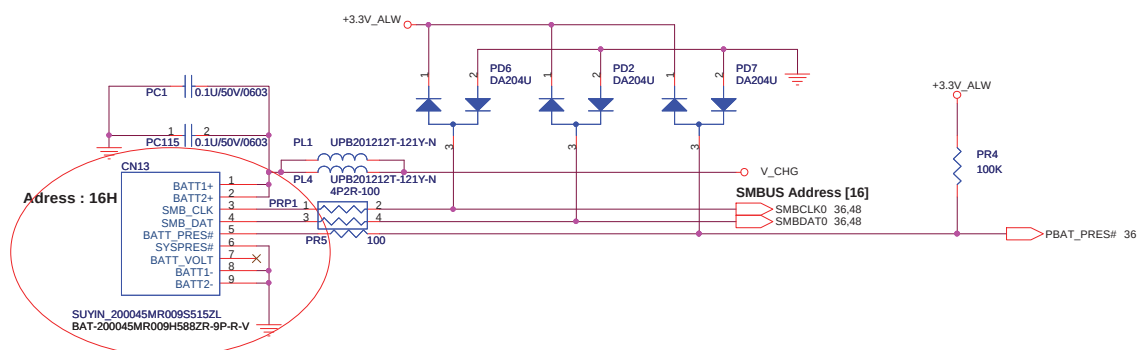
+1.05V_VCCP

08/27 : Remove 0 ohm (PR79)

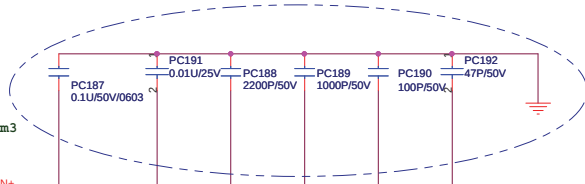


0910 Michael: Add Cap to RC delay for CPU BSEL issue

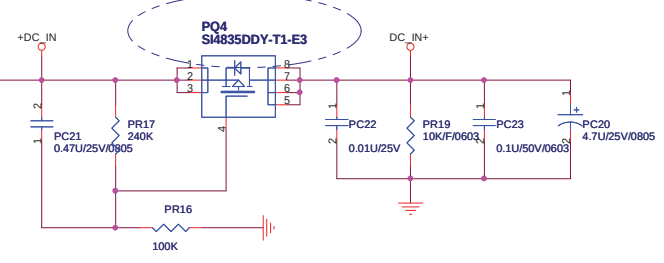
TON	PR185=237K
Frequency	300K



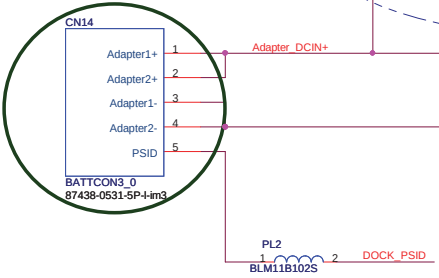
0311-Rick: Add PC187-PC192 for EMC

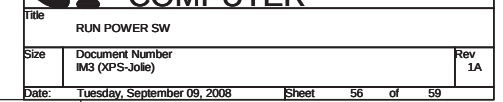
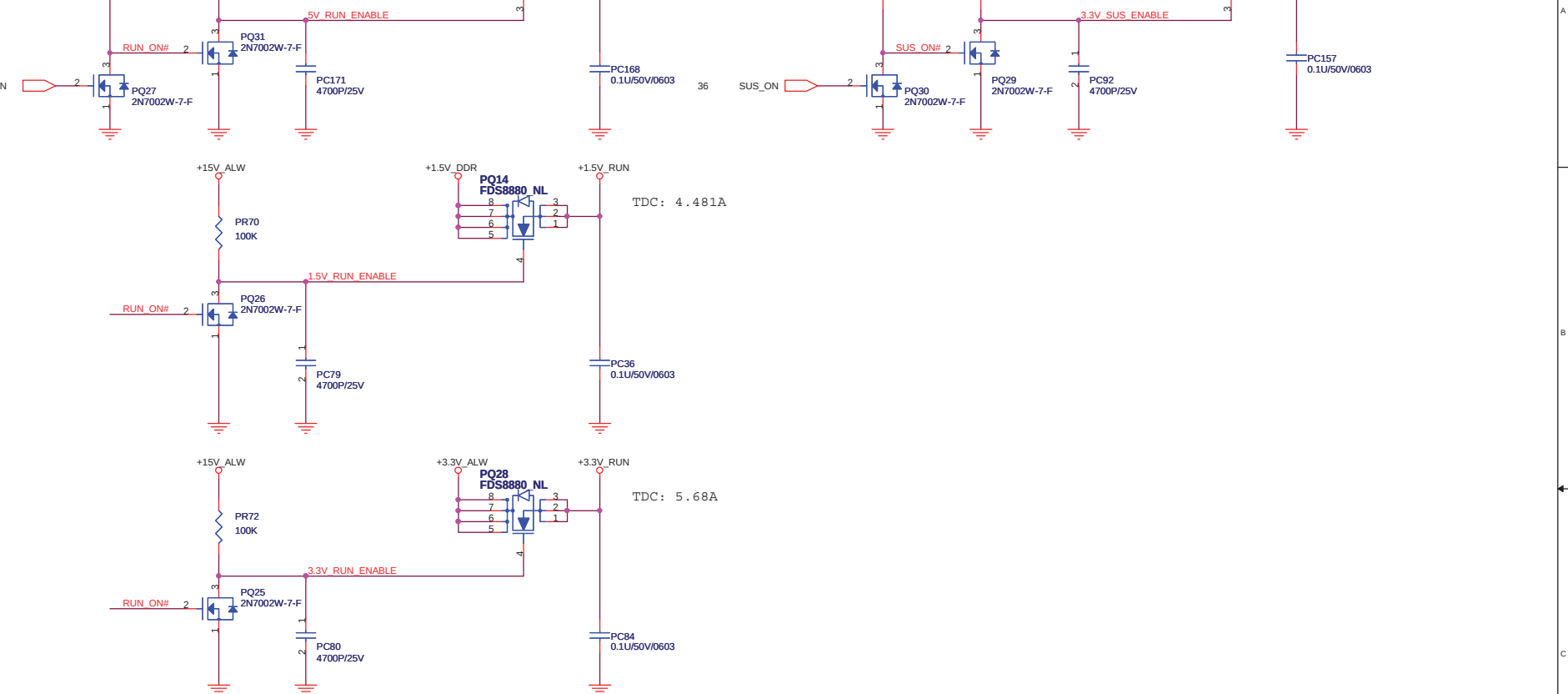


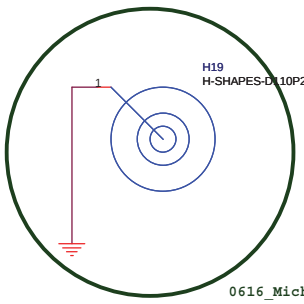
0709-Rick: Change PQ4 Value



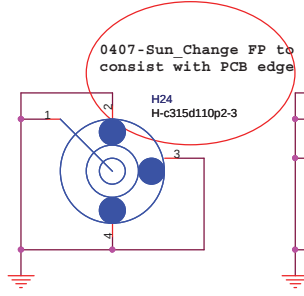
0823 Michael: Change Footprint from 87438-0531-5p-L to 87438-0531-5p-1-im3



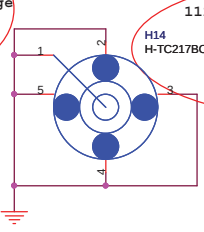




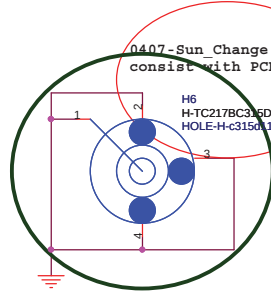
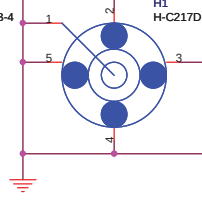
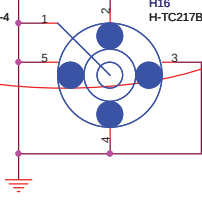
0616_Michael:Change footprint



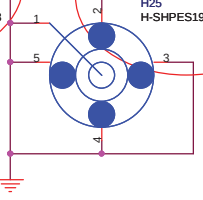
0407-Sun_Change FP to consist with PCB edge



1123-Sun_Change FP

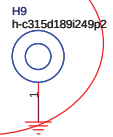
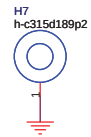


0407-Sun_Change FP to consist with PCB edge

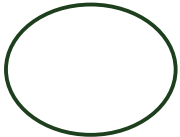
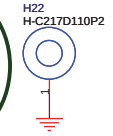
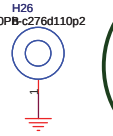
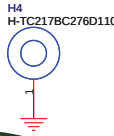
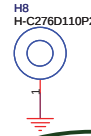
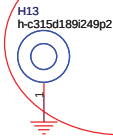


0407-Sun_Change FP to consist with PCB edge

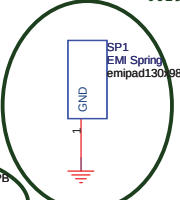
0616_Michael:Change footprint



1123-Sun_Change FP

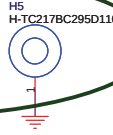
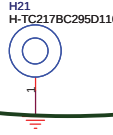
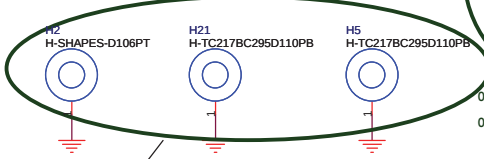
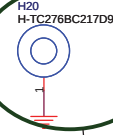
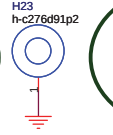
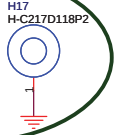
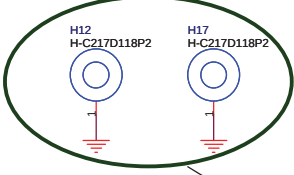


0829_Michael:Remove H3



0411-Sun_Add SP1

0605_Michael: Add connect to GND



0616_Michael:Change footprint