EV@ --- GPU only
MS@ --- iGPU & GPU Muxless
W@ --- Whistler GPU
G@ --- Granville GPU
DO@ --- 4 DIMM
SP@ --- Operation P/N

ZYF SYSTEM BLOCK DIAGRAM

GPU CORE PWR ISL6264 P44
CHARGER ISL88731 P37
GPU IO PWR ISL62827 P45
3/5V SYS PWR RT8206 P38
DISCHARGER +3V,+ 5V,+1.5V,+1.05V,+1.1V_VTT P46
CPU CORE PWR ISL62882 P39
+1.0V/+1.8V RT9018A + TPS54418 P47
CPU VTT ARD: 1.05V CFD: 1.1V UP61111AQDD P411
CPU VGFX_AXG ISL62881 P40
VTT 1.05V UP61111AQDD P41
THERMAL PROTECTION P47
DDR3 PWR RT8207A P42

BCLK: 133MHz
PEG_CLK: 100MHz
DPLL_REF_SSCLK: 120MHz

intel
<MCH Processor>
Sandy Bridge
rPGA 989
(37.5mm X 37.5mm)
P3.4.5.6
DDR SYSTEM MEMORY
PCI-E X16
FDI
DMI

Fan Driver (PWM Type) P35
CPU XDP Conn. P17

DDR III
SO-DIMM 0
SO-DIMM 1
SO-DIMM 2
SO-DIMM 3
P13,14, 15, 16
Dual Channel
1066/ 1333 MHz
800 MT/s 1066 MT/s

PCIE
2.5GT/s
AMD GPU
Granville-Pro / Whistle-Pro
2GB/1GB
(128Mb/64Mb x 32 IO x 8 pcs)
P18,19,20,21,22,23,24,25
CRT
LVDS
LVDS_CRT Switch Grapgics P26
CRT P26
LVDS P26
X'TAL 27.0MHz

FDI interface
X4 DMI interface

intel
<PCH>
FDI
DMI
Graphics Interfaces
INT_CRT
INT_LVDS
INT_HDMI
HDMI
HDMI P27

Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3

HDD (SATA) *2 P28
SATA0
SATA1
SATA5
SATA4
USB 2.0
Azalia
SATA
6.0 GT/s
SATA
3.0 GT/s
CougarPoint
USB
HDA
SPI
LPC
mBGA 989
(27mm X 25mm)
P7.8.9.10.11.12
PCI-E
RTC
P9
X'TAL 32.768KHz

eSATA Conn. USB 9 (Debug) P33
eSATA Buffer P33
ODD (SATA) P28
USB 2.0 Port x 3 USB 1, 3, 11, 12 (Debug) P33
Bluetooth USB 4 P34
CCD USB 8 P26
FingerPrint USB 2 P34

PCI-Express
2.5GT/s
PCIE-2
CLKOUT_PEG_3
USB3.0 Chip UPD720200F1 P34
USB 3.0 Conn . P34
PCIE-3 & 6
CLKOUT_PEG_1&2
PCIE-5
CLKOUT_PCIE2
PCIE-6
CLKOUT_PEG_B
Mini Card WLAN
USB 10
P29

Audio CODEC ALC669X P30
SPI ROM 4MB x1 (Basic ME+Braidwood) P8
EC (WPC791) P36
IEEE1394 & Media Cardreader JM388A P32
X'TAL 24.576MHz
IEEE1394a connector P32
Card Reader Connector P32
Realtek Giga-LAN RTL8111E P33 & Daughter Board
X'TAL 25MHz
Transformer Daughter Board
RJ45 Connector Daughter Board

SPI ROM P36
Touch Pad P35
K/B COON. P35
CIR P36

Front Stereo Amp (G1453L/ 2W+2W) P31
Center Mono Amp (G1442/ 2W) P30
Rear Audio Amp & Head phone TPA6047 P31
Sub-Amplifier (TPA311D1) P31
Front Speaker P31
Center Speaker P31
Speaker P31
S/PDIF P31
SUBWOOFER P31
Line in P31
MIC Jack P31
Int. D-MIC P31

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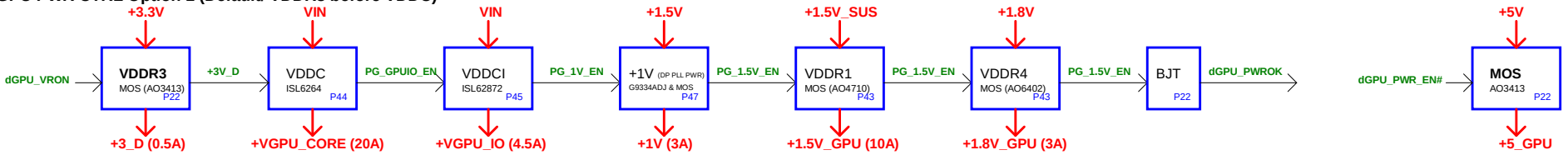
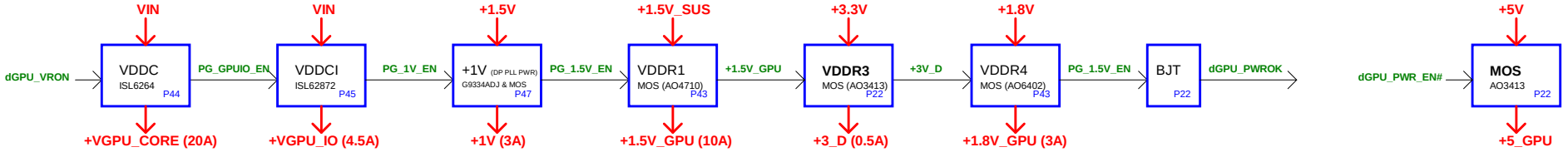
Size
Document Number
ZYF Block Diagram
Rev 1A
Date: Monday, November 08, 2010
Sheet 1 of 50

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



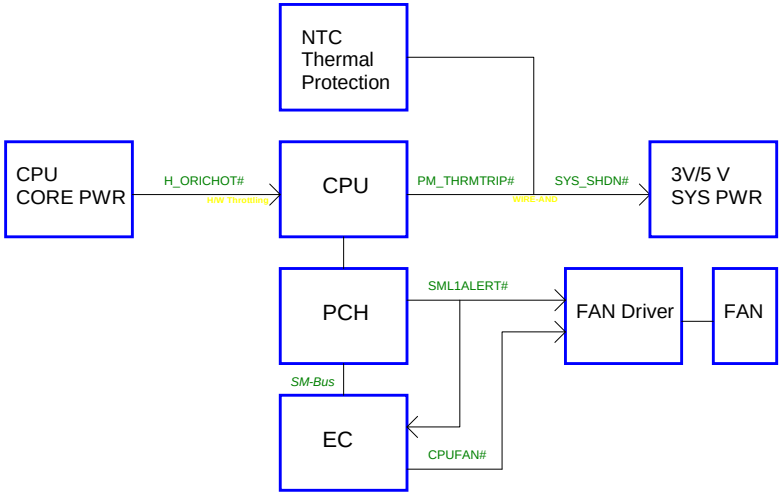
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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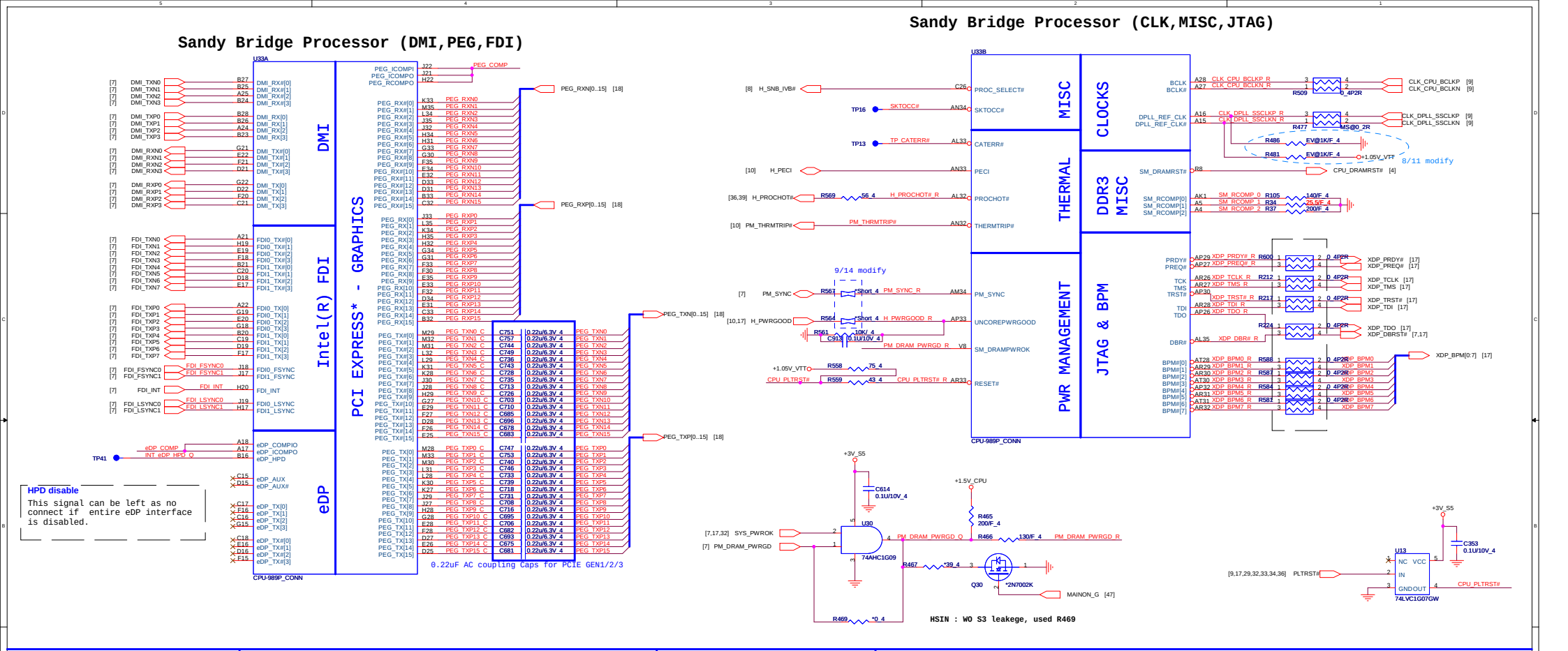
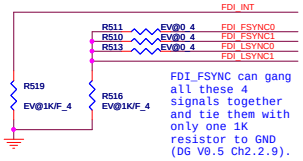
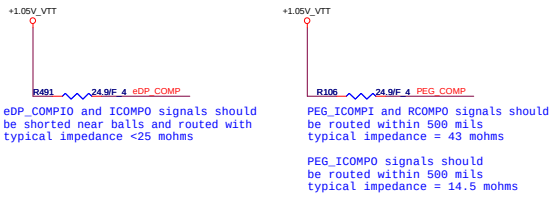


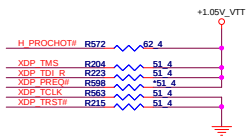
FDI Disabling (Discrete Only)

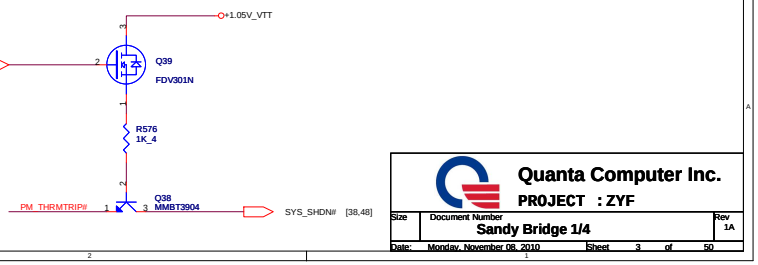


DP & PEG Compensation

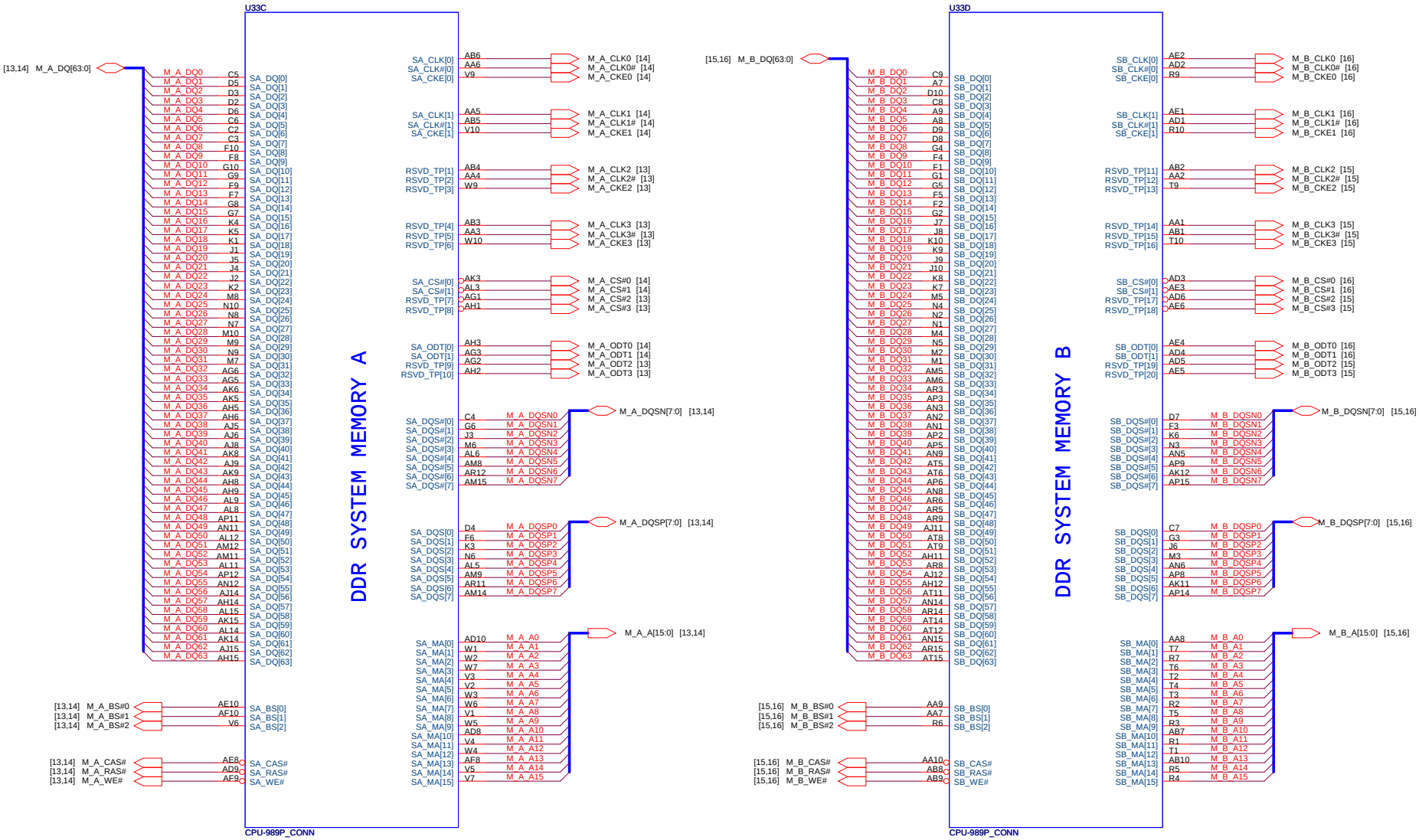


Processor pull-up(CPU)





Sandy Bridge Processor (DDR3)



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	Sandy Bridge 2/4	1A
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Sandy Bridge Processor (POWER)

CPU Core Power

SNB 45W:52A

Spec	Real
470uF/4mohm x 4	470uF/4mohm x 4
22uF x 16	22uF x 14
10uF x 10	10uF x 10

CPU VTT

SNB 45W:8.5A

Spec	Real
330uF/6mohm x 2	330uF/10mohm x 1
22uF x 12	22uF x 10
22uF x 7 (Non-stuff)	10uF x 2

CPU VCCPL

SNB 45W:1.5A

Spec	Real
330uF/7mohm x 1	10uF x 1
10uF x 1	1uF x 2
1uF x 2	

CPU VGT

SNB 45W:21.5A

Spec	Real
330uF/10mohm x 2	330uF/10mohm x 2
470uF/4mohm x 2	22uF x 8
22uF x 12	10uF x 6

Sandy Bridge Processor (GRAPHIC POWER)

CPU MCH

SNB 45W: 5A

Spec	Real
330uF/6mohm x 1	10uF x 8
10uF x 6	

CPU SA

SNB 45W: 6A

Spec	Real
330uF/7mohm x 1	10uF x 3
10uF x 3	

POWER

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

MISC

1.8V RAIL

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

8/3 del

8/5 del

8/17 modify

8/11 change 3528 type

8/17 change 3528 type

9/13 add

8/17add

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Close to VR

Place PU resistor close to CPU

SVID DATA

Close to VR

Place PU resistor close to CPU

SVID ALERT

6A/maximum

	E	MS
Ra	0 ohm	NA

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Sandy Bridge 3/4

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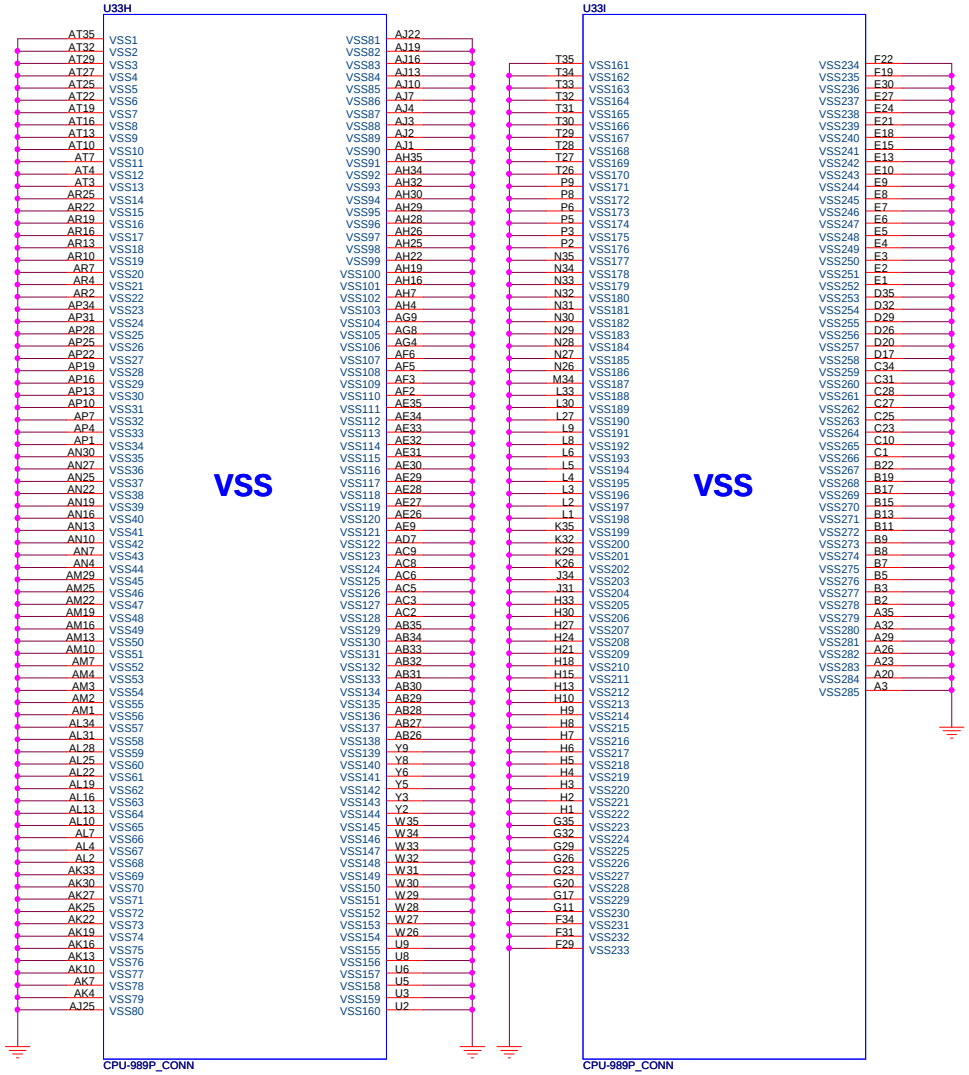
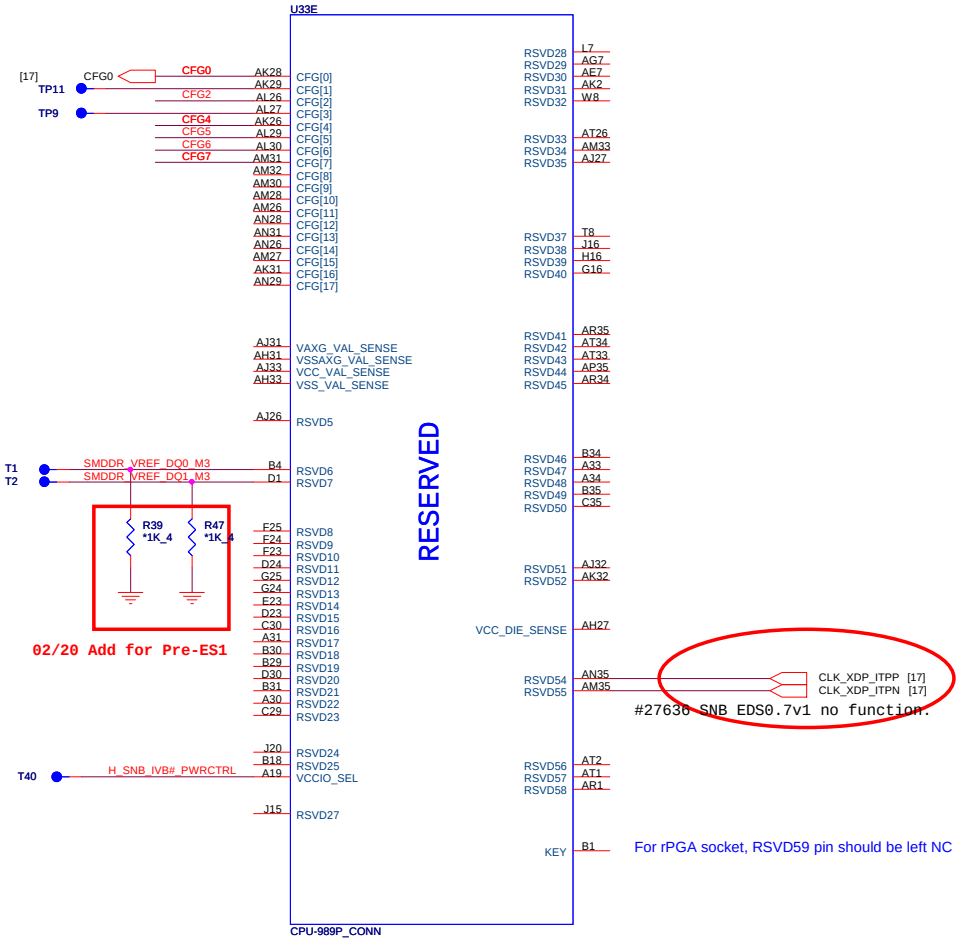
Sandy Bridge Processor (GND)



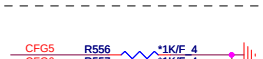
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	**Lane Reversed**
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Quanta Computer Inc.
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	Sandy Bridge 4/4	1A

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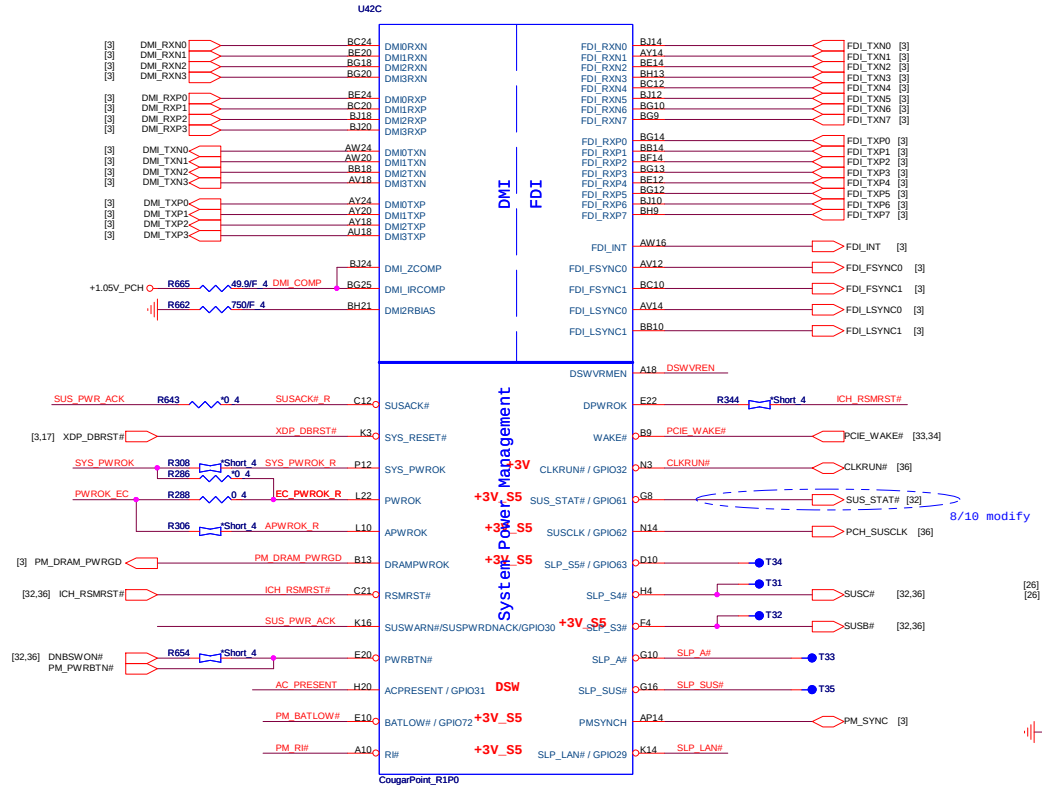
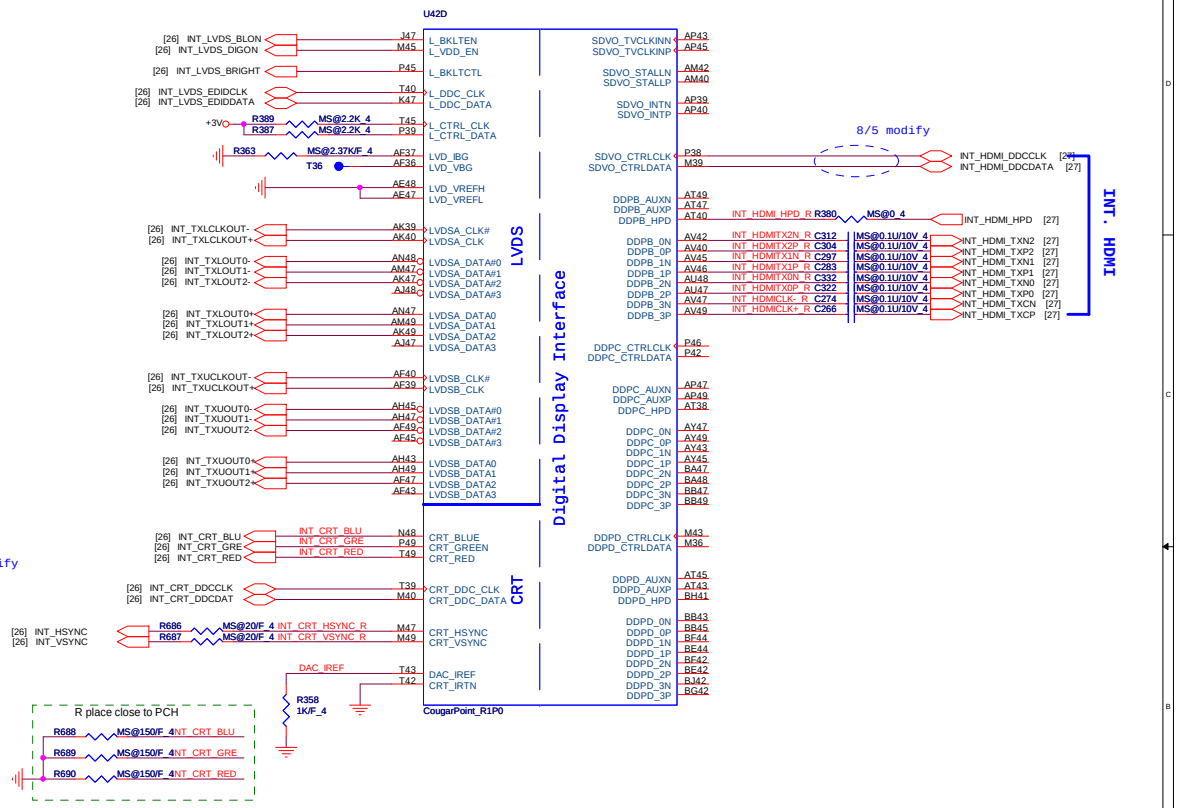
Cougar Point (DMI,FDI,PM)

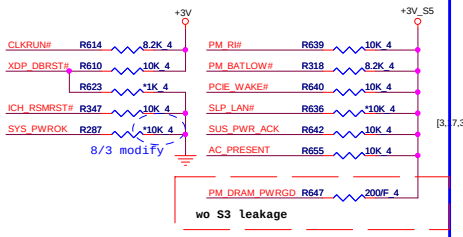


Cougar Point (LVDS,DDI)

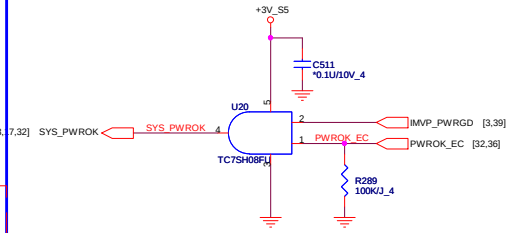


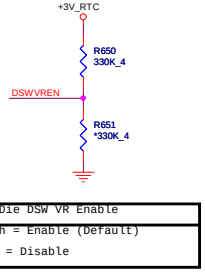
PCH Pull-high/low(CLG)

CRB 1.0 change R8315 to 1K



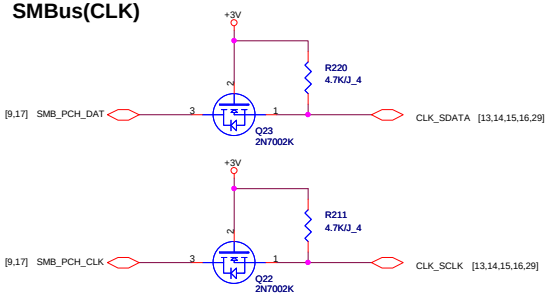
System PWR_OK(CLG)





On Die DSW VR Enable
High = Enable (Default)
Low = Disable

SMBus(CLK)



Quanta Computer Inc.
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	Cougar Point 1/6	1A
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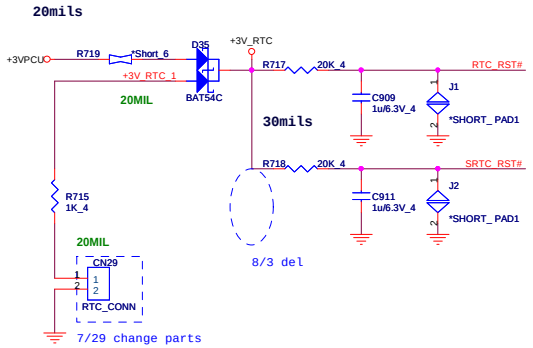
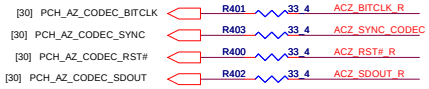
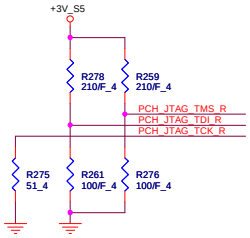
RTC Circuitry(RTC)



HDA Bus(CLG)

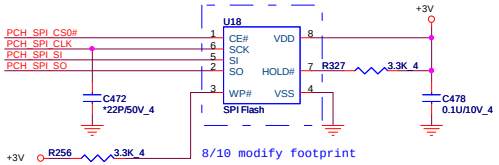


PCH JTAG Debug (CLG)



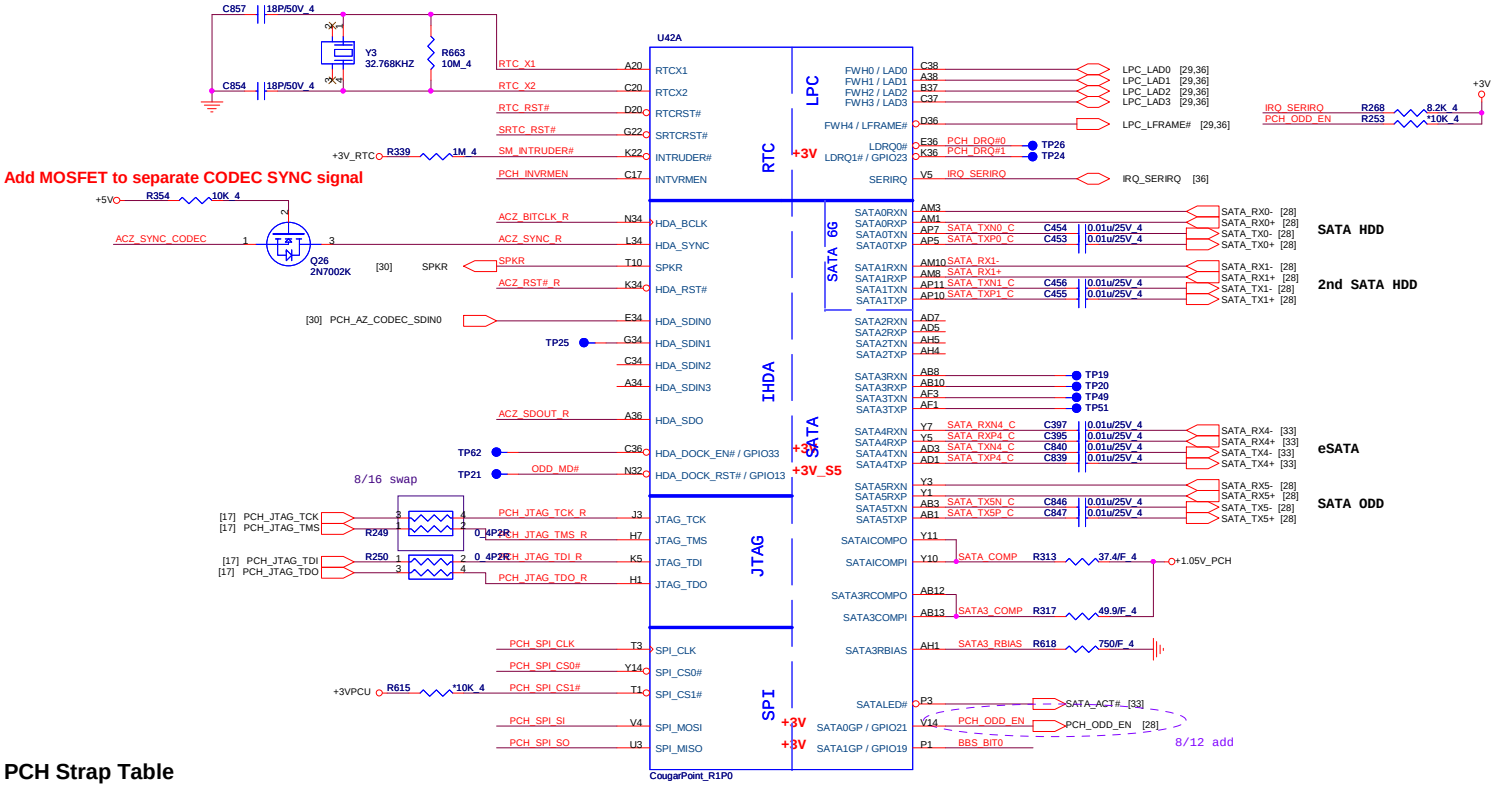
PCH Dual SPI (CLG)

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00



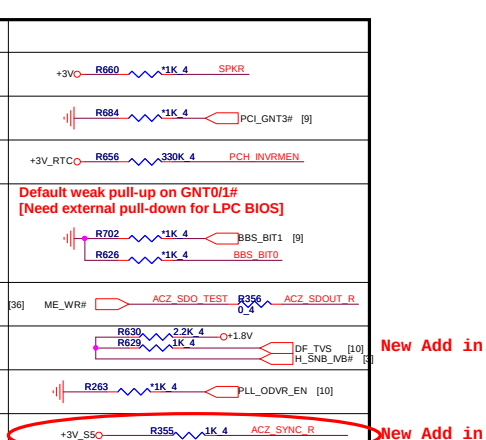
PCH2(CLG)

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)



New Add in CPT EDS Rev1.0 at 0316

New Add in CPT EDS Rev1.0 at 0316

3/16 Remove based on CPT EDS rev1.0

3/16 Remove based on CPT EDS rev1.0

3/16 Remove based on CPT EDS rev1.0

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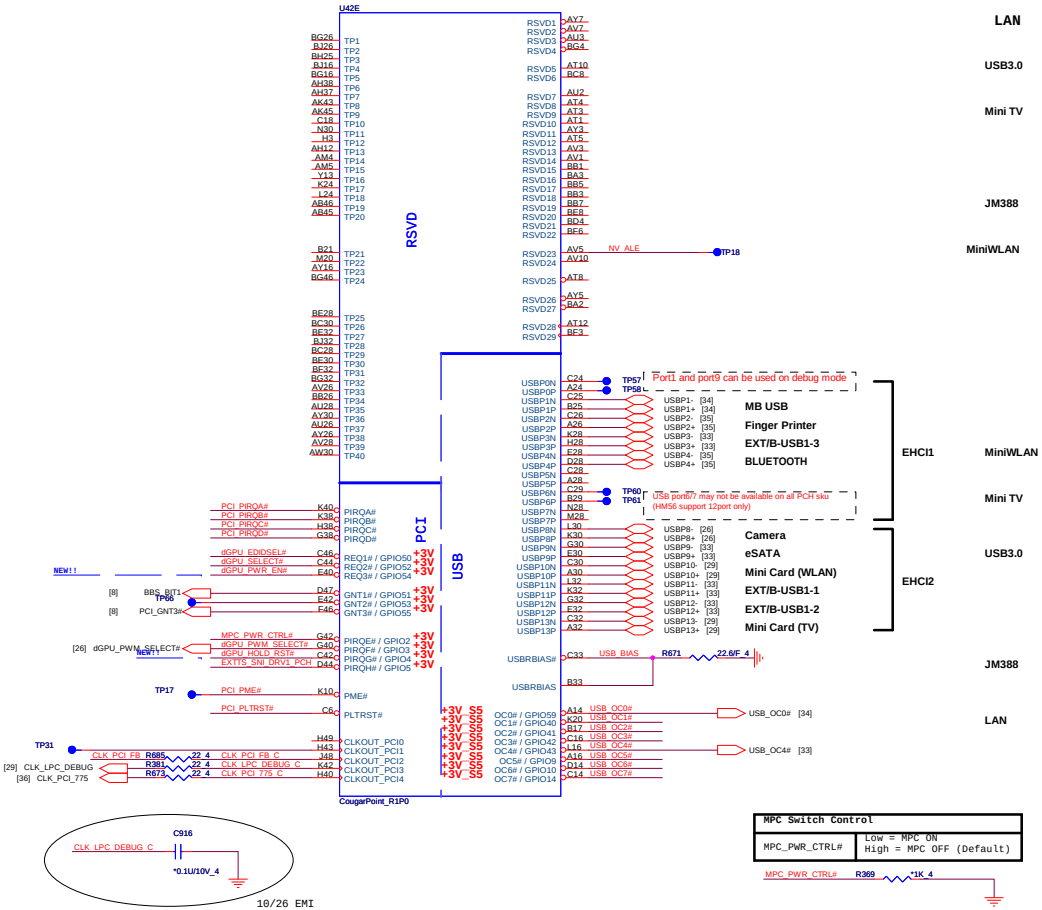
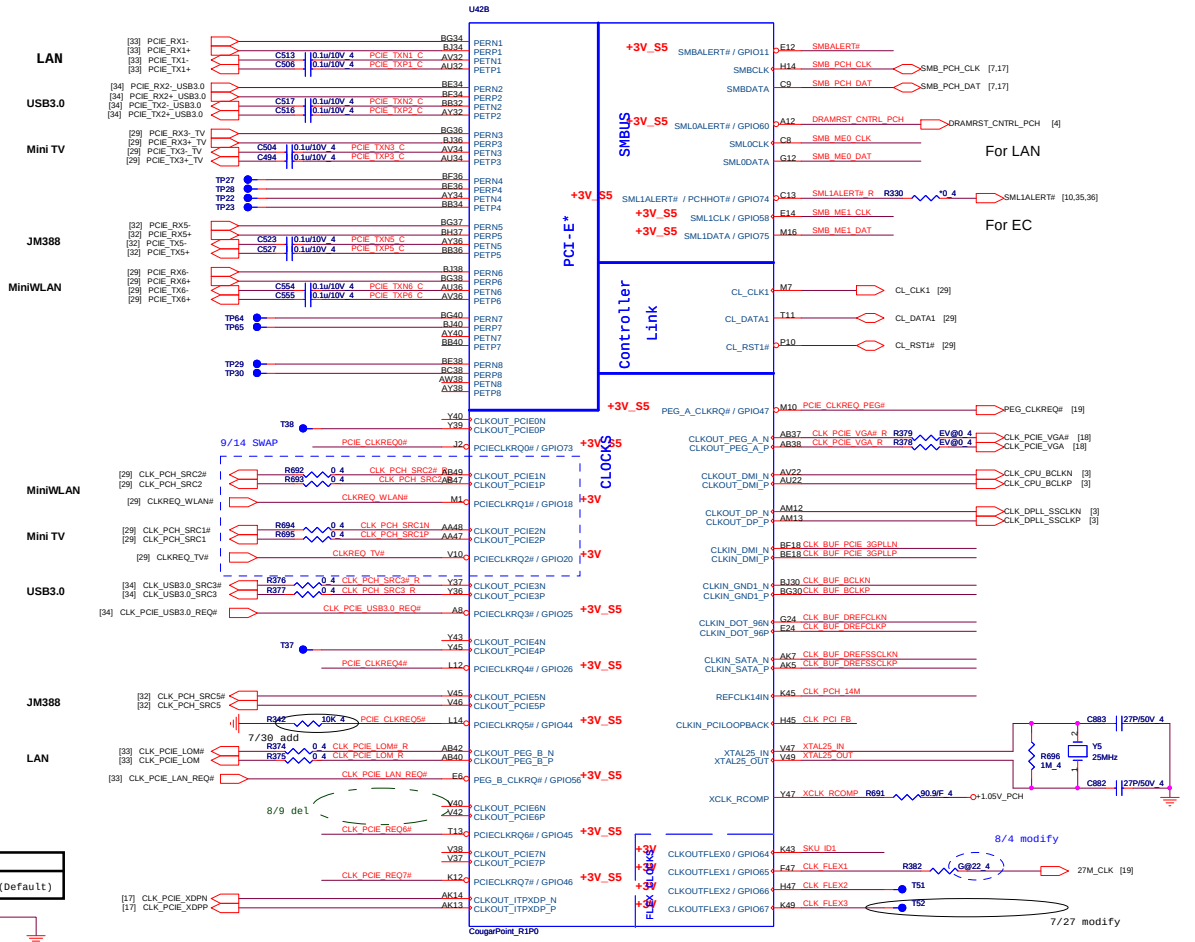
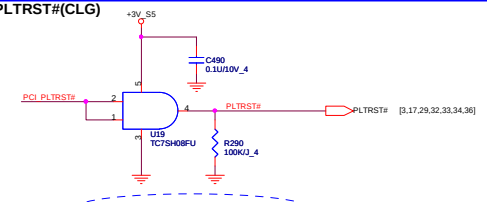
Cougar Point-M (PCI,USB,NVRAM)



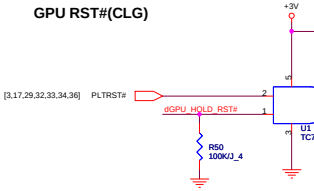
Cougar Point-M (PCI-E,SMBUS,CLK)



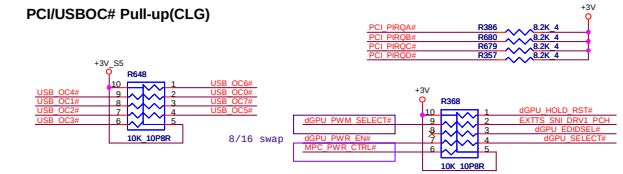
PLTRST#(CLG)



GPU RST#(CLG)



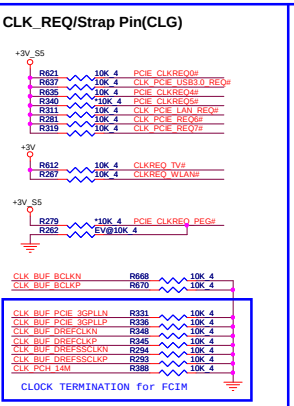
PCI/USBOC# Pull-up(CLG)



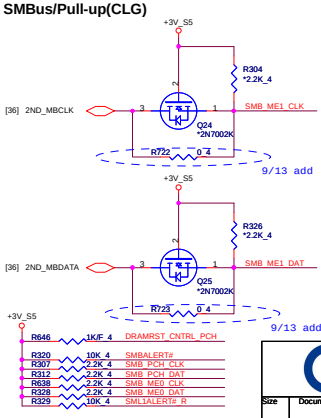
	DGPU_PW_CTRL# (GPIO68)	SKU_ID1 (GPIO53)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
Discrete Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	Discrete/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
1 = GPU power is control by H/W (pure Discrete SKU)

CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	Cougar Point 3/6	1A

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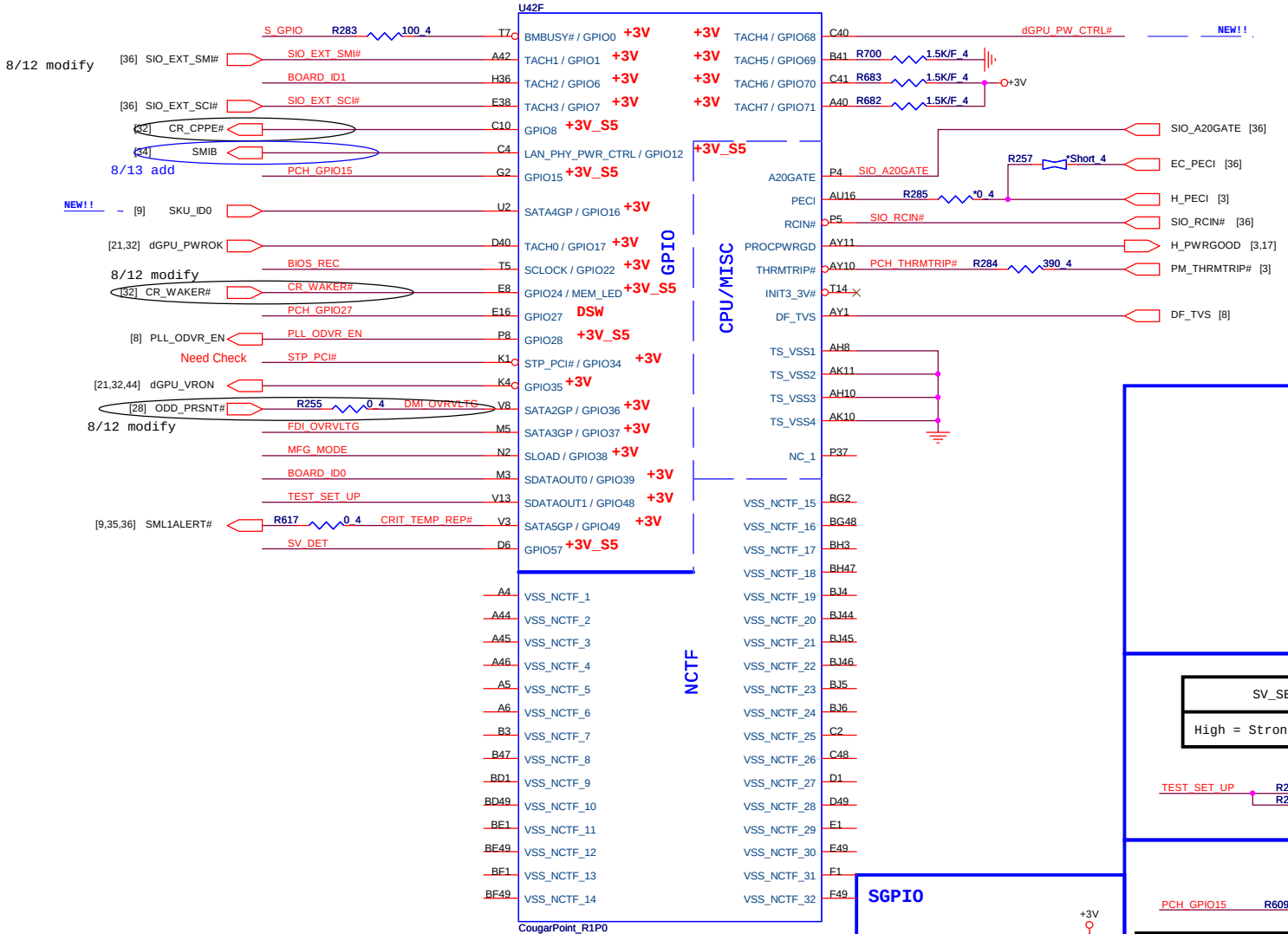
Cougar Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down(CLG)

8/16 modify

PD3 no PU, PD3 connect to EC

CR_WAKER# R298 10K_4
SMIB R296 *10K_4
PLL_ODVR_EN R280 10K_4

SIO_EXT_SMI# R701 10K_4
SIO_EXT_SCI# R359 10K_4
STP_PCI# R622 *10K_4
SIO_A20GATE R252 10K_4
SIO_RCIN# R251 10K_4
CRIT_TEMP_REP# R628 10K_4

8/16 modify

PCH_GPIO27 R335 *10K_4

SV_SET_UP
High = Strong (Default)

+3V_S5 R303 *10K_4 SV_DET R297 100K/J_4

TEST_SET_UP R266 10K_4 R291 *0_4

R624 *10K_4 BOARD_ID0 R611 *10K_4
R675 *10K_4 BOARD_ID1 R677 *10K_4

PCH_GPIO15 R609 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

NEW

high	GPU power is control by H/W (pure Discrete SKU)
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

R699 *10K_4 dGPU_PW_CTRL# R681 100K/F_4

SGPIO

S_GPIO R254 1K/F_4 R265 *0_4

R260 100K/J_4 FDI_OVRVLTG R277 *10K_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI_OVRVLTG R292 200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS_REC R282 10K_4 R264 *0_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

MFG_MODE R613 10K_4 R625 *0_4

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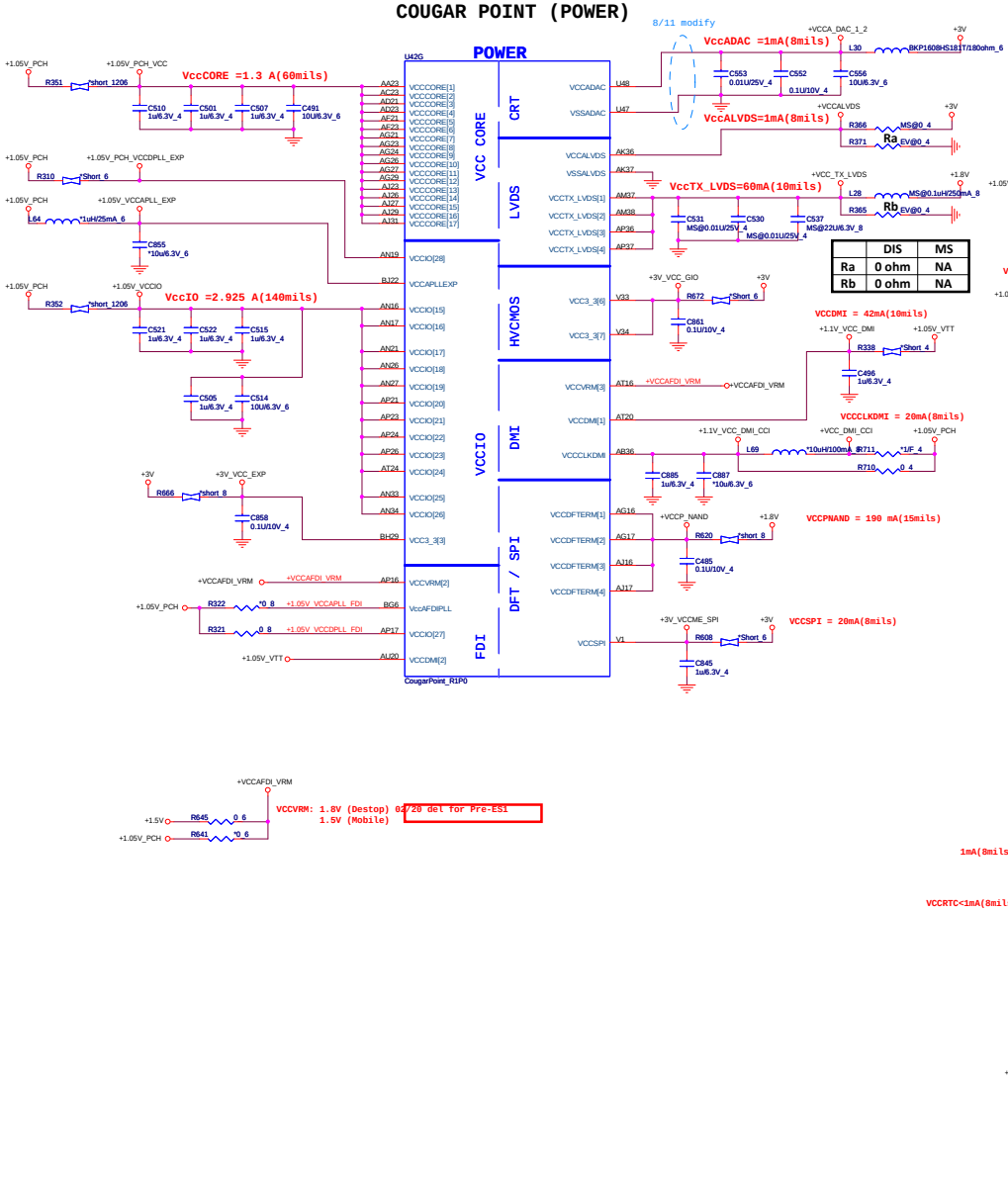
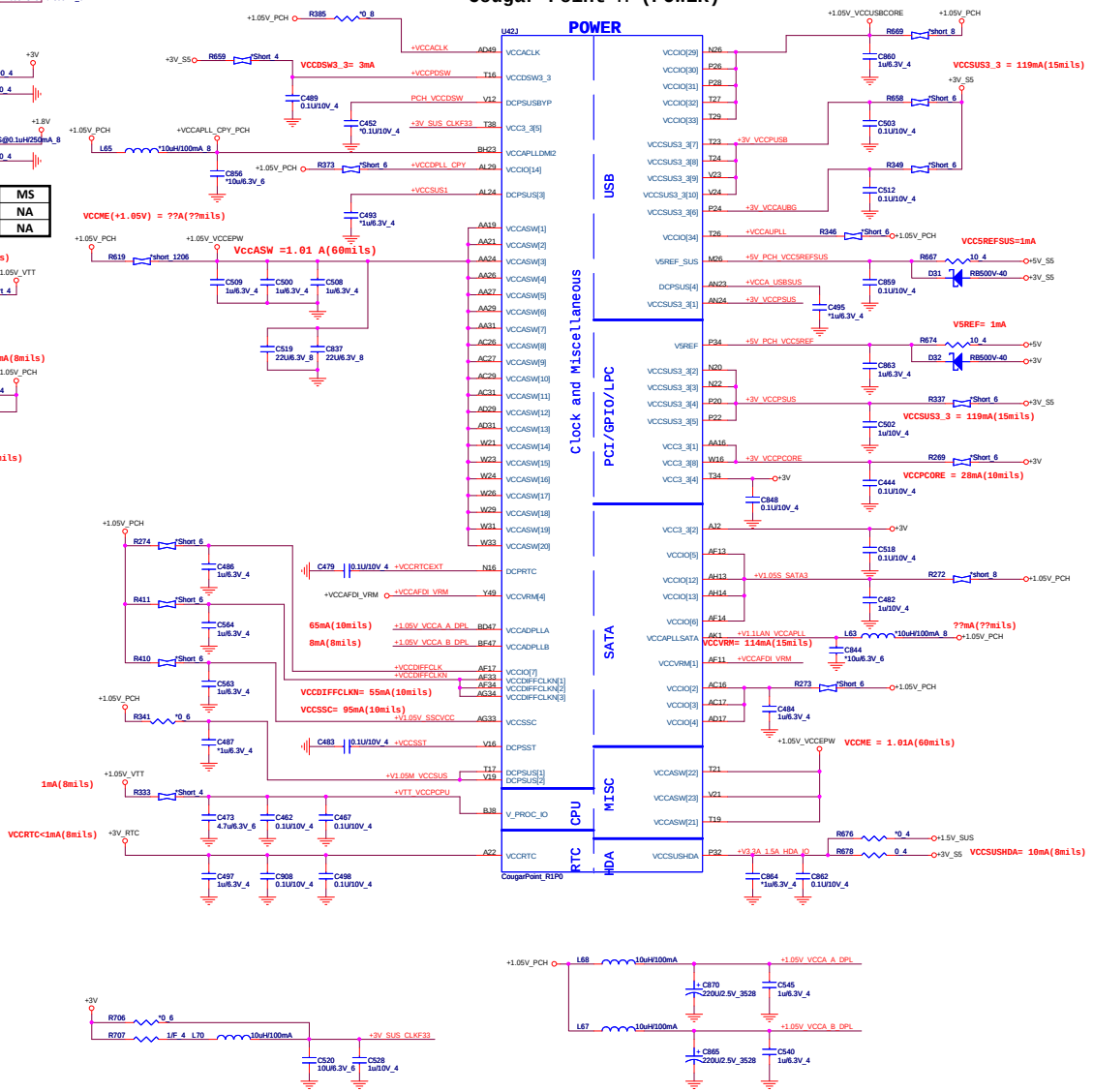
PCH5(CLG)

COUGAR POINT (POWER)



Cougar Point-M (POWER)



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	Cougar Point 5/6	1A
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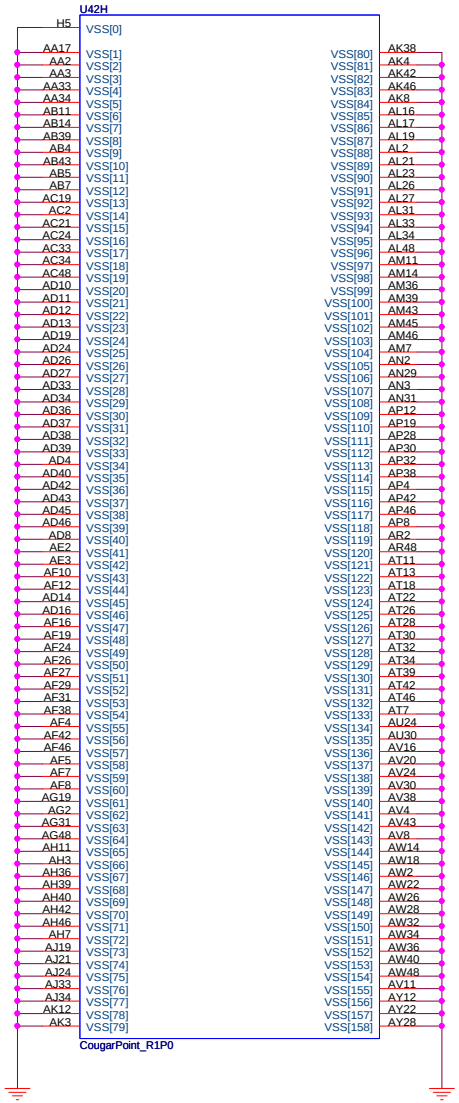
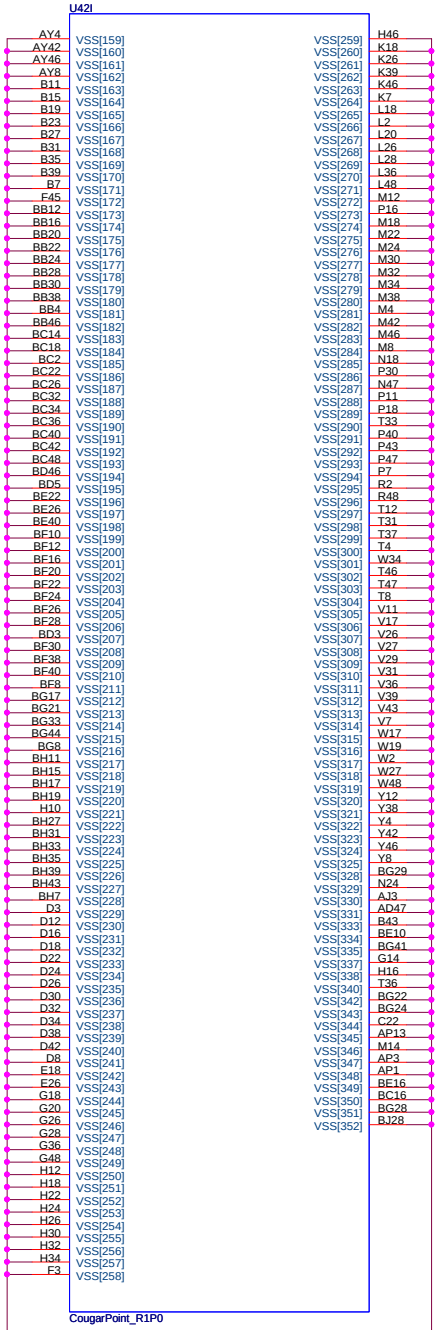
PCH6(CLG)

IBEX PEAK-M (GND)





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Size	Document Number	Rev
	Cougar Point 6/6	1A
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	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DO@DDR3-DIMM0_H=4.0_RVS

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DO@DDR3-DIMM0_H=4.0_RVS

2.48A

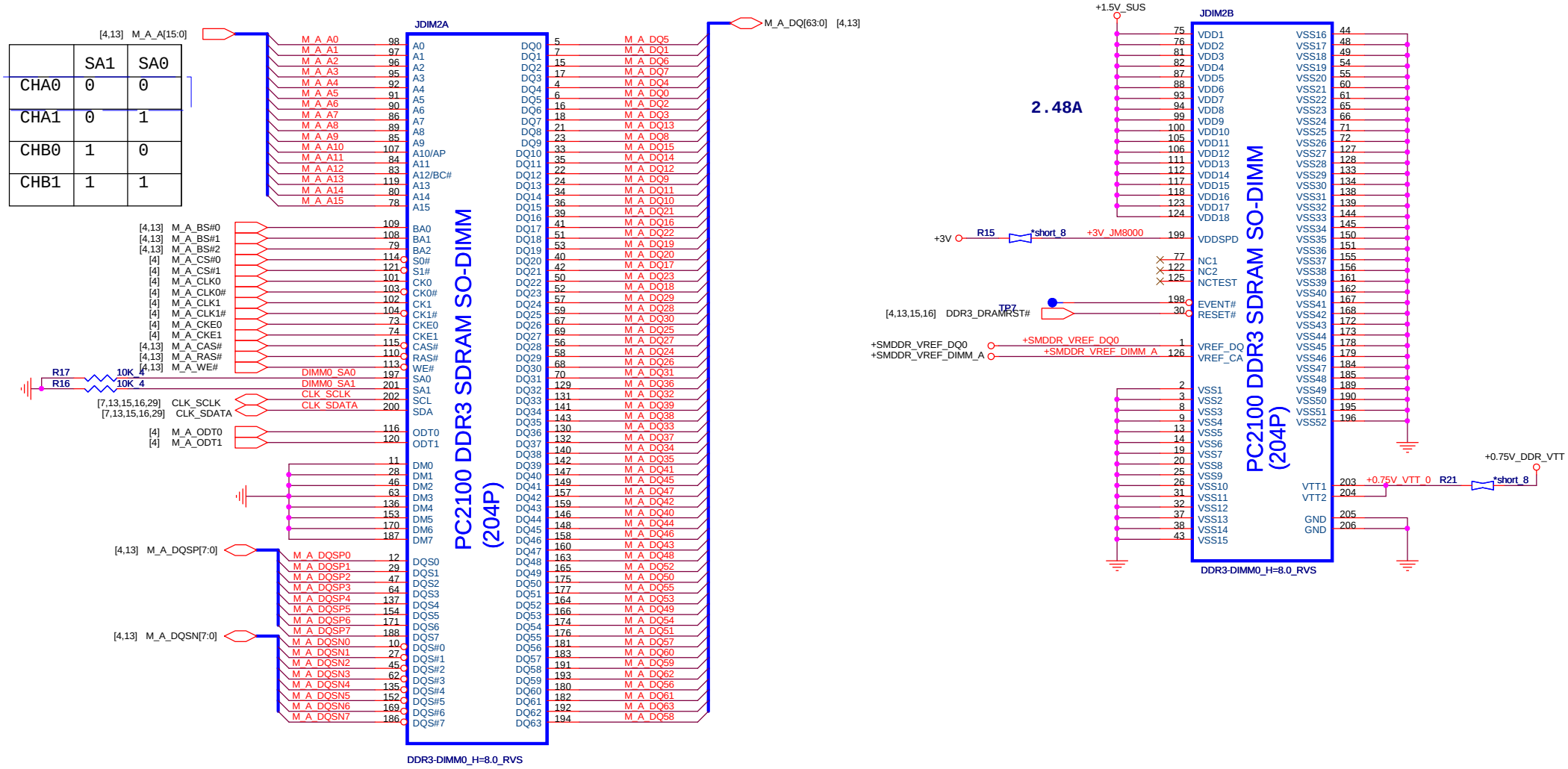
8/4 modify

8/3 add

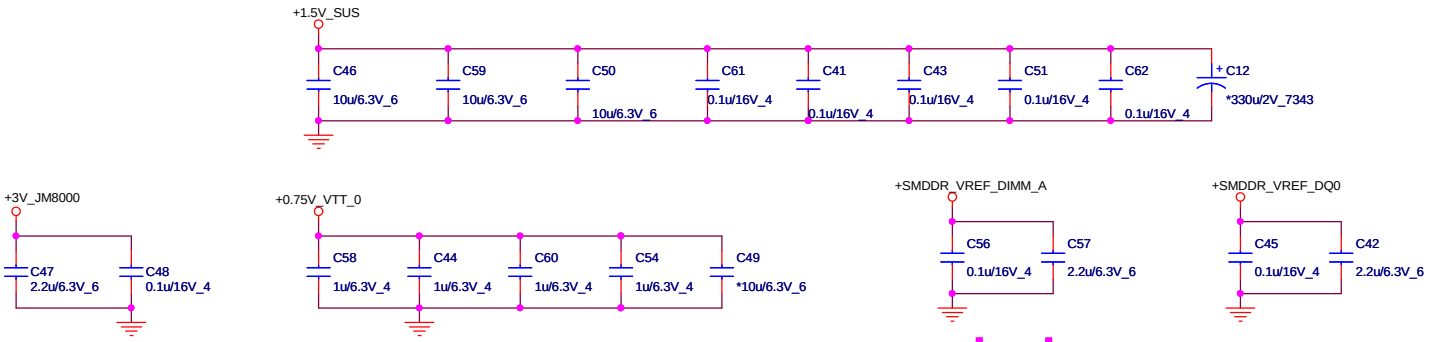
Place these Caps near So-Dimm0.

Quanta Computer Inc.	
PROJECT : ZYF	
Size	Document Number: DDRIII SO-DIMM-0 — Rev: 1A
Date: Monday, November 08, 2010	Sheet 13 of 50

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



Place these Caps near So-Dimm0.

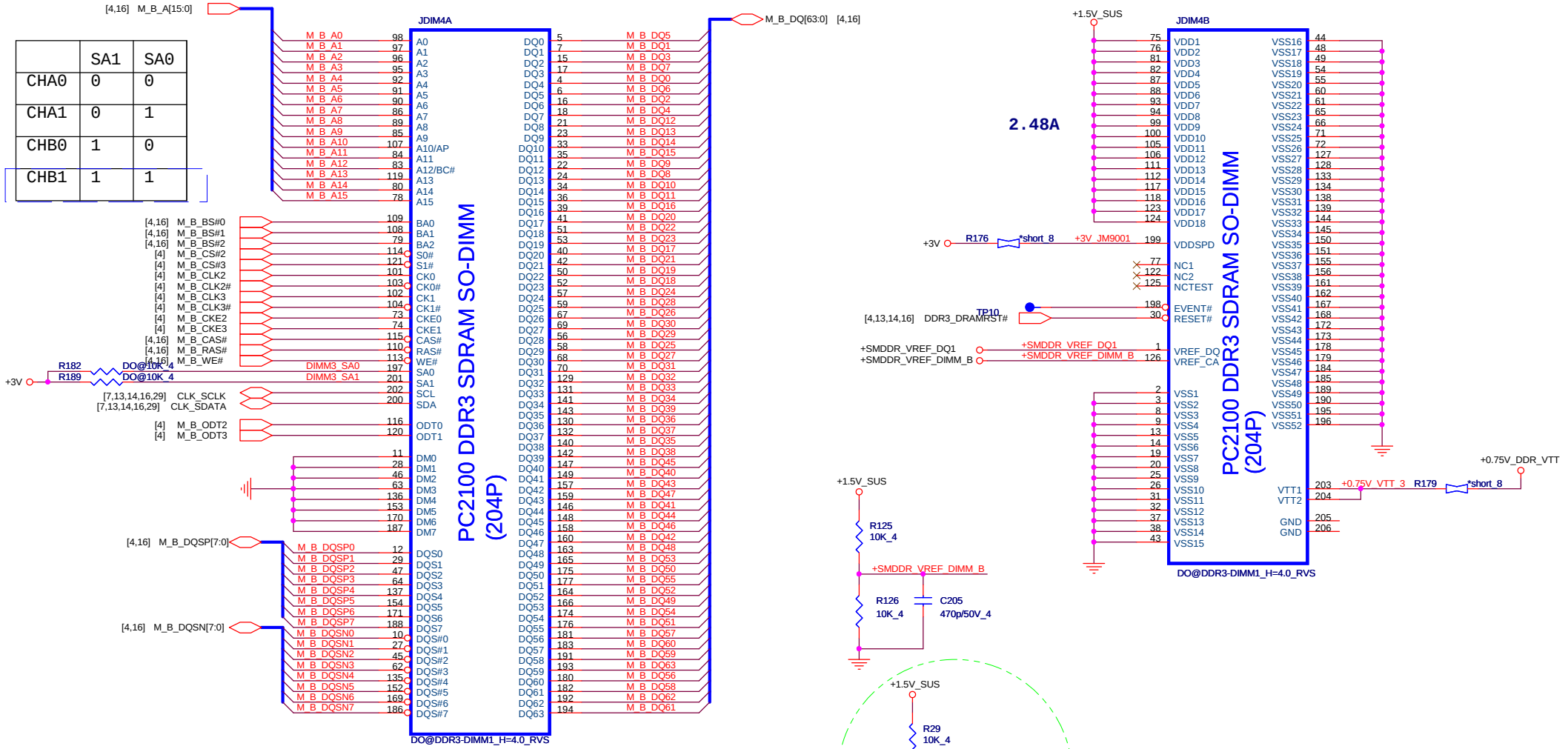


modify

Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
Date: Monday, November 08, 2010	Sheet 14 of 50	

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



Quanta Computer Inc.

PROJECT : ZYF

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
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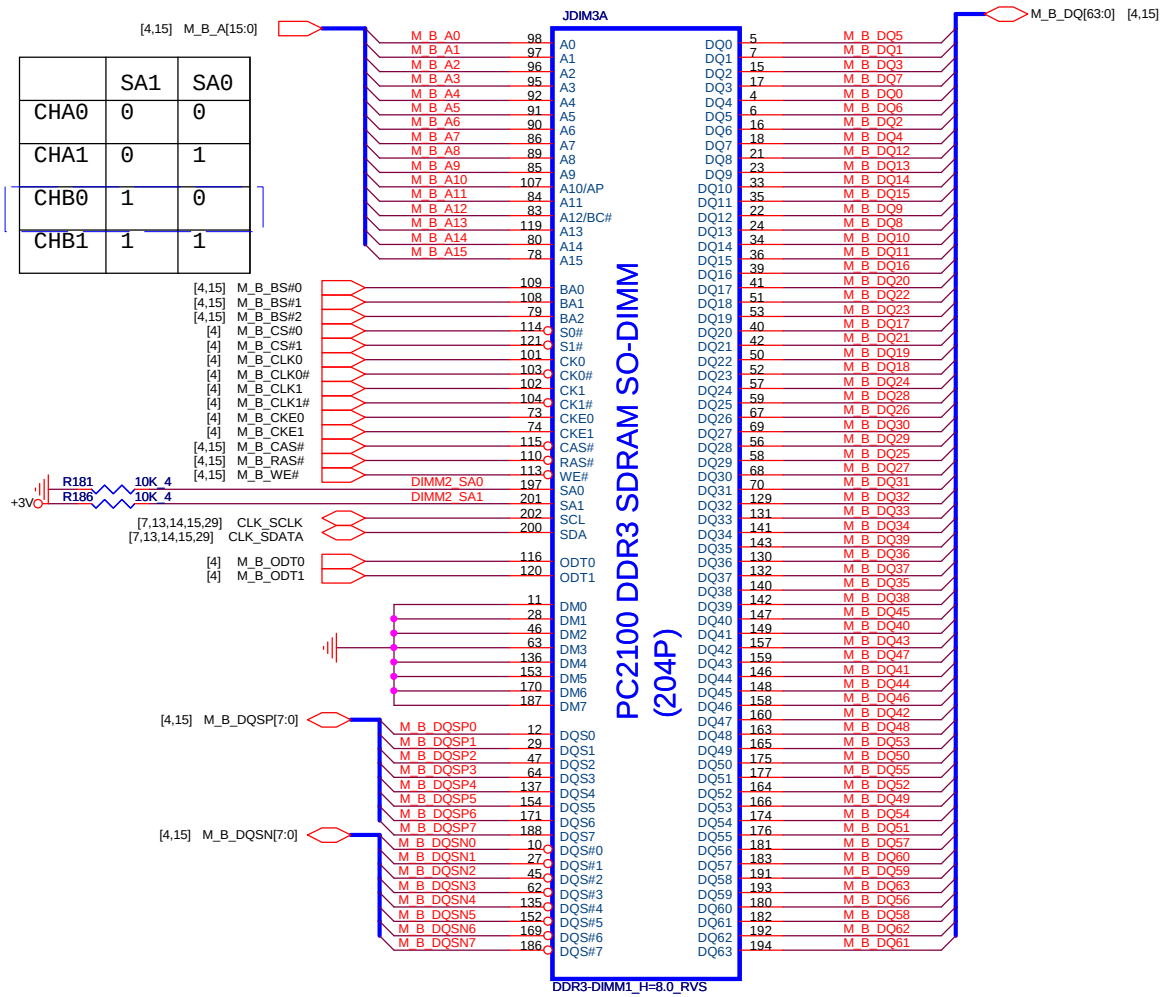
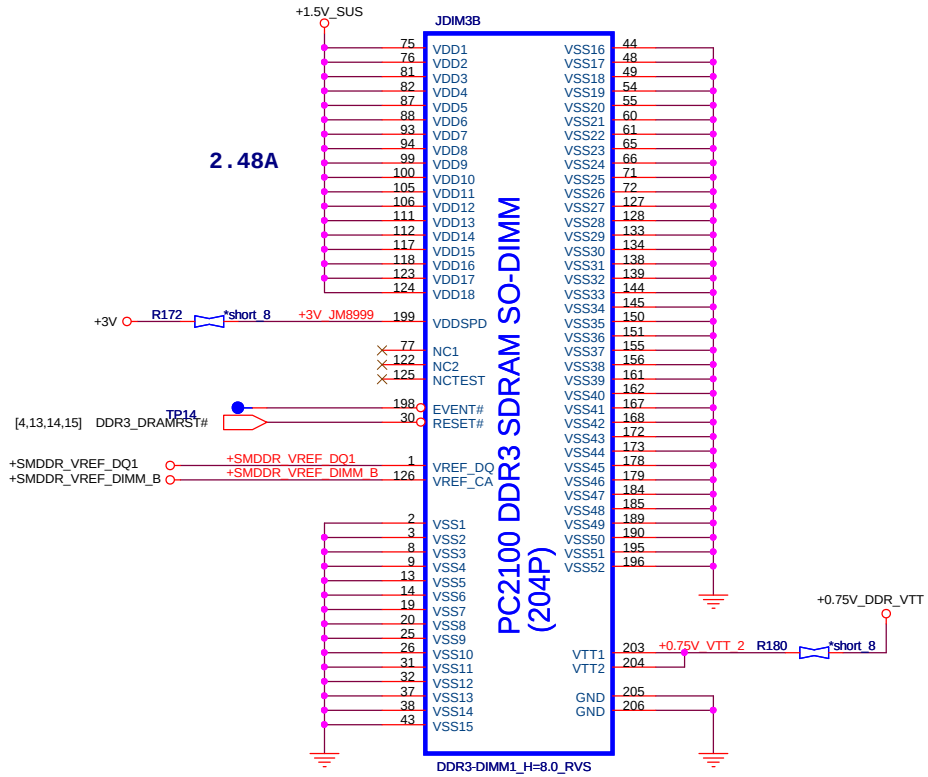
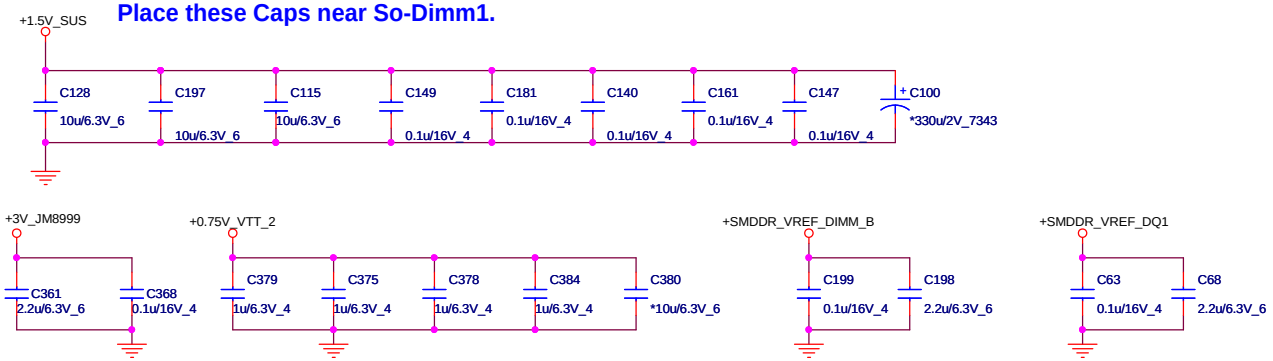
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1





Place these Caps near So-Dimm1.



modify

Quanta Computer Inc.
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	DDRIII SO-DIMM-1	1A
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CPU XDP Connector(CPU)

9/16 del CN21,R578 & C807

[3] XDP_PREQ# TP83
[3] XDP_PRDY# TP81
[3] XDP_BPM0 TP80
[3] XDP_BPM1 TP88
[3] XDP_BPM2 TP82
[3] XDP_BPM3 TP87
[3] XDP_BPM4 TP85
[3] XDP_BPM5 TP84
[3] XDP_BPM6 TP89
[3] XDP_BPM7 TP86
[7] PM_PWRBTN# R574 1K_4 HOOK2_CFG0 TP79
[6] CFG0

[3,7] XDP_DBRST# TP78
[7,9] SMB_PCH_DAT TP77
[7,9] SMB_PCH_CLK TP76
[3] XDP_TRST# TP75

TP90 PWROK_XDP R570 0_4 SYS_PWROK [3,7,32]
TP91 R566 *0_4 PCH_JTAG_TCK [8]
TP92 H_CPUPWRGD_XDP R579 1K_4 H_PWRGOOD [3,10]
TP93 XDP_RST#_R R577 1K_4 PLTRST# [3,9,29,32,33,34,36]

[3] XDP_TDI *0_4 R565 XDP_TDI TP68
[8] PCH_JTAG_TDI
[8] PCH_JTAG_TMS *0_4 R562 XDP_TMS TP69
[3] XDP_TMS
[3] XDP_TCLK TP72

Place near to XDP connector

R573 51_4 +1.05V_VTT
TP67 XDP_TDO XDP_TDO [3]
R568 *0_4

+3V_S5
R575 210/F_4
PCH_JTAG_TDO [8]
R571 100/F_4

if no used PCH XDP, please reserved for S5 leakage

ITPCLK/ITPCLK# (Processor BCLK_ITP/BCLK_ITP#) Topology for debug port DG

[6] CLK_XDP_ITPP R585 *0_4 CLK_ITPP TP70
[6] CLK_XDP_ITPN R586 *0_4 CLK_ITPN TP71
[9] CLK_PCIE_XDPP R231 0_4
[9] CLK_PCIE_XDPN R232 0_4

SCREW HOLE

HOLE18 *HG-C315D118P2
HOLE12 *HG-C315D118P2
HOLE11 *HG-C315D118P2
HOLE21 *HG-TC276BC315D118P2
HOLE2 *HG-C315D118P2
HOLE20 *HG-C315D118P2
HOLE19 *HG-C315D118P2
HOLE7 *H-TC315BE335X276D118P2
HOLE9 *HG-C315D118P2
HOLE4 *HG-C315D118P2
HOLE3 *HG-C315D118P2
HOLE5 *HG-C315D118P2
HOLE22 *HG-TC276BC315D118P2
HOLE17 *HG-C315D118P2
HOLE1 *HG-C315D118P2
PAD1 *CPAD-C197
HOLE6 *HG-C315D118P2
HOLE14 *O-ZYA-1
HOLE16 *O-ZYA-2
HOLE10 *H-C95D95N

CPU NUT

HOLE26 H-TC236I146BC276D146P2
HOLE25 H-TC236I146BC276D146P2
HOLE29 H-TC236I146BC276D146P2
HOLE30 H-TC236I146BC276D146P2

PCH & GPU NUT

HOLE15 H-C315D146P2
HOLE24 H-TC146BC315D146P2
HOLE13 H-C315D146P2
HOLE28 H-C315D146P2
HOLE8 H-C315I146D146P2

PCH NUT

HOLE31 H-C315D146P2
HOLE27 H-C315D146P2

MINI CARD NUT

HOLE23 H-TC197BC59D59P2

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	XDP/ Hole	1A

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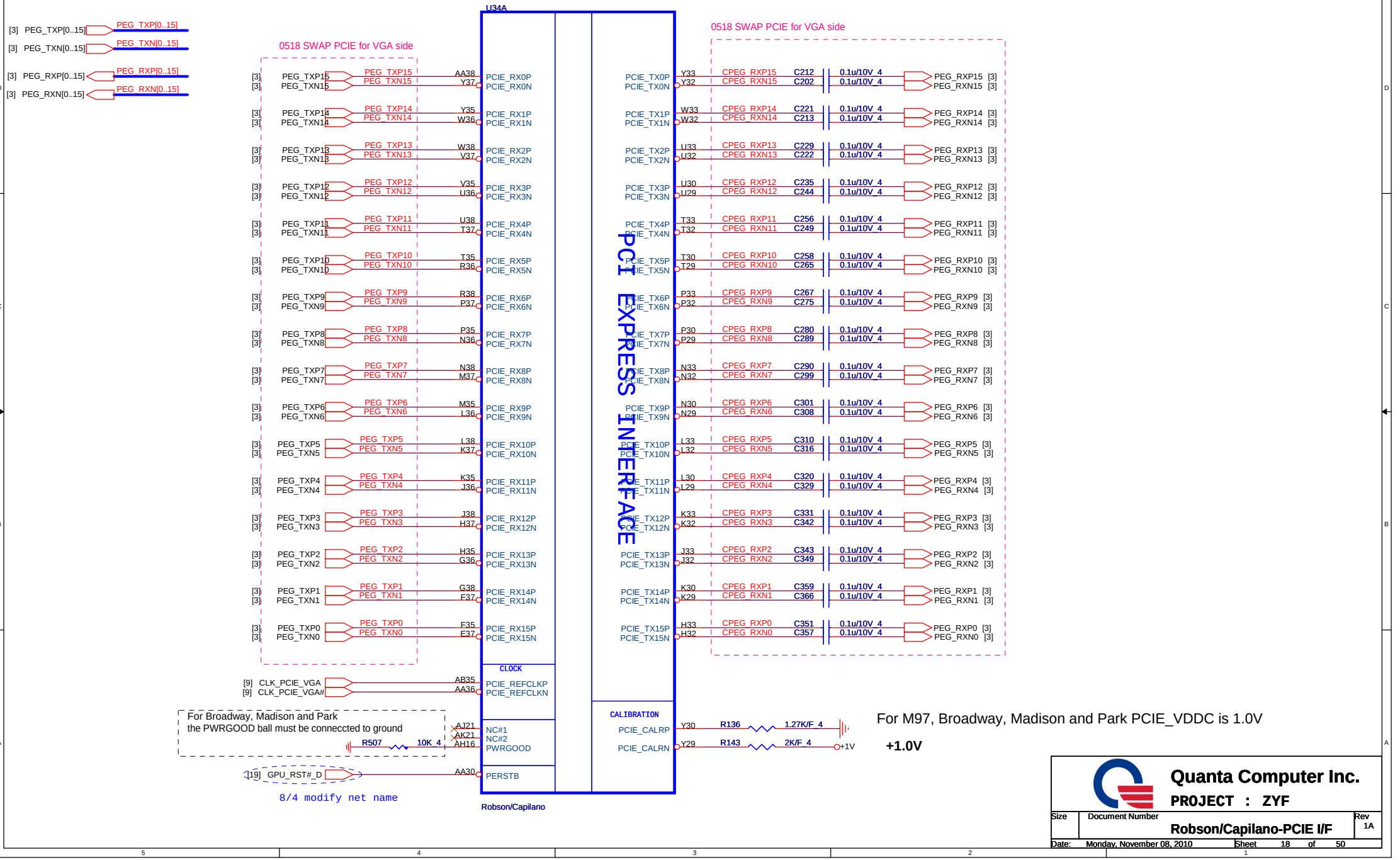

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK

1.8V GPIO

3.3V GPIO

8/4 modify

8/4 modify

8/3 del

8/4 modify net name

9/14 add

P/N ?

For EMI

Change C612/C613 from 18p to 27p at B-test

HDMI

Display Port

LVDS

CRT

Robson/Capilano

Robson/Capilano

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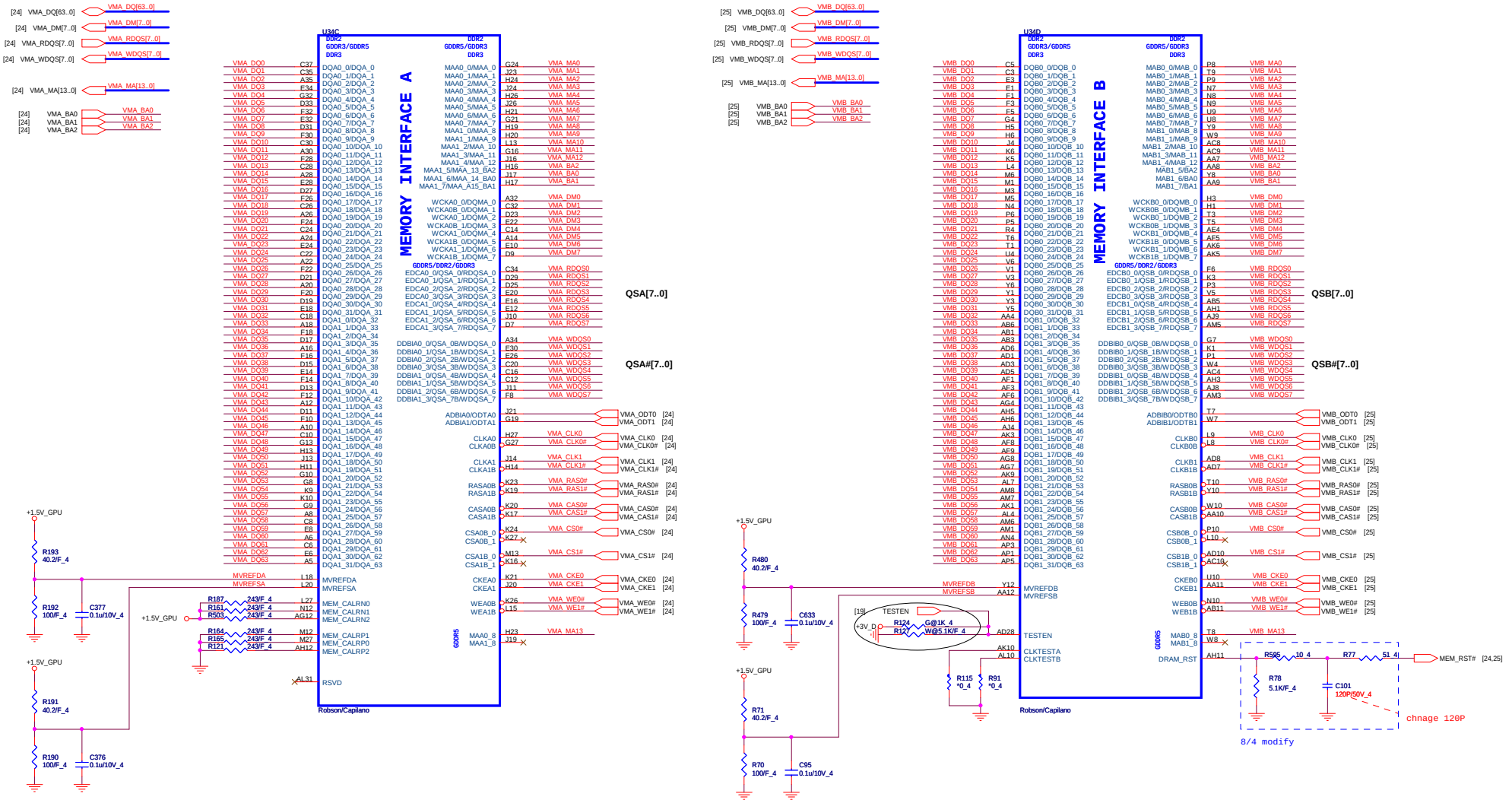

Quanta Computer Inc.			
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Size	Document Number	Rev	
	Robson/Capilano-MEM I/F	1A	
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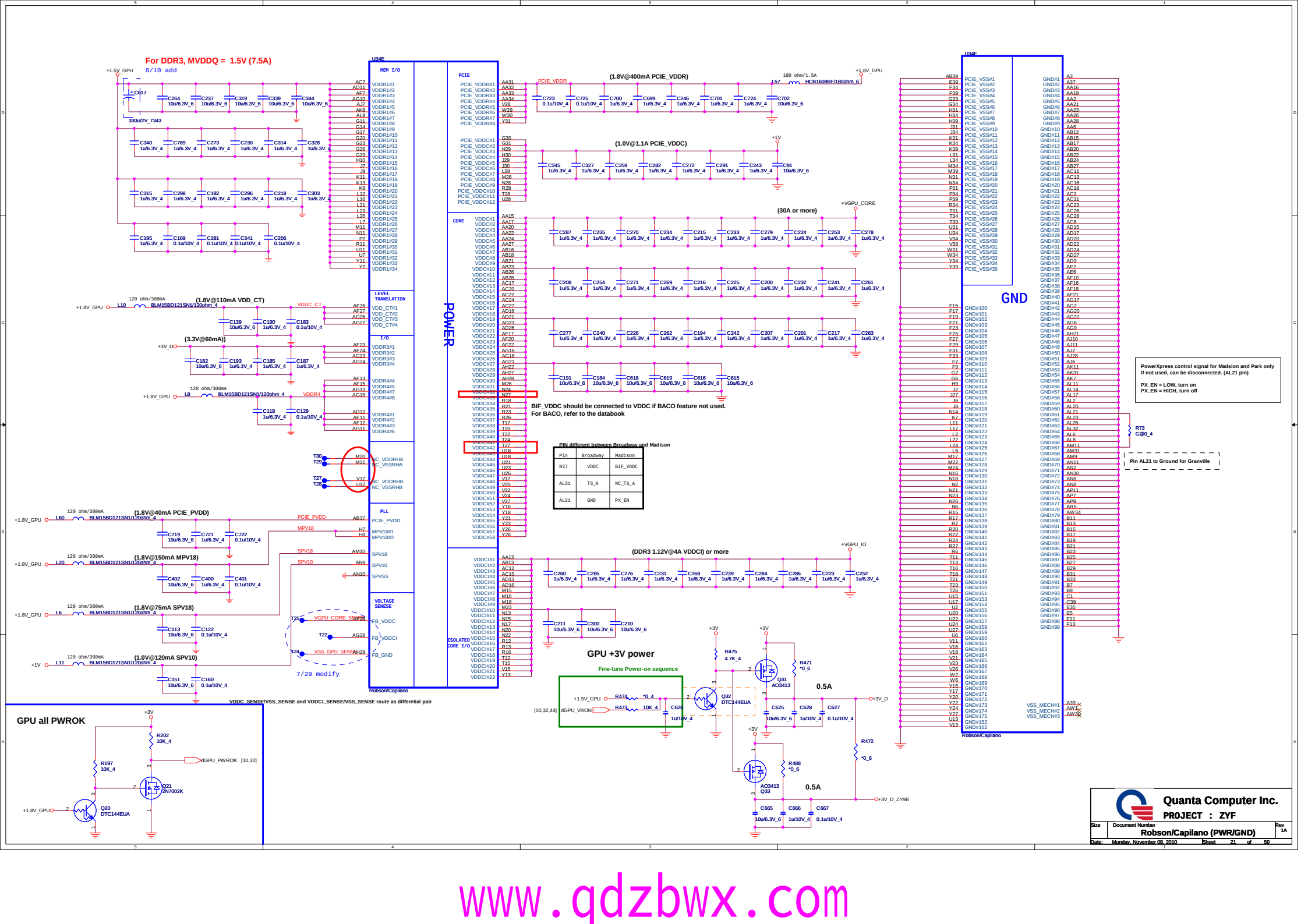
For DDR3, MVDDQ = 1.5V (7.5A)
8/10 add
U34E
MEM I/O
POWER
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
PCIE
CORE
ISOLATED CORE I/O
(1.8V@400mA PCIE_VDDR)
(1.0V@1.1A PCIE_VDDC)
(30A or more)
(DDR3 1.12V@4A VDDCI) or more
(1.8V@110mA VDD_CT)
(3.3V@60mA))
(1.8V@40mA PCIE_PVDD)
(1.8V@150mA MPV18)
(1.8V@75mA SPV18)
(1.0V@120mA SPV10)
BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
PIN different between Broadway and Madison
Pin | Broadway | Madison
N27 | VDDC | BIF_VDDC
AL31 | TS_A | NC_TS_A
AL21 | GND | PX_EN
GPU +3V power
Fine-tune Power-on sequence
0.5A
0.5A
GPU all PWROK
VDDC_SENSE/VSS_SENSE and VDDCI_SENSE/VSS_SENSE route as differetial pair
7/29 modify
U34F
GND
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected. (AL21 pin)
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
Pin AL21 to Ground for Granville
Quanta Computer Inc.
PROJECT : ZYF
Robson/Capilano (PWR/GND)
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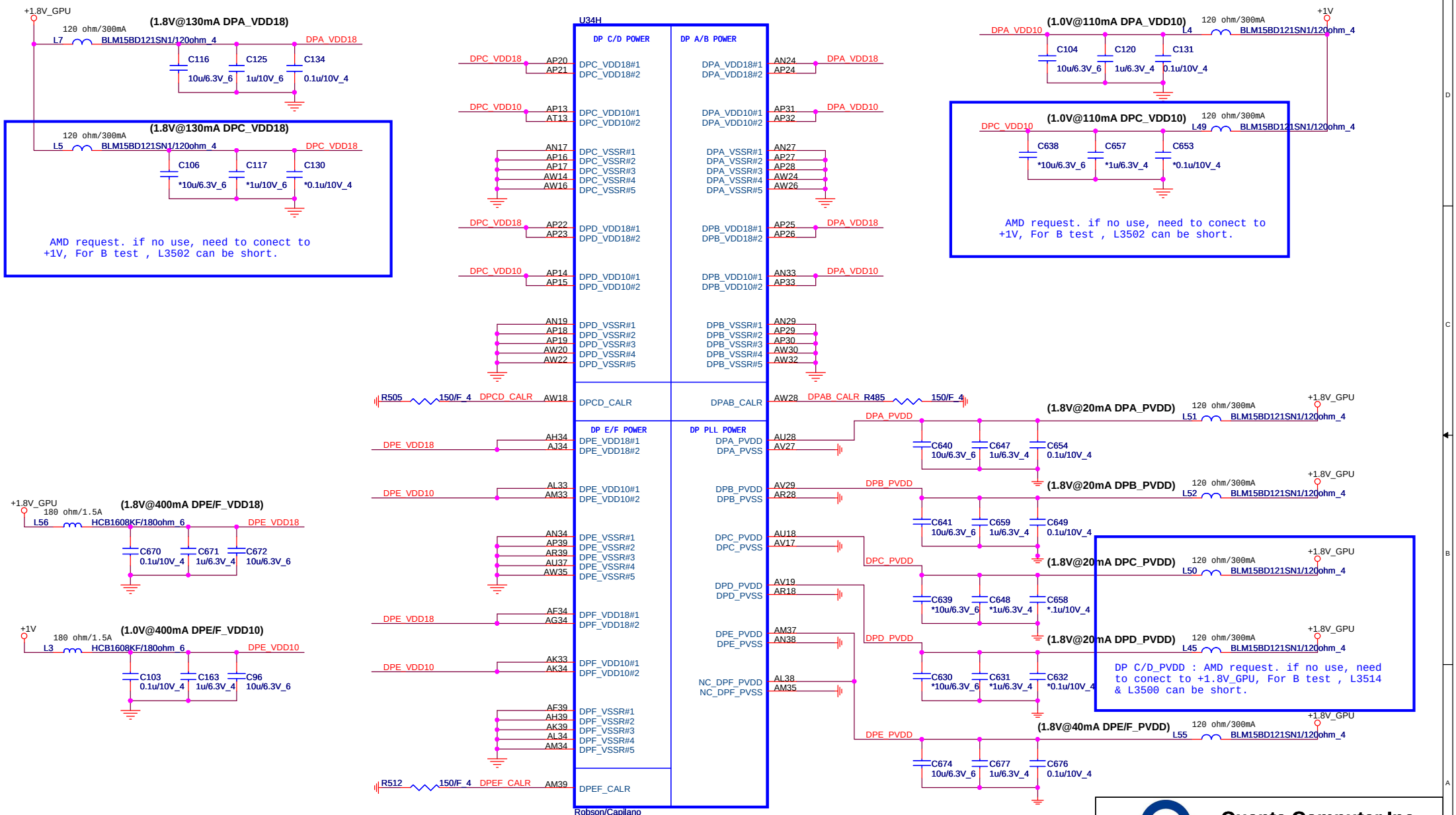
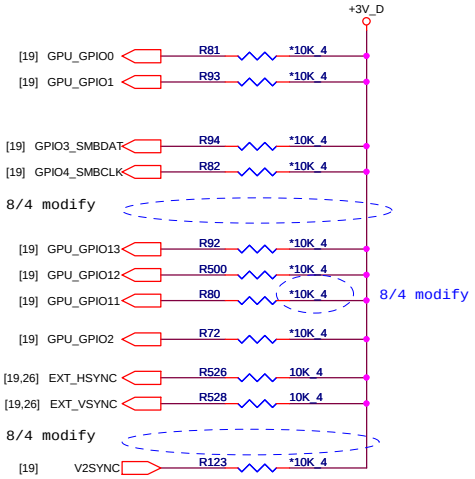
www.qdzbwx.com



PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

Audio Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

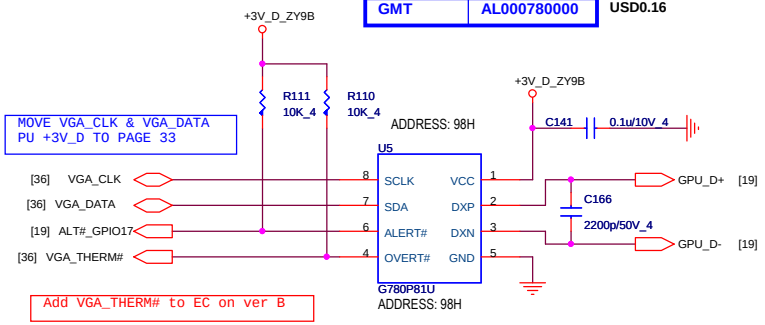
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

Thermal Sensor

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

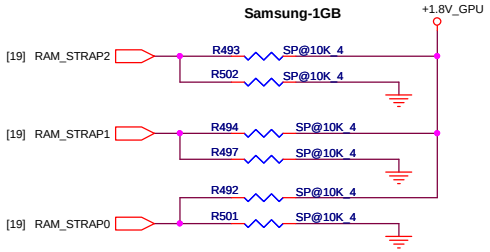
USD0.16



DDR3 VRAM SIZE Strap

DDR3 VRAM size

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW05	1GB	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04	1GB	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03	2GB	1	0	1
Samsung	K4W1G1646G-HC11	AKD5EGGT503		0	1	1
	K4W1G1646E-HC12	AKD5LGGT506	1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT511	2GB	0	0	1
AMD	23EY2387MA-12	AKD5LGGT700	1GB	0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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	Strip/Thermal	1A
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CHANNEL A: 512 / 1GMB DDR3 (64/128M*16*4pcs)

[20] VMA_DQ[63..0] — VMA_DQ[63..0]
[20] VMA_DM[7..0] — VMA_DM[7..0]
[20] VMA_RDQS[7..0] — VMA_RDQS[7..0] — QSA[7..0]
[20] VMA_WDQS[7..0] — VMA_WDQS[7..0] — QSA#[7..0]

TOP Left

BOT Left

BOT Right

TOP Right

Group-A0 VREF

+1.5V_GPU
R244 4.99K/F_4 — VREFC_VMA1 — R240 4.99K/F_4 — C407 0.1u/10V_4
R597 4.99K/F_4 — VREFD_VMA1 — R591 4.99K/F_4 — C831 0.1u/10V_4
R596 4.99K/F_4 — VREFC_VMA2 — R599 4.99K/F_4 — C812 0.1u/10V_4
R245 4.99K/F_4 — VREFD_VMA2 — R241 4.99K/F_4 — C408 0.1u/10V_4

Group-A1 VREF

+1.5V_GPU
R593 4.99K/F_4 — VREFC_VMA3 — R590 4.99K/F_4 — C830 0.1u/10V_4
R592 4.99K/F_4 — VREFD_VMA3 — R589 4.99K/F_4 — C829 0.1u/10V_4
R243 4.99K/F_4 — VREFC_VMA4 — R233 4.99K/F_4 — C428 0.1u/10V_4
R242 4.99K/F_4 — VREFD_VMA4 — R239 4.99K/F_4 — C406 0.1u/10V_4

MEM_A0 CLK

VMA_CLK0
VMA_CLK0#
R236 56.2/F_4 — R237 56.2/F_4
C430 0.01u/16V_4

Group-A0 decoupling CAP

+1.5V_GPU
C420 1u/6.3V_4 — C421 1u/6.3V_4 — C422 1u/6.3V_4 — C823 1u/6.3V_4 — C795 1u/6.3V_4 — C414 1u/6.3V_4 — C405 1u/6.3V_4 — C418 1u/6.3V_4
C794 1u/6.3V_4 — C388 1u/6.3V_4 — C419 1u/6.3V_4 — C818 1u/6.3V_4 — C822 1u/6.3V_4 — C798 1u/6.3V_4 — C819 1u/6.3V_4 — C821 1u/6.3V_4
C828 10u/6.3V_6 — C426 10u/6.3V_6 — C827 10u/6.3V_6 — C427 10u/6.3V_6 — C425 10u/6.3V_6

Group-A1 decoupling CAP

+1.5V_GPU
C815 1u/6.3V_4 — C390 1u/6.3V_4 — C392 1u/6.3V_4 — C411 1u/6.3V_4 — C409 1u/6.3V_4 — C810 1u/6.3V_4 — C417 1u/6.3V_4 — C814 1u/6.3V_4
C817 1u/6.3V_4 — C415 1u/6.3V_4 — C412 1u/6.3V_4 — C410 1u/6.3V_4 — C416 1u/6.3V_4 — C816 1u/6.3V_4 — C811 1u/6.3V_4 — C813 1u/6.3V_4
C424 10u/6.3V_6 — C825 10u/6.3V_6 — C423 10u/6.3V_6 — C824 10u/6.3V_6 — C826 10u/6.3V_6

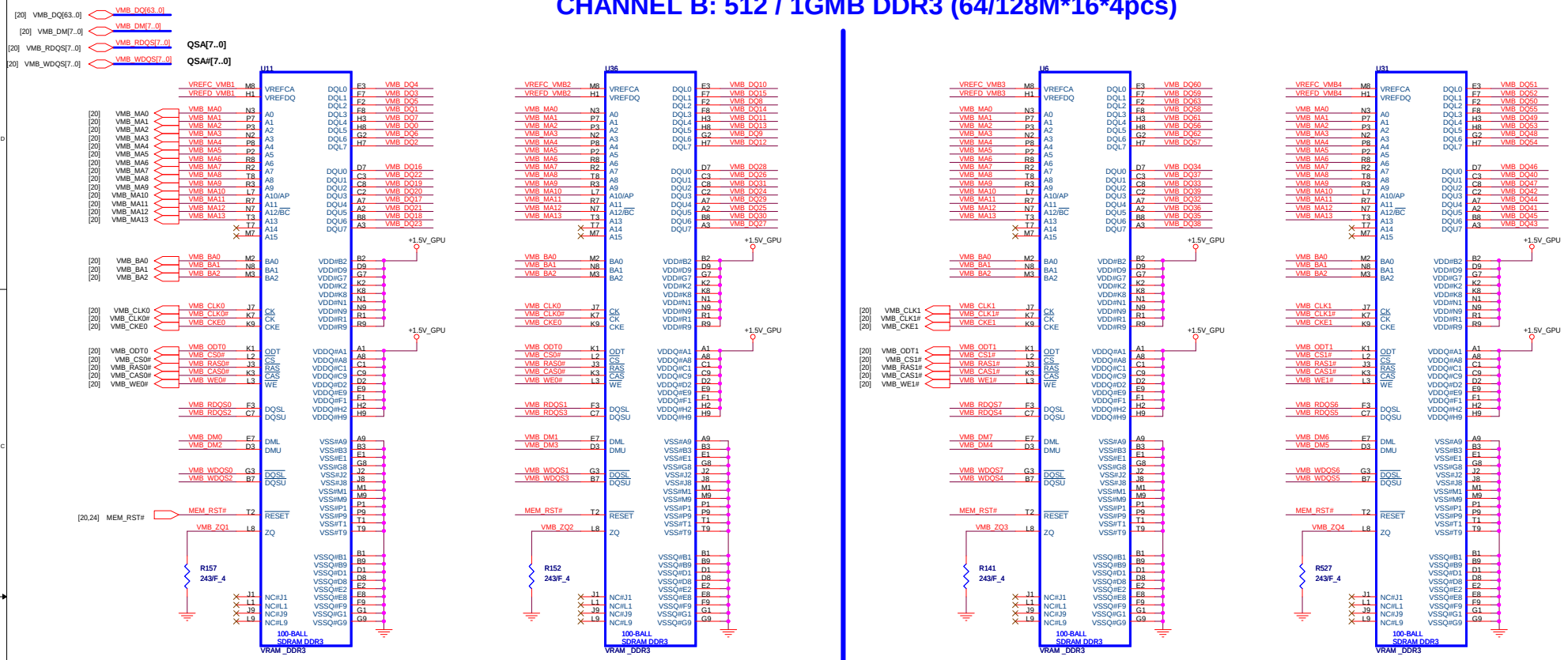
MEM_A1 CLK

VMA_CLK1
VMA_CLK1#
R235 56.2/F_4 — R234 56.2/F_4
C429 0.01u/16V_4

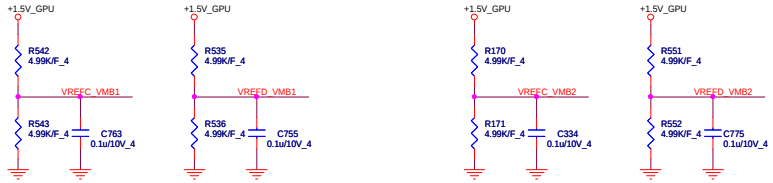
Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	MEMORY 1 channel A	1A
Date: Monday, November 08, 2010	Sheet 24 of 50	

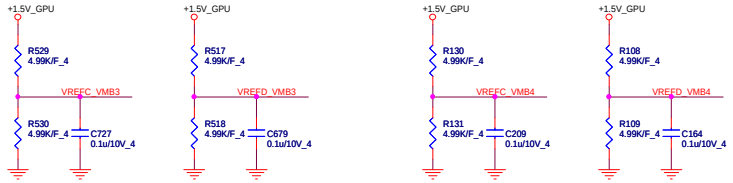
CHANNEL B: 512 / 1GMB DDR3 (64/128M*16*4pcs)



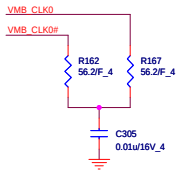
Group-B0 VREF



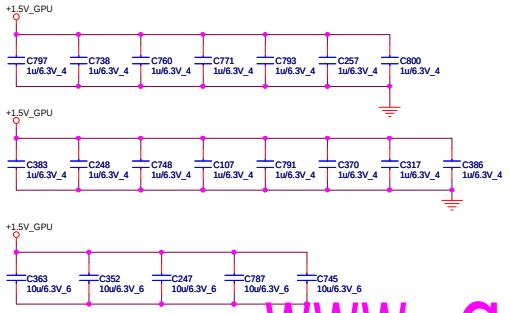
Group-B1 VREF



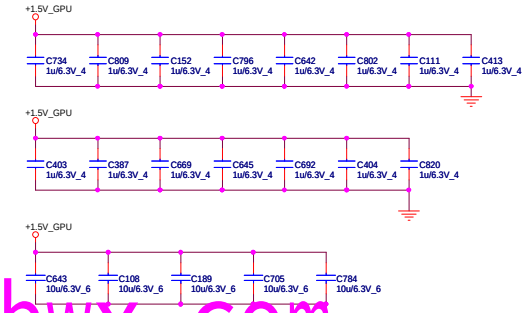
MEM_B0 CLK



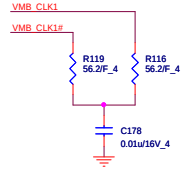
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	MEMORY 2 channel B	1A
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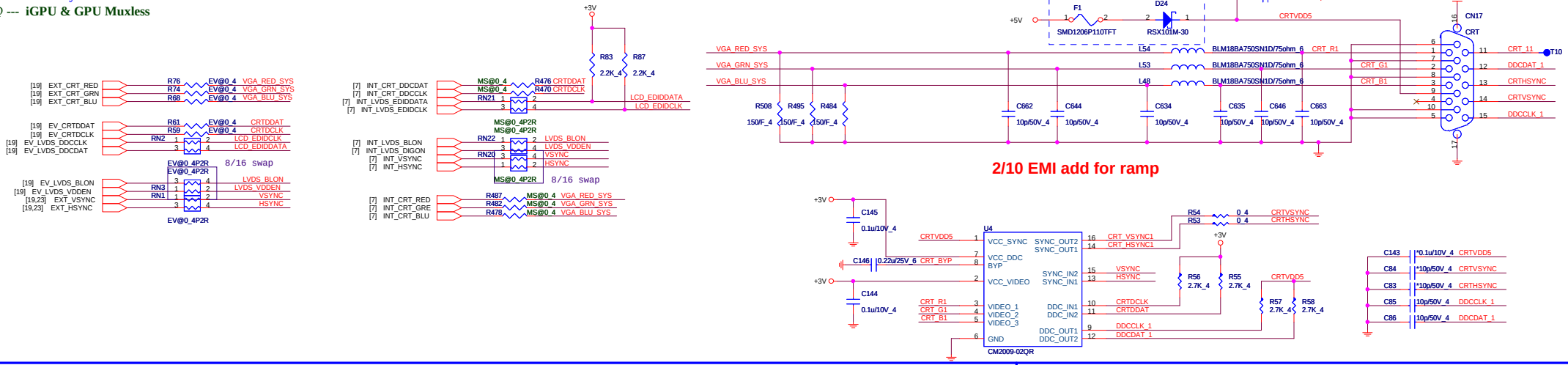
CRT

EV@ --- GPU only

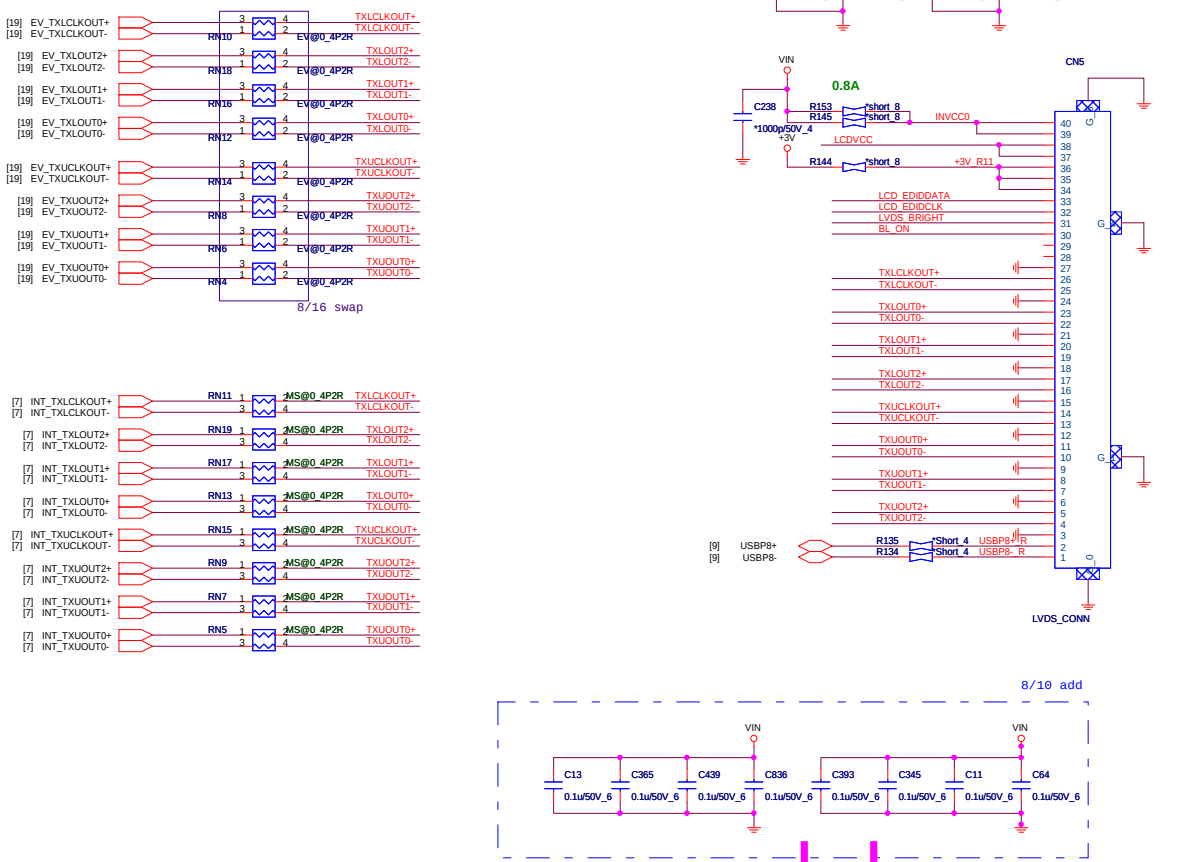
MS@ --- iGPU & GPU Muxless



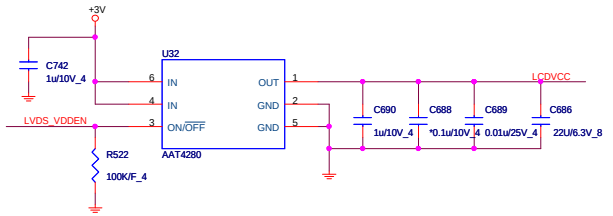
LVDS

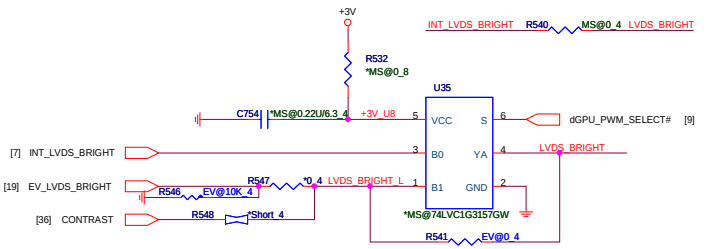
EV@ --- GPU only

MS@ --- iGPU & GPU Muxless

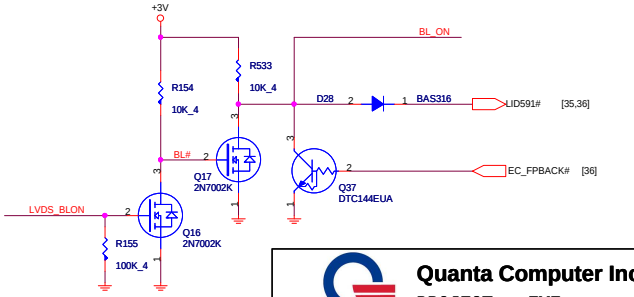


LCD Power





Backlight Control



Quanta Computer Inc.

PROJECT : ZYF

Size	Document Number	Rev
	CRT/LVDS/LID	1A

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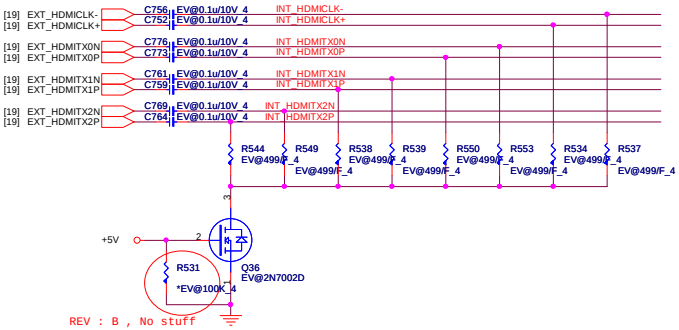
Graphic HDMI source

EV@ --- GPU only

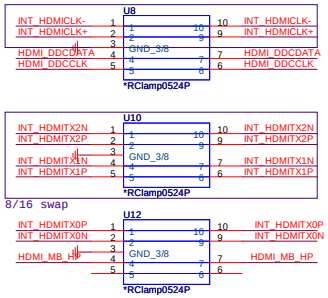
MS@ --- iGPU & GPU Muxless



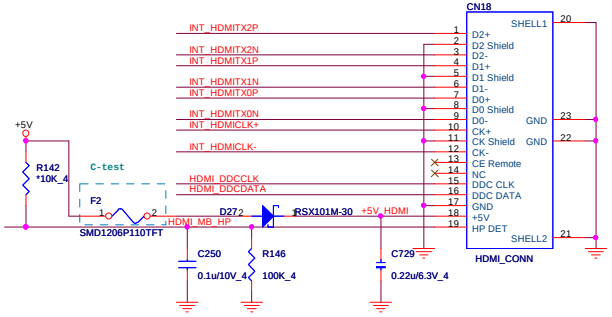
REV : B , No stuff

ESD Protect

8/16 swap



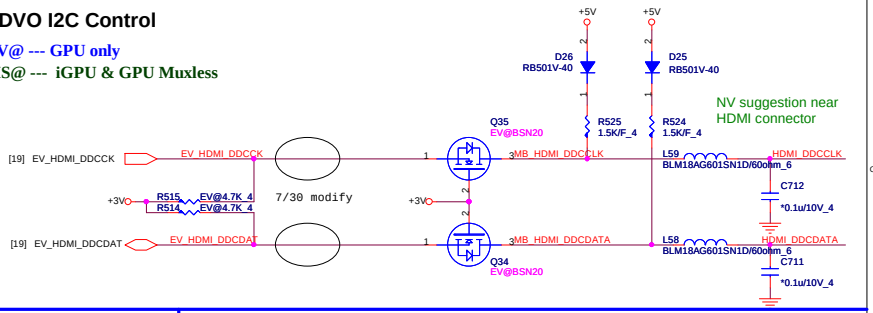
HDMI connector



SDVO I2C Control

EV@ --- GPU only

MS@ --- iGPU & GPU Muxless

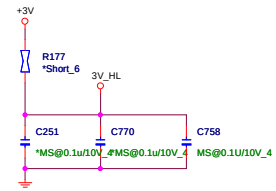


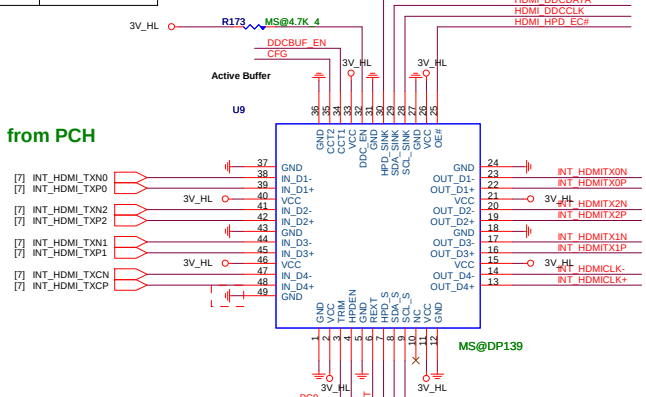
HDMI LEVEL SHIFTER

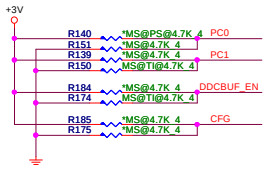
EV@@ --- GPU only

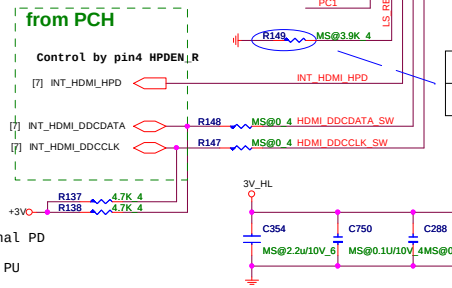
MS@ --- iGPU & GPU Muxless

Parade	*AL008101000*
TI	*AL000139000*









TI 3.9K	*CS23902JB00*
PS 499	*CS14992FB24*

close to pin2/11/15/21/26/33/40/46

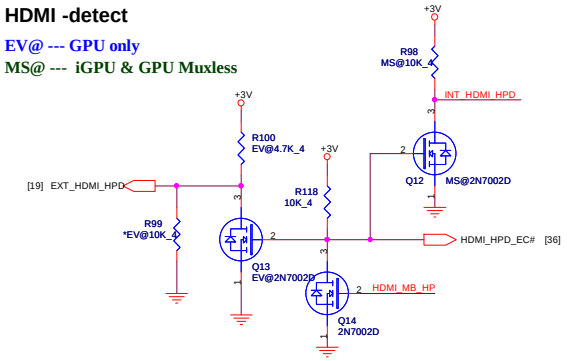
Equalization Control		
PC1	PC0	EQ Control
PIN4	PIN3	
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

HDMI -detect

EV@ --- GPU only

MS@ --- iGPU & GPU Muxless



Quanta Computer Inc.

PROJECT : ZYF

Size	Document Number	Rev
	HDMI/ LEVEL SHIFTER	1A
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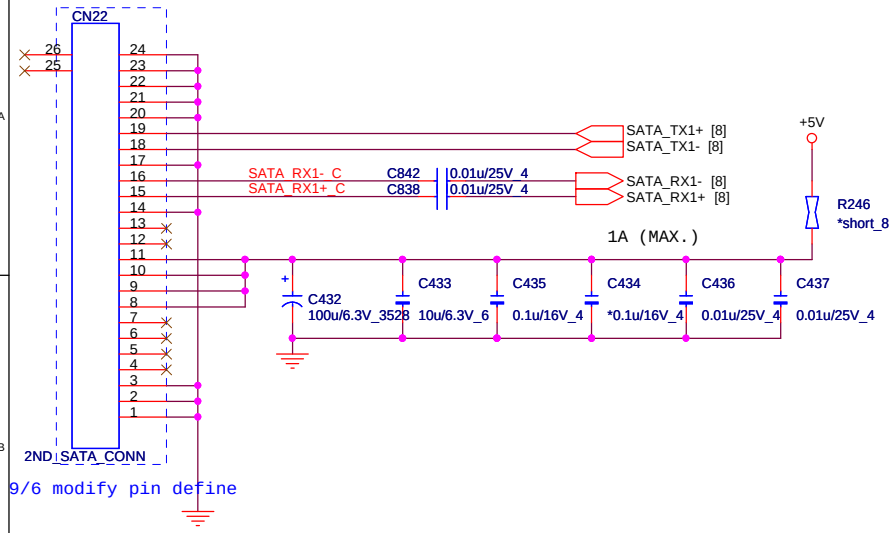
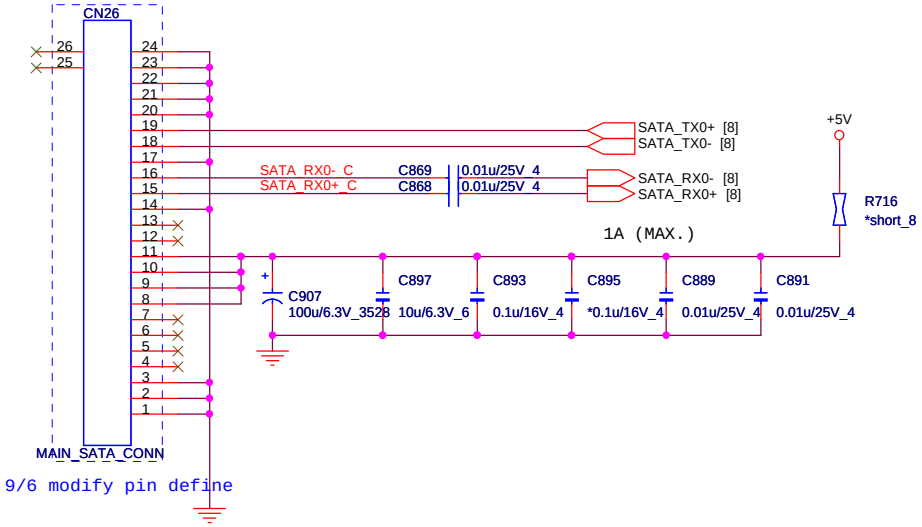
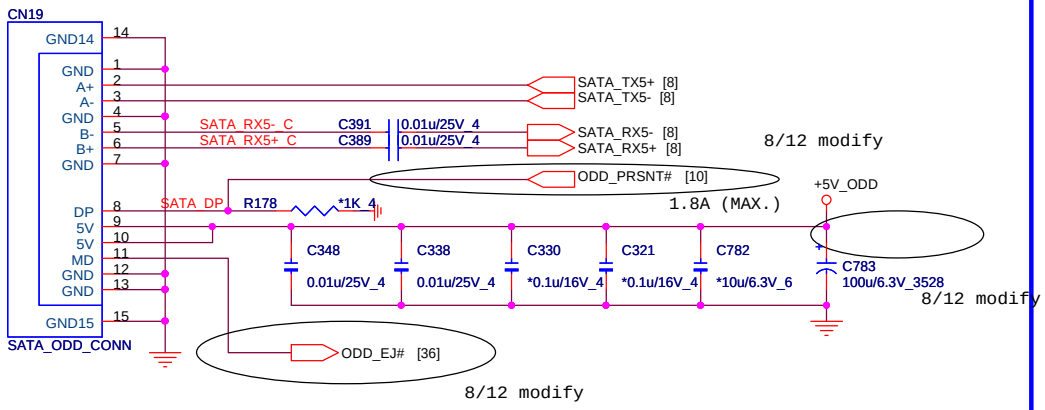
2nd SATA HDD (edge of board)



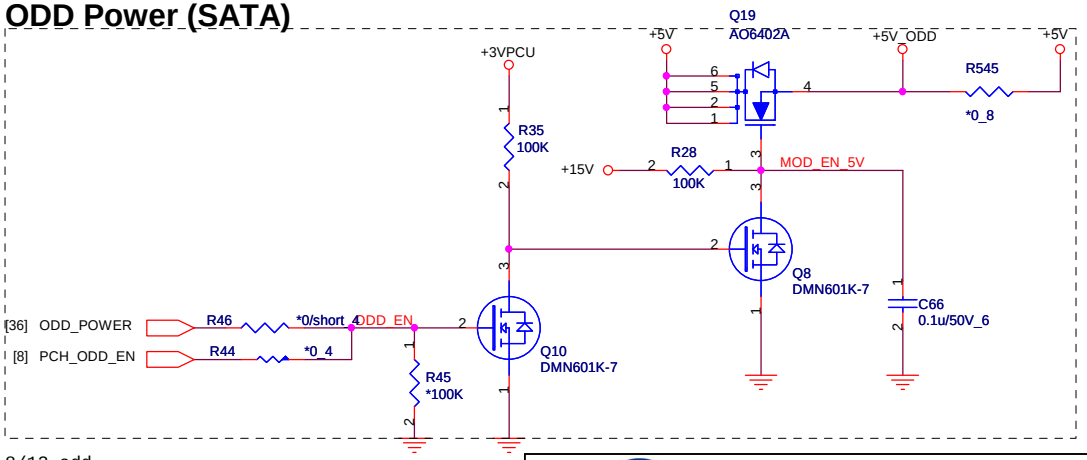
MAIN SATA HDD



ODD (SATA)



ODD Power (SATA)



Quanta Computer Inc.

PROJECT : ZYF

Size	Document Number	Rev
	SATA-HDD/ODD	1A

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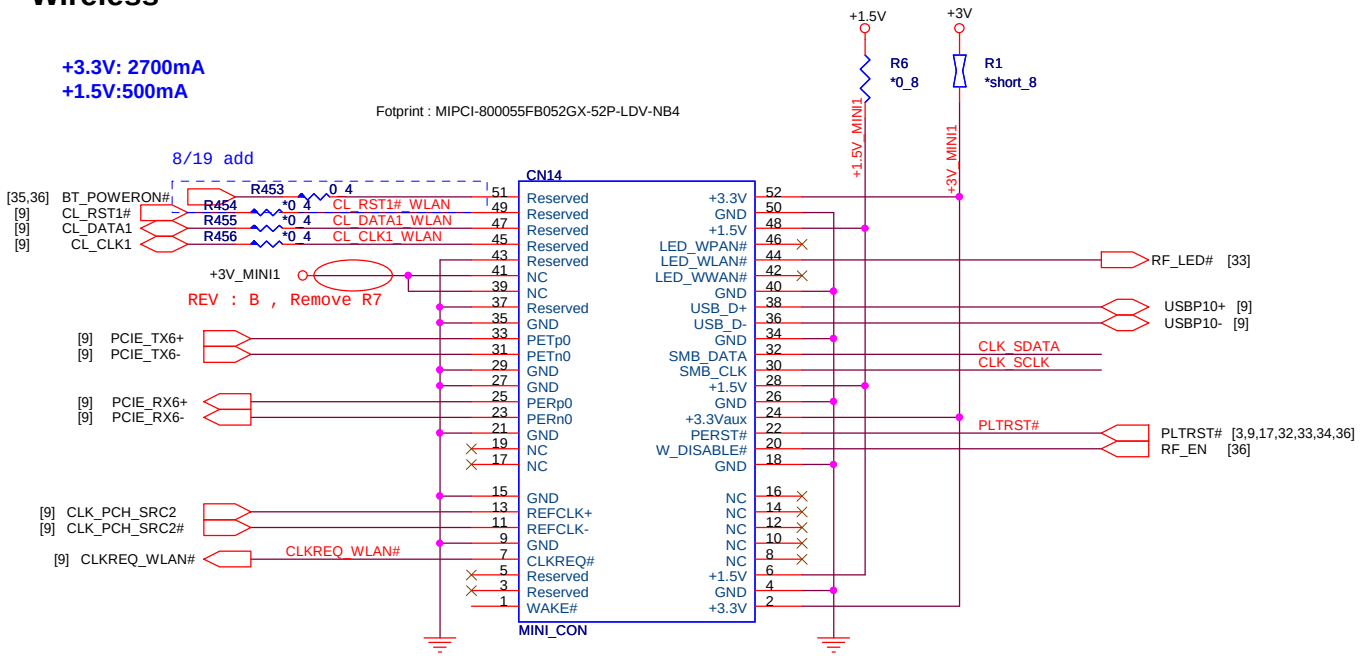
Wireless

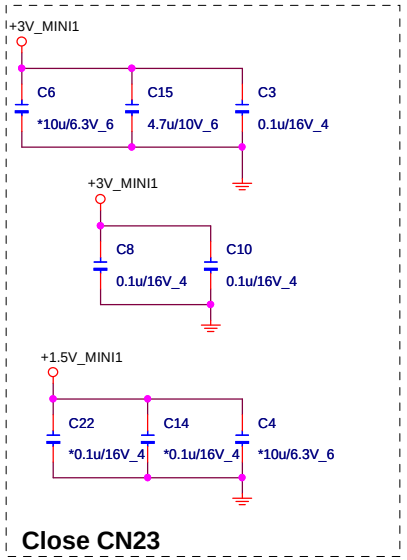
+3.3V: 2700mA
+1.5V:500mA

Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4

8/19 add

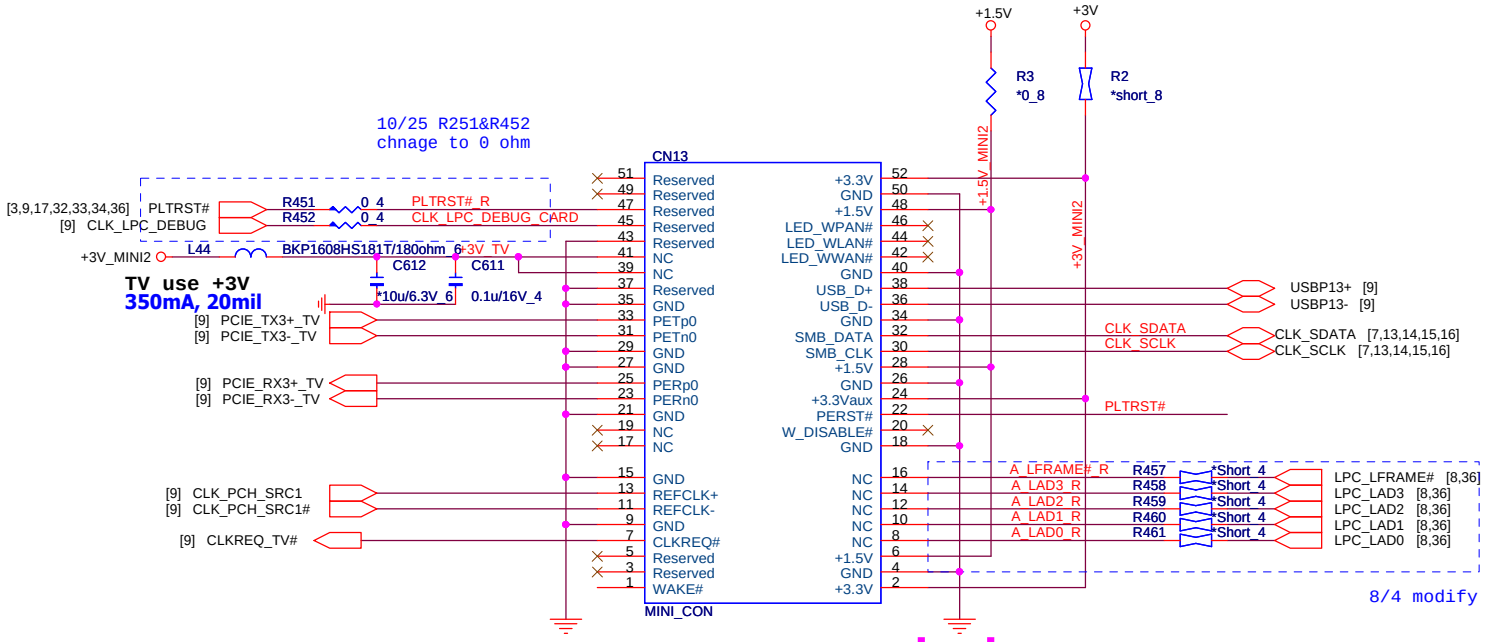


H=9



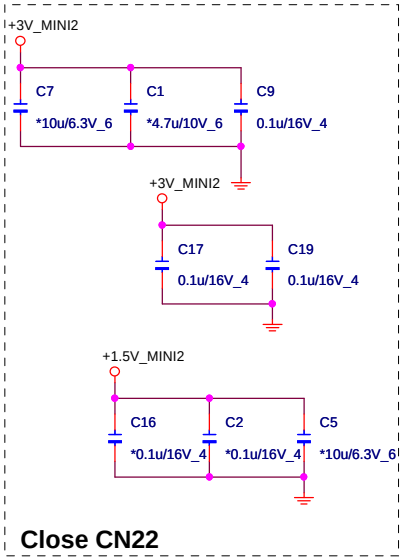
TV and Debug

10/25 R251&R452
chnage to 0 ohm



8/4 modify

H=4



Quanta Computer Inc.		
PROJECT : ZYF		
Size	Document Number: MINI PCI-E card/TV	Rev 1A
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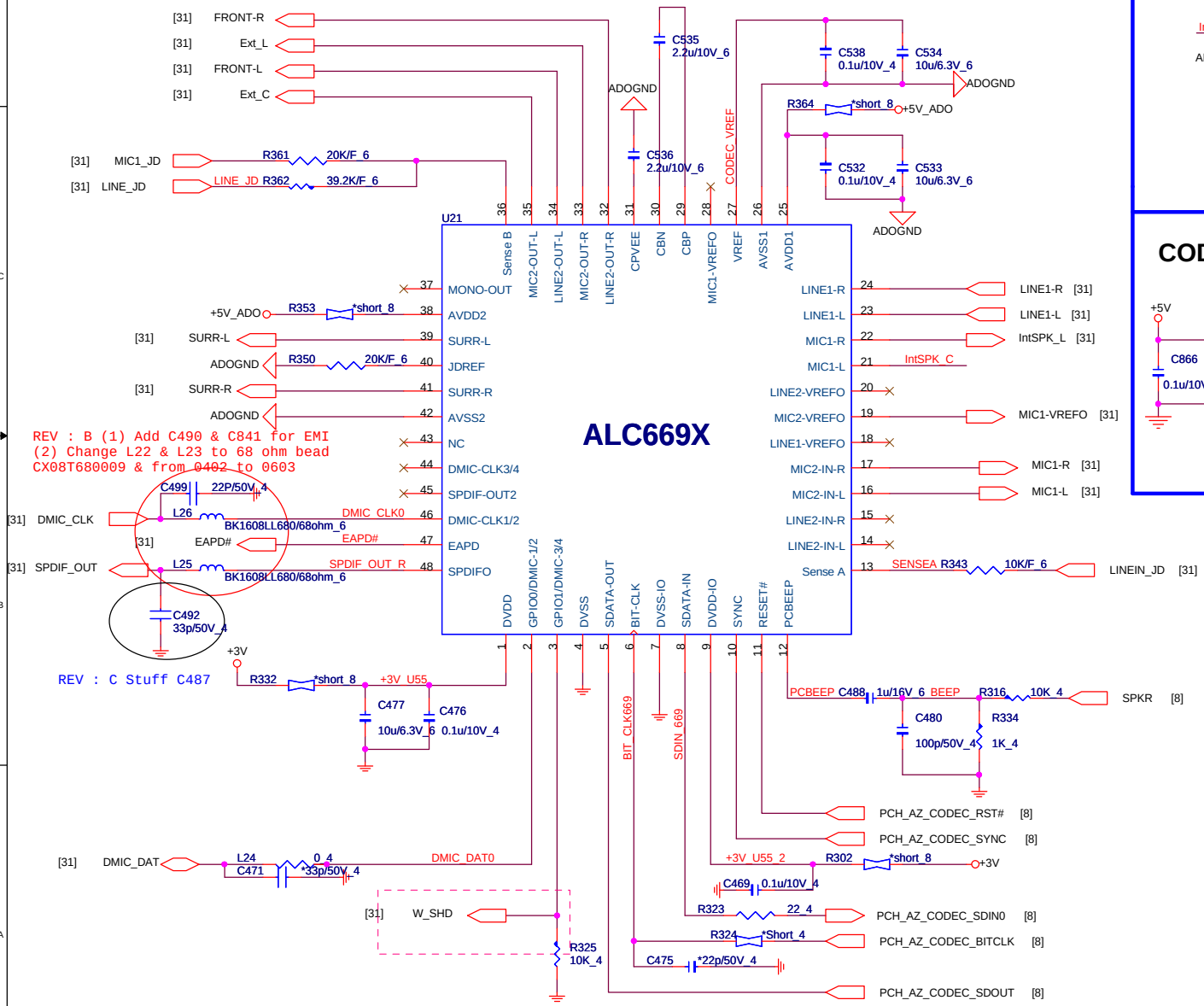
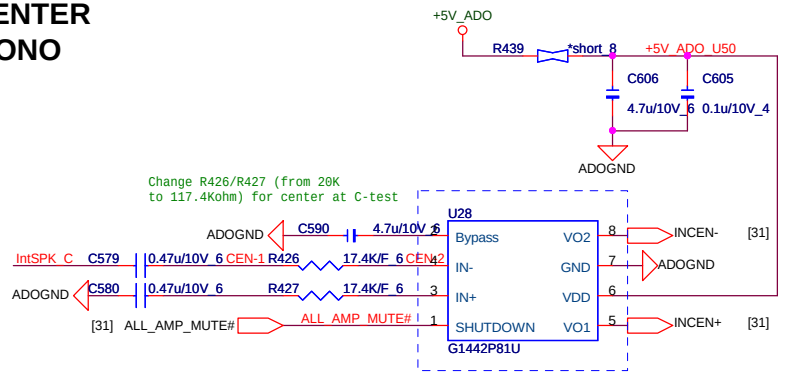
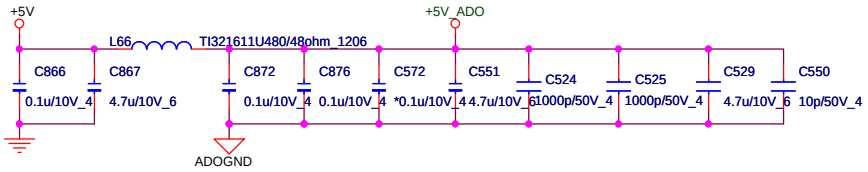
CODEC(ALC669X)



CENTER MONO



CODEC/AMP Power



PCH_AZ_CODEC_RST#

C481 *100p/6.3V_6

FOR ESD

Quanta Computer Inc.

PROJECT : ZYF

Size	Document Number	Rev
	REALTEK ALC889X/MONO-AMP	1A
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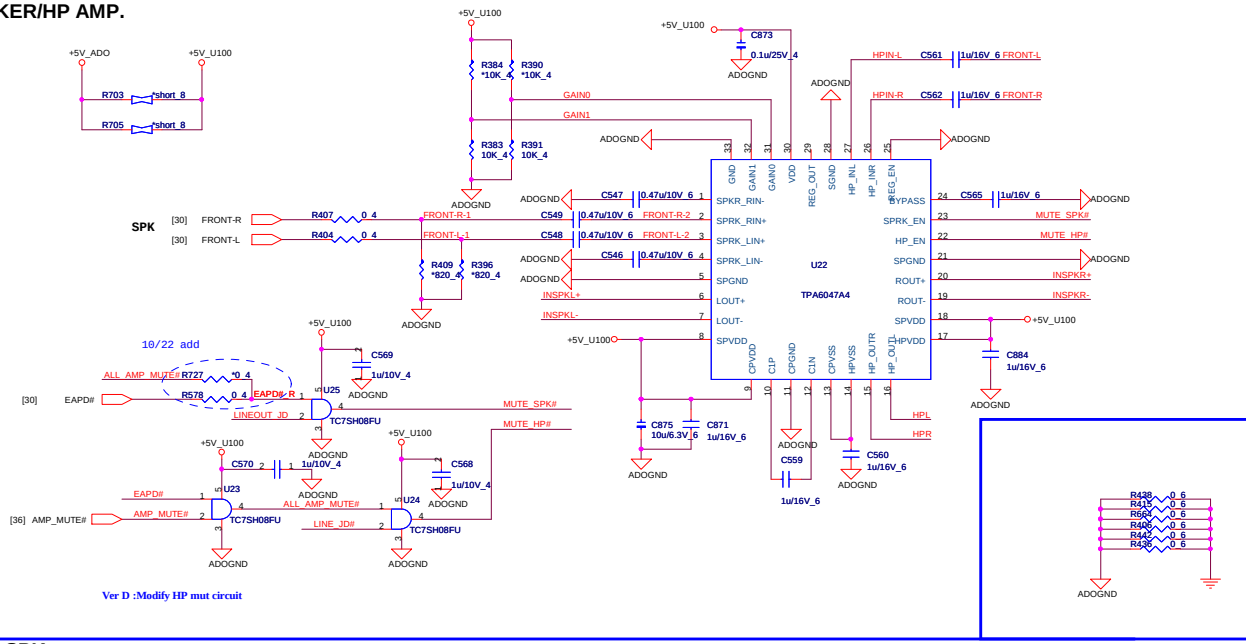
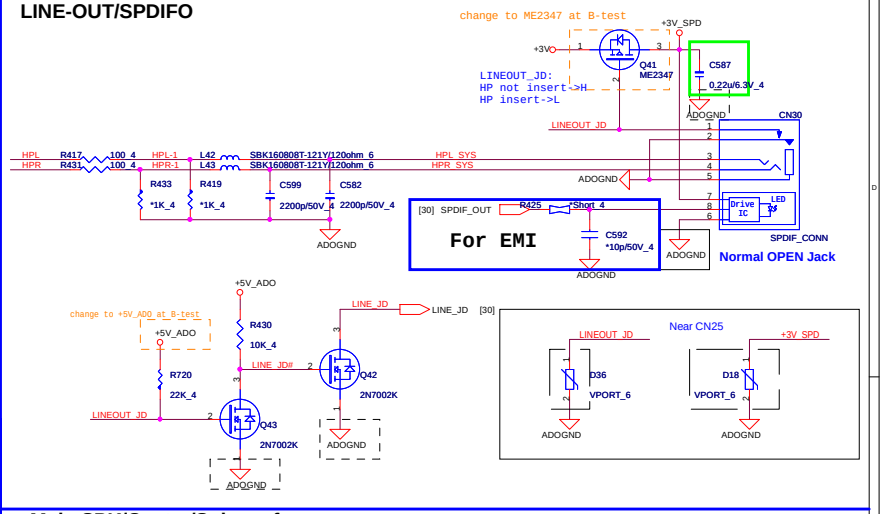
SPEAKER/HP AMP.

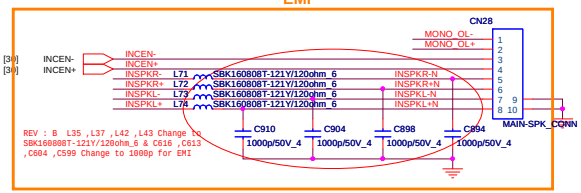


LINE-OUT/SPDIFO

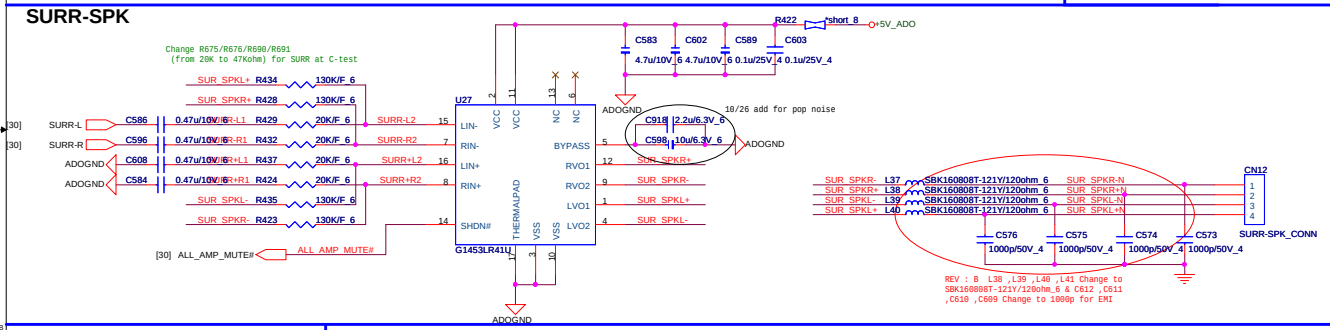


Main SPK/Center/Subwoofer

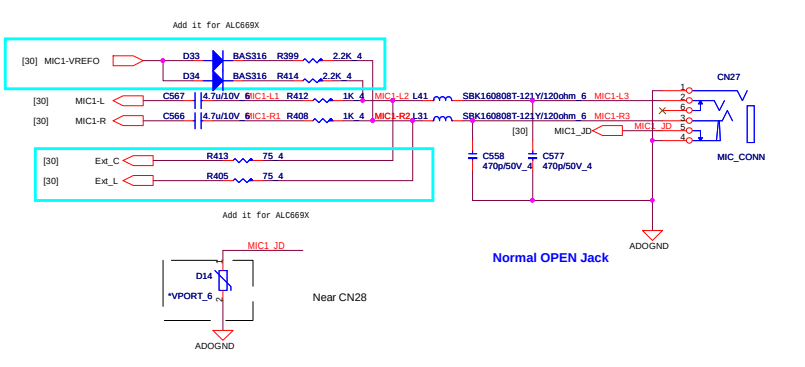
EMI



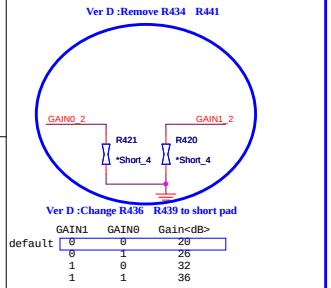
SURR-SPK



MIC

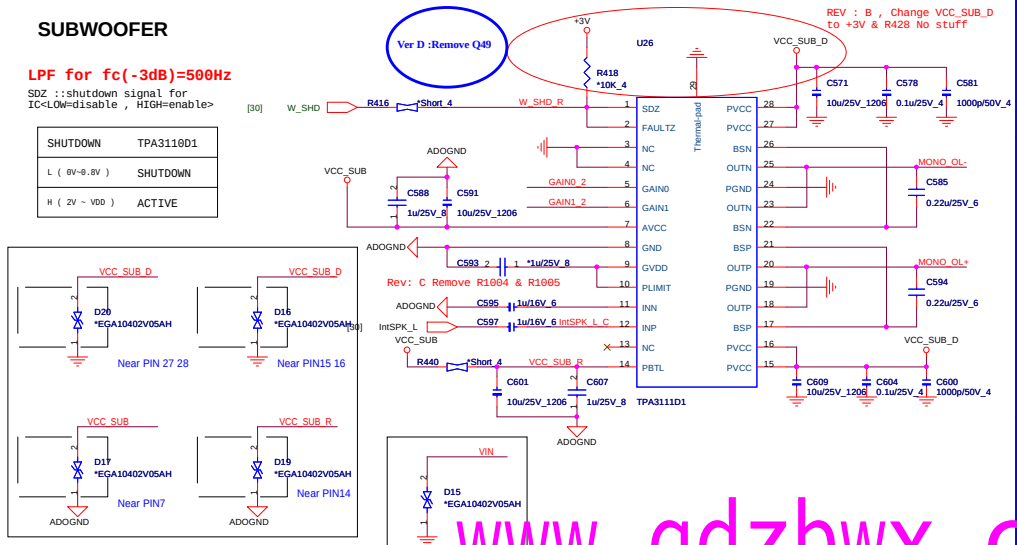


AMO GAIN



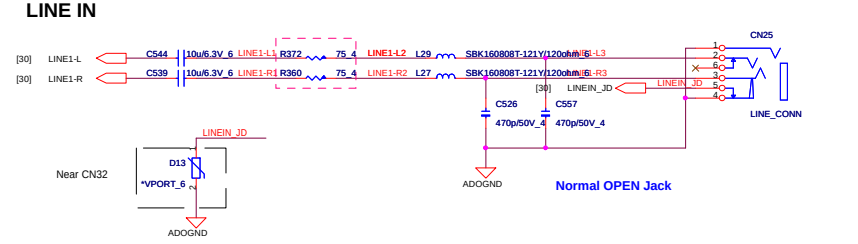
GAIN1	GAIN0	Gain<dB>
default 0	0	20
0	1	26
1	0	32
1	1	36

SUBWOOFER

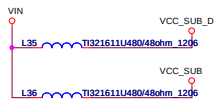


SHUTDOWN	TPA3110D1
L (0V~0.8V)	SHUTDOWN
H (2V ~ VDD)	ACTIVE

LINE IN

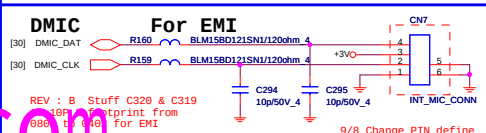


SUBWOOFER Power(AMP)



DMIC

For EMI



Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	AMP/AUDIO JACK/WOOFER	1A
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Card Reader

20mil
C896 10u/6.3V_6
C888 0.1u/10V_4
C892 0.1u/10V_4
8/18 change 0603 type

+3V R709 *short_8 VD33
40mil
C890 0.1u/10V_4

MDIO[0:5] signals skew should be smaller +/- 200mil for SDA 3.0

VD33
C879 0.1u/10V_4
C878 0.22u/6.3V_4
R698 22_4 XD_CE#
C874 *18P/50V_4
VD18
C877 0.1u/10V_4

SDXD/MS_DATA0 SDXD/MS_DATA1 SDXD/MS_DATA2 SDXD/MS_DATA3 XD_CE#_R XD_WE XD_CLE 1394_XOUT 1394_XIN

C886 0.1u/10V_4
[3,9,17,29,33,34,36] PLTRST# R704 100/F_4 A_RST#_PCIC
[9] CLK_PCH_SRC5#
[9] CLK_PCH_SRC5
7/30 modify
VD18
12K_4 R708 APREXT
[9] PCIE_TX5+ PCIE_TX5+
[9] PCIE_TX5- PCIE_TX5-
[9] PCIE_RX5- PCIE_RX5- C903 0.1U/10V_4 PCIE_RX5-_C
[9] PCIE_RX5+ PCIE_RX5+ C902 0.1U/10V_4 PCIE_RX5+_C

JMB388 A
U43
JMB388A

XRSTN XTEST APCLKN APCLKP APVDD APGND APREXT APRXP APRXN APV18 APTXN APTXP
T-PAD MDIO0 MDIO1 MDIO2 MDIO3 DV33 SSDV33_18 MDIO5 MDIO4 MDIO7 TXOUT TXIN DV18
TREXT TPBIAS_1 TPA1P TPA1N TPB1P TPB1N TAV33 MDIO8 MDIO9 MDIO10 MDIO11 MDIO12
CPPE_N CR1_CD2N CR1_CD1N CR1_CD0N CR1_PCTLN DV18 DV33 DV33 CR_LEDN MDIO14 MDIO13 MDIO6

R697 12K_4 TPBIAS0
1394_TPA0+ 1394_TPA0- 1394_TPB0+ 1394_TPB0-
VD33
XD/MMS_DATA4 XD/MMS_DATA5 XD/MMS_DATA6 XD/MMS_DATA7 XD-RE#

SD\XD_WP# R712 1K_4 MMI_VCC
XD_R/B R713 1K_4
MMI_VCC
C906 10u/6.3V_6
20mil
8/18 change 0603 type

+3V R714 *10K_4
R721 *0_4
9/9 add
[10] CR_CPPE#
[10] CR_WAKER# *BAS316 D29
VD33
VD18
C905 10u/6.3V_6
C899 0.1u/10V_4

XD_CDSW# SD_C/D
C901 *0.1u/10V_4
C900 *0.1u/10V_4

C880 27P/50V_4 7mil 1394_XIN
Y4 24.576MHZ
C881 27P/50V_4 7mil 1394_XOUT
Close to pin (500mil)

MMI_VCC
C543 0.1u/10V_4
C541 0.1u/10V_4
C542 0.1u/10V_4
Close to CN11

CN11
XD_R/B XD_RE# XD_CE# XD_CLE SD/XD/MS_CMD XD_WE SD\XD_WP# SD/XD/MS_DATA0 SD/XD/MS_DATA1 SD/XD/MS_DATA2 SD/XD/MS_DATA3 XD_WE XD_CE# SD/XD/MS_DATA3 MS_INS# SD/XD/MS_DATA2 SD/XD/MS_DATA0
XD-R/B XD-RE XD-CE XD-CLE XD-ALE XD-WE XD-WP XD-D0 XD-D1 SD-DAT2 SD-DAT3 SD-CMD 4IN1-GND1 MS-VCC MS-SCLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0
MS-DATA1 MS-BS 4IN1-GND2 SD-VCC SD-CLK SD-DAT0 XD-D2 XD-D3 XD-D4 SD-DAT1 XD-D5 XD-D6 XD-D7 XD-VCC XD-CD-SW SD-WP-SW SD-CD-SW
SHIELD1-GND SHIELD2-GND SHIELD3-GND SHIELD4-GND
CONN_CARDREADER

8/4 modify
MMI_VCC
SD/XD/MS_DATA1 XD-WE XD_CE# SD/XD/MS_DATA0 SD/XD/MS_DATA2 SD/XD/MS_DATA3 XD/MMS_DATA4 SD/XD/MS_DATA1 XD/MMS_DATA5 XD/MMS_DATA6 XD/MMS_DATA7 XD_CDSW# SD\XD_WP# SD_C/D
20mil

As close as possible to CN35 Pin12

1394 [FIW]

10mil
TPBIAS0 C853 0.33u/6.3V_4
R661 56.2/F_4 R657 56.2/F_4
1394_TPA0+ 1394_TPA0-
1394_TPB0- 1394_TPB0+
R649 56.2/F_4 R652 56.2/F_4
10mil
R644 4.99K/F_4 C851 220P/50V_4

1394_TPB0- D9 *EGA10402V05AH
1394_TPA0- D11 *EGA10402V05AH
1394_TPA0+ D12 *EGA10402V05AH
1394_TPB0+ D10 *EGA10402V05AH

CN24
1394_TPA0+ 1394_TPB0+ 1394_TPB0- 1394_TPA0-
1394_CONN

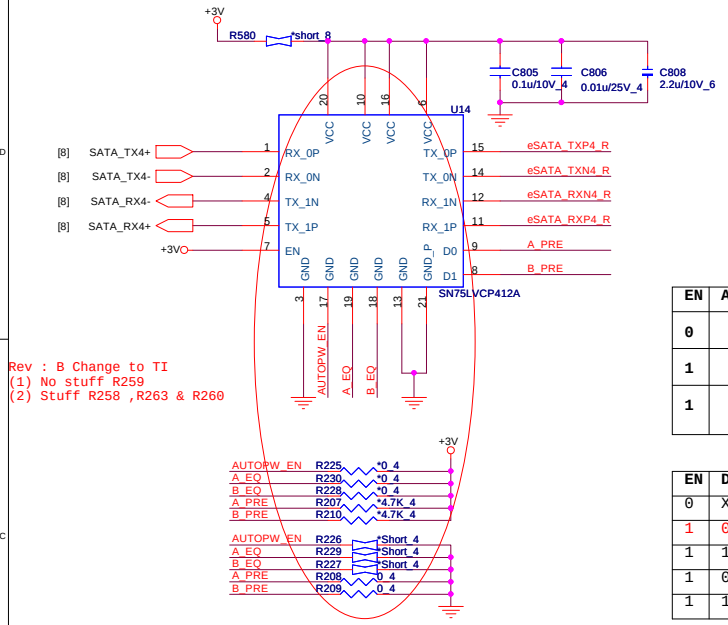
These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.

Power sequence

CN16
[35,36] NBSWON# +3V_S5
[7,36] DNBSWON#
[36,42] SUSON
[7,36] SUSB#
+3V +VCC_GFX +VCC_CORE
[7,36] PWROK_EC
[3,9,17,29,33,34,36] PLTRST#
+3V_D +1V +1.8V_GPU
[9,19] GPU_RST#
TP73
S5_ON [36,38,41,48] ICH_RSMRST# [7,36] SUSC# [7,36] 1.5V_SUS MAINON [36,42,47] GFX_PWRGD [36,39] VRON [36,39] HWPG [36] SYS_PWROK [3,7,17] dGPU_VRON [10,21,44]
VGPU_CORE_IO +VGPU_CORE +1.5V_GPU
dGPU_PWROK [10,21] SUS_STAT# [7]
*CON30_DEBUG

Quanta Computer Inc.
PROJECT : ZYF
Size | Document Number: Card Reader & 1394 | Rev 1A
Date: Monday, November 08, 2010 | Sheet 32 of 50

ESATA & USB



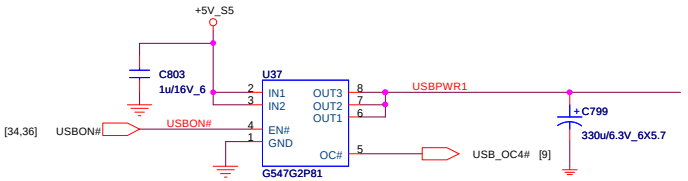
Rev : B Change to TI
(1) No stuff R259
(2) Stuff R258 ,R263 & R260

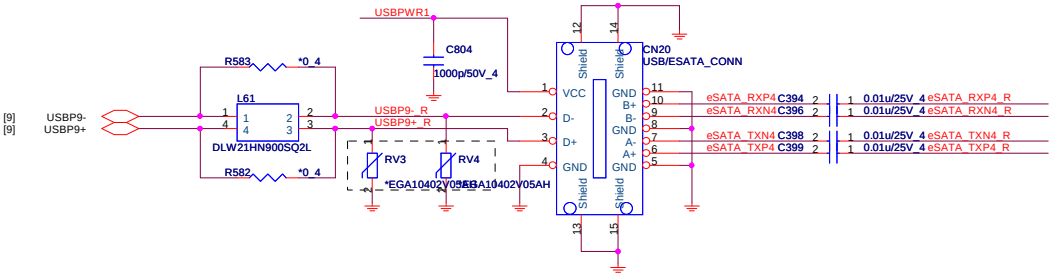
AL008511001

EN	A_PRE	B_PRE	dB
0	X	X	Power down mode
1	0	0	Pre-emphasis disable
1	1	1	Pre-emphasis enable

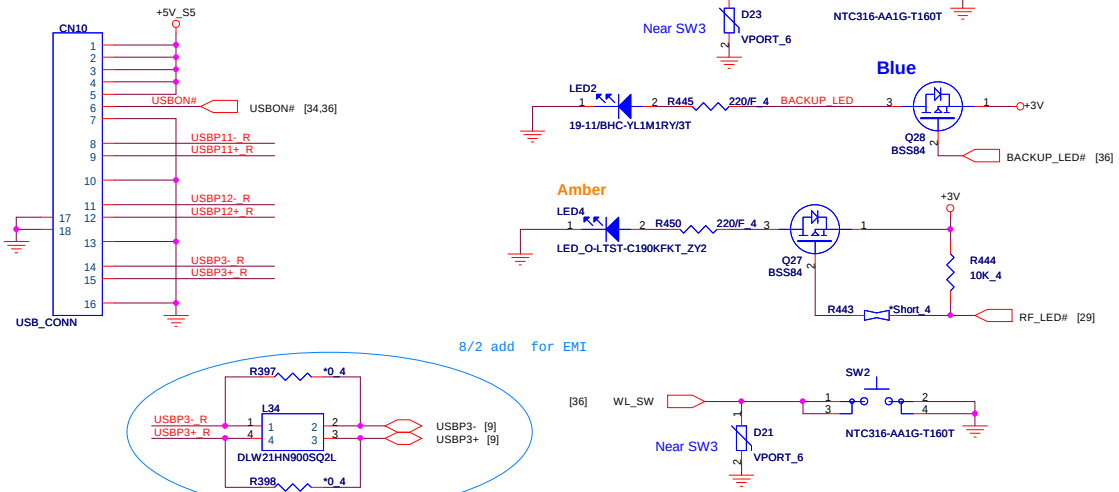
ALLVC412000

EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

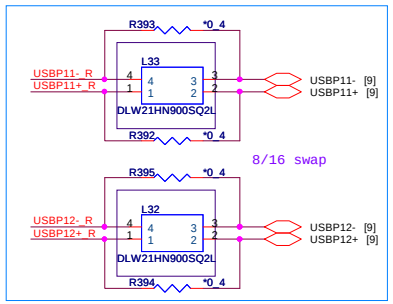




To USB/B



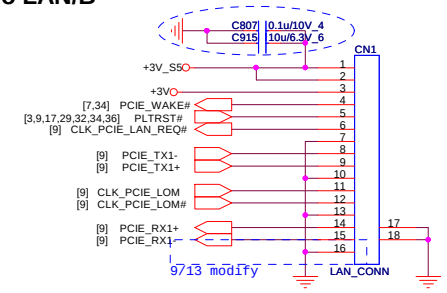
8/2 add for EMI



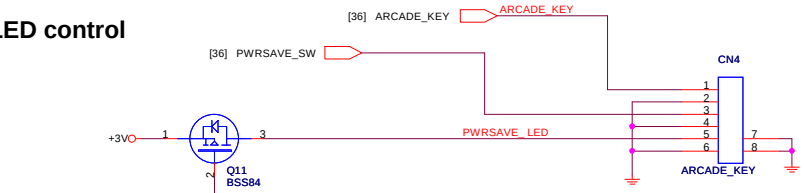
8/2 add for EMI

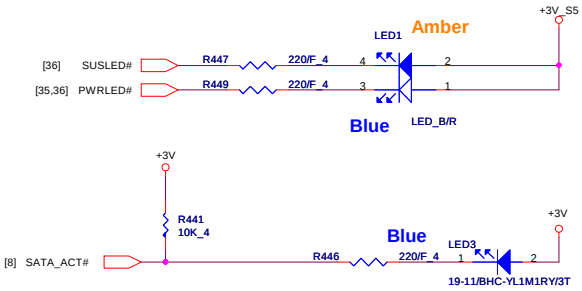
To LAN/B

10/22 add



Keyboard LED control





Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	USB/eSATA/TP_Screen	1A

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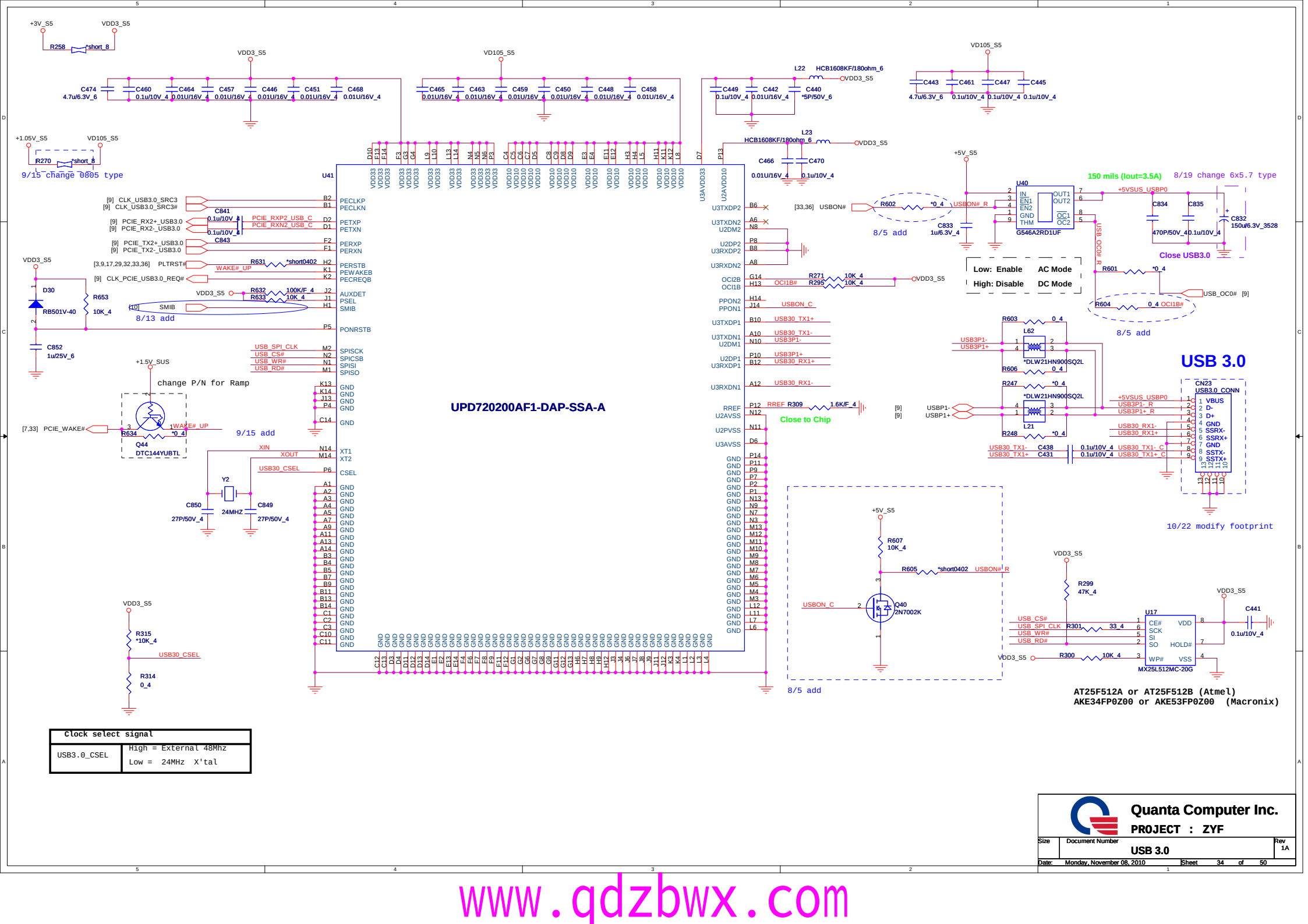
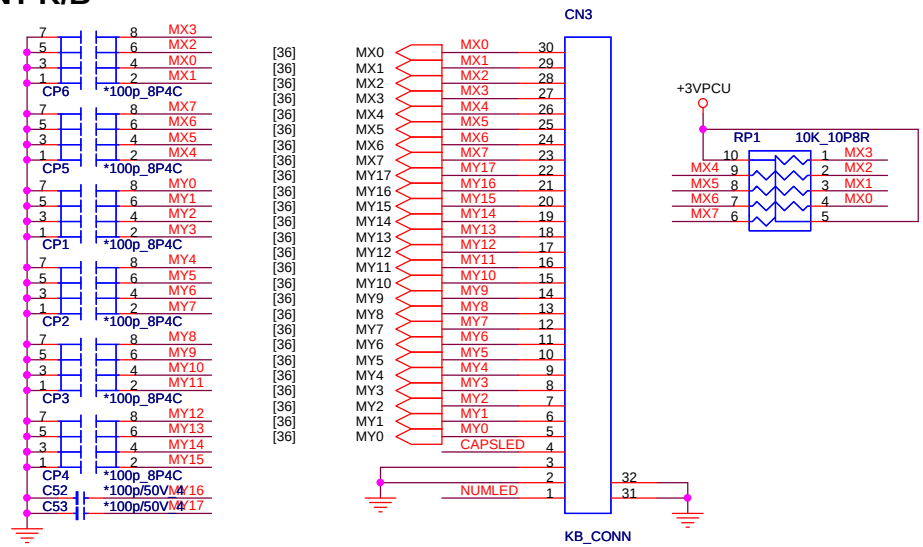
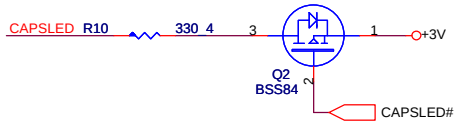


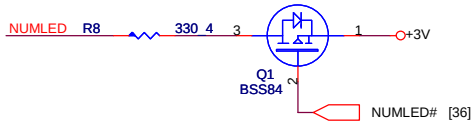
INT K/B



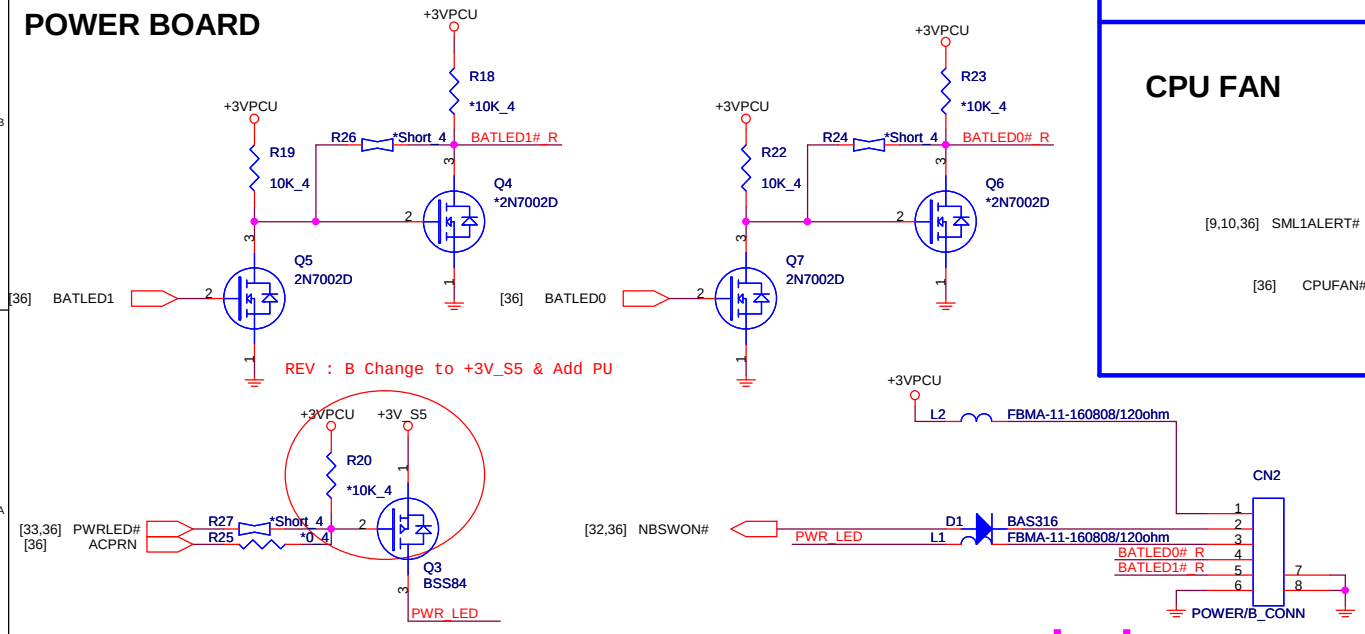
AMBER LED (HKC)



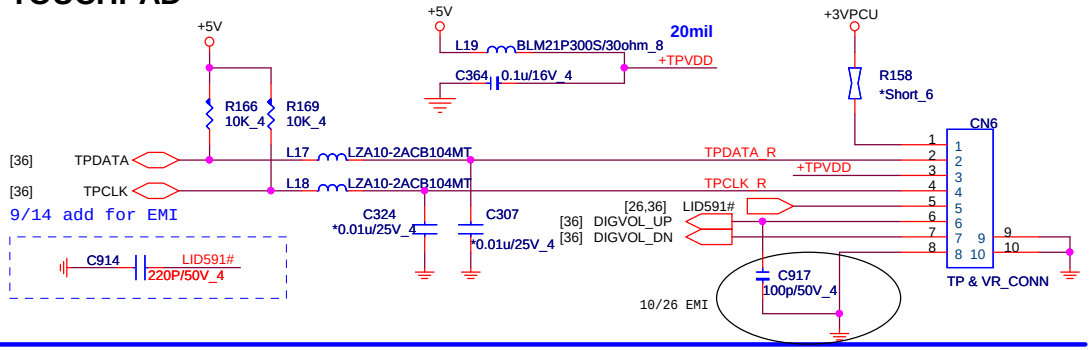
AMBER LED (HKC)



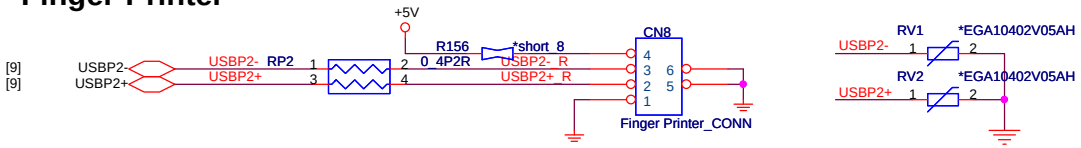
POWER BOARD



TOUCHPAD

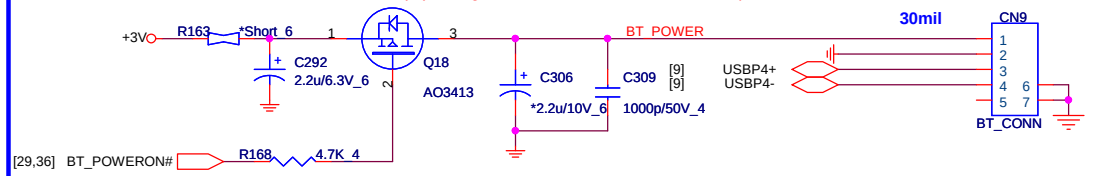


Finger-Printer

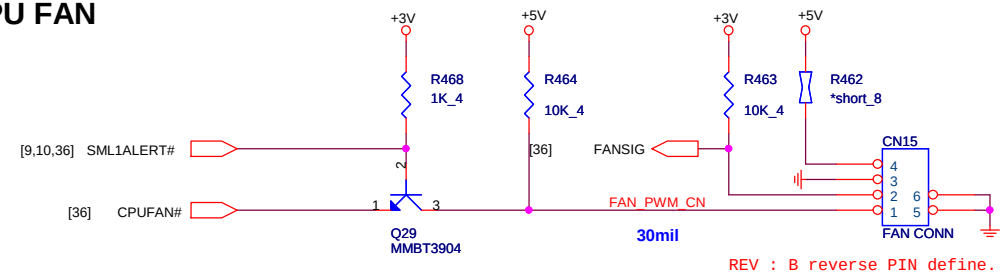


BLUETOOTH

Rev: B (1) del. R575
(2)change C789 from .33u to 2.2u
(3)Change R574 from 4.7K to short pad



CPU FAN



Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	KB/FAN/TP+FP/BT	1A

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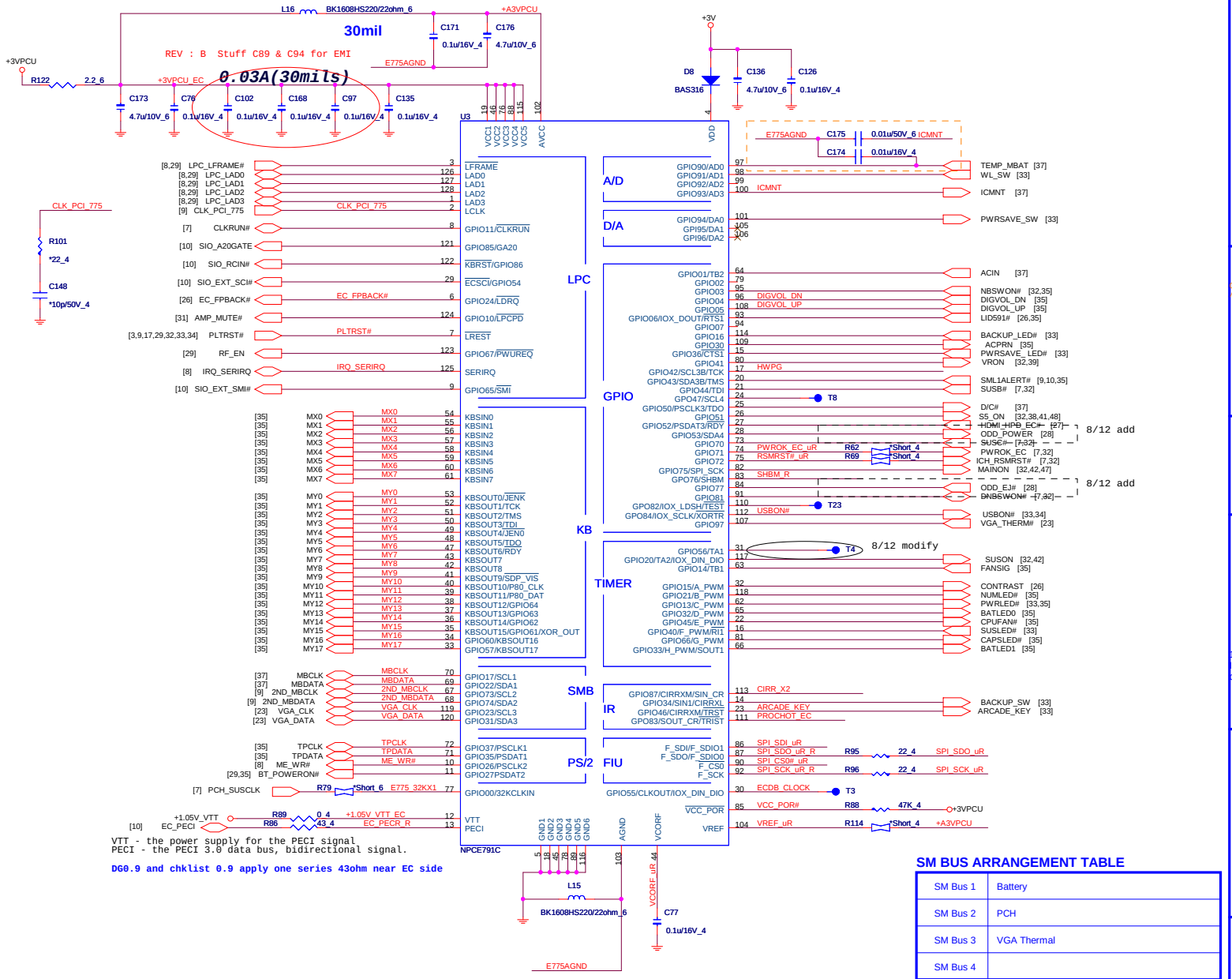
EC



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	

I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

SHBM R84 *10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

Change pull-up resistor (R148 /R154) from 10K to 4.7Kohm

MBCLK R60 4.7K_4
MBDATA R51 4.7K_4

2ND_MBCLK R48 10K_4
2ND_MBDATA R49 10K_4

REV : B Change from +3V to +3V_S5

VGA_CLK R112 10K_4
VGA_DATA R113 10K_4

INTERNAL KEYBOARD STRIP SET

MY0 R43 10K_4

SPI FLASH

U7 W25X16AVSSIG

SPI_SDI_uR R104 22_4 SPI_SDI_uR_R
R103 100K_4 SPI_SDI_uR pull-down 100Kohm at B-test
SPI_SDO_uR
SPI_SCK_uR
R97 10K_4 SPI_CS0#_uR
C236 0.1u/16V_4

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add
Winbond W25X16AVSSIG
AKE38ZP0N01
EON EN25F16-100HIP
AKE38ZA0Q00
AMIC A25L016
AKE38ZN0800

R133 0_4 H_PROCHOT# [3,39]
PROCHOT_EC
Q15 2N7002K
R129 100K_4

HWPG

R52 10K_4
HWPG [32]
[47] HWPG_1.8V D5 BAS316
[43] HWPG_VCCSA D2 BAS316
[42] HWPG_VDDR D7 BAS316
[38] SYS_HWPG D3 BAS316
[32,39] GFX_PWRGD D4 MS@BAS316
[41,43] HWPG_VTT D6 BAS316

7/29 modify

VR Cap.

R102 *10K_4
R120 *10K_4
DIGVOL_UP
DIGVOL_DN
Place two near EC
C142 0.1u/16V_4
C172 0.1u/16V_4

POWER-ON Switch

Rev: B not stuff SW1

NBSWON#
SW1 *TIME-532-S-V-T/R

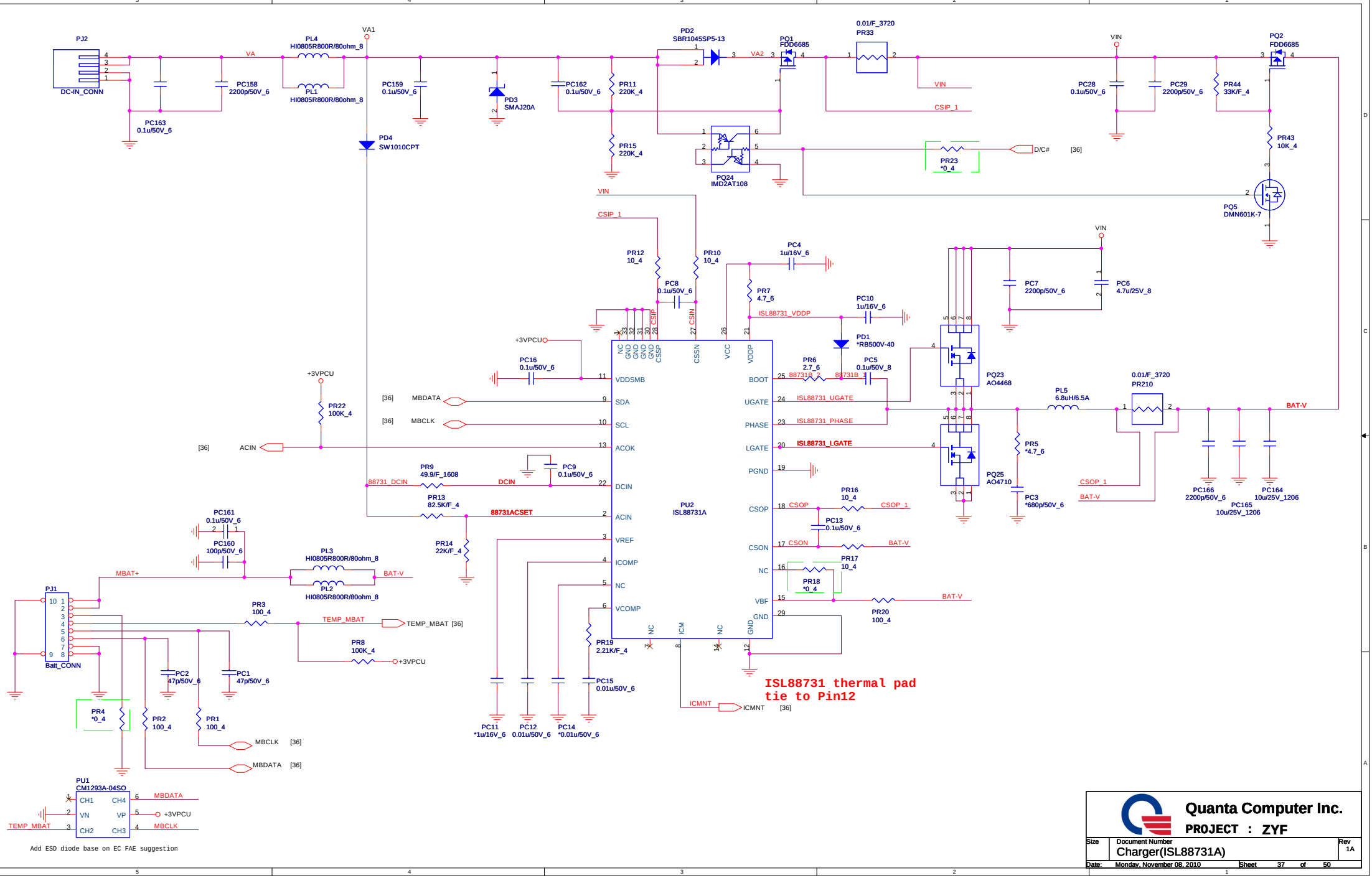
CIR

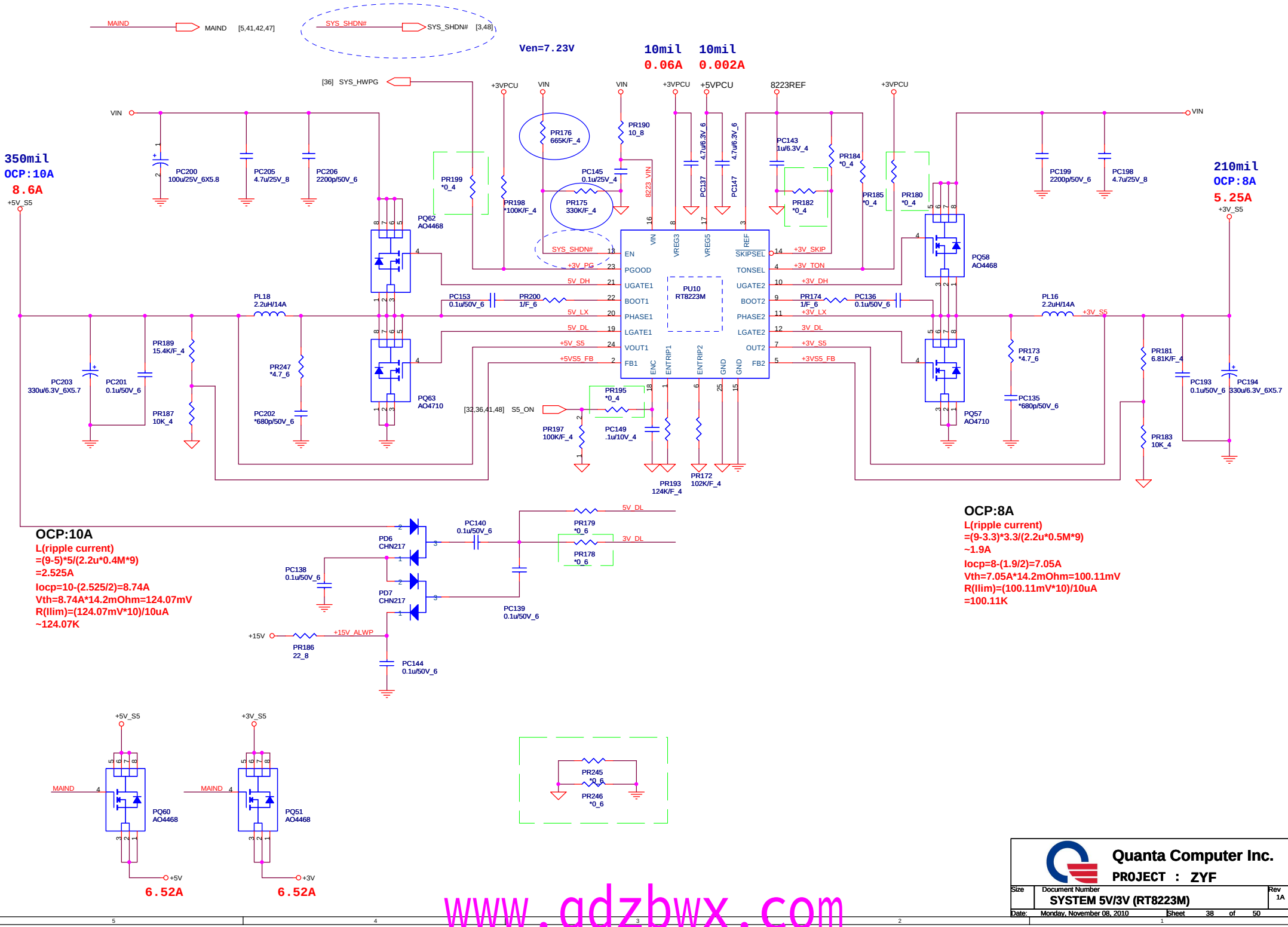
R448 *10K_4
CIRR_X2
C610 4.7u/10V_8
U29 IRM-V538-TR1
D22 *VPORT_6

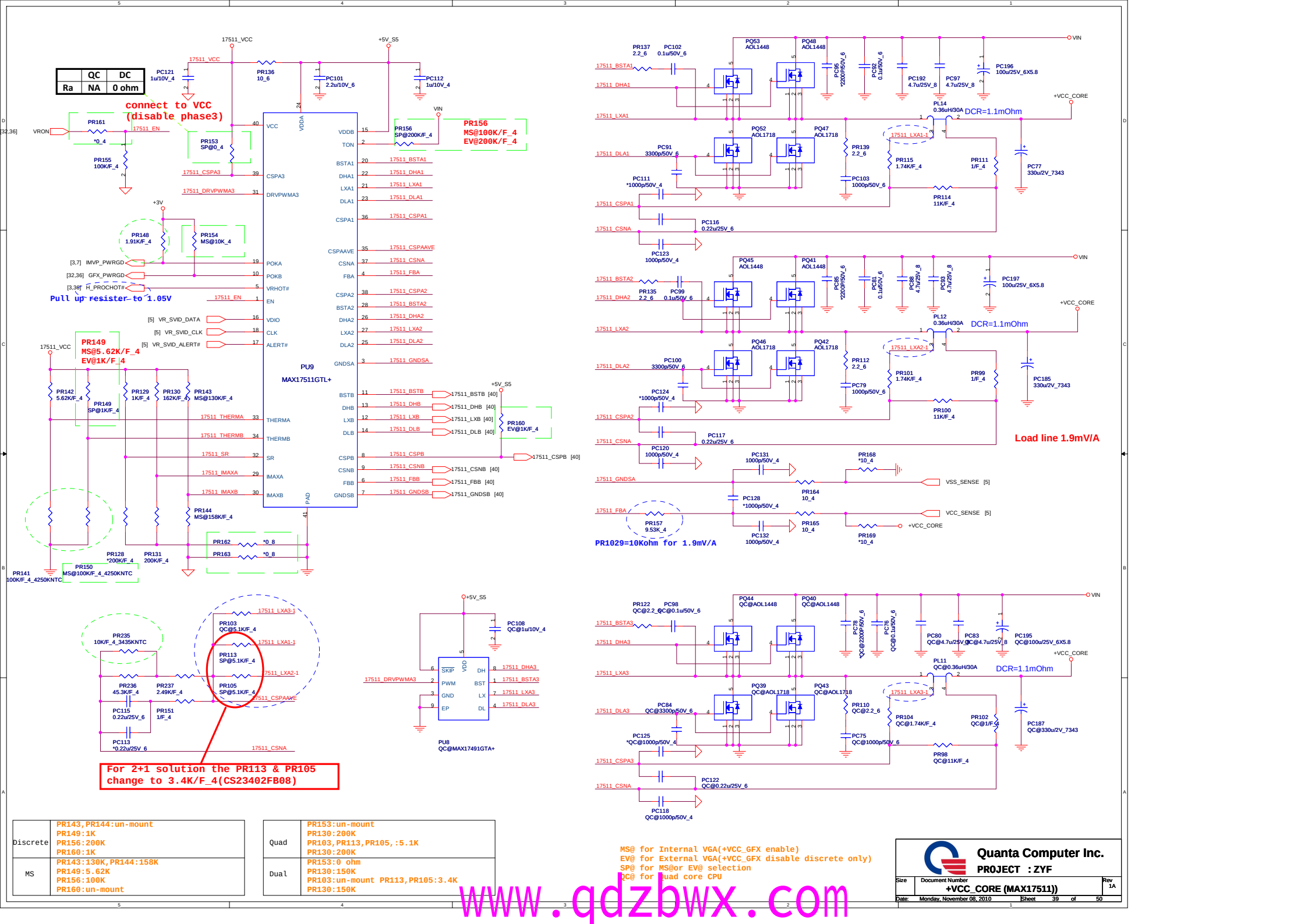
Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

Date: Monday, November 08, 2010 Sheet 36 of 50





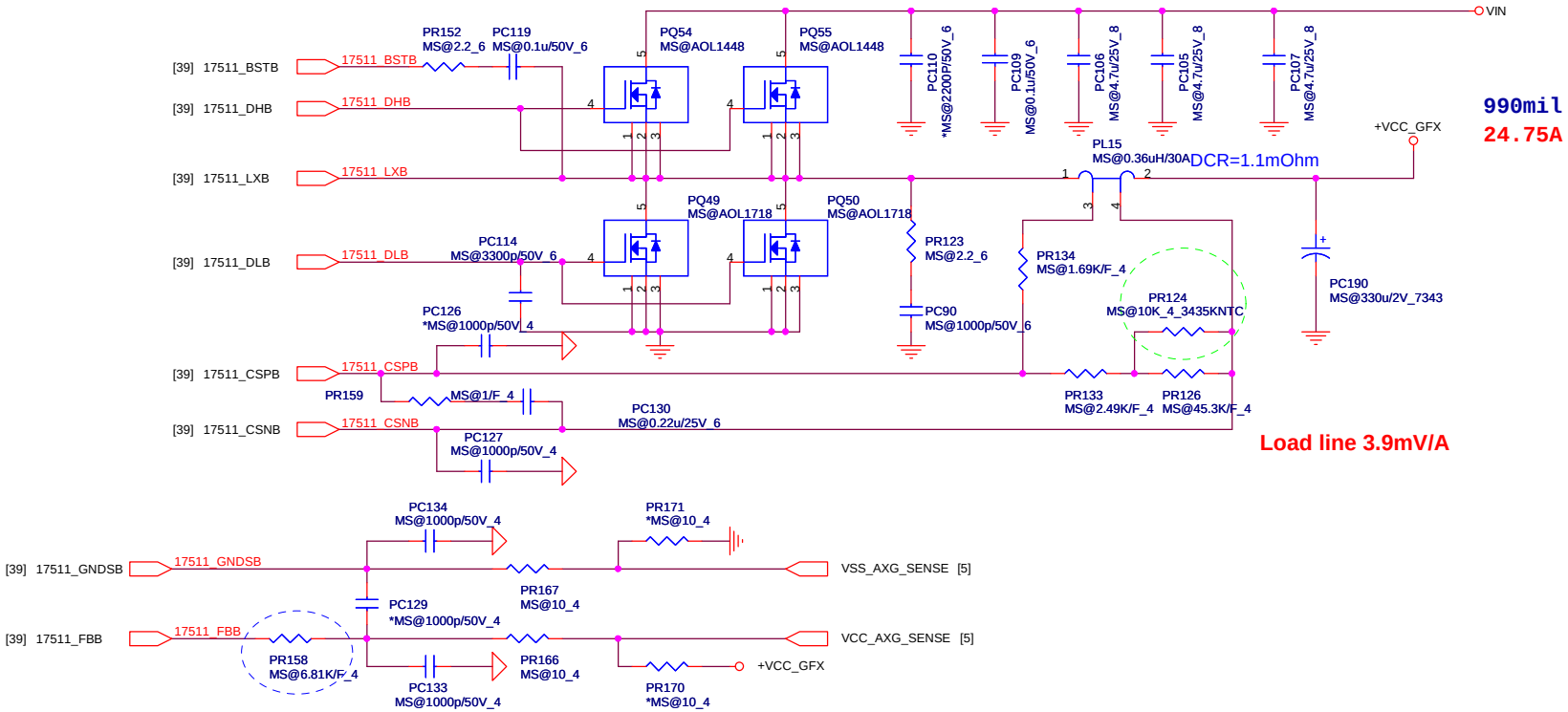


Discrete	PR143,PR144:un-mount PR149:1K PR156:200K PR160:1K
MS	PR143:130K,PR144:158K PR149:5.62K PR156:100K PR160:un-mount

Quad	PR153:un-mount PR130:200K PR103,PR113,PR105,:5.1K PR130:200K
Dual	PR153:0 ohm PR130:150K PR103:un-mount PR113,PR105:3.4K PR130:150K

MS@ for Internal VGA(+VCC_GFX enable)
EV@ for External VGA(+VCC_GFX disable discrete only)
SP@ for MS@or EV@ selection
QC@ for Quad core CPU

Size	Document Number	Rev
	+VCC_CORE (MAX17511))	1A
Date: Monday, November 08, 2010	Sheet 39 of 50	

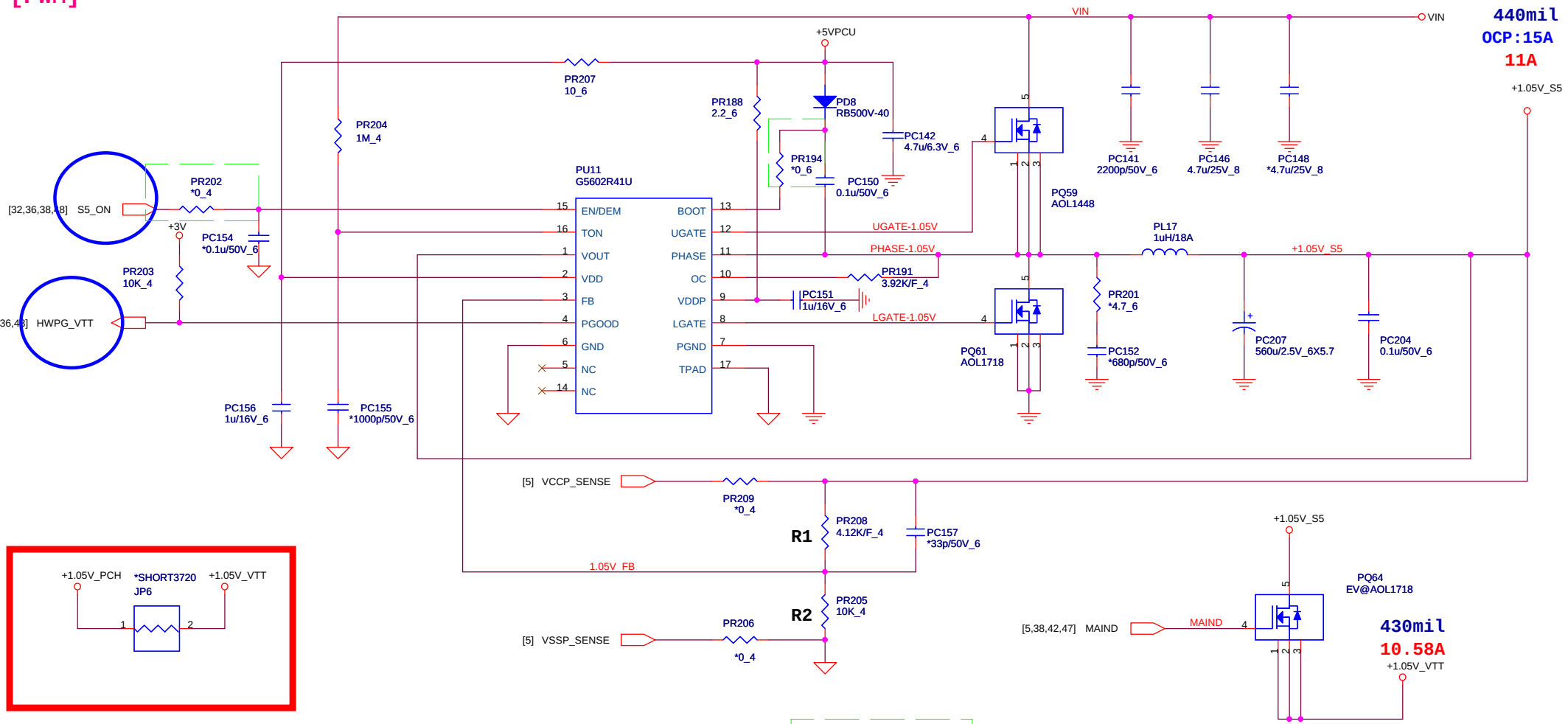


Quanta Computer Inc.

PROJECT : ZYF

Size	Document Number	Rev
	+VCC_GFX (MAX17511))	1A
Date: Monday, November 08, 2010	Sheet 40 of 50	

[PWM]



440mil
OCP:15A
11A

430mil
10.58A

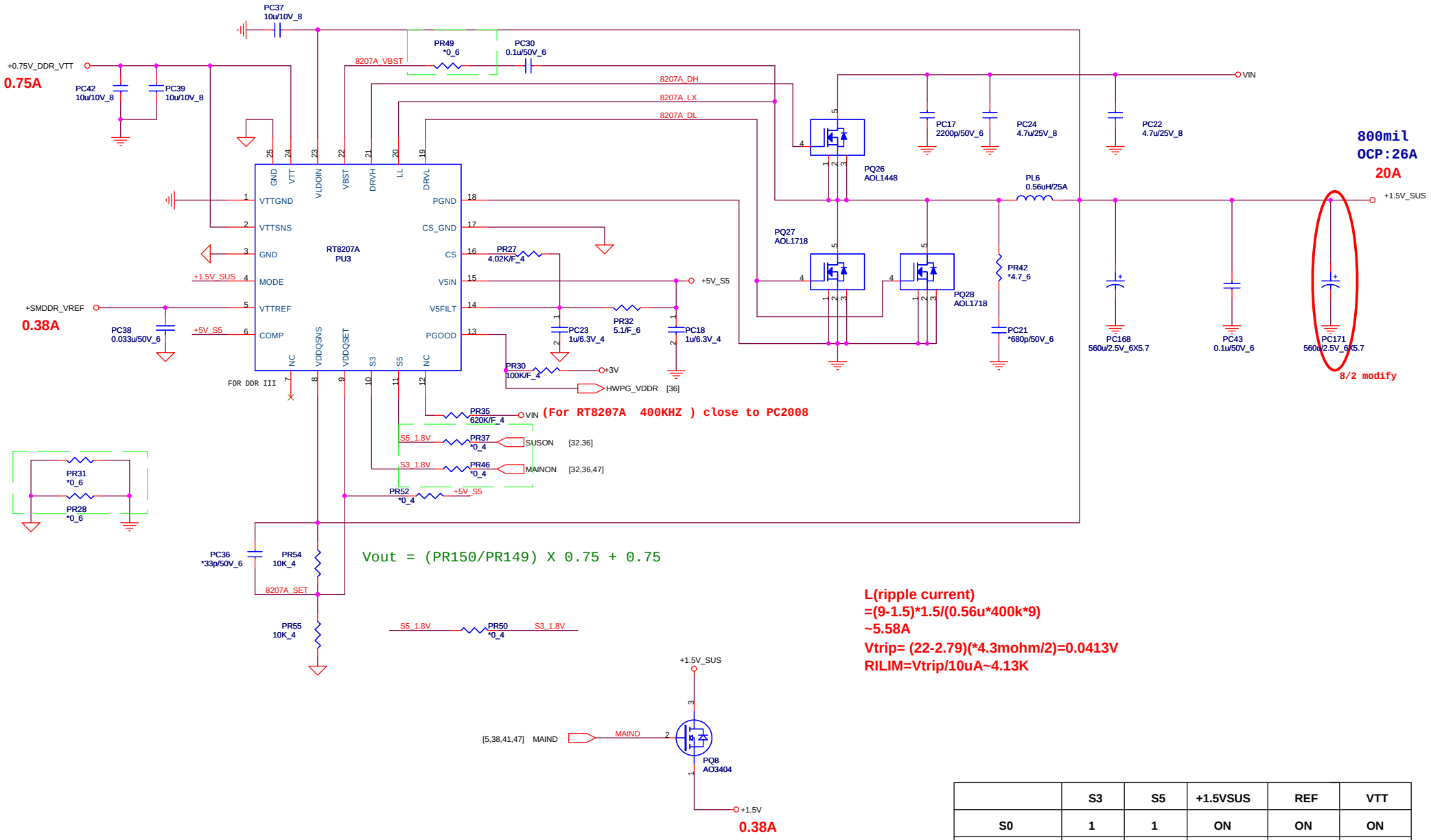
TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A
4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date: Monday, November 08, 2010	Sheet 41 of 50	

[PWM]



L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K

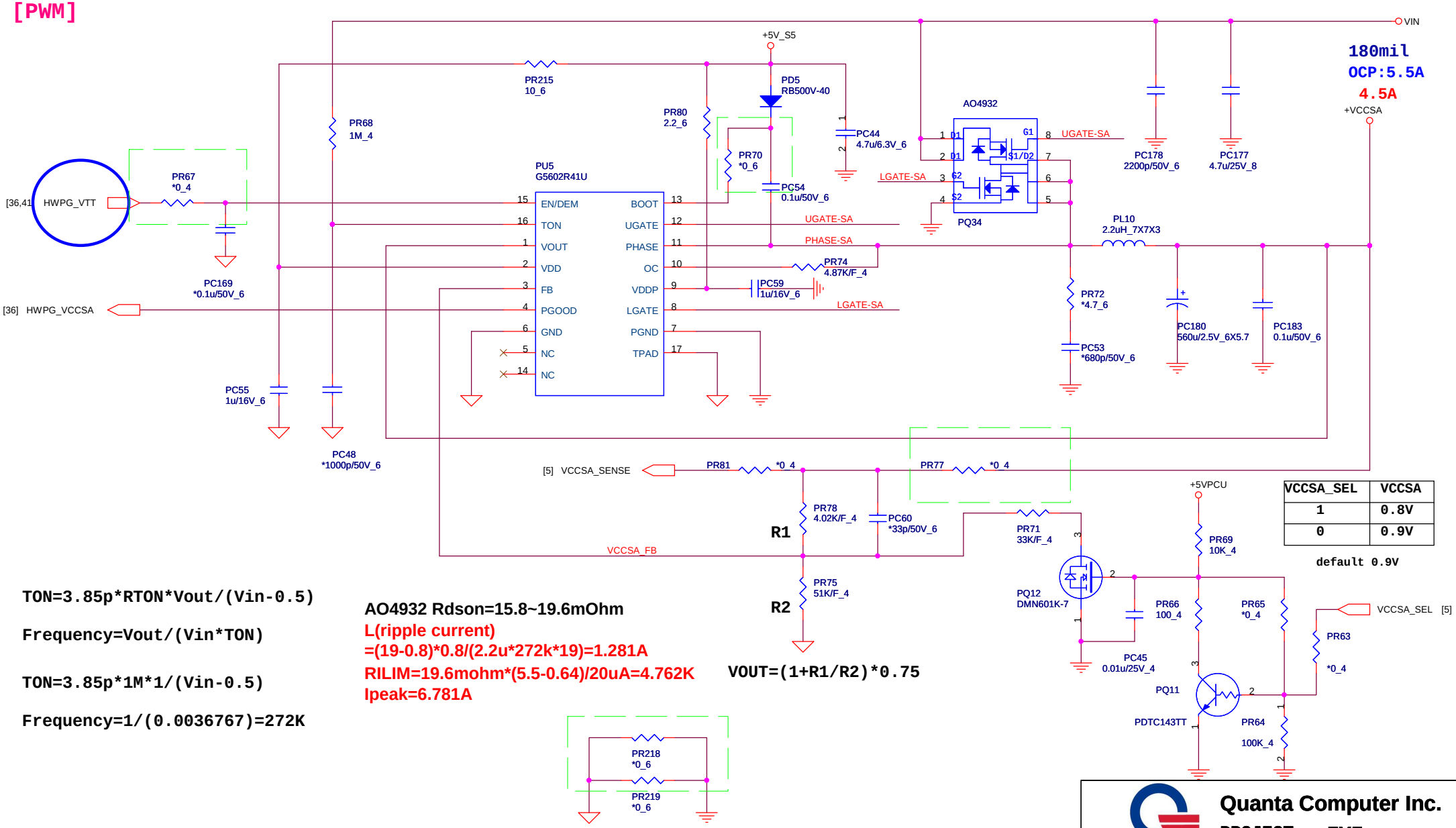
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

Date: Monday, November 08, 2010 Sheet 42 of 50

[PWM]



VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4932 Rdson=15.8~19.6mOhm

L(ripple current)
=(19-0.8)*0.8/(2.2u*272k*19)=1.281A

RILIM=19.6mohm*(5.5-0.64)/20uA=4.762K

Ipeak=6.781A

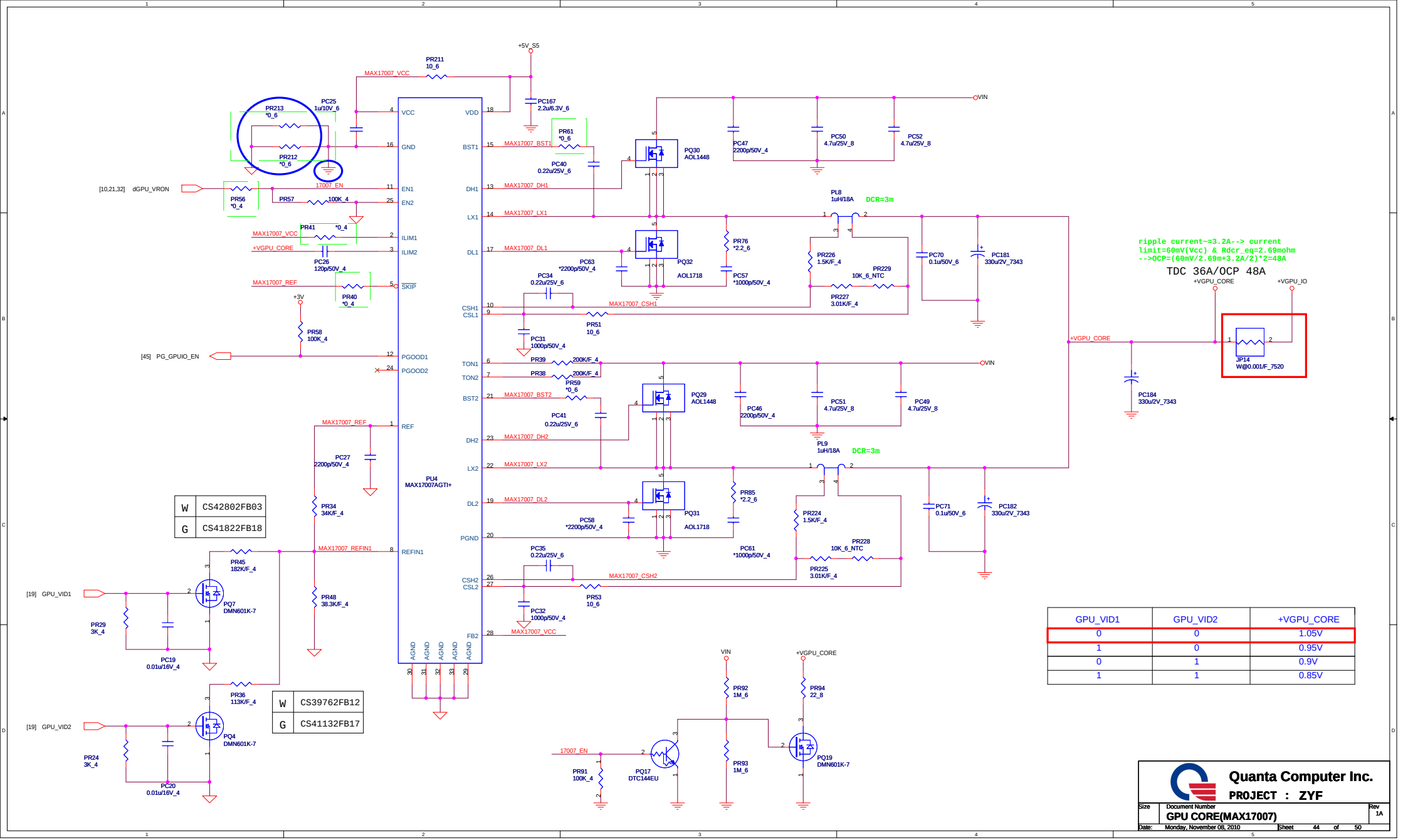
VOUT=(1+R1/R2)*0.75

Quanta Computer Inc.

PROJECT : ZYF

Size	Document Number	Rev
	+1.05V(UP6111AQDD)	1A

Date: Monday, November 08, 2010 Sheet 43 of 50



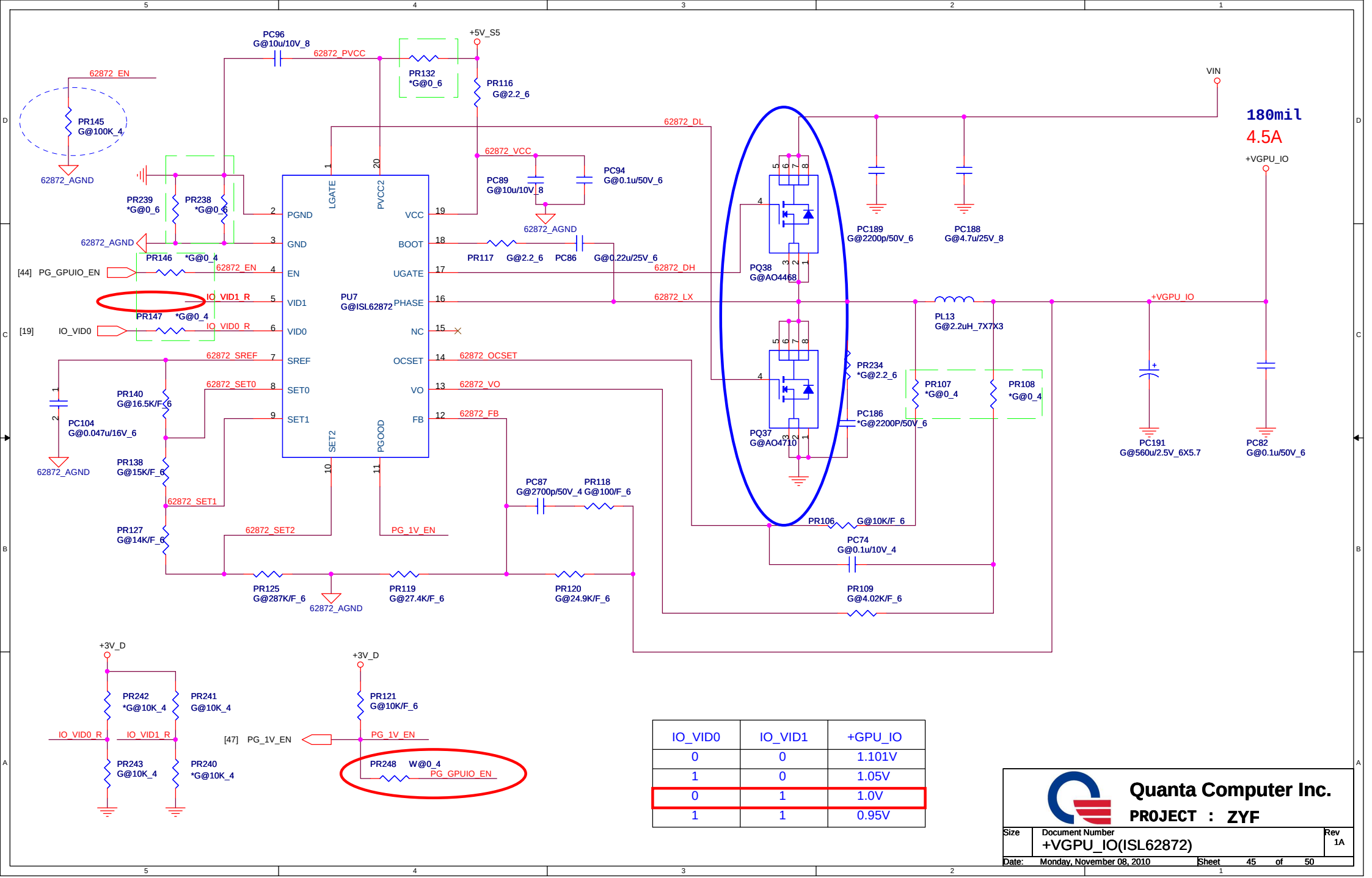
W	CS42802FB03
G	CS41822FB18

W	CS39762FB12
G	CS41132FB17

GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	1.05V
1	0	0.95V
0	1	0.9V
1	1	0.85V

Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	GPU CORE(MAX17007)	1A
Date: Monday, November 08, 2010	Sheet 44 of 50	



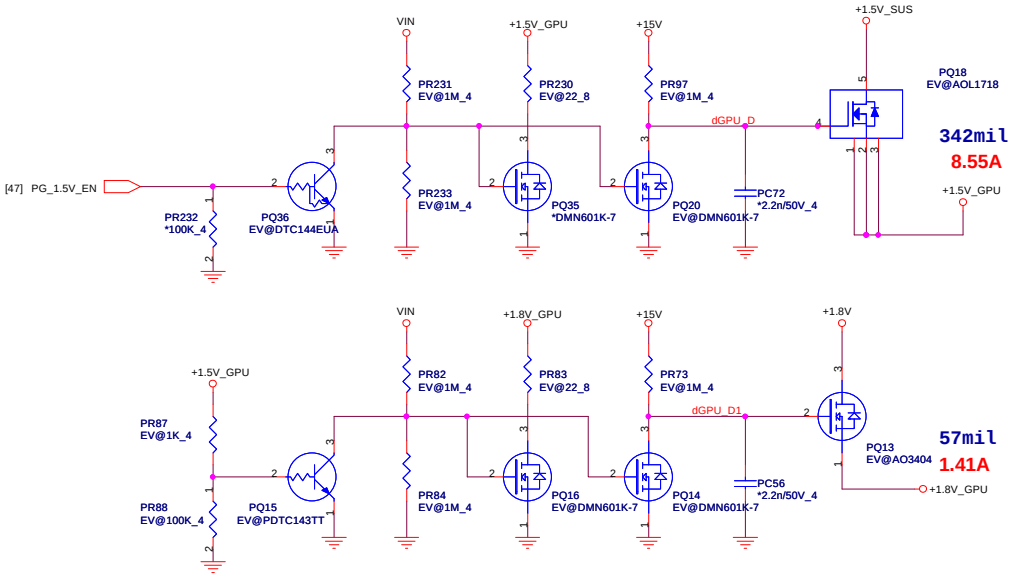
IO_VID0	IO_VID1	+GPU_IO
0	0	1.101V
1	0	1.05V
0	1	1.0V
1	1	0.95V

Quanta Computer Inc.

PROJECT : ZYF

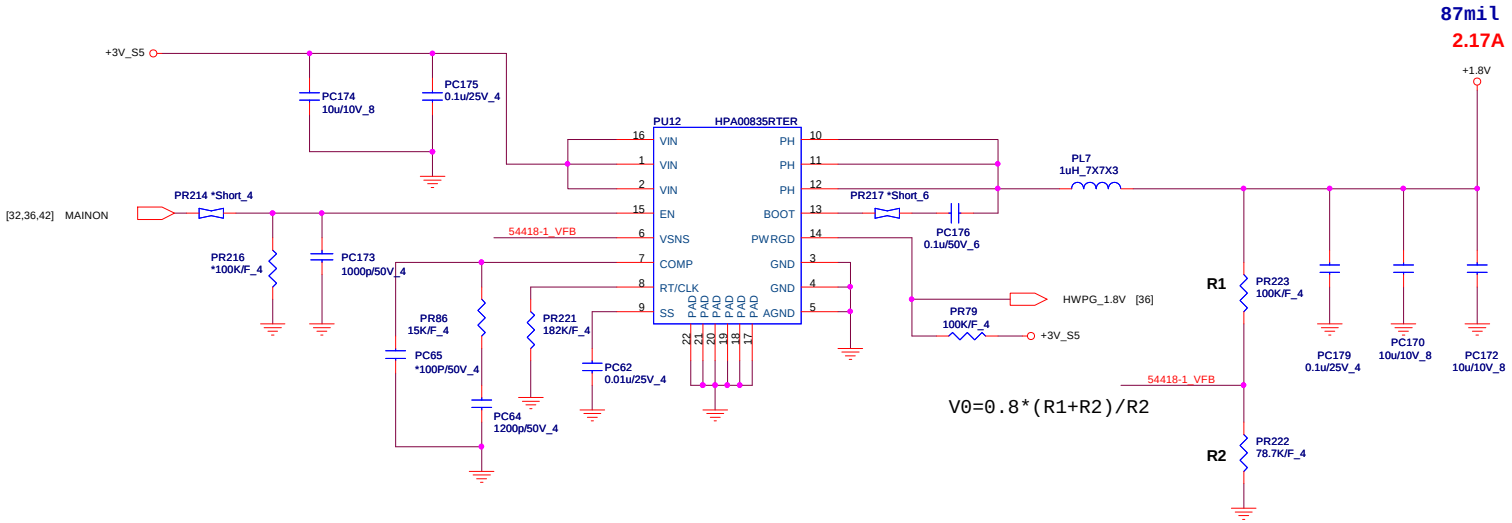
Size	Document Number	Rev
	+VGPU_IO(ISL62872)	1A

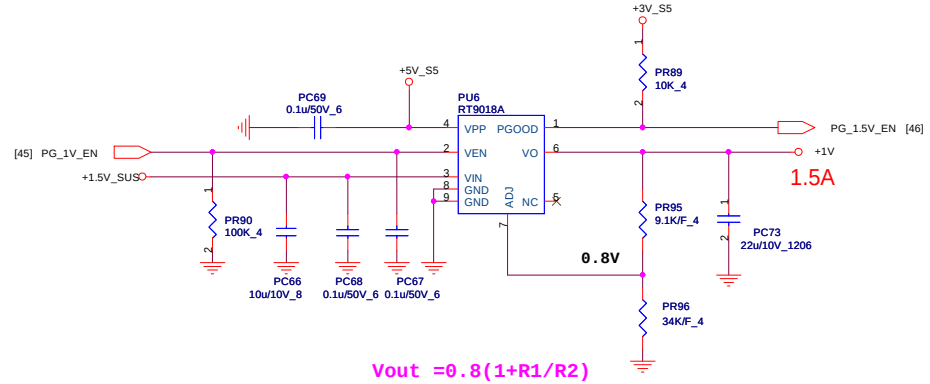
Date: Monday, November 08, 2010 Sheet 45 of 50

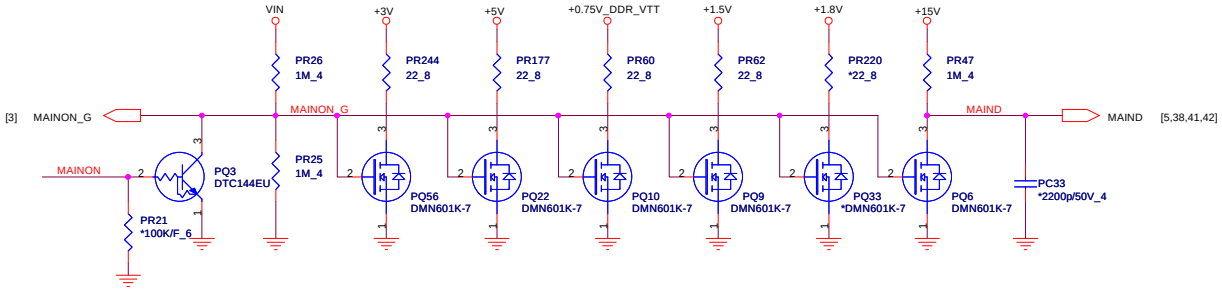


Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	GPU_PWR	1A
Date: Monday, November 08, 2010	Sheet 46 of 50	





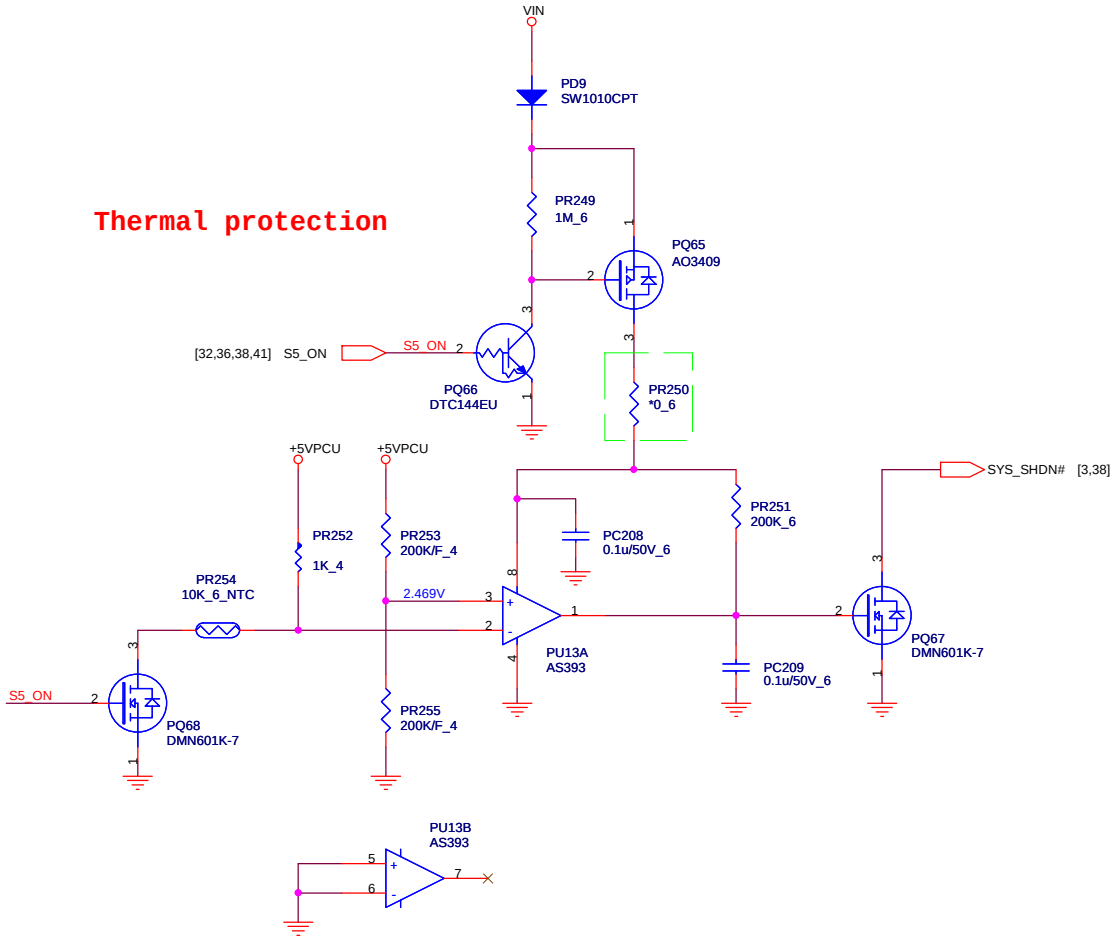


Quanta Computer Inc.
PROJECT : ZYF

Size	Document Number	Rev
	+1V/+1.8V/Discharge	1A

Date: Monday, November 08, 2010 Sheet 47 of 50

Thermal protection



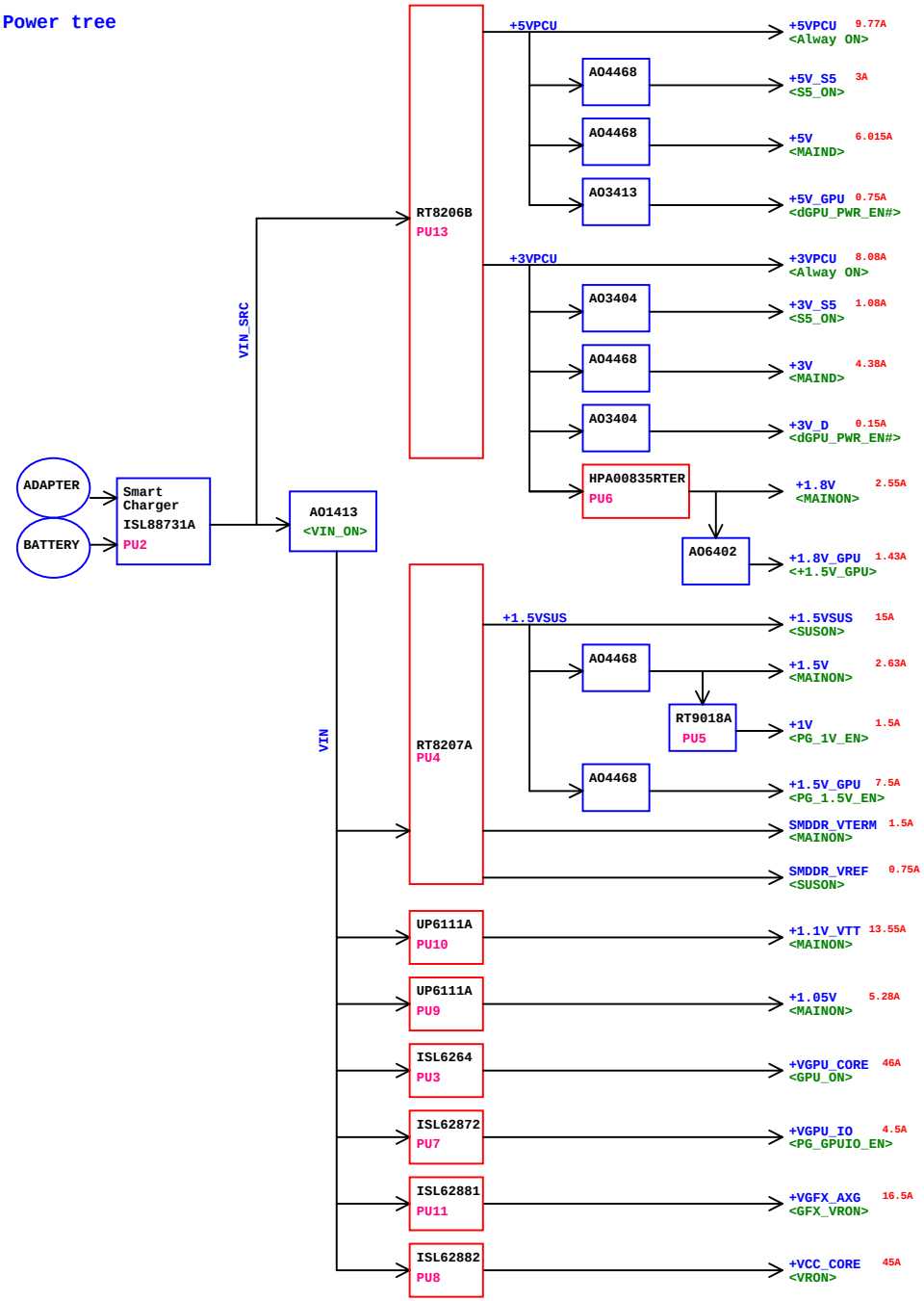
For EC control thermal protection (output 3.3V)

Quanta Computer Inc.

PROJECT : ZYF

Size	Document Number	Rev
	Thermal protect	1A
Date: Monday, November 08, 2010	Sheet 48 of 50	

ZYB Power tree



PROJECT : ZYB & ZYBA
Quanta Computer Inc.

Size	Document Number	Rev
	ZYA/B Power tree	1A
Date: Monday, November 08, 2010	Sheet 49 of 49	

Model

ZYF MB

CHANGE LIST

REV		
A	2010/07/27	page 40&41:Mark Lo change CPU solution page 28:Delete HDMI Switch circuit & add R584,R585 for Muxless DATA,CLK pin page 33:add CN27 for power sequence
	2010/07/28	page 14:del R18,R30,R32,R32,R33,R39,R40,R45 page 16:del R47,R51,R60,76,R169,R180,R190,R213 Mark Lo change power circuit
	2010/07/29	page 9:change CN20 parts page 29:change CN22 & CN23 parts page 37:add T21,T23
	2010/07/30	page 28:add HDMI LEVEL SHIFTER circuit & del R584,R585 page 9:add R8421 page 8:add C1160,C1161 page 19:add T28
	2010/08/02	page 33:add L63,L64,L65 & R620,R621,R622,R623,R624,R625 for EMI
	2010/08/03	page 13:add R29,R30,C79 page 15:add R169,R179,C302 page 17:add hole 1~31& PAD1
	2010/08/04	page 5:del C8348,C8479 page 8:del C8363 page 9:add R8587 page 10:add R8496,R8480 page 13:del R31,TP8231 page 14:del R34,TP8232 page 15:del R217,TP8233 page 16:del R218,TP8234 page 19:del R93,R103 & add T30,T31,T32,T29 & del SOUT_GPIO8 ,SIN_GPIO9,SCLK_GPIO10,IO_VID1 net page 23:del U1,R58,R57,C80 page 26:del RN12,RN11,RN5,RN7 & add R535,R552,R557,R575,R576,R549,R577,R580 page 27:del R552,R556,R557,R576,R577,R580,R581,R583 page 32:add D16 & CR_WAKER# net page 34:add R1331
	2010/08/06	page 8:del R64,R65 page 32:add R245,R1332,Q20,R1334,R1333 & OCI1B# net & del C1268,R1317,R1318 page 34:CN31 change footprint
	2010/08/11	page 3: CLK_DPLL_SSCLKN_R net from GND change PU to +1.05V_VTT page 5:C8474 change to 3528 type page 11: del R8498
	2010/08/12	page 8: add PCH_ODD_EN net page 10: add ODD_PRSNT# net ,R8498 & CR_CPPE# net page 28: add ODD Power circuit page 36: add ODD_EJ# & ODD_POWER net
	2010/08/13	page 4: SWAP DDR control pin page 10: add SMIB net for USB3.0
	2010/08/17	page 5: add PQ26 & change C682 to 3528 type,R8291,R8282 to 1206 type
	2010/08/18	Power engineer update power circuit page 32 :C895,C897& C896 change to 0603 type
	2010/08/19	page 34 :C1265 chnage to 6x5.7 type
C	2010/09/6	page 28 :CN22,CN26 change footprint page 32 :add R721
	2010/09/13	page 9 :add C912 page 9 :add R722,R723 for SMBus
	2010/09/14	page 3 :R567,R564 change short pad page 7 :R308,R306,R344 change short pad page 8 :R719 change short pad page 9 :Del R305 page 11 :R351,R310,R352,R66,R388,R620,R608,R659,R619,R274,R411,R410,R333,R669,R658,R349,R346,R337,R269,R272,R273, change short pad page 13 :R11 change short pad page 14 :R21 change short pad page 15 :R179 change short pad page 16 :R180 change short pad page 19 :add R724,R726,R725 page 26 :R153,R145 change short pad page 27 :R177 change short pad page 28 :R246,R716 change short pad page 29 :R1,R2 change short pad page 30 :R439,R364,R353,R332 change short pad page 31 :R703,R705,R422,R416,R440, change short pad page 32 :R709 change short pad page 33 :R580 change short pad page 34 :R258,R270,R605 change short pad page 35 :R158,R156,R462 change short pad
	2010/09/16	page 17 :Del CN21,R578,C807
3C	2010/10/22	page 30 :U28 pin1 chnge net name to ALL_AMP_MUTE# for "bo" noise & change footprint page 31 :add R727,R578 & ALL_AMP_MUTE# net for "bo" noise page 33 :add C807,C915

Quanta Computer Inc.

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