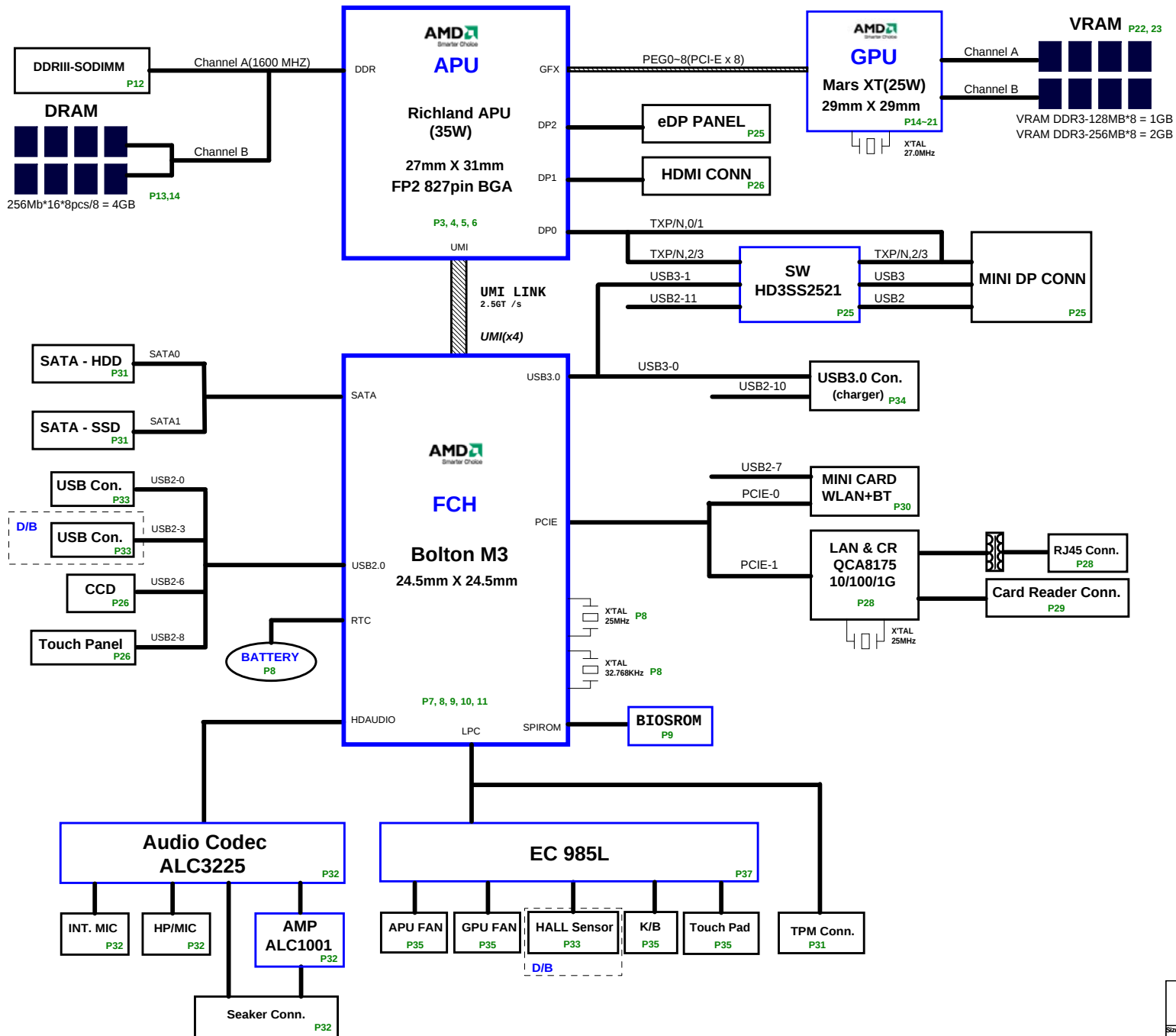


ZRI/ZQI Block Diagram



PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 6 : GND
LAYER 8 : BOT

Charger (BQ24737RGRR)	P38
SYSTEM 5V/3V (TPS51225RUKR)	P39
+1.5VSUS(TPS51216)	P40
+1.2V(TPS51211) / +2.5V	P41
1.1V_DUAL(TPS51211)	P42
+VDD_CORE (ISL62771)	P43
+VGPU_CORE(TPS51728)	P44
+PCIE_VDDC_GFX(TPS51211)	P45
+1.8V_GFX(TPS54318RTER)	P46
Discharge /Thermal	P47

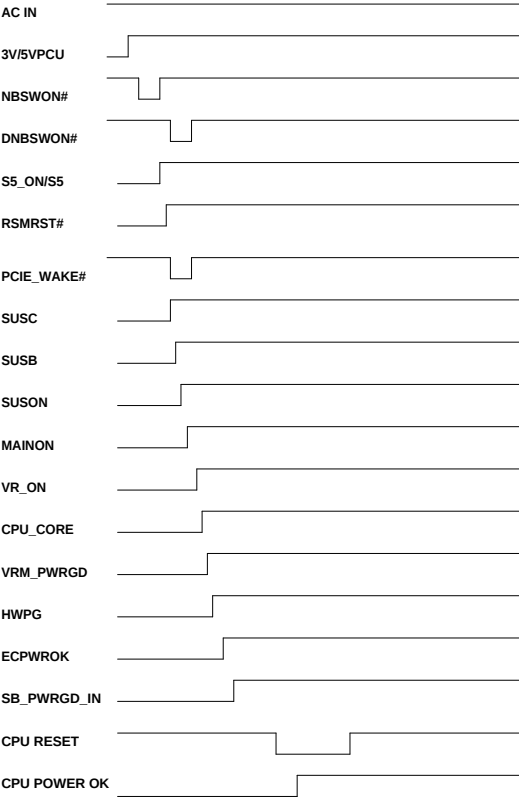
BOM Option

ITEM	DESCRIPTION	MARK
1	LVDS Panel Sku	LVDS@
2	eDP Panel Sku	eDP@
3	VGA Sku	EV@
4	VGA Thames Sku	EV_T@
5	VGA Mars Sku	EV_M@
6	VGA Sku for Thames and Mars stuff different value parts	EV_SP@
7	GPU 128bit Sku	EV_128@
8	GPU 128bit Sku of Special part value change	EV_128SP@
9	USB Charge Functions Sku	CH@
10	No USB Charge Functions Sku	NCH@
11	USB3.0 Re-Driver Sku	RD@
12	No USB3.0 Re-Driver Sku	NRD@
13	Always connect functions Sku	AC@
14	No Always connect functions Sku	NAC@
15	Special part value change or modify for different BOM sku	SP@
16	Key Board Back light Sku	KBL@
17	SSD Sku	SSD@
18	Touch panel Sku	TP@

Page 9 GPIO strap pin

ITEM	DESCRIPTION	MARK
1	Synaptics touch pad	SYNP@
2	ELAN touch pad	ELAN@
3	For UMA Sku	UMA@
4	ELPIDA on board DRAM	ELP@
5	HYNIX on board DRAM	HYN@

Power Sequence



Hudson M3 SMBUS

FCH SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD26 AD25	DDR / WLAN
SCLK1 SDATA1 (+3V_S5)	T7 R7	Touch Pad
SMB_EC_CLK (SCLK2) SMB_EC_DAT (SDATA2) (+3V_S5)	H19 G19	EC
SCLK3 SDATA3 (+3VPCU)	G22 G21	Not used
SCL4 SDATA4 (+3V_S5)	J19 K19	Not used

EC SMBUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	70 69	Battery, FCH
APU_SIC_EC APU_SID_EC (+3V_S5)	67 68	APU
GPUP_CLK GPUP_DATA (+3V_GFX)	119 120	GPU
TPCLK TPDATA (+3V)	72 71	Touch Pad

EC	FCH	Device I2C_Device(S)			
I2Ce_1 (M)	I2Cf_2 (M)	Charger	Battery		ALL/S5
I2Ce_2 (M)		APU			ALL
I2Ce_3 (M)					
	I2Cf_3 (M)	APU			S5
	I2Cf_1 (M)				S5
	I2Cf_0 (M)	DDR	WLAN/3G	Image Sensor	S0

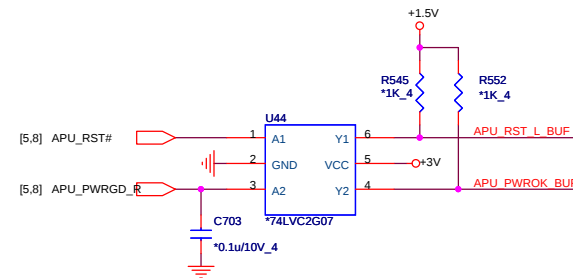
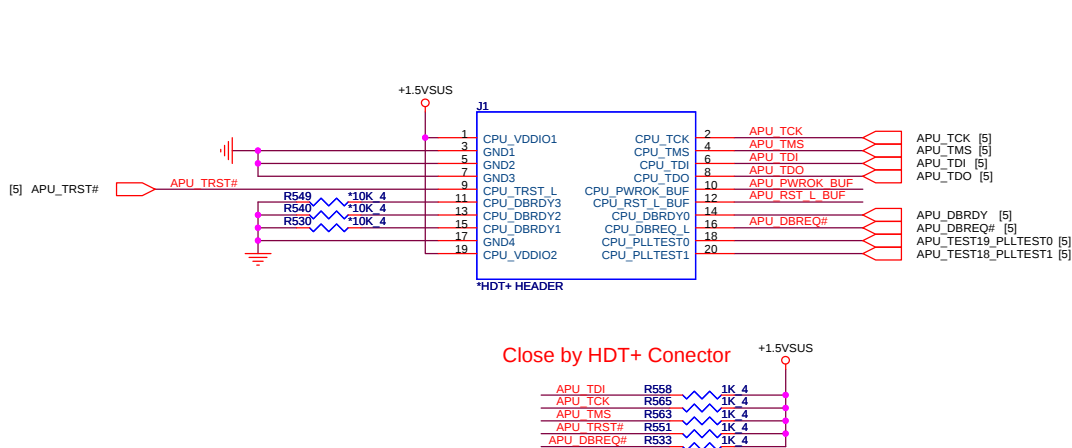
EC will Conflict with FCH.
Do not mount

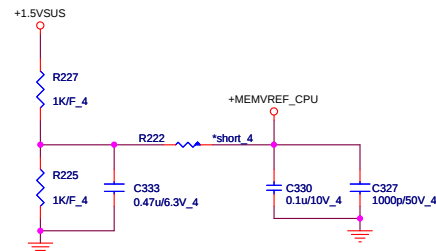
PEG X 8

PEG X 8

A10	AJ05757RT01
A8	AJ05557UT01
A6	AJ053578T01

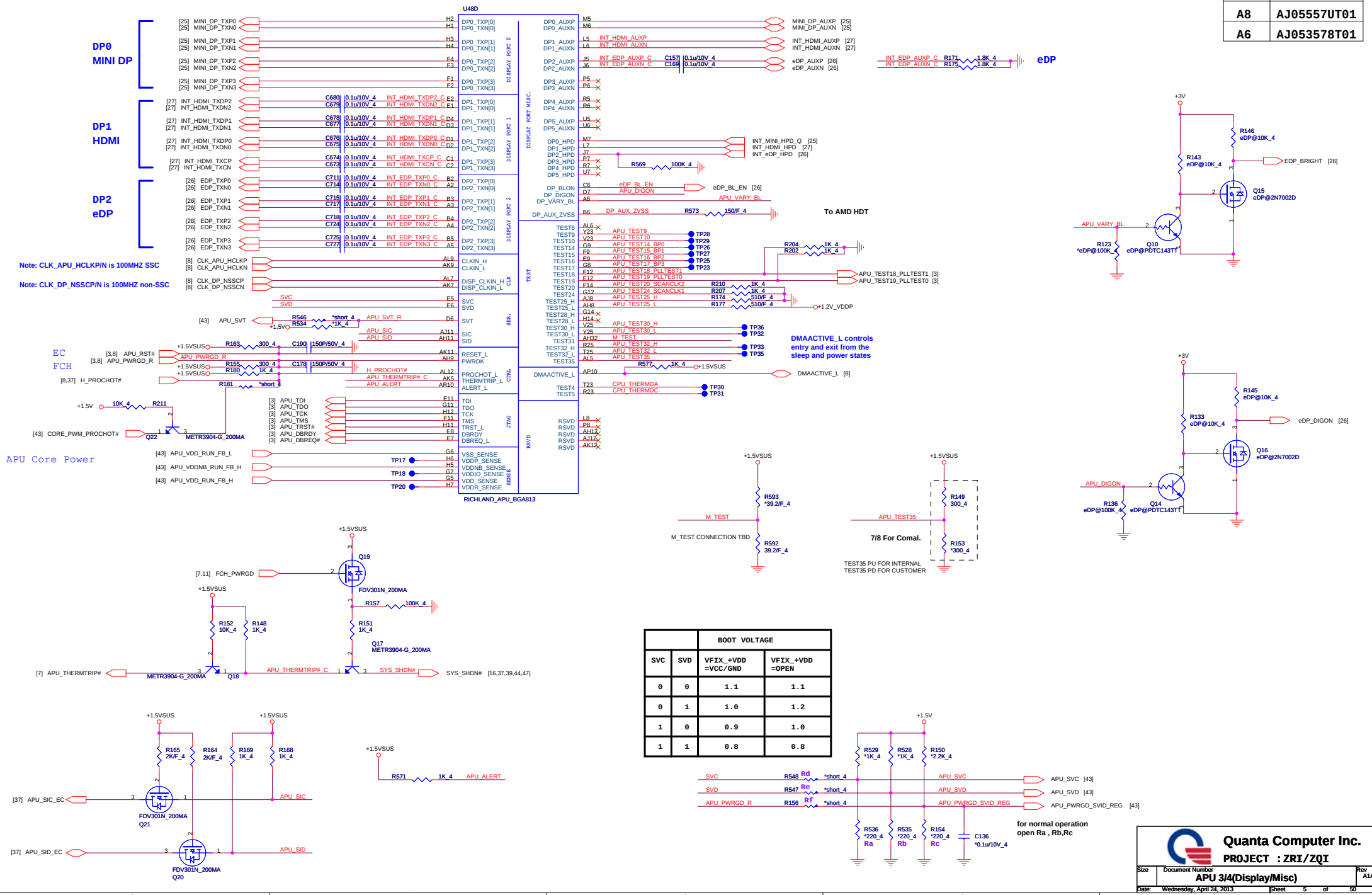
HDT+ Connector for Debug only



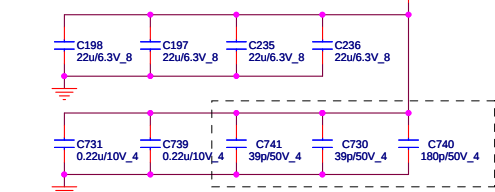
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A6	AJ053578T01

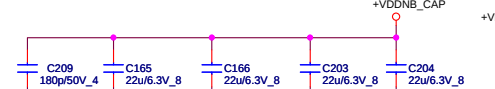
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A8	AJ05557UT01
A6	AJ053578T01



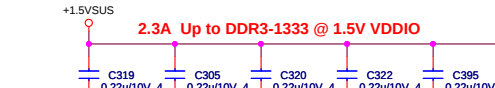
22A Maximum IDDNBSpike 33A



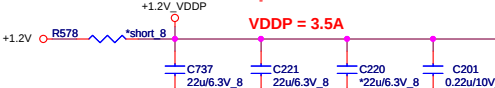
For EMI



VDDP = 3.5A



VDDA = 0.75A

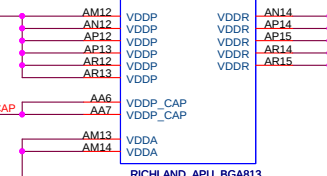
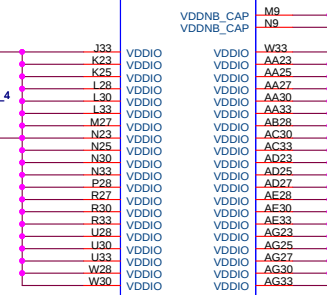
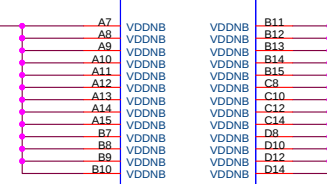
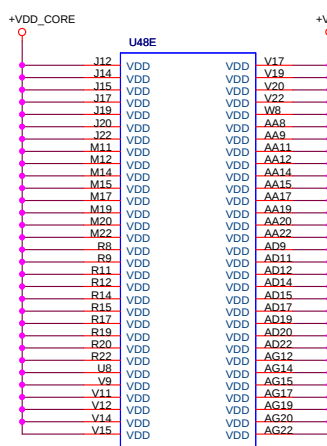


VDDA = 0.75A



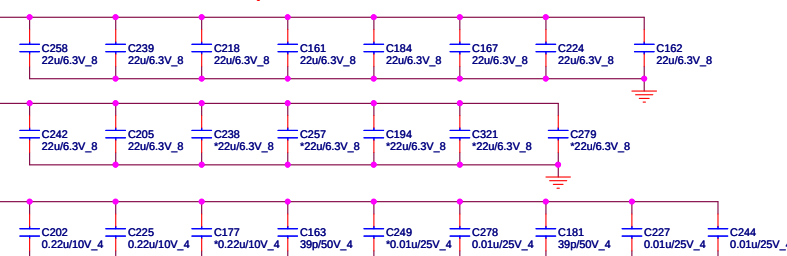
VDDA = 0.75A

A10	AJ05757RT01
A8	AJ05557UT01
A6	AJ053578T01



RICHLAND_APU_BGA813

22A Maximum IDDSpike 35A



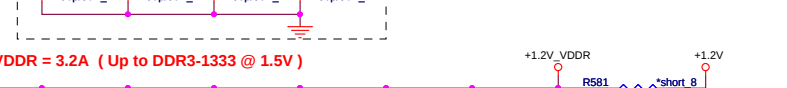
For EMI

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	1.0V ~ 1.3V
VDDNB	+VDDNB_CORE	1.05V ~ 1.325V
VDDIO	+1.5VSUS	1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



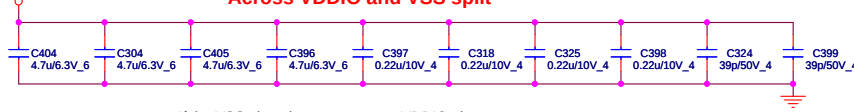
VDDR = 3.2A (Up to DDR3-1333 @ 1.5V)



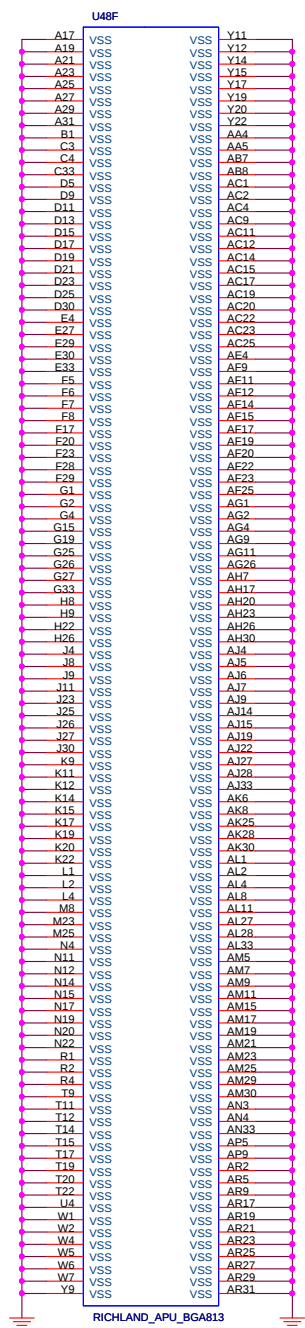
VDDR = 3.2A (Up to DDR3-1333 @ 1.5V)

DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split



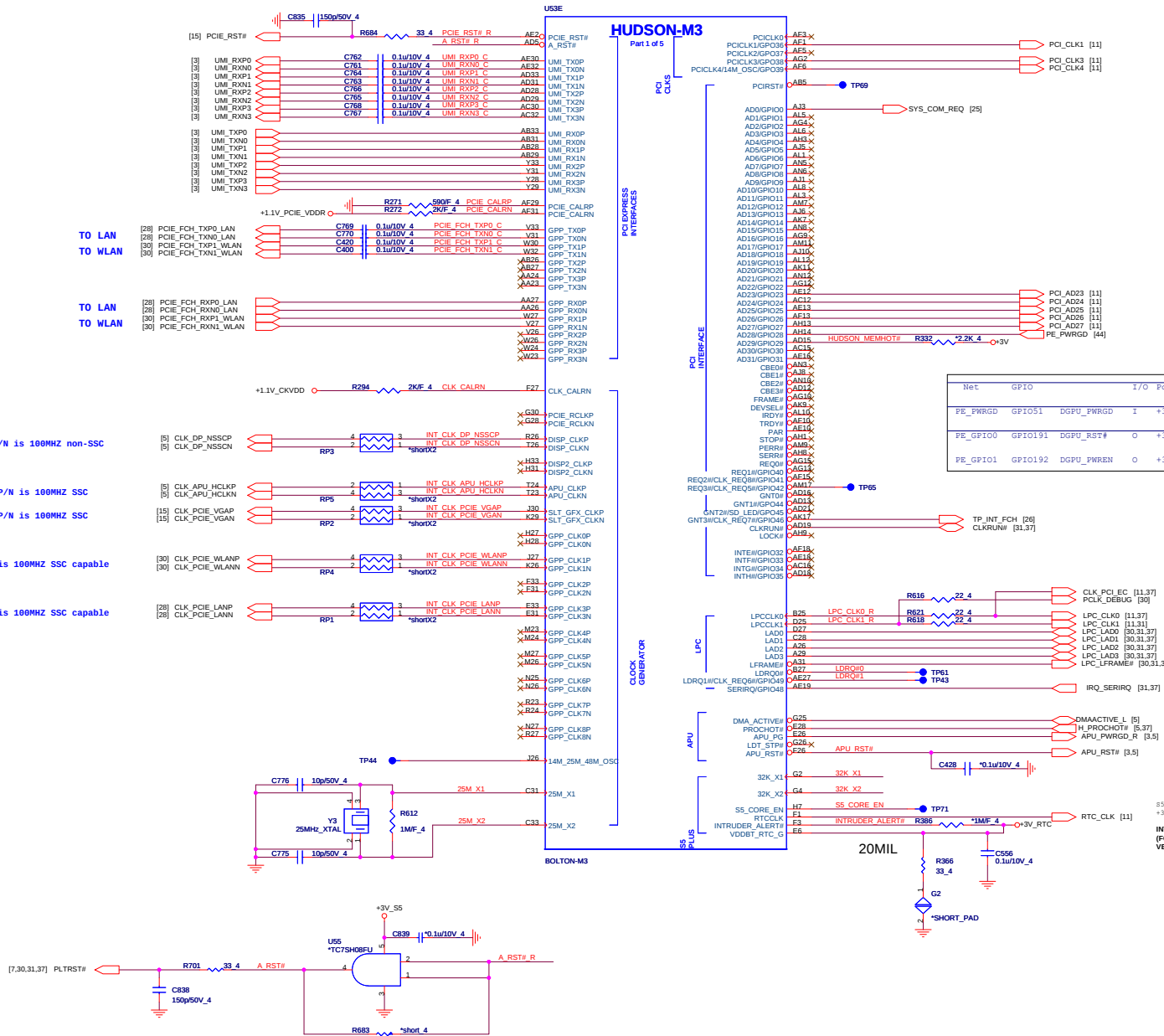
If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows



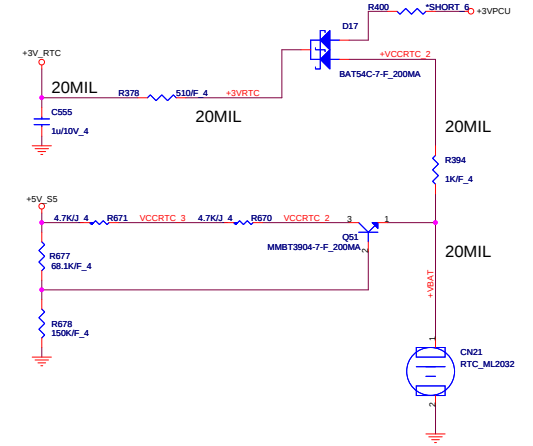
RICHLAND_APU_BGA813

Quanta Computer Inc.
PROJECT : ZRI/ZQI

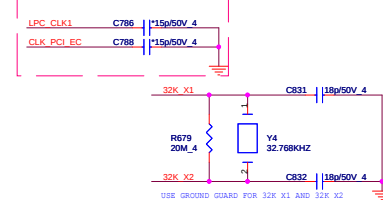
Size	Document Number	Rev
	APU 4/4(POWER/GND)	A1A
Date:	Wednesday, April 24, 2013	Sheet 6 of 50



RTC Circuitry(RTC)



For EMI

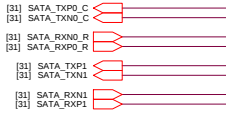


S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation

INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT)

SATA0 HDD

SATA1 SSD



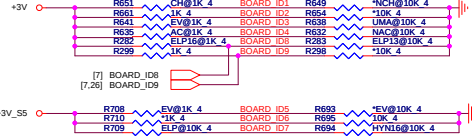
PLACE SATA CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3

+1.1V_AVDD_SATA

Integrated Clock Mode: SATA_X1, SATA_X2 leave unconnect.



Initial BIOS set internal pull down



BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID9
USB Charge	H	L				
No USB Charge						
Reserved		H				
VGA SKU			H	L		
UMA SKU						
AC					H	L
No AC						
VRAM 2G					H	L
VRAM 4G						
Non Touch Panel						H
Touch Panel						L

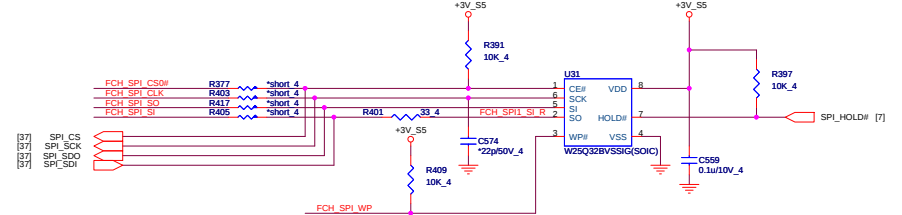
<= PD by cable

OnBorad RAM SETTING

ID6	ID7	ID8	
0	0	1	HYNIX DDR3L 1600 4GB H5TC46G3AFR-PBA
0	1	0	ELPIDA DDR3L 1333 4GB EDJ4216EB8G-DJ-F
0	1	1	ELPIDA DDR3L 1600 4GB EDJ4216EF8G-GNL-F
1	0	0	Disable OnBorad RAM

U538

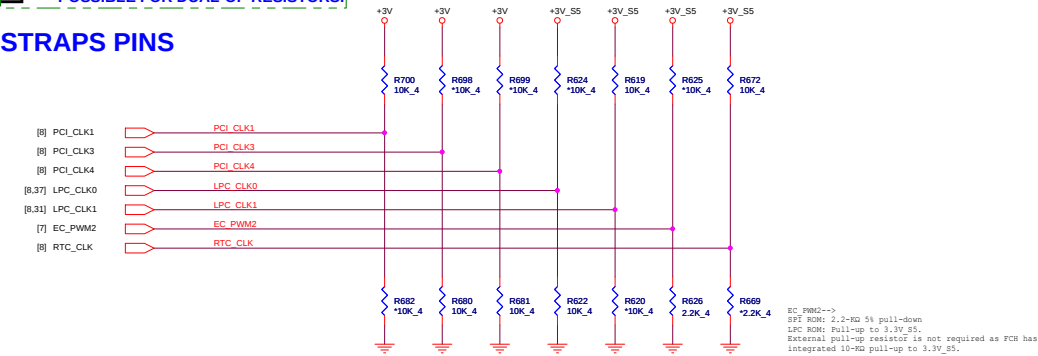
HUDSON-M3





OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

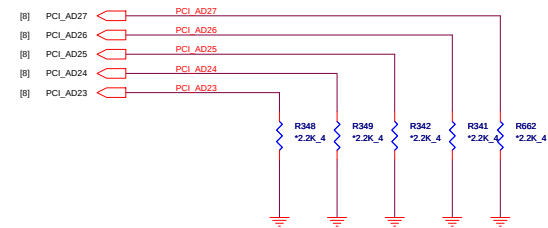


REQUIRED STRAPS

	-----	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

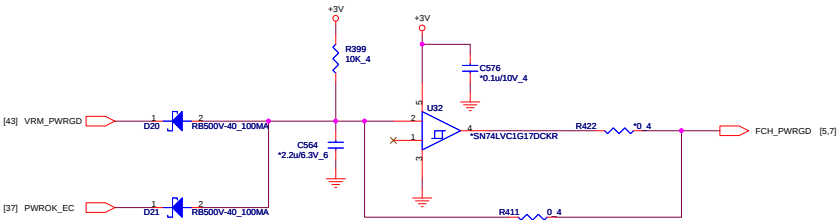
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

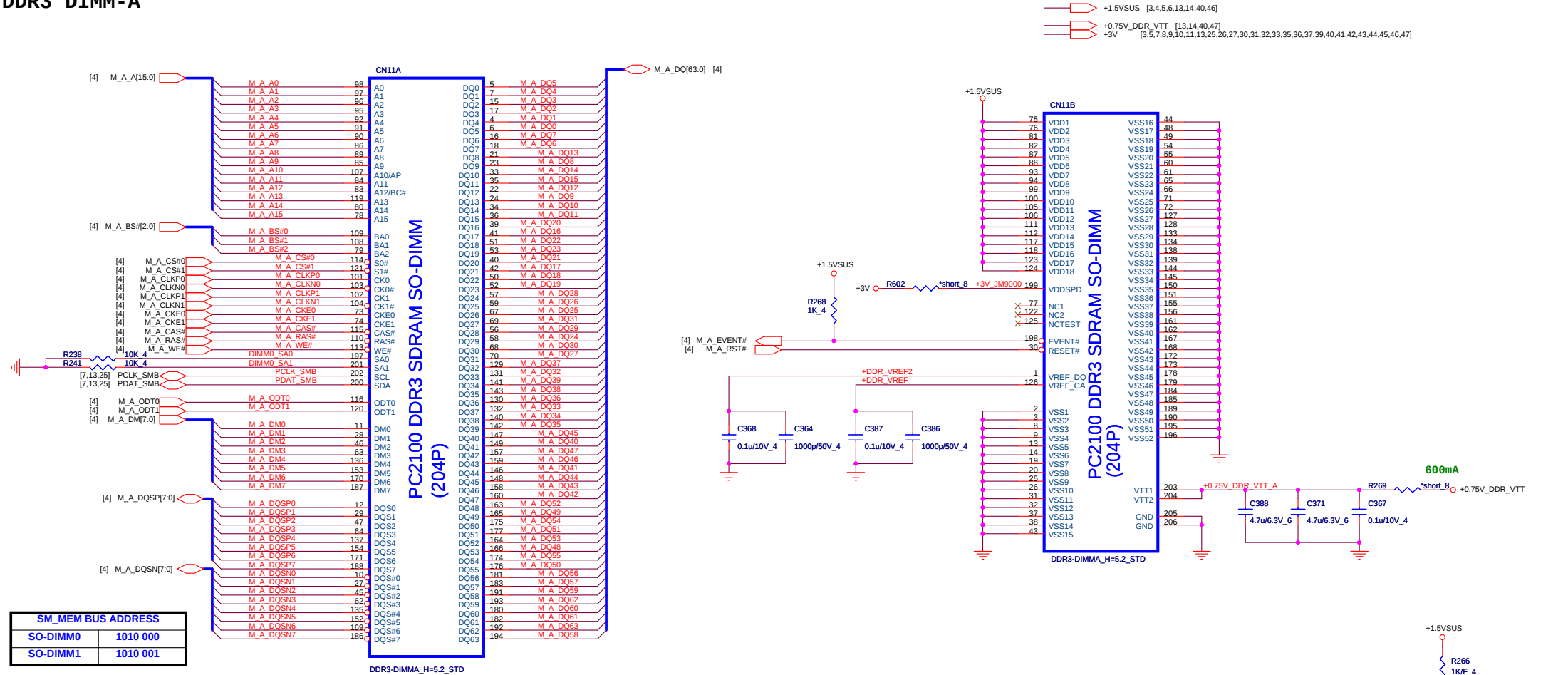


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

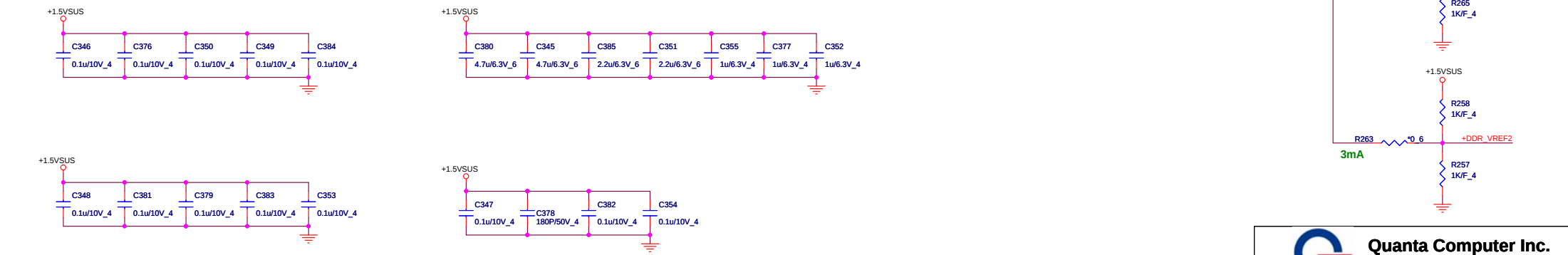
FCH PWRGD CKT



DDR3 DIMM-A

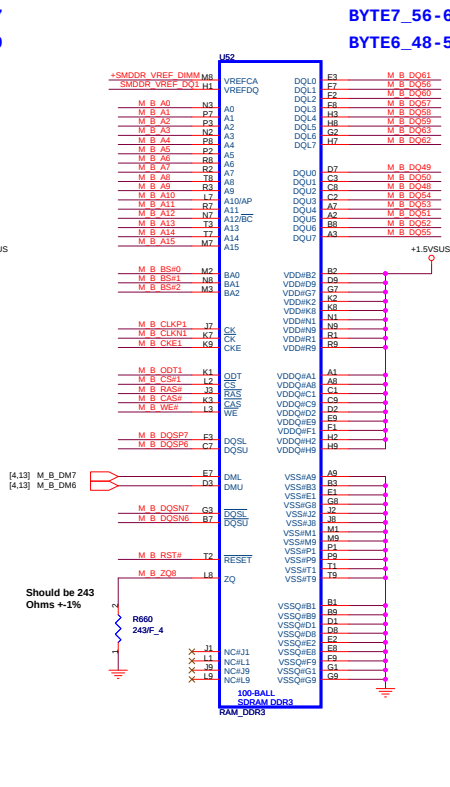
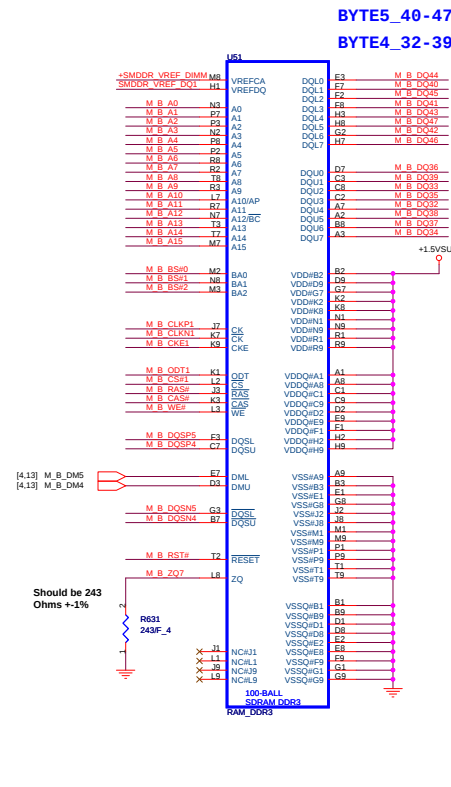
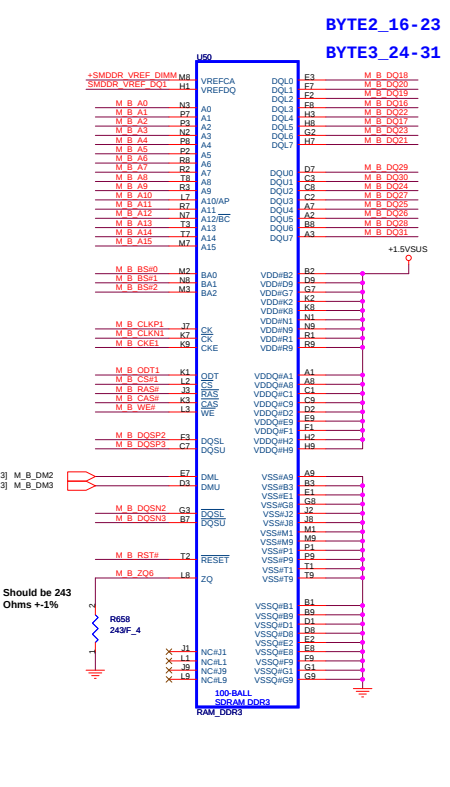
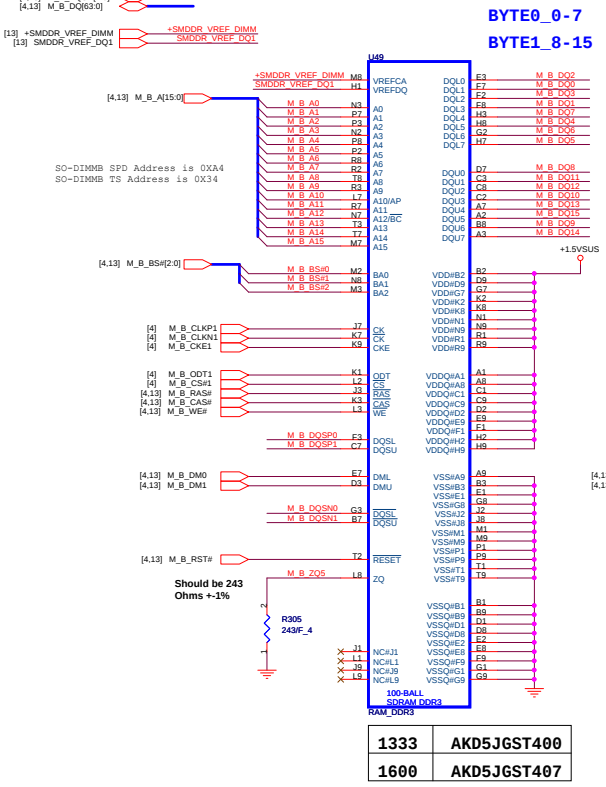
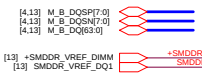


Place these Caps near So-Dimm A

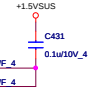
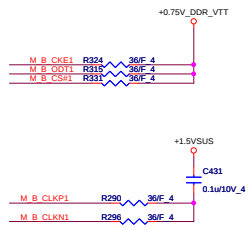
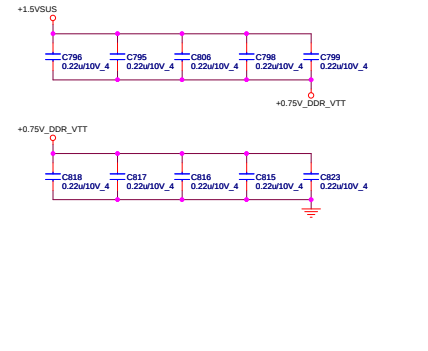
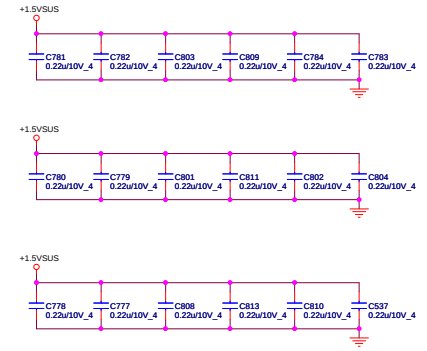


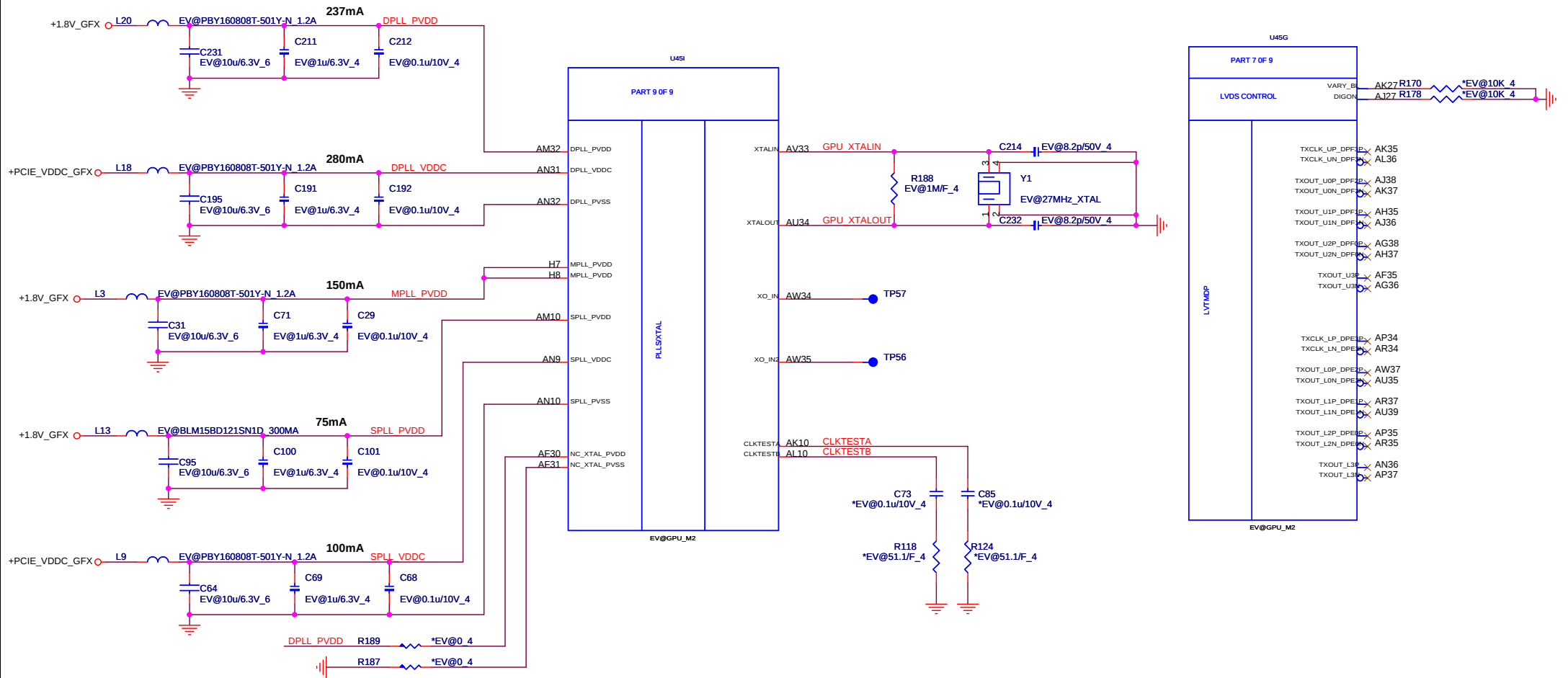
 Quanta Computer Inc. PROJECT : ZRI/ZQI	
Size	Document Number
DDR3 SO-DIMM A	
Date: Wednesday, April 24, 2013	Sheet 12 of 50

<DDR>



Place these Caps near Memory Down

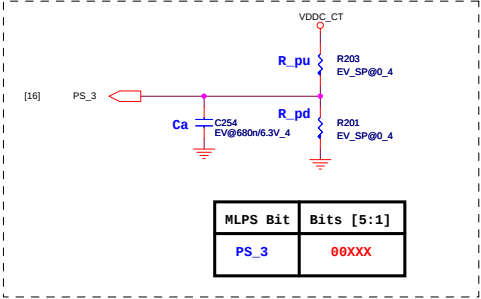




Vendor	Vendor P/N	STN B/S P/N	Size	MLPS
Hynix	H5TQ2G63DFR-11C (128M*16)	AKD5MGWTW17 * 8	2GB	000
	H5TC2G63FFR-11C (128M*16)	AKD5MZDTW05 * 8	2GB	001
Micron	MT41K256M16HA-107G (256M*16)	AKD5PGSTL05 * 8	4GB	011

Mars USE

SP : Mars DDR3 Memory TYPE Set



MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	0 000
8.45K	2K	F 001
4.53K	2K	B 010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	1M	110
4.75K	NC	111

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
1M	CS51002FB11

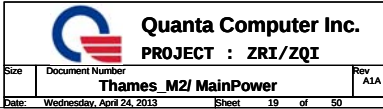
Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

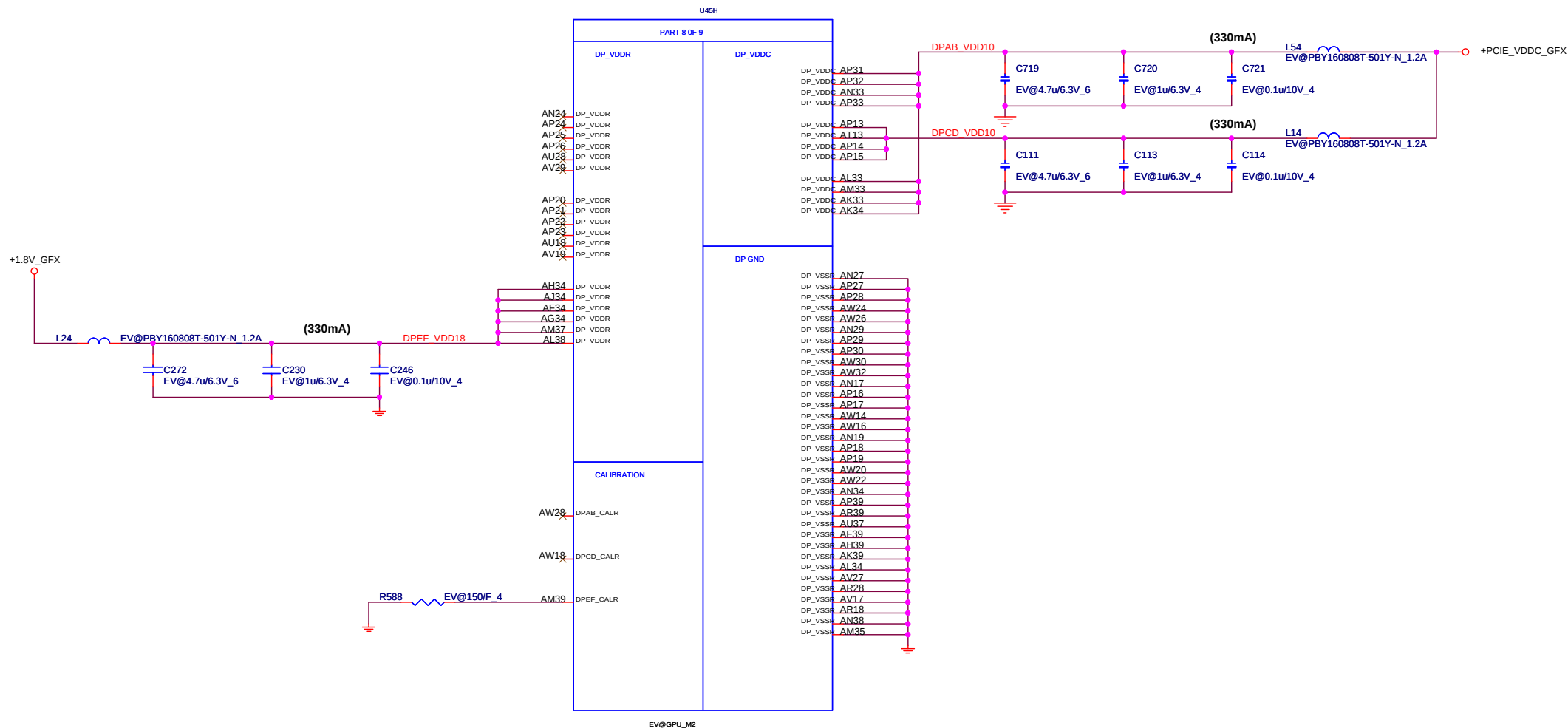
CONFIGURATION STRAPS – SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWR5_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 110 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

System Memory Aperture size

GPIO9 BIOSROM		GPIO11 ROMIDCFG0	GPIO12 ROMIDCFG1	GPIO13 ROMIDCFG2
0	128M	0	0	0
0	256M	1	0	0
0	64M	0	1	0
0	32M	1	1	0

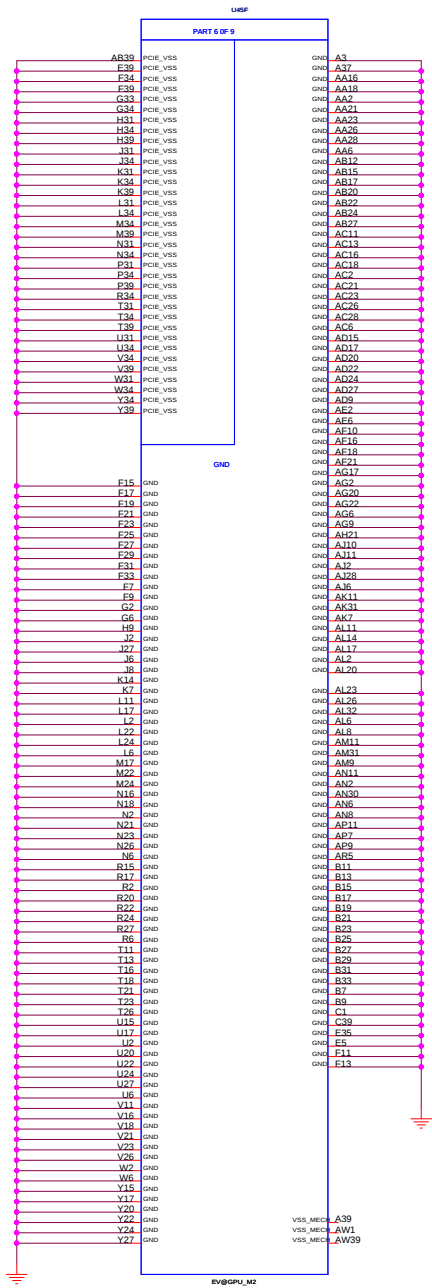


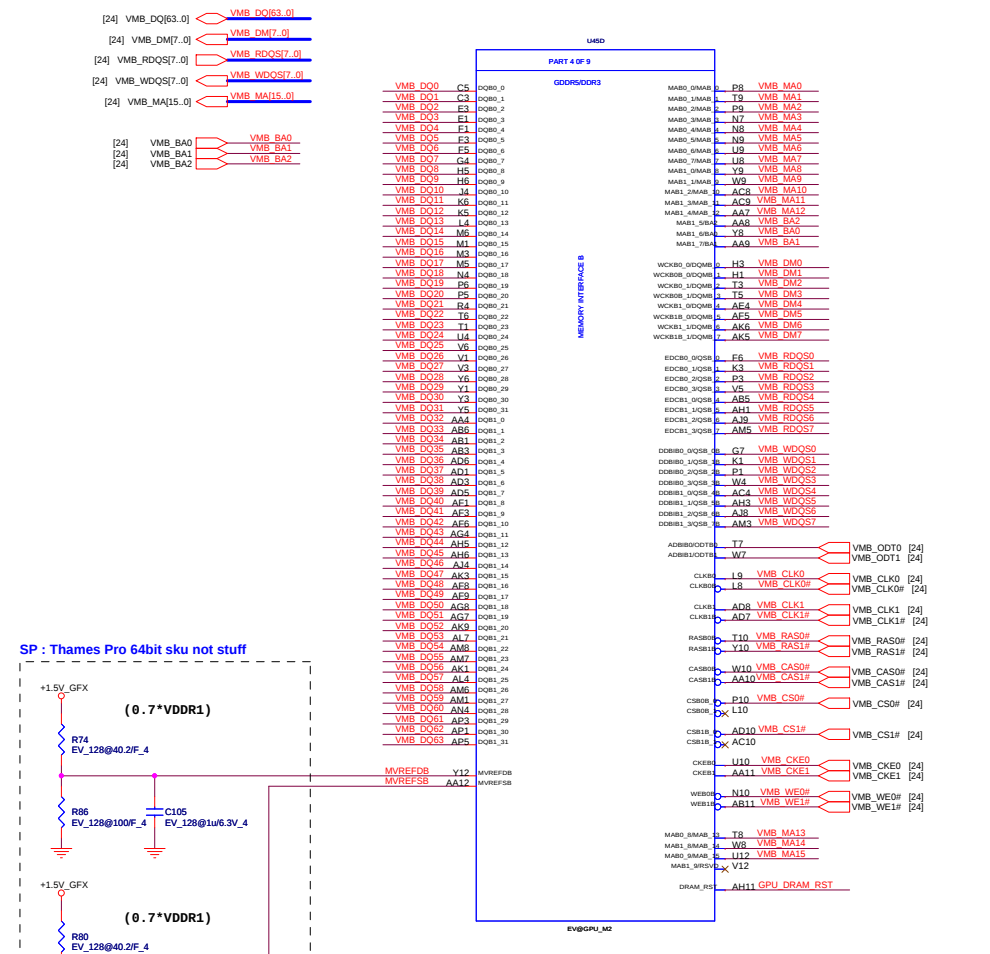
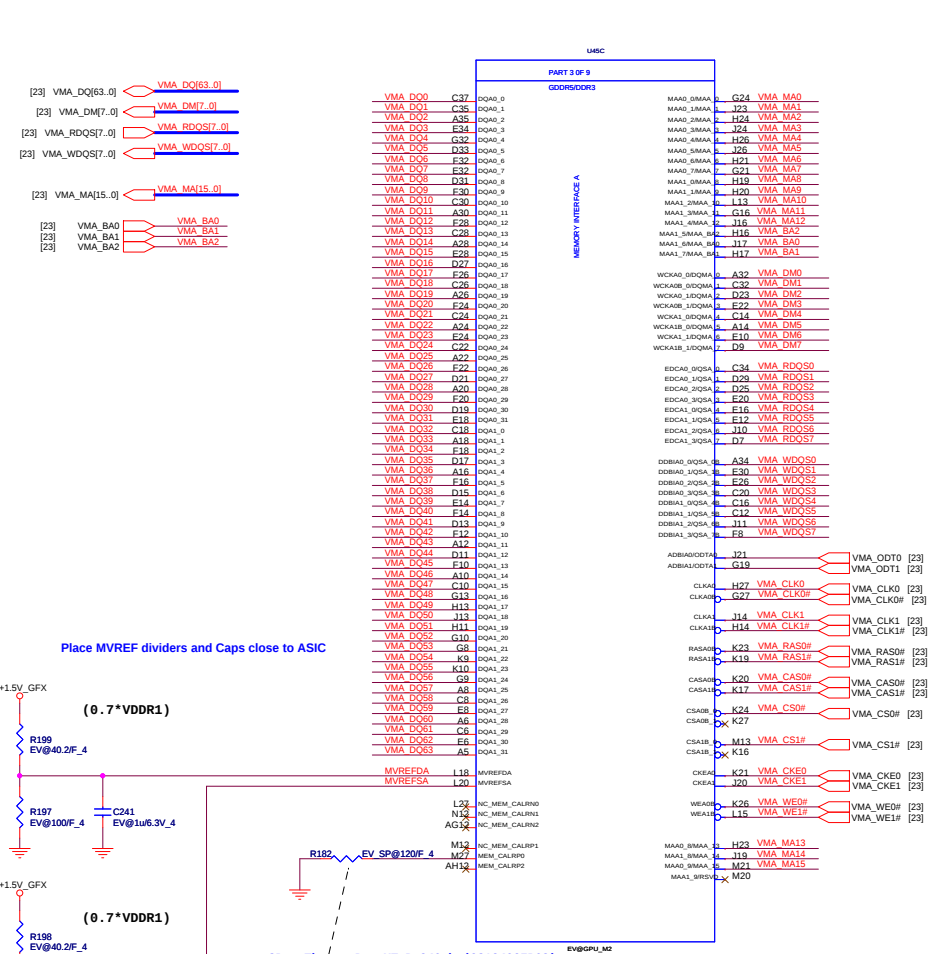




Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	Thames_M2/ DP_Powers	A1A
Date:	Wednesday, April 24, 2013	Sheet 20 of 50





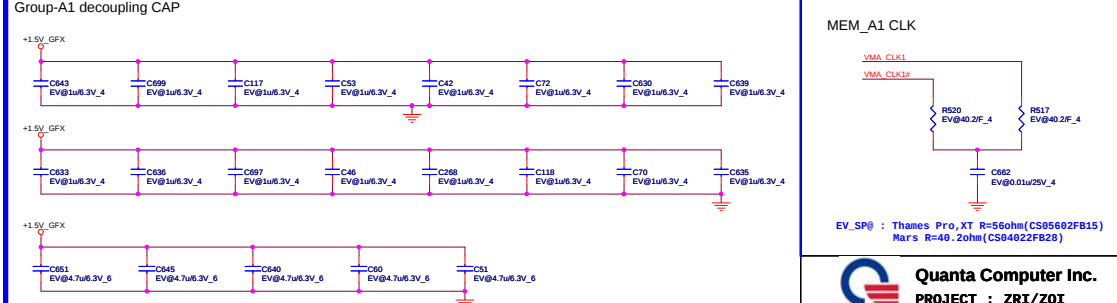
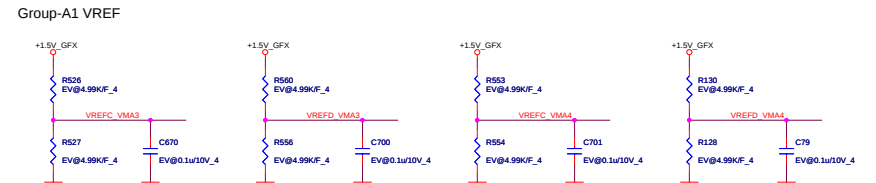
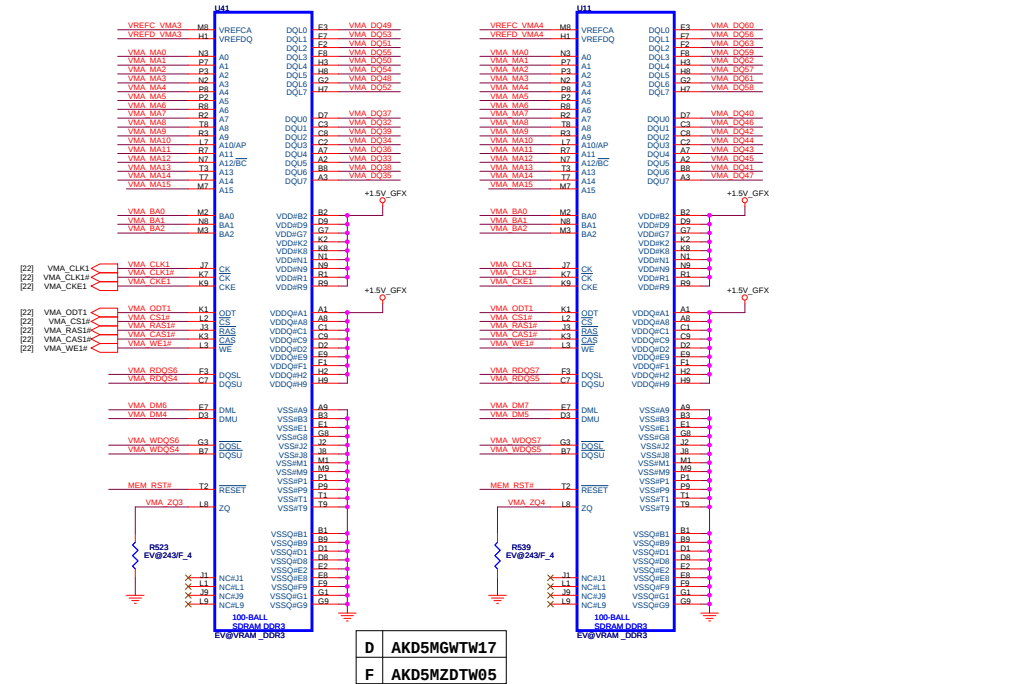
[22] VMA_DQ[63..0] VMA_DQ[63..0]

[22] VMA_DM[7..0] VMA_DM[7..0]

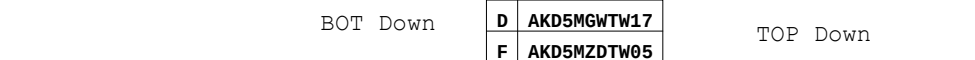
[22] VMA_RDQS[7..0] VMA_RDQS[7..0] QSA[7..0]

[22] VMA_WDQS[7..0] VMA_WDQS[7..0] QSA#[7..0]

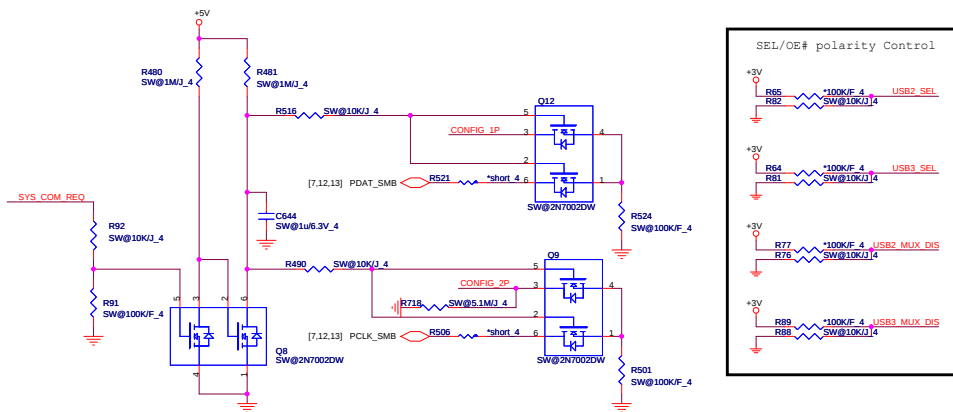
[22] VMA_MA[15..0] VMA_MA[15..0]



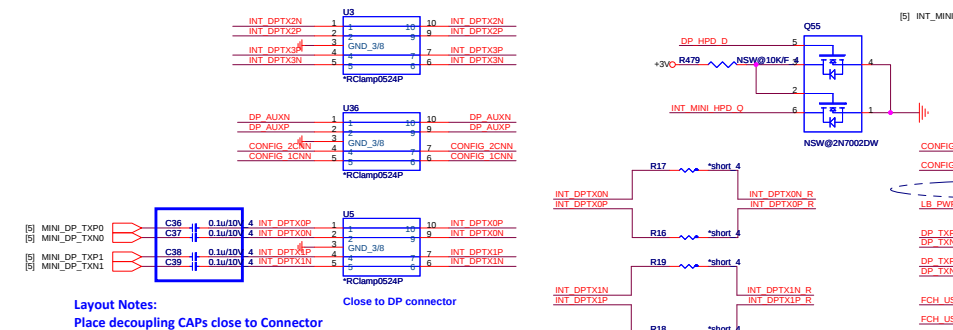
[22] VMB_DQ[63..0] VMB_DQ[63..0]



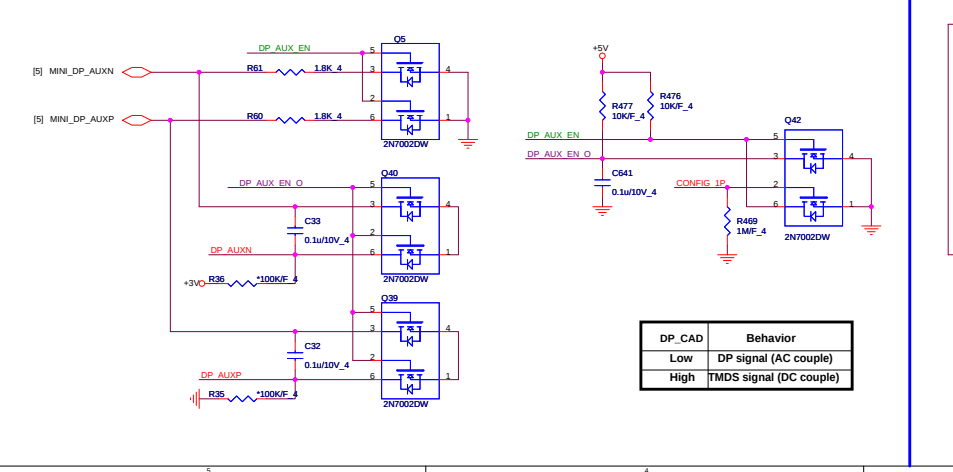
mini DP ML (DPP)



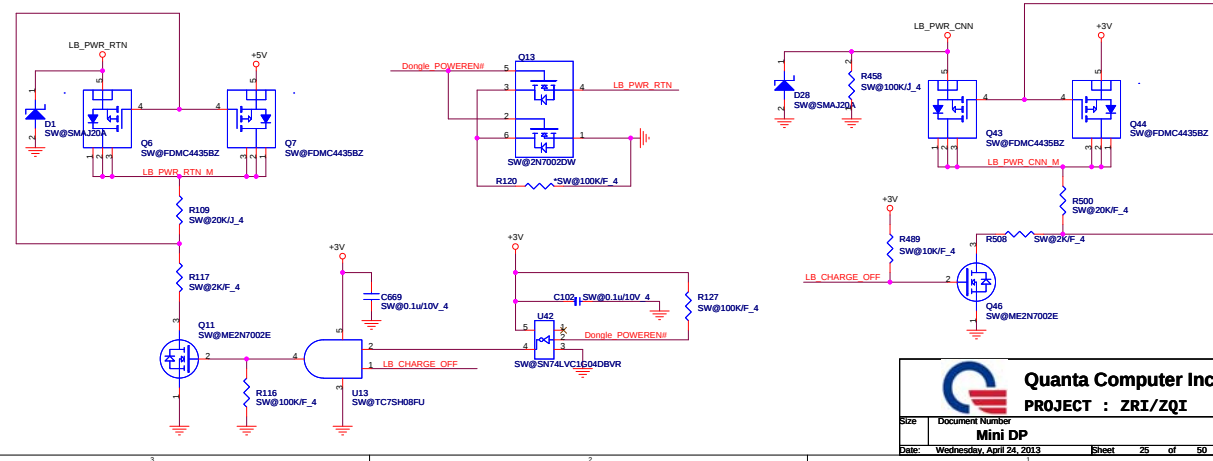
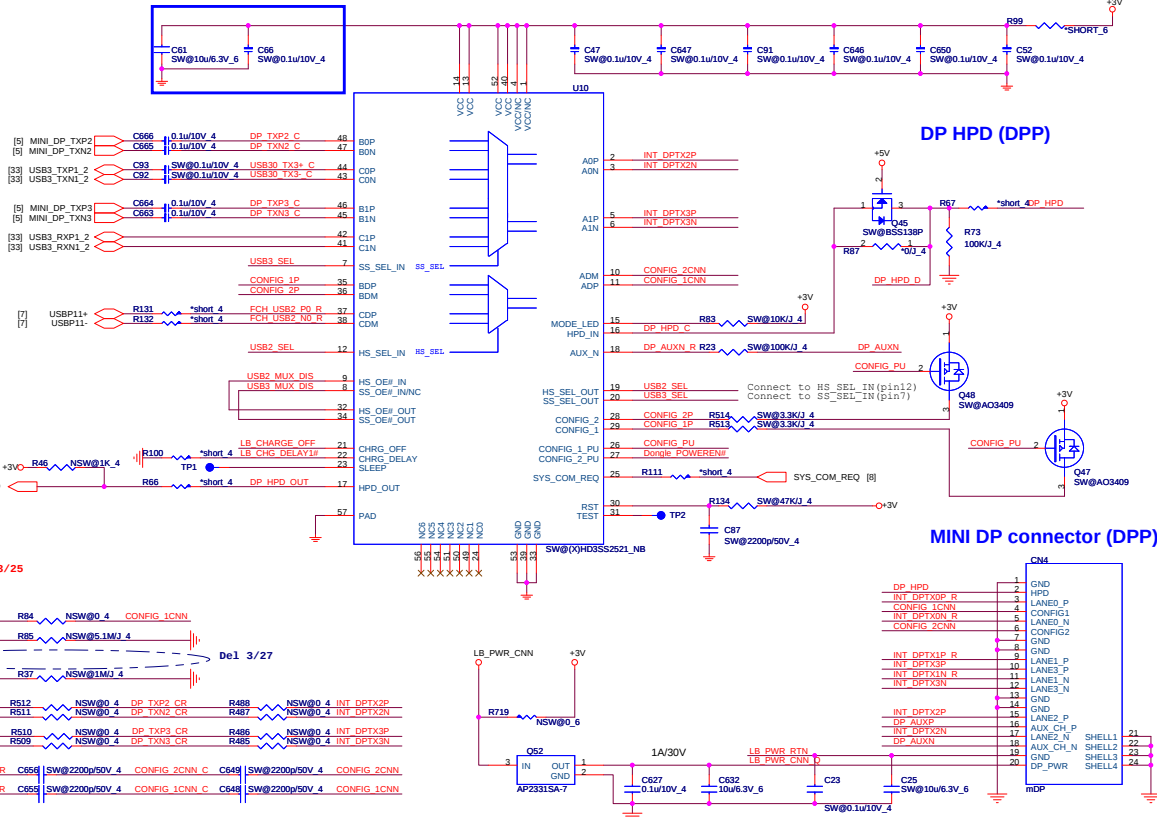
ESD Protect (EMC)



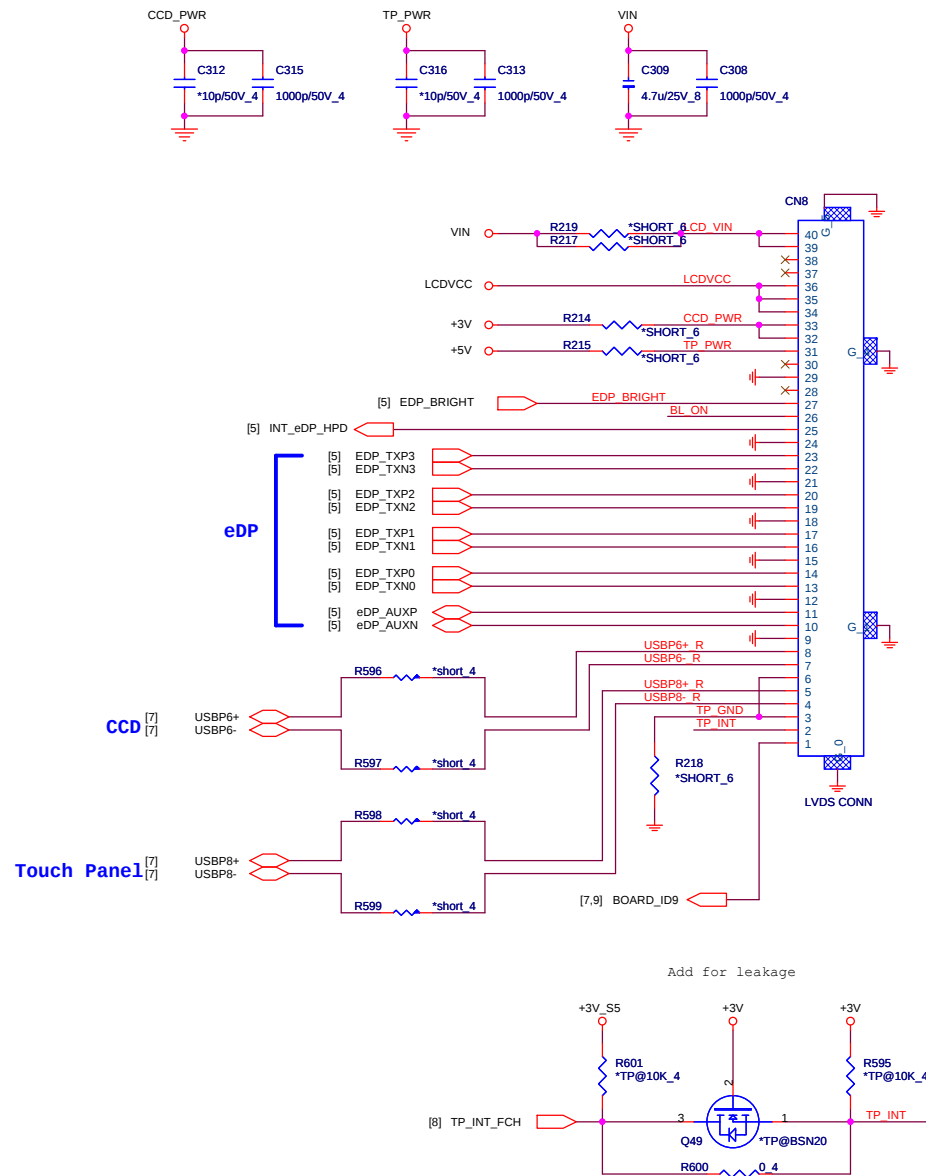
mDP AUX (DPP)



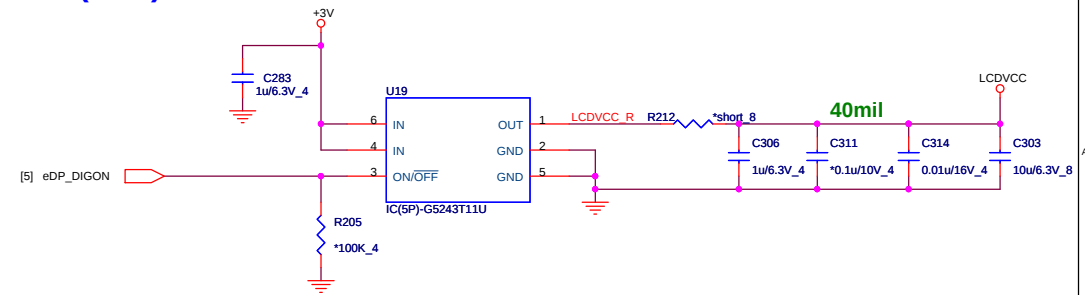
Layout Notes:
Place near Pin13 and Pin14



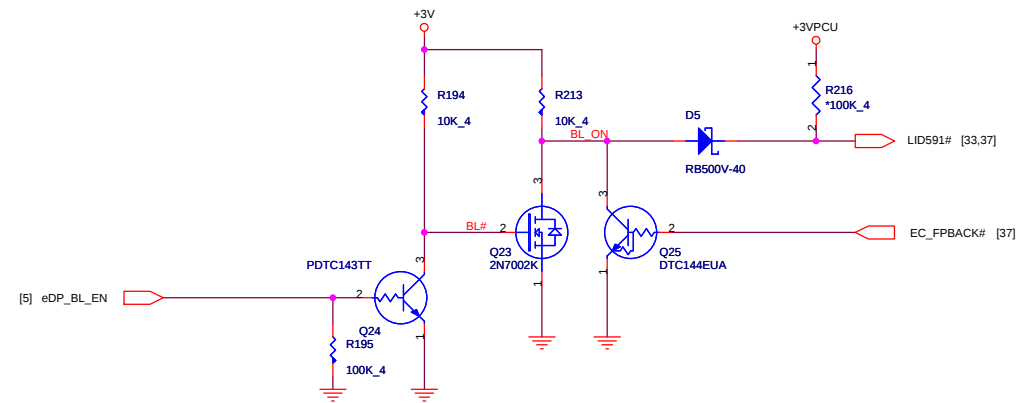
eDP(LDS)



LCD PW(LDS)

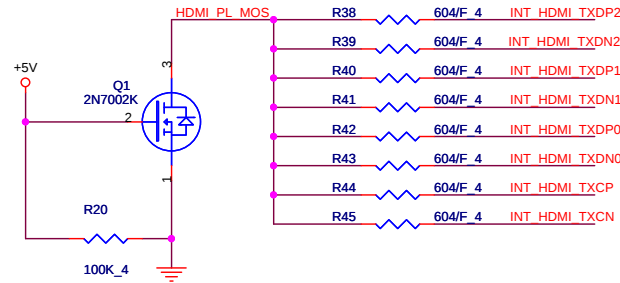
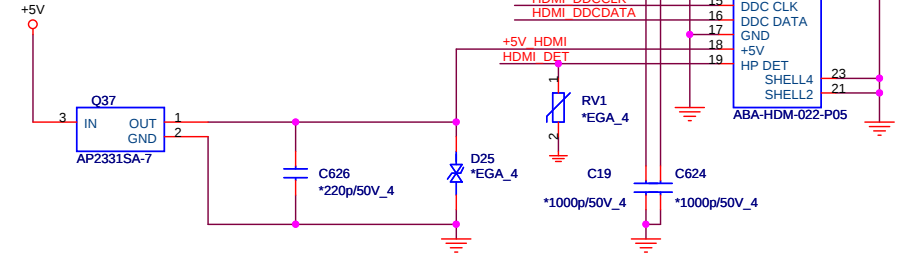
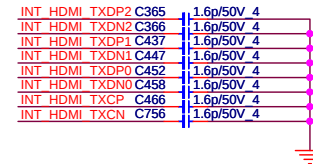
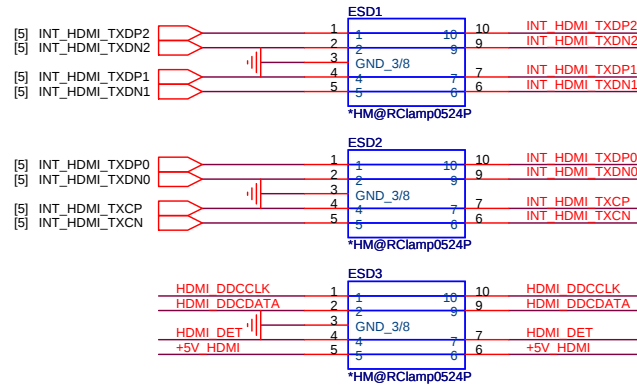


Backlight Control(LDS)



HDMI

ESD

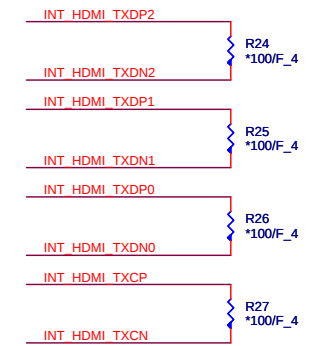


HDMI SDVO I2C Control

HDMI HPD SENSE

EMI reserve for HDMI(EMC)

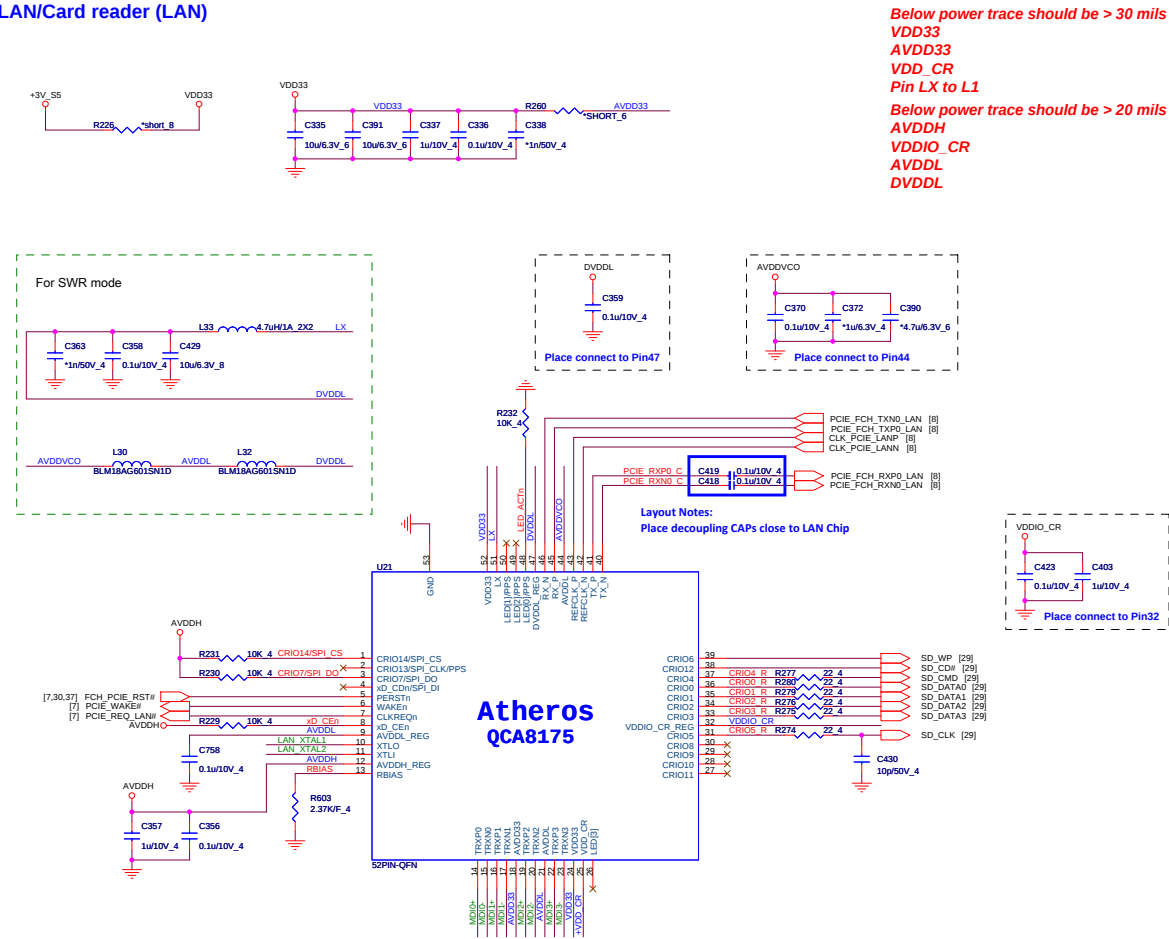
Close connector



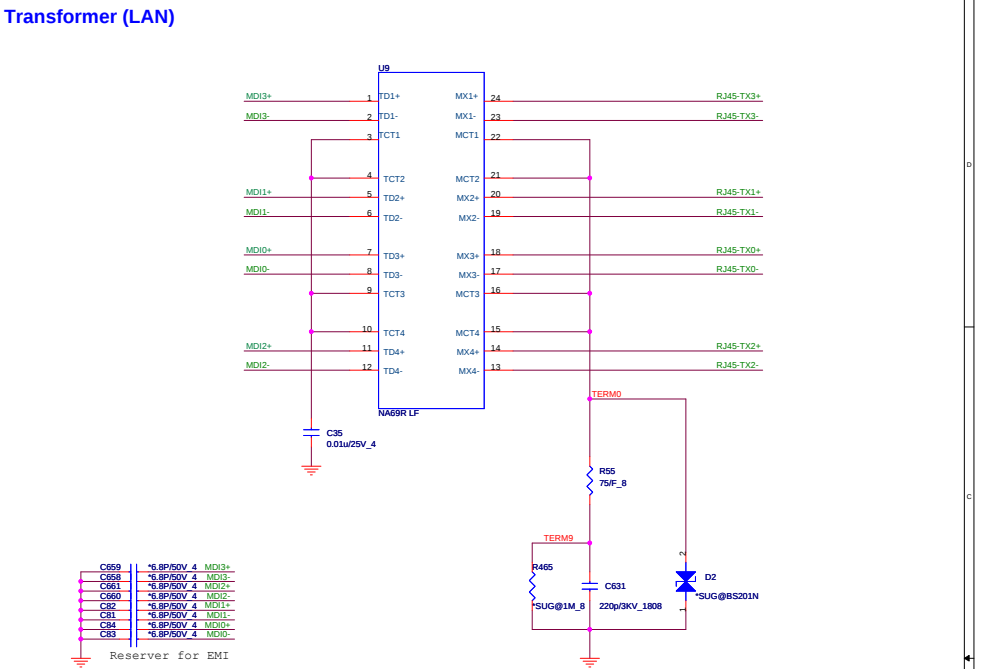
Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	HDMI	A1A
Date:	Wednesday, April 24, 2013	Sheet 27 of 50

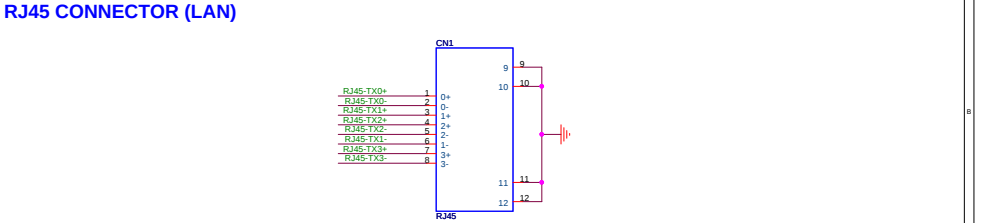
LAN/Card reader (LAN)



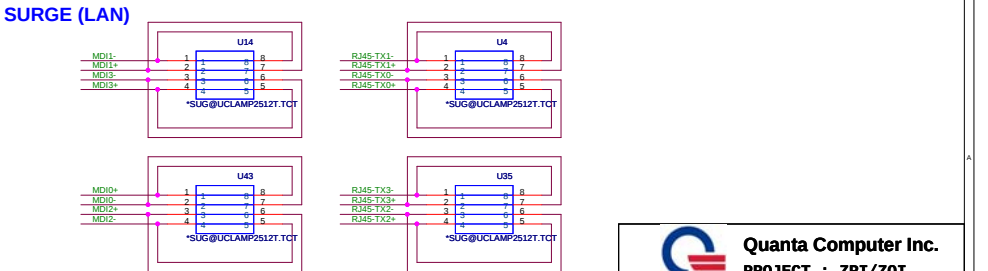
Transformer (LAN)



RJ45 CONNECTOR (LAN)

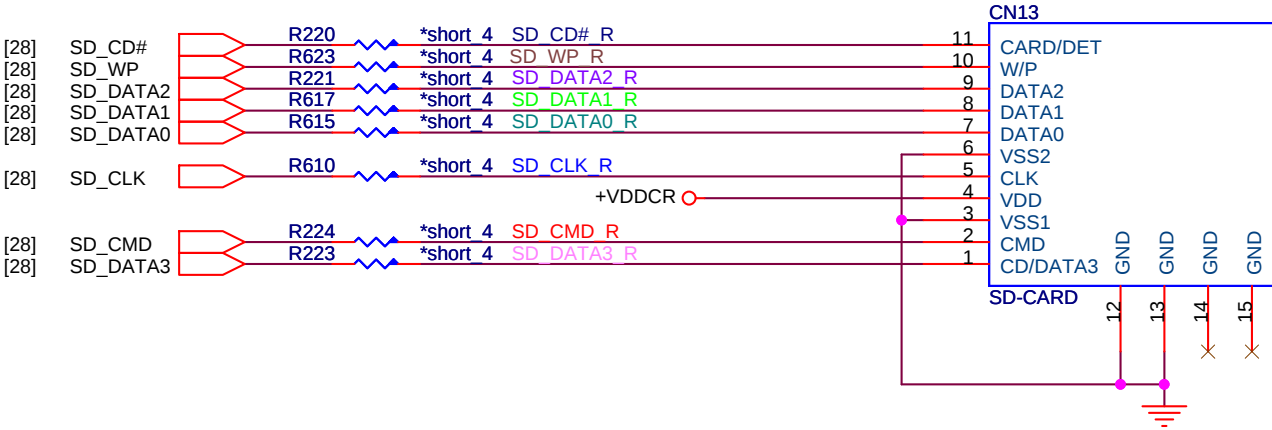


SURGE (LAN)

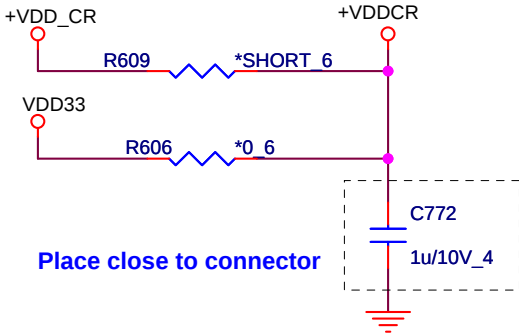
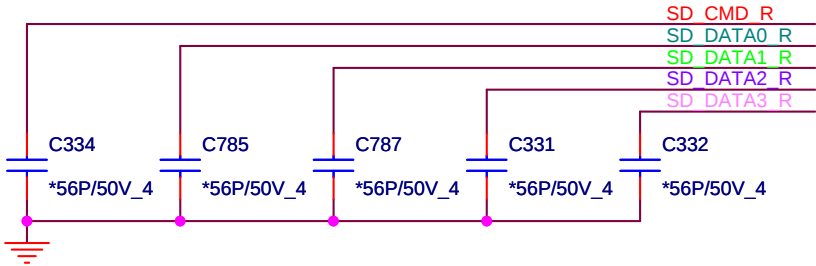


CARD READER CONNECTOR (MMC)

SD/MMC CARD READER (MMC)



EMI

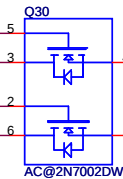


Quanta Computer Inc.
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+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

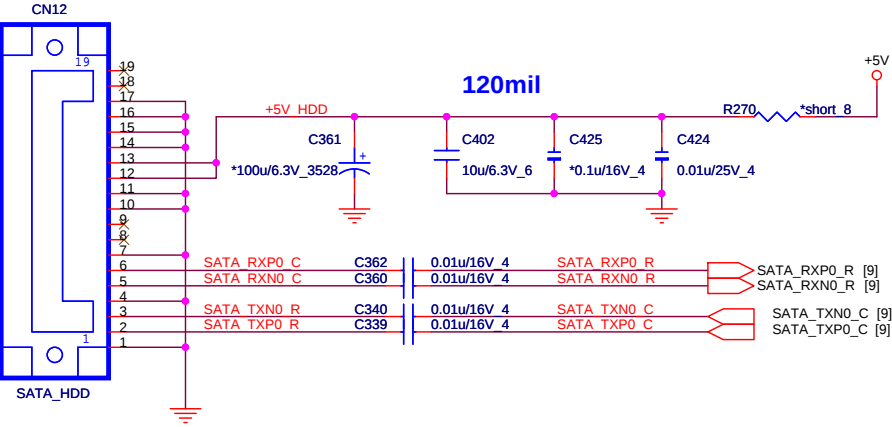


EC: +3VPCU

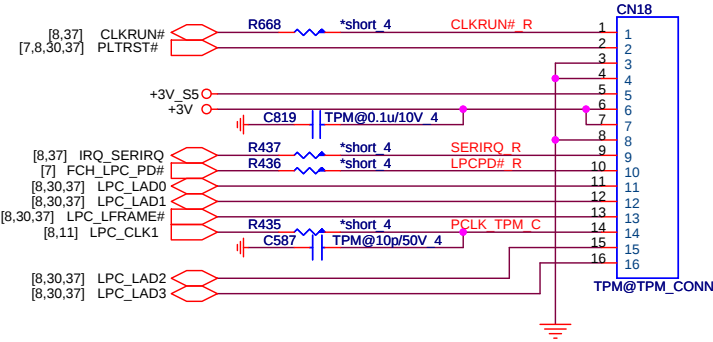


Size	Document Number	Rev
	MINI PCIE(WLAN/BT)	A1A
Date:	Wednesday, April 24, 2013	Sheet 30 of 50

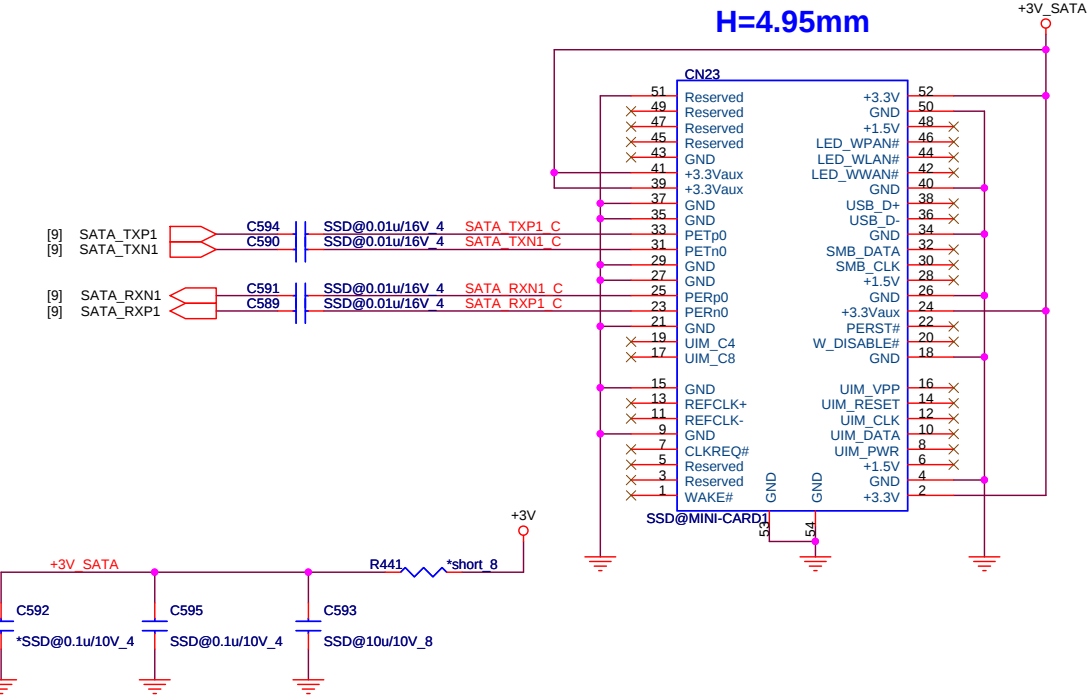
SATA HDD



TPM



MINI-CARD SSD

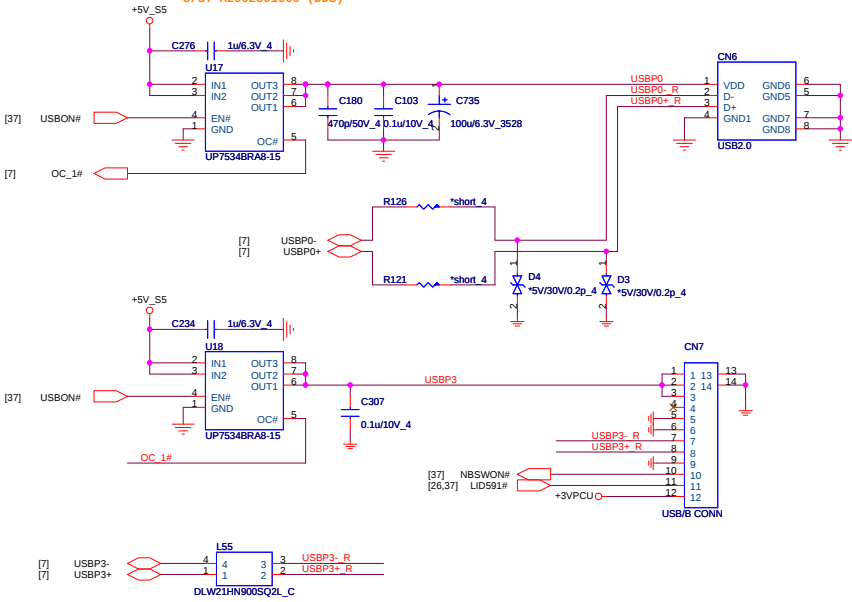


SATA Re-driver

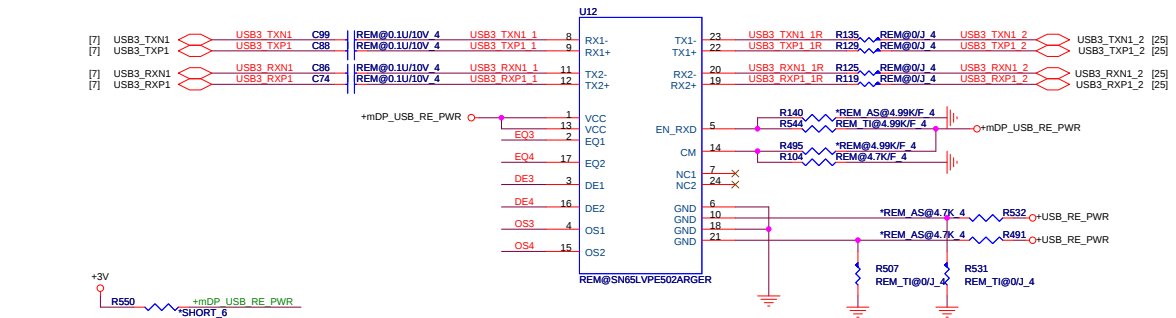
rating = 1000mA @ 128G

INT & EXT USB2.0

Active Low:
1st: AL007534009 (Promate)
2nd: AL000547005 (GMT)
3rd: AL002501000 (DDS)

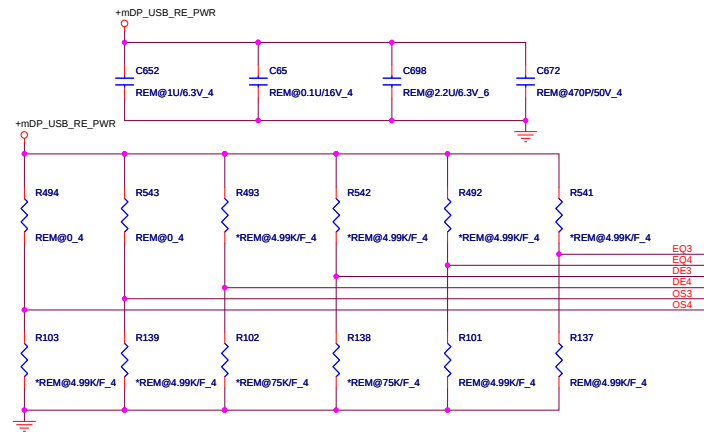


mDP USB3.0 re-driver IC

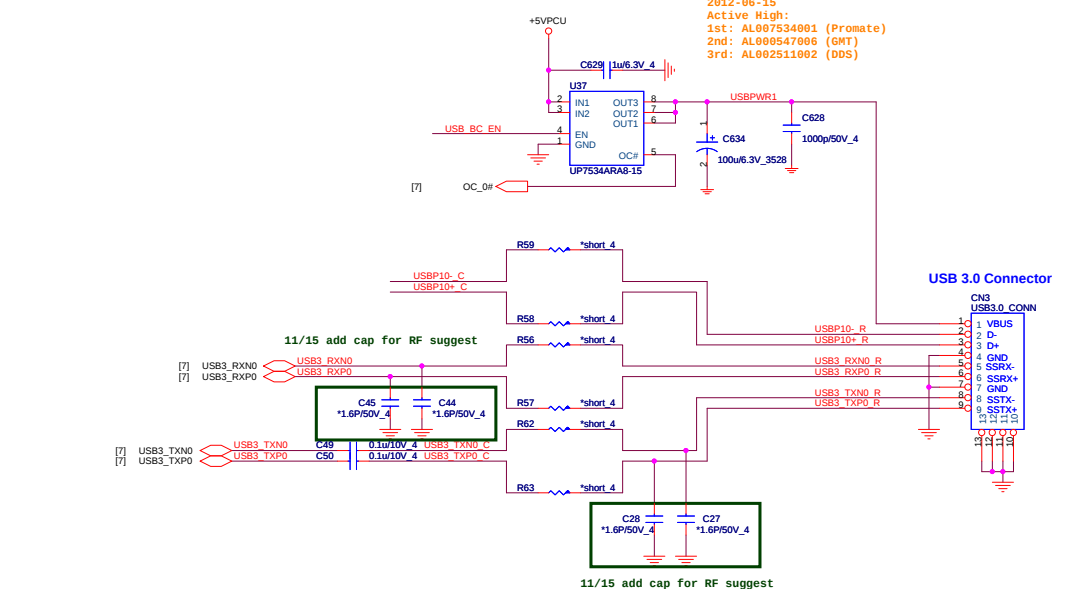


USB3_RXP1 R515 NREM@0/0_4 USB3_RXP1_2
USB3_RXN1 R510 NREM@0/0_4 USB3_RXN1_2
USB3_TXN1 R525 NREM@0/0_4 USB3_TXN1_2
USB3_TXP1 R522 NREM@0/0_4 USB3_TXP1_2

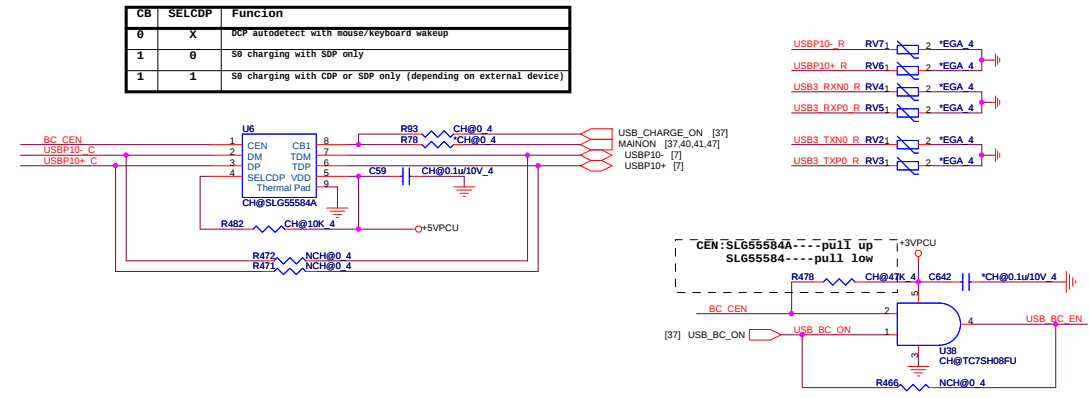
Control pins setting			
EN_RXD	Device function	CM	Device function
1(default)	Normal Operation	0(default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode



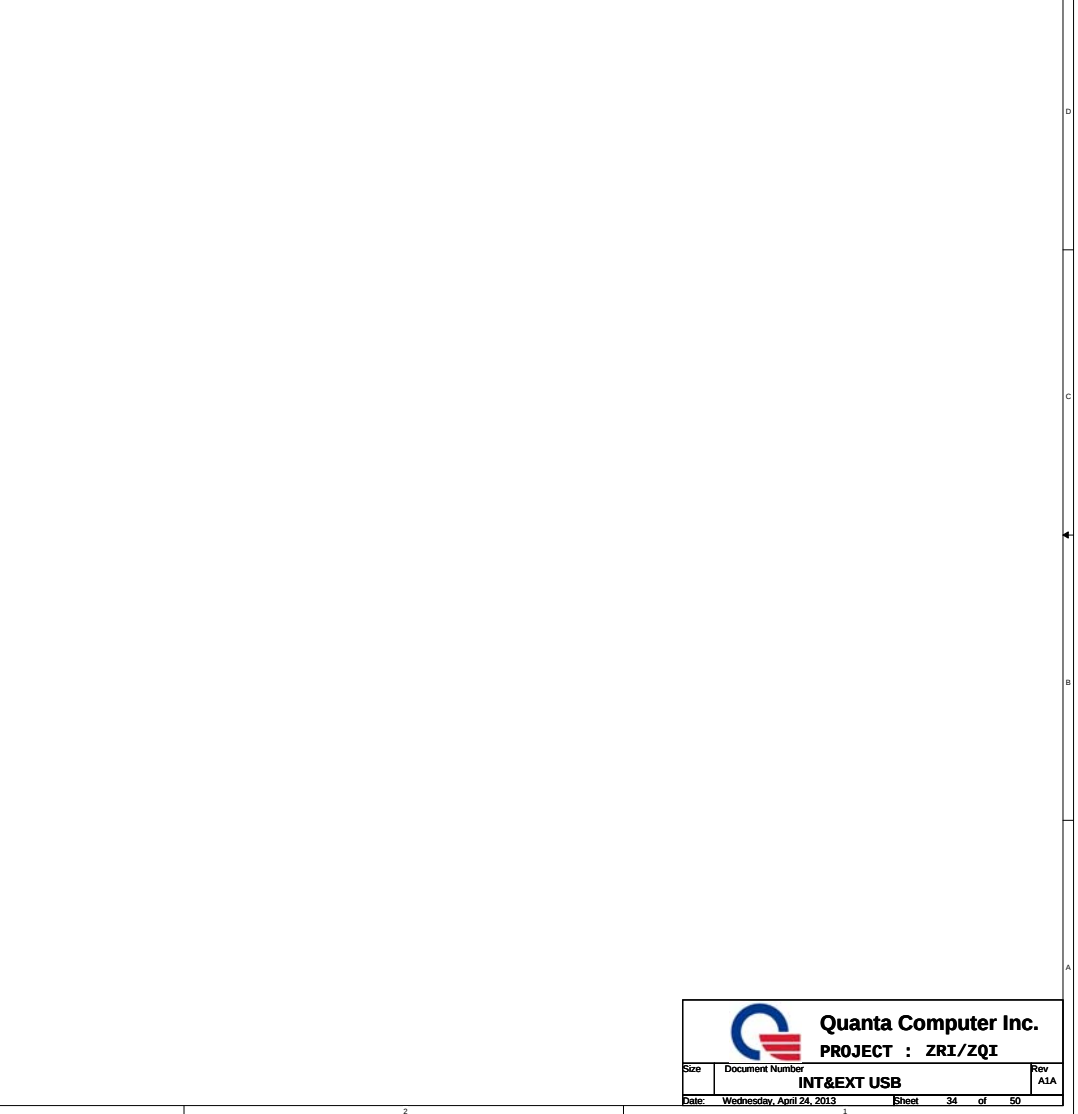
USB3.0/2.0



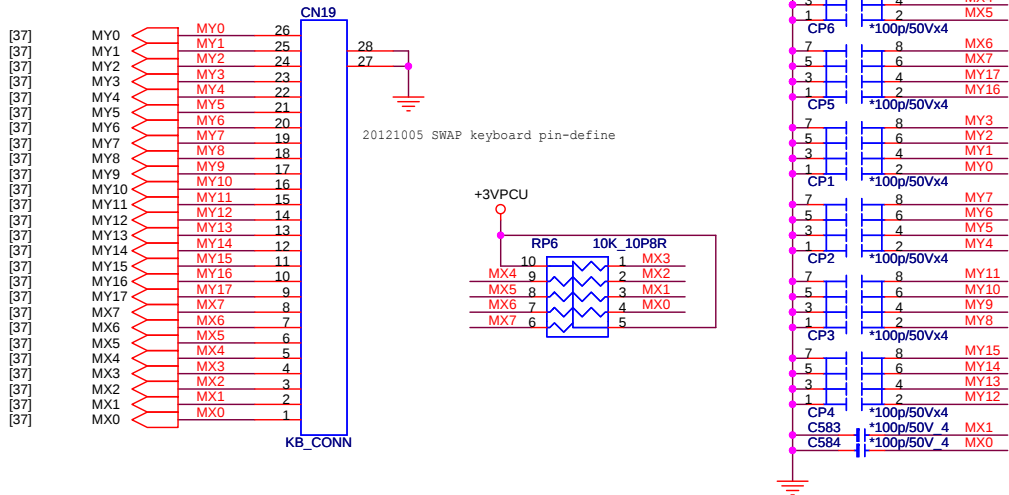
USB Charger to 3.0



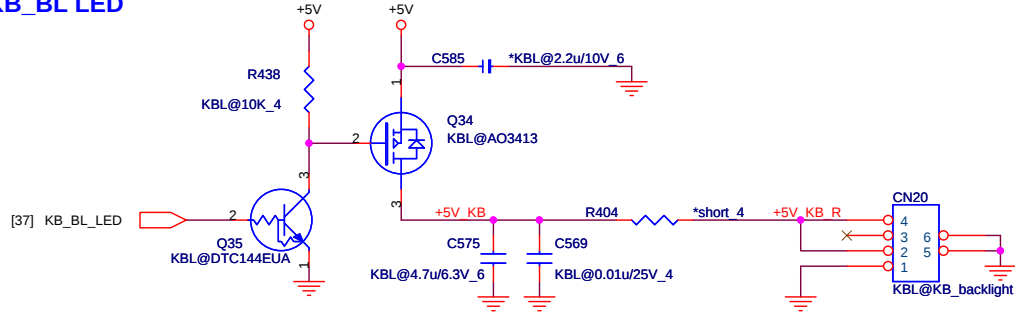
USB3.0 re-driver IC



K/B(KBC)

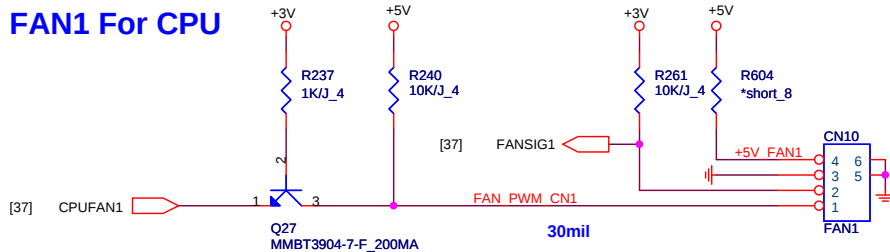


KB_BL LED

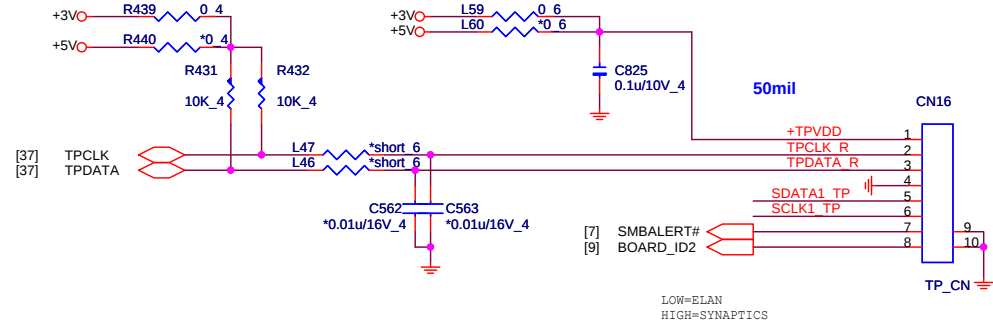
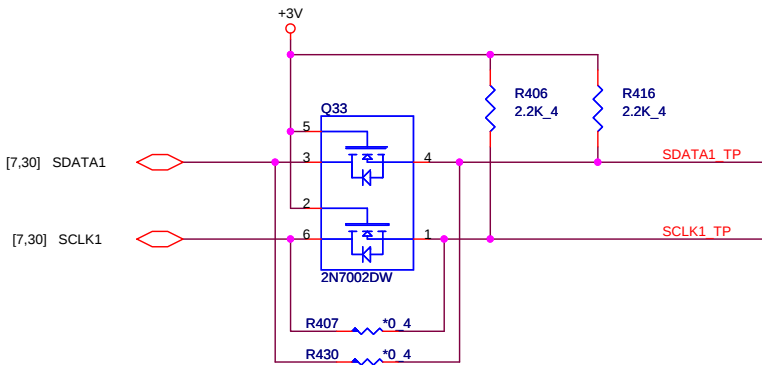


CPU FAN(THM)

FAN1 For CPU

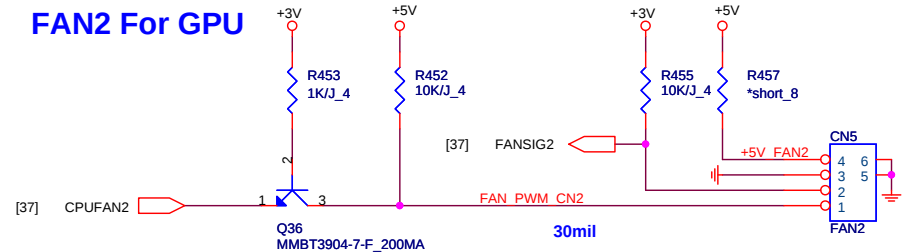


TOUCHPAD BOARD CONN(TPD)



If need to support XT(25) GPU, need check with thermal

FAN2 For GPU



Quanta Computer Inc.

PROJECT : ZRI/ZQI

Size	Document Number
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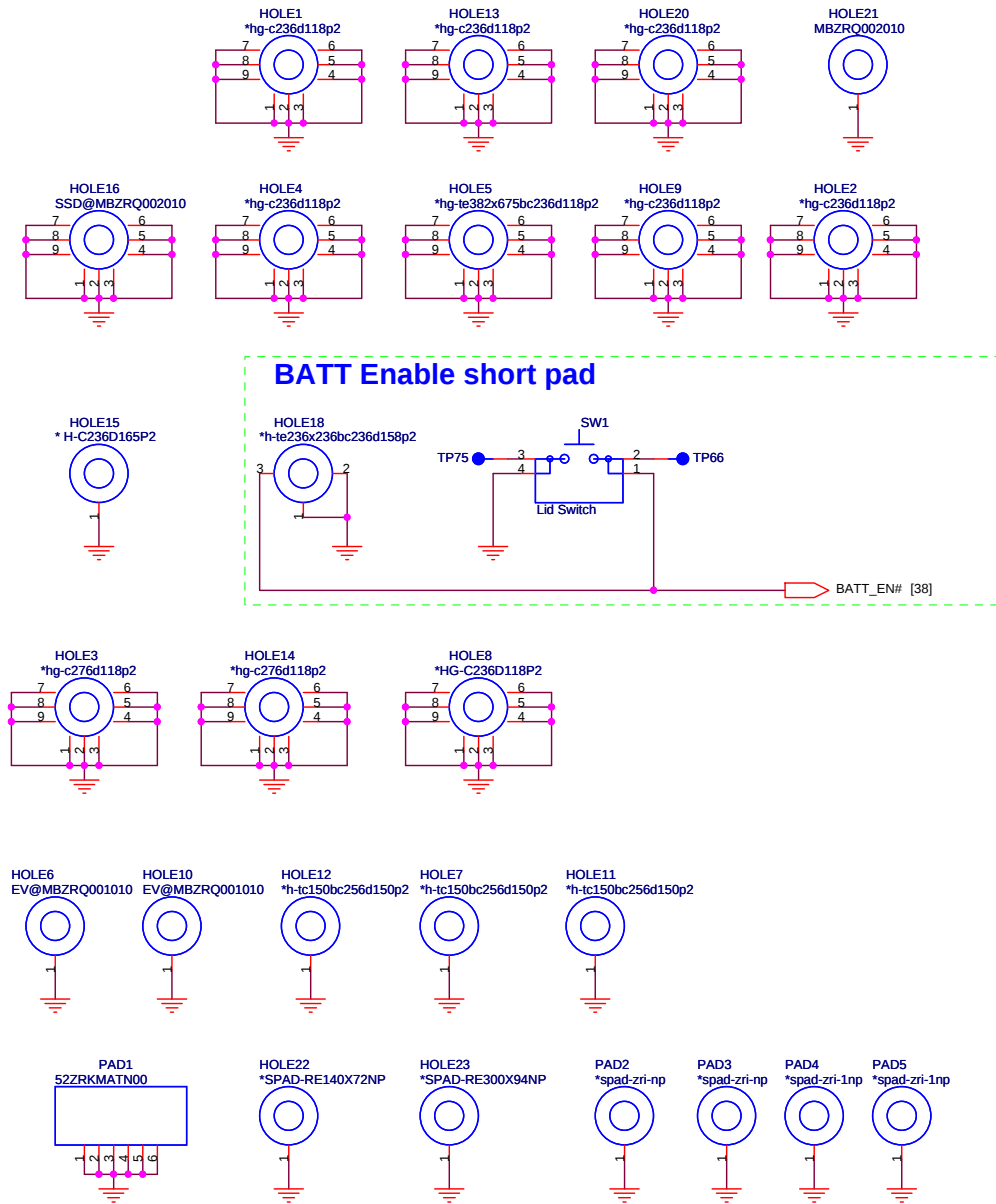
KB/TP/FAN

Rev
A1A

Date: Wednesday, April 24, 2013

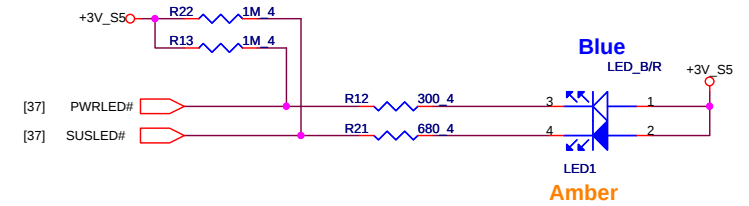
Sheet 35 of 50

HOLE(OTH)

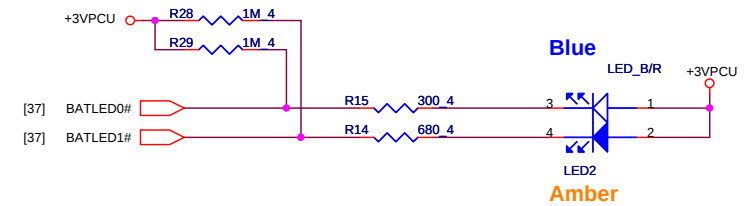


LED(UIF)

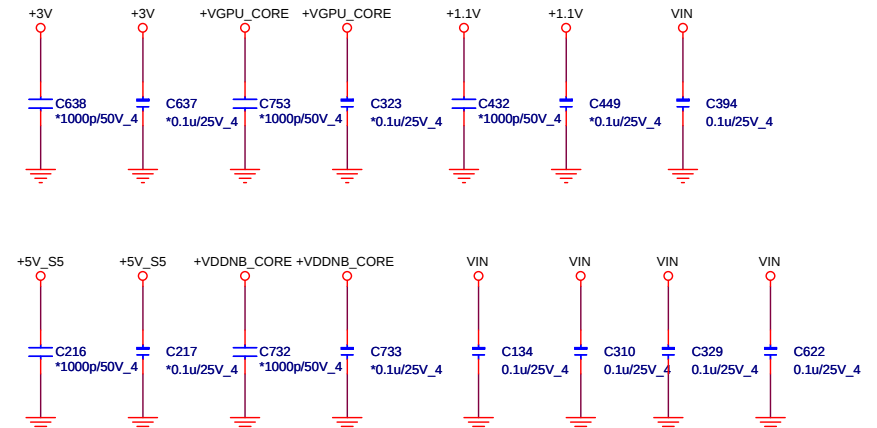
Power



Battery



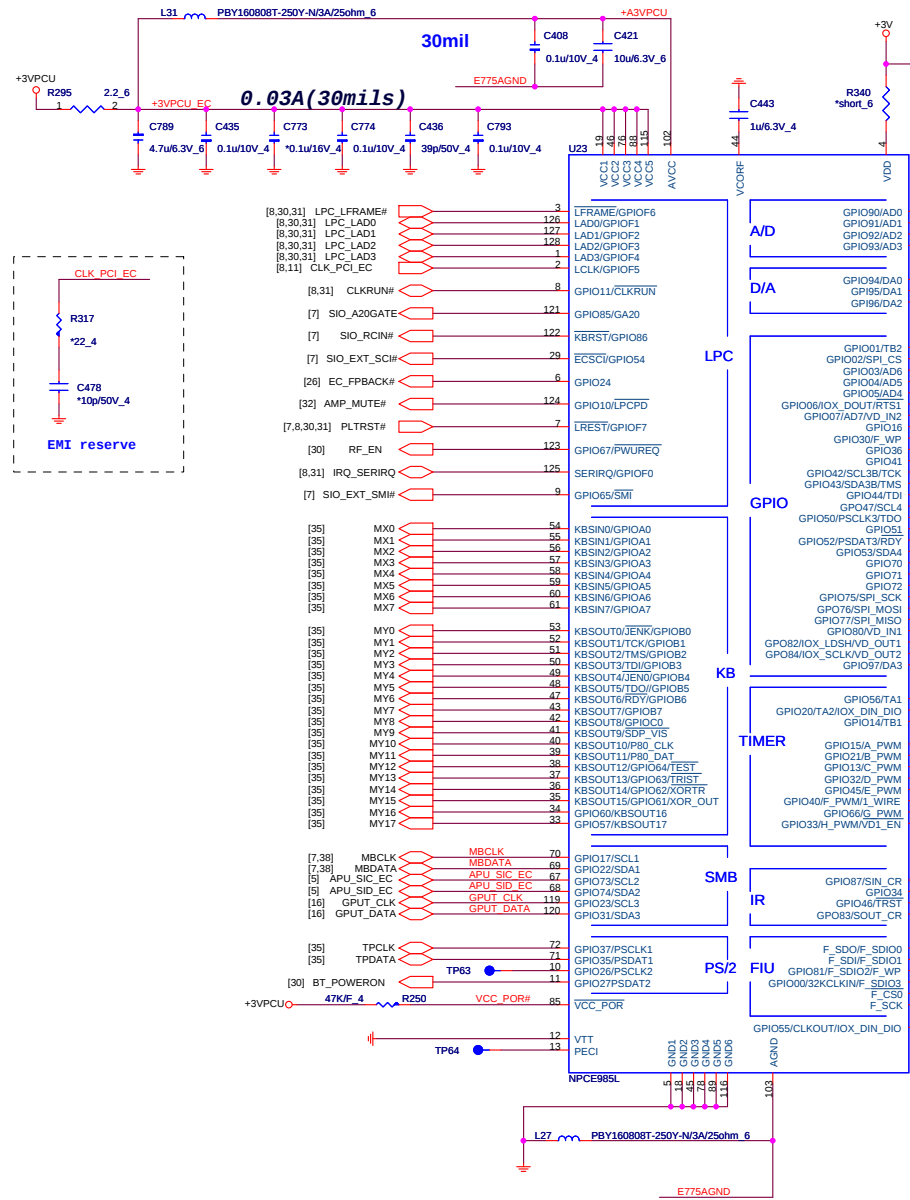
EE RETURN-PATH CAPACITORS(EMC)



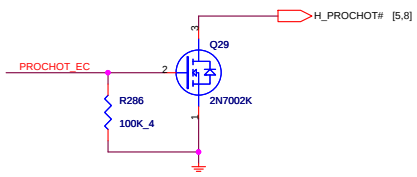
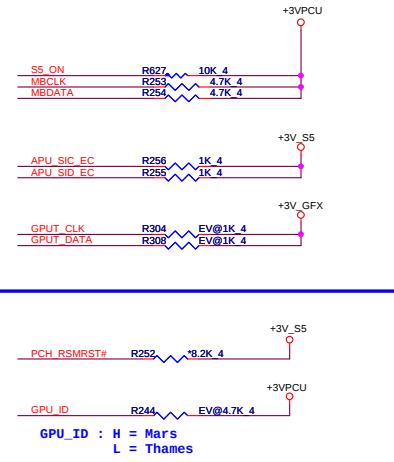
Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	LAN DB/ LED/ EMI/ Hole	A1A
Date:	Wednesday, April 24, 2013	Sheet 36 of 50

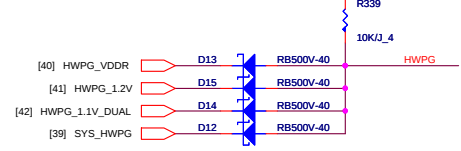
EC(KBC)



SM BUS PU(KBC)



HWPG(KBC)



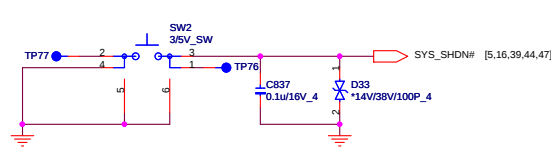
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery, FCH
SM Bus 2	APU
SM Bus 3	GPU

Placement for EC of VIN power plan



3/5VPCU reset switch (CLG)



TDC : 0.38A
PEAK : 0.5A
Width : 20mil

TDC : 0.75A
PEAK : 1A
Width : 40mil

+SMDDR_VREF

PC184
0.22u/10V_4

+3V

PR126
100K/F_4

[37] HWPV_VDDR

[34,37,41,47] MAINON

[37] SUSON

VREF=1.8V

51216 S3

51216 S5

PC186
0.1u/10V_4

PR248
10K/F_4

PR251
51K/F_4

PC187
0.01u/25V_4

OCP=18A
L ripple current
= $(19-1.5) \cdot 1.5 / (0.68u \cdot 400k \cdot 19)$
=5.079A
 $V_{trip} = 18 - (5.079/2) \cdot 4.3mohm$
=0.06647V
 $R_{limit} = 0.06647 / 10uA \cdot 8 = 53.183Kohm$

+0.75V_DDR_VTT
PC180
10u/6.3V_8
PC96
10u/6.3V_8

VTTREF

VTTGND

VTTSENS

VTT

VLDIOIN

V5IN

DRVH

VBST

SW

DRVH

DRVH

VBST

SW

DRVH

DRVH

DRVH

DRVH

DRVH

DRVH

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VDDQSNS

VDDQSNS

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Close to IC

Greater than or equal 40mil

+5V_S5

PC176
10u/6.3V_8

PC103
1u/10V_4

PQ21
RJK03J6DPA

PC109
2200p/50V_4

PC111
4.7u/25V_8

PC105
0.1u/50V_6

PC108
*680p/50V_6

PC112
4.7u/25V_8

PC175
0.1u/50V_6

PC174
330u/2.5V_6X4.2

PC173
*4.7_6

PC108
*680p/50V_6

PC109
2200p/50V_4

PC111
4.7u/25V_8

PC105
0.1u/50V_6

PC108
*680p/50V_6

PC112
4.7u/25V_8

PC175
0.1u/50V_6

PC174
330u/2.5V_6X4.2

PC173
*4.7_6

PC108
*680p/50V_6

PC109
2200p/50V_4

PC111
4.7u/25V_8

PC105
0.1u/50V_6

PC108
*680p/50V_6

PC112
4.7u/25V_8

RDson=4.3mohm

Close to output cap

C-Test

C-Test

+1.5VSUS
1.5 Volt +/- 5%
TDC : 11.3A
PEAK : 15A
OCP : 18A
Width : 480mil

+1.5VSUS

PC174
330u/2.5V_6X4.2

PC175
0.1u/50V_6

PC108
*680p/50V_6

PC109
2200p/50V_4

PC111
4.7u/25V_8

PC105
0.1u/50V_6

PC108
*680p/50V_6

PC112
4.7u/25V_8

PC175
0.1u/50V_6

PC174
330u/2.5V_6X4.2

PC173
*4.7_6

PC108
*680p/50V_6

PC109
2200p/50V_4

PC111
4.7u/25V_8

PC105
0.1u/50V_6

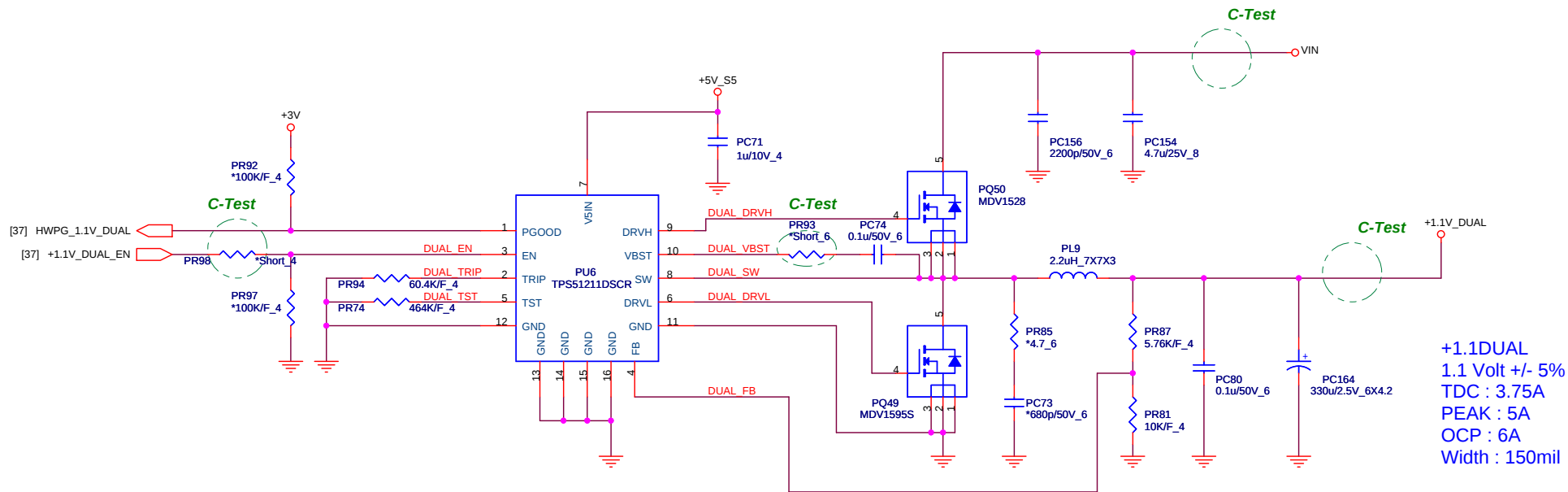
TDC : 0.38A
PEAK : 0.5A
Width : 20mil



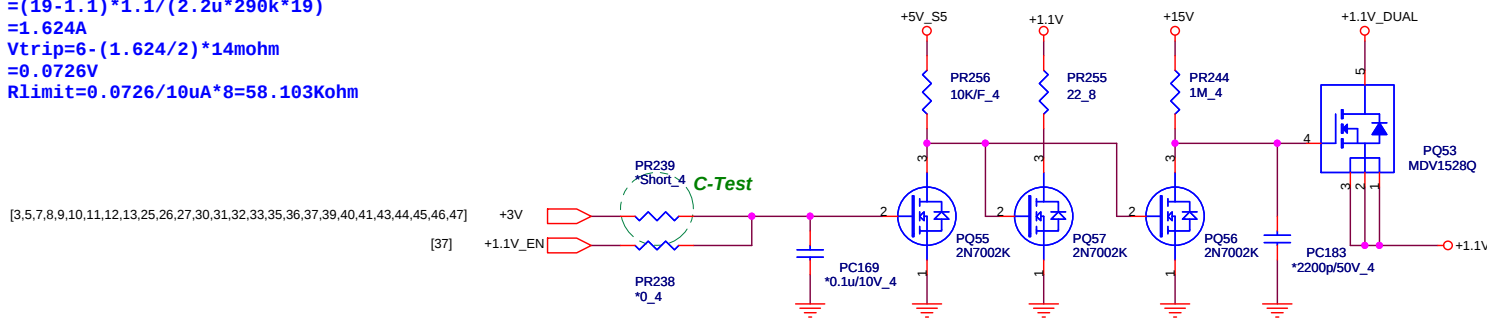
Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	A1A

Date: Wednesday, April 24, 2013 Sheet 40 of 50

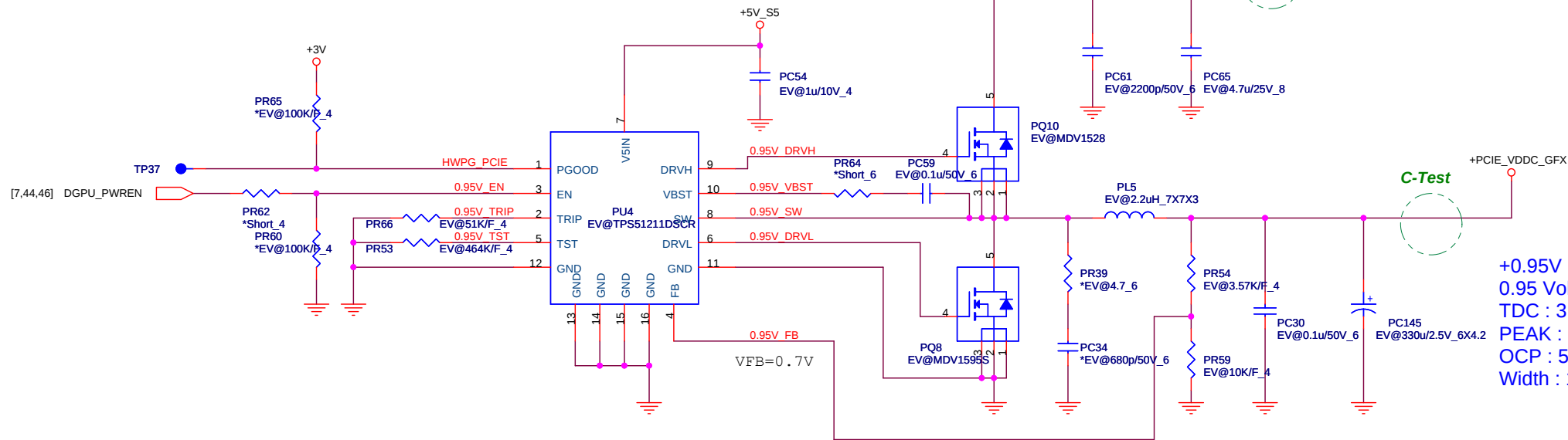


OCP=6A
 L ripple current
 $= (19 - 1.1) * 1.1 / (2.2u * 290k * 19)$
 $= 1.624A$
 $V_{trip} = 6 - (1.624 / 2) * 14mohm$
 $= 0.0726V$
 $R_{limit} = 0.0726 / 10uA * 8 = 58.103Kohm$



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PROJECT : ZRI/ZQI

Size	Document Number	Rev
	+1.1V_DUAL(TPS51211)	A1A
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+0.95V
 0.95 Volt +/- 5%
 TDC : 3.2A
 PEAK : 4.3A
 OCP : 5.2A
 Width : 130mil

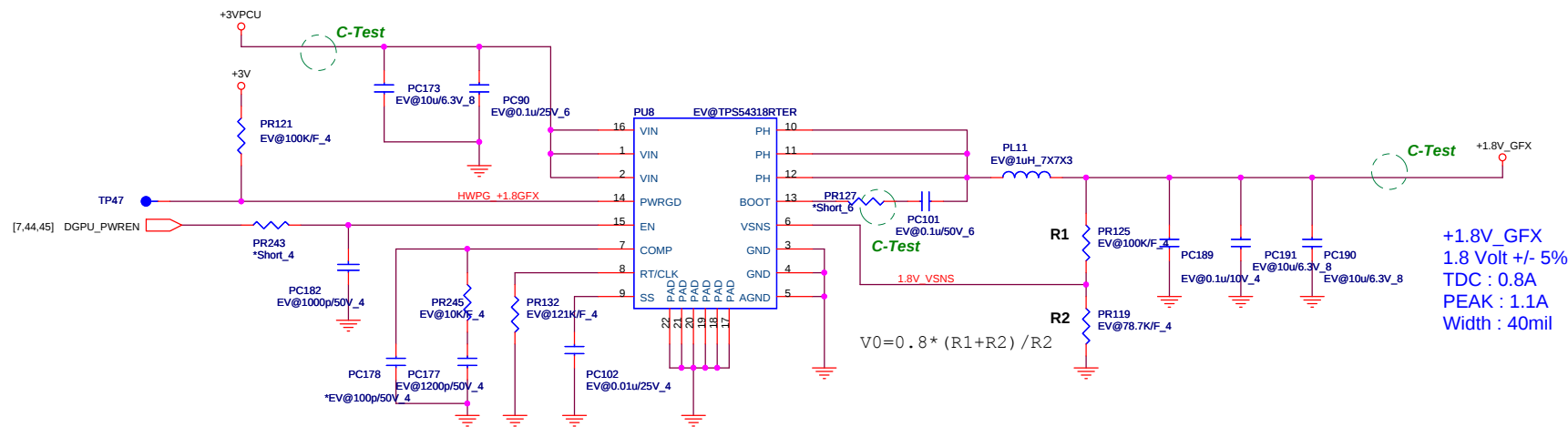
OCP=5.2A
 L ripple current
 $= (19 - 0.95) * 0.95 / (2.2u * 290k * 19)$
 $= 1.415A$
 $V_{trip} = 5.2 - (1.415 / 2) * 14mohm$
 $= 0.06289V$
 $R_{limit} = 0.06289 / 10uA * 8 = 50.318Kohm$



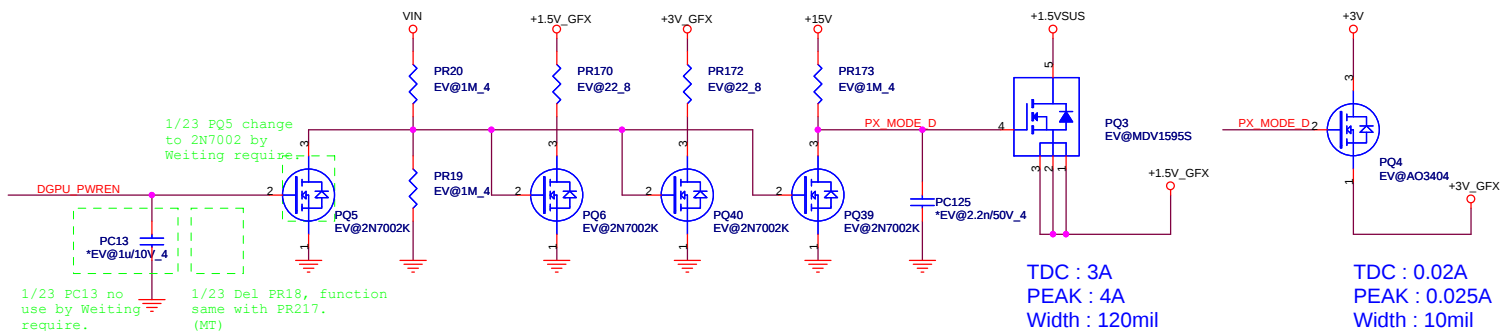
Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	+1.05V(TPS51211)	A1A

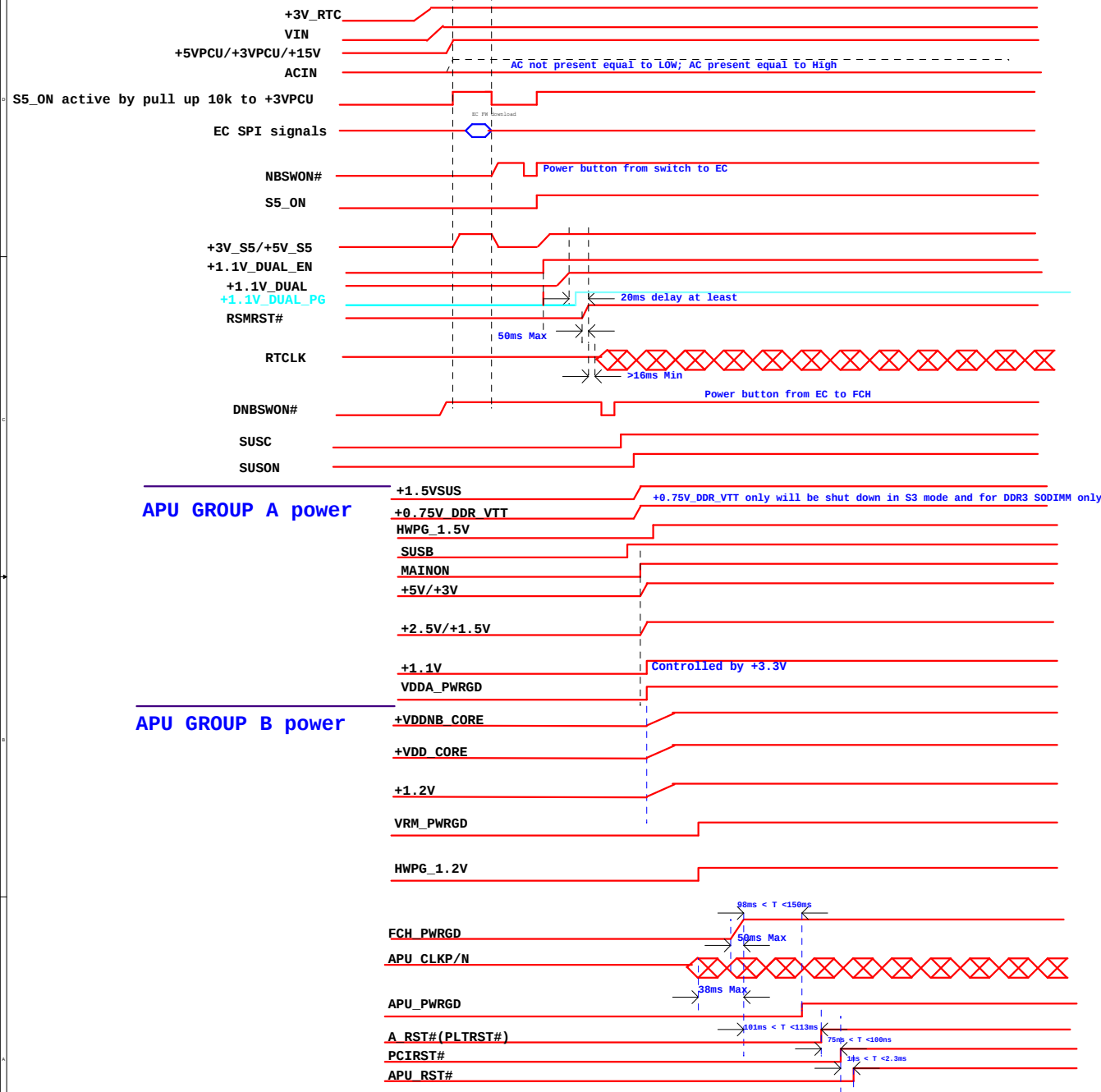
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+1.8V_GFX
1.8 Volt +/- 5%
TDC : 0.8A
PEAK : 1.1A
Width : 40mil



ZRP Power On Sequence: S5 > S0



APU Power on sequence required:

Llano APU:

1.Group A (+1.5VSUS, +2.5V_VDDA) ramp before Group B
(+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M3:

- 1.+3V_S5 ramp before +1.1V_DUAL
- 2.+3V ramp before +1.1V
- 3.+3V_S5,+3V ramping down time > 300us
- 4.100us <= +3V_S5,+3V <= 40ms
- 5.100us <= All power rails except +3V_S5,+3V <= 40ms

Power Tree Table

