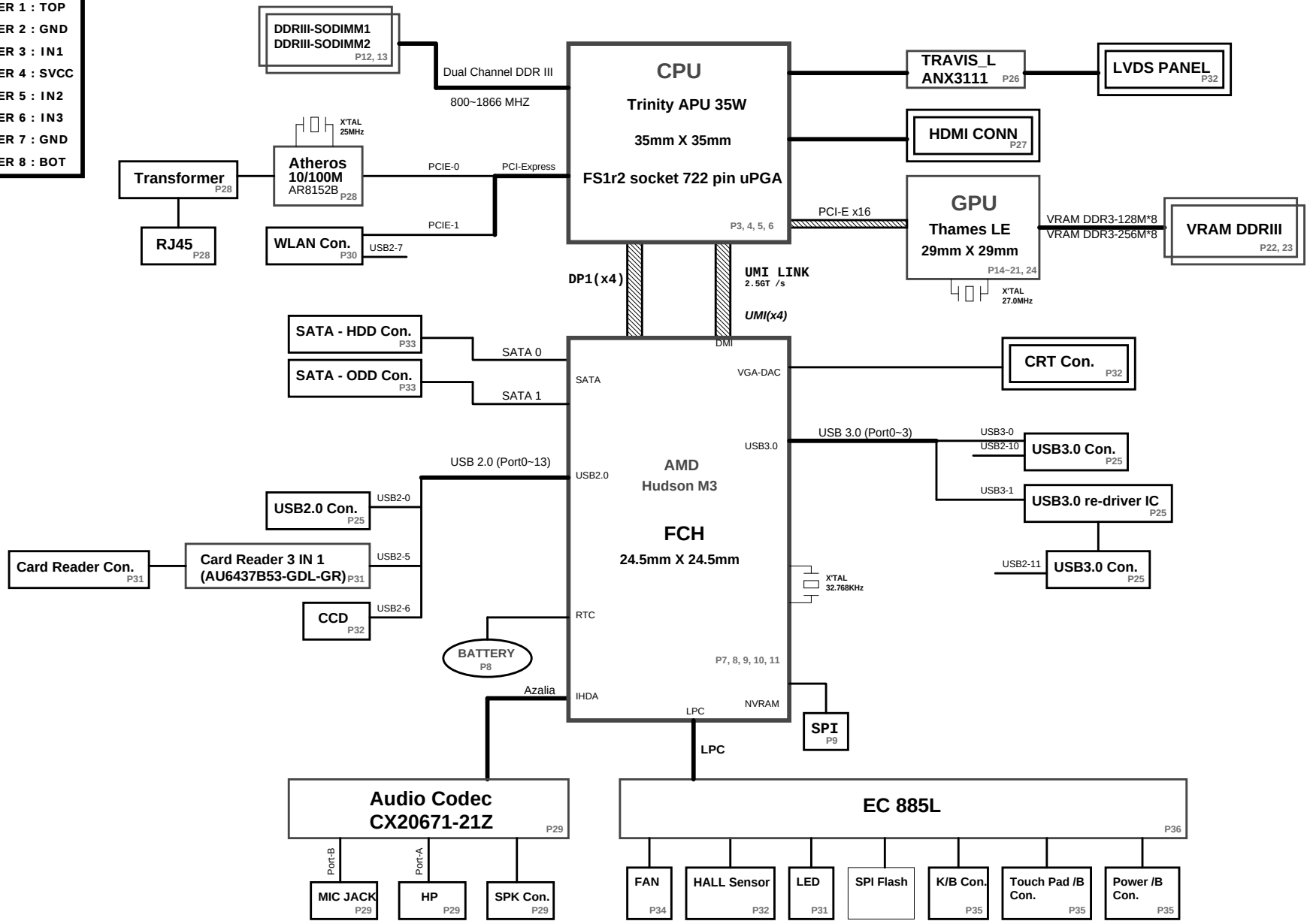
14" BY6/BY6D Comal Block Diagram

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



POWER SYSTEM

ISL88731CHRTZ-T	P37
TPS51123A	P38
TPS51216RUKR	P39
TPS51211DSCR	P40
TPS51211DSCR	P41
OSL6277	P42
G9661-25ADJF12U	P43
ISL95870AHRUZ-L	P44

CHARGER P37

+15V
+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
P38

+SMDDR_VTERM
+SMDDR_VREF
+1.5VSUS
+1.5V_S5
+1.5V
P39

+1.2V_VDDPR P40

+1.1V_DUAL
+1.1V
P41

+VDD_CORE
+VDDNB_CORE P42

+2.5V_VDDA
DISCHARGE P43

+VGPU_CORE
+3V_GPU
+1.8V_GPU
+1.5V_GPU
+1V_GPU
P44

Quanta Computer Inc.
PROJECT : BY6/BY6D

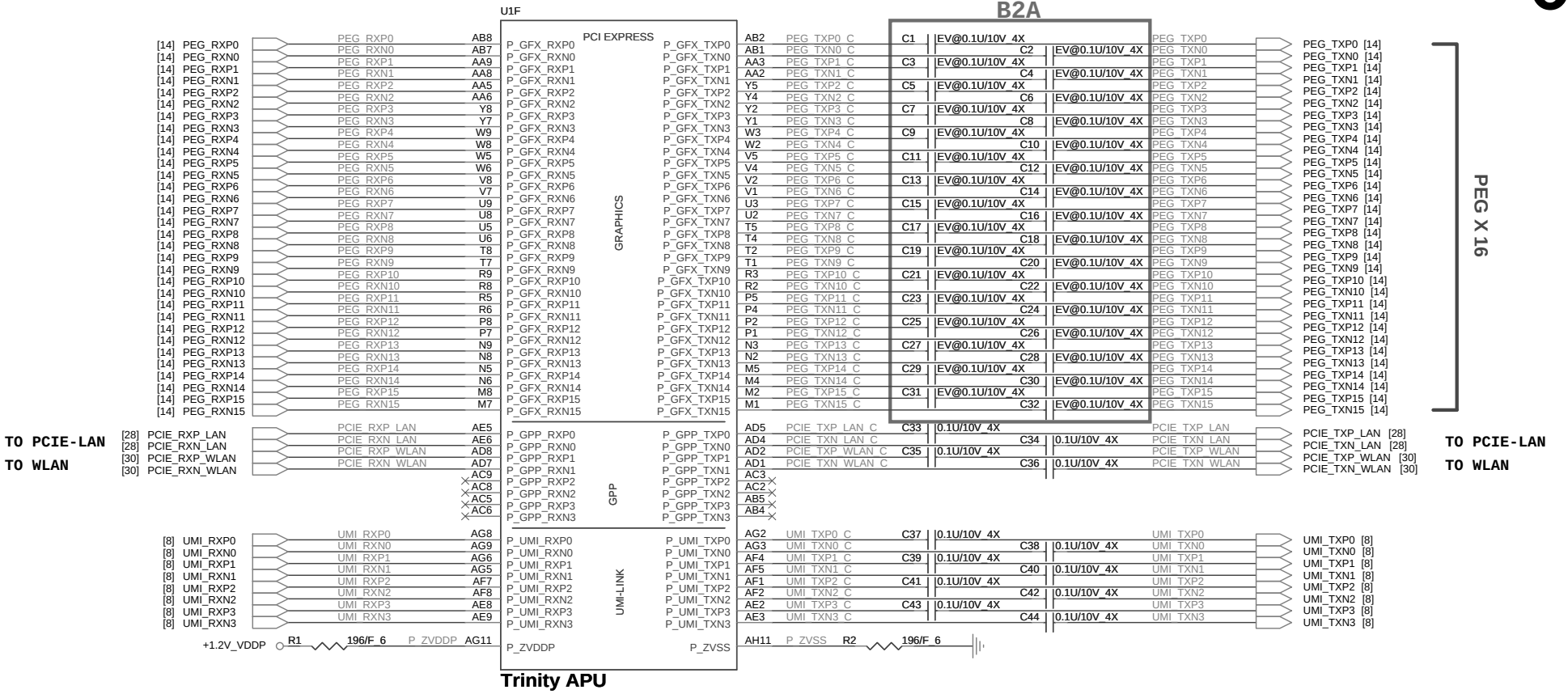
Size	Document Number	Rev
	Block Diagram	A1A
Date: Monday, February 13, 2012	Sheet 1 of 47	

Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3VPCU	+3.3V	AC/DC Insert enable	S0~S5
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P	S0
+1.5VSUS	+1.5V	S5_ON	S0~S3
+1.5V	+1.5V	MAIN_ON	S0
+1.2V_VDDPR	+1.2V	VDDA_PWRGD	S0
+1.1V_DUAL	+1.1V	+1.1V_DUAL_EN	S0~S5
+1.1V	+1.1V	MAIN_ON	S0
+VDD_CORE	~	VDDA_PWRGD	S0
+VDDNB_CORE	~	VDDA_PWRGD	S0
+VGPU_CORE		PX_MODE	S0
+1.8V_GPU	+1.8V	PE_GPIO1	S0
+1V_GPU	+1V	DGPU_PWREN	S0
+3V_GPU	+3.3V	PE_GPIO1	S0
+1.5V_GPU	+1.5V	PX_MODE_D	S0
+2.5V_VDDA	+2.5V	MAIN_ON	S0

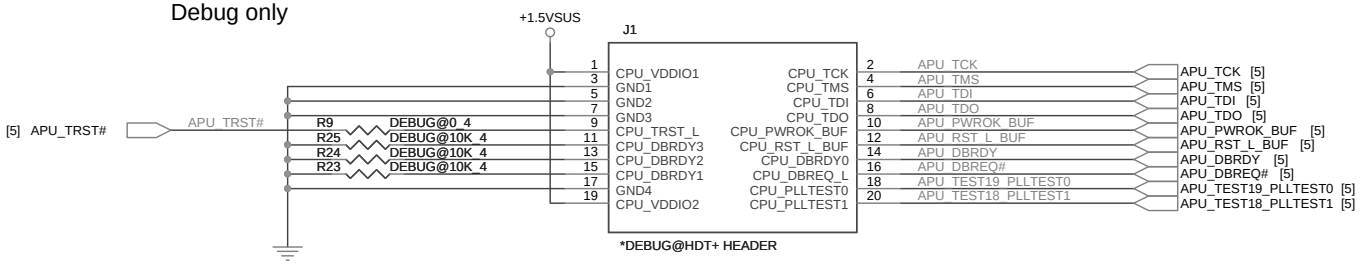
GND PLANE	PAGE
GND_SIGNAL	32
8769GND	36
	28
GND	ALL
ADOGND	29

ITEM	Value Code	FUNCTIONS
1	CEC@	CEC
2	Debug@	HDT+ Debug
3	EV@	DISCRETE
4	IV@	UMA
5	U3@	Internal USB 3.0
6	1G4@	VRAM 1Gb*4
7	1G8@	VRAM 1Gb*8
8	2G@	VRAM 2Gb
9	AMD@	AMD VRAM
10	DIS@	DISCRETE
11	M2@	M2 FCH
12	M3@	M3 FCH
13	NMP@	LPC Debug Card
14	PX4@	PX4 Mode
15	PX5@	PX5 Mode
16	Sam@	Samsung VRAM
17	U2@	USB 2.0 (colay W USB 3.0)



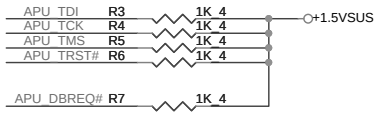
HDT+ Connector

Debug only

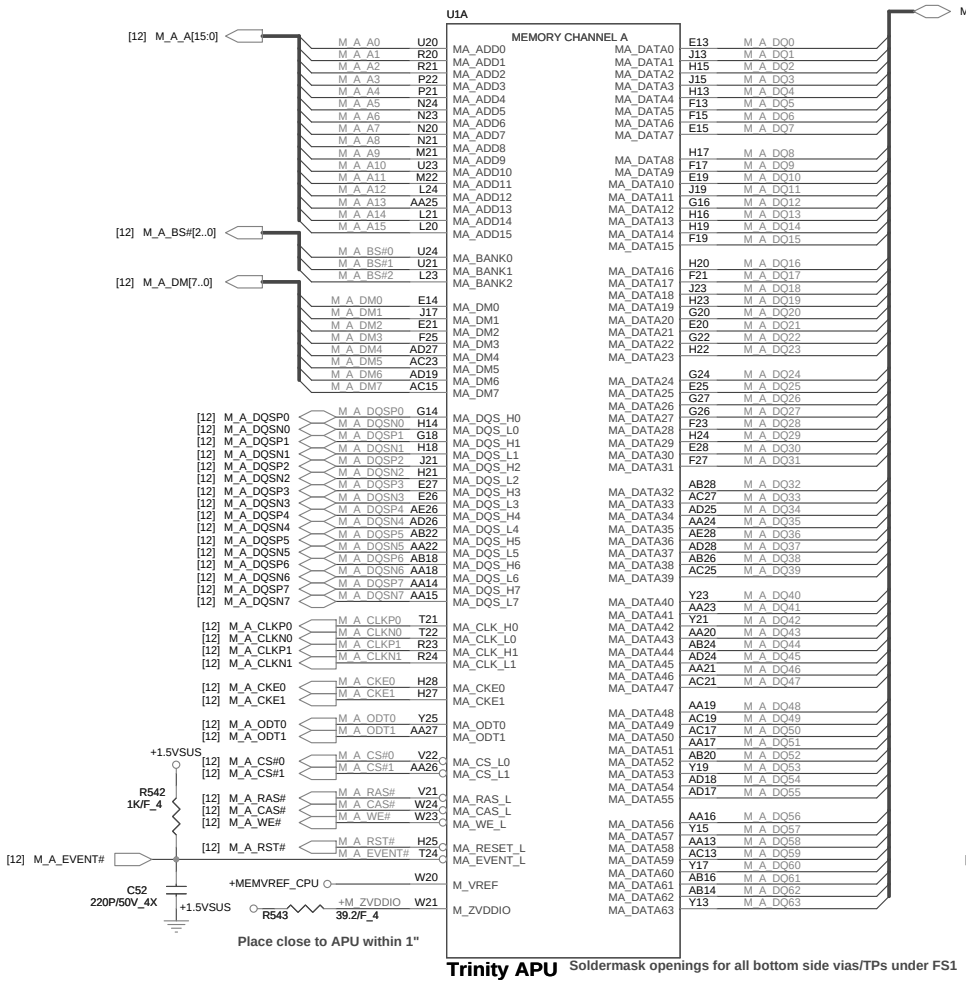


*DEBUG@HDT+ HEADER

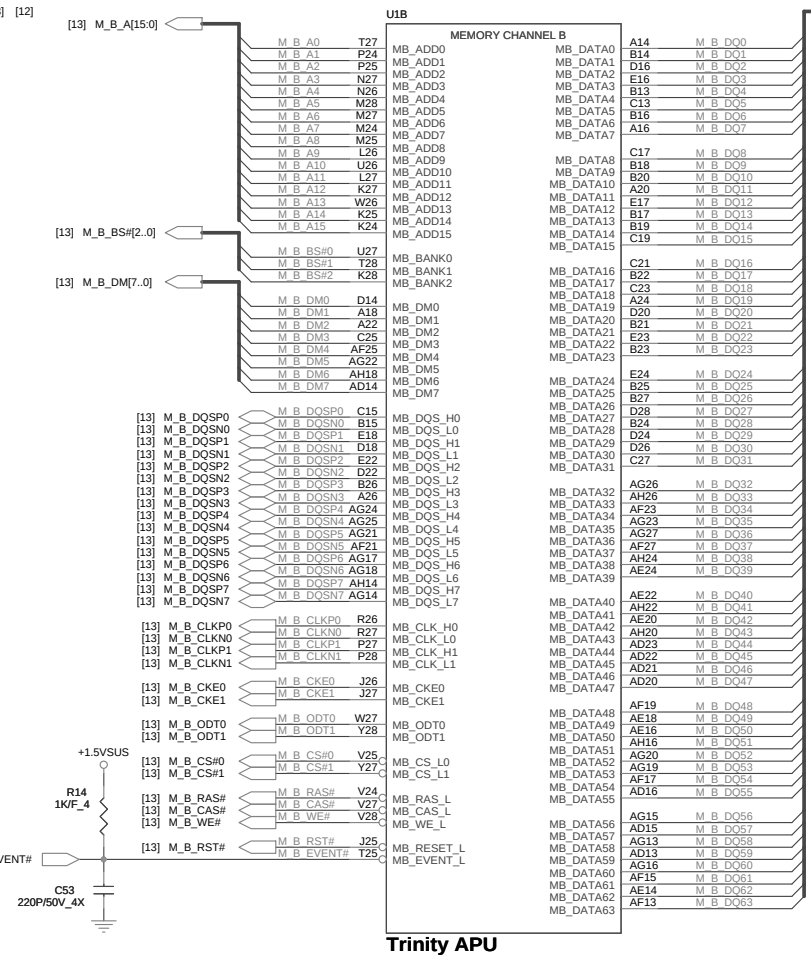
Close by HDT+ Conector



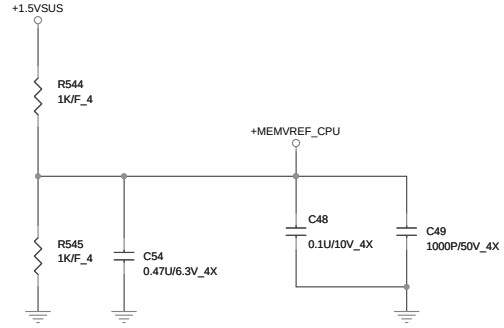
Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number	Rev
	APU 1/4(PCIE/UMI/GPP/HDT)	1A
Date: Tuesday, February 14, 2012	Sheet 3 of 47	



Trinity APU Soldermask openings for all bottom side vias/TPs under FS1



Trinity APU

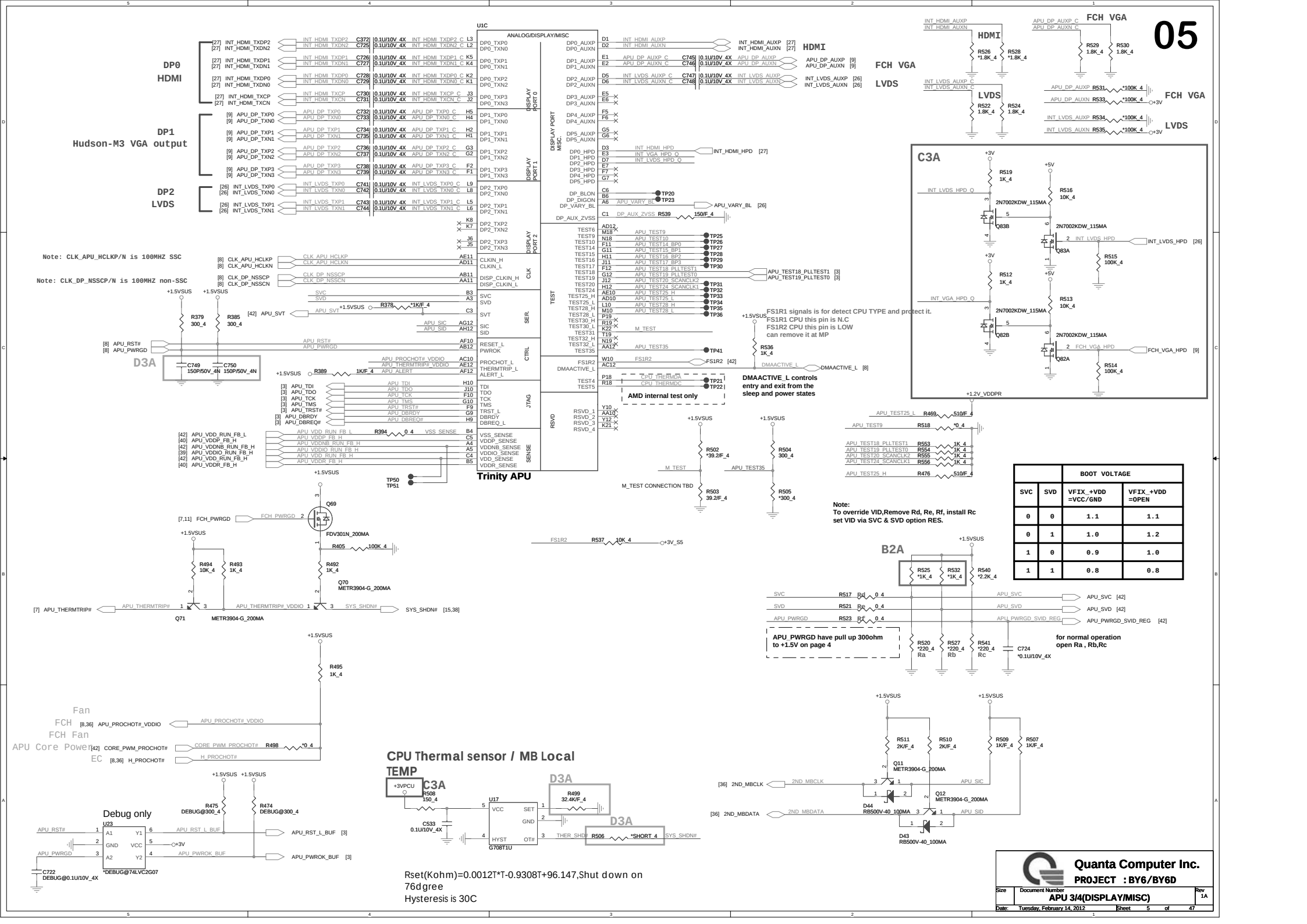


Quanta Computer Inc.

PROJECT : BY6/BY6D

Size	Document Number	Rev
	APU 2/4(DDR3 MEM I/F)	1A

Date: Tuesday, February 14, 2012 Sheet 4 of 47


05
DP0
HDMI
DP1
Hudson-M3 VGA output
DP2
LVDS
U1C
ANALOG/DISPLAY/MISC
Trinity APU
HDMI
FCH VGA
LVDS
C3A
D3A
B2A
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
FS1R1 signals is for detect CPU TYPE and protect it.
FS1R1 CPU this pin is N.C
FS1R2 CPU this pin is LOW
can remove it at MP
DMAACTIVE_L controls
entry and exit from the
sleep and power states
AMD internal test only
M_TEST CONNECTION TBD
Note:
To override VID,Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.
APU_PWRGD have pull up 300ohm
to +1.5V on page 4
for normal operation
open Ra , Rb,Rc
BOOT VOLTAGE
SVC
SVD
VFIX_+VDD =VCC/GND
VFIX_+VDD =OPEN
0 0 1.1 1.1
0 1 1.0 1.2
1 0 0.9 1.0
1 1 0.8 0.8
Fan
FCH Fan
APU Core Power
EC
CPU Thermal sensor / MB Local TEMP
Debug only
Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 76dgree
Hysteresis is 30C
Quanta Computer Inc.
PROJECT : BY6/BY6D
APU 3/4(DISPLAY/MISC)
Rev 1A
Tuesday, February 14, 2012
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APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

EMI

+VDD_CORE — C58 470P/50V_4X, C59 470P/50V_4X, C60 470P/50V_4X

U1D

+VDD_CORE

36A
Maximum IDDspike 50A

D3A
C64 22U/6.3V_6X, C73 22U/6.3V_6X, C61 22U/6.3V_6X, C65 22U/6.3V_6X, C66 22U/6.3V_6X, C129 ESD@39P/50V_4N, C141 ESD@39P/50V_4N
C129 and C141 close to C61 and C65

C67 22U/6.3V_6X, C74 22U/6.3V_6X, C75 22U/6.3V_6X, C62 22U/6.3V_6X, C68 22U/6.3V_6X

C76 0.22U/10V_4X, C77 0.22U/10V_4X, C71 180P/50V_4N, C72 180P/50V_4N, C78 0.01U/25V_4X, C79 0.01U/25V_4X, C136 0.01U/25V_4X

25A
Maximum IDDNBspike 33A

+VDDNB_CORE

D3A
C281 ESD@39P/50V_4N, C323 ESD@39P/50V_4N, C69 22U/6.3V_6X, C63 22U/6.3V_6X, C70 10U/6.3V_8X
Close to C80 and C82

C80 0.22U/10V_4X, C81 0.22U/10V_4X, C82 180P/50V_4N, C83 180P/50V_4N, C84 180P/50V_4N

+VDDNB_CAP

C85 22U/6.3V_6X, C86 22U/6.3V_6X, C87 180P/50V_4N

DECOUPLING between PROCESSOR and DIMMs
Across VDDIO and VSS split

+1.5VSUS

C88 0.22U/10V_4X, C89 0.22U/10V_4X, C90 180P/50V_4N, C91 180P/50V_4N

VDDIO=4.6A (Up to DDR3_1600 @ 1.5V)

+1.5VSUS

C92 0.22U/10V_4X, C93 0.22U/10V_4X, C94 0.22U/10V_4X, C95 0.22U/10V_4X, C96 0.22U/10V_4X, C97 0.22U/10V_4X

C98 22U/6.3V_6X, C99 22U/6.3V_6X, C100 22U/6.3V_6X, C101 22U/6.3V_6X, C102 4.7U/6.3V_6X, C103 4.7U/6.3V_6X, C104 4.7U/6.3V_6X, C105 4.7U/6.3V_6X

C137 180P/50V_4N, C106 180P/50V_4N

D3A
+1.2V_VDDPR — R11 *SHORT_8

VDDP_A + VDDP_B = 5A

+1.2V_VDDP

C107 22U/6.3V_6X, C108 10U/6.3V_8X, C109 10U/6.3V_8X, C110 10U/6.3V_8X

C114 0.22U/10V_4X, C115 0.22U/10V_4X, C116 180P/50V_4N, C117 180P/50V_4N

VDDR = 3.3A (Up to DDR3_1600 @ 1.2V)

+1.2V_VDDPR

+1.2V_VDDR — R12 *SHORT_8

D3A

C111 10U/6.3V_8X, C112 10U/6.3V_8X, C113 10U/6.3V_8X

C118 0.22U/10V_4X, C119 0.22U/10V_4X, C120 1000P/50V_4X, C121 180P/50V_4N, C122 180P/50V_4N

VDDA = 0.75A

+2.5V_VDDA — L1 HCB1608KF-221T20_2A

B2A

C123 4.7U/6.3V_6X, C124 0.22U/10V_4X, C125 3300P/50V_4X

D3A
C573 ESD@39P/50V_4N
Close to L1

Trinity APU

U1E

Trinity APU

Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: APU 4/4(POWER/GND)	Rev: 1A
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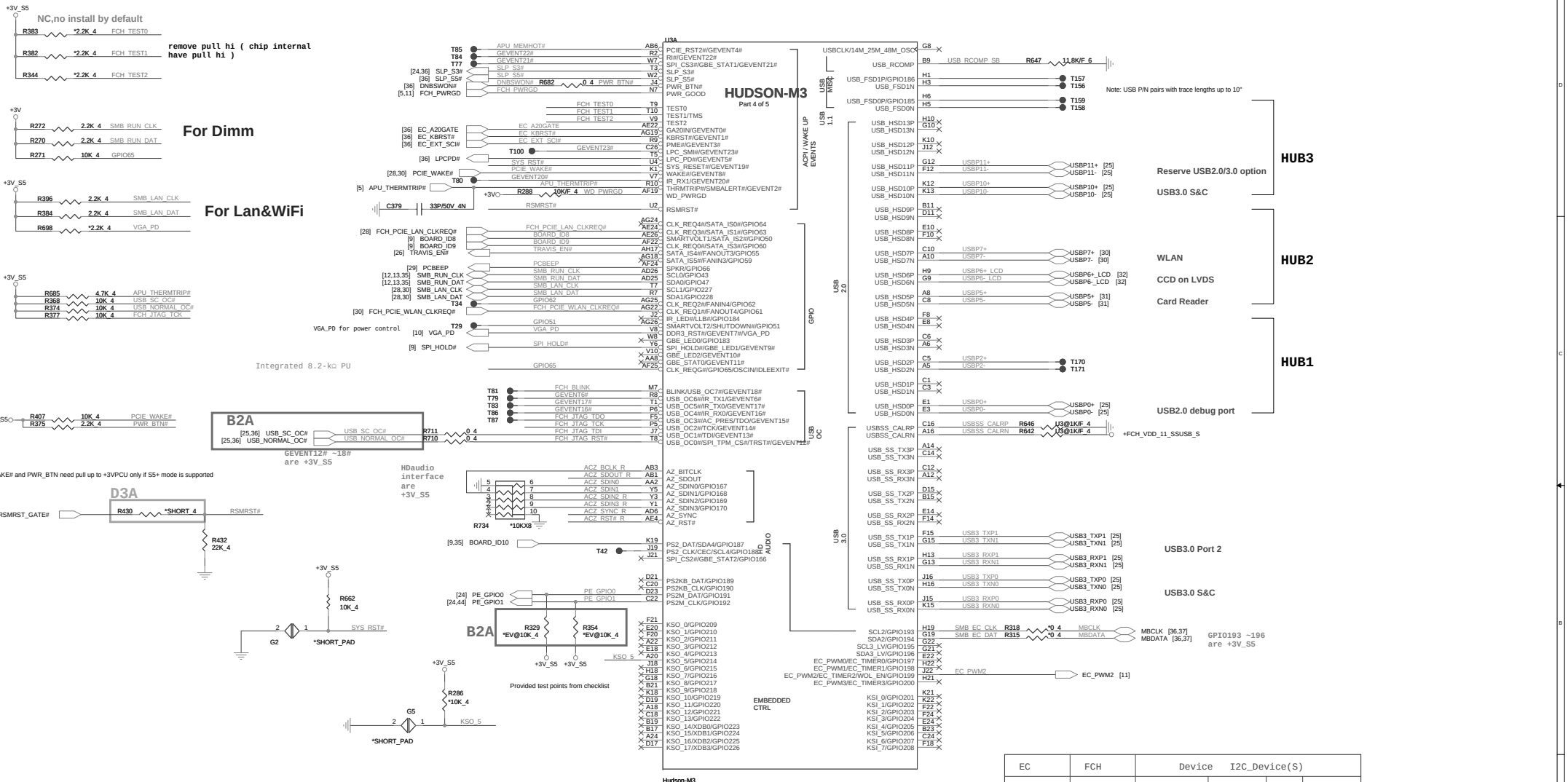

EC	FCH	Device	I2C_Device(S)		
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		EEPROM	APU		ALL
I2Ce_3(M)		VGA Thermal			
	I2Cf_3(M)			APU	S5
	I2Cf_1(M)	Lan	WLan		S5
	I2Cf_0(M)	Dimm	Clk Gen		S0

Quanta Computer Inc.
PROJECT : BY6/BY6D

Size	Document Number	Rev
	FCH 1/5(GPIO/USB/AZ)	1A

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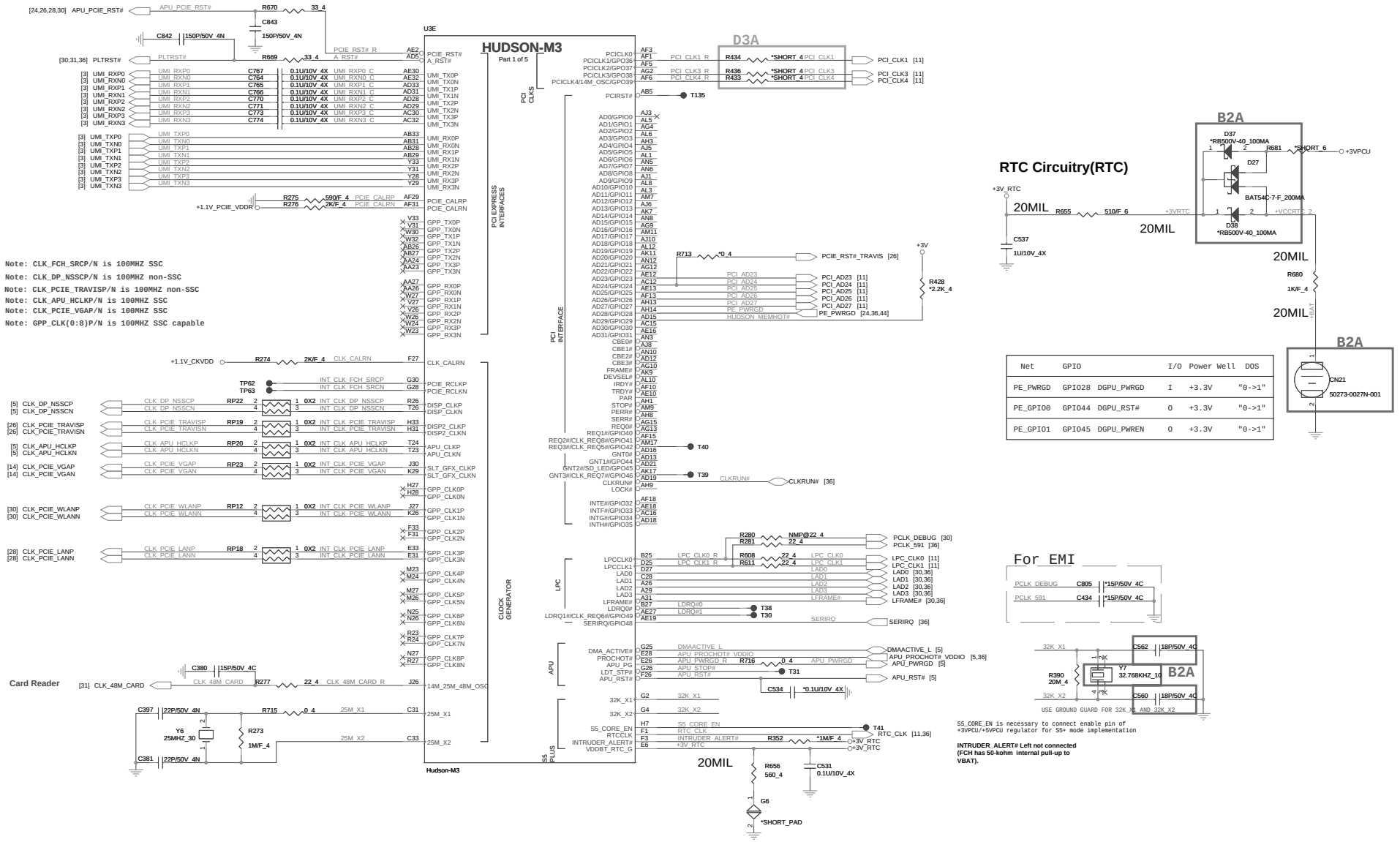
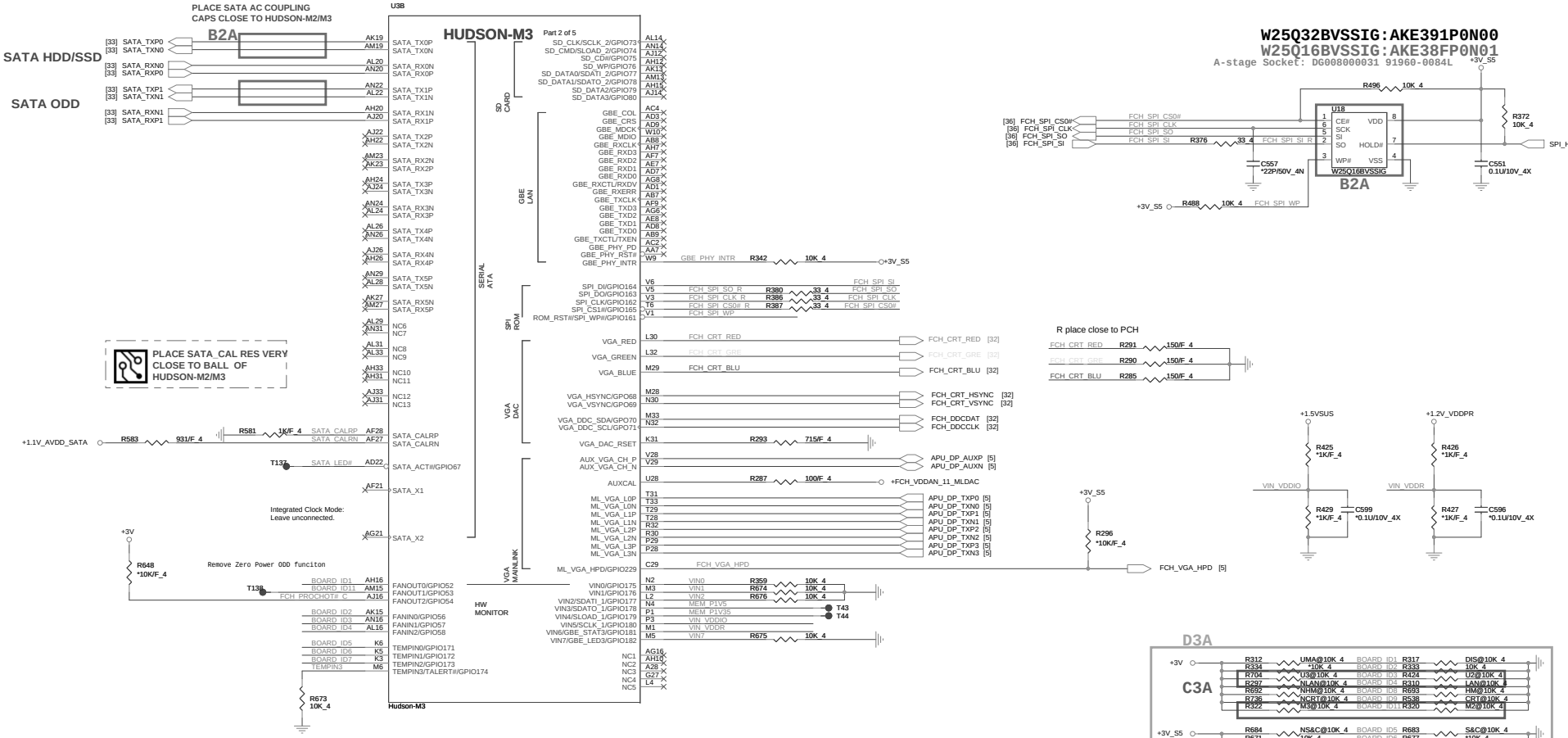


Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: FCH 2/5(ACPI/PCI/CLK)	Rev: 1A
Date: Tuesday, February 14, 2012	Sheet 8 of 47	



BOARD ID SETTING

	Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11
	UMA SKU VGA SKU	H L										
	VRAM 900M VRAM 800M		H L									
C3A	USB3.0 USB2.0			H L								
B2A	W/O LAN W LAN				H L							
	W/O S&C W S&C					H L						
	W/O BT W BT						H L					
	W/O CEC W CEC							H L				
B2A	W/O HDMI W HDMI								H L			
	W/O CRT W CRT									H L		
	Metal/IMR TEXTURE										H L	
C3A B2A	FCH-M3 FCH-M2											H L

Quanta Computer Inc.
PROJECT : BY6/BY6D

Size	Document Number	Rev
	FCH 3/5(SATA/VGA/GND/SPI)	1A

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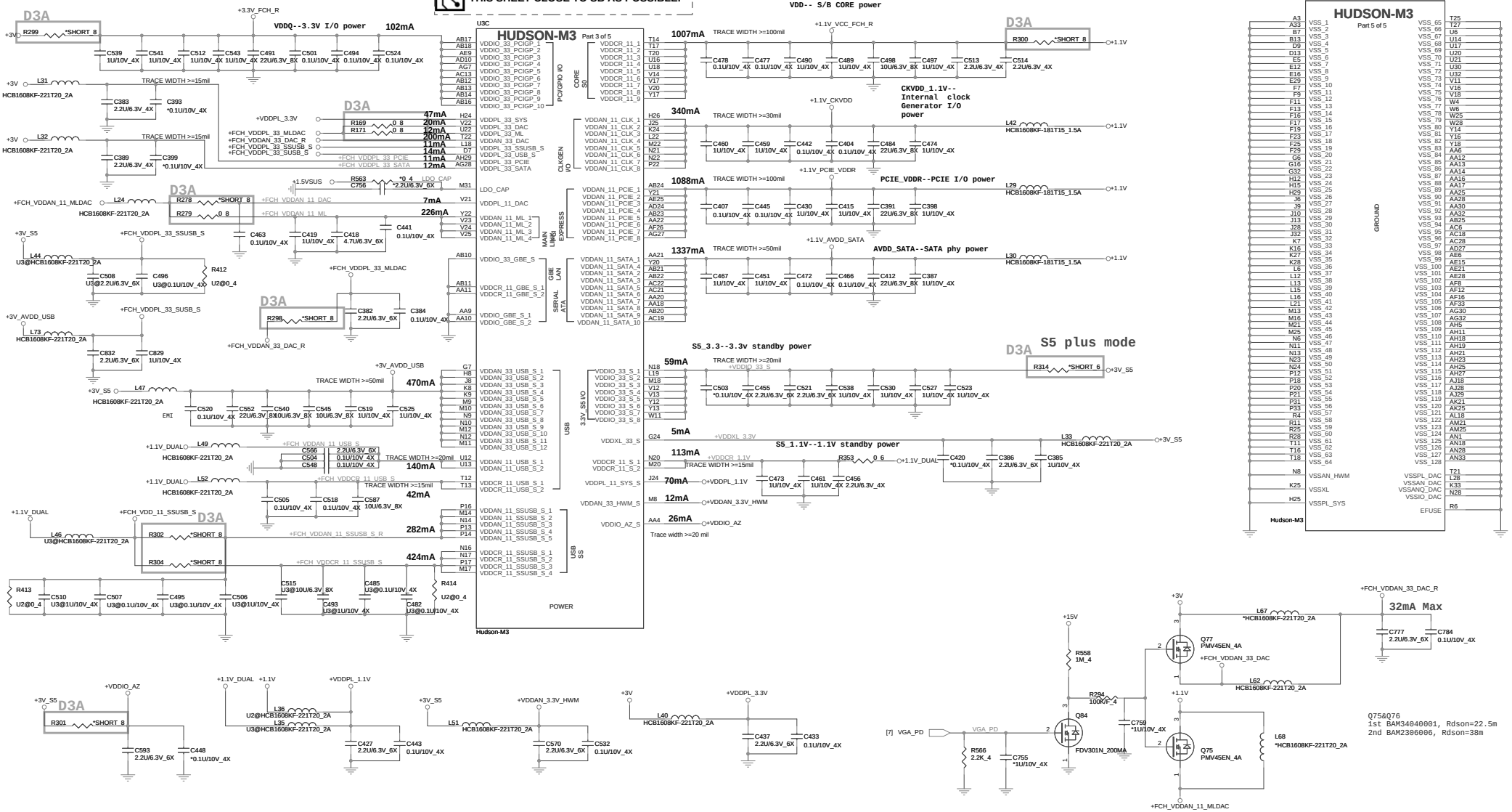
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



Quanta Computer Inc.			
PROJECT : BY6/BY6D			
Size	Document Number		Rev
	FCH 4/5(POWER)		1A
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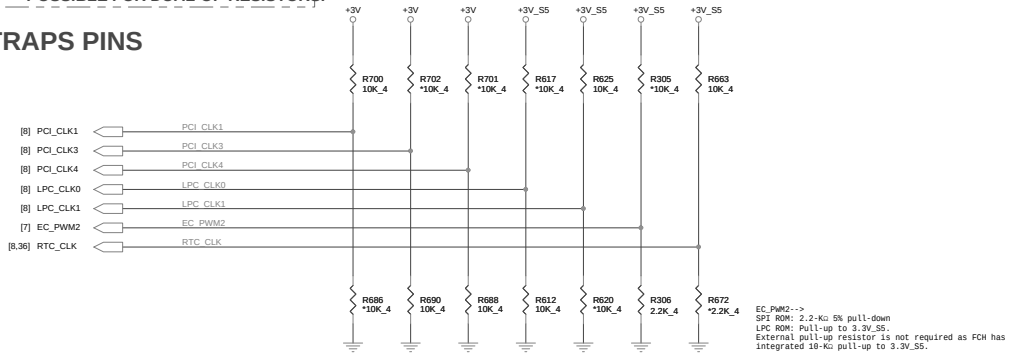
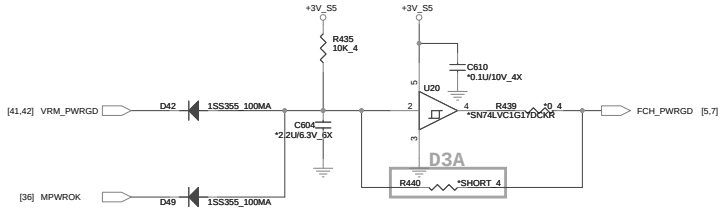
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS





FCH PWRGD CKT

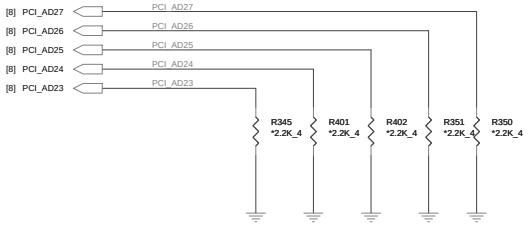
Remove PCI_CLK2 function

REQUIRED STRAPS

	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Quanta Computer Inc.
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	FCH 5/5(STRAP & PWRGD)	1A
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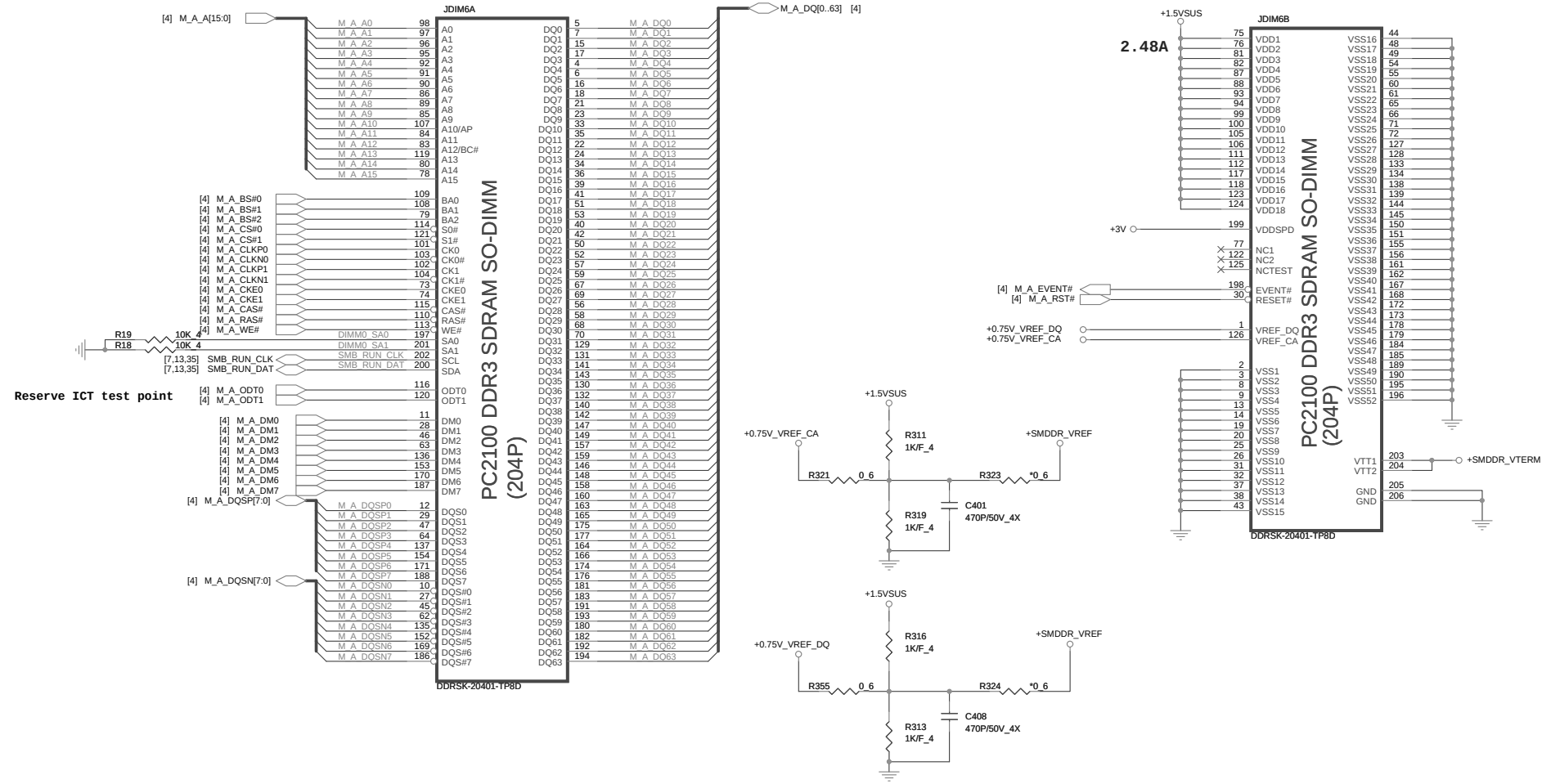
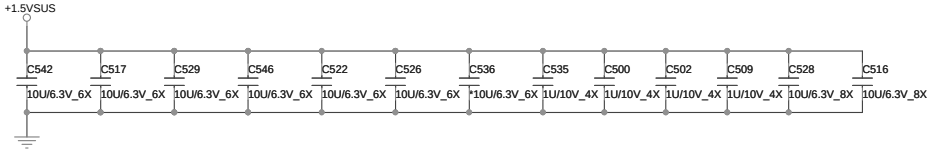
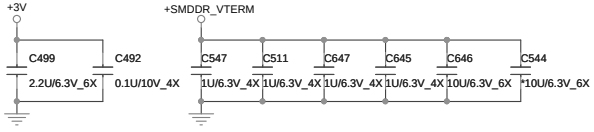
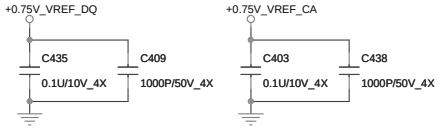
DDR_STD(DDR)



Place these Caps near So-Dimm0.

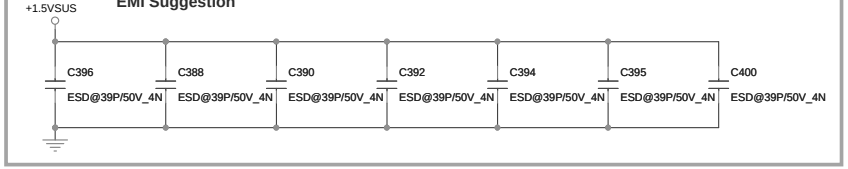






D3A

EMI Suggestion



Quanta Computer Inc.

PROJECT : BY6/BY6D

Size	Document Number	Rev
	DDR3 DIMM-1	1A

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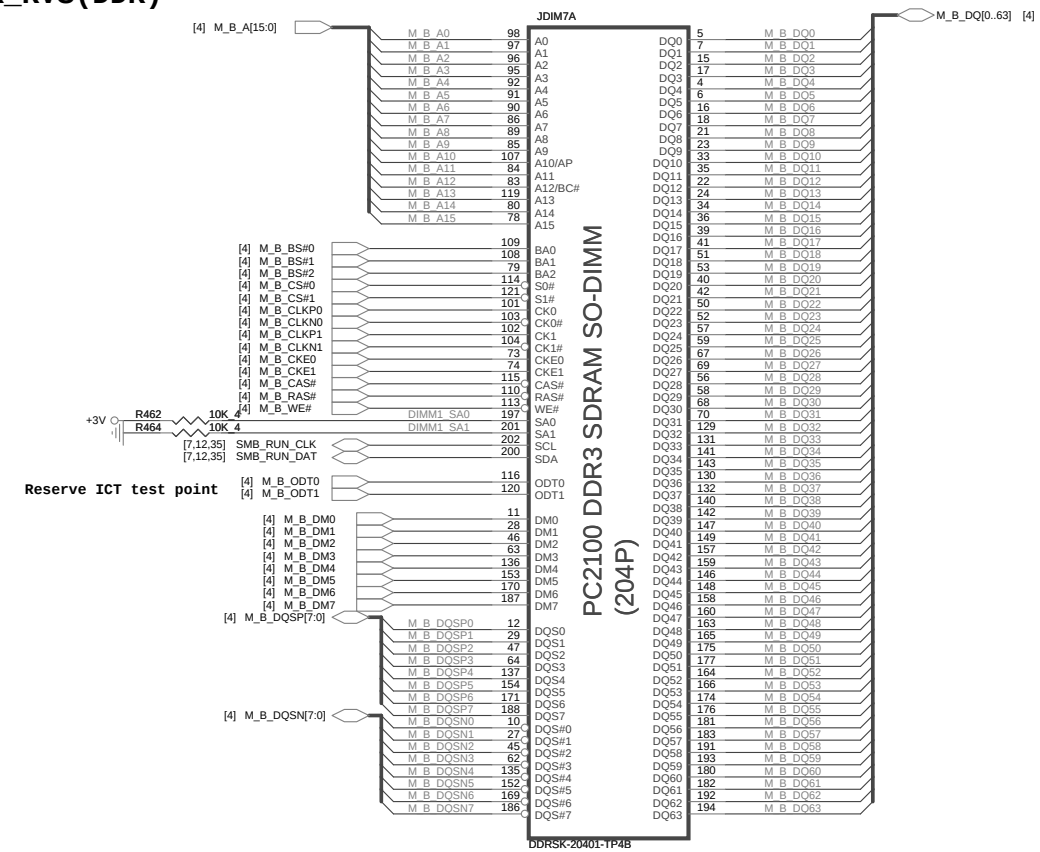
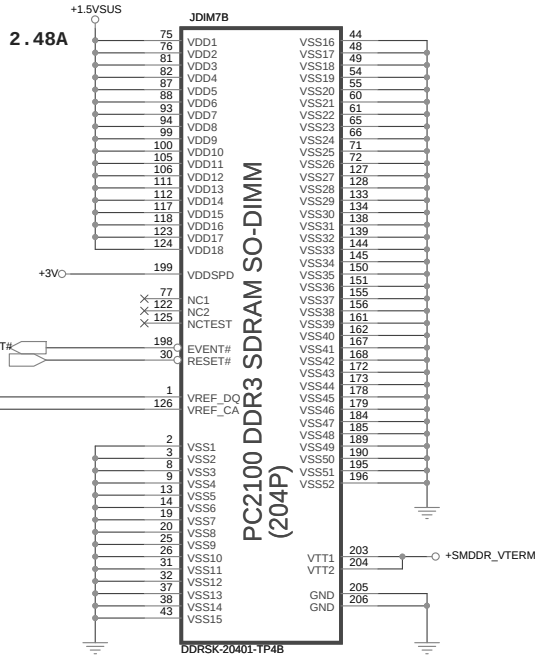
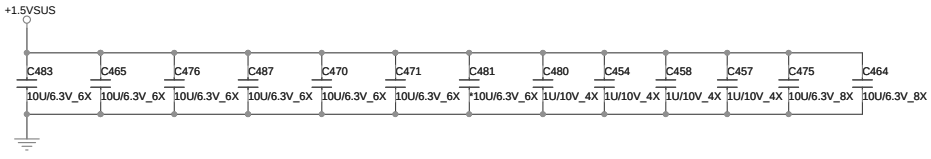
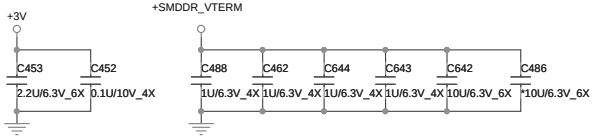
DDR_RVS(DDR)

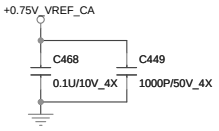


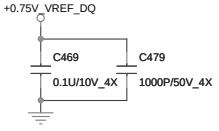


Place these Caps near So-Dimm1.

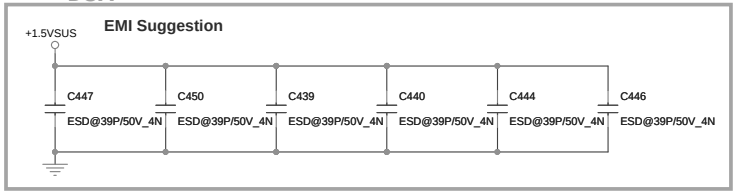








D3A



Quanta Computer Inc.

PROJECT : BY6/BY6D

Size	Document Number	Rev
	DDR3 DIMM-2	1A

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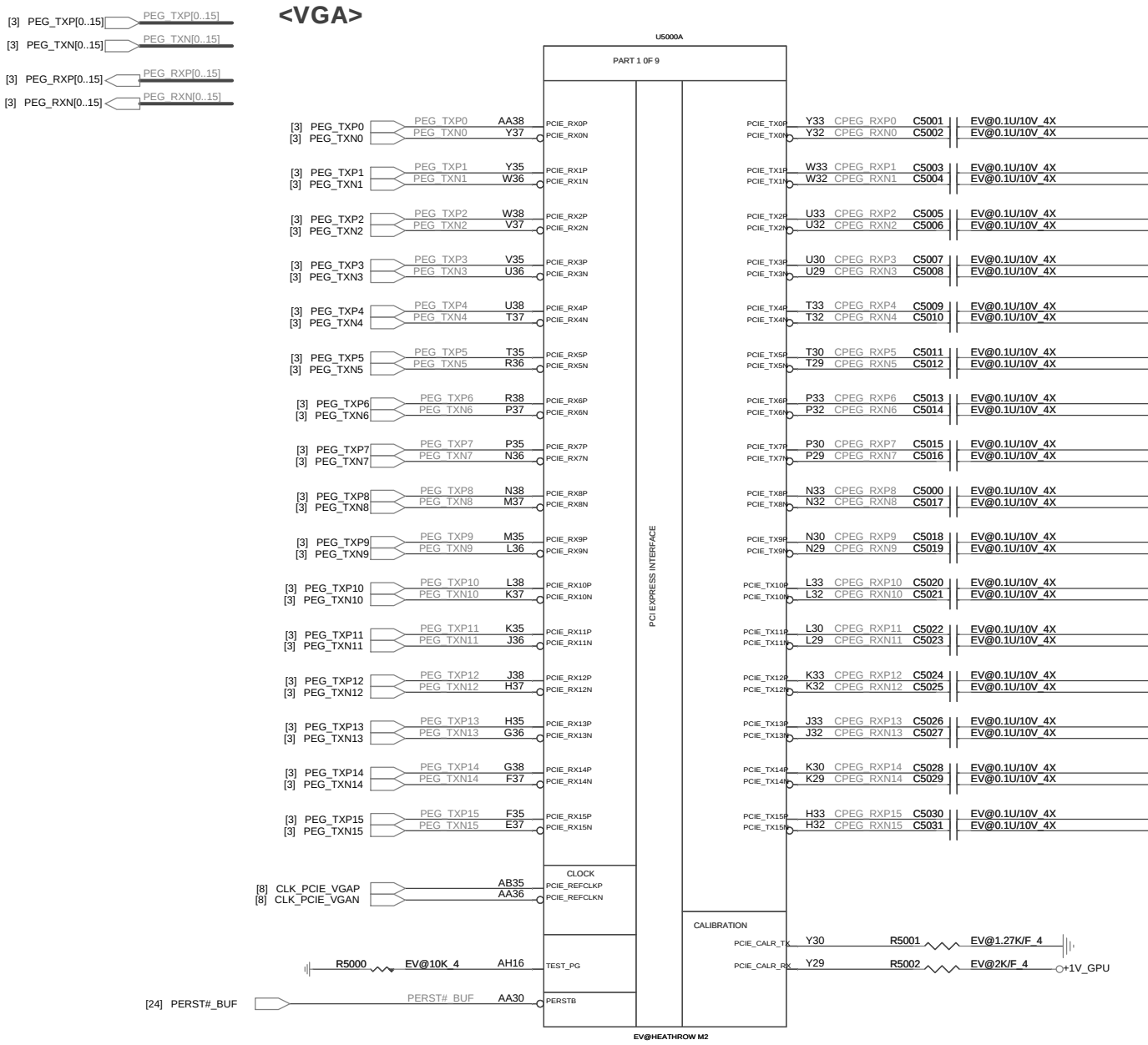


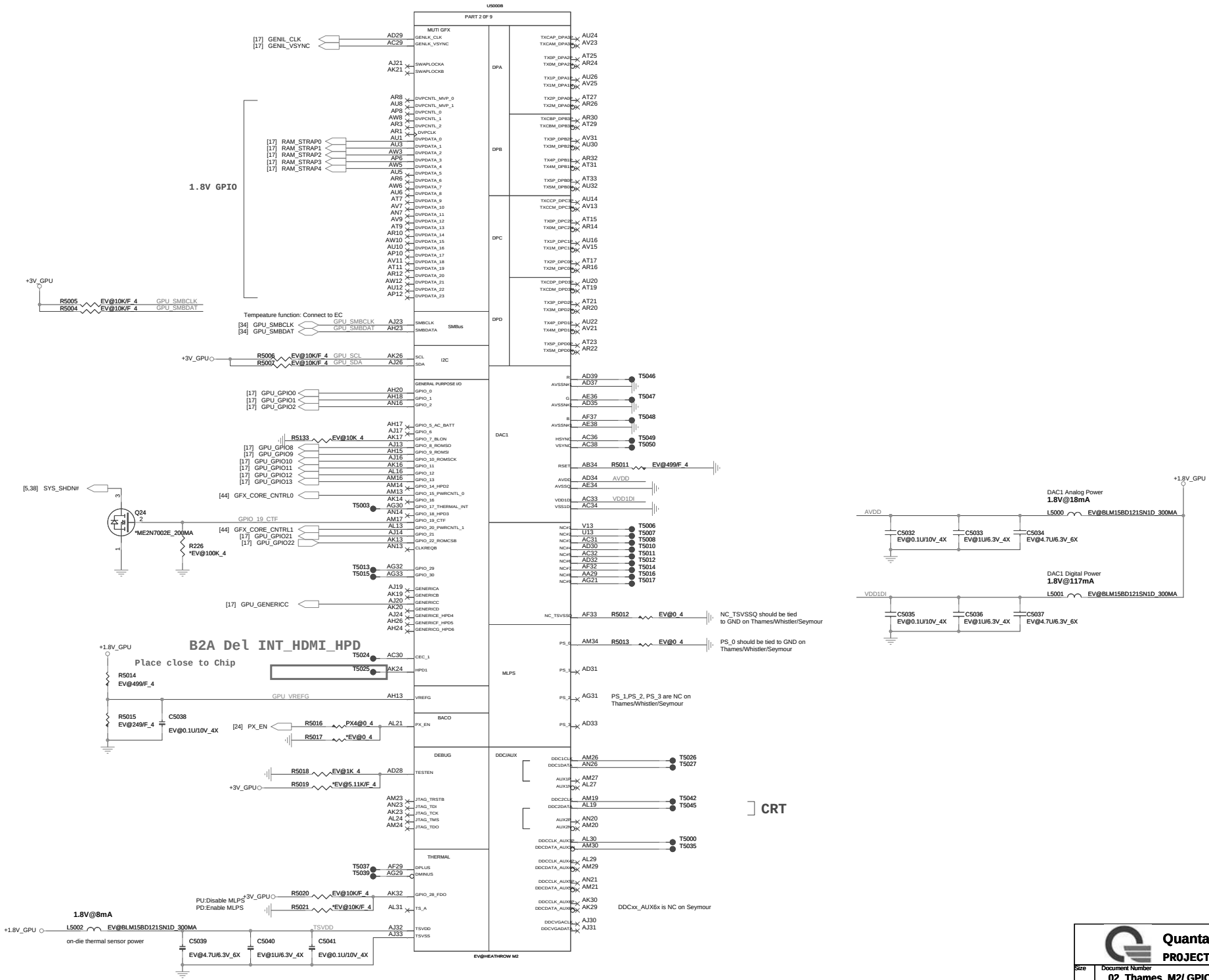
Thames and Seymour Power-on sequence

1 => +1V_GPU
2 => +3V_GPU
3 => +VGPU_CORE,+1.5V_GPU
4 => +1.8V_GPU

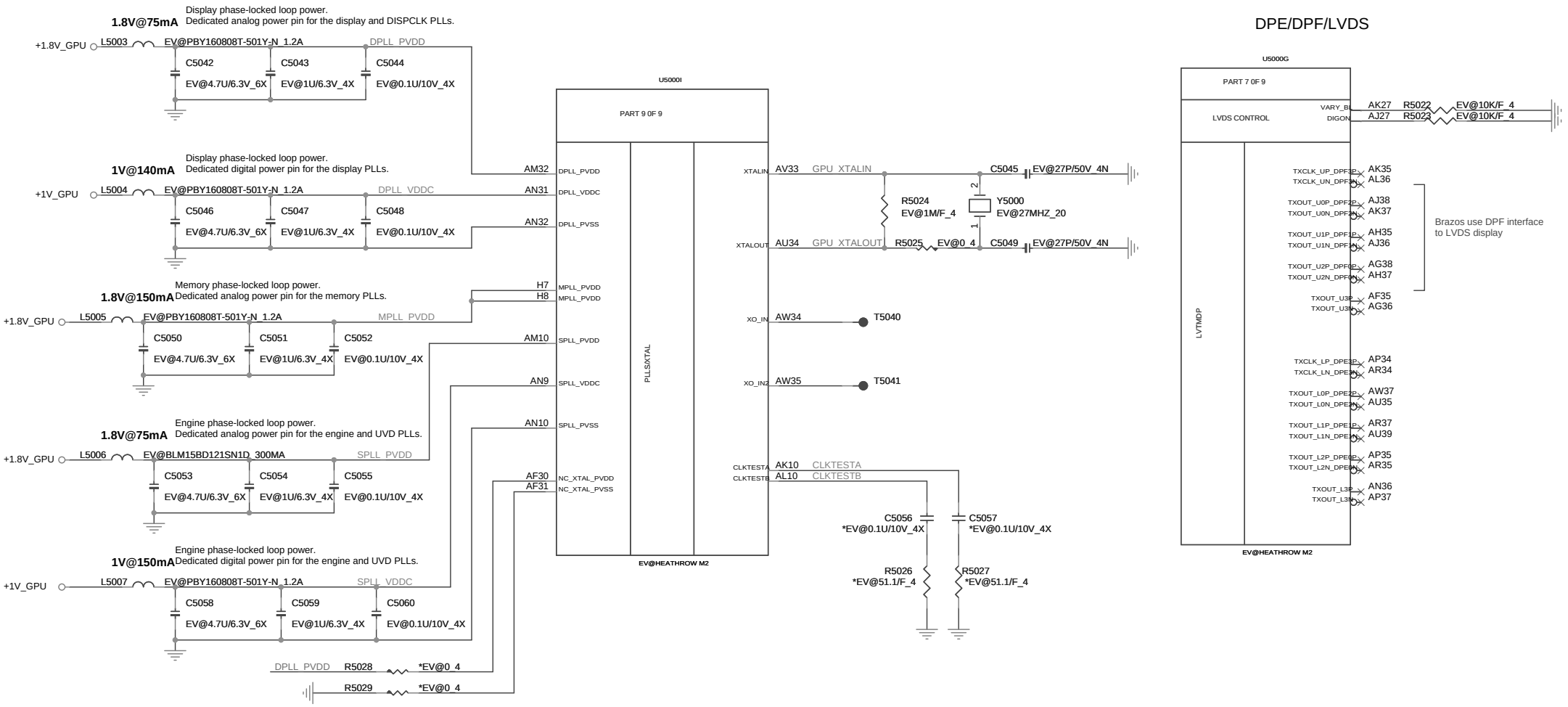
PEG

Intel platform: Lane0 ~ Lane15
Brazos platform: Lane12 ~ Lane15
Comal and Sabine platform: Lane8 ~Lane15

Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: Thames_M2/ PEG*16	Rev: A1A
Date: Monday, February 13, 2012	Sheet 14 of 47	

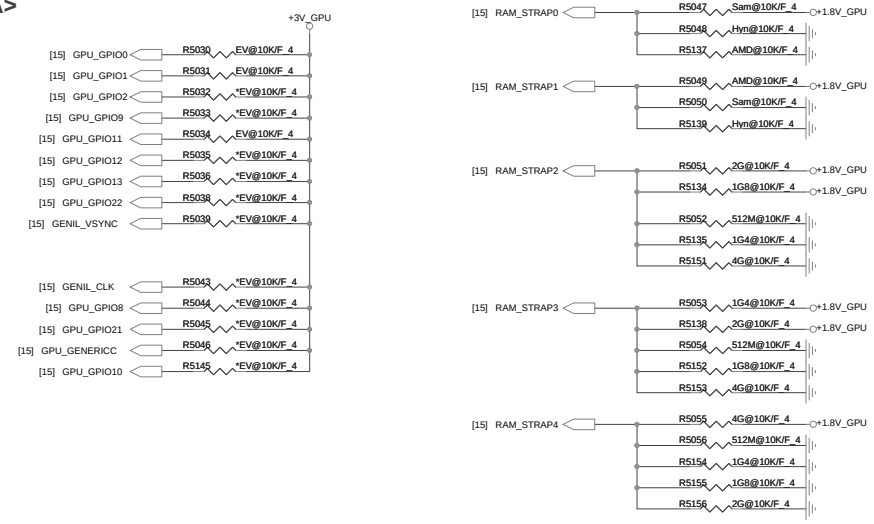


Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: 02_Thames_M2/ GPIO_DP_CRT_I2C	Rev: A1A
Date: Monday, February 13, 2012	Sheet 15 of 47	



Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: Thames_M2/ XTAL_LVDS	Rev: A1A
Date: Monday, February 13, 2012	Sheet 16 of 47	

<VGA>



DDR3 Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP4 DVPDATA_4	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63DFR-11C (64M*16)	AKD5LZWTW02 * 4	512MB	0	0	0	0	0
		AKD5LZWTW02 * 8	1GB	0	0	1	0	0
	H5TQ2G63BFR-11C (128M*16)	AKD5MGWTW00 * 4	1GB	0	1	0	0	0
		AKD5MGWTW00 * 8	2GB	0	1	1	0	0
	H5TQ4G****** (256M*16)	AK********** * 8	4GB	1	0	0	0	0
Samsung	K4W1G1646G-BC11 (64M*16)	AKD5EGGT500 * 4	512MB	0	0	0	0	1
		AKD5EGGT500 * 8	1GB	0	0	1	0	1
	K4W2G1646C-HC11 (128M*16)	AKD5MGWT500 * 4	1GB	0	1	0	0	1
		AKD5MGWT500 * 8	2GB	0	1	1	0	1
	K4W4G****** (256M*16)	AK********** * 8	4GB	1	0	0	0	1
AMD	23EY2387MC11 (64M*16)	AKD5EZWT700 * 4	512MB	0	0	0	1	0
		AKD5EZWT700 * 8	1GB	0	0	1	1	0
	23EY4187MC11 (128M*16)	AKD5DZWT700 * 4	1GB	0	1	0	1	0
		AKD5DZWT700 * 8	2GB	0	1	1	1	0
	23EY********** (256M*16)	AK********** * 4	4GB	1	0	0	1	0

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	GENLK_CLK	Reserved	0
RESERVED	PS_1[2]	GPIO8	Reserved	0
RESERVED	NA	GPIO21	Reserved	0
RESERVED	NA	GENERICC	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

System Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1

EEPROM

Quanta Computer Inc.
PROJECT : BY6/BY6D

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	Thames_M2/ STRAPS_Thermal	A1A

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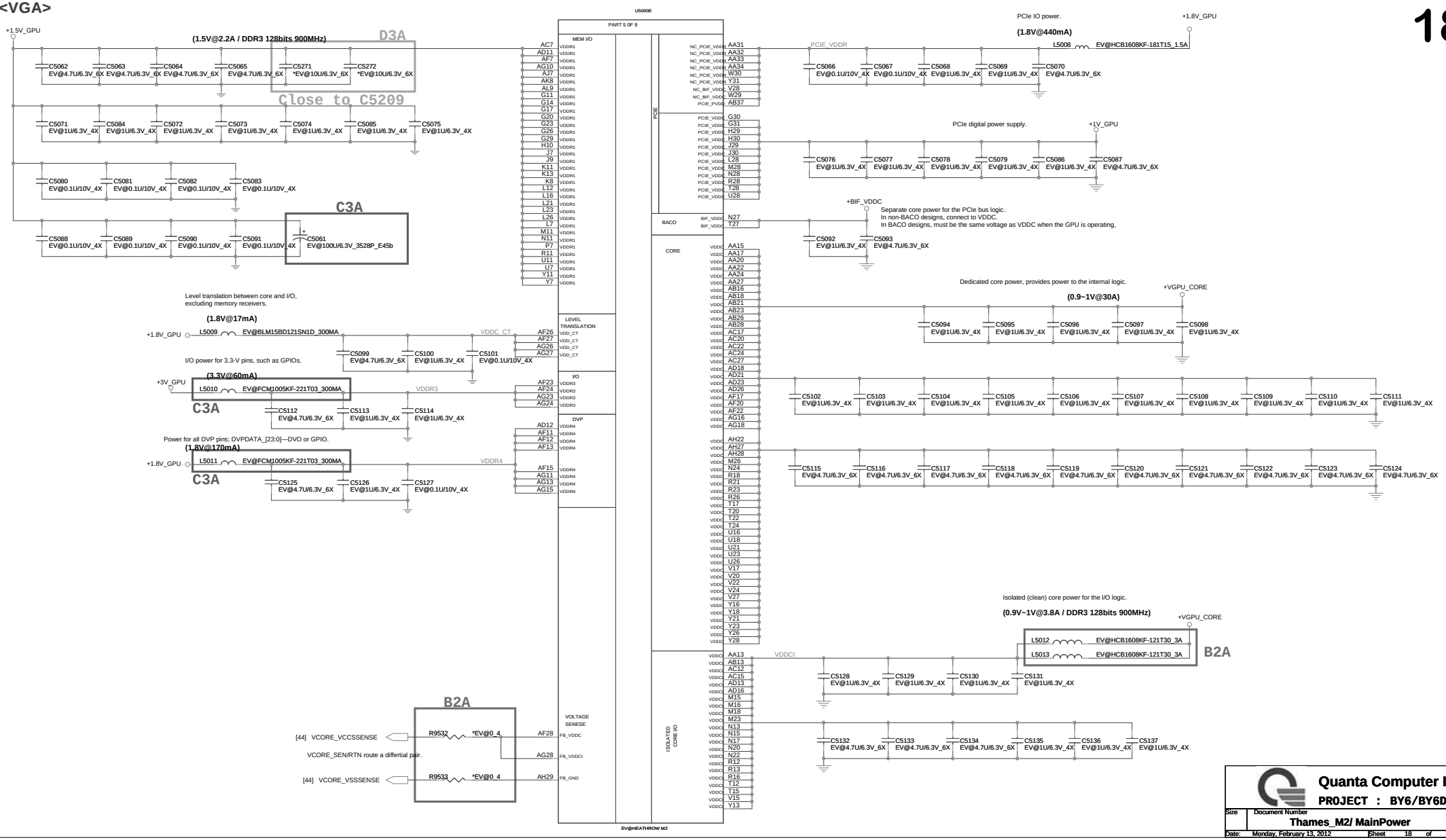
<VGA>



Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: Thames_M2/ MainPower	Rev: A1A
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<VGA>

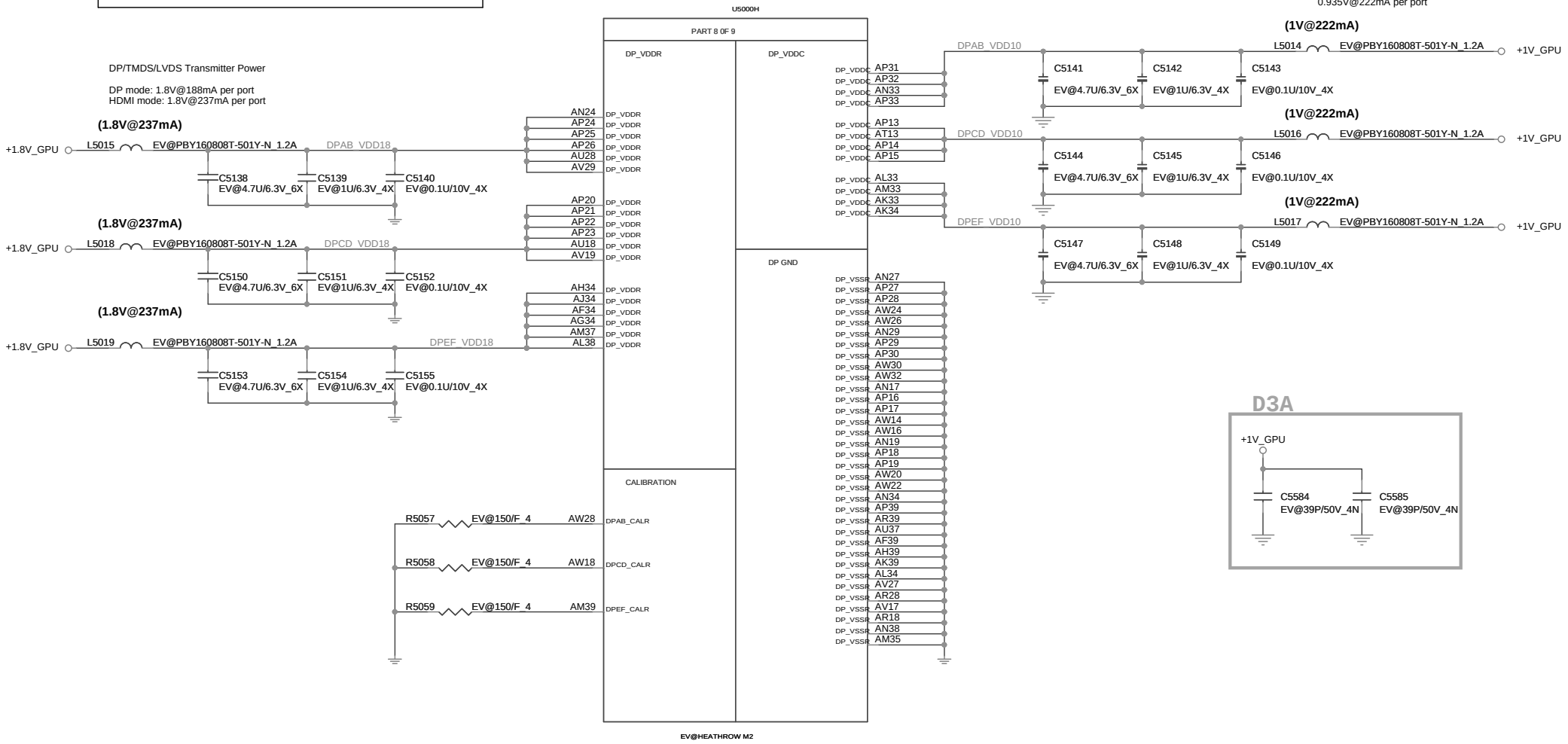
For Thames/Whistler/Seymour
a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames/Whistler/Seymour
a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

DP/TMDS/LVDS Transmitter Power

DP mode: 1.8V@188mA per port
HDMI mode: 1.8V@237mA per port



Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: Thames_M2/ DP_Powers	Rev: A1A
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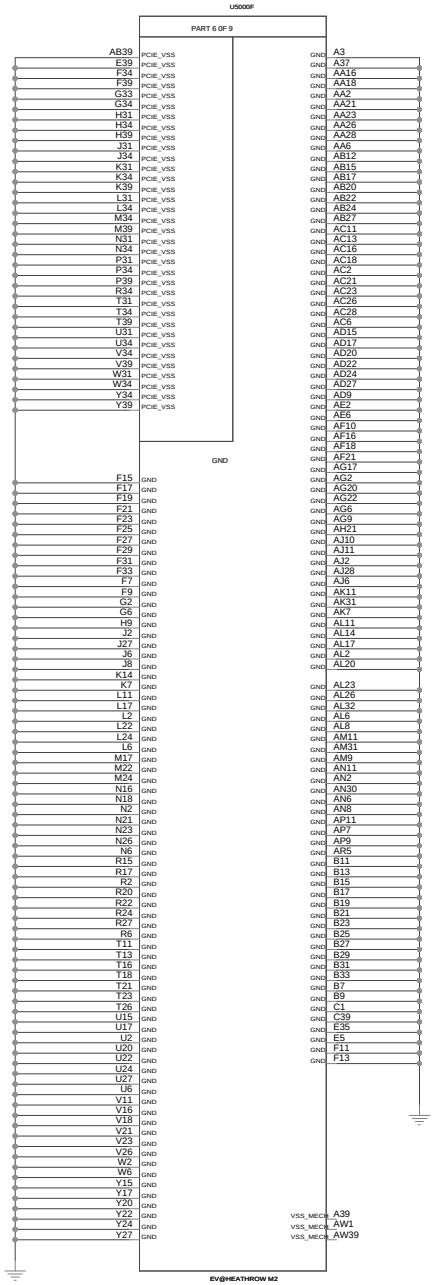

Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: Thames_M2/ GND	Rev: A1A
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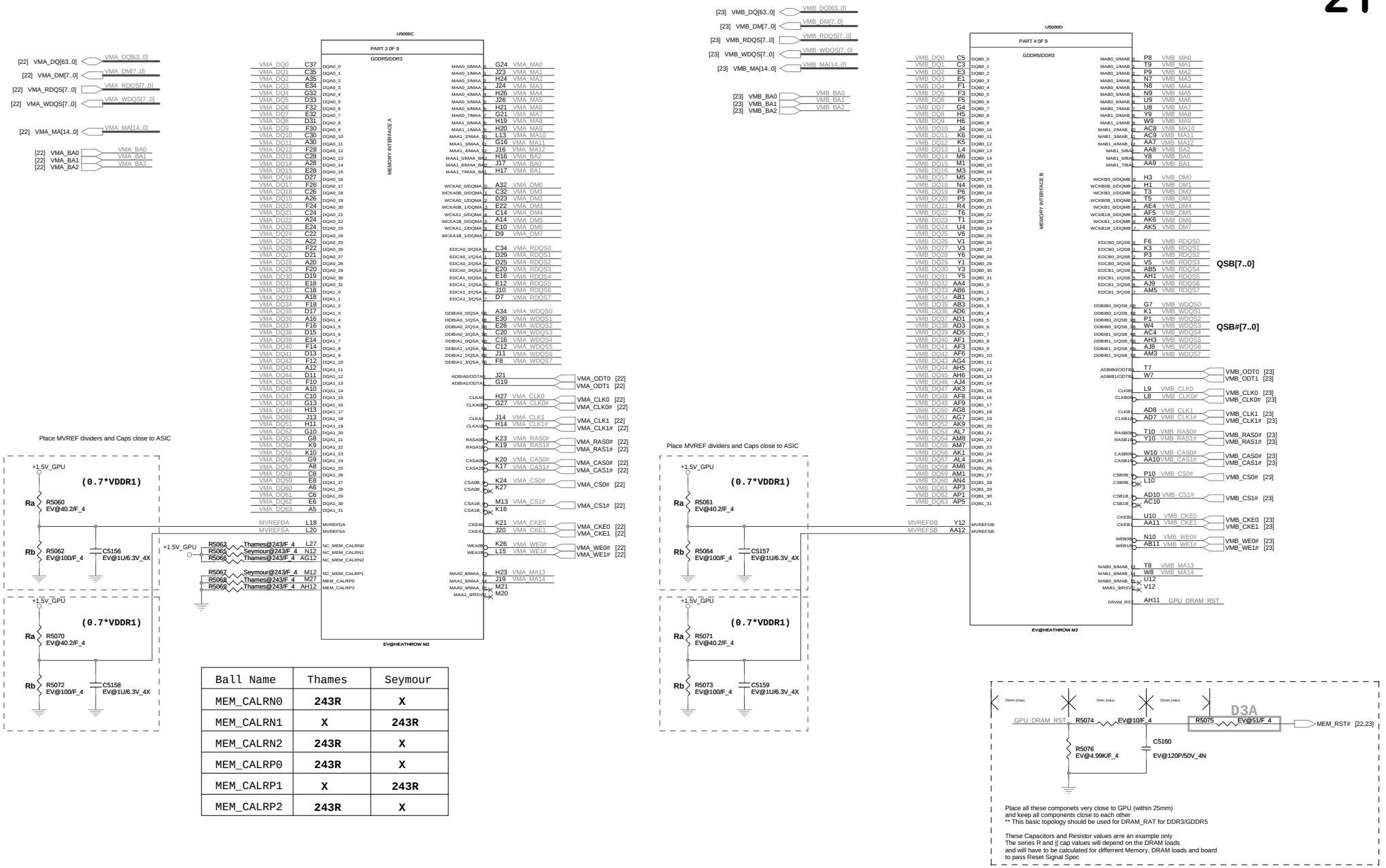
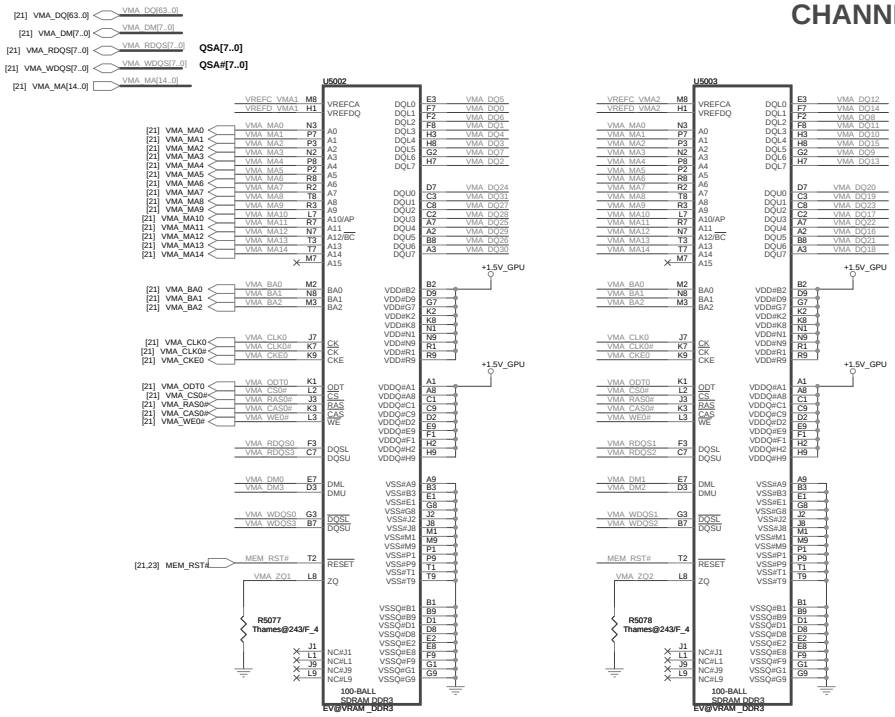


Ball Name	Thames	Seymour
MEM_CALRN0	**243R**	**X**
MEM_CALRN1	**X**	**243R**
MEM_CALRN2	**243R**	**X**
MEM_CALRP0	**243R**	**X**
MEM_CALRP1	**X**	**243R**
MEM_CALRP2	**243R**	**X**

Place all these componets very close to GPU (within 25mm)
and keep all components close to each other
** This basic topology should be used for DRAM_RAT for DDR3/GDDR5

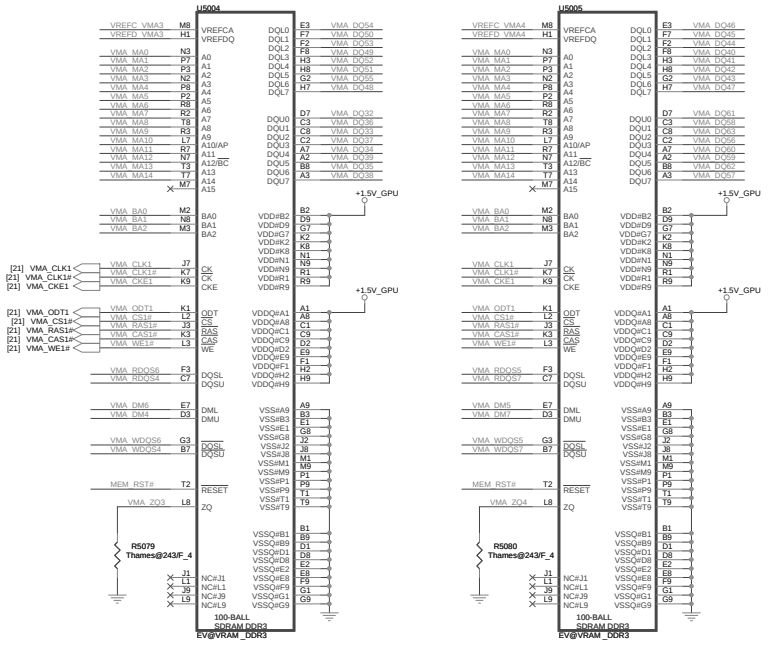
These Capacitors and Resistor values arre an example only
The series R and || cap values will depend on the DRAM loads
and will have to be calculated for differrent Memory, DRAM loads and board
to pass Reset Signal Spec

CHANNEL A: 512MB DDR3 (64M*16*4pcs) <VGA>



TOP Left

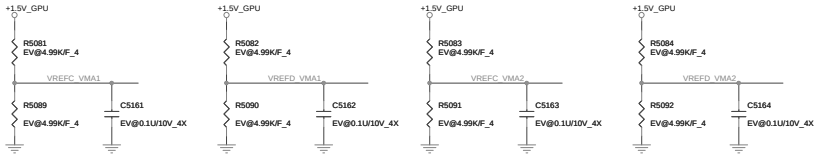
BOT Left



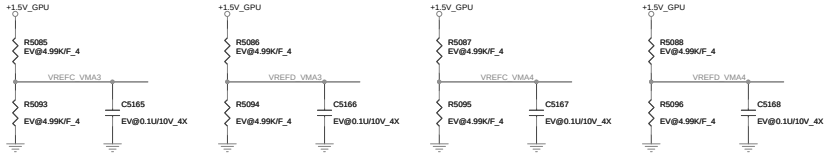
BOT Right

TOP Right

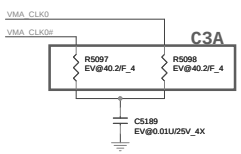
Group-A0 VREF



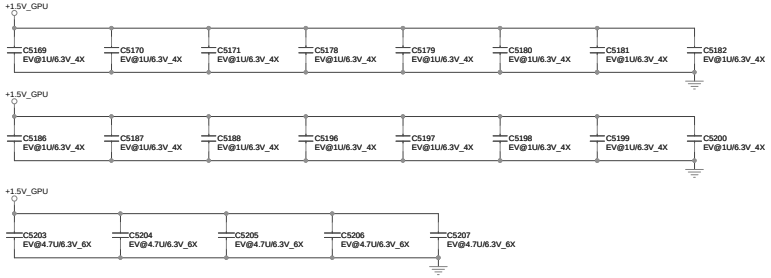
Group-A1 VREF



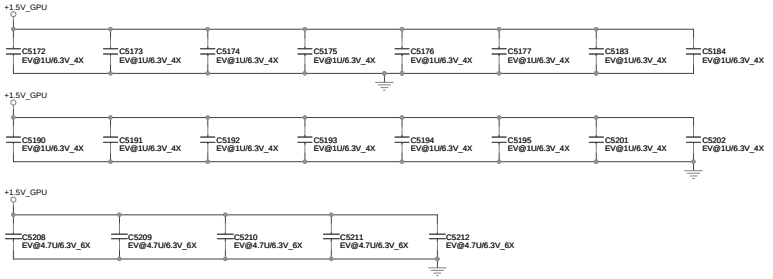
MEM_A0 CLK



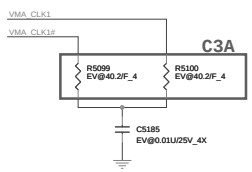
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



Quanta Computer Inc.

PROJECT : BY6/BY6D

Size	Document Number	Rev
	VRAM_A: DDR3*4PCS	A1A

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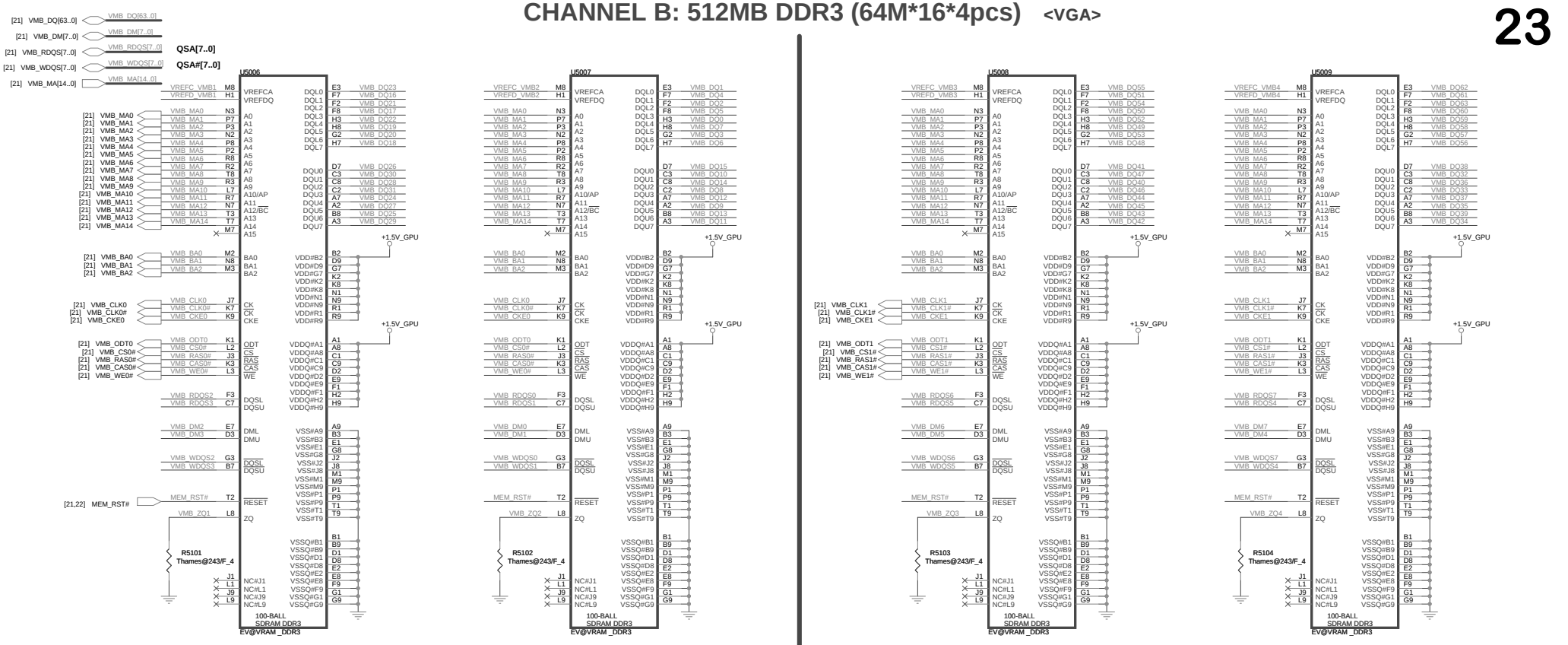
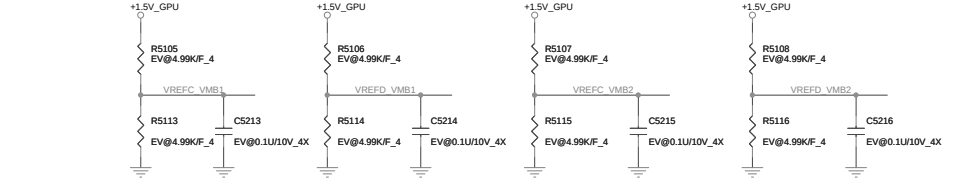
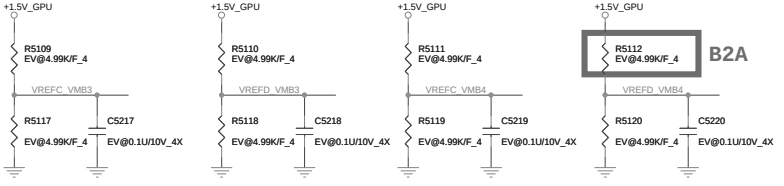
CHANNEL B: 512MB DDR3 (64M*16*4pcs) <VGA>



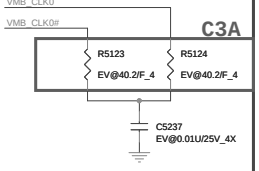
Group-B0 VREF



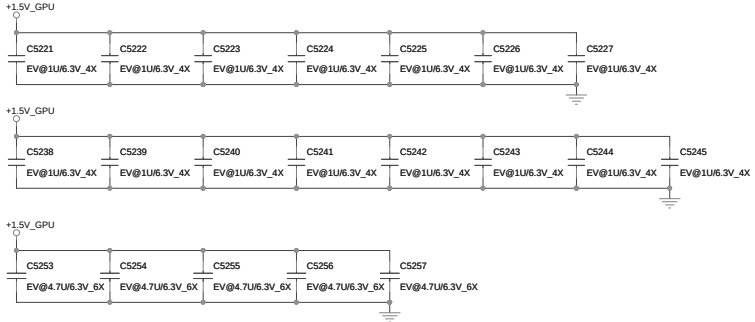
Group-B1 VREF



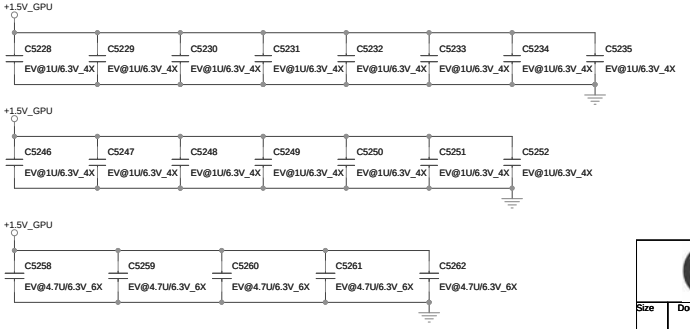
MEM_B0 CLK



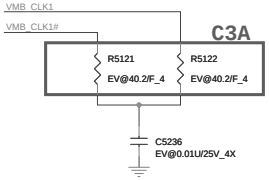
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.

PROJECT : BY6/BY6D

Size	Document Number	Rev
	VRAM_B: DDR3*4PCS	A1A
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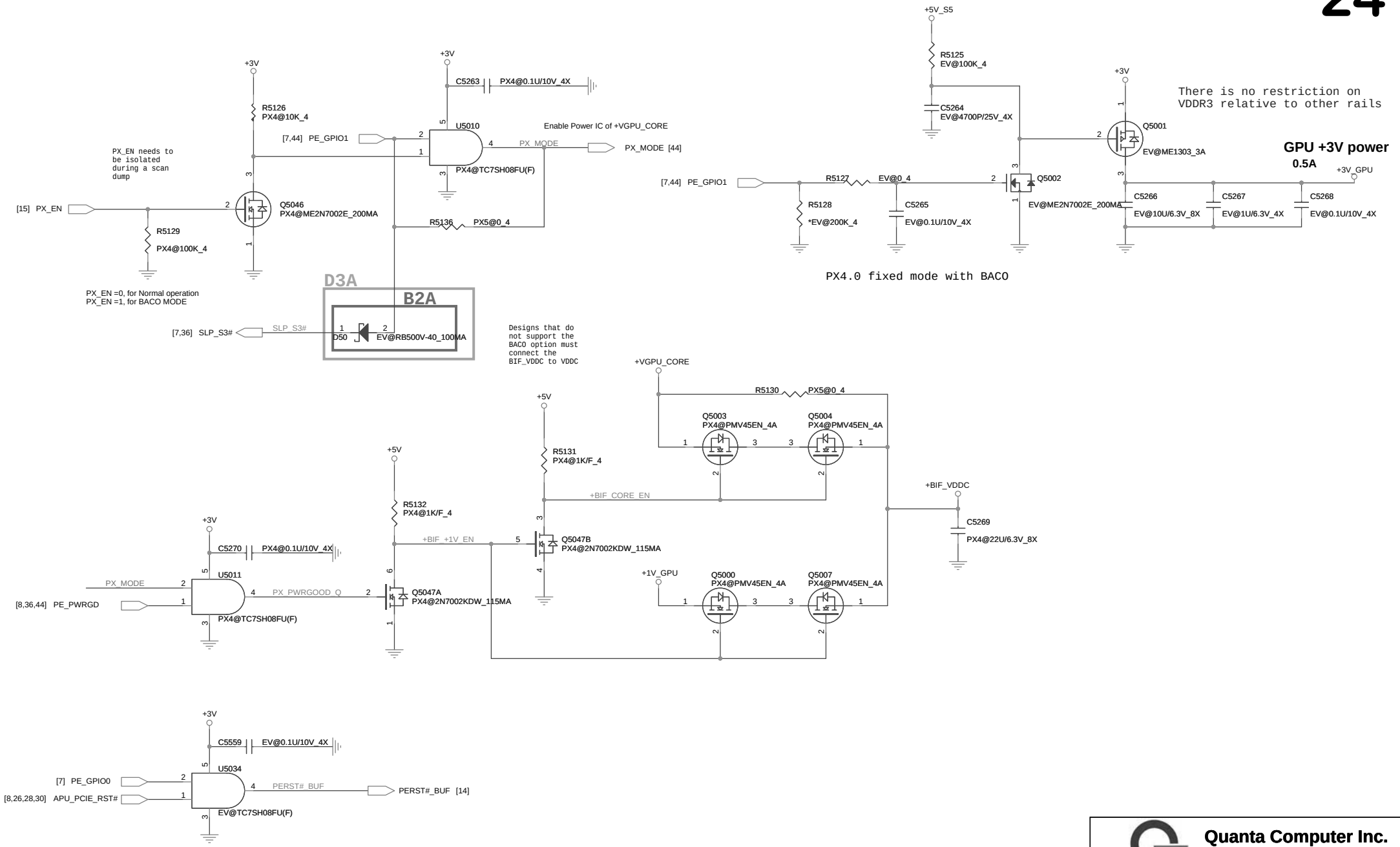

Quanta Computer Inc.		
PROJECT : BY6/BY6D		
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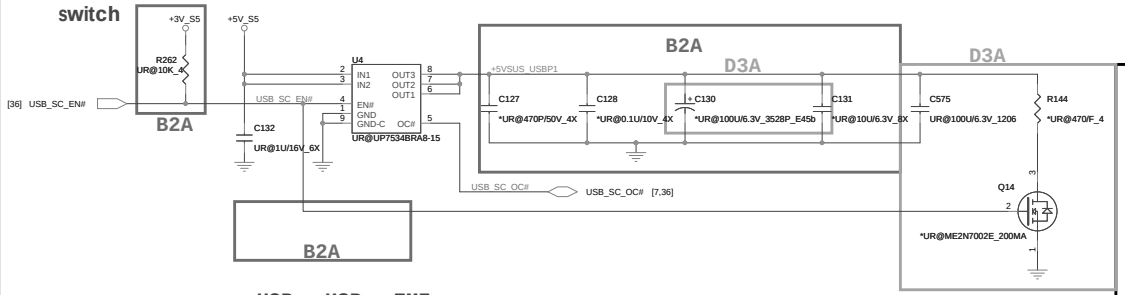
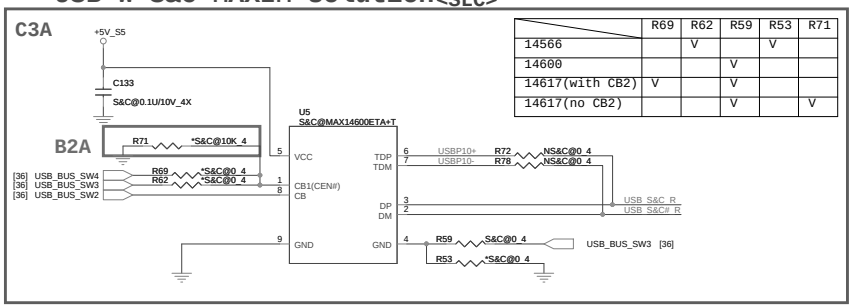
USB 3.0 Power switch

<USB> <U3B>



USB w S&C MAXIM solution<SLC>



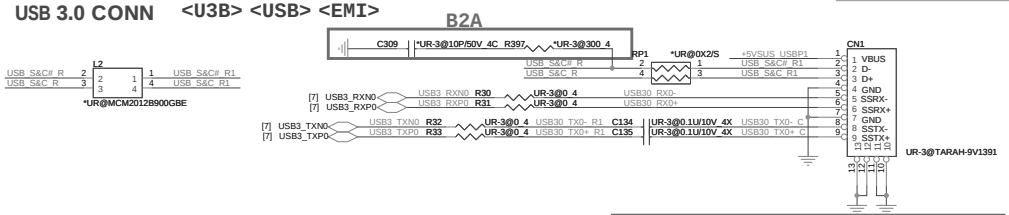
	R69	R62	R59	R53	R71
14566		V		V	
14600			V		
14617(with CB2)	V		V		
14617(no CB2)			V		V

CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

CB0	CB1	CB2	Status
X	X	1	Force Apple 2A Charger Mode
0	0	0	Autodetection charger mode
0	1	0	Force-Dedicated Charger Mode
1	0	0	USB Pass-Through Mode Connect DP/DM to TDP/TDM
1	1	0	USB Pass-Through Mode with CDP Emulation.Auto connect DP/DM to TDP/TDM depending on CDP status

USB 3.0 CONN

<U3B> <USB> <EMI>



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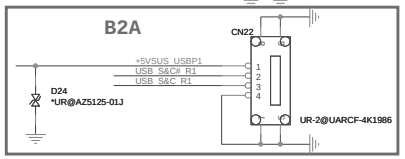

USB3.0 UR-3@TARAH-9V1391
USB2.0 UR-2@UARCF-4K1986

USB 3.0 CONN

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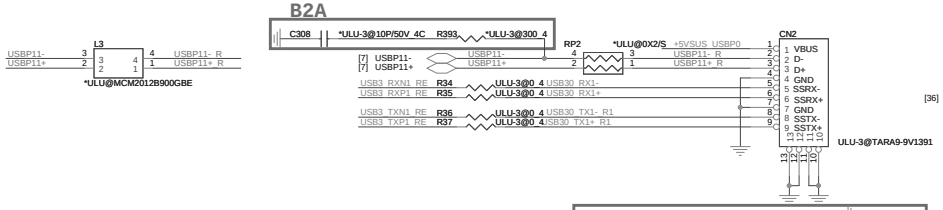
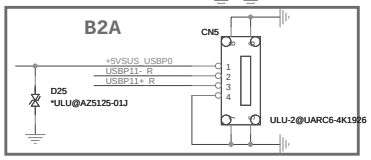
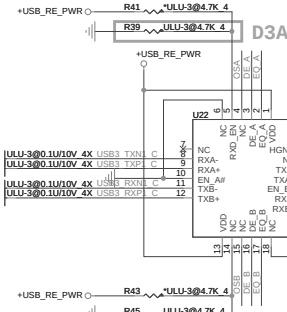
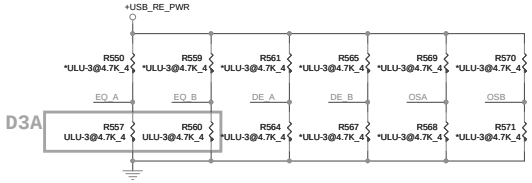
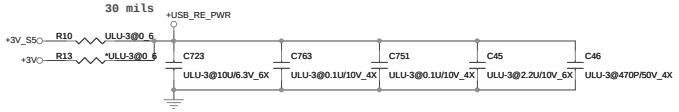


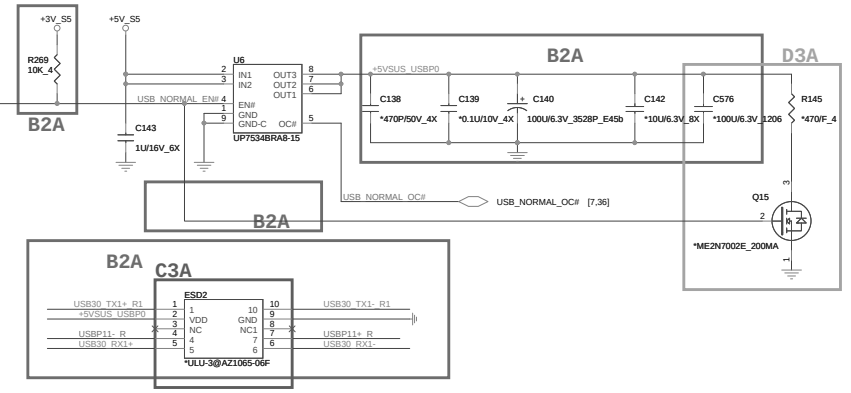


USB3.0 DFHS09FR085 ULU-3@TARA9-9V1391
USB2.0 DFHS04FR487 ULU-2@UARC6-4K1926

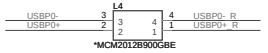


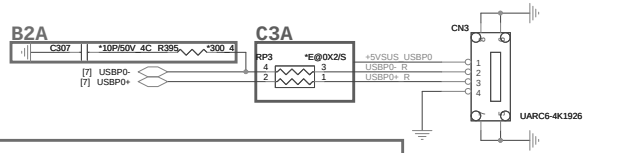


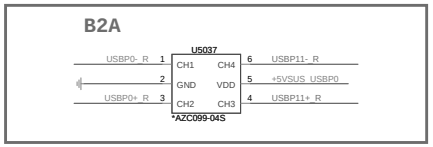




USB 2.0 CONN







Quanta Computer Inc.
PROJECT : BY6/BY6D

Size	Document Number	Rev
	USB2.0/USB3.0	1A

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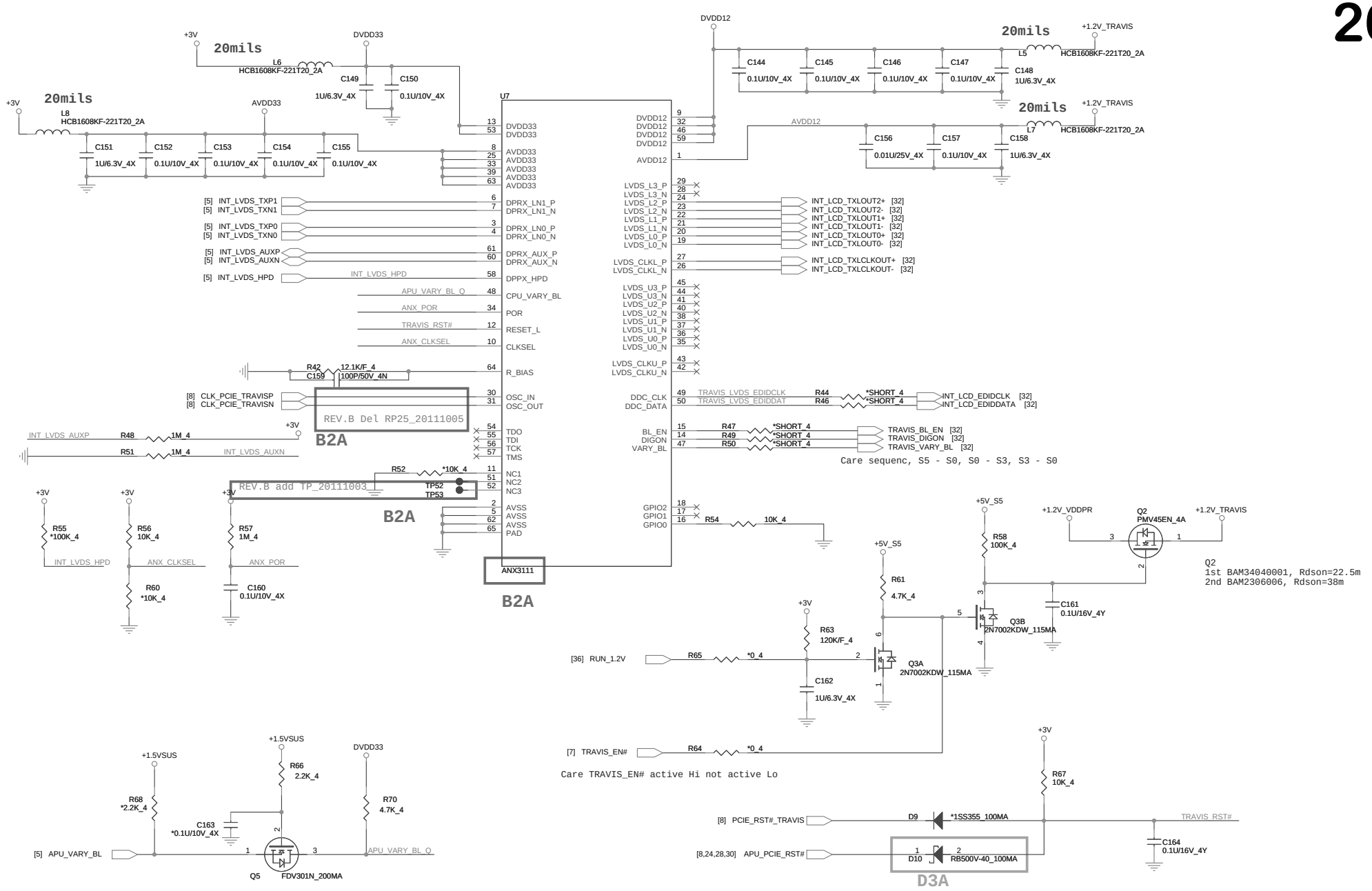

Quanta Computer Inc.		
PROJECT : BY6/BY6D		
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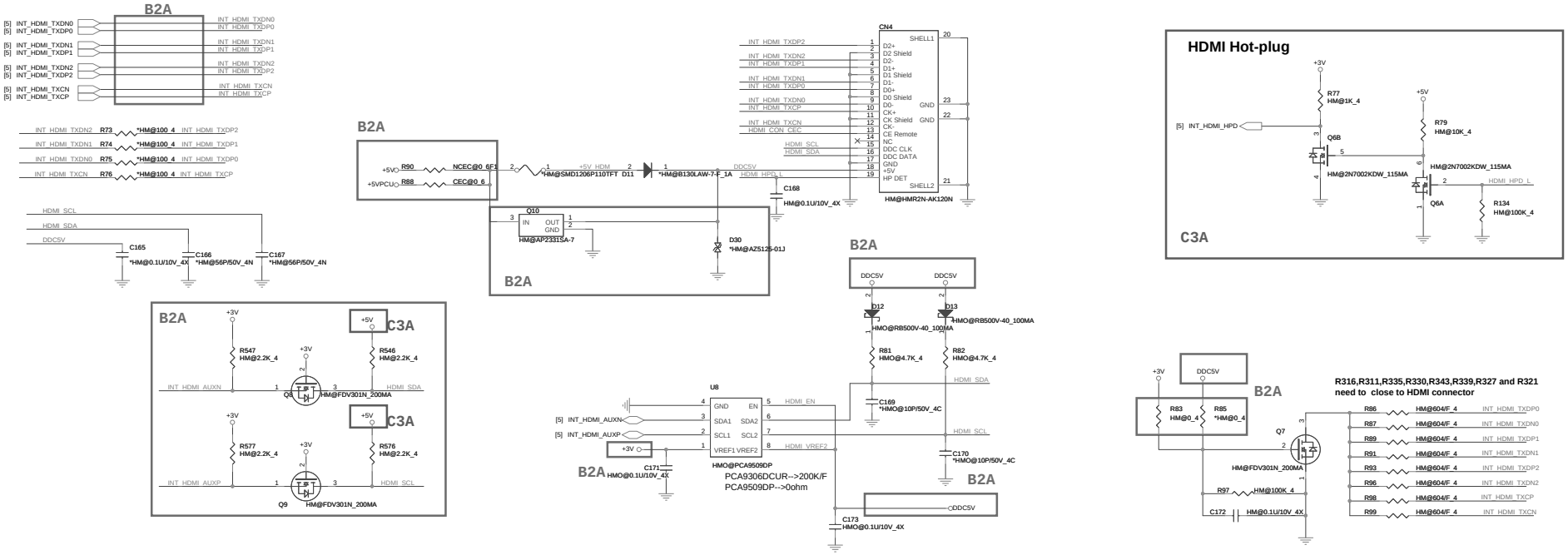
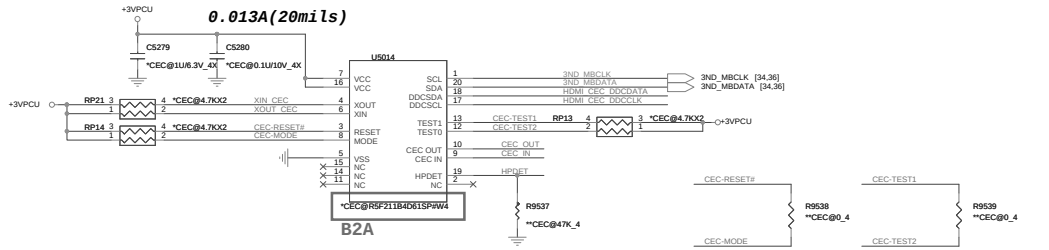
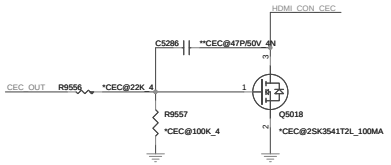
HDMI



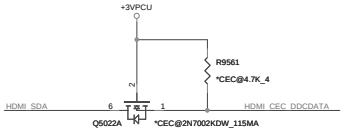
HDMI CEC <CEC>



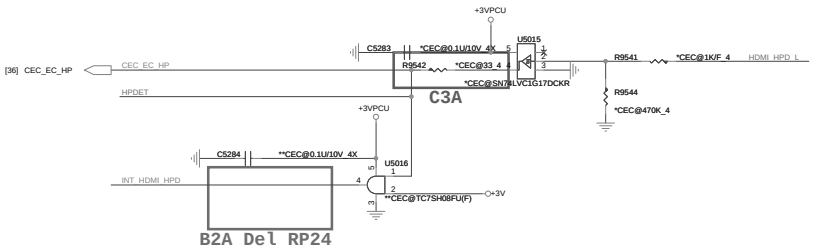
CEC Output <CEC> (To Connect)



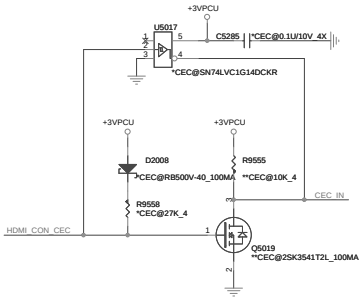
CEC SMBus Level Shift <CEC> (To CECC)



CEC HotPlug <CEC>



CEC Input <CEC> (To CECC)



Quanta Computer Inc.		
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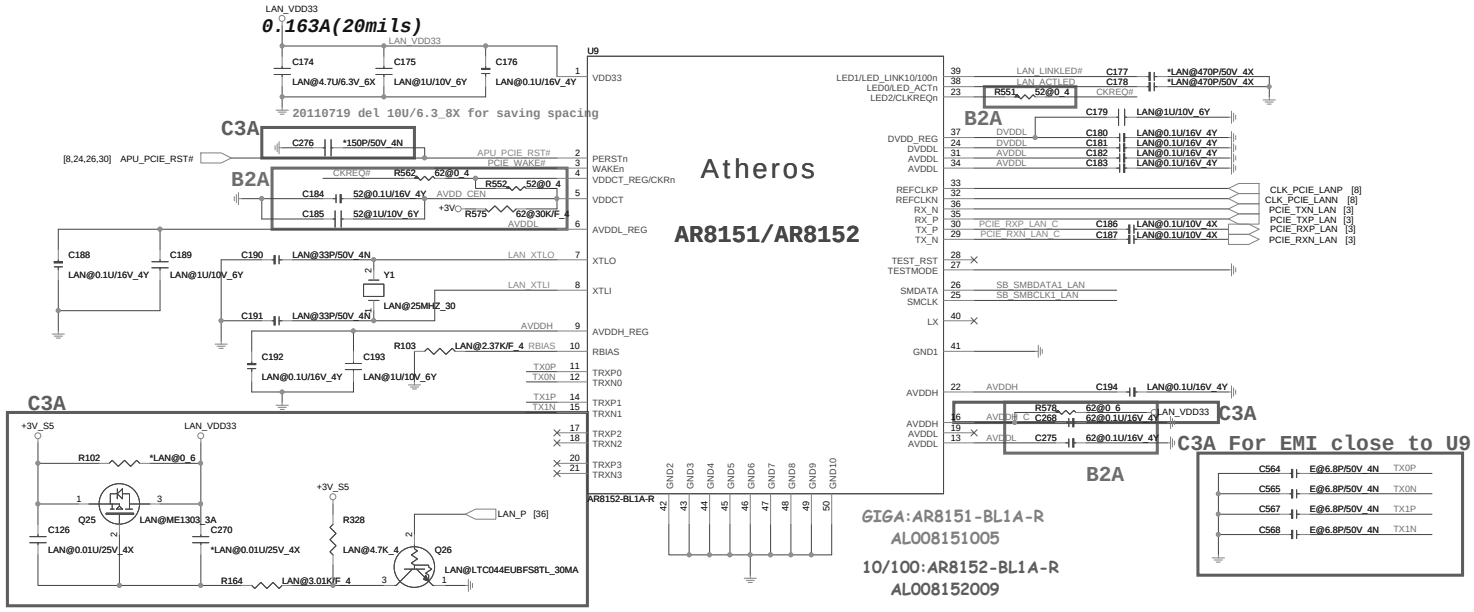
Atheros Lan <LAN> <LNG>



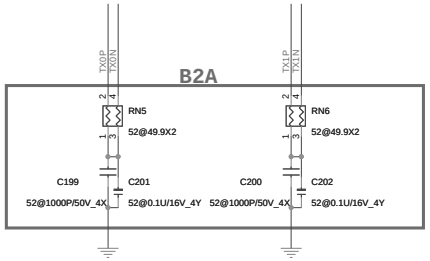
<LAN> <LNG> <LN1>

LAN-Wake up function <LAN>

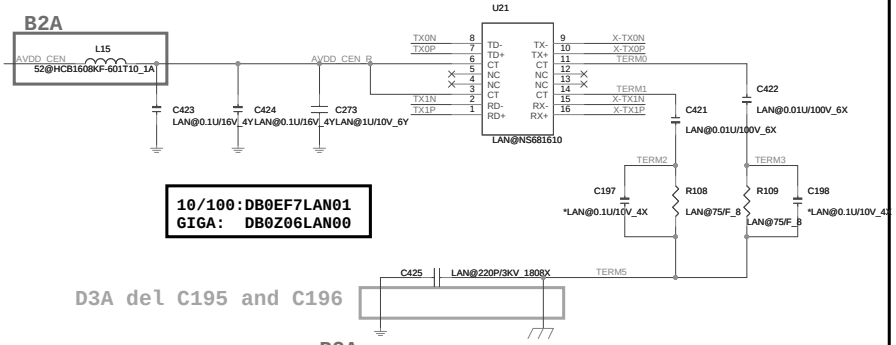
LAN-SM-Bus <LAN>

20110801 add SMbus for LAN

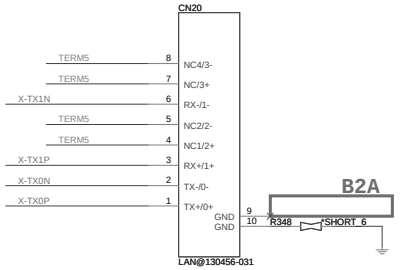
PLACE NEAR LAN IC SIDE <LAN> <LNG>



TRANSFORMER CONN <LAN> <LNG>



RJ45 <LAN> <LNG> <LN1>



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Power on Strapping pin

LAN_ACTLED R110 LAN@5.1K/F_6

LAN_LINKLED# R111 LAN@5.1K/F_6

Quanta Computer Inc.
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Size	Document Number	Rev
	ATHEROS LAN (AR8152B)	1A
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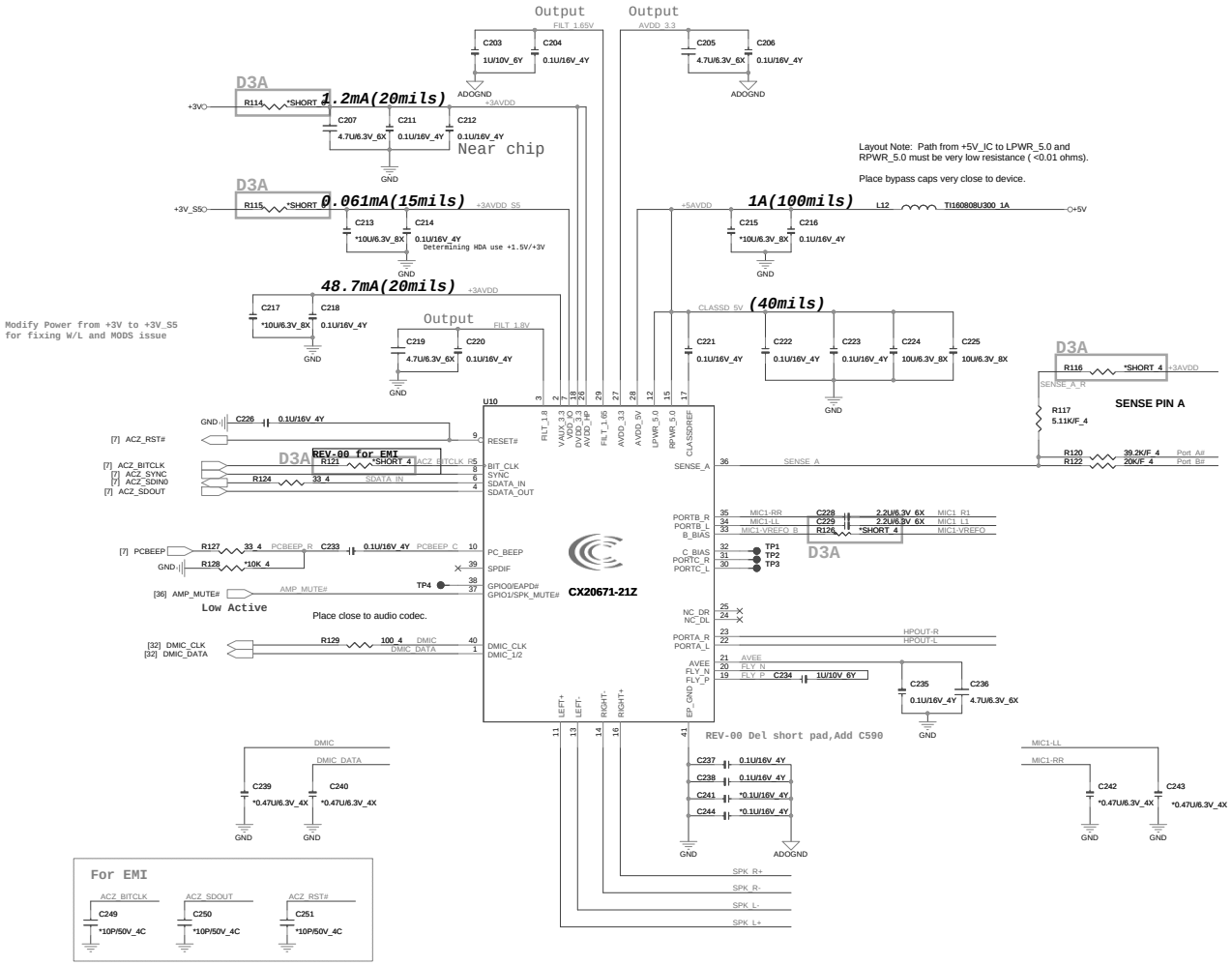
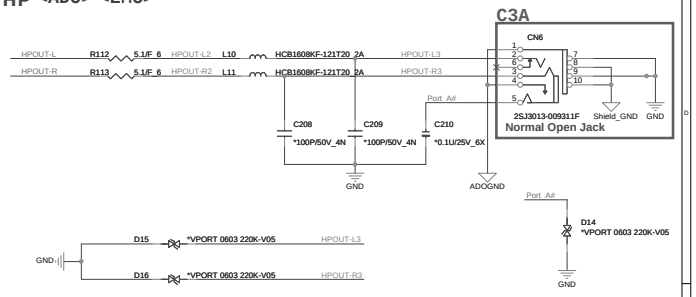
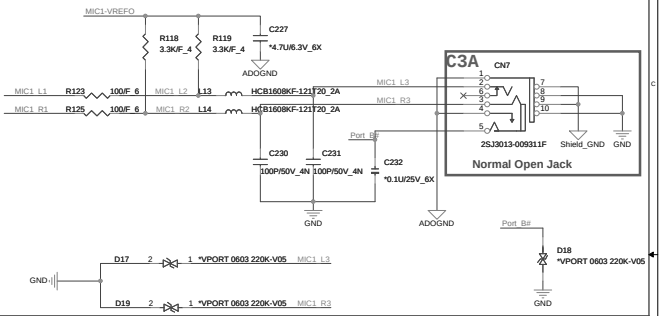
Codec (CX20671-21Z) <ADO> <EMI>



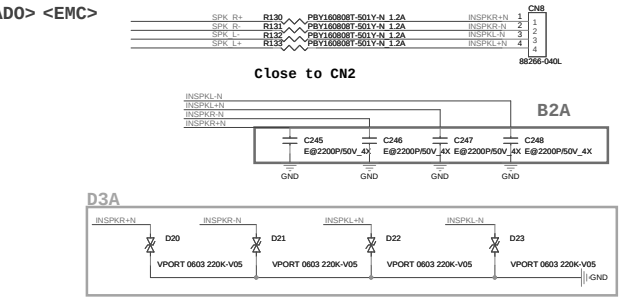
HP <ADO> <EMC>



External MIC <ADO> <EMC>



Internal Speaker <ADO> <EMC>



Quanta Computer Inc.		
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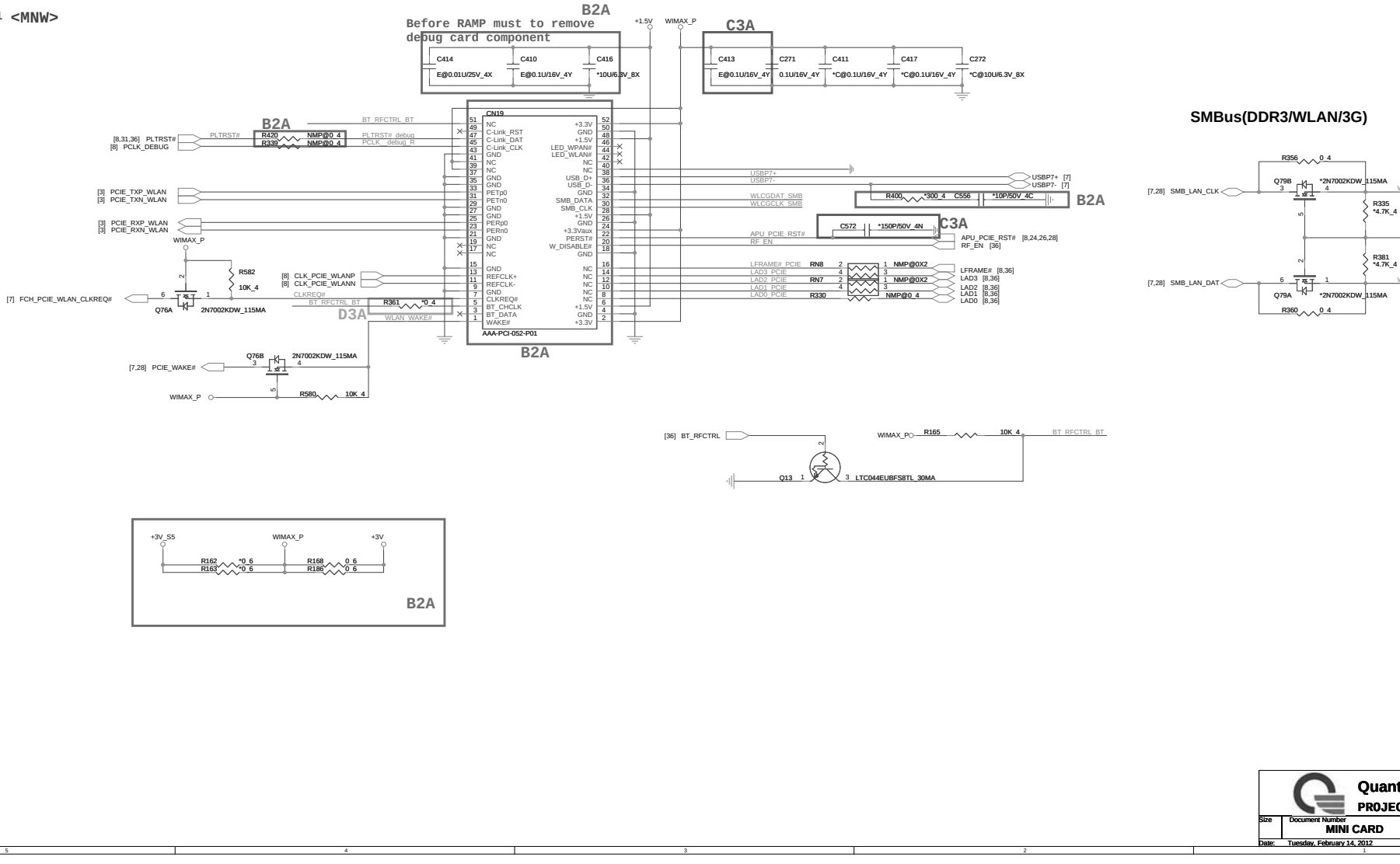
MINI Card Slot#1 <MNW>
(WiFi)

Before RAMP must to remove debug card component



SMBus(DDR3/WLAN/3G)

Quanta Computer Inc.			
PROJECT : BY6/BY6D			
Size	Document Number: MINI CARD		Rev: 1A
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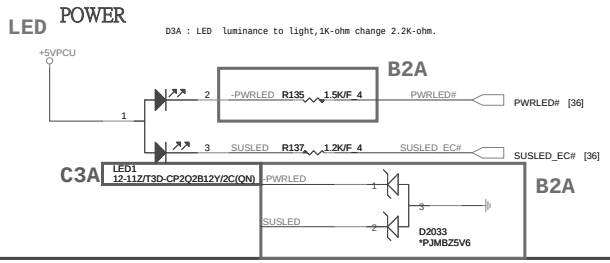
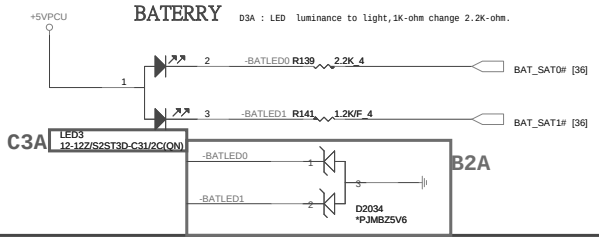
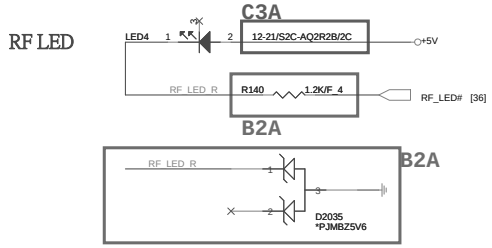
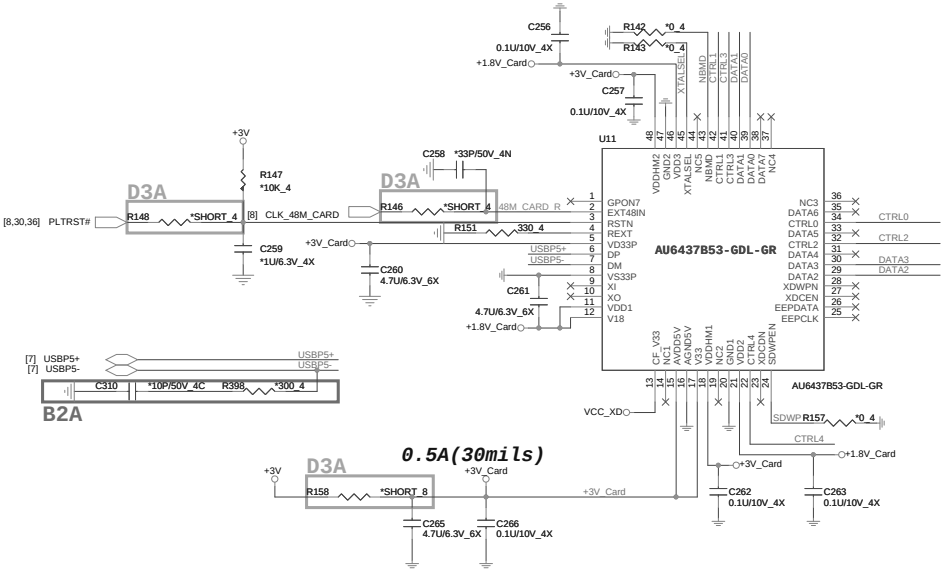






3 IN 1 CARD READER (Type: MS/MMC/SD) <MMC>

Card Reader (AU6437B53-GDL-GR)



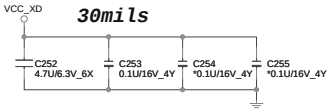
Clock input selection
1 : 48MHz input (default)
0 : 12MHz input

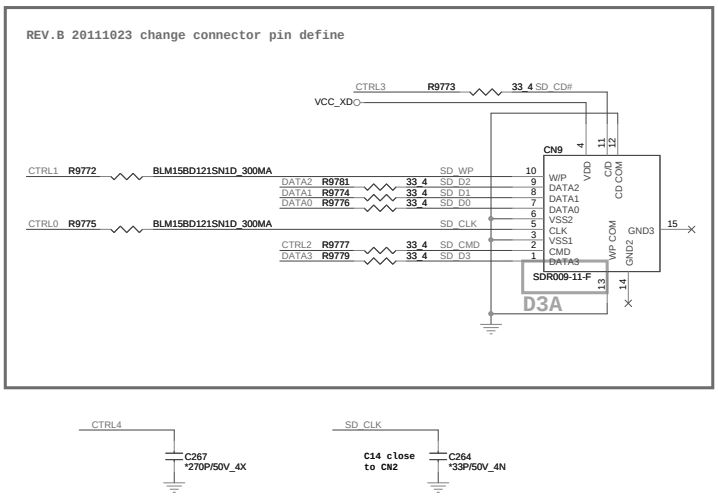
NBMD Power saving mode enable
1 : enable (default)
0 : disable

CTRL0 trace surround with GND

	SD	XD	MS
CTRL0	SDCLK	XDALE	MSBS
CTRL1	SDWP	XDCLE	MSCLK
CTRL2	SDCMD	XDRBD	
CTRL3	SDCDN	XDWRN	
CTRL4		XDRDN	MSINS

SD write protect enable
1 : decided by SDWP(default)
0 : SD always write-able





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	CARD READER/LED		1A
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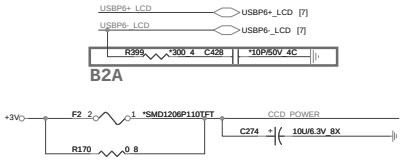
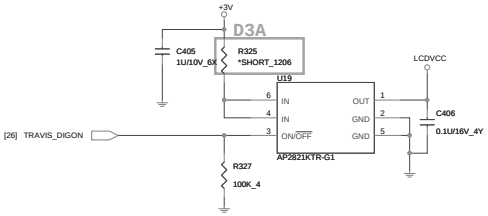
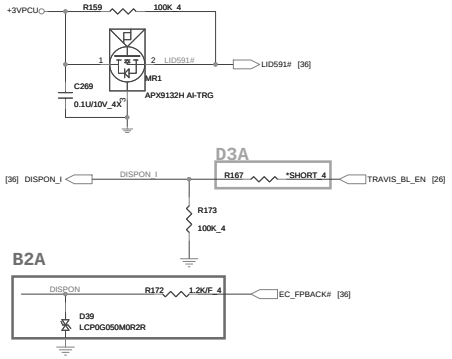
CCD [CCD]



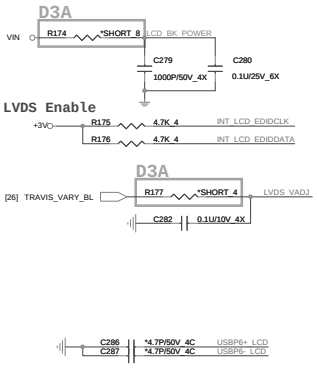
LCD POWER SWITCH <LDS>

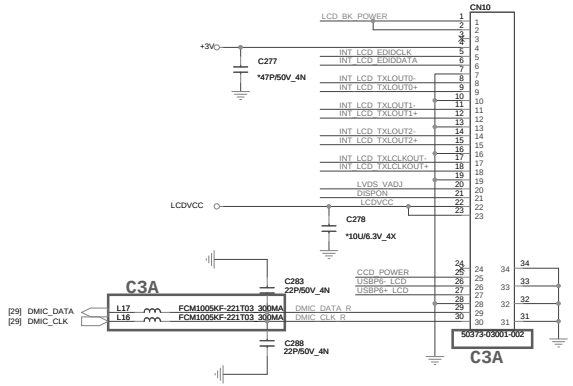


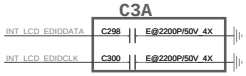
HALL SENSOR&BACK LIGHT SWITCH <HSR>

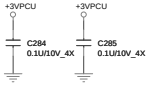


LCD Panel Module [LDS]

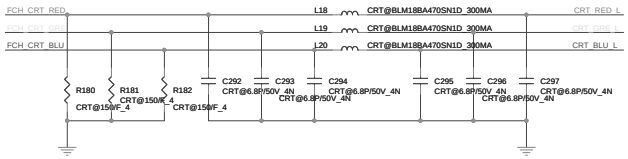


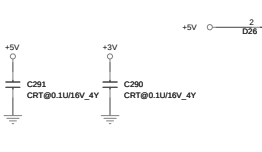


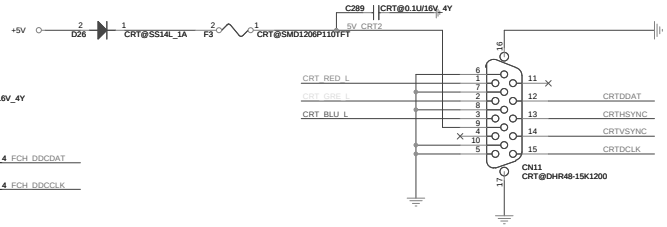


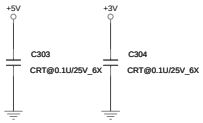


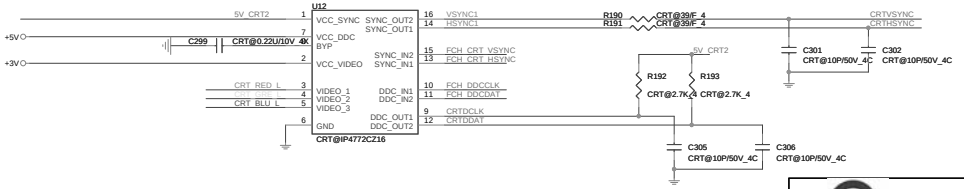
CRT [CRT]











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	LVDS/CCD/DRT	1A

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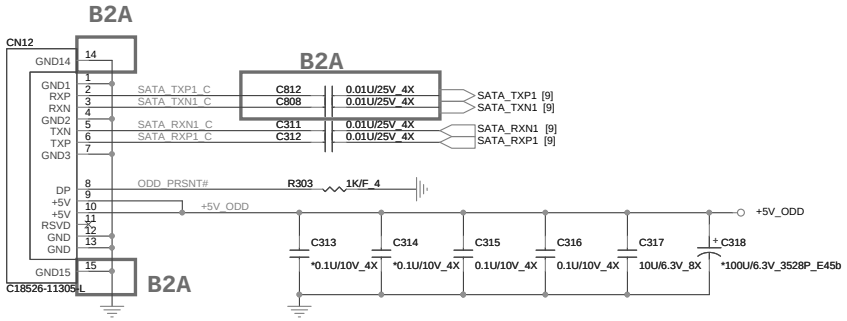
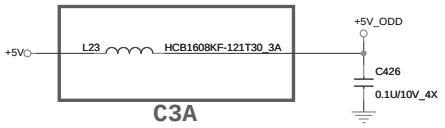
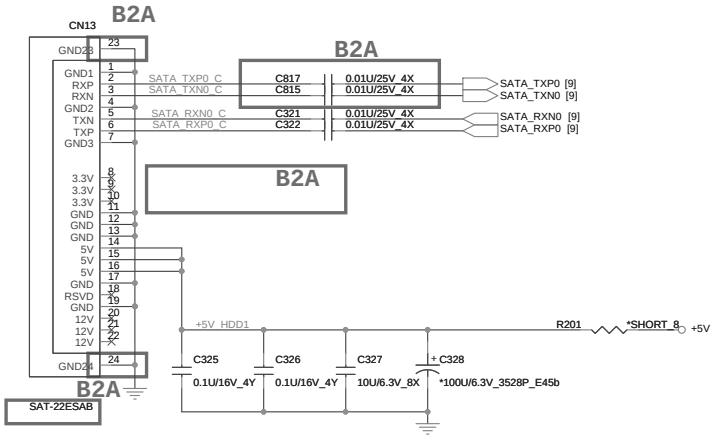
SATA ODD [ODD]





SATA HDD [HDD]



Quanta Computer Inc.
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	HDD/ODD	1A

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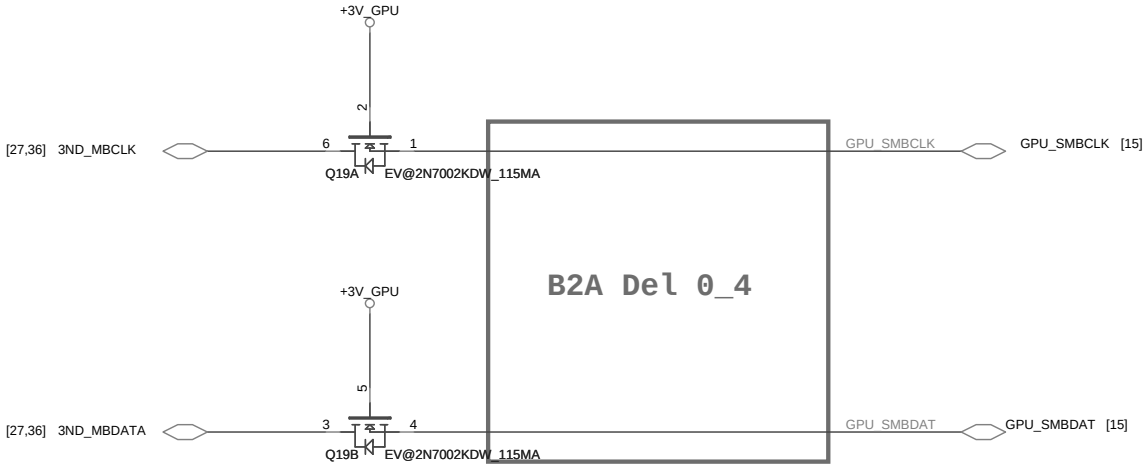
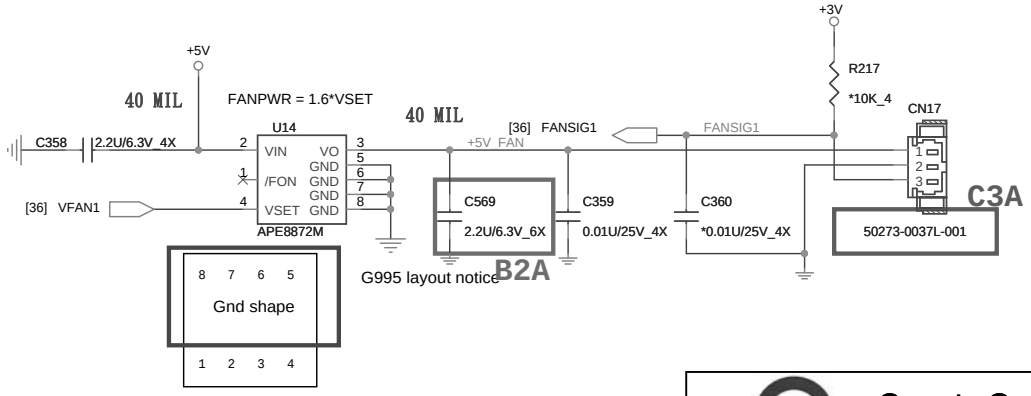
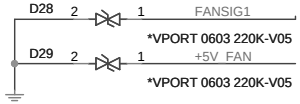
Thermal Sensor <THC>



Thermal	Ext Thermal	dGPU Int Thermal
EC(M) 3ND_SMB	U13	
EC(M) 3ND_SMB		dGPU int SMBUS
dGPU(M) SMB	U13	dGPU int SMBUS

FAN Control <THC>





Quanta Computer Inc.

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	THERMAL	1A

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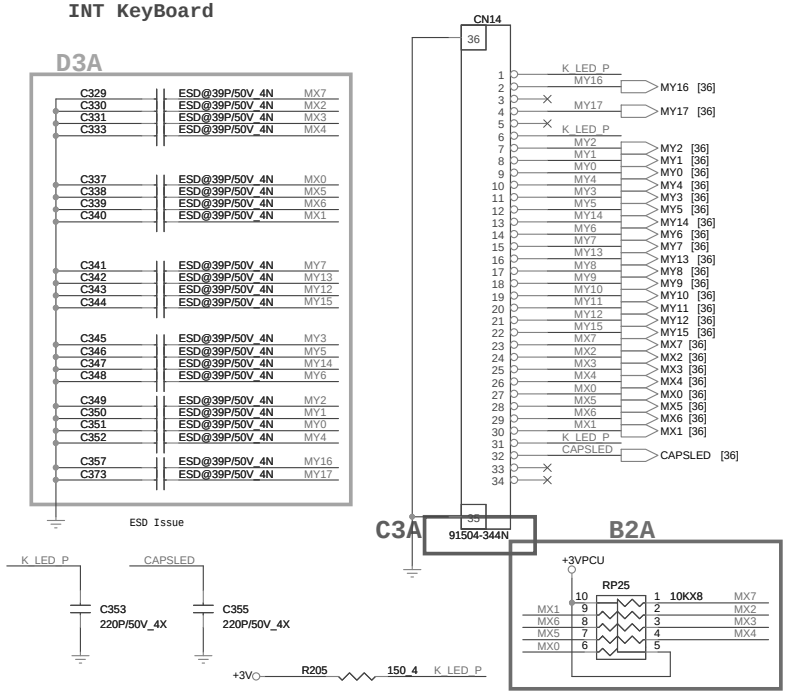
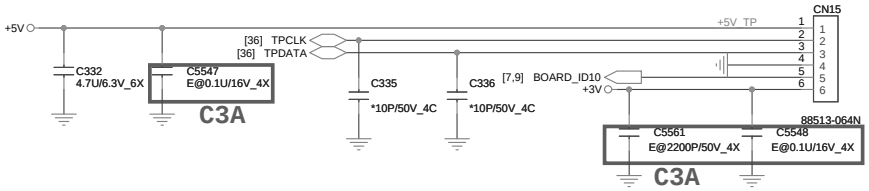
KEY BOARD Connector <KBC> <EMI>

INT KeyBoard



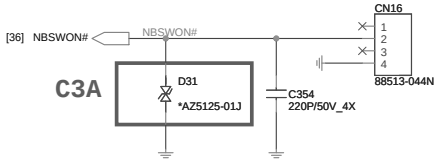
TOUCH PAD BOARD <TPD> <EMI>



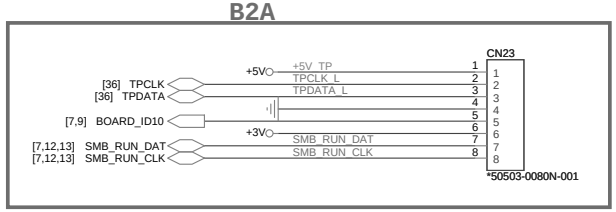
ID_Detect	default
Metal/IMR	H
TEXTURE	L

35

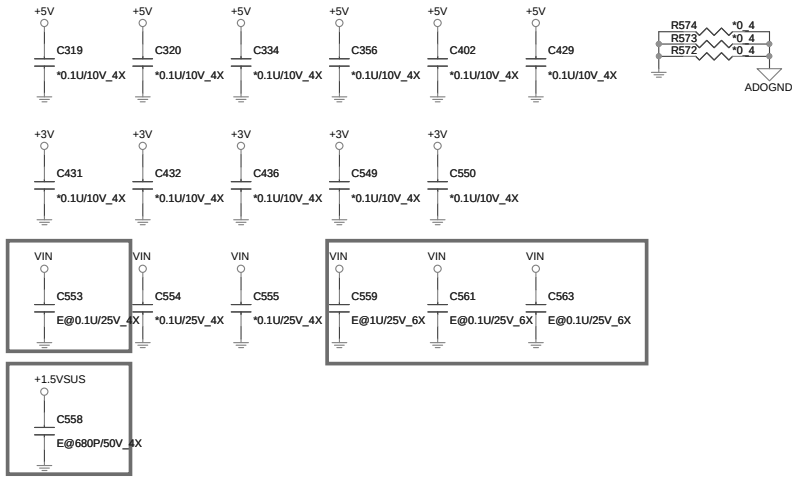
Power Board (UIF) <PSW>



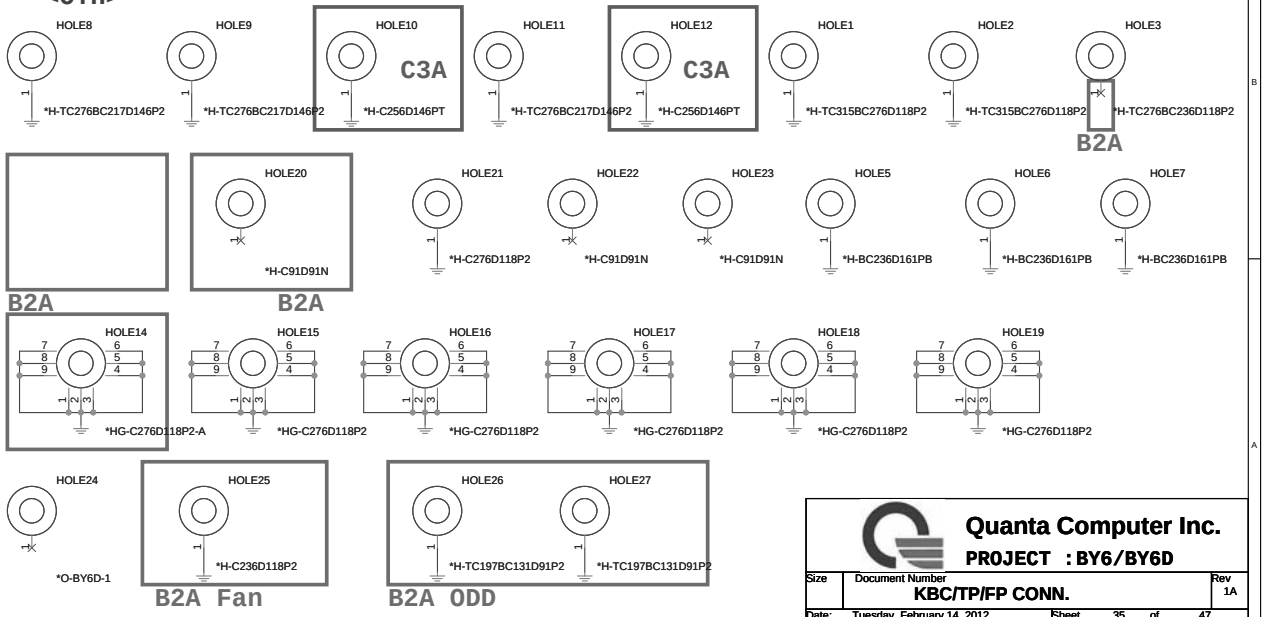
TP board <TPD>



EMI PAD <EMI>



HOLE <OTH>



Quanta Computer Inc.
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	KBC/TP/FP CONN.	1A

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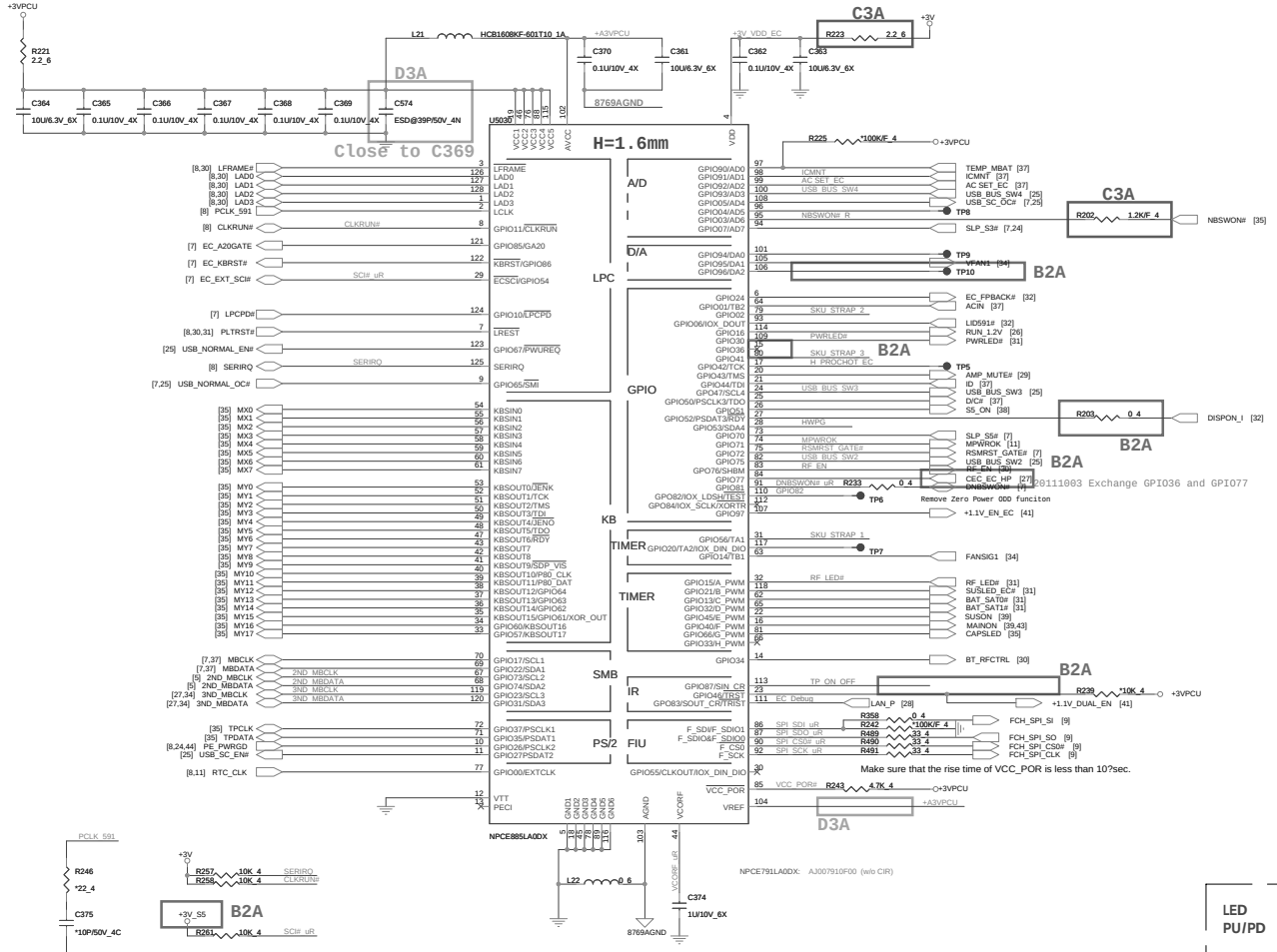
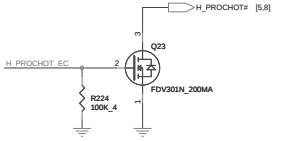
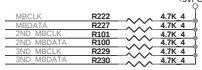
EC <KBC>



Intel Turbo mode only <CPU>



SM BUS PU <KBC>



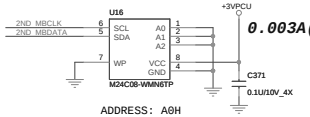
SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	3D Sensor	32H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H

Strap <KBC>

SHBM

ID EEPROM <KBC>

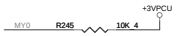


SPI FLASH <KBC>

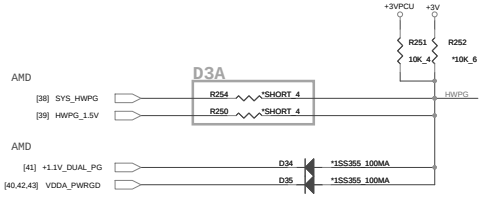
BY6-A1A Del SPI ROM

MX25L3205DM2I-12G: AKE39FP0Z00
W25Q16BVSSIG: AKE38FP0N01

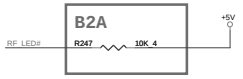
INTERNAL KEYBOARD STRIP SET <KBC>

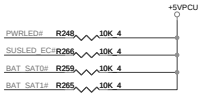


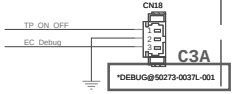
HWPG circuit <KBC>



LED PU/PD <LED>



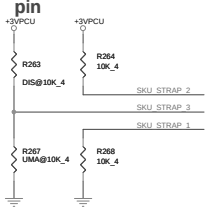




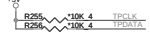
SKU STRAPPING:
Pull H SKU_STRAP_3 For Disctete
Pull L SKU_STRAP_3 For UMA
Pull SKU_STRAP_1=Lo&SKU_STRAP_2=Hi For 14"

SKU_STRAP_1(GPIO56)	SKU_STRAP_2(GPIO02)	SKU_STRAP_3(GPIO41)	SKU
0	0	0	Brazos UMA
0	0	1	Brazos DIS
0	1	0	COMAL UMA
0	1	1	COMAL DIS
1	0	0	Deccan UMA
1	0	1	Deccan DIS

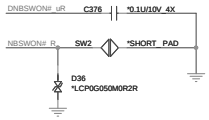
SKU strap pin <KBC>

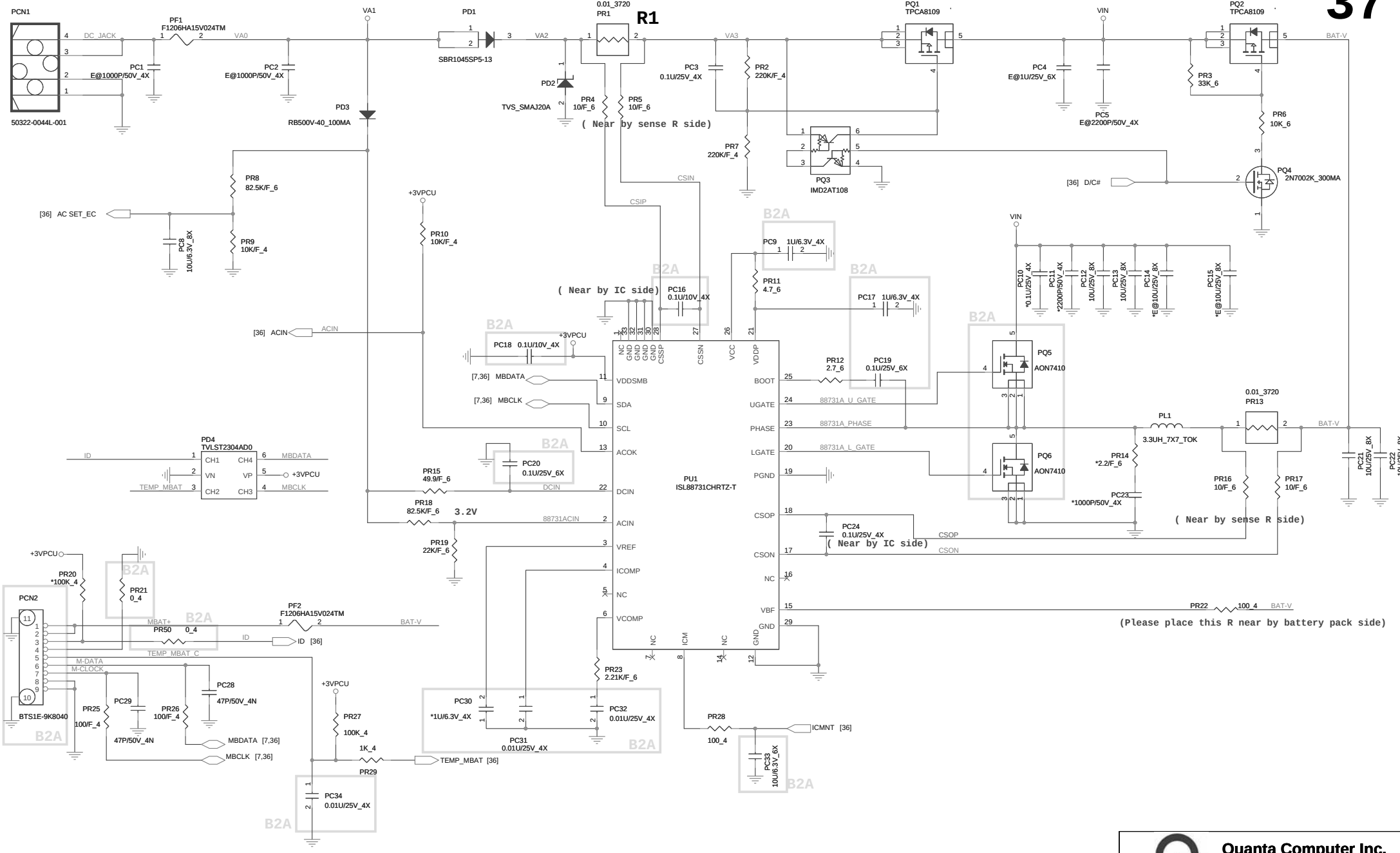


TP interface PU <KBC>

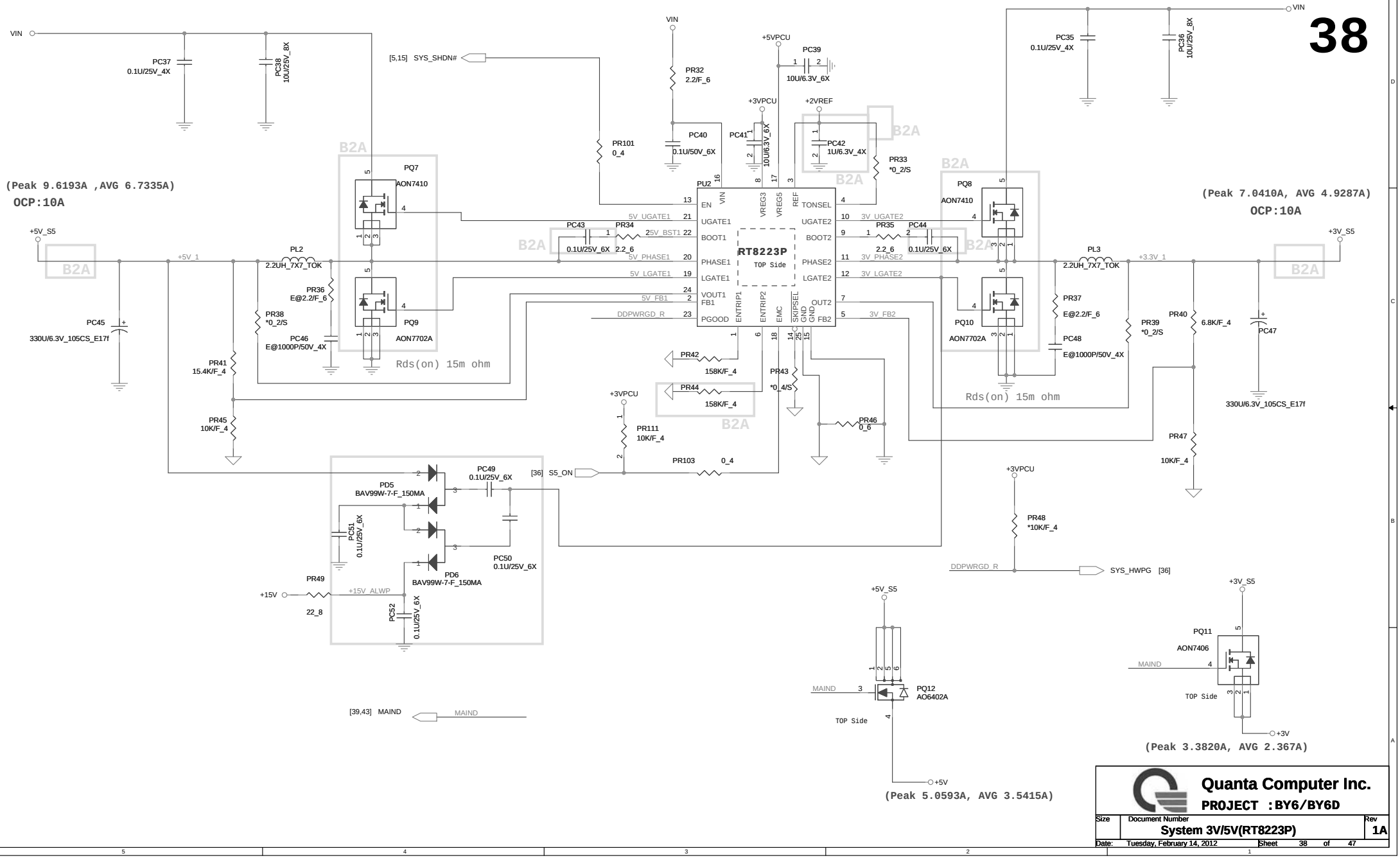


Power Button <KBC>

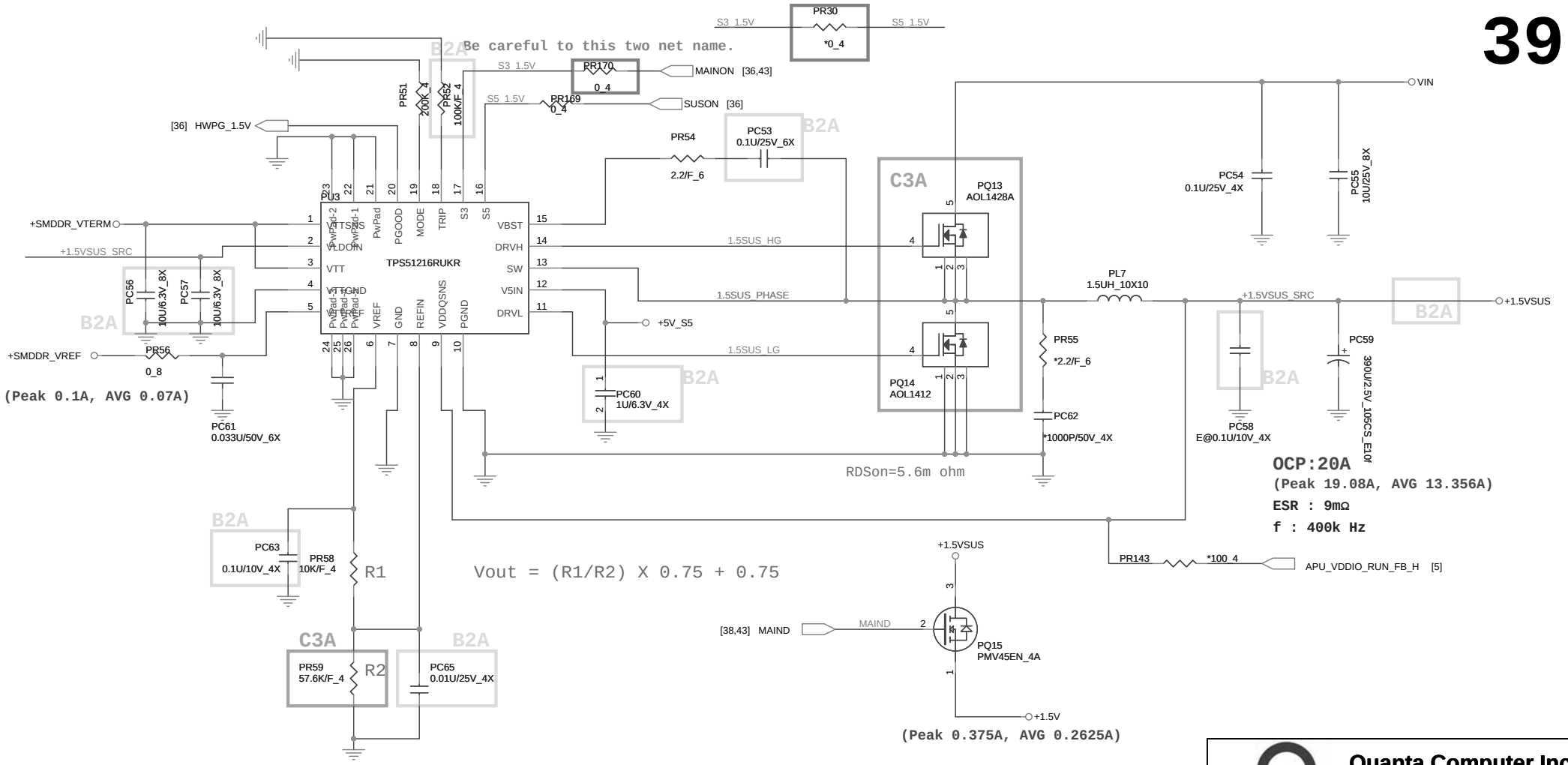




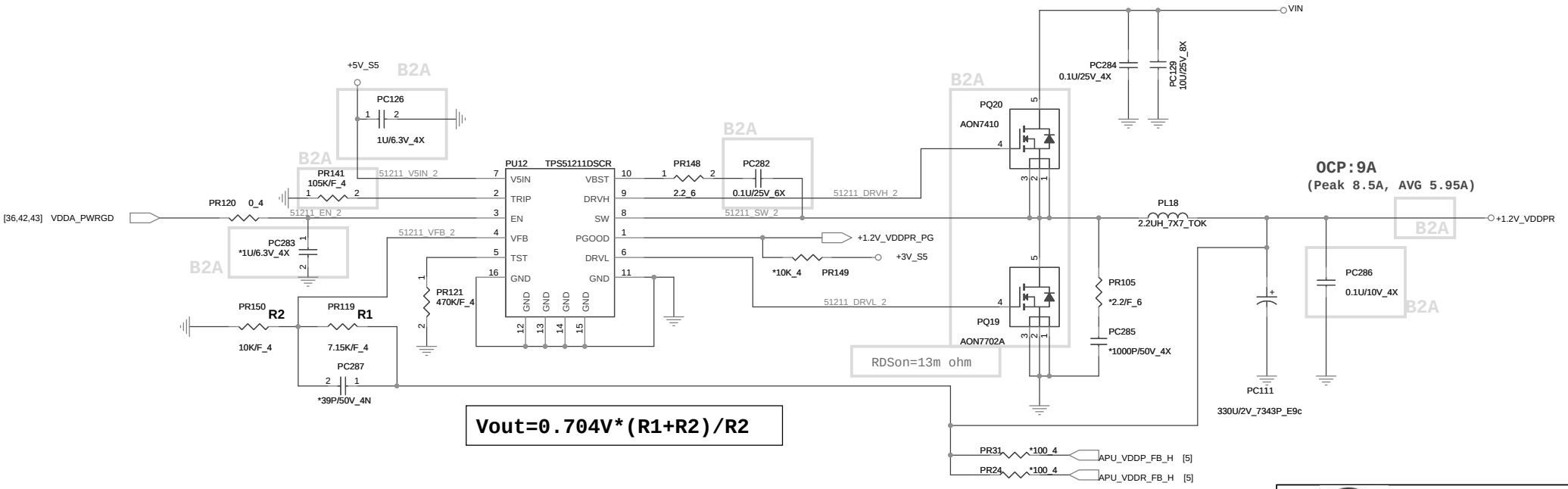
Quanta Computer Inc.			
PROJECT : BY6/BY6D			
Size	Document Number		Rev
	CHARGER (ISL88731C)		1A
Date: Tuesday, February 14, 2012		Sheet 37 of 47	



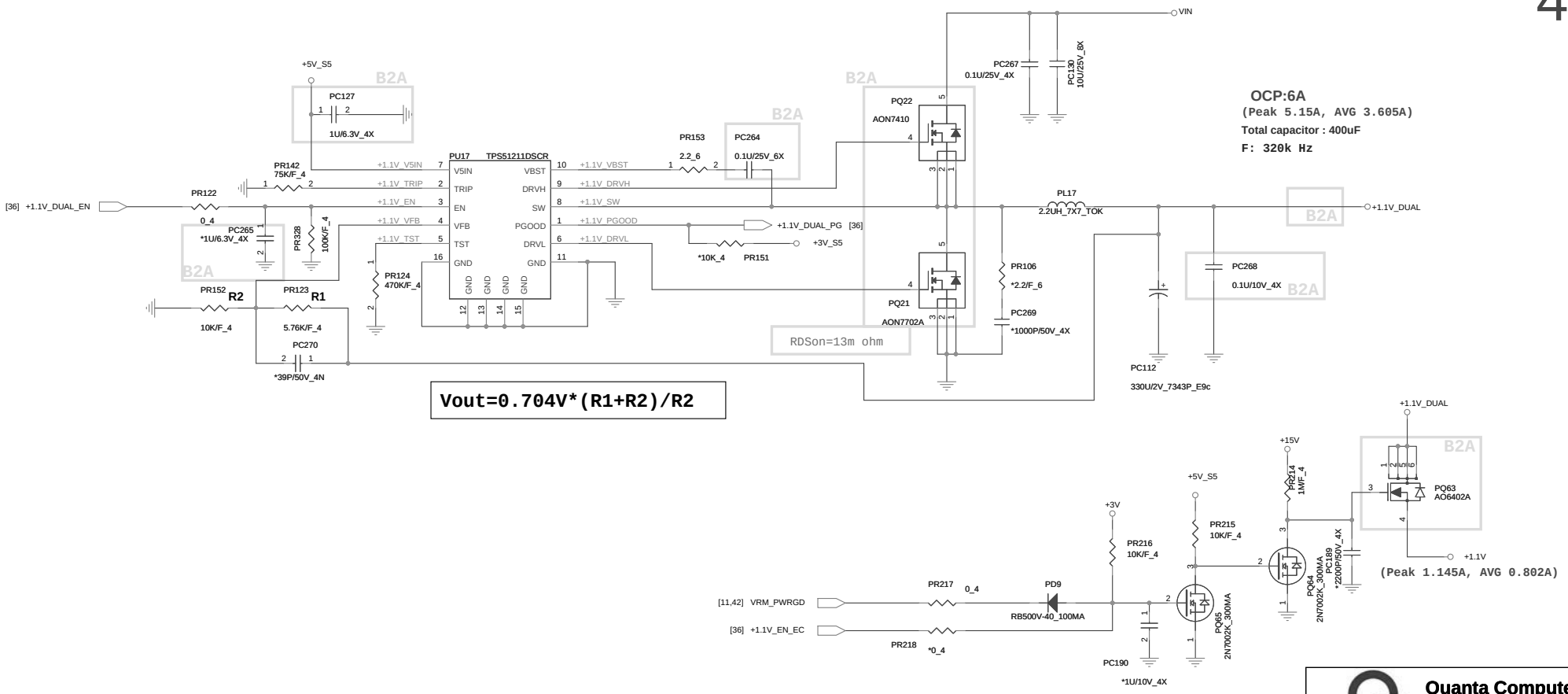
Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: System 3V/5V(RT8223P)	Rev: 1A
Date: Tuesday, February 14, 2012	Sheet 38 of 47	



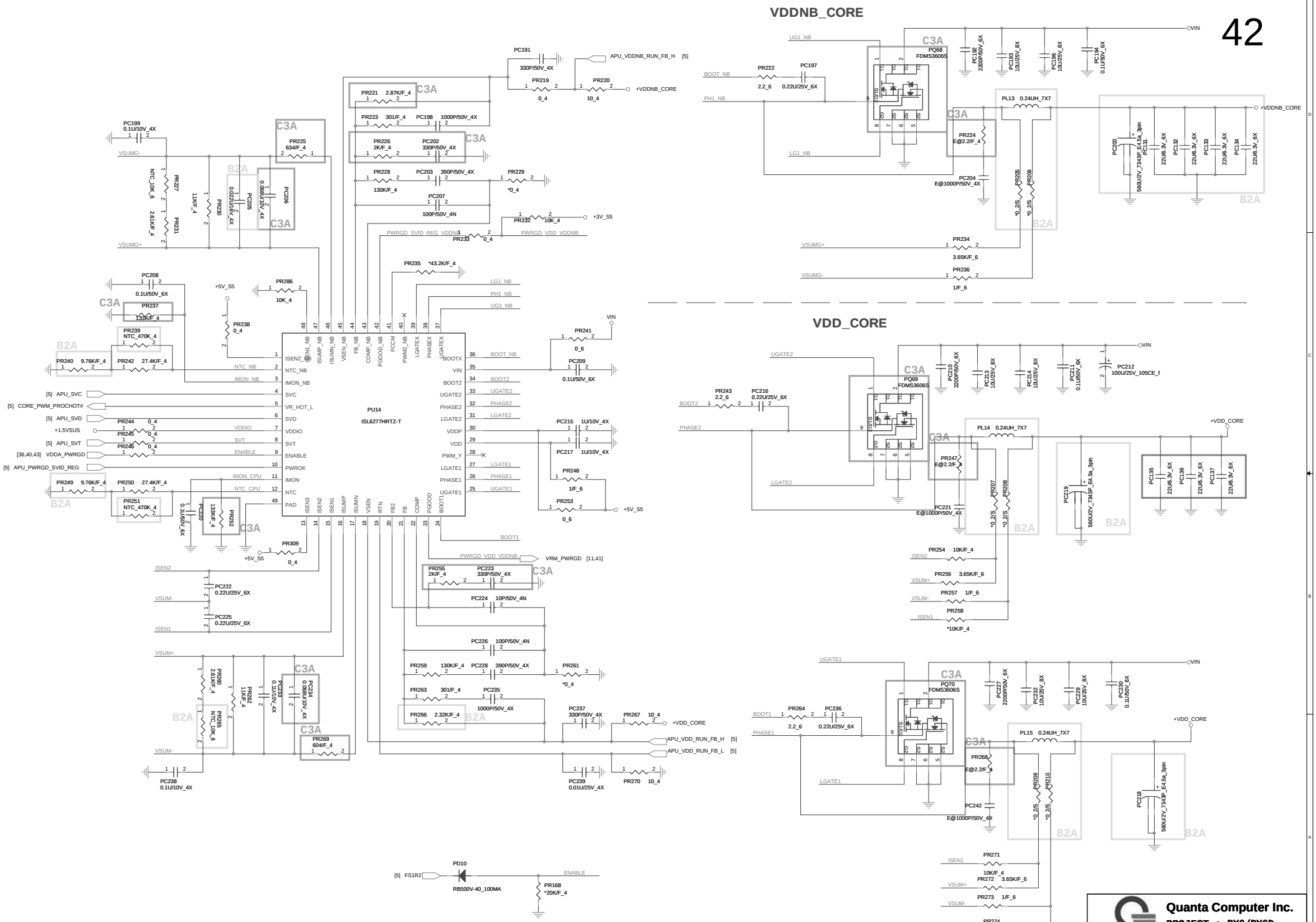
Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: +1.5VSUS (TPS51216RUKR)	Rev: 1A
Date: Tuesday, February 14, 2012	Sheet 39 of 47	



Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: +1.2V_VDDPR (TPS51211DSCR)	Rev: 1A
Date: Tuesday, February 14, 2012	Sheet 40 of 47	



Quanta Computer Inc.		
PROJECT : BY6/BY6D		
Size	Document Number: +1.1V_DUAL (TPS51211DSCR)	Rev: 1C
Date: Tuesday, February 14, 2012	Sheet 41 of 47	


VDDNB_CORE
VDD_CORE
ISL6277HRTZ-T
PU14
RB500V-40_100MA
PD10
Quanta Computer Inc.
PROJECT : BY6/BY6D
CPU_CORE (ISL6277HRTZ-T)
Size
Document Number
Rev
1C
Date: Tuesday, February 14, 2012
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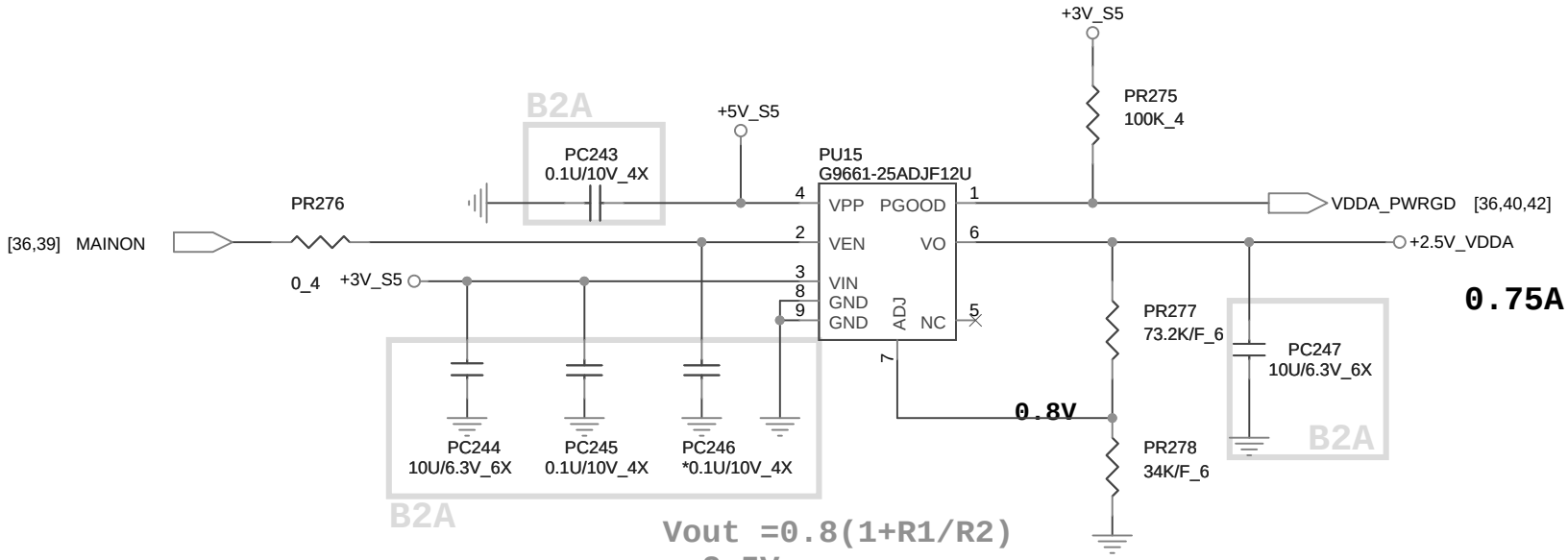
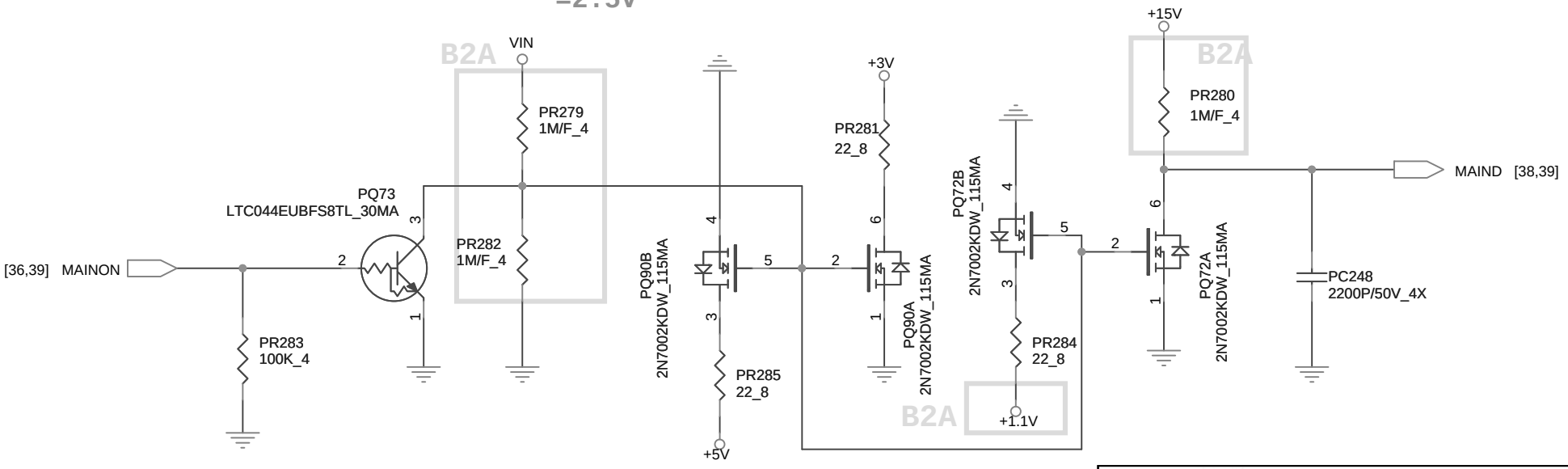
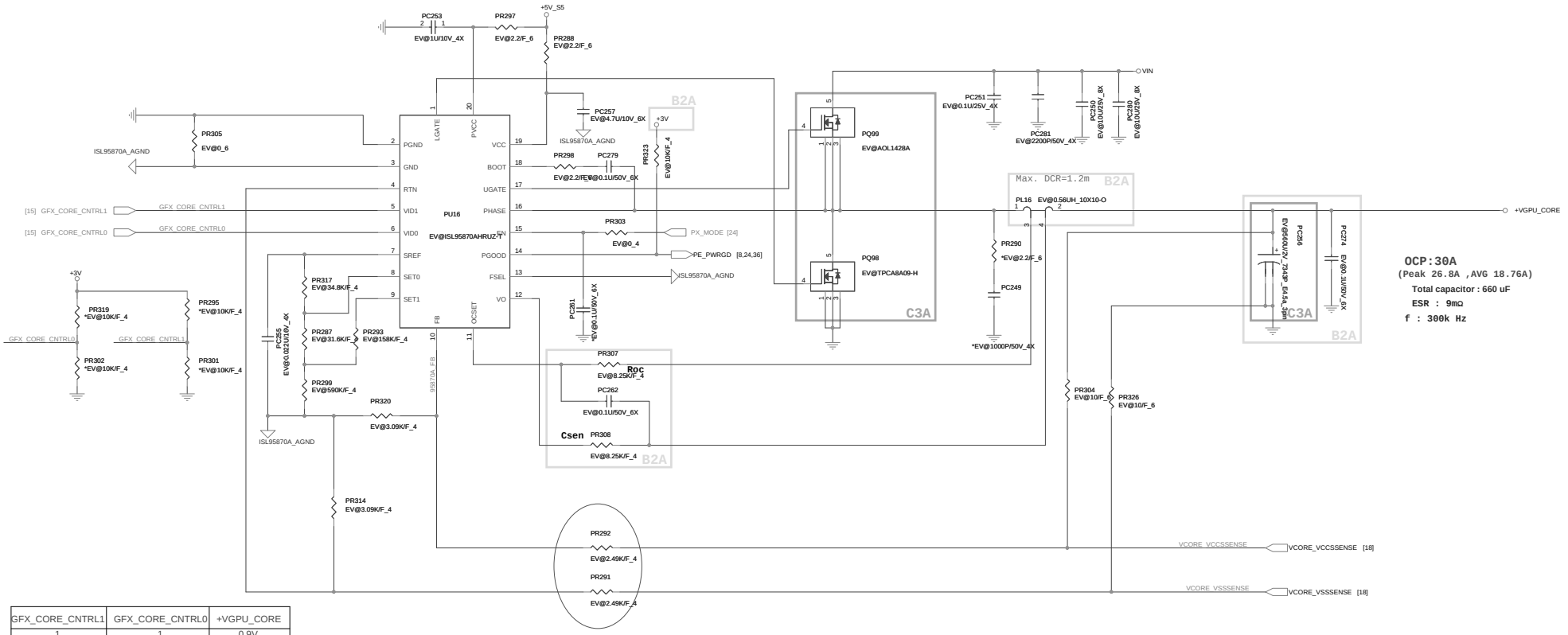




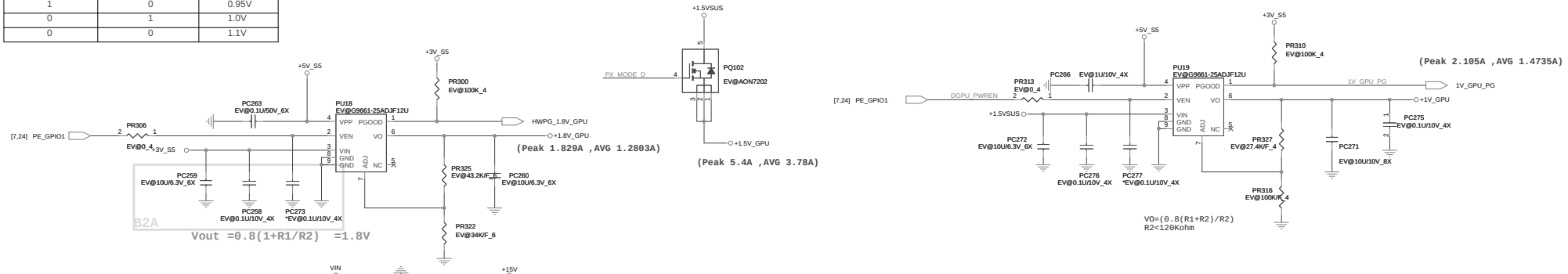
Quanta Computer Inc.

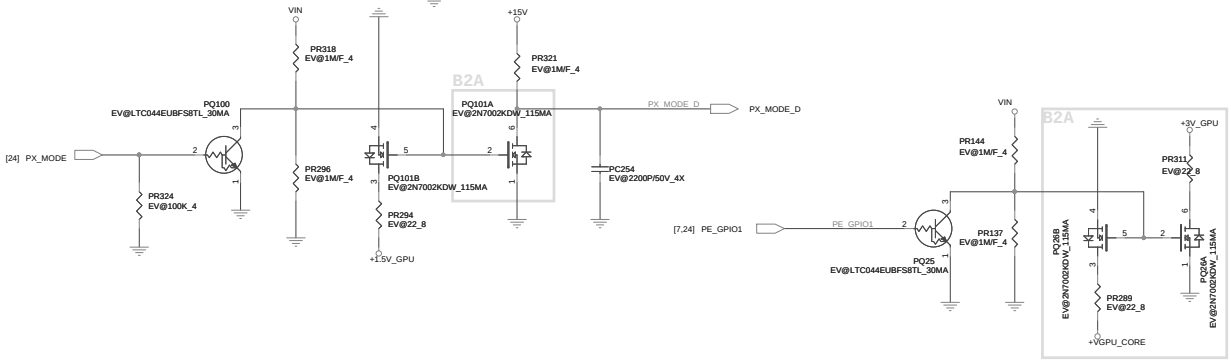
PROJECT : BY6/BY6D

Size	Document Number	Rev
	DISCHARGE	1A
Date: Tuesday, February 14, 2012	Sheet 43 of 47	

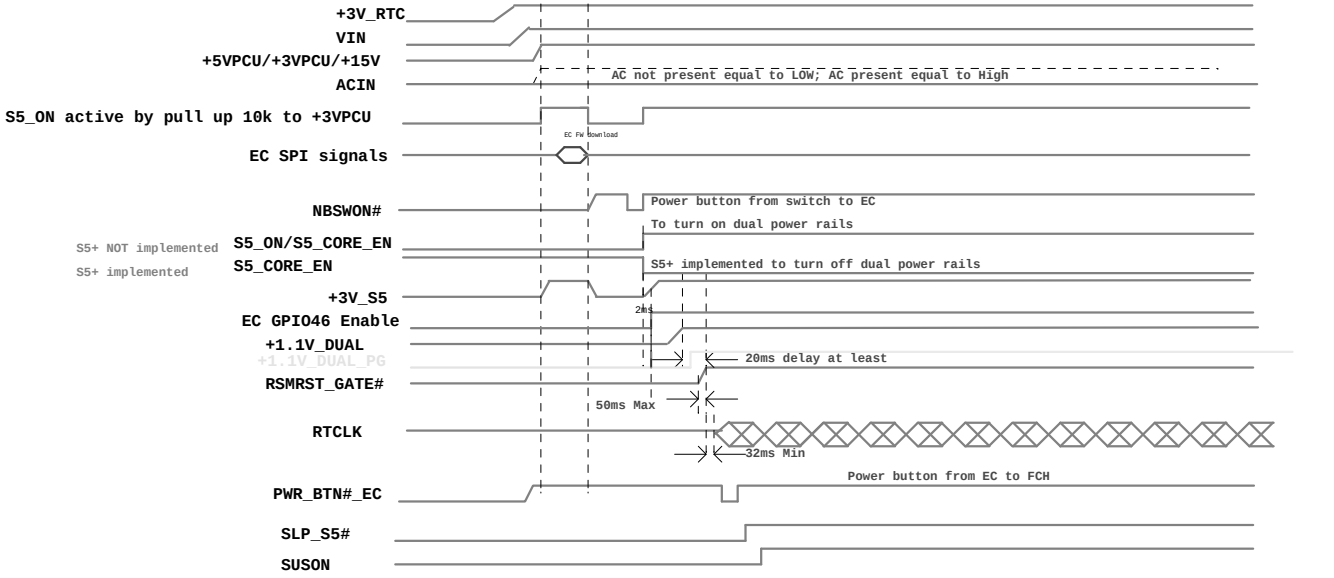


GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	0.95V
0	1	1.0V
0	0	1.1V

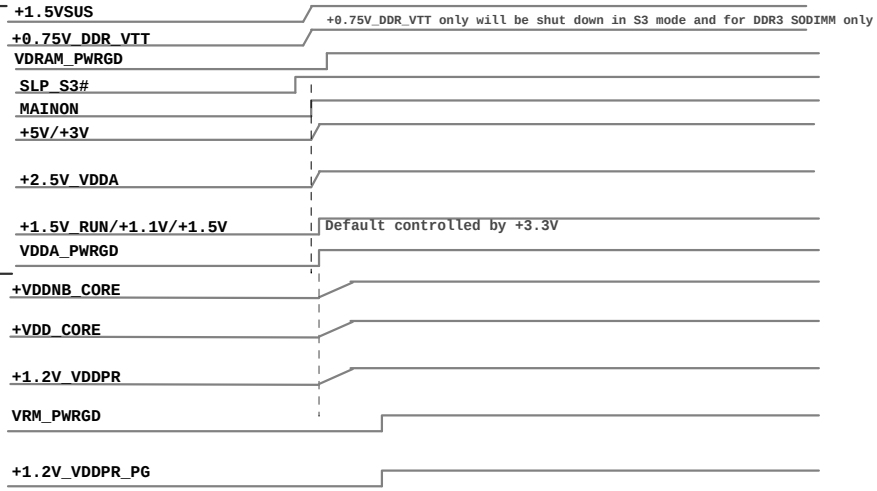




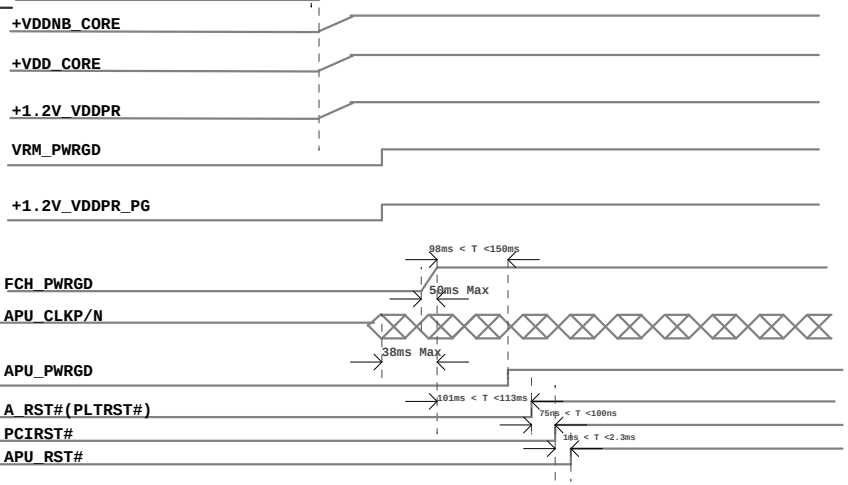
BY6/BY6D Power On Sequence: S5 > S0



APU GROUP A power



APU GROUP B power

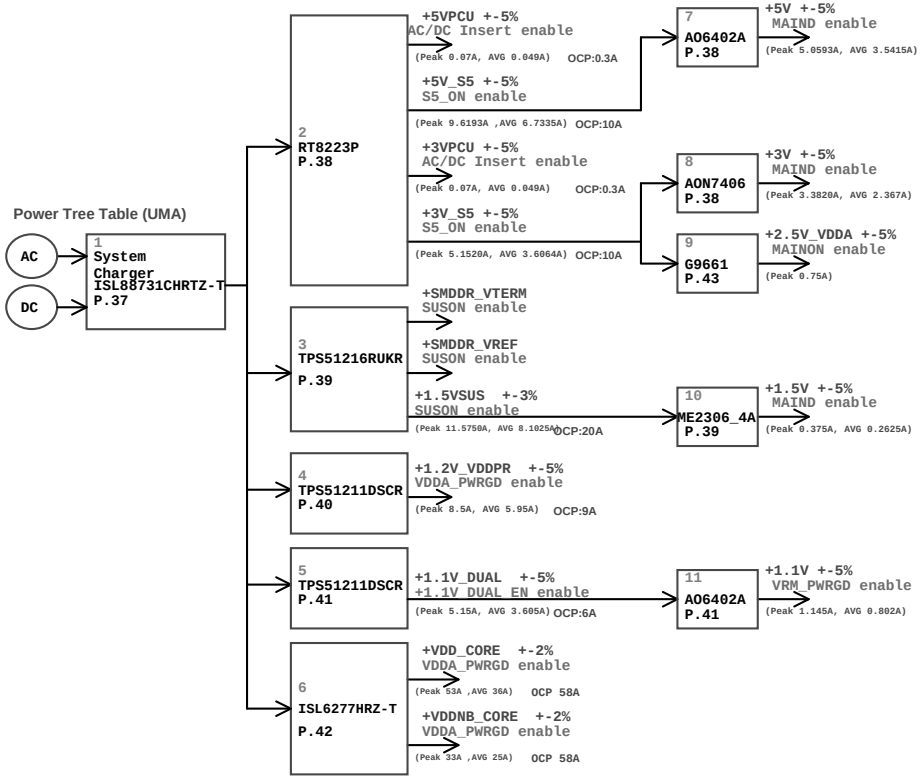


APU Power on sequence required:

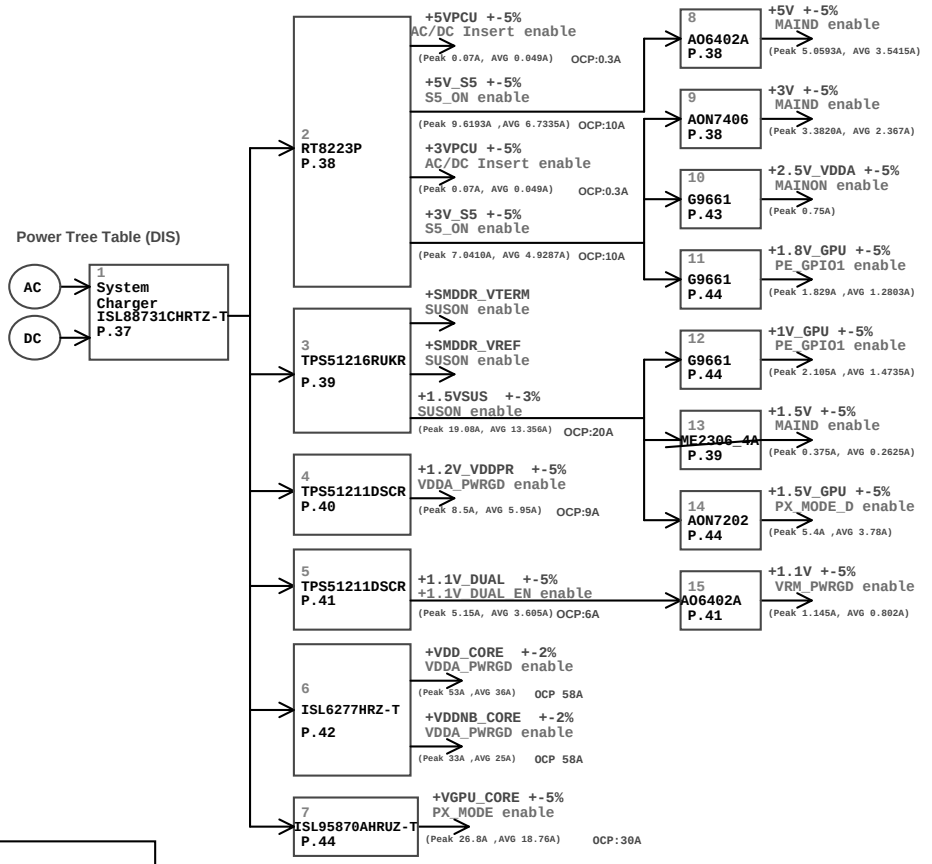
Llano APU:
1.Group A (+1.5VSUS, +2.5V_VDDA) ramp before Group B (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M2/M3:
1.+3V_S5 ramp before +1.1V_DUAL
2.+3V ramp before +1.1V
3.+3V_RTC must ramp at least 5 secs before the +3V_S5

Power Tree Table (UMA)



Power Tree Table (DIS)



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : BY6/BY6D

Size	Document Number	Rev
	POWER TREE TABLE	1A

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Model	REV	CHANGE LIST
BY6D MB	A1A	

MODEL	BY6D	
PAGE	FROM	
1	A1A	
2	A1A	
3	A1A	
4	A1A	
5	A1A	
6	A1A	
7	A1A	
8	A1A	
9	A1A	
10	A1A	
11	A1A	
12	A1A	
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40	A1A	
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42	A1A	
43	A1A	
44	A1A	
45	A1A	
46	A1A	

DOC NO. 204	PROJECT MODEL :	BY6D	APPROVED BY:		DATE:	2011/10/02
	PART NUMBER:		DRAWING BY:	Wei-Sheng	REVISON:	A1A

Quanta Computer Inc.
PROJECT : BY6D
Size | Document Number: Change List | Rev: A1A
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