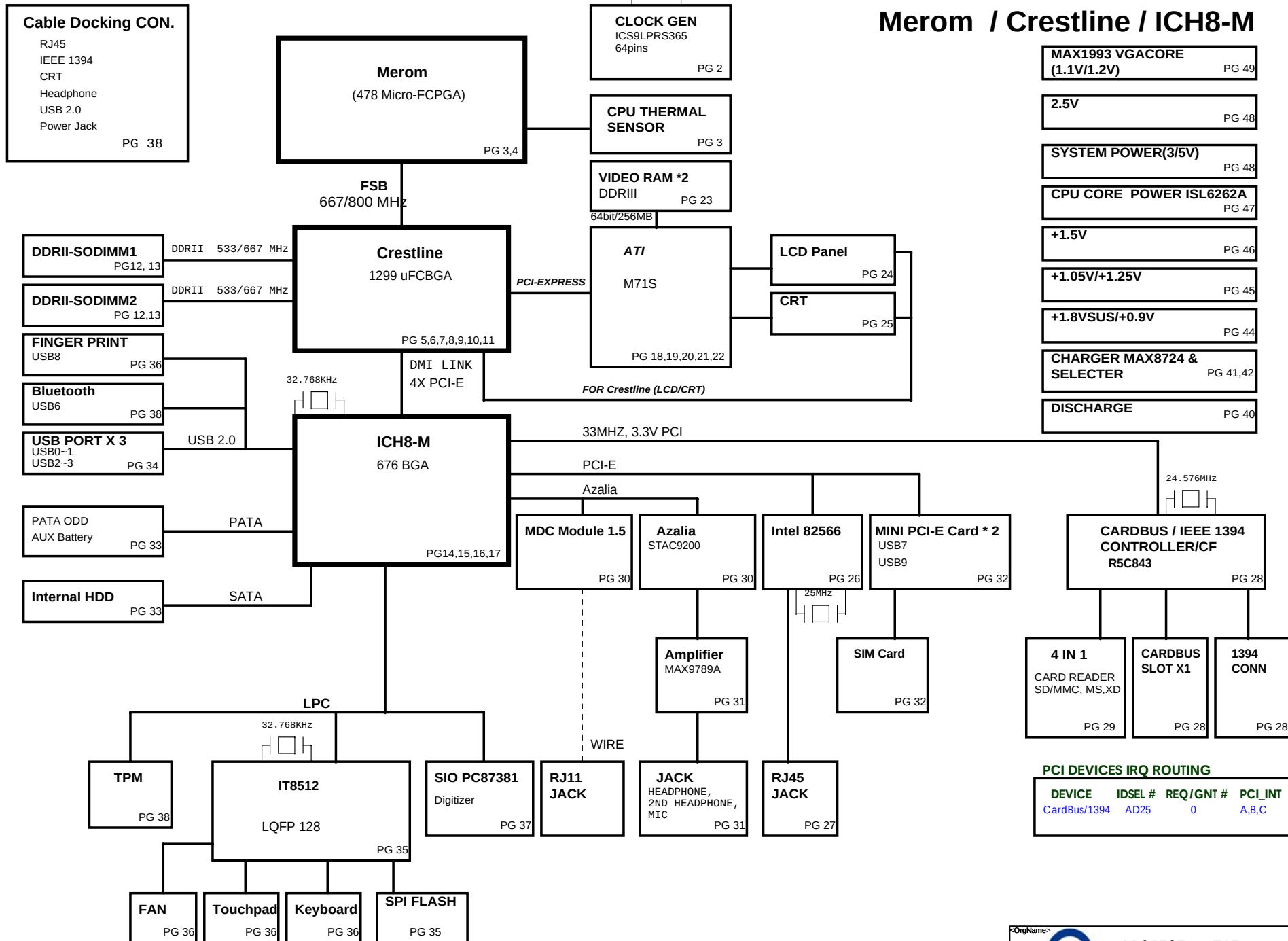
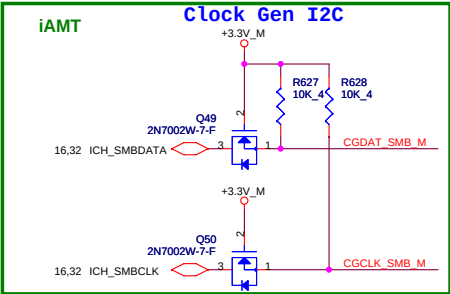
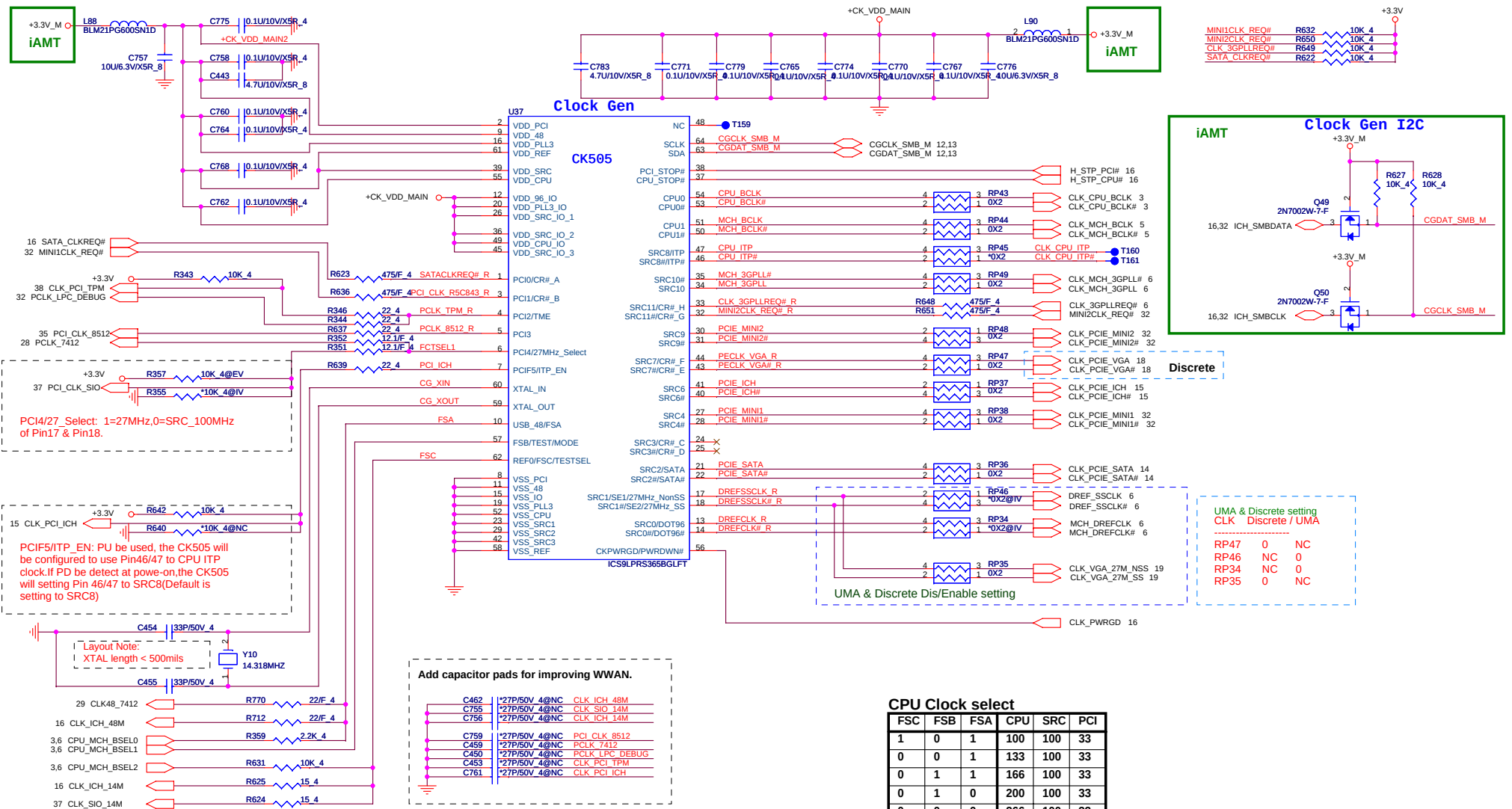


# TA7 BLOCK DIAGRAM

Merom / Crestline / ICH8-M





Discrete

UMA & Discrete setting  
CLK Discrete / UMA

|      |    |    |
|------|----|----|
| RP47 | 0  | NC |
| RP46 | NC | 0  |
| RP34 | NC | 0  |
| RP35 | 0  | NC |

Add capacitor pads for improving WWAN.

|      |               |                |
|------|---------------|----------------|
| C462 | *27P/50V 4@NC | CLK ICH 48M    |
| C755 | *27P/50V 4@NC | CLK SIO 14M    |
| C756 | *27P/50V 4@NC | CLK ICH 14M    |
| C759 | *27P/50V 4@NC | PCI CLK 8512   |
| C459 | *27P/50V 4@NC | PCLK 7412      |
| C450 | *27P/50V 4@NC | PCLK LPC DEBUG |
| C453 | *27P/50V 4@NC | CLK PCI TPM    |
| C761 | *27P/50V 4@NC | CLK PCI ICH    |

### CPU Clock select

| FSC | FSB | FSA | CPU  | SRC | PCI |
|-----|-----|-----|------|-----|-----|
| 1   | 0   | 1   | 100  | 100 | 33  |
| 0   | 0   | 1   | 133  | 100 | 33  |
| 0   | 1   | 1   | 166  | 100 | 33  |
| 0   | 1   | 0   | 200  | 100 | 33  |
| 0   | 0   | 0   | 266  | 100 | 33  |
| 1   | 0   | 0   | 333  | 100 | 33  |
| 1   | 1   | 0   | 400  | 100 | 33  |
| 1   | 1   | 1   | RSVD | 100 | 33  |

### GCLK\_SEL = FCTSEL1

| FCTSEL1 (PIN6)   | PIN13  | PIN14  | PIN17          | PIN18          |
|------------------|--------|--------|----------------|----------------|
| 0=UMA            | DOT96T | DOT96C | SRCT1/LCDT_100 | SRCC1/LCDT_100 |
| 1 = External VGA | SRCT0  | SRCC0  | 27Mout-NSS     | 27Mout-SS      |

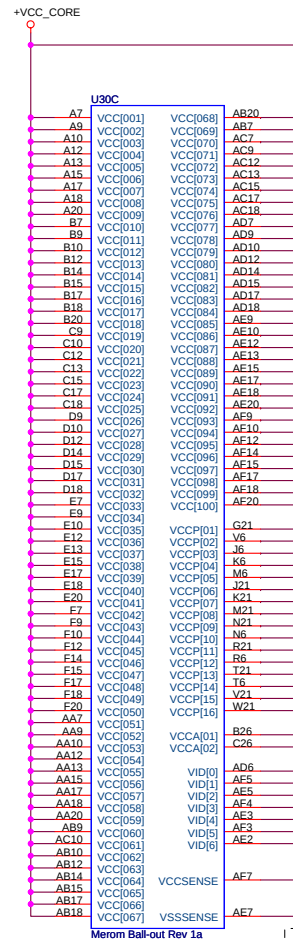
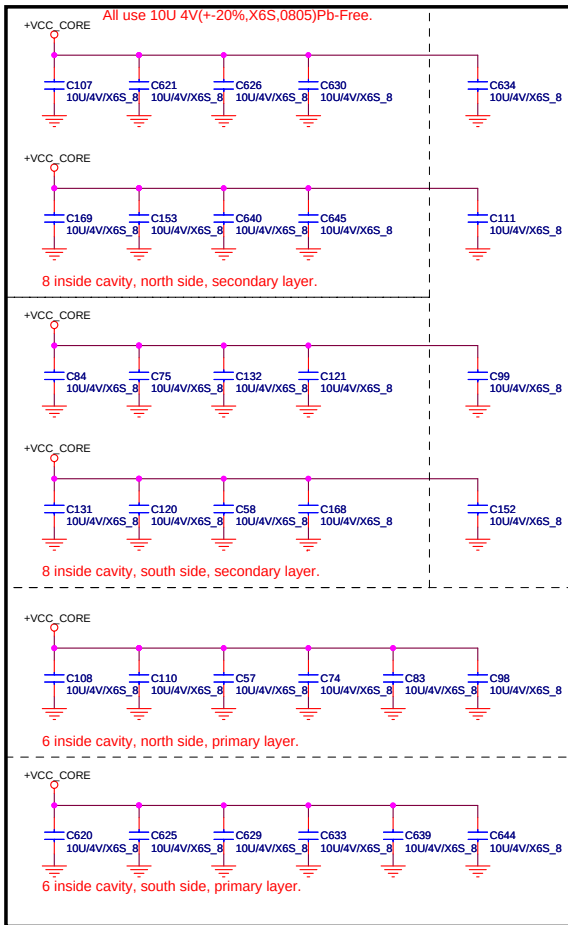
add R712 and R770  
remove R363  
for TI7412 change  
Mika 2006/11/30

R770 R712 change value from 15 to 12.1  
(CS01212FB14)  
Mika 2007/01/05

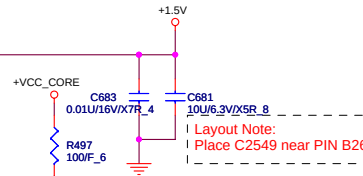
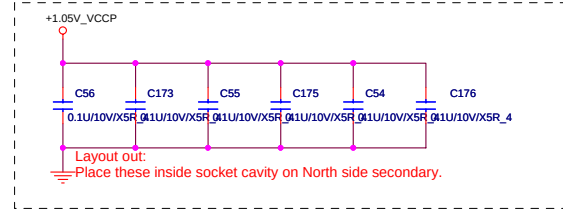
R770 R712 change value from 12.1 to 22  
(CS02202FB12)  
Mika 2007/03/02



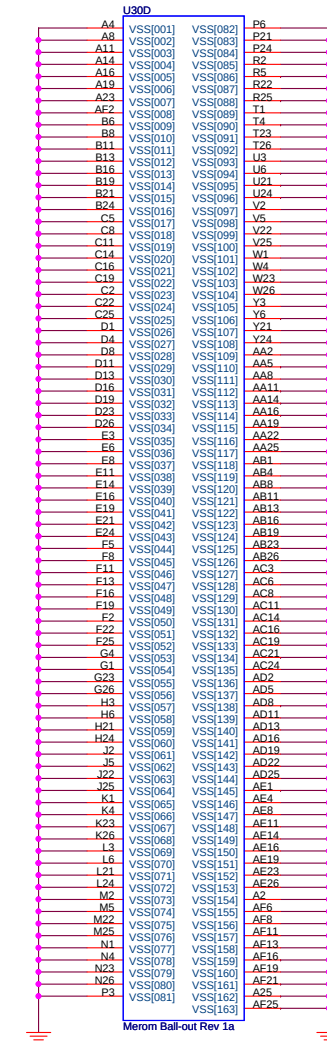
# CPU(Power)

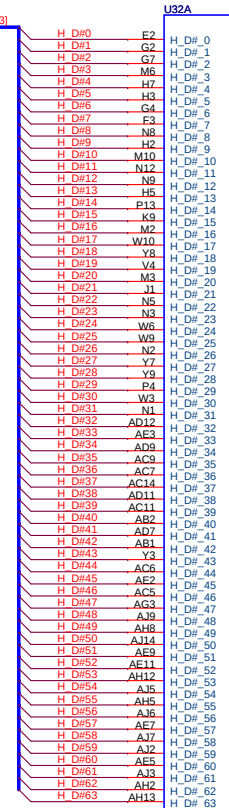
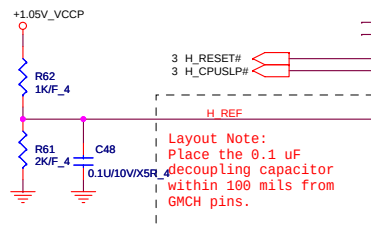
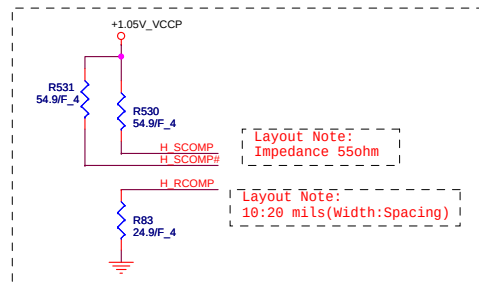
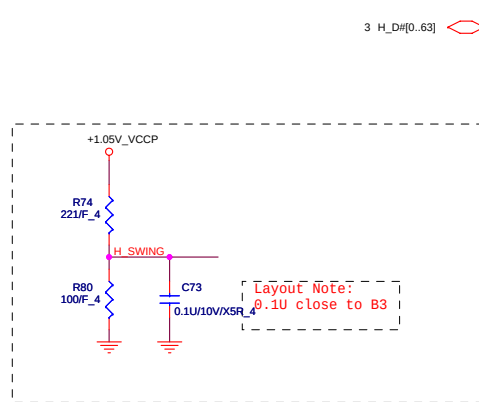


<REV.NO. 0.5/REF.NO.19343>  
 Ivcc Max 52A  
 Ivccp Max 6A(VCCP supply before Vcc stable)  
 Max 2A(VCCP supply after Vcc stable)  
 Ivcca Max 130mA

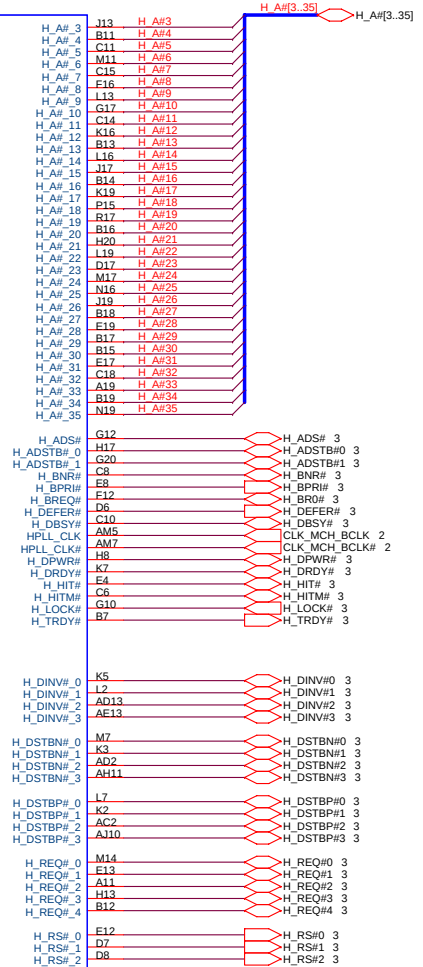


Layout Note:  
 Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.

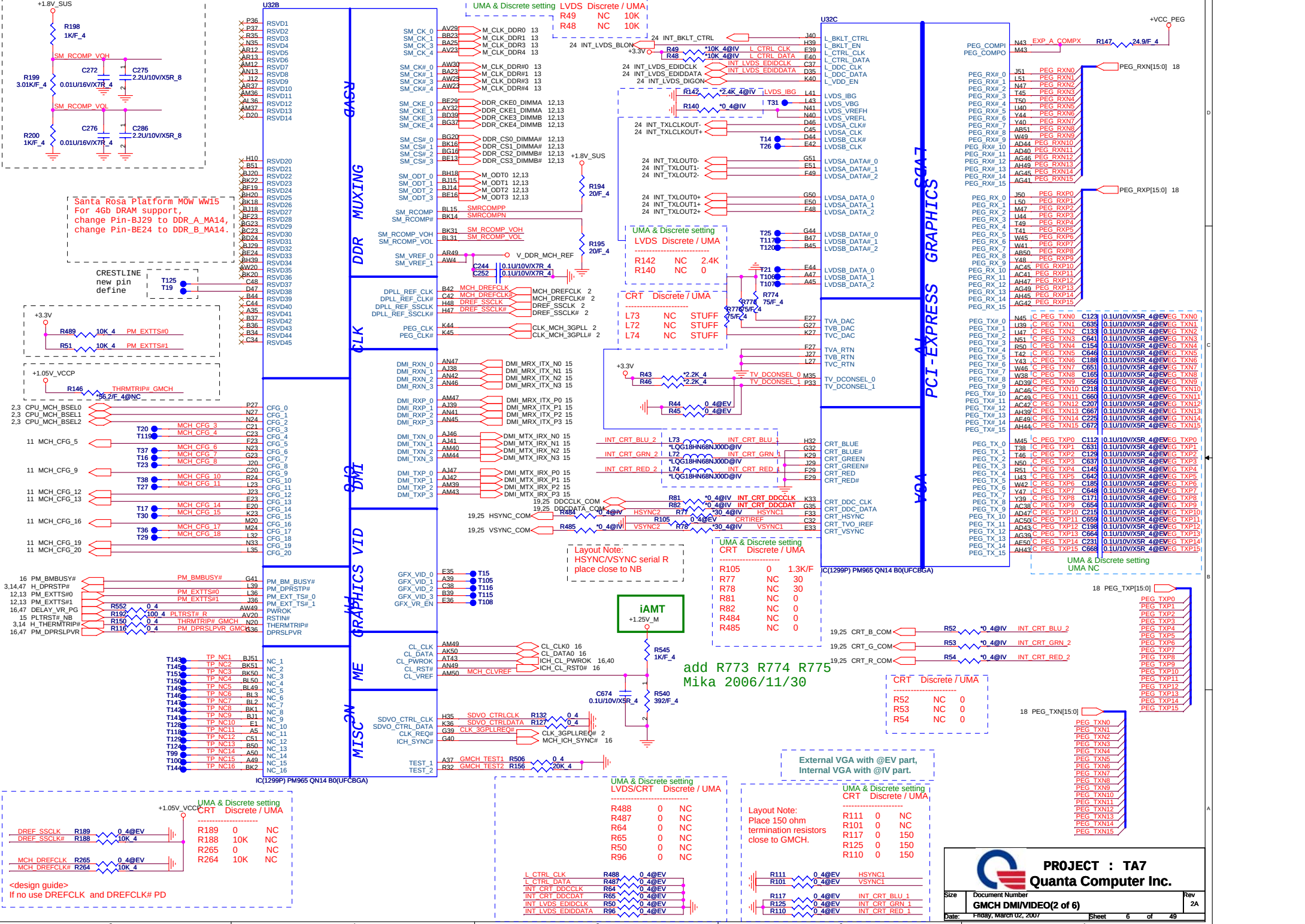


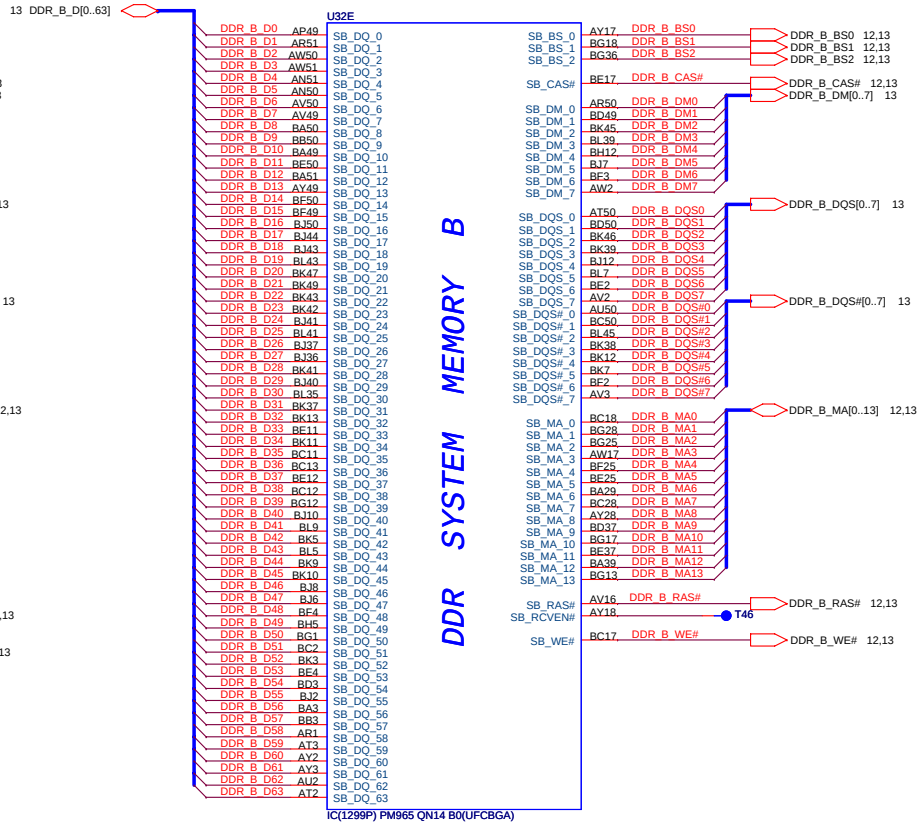
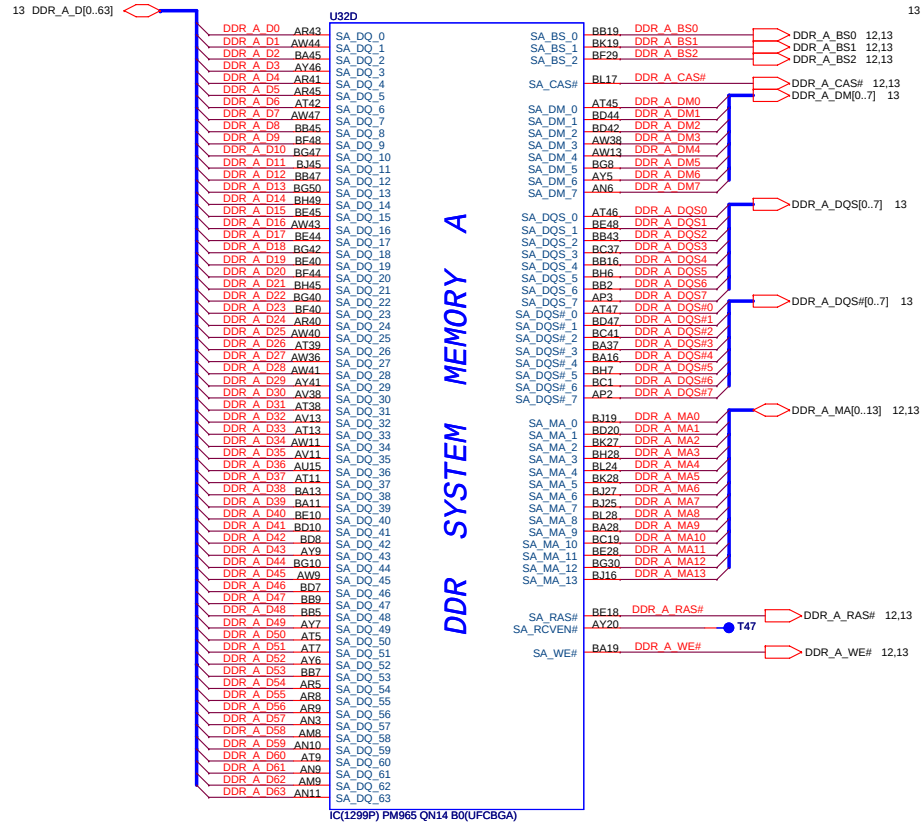


HOST

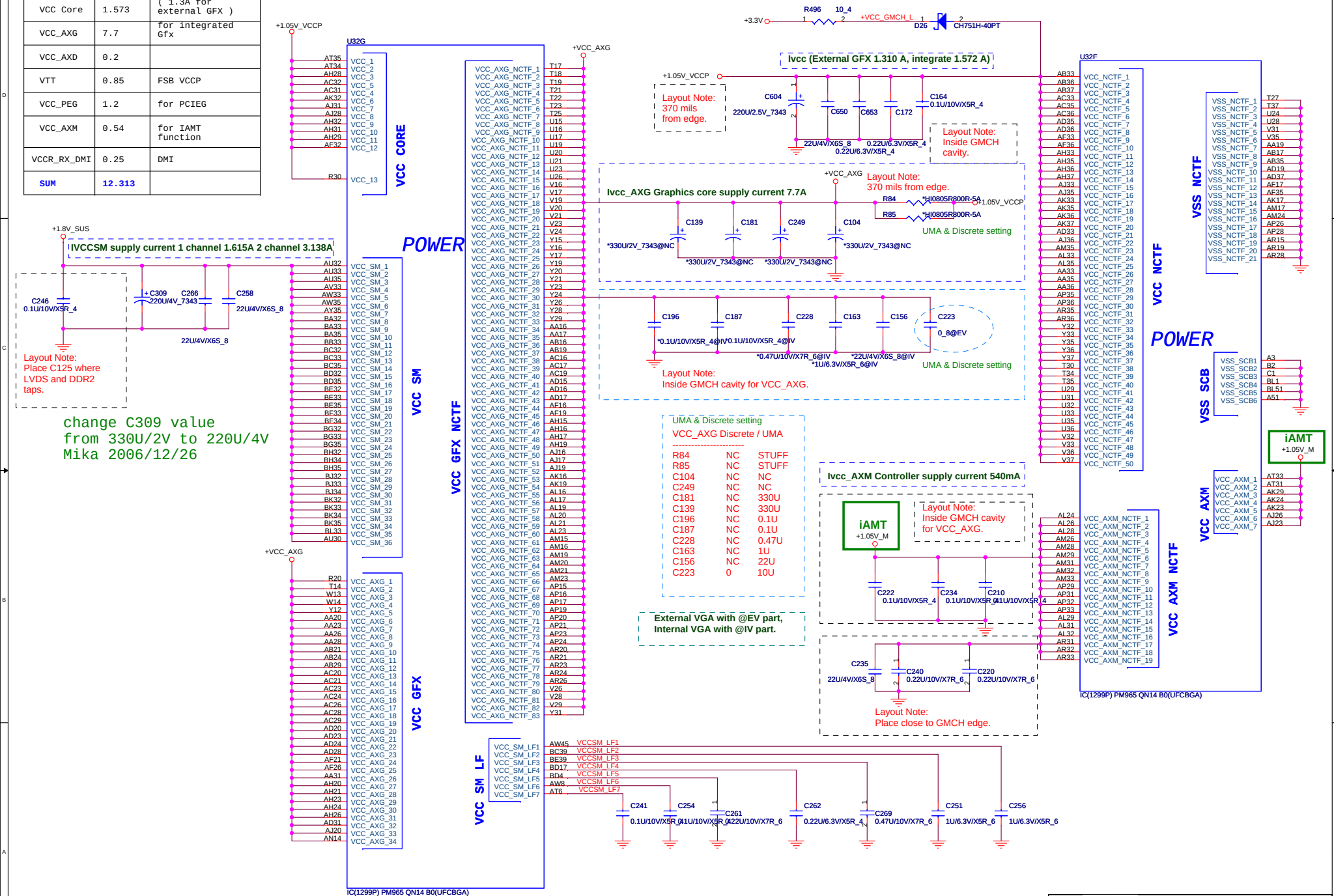






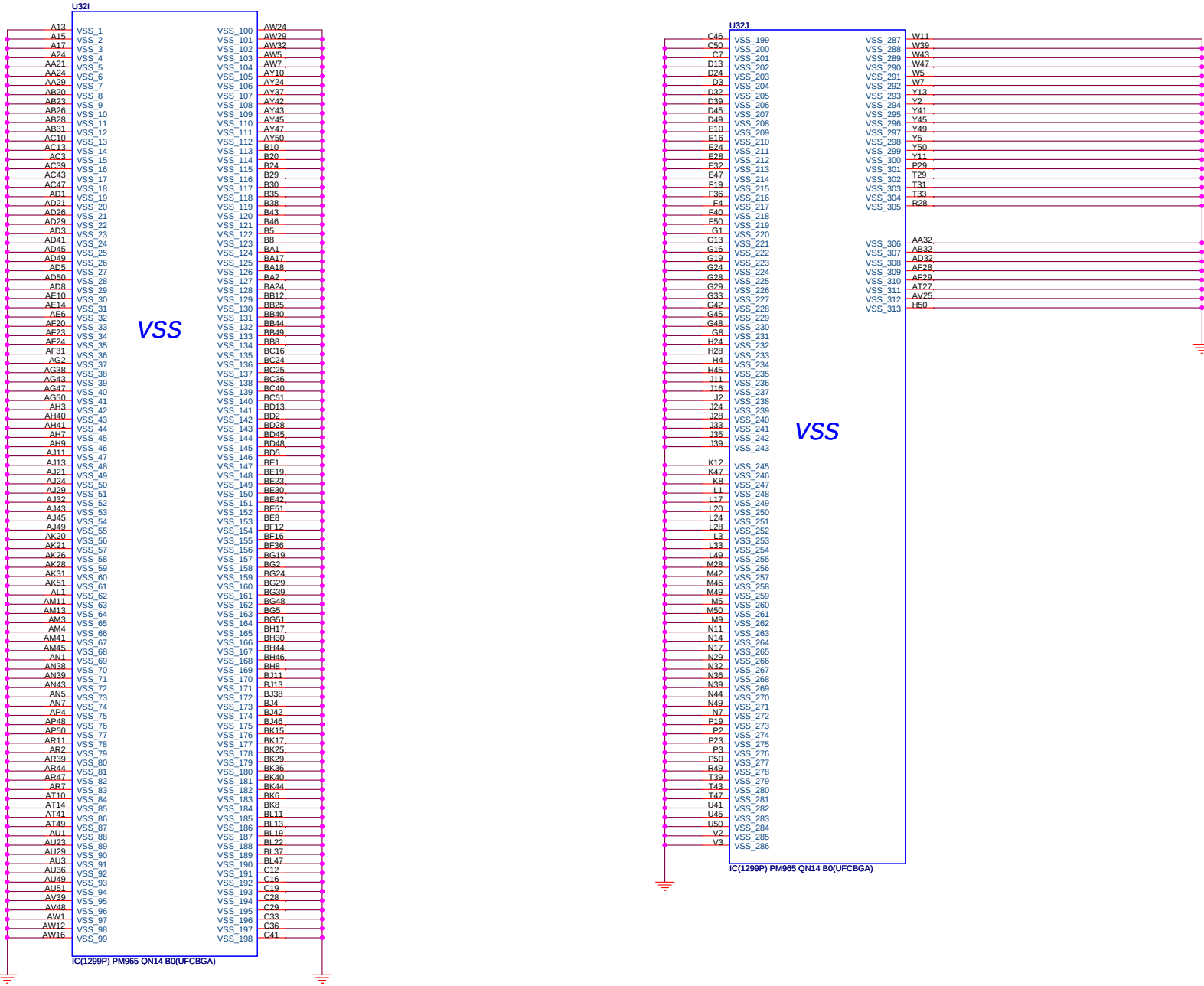


|             |               |                           |
|-------------|---------------|---------------------------|
| GMCH 1.05V  | current(A)    | Remark                    |
| VCC Core    | 1.573         | ( 1.3A for external GFX ) |
| VCC_AXG     | 7.7           | for integrated Gfx        |
| VCC_AXD     | 0.2           |                           |
| VTT         | 0.85          | FSB VCCP                  |
| VCC_PEG     | 1.2           | for PCIEG                 |
| VCC_AXM     | 0.54          | for IAMT function         |
| VCCR_RX_DMI | 0.25          | DMI                       |
| <b>SUM</b>  | <b>12.313</b> |                           |





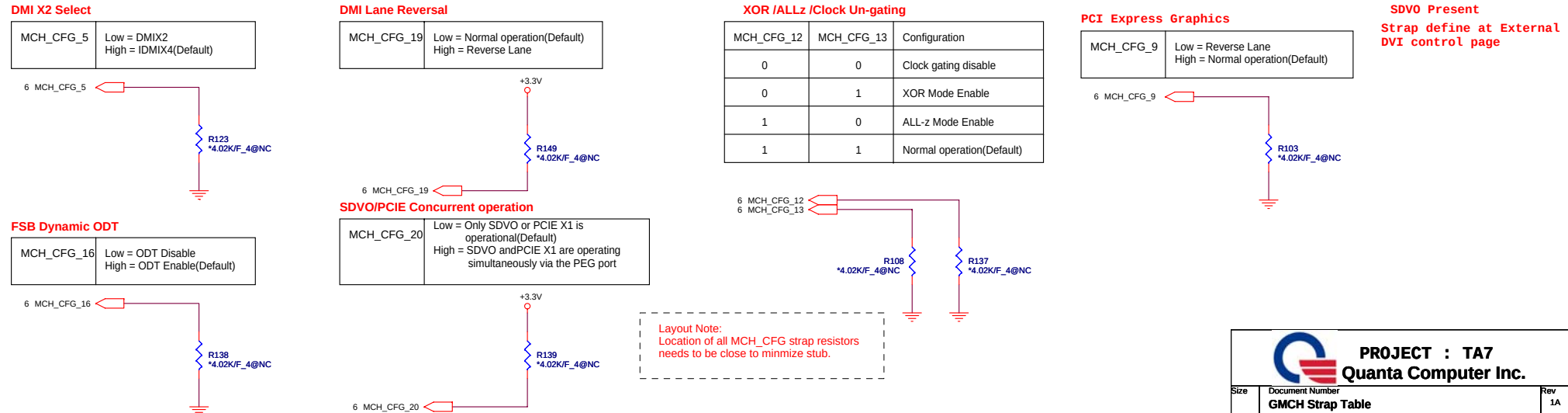


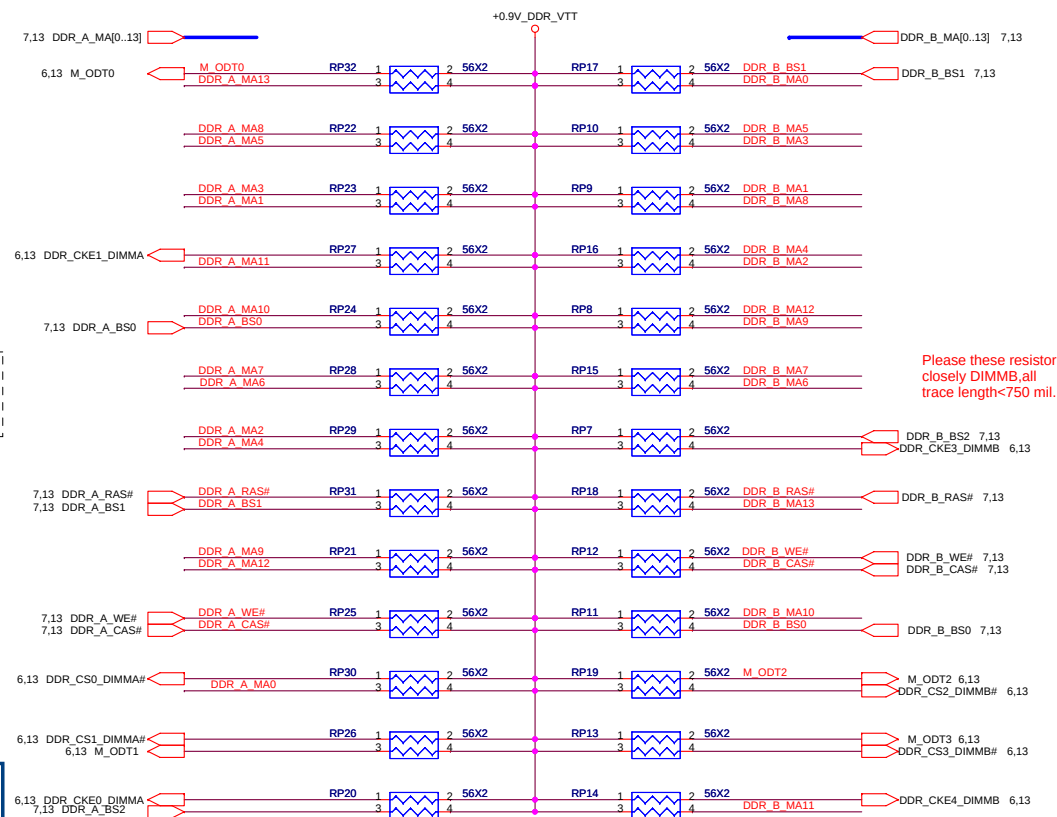
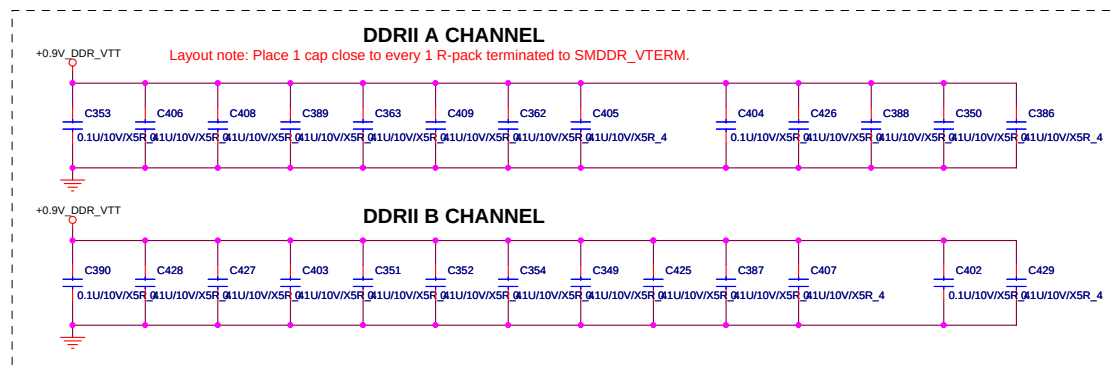


Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal  
CFG[17:3] Have internal Pull-up  
CFG[18:19] Have internal Pull-down  
Any CFG signal strapping option not list below should be left NC Pin

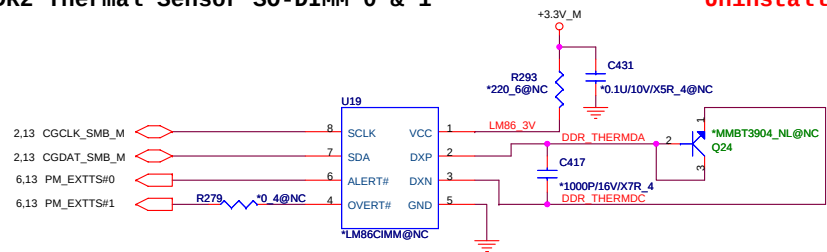
| Pin Name      | Strap description                  | Configuration                                                                                                        |
|---------------|------------------------------------|----------------------------------------------------------------------------------------------------------------------|
| CFG[2:0]      | FSB Frequency Select               | 010 = FSB 800MHz<br>011 = FSB 667MHz                                                                                 |
| CFG[4:3]      | Reserved                           |                                                                                                                      |
| CFG5          | DMI X2 Select                      | 0 = DMI X2<br>1 = DMI X4(Default)                                                                                    |
| CFG6          | Reserved                           |                                                                                                                      |
| CFG7          | CPU Strap                          | 0 = Reserved<br>1 = Mobile CPU(Default)                                                                              |
| CFG8          | Low power PCI Express              | 0 = Normal mode<br>1 = Low Power mode                                                                                |
| CFG9          | PCI Express Graphics Lane Reversal | 0 = Reverse Lanes<br>1 = Normal operation(Default)                                                                   |
| CFG[11:10]    | Reserved                           |                                                                                                                      |
| CFG[13:12]    | XOR/ALLZ                           | 00 = Reserved<br>01 = XOR Mode Enable<br>10 = All-Z Mode Enabled<br>11 = Normal operation(Default)                   |
| CFG[15:14]    | Reserved                           |                                                                                                                      |
| CFG16         | FSB Dynamic ODT                    | 0 = Dynamic ODT disable<br>1 = Dynamic ODT Enable(Default)                                                           |
| CFG[18:17]    | Reserved                           |                                                                                                                      |
| SDVO_CTRLDATA | SDVO Present                       | 0 = No SDVO Card present(Default)<br>1 = SDVO Card Present                                                           |
| CFG19         | DMI Lane Reversal                  | 0 = Normal operation(Default)<br>1 = Reverse Lanes                                                                   |
| CFG20         | SDVO/PCIE concurrent               | 0 = Only SDVO or PCIE x1 is operation(Default)<br>1 = SDVO and PCIE x1 are operating simultaneously via the PEG port |



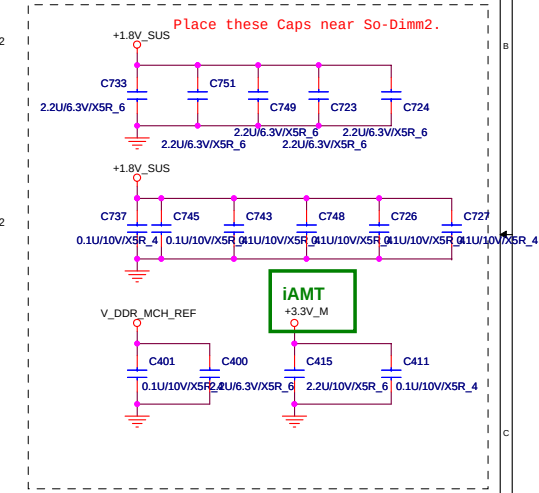
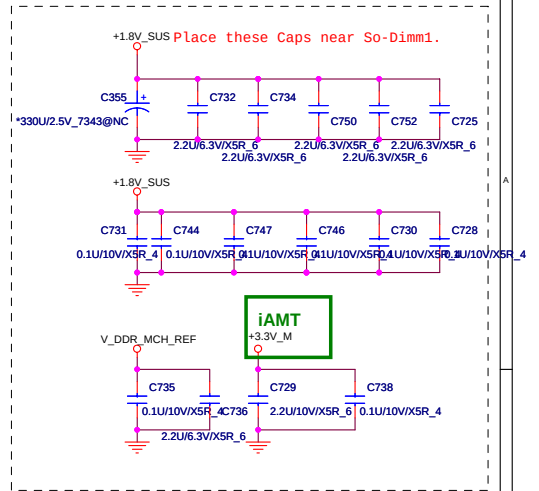


## DDR2 Thermal Sensor S0-DIMM 0 &amp; 1

Uninstall

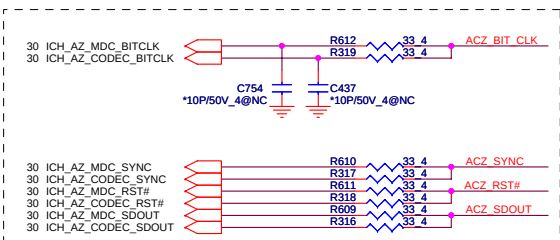
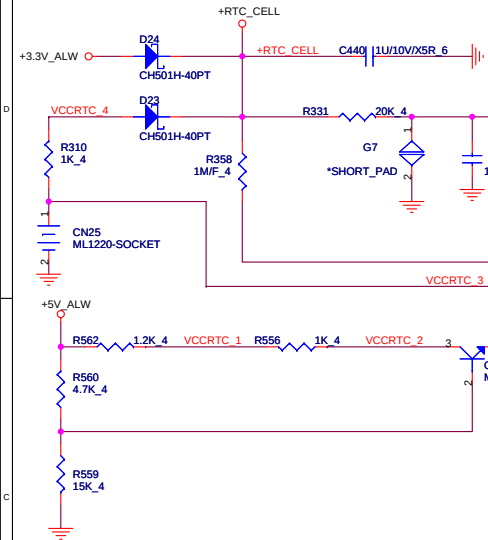


DDR2 Dual channel A/B CONN





# RTC



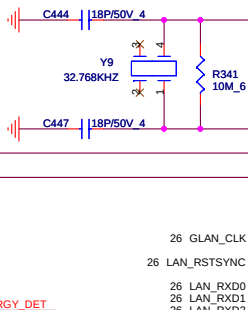
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R292, R286, R283 & R289 should equal distance to the T split trace point as R291, R285, R284 & R290 respectively. Basically, keep the same distance from T for all series termination resistors.



Distance between the ICH-8 M and cap on the "p" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.

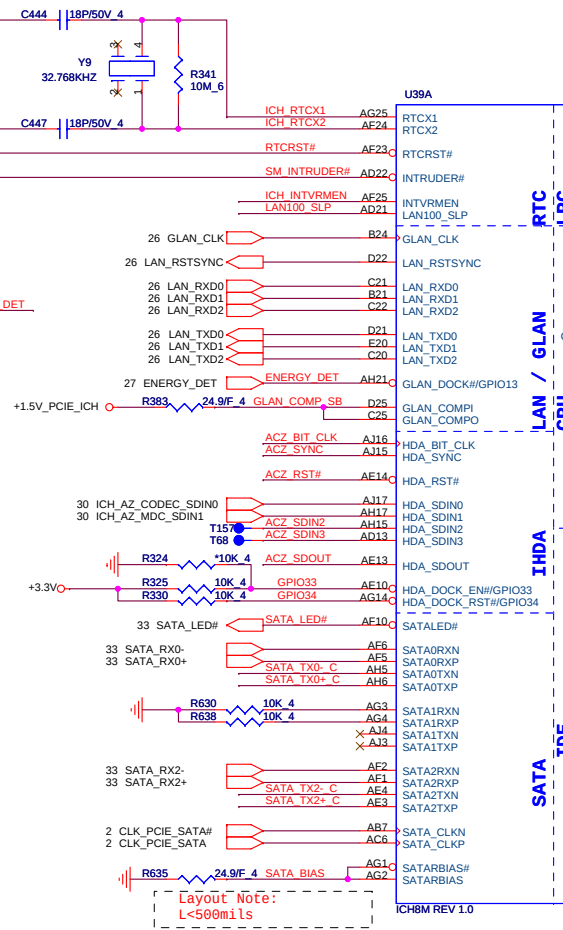


# SB Strap



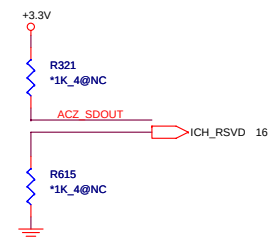
**ICH8M Internal VR Enable Strap**  
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)  
Low = Internal VR Disabled  
High = Internal VR Enabled(Default)

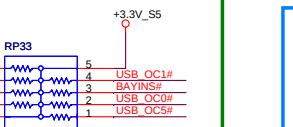
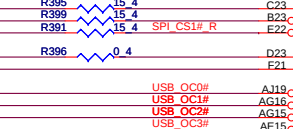
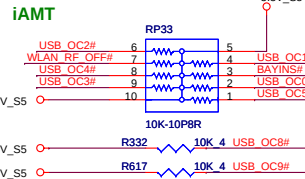
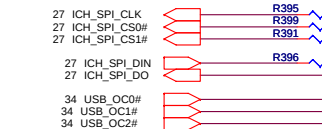
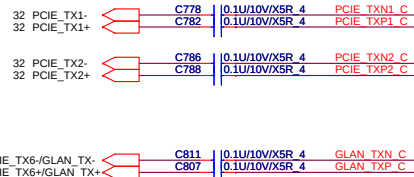
**ICH8M LAN100 SLP Strap**  
(Internal VR for VccLAN1.05 and VccCL1.05)  
Low = Internal VR Disabled  
High = Internal VR Enabled(Default)



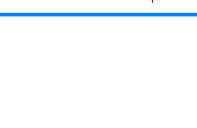
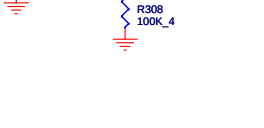
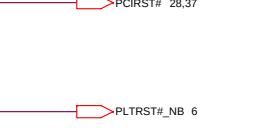
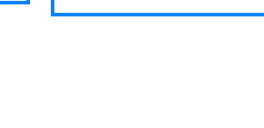
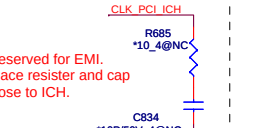
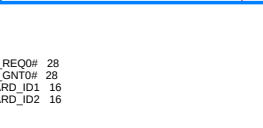
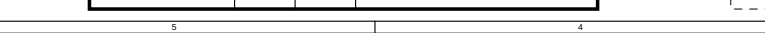
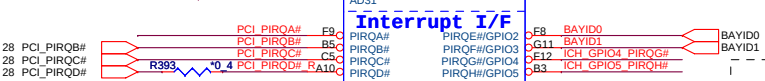
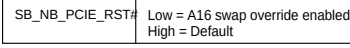
# XOR Chain Entrance Strap

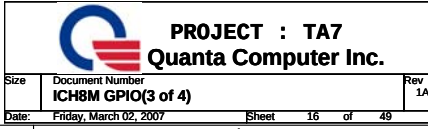
| ICH_RSVD | HDA_SDOUT | Description                |
|----------|-----------|----------------------------|
| 0        | 0         | RSVD                       |
| 0        | 1         | Enter XOR Chain            |
| 1        | 0         | Normal operation(Default)  |
| 1        | 1         | Set PCIE port config bit 1 |

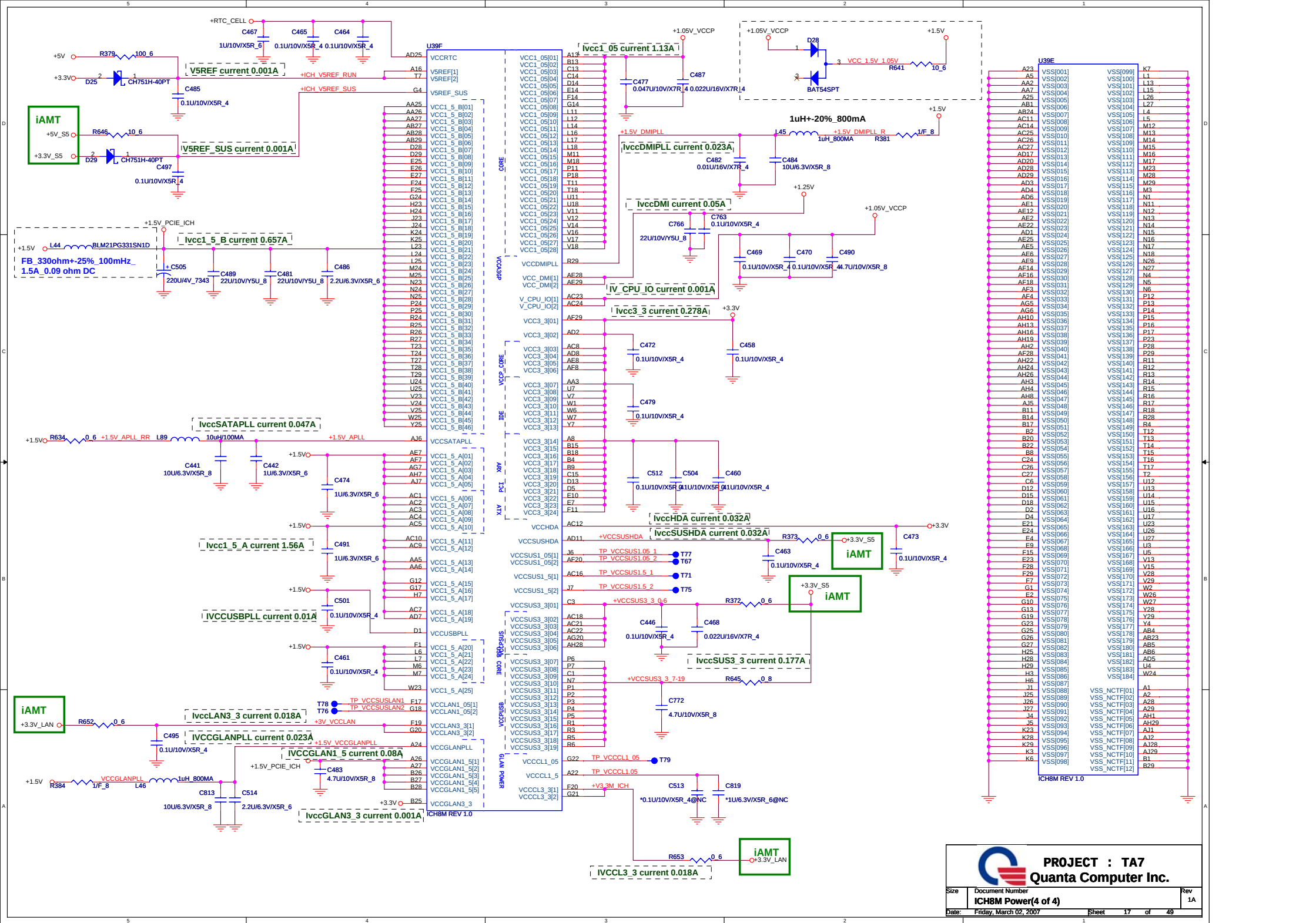


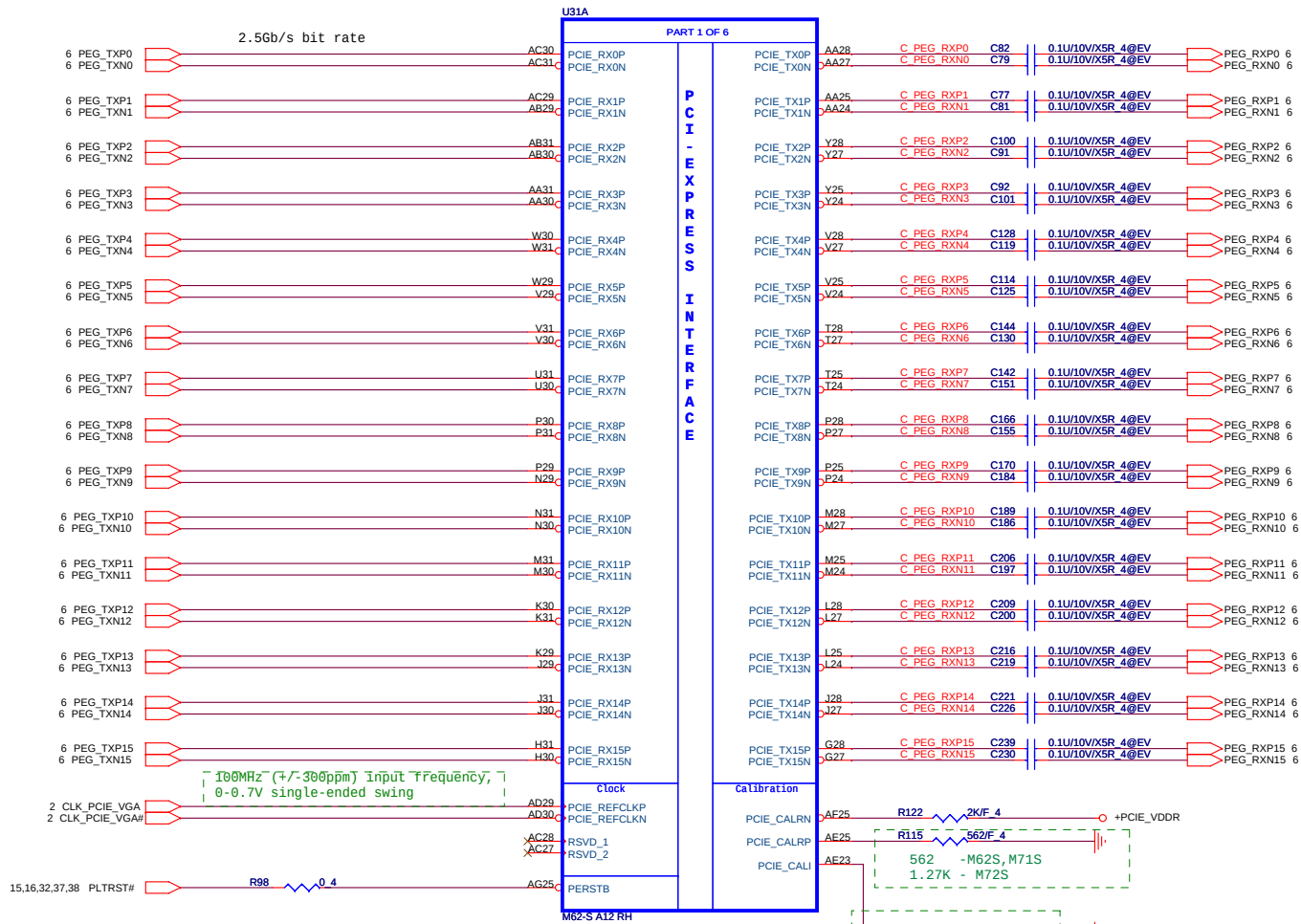


SPI\_CS# R R392 \*1K 4@NC  
PCI\_GNT0# R386 \*1K 4@NC



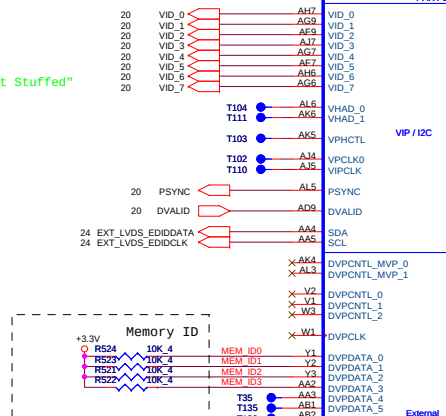






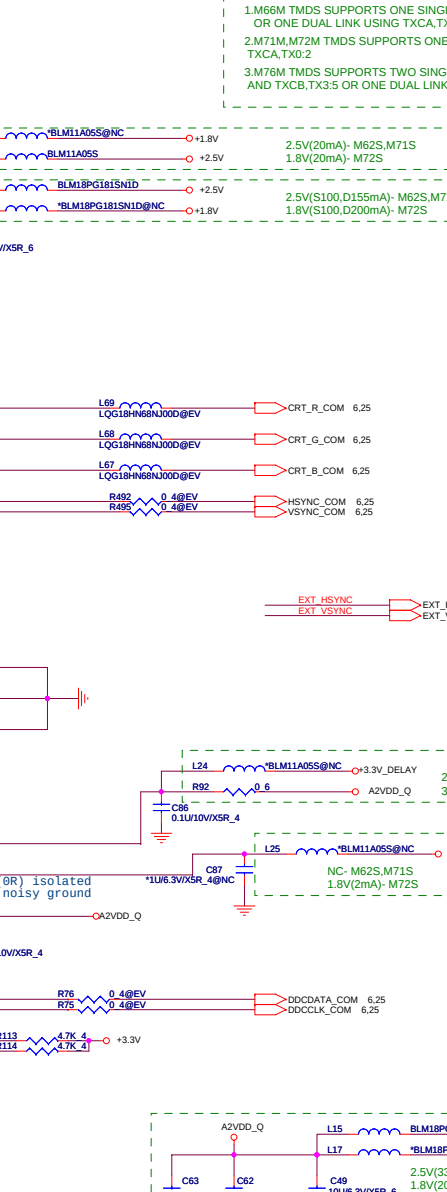
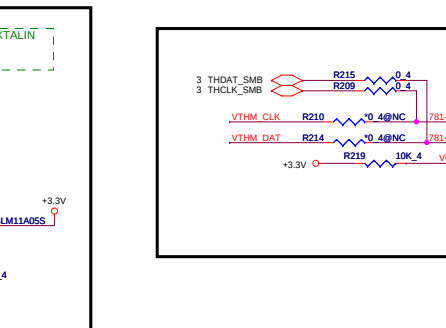
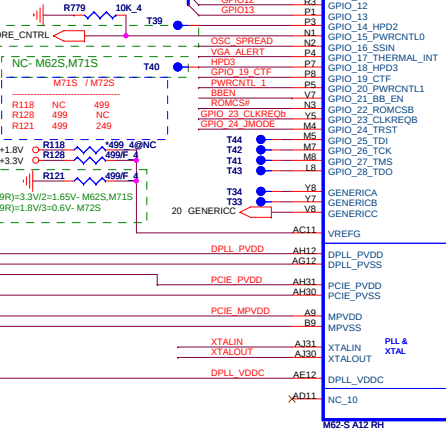
POWER  
+PCIE\_VDDR=1.2V  
+VDD\_MEM1.8V=1.8V  
+VGA\_CORE=1.0-1.1V - M62S, M71S  
0.95-1.1V - M72S





| Index | Label | Value      |
|-------|-------|------------|
| T32   | AK3   | DVPDATA_7  |
| T33   | AK1   | DVPDATA_8  |
| T38   | AK3   | DVPDATA_9  |
| T133  | AD1   | DVPDATA_10 |
| T132  | AD2   | DVPDATA_11 |
| T134  | AD3   | DVPDATA_12 |
| T126  | AK3   | DVPDATA_13 |
| T22   | AK3   | DVPDATA_14 |
| T18   | AK3   | DVPDATA_15 |
| T27   | AK1   | DVPDATA_16 |
| T121  | AH2   | DVPDATA_17 |
| T123  | AH1   | DVPDATA_18 |
| T113  | A35   | DVPDATA_19 |
| T112  | A11   | DVPDATA_20 |
| T122  | A12   | DVPDATA_21 |
| T114  | AK2   | DVPDATA_22 |
| T109  | AK3   | DVPDATA_23 |

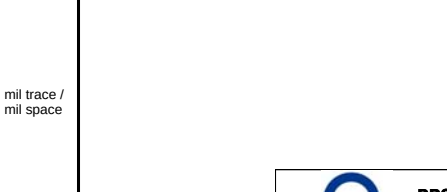
EXT LVDS\_BLON T5 GPIO\_0  
GPIO8 T7 GPIO\_7\_BLON  
GPIO9 T8 GPIO\_8\_ROMSO  
GPIO10 R1 GPIO\_9\_ROMSI  
GPIO11 P2 GPIO\_10\_ROMSCK



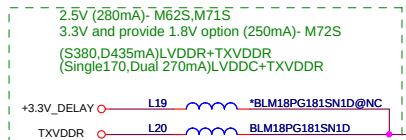
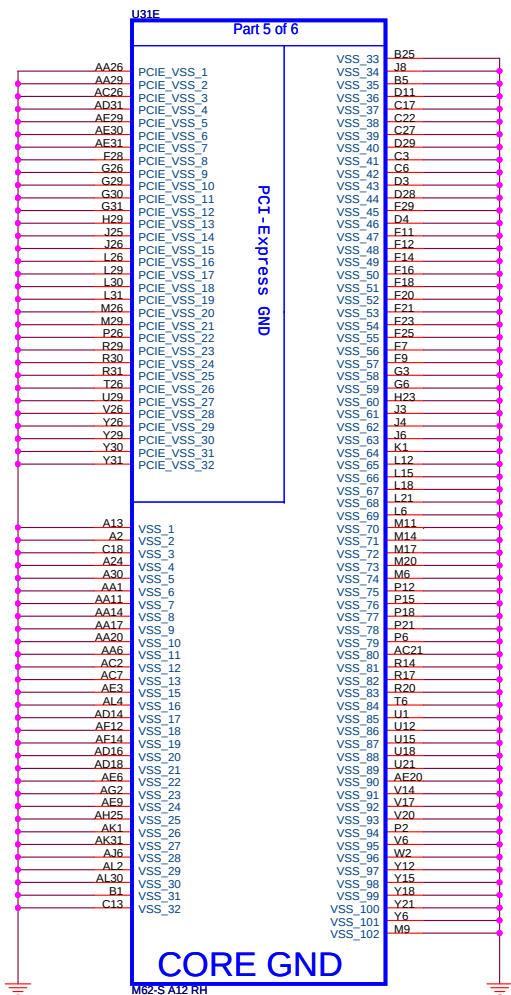
E LINK USING TXCA,TX0:2  
0:5

SINGLE LINK ONLY USING

E LINKS USING TXCA,TX0:2  
USING TXCA,TX0:5



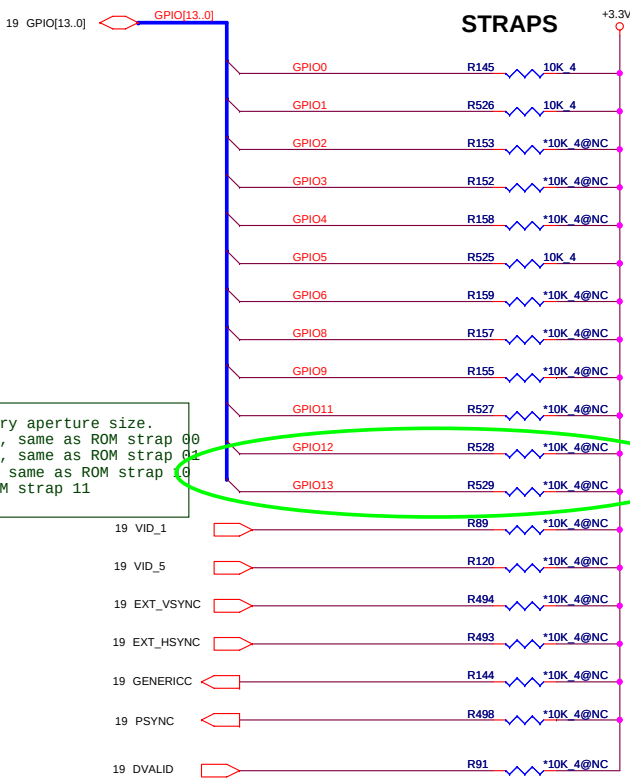




remove L23  
for normal work  
Mika 2006/11/30

2.5V(20mA)- M62S,M71S  
1.8V(20mA)- M72S

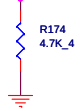
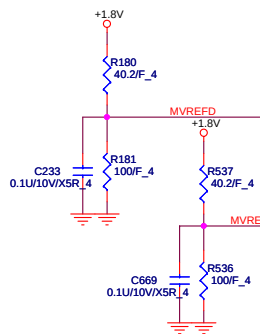
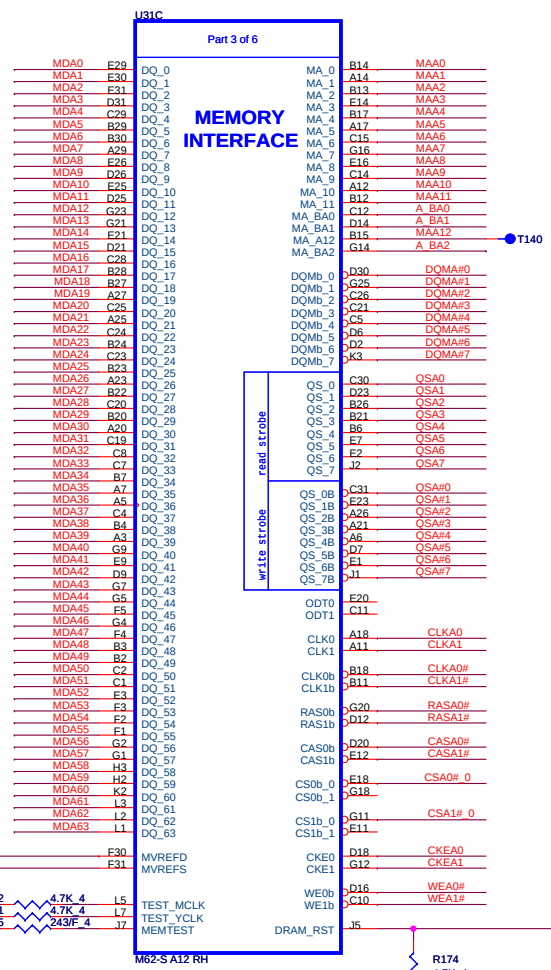
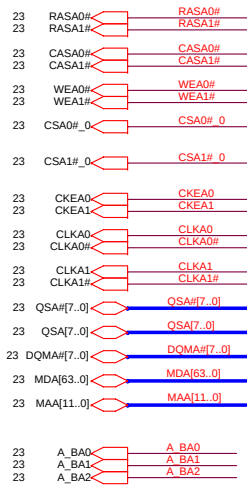
# STRAPS



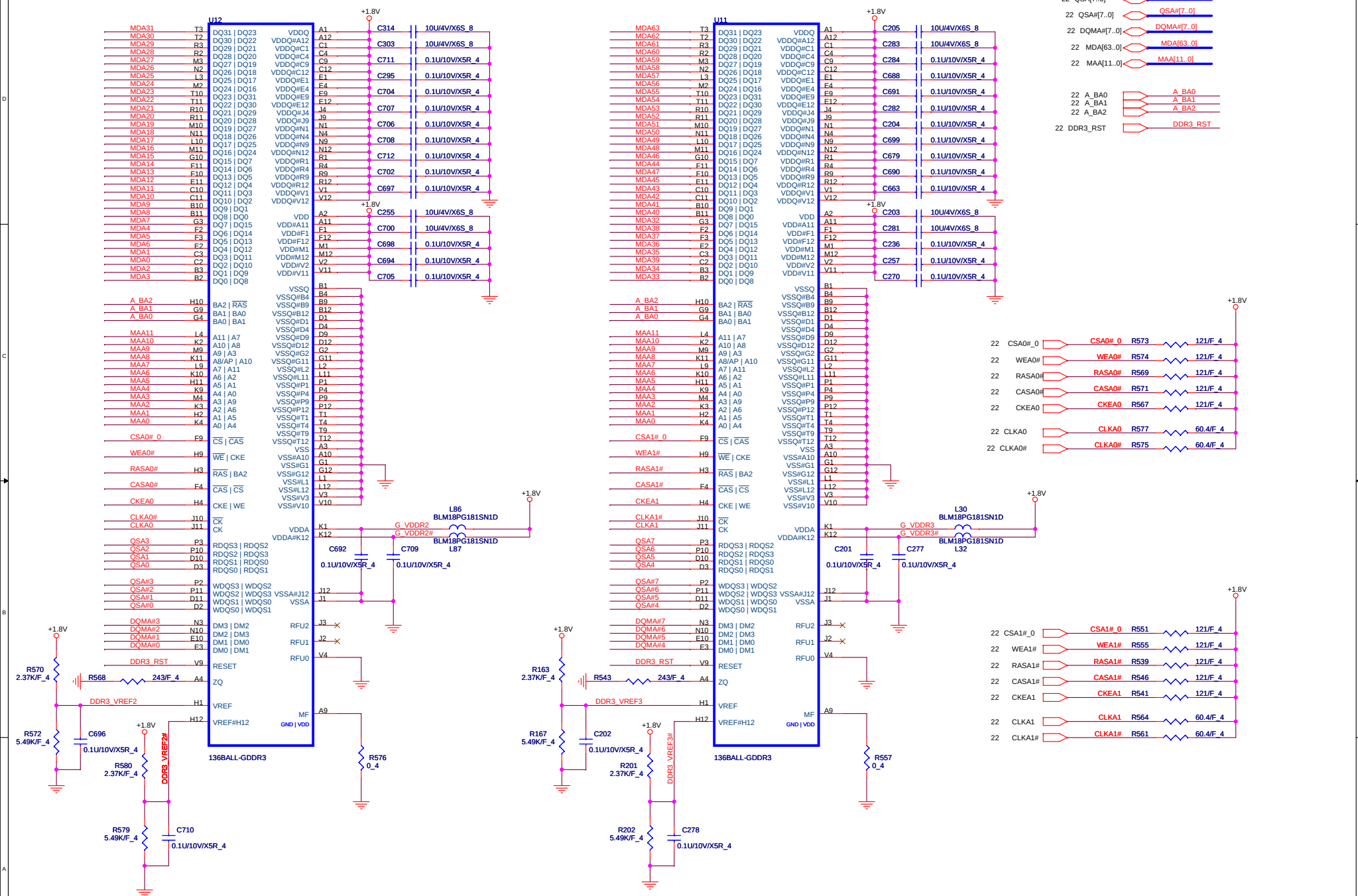
GPIO\_[13:12] is used to select the memory aperture size.  
GPIO\_[13:12] = 00: 128M memory aperture, same as ROM strap 00  
GPIO\_[13:12] = 01: 256M memory aperture, same as ROM strap 01  
GPIO\_[13:12] = 10: 64M memory aperture, same as ROM strap 10  
GPIO\_[13:12] = 11: reserved, same as ROM strap 11

| CONFIGURATION STRAPS                                                                                    |                        |                                                |                      |      |
|---------------------------------------------------------------------------------------------------------|------------------------|------------------------------------------------|----------------------|------|
| ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET |                        |                                                |                      |      |
| STRAPS                                                                                                  | PIN                    | DESCRIPTION OF DEFAULT SETTINGS                | RECOMMENDED SETTINGS |      |
|                                                                                                         |                        |                                                | M62S,M71S            | M72S |
| BIF_MSI_DIS                                                                                             | VID1                   | MESSAGE SIGNAL INTERRUPT ENABLED               | 0                    | 0    |
| BIF_64BAR_EN_A                                                                                          | VID5                   | 64 BIT BARS DISABLED                           | 0                    | 0    |
| TX_PWRS_ENB                                                                                             | GPIO0                  | PCIE FULL TX OUTPUT SWING                      | 1                    | 1    |
| TX_DEEMPH_EN                                                                                            | GPIO1                  | PCIE TRANSMITTER DE-EMPHASIS ENABLED           | 1                    | 1    |
| BIF_DEBUG_ACCESS                                                                                        | GPIO4                  | DEBUG SIGNALS NOT MUXED OUT                    | 0                    | 0    |
| PLL_IBIAS_RD_1:0                                                                                        | GPIO[6:5]              | BIAS CURRENT FOR PCIE PHY PLL                  | X X                  | X X  |
| ROMIDCFG(3:0)                                                                                           | GPIO[13:11,9]          | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT |                      |      |
| VIP_DEVICE_STRAP_ENA                                                                                    | VSYN                   | IGNORE VIP DEVICE STRAPS                       | 0                    | 0    |
| BIF_VGA_DIS                                                                                             | PSYN                   | VGA ENABLED                                    | 0                    | 0    |
|                                                                                                         | GPIO8                  | Reserved                                       |                      |      |
|                                                                                                         | GPIO[2:3]              | Reserved                                       |                      |      |
|                                                                                                         | H2SYN, V2SYN, GENERICC | Reserved                                       |                      |      |





## DDR3 BGA MEMORY

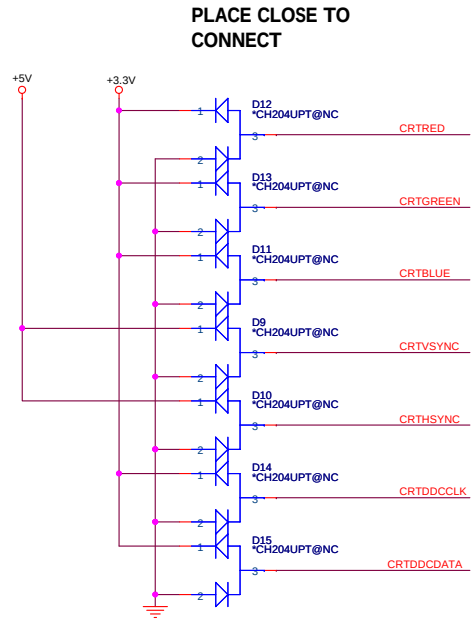
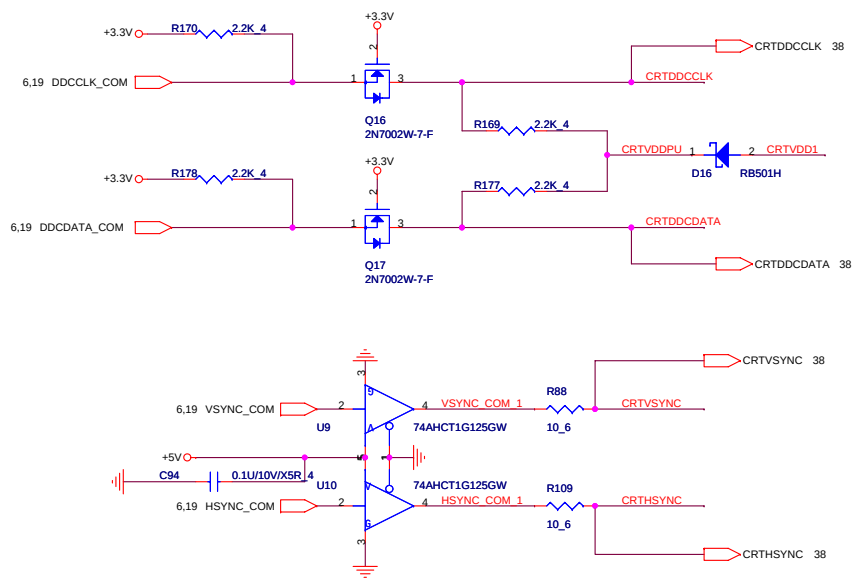


22 QSA[7..0] QSA[7..0]  
22 QSA[7..0] QSA[7..0]  
22 DQMA[7..0] DQMA[7..0]  
22 MDA[63..0] MDA[63..0]  
22 MAA[11..0] MAA[11..0]  
22 A\_BA0 A\_BA0  
22 A\_BA1 A\_BA1  
22 A\_BA2 A\_BA2  
22 DDR3\_RST DDR3\_RST

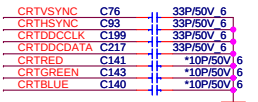
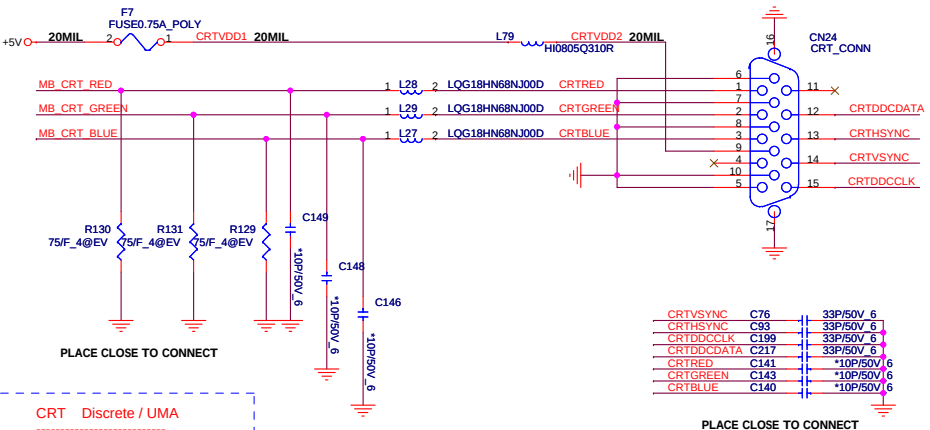
22 CSA0#\_0 CSA0#\_0 R573 121/F 4  
22 WEA0# WEA0# R574 121/F 4  
22 RASA0# RASA0# R569 121/F 4  
22 CASA0# CASA0# R571 121/F 4  
22 CKEA0 CKEA0 R567 121/F 4  
22 CLKA0 CLKA0 R577 60.4/F 4  
22 CLKA0# CLKA0# R575 60.4/F 4

22 CSA1#\_0 CSA1#\_0 R551 121/F 4  
22 WEA1# WEA1# R555 121/F 4  
22 RASA1# RASA1# R539 121/F 4  
22 CASA1# CASA1# R546 121/F 4  
22 CKEA1 CKEA1 R541 121/F 4  
22 CLKA1 CLKA1 R564 60.4/F 4  
22 CLKA1# CLKA1# R561 60.4/F 4





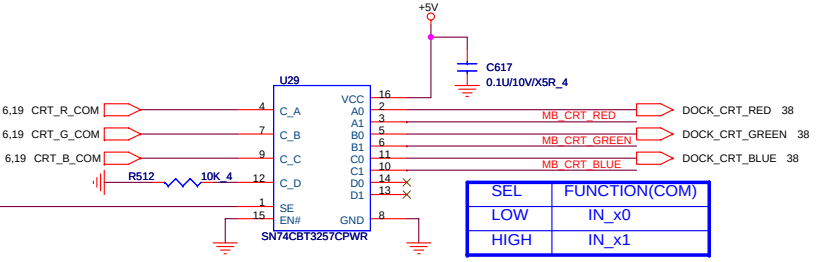
### CRT PORT



CRT Discrete / UMA

R130 75R 150R  
R131 75R 150R  
R129 75R 150R

Termination Resistor



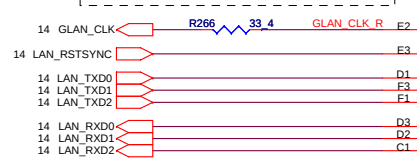
| SEL  | FUNCTION(COM) |
|------|---------------|
| LOW  | IN_x0         |
| HIGH | IN_x1         |



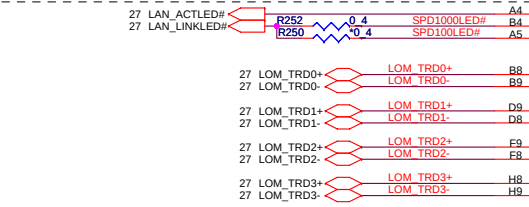
# LAN

|            |         |
|------------|---------|
| JKCLK Pin  | 0MHz    |
| Power down | 5MHz    |
| 10Mbps     | 50MHz   |
| 100Mbps    | 62.5MHz |
| 1000Mbps   |         |

Layout Note:  
Place series resistor close to LAN controller.



Layout Note:  
Place the resistors less than 1" from LAN controller.

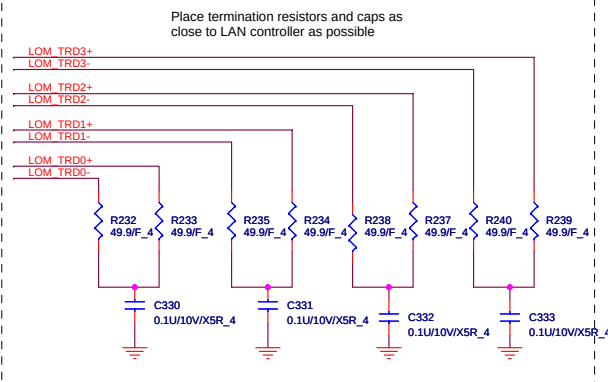


Layout Note:  
Connect the resistor to GND near ball E6

Test Mode Enable  
Strap low for normal operation  
82566 100-200 pull down for normal operation  
82562 200 pull down for normal operation

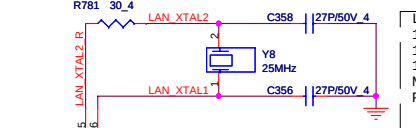
82562V and 82566MM  
R245, R254 NC

82566MM  
1. R232-R235, R237-R240 --- 49.9F (CS04992FB31).  
2. C330-C333 --- 0.1U.

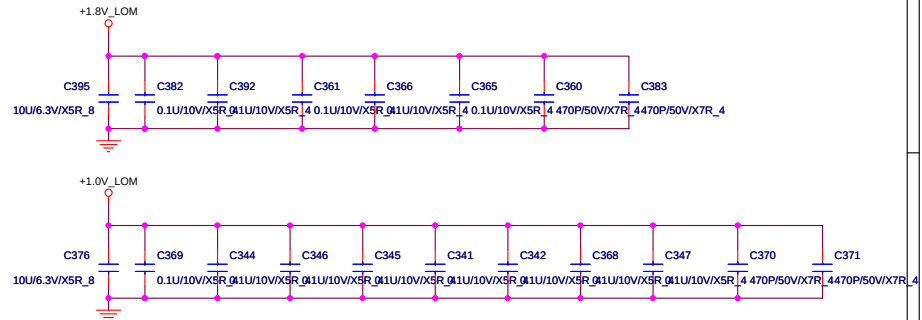
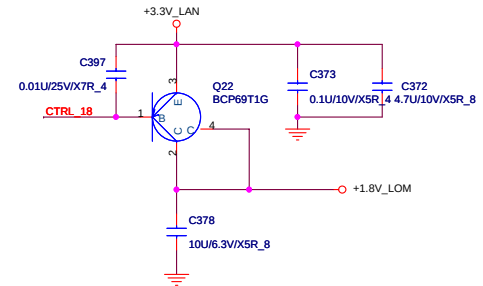
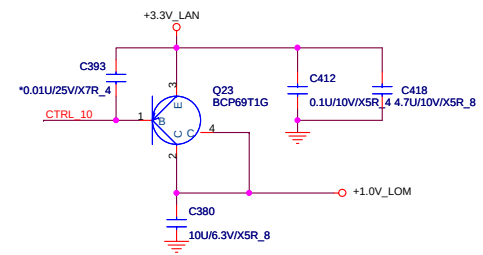


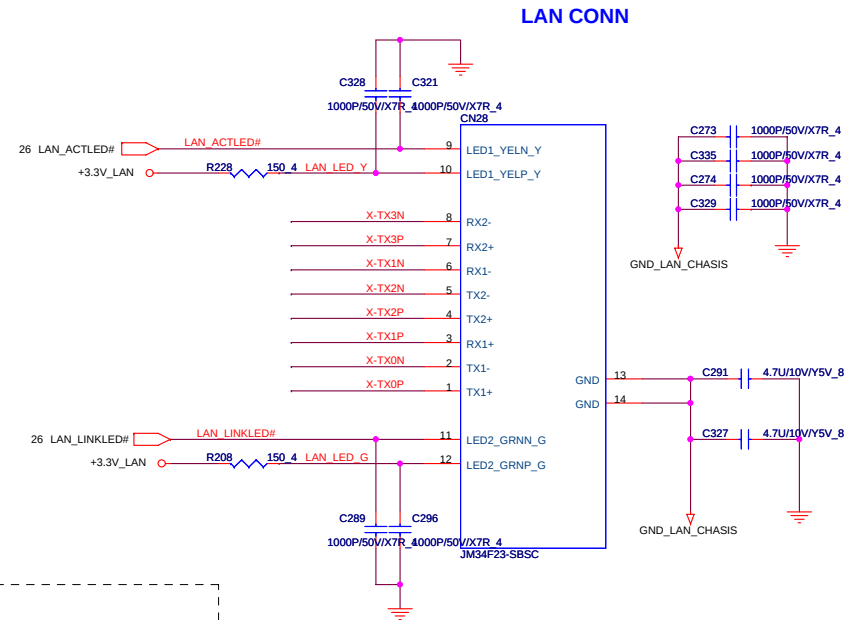
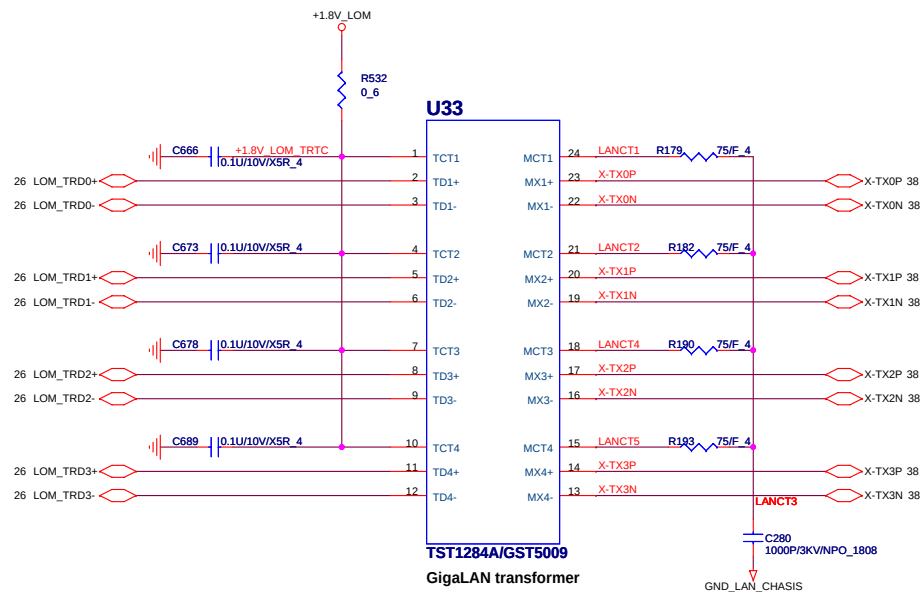
need FAE support  
82562 question  
(mode select)

add R781 30 ohm  
for Intel suggestion  
Mika 2007/02/14

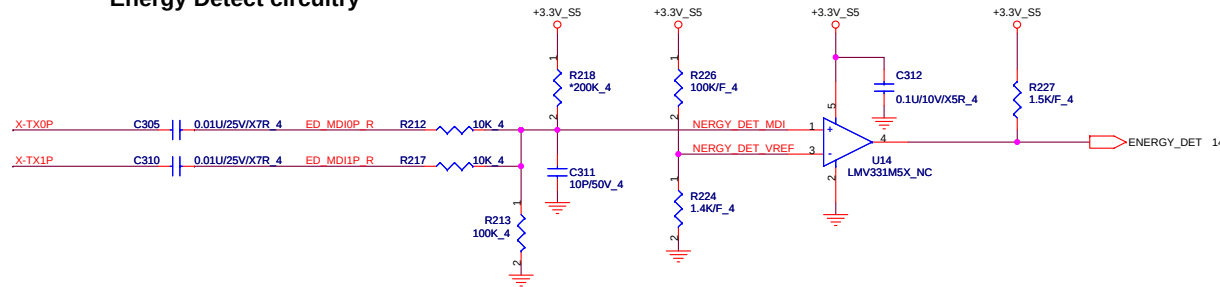


|            |                      |            |
|------------|----------------------|------------|
| Link Speed | LCI                  | GLCI       |
| 1000Mbps   | Runing               | Runing     |
| 100Mbps    | Runing               | Runing     |
| 10Mbps     | Runing               | Idle       |
| No Link    | Runing or power down | Idle       |
| Power down | Power down           | Power down |



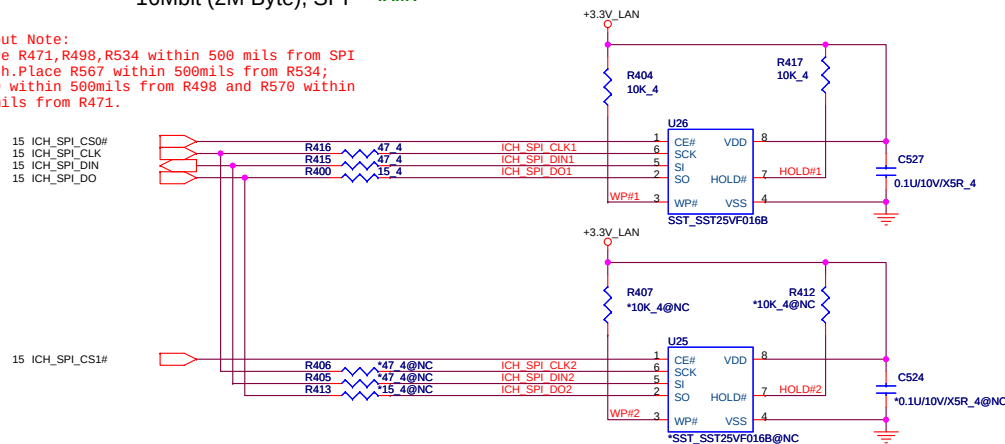


### Energy Detect circuitry

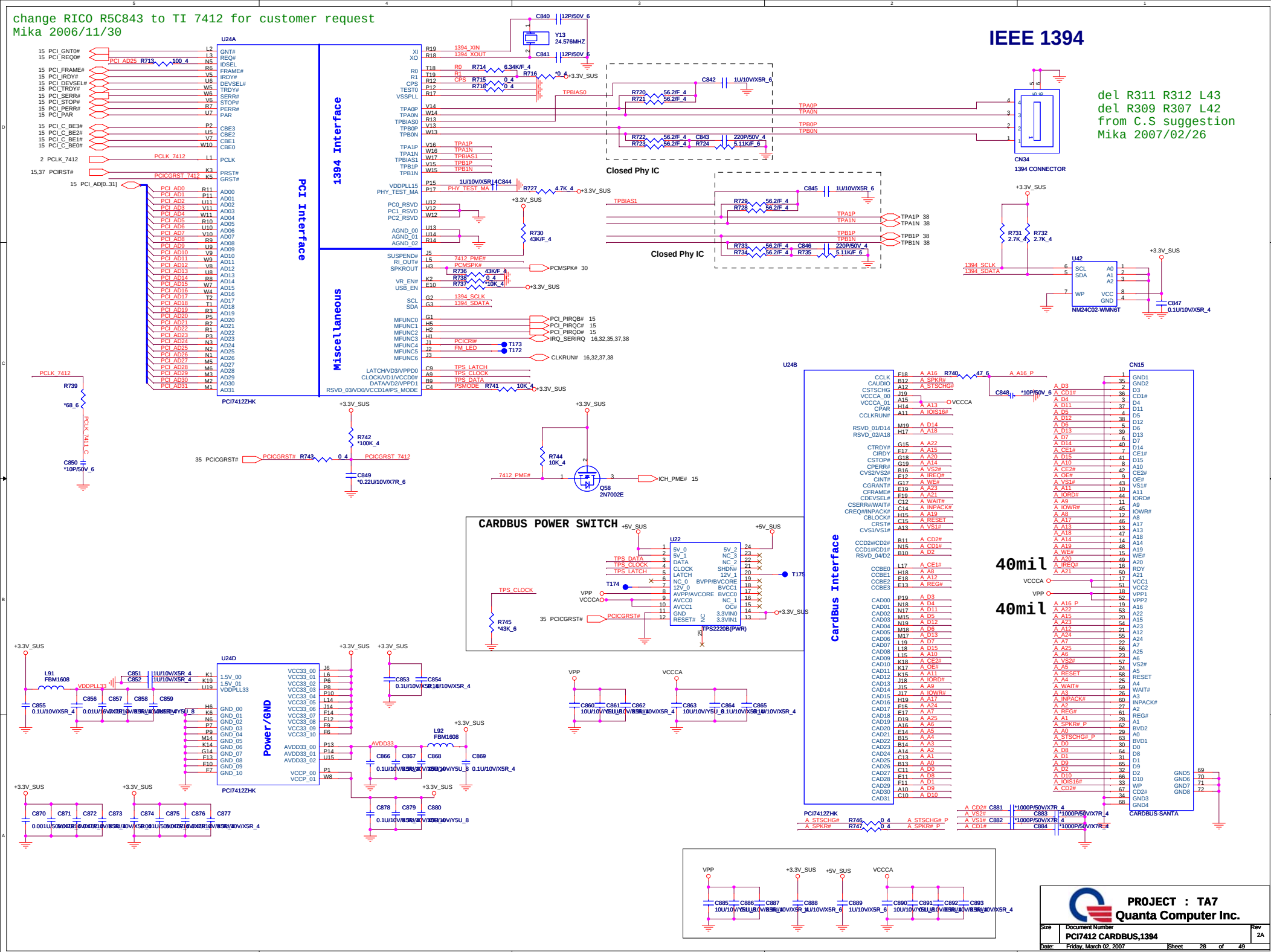


### 16Mbit (2M Byte), SPI iAMT

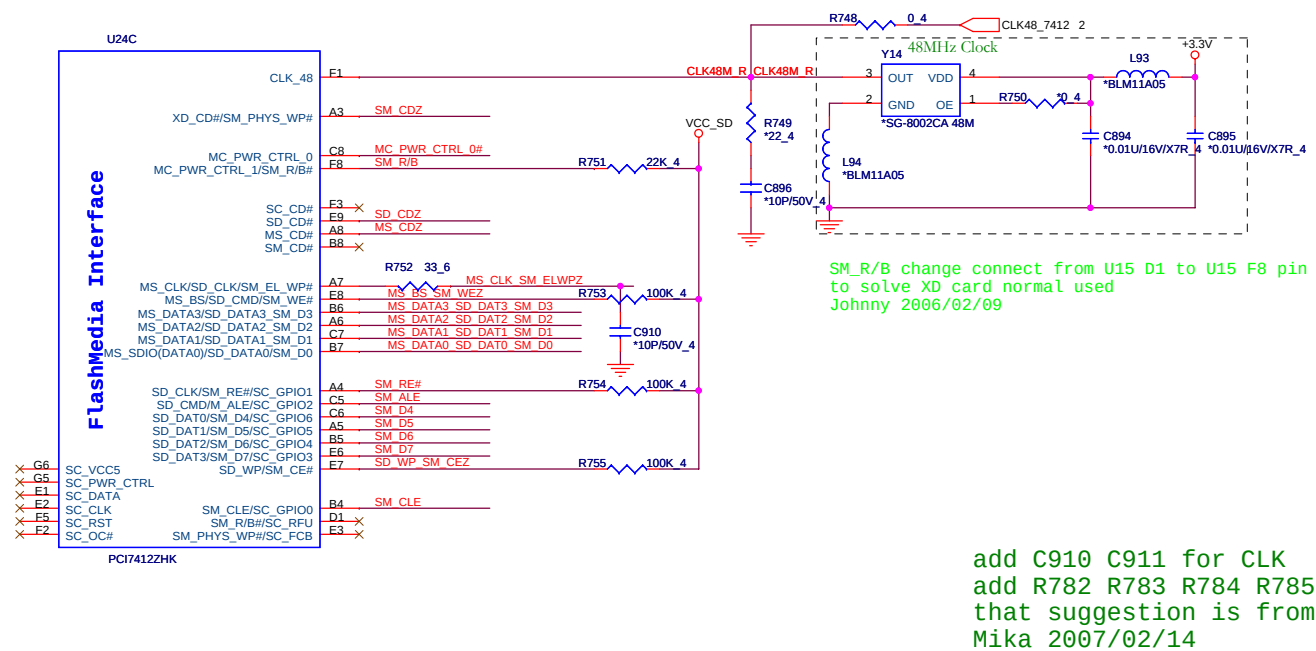
**Layout Note:**  
Place R471, R498, R534 within 500 mils from SPI  
Flash. Place R567 within 500mils from R534;  
R520 within 500mils from R498 and R570 within  
500mils from R471.



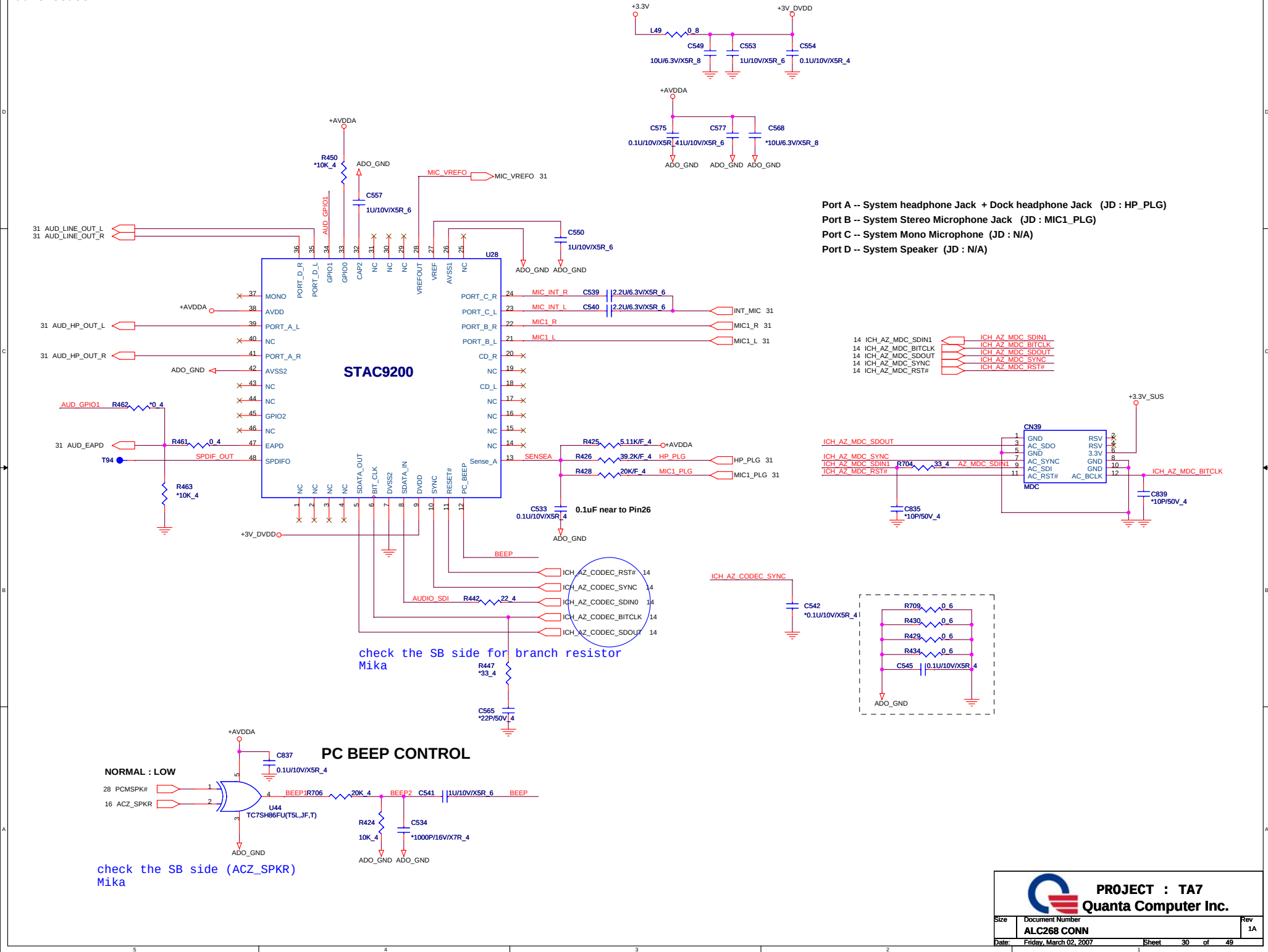
```
change RICO R5C843 to TI 7412 for customer request
Mika 2006/11/30
```



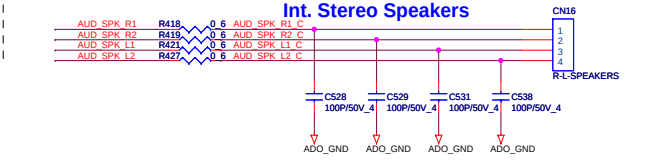
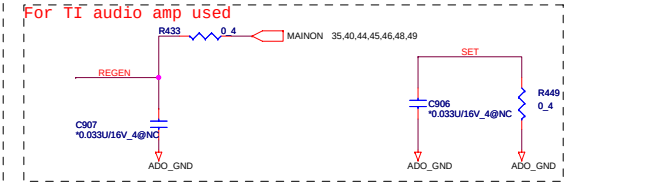
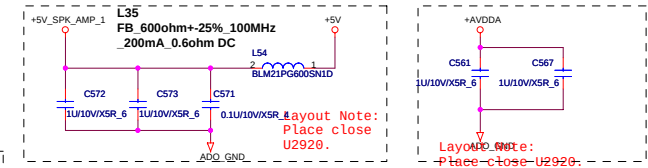
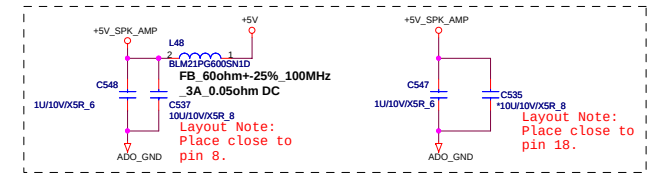
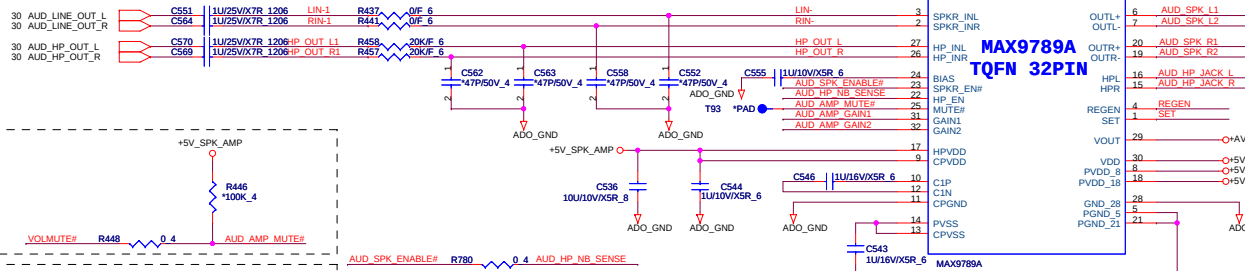
change RICO R5C843 to TI 7412 for customer request  
Mika 2006/11/30



Audio codec

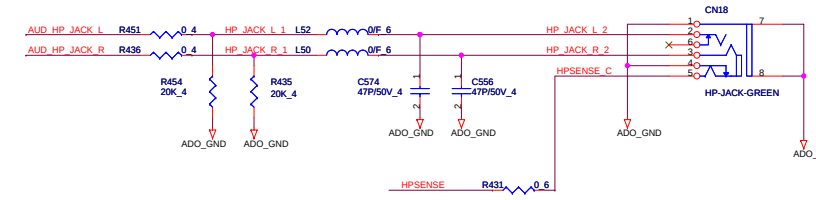


# AUDIO AMPLIFIER

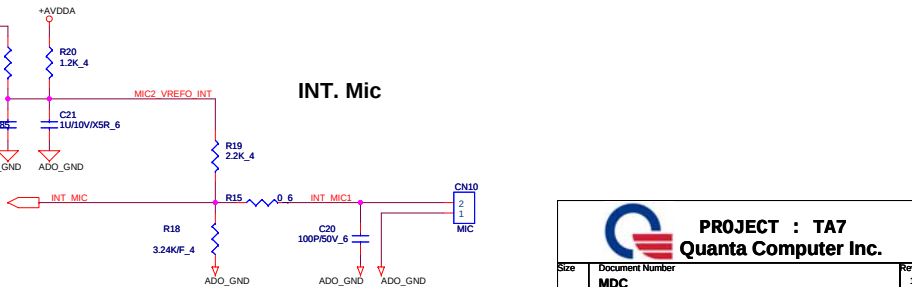
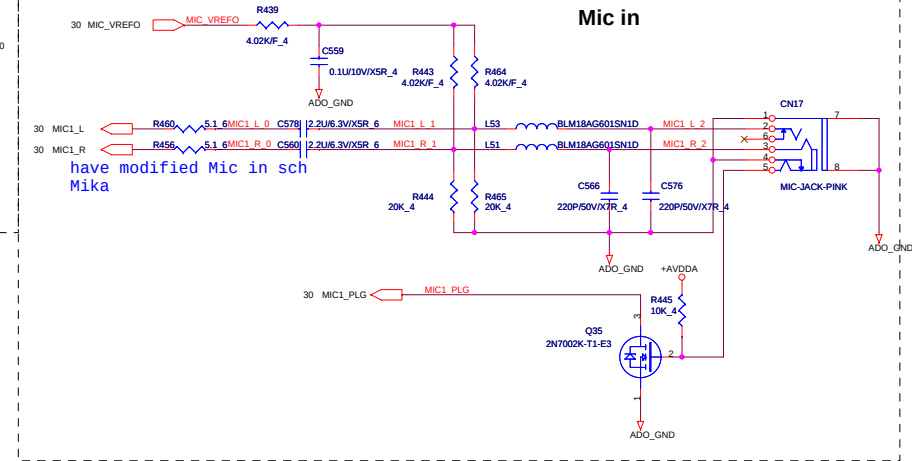
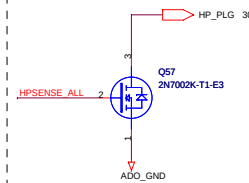


remove Q37 Q38 R438 R446 U45  
add R448 R705 R780  
change R437 R441 to 0ohm  
change C551 C564 C569 C570 to 1u  
solve audio bo sound Mika 2007/02/14

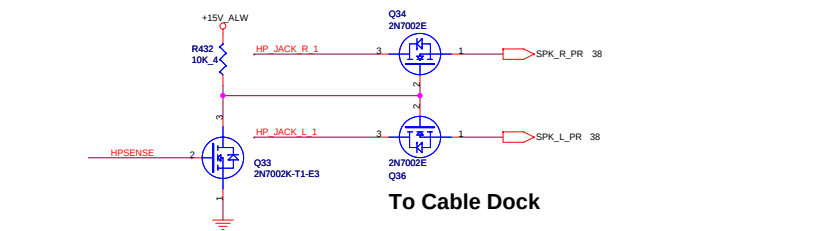
## Headphone out



L50 L52 P/N change to 0\_0603(CS00003F916)  
MIKA 2007/01/04



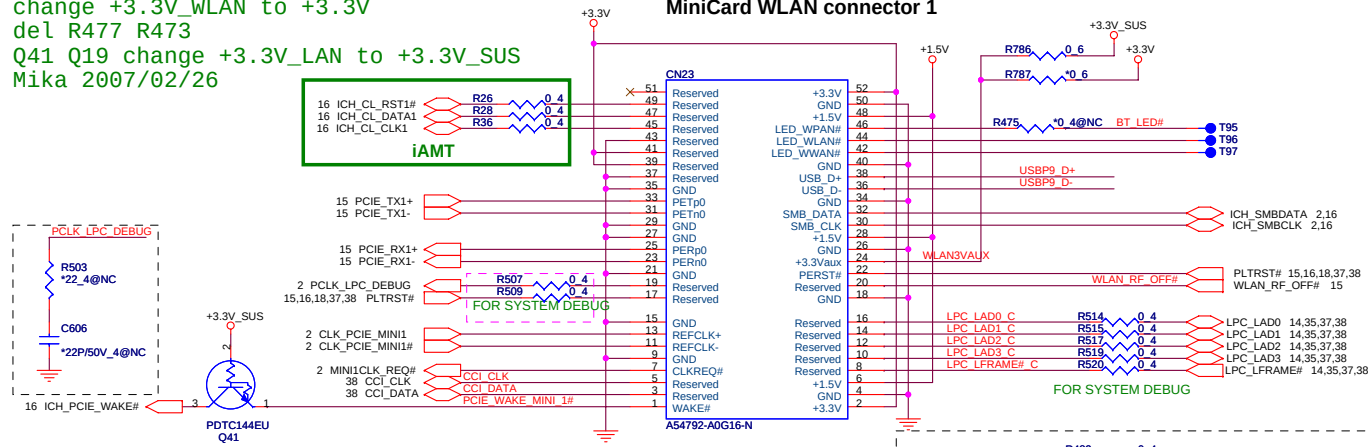
## To Cable Dock





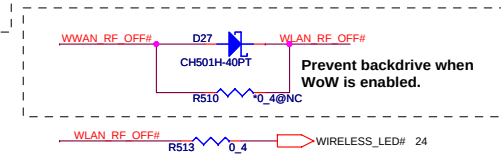
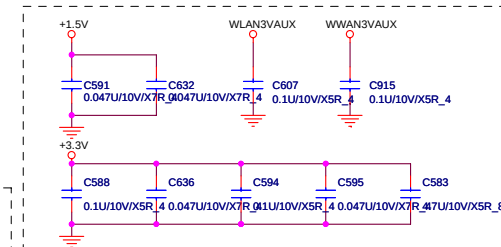
change +3.3V\_WLAN to +3.3V  
del R477 R473  
Q41 Q19 change +3.3V\_LAN to +3.3V\_SUS  
Mika 2007/02/26

### MiniCard WLAN connector 1



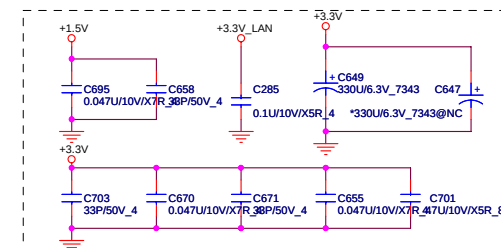
del R491 R486 Q39 Q40  
and directly connect both signal  
Mika 2007/02/26

add R786 R787 for select power  
Mika 2007/02/26

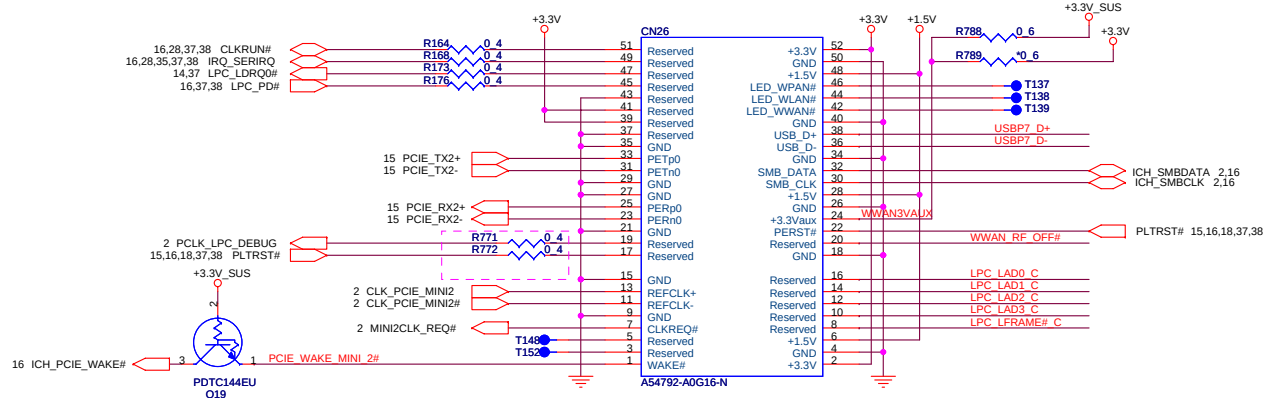


del R542 R538 Q42 Q43  
and directly connect both signal  
Mika 2007/02/26

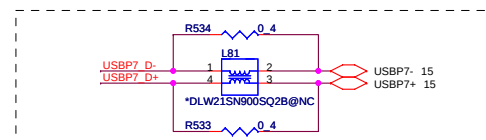
add R788 R789 for select power  
add C915 for WWAN3VAUX  
Mika 2007/02/26

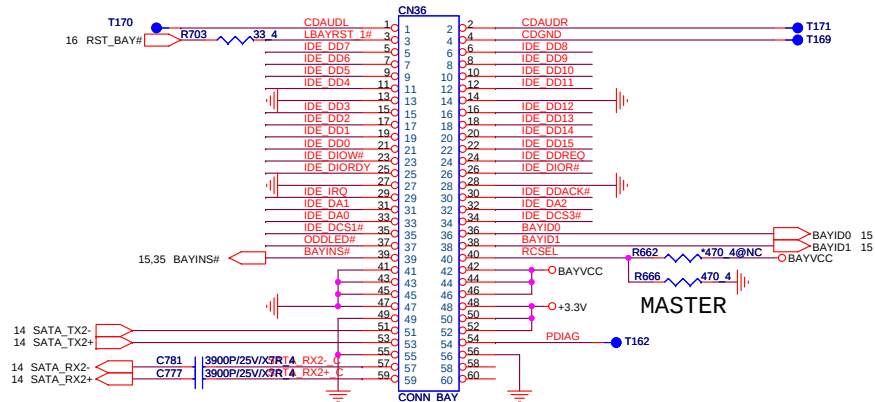
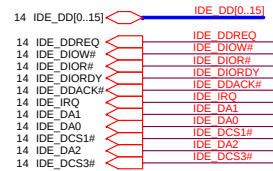
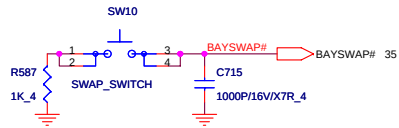


### MiniCard WWAN connector 2



add R771 R772  
for Debug card used  
Mika 2006/11/30

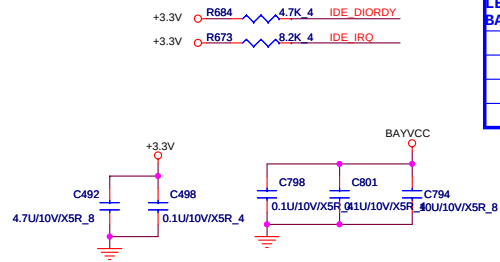




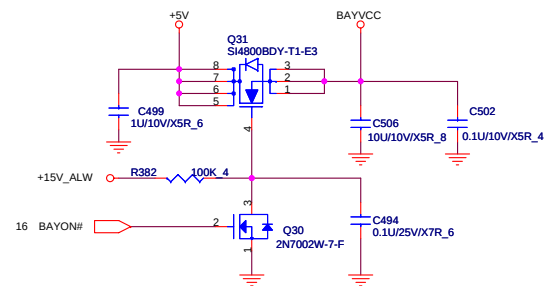
MASTER

### LBAY ID STATUS

| LEFT BAYID1 | LEFT BAYID0 | STATUS  |
|-------------|-------------|---------|
| 0           | 0           | Reserve |
| 0           | 1           | ODD     |
| 1           | 0           | Reserve |
| 1           | 1           | Reserve |

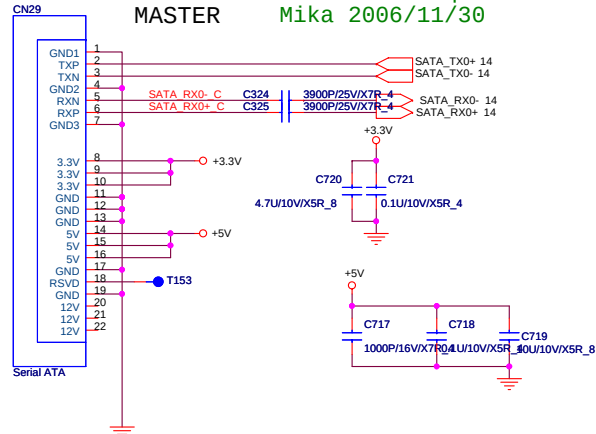


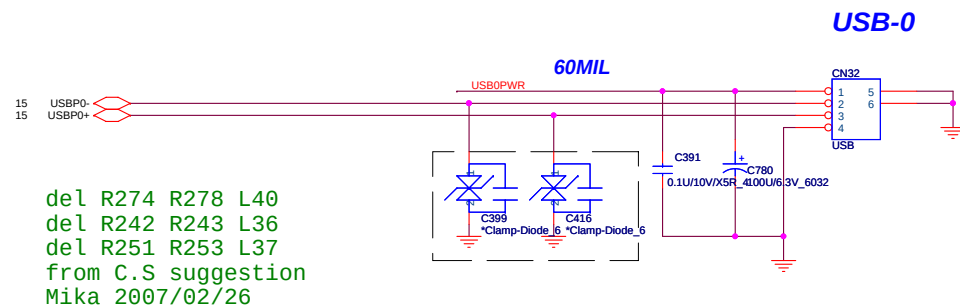
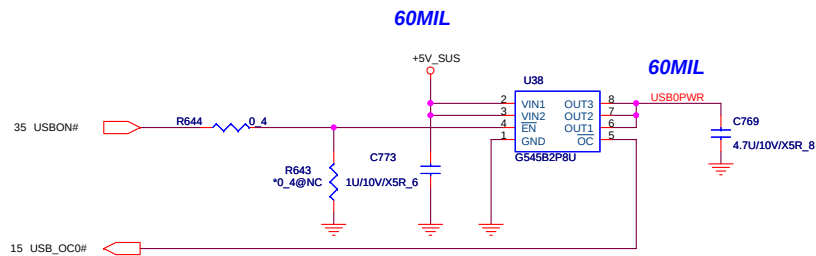
### BAY POWER CONTROL



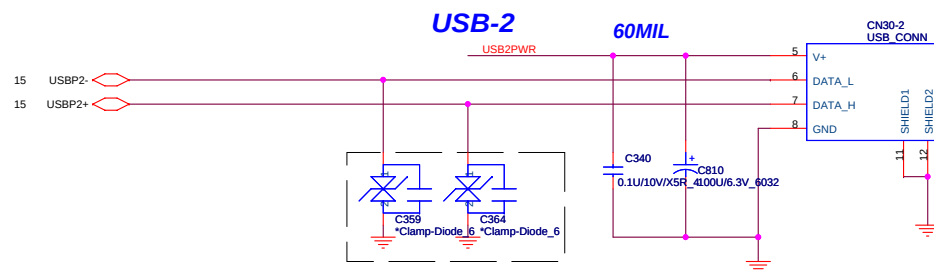
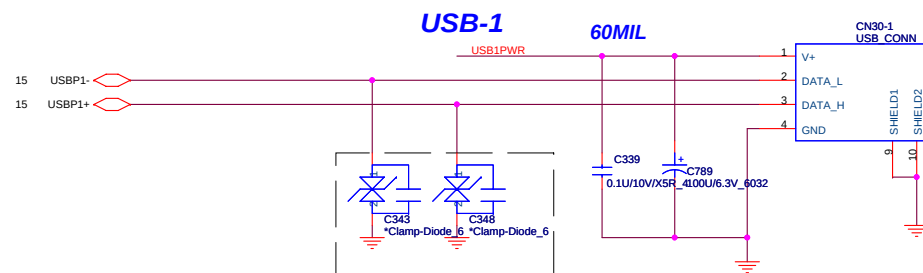
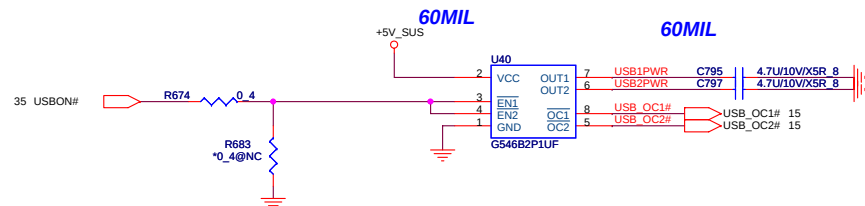
### SATA CONNECTOR

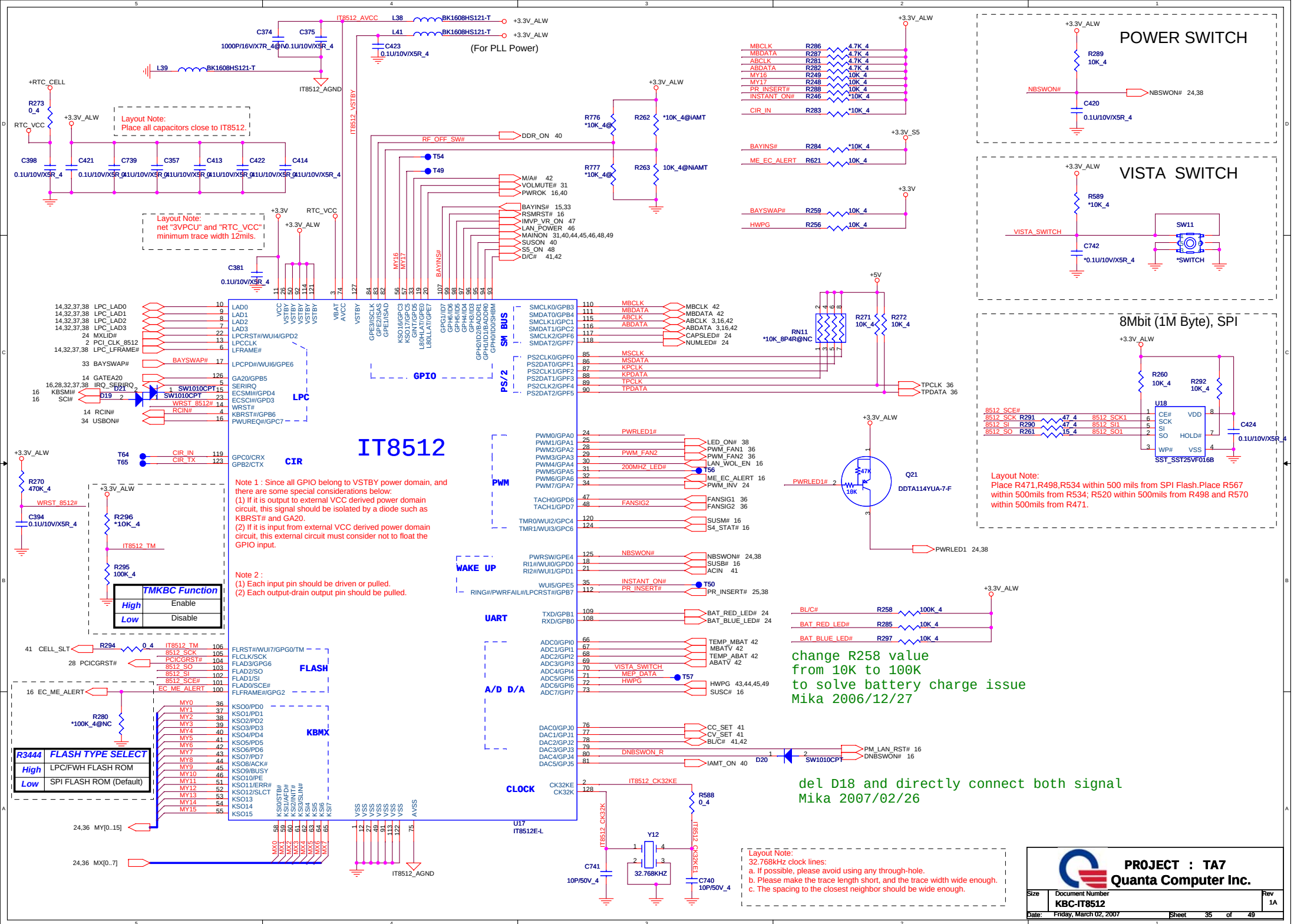
change SATA connector for M1 ME request  
Mika 2006/11/30



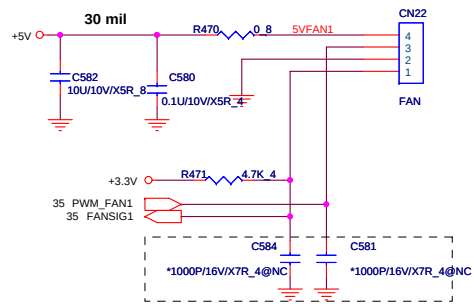


del R274 R278 L40  
del R242 R243 L36  
del R251 R253 L37  
from C.S suggestion  
Mika 2007/02/26

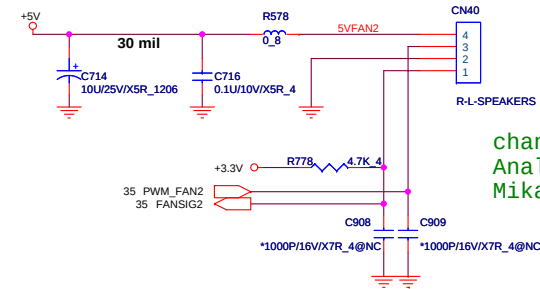




## CPU FAN

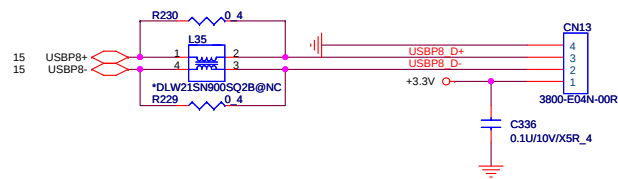


## Second FAN for Discrete VGA

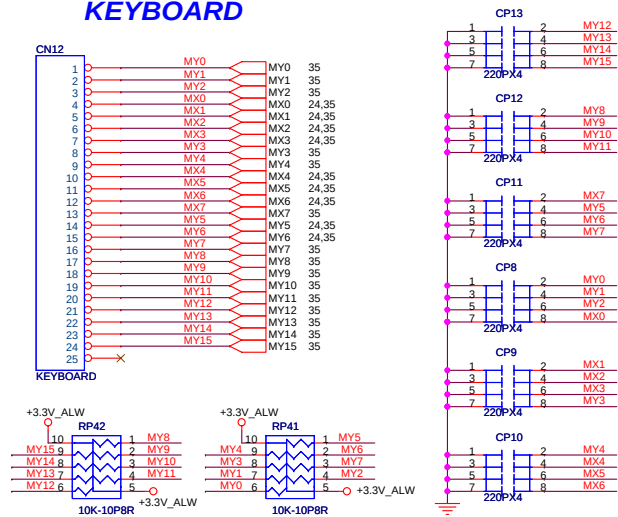


change FAN type from  
Analog to PWM  
Mika 2006/12/26

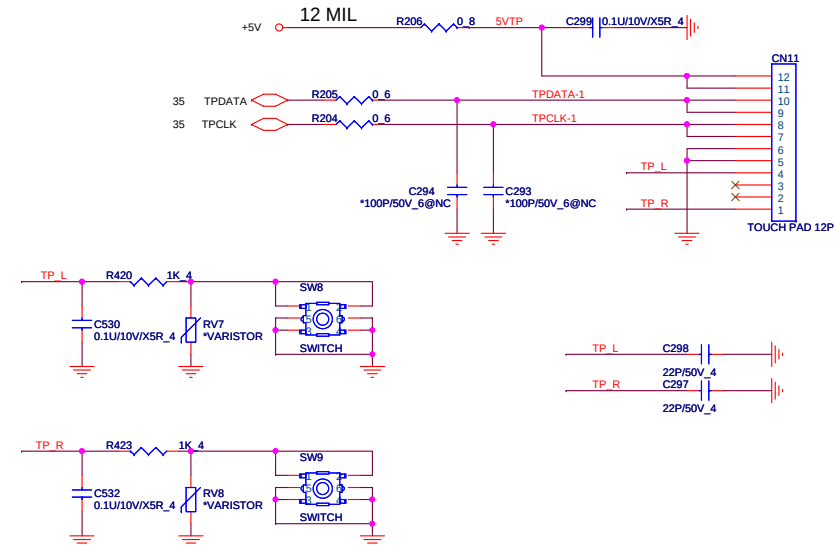
**FINGER PRINT CONN**



## KEYBOARD

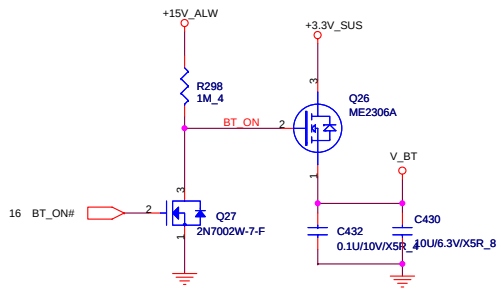


***TOUCHPAD CONN***

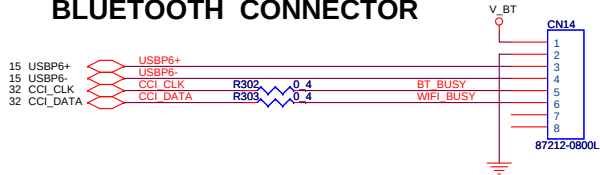




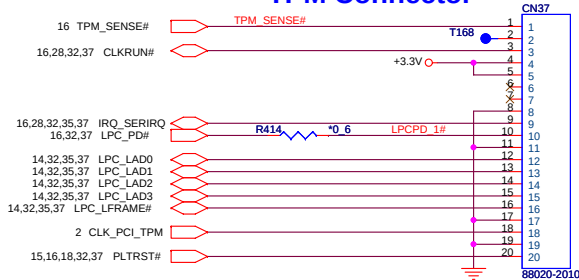




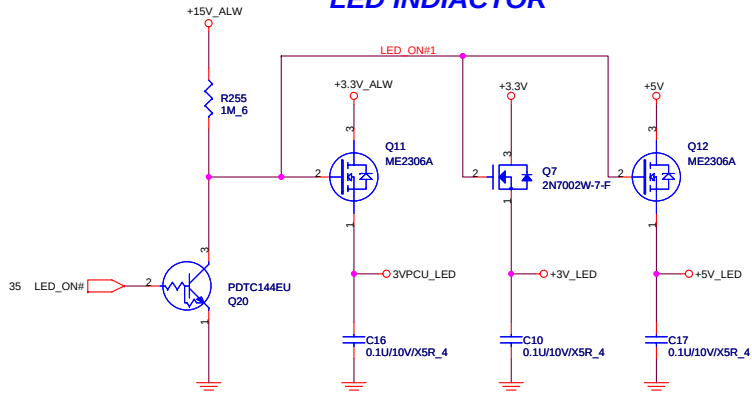
## BLUETOOTH CONNECTOR



## TPM Connector

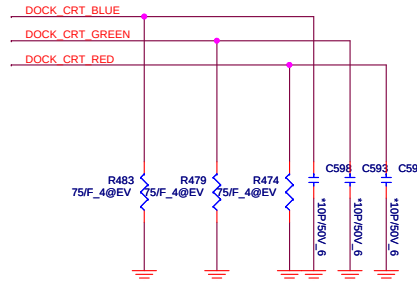
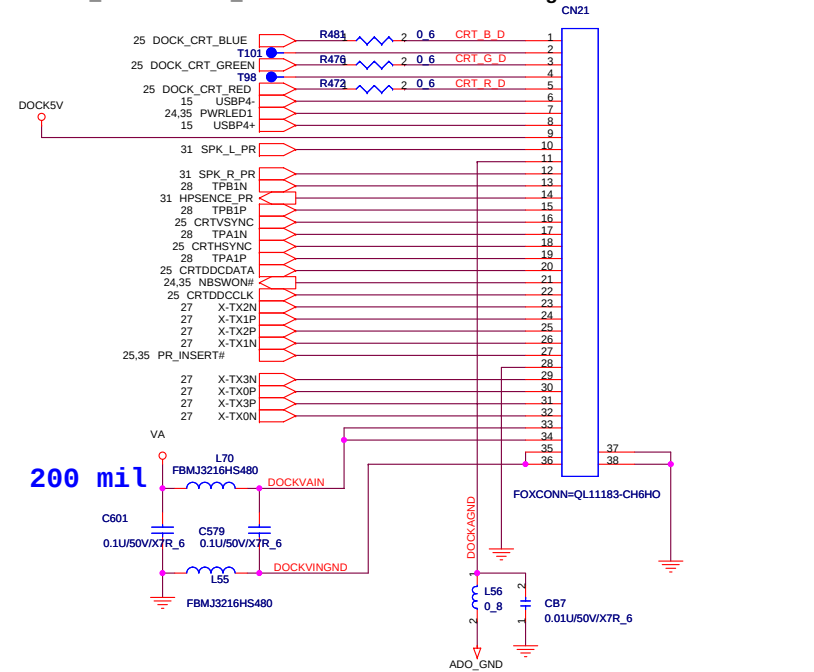


## LED INDIATOR



## CABLE DOCK

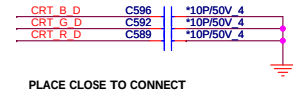
DOCK\_ID1# & DOCK\_ID2# don't use on Cable docking



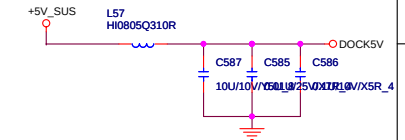
PLACE CLOSE TO CONNECT

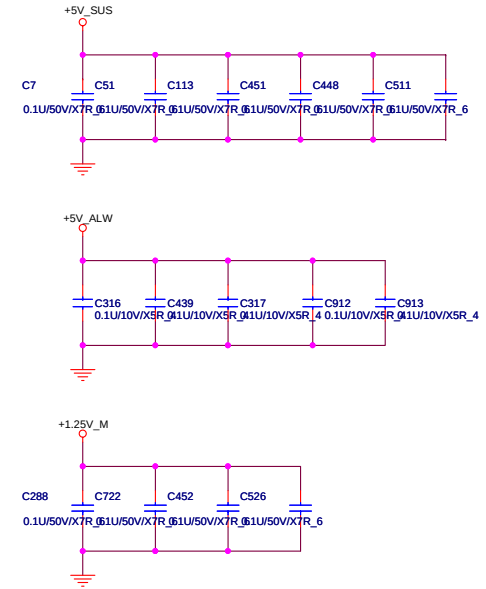
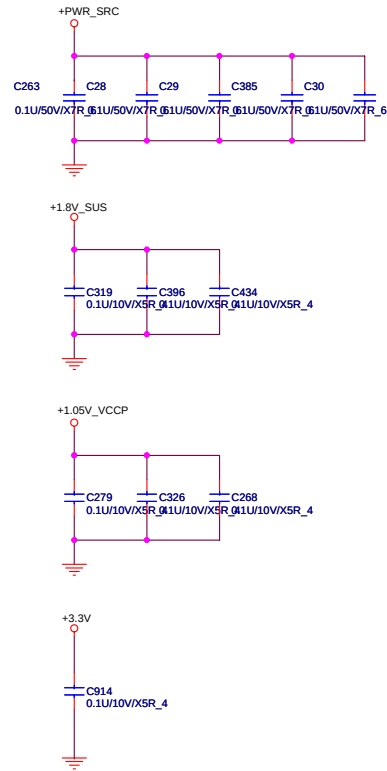
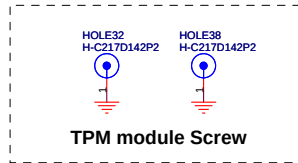
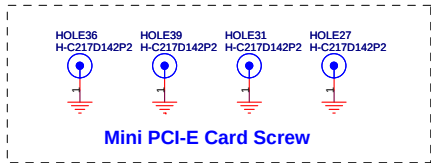
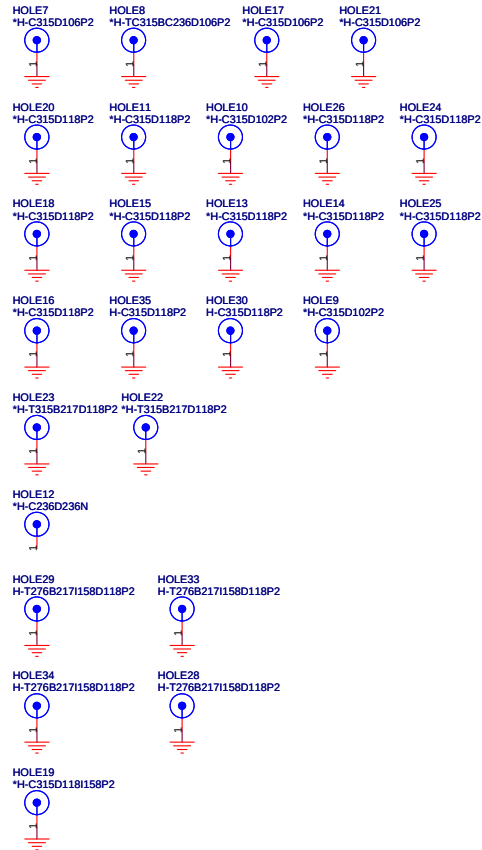
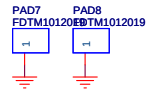
| CRT  | Discrete / UMA |
|------|----------------|
| R483 | 75R 150R       |
| R479 | 75R 150R       |
| R474 | 75R 150R       |

Termination Resistor

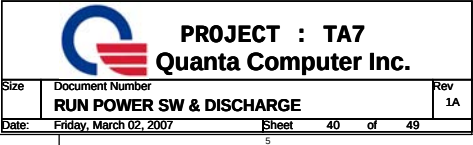


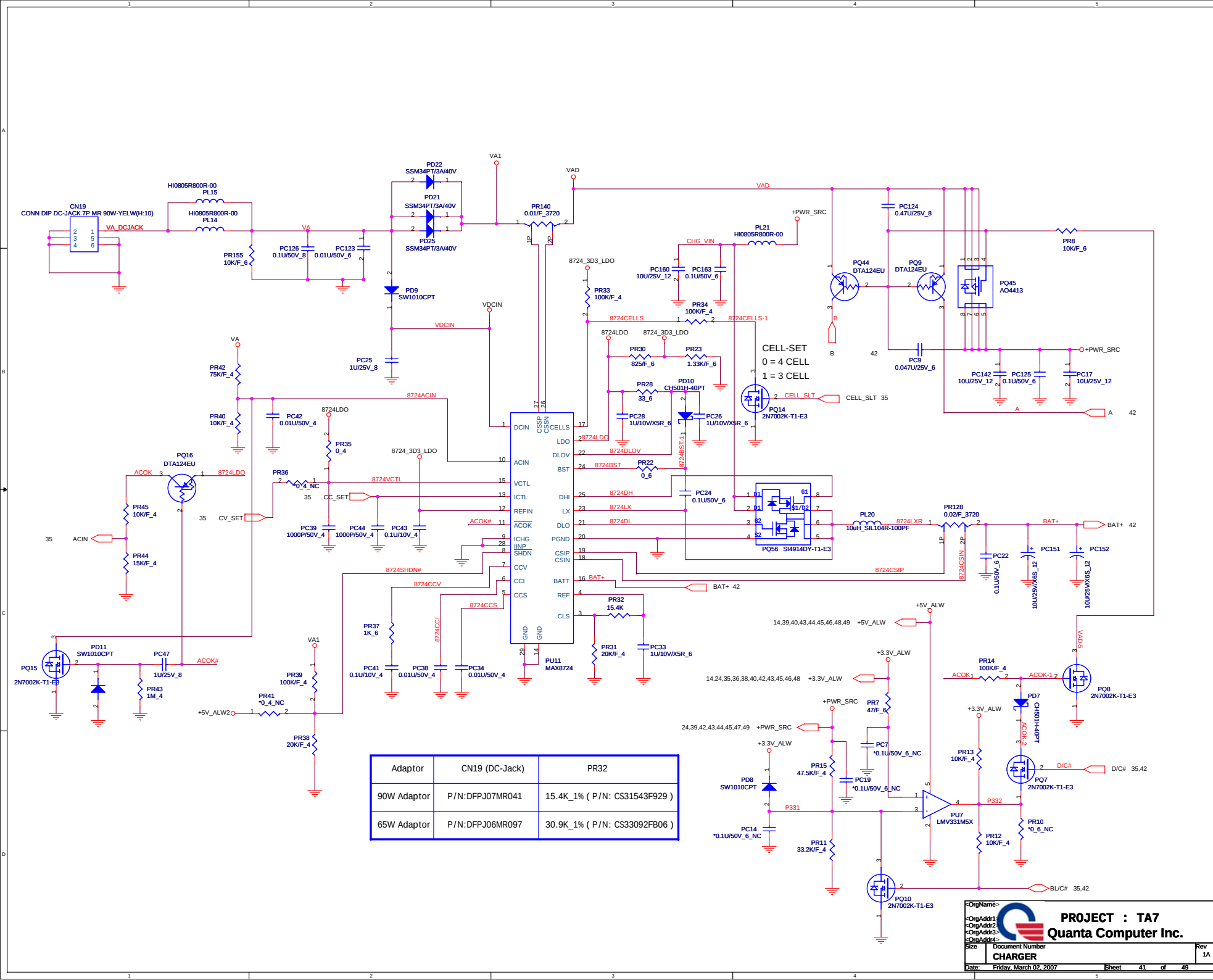
PLACE CLOSE TO CONNECT

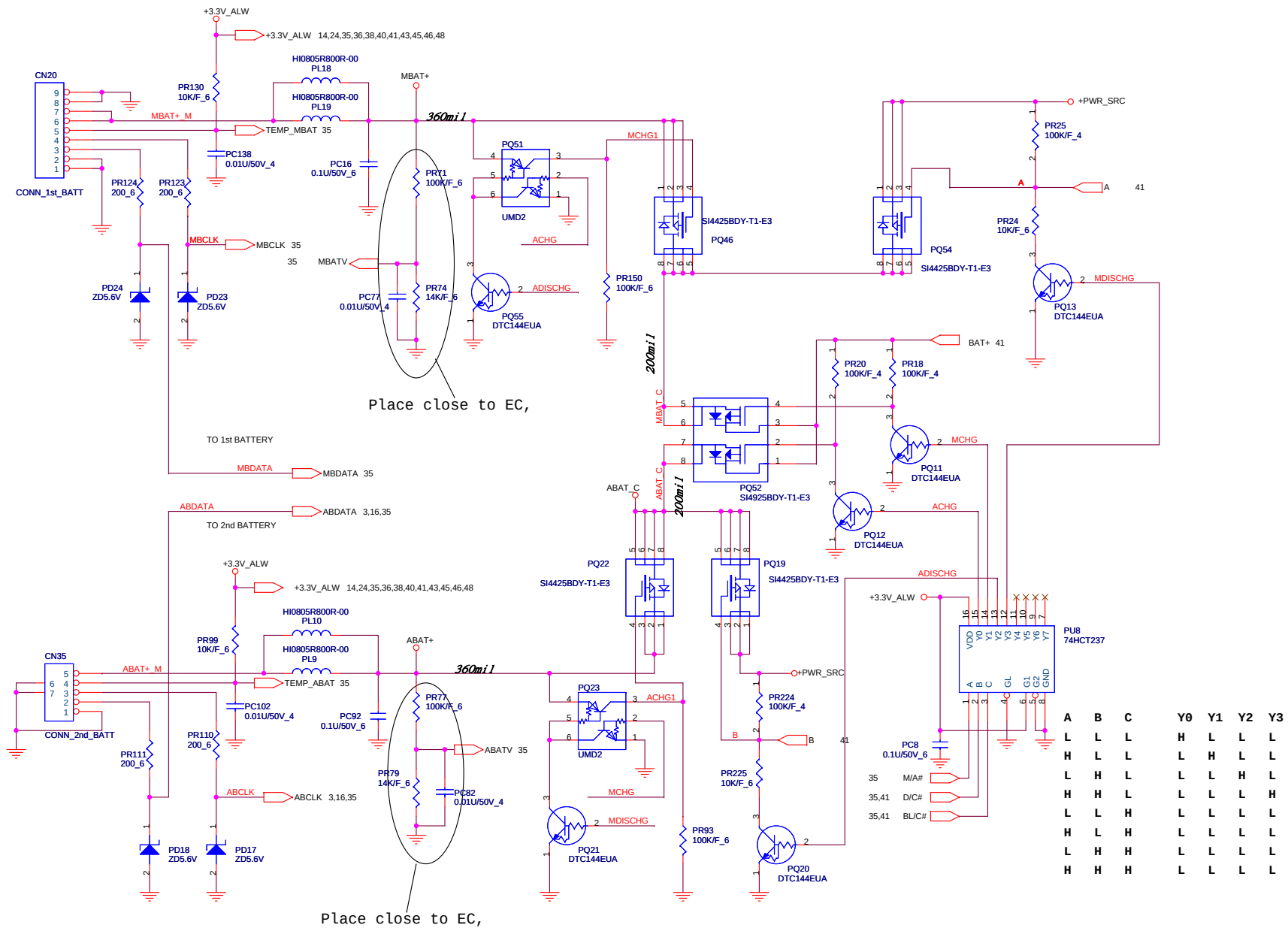


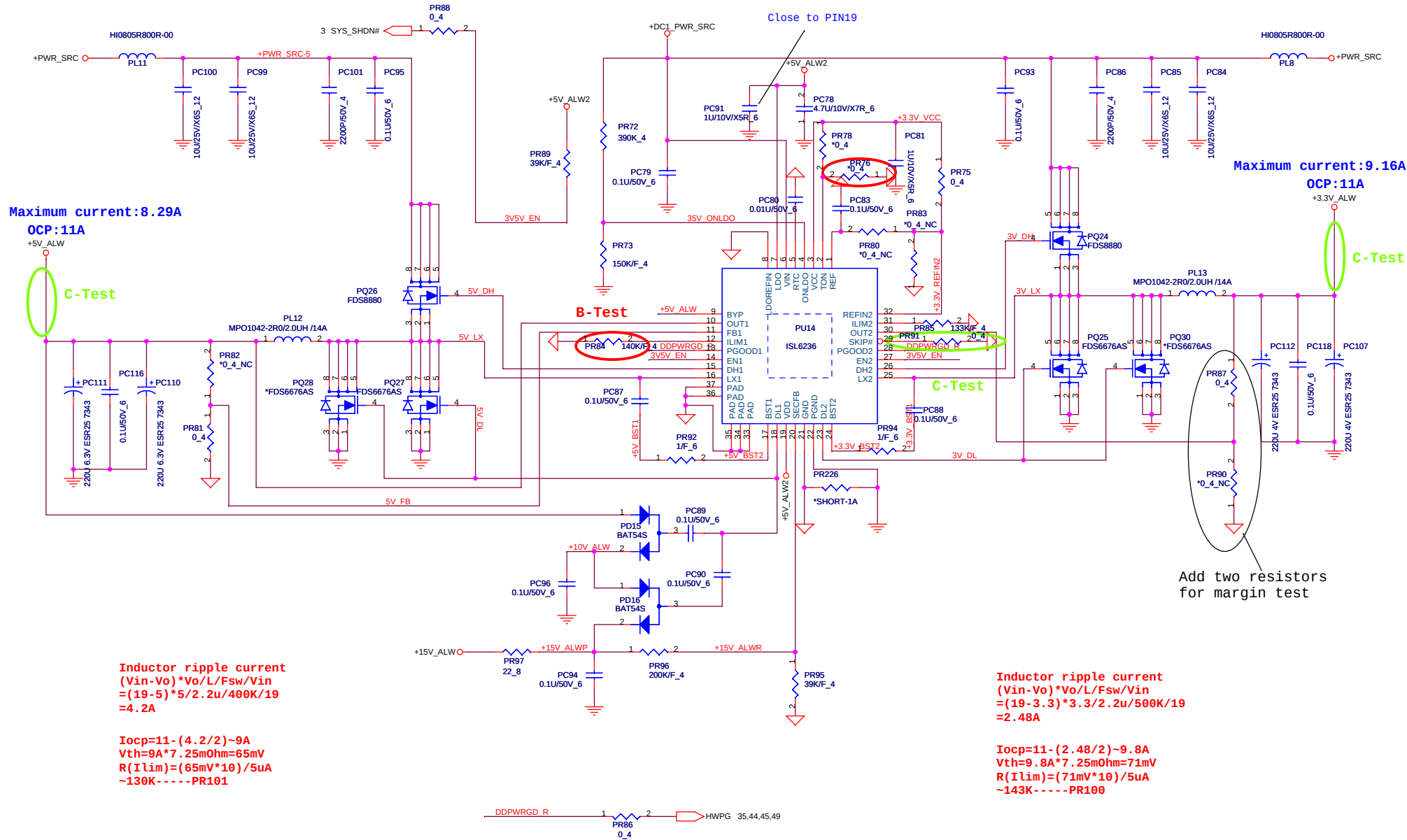


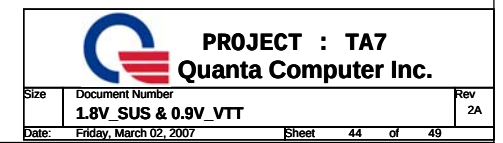
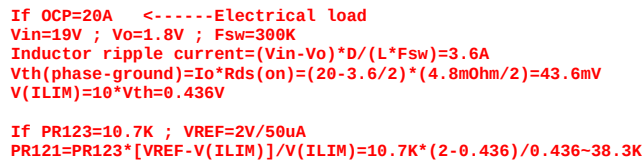
add C912 C913 C914  
from C.S suggestion  
Mika 2007/02/26



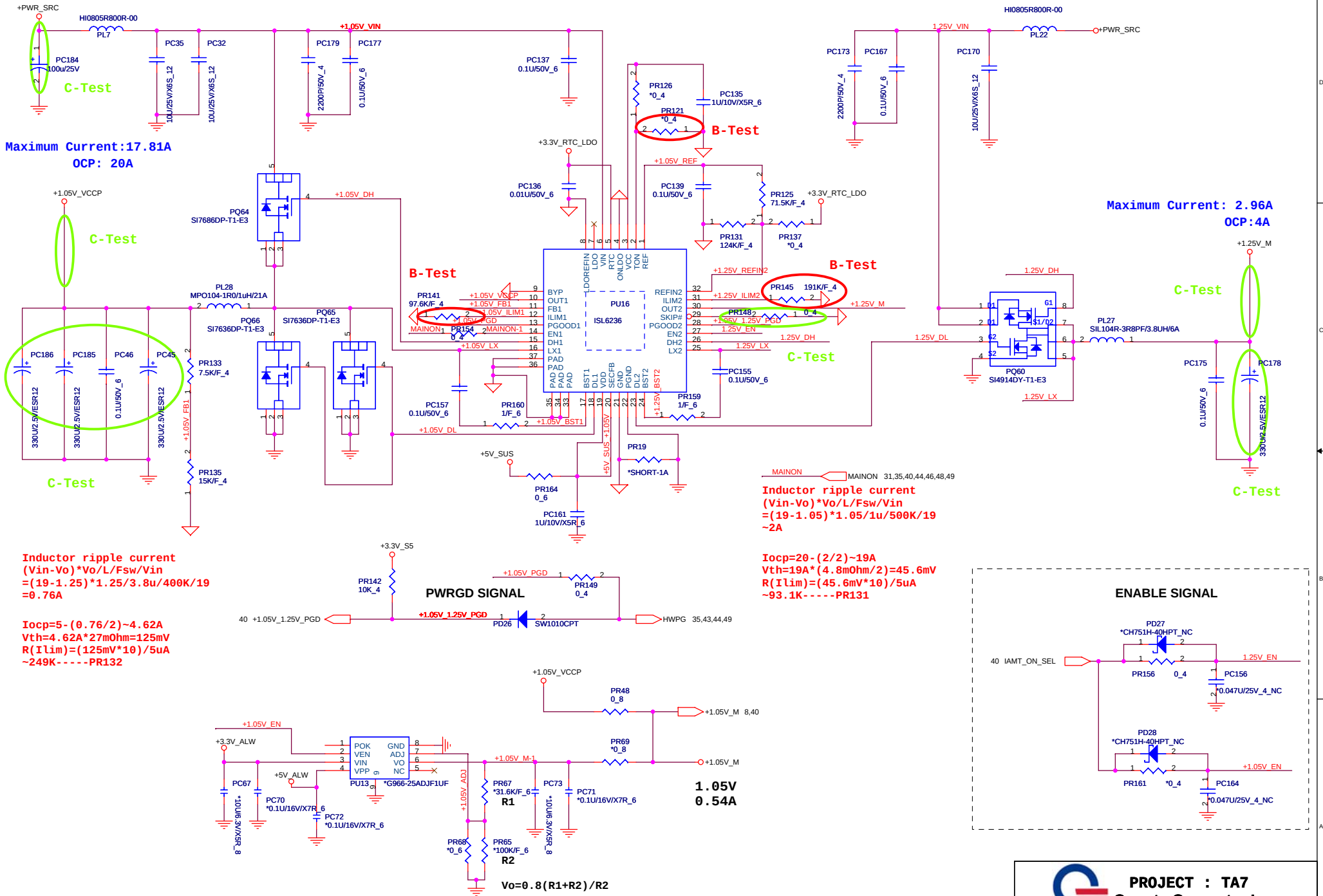


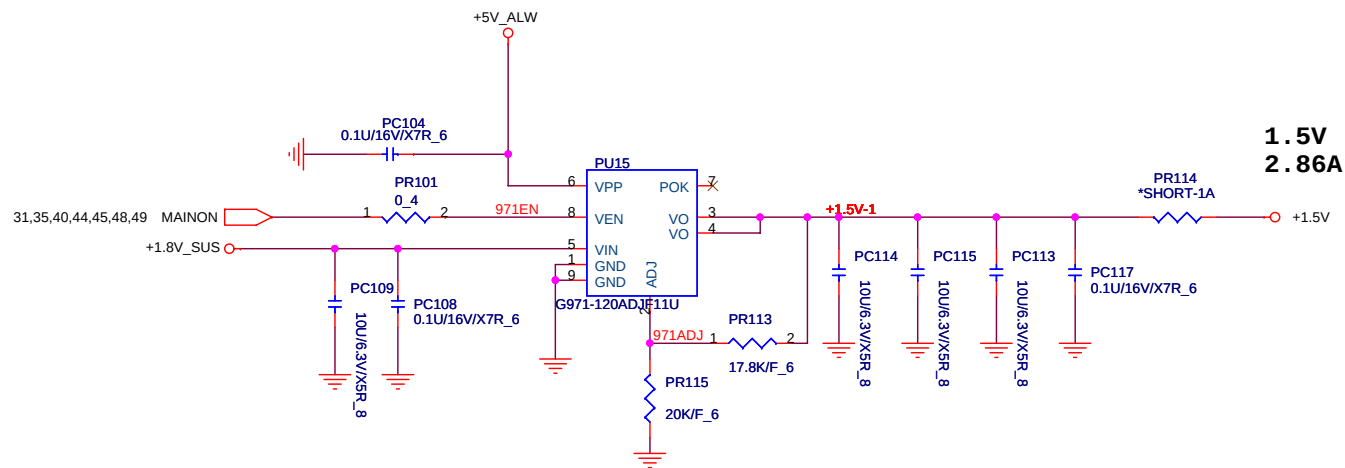




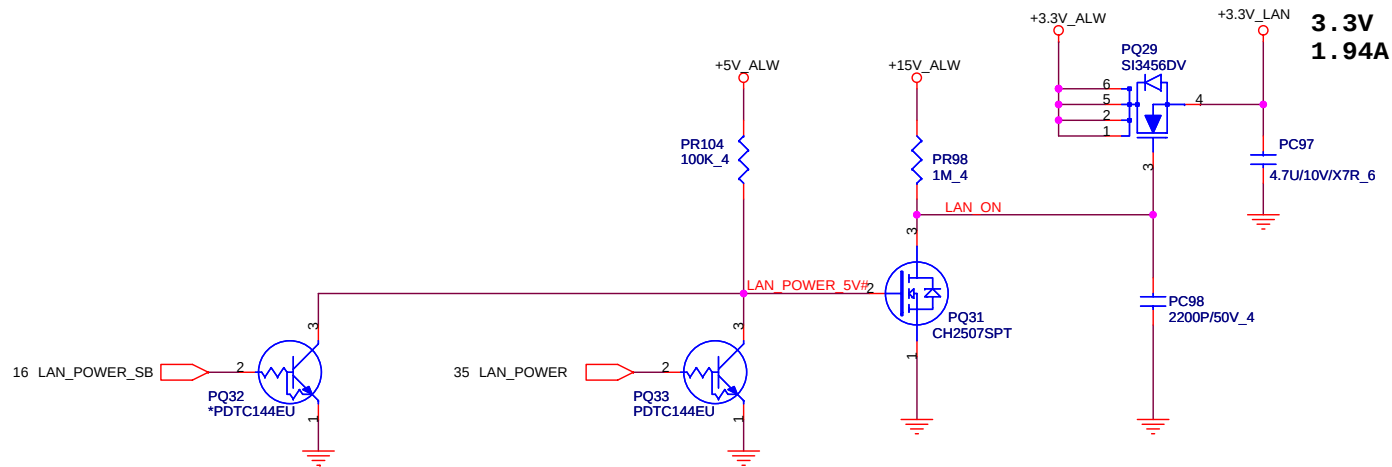








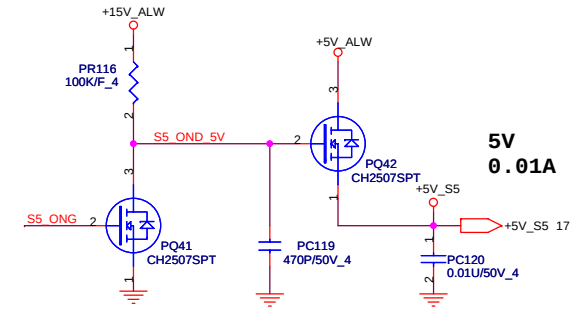
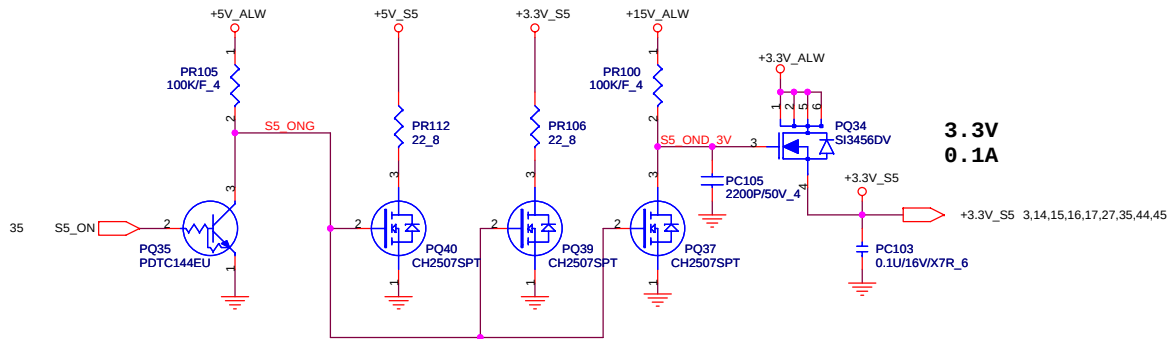
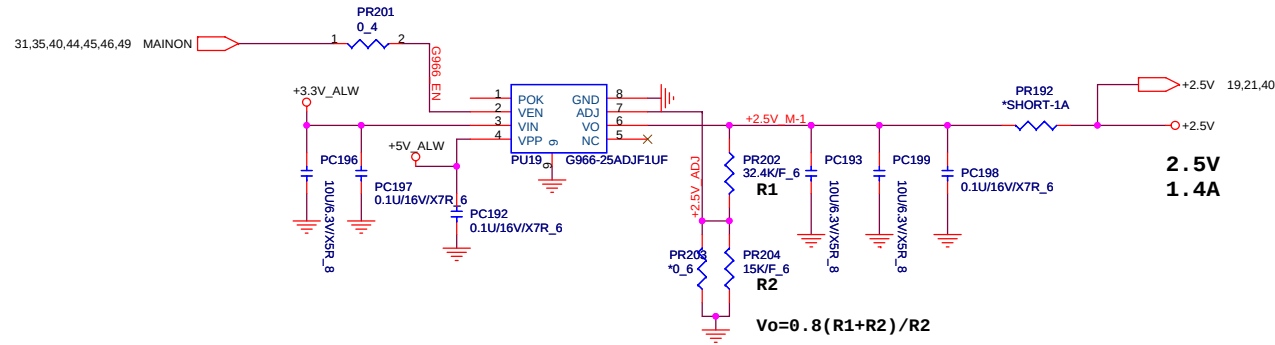
$$V_{out} = 0.8(1 + R1/R2) = 0.8(1 + 17.8K/20K) = 1.512V$$



**PROJECT : TA7**  
**Quanta Computer Inc.**



# For Discrete M71S Model Only



PROJECT : TA7  
Quanta Computer Inc.

| Size  | Document Number        | Rev            |
|-------|------------------------|----------------|
|       | +2.5V/3VS5/5VS5        | 1A             |
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Maximum Current: 15A  
OCP: 20A

