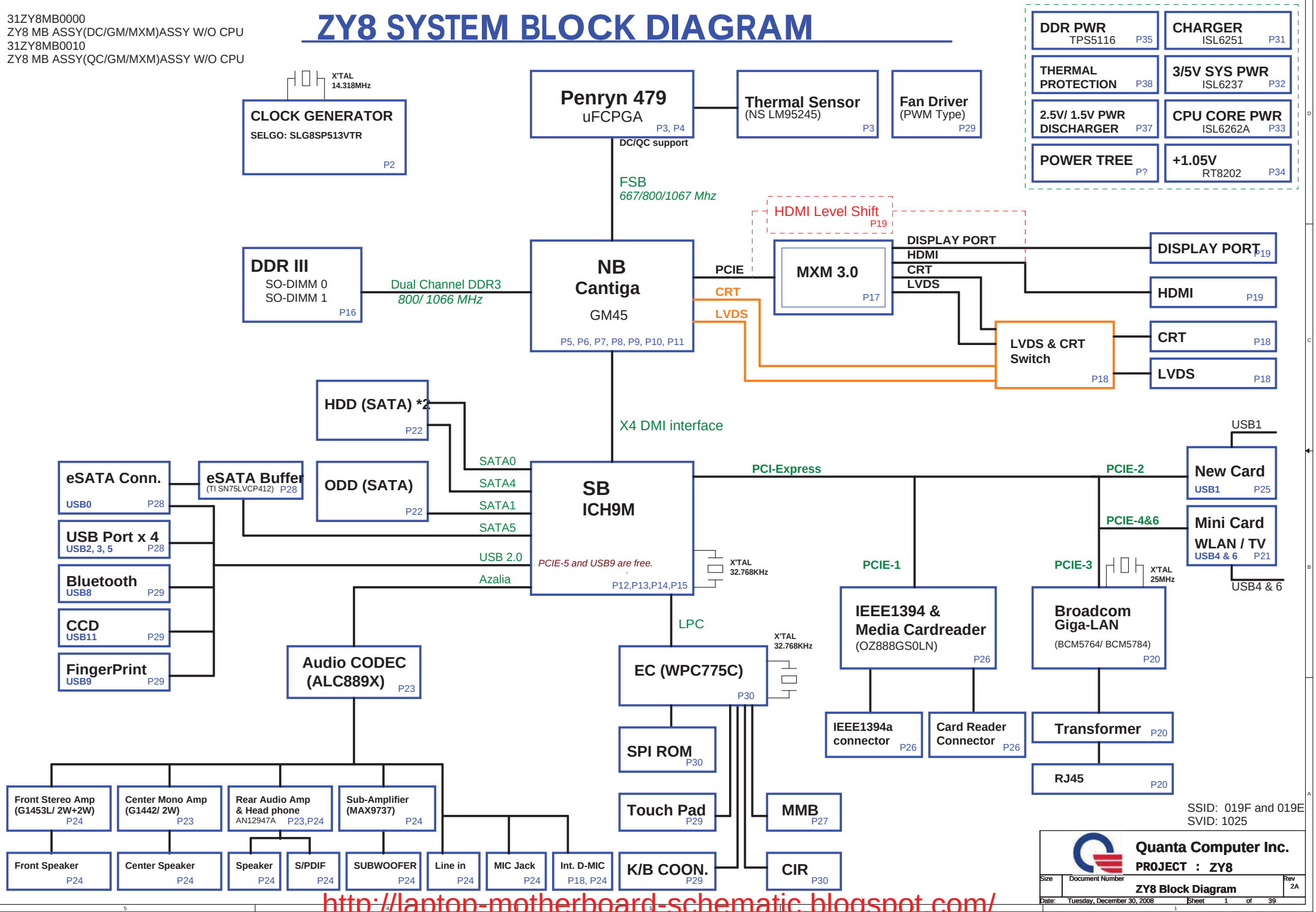
31ZY8MB0000
ZY8 MB ASSY(DC/GM/MXM)ASSY W/O CPU
31ZY8MB0010
ZY8 MB ASSY(QC/GM/MXM)ASSY W/O CPU

ZY8 SYSTEM BLOCK DIAGRAM

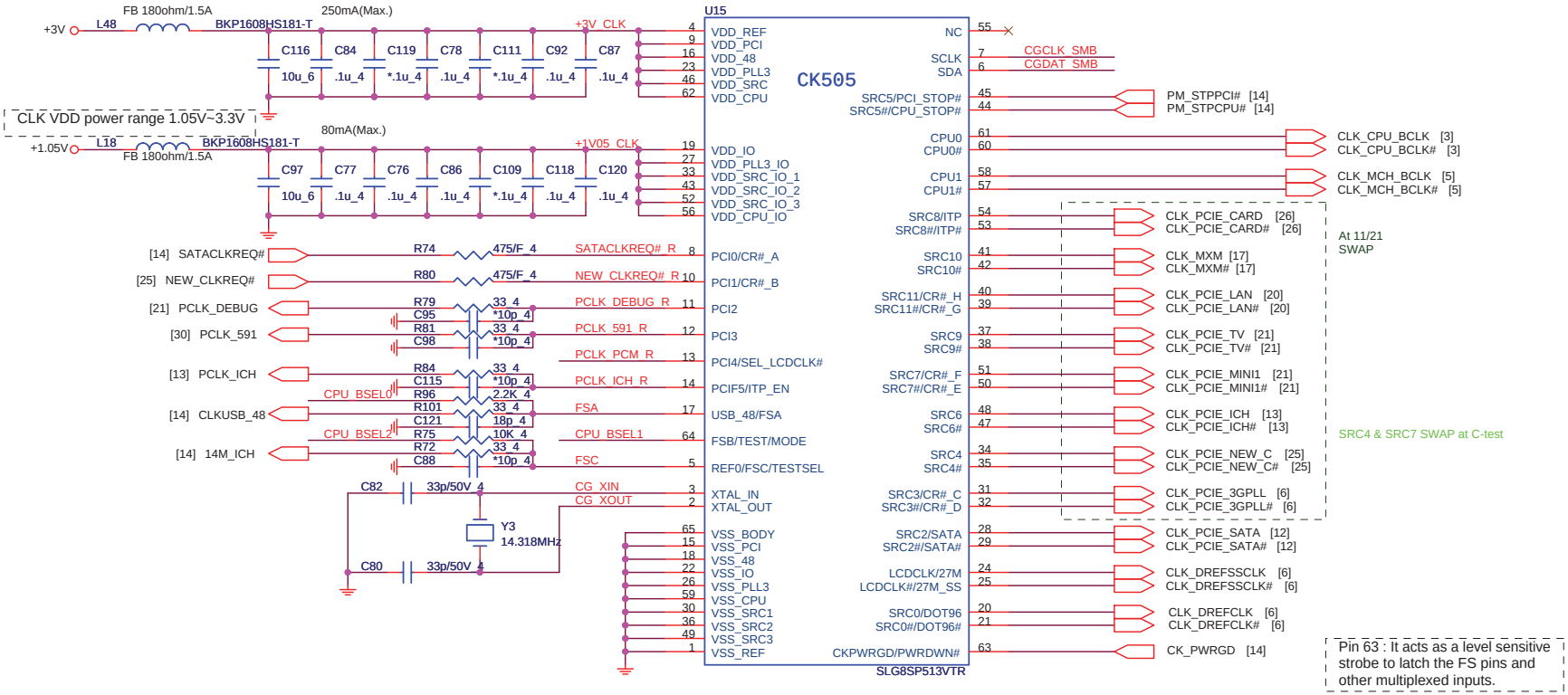


SSID: 019F and 019E
SVID: 1025

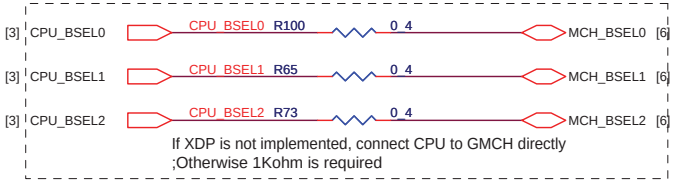
Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	ZY8 Block Diagram	2A
Date: Tuesday, December 30, 2008	Sheet 1 of 39	

Clock Generator



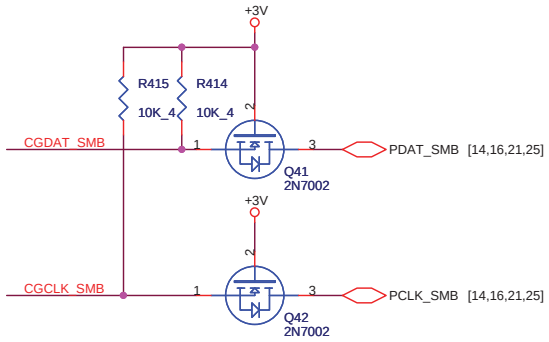
CPU Clock select



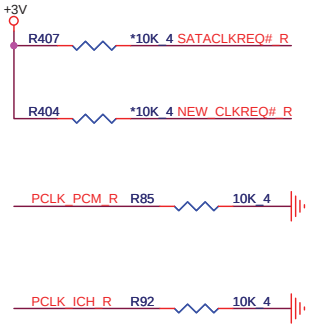
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

SMBus



Strap table



Pin 8 : PCI_0 or CKREQ#_A selection
0 = PCI_0 output
1 = CKREQ#_A (Control SRC_0 & SRC_2)

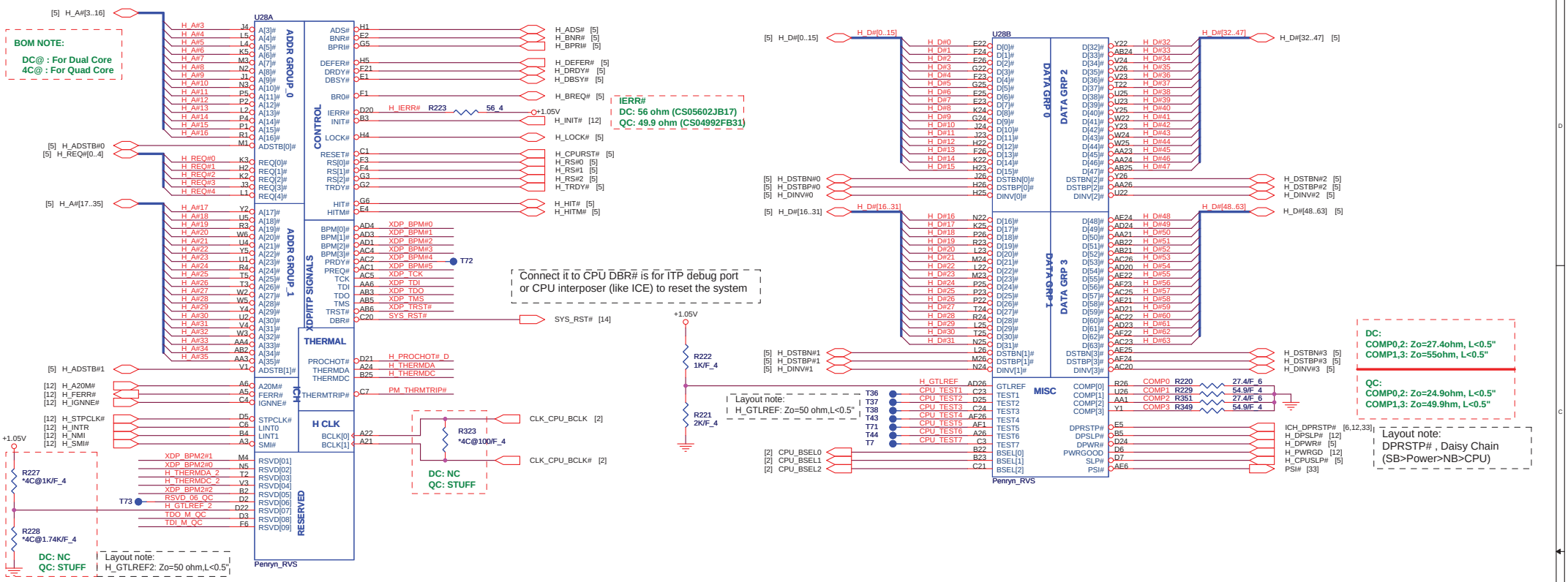
Pin 10 : PCI_1 or CKREQ#_B selection
0 = PCI_1 output
1 = CKREQ#_B (Control LCDCLK & SRC_4)

Pin 13 : For Pin 20/21 and 24/25 selection
0 = LCDCLK & DOT96 for internal graphic (Setting)
1 = 27M & 27M_SS &SRC_0 for external graphic

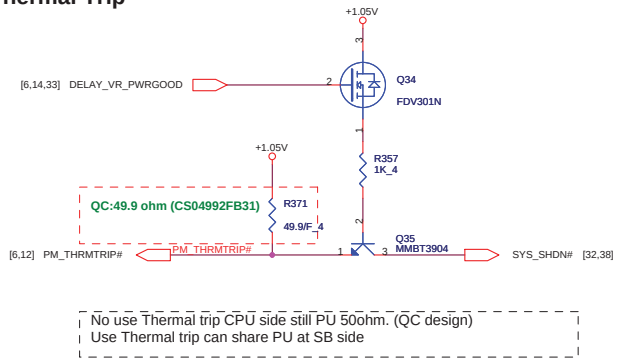
Pin 14 : For Pin 53/54 (CPU_ITP or SRC_8) selection
0 = SRC_8 (Setting)
1 = CPU_ITP

Quanta Computer Inc.
PROJECT : ZY8

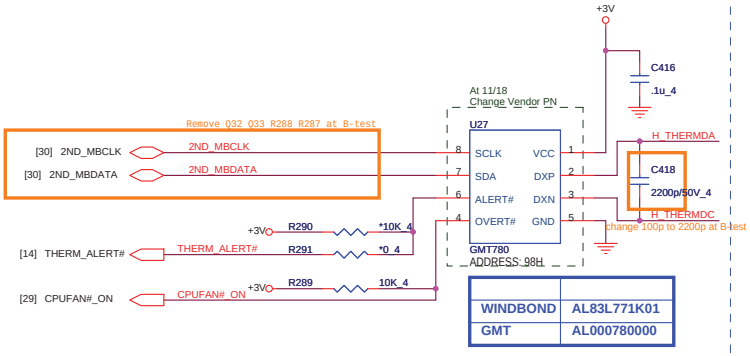
Size	Document Number	Rev
	CLOCK GENERATOR	2A
Date: Tuesday, February 17, 2009	Sheet 2 of 39	



Thermal Trip

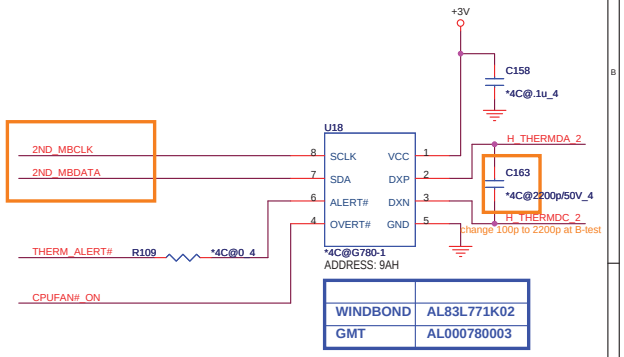


CPU #1 Thermal monitor



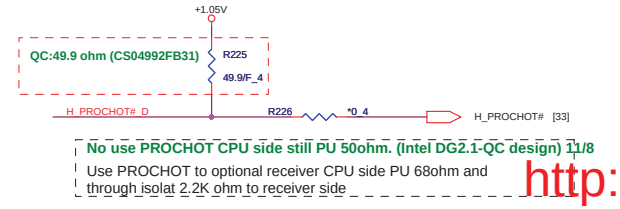
WINDBOND	AL83L771K01
GMT	AL000780000

CPU #2 Thermal monitor

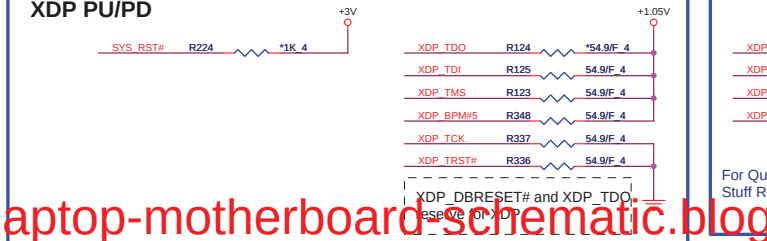


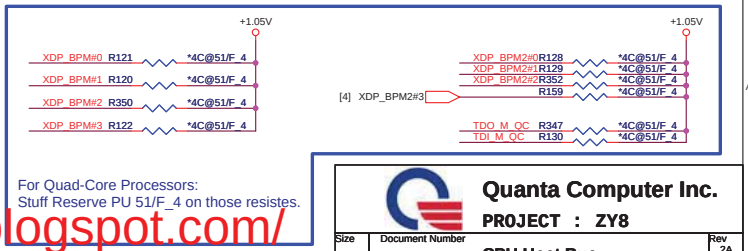
WINDBOND	AL83L771K02
GMT	AL000780003

Processor hot



XDP PU/PD

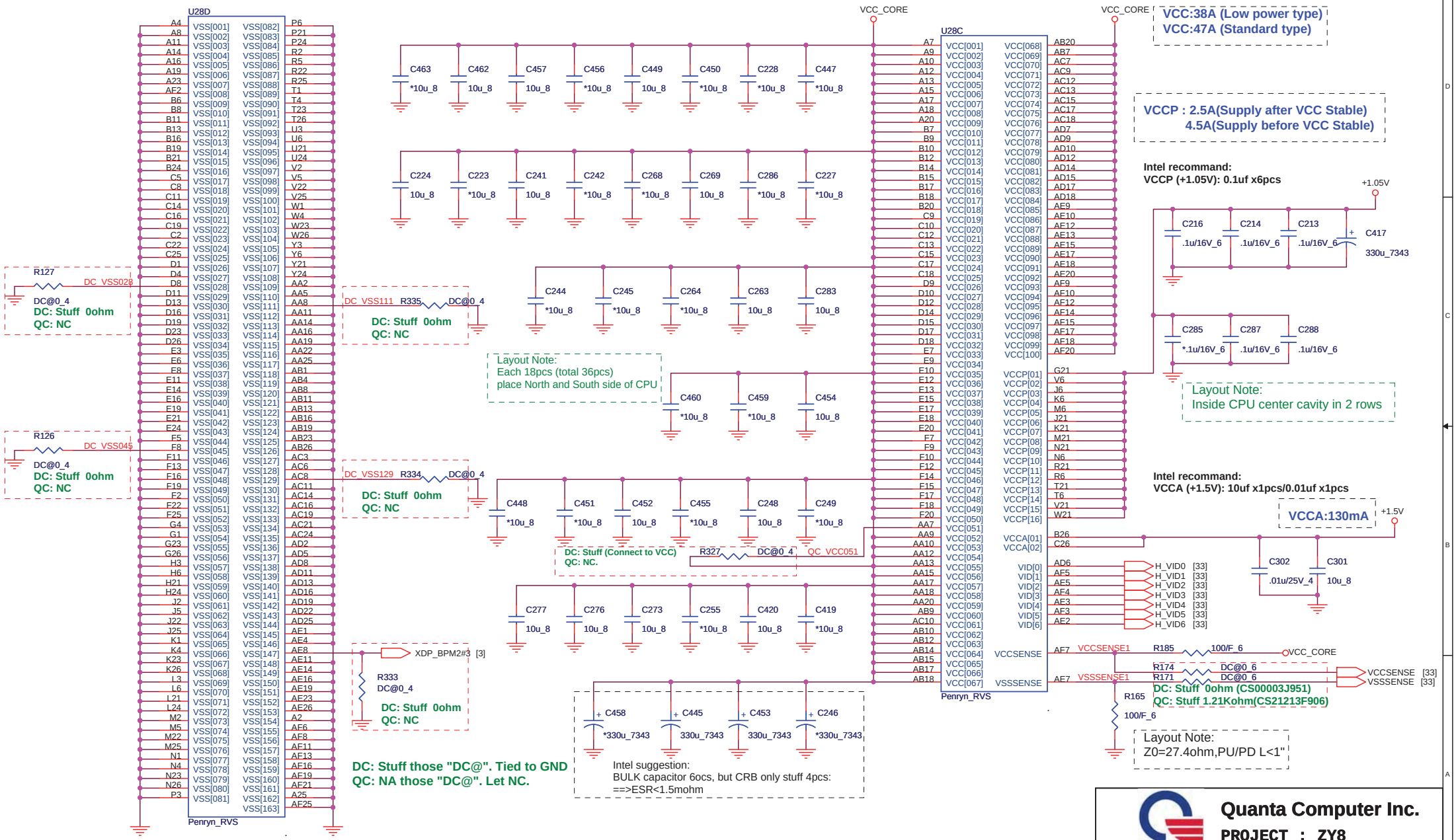




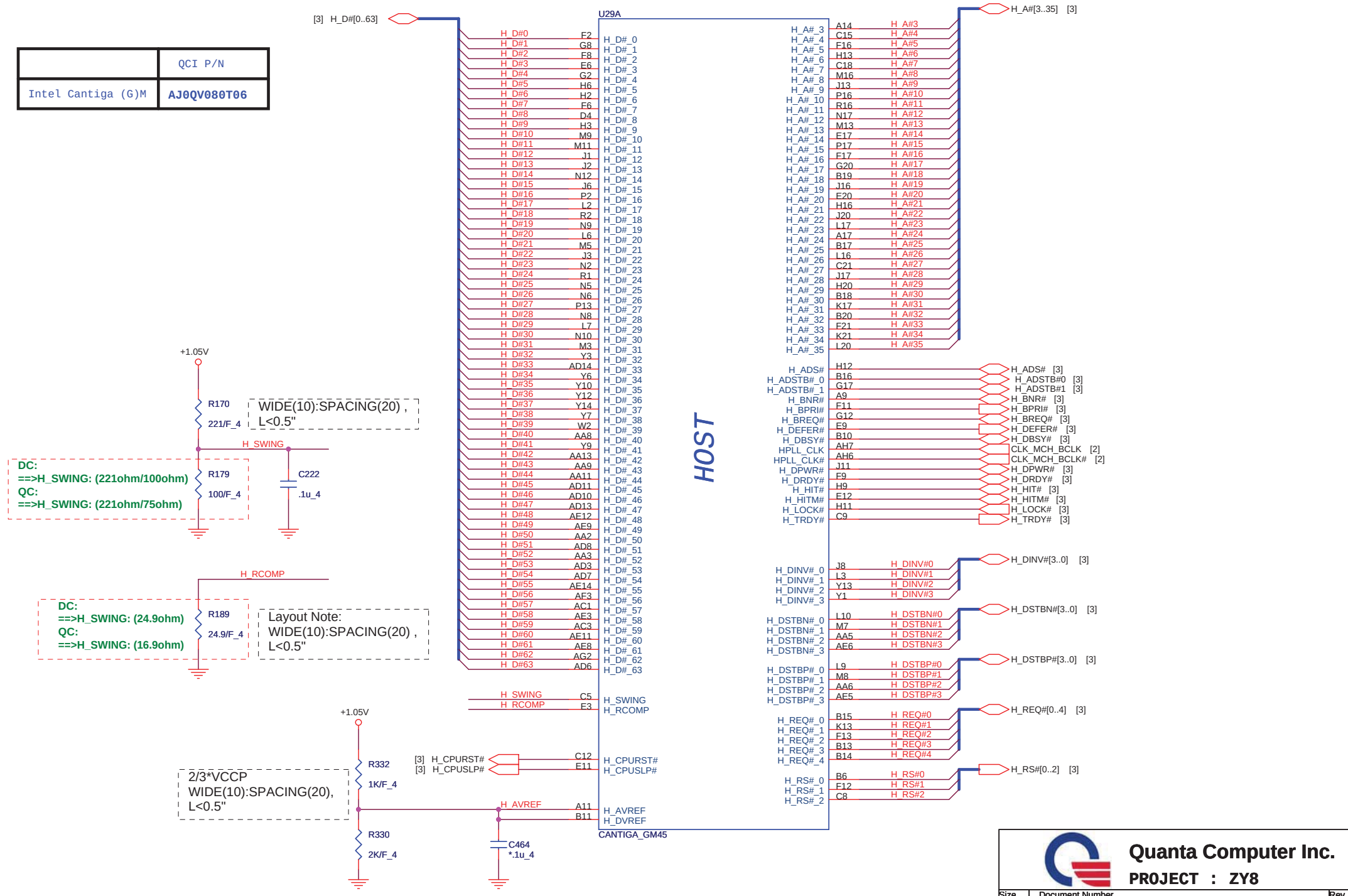
Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	CPU Host Bus	2A

Date: Friday, February 13, 2009 Sheet 3 of 39



	QCI P/N
Intel Cantiga (G)M	AJ0QV080T06



Quanta Computer Inc.

PROJECT : ZY8

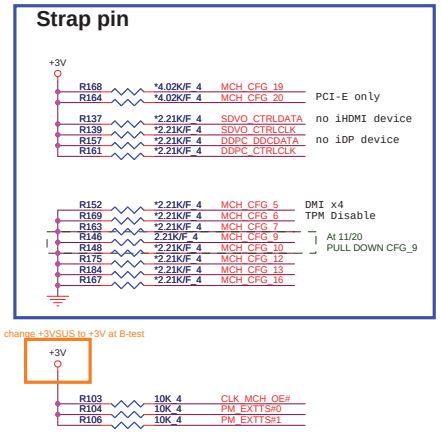
Size	Document Number	Rev
	GMCH HOST	3B

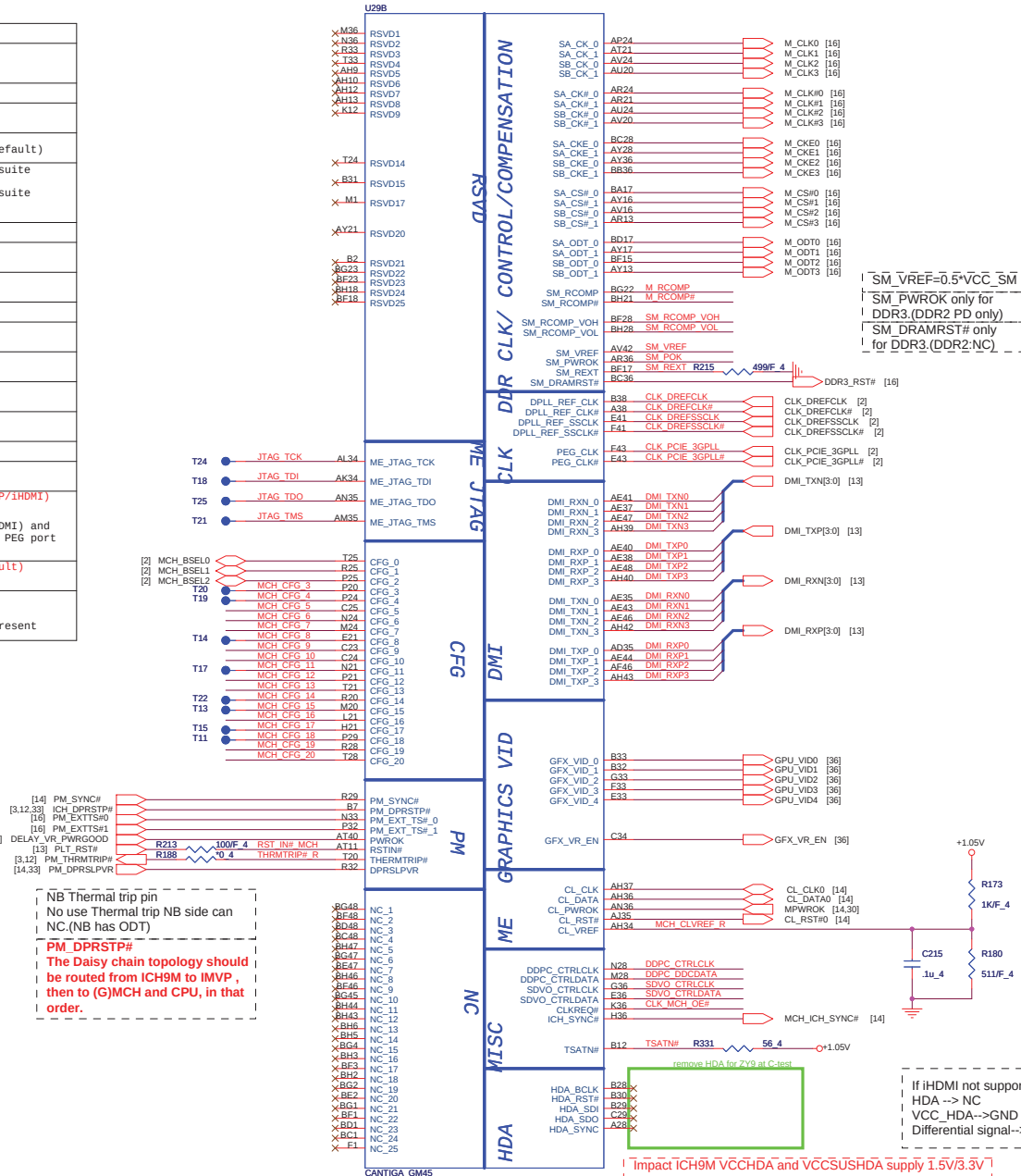
Date: Wednesday, February 11, 2009 Sheet 5 of 39

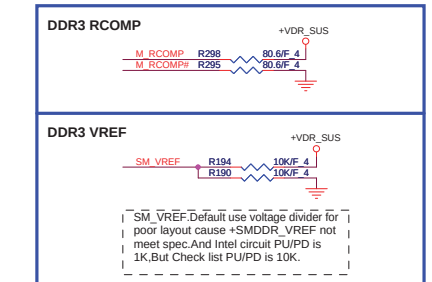
Strap table

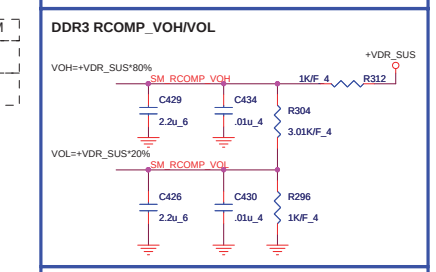
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/iHDMI Device Present(Default) 1 = SDVO/iHDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

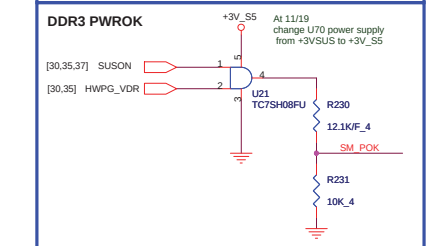
Strap pin

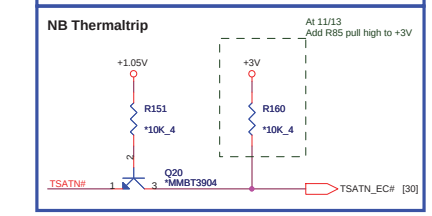












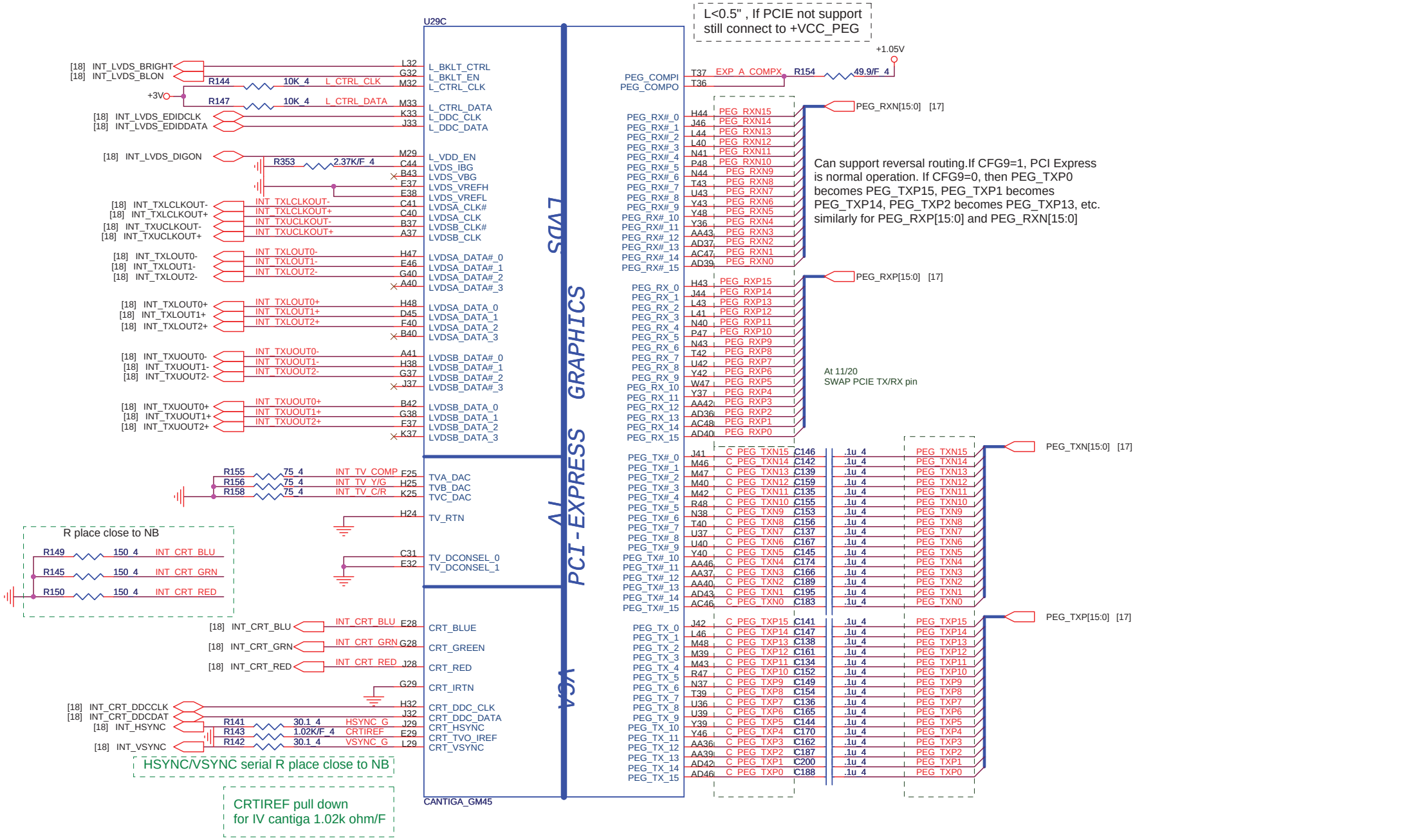
CRB 1.0 : CL_VREF=0.355V (1K/511ohm)
DG 2.1 : CL_VREF=0.35V (1K/500ohm)

DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

If iHDMI not support
HDA --> NC
VCC_HDA-->GND
Differential signal-->NC

<Checklist ver0.8/DG2.1>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number | Rev 3B
GMCH DMI
Date: Wednesday, February 11, 2009 | Sheet 6 of 39

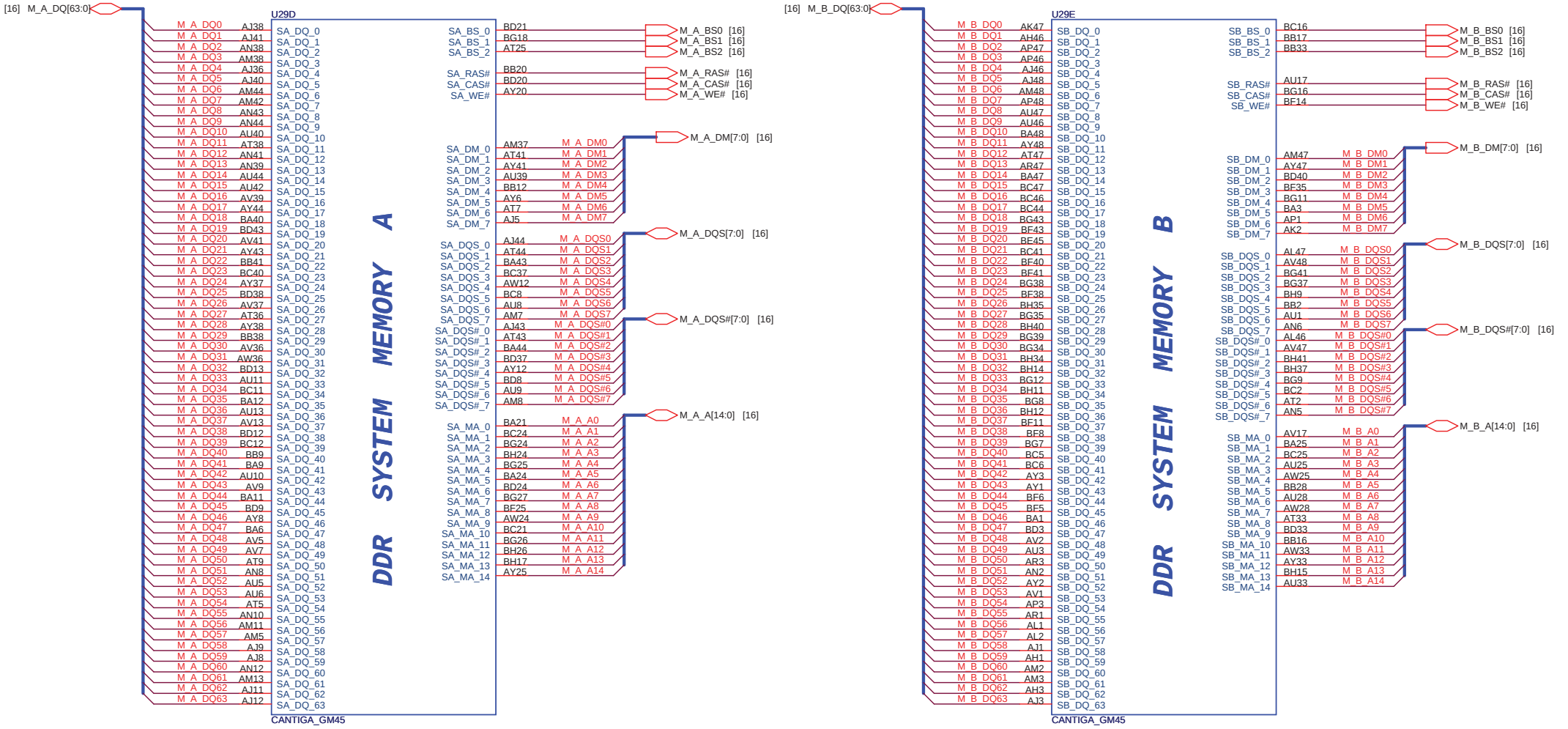


Quanta Computer Inc.

PROJECT : ZY8

Size	Document Number	Rev
	GMCH VGA/PEG	3B

Date: Wednesday, February 11, 2009 Sheet 7 of 39



GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZY8

Size	Document Number	Rev
	GMCH DDR I/F	3B

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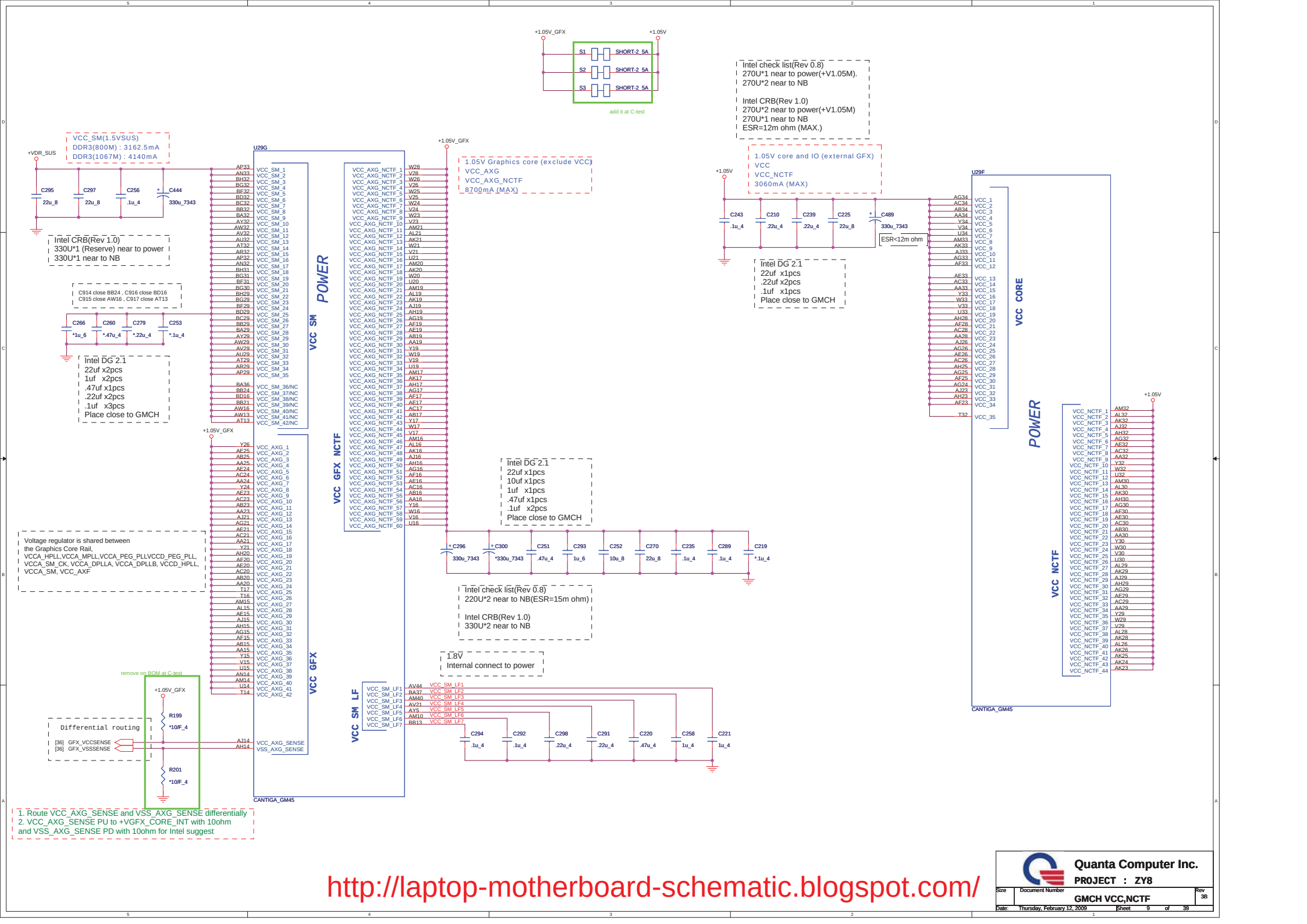


Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	GMCH VCC,NCTF	3B

Date: Thursday, February 12, 2009 Sheet 9 of 39

Power consumption reference to Intel
Cantiga chipset EDS Volume1. Section 10

CRT DAC (3.3V)
73mA

TV DAC (3.3V)
5mA

VTT (1.05V)
FSB (1067MHZ):852mA

Intel DG2.1
10uH, 10%(1210)
0.45A DCR_max = 0.39ohm

Display PLL_A/B (1.05V)
64.8mA

VCCA_DPLLA/B always keep to +1.05V
(If no use IV dynamic core power)

USE same GND plane

Intel DG 2.1
4.7uf x2pcs
2.2uf x1pcs
.47uf x1pcs
Place close to GMCH

Intel DG 2.1
10uf x1pcs
.1uf x1pcs
Place close to GMCH

Host PLL(1.05V)
24mA

LVDS analog (1.8V)
13.2mA

Band Gap (1.5V)
414uA

VCC_AXF(1.05V)
321.35mA

Check list 2.2
don't need

IO logic and DLL(1.05V)
DDR3(1066):747.5mA

Analog PLL(1.05V)
50mA

Clock supply(1.5V)
DDR3(1066):149.5mA

0805 1uH , Rdc = 0.14 - 0.26.
Max rated current = 220 mA

MEM PLL(1.05V)
139.2mA

Clock logic(1.05V)
DDR3(1066):37.95mA

LVDS Transmitter(1.8V)
118.8mA

Check list 2.2
DDR3=>0 ohm
DDR2=>0.1uH, DCR<160 mohm

CRB : 0 ohm
DG2.1 : 2.2nH

TV analog(3.3V)
79mA

3.3V
105.3mA

GMCH iHDA no use
==>pull-down 0ohm

Intel HDA(1.5V)
50mA

PCI-E(1.05V)
1782mA

VCCD_QDAC share to TV and CRT
and Thermal sensor

DMI termination(1.05V)
456mA

TV(1.5V)
35mA

HPLL(1.05V)
157.2mA

CRT Quiet and Thermal sensor(1.5V)
2.2mA

CRB no 10U
Check list need min 10U~100U
for VCCA_QDAC

Digital PLL(1.05V)
50mA

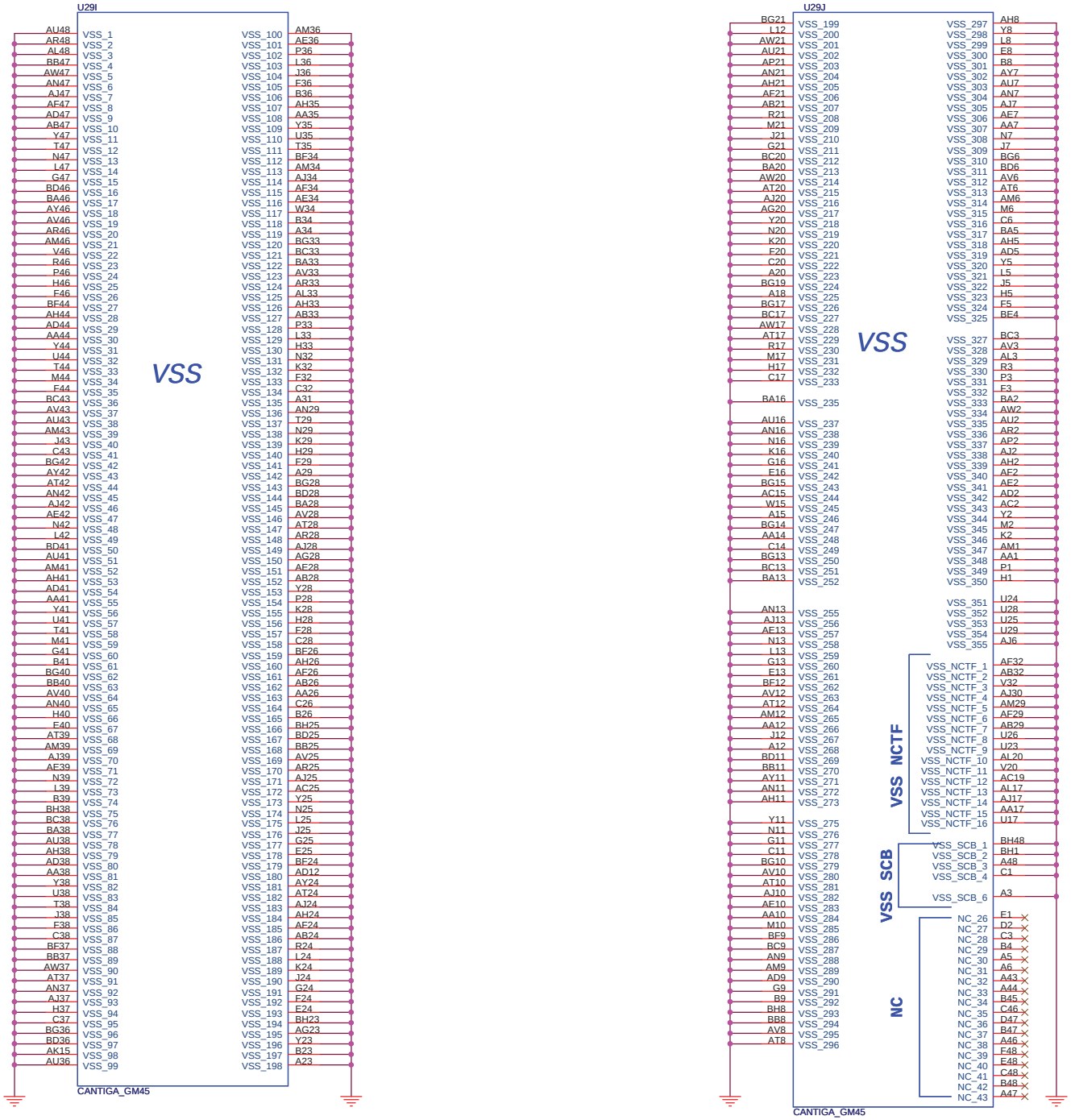
LVDS digital(1.8V)
60.31mA

1.05V
Internal connect to power

CANTIGA_GM45

POWER

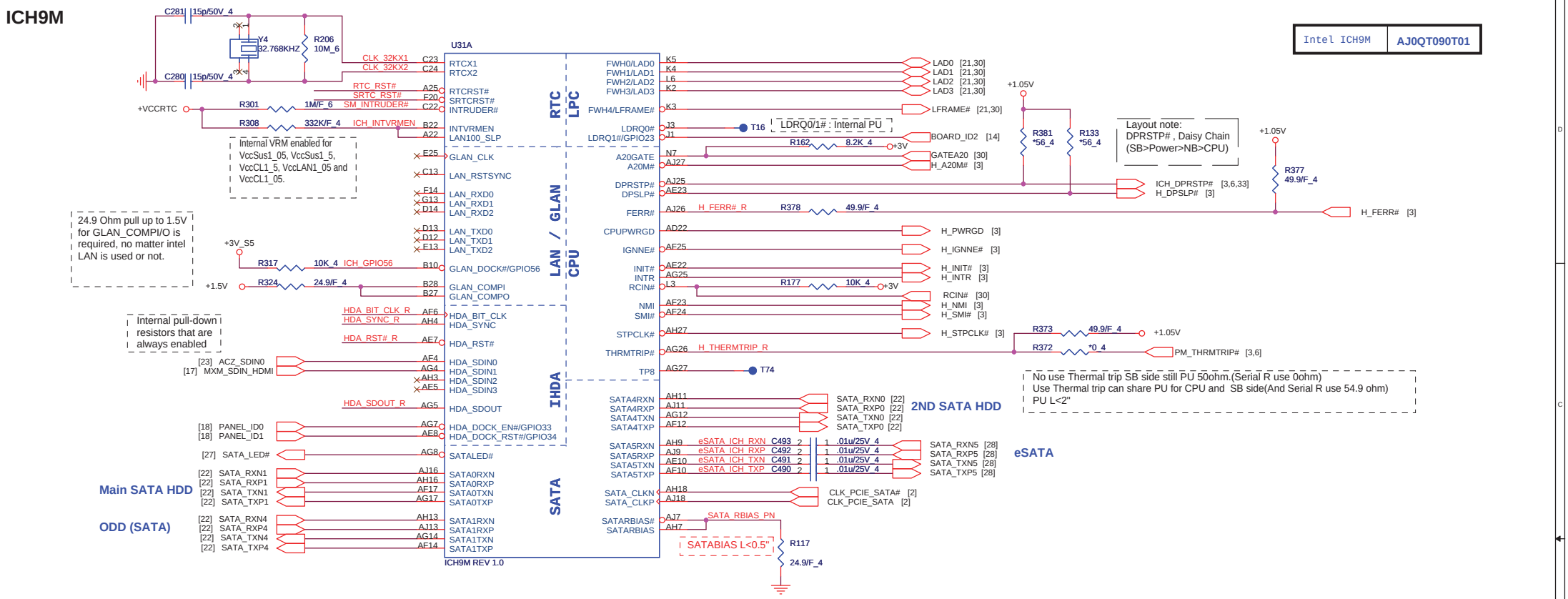
Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number | Rev
GMCH POWER | 3B
Date: Monday, February 16, 2009 | Sheet 10 of 39



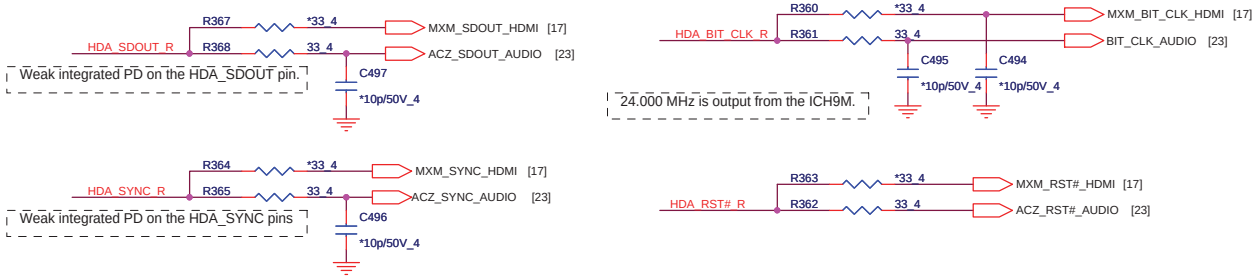
Quanta Computer Inc.

PROJECT : ZY8

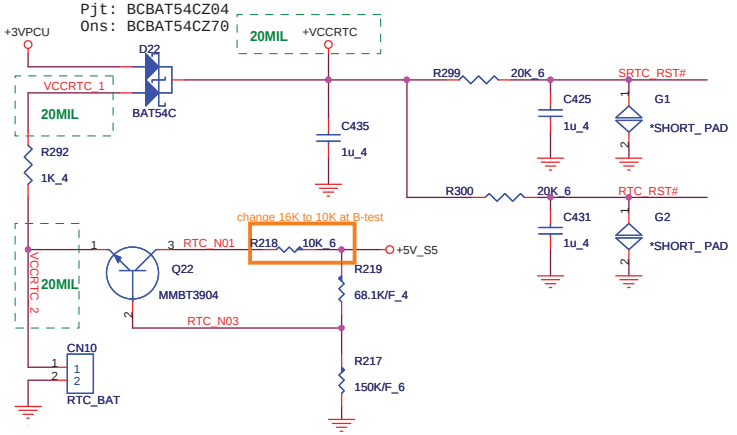
Size	Document Number	Rev
	GMCH VSS	3B
Date: Wednesday, February 11, 2009	Sheet 11 of 39	



HD Audio



RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT / Description 0 / 0 / RSVD 0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Reserve pin config bit 1	[14] ICH_TP3 — ICH_TP3 — R316 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R366 *1K_4 — +1.5V

Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number: ICH9M HOST | Rev 3B
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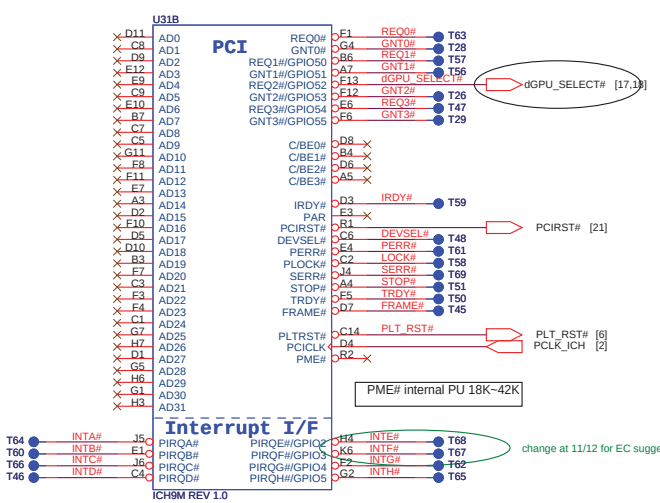
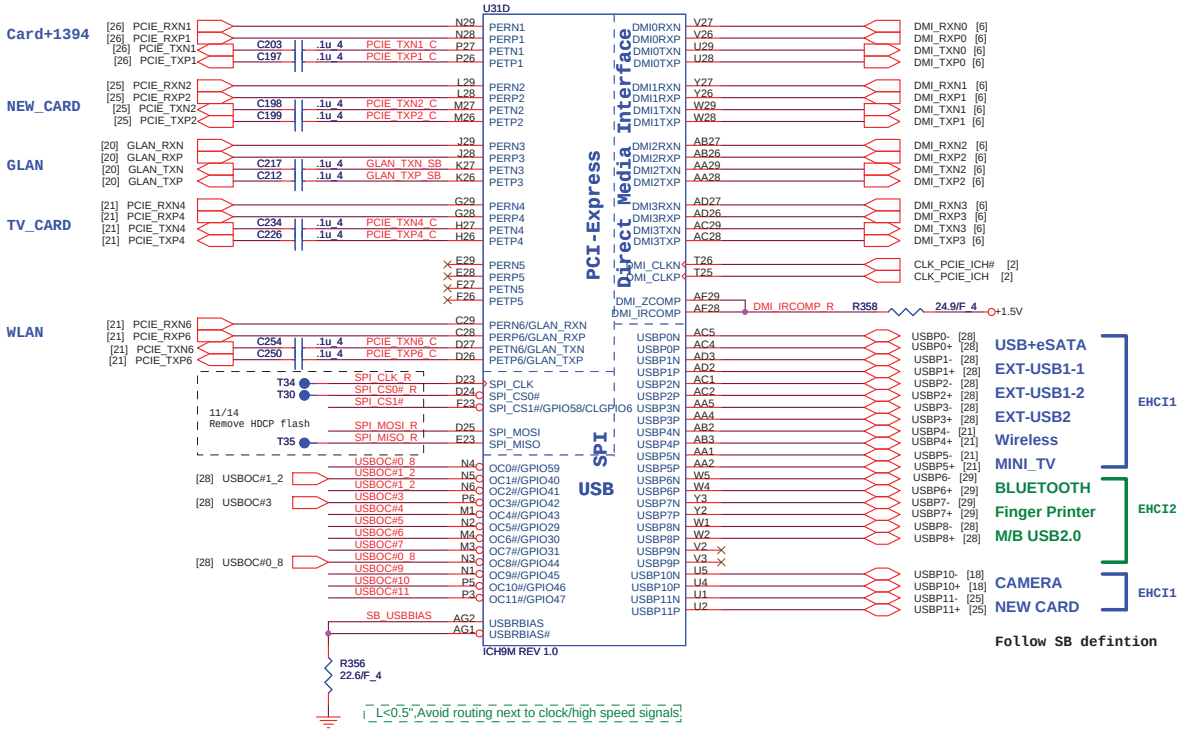
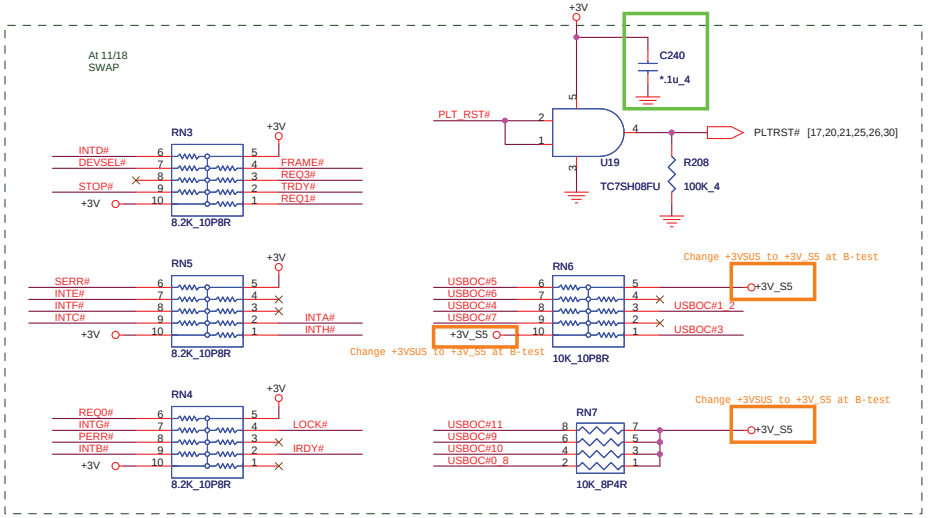
ICH9M



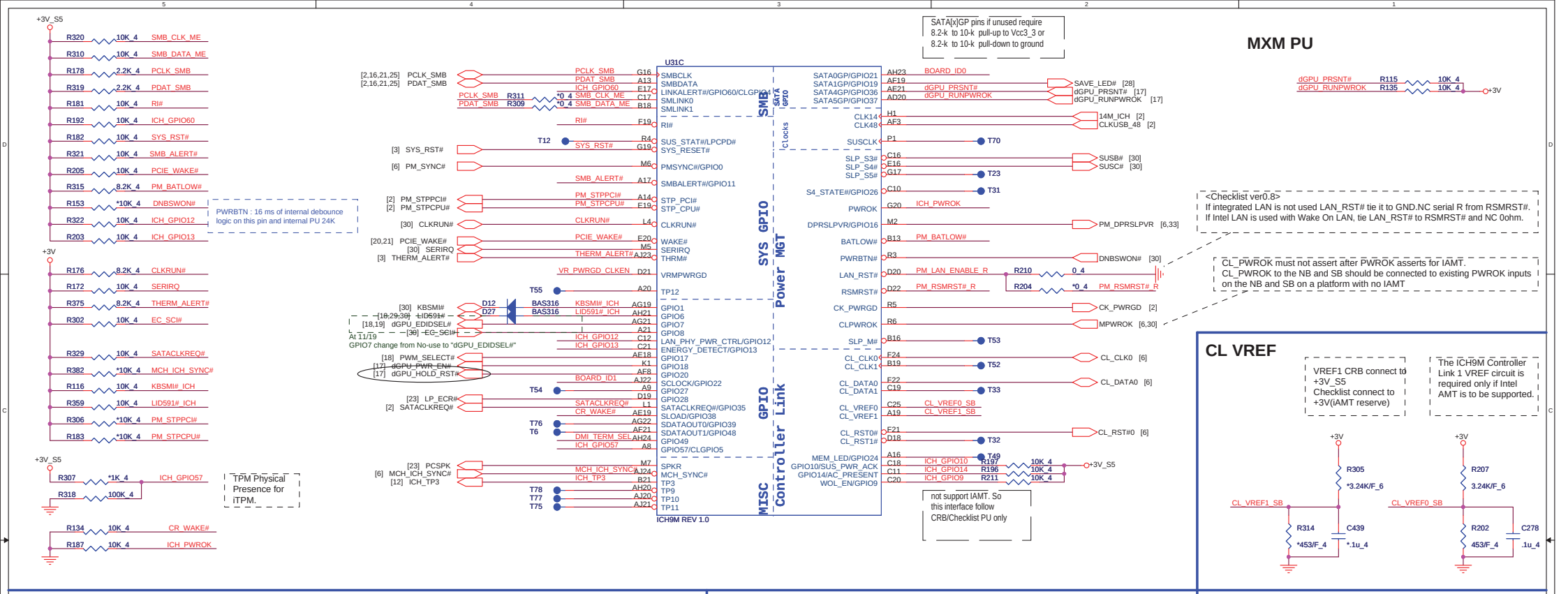




South Bridge Strap Pin (2/3)

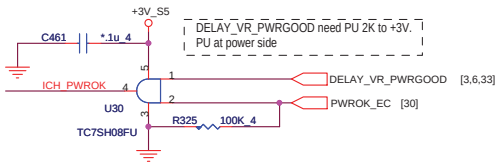
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R193 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_R R200 *20K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / **LPC(Default)**	GNT0# R186 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R191 *1K_4

Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number: ICH9M PCIE / PCI / USB | Rev 3B
Date: Friday, February 13, 2009 | Sheet 13 of 39

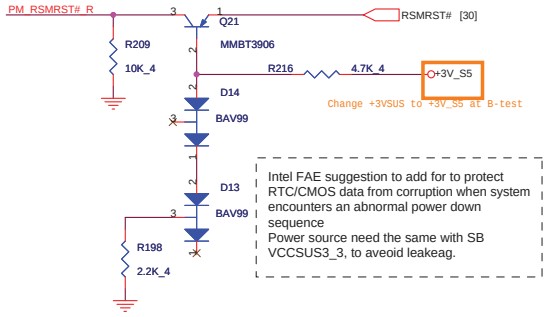


CL VREF

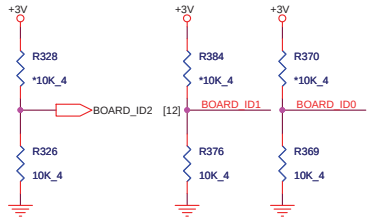
ICH PWROK



Resume RST



M/B ID

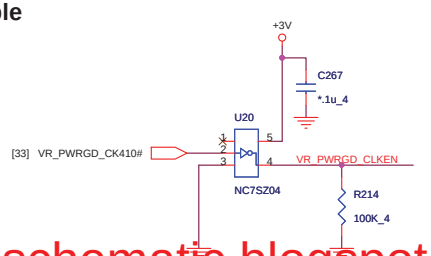


Board ID	ID2	ID1	ID0
default	0	0	0
	0	0	1
	0	1	0
	0	1	1
	1	0	0

South Bridge Strap Pin (3/3)

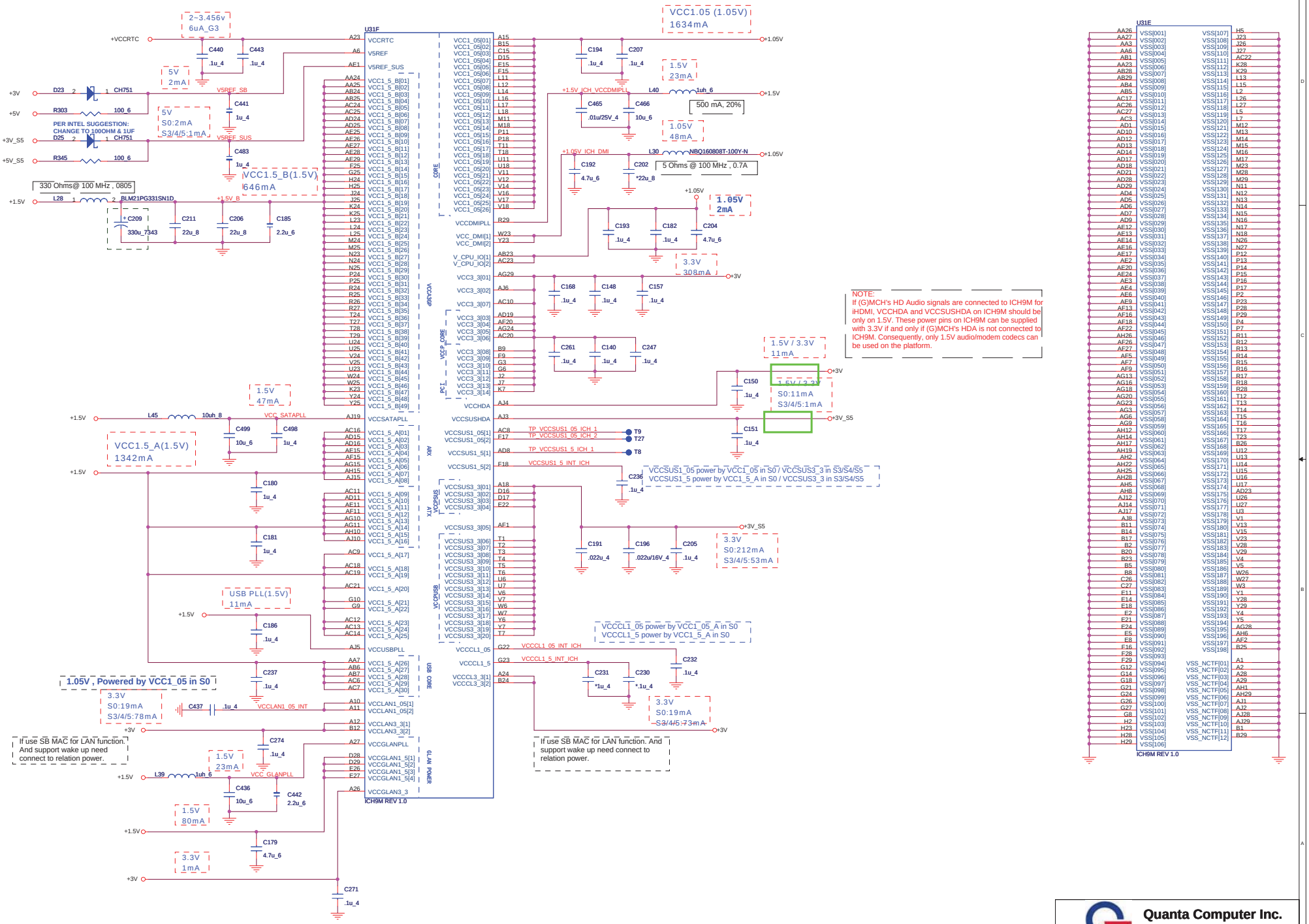
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R166 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R383 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number | ICH9M GPIO | Rev 3B
Date: Monday, January 05, 2009 | Sheet 14 of 39

ICH9M



Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	ICH9 POWER	3B

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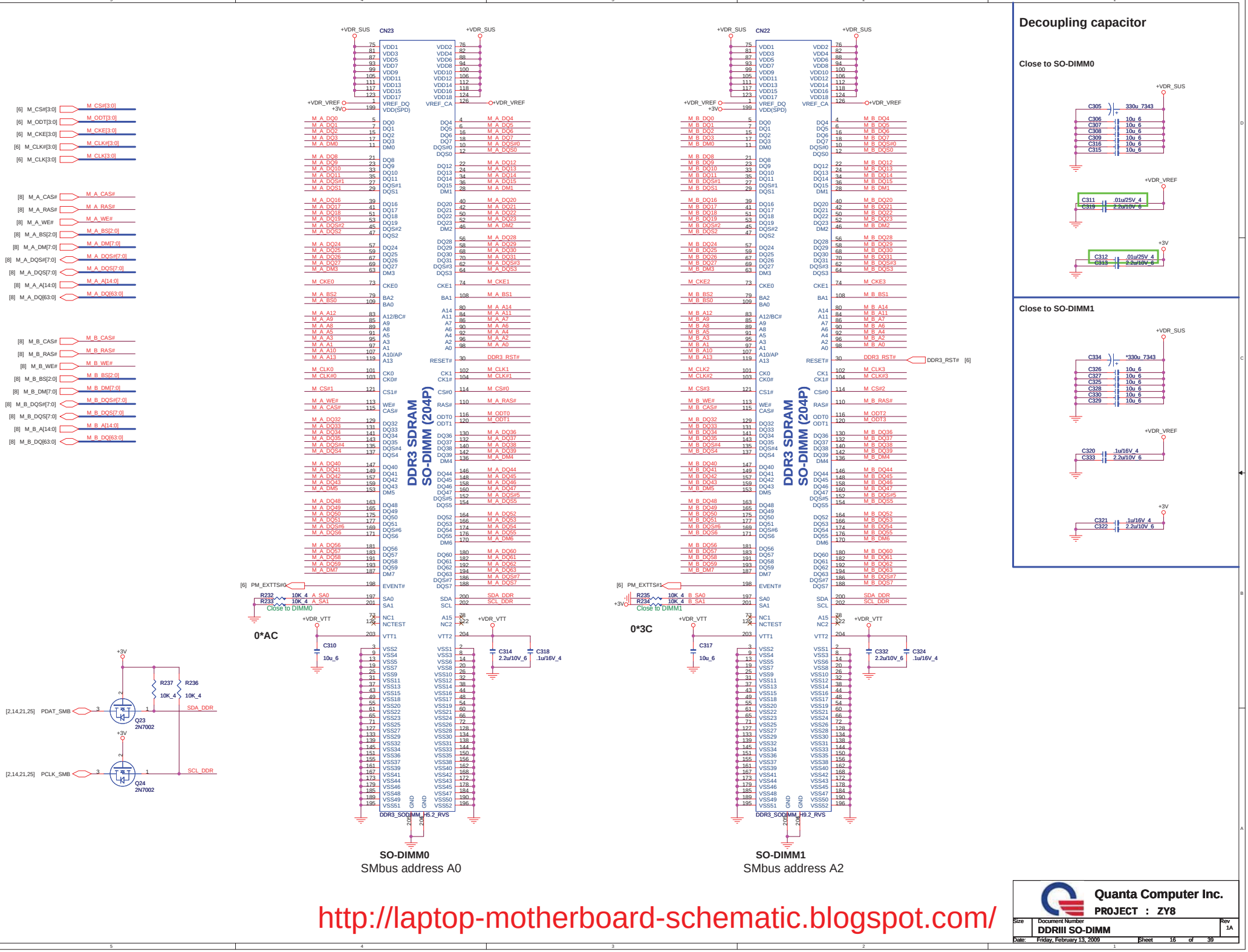

Decoupling capacitor
Close to SO-DIMM0
Close to SO-DIMM1
DDR3 SDRAM SO-DIMM (204P)
DDR3_SODIMM_H5.2_RVS
DDR3_SODIMM_H9.2_RVS
SO-DIMM0
SMbus address A0
SO-DIMM1
SMbus address A2
0*AC
0*3C
Close to DIMM0
Close to DIMM1
Quanta Computer Inc.
PROJECT : ZY8
DDRIII SO-DIMM
Friday, February 13, 2009
http://laptop-motherboard-schematic.blogspot.com/

MXM Module

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM

At 11/21
update MXM footprint to mxm-mm70-314-310b1-1-270p

CN25A

MXM3_2.0 CONNECTOR

CN25B

MXM3_2.0 CONNECTOR

MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	Int. DP	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

MXM Reset

Thermo SMBus

MXM VIN Power switch

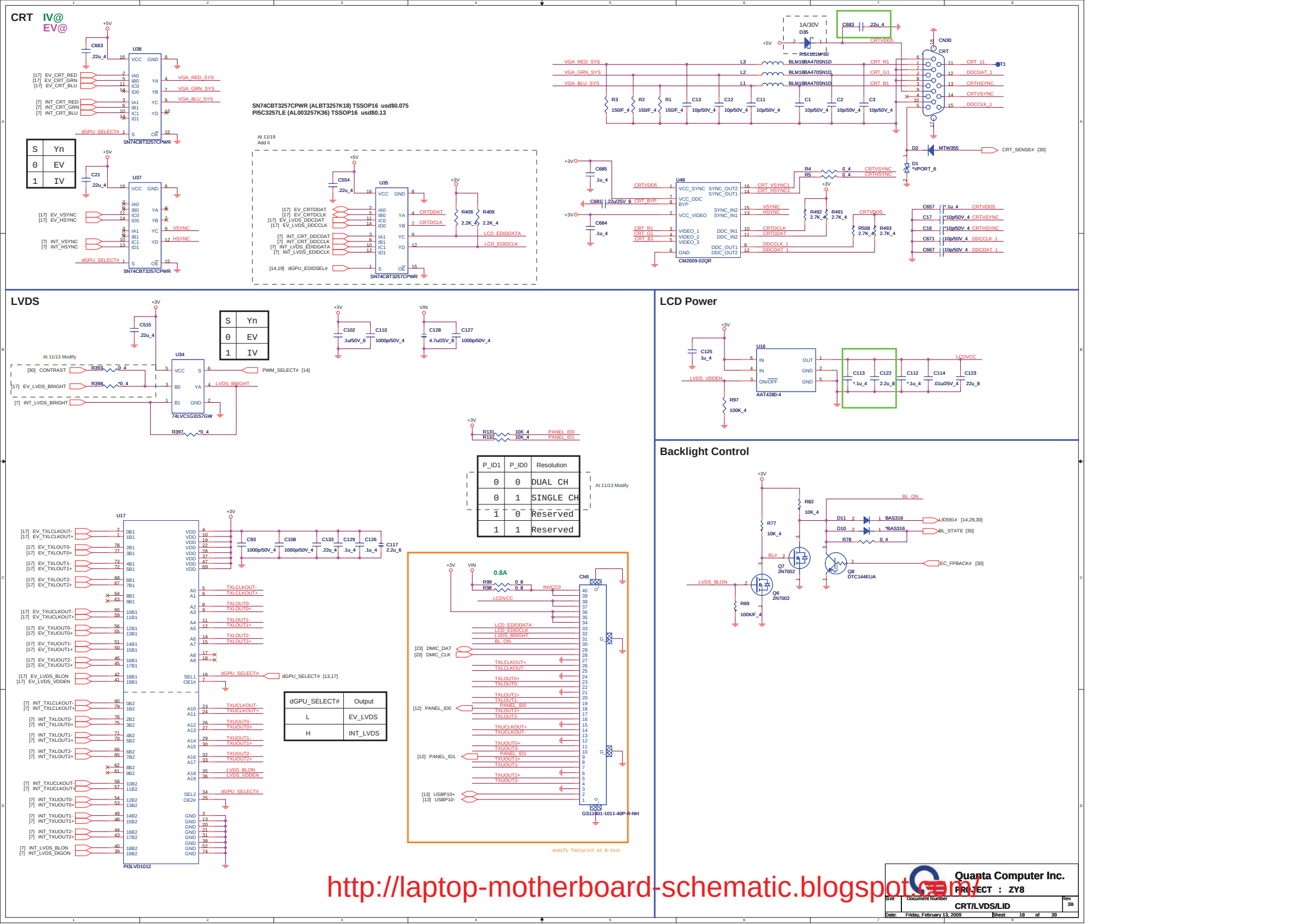
dGPU_PWR_EN#	Behavior
Low	Enable dGPU PWR
High	Disable dGPU PWR

MXM 3V/5V Power switch

S	Yn
0	IA0
1	IA1

Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	MXM3.0	3B
Date: Friday, February 13, 2009	Sheet 17 of 39	


CRT IV@ EV@
SN74CBT3257CPWR (ALBT3257K18) TSSOP16 usd$0.075
PI5C3257LE (AL003257K36) TSSOP16 usd$0.13
At 11/19 Add it
S Yn
0 EV
1 IV
CRT_SENSE# [30]
MTW355
*VPORT_6
CM2009-02QR
LVDS
At 11/13 Modify
74LVC1G3157GW
PWM_SELECT# [14]
LVDS_BRIGHT
P_ID1 P_ID0 Resolution
0 0 DUAL CH
0 1 SINGLE CH
1 0 Reserved
1 1 Reserved
At 11/13 Modify
PI3LVD1012
dGPU_SELECT# Output
L EV_LVDS
H INT_LVDS
0.8A
GS12401-1011-40P-R-NH
modify footprint at B-test
LCD Power
AAT4280-4
Backlight Control
Q7 2N7002
Q6 2N7002
Q8 DTC144EUA
http://laptop-motherboard-schematic.blogspot.com/
Quanta Computer Inc.
PROJECT : ZY8
CRT/LVDS/LID
Rev 3B
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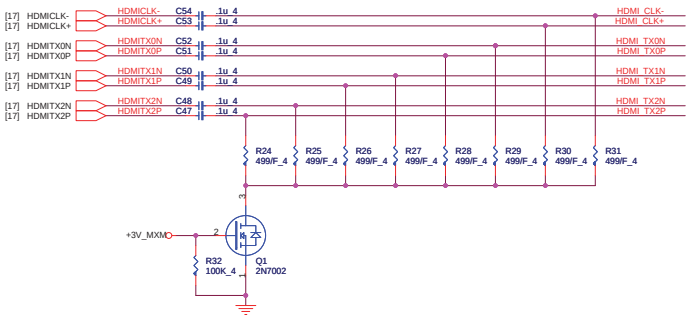
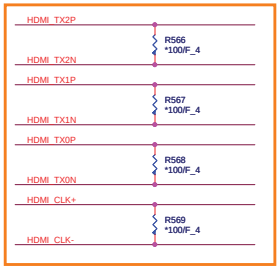
HDMI

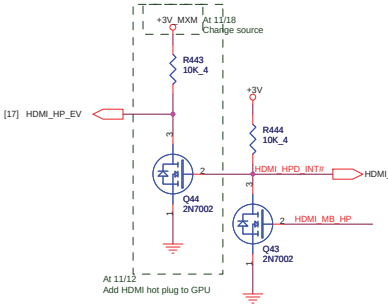
TMDS (DC-coupled)
DP(AC-coupled)



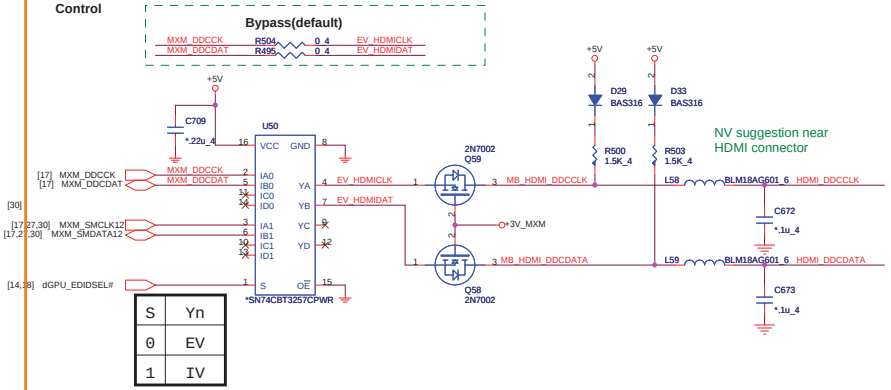


Close CN27

HDMI Hot-PLUG to SB and GPU

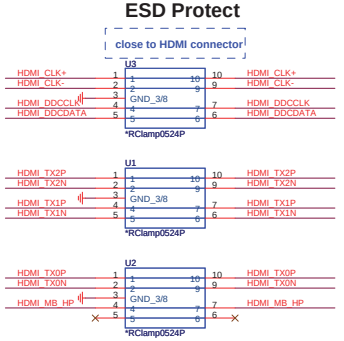


SDVO I2C Control

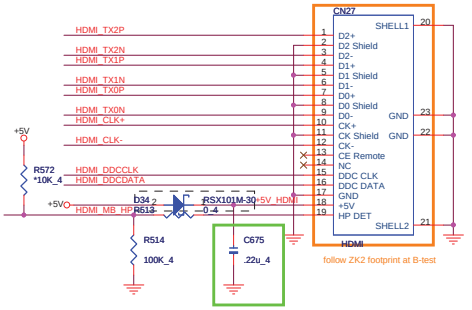


S	Yn
0	EV
1	IV

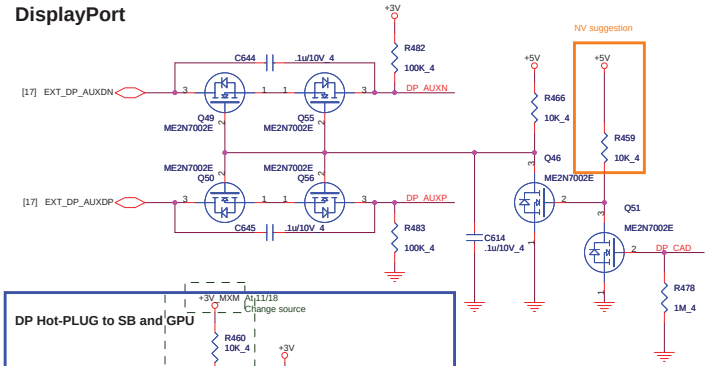
ESD Protect

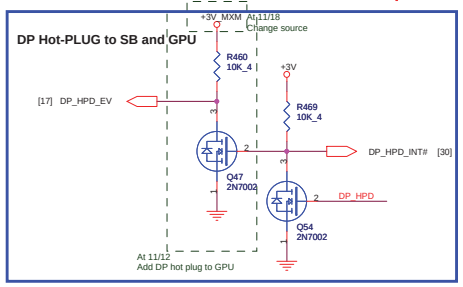


HDMI connector



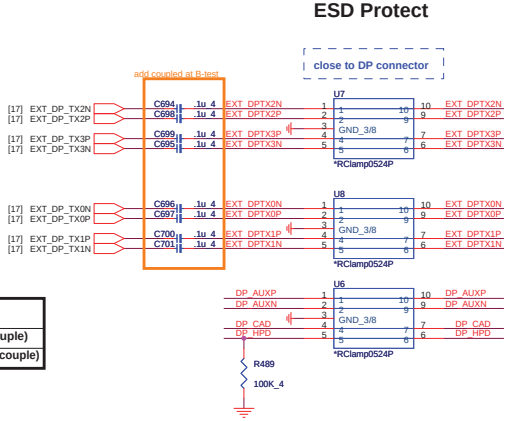
DisplayPort





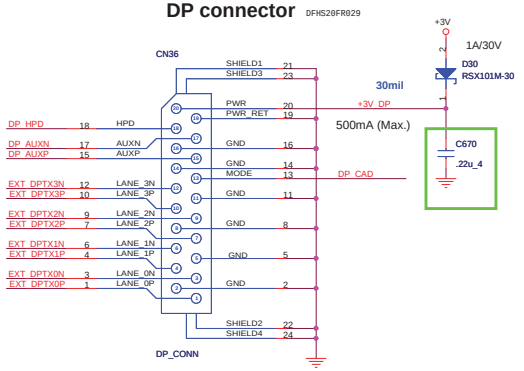
DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

ESD Protect



DP connector

DFHS20FR029



Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number | Rev
HDMI/DP | 3B
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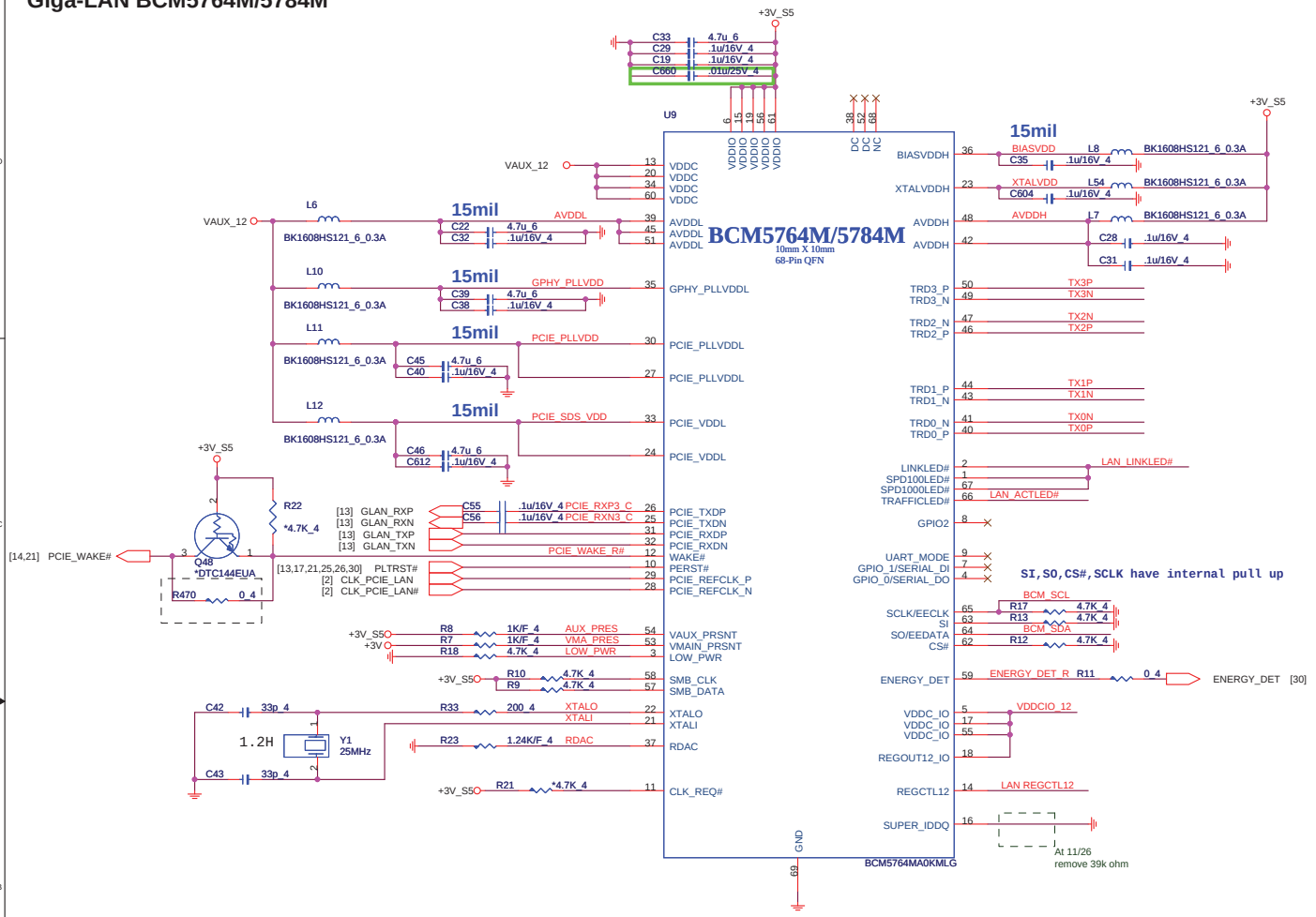
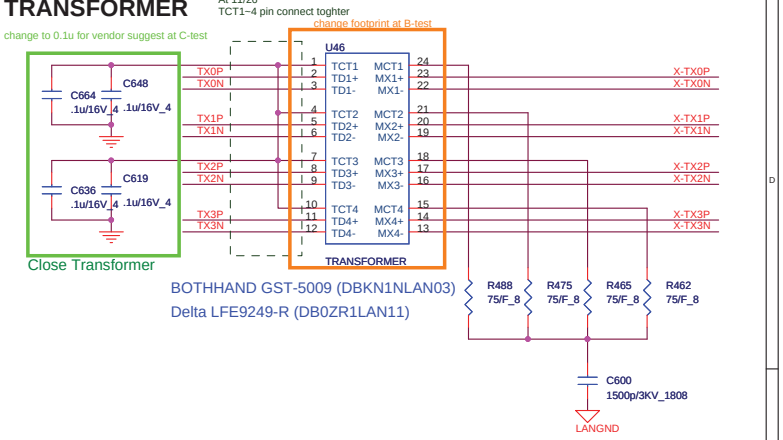
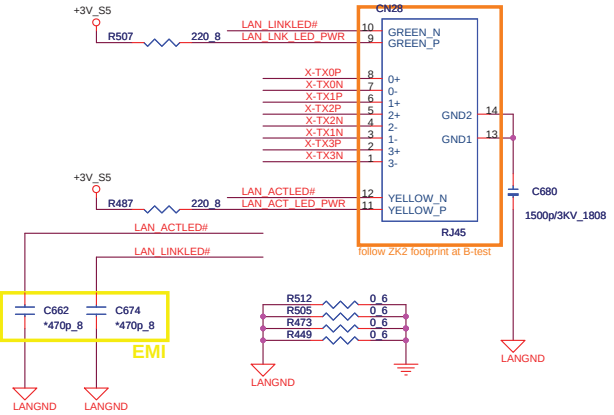
Giga-LAN BCM5764M/5784M



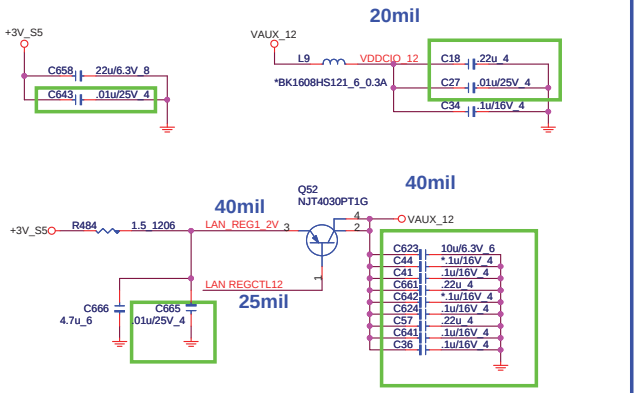
TRANSFORMER



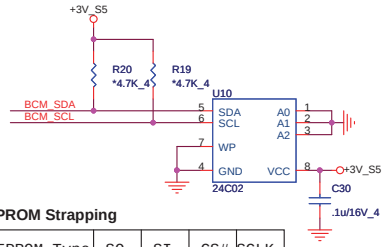
RJ45



LAN POWER



EEPROM



EEPROM Strapping

EEPROM Type	SO	SI	CS#	SCLK
24c02	1	0	0	0

Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number | Rev
LAN (BCM5764M/5784M) | 3B
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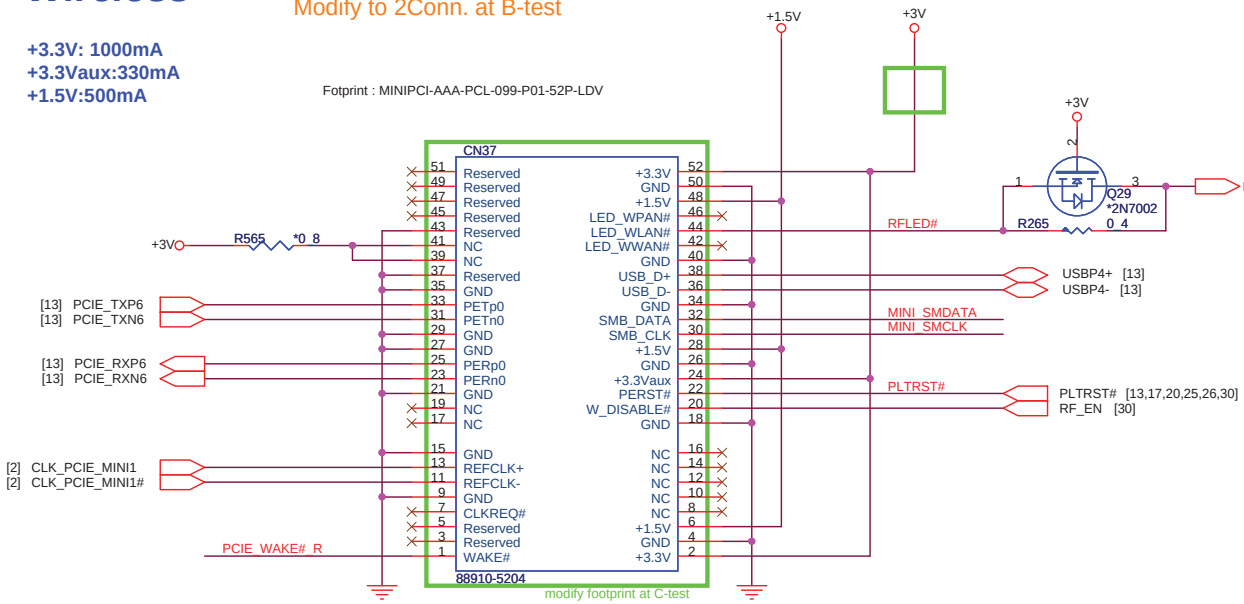
Wireless

Modify to 2Conn. at B-test

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Fotprint : MINIPCI-AAA-PCL-099-P01-52P-LDV



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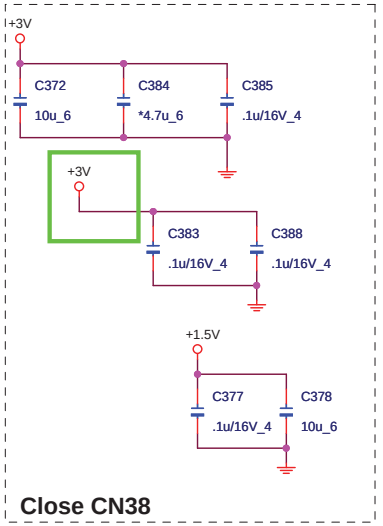
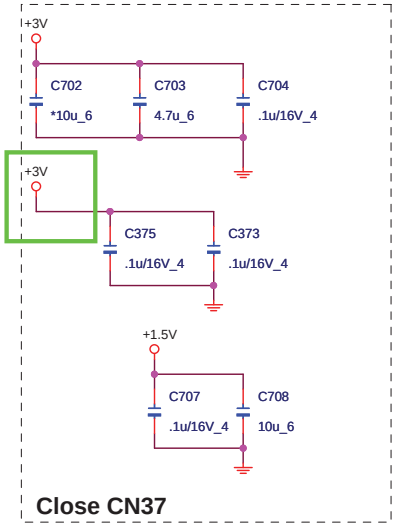
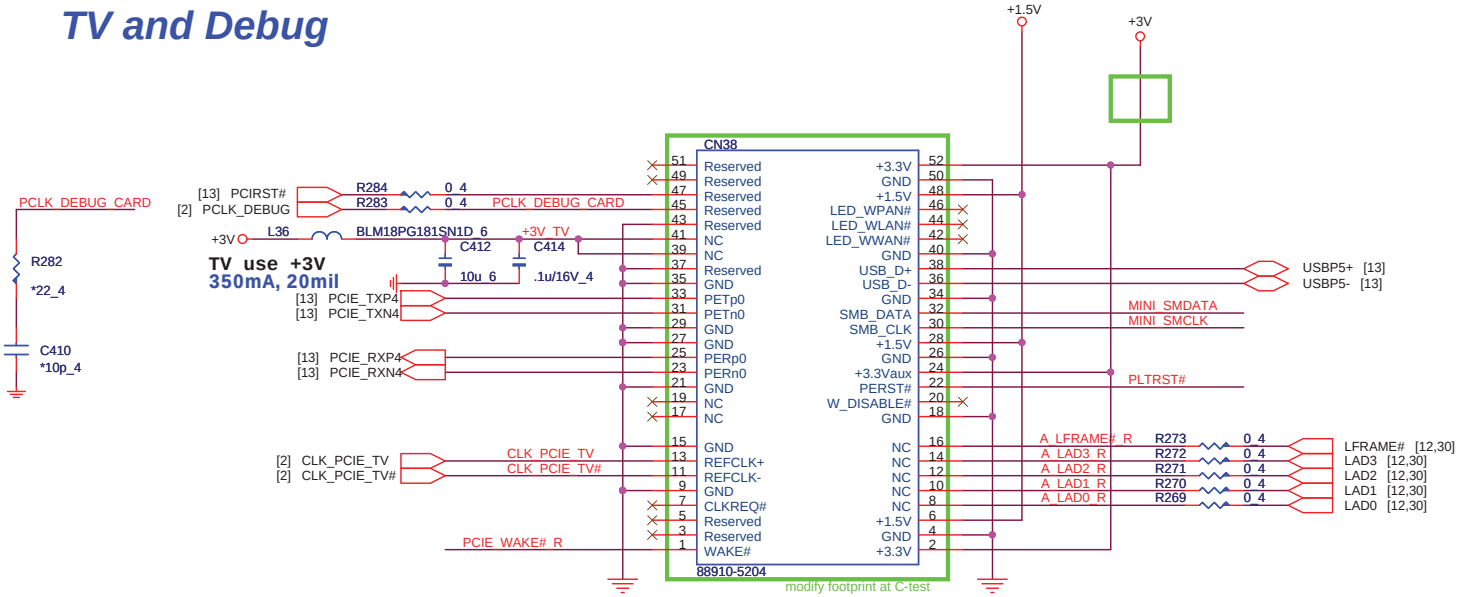
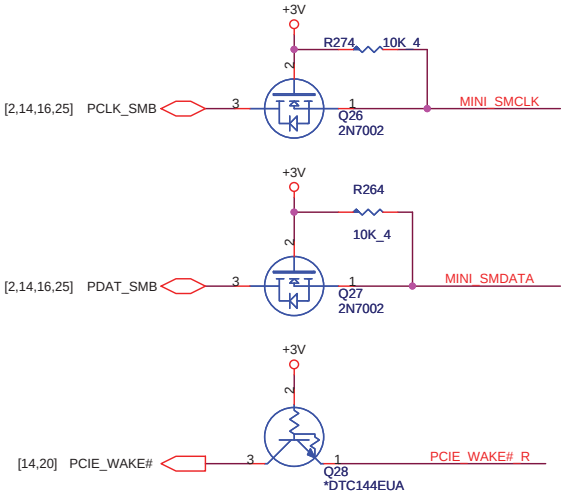




TV and Debug



H=9



Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	MINI PCI-E card/TV	3B
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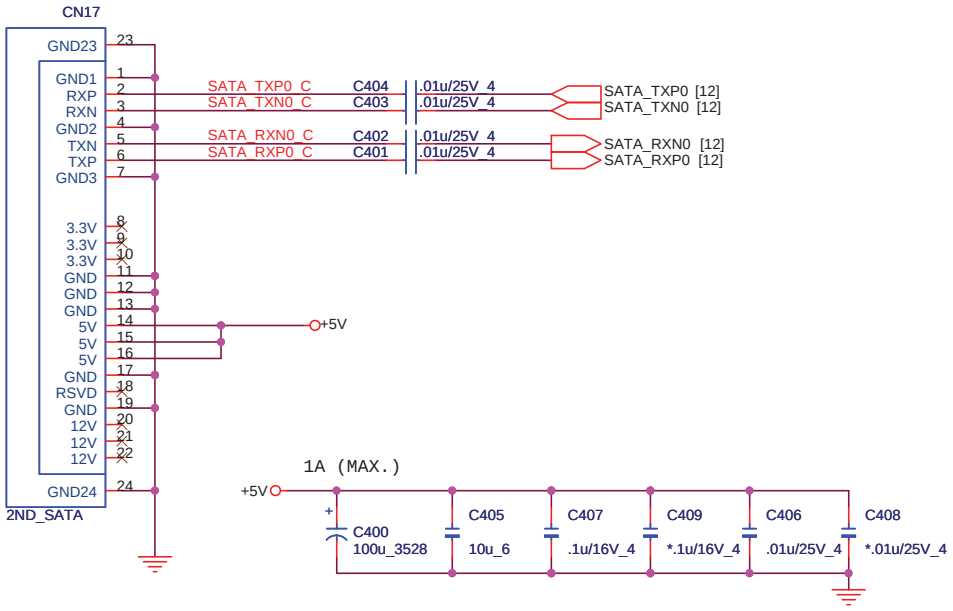
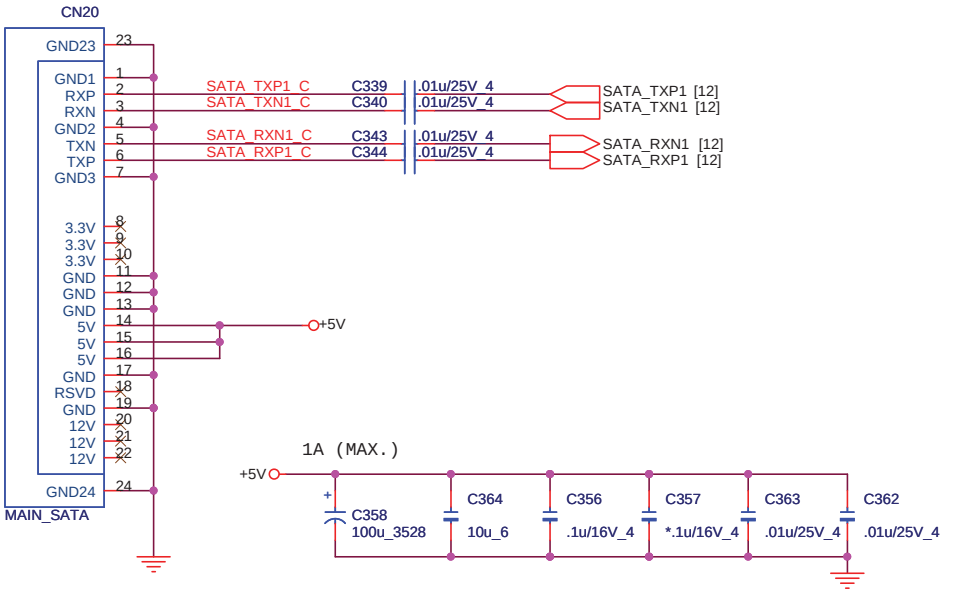
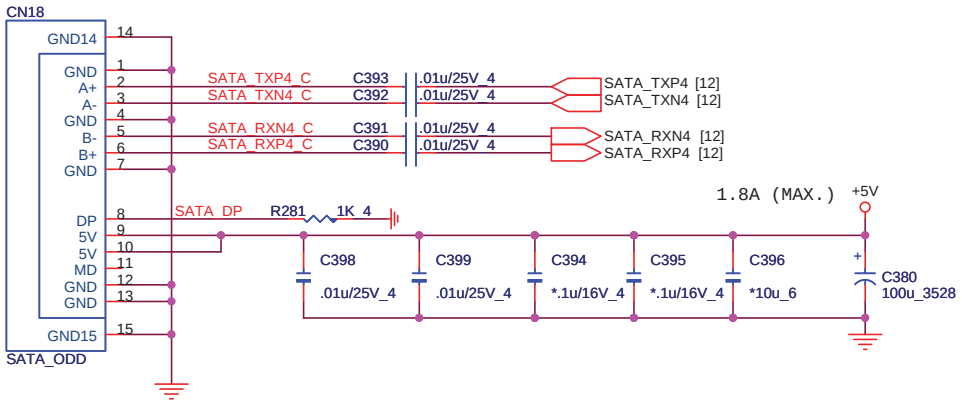
2nd SATA HDD (edge of board)



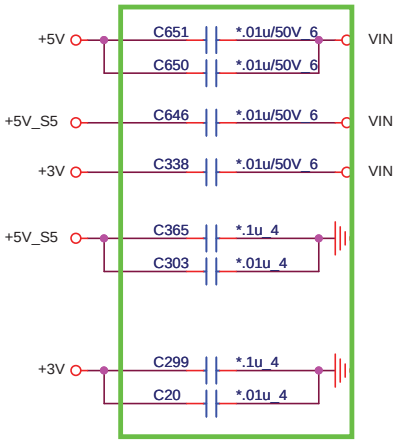
MAIN SATA HDD

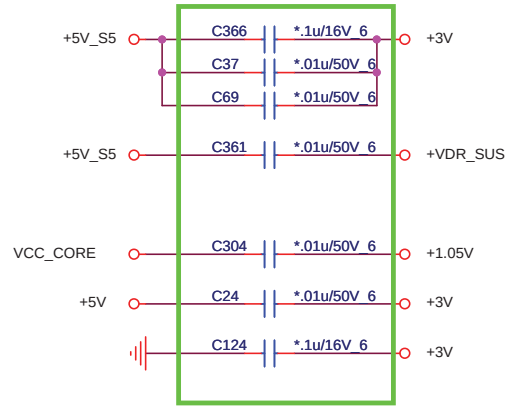


ODD (SATA)



EE RETURN-PATH CAPACITORS





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PROJECT : ZY8

Size	Document Number	Rev
	SATA-HDD/ODD	3B
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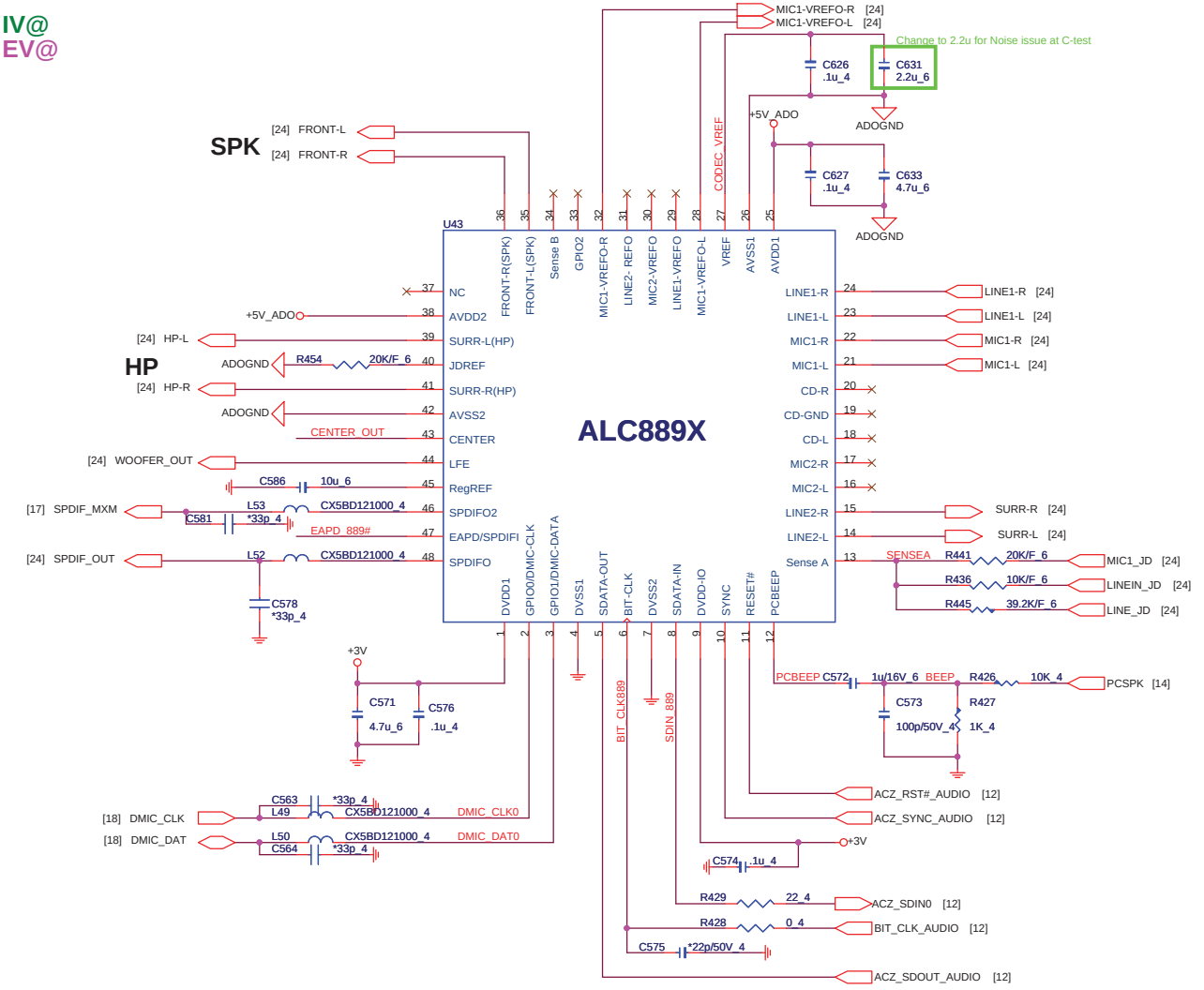
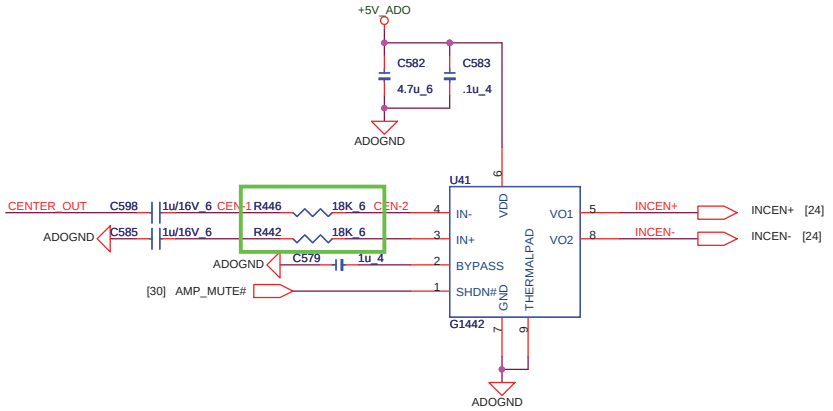
CODEC(ALC889X)

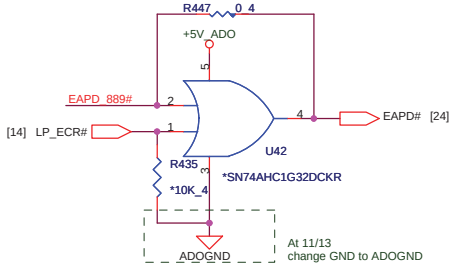
IV@
EV@



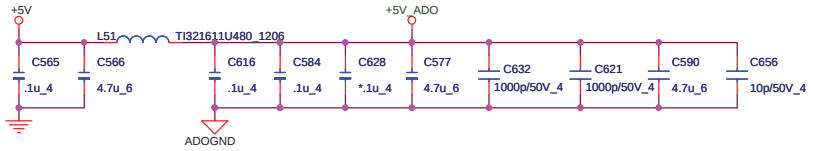
CENTER MONO



EAPD pin



CODEC/AMP Power



Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	REALTEK ALC889X/MONO-AMP	3B
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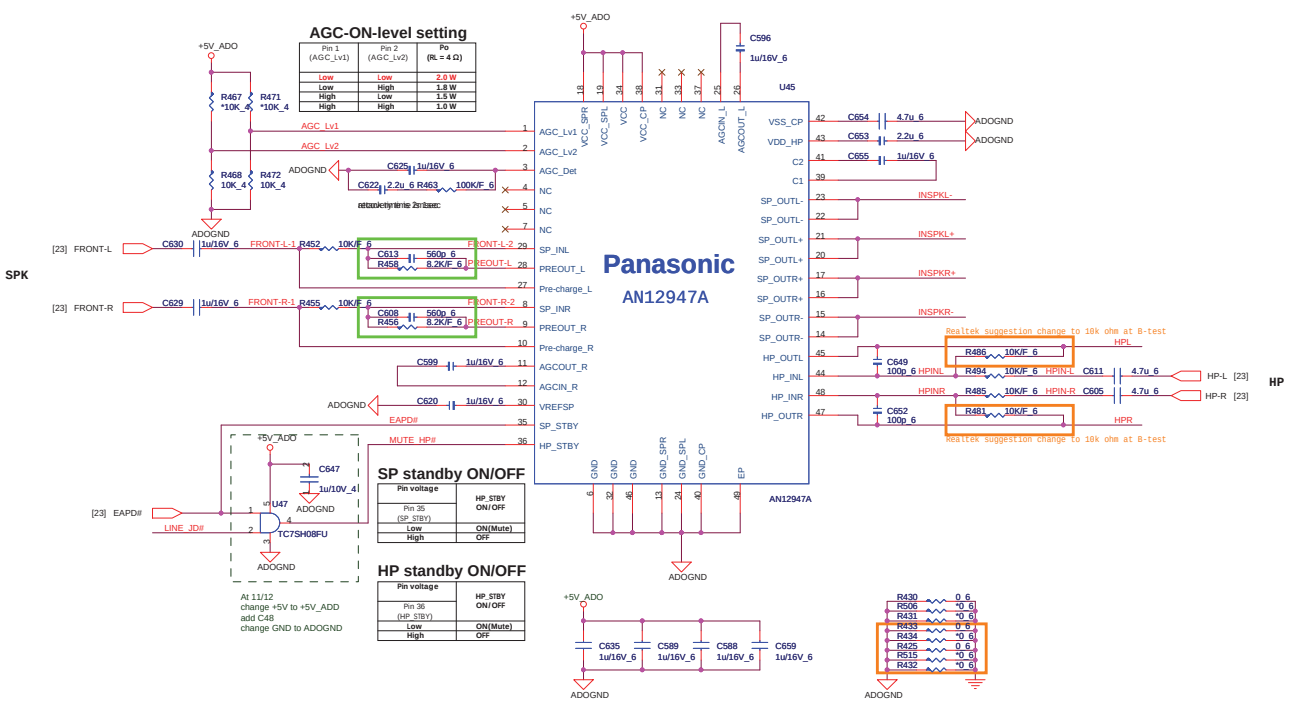
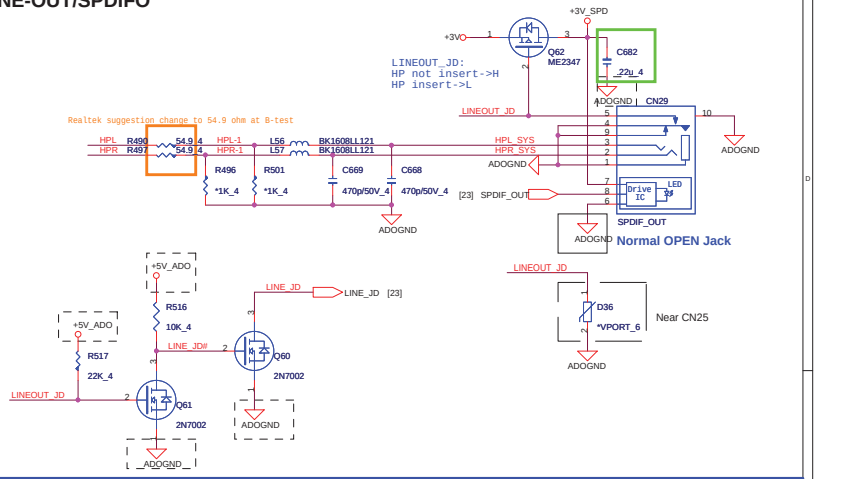
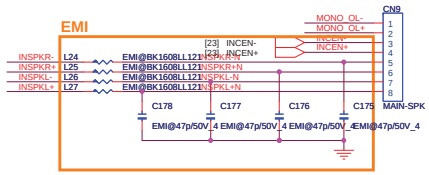
SPEAKER/HP AMP.



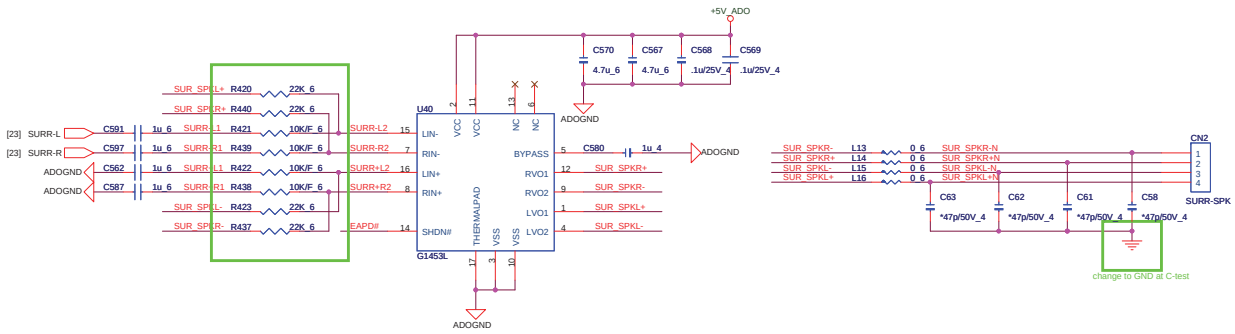
LINE-OUT/SPDIFO



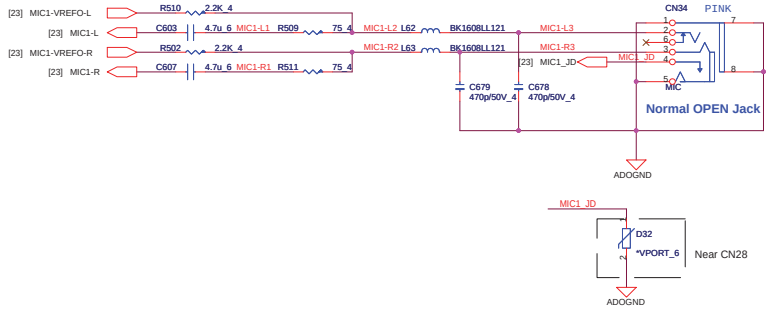
Main SPK/Center/Subwoofer



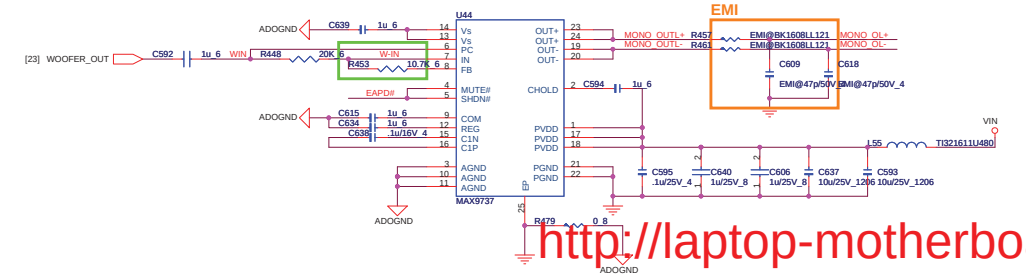
SURR-SPK



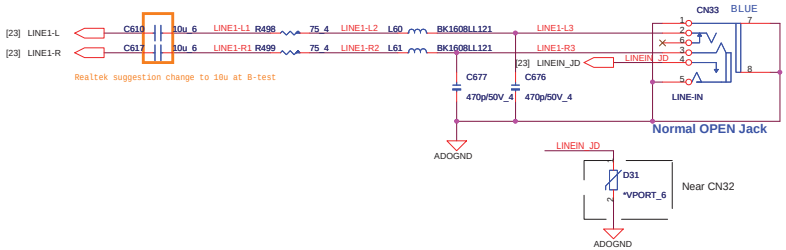
MIC



SUBWOOFER



LINE IN



Quanta Computer Inc.
PROJECT : ZY8
AMP/AUDIO JACK/WOOFER
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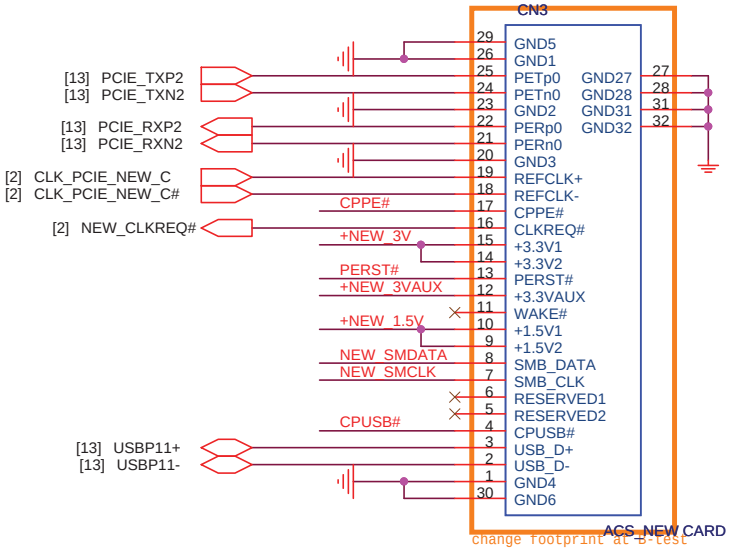
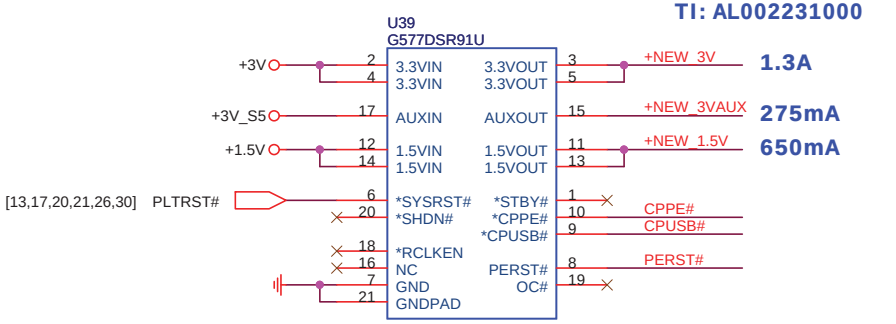
NEW CARD

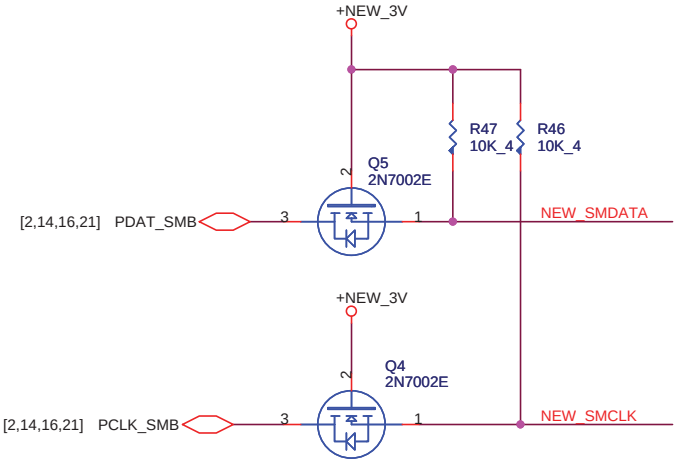


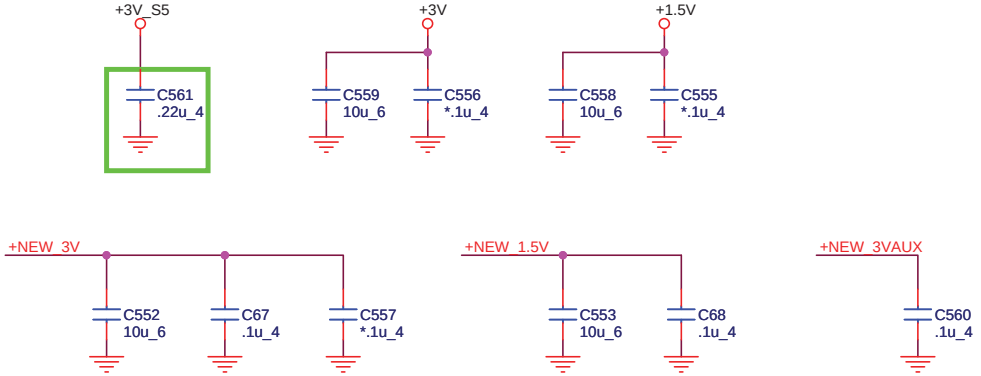
At 11/18
Change GMT cost down version.

NEW CARD'S POWER SWITCH

GMT: AL000577002
TI: AL002231000







Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	NEW CARD	3B
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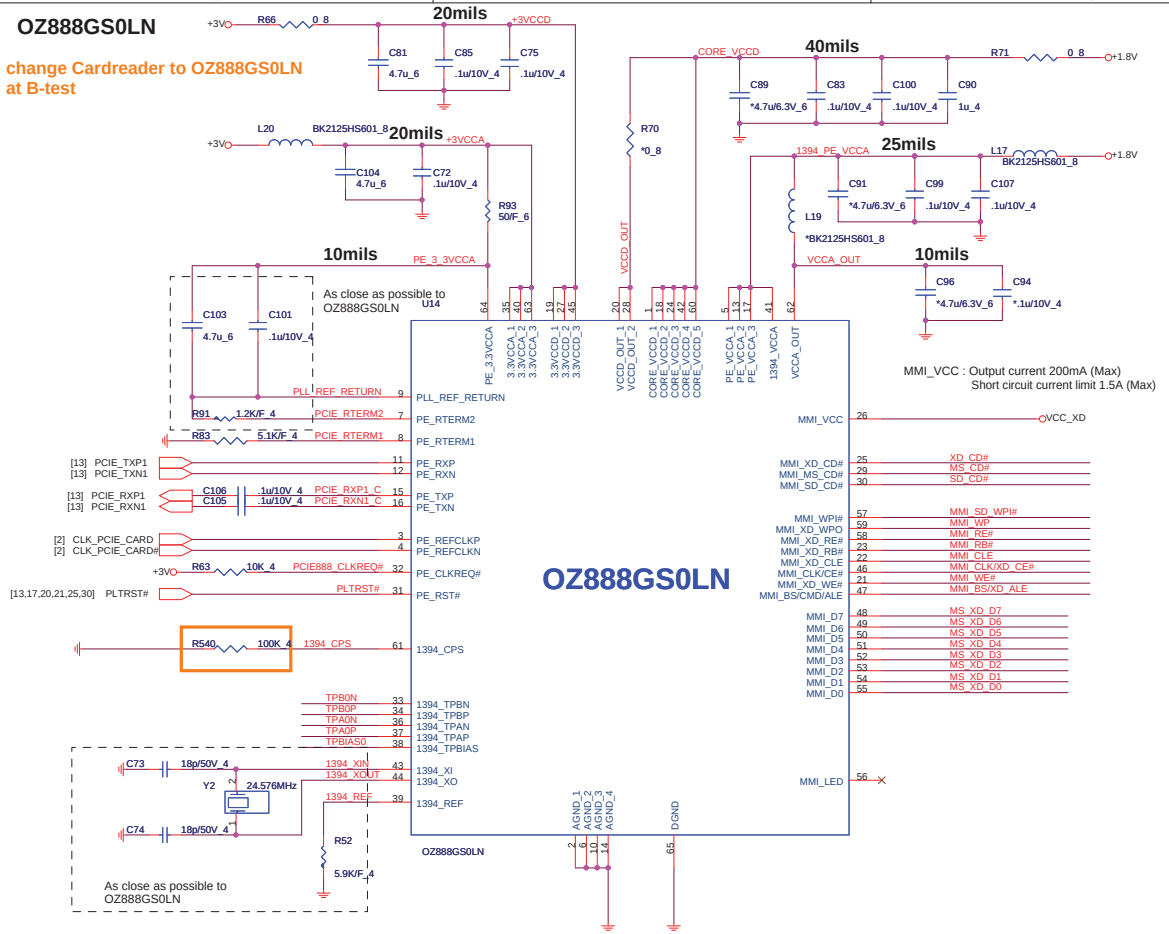
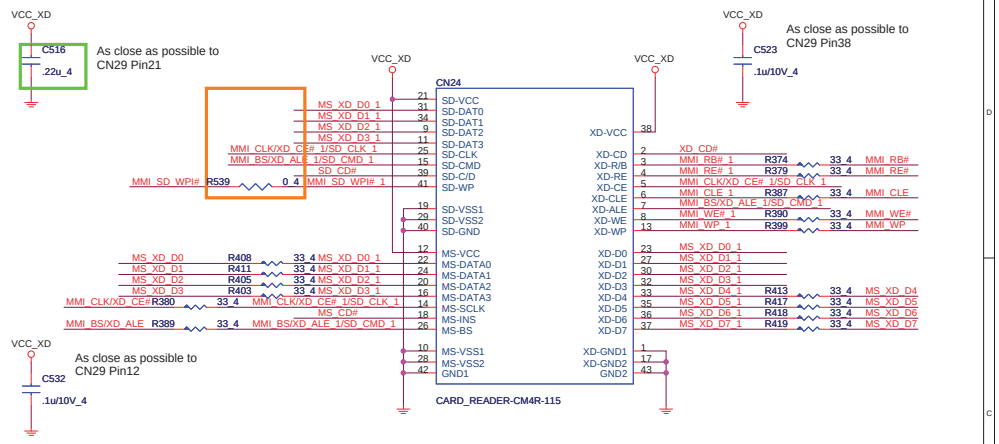
OZ888GS0LN

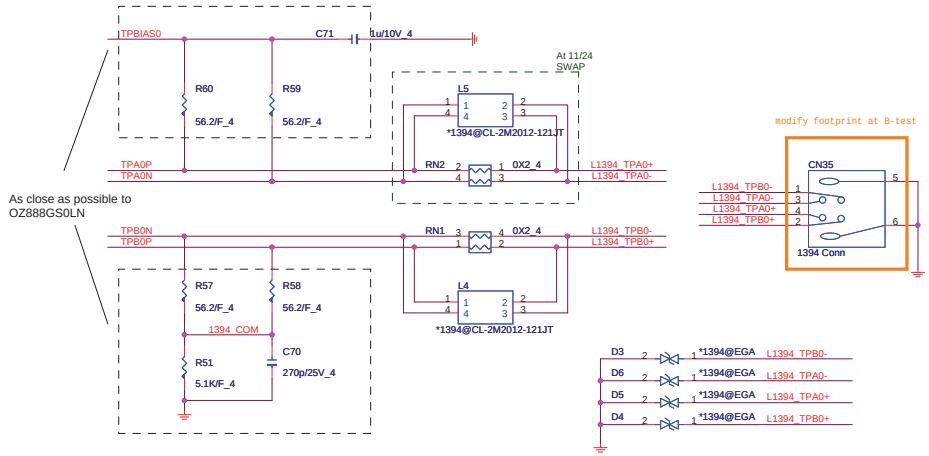
change Cardreader to OZ888GS0LN at B-test



5 IN 1 CARD READER



1394



Quanta Computer Inc.

PROJECT : ZY8

Size	Document Number	Rev
	OZ888GS0L1N	3B

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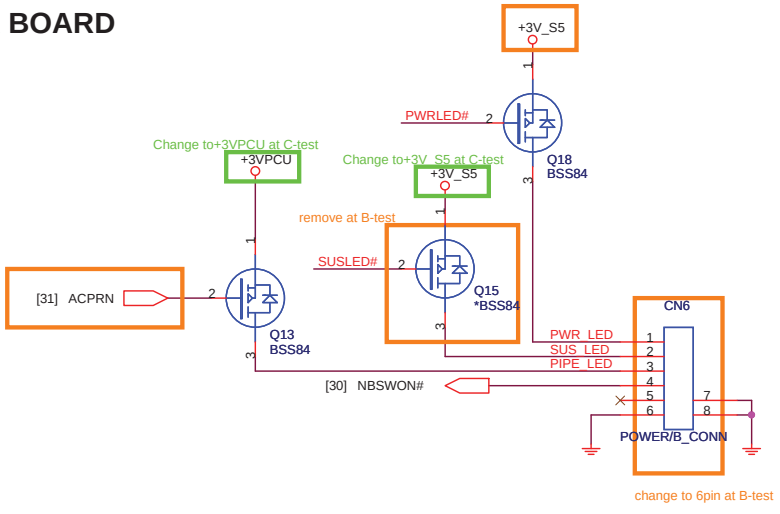
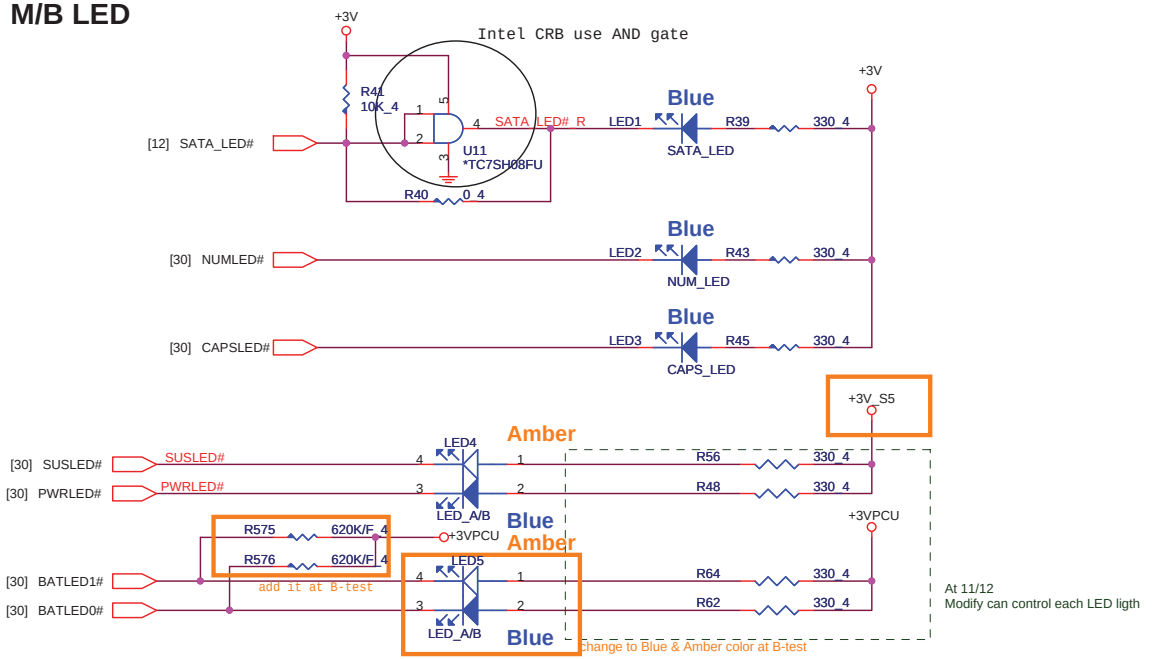
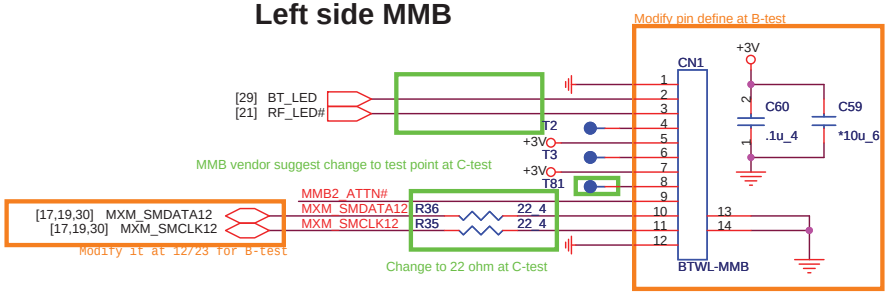
POWER BOARD



M/B LED

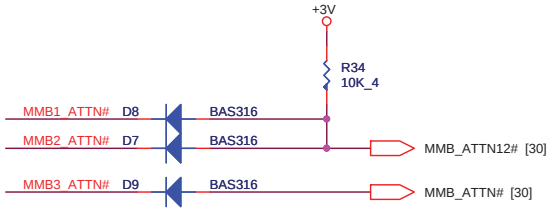


Left side MMB

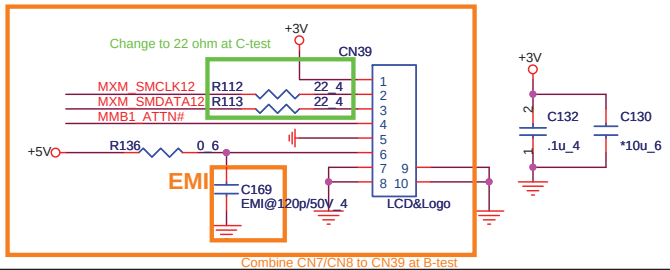


MXMCLK=MXM_SMCLK; MXMDATA=MXM_SMDATA12
MMB1 and MMB2 need add ISOLATE circuit where are on MXM page.

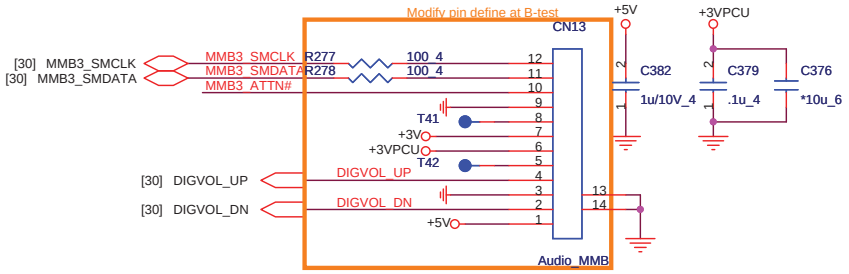
MMB Status



LCD BL_ON/OFF MMB & Backlight Logo LED



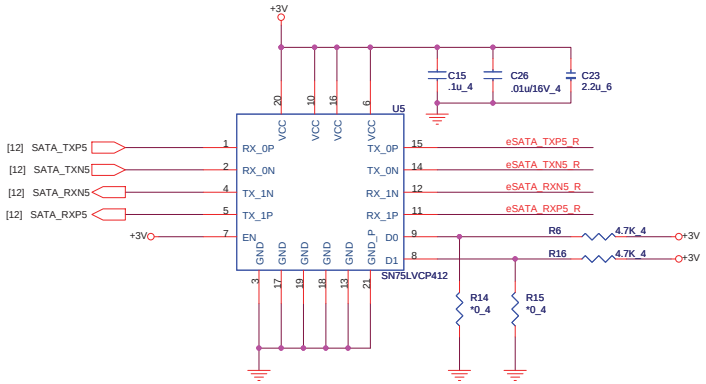
Right Side MMB



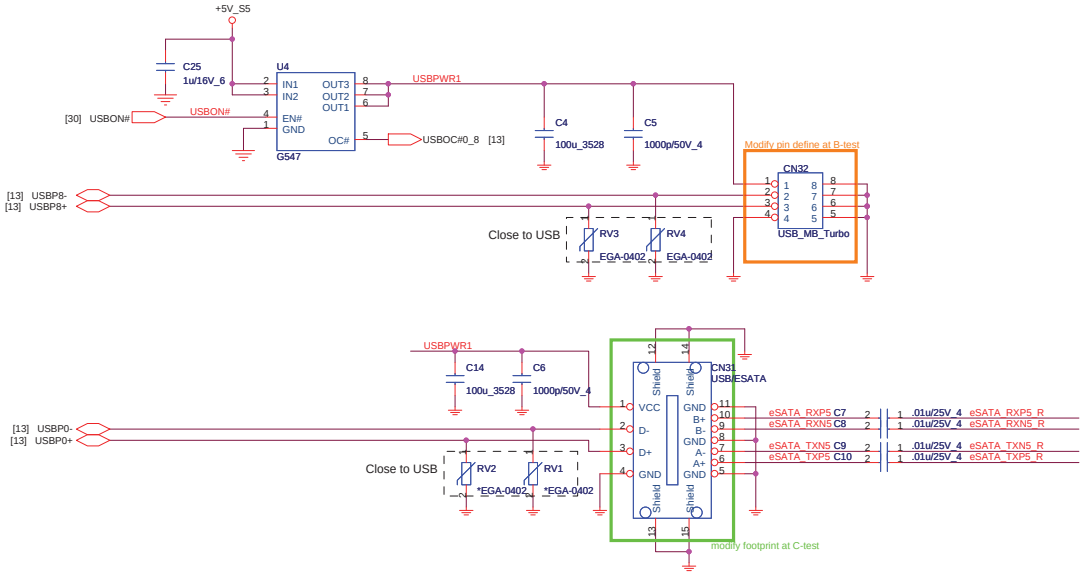
Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	3B
Date: Friday, February 13, 2009	Sheet 27 of 39	

USB & ESATA

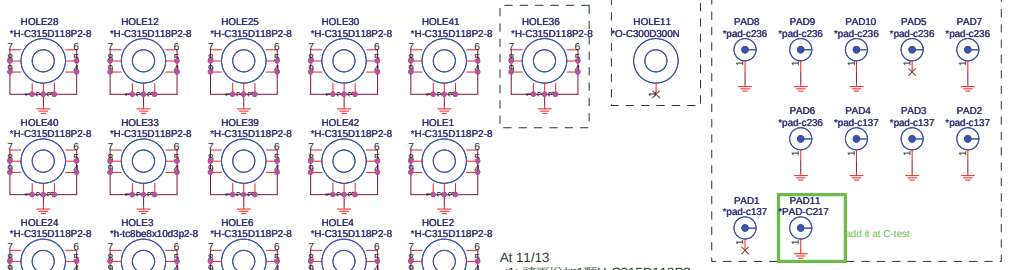


EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

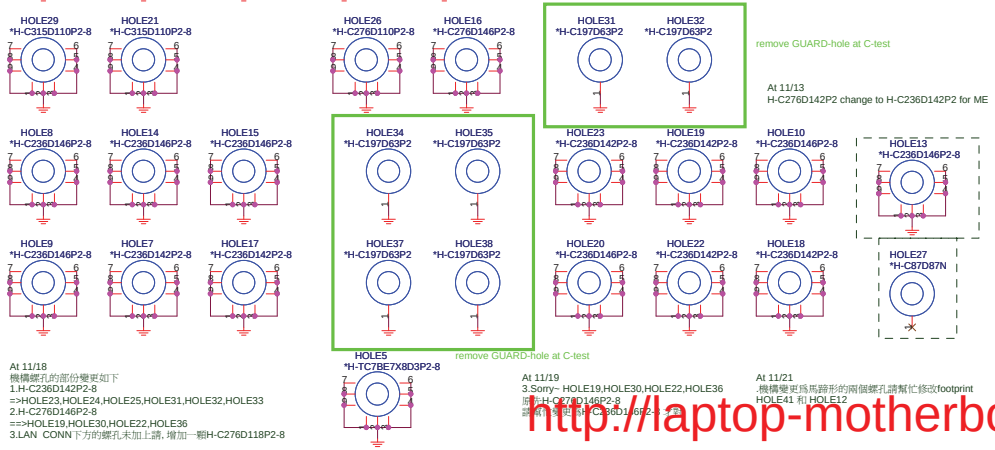


HOLES

At 11/13
change HOLE1~38 1PIN to 9PIN



At 11/13
<1>請再增加1顆H-C315D118P2
<2> HOLE22 請變更爲H-C236D142P2 (機構有改小)
<3>增加 1顆固定孔H-C87D87N ,(1788.00 944.00)



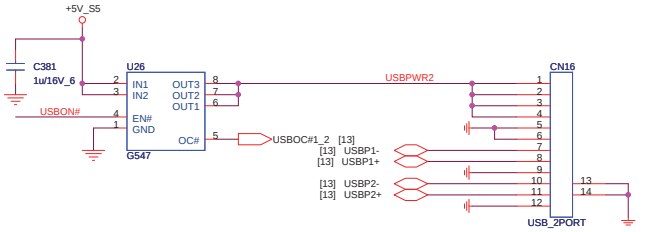
At 11/13
H-C276D142P2 change to H-C236D142P2 for ME

At 11/18
機構螺孔的部份變更如下
1.H-C236D142P2-8
=>HOLE23,HOLE24,HOLE25,HOLE31,HOLE32,HOLE33
2.H-C276D146P2-8
==>HOLE19,HOLE30,HOLE22,HOLE36
3.LAN CONN下方的螺孔未加上請, 增加一顆H-C276D118P2-8

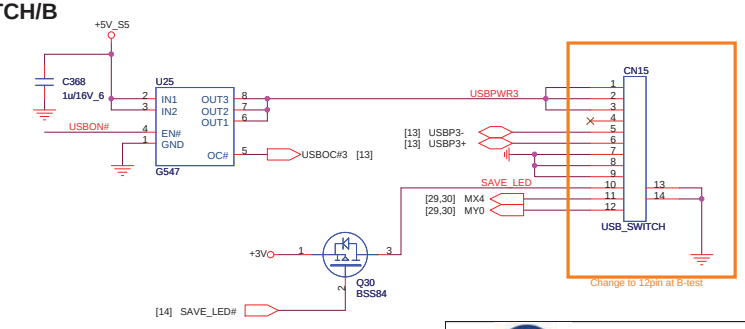
At 11/19
3.Sorry~ HOLE19,HOLE30,HOLE22,HOLE36
請改H-C276D146P2-8
請改H-C236D146P2-8

At 11/21
.機構變更爲馬蹄形的兩個螺孔請幫忙修改footprint
HOLE41 和 HOLE12

USB_2PORT/B



USB_SWITCH/B



Quanta Computer Inc.
PROJECT : ZY8
Size: Document Number: USB/eSATA Rev 3B
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INT K/B

At 11/18 SWAP

CP6 *100px4: MX3 MX2 MX1 MX0
CP5 *100px4: MX7 MX6 MX5 MX4
CP1 *100px4: MY0 MY1 MY2 MY3
CP2 *100px4: MY4 MY5 MY6 MY7
CP3 *100px4: MY8 MY9 MY10 MY11
CP4 *100px4: MY12 MY13 MY14 MY15
C323 *100p_4 MY16
C331 *100p_4 MY17

CN11 → KB

[28,30] MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15 MY16 MY17
[30] MX7 MX6 MX5
[28,30] MX4
[30] MX3 MX2 MX1 MX0

+3VPCU
RP1 10K_10P8R: MX4 MX5 MX6 MX7 / MX3 MX2 MX1 MX0

TOUCHPAD & Finger-Printer CONN.

+5V
R238 10K_4
R239 10K_4
L31 BLM21P300S
C335 .1u/16V_4
20mil
L32 LZA10-2ACB104MT
L33 LZA10-2ACB104MT
[30] TPDATA
[30] TPCLK
C337 *.01u/25V_4
C336 *.01u/25V_4
+TPVDD
TPDATA_R
TPCLK_R
CN12
[13] USBP7-
[13] USBP7+
USBP7-
USBP7+
MX2
MY0
TP_LED
RV5 *EGA-0402
RV6 *EGA-0402
add ESD protect at B-test
+3V
Q25 BSS84
[30] TP_LED#
[14,18,30] LID591#
+3VPCU
TP_FP_CONN

BLUETOOTH CONNECTOR

Change +3VSUS to +3V_S5 at B-test
+3V_S5
Q31 AO3413
[30] BT_POWERON#
30mil
BT_POWER
C389 2.2u_6
C397 1000p/50V_4
[13] USBP6+
[13] USBP6-
[27] BT_LED
CN14 BT_CONN
C386 *.01u_4

Keyboard LED control

Remove: U12, C64, R44, C66.
Stuff: Q3, R42, Q2
at C-test

+5V
C64 *2.2u_6
U12
VIN VO
/FON GND GND GND
VSET GND
*G991
R44 *10K_4
[30] KB_LED
20mil
KB_LED_PWR
C66 *10u_6
C65 .01u/25V_4
KBPWR = 1.6*VSET
change pin define at B-test
CN4 KB_LED
check pin define
R42 10K_4
Q3 AO3413
KB_LED#
Q2 DTC144EU

CPU FAN

+3V
+5V
R480 10K_4
R464 10K_4
R474 10K_4
R477 10K_4
FAN_PWM_E
[30] FANSIG
CN26 FAN
[3] CPUFAN#_ON
R476 10K_4
FAN_PWM_B
Q57 MMBT3904
Q53 MMBT3904
FAN_PWM_CN
30mil
[30] CPUFAN#

Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	KB/FAN/TP+FP/BT	3B

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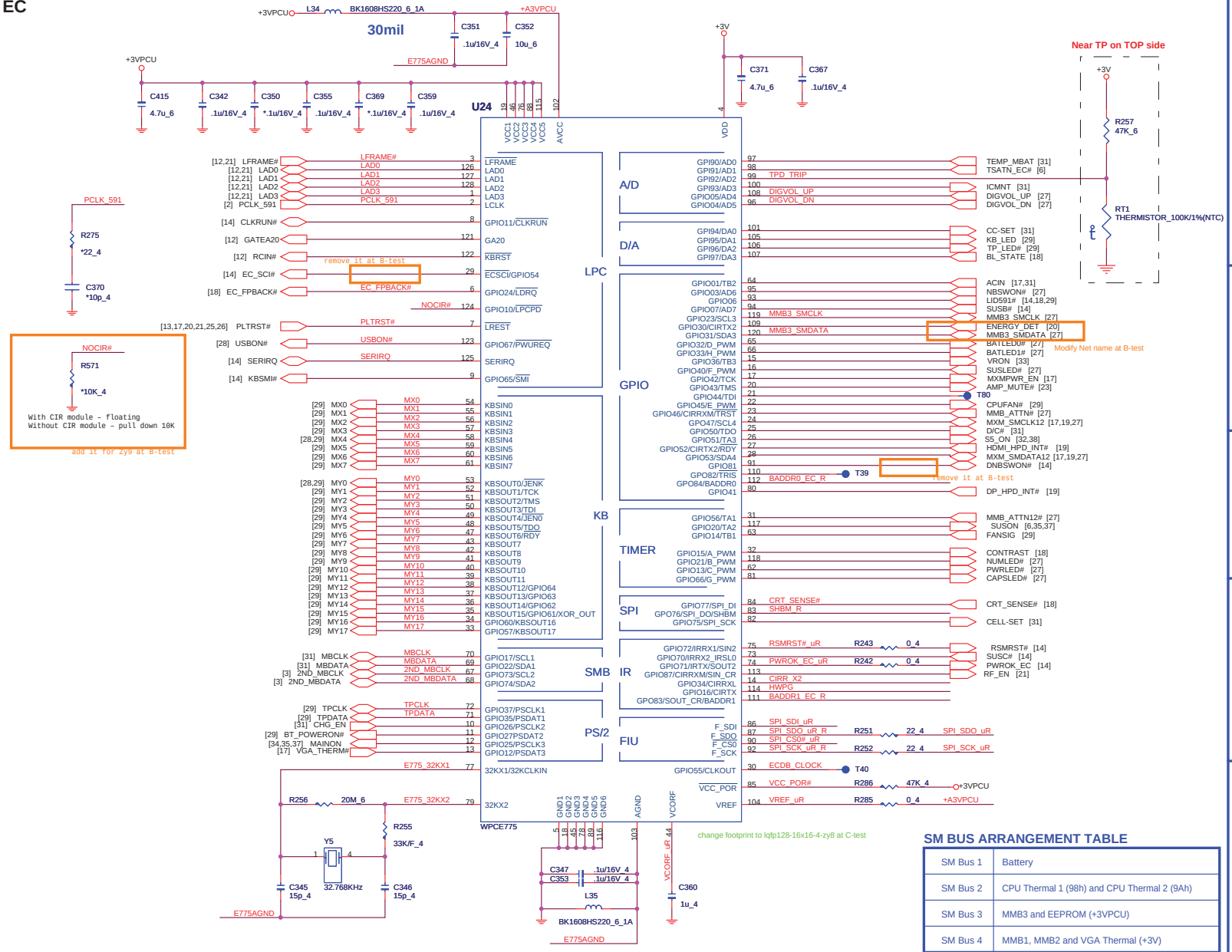
EC



I/O ADDRESS SETTING

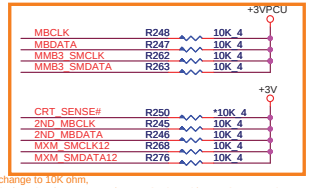
BADDR1-0	I/O Address	
	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0_EC_R — R260 — 10K_4
BADDR1 — BADDR1_EC_R — R259 — *10K_4
SHBM — SHBM_R — R249 — 10K_4

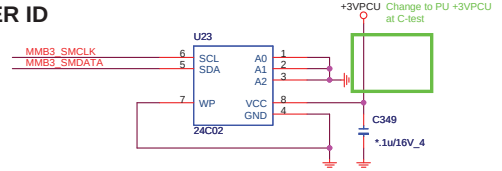
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

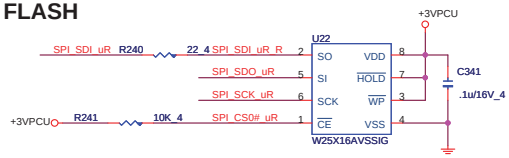


change to 10K ohm,
2nd MBCLK/MBDATA and MXM_SMCLK12/MXM_SMDATA12 PU to +3V at B-test

ACER ID



SPI FLASH

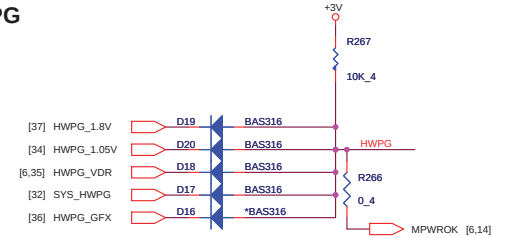


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

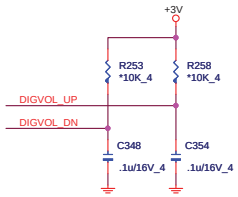
At 11/24 add

Winbond	W25X16AVSSIG	AKE38ZP0N01
MXIC	MX25L1605AM2C-15G	AKE37FP0Z13
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

HWPG

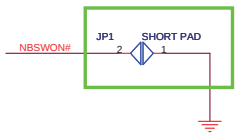


VR Cap.

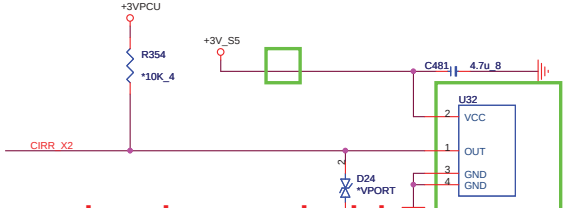


Place two near EC

POWER-ON Switch

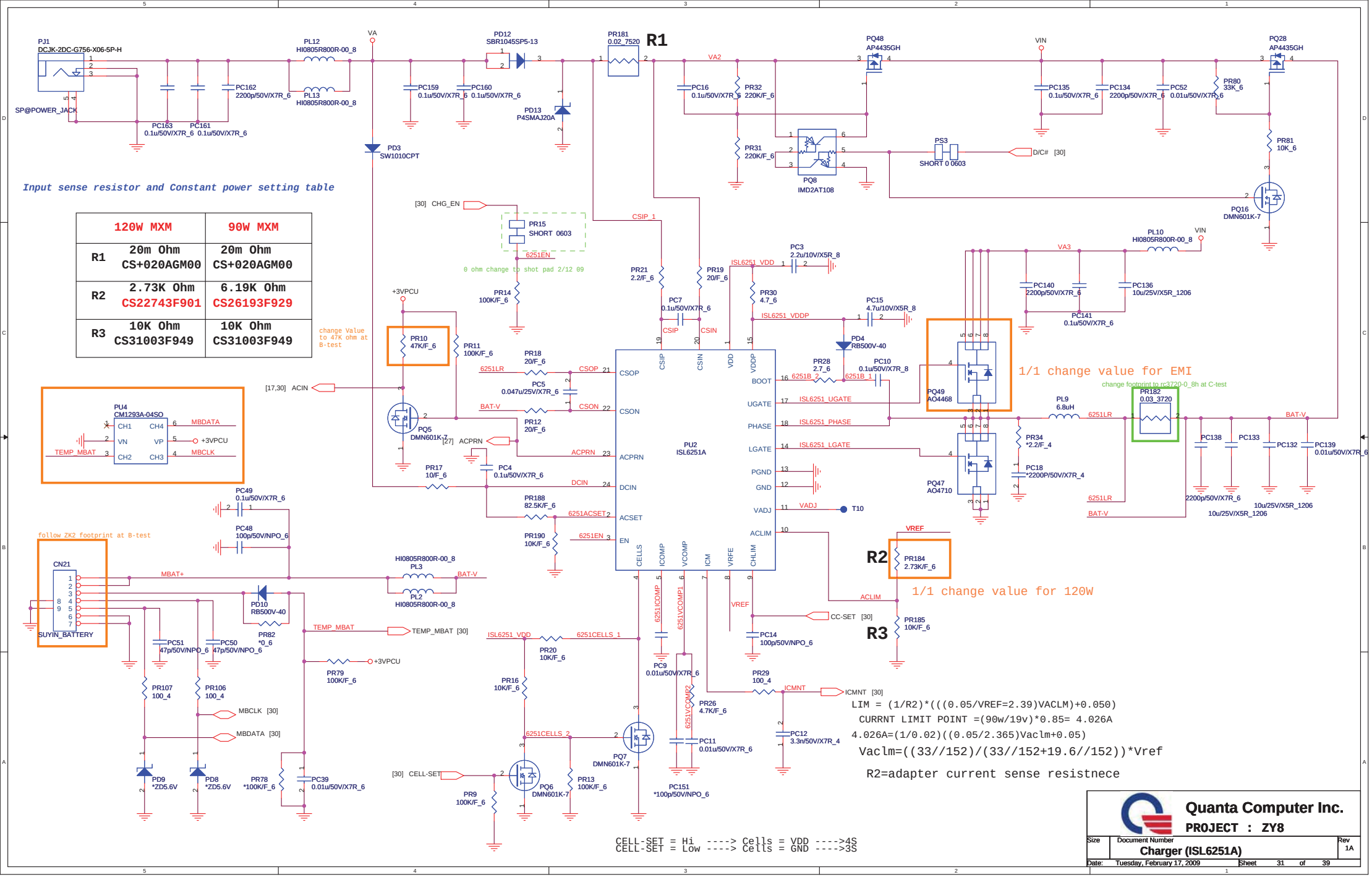


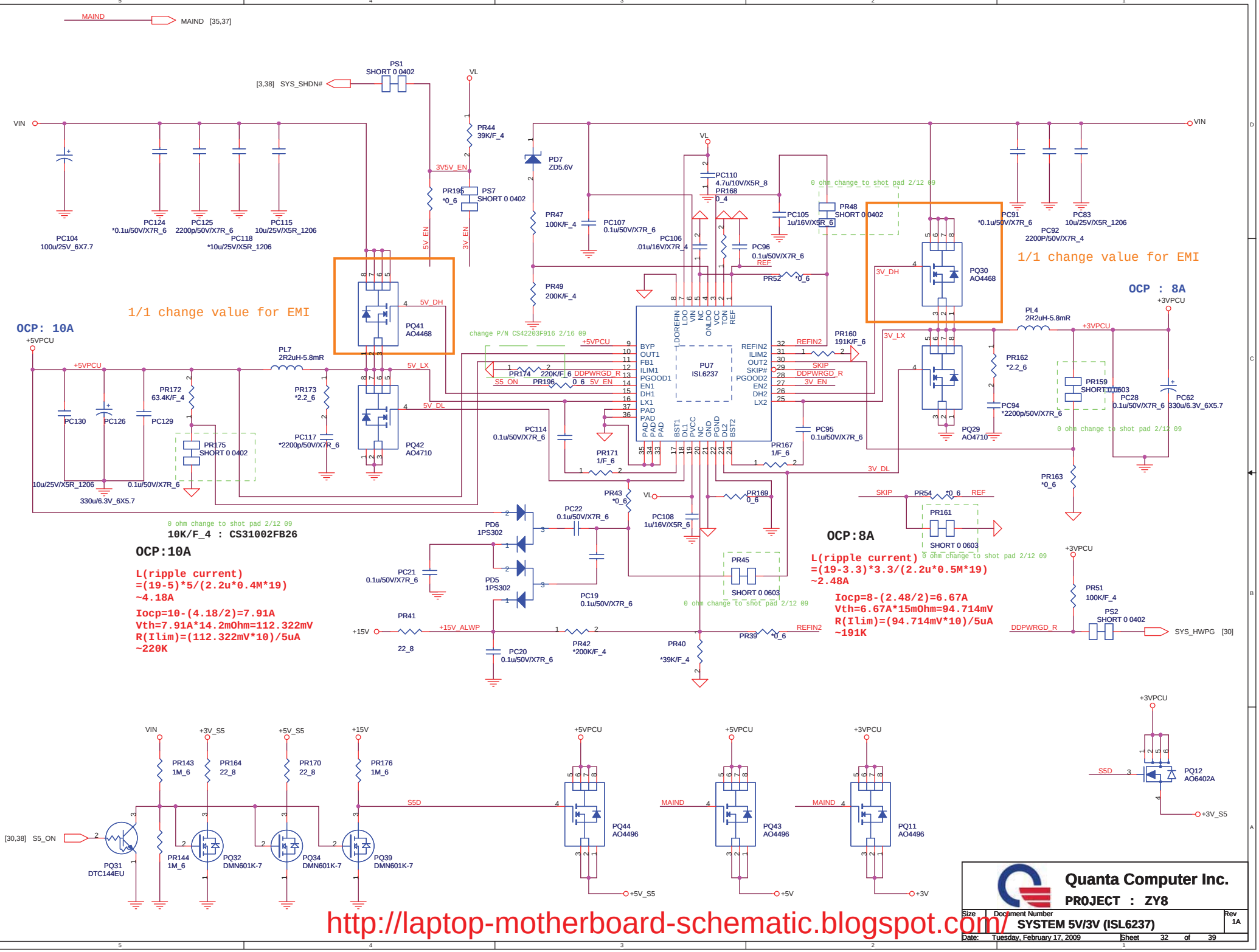
CIR

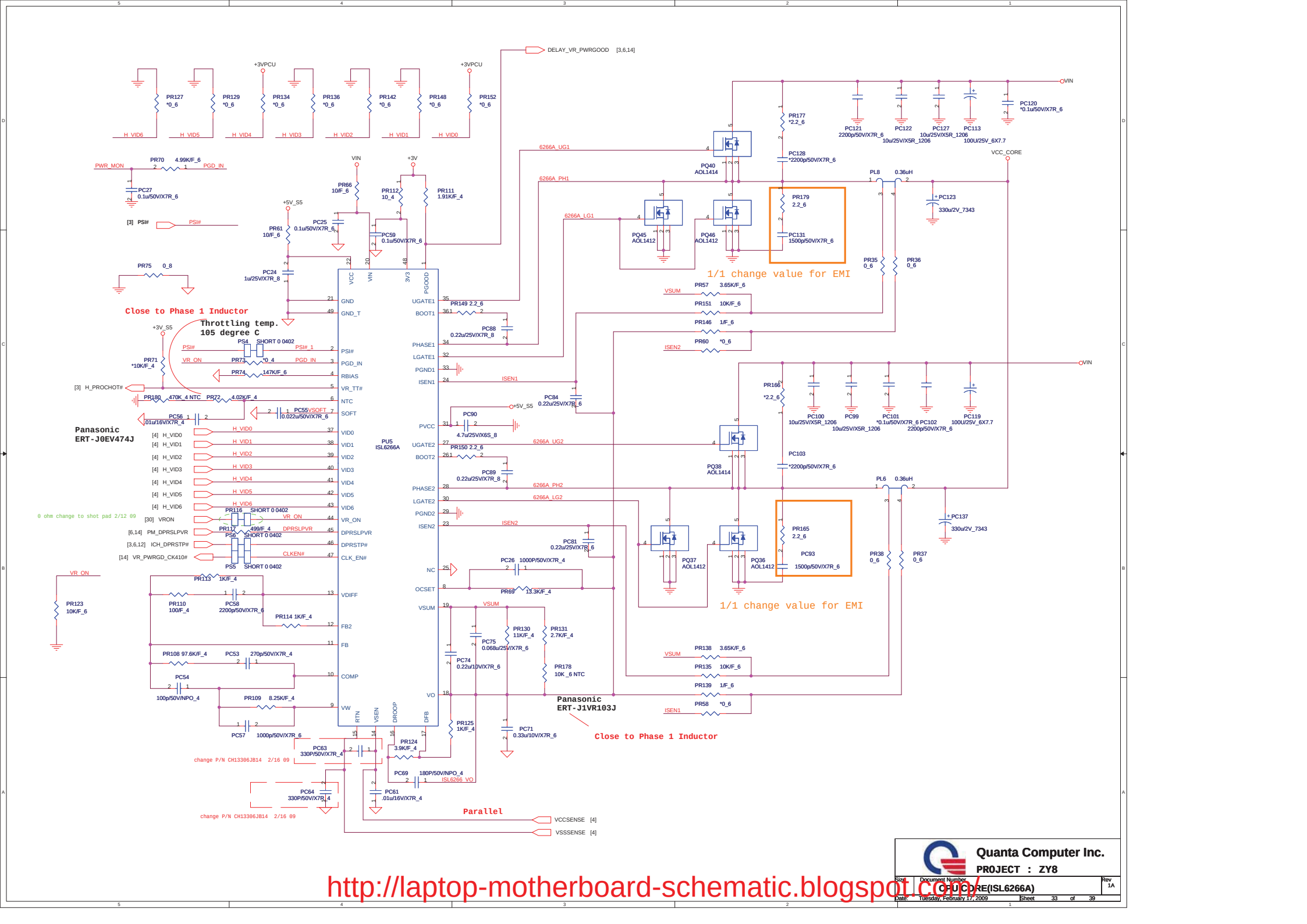


INTERNAL KEYBOARD STRIP SET

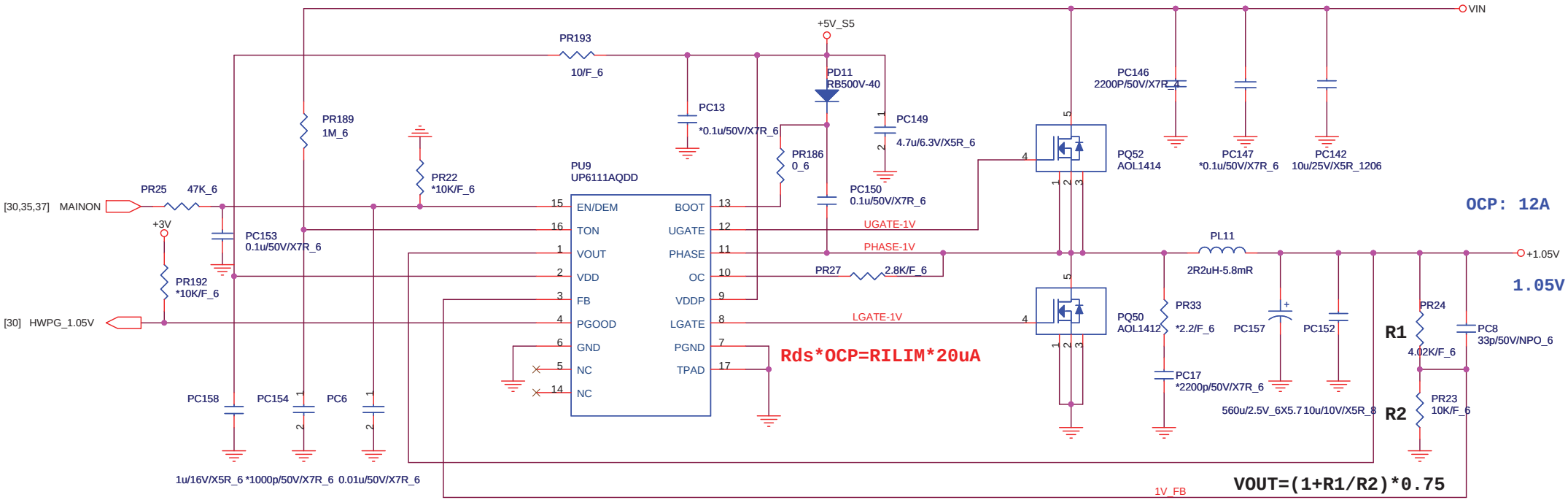
Quanta Computer Inc.			
PROJECT : ZY8			
Size	Document Number		Rev
	WPCE775C_0DG & FLASH		3B
Date: Friday, February 13, 2009		Sheet 30 of 39	







Quanta Computer Inc.
PROJECT : ZY8
Size: Document Number: CPU CORE(ISL6266A) Rev 1A
Date: Tuesday, February 17, 2009 Sheet 33 of 39



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AOL1412 Rdson=4.6mOhm

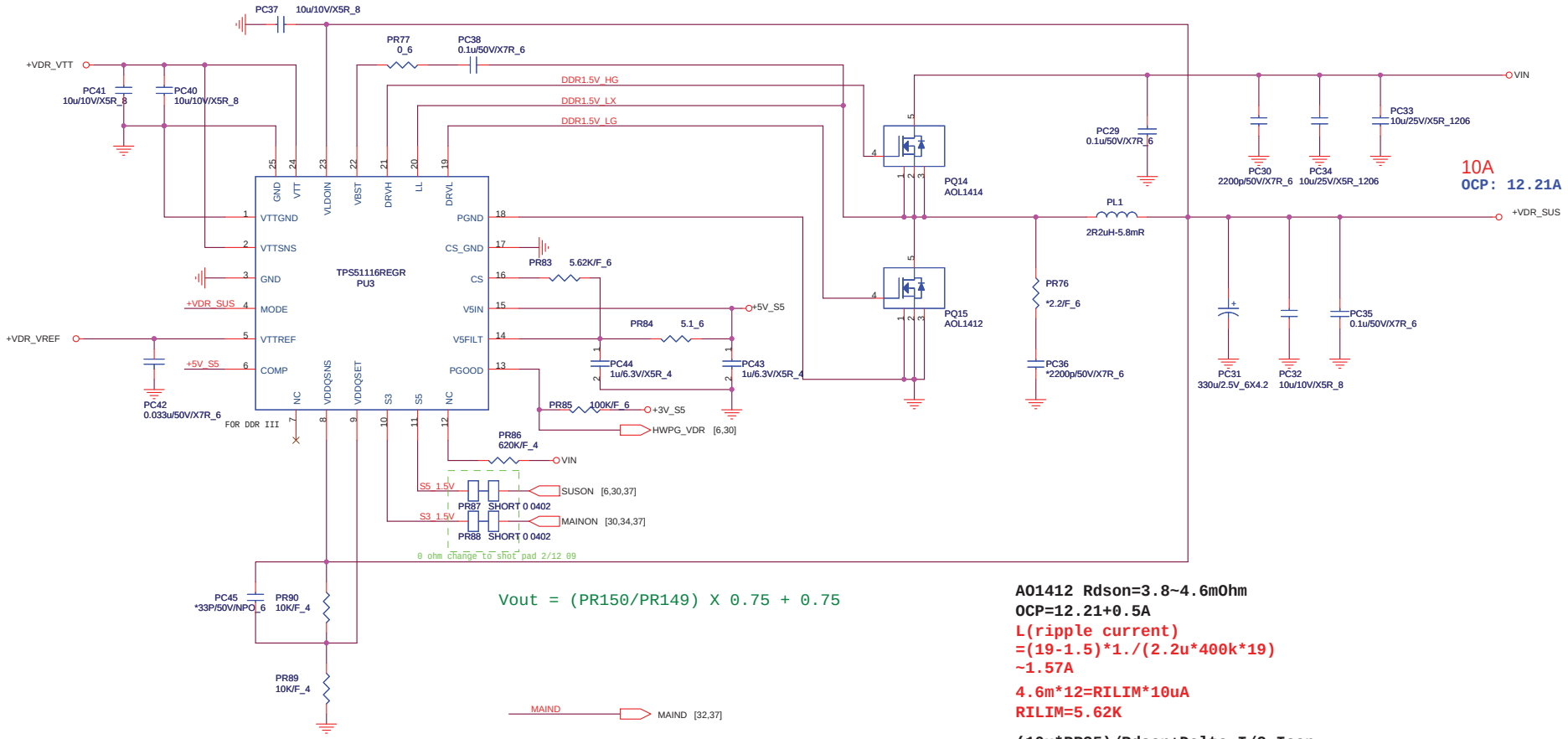
OCP=16-0.8A

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

4.6m*12=RILIM*20uA

RILIM=2.76K--- 2.8K

Quanta Computer Inc.		
PROJECT : ZY8		
Size	Document Number: VCCP 1.05V(UP6111A)	Rev: 1A
Date: Tuesday, February 17, 2009	Sheet 34 of 39	

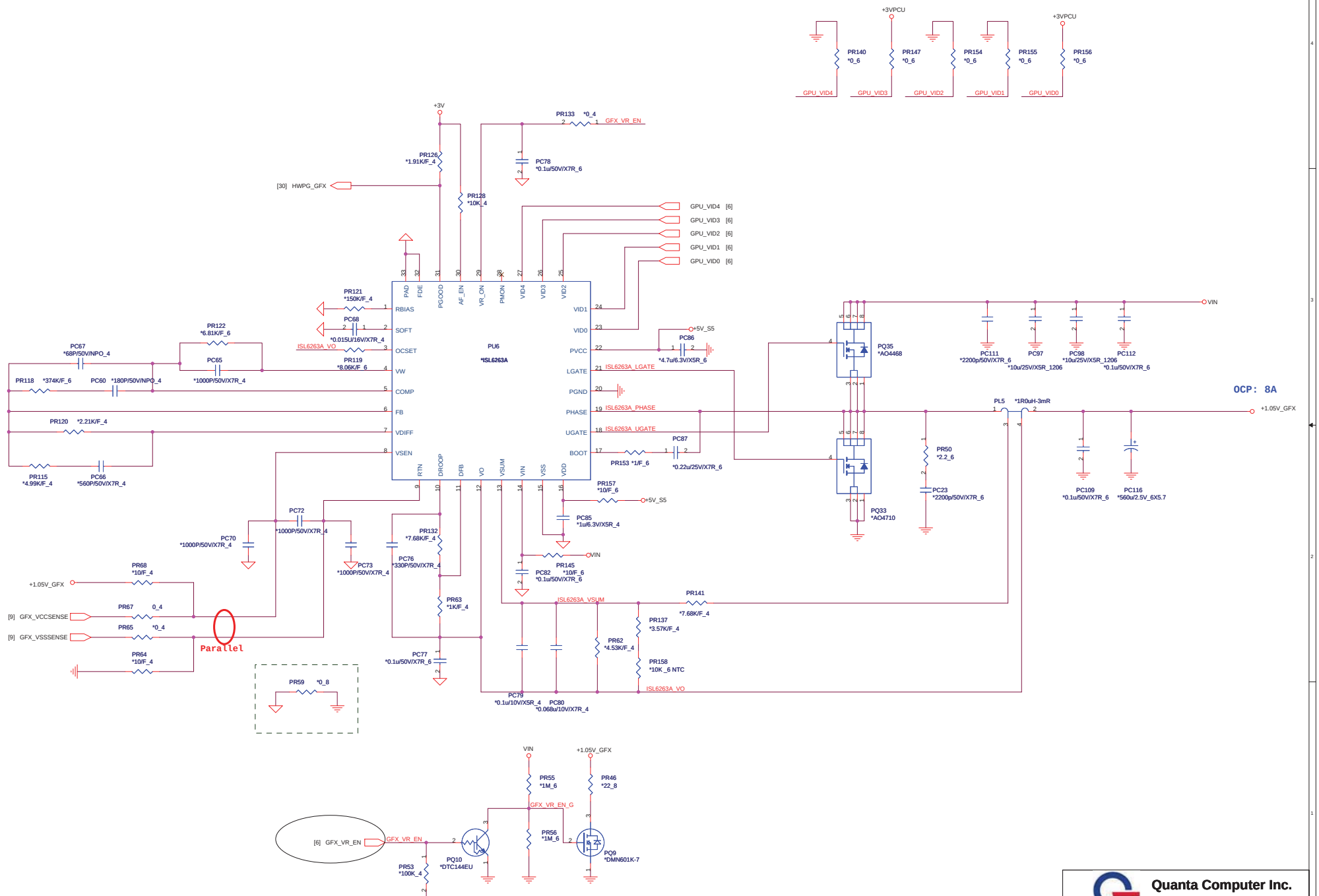


AO1412 Rdson=3.8~4.6mOhm
OCP=12.21+0.5A
L(ripple current)
=(19-1.5)*1./(2.2u*400k*19)
~1.57A

4.6m*12=RILIM*10uA
RILIM=5.62K

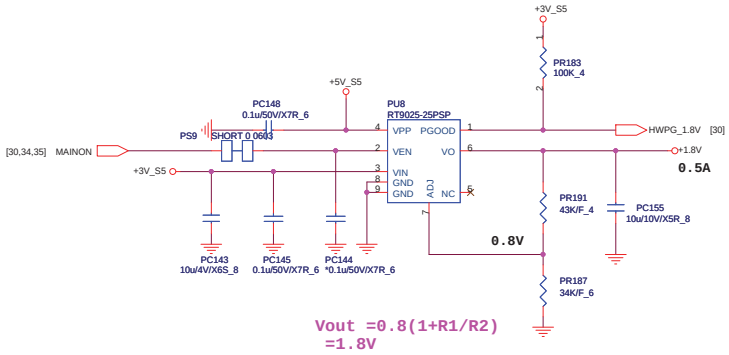
(10u*PR35)/Rdson+Delta_I/2=Iocp

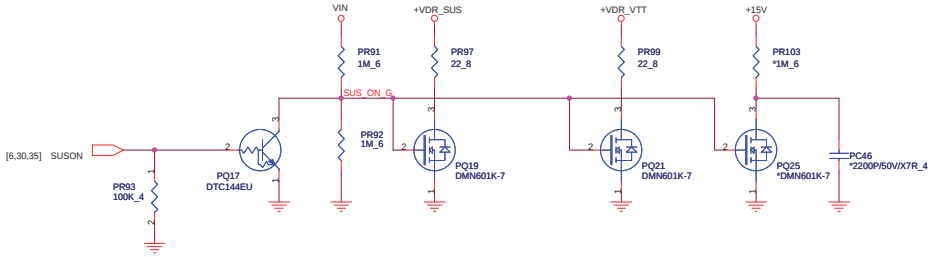
Quanta Computer Inc.
PROJECT : ZY8
Size: C | Document Number: DDR 1.8V(TPS51116) | Rev: 1A
Date: Tuesday, February 17, 2009 | Sheet 35 of 39

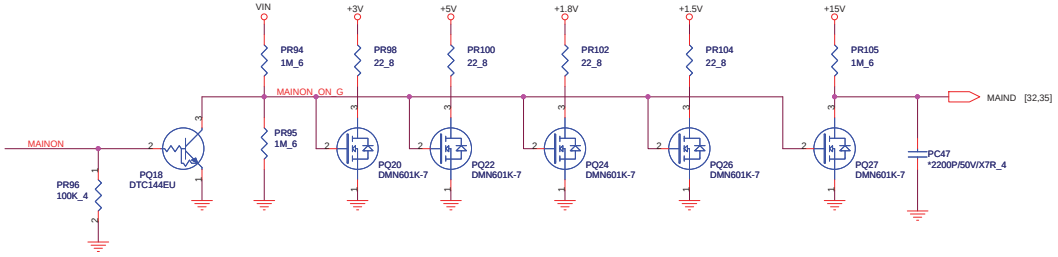


Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	1.05V GFX (ISL6263A)	1A
Date: Tuesday, February 17, 2009	Sheet 36 of 39	







Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	Discharge/1.5V	1A

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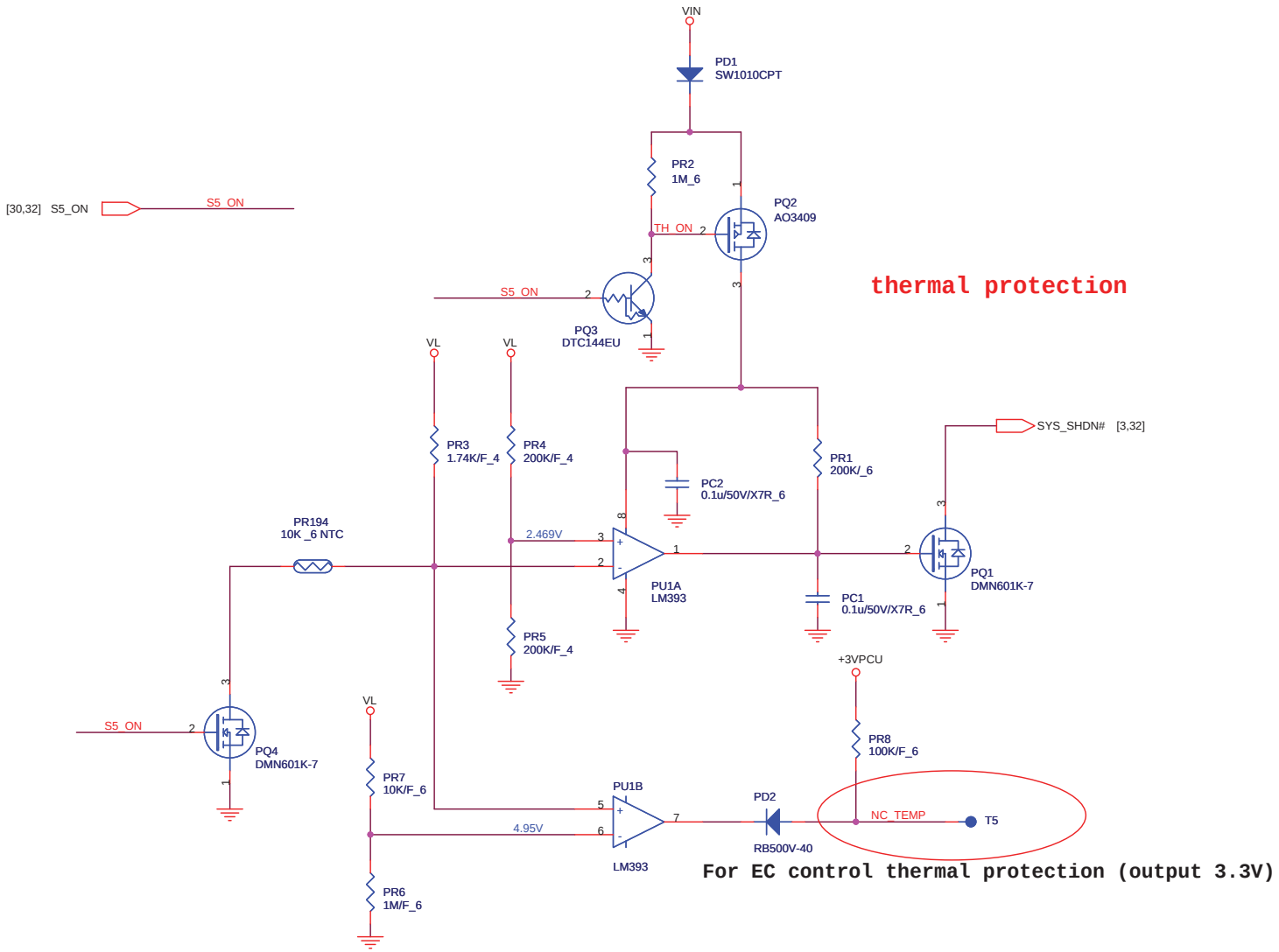

Quanta Computer Inc.		
PROJECT : ZY8		
Size	Document Number: Thermal Protection	Rev: 1A
Date: Tuesday, February 17, 2009	Sheet 38 of 39	

CHANGE LIST

Model	REV	CHANGE LIST
ZY8 MB	1A	FIRST RELEASED: E20080?-???? (PCB: DA0ZY8MB6A0)
	2A	Page10 : Correct LVDS power of NorthBridge to +VDR_SUS Page12 : Change 32.768KHz (Y2) to normal type(H3.5) Change RTC battery connector type (CN34) to DFHD02MR311 Swap SATA port between port-1 (ODD) and port-4 (2ND HDD) Page3 :Remove Q32, Q33, R288,R287,R111 and R110 for Thermal monitor Page6 :Change PU power +3VSUS to +3V Add HDA function for ZY9 Page7 :Add HSYNC/VSYNC to GND for ZY9 MXM Page12 :Add HDA function for ZY9 Page17 :Add iHMDI function for ZY9 Change U33 power and Input Change U36 power Page19 :Add HDMI Level Shift for ZY9 Add Cap. for DP signal Change HDMI Conn footprint Page20 :Change transformer and RJ45 footprint Page21 :Change Conn pcs to Two pcs Page23 :Co-layout ALC888 for ZY9 Page25 :Change New Card Conn footprint Page26 :Change CardReader to OZ888GS0LN Page27 :Change Power Board Conn to 6 pin Change CN1 and CN13 pin define Combine LCD BL ON/OFF and Logo LED conn. to CN39 Page28 :Change USB CN32 pin define Change CN15 to 12pin Page29 :Add ESD protect for FP change PQ37 from BAM14140001 to BAM14120000 change PQ35, PQ30,PQ49 from BAM44960000 to BAM44680003 change PC131,PC93 from CH22206KB16 to CH21506K915 changePR184 from CS26193F929 to CH22743F901 PR179,PR165 mount PC112,PC109,PC120,PC101,PC147,PC156,PC91,PC29,PC35,PC135,PC160,PC159,PC141 un-mount change PU9 from AL0006111002 to AL008202001 change PU7 from AL006237000 to AL008206000 change PU3 from AL051116008 to AL008207000
	3A	
	3C	

MODEL	ZY8	
	FROM	To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
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	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B

DOC NO.	PROJECT MODEL :	ZY8	APPROVED BY:		DATE:	2008/06/27
	PART NUMBER:		DRAWING BY:		REVISON:	1A