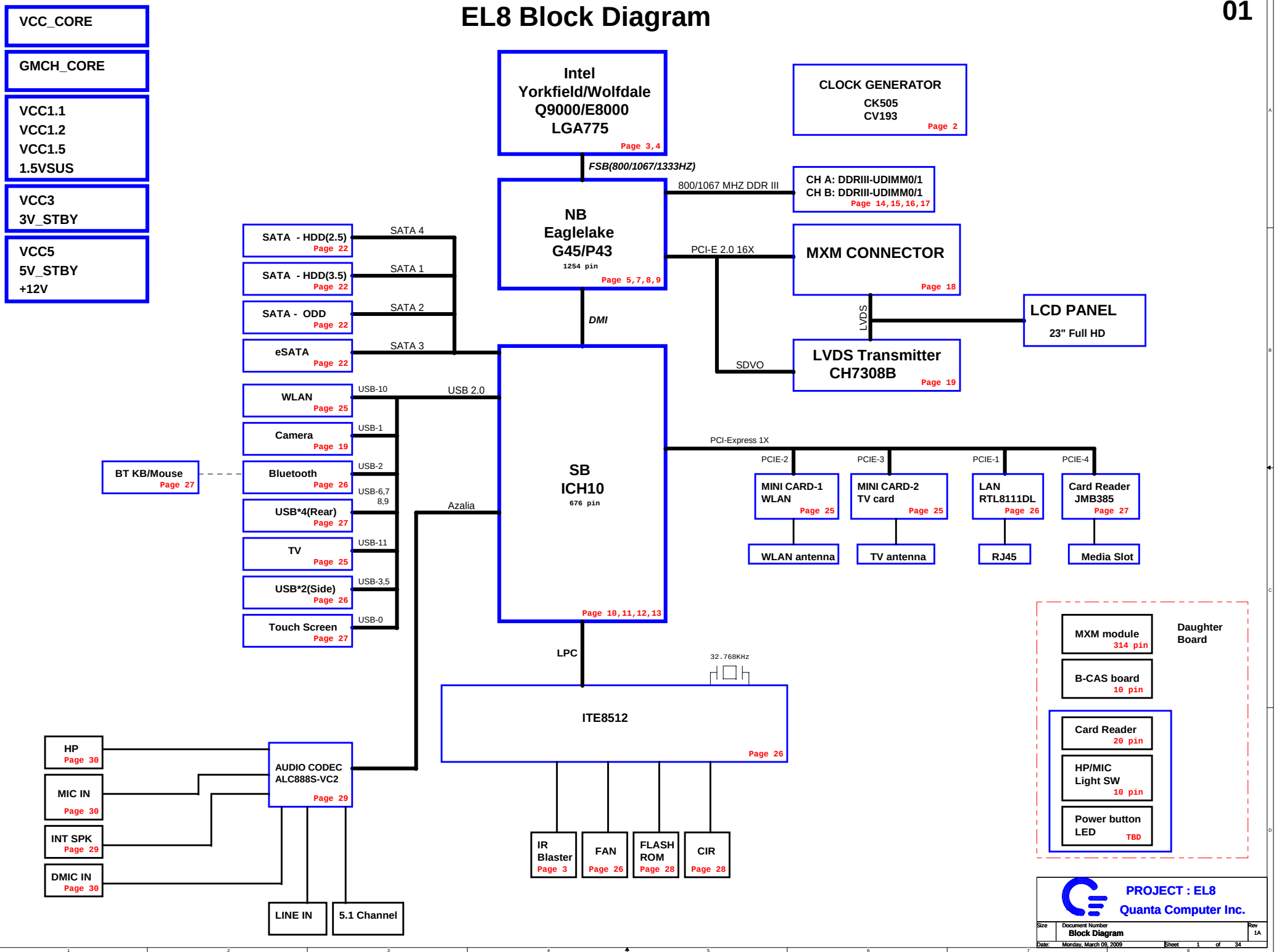
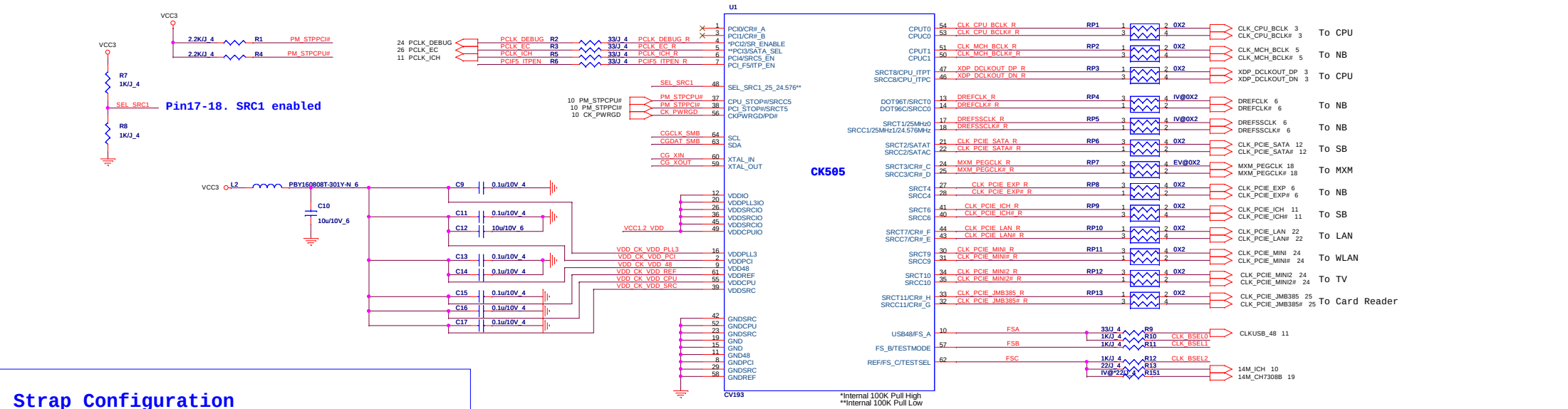


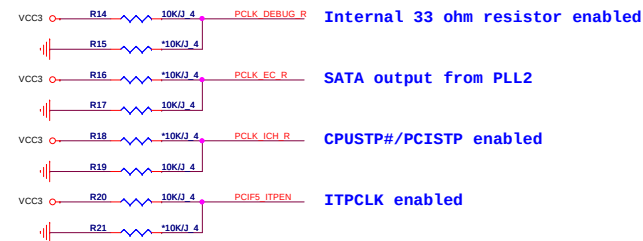
EL8 Block Diagram

01





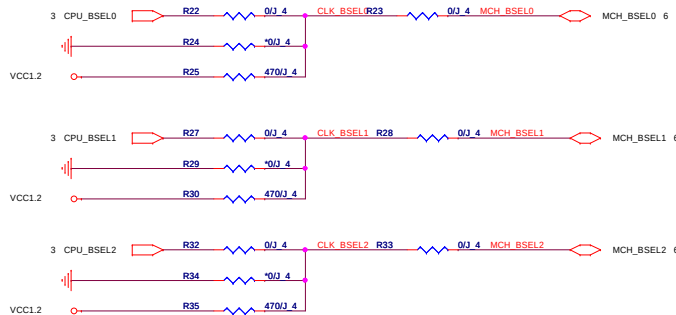
Strap Configuration



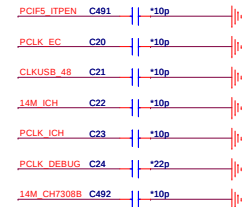
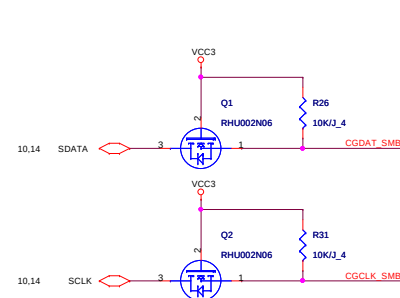
FREQ. SEL TABLE

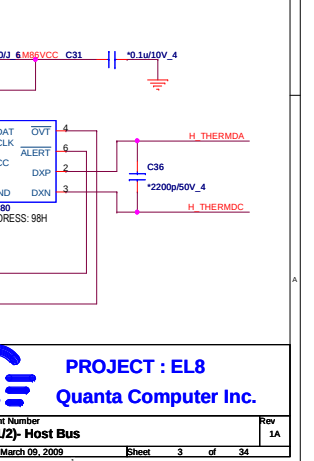
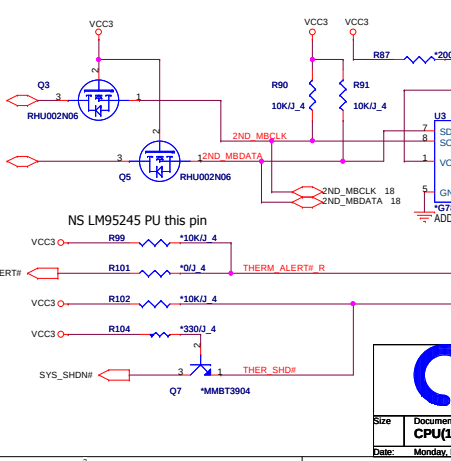
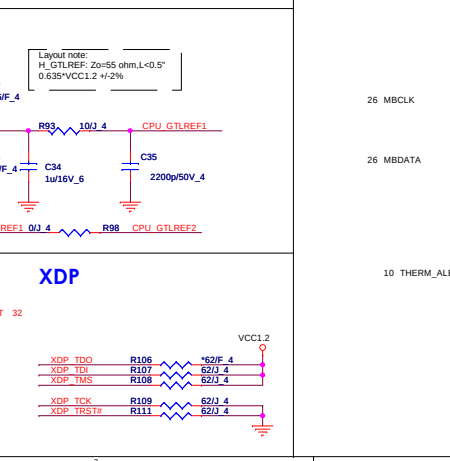
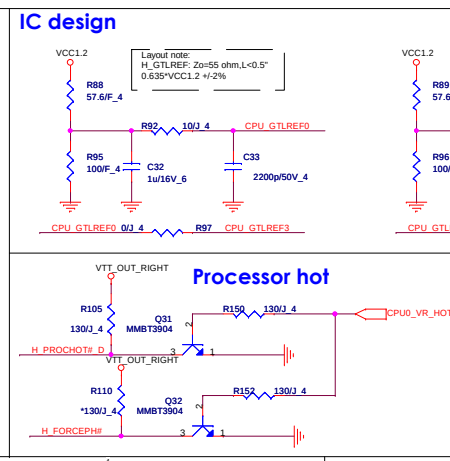
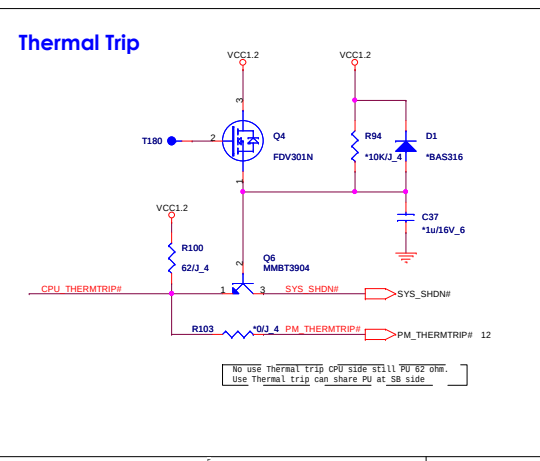
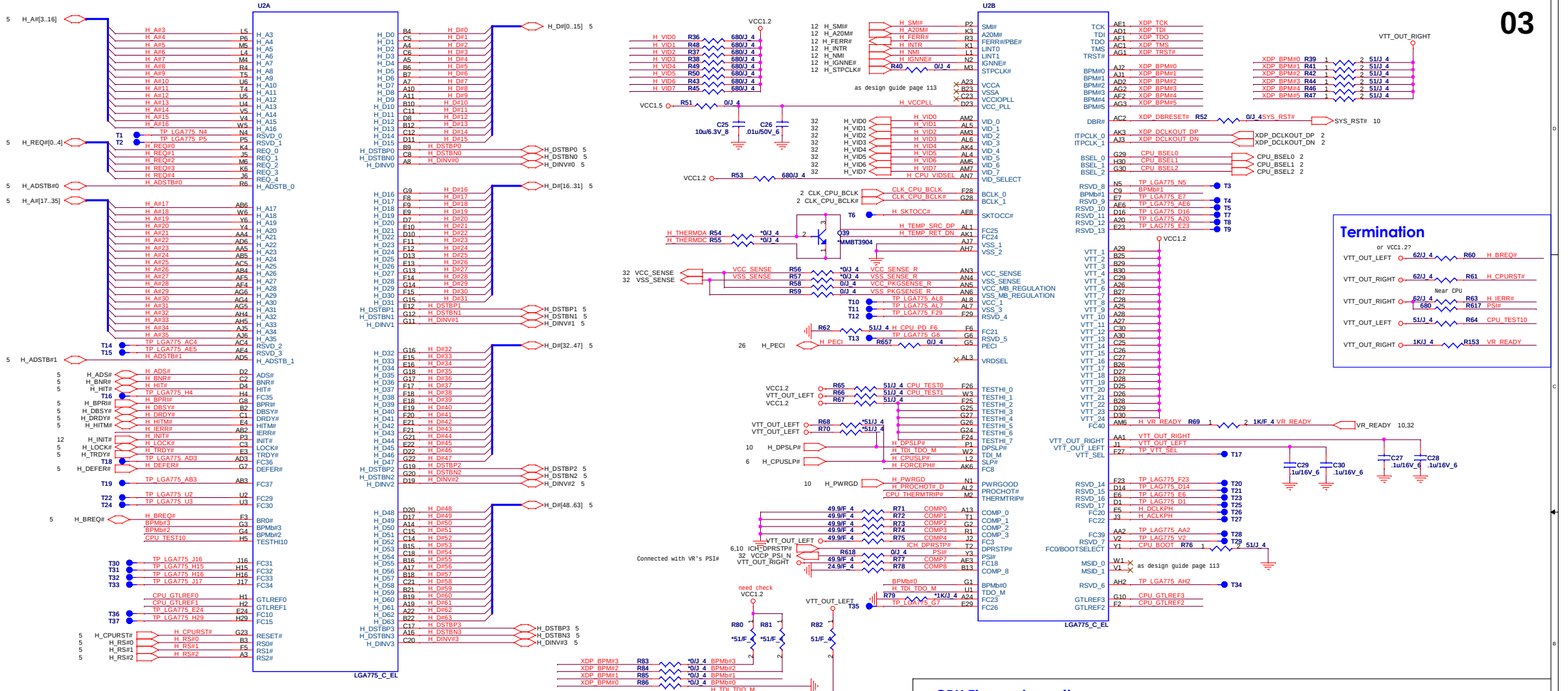
BSEL Frequency Select Table

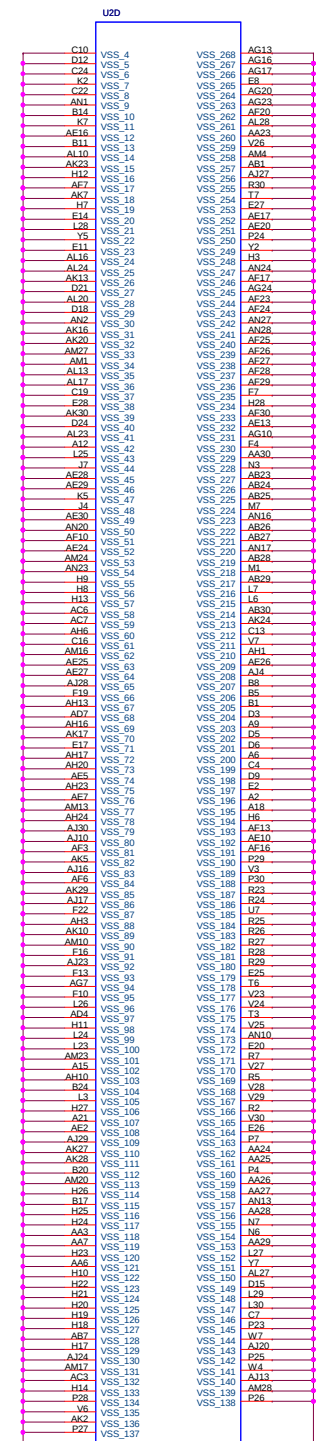
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	0	0	333Mhz
1	0	1	100Mhz
1	1	0	400Mhz
1	1	1	Reserved



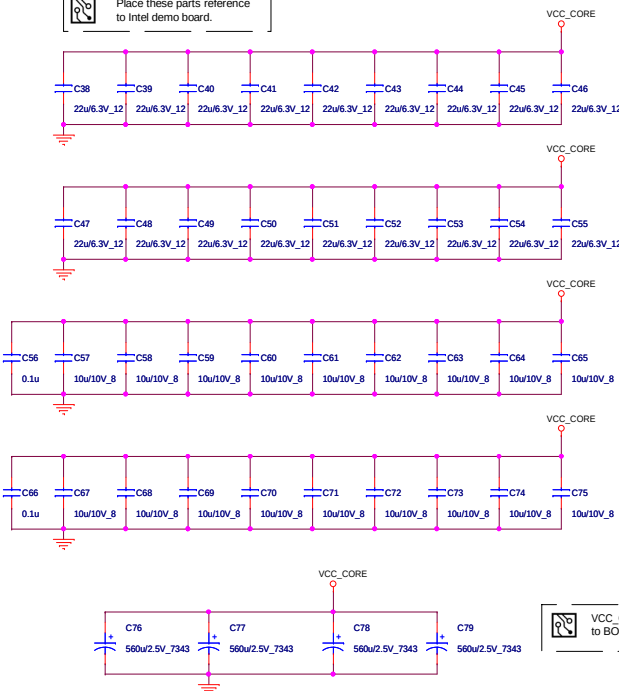
Clock Gen I2C







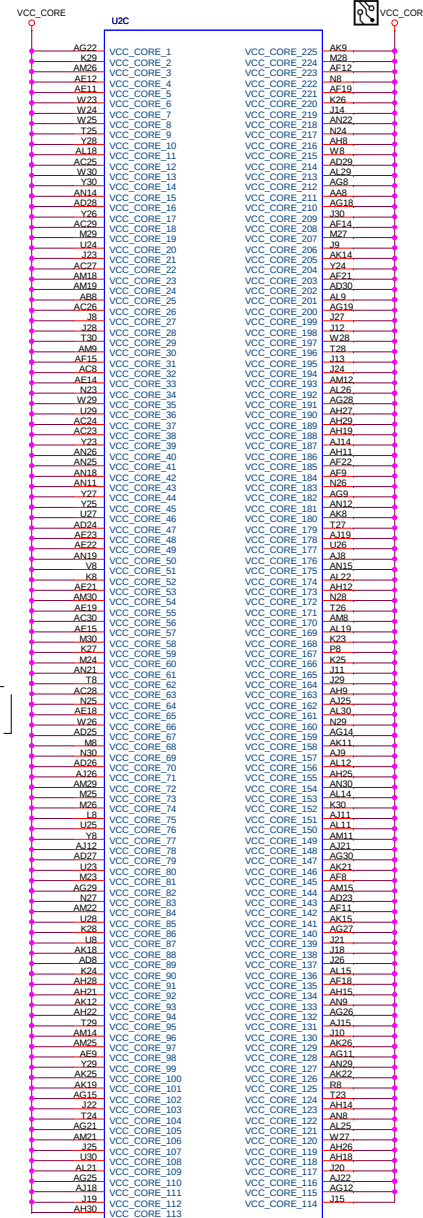
Place these parts reference to intel demo board.



VCC_CORE Bulk CAP's place to BOT of CPU central

Yorkfield/Wolfdale CPU Power Status and max current table

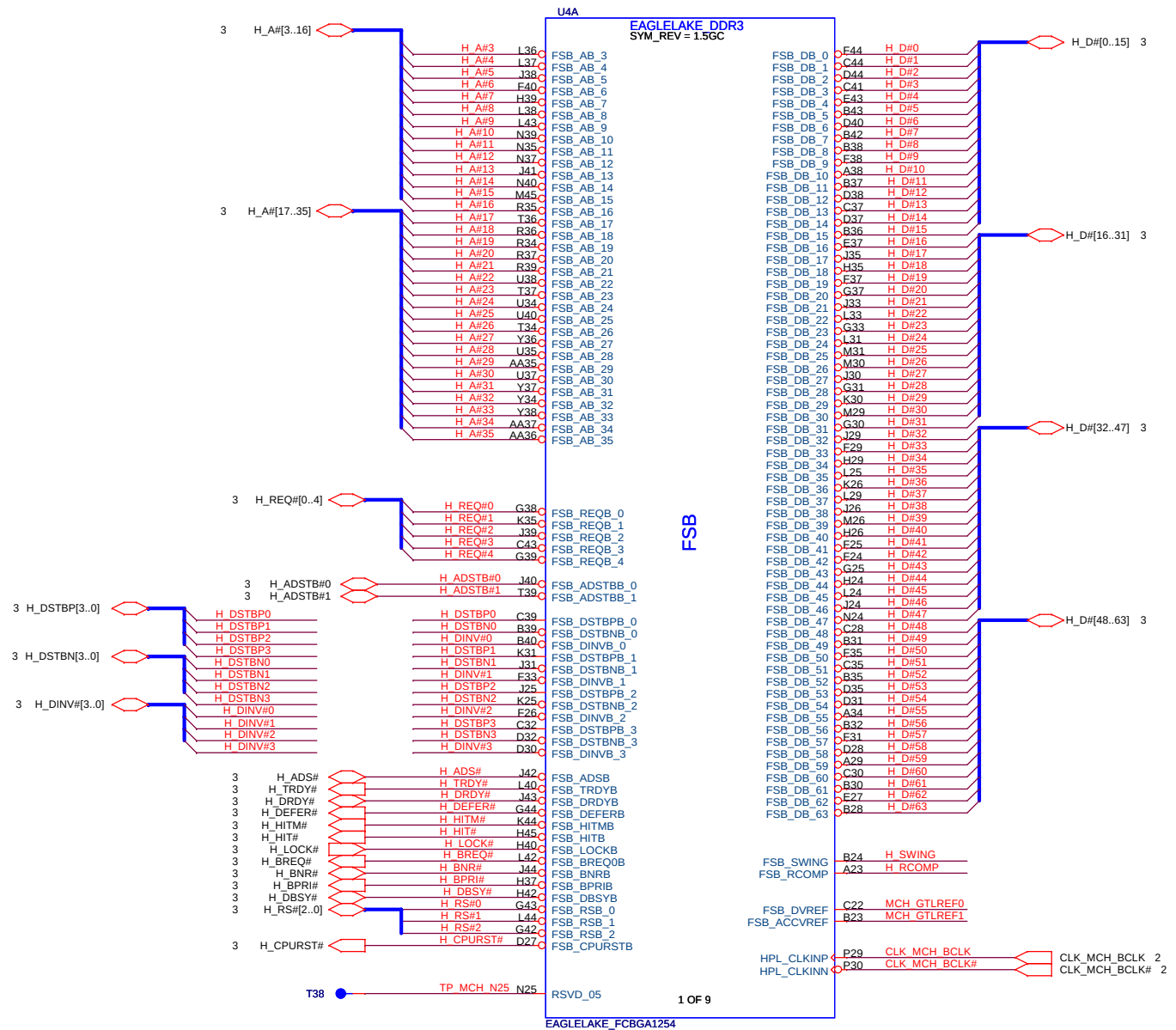
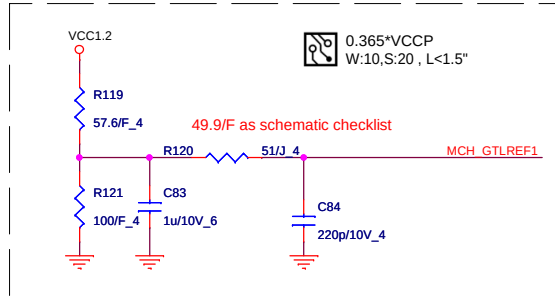
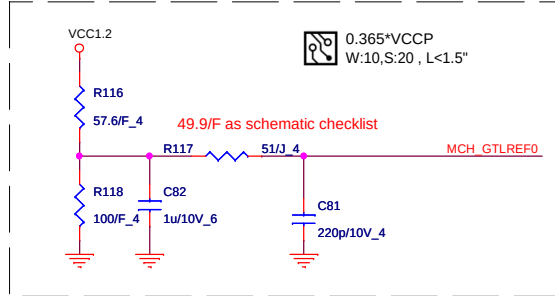
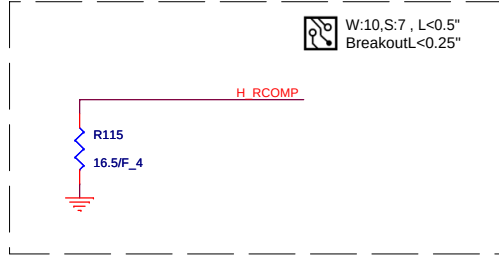
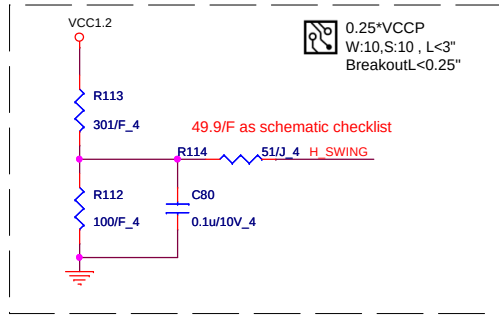
POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	100A	Yorkfield@65W
VCC_CORE	O	X	X	VID	75A	Wolfdale
VTT	O	X	X	VCC1.2	8A	After VCC stable
VTT	O	X	X	VCC1.2	7A	Before VCC stable
VCC_PLL	O	X	X	VCC1.5	260mA	

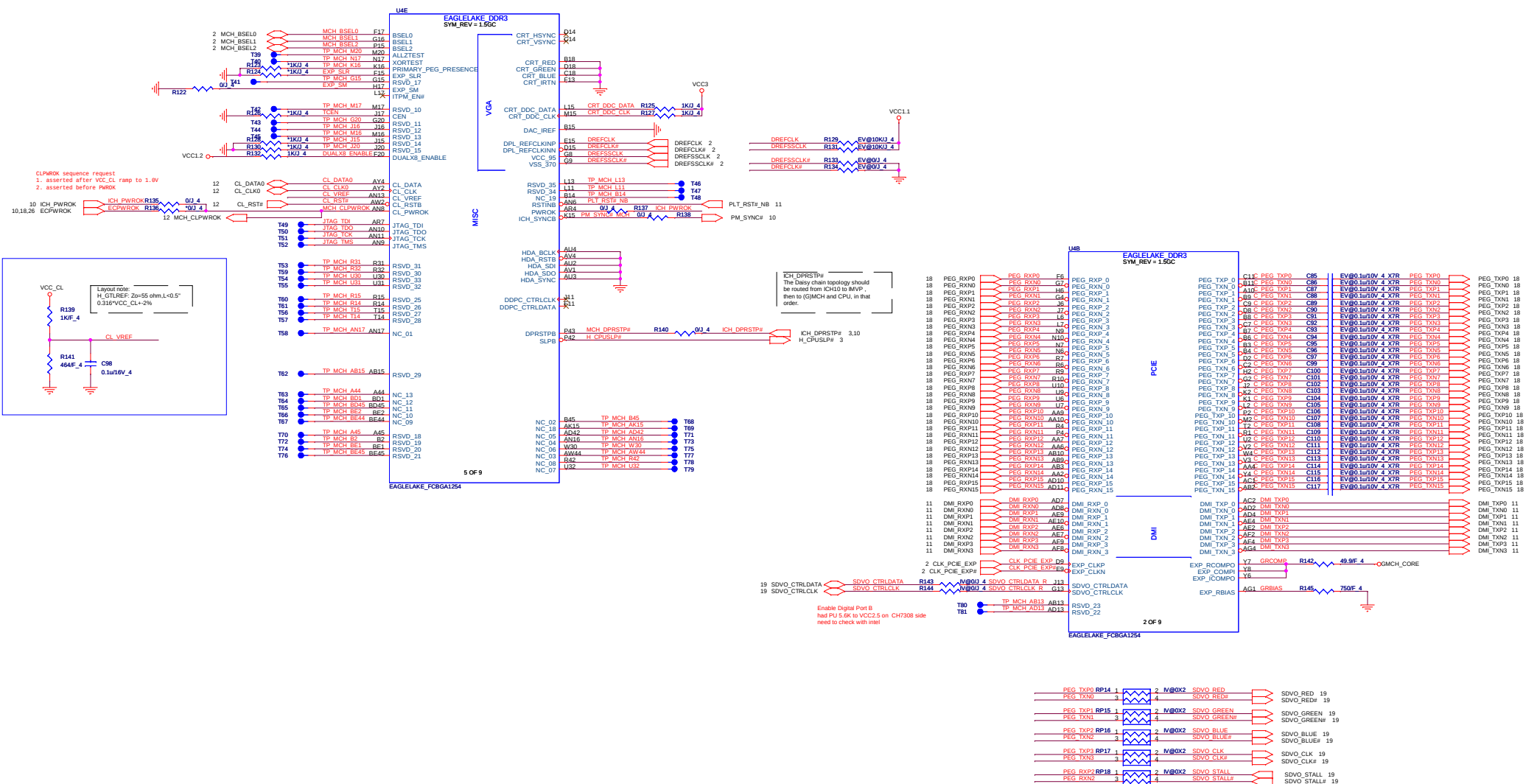


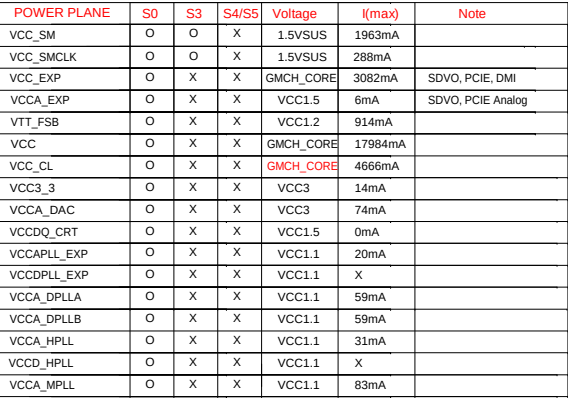
LGA775_C_EL

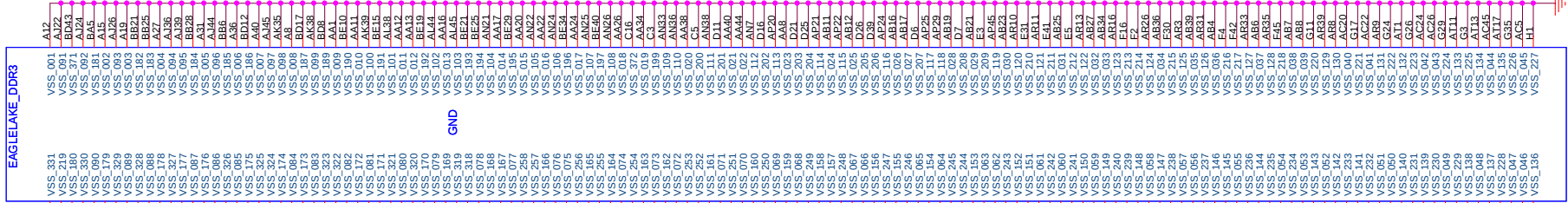


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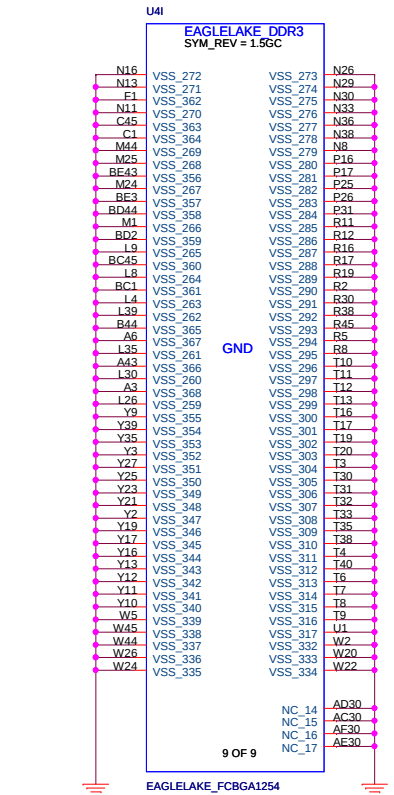








U4H
EAGLELAKE_FCBGA1254
SYM_REF = 1.5GC
8 OF 9

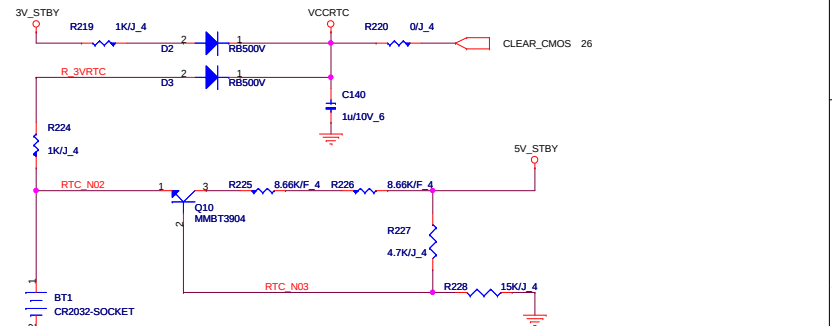
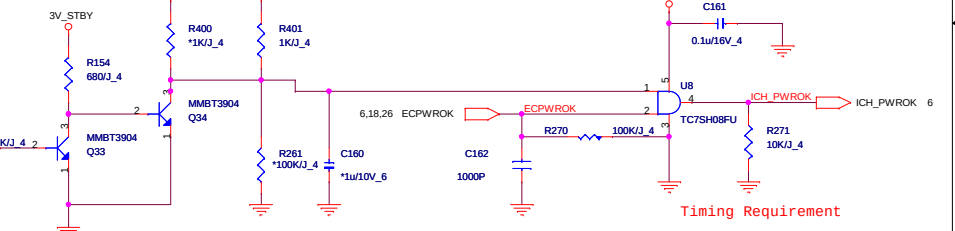




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Size	Document Number	Rev
	NB (5/5)- VSS	1A
Date:	Monday, March 09, 2009	Sheet 9 of 34

Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect			This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU			
TP3	XOR Chain Entrance	PWROK	ICH_TP3	HDA_SDOUT	Description	
			0	0	RSVD	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	0	1	Enter XOR Chain	
			1	0	Normal operation(Default)	
			1	1	Set PCIE port config bit 1	



 PROJECT : EL8 Quanta Computer Inc.		
Size	Document Number	Rev
	SB (1/4)- HOST	1A
Date:	Monday, March 09, 2009	Sheet 10 of 34

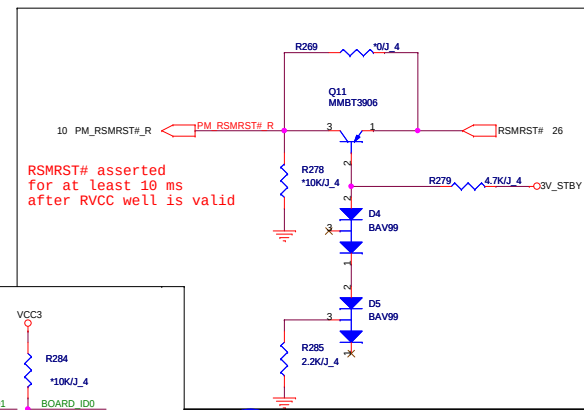
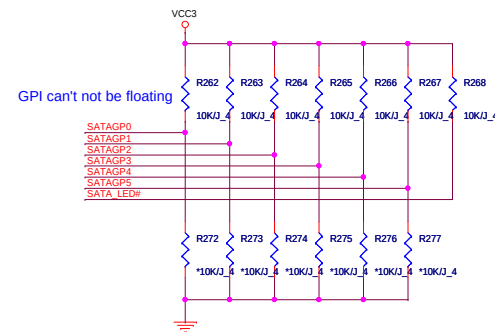
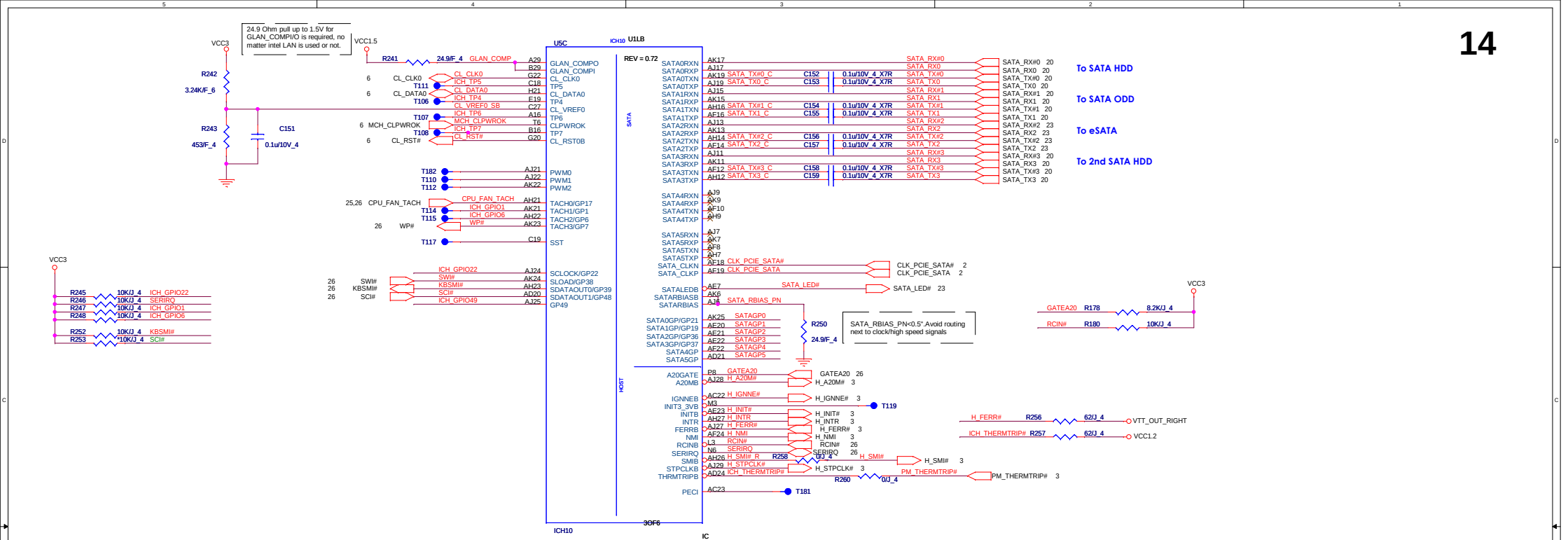
1

1

1

1

1



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode 10,21	SPKR SPKR R286 *1K/J_4 -> OVCC3
GPIO49	DMI Termination Voltage	PWROK	0 = AC coupled 1 = DC coupled Internal PU	ICH_GPIO49 R292 *1K/J_4

Board ID Table

BOARD_ID3 of TE1M always keep low, TE1 hasn't support TV

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ G-SENSOR W/O G-SENSOR			H L		
W/ TV W/O TV		H L			
W/ HDMI W/O HDMI	H L				

PROJECT : EL8

Quanta Computer Inc.

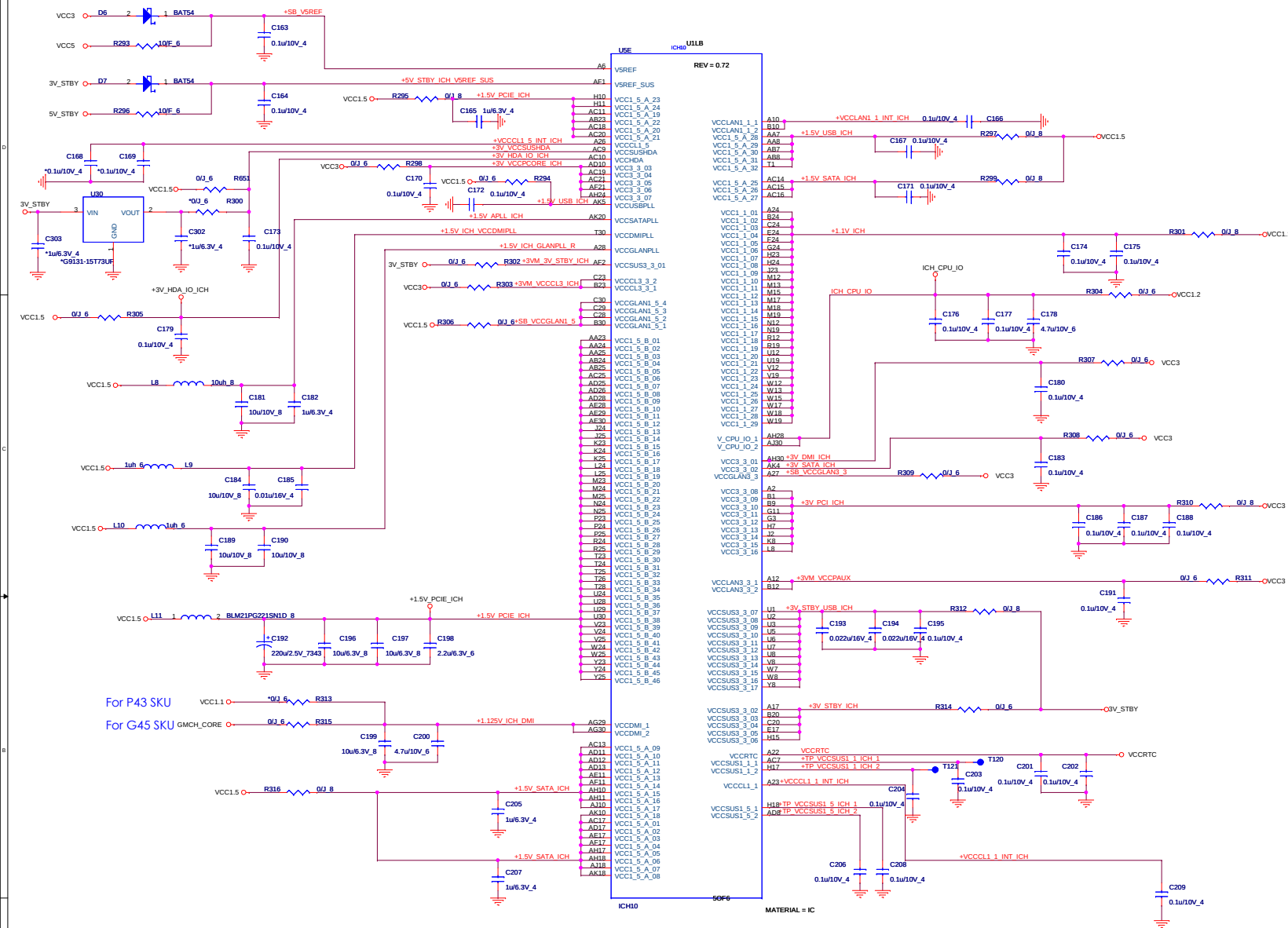
Size: Document Number

SB(3/4) SATA/GPIO

Rev: 1A

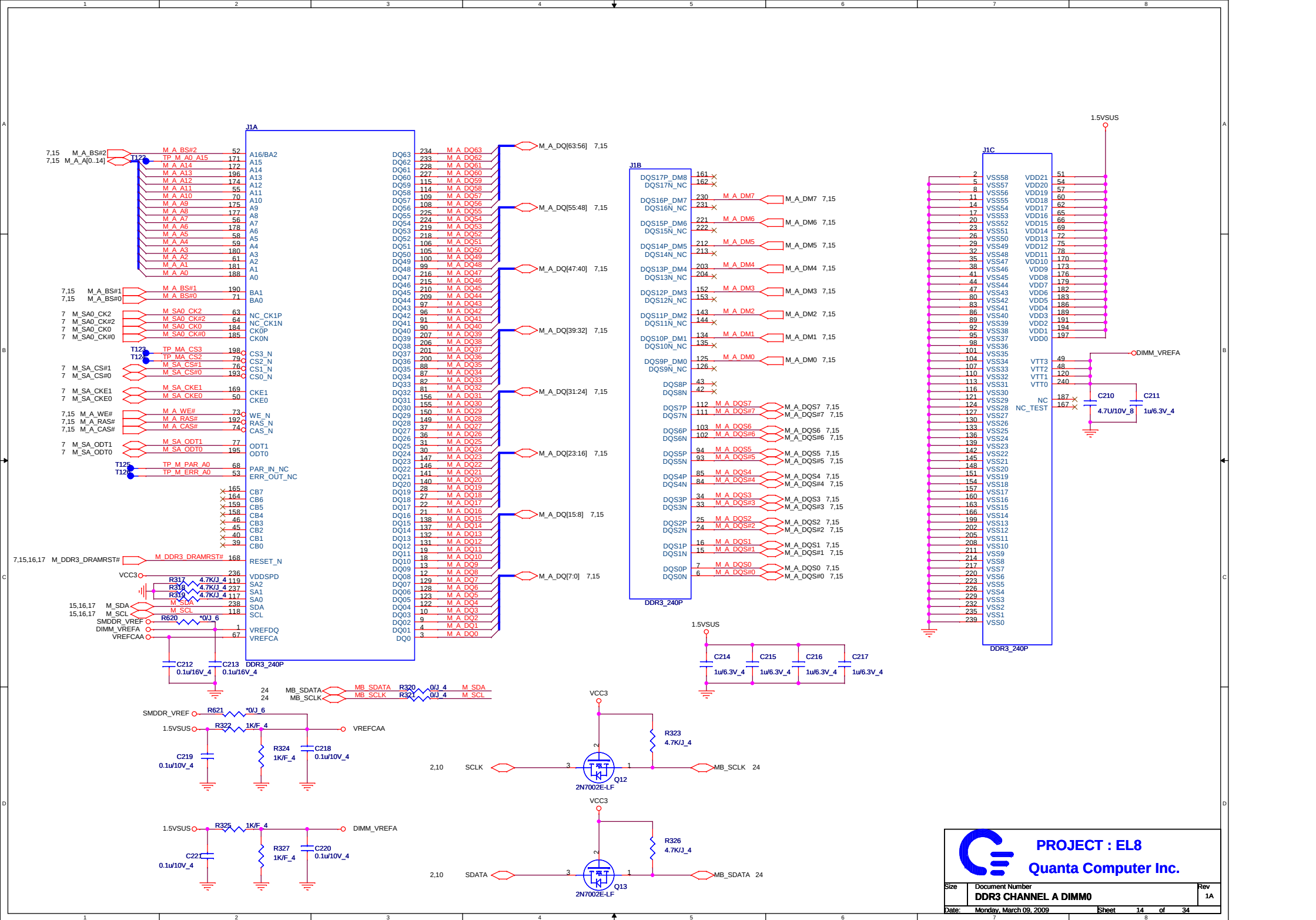
Date: Monday, March 09, 2009

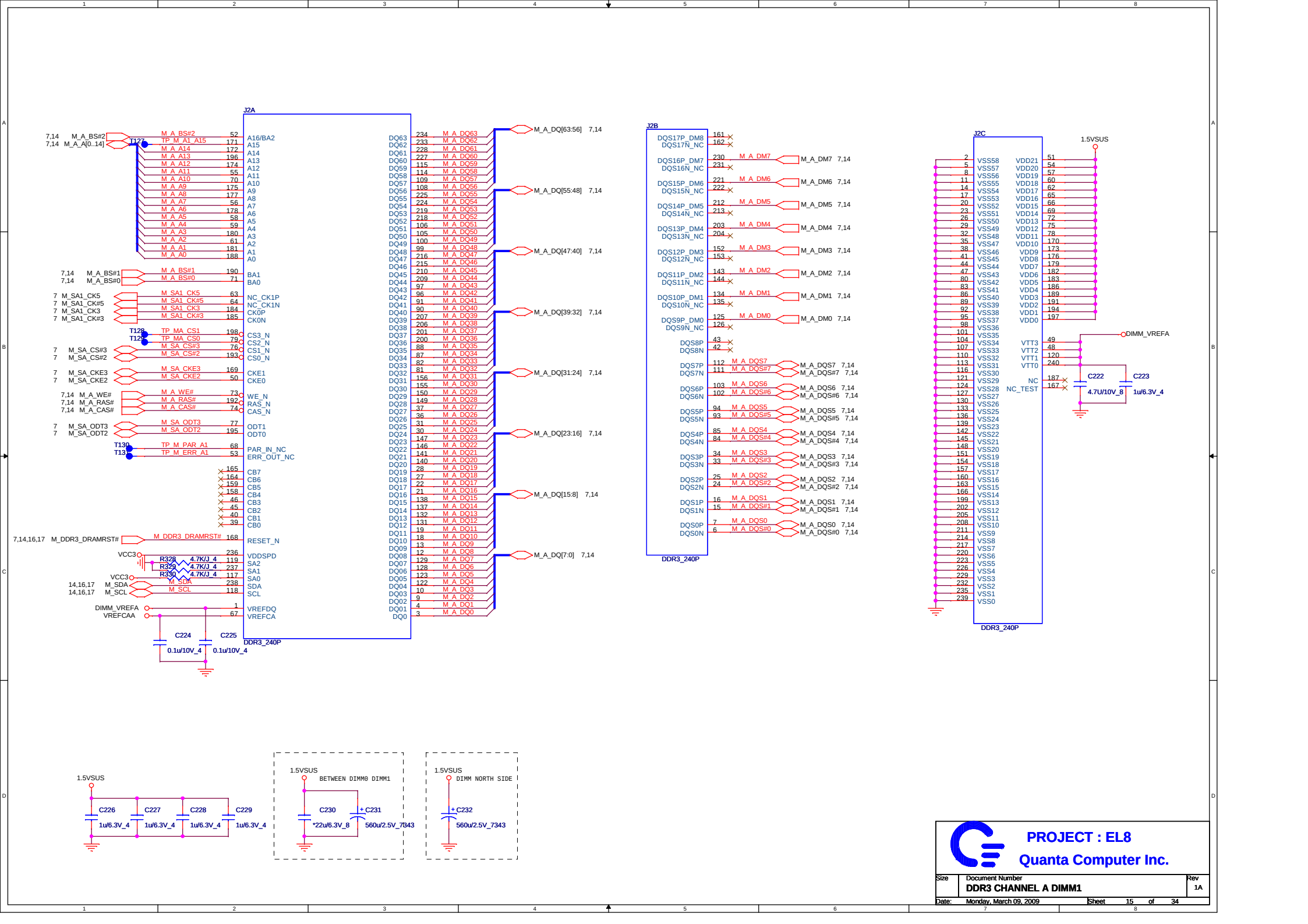
Sheet: 12 of 34

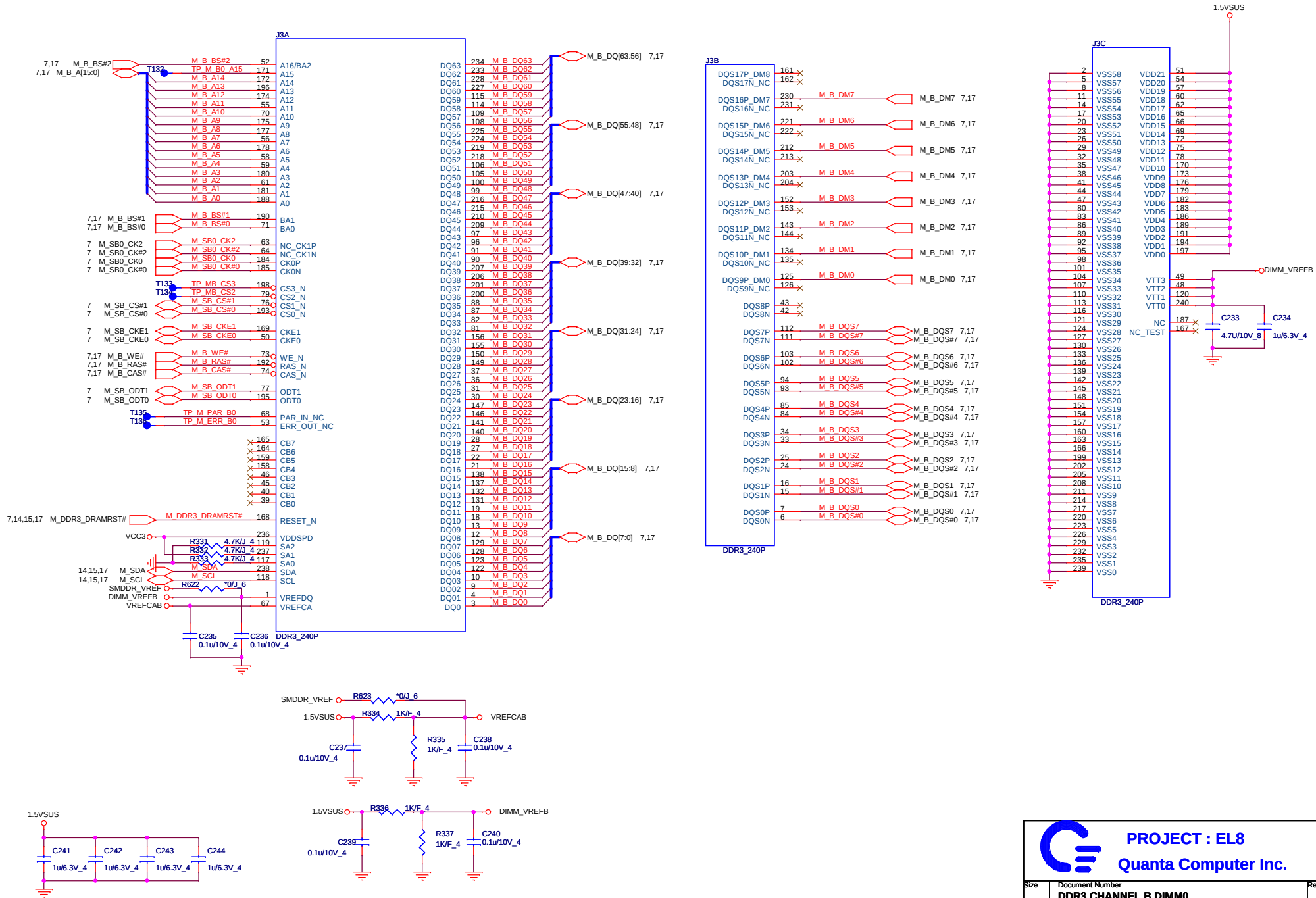


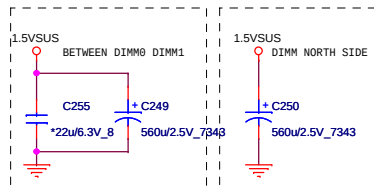
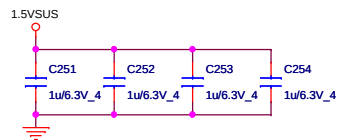
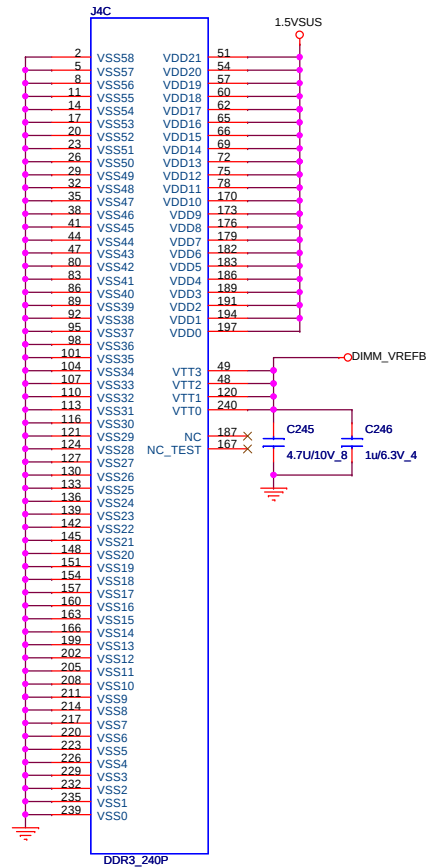
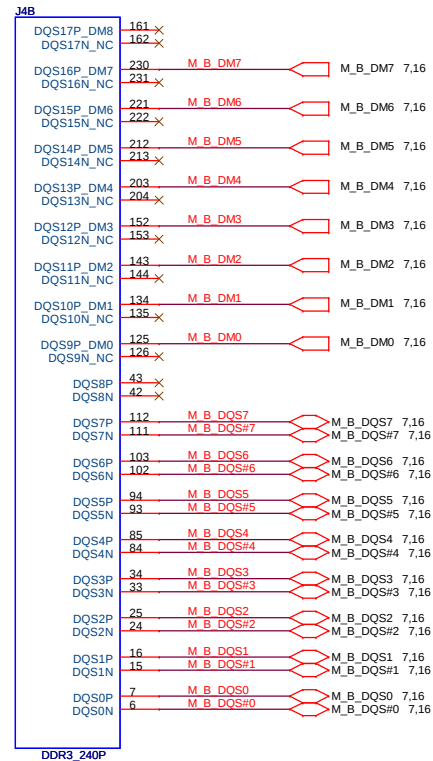
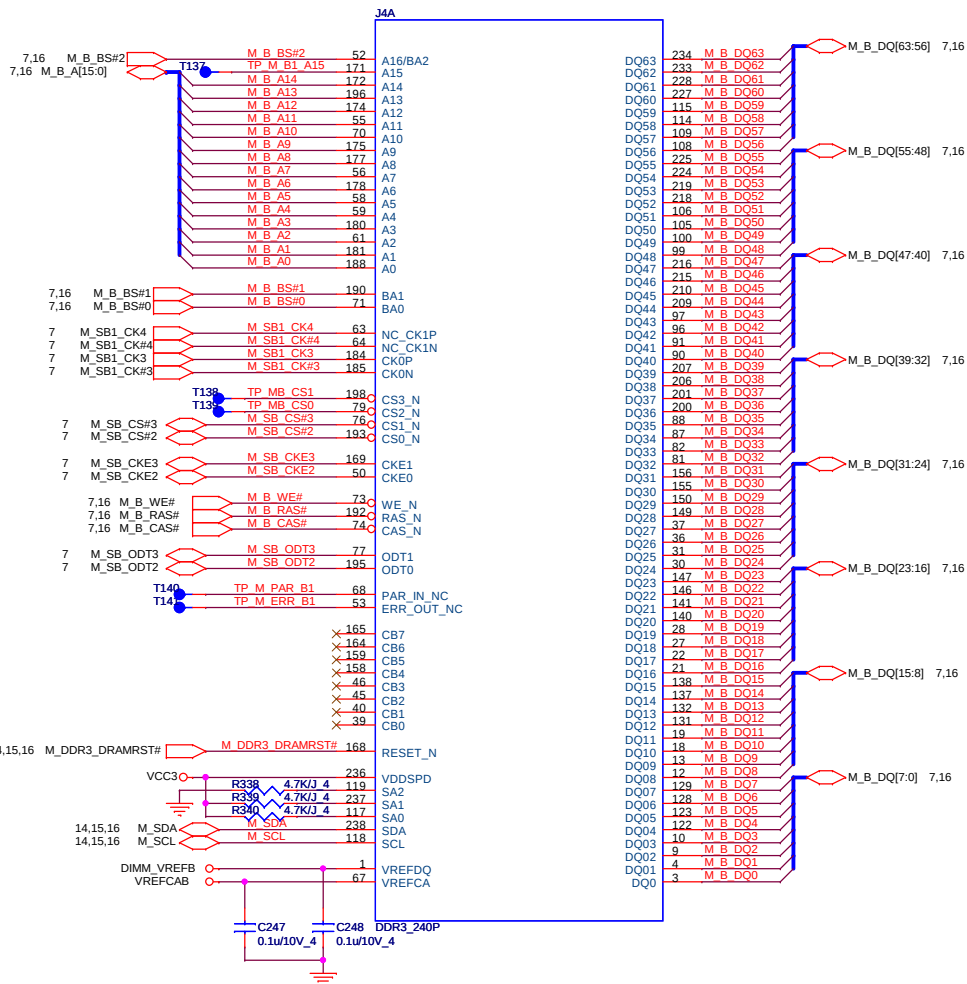
SB Power Status and max current table(2/2)

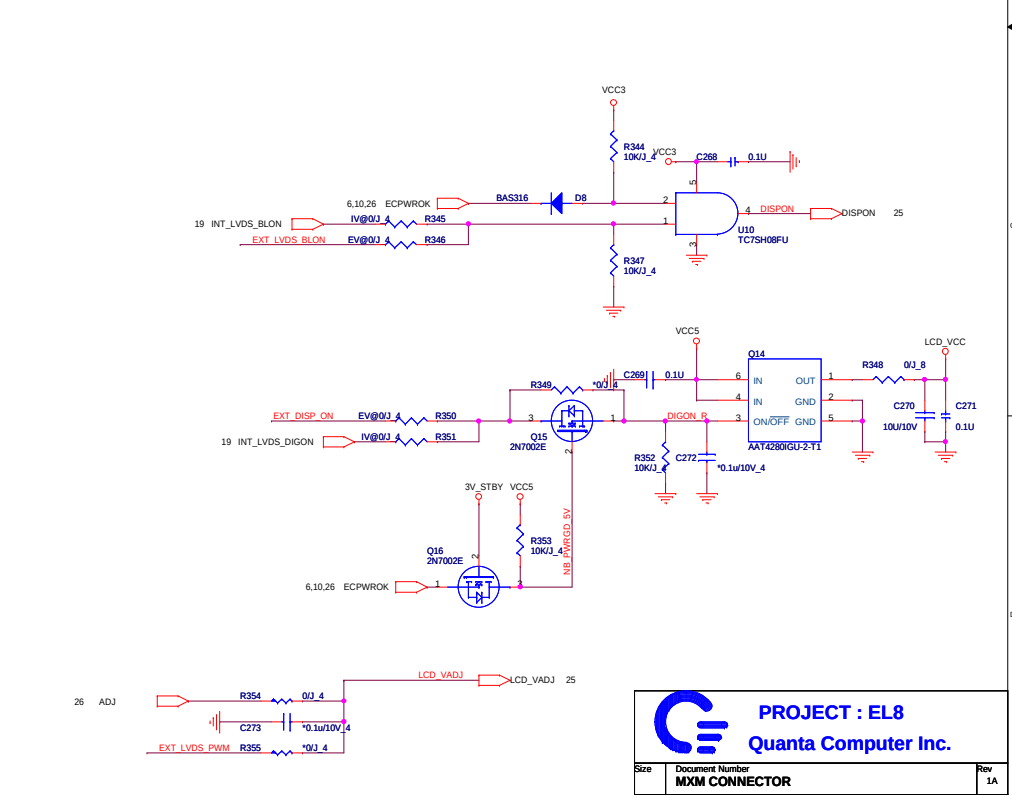
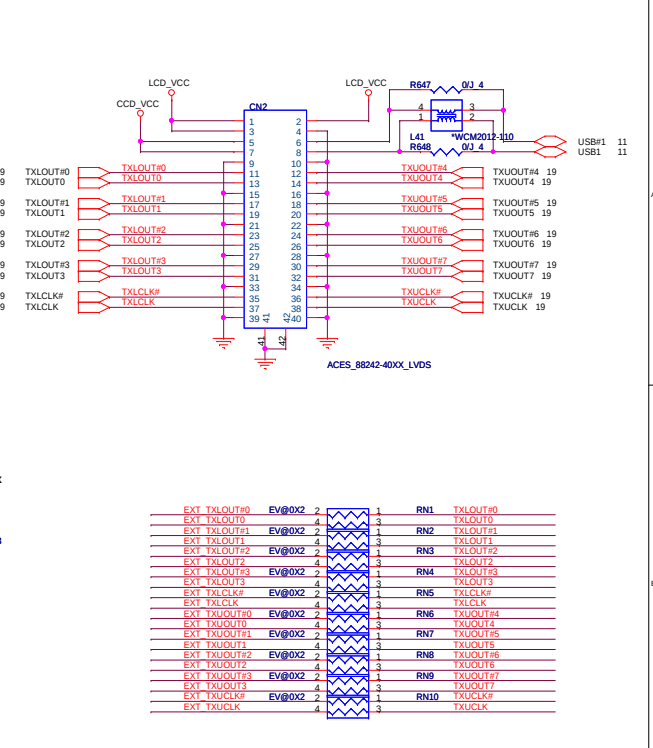
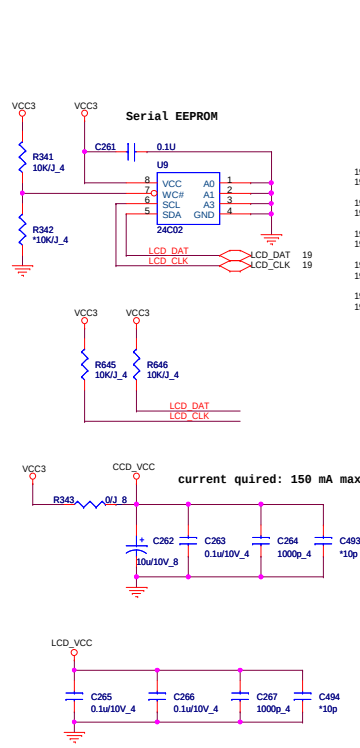
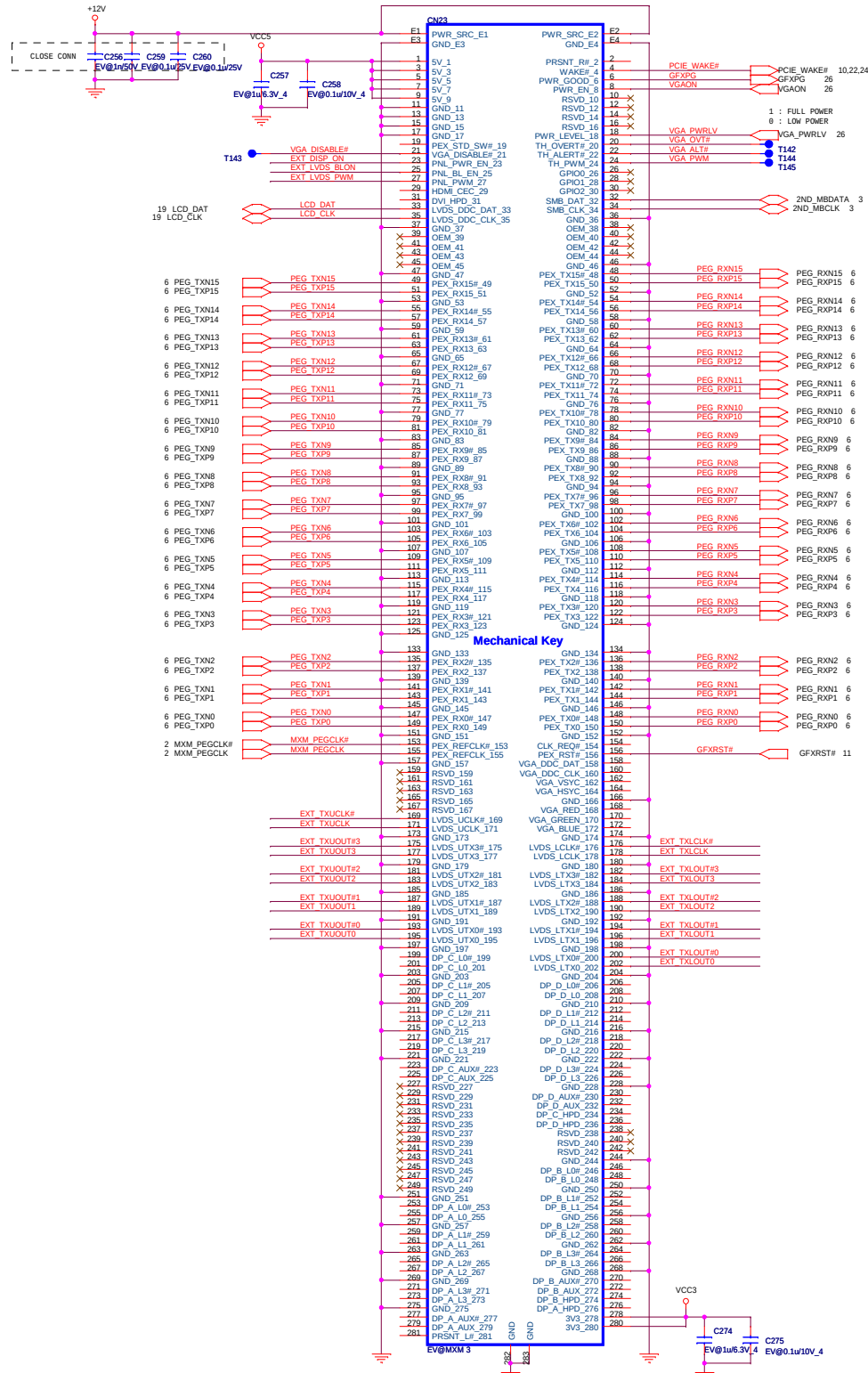
POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_1	O	X	X	VCC1.1	1.634A	ICH CORE
VCCDMPPLL	O	X	X	VCC1.5	23mA	
VCC_DMI	O	X	X	GMCH_CORE	50mA	1.125V@G45, 1.1V@P43
V_CPU_IO	O	X	X	VCC1.2	2mA	
VCC3_3	O	X	X	VCC3	308mA	
VCCCHDA	O	X	X	VCC1.5	70mA	
VCCSUSHDA	O	O	O	RVCC1.5	70mA	
VCCSUS1_1	X	X	X	1.1V	X	Internal VR powered
VCCSUS1_5	X	X	X	1.5V	X	Internal VR powered
VCCSUS3_3	O	O	O	3V_STBY	212mA	53mA@S3/S5
VCCCL1_1	X	X	X	1.1V	X	Internal VR powered
VCCCL1_5	X	X	X	1.5V	X	Internal VR powered
VCCCL3_3	O	X	X	VCC3	73mA	S3/S5 powered when AMT activated

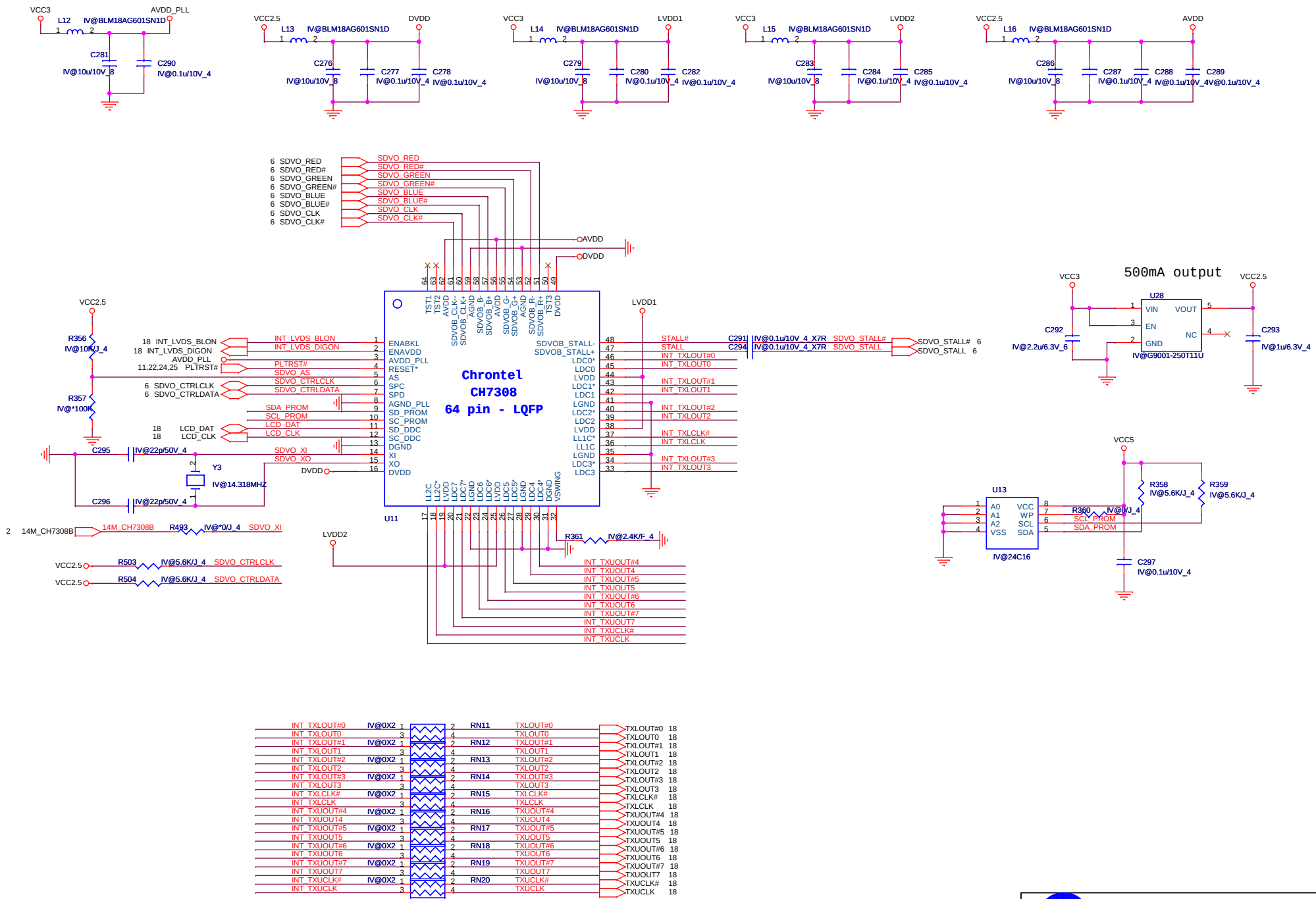


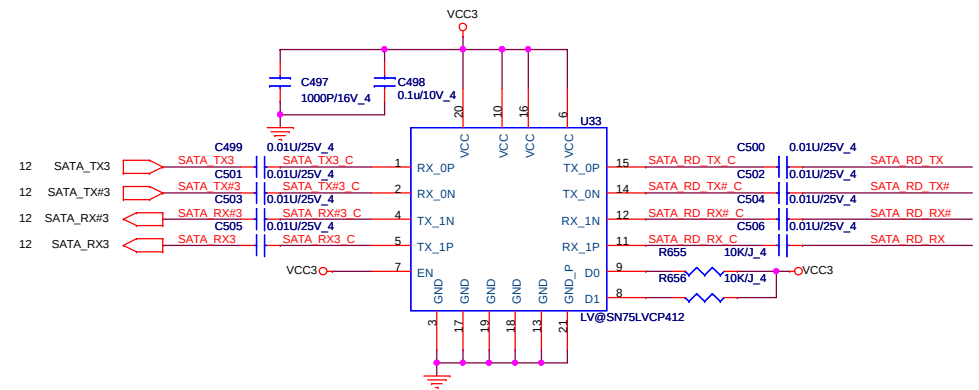
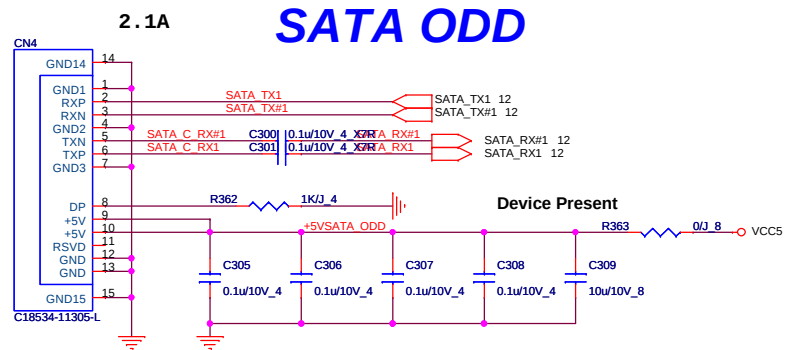




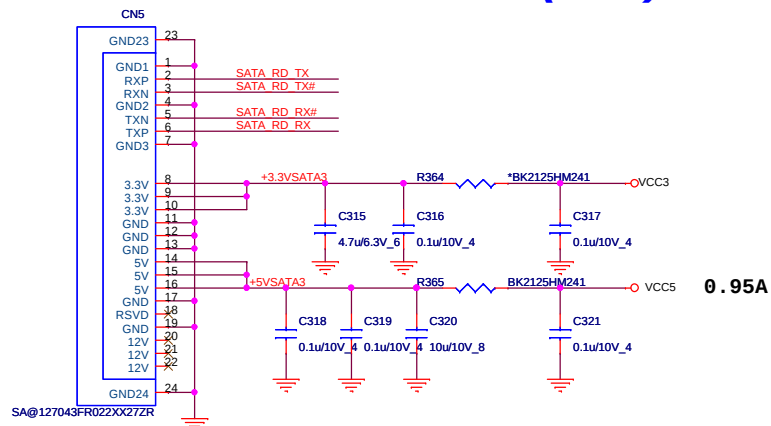




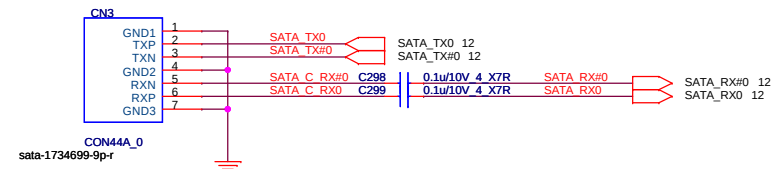




2nd SATA HDD(2.5")

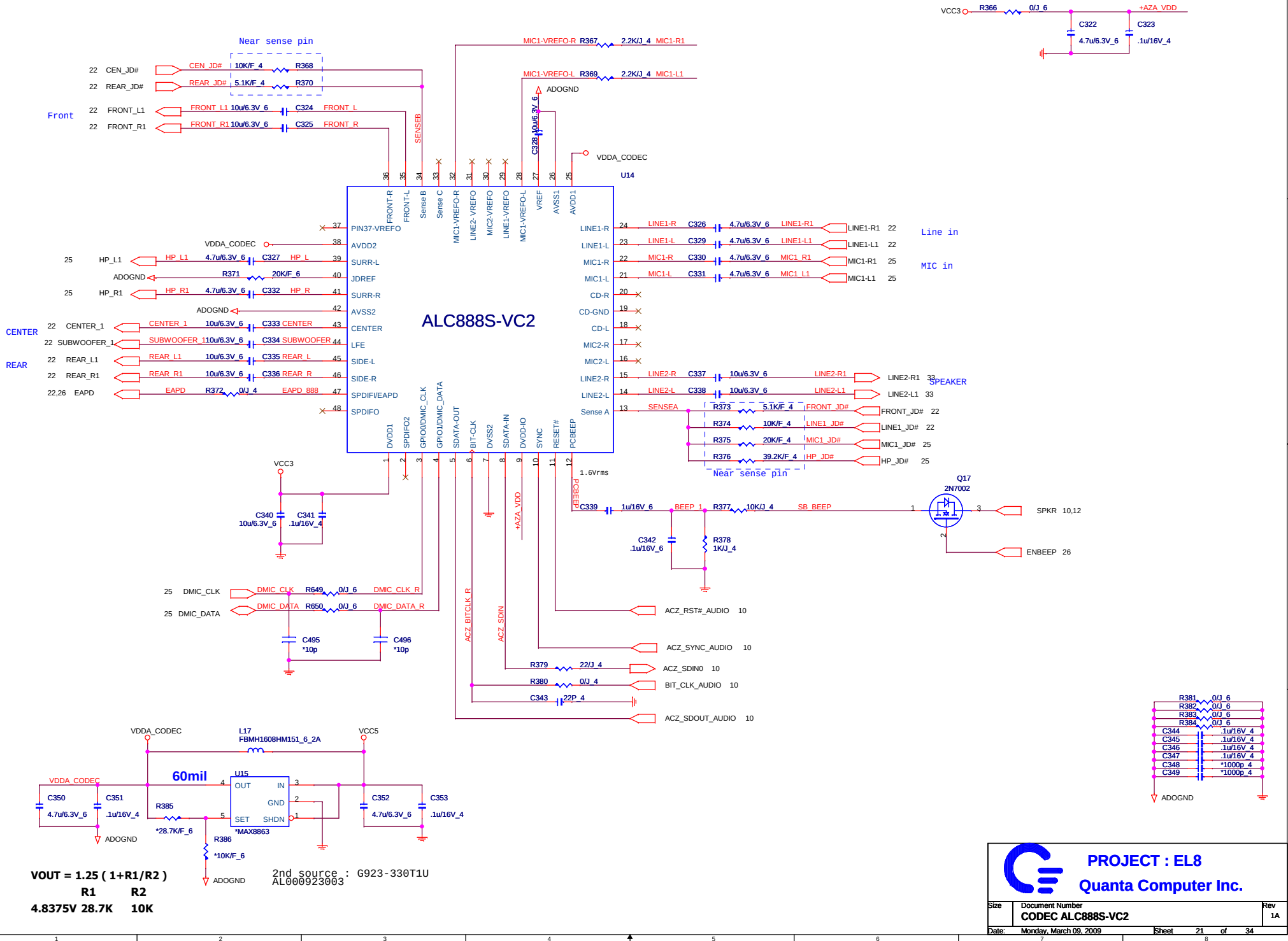


SATA HDD(3.5")



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CODEC



11 USB#6 USB#6



The diagram shows a transmission line between two connectors, CN10 and CN11. CN10 is a 4-pin connector with pins 2 (GND), 1 (SIG), and 3 (GND). CN11 is a 4-pin connector with pins 1 (SIG) and 2 (GND). A red line represents the signal path, labeled with $Z = 75\text{ OHM}$ and ANT. The signal path is connected to a resistor R430 (100 Ohms) and a capacitor C43 (0.01 uF) in parallel, which is then connected to the ANT_GND plane. The text 'Vertical' is written next to the connector CN11.

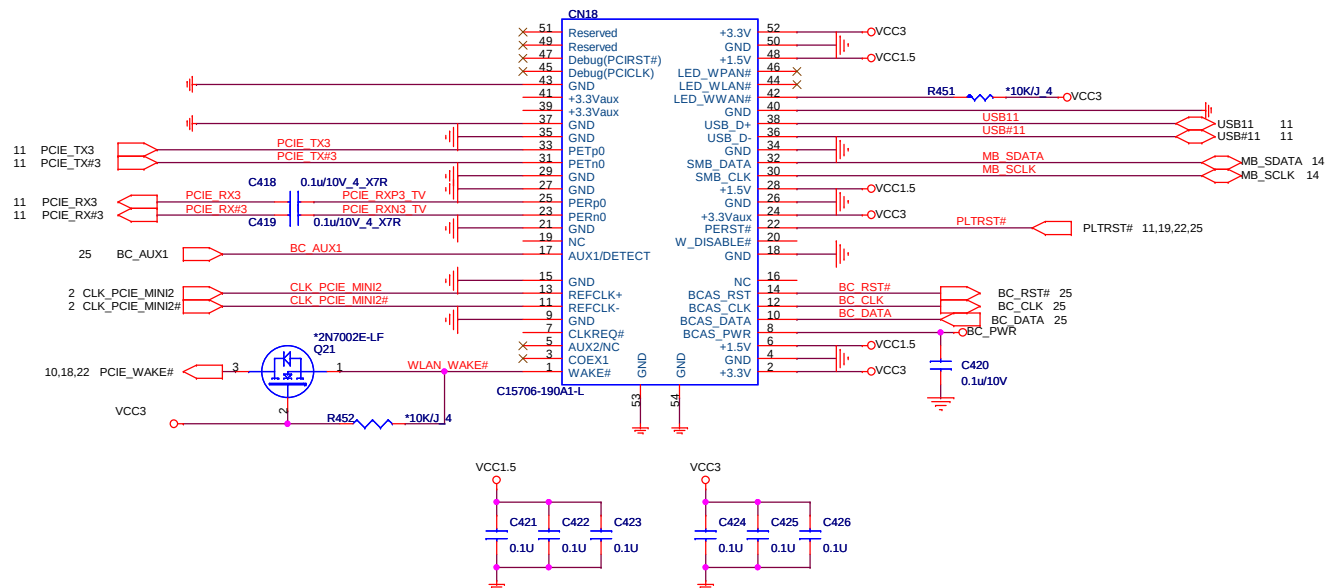
Figure 10 shows the SATA RX2 and TX2 signal connections. The SATA controller pins are connected to the SATA connector pins as follows:

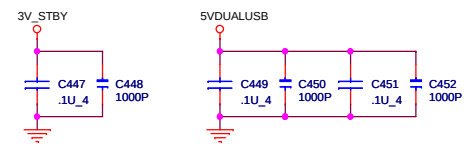
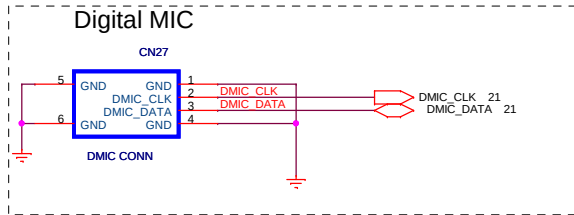
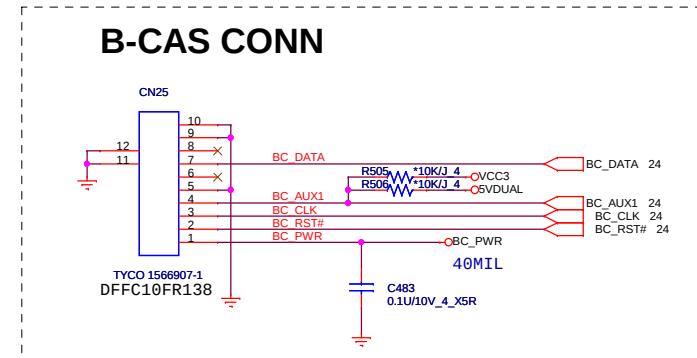
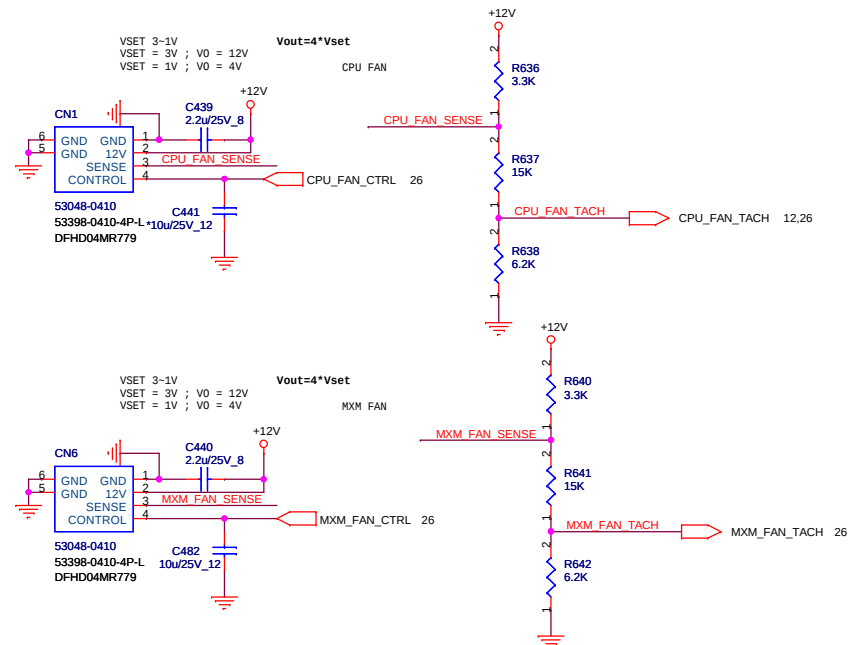
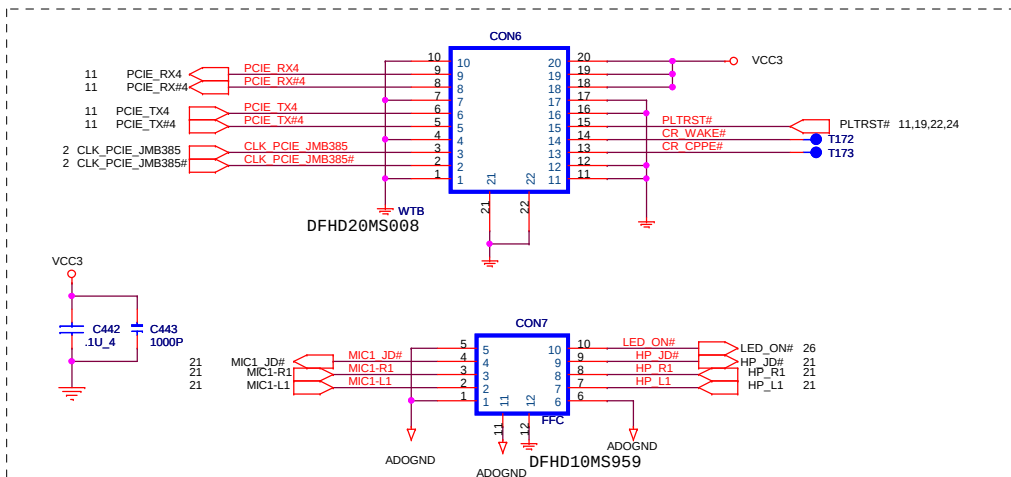
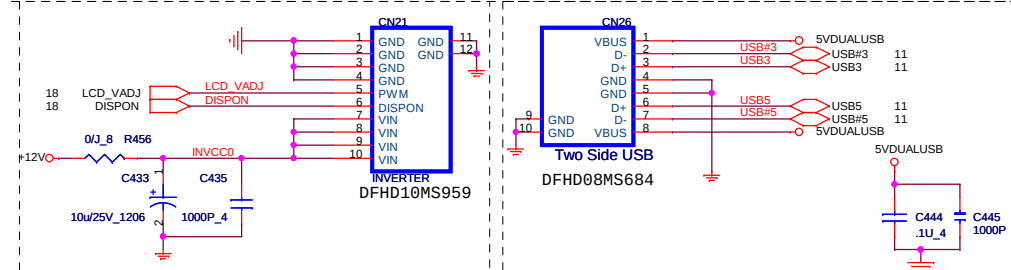
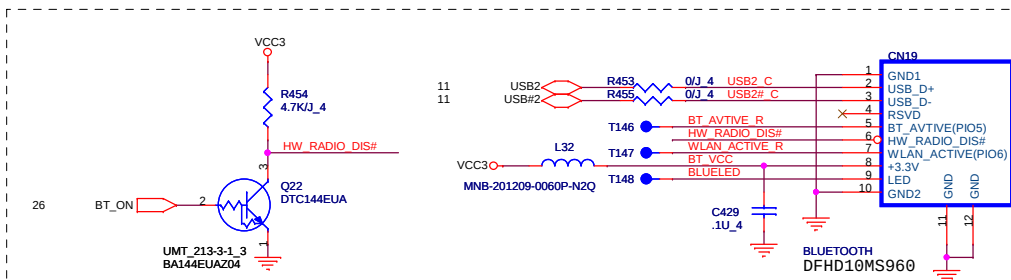
- SATA_TX2 (Pin 12) connects to TXP (Pin 2)
- SATA_TX2 (Pin 13) connects to TXN (Pin 3)
- SATA_RX2 (Pin 14) connects to RXN (Pin 5)
- SATA_RX2 (Pin 15) connects to RXP (Pin 6)

The SATA connector is labeled "E-SATA" and "sata-2sa1506-000d11-7p". The connector pins are: 1: GND1, 2: TXP, 3: TXN, 4: GND2, 5: RXN, 6: RXP, 7: GND5, 8: RXN, 9: GND4, 10: GND.

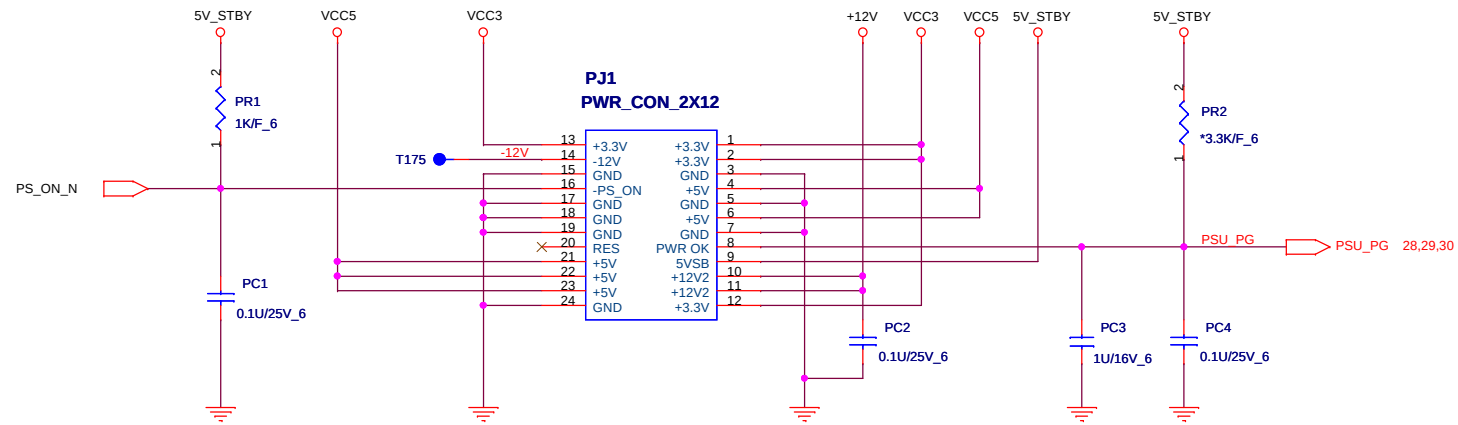
[illegible]

Pin connection diagram for the HOME button. The diagram shows a 10-pin connector labeled CON10. Pin 1 is connected to VCC3. Pin 2 is connected to a 0.1uF/10V_4 capacitor, which is also connected to VCC3. Pin 3 is connected to ATTN. Pin 4 is connected to MBDATA1. Pin 5 is connected to MBDCLK1. Pin 6 is connected to ground. Pin 7 is connected to ground. Pin 8 is connected to ground. Pin 9 is connected to ground. Pin 10 is connected to ground. The connector is labeled HOME BUTTON.



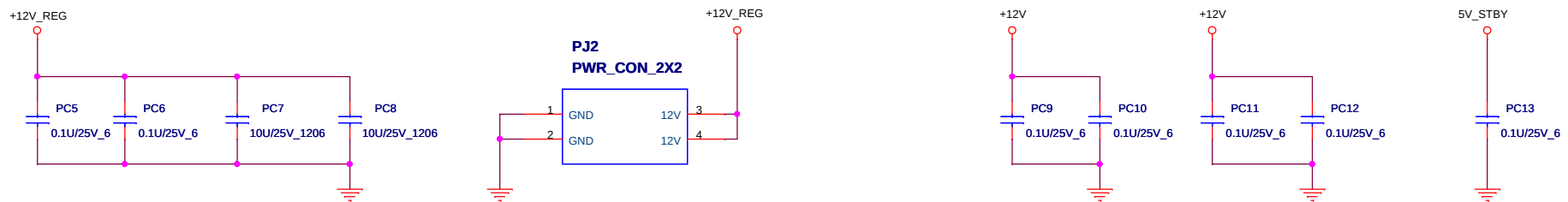


PSU 24PIN Connector

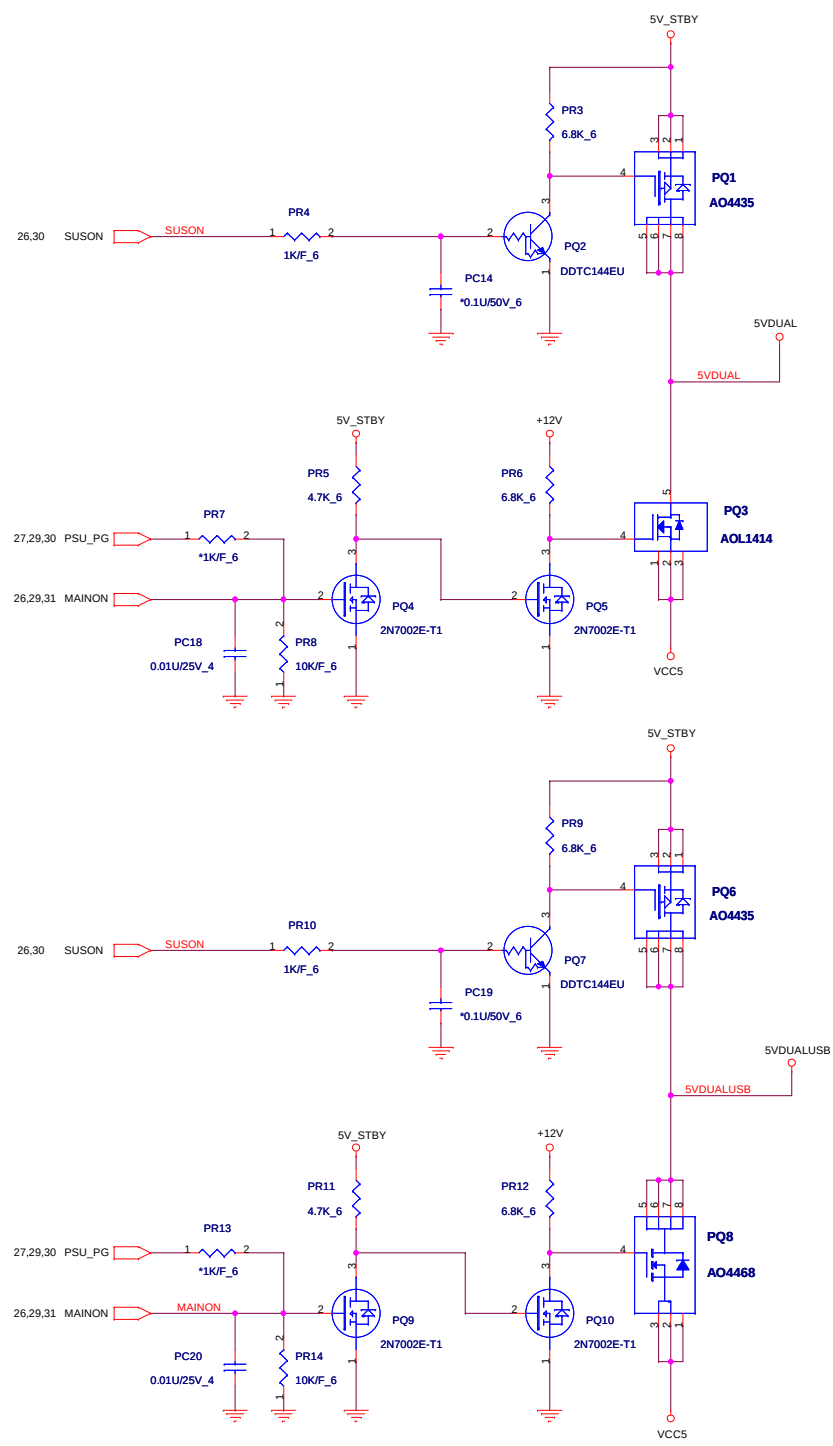


P3V3_STB : Stand-by power source only
 P3V3 : Normal power source only
 P3V3_DUAL : Both power source switching

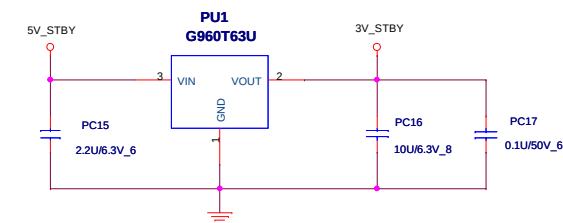
4PIN +12V_REG for CPU_CORE



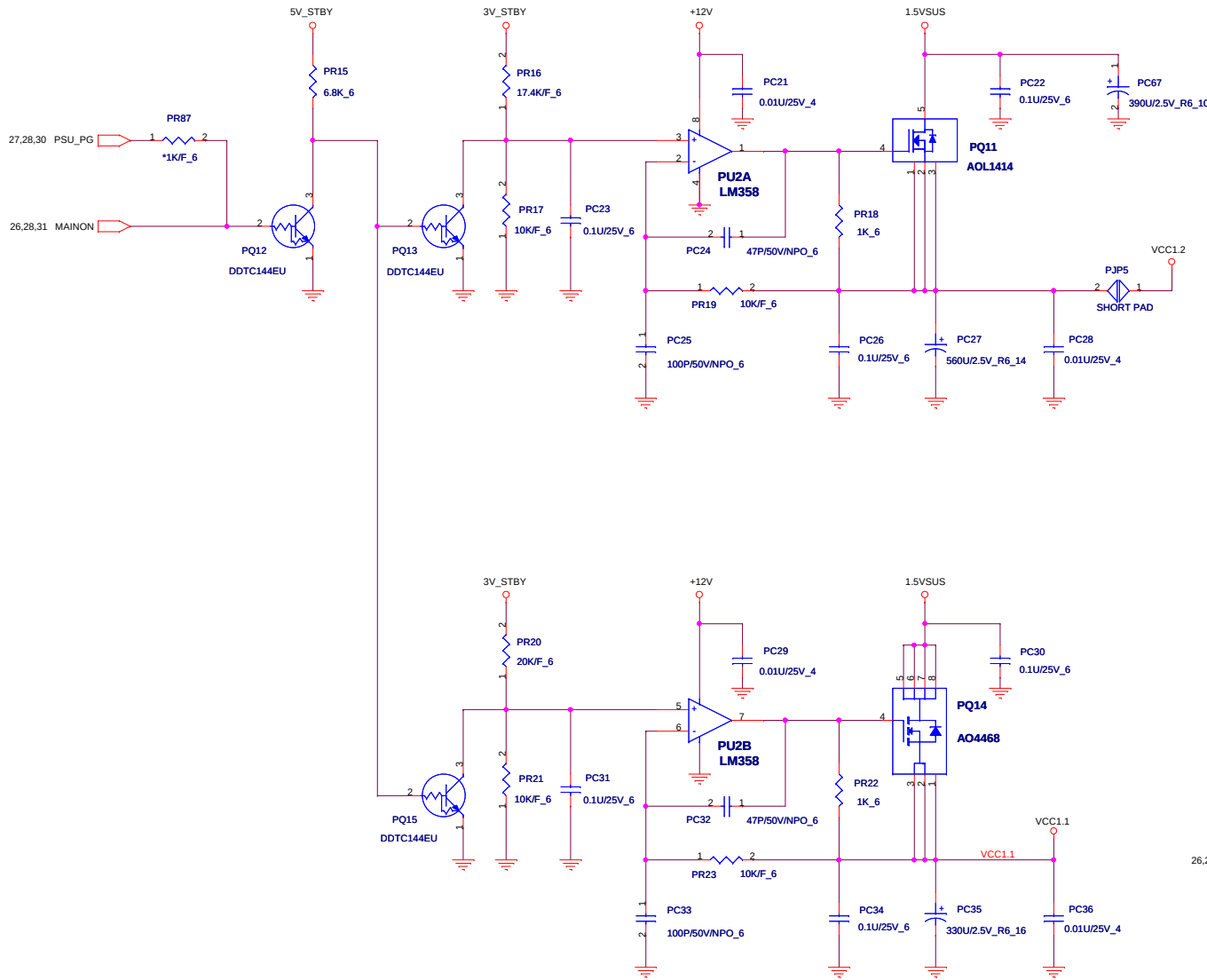
5VDUAL, 5VDUALUSB, 3V_STBY



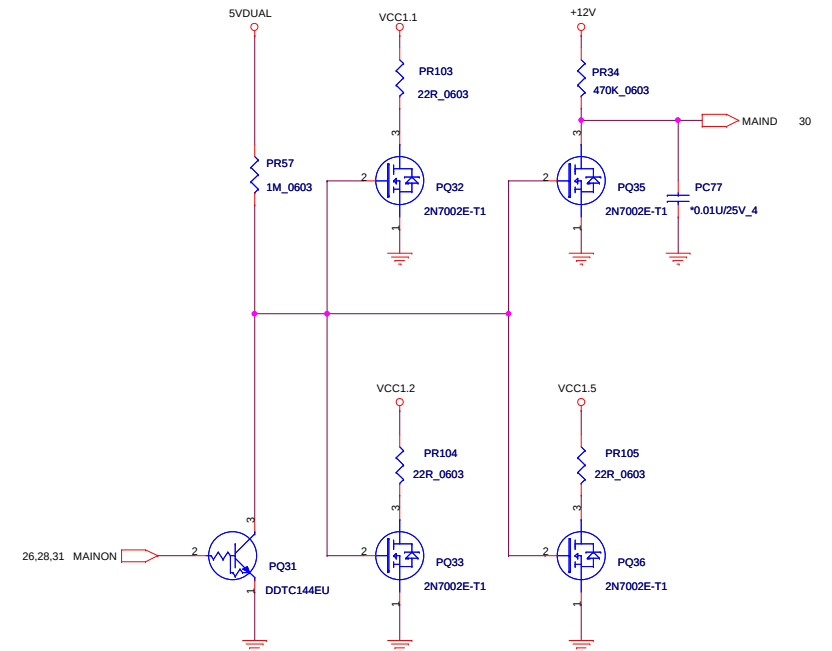
for EC



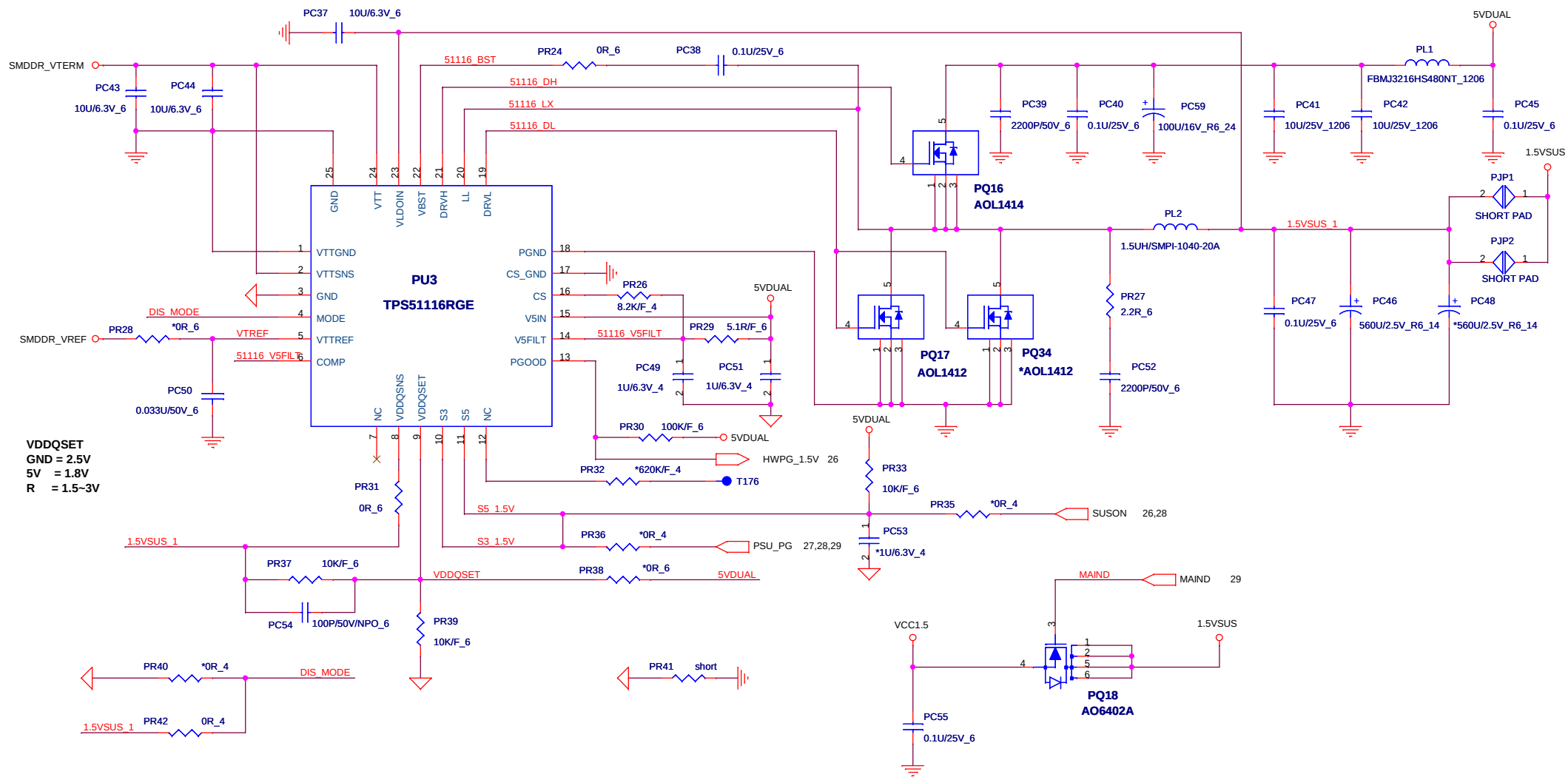
VCC1.2, VCC1.1



For ICH10



DDR3 1.5V(TPS51116)



$$deI_{IL} = (5V - 1.5V) \times 1.5V / (1.5u \times 400K \times 19V) = 4.6A$$

$$(10uA \times PR26 / R_{dson}) + deI_{IL} / 2 = I_{ocp}$$

$$(10uA \times 8.2K / 4.6m) + deI_{IL} / 2 = 20.1A$$

A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

