

SJM11_MS (ZH8) BLOCK DIAGRAM

PCB STACK UP 8L HDI

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

XTAL
Y2
14.318MHZ

CLOCK
CK505 (QFN-64)
PG2

FAN & THERMAL
P3

POWER

SYSTEM 5V/3V
RT8206B P24

CPU Core
ISL6261A P25

DDR Power
RT8207A P26

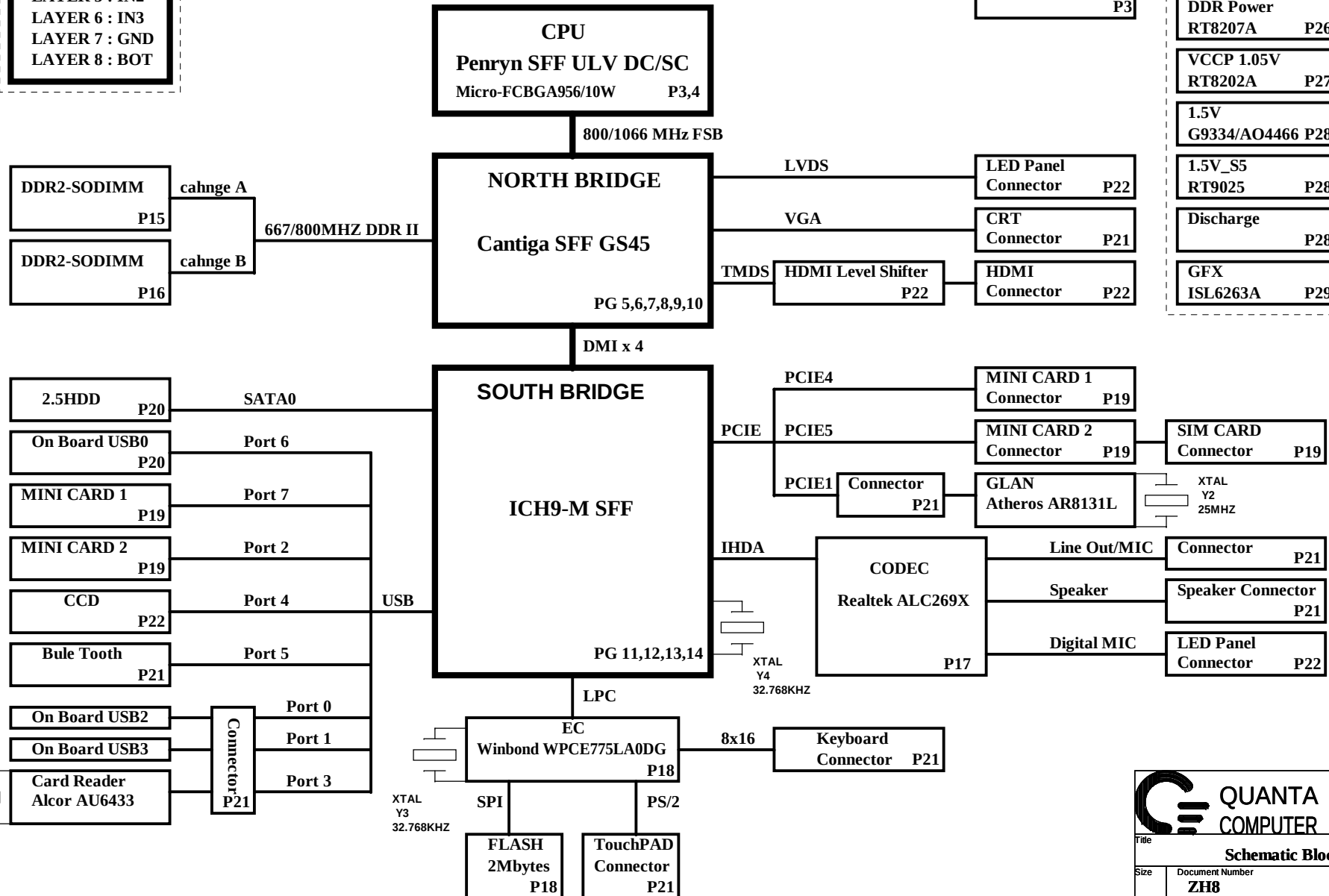
VCCP 1.05V
RT8202A P27

1.5V
G9334/AO4466 P28

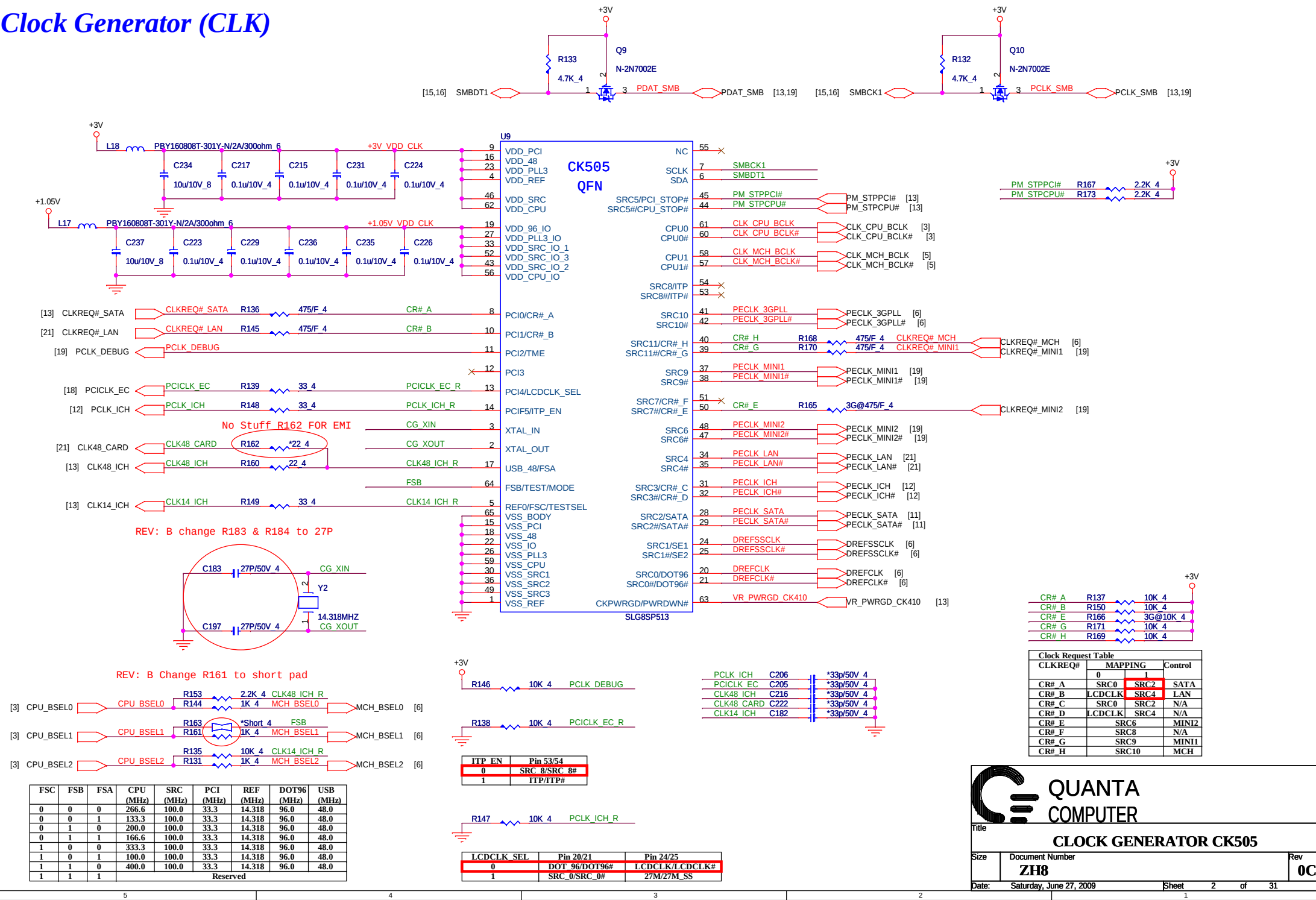
1.5V_S5
RT9025 P28

Discharge
P28

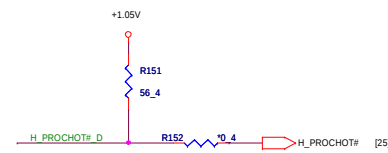
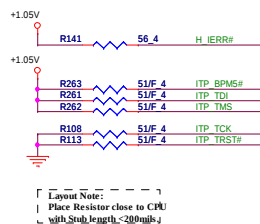
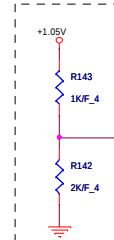
GFX
ISL6263A P29



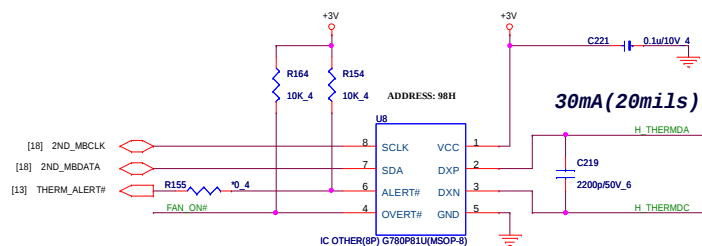
Clock Generator (CLK)



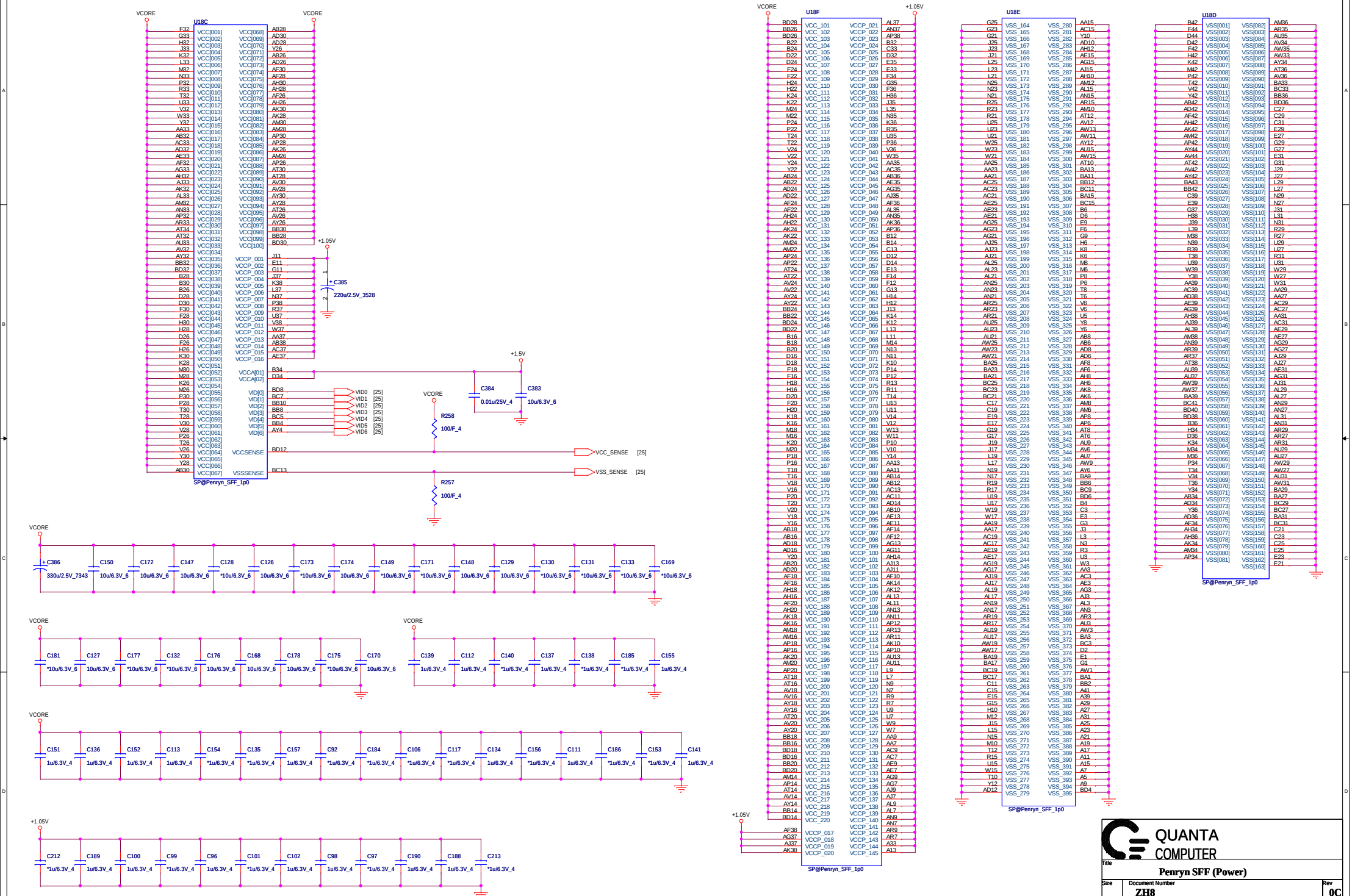
1.2G	AJSLGAMVT02
1.4G	AJSLGFMTT00



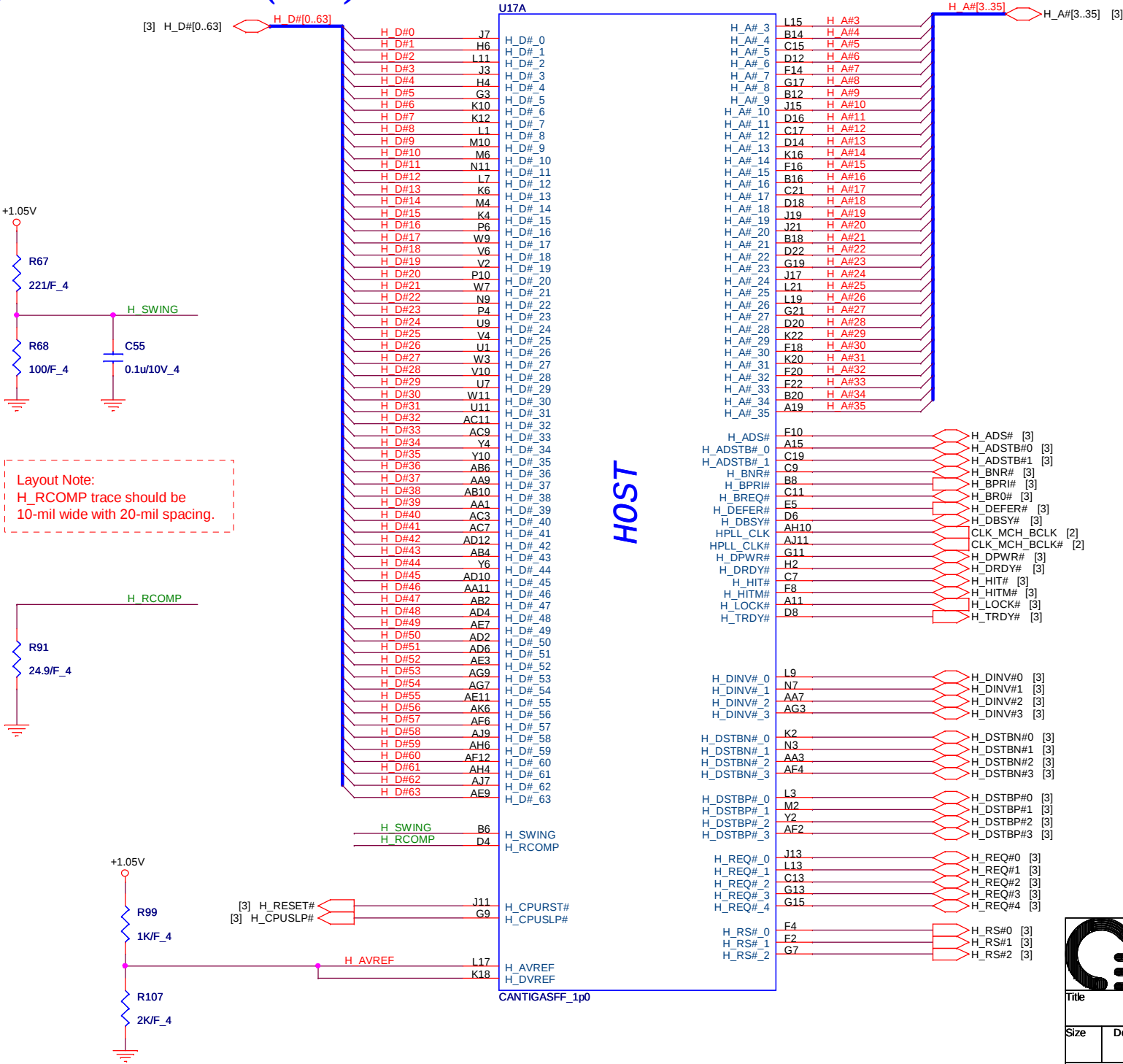
CPU Thermal Monitor(THM)



Penryn SFF - Power (CPU)



Cantiga SFF - Host Bus (CLG)

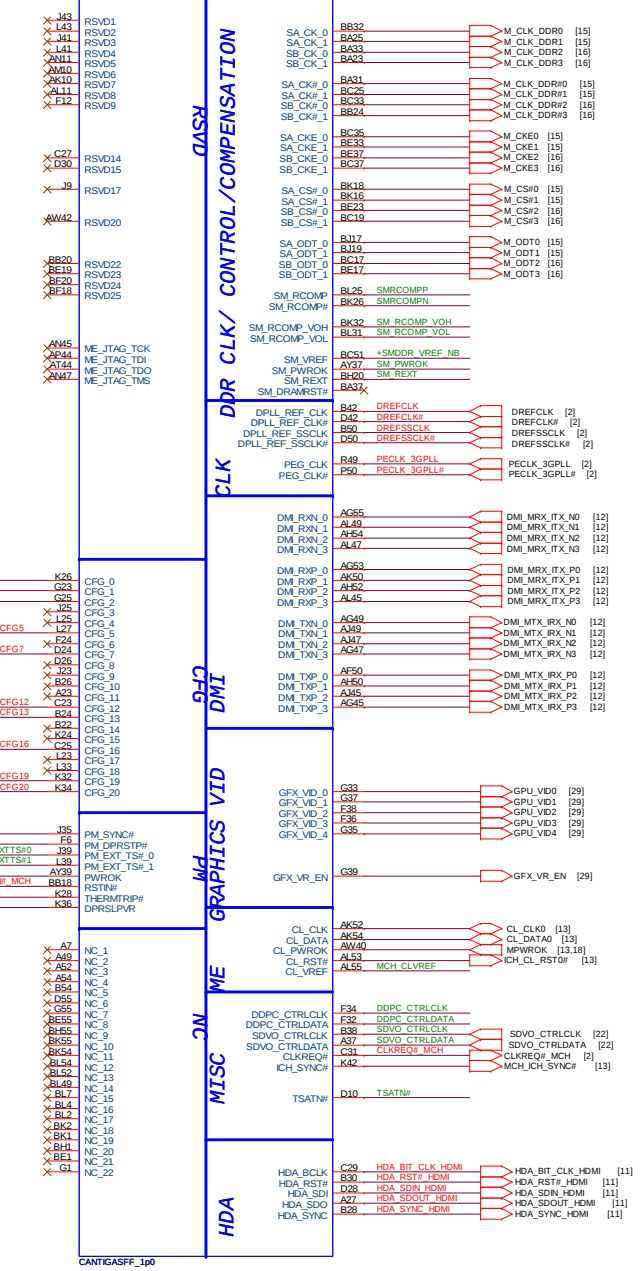
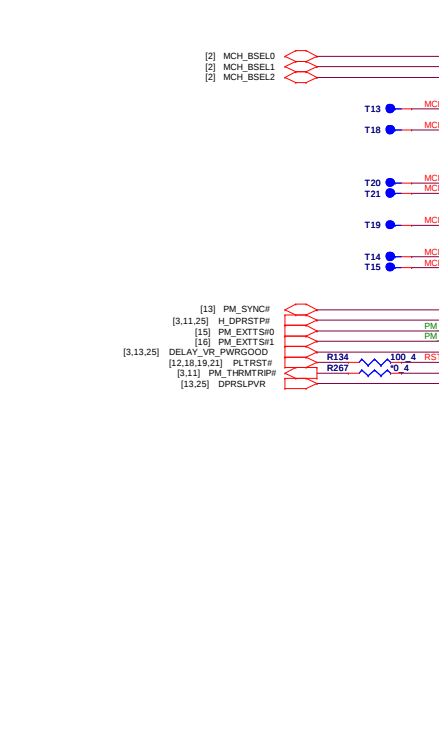


Cantiga SFF - DMI/VGA (CLG)

Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Other = Reserved
CFG4:3	Reserved	
CFG5	DMI x2 Select	1 = DMI x2 0 = DMI x1
CFG6	ITPM Host Interface	1 = ITPM enabled 0 = ITPM disabled
CFG7	Intel Management Engine Crypto TLS Engine Crypto Strap	1 = ITPM enabled 0 = ITPM disabled
CFG8	Reserved	
CFG9	PCI Express Lane	1 = Normal operation : Lane Numbered in Order 0 = Reverse Lanes
CFG10	PCI Express enable	1 = Enabled 0 = Disabled
CFG11	Reserved	
CFG12	ALLZ	1 = Disabled 0 = ALLZ mode enabled
CFG13	XOR	1 = Disabled 0 = XOR mode enabled
CFG14	Reserved	
CFG15	Reserved	
CFG16	FSB Dynamic ODT	1 = Dynamic ODT enabled 0 = Dynamic ODT disabled
CFG17	Reserved	
CFG18	Reserved	
CFG19	DMI Lane Reversal	1 = Reverse Lanes 0 = Normal operation : Lane Numbered in Order
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIe	1 = Digital DisplayPort (SDVO/DP/HDMI) and PCIe are operating simultaneously via the PCIe port 0 = Digital DisplayPort (SDVO/DP/HDMI) or PCIe are operational
SDVO_CTRLDATA	SDVO Present	1 = SDVO/DP/HDMI interface enabled 0 = No SDVO/DP/HDMI interface enabled
L_DDC_DATA	Local Flat Panel (LEP) Present	1 = LEP Card Present, PCIe disabled 0 = LEP Disabled
DDPC_CTRLDATA	Digital Display	1 = Digital display (HDMI/DP) device present 0 = Digital display (HDMI/DP) interface absent

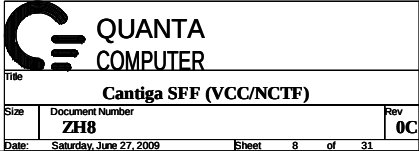
The recommended pull-up resistor value is 4.02 kΩ ±1%.

The recommended pull-down resistor value is 2.21 kΩ ±1%.

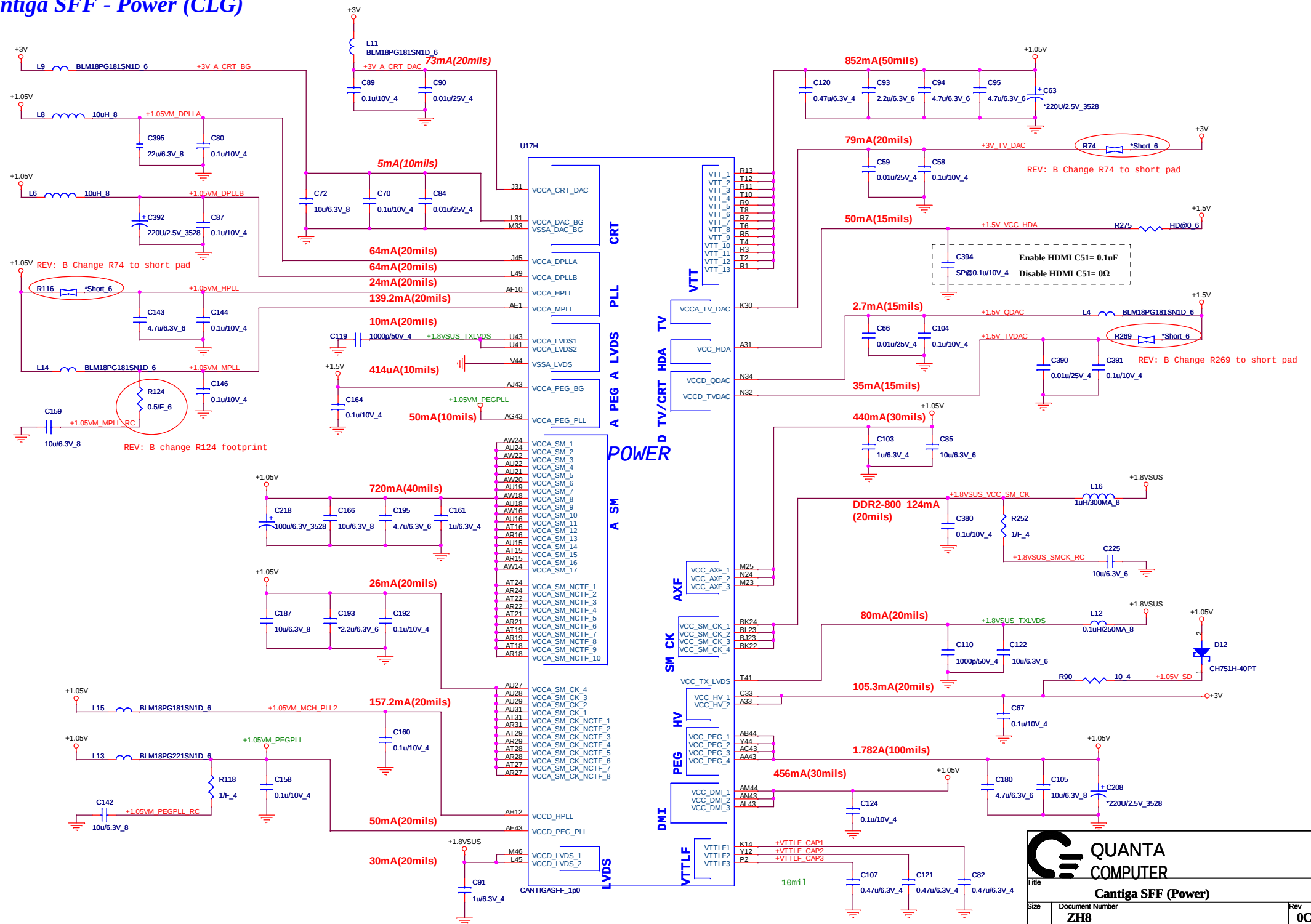


QUANTA COMPUTER	
Title	
Cantiga SFF (DDRIII)	
Size	Document Number ZH8
	Rev 0C
Date:	Saturday, June 27, 2009
Sheet	7 of 31

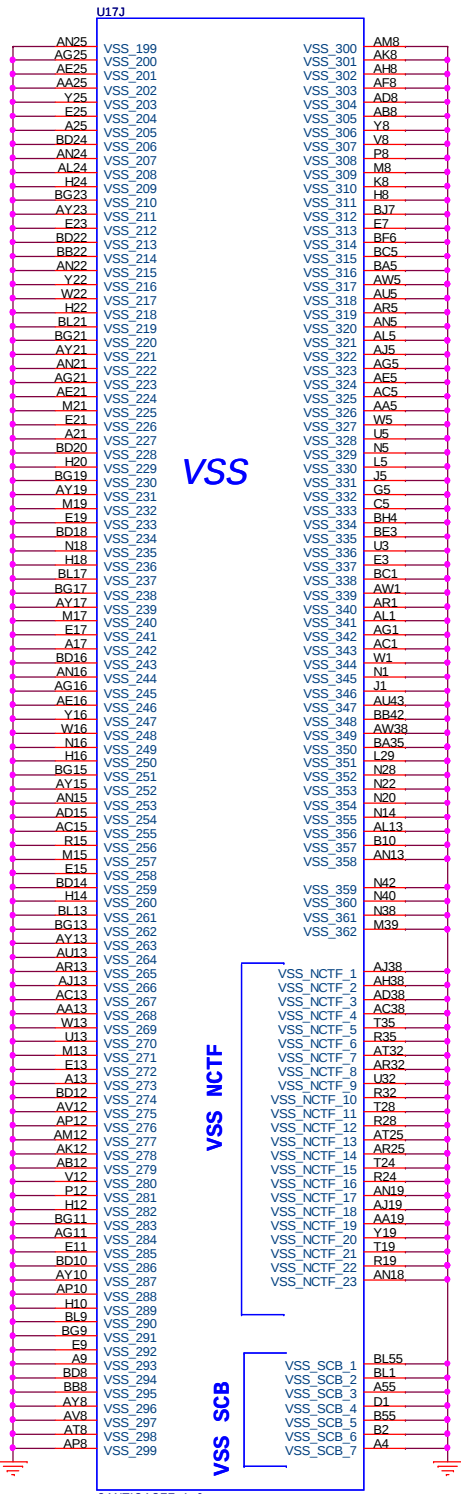
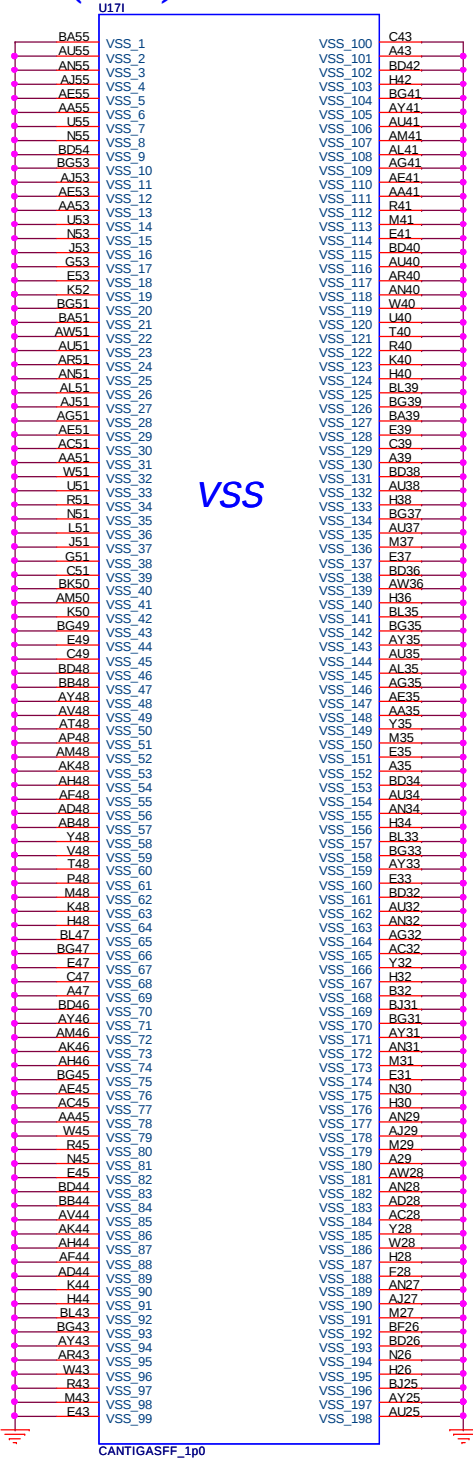
lvcc internal VGA 2.4A
(Shape or 140mils)



		QUANTA COMPUTER	
Title			
Cantiga SFF (Power)			
Size	Document Number		Rev
	ZH8		00
Date:	Saturday, June 27, 2009	Sheet	9 of 31



Cantiga SFF - GND (CLG)





QUANTA
COMPUTER

Title

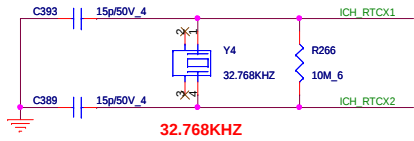
Cantiga SFF (GND)

Size	Document Number	Rev
	ZH8	0C

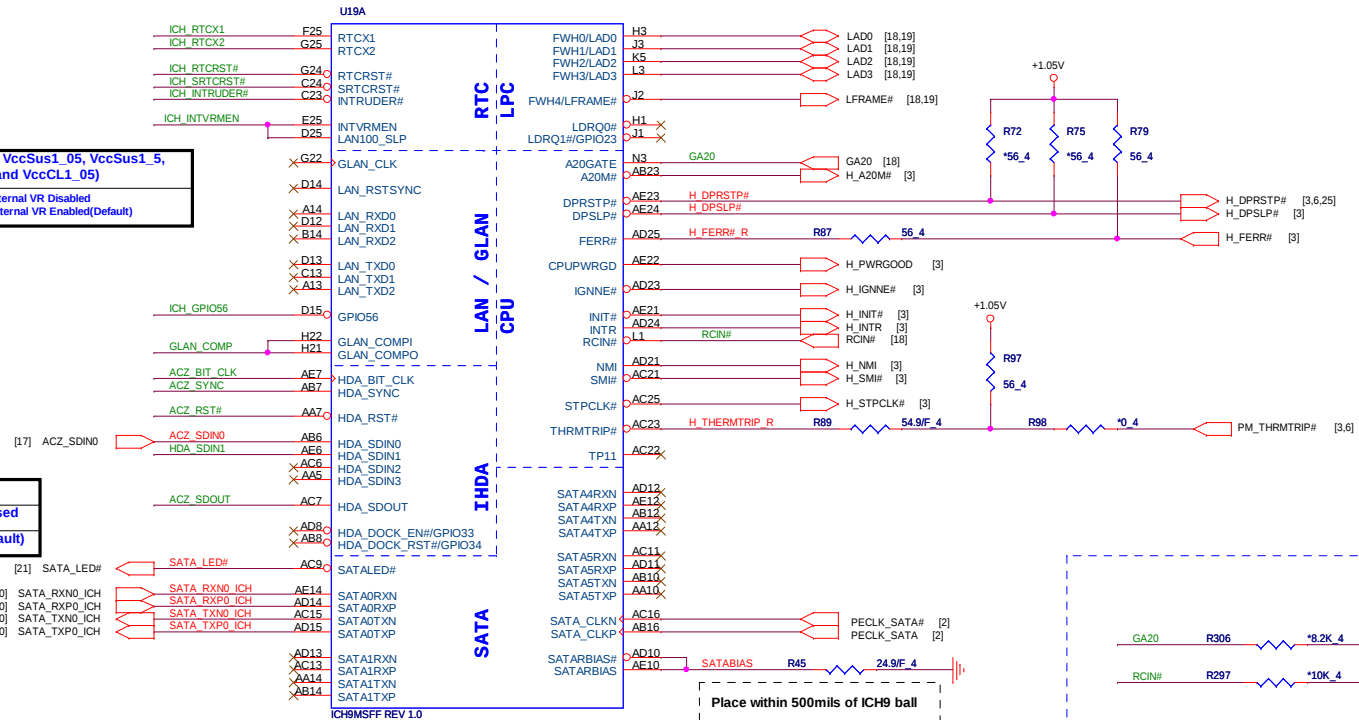
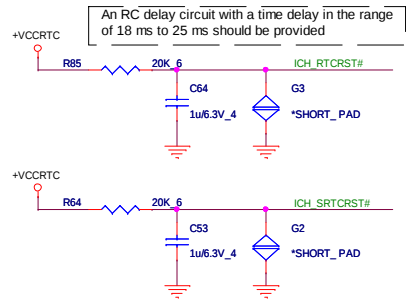
Date: Saturday, June 27, 2009

Sheet 10 of 31

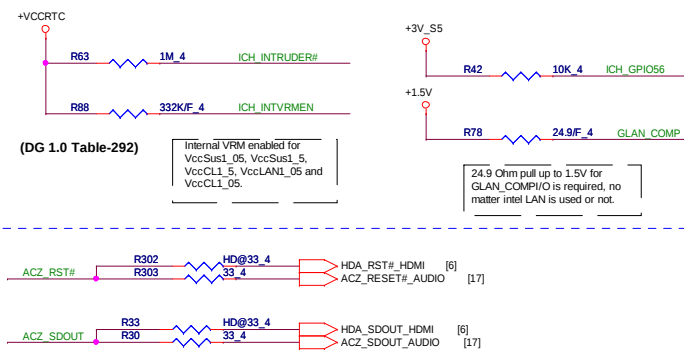
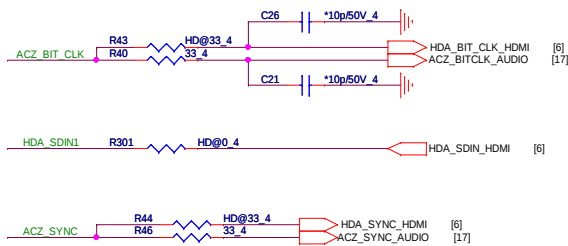
RTC CRYSTAL



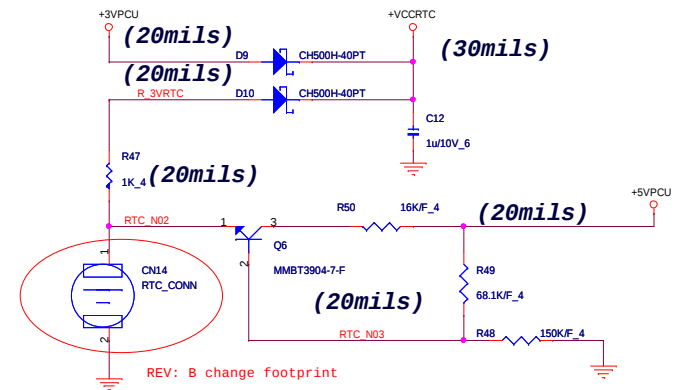
RESET JUMP



HD Audio Interface



RTC BATTERY (RTC)



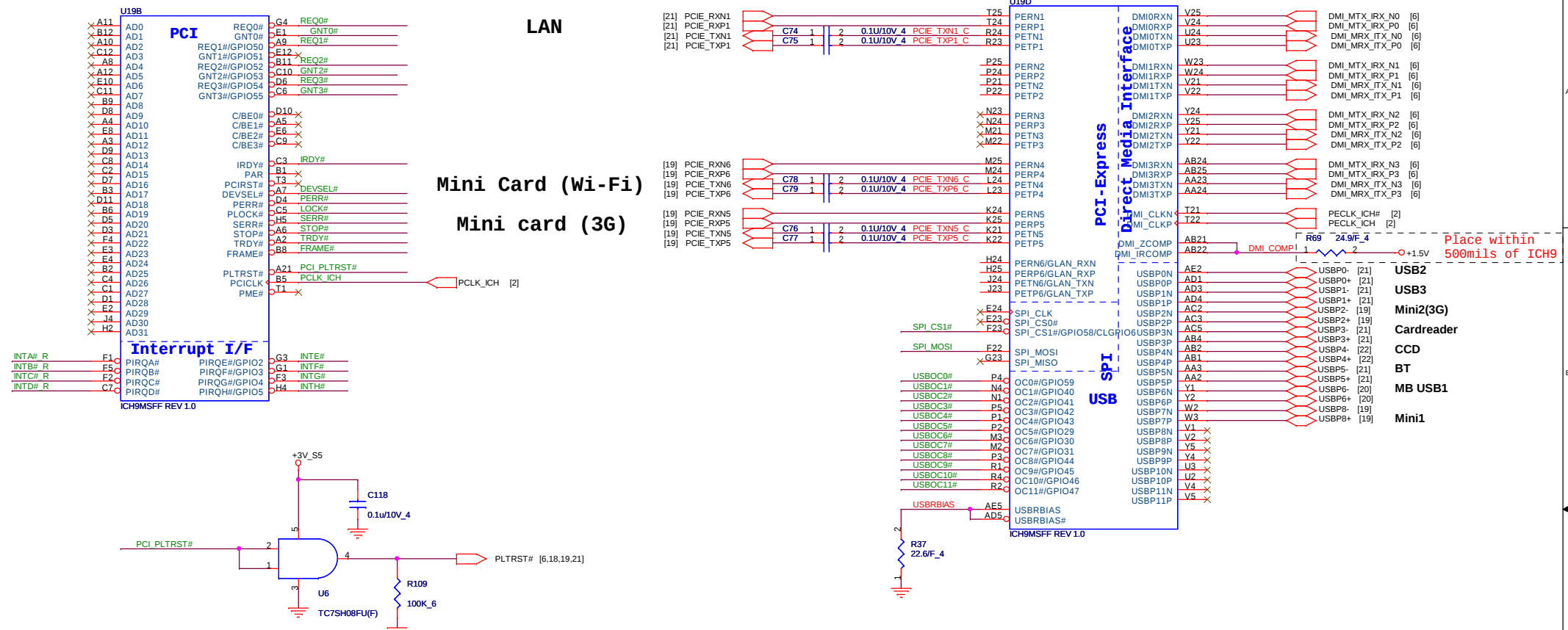
South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect			This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU			
	XOR Chain Entrance	PWROK	ICH_TP3	HDA_SDOUT	Description	
			0	0	RSVD	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	0	1	Enter XOR Chain	
			1	0	Normal operation(Default)	
			1	1	Set PCIe port config bit 1	

 QUANTA COMPUTER			
Title			
ICH9M SFF (Host/SATA/HDA)			
Size	Document Number		Rev
	ZH8		00
Date:	Saturday, June 27, 2009	Sheet	11 of 31

ICH9M SFF - USB/PCIE/DMI (CLG)

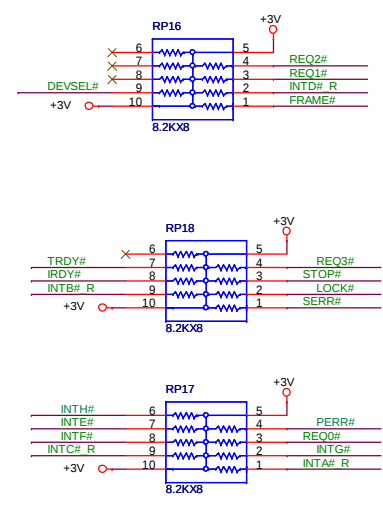
Place TX DC blocking caps close ICH9.



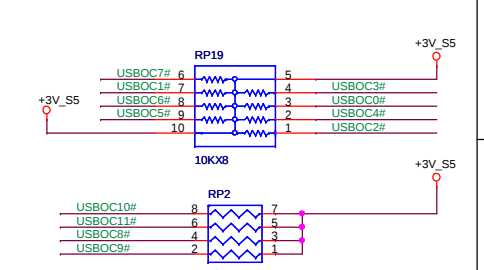
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	GNT2# T6
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# T4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI T11
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 SPI_CS#1 Boot Location 0 1 SPI(Default)	GNT0# T2
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 0 PCI	SPI_CS1# T10

PCI PULL-UP



USBOC# PULL-UP



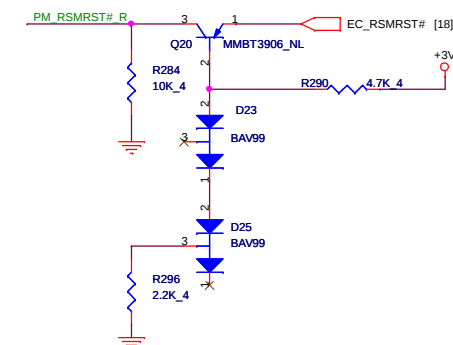
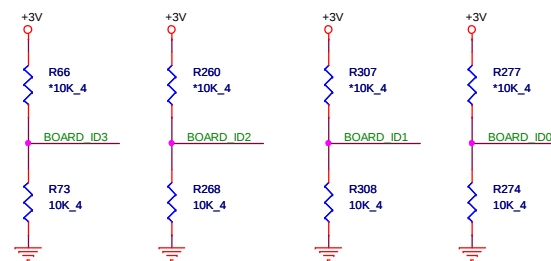
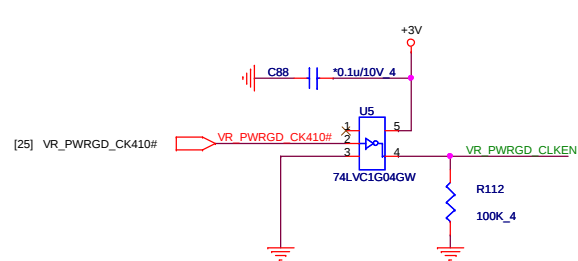
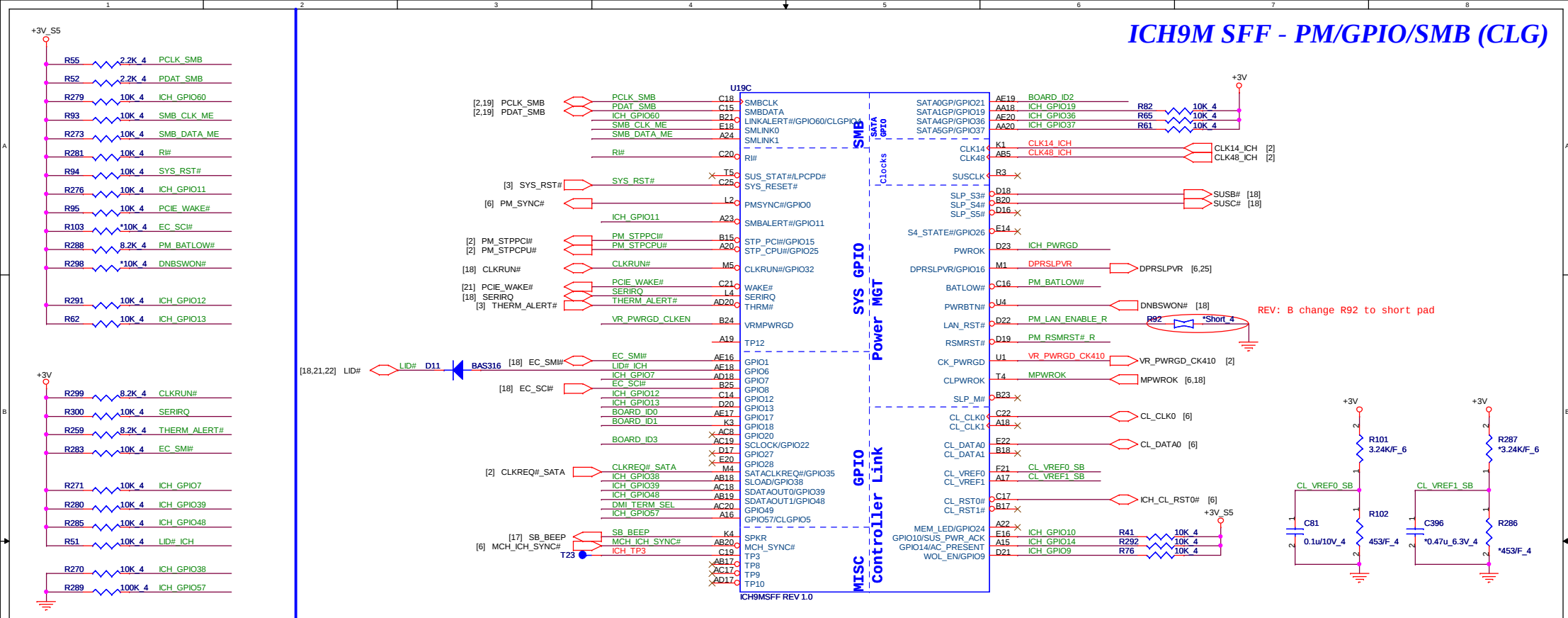
QUANTA
COMPUTER

File: ICH9M SFF (USB/PCIE/DMI)

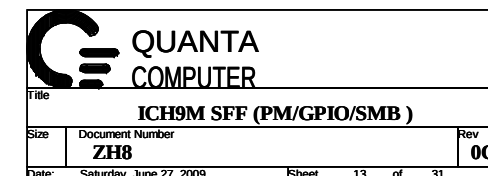
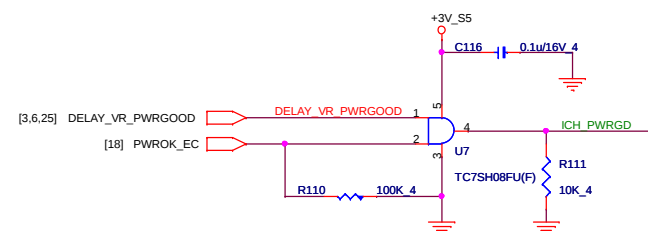
Size	Document Number	Rev
	ZH8	0C

Date: Saturday, June 27, 2009	Sheet 12 of 31
-------------------------------	----------------

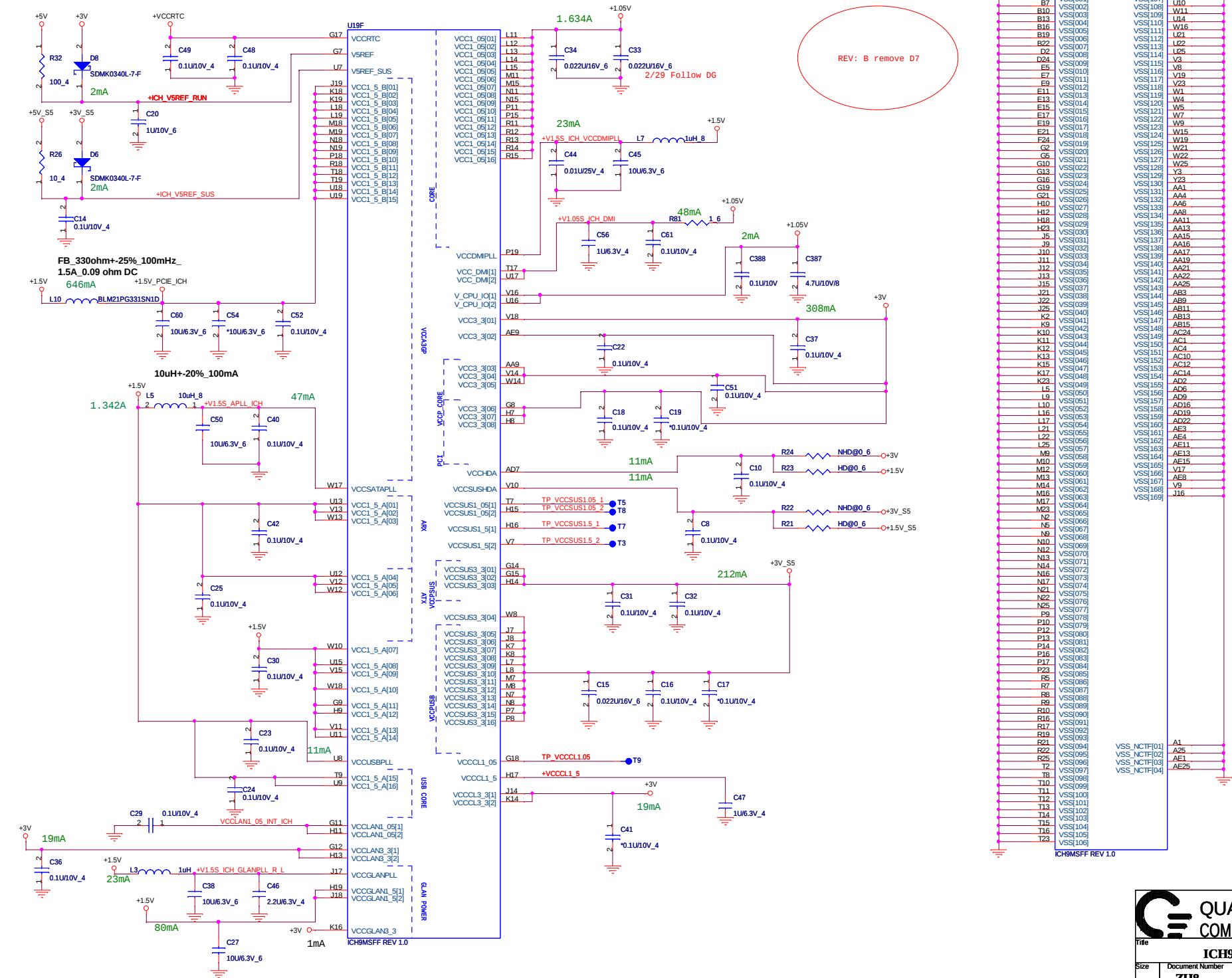
ICH9M SFF - PM/GPIO/SMB (CLG)



South Bridge Strap Pin (3/3)				
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPI020	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPI049	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	



ICH9M SFF - Power/GND (CLG)



REV: B remove D7



QUANTA
COMPUTER

Title

ICH9M SFF (Power/GND)

Size

Document Number

Date

Saturday, June 27, 2009

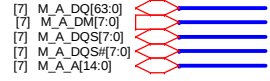
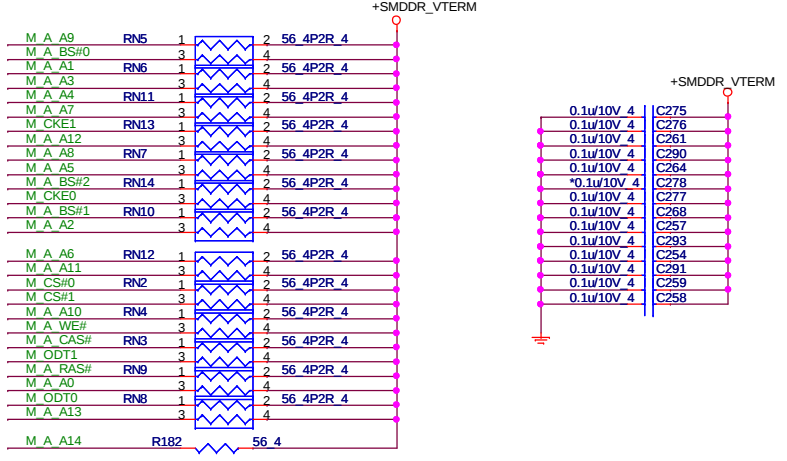
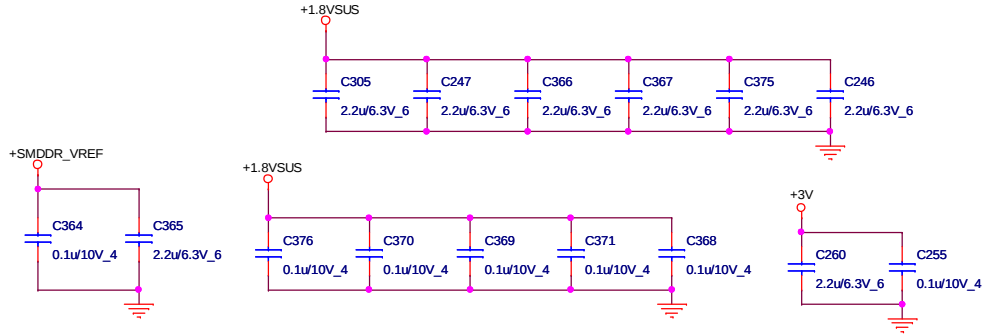
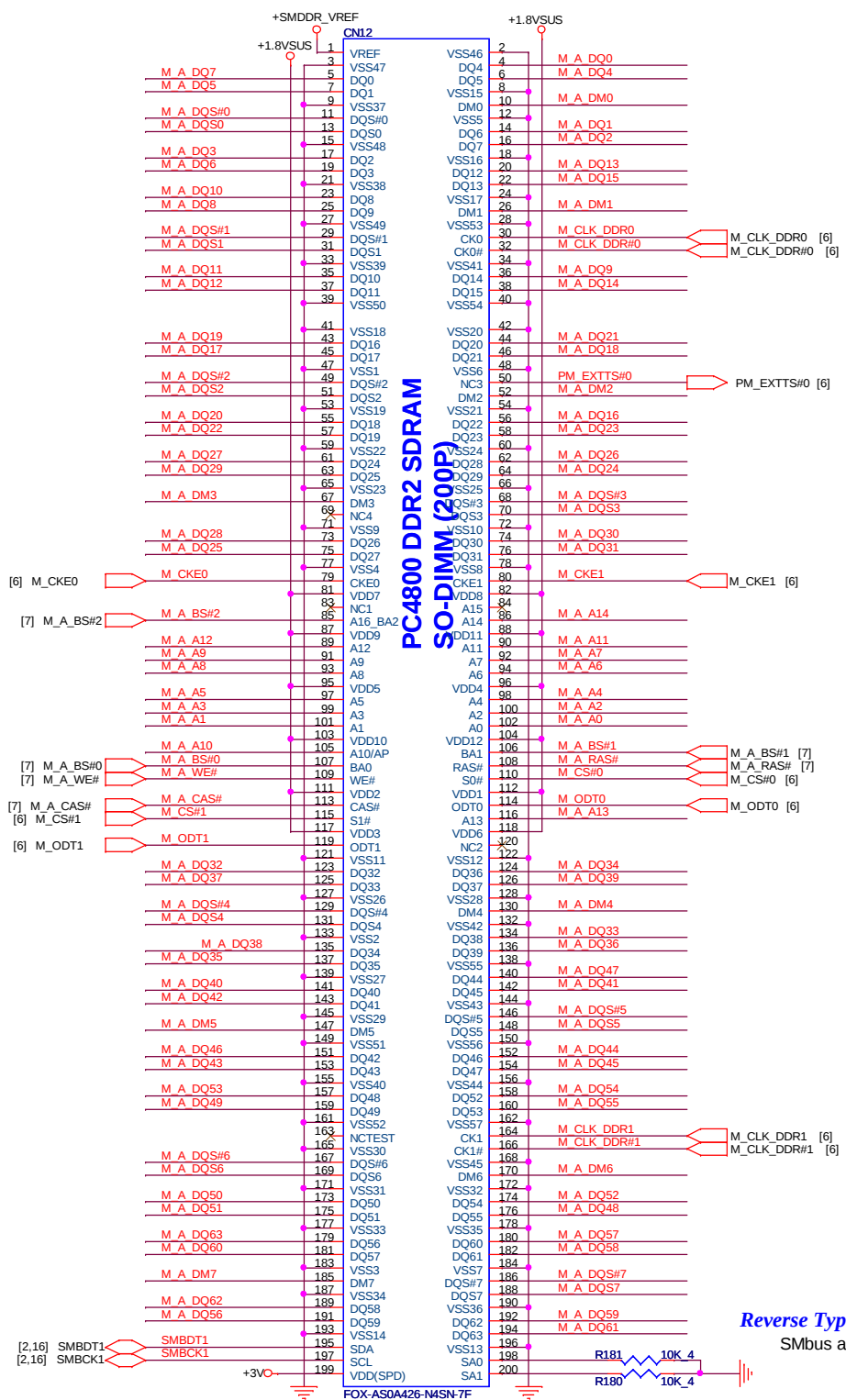
Sheet

14 of 31

Rev

0C

DDRII SO-DIMM (DDR)



Reverse Type H: 5.2mm
SMBus address A0



QUANTA
COMPUTER

Title

DDRII SO-DIMM

Size

Document Number

ZH8

Date

Saturday, June 27, 2009

Sheet

15

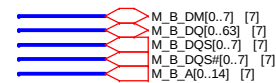
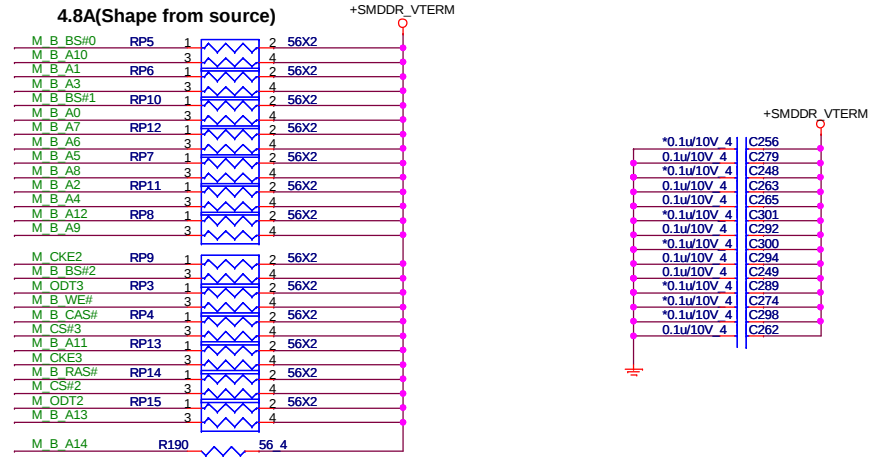
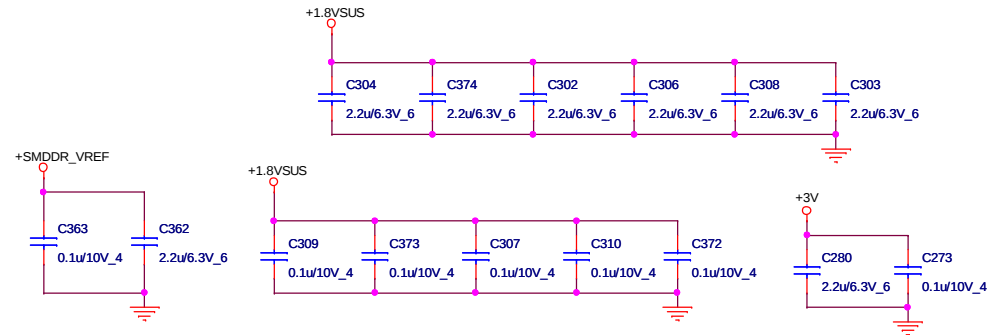
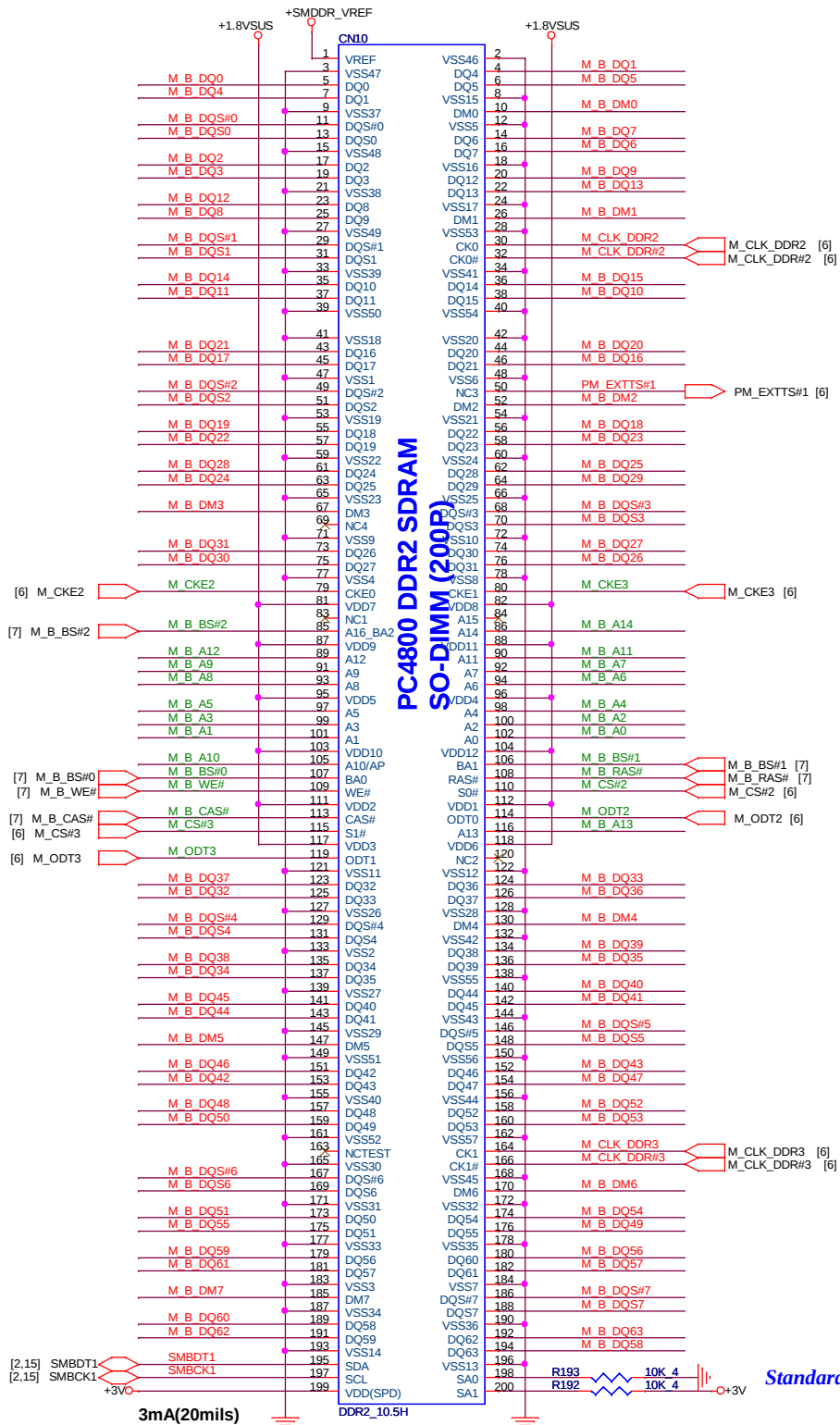
of

31

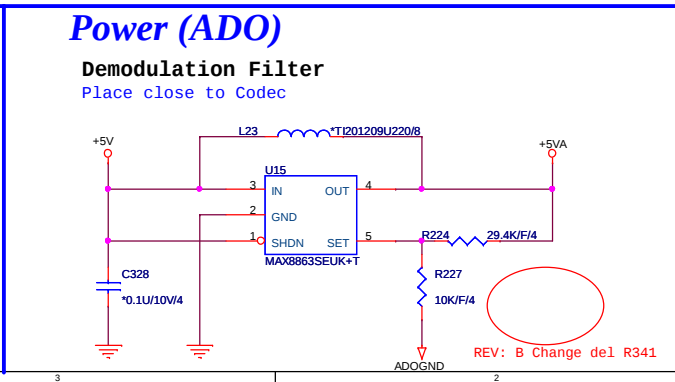
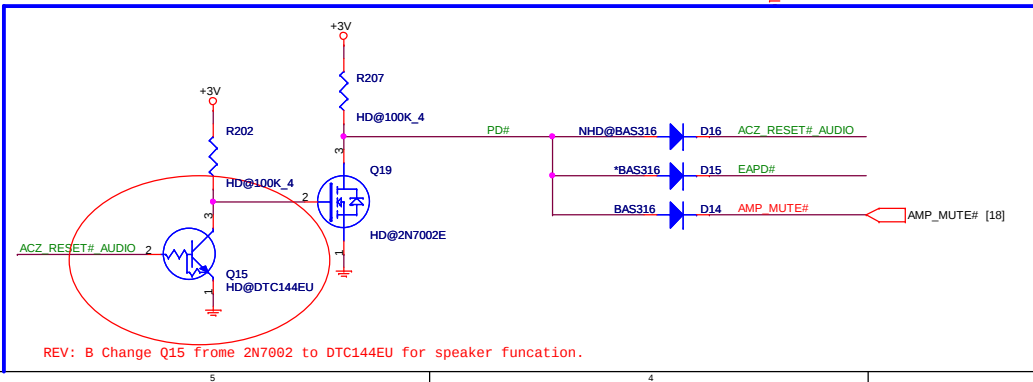
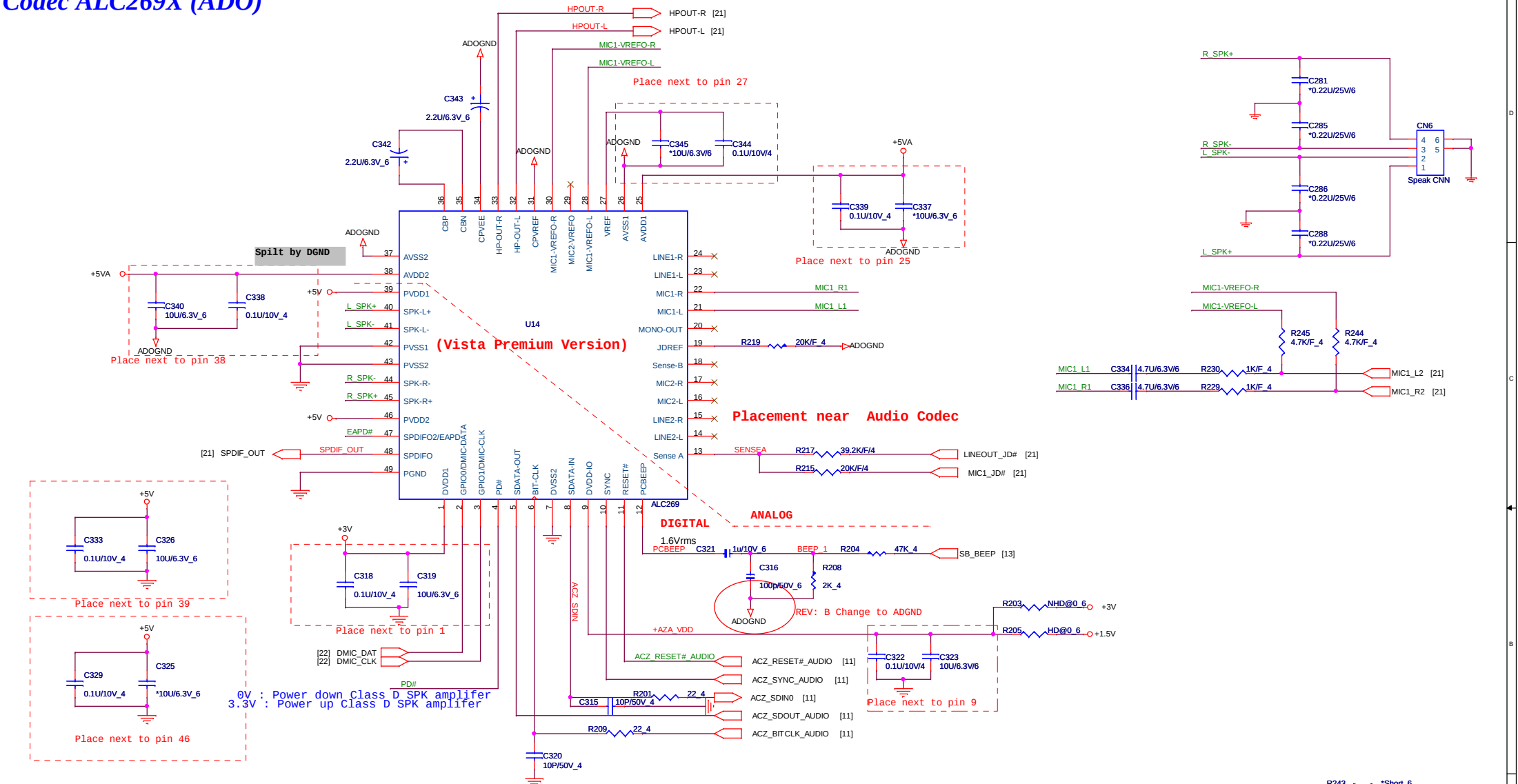
Rev

0C

DDRII SO-DIMM (DDR)



Codec ALC269X (ADO)



QUANTA COMPUTER

File: **Codec ALC269X**

Size	Document Number	Rev
	ZH8	0C

Date: Saturday, June 27, 2009 Sheet 17 of 31

R243 *Short 6

R248 *Short 6

R211 *Short 6

R231 *Short 6

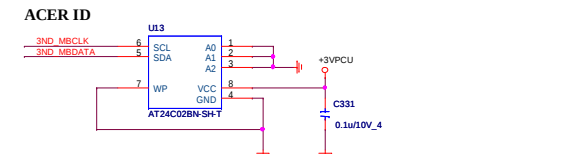
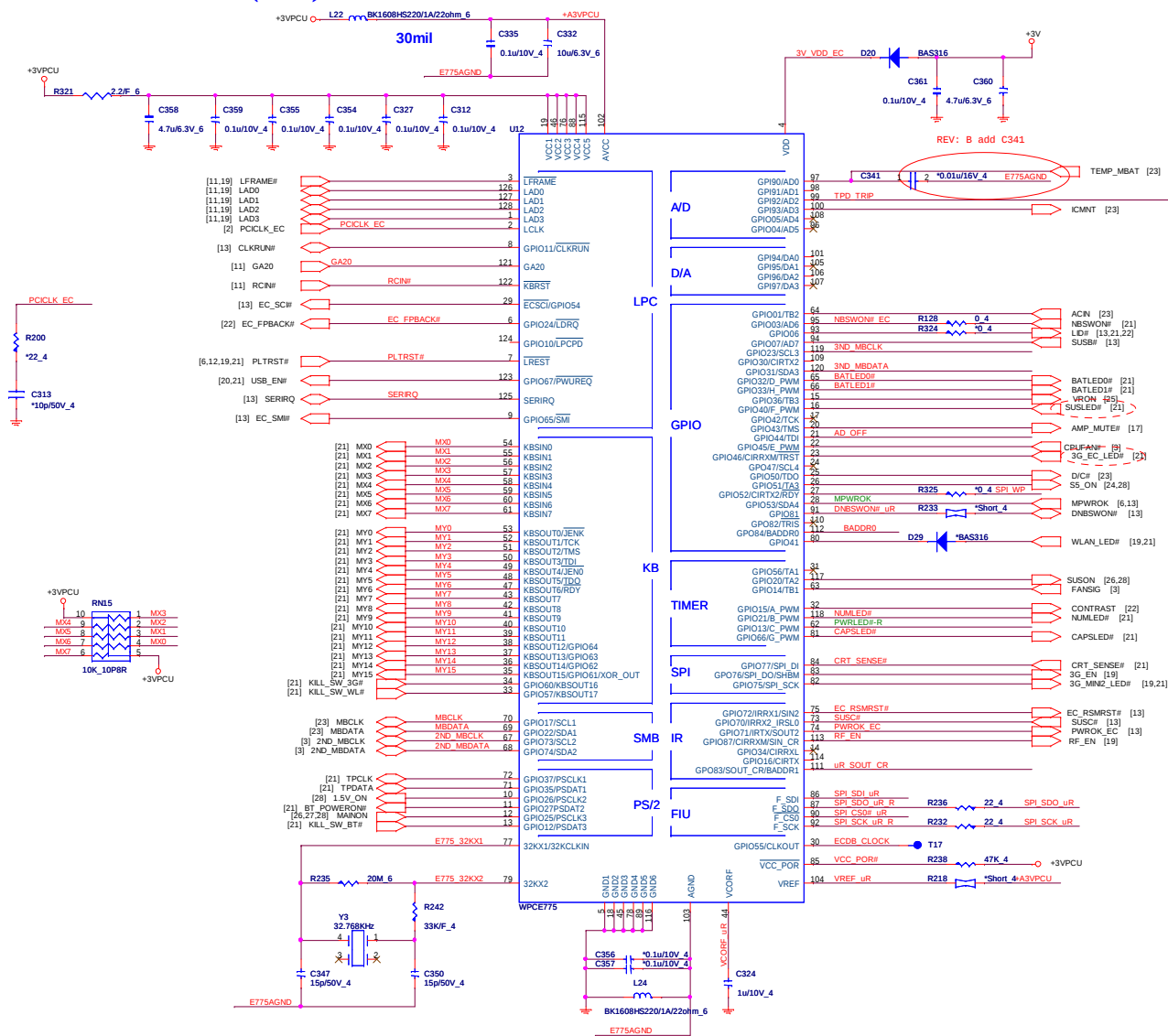
C349 *Short 4

C330 *Short 4

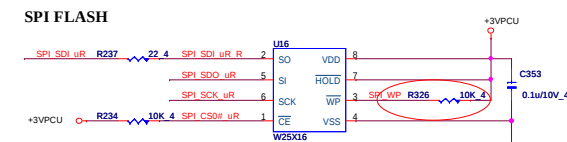
S2 *Short 6

ADOGND

EC WPCE775LA0DG (KBC)

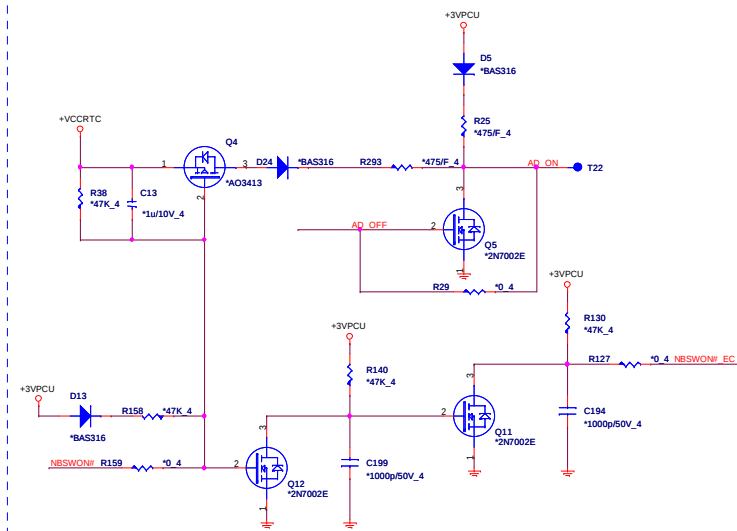


SPI FLASH

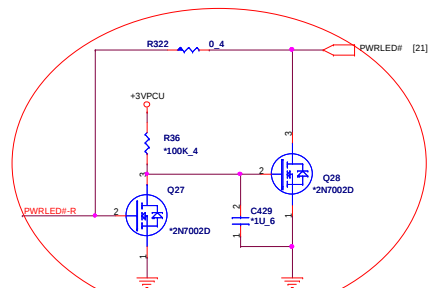
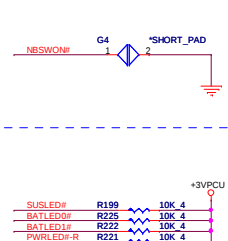


SPL Flash Source	P/N
Winbond W25X16AVSSIG	AKE38ZF9N01
MXIC MX25L1605AM2C-15G	AKE37FP9Z13
EON EN25F16-100H1P	AKE38ZA0Q00
AMIC A25L016	AKE38ZN0000

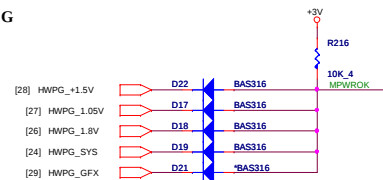
GREEN ADAPTER CIRCUIT



POWER SWITCH



HWPG



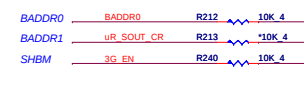
INTERNAL KEYBOARD STRIP SET



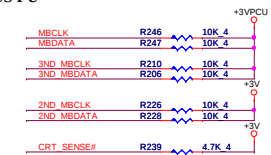
I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS



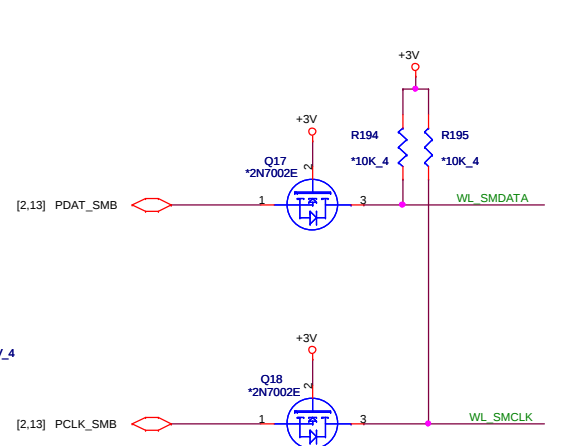
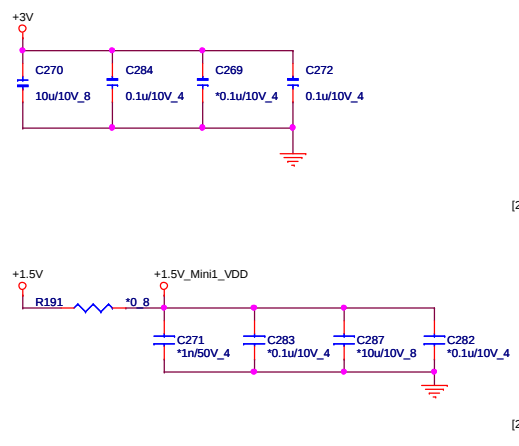
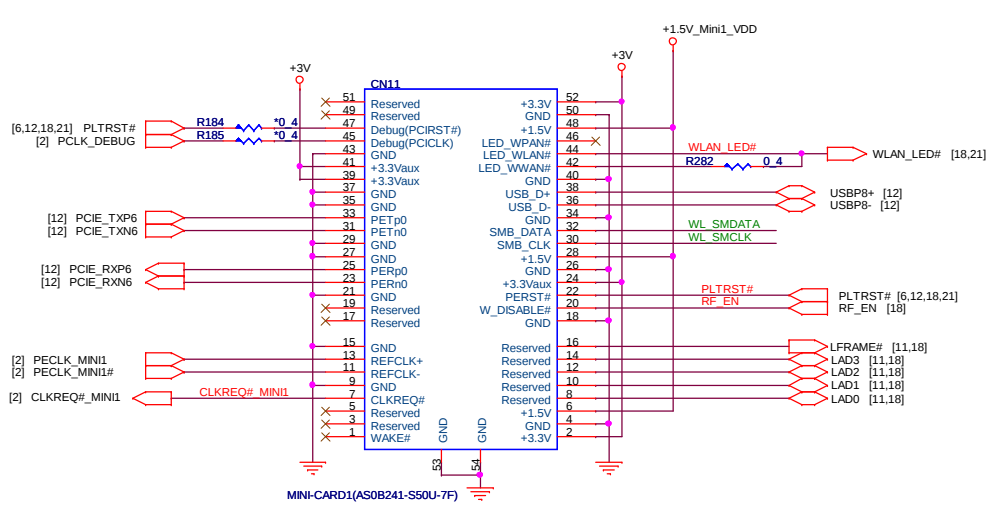
SM BUS PU



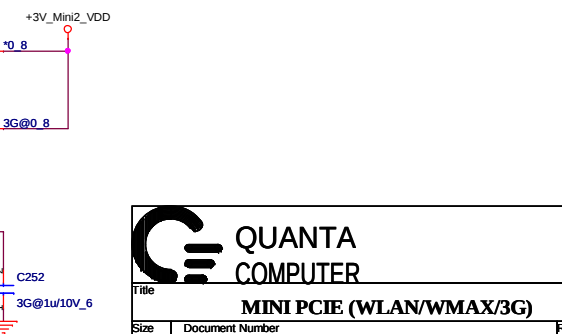
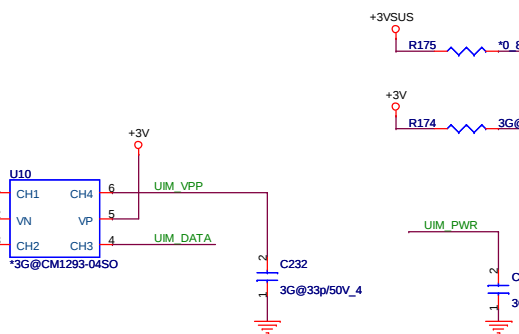
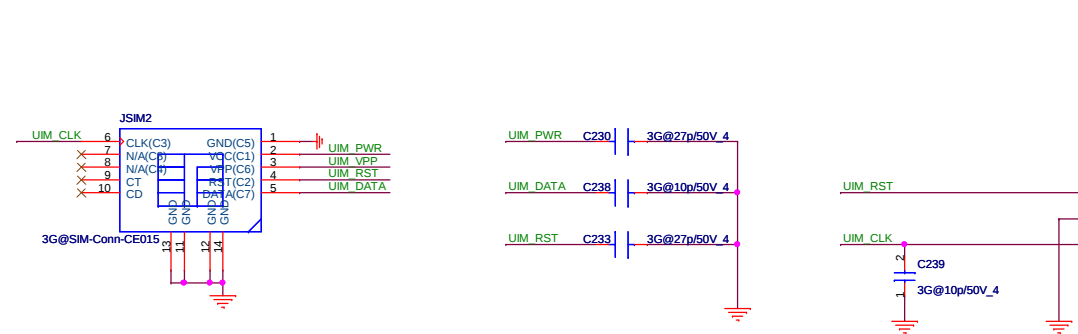
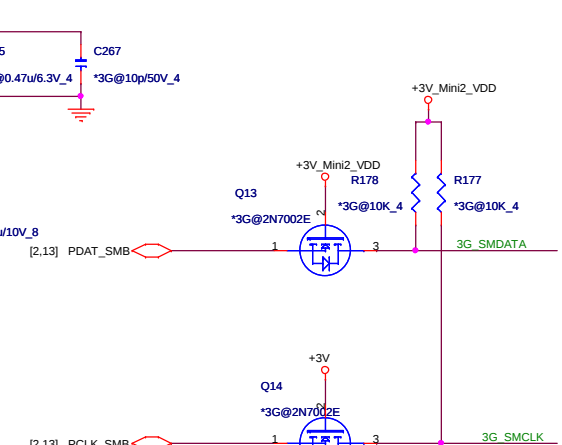
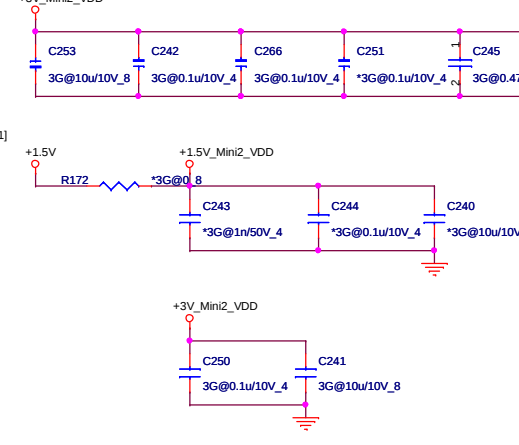
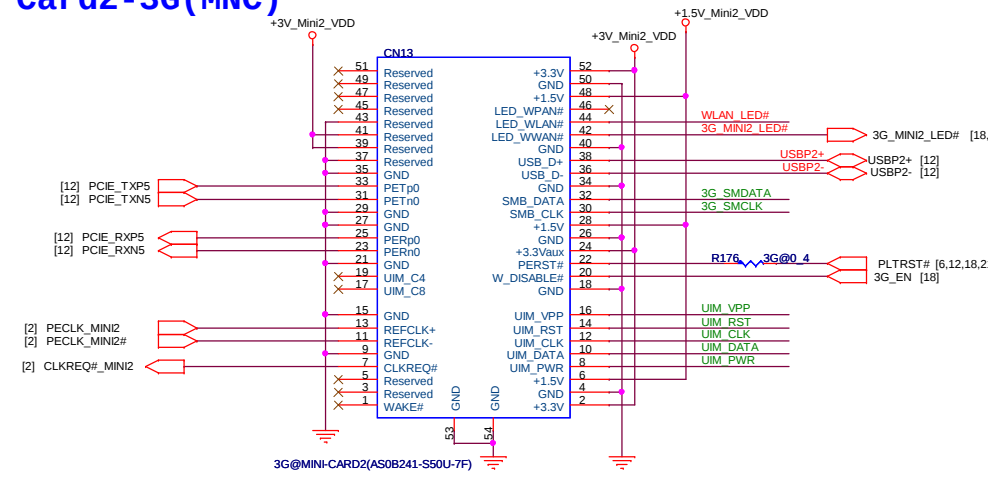
Title **EC WPCE775LA0DG**

Size	Document Number		
	ZH8		
Date:	Saturday, June 27, 2009	Sheet	18 of 31

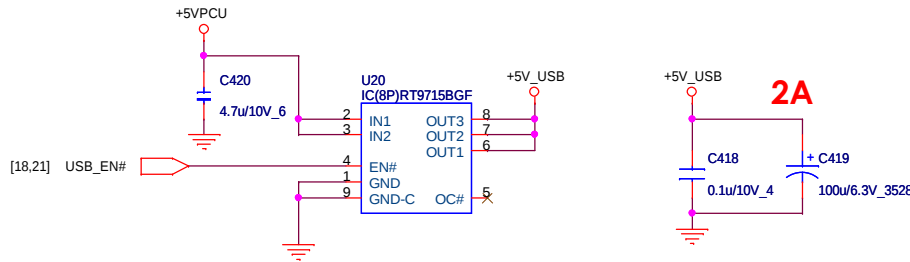
Mini Card1-WLAN/WMAX(MPC)



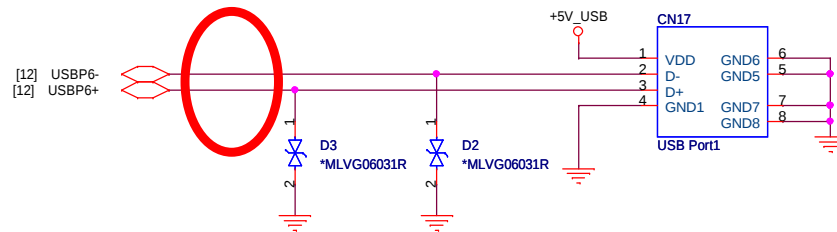
Mini Card2-3G(MNC)



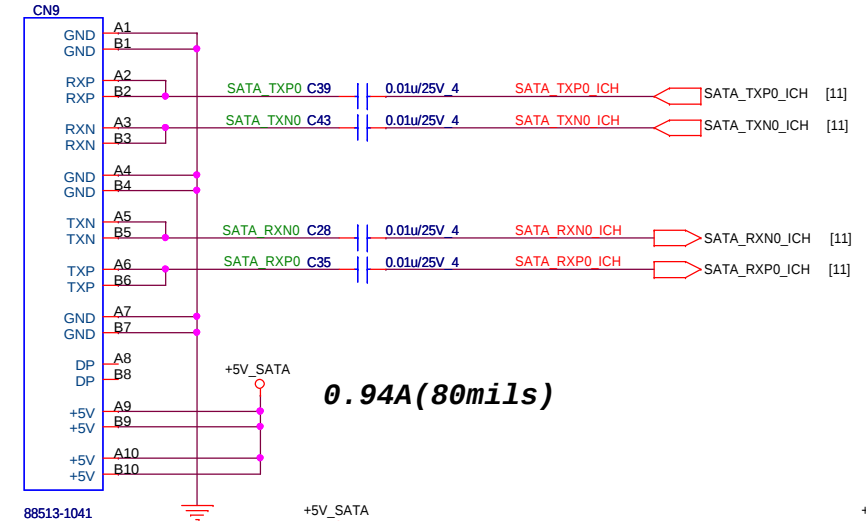
MB USB (USB)



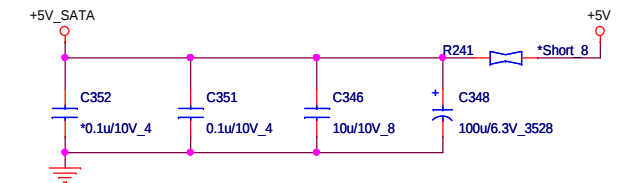
Remove R6、R7、L2



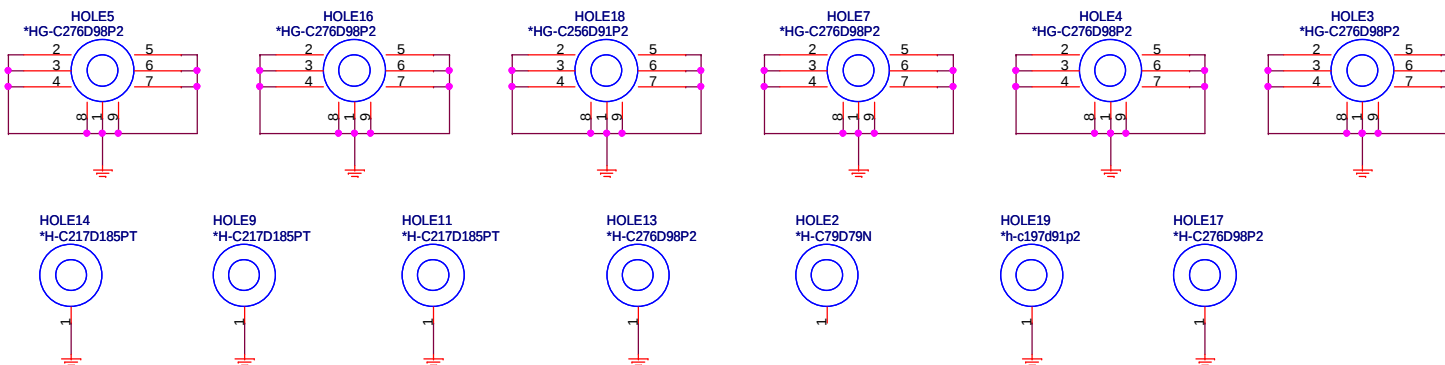
2.5" SATA HDD(HDD)



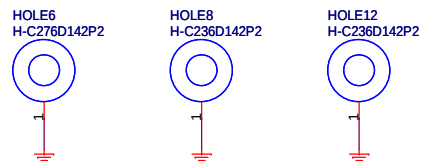
0.94A(80mils)



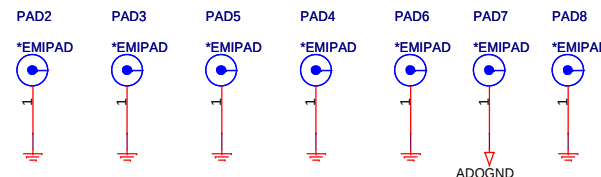
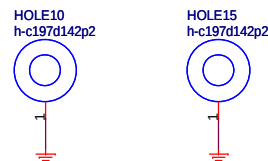
HOLE (EXC)



FAN nut

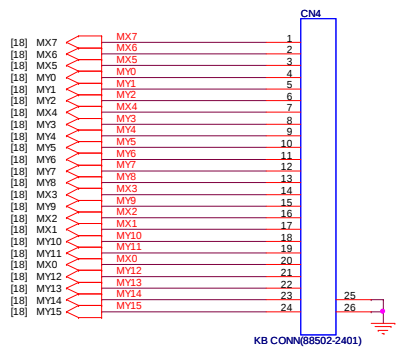


Minipci nut

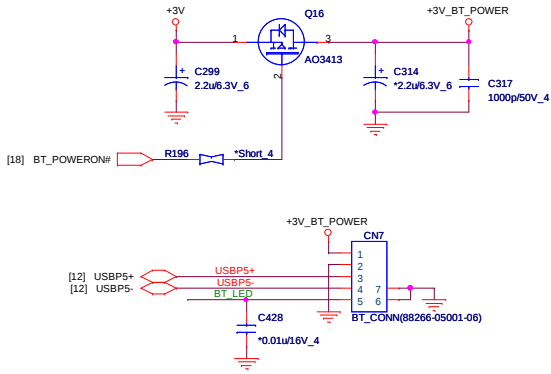


Title		
USB/HDD/HOLE		
Size	Document Number	Rev
	ZH8	0C
Date:	Saturday, June 27, 2009	Sheet 20 of 31

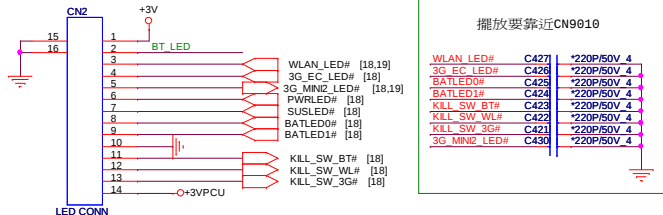
Keyboard(KBC)



BuleTooth (BTM)

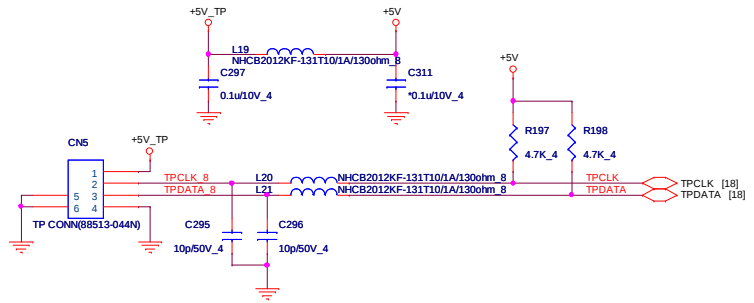


LED D/B (UIF)

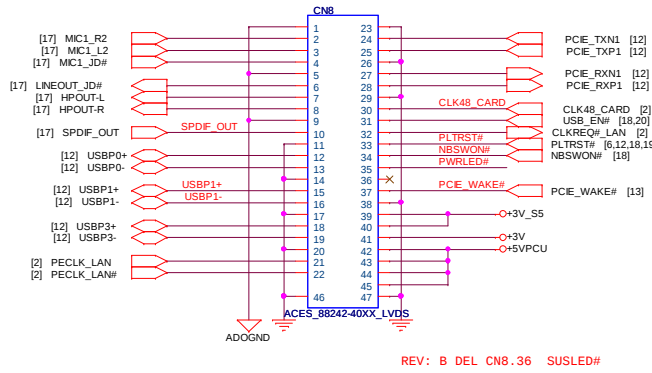


Check P/N footprint

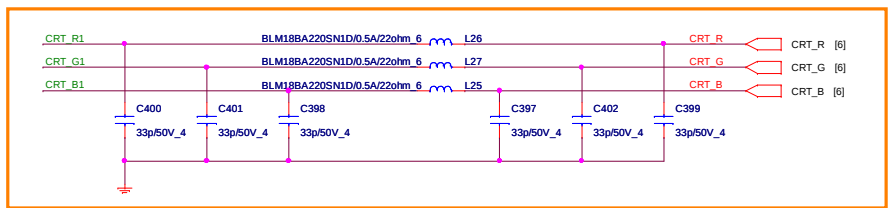
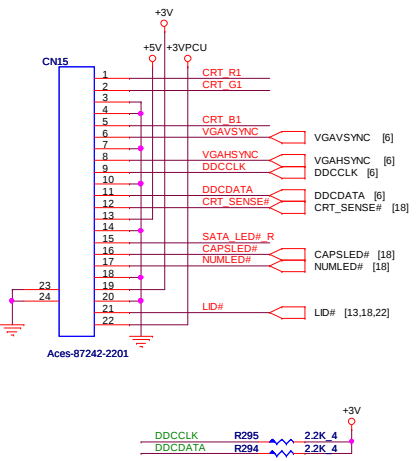
Touch Pad D/B (TPD)



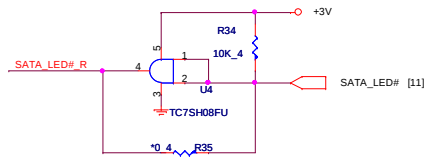
Card Reader/USB DB
CONNECTER(MMC)/Power Connector



CRT D/B (UIF)



For EMI



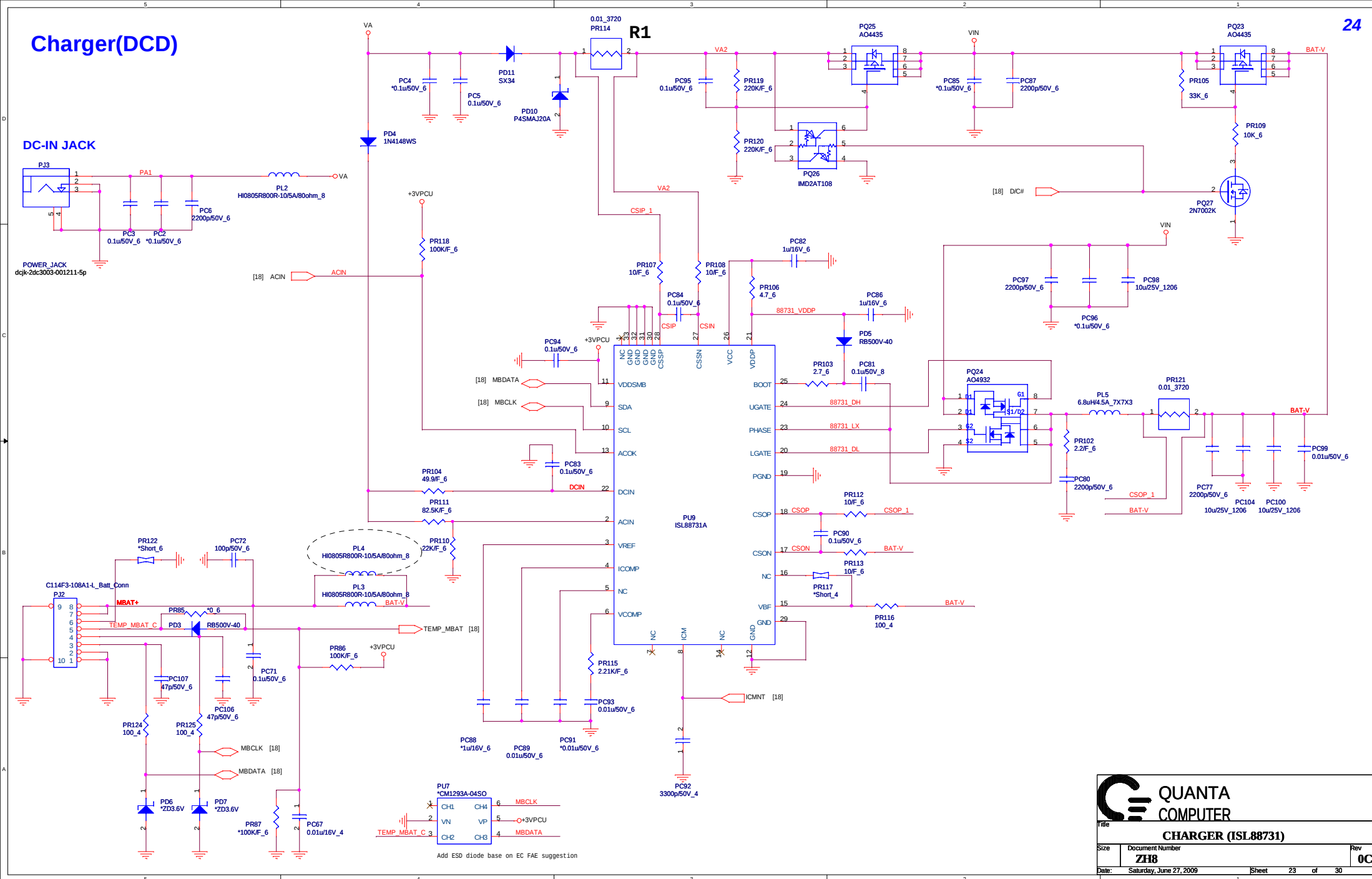
QUANTA
COMPUTER

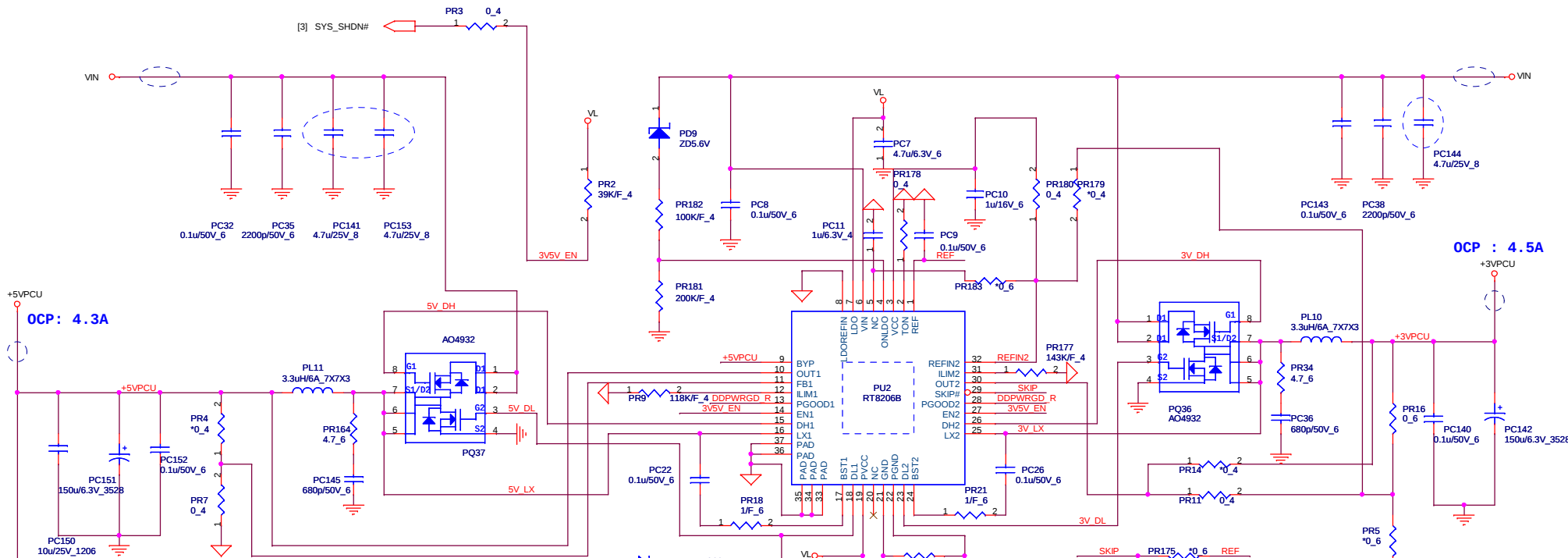
Title: **KB/BT/PR/TP/LAN/LED/CR Connects**

Size	Document Number	Rev
	ZH8	0C

Date: **Saturday, June 27, 2009** Sheet **21** of **31**

Charger(DCD)



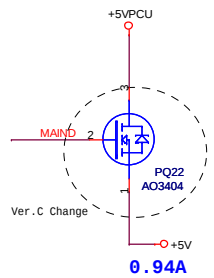


OCP: 4.3A

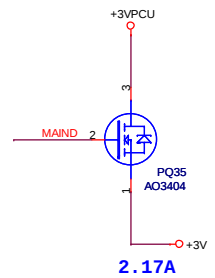
OCP: 4.5A

AO4932 Rds=15.8~19.6mOhm
 +5VPCU OCP:4.3A 400K
 $L(\text{ripple current}) = (19-5) * 5 / (3.3u * 400k * 19) \sim 2.791A$
 $I_{ocp} = 4.3 - (2.791/2) \sim 2.9045A$
 $V_{th} = 2.9045A * 19.6mOhm = 56.9282mV$
 $R(I_{lim}) = (56.9282mV * 10) / 5uA \sim 113.8K = 118K$

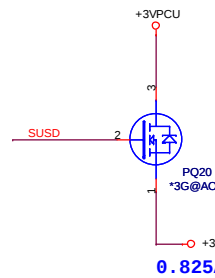
AO4932 Rds=15.8~19.6mOhm
 +3VPCU OCP:4.5A 500K
 $L(\text{ripple current}) = (19-3.3) * 3.3 / (3.3u * 500k * 19) \sim 1.653A$
 $I_{ocp} = 4.5 - (1.653/2) \sim 3.6735A$
 $V_{th} = 3.6735A * 19.6mOhm = 72mV$
 $R(I_{lim}) = (72mV * 10) / 5uA \sim 144K = 143K$



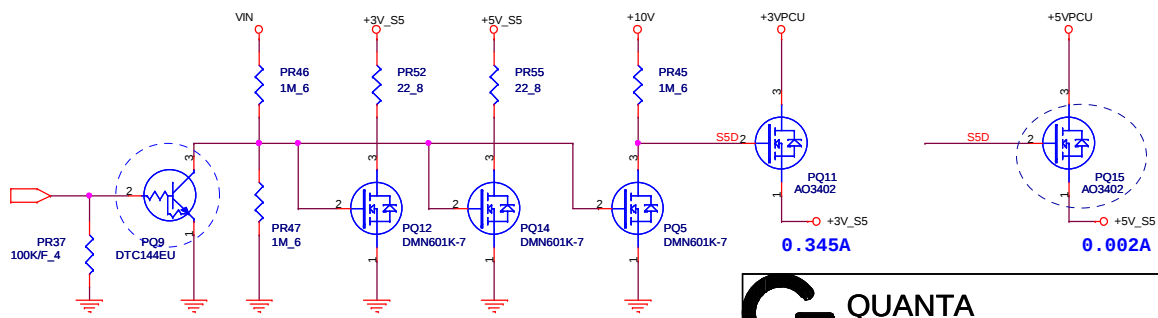
0.94A



2.17A



0.825A



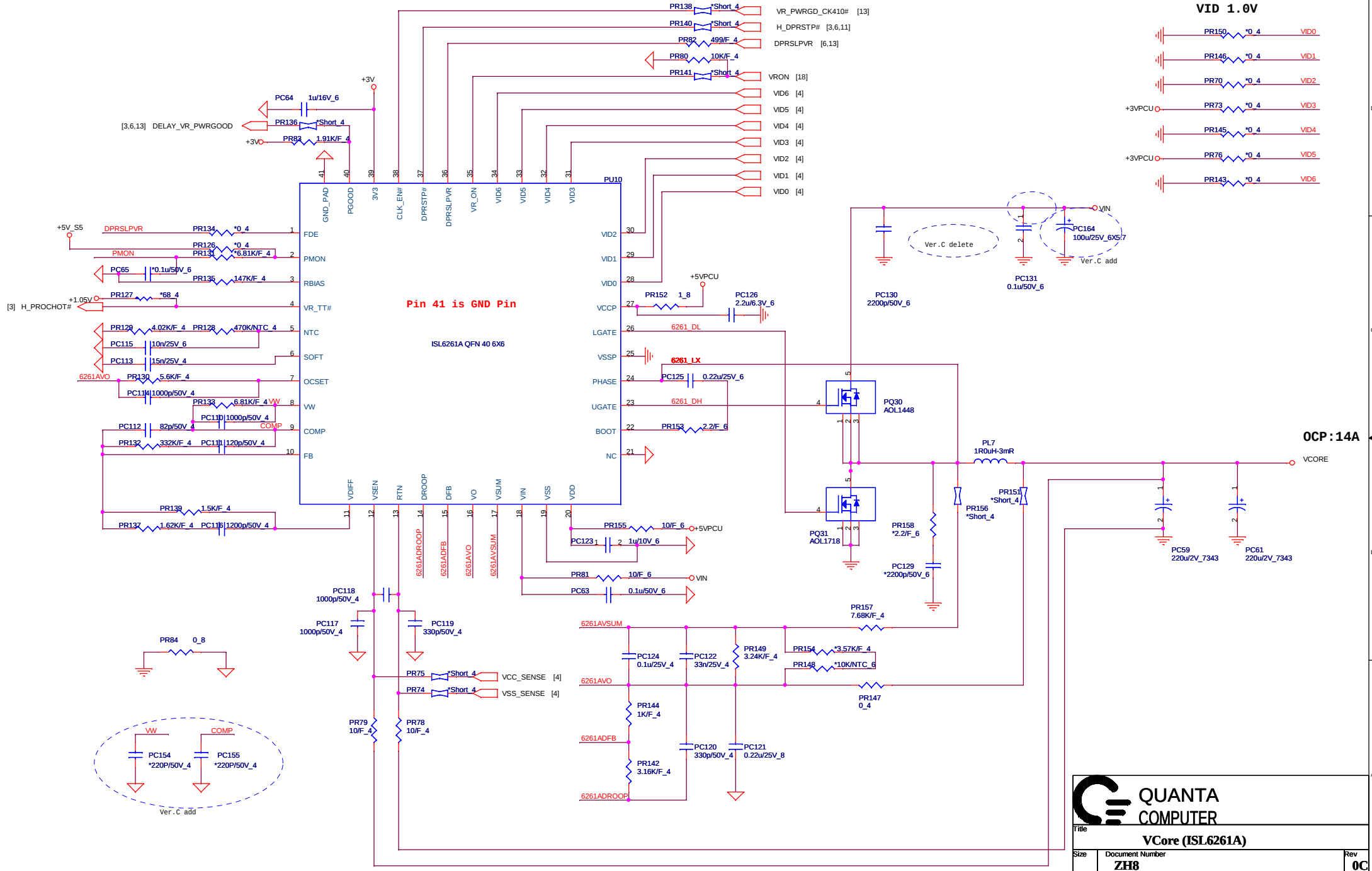
0.345A

QUANTA COMPUTER

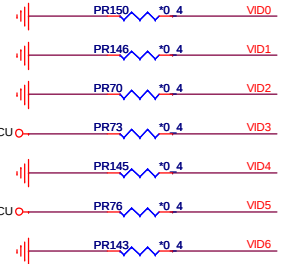
Title: **SYSTEM 5V/3V (RT8206B)**

Size: **ZH8** Document Number: **Rev 0C**

Date: **Saturday, June 27, 2009** Sheet: **24** of **30**



VID 1.0V



OCP:14A



QUANTA
COMPUTER

Title

VCore (ISL6261A)

Size

Document Number

Rev

ZH8

0C

Date

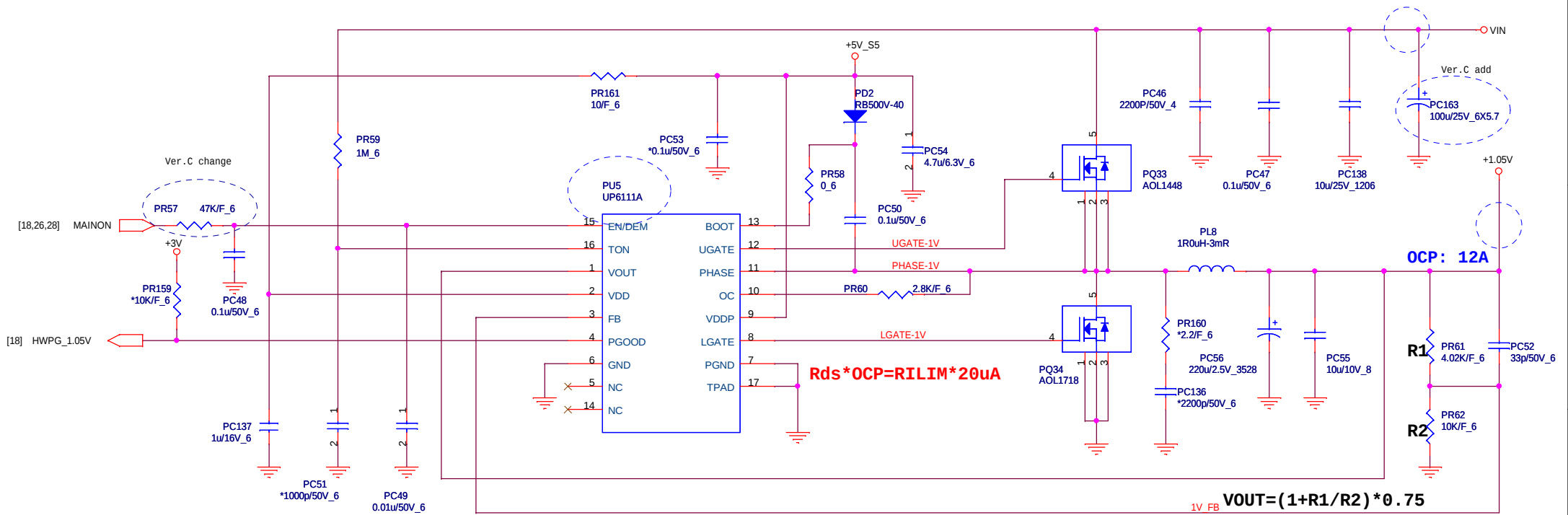
Saturday, June 27, 2009

Sheet

25

of

30



$$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * T_{ON})$$

$$T_{ON} = 3.85p * 1M * 1 / (V_{in} - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

$$AOL1412 \quad R_{dson} = 4.6m\Omega$$

$$OCP = 16 - 0.8A$$

$$L(\text{ripple current}) = (19 - 1.05) * 1.05 / (1\mu * 272k * 19) \sim 3.646A$$

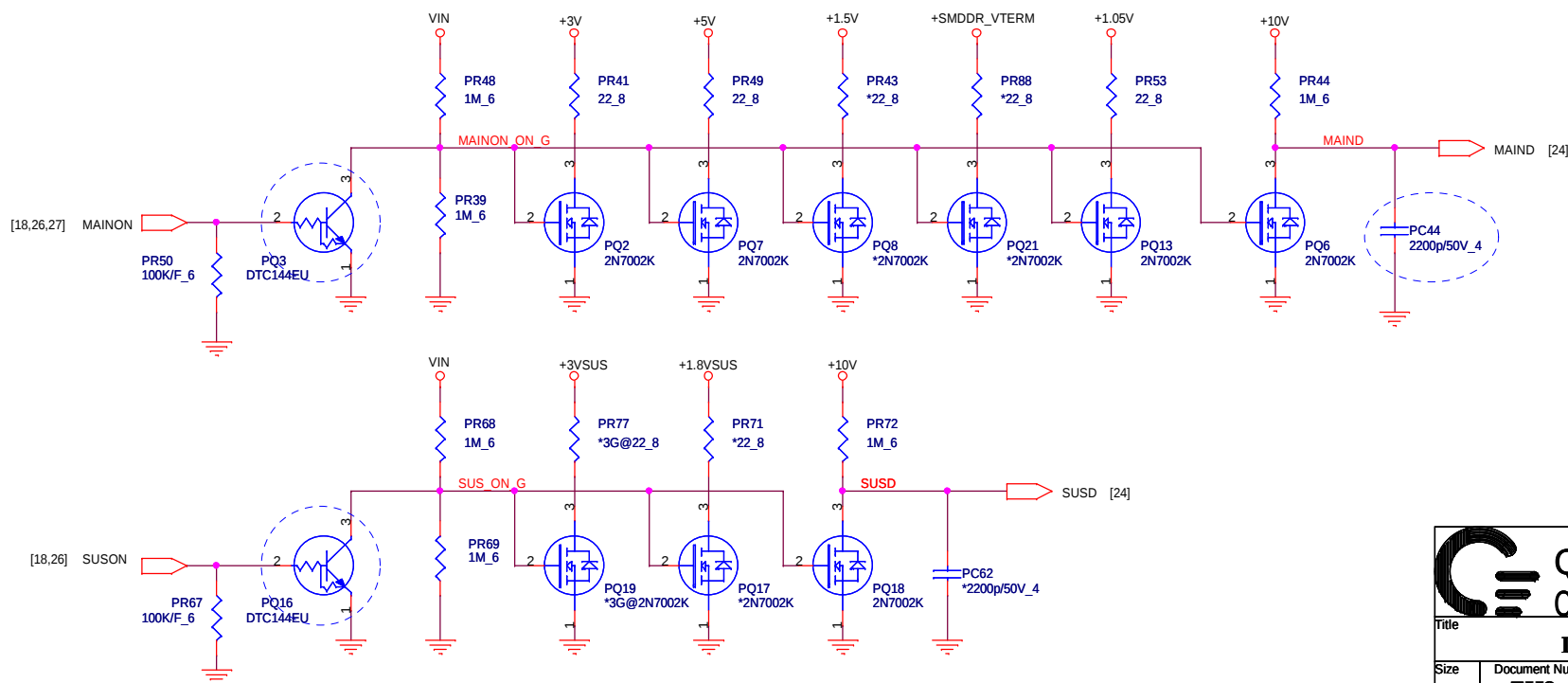
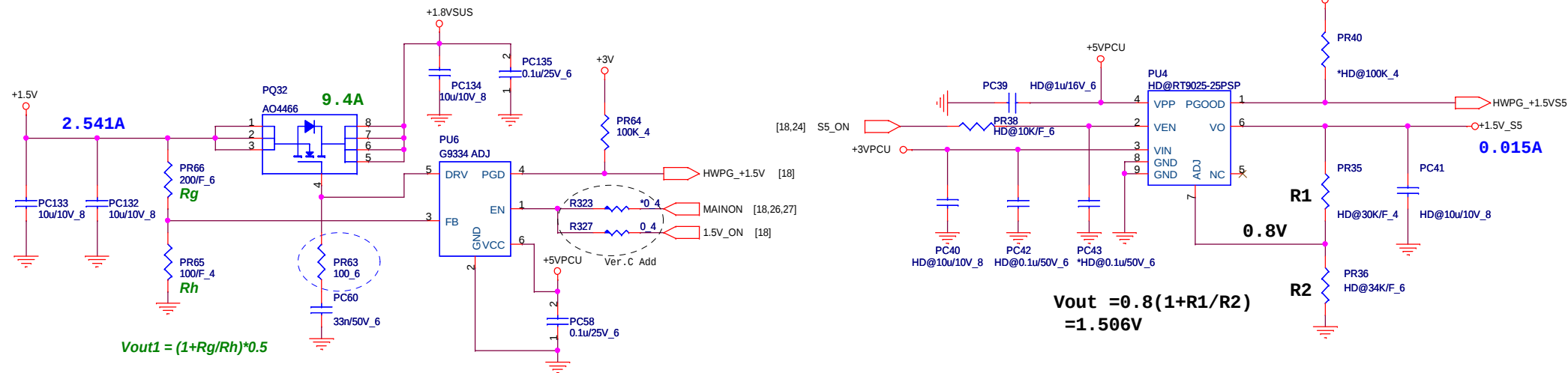
$$4.6m * 12 = R_{ILIM} * 20\mu A$$

$$R_{ILIM} = 2.76K \text{ --- } 2.8K$$

		QUANTA COMPUTER	
		Title	
Size		Document Number	
Date:		Rev	
Saturday, June 27, 2009		ZH8	
Sheet		of	
1		27 30	
		OC	

Discharger/1.5V(DCD)

29



 QUANTA COMPUTER		
Title: Discharge/1.5V		
Size:	Document Number: ZH8	Rev: 0C
Date:	Saturday, June 27, 2009	Sheet 28 of 30

[illegible]

EC GPIO Setting

Pin Name	Net Name	Setting	Description
GPIO1	ACIN	GPI	EC Detect AC Adapter State
GPIO3	NBSWON#	GPI	Pwr switch in
GPIO4/AD5		GPI	No used
GPIO5/AD4		GPI	No used
GPIO6	LID#	GPI	Reserved for Lid function
GPIO7	SUSB#	GPI	S.B sleep S3 pin
GPIO10/LPCPD#		GPI	No used
GPIO11/CLKRUN#	CLKRUN#	O	Clock Run
GPIO12/PSDA13	KILL_SW_BT#	GPI	Detect bulb tooth enable/disable
GPIO13/C_PWM	PWRL LED#	O	Power on LED drive
GPIO14/TB1	FANSIG	GPI	To detect FAN speed
GPIO15/A_PWM	CONTRAST	O	EC PWM for Panel Brightness
GPIO16/CIRTX		GPI	No used
GPIO17/SC1	MBCLK	O	SMBus Clock for M/B
GPIO20/TA2		GPI	No used
GPIO21/B_PWM	NUMLED#	O	Number Lock LED drive
GPIO22/SDA1	MBDATA	I/O	SMBus Data for M/B
GPIO23/SC13	3ND_MBCLK	O	SMBus Clock for acer ID flash
GPIO24/LDRQ#	EC_FPBACK#	GPO	Panel back light control
GPIO25/PSCLK3	MAINON	GPO	Turn On/Off main power
GPIO26/PSCLK2		GPI	No used
GPIO27/PSDA12	BT_POWERON#	GPO	Turn On/Off hule tooth power
GPIO30/CIRTX2		GPI	No used
GPIO31/SDA3	3ND_MBDATA	I/O	SMBus Data for acer ID flash
GPIO32/D_PWM	BATLED0#	GPO	Battery status LED drive
GPIO33/B_PWM	BATLED1#	GPO	Battery status LED drive
GPIO34/CIRRX1		GPI	No used
GPIO35/PSDAT1	TPDATA	O	PS/2 data for touch pad
GPIO36/TB3	VRON	GPO	Turn On/Off CPU Power
GPIO37/PSCLK1	TPCLK	O	PS/2 clock for touch pad
GPIO40/F_PWM	SUSLED	GPO	S3 state LED drive
GPIO41	3G_WAKEUP	S5	3G wake up
GPIO42/TC		GPI	No used
GPIO43/TMS	AMP_MUTE#	GPO	Turn On/Off Audio Amplifier
GPIO44/TDI		GPI	No used
GPIO45/E_PWM	CPUEAN#	O	EC PWM for Fan Module
GPIO46/cirrxm/trst#	3G_WAKE_1	GPI	3G wake up
GPIO47/SC14		GPI	No used
GPIO50/TDO	D/C#	GPO	Battery charge / discharge control
GPIO51/TA3	S5_ON	GPO	Turn On/Off S5 Power plane
GPIO52/cirtx2/trdy#	PCIE_WAKE#_EC	GPI	No used
GPIO53/SDA4	EC_SC1#	O	EC SCI
GPIO54/EC_SC1#	ECDB_CLOCK	GPI	No used
GPIO55/CLKOUT	ECDB_CLOCK	GPI	No used
GPIO56/TA1		GPI	No used
GPIO57/KBSOUT17	KILL_SW_WL#	GPI	Detect mini card 1 (WLAN) enable/disable
GPIO60/KBSOUT16	KILL_SW_3G#	GPI	Detect mini card 2 (3G) enable/disable
GPIO61/KBSOUT15	MY15	O	Keyboard scan output
GPIO62/KBSOUT14	MY14	O	Keyboard scan output
GPIO63/KBSOUT13	MY13	O	Keyboard scan output
GPIO64/KBSOUT12	MY12	O	Keyboard scan output
GPIO65/SM1#	EC_SMI#	O	EC SMI
GPIO66/G_PWM	CAPSLED#	O	Caps Lock LED drive
GPIO67/PWUREQ	USB_EN#	GPO	USB power enable/disable
GPIO70/IRRX2_IRSL0	SUSC#	GPI	S.B sleep S4 pin
GPIO71/IRTX/SOUT2	PWROK_EC	GPO	System Power Good for PCI Reset
GPIO72/IRRX1/SIN2	EC_RSMRST#	GPO	S.B Resume Power Reset
GPIO73/SC12	2ND_MBCLK	O	SMBus Clock for CPU thermal
GPIO74/SDA2	2ND_MBDATA	I/O	SMBus Data for CPU thermal
GPIO75/SPI_SCK	PCI_RESET	GPO	PL TRS1# enable/disable for mini card 2
GPIO76/SPI_DO/SHBM	3G_EN	GPO	Mini card 2 (3G) enable/disable
GPIO77/SPI_DI	CRT_SENSE#	GPI	To detect CRT
GPI081	DNBSWON#	GPO	S.B Power button Event
GPIO82/TRIS#		GPI	No used
GPIO83/SOUT_CR/BADDR1	uR_SOUT_CR	GPI	No used (Address Setting)
GPIO84/BADDR0	BADDR0	GPI	No used (Address Setting)
GPIO87/CIRRRXM/SIN_CR	RE_EN	GPO	Mini card 1 (WLAN) enable/disable
GPIO90/AD0	TEMP_MBAT	I	EC detect battery state
GPIO91/AD1		GPI	No used
GPIO92/AD2	TPD_TRIP	GPI	No used
GPIO93/AD3	ICMNT	GPI	EC detect system current in AC mode
GPIO94/DA0		GPI	No used
GPIO95/DA1		GPI	No used
GPIO96/DA2		GPI	No used
GPIO97/DA3		GPI	No used

ICH9M GPIO Setting

Pin Name	Power	ICH9M Default	Net Name	Description	Setting	Internal PU/PD	External PU/PD
GPIO0/PMSYNC#	Core	GPI	PM_SYNC#	Power Management Sync	O		
GPIO1	Core	GPI	EC_SMI#	EC SMI	GPI		PU 10KΩ to +3V
GPIO2/PIRQ#	Core	GPI	INT#	No used	GPI		PU 10KΩ to +3V
GPIO3/PIRQ#	Core	GPI	INT#	No used	GPI		PU 10KΩ to +3V
GPIO4/PIRQ#	Core	GPI	INTG#	No used	GPI		PU 10KΩ to +3V
GPIO5/PIRQH#	Core	GPI	INTH#	No used	GPI		PU 10KΩ to +3V
GPIO6	Core	GPI	LID#_ICH	Lid function	GPI		PU 10KΩ to +3V
GPIO7	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO8	GPI	EC_SC1#		EC SCI Interrupt	GPI		PU 10KΩ to +3V S5
GPIO9/WOL_EN	S5	Native	ICH_GPIO9	No used	GPI		PU 10KΩ to +3V S5
GPIO10/SUS_PWR_ACK	S5	GPI	ICH_GPIO10	No used	GPI		PU 10KΩ to +3V S5
GPIO11/SMBALERT#	S5	Native	ICH_GPIO11	No used	GPI		PU 10KΩ to +3V S5
GPIO12/LAN_PHY_PWR_CTRL	S5	GPO	ICH_GPIO12	No used	GPI		PU 10KΩ to +3V S5
GPIO13	S5	GPI	ICH_GPIO13	No used	GPI		PU 10KΩ to +3V S5
GPIO14/AC_PRESENT	S5	GPI	ICH_GPIO14	No used	GPI		PU 10KΩ to +3V S5
GPIO15/STP_PC1#	S5	Native	PM_STPPC1#	Stop PCI Clock	O		
GPIO16/DPRS1PVR	Core	Native	DPRS1PVR	Deeper Sleep-Voltage Regulator	O	PD 20KΩ	
GPIO17	Core	GPO	BORAD_ID0	M/B ID Setting	GPI		Pu or PD 10KΩ
GPIO18	Core	GPO	BORAD_ID1	M/B ID Setting	GPI		Pu or PD 10KΩ
GPIO19/SATA1GP	Core	GPI	ICH_GPIO19	No used	GPI		PU 10KΩ to +3V
GPIO20	Core	GPI		No used	GPO	PD 20KΩ	
GPIO21/SATA0GP	Core	GPO	BORAD_ID2	M/B ID Setting	GPI		Pu or PD 10KΩ
GPIO22/SCLOCK	Core	GPI	BORAD_ID3	M/B ID Setting	GPI		Pu or PD 10KΩ
GPIO23/LDRQ1#	Core	Native		No used	GPI	PU 20KΩ	
GPIO24/MEM1LED	S5	GPO		No used	GPO		
GPIO25/STP_CPU#	S5	Native	PM_STPCPU#	Stop CPU Clock	O		
GPIO26/S4_STATE#	S5	Native		No used	GPI		
GPIO27	S5	GPO		No used	GPO		
GPIO28	S5	GPO		No used	GPO		
GPIO29/OC5#	S5	Native	USBOC5#	No used	GPI		PU 10KΩ to +3V S5
GPIO30/OC6#	S5	Native	USBOC6#	No used	GPI		PU 10KΩ to +3V S5
GPIO31/OC7#	S5	Native	USBOC7#	No used	GPI		PU 10KΩ to +3V S5
GPIO32/CLKRUN#	Core	GPO	CLKRUN#	PCI Clock Run	I		PU 8.2KΩ to +3V
GPIO33/HDA_DOCK_EN#	Core	GPO		No used	GPO	PU 20KΩ	
GPIO34/HDA_DOCK_RST#	Core	GPO		No used	GPO		
GPIO35/SATACLKREQ#	Core	GPO	CLKREQ#_SATA	SATA Clock Request	O		PU 10KΩ to +3V
GPIO36/SATA0GP	Core	GPI	ICH_GPIO36	No used	GPI		PU 10KΩ to +3V
GPIO37/SATA5GP	Core	GPI	ICH_GPIO37	No used	GPI		PU 10KΩ to +3V
GPIO38/SLOAD	Core	GPI	ICH_GPIO38	No used	GPI		PD 10KΩ to GND
GPIO39/SDATAOUT0	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO40/OC1#	S5	Native	USBOC1#	No used	GPI		PU 10KΩ to +3V S5
GPIO41/OC2#	S5	Native	USBOC2#	No used	GPI		PU 10KΩ to +3V S5
GPIO42/OC3#	S5	Native	USBOC3#	No used	GPI		PU 10KΩ to +3V S5
GPIO43/OC4#	S5	Native	USBOC4#	No used	GPI		PU 10KΩ to +3V S5
GPIO44/OCB#	S5	Native	USBOC8#	No used	GPI		PU 10KΩ to +3V S5
GPIO45/OC9#	S5	Native	USBOC9#	No used	GPI		PU 10KΩ to +3V S5
GPIO46/OC10#	S5	Native	USBOC10#	No used	GPI		PU 10KΩ to +3V S5
GPIO47/OC11#	S5	Native	USBOC11#	No used	GPI		PU 10KΩ to +3V S5
GPIO48/SDATAOUT1	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO49	Core	GPO	DMI_TERM_SEL	No used	GPO	PU 20KΩ	
GPIO50/REQ1#	Core	Native	REQ1#	No used	GPI		PU 10KΩ to +3V
GPIO51/GNT1#	Core	Native		No used	GPI	PU 20KΩ	
GPIO52/REQ2#	Core	Native	REQ2#	No used	GPI		PU 10KΩ to +3V
GPIO53/GNT2#	Core	Native		No used	GPI	PU 20KΩ	
GPIO54/REQ3#	Core	Native	REQ3#	No used	GPI		PU 10KΩ to +3V
GPIO55/GNT3#	Core	Native		No used	GPI	PU 20KΩ	
GPIO56	S5	GPI	ICH_GPIO56	No used	GPI		PU 10KΩ to +3V S5
GPIO57	S5	GPI	ICH_GPIO57	No used	GPI		PD 100KΩ to GND
GPIO58/SPI_CS1#	S5	GPI	SPI_CS1#	No used	GPI	PU 20KΩ	
GPIO59/OC0#	S5	Native	USBOC0#	No used	GPI		PU 10KΩ to +3V S5
GPIO60/LINKALERT#	S5	Native	ICH_GPIO60	No used	GPI		PU 10KΩ to +3V S5

CK505 Clock Setting Table

Pin Name	Pin	Net Name	Description
CPU_0	61	CLK_CPU_BCLK	Differential CPU clock
CPU_0#	60	CLK_CPU_BCLK#	
CPU_1	58	CLK_MCH_BCLK	Differential NB GS45 clock
CPU_1#	57	CLK_MCH_BCLK#	

PCI Express Clock

Pin Name	Pin	Net Name	Description
SRC0/DOTR6	20	DREFCLK	96MHz DOT clock for NB GS45
SRC0#D0TR6#	21	DREFCLK#	
LCDCCLK/27M	24	DREFSSCLK#	Clock output for NB GS45 graphic controller
LCDCCLK#/27M_SS	25	DREFSSCLK#	
SRC2	28	PECLK_SATA	Differential Serial Reference Clock for SB ICH9M SATA
SRC2#	29	PECLK_SATA#	
SRC3#CR#_C	31	PECLK_ICH	Differential Serial Reference Clock for SB ICH9M
SRC3#CR#_D	32	PECLK_ICH#	
SRC4	34	PECLK_LAN	Differential Serial Reference Clock for on board LAN
SRC4#	35	PECLK_LAN#	
SRC6	48	PECLK_MINI2	Differential Serial Reference Clock for Mini Card 2
SRC6#	47	PECLK_MINI2#	
SRC7#CR#_E	51		No use
SRC8#CPU_ITP	54	CLKREQ#_MINI2	Clock Request for Mini Card 2 (SRC6)
SRC8#CPU_ITP#	53		No use
SRC9	37	PECLK_MINI1	Differential Serial Reference Clock for MINI CARD 1
SRC9#	38	PECLK_MINI1#	
SRC10	41	PECLK_3GPL#	Differential Serial Reference Clock for NB GS45
SRC10#	42	PECLK_3GPL#	
SRC11#CR#_H	40	CLKREQ#_MCH	Clock Request for NB GS45 (SRC10)
SRC11#CR#_G	39	CLKREQ#_MINI1	Clock Request for Mini Card 1 (SRC9)

PCI Clock

Pin Name	Pin	Net Name	Description
PCI0#CR#_A	8	CLKREQ#_SATA	Clock Request for SATA (SRC2)
PCI1#CR#_B	10	CLKREQ#_LAN	Clock Request for on board LAN (SRC4)
PCI2	11	PCLK_DEBUG	PCI clock for debug card
PCI3	12		No use
PCI4	13	PCLK_EC	PCI clock for EC
PCI5	14	PCLK_ICH	PCI clock for SB ICH9M

Other Clock

Pin Name	Pin	Net Name	Description
USB_4B	17	CLK4B_ICH	48MHz for SB ICH9M
REF	5	CLK14_ICH	14.318MHz for SB ICH9M

Clock Request Table		
CLKREQ#	MAPPING	Control
CR#_A	SRC0	SRC2
CR#_B	SRC0	SRC4
CR#_C	SRC0	SRC2
CR#_D	LCDCCLK	SRC4
CR#_E		SRC6
CR#_F		SRC8
CR#_G		SRC9
CR#_H		SRC10



QUANTA
COMPUTER

Title		Schematic Setting	
Size	Document Number	Rev	
	ZH8	0C	
Date:	Saturday, June 27, 2009	Sheet	31 of 31