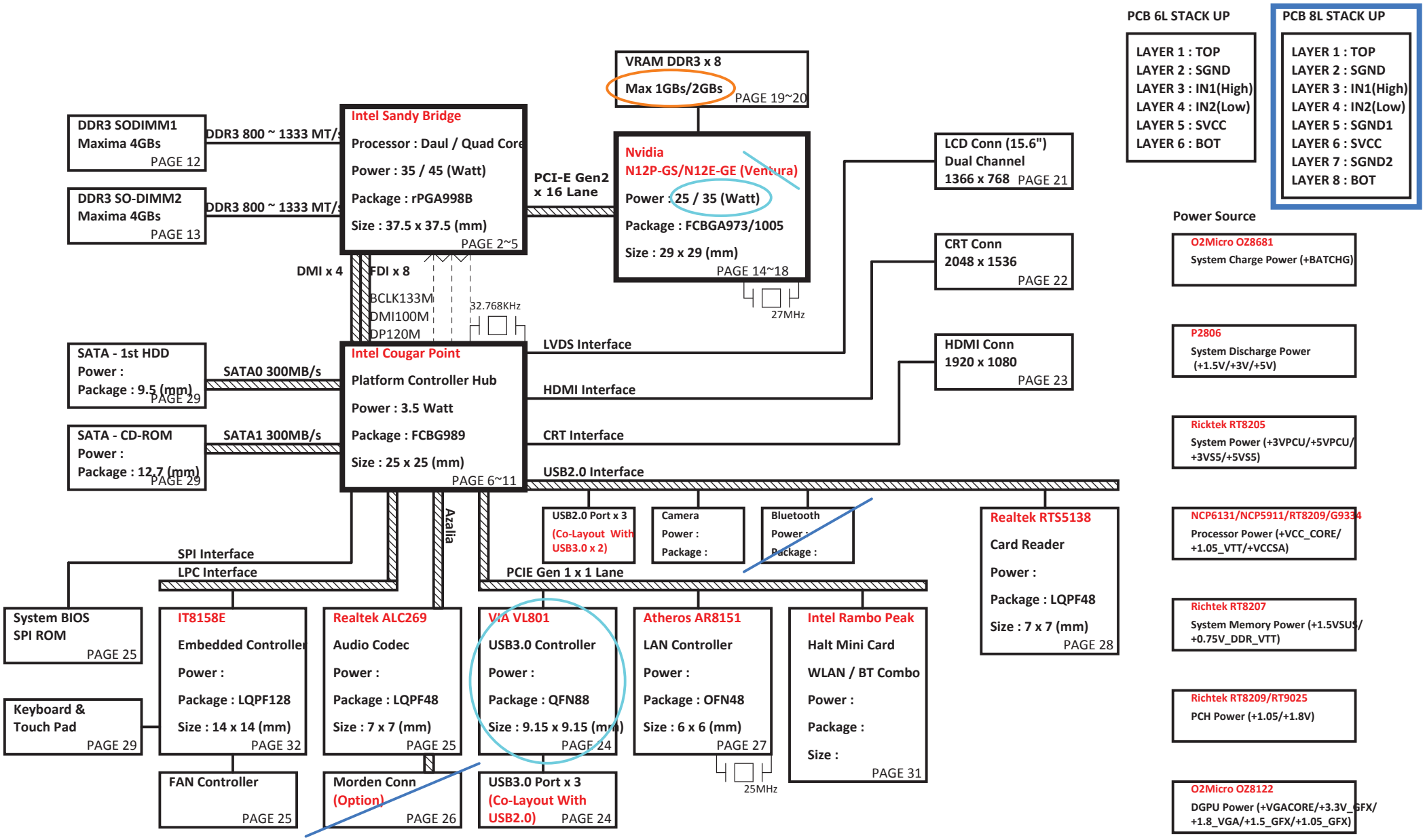
TWH (15.6") Intel Huron River Platform Block Diagram 01



NB5	PROJECT : TWH Quanta Computer Inc.	
Size A3	Document Number Block Diagram	Rev A
Date: Monday, November 15, 2010	Sheet 1 of 40	

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

02

U15A

DMI

Intel(R) FDI

eDP

PCI EXPRESS* - GRAPHICS

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

SNB_IVB# N.A at SNB EDS #27637 0.7v1

Placement close to EC.

9/9 add for PDG update

11/12 short

8/31 reserved for "boot hang 47" issue

3/26 DB del for DG update.

CPU RESET#

8/26 A-->B modify

U15B

MISC

THERMAL

PWR MANAGEMENT

CLOCKS

DDR3 MISC

JTAG & BPM

3/26 DB for H/W modify.

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

CPU XDP

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

DDR3 DRAM RESET

11/12 short

SM_DRAMPWROK Processor Input.

3/26 DB del for DG update.

10/11 change

8/31 change to 0 ohm

11/8 add

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

FDI disable (DIS only stuff)

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

Embedded Display PLL Clock

3/26 DB change Part reference.

	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

DP & PEG Compensation

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Processor 1/4 (Host/GPU)	A
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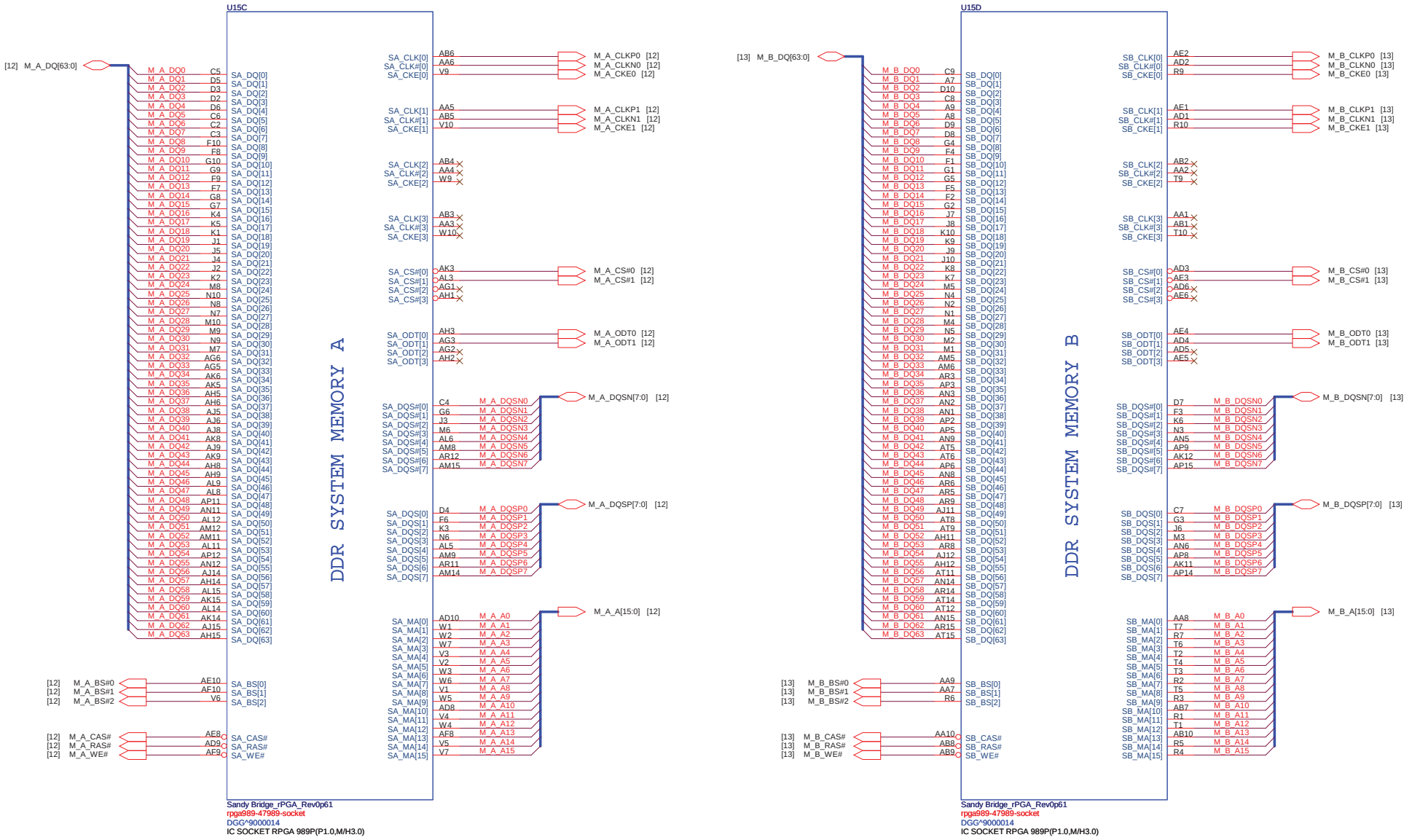
Sandy Bridge Processor (DDR3)



NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Processor 2/4 (Memory)	A

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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

04

9/4 all of these 22uF/6.3V capacitors are replaced by 10uF/6.3V in BOM

9/4 all of these 22uF/6.3V capacitors are replaced by 10uF/6.3V in BOM

SNB: 55A

+VCC_CORE

U15F

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

C48 22U/6.3VS_8 C473 22U/6.3VS_8 C127 22U/6.3VS_8
C108 22U/6.3VS_8 C92 22U/6.3VS_8 C58 22U/6.3VS_8
C51 22U/6.3VS_8 C28 22U/6.3VS_8 C178 22U/6.3VS_8
C206 22U/6.3VS_8 C165 22U/6.3VS_8 C49 22U/6.3VS_8
C125 22U/6.3VS_8 C477 *22U/6.3VS_8 C141 22U/6.3VS_8
C144 22U/6.3VS_8 C147 22U/6.3VS_8 C197 22U/6.3VS_8
C157 22U/6.3VS_8 C107 22U/6.3VS_8 C151 22U/6.3VS_8
C46 *22U/6.3VS_8 C467 *22U/6.3VS_8 C430 22U/6.3VS_8
C461 22U/6.3VS_8 C29 22U/6.3VS_8 C53 22U/6.3VS_8
C41 22U/6.3VS_8 C431 22U/6.3VS_8 C47 *22U/6.3VS_8

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

3/26 DB change 10U FP to 0805.

SNB: 8.5A

+1.05V_VTT

C135 22U/6.3VS_8 C137 22U/6.3VS_8 C450 22U/6.3VS_8
C179 22U/6.3VS_8 C138 22U/6.3VS_8 C209 22U/6.3VS_8
C136 *22U/6.3VS_8 C148 22U/6.3VS_8 C464 22U/6.3VS_8
C470 *22U/6.3VS_8 C142 *22U/6.3VS_8 C121 *22U/6.3VS_8
5/14 modify
C445 22U/6.3VS_8 C120 *22U/6.3VS_8 C198 *22U/6.3VS_8
C446 *22U/6.3VS_8 C454 22U/6.3VS_8 C158 *22U/6.3VS_8
C460 *22U/6.3VS_8 C457 22U/6.3VS_8 C101 22U/6.3VS_8

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

+1.05V_VTT_40 R66 *0_4/S

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

VCC_SENSE AJ35
VSS_SENSE AJ34
VCCIO_SENSE B10
VSSIO_SENSE A10

3/26 DB Modify.

R128 100_4 +VCC_CORE
VCC_SENSE [39]
VSS_SENSE [39]
R133 100_4
VCCP_SENSE [34]
VSSP_SENSE
TP53

Trace Route to Power IC area.

[2,10,12,13,32,33,38] +1.5VSUS
[2,10,27] +1.5V_CPU
[2,29,33,34,38,39] +1.05V_VTT
[33] +VCCSA
[39,40] +VCC_GFX
[39,40] +VCC_CORE

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX SNB: 21.5A

C472 22U/6.3V_8 C167 22U/6.3V_8
C193 22U/6.3V_8 C208 22U/6.3V_8
C192 22U/6.3V_8 C511 22U/6.3V_8
C207 22U/6.3V_8 C166 22U/6.3V_8
C512 22U/6.3V_8 C169 22U/6.3V_8
C168 22U/6.3V_8 C471 22U/6.3V_8

5/4: add C8260/ C8322

Ra R473 *0_4

	DIS	SG/UMA
Ra	Stuff	NC

+1.8V SNB: 1.5A

C42 10U/6.3V_8 C45 1U/6.3V_4 C44 1U/6.3V_4 C432 330U/2V_7343

330uF x1, 10uF_8 x1, 1uF_4 x2 Socket BOT edge.

3/26 DB change 10U FP to 0805.

U15G

GRAPHICS

1.8V RAIL

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34

3/26 DB Modify.

R136 100_4 +VCC_GFX
VCC_AXG_SENSE [39]
VSS_AXG_SENSE [39]
R138 100_4

VREF

SM_VREF AL1

+VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

R157 *0_8 DDR_VTTREF [12,13,32]
R165 100K_4
Q19 2N7002
MAIND
MAIND [36]

DDR3 -1.5V RAILS

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

11/13 C516 mount for S3 black screen issue
5/14 modify

SNB: 5A +1.5V_CPU

C134 10U/6.3V_6 C152 10U/6.3V_8 C204 10U/6.3V_6 C153 10U/6.3V_6
4/27: layout modify
330uF x1, 10uF_8 x6 Socket BOT edge.
C173 10U/6.3V_6 C213 10U/6.3V_6 C516 220U/6.3V_6X4.5ESR18

8/31 C516 FP changed from 330U_2.5V_5.0x5.9ESR10m to 220U/6.3V_6x4.5ESR18

3/26 DB change 10U FP to 0805.

SA RAIL

VCCSA1 M27
VCCSA2 M26
VCCSA3 J26
VCCSA4 J25
VCCSA5 J24
VCCSA6 H26
VCCSA7 H25
VCCSA8 H25

SNB: 6A +VCCSA

C447 10U/6.3V_8 C31 10U/6.3V_8 C97 10U/6.3V_8 C24 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

3/26 DB change 10U FP to 0805.

MISC

VCCSA_SENSE H23 VCCUSA_SENSE R388 *0_4/S short0402 VCCUSA_SENSE [33]

11/12 short

R392 10K_4
FC_C22 C22 H_FC_C22
VCCSA_VID1 C24
VCCSA_SEL [33]
R393 10K_4

5/11: Add for intel CRB

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

Place PU resistor close to VR

R124 *54.9/F_4 +1.05V_VTT
H_CPU_SVIDCLK
3/26 DB Modify.
VR_SVID_CLK [39]

SVID DATA

+1.05V_VTT +1.05V_VTT

Place PU resistor close to CPU

R121 130/F_4
R118 *130/F_4
Place PU resistor close to VR

H_CPU_SVIDDAT
3/26 DB Modify. 5/12: modify
VR_SVID_DATA [39]

SVID ALERT

Place PU resistor close to CPU

+1.05V_VTT R158 75_4
H_CPU_SVIDALRT# R166 43_4
3/26 DB Modify.
VR_SVID_ALERT# [39]

9/8 delete JP1

+1.5VSUS +1.5V_CPU +1.5VSUS

Q40 AON7410

C515 0.1U/10V_4
C517 0.1U/10V_4
C518 0.1U/10V_4
C514 0.1U/10V_4

3/26 DB add for Intel. Placement close to CPU.

R170 220_8
MAIND
C262 *470P/50V_4
Q20 2N7002
MAIN_ONG [2,36]
5/6: modify

CPU VDDQ

PROJECT : TWH
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Processor 3/4 (Power)	A
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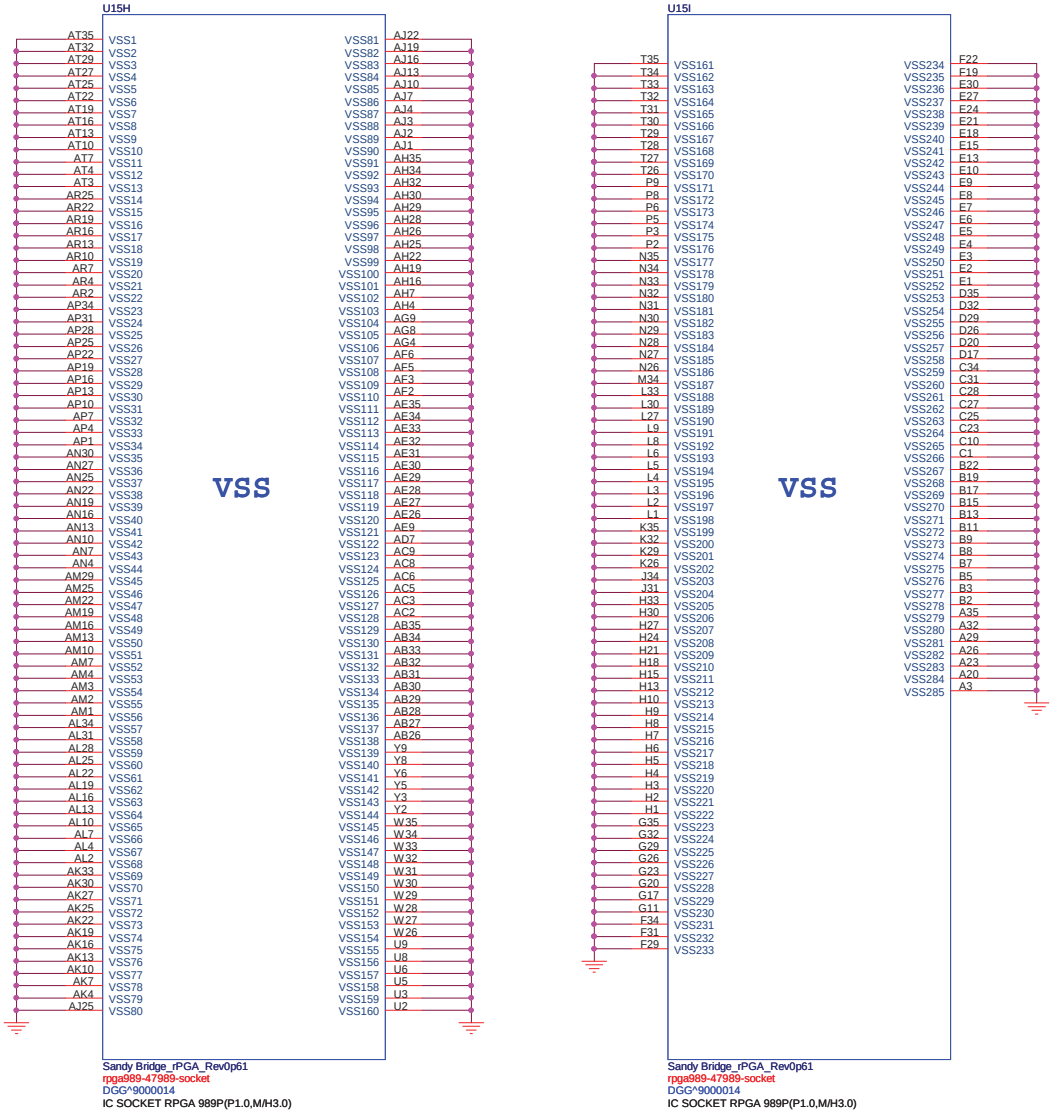
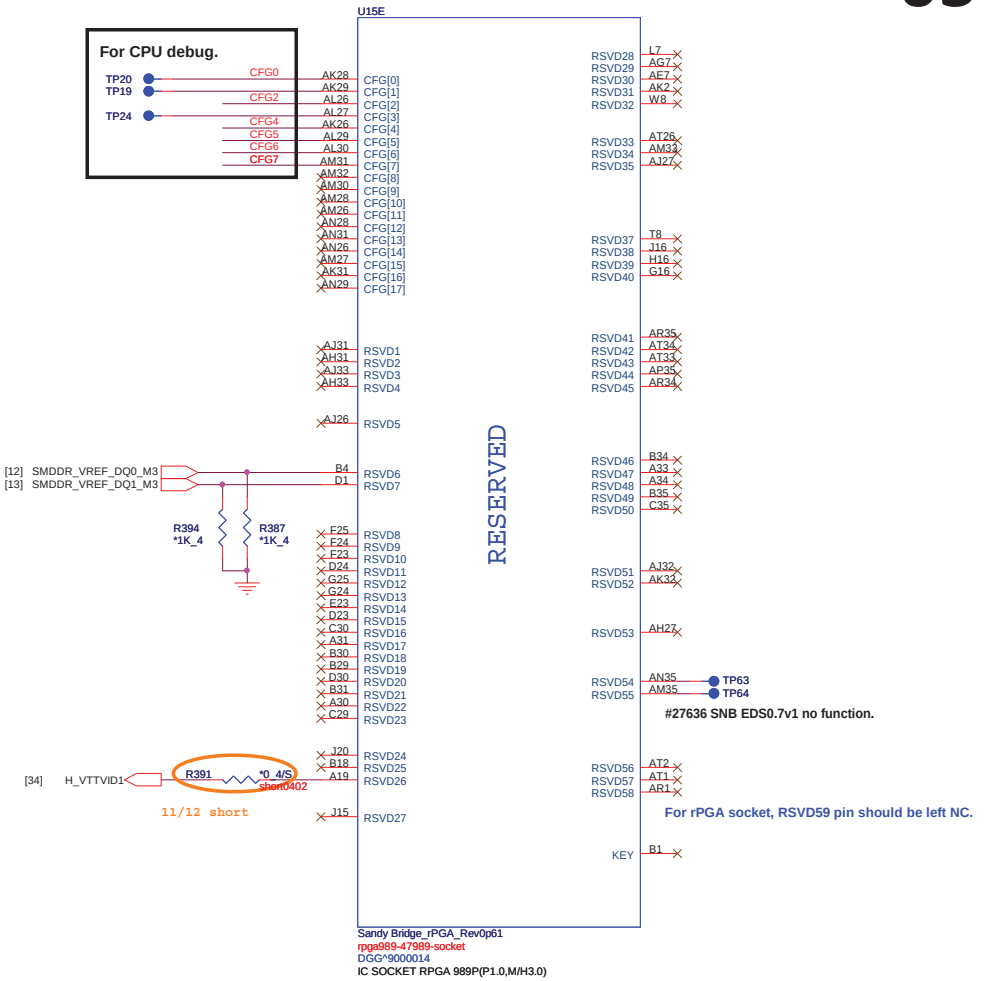
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

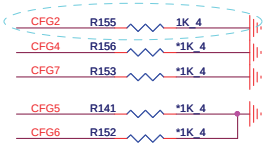


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

(hh) TWH PEG bus is Lane Reversed



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Processor 4/4 (Ground)	A

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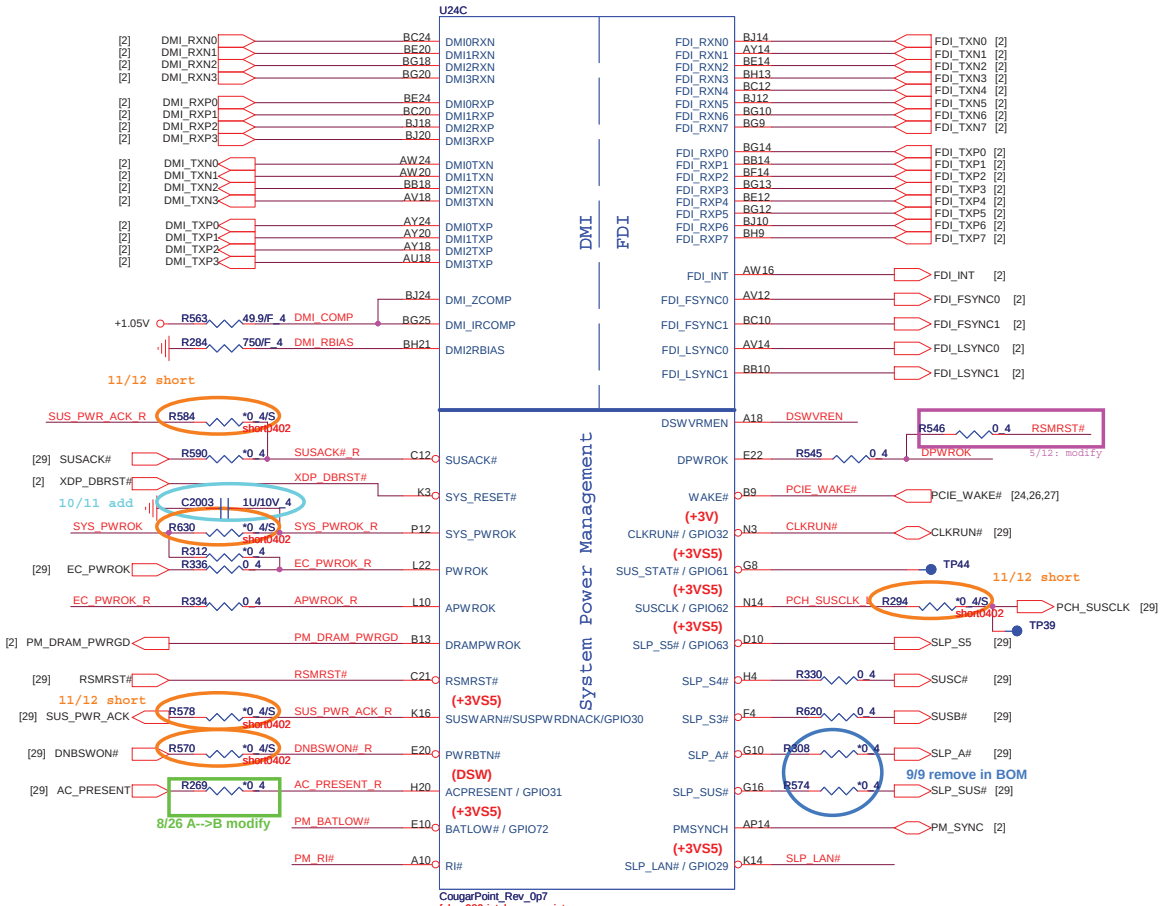
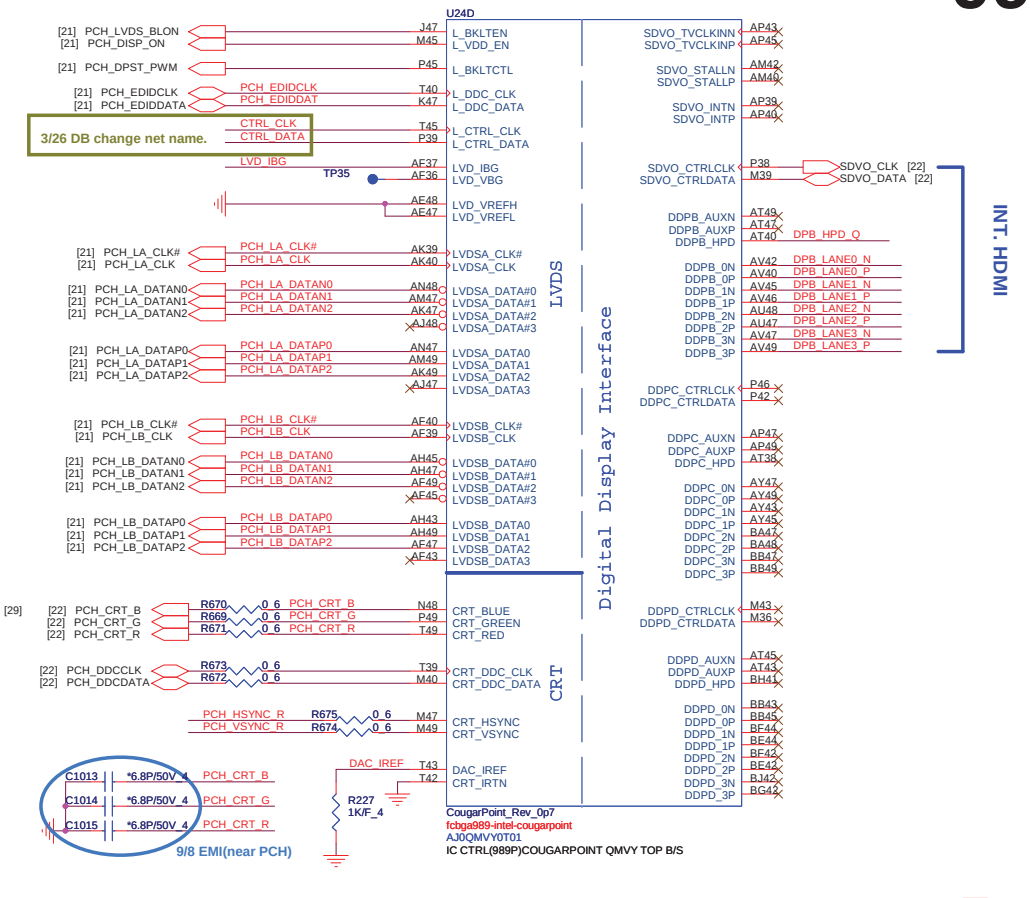
Cougar Point (DMI,FDI,PM)

Cougar Point (LVDS,DDI)

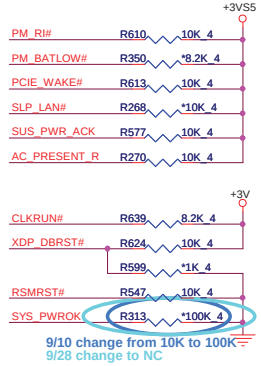
06



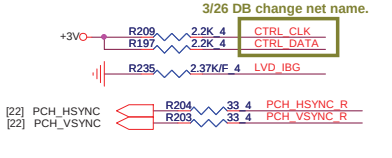


[7,10,21,22,23,27,28,36] +5V
[2,7,8,9,10,12,13,14,21,22,23,24,25,26,27,28,29,34,36,37,39] +3V
[2,7,8,9,10,14,24,29,31,33,35,36,38] +3VS5
[7,21,27,28,29,30,31] +3VPCU
[7,10] +3V_DSW
[7,10,29] +3V_RTC

PCH Pull-high/low(CLG)

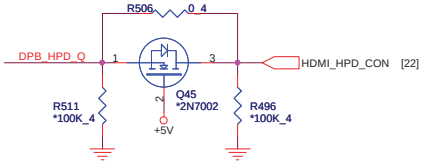


INT LVDS & CRT disable (DIS only remove)

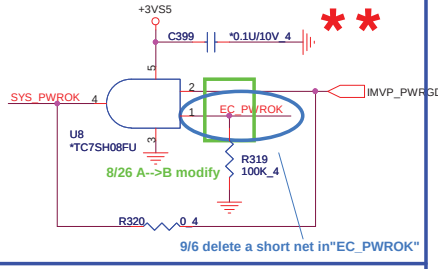


INT HDMI disable (DIS only remove)

INT HDMI Detect Function

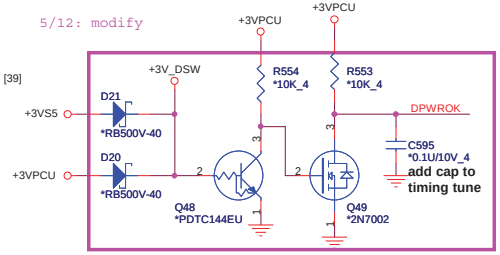


System PWR_OK(CLG)



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

DPWROK FOR DSW



NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (Host/Display)	A
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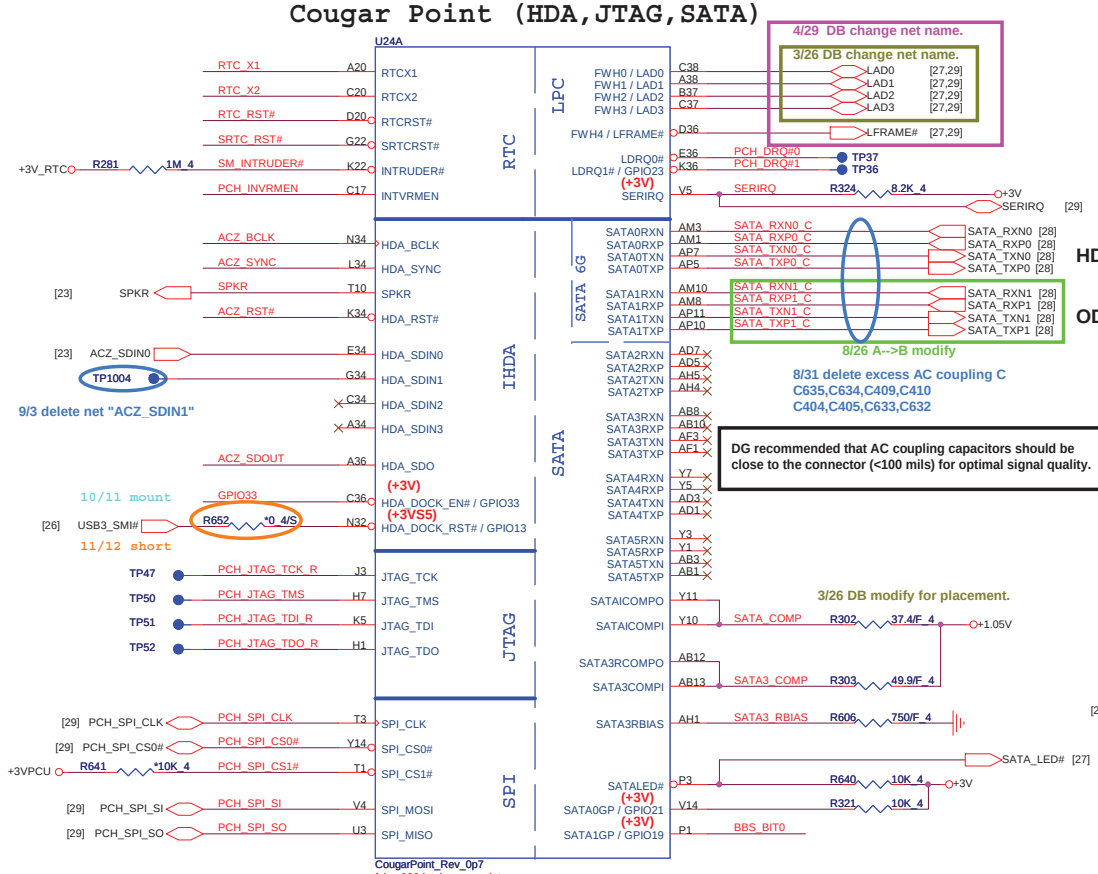
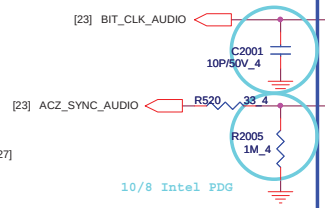
Cougar Point (HDA,JTAG,SATA)



CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMVY0T01
IC CTRL(989P)COUGARPOINT QMVY TOP B/S

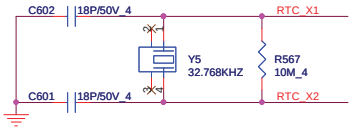
10/8 add for EMI



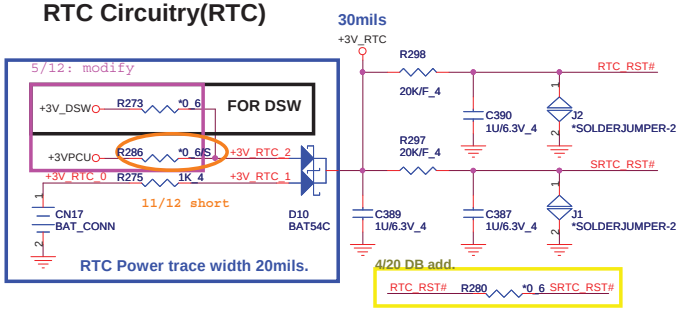
10/8 Intel PDG

RTC Clock 32.768KHz

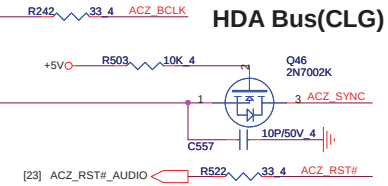
07



RTC Circuitry(RTC)

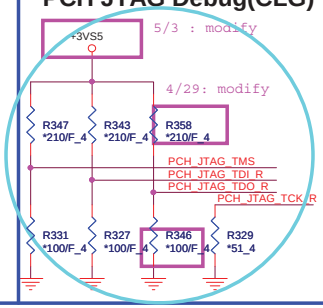


HDA Bus(CLG)



9/3 delete MDC function support
"ACZ_BCLK"-R246-"BIT_CLK_MDC"
"ACZ_SYNC"-R214-"ACZ_SYNC_MDC"
"ACZ_RST#"-R527-"ACZ_RST#_MDC"
"ACZ_SDOUT"-R539-"ACZ_SDOUT_MDC"

PCH JTAG Debug(CLG)



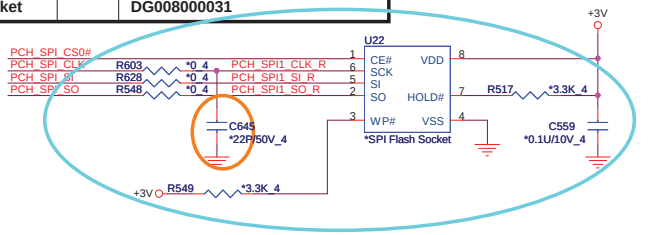
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R636 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R518 *1K_4, R514 10K_4, +3V, PCI_GNT3# [8], Bios request, for can't boot Capella 4/23
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R566 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R540 *1K_4, 8/26 A-->B modify, GPIO33_E [29]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1, GNT0# 1 → Boot Location SPI	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK	GNT1# 1, GNT0# 0 → Boot Location LPC	R602 *1K_4, R513 *1K_4, BBS_BIT0, BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R608 *1K_4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm 4/29 modify	+1.8V R616 2.2K_4, R607 4.7K_4, NV_CLE [8], H_SNB_IVB# [2], N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R215 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	8/26 A-->B modify, [29] GPIO33_E, ACZ_SDOUT R544 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R611 *1K_4, 4/29 reserve., ICC_EN# [9]
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R617 *1K_4 PLL_ODVR_EN [9]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R604 1K_4 +3V

Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

10/13 remove all R (Intel confirmed)

PCH SPI ROM(CLG)



[10] +V3.3A_1.5A_HDA_IO
[2,6,8,9,10,12,13,14,21,22,23,24,25,26,27,28,29,34,36,37,39] +3V
[6,21,27,28,29,30,31] +3VPCU
[6,10] +3V_DSW
[6,10,29] +3V_RTC
[4,10,36,38] +1.8V

NB5

PROJECT : TWH
Quanta Computer Inc.

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Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

08

11/8
change net name to "PCH_GPIO4"
delete "DGPU_IDLE_INT#" pull-hi

PCI/USBOC# Pull-up(CLG)

PCI_PIRQA# R198 8.2K_4
PCI_PIRQB# R531 8.2K_4
PCI_PIRQC# R234 8.2K_4
PCI_PIRQD# R238 8.2K_4

3/26 DB change Part reference.
PCH_GPIO4
RP12 10K_10P8R_6
MPC_PWR_CTRL#
BT_COMBO_EN#
LCD_BK

3/26 DB change Part reference.
RP13 10K_10P8R_6
USB_OC4# USB_OC6#
USB_OC1# USB_OC0#
USB_OC2# USB_OC7#
USB_OC3# USB_OC5#

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R521 *1K_4

U24E

RSVD: TP1–TP20, TP21–TP24, TP25–TP40

NVRAM: NV_CE#0–3, NV_DQS0, NV_DQS1, NV_DQ0–NV_DQ15, NV_ALE, NV_CLE, NV_RCOMP, NV_RB#, NV_RE#_WRB0, NV_RE#_WRB1, NV_WE#_CK0, NV_WE#_CK1

PCI: PIRQA#–PIRQD#, BT_COMBO_EN#, BBS_BIT1, PCI_GNT3#, LCD_BK, MPC_PWR_CTRL#, PCH_GPIO4, DGPU_IDLE_INT#, PCI_PME#, PCI_PLTRST#, CLK_PCI_TPM_R, CLK_PCI_CARD_R, CLK_PCI_FB, CLK_PCI_FB_R, CLK_PCI_LPC_R, CLK_PCI_EC_R

USB: USBP0N–USBP13P, USBRBIAS#, USB_BIAS, USB_OC0#–USB_OC7#

11/8 delete R2001

Bios swap GPIO 4/23.

9/5 remove R213 in BOM

9/8 EMI(near PCH)

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMVY0T01
IC CTRL(989P)COUGARPOINT QMVY TOP B/S

WLAN / LAN / USB3.0

WLAN: PCIE_RXN1/RXP1/TXN1/TXP1 → C385/C379 0.1U/10V_4 → PCIE_TXN1_C / PCIE_TXP1_C

LAN: PCIE_RXN2_LAN/RXP2_LAN/TXN2_LAN/TXP2_LAN → C345/C353 0.1U/10V_4 → PCIE_TXN2_LAN_C / PCIE_TXP2_LAN_C

USB3.0: PCIE_RXN3_USB3/RXP3_USB3/TXN3_USB3/TXP3_USB3 → C355/C358 0.1U/10V_4 → PCIE_TXN3_USB3_C / PCIE_TXP3_USB3_C

8/26 A-->B modify

8/26 A-->B modify

USBP1- / USBP1+ — USB2.0 — EXTERNAL USB2.0
USBP2- / USBP2+ — USB2.0 — USB2.0/USB3.0 COMBO
USBP4- / USBP4+ — USB2.0 — USB2.0/USB3.0 COMBO

HM65 Port6 & Port7 are disable

TP1001 / TP1002 — Bluetooth
USBP9- / USBP9+ — Camera
USBP10- / USBP10+ — WLAN
USBP12- / USBP12+ — Card Reader

9/3 delete BT function (USB) delete net "USB8+/-"

R541 22.6/F_4

9/4 Change net name "BOARD_ID1" to "INT_BT_COMBO_EN#"

[27] INT_BT_COMBO_EN#
[9] BOARD_ID2

Bios swap GPIO 4/23.
[9] BOARD_ID0

U24B

PCI-E*: PERN1–8, PERP1–8, PETN1–8, PETP1–8

SMBUS: SMBALERT# / GPIO11, SMBCLK, SMBDATA, SMLOALERT# / GPIO60, SMLOCLK, SMLODATA, SML1ALERT# / PCHHOT# / GPIO74, SML1CLK / GPIO58, SML1DATA / GPIO75

Controller Link: CL_CLK1, CL_DATA1, CL_RST1#

CLOCKS: CLKOUT_PCIE0N/P, CLKOUT_PEG_A_N/P, CLKOUT_DMI_N/P, CLKOUT_DP_N/P, CLKIN_DMI_N/P, CLKIN_GND1_N/P, CLKIN_DOT_96N/P, CLKIN_SATA_N/P, REFCLK14IN, CLKIN_PCILOOPBACK, XTAL25_IN, XTAL25_OUT, XCLK_RCOMP

FLEX CLOCKS: CLKOUTFLEX0 / GPIO64, CLKOUTFLEX1 / GPIO65, CLKOUTFLEX2 / GPIO66, CLKOUTFLEX3 / GPIO67

3/26 DB del external clock generator.

8/26 A-->B modify change FP

Remove Ra, Rb for UMA & SG. 27MHz support DIS only.

9/11 add R1015, exchange 27M net

10/8 remove 27M circuit

10/8 add for EMI

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMVY0T01
IC CTRL(989P)COUGARPOINT QMVY TOP B/S

SMBus/Pull-up(CLG)

4/20 modify

Q50 2N7002: [13,17,29] MBCLK2 → SMB_ME1_CLK; R586 2.2K_4; +3V / +3VS5
Q51 2N7002: [13,17,29] MBDATA2 → SMB_ME1_DAT; R587 2.2K_4
Q44 2N7002: SMB_PCH_DAT → SMB_RUN_DAT [12,13]; R487 4.7K_4; +3V
Q43 2N7002: SMB_PCH_CLK → SMB_RUN_CLK [12,13]; R486 4.7K_4

CLK_REQ/Strap Pin(CLG)

10/10 R638 mount

CLK_PCIE_REQ1# R638 10K_4
CLK_PCIE_REQ2# R323 10K_4
CLK_PCIE_REQ0# R597 10K_4
CLK_PCIE_REQ3# R612 10K_4
CLK_PCIE_REQ4# R287 10K_4
CLK_PEGB_REQ# R360 *10K_4
CLK_PEGA_REQ# Ra R344 10K_4
SG : Rb ; UMA : Ra
CLK_PEGA_REQ# Rb R328 *10K_4
CLK_PEGB_REQ# R111 10K_4
CLK_BUF_BCLK_N R556 10K_4
CLK_BUF_BCLK_P R558 10K_4
CLK_BUF_PCIE_3GPLL# R291 10K_4
CLK_BUF_PCIE_3GPLL R295 10K_4
CLK_BUF_DREFCLK# R258 10K_4
CLK_BUF_DREFCLK R262 10K_4
CLK_BUF_DREFSSCLK# R315 10K_4
CLK_BUF_DREFSSCLK R314 10K_4
CLK_PCH_14M R216 10K_4

CLOCK TERMINATION for FCIM

PCIE Clock

WLAN: [27] CLK_PCIE_WLANN/P, [27] PCIE_CLKREQ_WLAN# → RP7 0_4P2R_04 → CLK_PCH_SRC0N/P, CLK_PCIE_REQ0#
LAN: [24] CLK_PCIE_LANN/P, [24] PCIE_CLKREQ_LAN# → RP6 0_4P2R_04 → CLK_PCH_SRC2N/P, CLK_PCIE_REQ1#
GPU: [14] CLK_PCIE_VGA#/P, [14] PCIE_CLKREQ_VGA# → RP5 0_4P2R_04 → CLK_PCH_PEGAN/P, CLK_PCIE_REQ#
USB3.0: [26] CLK_PCIE_USB3N/P → RP8 0_4P2R_04 → CLK_PCH_PEGBN/P

3/26 DB change Part reference.

11/11 delete R359

[2,6,7,9,10,12,13,14,21,22,23,24,25,26,27,28,29,34,36,37,39] +3V
[2,6,7,9,10,14,24,29,31,33,35,36,38] +3VS5

PLTRST#(CLG)

C406 *0.1U/10V_4
U9 *TC7SH08FU
PCI_PLTRST# → PLTRST# [2,14,24,26,27,29]
R338 100K_4
R352 0_4

4/29 modify

SMBus/Pull-up(CLG)

R333 1K_4 DRAMRST_CNTRL_PCH
R282 10K_4 SMBALERT#
R351 2.2K_4 SMB_PCH_CLK
R337 2.2K_4 SMB_PCH_DAT
R534 2.2K_4 SMB_ME0_CLK
R292 2.2K_4 SMB_ME0_DAT
R289 10K_4 SML1ALERT# R

NB5

PROJECT : TWH
Quanta Computer Inc.

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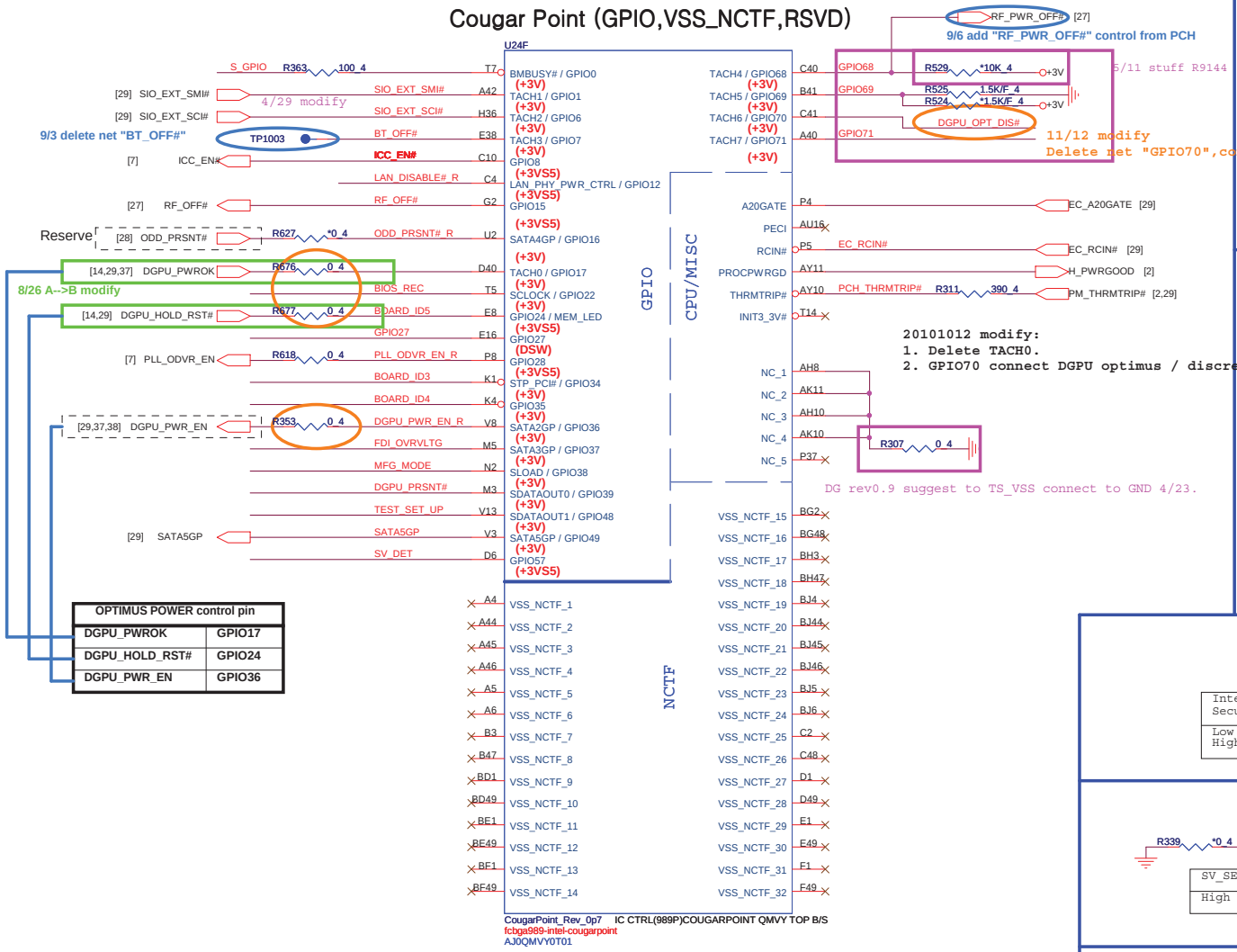
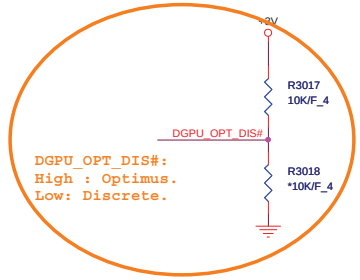
Cougar Point (GPIO,VSS_NCTF,RSVD)



OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

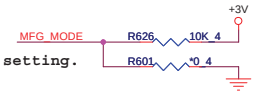
Clock Gen Power OK (CLG)

3/26 DB del external clock generator.

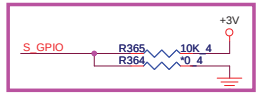


09

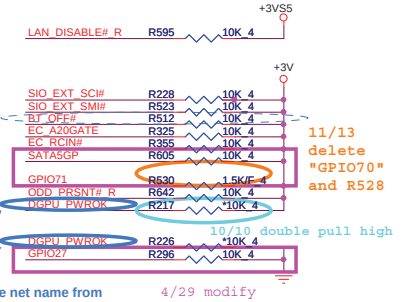
MFG-TEST

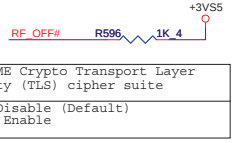


Bios swap GPIO 4/23.



GPIO Pull-up/Pull-down(CLG)





Intel ME Crypto Transport Layer Security (TLS) cipher suite	
Low = Disable (Default) High = Enable	

BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP	
High = Strong (Default)	

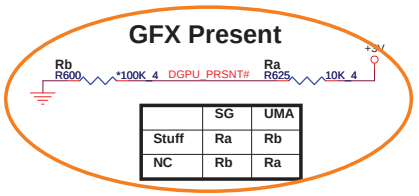
TEST DETECT	
Low = Default	

10/11 no need pull high

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

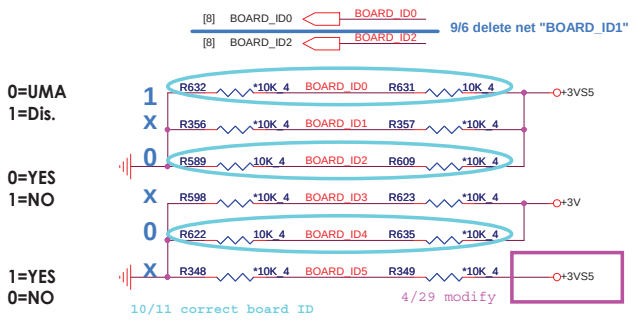
GFX Present



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
LG	0=LG 1=CB					
UMA/Dis.						
15.6"/ 14"			0=QLH/TWH 1=QLC/SWH			
MDC						
Dobly					0=NO 1=YES	
Optiums						



[2,6,7,8,10,12,13,14,21,22,23,24,25,26,27,28,29,34,36,37,39] +3V
[2,6,7,8,10,14,24,29,31,33,35,36,38] +3VS5

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Cougar Point-M (POWER)

COUGAR POINT (POWER)

10

11/12 add for CRT wave noise

U3001 *G910T21U — +5V → +3V_LDO (Vin, Vout, GND); C3009 *1U/6.3V_4

U24J

Clock and Miscellaneous

+1.05V R508 *0_8; +3VS5 R283 0_4; +3V_DSW R288 *0_4

+VCCACLK AD49 VCCACLK

+VCCPDSW T16 VCCDSW3_3 — 3mA (10mils)

PCH_VCCDSW V12 DCPSUSBYP — C383 0.1U/10V_4; C408 *0.1U/10V_4

5/12: modify

+3V_SUS_CLKF33 T38 VCC3_3[5]

10/8 remove for leakage

4/29: modify

+1.05V +VCCAPLL_CPY_PCH — L30 *10uH/100mA_8 — C603 *10U/6.3V_6

BH23 VCCAPLLDMI2

+VCCDPLL_CPY AL29 VCCIO[14]

+VCCSUS1 AL24 DCPSUS[3] — C367 *1U/6.3V_4

+1.05V R569 *0_6/S

+1.05V +1.05V_VCCEPW — 1.01A (60mils) — R249 0.002/F_1206 — C351 1U/6.3V_4; C369 1U/6.3V_4; C352 1U/6.3V_4

AA19 VCCASW[1]; AA21 VCCASW[2]; AA24 VCCASW[3]; AA26 VCCASW[4]; AA27 VCCASW[5]; AA29 VCCASW[6]; AA31 VCCASW[7]; AC26 VCCASW[8]; AC27 VCCASW[9]; AC29 VCCASW[10]; AC31 VCCASW[11]; AD29 VCCASW[12]; AD31 VCCASW[13]; W21 VCCASW[14]; W23 VCCASW[15]; W24 VCCASW[16]; W26 VCCASW[17]; W29 VCCASW[18]; W31 VCCASW[19]; W33 VCCASW[20]

C340 22U/6.3VS_8; C341 22U/6.3VS_8

11/12 short

+1.05V R335 *0_6/S — C407 1U/6.3V_4

C388 0.1U/10V_4 +VCCRTCEXT N16 DCPRTC

+1.05V R504 *0_6/S — C542 1U/6.3V_4

+VCCAFDI_VRM Y49 VCCVRM[4] — 160mA (20mils)

+1.05V_VCCA_A_DPL BD47 VCCADPLLA — 65mA (10mils)

+1.05V R557 *0_6/S — C592 1U/6.3V_4

+1.05V_VCCA_B_DPL BF47 VCCADPLLB — 8mA (10mils)

+VCCDIFFCLK AF17 VCCIO[7]; +VCCDIFFCLKN AF33 VCCDIFFCLKN[1]; AF34 VCCDIFFCLKN[2]; AG34 VCCDIFFCLKN[3] — 55mA (10mils)

+1.05V R293 *0_6 — C374 *1U/6.3V_4

+V1.05V_SSCVCC AG33 VCCSSC — 95mA (10mils)

C384 0.1U/10V_4 +VCCSST V16 DCPSST

+V1.05M_VCCSUS T17 DCPSUS[1]; V19 DCPSUS[2]

+1.05V R588 *0_4/S short402 — V_PROC_IO=1mA (10mils) — C621 4.7U/6.3V_6; C617 0.1U/10V_4; C613 0.1U/10V_4

+VTT_VCCPCPU BJ8 V_PROC_IO

+3V_RTC A22 VCCRTC — VCCRTC<1mA (10mils) — C386 1U/6.3V_4; C382 0.1U/10V_4; C375 0.1U/10V_4

PCI/GPIO/LPC

+1.05V_VCCUSBCORE +1.05V — R543 *0_8/S — C571 1U/6.3V_4 — 119mA (20mils)

+3VS5 — R267 *0_6/S — C360 0.1U/10V_4

R264 *0_6/S — C346 0.1U/10V_4

+3V_VCCPUSB N26 VCCIO[29]; P26 VCCIO[30]; P28 VCCIO[31]; T27 VCCIO[32]; T29 VCCIO[33]

+3V_VCCAUBG T23 VCCSUS3_3[7]; T24 VCCSUS3_3[8]; V23 VCCSUS3_3[9]; V24 VCCSUS3_3[10]; P24 VCCSUS3_3[6]

+VCCAUPLL T26 VCCIO[34] — R259 *0_6/S — +1.05V

+5V_PCH_VCC5REFSUS M26 V5REF_SUS

+VCCA_USBSUS AN23 DCPSUS[4] — C365 *1U/6.3V_4

+3V_VCCPSUS AN24 VCCSUS3_3[1]

11/12 short

+5V_PCH_VCC5REF P34 V5REF

+3V_VCCPSUS N20 VCCSUS3_3[2]; N22 VCCSUS3_3[3]; P20 VCCSUS3_3[4]; P22 VCCSUS3_3[5] — 119mA (15mils) — R290 *0_6/S — +3VS5

C366 1U/6.3V_4

+3V_VCCPCORE AA16 VCC3_3[1]; W16 VCC3_3[8]; T34 VCC3_3[4] — 266mA (20mils) — R332 *0_6/S — +3V

C403 0.1U/10V_4

C400 0.1U/10V_4

SATA

+3V AJ2 VCC3_3[2]

C338 0.1U/10V_4

AF13 VCCIO[5]; AH13 VCCIO[12]; AH14 VCCIO[13]; AF14 VCCIO[6]

+V1.05S_SATA3 — R318 *0_8/S — +1.05V

C402 0.1U/10V_4

AK1 VCCAPLLSATA; AF11 VCCVRM[1] — +V1.1LAN_VCCAPLL — L35 *10uH/100mA_8 — +1.05V

+VCCAFDI_VRM

C652 *10U/6.3V_6

AC16 VCCIO[2]; AC17 VCCIO[3]; AD17 VCCIO[4]

+1.05V_VCCIO1 — R362 *0_6/S — +1.05V

C412 1U/6.3V_4

MISC

1.01A (60mils)

+1.05V +1.05V_VCCEPW

T21 VCCASW[22]; V21 VCCASW[23]; T19 VCCASW[21]

10mA (10mils)

+V3.3A_1.5A_HDA_IO — R550 *0_4 — +1.5VSUS

HDA

VCCSUSHDA P32 — R552 0_4 — +3VS5

C580 0.1U/10V_4; C575 *1U/6.3V_4

CPU

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fcbga989-intel-cougarpoint
AJ0QMVY0T01
IC CTRL(989P)COUGARPOINT QMVY TOP B/S

[4,7,36,38] +1.8V
[2,4,12,13,32,33,38] +1.5VSUS
[6,7,8,35] +1.05V

[6,7,21,22,23,27,28,36] +5V
[21,23,26,31,32,33,34,35,36,37,38,39,40] +5VS5
[2,6,7,8,9,12,13,14,21,22,23,24,25,26,27,28,29,34,36,37,39] +3V
[2,6,7,8,9,14,24,29,31,33,35,36,38] +3VS5
[6,7] +3V_DSW
[6,7,29] +3V_RTC

U24G

VCC CORE

1.3 A (60mils)

+1.05V +1.05V_PCH_VCC — R301 0.002/F_1206 — C350 1U/6.3V_4; C361 1U/6.3V_4; C370 10U/6.3VS_6; C349 1U/6.3V_4

AA23 VCCCORE[1]; AC23 VCCCORE[2]; AD21 VCCCORE[3]; AD23 VCCCORE[4]; AF21 VCCCORE[5]; AF23 VCCCORE[6]; AG21 VCCCORE[7]; AG23 VCCCORE[8]; AG24 VCCCORE[9]; AG26 VCCCORE[10]; AG27 VCCCORE[11]; AG29 VCCCORE[12]; AJ23 VCCCORE[13]; AJ26 VCCCORE[14]; AJ27 VCCCORE[15]; AJ29 VCCCORE[16]; AJ31 VCCCORE[17]

+1.05V +1.05V_PCH_VCCDPLL_EXP — R274 *0_6/S

+1.05V +1.05V_VCCAPLL_EXP — L31 *1uH/25mA_6 — C604 *10U/6.3V_6

AN19 VCCIO[28]; BJ22 VCCAPLLEXP

VCCIO

+1.05V +1.05V_VCCIO — 2.925 A (140mils) — R257 0.002/F_1206 — C330 1U/6.3V_4; C334 1U/6.3V_4; C329 10U/6.3VS_6; C356 1U/6.3V_4; C344 1U/6.3V_4

AN16 VCCIO[15]; AN17 VCCIO[16]; AN21 VCCIO[17]; AN26 VCCIO[18]; AN27 VCCIO[19]; AP21 VCCIO[20]; AP23 VCCIO[21]; AP24 VCCIO[22]; AP26 VCCIO[23]; AT24 VCCIO[24]; AN33 VCCIO[25]; AN34 VCCIO[26]

+3V +3V_VCC_EXP — R564 0_8 — C600 0.1U/10V_4

160mA (15mils)

(Mobile 1.5V) +VCCAFDI_VRM

+1.5V_CPU R500 0_6; +1.05V R501 *0_6 — +VCCAFDI_VRM AP16 VCCVRM[2]

+1.05V_VCCAPLL_FDI

+1.05V R316 *0_8; R304 0_8 — BG6 VccAFDIPLL; AP17 VCCIO[27]

+1.05V_VCCDPLL_FDI

+1.05V AU20 VCCDMI[2]

BH29 VCC3_3[3]

CRT

VCCADAC

VSSADAC

LVDS

VCCTX_LVDS[1]; VCCTX_LVDS[2]; VCCTX_LVDS[3]; VCCTX_LVDS[4]

VCCALVDS AK36; VSSALVDS AK37

HVCMOS

VCC3_3[6] V33; VCC3_3[7] V34

DMI

VCCVRM[3] AT16; VCCDMI[1] AT20; VCCCLKDMI AB36

NAND / SPI

VCCPNAND[1] AG16; VCCPNAND[2] AG17; VCCPNAND[3] AJ16; VCCPNAND[4] AJ17

VCCSPI V1

FDI

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fcbga989-intel-cougarpoint
AJ0QMVY0T01
IC CTRL(989P)COUGARPOINT QMVY TOP B/S

+1.05V — 65mA (10mils) — L25 10uH/100MA_8 — +1.05V_VCCA_A_DPL — C543 1U/6.3V_4; C540 *220U/2.5V_3528

8mA (10mils) — L27 10uH/100MA_8 — +1.05V_VCCA_B_DPL — C586 1U/6.3V_4; C576 *220U/2.5V_3528

5/14 modify

+3V — 20mA (10mils) — R536 *0_6 +3V_SUS_CLKF33; R537 1/F_4 +3V_SUS_CLKF33_R — L28 10uH/100MA_8 — C568 1U/6.3V_4; C567 10U/6.3VS_6

20mA (10mils)

+1.05V +VCC_DMI_CCI — R591 *1/F_4; R592 0_4 — L33 *10uH/100mA_8 — +1.1V_VCC_DMI_CCI

+3V_LDO — U48 1mA (10mils) — L24 HCB1608KF-181T15/1.5A_6 — +3V

C523 10U/6.3VS_6; C525 0.1U/10V_4; C524 0.01U/25V_4

U47 — 1mA (10mils) — R489 *0_6

+VCCALVDS — Ra R561 0_4; Rb R562 *0_4

60mA (10mils)

+VCC_TX_LVDS — L29 0.1uH/250mA_8 — +1.8V

Ra R551 *0_4; Rb R551 *0_4

C584 22U/6.3VS_8; C581 0.01U/25V_4; C582 0.01U/25V_4

SG & UMA : Ra
DIS : Rb

+3V_VCC_GIO — R243 *0_6/S — +3V

C333 0.1U/10V_4

42mA (10mils)

+VCCAFDI_VRM — +1.1V_VCC_DMI — R279 *0_4/S — +1.05V

C376 1U/6.3V_4

+1.1V_VCC_DMI_CCI

C616 1U/6.3V_4; C619 *10U/6.3V_6

190 mA (15mils)

+VCCP_NAND — +1.8V — R317 *0_8/S

C401 0.1U/10V_4

11/12 short

20mA (10mils)

+3V_VCCME_SPI — R643 *0_6/S — +3V

C646 1U/6.3V_4

+5V_PCH_VCC5REF — R241 10_4 — +5V

V5REF= 1mA — D9 RB500V-40 — +3V

C332 1U/6.3V_4

+5V_PCH_VCC5REFSUS — R560 10_4 — +5VS5

VCC5REFSUS=1mA — D22 RB500V-40 — +3VS5

C589 0.1U/10V_4

NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (Power)	A
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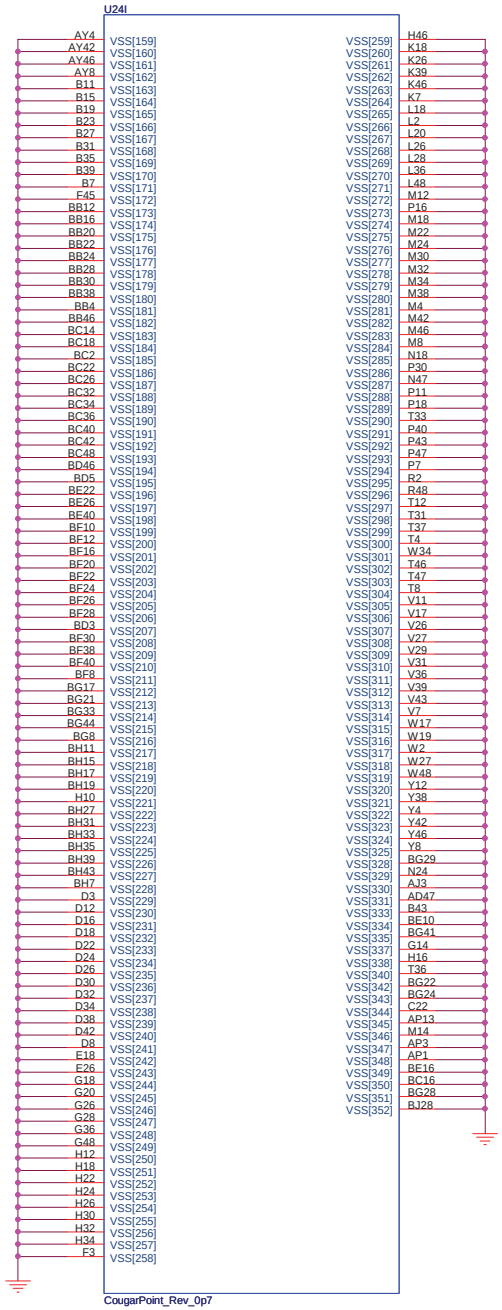
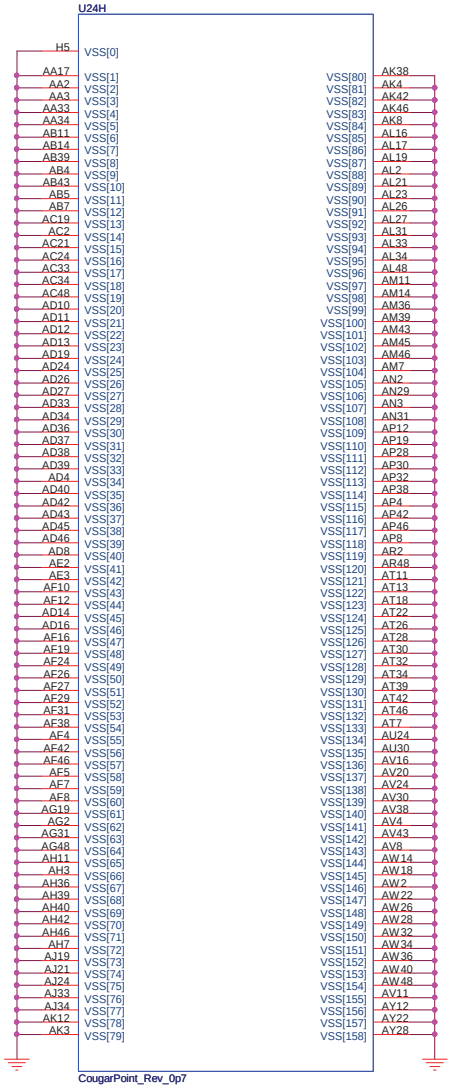
IBEX PEAK-M (GND)



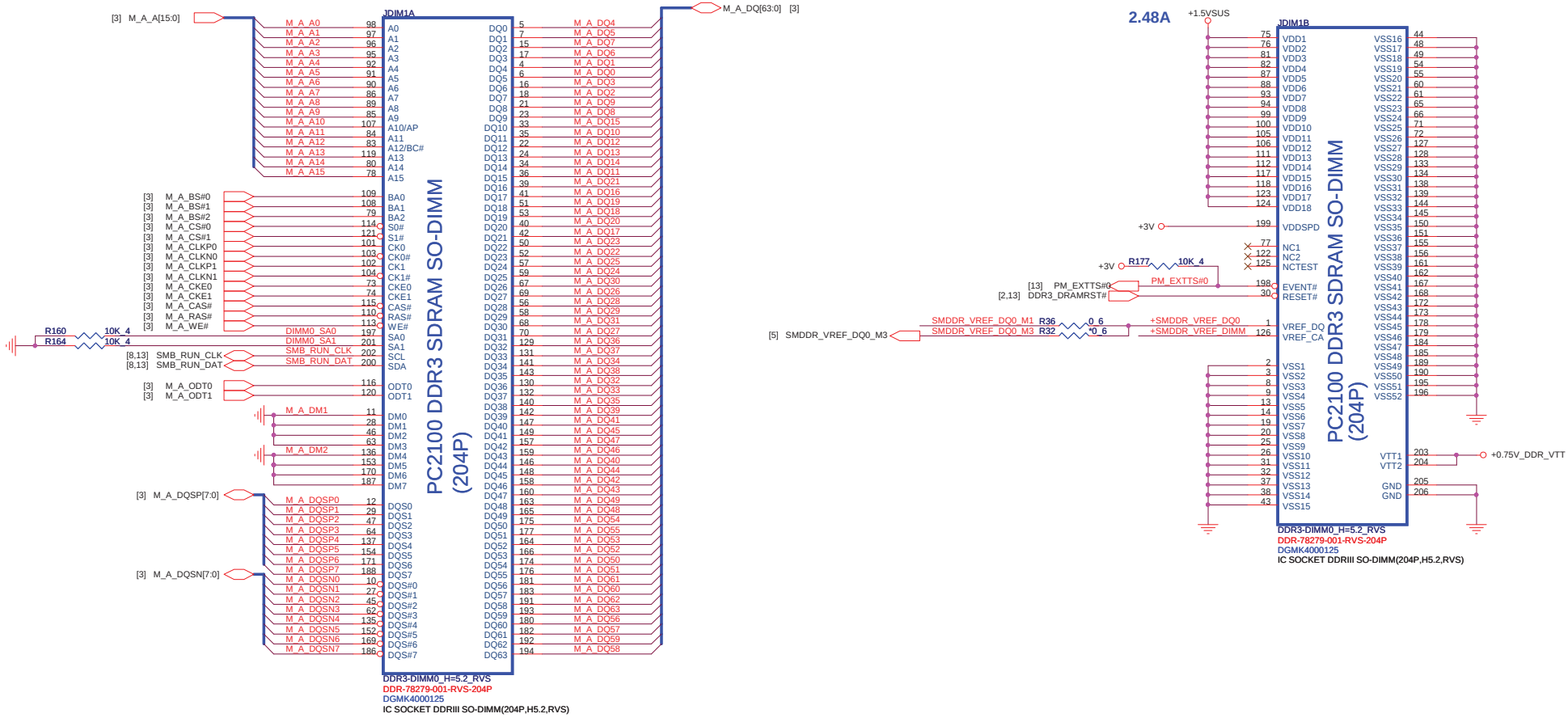
IBEX PEAK-M (GND)



NB5

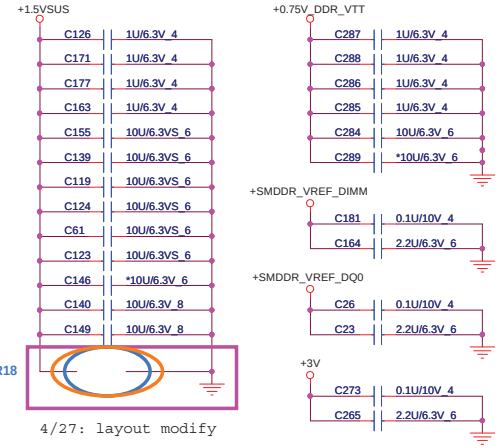
PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (Ground)	A
Date: Monday, November 15, 2010	Sheet 11 of 40	



Remove M2 Solution (Intel 436996 Doc)

Place these Caps near So-Dimm0.

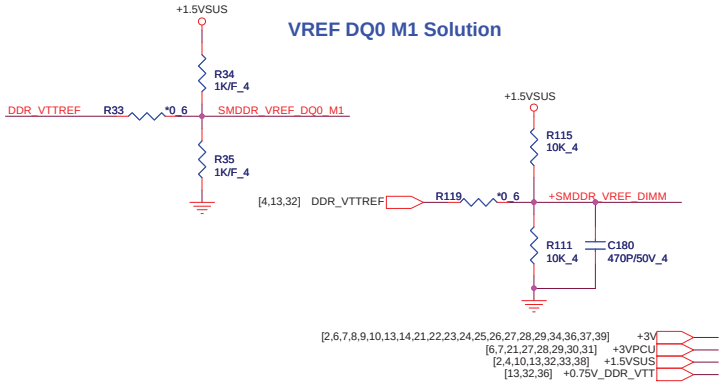


8/31 C513 FP changed from 330U_2.5V_5.0x5.9ESR10m to 220U/6.3V_6x4.5ESR18

11/13 delete C513

4/27: layout modify

VREF DQ0 M1 Solution



NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 1/2 (5.2H)	A
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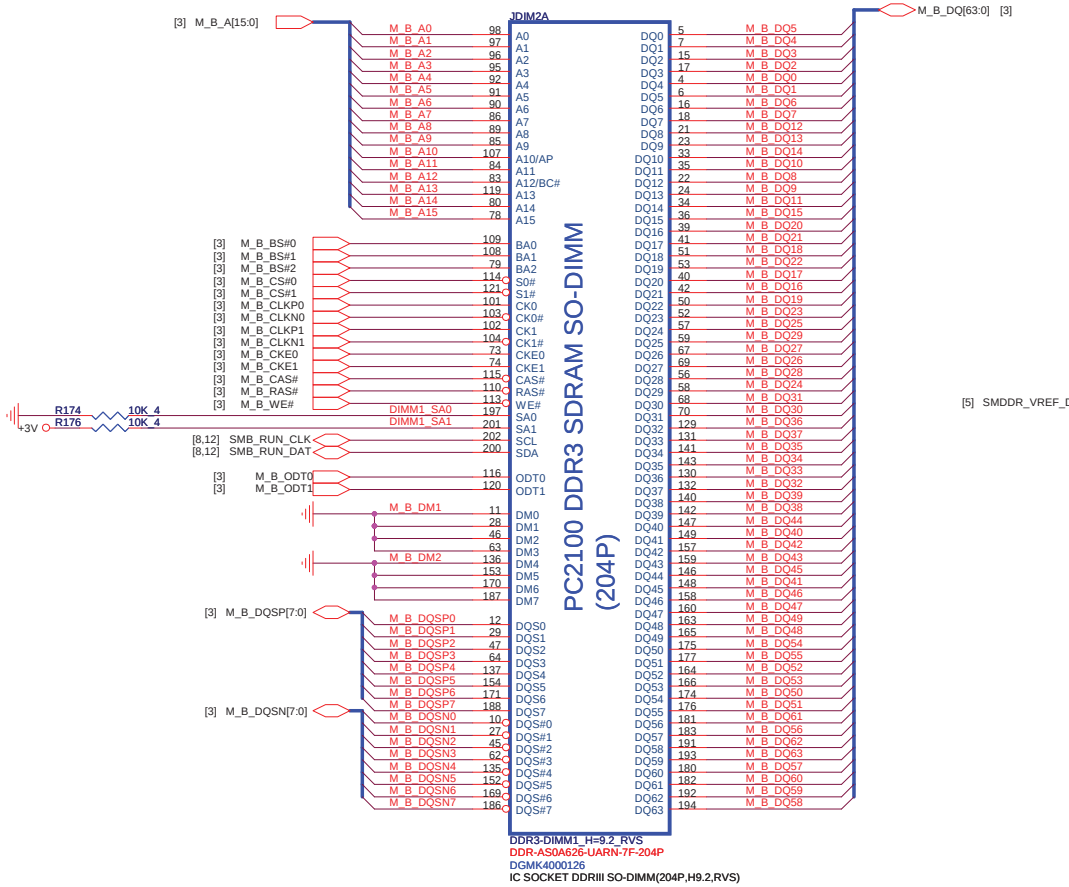
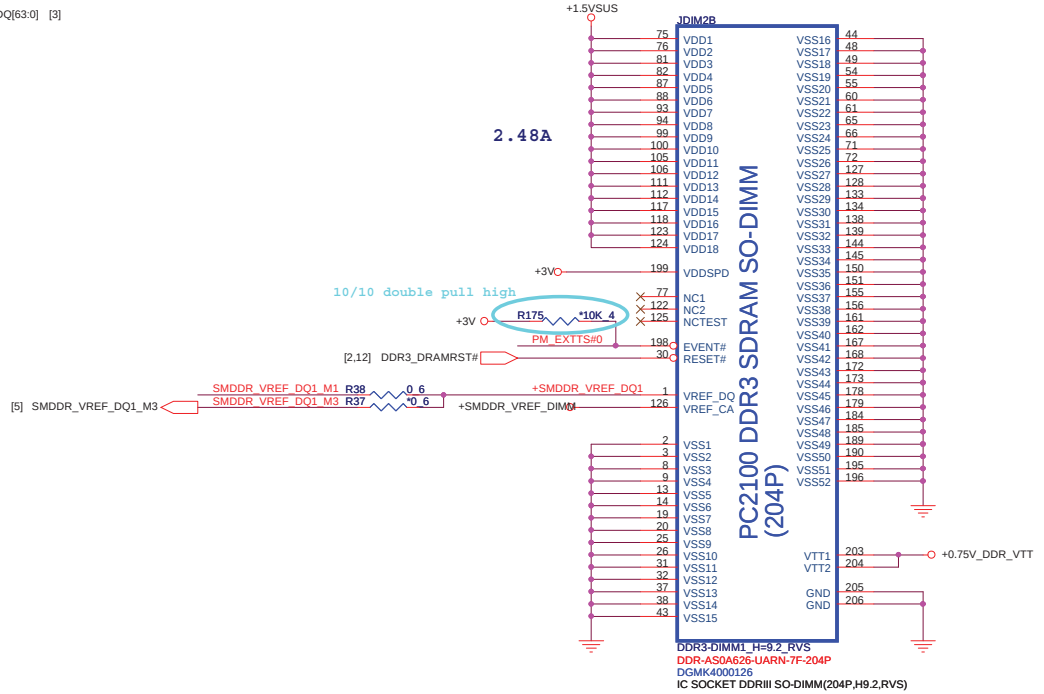
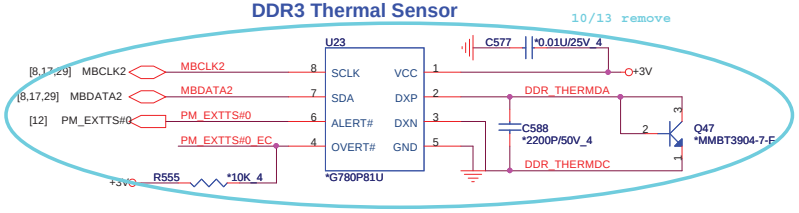


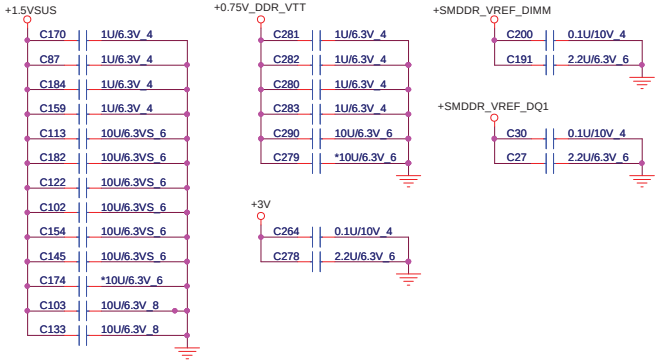


DDR3 Thermal Sensor

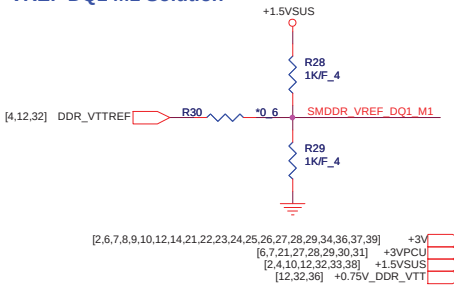


Remove M2 Solution (Intel 436996 Doc)

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



NB5	PROJECT : TWH Quanta Computer Inc.
Size: Custom	Document Number: System Memory 2/2 (9.2H) — Rev: A
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Power Sequence

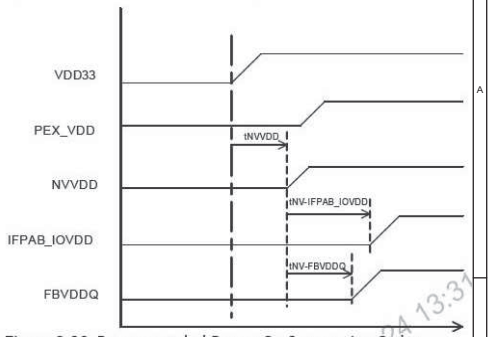


Figure 3.20 Recommended Power On Sequencing Order

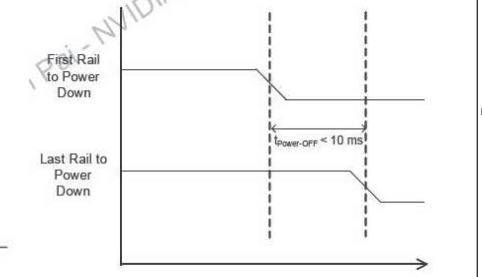


Figure 3.21 Recommended Power Off Sequencing Order

NVVDD Settling Time

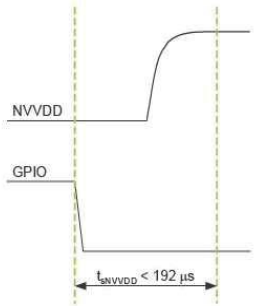
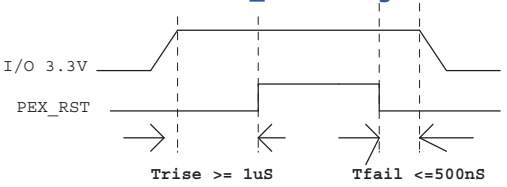


Figure 3.12 NVVDD Settling Time

PEX_RST timing



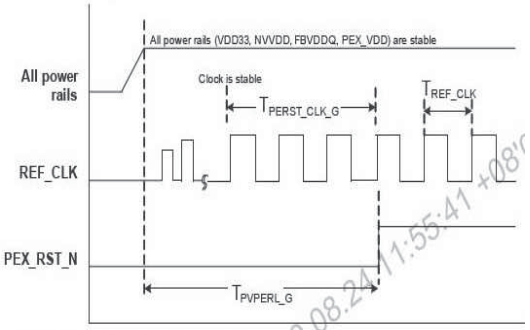
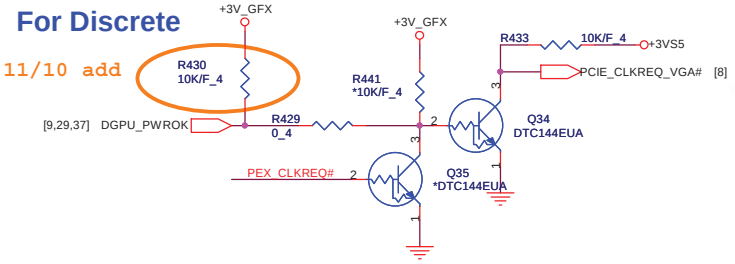


Figure 3-18. PEX_RST_N Timing for GPU

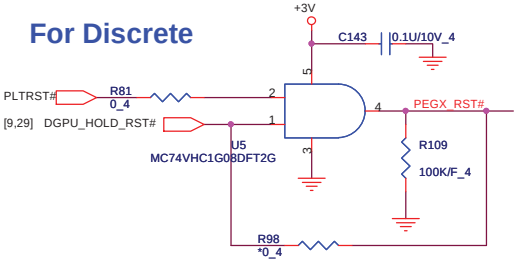
Table 3-8. N11x Reset Requirements for PCI Express 2.0

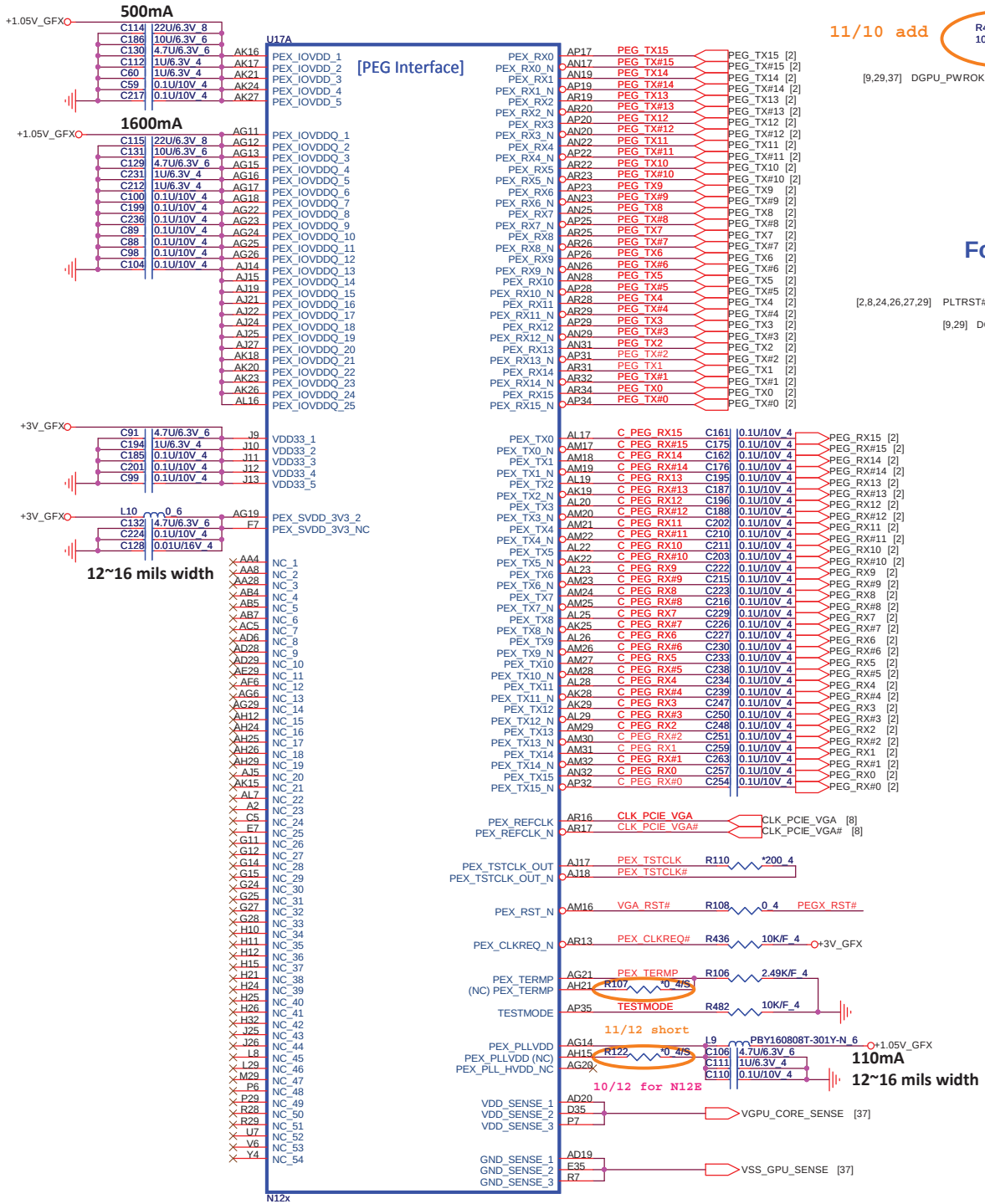
Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

For Discrete



For Discrete





NB5	PROJECT : TWH Quanta Computer Inc.
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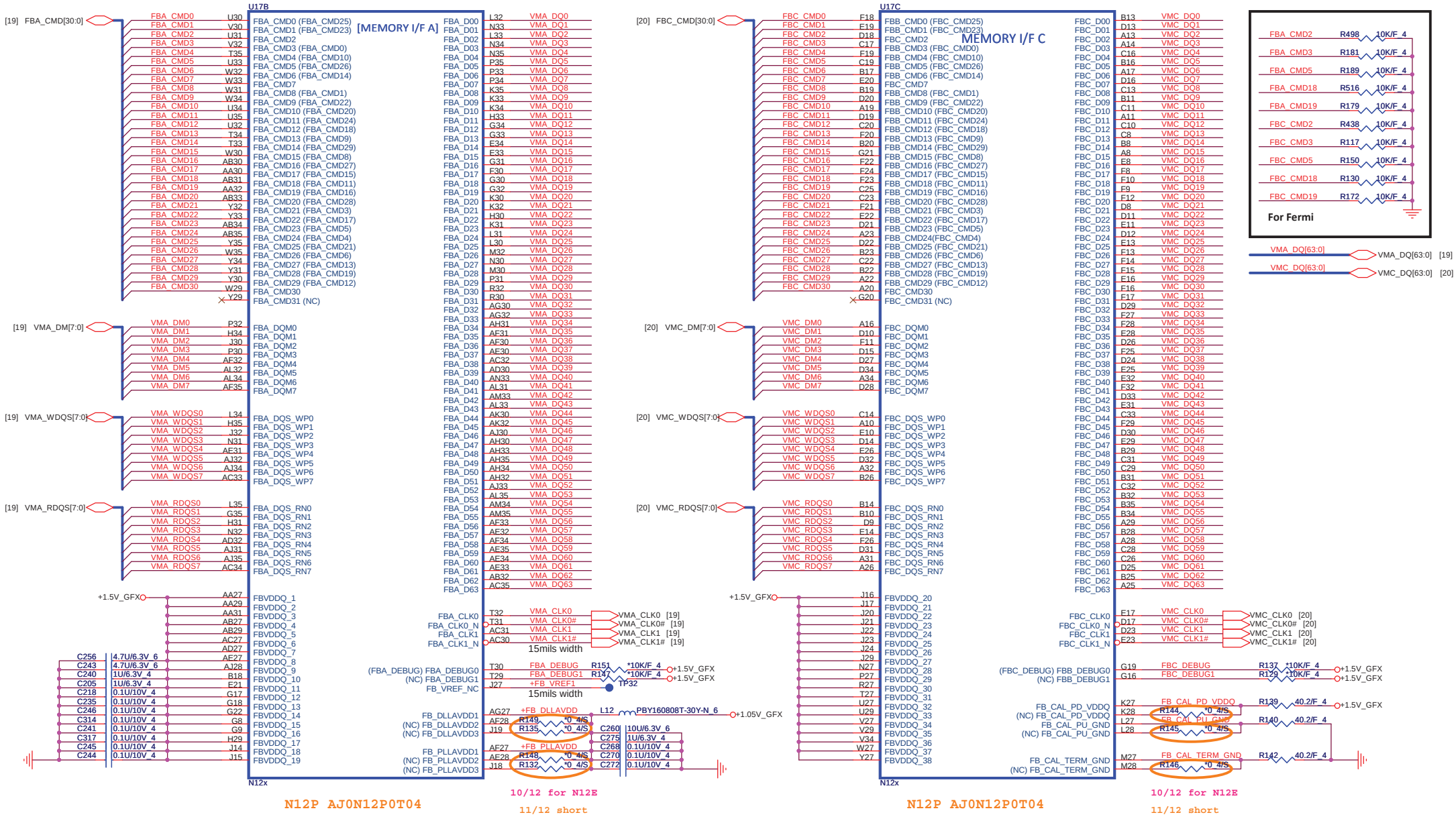
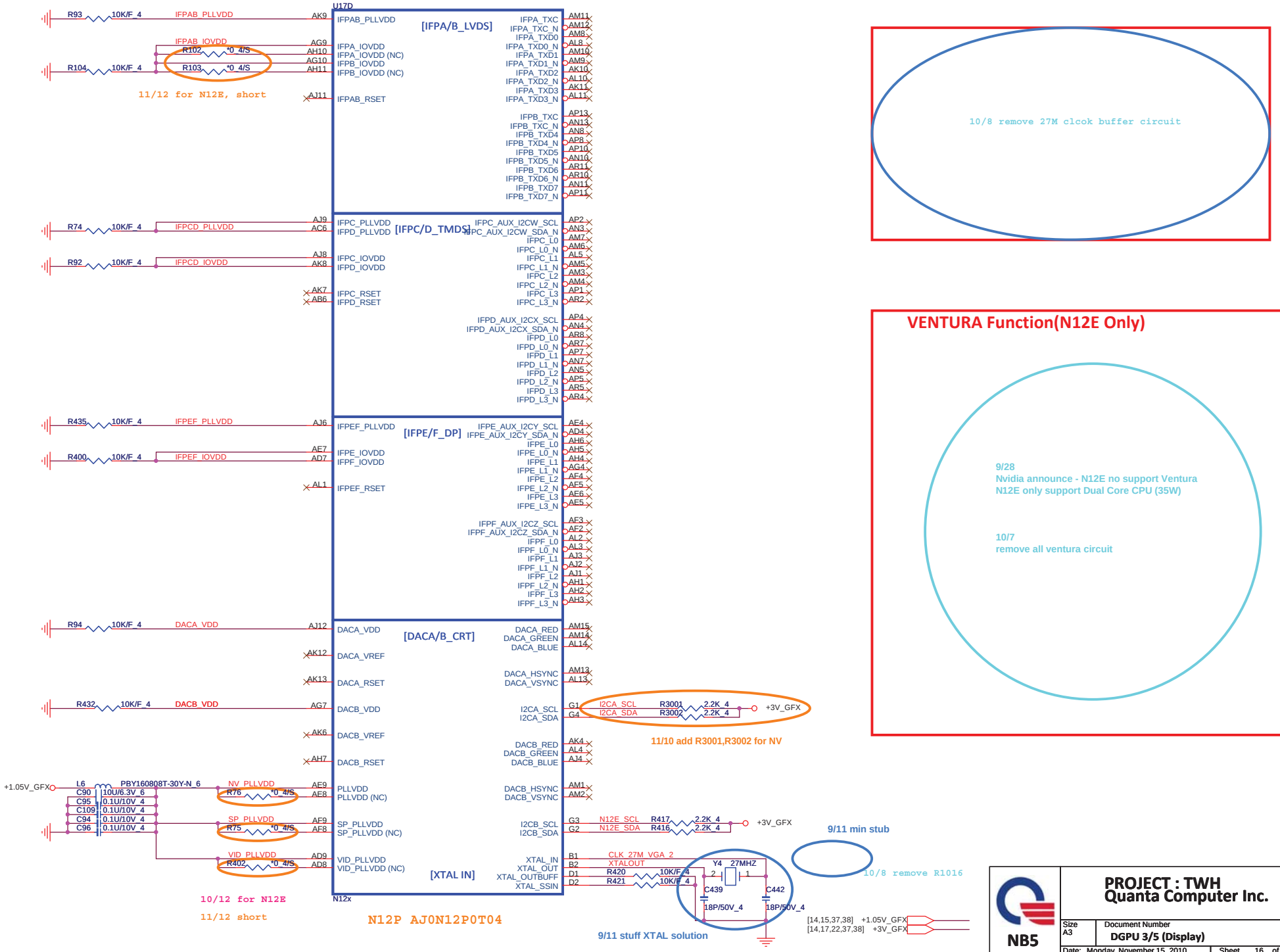

U17B
[MEMORY I/F A]
U17C
MEMORY I/F C
N12x
N12P AJ0N12P0T04
10/12 for N12E
11/12 short
For Fermi



10/8 remove 27M clcok buffer circuit

VENTURA Function(N12E Only)

9/28
Nvidia announce - N12E no support Ventura
N12E only support Dual Core CPU (35W)

10/7
remove all ventura circuit

NB5	PROJECT : TWH Quanta Computer Inc.	
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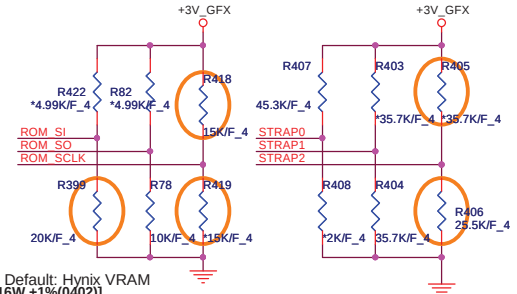
N11P-GS ES
Strap2 = 35K Pull High
ROM_CLK=15k Pull High

N11P-GS QS
Strap2 = 5K Pull down
ROM_CLK=15k Pull High

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Default: Hynix VRAM

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 [RES CHIP 20K 1/16W +-1%(0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)

ROM_SI
Hynix 64Mx16 -->15K PD
Samsung 64Mx16 -->20K PD
Hynix 128Mx16 -->35K PD
Samsung 128Mx16 -->45K PD

ROM_SO
--> 10K PD

ROM_SCLK
N11P-GS (DID=0DF0) ---> 15k PU
N12P-GS (DID=0DF4) --->15K PD
N12E-GE (DID=0DCE) --->15K PD

STRAP0
-->45K PU

STRAP1
N11P-GS -->35K PD
N12P-GS waiting PUN update
N12E-GE waiting PUN update

STRAP2
N11P-GS (DID=0DF0) ---> 5k PD
N12P-GS (DID=0DF4) --->25K PD
N12E-GE (DID=0DCE)--->35K PU

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

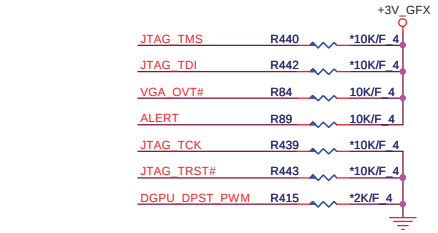
VRAM Configuration Table

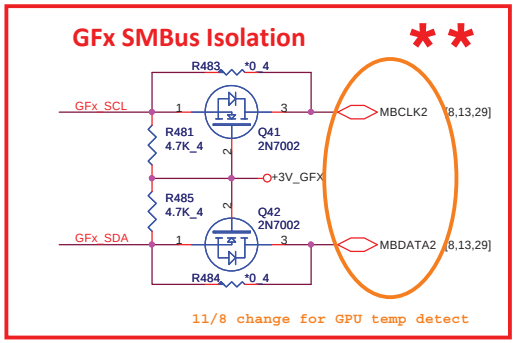
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

AKD58GGT^01
AKD5LZGTW00
AKD5LGGT502

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL





N12P AJ0N12P0T04

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NB5

Size	Document Number	Rev
Custom	DGPU 4/5 (MIO/GPIO)	A

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+VGACORE

U17F

[GPU VDD]

AB11	VDD_001	VDD_057	P21		
AB13	VDD_002	VDD_058	P23		
AB15	VDD_003	VDD_059	P25		
AB17	VDD_004	VDD_060	R11		
AB19	VDD_005	VDD_061	R12		
AB21	VDD_006	VDD_062	R13		
AB23	VDD_007	VDD_063	R14		
AB25	VDD_008	VDD_064	R15		
AC11	VDD_009	VDD_065	R16		
AC12	VDD_010	VDD_066	R17		
AC13	VDD_011	VDD_067	R18		
AC14	VDD_012	VDD_068	R19		
AC15	VDD_013	VDD_069	R20		
AC16	VDD_014	VDD_070	R21		
AC17	VDD_015	VDD_071	R22		
AC18	VDD_016	VDD_072	R23		
AC19	VDD_017	VDD_073	R24		
AC20	VDD_018	VDD_074	R25		
AC21	VDD_019	VDD_075	T12		
AC22	VDD_020	VDD_076	T14		
AC23	VDD_021	VDD_077	T16		
AC24	VDD_022	VDD_078	T18		
AC25	VDD_023	VDD_079	T20		
AD12	VDD_024	VDD_080	T22		
AD14	VDD_025	VDD_081	T24		
AD16	VDD_026	VDD_082	V11		
AD18	VDD_027	VDD_083	V13		
AD22	VDD_028	VDD_084	V15		
AD24	VDD_029	VDD_085	V17		
L11	VDD_030	VDD_086	V19		
L12	VDD_031	VDD_087	V21		
L13	VDD_032	VDD_088	V23		
L14	VDD_033	VDD_089	V25		
L15	VDD_034	VDD_090	W11		
L16	VDD_035	VDD_091	W12		
L17	VDD_036	VDD_092	W13		
L18	VDD_037	VDD_093	W14		
L19	VDD_038	VDD_094	W15		
L20	VDD_039	VDD_095	W16		
L21	VDD_040	VDD_096	W17		
L22	VDD_041	VDD_097	W18		
L23	VDD_042	VDD_098	W19		
L24	VDD_043	VDD_099	W20		
L25	VDD_044	VDD_100	W21		
M12	VDD_045	VDD_101	W22		
M14	VDD_046	VDD_102	W23		
M16	VDD_047	VDD_103	W24		
M18	VDD_048	VDD_104	W25		
M20	VDD_049	VDD_105	Y12		
M22	VDD_050	VDD_106	Y14		
M24	VDD_051	VDD_107	Y16		
P11	VDD_052	VDD_108	Y18		
P13	VDD_053	VDD_109	Y20		
P15	VDD_054	VDD_110	Y22		
P17	VDD_055	VDD_111	Y24		
P19	VDD_056				

N12x

N12P AJ0N12P0T04

+VGACORE

C723	C724	C725	C726
0.1U/10V_4	0.1U/10V_4	1U/6.3V_4	4.7U/6.3V_6

+VGACORE

C727	C728	C729	
10U/6.3V_8	10U/6.3V_8	47U/6.3V_8	

U17G

[GPU GND]

AA2	GND_1	GND_97	E9		
AA5	GND_2	GND_98	E12		
AA11	GND_3	GND_99	E15		
AA12	GND_4	GND_100	E18		
AA13	GND_5	GND_101	E24		
AA14	GND_6	GND_102	E27		
AA15	GND_7	GND_103	E30		
AA16	GND_8	GND_104	F2		
AA17	GND_9	GND_105	F5		
AA18	GND_10	GND_106	F31		
AA19	GND_11	GND_107	F34		
AA20	GND_12	GND_108	J2		
AA21	GND_13	GND_109	J5		
AA22	GND_14	GND_110	J31		
AA23	GND_15	GND_111	J34		
AA24	GND_16	GND_112	L9		
AA25	GND_17	GND_113	M2		
AA34	GND_18	GND_114	M5		
AB12	GND_19	GND_115	M11		
AB14	GND_20	GND_116	M13		
AB16	GND_21	GND_117	M15		
AB18	GND_22	GND_118	M17		
AB20	GND_23	GND_119	M19		
AB22	GND_24	GND_120	M21		
AB24	GND_25	GND_121	M23		
AC9	GND_26	GND_122	M25		
AD11	GND_27	GND_123	M31		
AD13	GND_28	GND_124	M34		
AD15	GND_29	GND_125	N11		
AD17	GND_30	GND_126	N12		
AD2	GND_31	GND_127	N13		
AD5	GND_32	GND_128	N14		
AD21	GND_33	GND_129	N15		
AD23	GND_34	GND_130	N16		
AD25	GND_35	GND_131	N17		
AD31	GND_36	GND_132	N18		
AD34	GND_37	GND_133	N19		
AE11	GND_38	GND_134	N20		
AE12	GND_39	GND_135	N21		
AE13	GND_40	GND_136	N22		
AE14	GND_41	GND_137	N23		
AE15	GND_42	GND_138	N24		
AE16	GND_43	GND_139	N25		
AE17	GND_44	GND_140	P12		
AE18	GND_45	GND_141	P14		
AE19	GND_46	GND_142	P16		
AE20	GND_47	GND_143	P18		
AE21	GND_48	GND_144	P20		
AE22	GND_49	GND_145	P22		
AE23	GND_50	GND_146	P24		
AE24	GND_51	GND_147	R2		
AE25	GND_52	GND_148	R5		
AG2	GND_53	GND_149	R31		
AG31	GND_54	GND_150	R34		
AG34	GND_55	GND_151	T11		
AK2	GND_56	GND_152	T13		
AG5	GND_57	GND_153	T15		
AK31	GND_58	GND_154	T17		
AK34	GND_59	GND_155	T19		
AK5	GND_60	GND_156	T21		
AK14	GND_61	GND_157	T23		
AL6	GND_62	GND_158	T25		
AL9	GND_63	GND_159	U11		
AL12	GND_64	GND_160	U12		
AL15	GND_65	GND_161	U13		
AL18	GND_66	GND_162	U14		
AL21	GND_67	GND_163	U15		
AL24	GND_68	GND_164	U16		
AL27	GND_69	GND_165	U17		
AL30	GND_70	GND_166	U18		
AN2	GND_71	GND_167	U19		
AN34	GND_72	GND_168	U20		
AP3	GND_73	GND_169	U21		
AP6	GND_74	GND_170	U22		
AP9	GND_75	GND_171	U23		
AP12	GND_76	GND_172	U24		
AP15	GND_77	GND_173	U25		
AP18	GND_78	GND_174	V2		
AP21	GND_79	GND_175	V5		
AP24	GND_80	GND_176	V9		
AP27	GND_81	GND_177	V12		
AP30	GND_82	GND_178	V14		
AP33	GND_83	GND_179	V16		
B3	GND_84	GND_180	V18		
B6	GND_85	GND_181	V20		
B9	GND_86	GND_182	V22		
B12	GND_87	GND_183	V24		
B15	GND_88	GND_184	V31		
B21	GND_89	GND_185	Y11		
B24	GND_90	GND_186	Y13		
B27	GND_91	GND_187	Y15		
B30	GND_92	GND_188	Y17		
B33	GND_93	GND_189	Y19		
C2	GND_94	GND_190	Y21		
C34	GND_95	GND_191	Y23		
E6	GND_96	GND_192	Y25		

N12x

N12P AJ0N12P0T04

N12P-GS (GB2-128) Stuff

+VGACORE

C693	C694	C695	C696	C697	C698	C699	C700	C701	C702	C703
0.01U/16V_4	0.01U/16V_4	0.01U/16V_4	0.01U/16V_4	0.01U/16V_4	0.01U/16V_4	0.01U/16V_4	0.01U/16V_4	0.022U/16V_4	0.022U/16V_4	0.022U/16V_4

+VGACORE

C704	C705	C706	C707	C708	C709	C710
0.47U/10V_4	0.47U/10V_4	0.47U/10V_4	0.22U/6.3V_4	0.22U/6.3V_4	0.22U/6.3V_4	22U/6.3V_8

N12E-GE : C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411 stuff 0.1U/10V_4.
N12E-GE : C412 Stuff 47U/6.3V_8

N12E-GE (GB3-128) Stuff

+VGACORE

C711	C712	C713	C714	C715
*0.1U/10V_4	*0.1U/10V_4	*0.1U/10V_4	*1U/6.3V_4	*1U/6.3V_4

+VGACORE

C716	C717	C718	C719	C720	C721	C722
*1U/6.3V_4	*1U/6.3V_4	*1U/6.3V_4	*1U/6.3V_4	*1U/6.3V_4	*4.7U/6.3V_6	*4.7U/6.3V_6

9/28 need check for N12E

[37] +VGACORE

NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
A3	DGPU 5/5 (Power/Ground)	A
Date: Monday, November 15, 2010	Sheet 18 of 40	

CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

VRAM3 / VRAM8 / VRAM4 / VRAM7 — 96-BALL SDRAM DDR3 — VRAM_DDR3

Should be 240 Ohms +-1%

R185 243/F_4
R490 243/F_4
R180 243/F_4
R497 243/F_4

[15] FBA_CMD5

VMA_ZQ1 / VMA_ZQ2 / VMA_ZQ3 / VMA_ZQ4

+1.5V_GFX

VMA_CLK0 — R178 160/F_4 — VMA_CLK0#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R505 1.33K/F_4 — VREFC_VMA1 — R499 1.33K/F_4 — C530 0.1U/10V_4
R188 1.33K/F_4 — VREFD_VMA1 — R182 1.33K/F_4 — C295 0.1U/10V_4

[15] FBA_CMD17 — FBA_CMD17 — TP29
[15] FBA_CMD1 — FBA_CMD1 — TP33

VMA_CLK1 — R183 160/F_4 — VMA_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R187 1.33K/F_4 — VREFC_VMA3 — R186 1.33K/F_4 — C297 0.1U/10V_4
R507 1.33K/F_4 — VREFD_VMA3 — R515 1.33K/F_4 — C544 0.1U/10V_4

Samsung 900MHz 1G AKD5LGHT500

[15,20,37,38] +1.5V_GFX

+1.5V_GFX
C528 1U/10V_4
C555 1U/10V_4
C318 1U/10V_4
C519 1U/10V_4

+1.5V_GFX
C531 10U/6.3V_8
C554 0.1U/10V_4
C316 0.1U/10V_4
C553 0.1U/10V_4
C521 0.1U/10V_4
C294 0.1U/10V_4

+1.5V_GFX
C527 10U/6.3V_8
C556 0.1U/10V_4
C551 0.1U/10V_4
C296 0.1U/10V_4
C535 0.1U/10V_4
C537 0.1U/10V_4
C300 0.1U/10V_4
C529 0.1U/10V_4

+1.5V_GFX
C291 10U/6.3V_8
C539 10U/6.3V_8
C292 0.1U/10V_4
C293 0.1U/10V_4
C301 0.1U/10V_4
C520 0.1U/10V_4
C315 0.1U/10V_4

+1.5V_GFX
C532 10U/6.3V_8
C538 10U/6.3V_8
C541 0.1U/10V_4
C552 0.1U/10V_4
C526 0.1U/10V_4

NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory 1/2 (DDR3)	A

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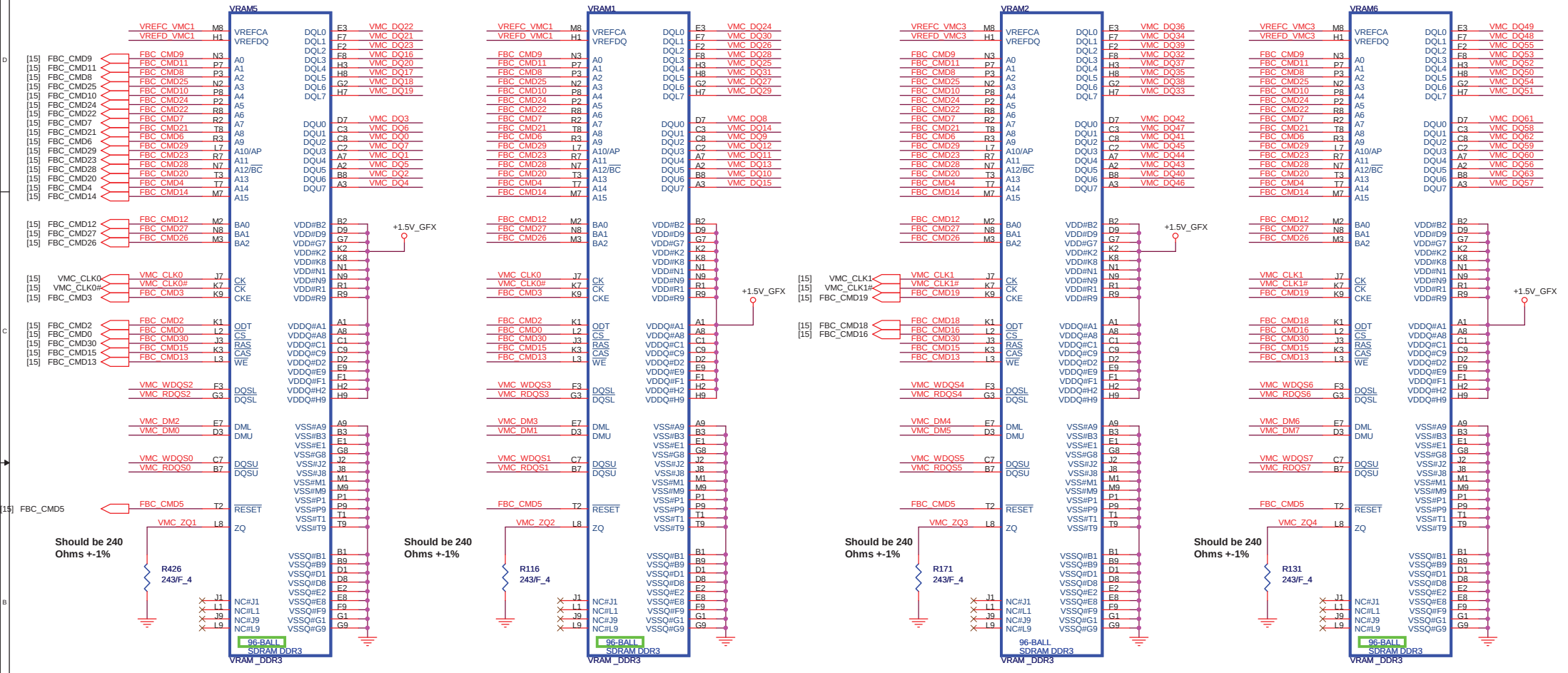
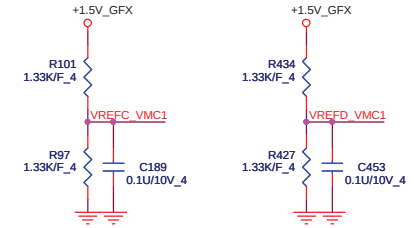
CHANNEL B: 256MB/512MB DDR3

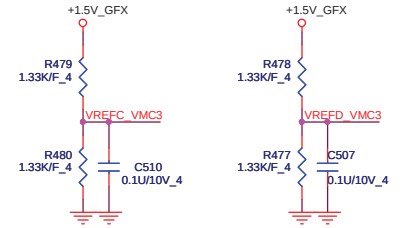
[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

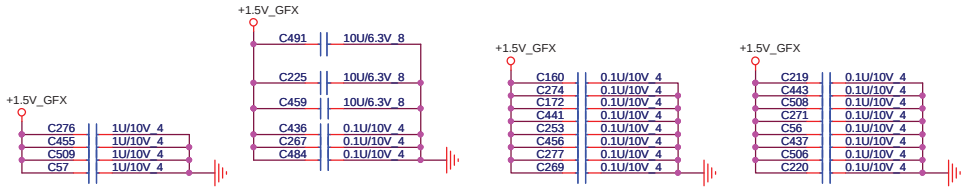


Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)



Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)





[15] FBC_CMD17 — FBC_CMD17 — TP26
[15] FBC_CMD1 — FBC_CMD1 — TP21

[15,19,37,38] +1.5V_GFX

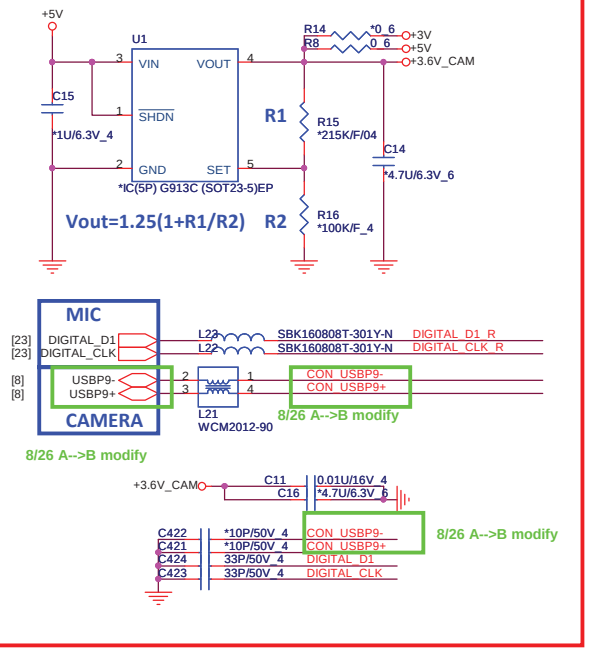
Samsung 900MHz 1G AKD5LGHT500

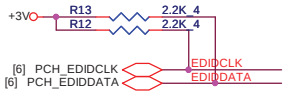
NB5

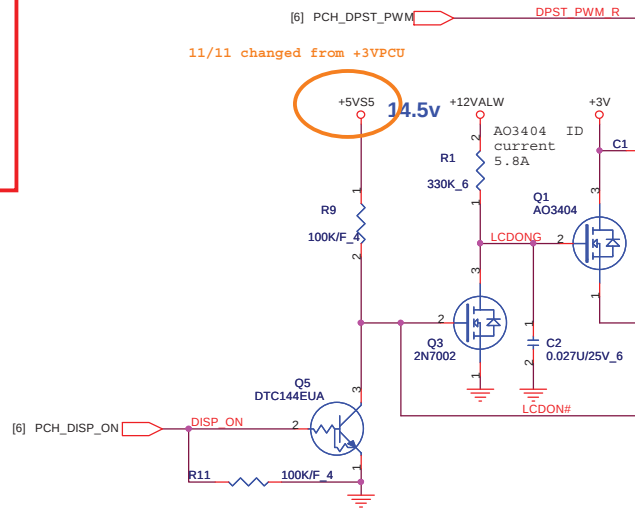
PROJECT : TWH
Quanta Computer Inc.

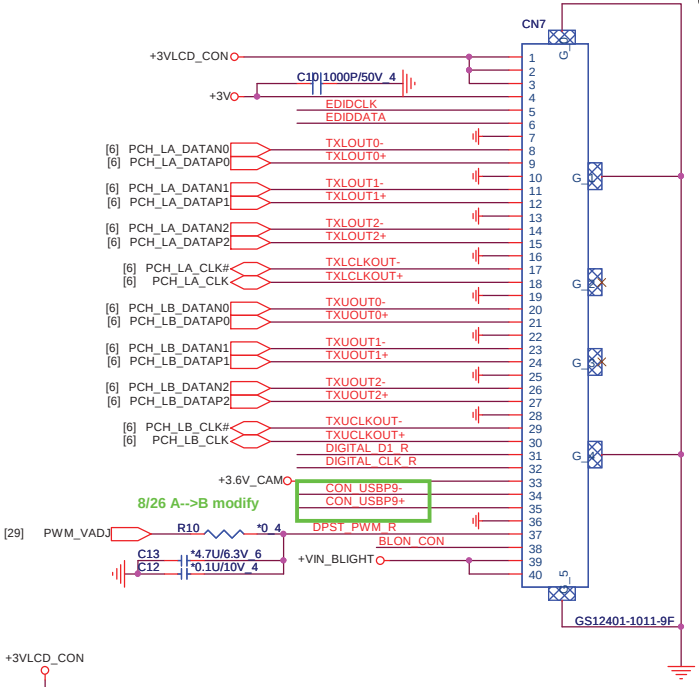
Size	Document Number	Rev
Custom	DGPU Memory 2/2 (DDR3)	A
Date: Monday, November 15, 2010	Sheet 20 of 40	

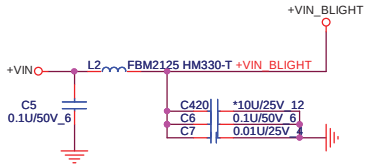
USB Camera Connector

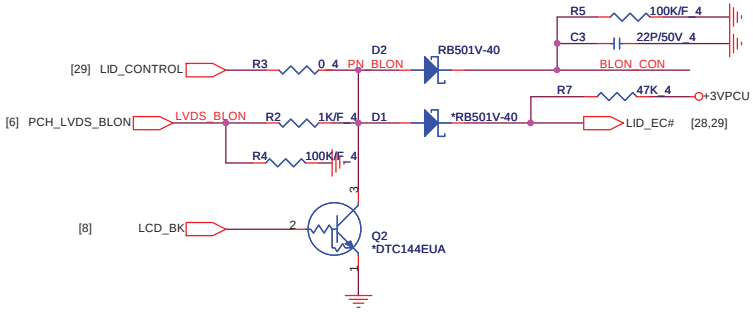












[2,6,7,8,9,10,12,13,14,22,23,24,25,26,27,28,29,34,36,37,39] +3V
[6,7,27,28,29,30,31] +3VPCU
[6,7,10,22,23,27,28,36] +5V
[30,31,32,33,34,35,36,37,38,40] +VIN

PROJECT : TWH
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	A
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CRT PORT

40 MIL

40 mils
+5V F1 +5VCRT FUSE1A6V_POLY +5VCRT
C20 0.1U/10V_4
SSM14 spec is 40V 1A

[6] PCH_CRT_R L4 BLM18BA470SN1D CRT_R_CON
[6] PCH_CRT_G L5 BLM18BA470SN1D CRT_G_CON
[6] PCH_CRT_B L3 BLM18BA470SN1D CRT_B_CON
R44 R45 R46 150/F_4
C43 C39 C40 6.8P/50V_4
C34 C36 C38 6.8P/50V_4
+5VCRT
CRT_DDCDATA_CON C33 *470P/50V_4
CRT_HSYNC_CON C32 *47P/50V_6
CRT_VSYNC_CON C25 *47P/50V_6
CRT_DDCCLK_CON C22 *470P/50V_4
CRT CONN CN9
EMI

Driven Strong

U3 M74VHC1GT125DF2G
[6] PCH_VSYNC CRT_VSYNC CRT_VSYNC_CON
C35 0.1U/10V_4 +5V
[6] PCH_HSYNC CRT_HSYNC CRT_HSYNC_CON
U4 M74VHC1GT125DF2G

Isolation

[6] PCH_DDCCLK CRT_DDCCLK
[6] PCH_DDCDATA CRT_DDCDATA
+3V
R48 *0_4 Q10 2N7002
R47 2.2K_4
R56 2.2K_4
Q13 2N7002 R57 *0_4
R51 *0_4/S short0402 CRT_DDCCLK_CON
R50 4.7K_4
+5VCRT D3 RB501V-40 +5VCRT2
R52 4.7K_4
R53 *0_4/S short0402 CRT_DDCDATA_CON

HDMI PORT

HDMI SMBus Isolation

+3V R126 2.2K_4
[6] SDVO_CLK HDMI_SCL_R Q16 FDV301N HDMI_SCLK
+3V R112 2.2K_4
[6] SDVO_DATA HDMI_SDA_R Q15 FDV301N HDMI_SDATA

+5V_HDMIC C221 *0.01U/16V_4
for EMI request

EMI Solution

C_TX2_HDMI+ R169 *0_4 C_TX2_HDMI-
C_TX1_HDMI+ R161 *0_4 C_TX1_HDMI-
C_TX0_HDMI+ R154 *0_4 C_TX0_HDMI-
C_TXC_HDMI+ R143 *0_4 C_TXC_HDMI-

[6] IN_D2 IN_D2 C266 0.1U/10V_4 C_TX2_HDMI+
[6] IN_D2# C261 0.1U/10V_4 C_TX2_HDMI-
[6] IN_D1 C258 0.1U/10V_4 C_TX1_HDMI+
[6] IN_D1# C255 0.1U/10V_4 C_TX1_HDMI-
[6] IN_D0 C252 0.1U/10V_4 C_TX0_HDMI+
[6] IN_D0# C249 0.1U/10V_4 C_TX0_HDMI-
[6] IN_CLK C242 0.1U/10V_4 C_TXC_HDMI+
[6] IN_CLK# C237 0.1U/10V_4 C_TXC_HDMI-
CN13 HDMI CONN
SHELL1 D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CEC Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL2
CH751H-40GP D19 D18
5V_HSMBCK R468 2.2K_4
5V_HSMBDT R467 2.2K_4
HDMI_SCLK HDMI_SDATA
C228 C232 *10P/50V_4
+5V F2 FUSE1A6V_POLY +5V_HDMIC
[29] HDMI_HPD HDMI_DET_N R114 10K/F_4 L11 HDMI_DET_C BLM18BA470SN1D
C214 220P/50V_4
D4 BAV99W +3V R113 110K/F_4
B-stage change
10/8 add for EMI
11/11 pin 13,17 -> NC
for HDMI 7-13 test issue

+3V Q18 2N7002
DGPU_CL_HDMIP
R472 680/F_4 C_TX2_HDMI+
R471 680/F_4 C_TX2_HDMI-
R469 680/F_4 C_TX1_HDMI+
R466 680/F_4 C_TX1_HDMI-
R464 680/F_4 C_TX0_HDMI+
R461 680/F_4 C_TX0_HDMI-
R458 680/F_4 C_TXC_HDMI+
R455 680/F_4 C_TXC_HDMI-
9/1 change to 680ohm
8/31UMA/OPTIMUS-680 ohm, DISCRETE-499 ohm

R449 0_4 +3V
R450 *0_4 +3V_GFX
Q39 MMBT3904-7-F
HDMI_DET_P R451 150K/F_4 HDMI_HPD
[6] HDMI_HPD_CON HDMI_HPD_3V
R465 10K_4
R452 *348K/F_4

NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Connector	A
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Internal Speaker

INT SPEAKER CONN

9/8 EMI need change to 680p

9/5 add de-pop circuit, add
C1002,C1003,C1004
Q1005,Q1006,Q1007
R1007,R1008,R1009,R1010,R1011,R1012,R1013,R1014

9/5 "PD#" circuit modify
1.delete R650,R372,R373,Q27,Q28,D16,D17,D15
2.add Q1002,Q1003,Q1004,R1004,R1005,R1006

10/5 change VB6

11/12 short

8/26 A-->B modify

9/8 EMI(near CN18)

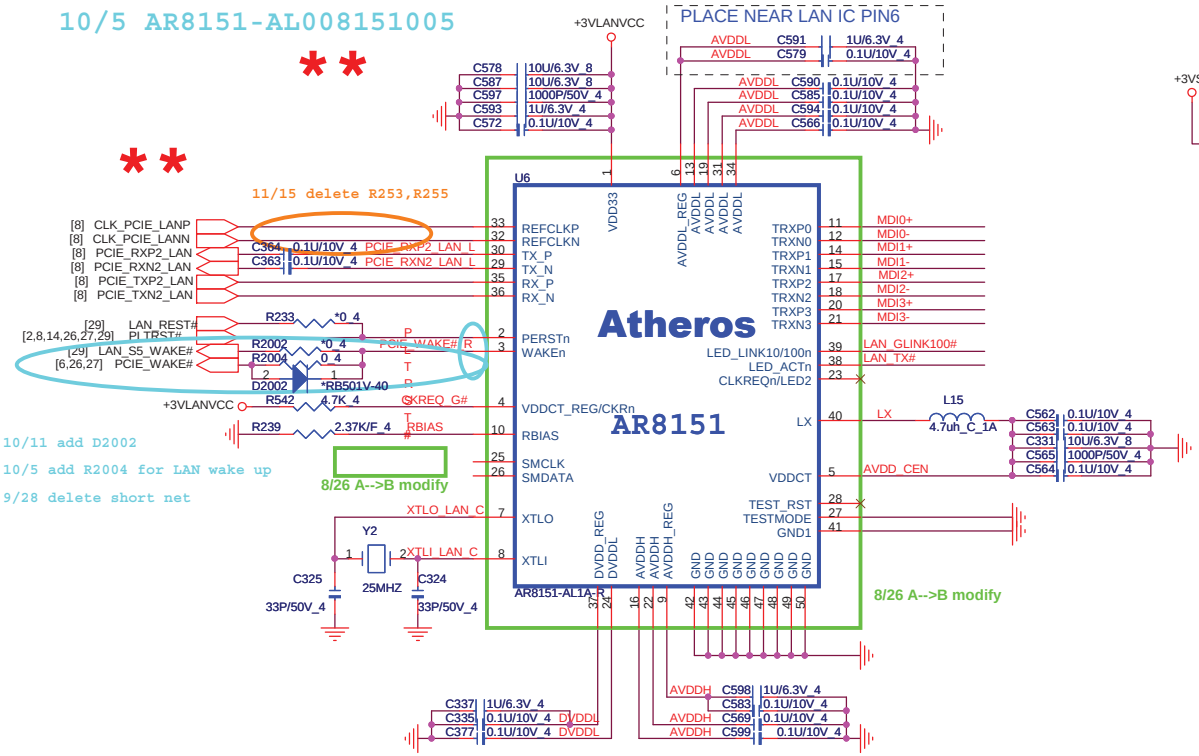
10/8 change net name

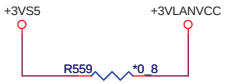
10/11 R361 mount, other unmount

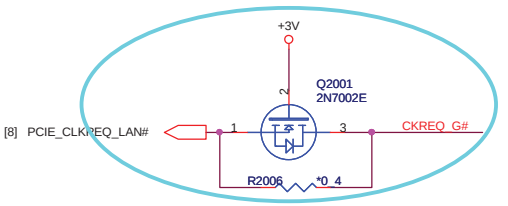
ALC269Q-VB6-GR

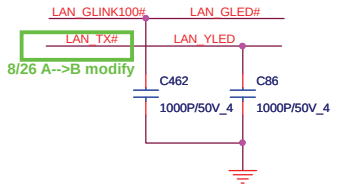
DUAL USB CONN

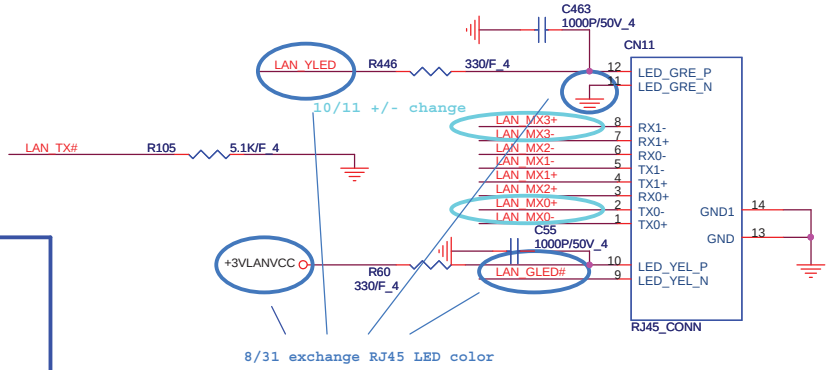
Atheros Lan

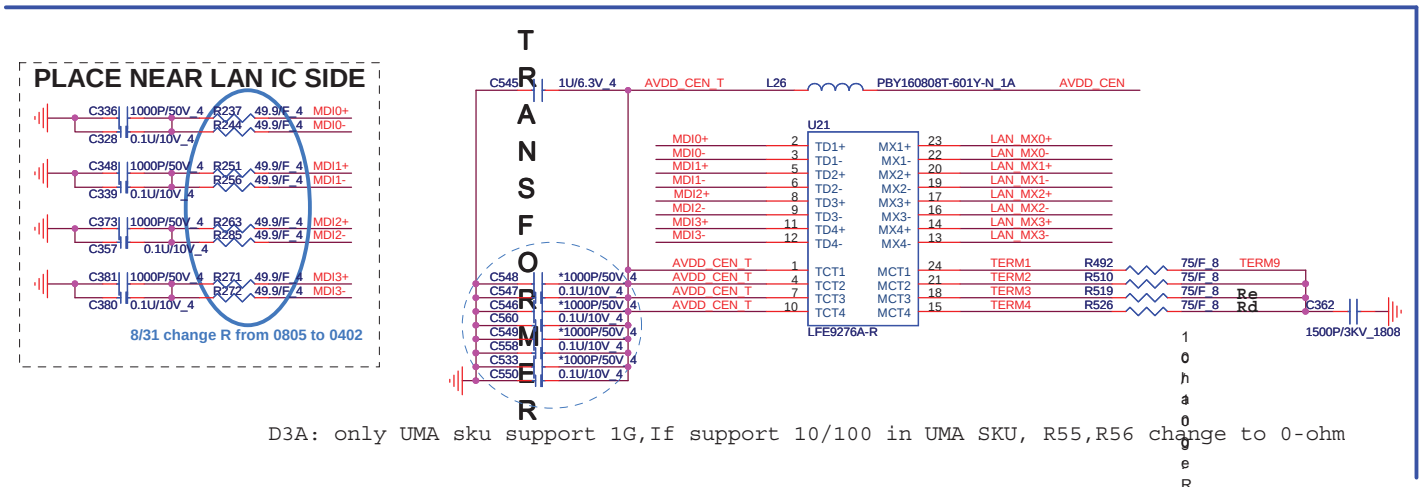












D3A: only UMA sku support 1G,If support 10/100 in UMA SKU, R55,R56 change to 0-ohm

NB5	PROJECT : TWH Quanta Computer Inc.	
Size: Custom	Document Number: LAN Controller (Atheros_AR8151)	Rev: A
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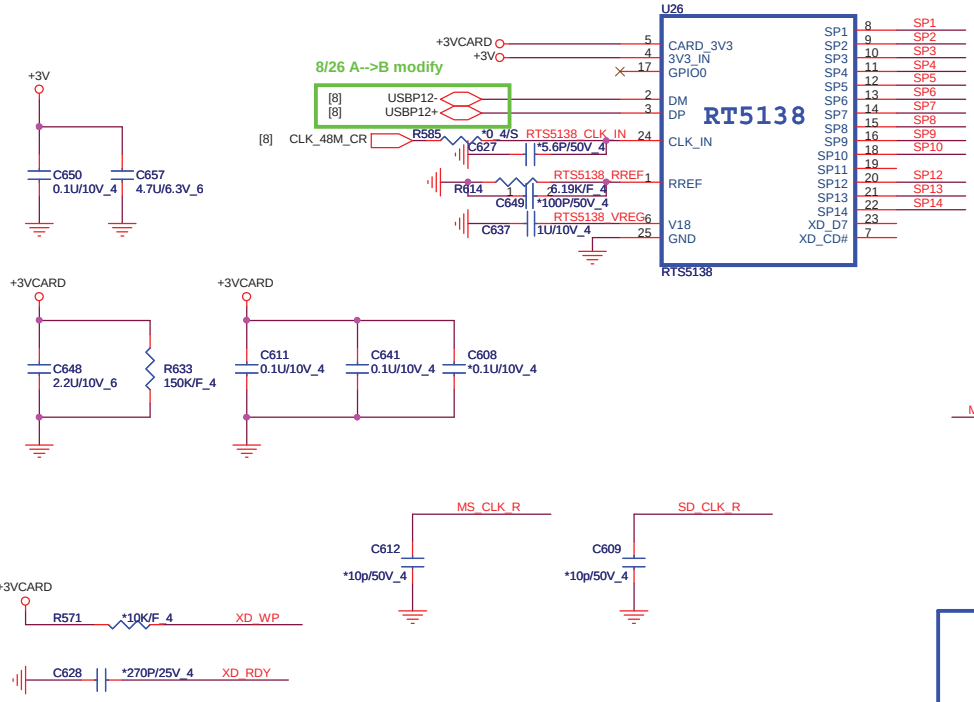
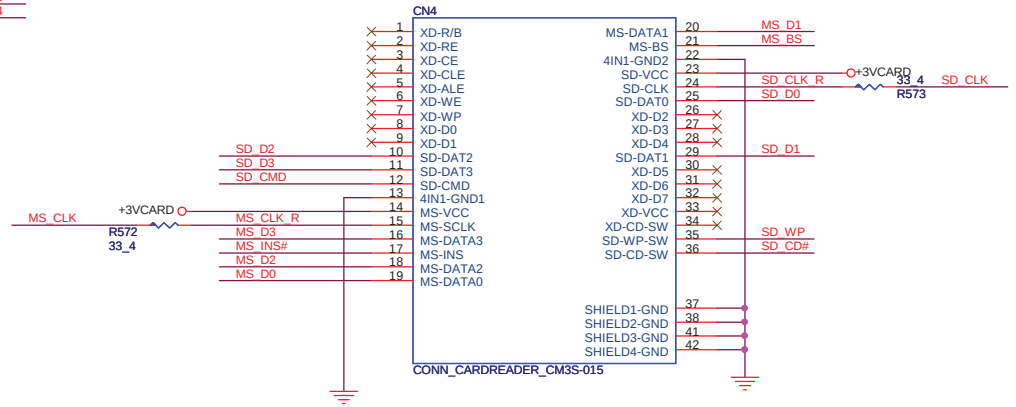
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS

Share Pin





System Screw Hold

9/9 ME modify FP

HS1 *H-C315D110P2
HS2 *H-C315D110P2
HS3 *H-C236D110P2
HS4 *O-TWH-4
HS5 *h-tc472bc315d110p2
HS6 *H-C315D110P2
HS7 *h-tc472bc315d110p2
HL1 *H-C394D157P2

H5 *H-TS394BC315D110P2
H3 *H-TS394BC315D110P2
H4 *H-TS394BC315D110P2
H1 *h-tr315x295br394x295d110p2
H6 *O-TWH-2
H7 *H-C110D110N
H2 *H-C110D110N
H8 *O-TWH-3

System Pad(Top)

P1 P2 P3 P4 P5 P6 P7 P8 B2

H9 *O-TWH-3
H10 *O-TWH-3

System Pad(Button)

P9 P10 P11 P13 P12 P14 B3

CPU Bracket

HC1 *H-TC276BC197D150P2
HC2 *H-TC276BC197D150P2
HC3 *H-TC276BC197D150P2
HC4 *H-TC276BC197D150P2

GPU Bracket

HG1 *H-TC276BC197D150P2
HG2 *H-TC276BC197D150P2
HG3 *H-TC276BC197D150P2

MDC NU Screw Hold

9/6 delete MDC function
ND1,ND2

PCH NU Screw Hold

NP1 *H-C256D122P2
NP2 *H-C256D122P2
NS1 *H-C256D67P2
NL1 *H-C256D161P2

PROJECT : TWH
Quanta Computer Inc.

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Size	Document Number	Rev
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check ??

VIA VL801

U27

PORT1

PORT2

PORT3

PORT4

USB3.0 X 2/USB2.0 COMBO

USB 3.0

USB 3.0

11/12 add

8/26 A-->B modify

11/15 add for S3 issue debug

11/10 modify

11/10 cost down

10/5 Support flash
- MX25L512, MX25L5121E,
- SST25VF512, SST25VF010A
- EN25F05, EN25F10

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USB 3.0 Controller (TI_TUSB7320)

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Mini Card WLAN/BT(Option)

9/4
1.change net name "+MINIEC_5V" to "INT_BT_OFF#"
2.add R1003, net name "INT_BT_OFF#"

EC debug pin

9/28 modify

9/3 delete BT function (USB)
delete net "BLUELED", R18

11/11 mount

9/6 power changed from +3V to +3V_WLAN_P

CN8
MLX_67910-5700
MIPCIEXP-1775838-1-52P

9/6 add "RF_PWR_OFF#" control from PCH

9/6 R17-stuff, R20-unstuff

Avoid leakage issue

PIN44

PIN7

PIN5

Mini Card Reset

U2
MC74VHC1G08DFT2G

Support Wake Function(Reserve)

For EMI Suggestion

LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

LED Status

(Orange)
(White)
(White)
(White)

19-22SURSYGC/S530-A2/TR8

9/3 delete BT function (USB)
delete net "BLUELED", Q31

MDC Connector(Option)

9/3 delete MDC function
R538, C570
CN15
C308, R192, R193, C307, C309, C306, C305
"ACZ_SDOUT_MDC"
"ACZ_SYNC_MDC"
"ACZ_SDIN1"
"ACZ_RST#_MDC"
"BIT_CLK_MDC"

PIN19,51

9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

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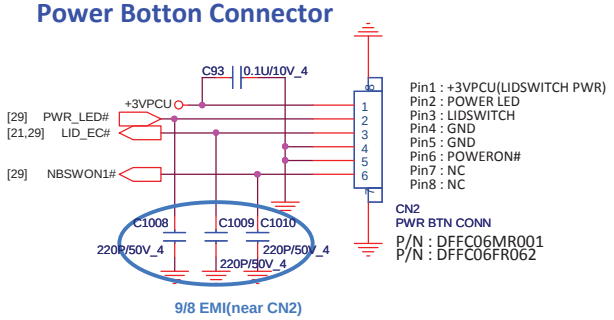
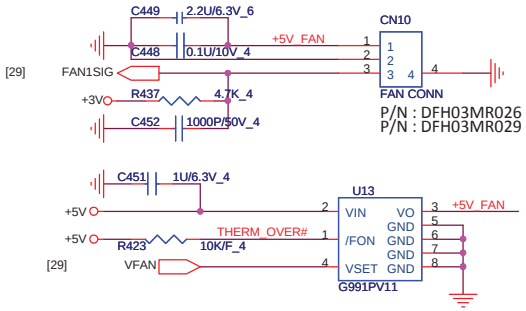
Power Botton Connector



9/8 EMI(near CN2)

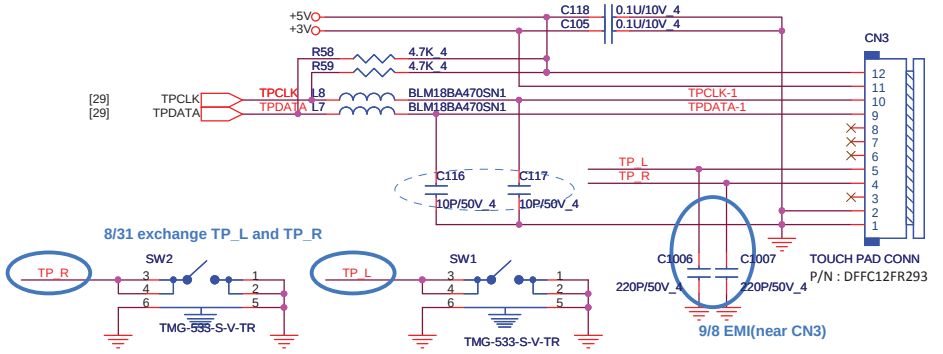
CPU FAN



Touch Pad Connector

B-stage change footprint to BL121-12R-TAND-12P-L

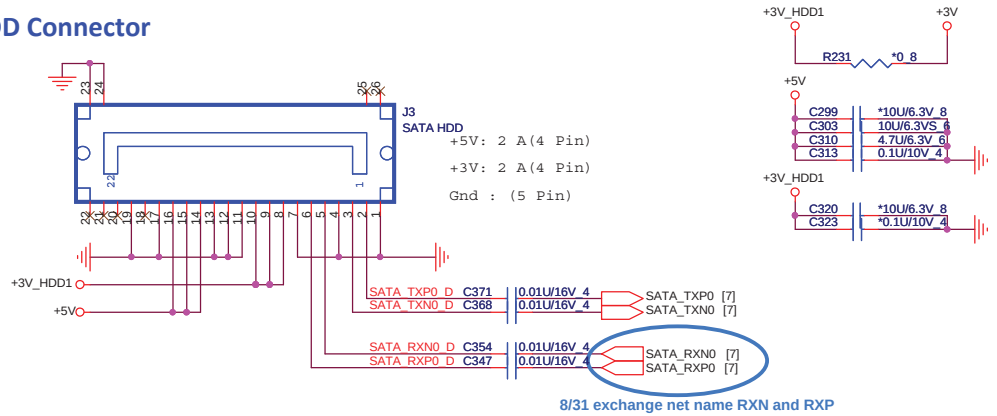
25 mils



8/31 exchange TP_L and TP_R

9/8 EMI(near CN3)

SATA HDD Connector

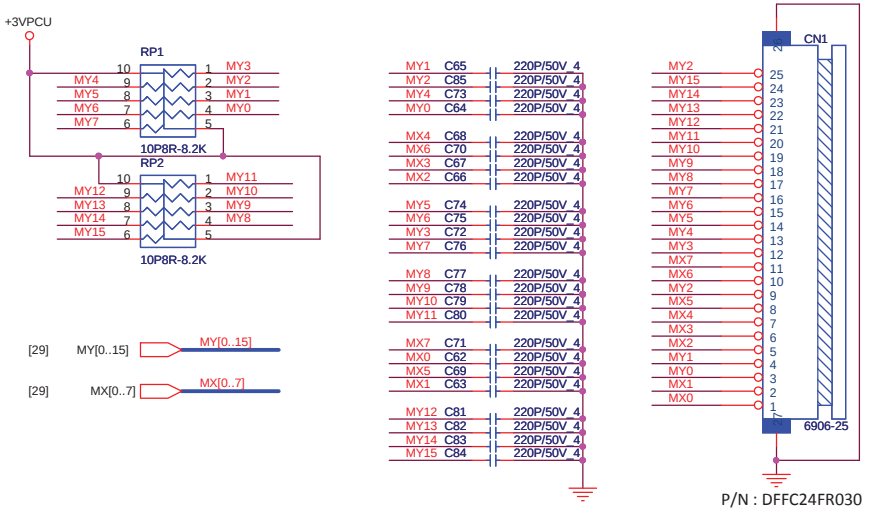


8/31 exchange net name RXN and RXP

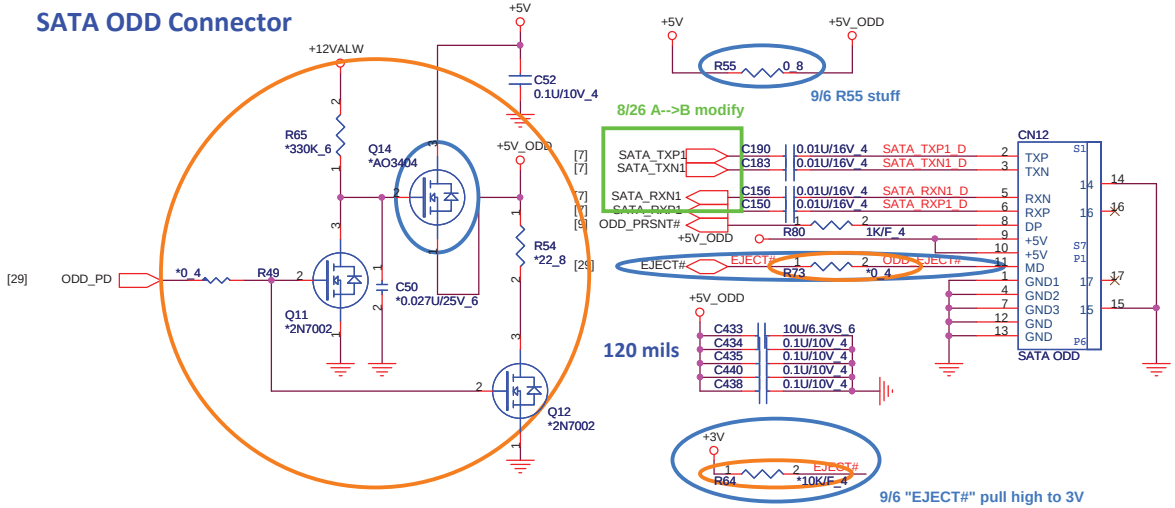
BT Connector

8/31 delete BT function (USB)
delete CN20, net "BT_OFF#","BLUELED","USB8+","USB8-"

Keyboard Connector



SATA ODD Connector



[2,4,10,27] +1.5V_CPU
[2,6,7,8,9,10,12,13,14,21,22,23,24,25,26,27,29,34,36,37,39] +3V
[6,7,10,21,22,23,27,36] +5V

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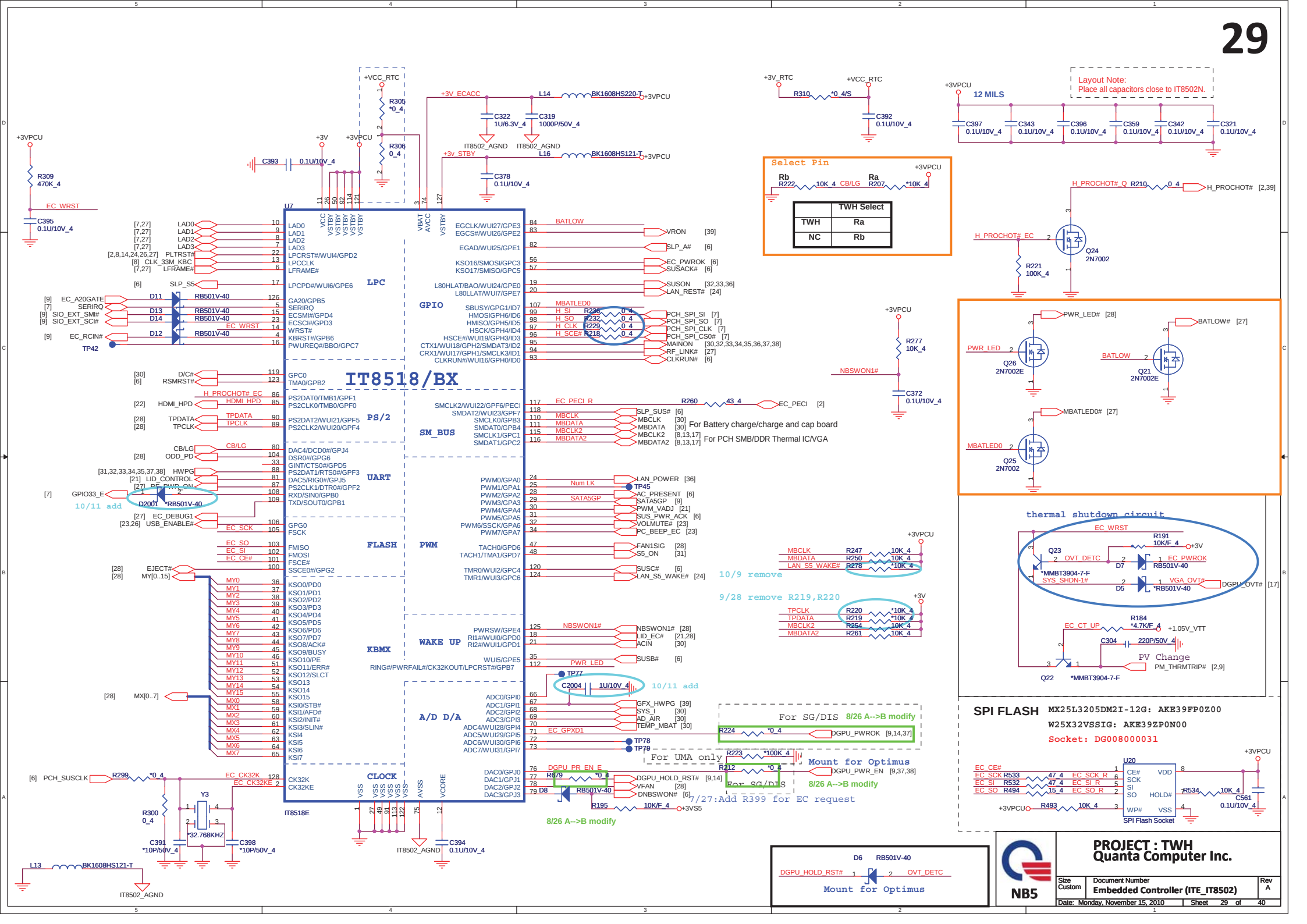
IT8518/BX
U7
IT8518E
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
Select Pin
TWH Select
TWH Ra
NC Rb
Layout Note:
Place all capacitors close to IT8502N.
12 MILS
thermal shutdown circuit
SPI FLASH MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031
For Battery charge/charge and cap board
For PCH SMB/DDR Thermal IC/VGA
10/11 add
10/9 remove
9/28 remove R219,R220
8/26 A-->B modify
For UMA only
Mount for Optimus
For SG/DIS
7/27:Add R399 for EC request
PV Change
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Embedded Controller (ITE_IT8502)
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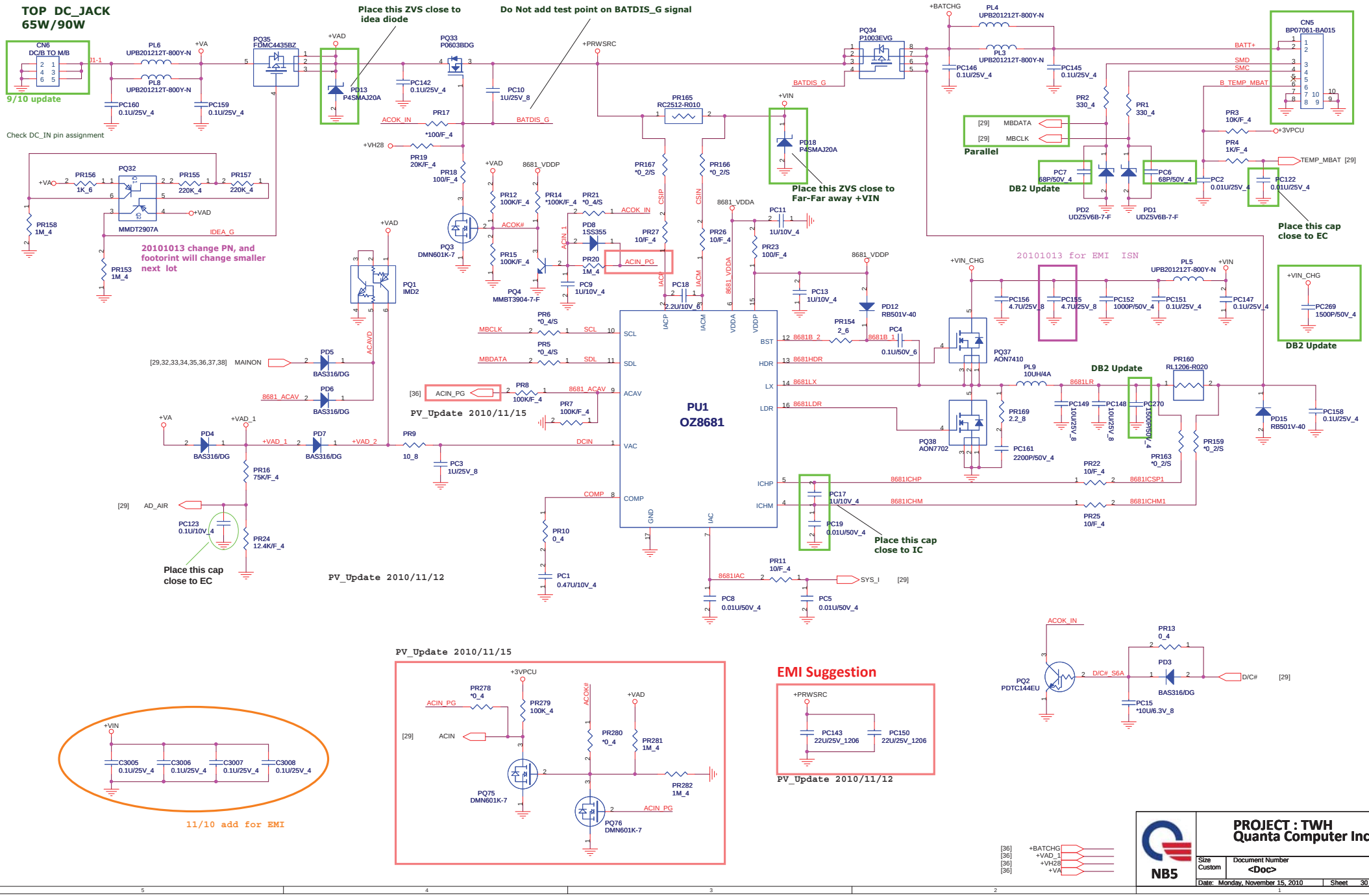
TOP DC_JACK
65W/90W
9/10 update
Check DC_IN pin assignment
Place this ZVS close to idea diode
Do Not add test point on BATDIS_G signal
20101013 change PN, and footorint will change smaller next lot
PU1
OZ8681
PV_Update 2010/11/15
PV_Update 2010/11/12
Parallel
DB2 Update
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
Place this cap close to IC
20101013 for EMI ISN
EMI Suggestion
11/10 add for EMI
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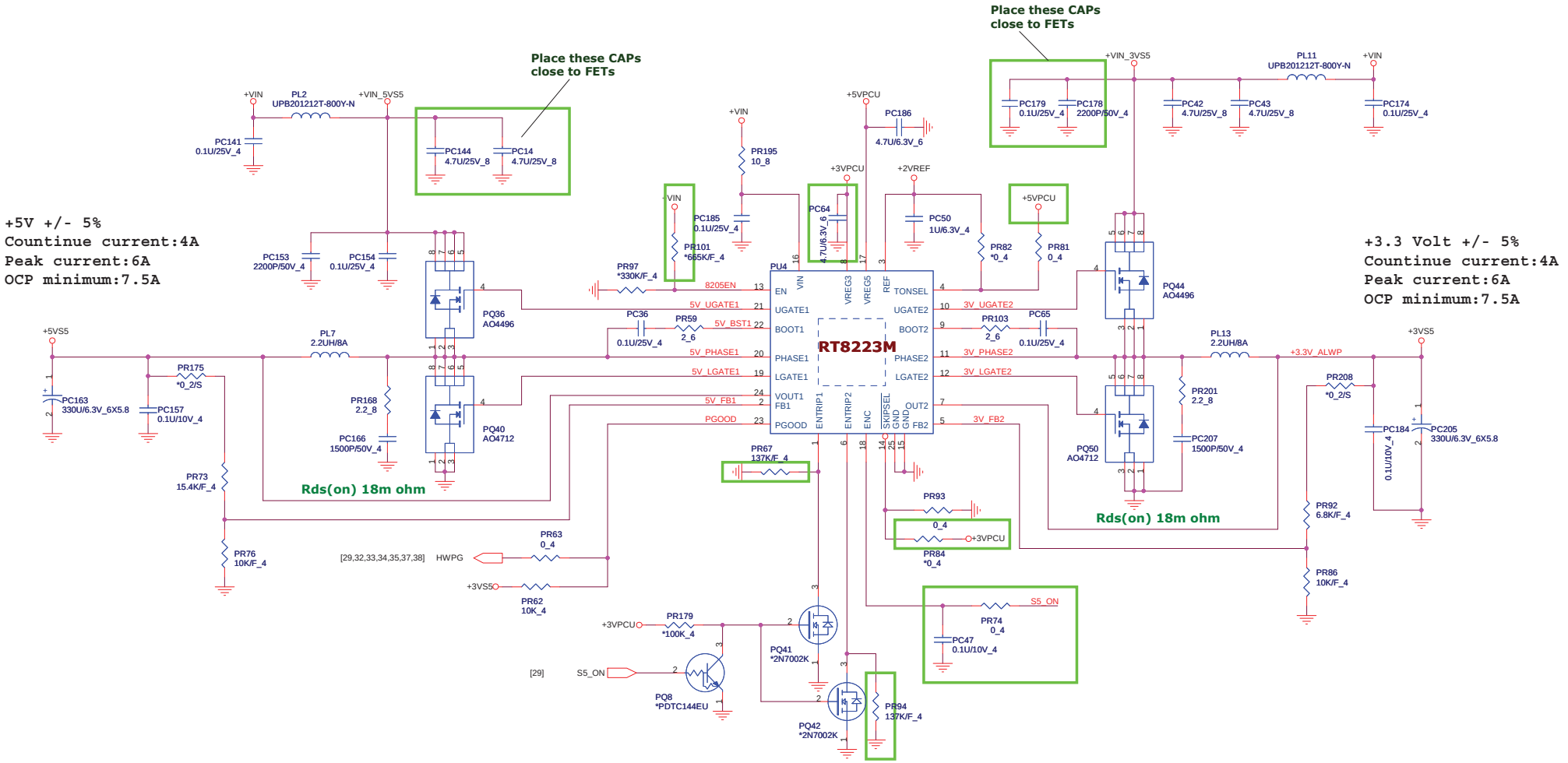
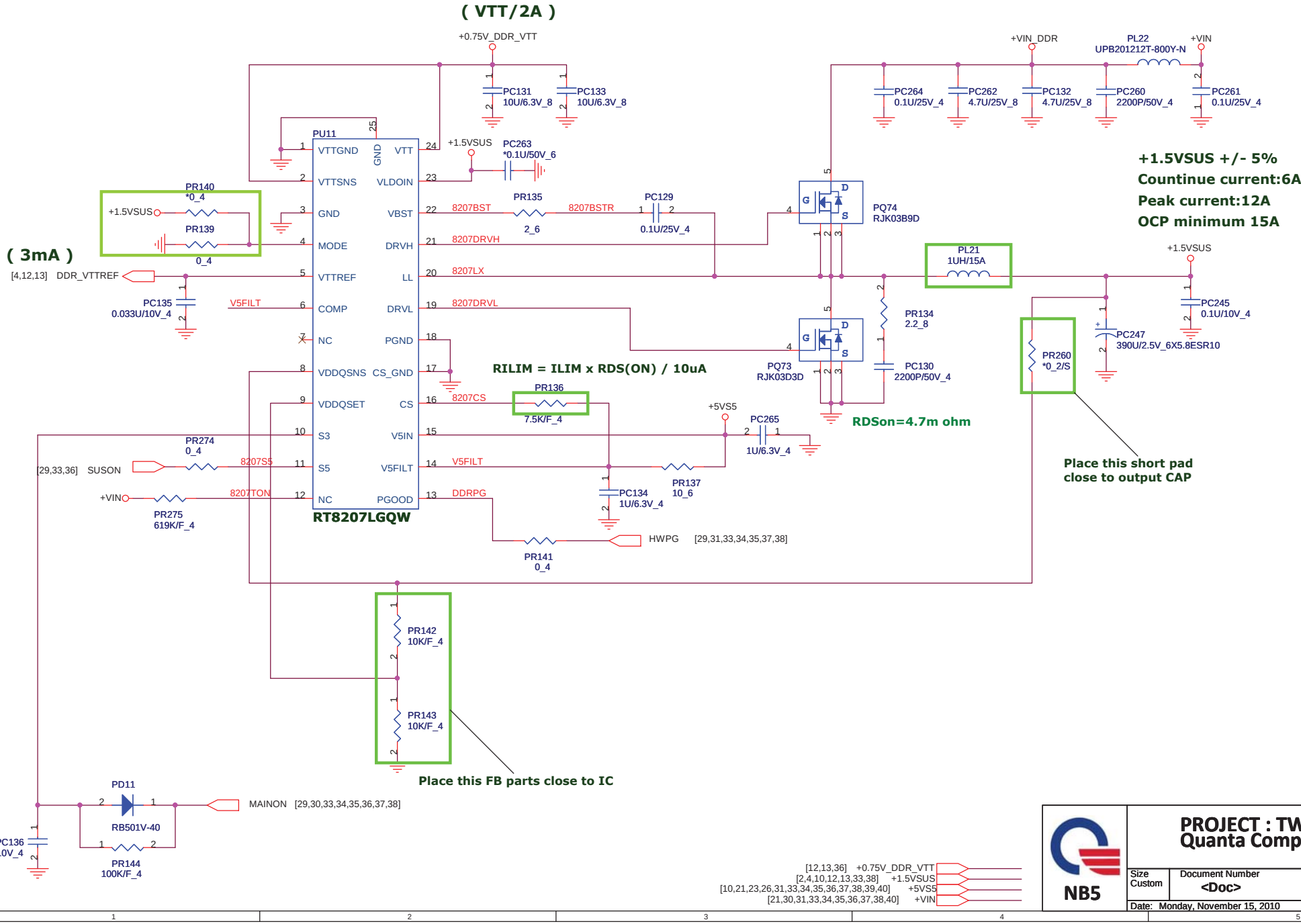

+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
Place these CAPs close to FETs
Place these CAPs close to FETs
RT8223M
Rds(on) 18m ohm
Rds(on) 18m ohm
PL2 UPB201212T-800Y-N
PL11 UPB201212T-800Y-N
PL7 2.2UH/8A
PL13 2.2UH/8A
PU4
PQ36 AO4496
PQ40 AO4712
PQ44 AO4496
PQ50 AO4712
PQ41 *2N7002K
PQ42 *2N7002K
PQ8 *PDTC144EU
PR195 10_8
PR101 *665K/F_4
PR97 *330K/F_4
PR67 137K/F_4
PR73 15.4K/F_4
PR76 10K/F_4
PR63 0_4
PR62 10K_4
PR93 0_4
PR84 *0_4
PR179 *100K_4
PR74 0_4
PR94 137K/F_4
PR82 *0_4
PR81 0_4
PR103 2_6
PR59 2_6
PR175 *0_2/S
PR168 2.2_8
PR201 2.2_8
PR208 *0_2/S
PR92 6.8K/F_4
PR86 10K/F_4
PC36 0.1U/25V_4
PC65 0.1U/25V_4
PC50 1U/6.3V_4
PC64 4.7U/6.3V_6
PC186 4.7U/6.3V_6
PC185 0.1U/25V_4
PC141 0.1U/25V_4
PC144 4.7U/25V_8
PC14 4.7U/25V_8
PC153 2200P/50V_4
PC154 0.1U/25V_4
PC166 1500P/50V_4
PC163 330U/6.3V_6X5.8
PC157 0.1U/10V_4
PC179 0.1U/25V_4
PC178 2200P/50V_4
PC42 4.7U/25V_8
PC43 4.7U/25V_8
PC174 0.1U/25V_4
PC207 1500P/50V_4
PC184 0.1U/10V_4
PC205 330U/6.3V_6X5.8
PC47 0.1U/10V_4
+VIN
+VIN_5VS5
+VIN_3VS5
+5VPCU
+3VPCU
+2VREF
+5VS5
+3VS5
+3.3V_ALWP
8205EN
5V_UGATE1
5V_BST1
5V_PHASE1
5V_LGATE1
5V_FB1
PGOOD
3V_UGATE2
3V_PHASE2
3V_LGATE2
3V_FB2
S5_ON
HWPG
[29,32,33,34,35,37,38]
[29]
EN
VIN
UGATE1
BOOT1
PHASE1
LGATE1
VOUT1
FB1
PGOOD
VREG3
VREG5
REF
TONSEL
UGATE2
BOOT2
PHASE2
LGATE2
OUT2
FB2
ENTRIP1
ENTRIP2
ENC
SKIPSEL
GND
GND
GND



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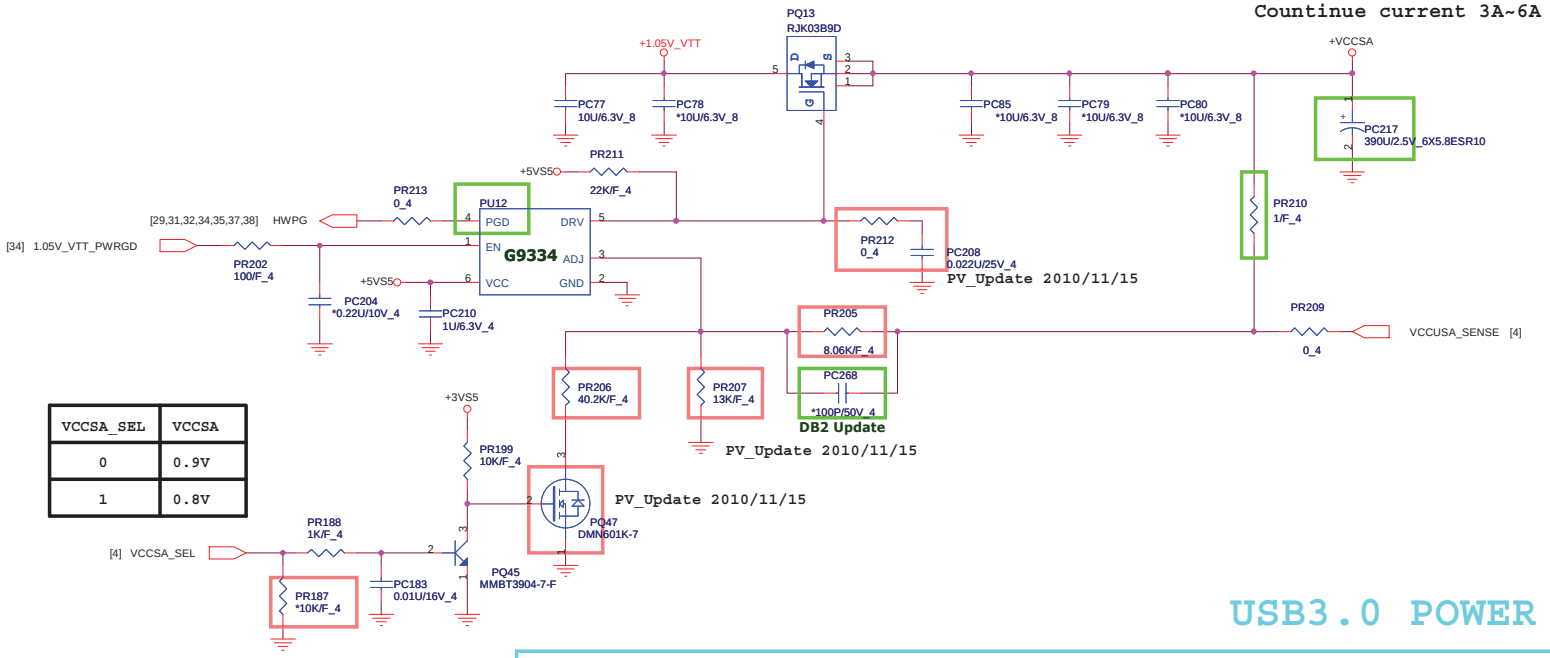
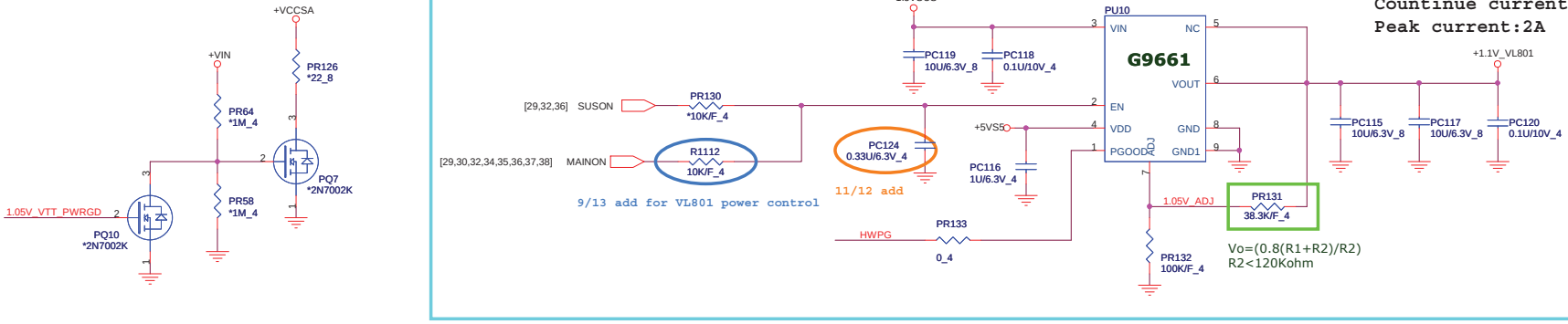
VCCSA (0.9V) +/- 5%
Countinue current 3A~6A



VCCSA_SEL	VCCSA
0	0.9V
1	0.8V

USB3.0 POWER

+1.1V +/- 5%
Countinue current:650mA
Peak current:2A



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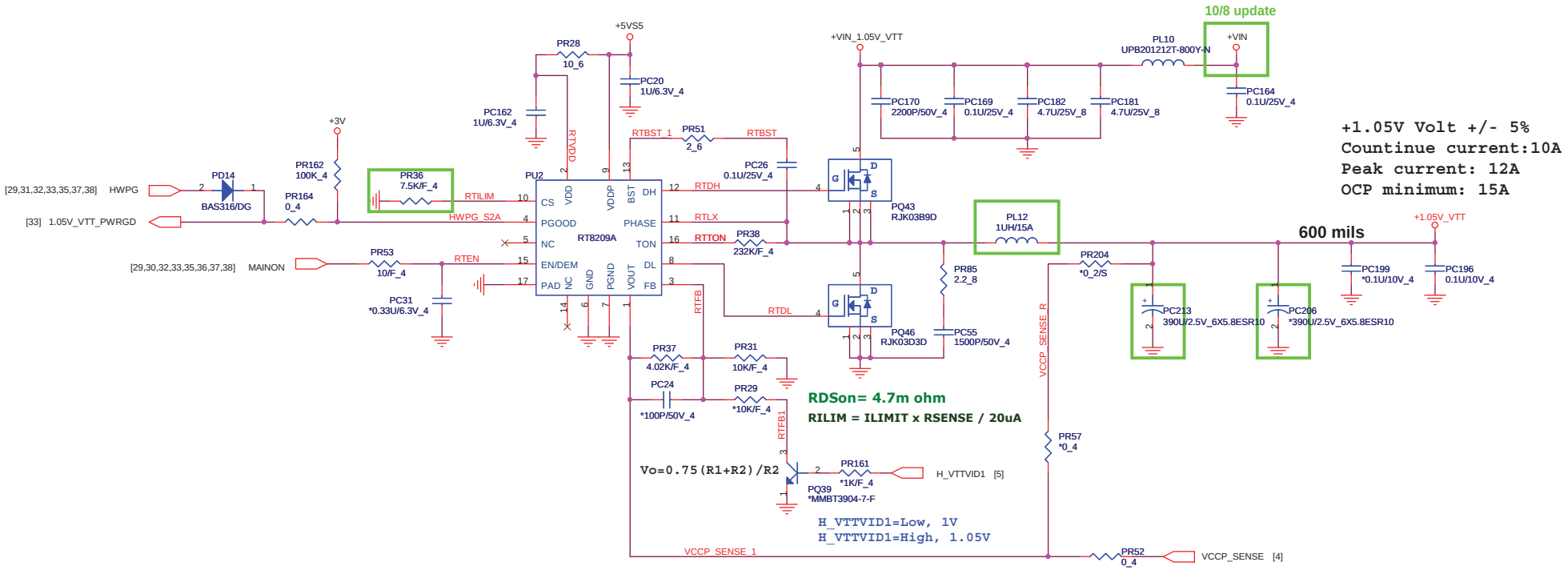

NB5	PROJECT : TWH Quanta Computer Inc.		
	Size: Custom	Document Number: <Doc>	Rev: A
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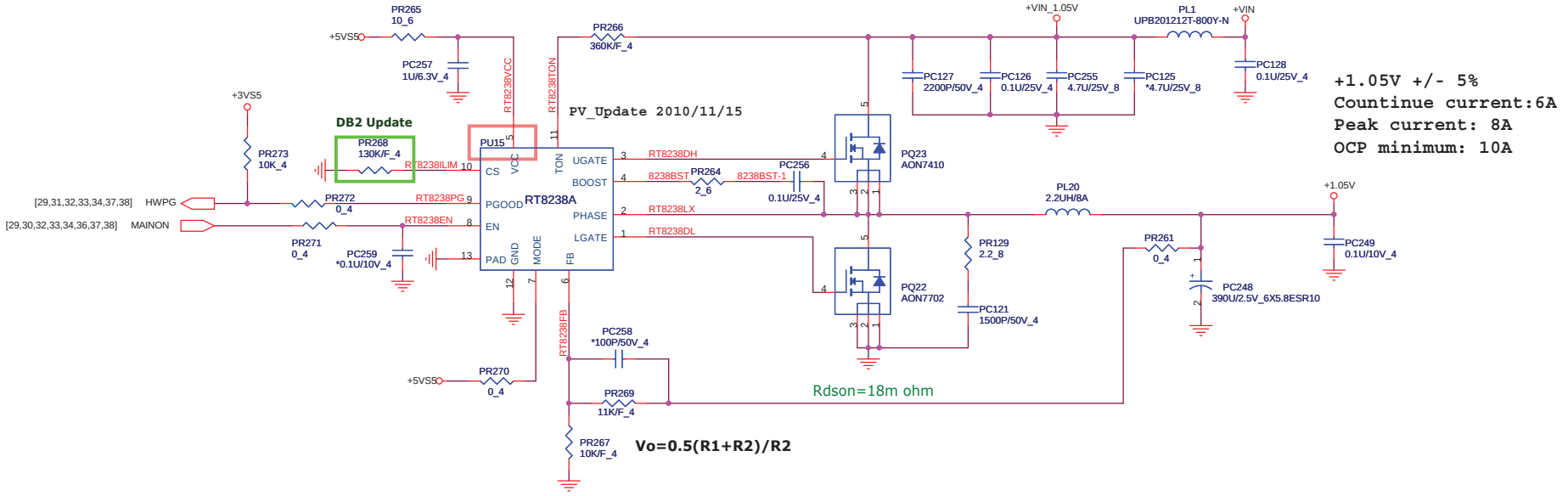

NB5	PROJECT : TWH Quanta Computer Inc.	
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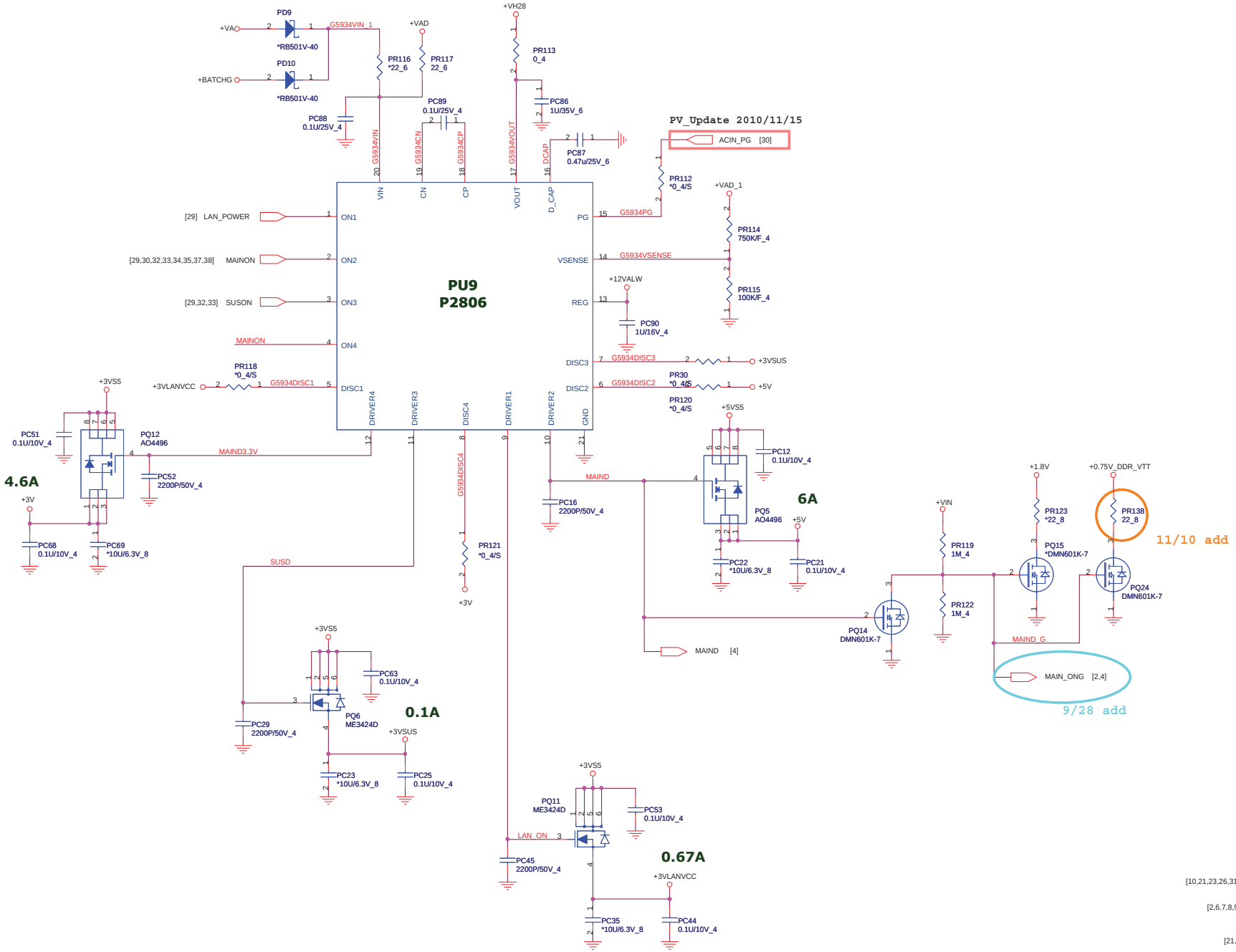

[12,13,32] +0.75V_DDR_VTT
[24] +3VLANVCC
[2,4,10,12,13,32,33,38] +1.5VSUS
[30] +BATCHG
[21,28,38] +12VALW
[10,21,23,26,31,32,33,34,35,37,38,39,40] +5VS5

[2,6,7,8,9,10,14,24,29,31,33,35,38] +3VS5
[30] +VAD_1
[30] +VH28
[4,7,10,38] +1.8V
[21,30,31,32,33,34,35,37,38,40] +VIN
[6,7,10,21,22,23,27,28] +5V
[30] +VA

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ciucuit default is N12E

VGA type	PQ17 PQ19 PQ16 PQ18	PR252
N12E peak 53.4A	POP(SMT)	1.37K
N12P peak 35.32A	NA(no SMT)	806 ohm (CS18062FB29)

Nvideo N12E

CNTRL1 GPIO6	CNTRL0 GPIO5	N11E-GE
0	0	0.9125V
0	1	0.8625V
1	0	0.8125V
1	1	N/A

PR230=180K PR232=49.9K PR226=681K
PR227=324K

Nvideo N12P

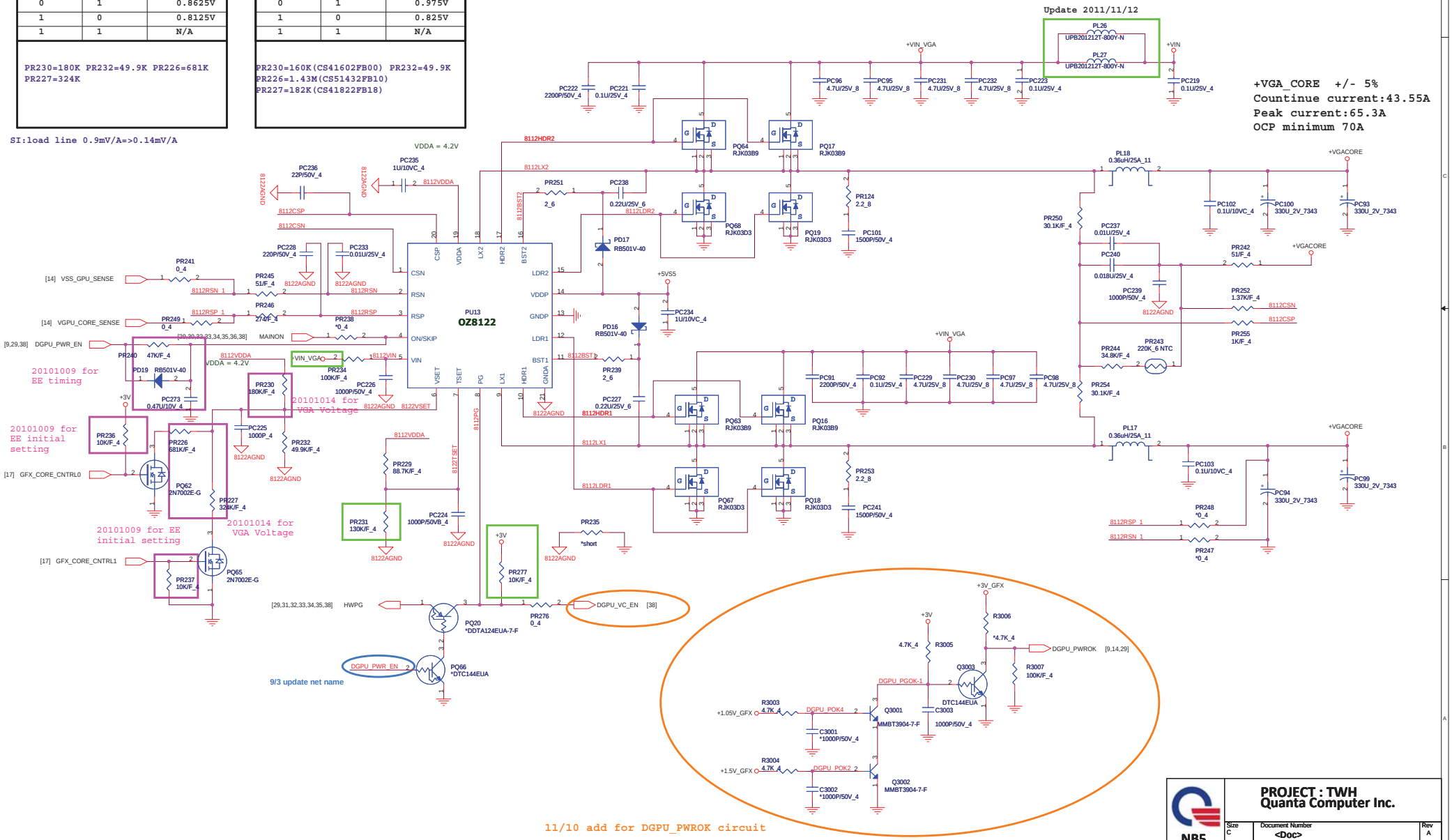
CNTRL1 GPIO6	CNTRL0 GPIO5	N11E-GE
0	0	1V
0	1	0.975V
1	0	0.825V
1	1	N/A

PR230=160K(CS41602FB00) PR232=49.9K
PR226=1.43M(CS51432FB10)
PR227=182K(CS41822FB18)

SI:load line 0.9mV/A=>0.14mV/A

Update 2011/11/12

+VGA_CORE +/- 5%
Countinue current:43.55A
Peak current:65.3A
OCP minimum 70A



11/10 add for DGPU_PWROK circuit

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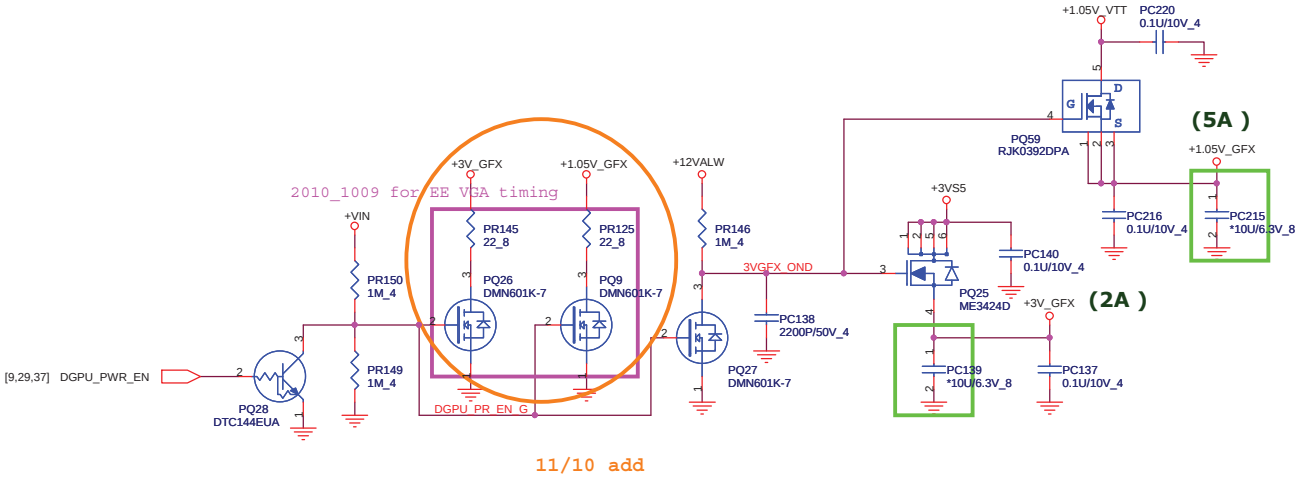
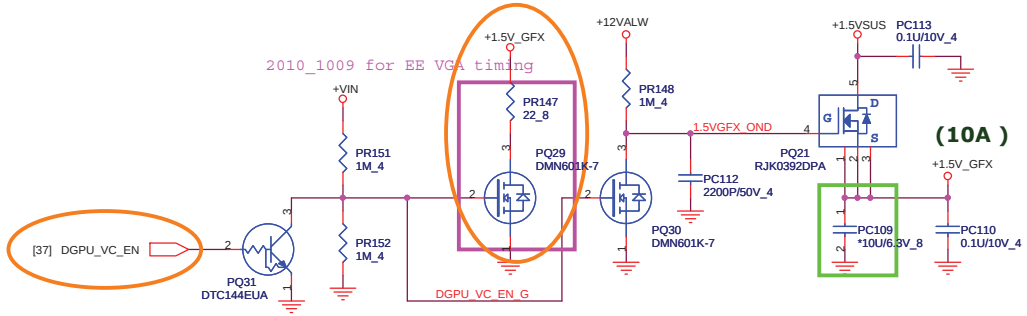
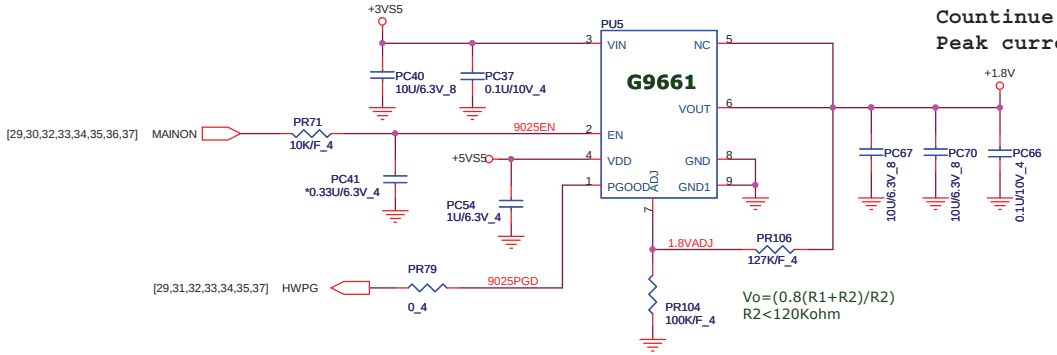
VGA Core



11/10 add





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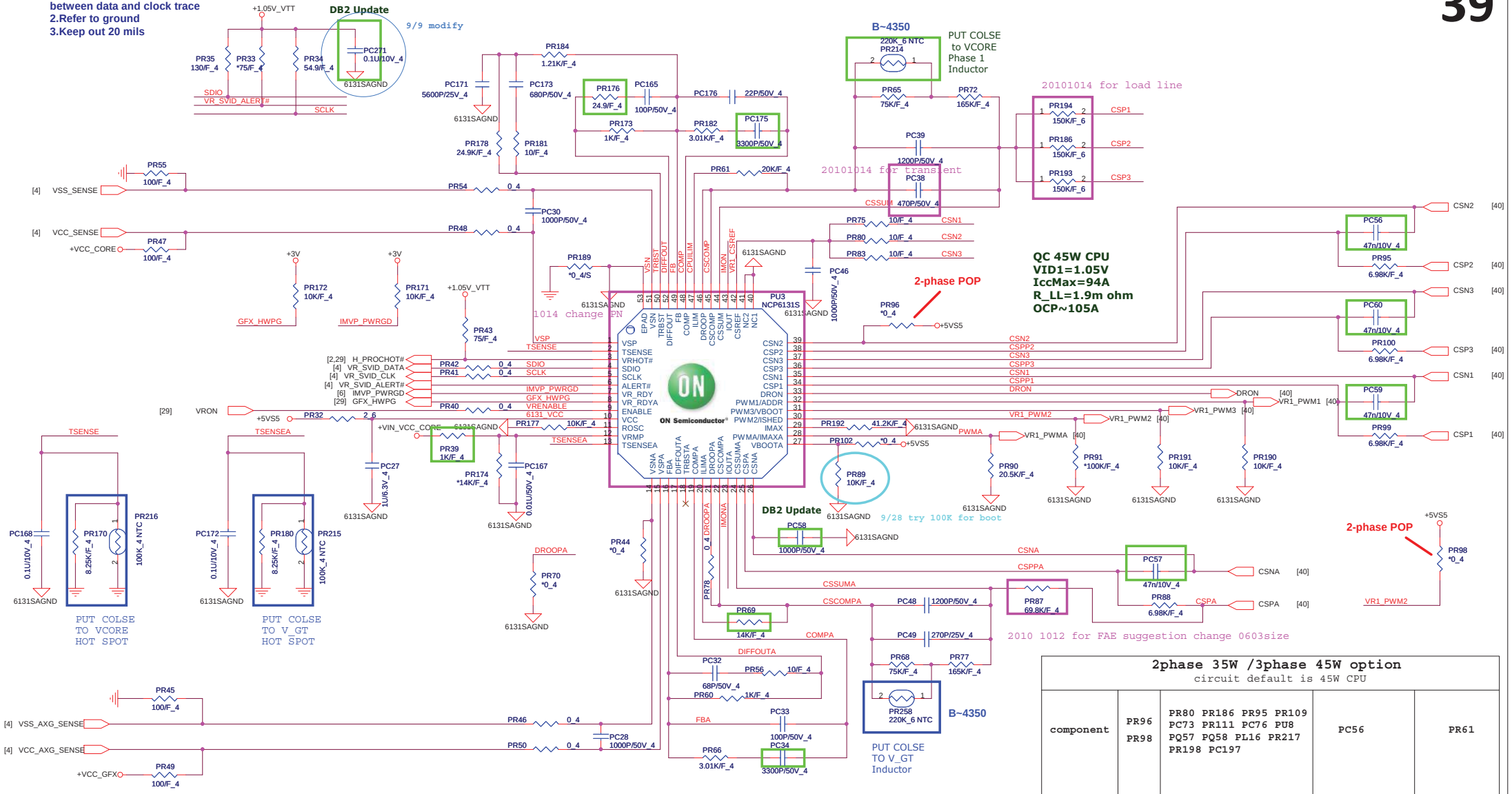
1.Alert trace routing
between data and clock trace
2.Refer to ground
3.Keep out 20 mils



2phase 35W /3phase 45W option circuit default is 45W CPU				
component	PR96 PR98	PR80 PR186 PR95 PR109 PC73 PR111 PC76 PU8 PQ57 PQ58 PL16 PR217 PR198 PC197	PC56	PR61
2phase 35WCPU	POP	NA(NO SMT)	Change to 0ohm (CS00002JB38)	12.1K (CS31212FB28) OCP 65A
3Phase 45WCPU	NA	POP(SMT)	POP	20K OCP 105A

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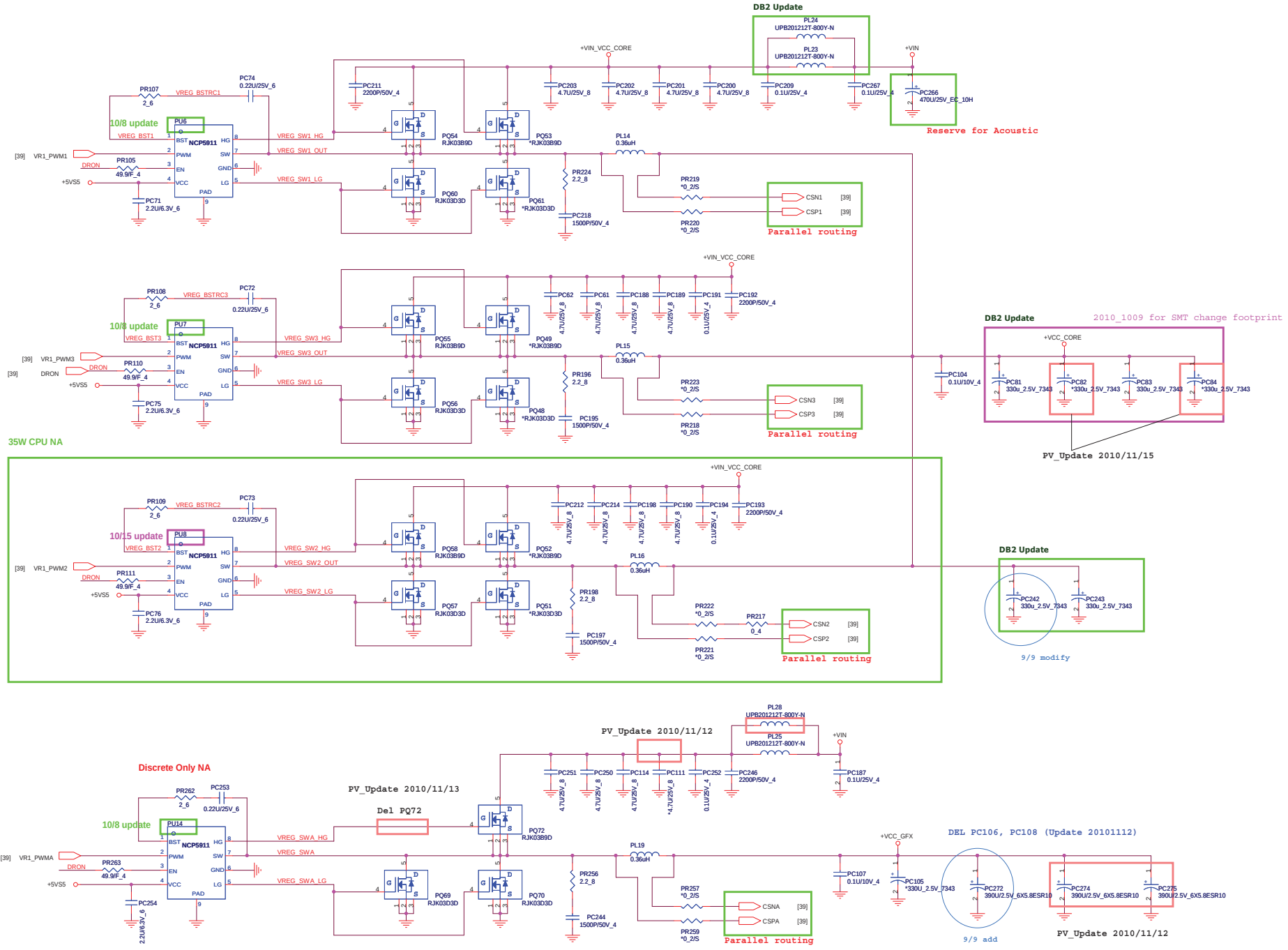

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