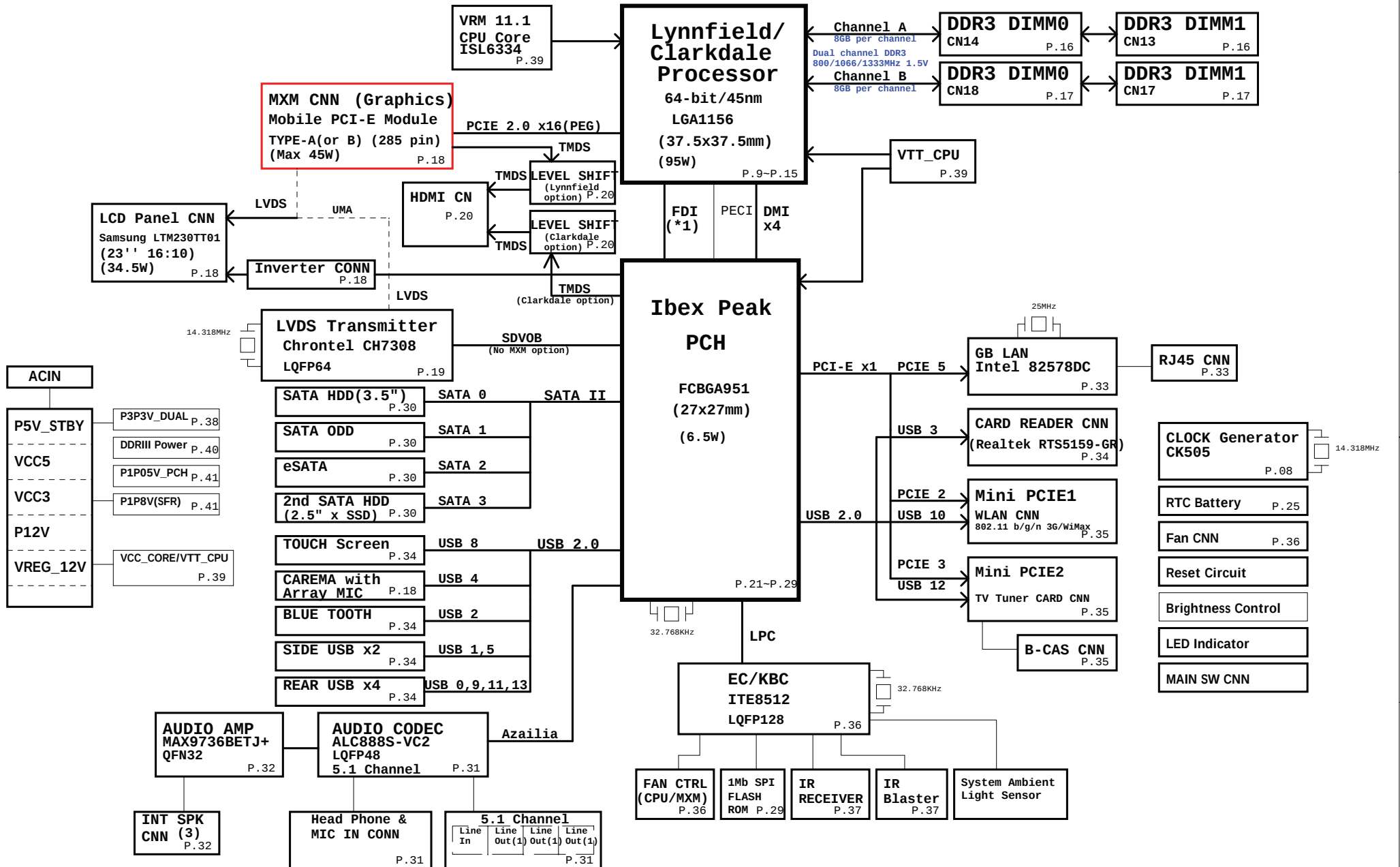


EL5 Block Diagram :

<http://hobi-elektronika.net>



FDI - Used only for the Clarkdale processor.

Net name Description :**Voltage Rails**

P5V_STBY	5.0V always on power rail by LATCH or ACIN
P3P3V_STBY	3.3V always on power rail by LATCH or ACIN
P1P5V	1.5V switched power rail by SUSB#/PM_SLP_S3#
P2P5V	2.5V switched power rail by SUSB#/PM_SLP_S3#
VCC3	3.3V switched power rail by SUSB#/PM_SLP_S3#
VCC5	5.0V switched power rail by SUSB#/PM_SLP_S3#
P12V	12V switched power rail by SUSB#/PM_SLP_S3#
VREG_12V	12V switched power rail for CPU Vcore
VCCP	Core Voltage for CPU
P1V1_CPU_VTT	1.1V power rail for AGTL+ termination & PCH DMI I/F by SUSB#/PM_SLP_S3#
P1P05V_PCH	1.05V power rail for PCH Core;PCH I/O;DMI;PCIE;SATA by SUSB#/PM_SLP_S3#
P1P8_SFR	1.8V power rail for CPU PLL & PCH NAND I/F by SUSC#/PM_SLP_S4#
P1P5V_SUS	1.5V power rail for DDRIII by SUSC#/PM_SLP_S4#
0.75VDDT_DDR3	0.75V DDRIII Termination Voltage by SUSB#/PM_SLP_S3#

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

or _N = Active Low signal

Board Stack up Description**PCB Layers**

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Power Plane
Layer 3		Normal Signal / Ground 1 Plane
Layer 4		Stripline Layer(High Speed)
Layer 5		Ground Plane
Layer 6		Solder Side, Microstrip signal Layer

Layers : 6 Depth 1.2mm Impence 55 ohms +/- 10%

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR3 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR3 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR3 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
Lan	50 ohm +/- 15%		

For no M3 support with Intel LAN:

- 1.05 V ME powered by 1.05 V PCH
- 3.3 V SPI (3.3 V EPW) powered by 3.3 V Main
- VCCLAN (LAN MAC well) is powered by 1.05 ME well (which is powered by 1.05 PCH)
- VCCLANPHY power is gated by SLP_LAN#

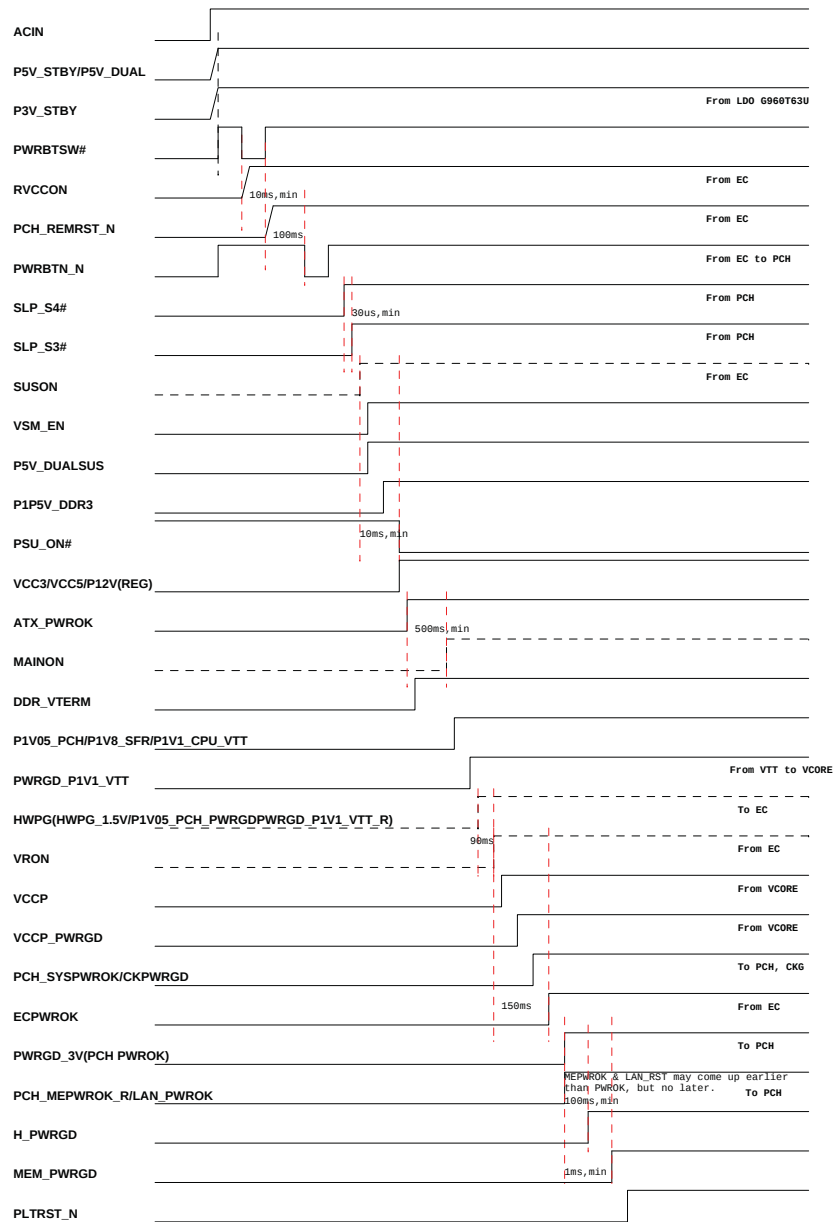
03

Quanta Computer Inc(QCI). 211, Wen Hua 2nd Rd., Kwei Shan, Tao Yuan 3327, Taiwan Tel : +886-3-327-2345	
File	
Timing Diagram	
Size	Document Number
Customer	ELS
Date	Rev
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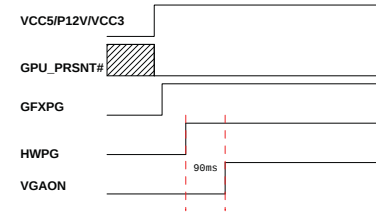
Power on Sequence :

<http://hobi-elektronika.net>

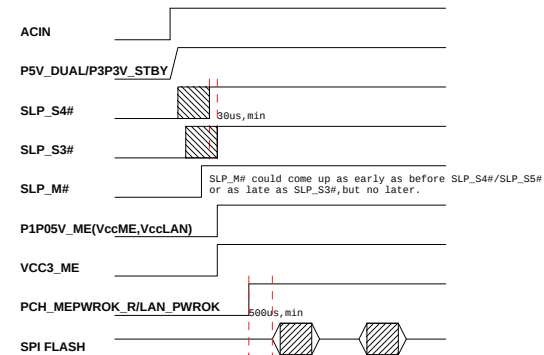
04



MXM POWER ON



SLP_M#, M3 ON

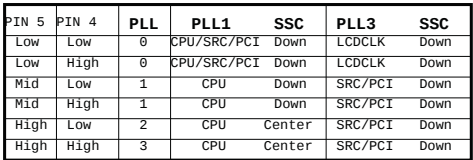


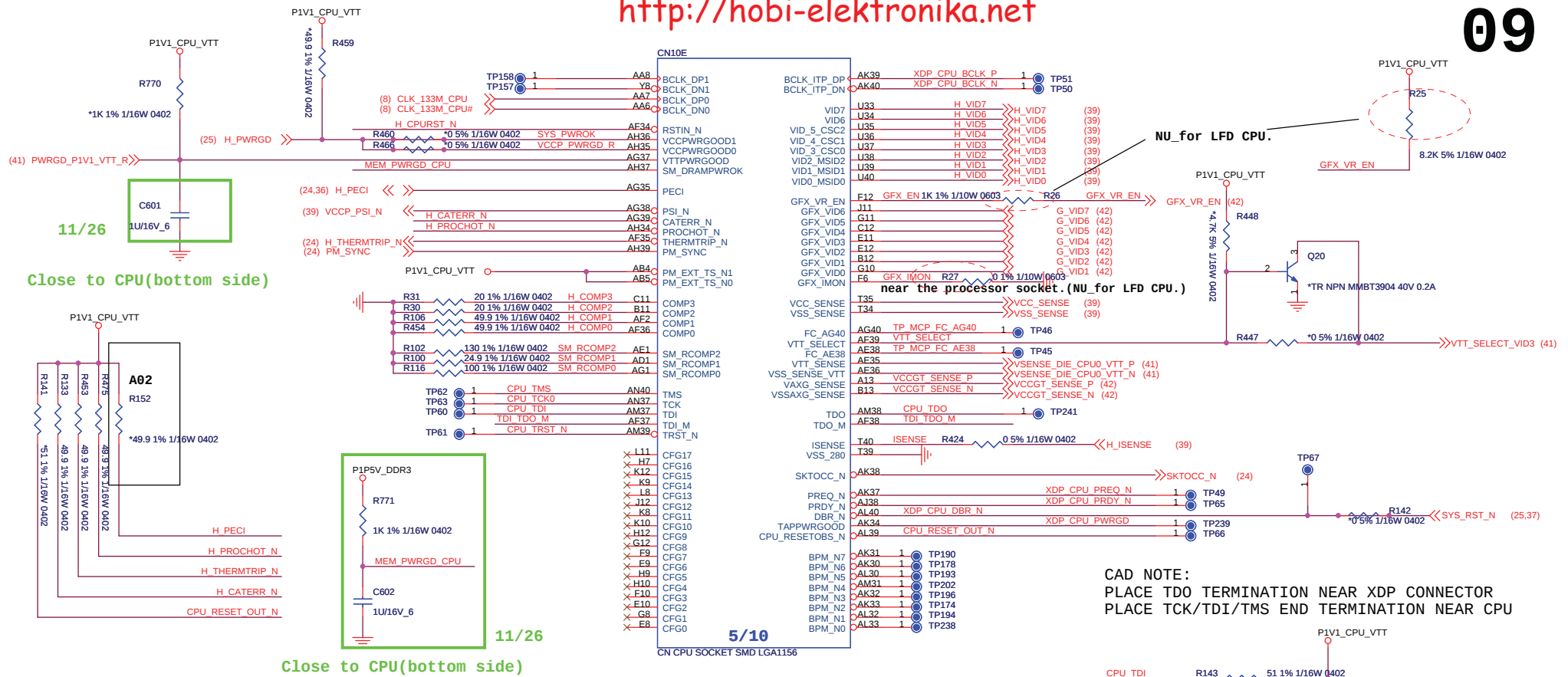
Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Lynnfield : Default for initial power up	0.65V~1.4V 1.1V	90A(TDC) Max:110A
VTT_CPU	Lynnfield : Memory controller & shared cache Ibex Peak : DMI Ibex Peak : CPU_IO	1.045V~1.1V~1.155V 1.1V 1.05V~1.1V~1.16V	30A(TDC) Max: 35A 0.065A 0.001A
P1P8V(SFR)	Lynnfield : Internal processor PLL Ibex Peak : Internal PLL & VRMs Ibex Peak : Dual channel NAND I/F NVRAM : VCCQ NVRAM : VREF	1.71V~1.8V~1.89V 1.71V~1.8V~1.89V 1.71V~1.8V~1.89V	1.1A 0.196A 0.156A
P1P5V_SUS	Lynnfield : CPU I/O Voltage for DDRIII DIMM :	1.425V~1.5V~1.575V	6A
0.75VDDT_DDR3	DDRIII Terminator:	0.75V	?A
P1P05V_PCH	Ibex Peak : VccCore Ibex Peak : Vcc core I/O buffer Ibex Peak : DMI buffer voltage Ibex Peak : Intel Management Engine Ibex Peak : Display PLL A power Ibex Peak : Display PLL B power Ibex Peak : LAN	0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V	1.629A 3.251A 0.065A 2.222A 0.075A 0.075A 0.372A
P1P5V	Mini PCIE : +1.5V(WLAN) Mini PCIE : +1.5V(TV)		
P2P5V	CH7308 : DVDD		
VCC3	Ibex Peak : I/O buffer voltage Ibex Peak : Display DAC Analog power CLK Gen.CK505 : VDD NVRAM : VCC MXM : 3V3 CH7308 : LVDD ALC888S : DVDD Mini PCIE : +3.3V(WLAN) Mini PCIE : +3.3V(TV) Bluetooth : +3.3V Media Card : +3.3V(JMB385) EC(IT8512) : VCC CAREMA	3.14V~3.3V~3.47V 3.14V~3.3V~3.47V	0.357A 0.069A
VCC5	Ibex Peak : Core well Ref. voltage MXM : 5V SATA ODD SATA HDD(2.5" x SSD) ALC888S : AVDD Audio AMP(MAX9736BETJ) : Touch Screen LCD Panel USB: x 5 ports	4.75V~5V~5.25V 5V	0.001A 2.5A
P3P3V_STBY	Ibex Peak : Intel Management Engine Ibex Peak : Suspend well I/O Buffer Ibex Peak : HD Audio controller Suspend Voltage LAN RTL8111DL : VDD IR Receiver EC(IT8512) : VSTBY SPI FLASH ROM	3.14V~3.3V~3.47V 3.14V~3.3V~3.47V 3.14V~3.3V~3.47V	0.086A 0.168A 0.006A
P5V_STBY	Ibex Peak : Suspend well Ref. Voltage	4.75V~5V~5.25V	0.001A
P12V	MXM : 12V INVERTER : Vin FAN_CPU FAN_MXM Audio AMP(MAX9736BETJ) : PVDD		

Date	Change Item Description	Note
11/13	1.PAGE25 ADD R766 SLP_S4#	
	2.PAGE29 ADD R767、R768、R769	
11/24	1.PAGE38 ADD PC179、PR157	
11/26	1.PAGE9 ADD C601、C602、C603、R770、R771	
11/30	1.PAGE34 ADD R772、C604	
12/01	1.PAGE18 Del R49、R53、R54、C120、Add U2、R773、R774、R775、R776、C605、C606、C607、C608、U26、Q46。For EDID	
12/03	1.PAGE41 Add PR85、PR158	
	2.PAGE19 Add PU12、PR159、PR160、PR161、PC180、PC181、PC182、PC183、PC184 For P2P5V	
	3.PAGE20 Add U25、L29、R49、R54、R55、R67、R68、R349、R681、R682、R712、R724、R725、R779、R780、R781、R782、R783、R784、R785、R786、R787、R788、R789、R790、R791、R792、R793、C19、C21、C22、C120、C609、C610、C611 for MXM HDMI Repeater	
12/04	1.PAGE18 Add C617	
VER:C		
12/22	1.PAGE18 Del U26、R774、C606、Q46、C608、R776、R773、R775、C605、C607,Add R318、R696、R314、C605。For EDID	
	2.PAGE34 Change CN33 to 5PIN CONN	
01/05	1.PAGE39 Add PR163、R800、R801。	
01/07	1.PAGE34 Del R1、R2、Add L30。For EMI	
	2.PAGE33 ADD R802、D47。For LAN Wake up	
	3.PAGE40 PC160 connector to P1P5V_DDR3。	
01/11	1.PAGE35 Add R803、R804、R805、R806。For PCI_E detect	
	2.PAGE33 Add R807。For LAN LED	
VER:D		

Schmatic Change List:

Date	Change Item Description	Note



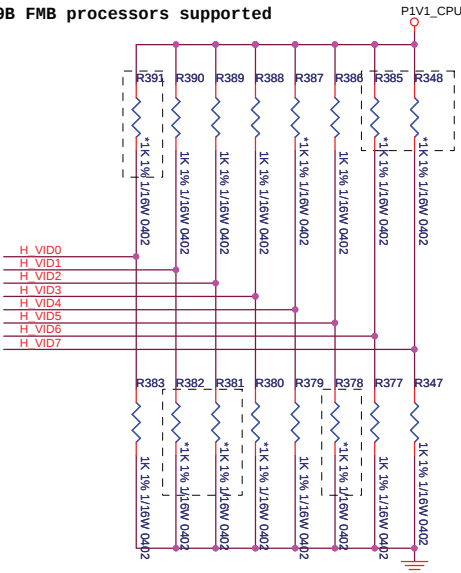


CFG	H	L	Notes
0			H:1x16, L:2x8
1	RSVD		
2	RSVD		
3	NORM	RSVD	LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		

CFG 0-6 all internal PULL-UP

Need to be placed close to processor to minimize ESD risk

VID[7:0] : 00101110 =>1.325V@VCC,Max
2009B FMB processors supported

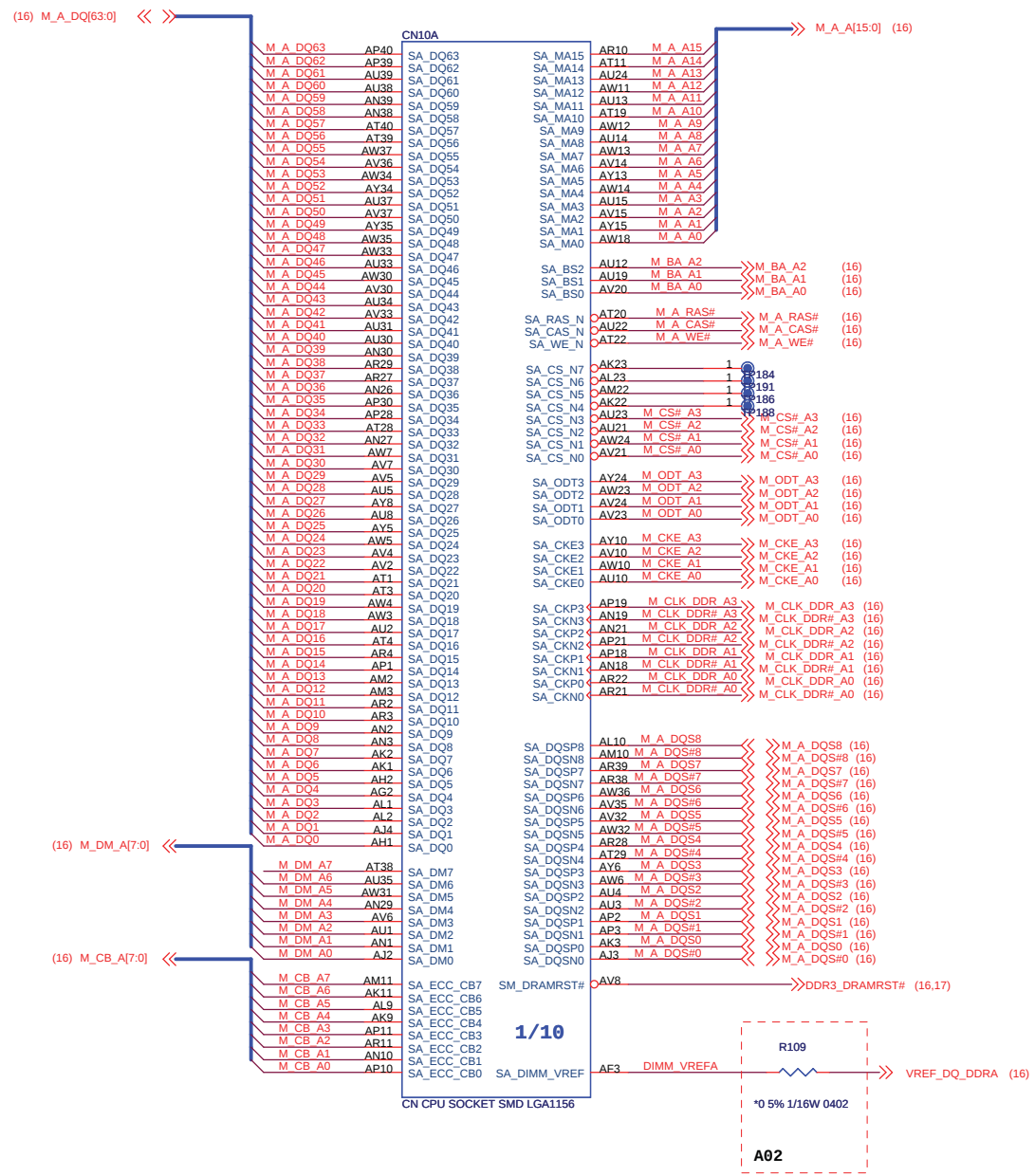


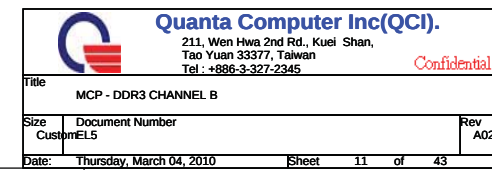
CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

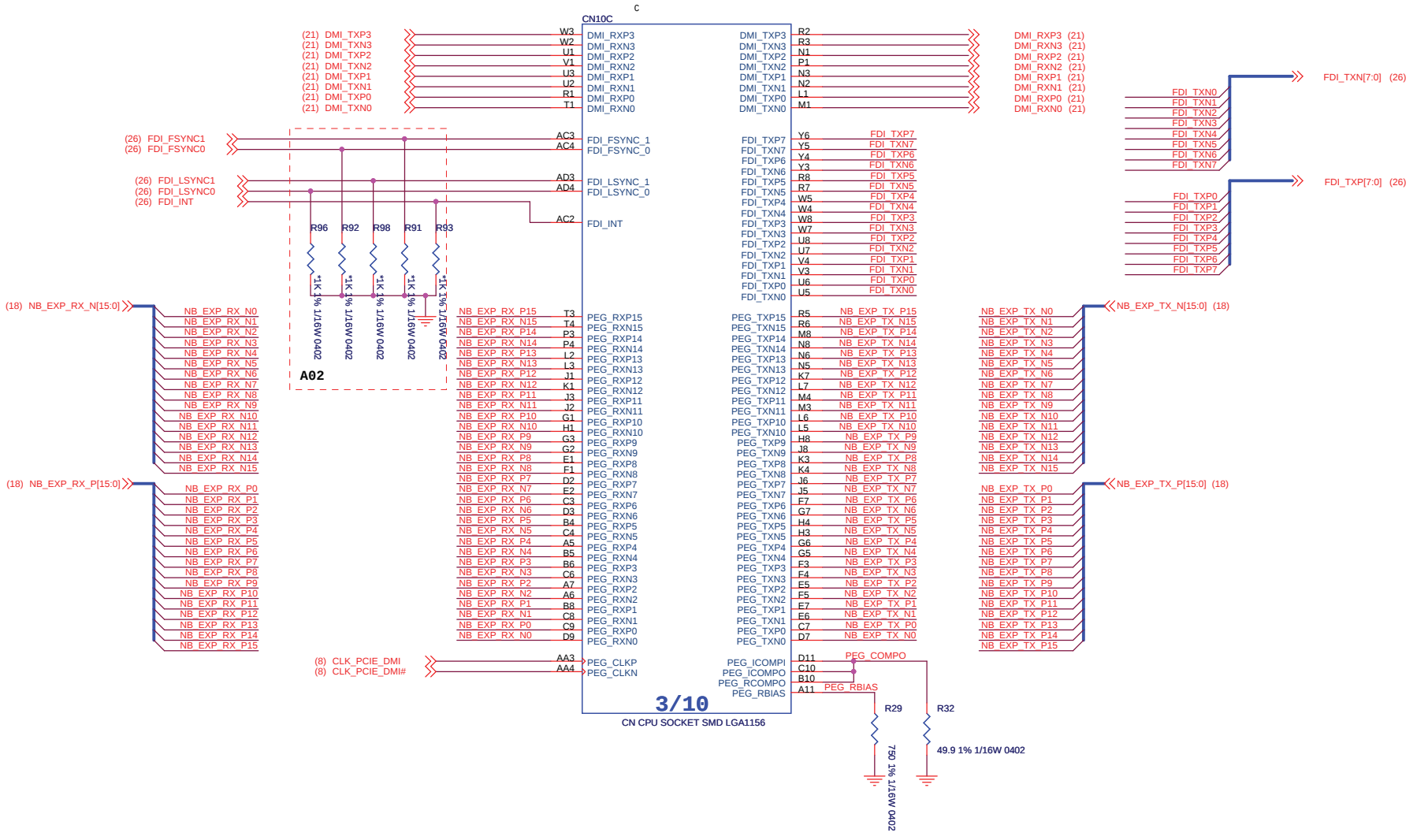
Quanta Computer Inc(QCI)
211, Wen Hwa 2nd Rd., Kuei Shan,
Tao Yuan 33377, Taiwan
Tel : +886-3-327-2345

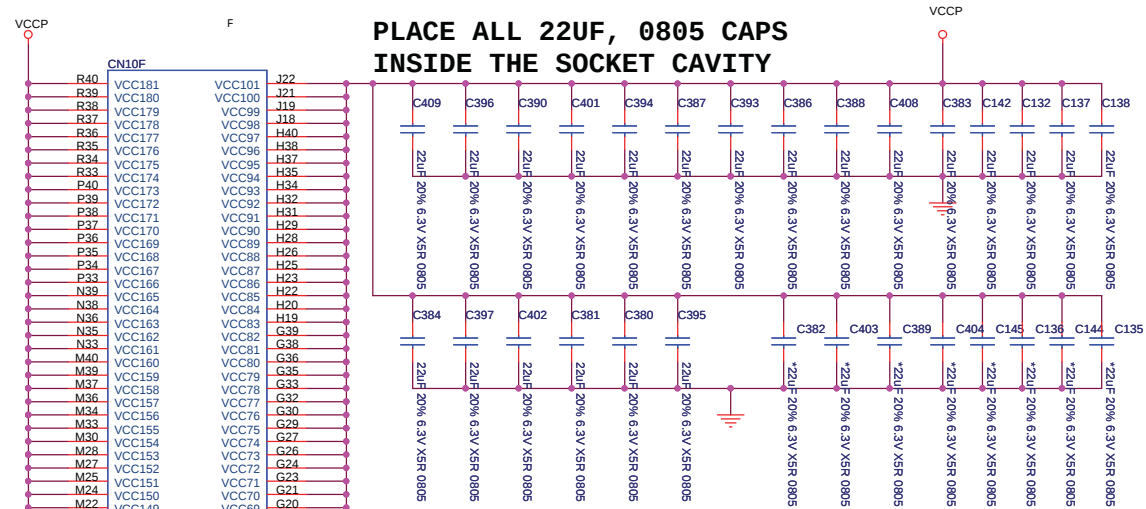
Confidential

Title: MCP - CLK,CTRL,MISC,DEBUG		
Size: CustomEL5	Document Number	Rev: A02
Date: Thursday, March 04, 2010	Sheet: 9	of 43

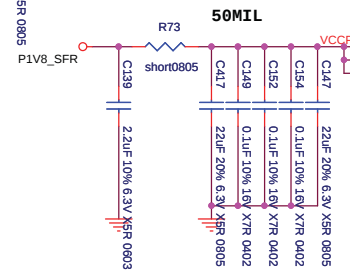




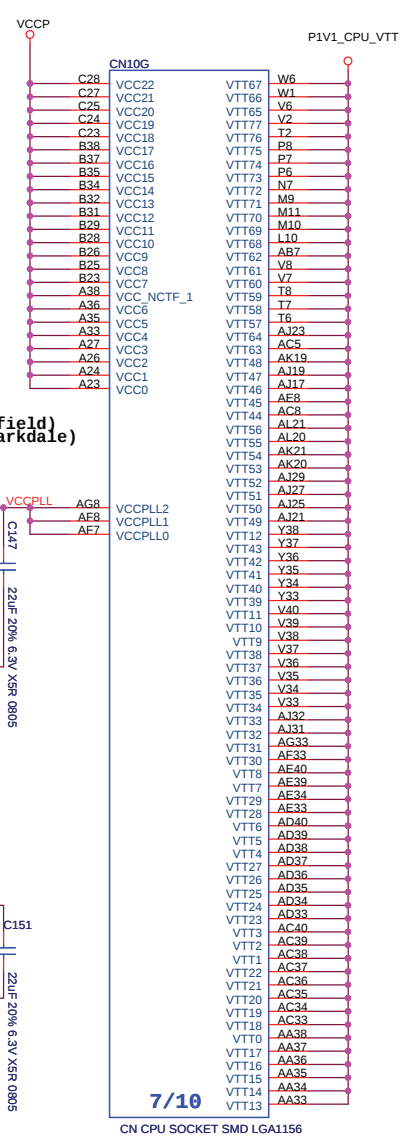
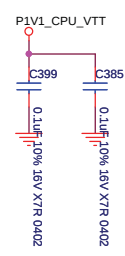
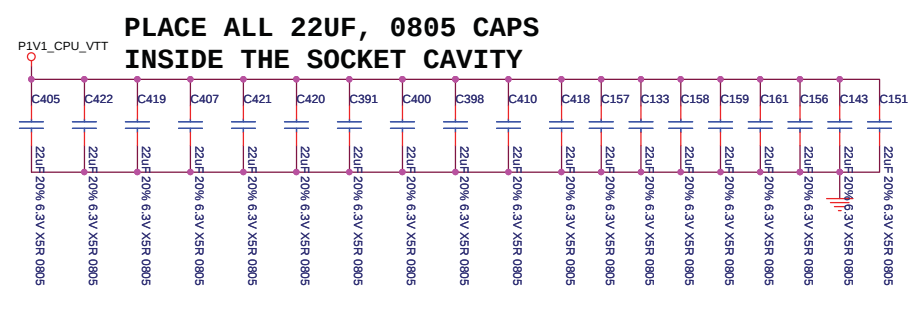




VCCPLL 1.1A(Lynnfield)
VCCPLL 0.196A(Clarkdale)



PLACE ALL 22UF, 0805 CAPS
INSIDE THE SOCKET CAVITY.
ON BOTTOM OF BOARD



CN CPU SOCKET SMD LGA1156

6/10

CN CPU SOCKET SMD LGA1156

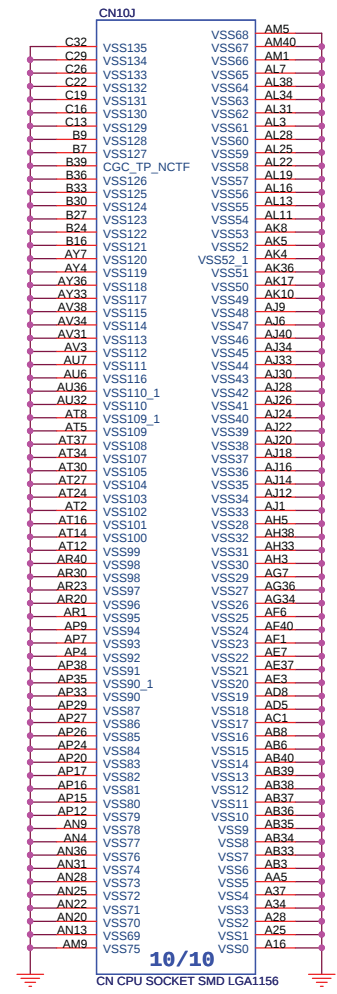
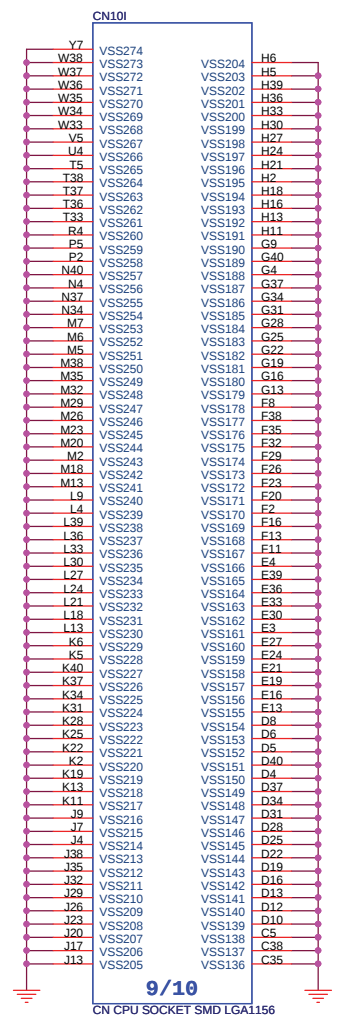
For DMI bus split power plane

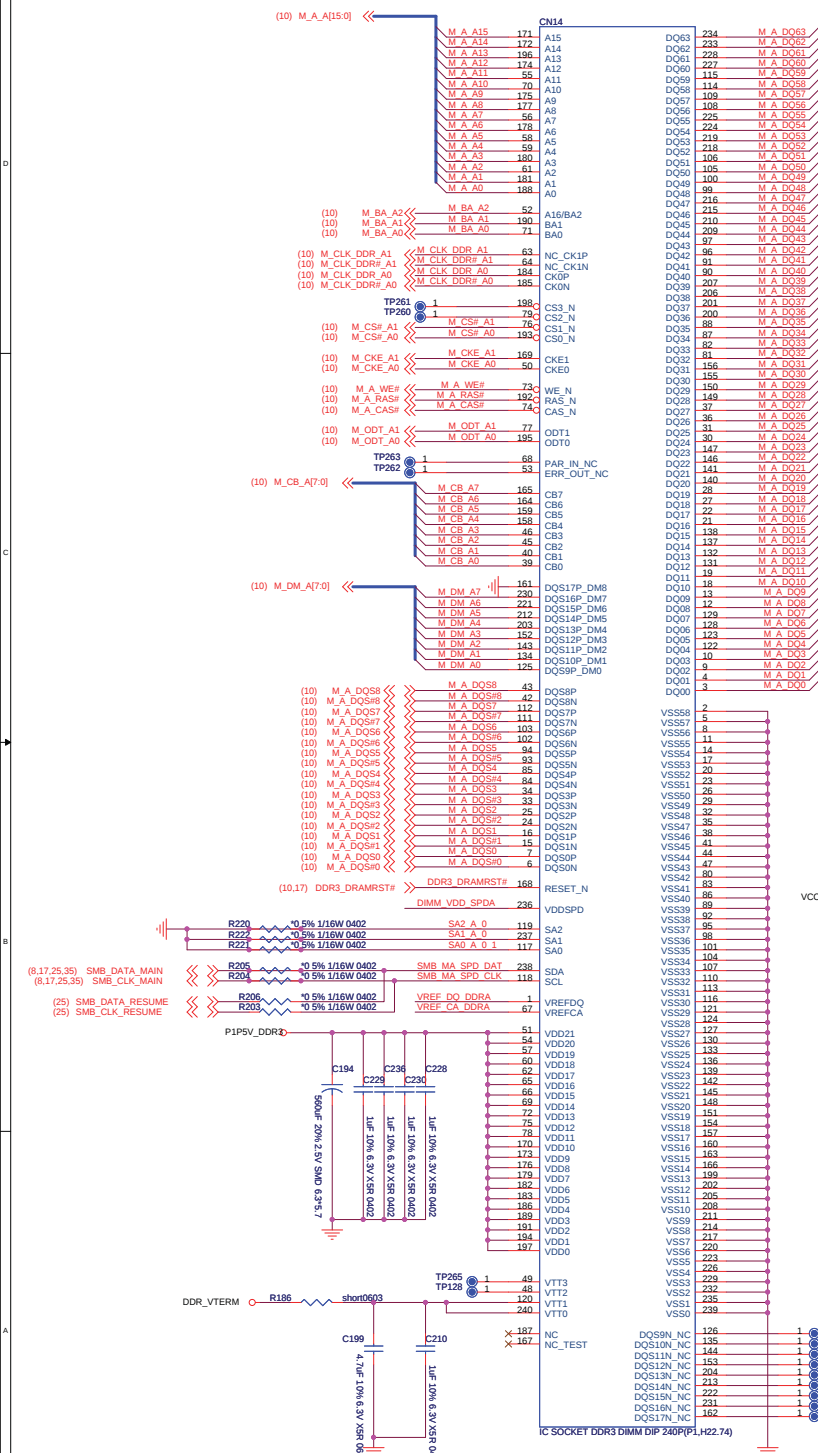
Quanta Computer Inc(QCI).
211, Wen Hwa 2nd Rd., Kuei Shan,
Tao Yuan 33377, Taiwan
Tel : +886-3-327-2345

Confidential

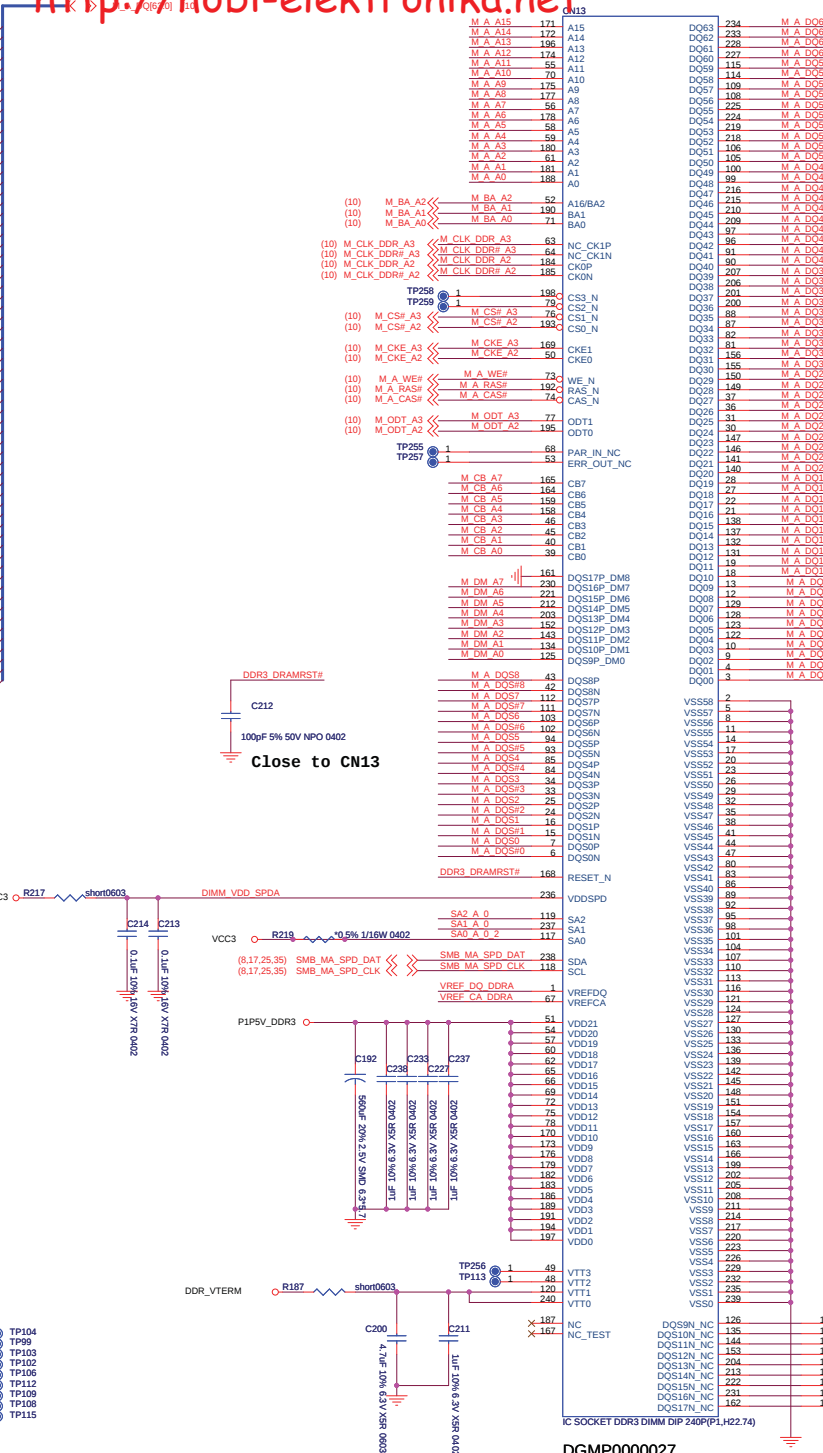
Title MCP - VCCP/ VTT		
Size CustomEL5	Document Number	Rev A02
Date: Thursday, March 04, 2010	Sheet 13	of 43

Date: Thursday, March 04, 2010 Sheet 14 of 43

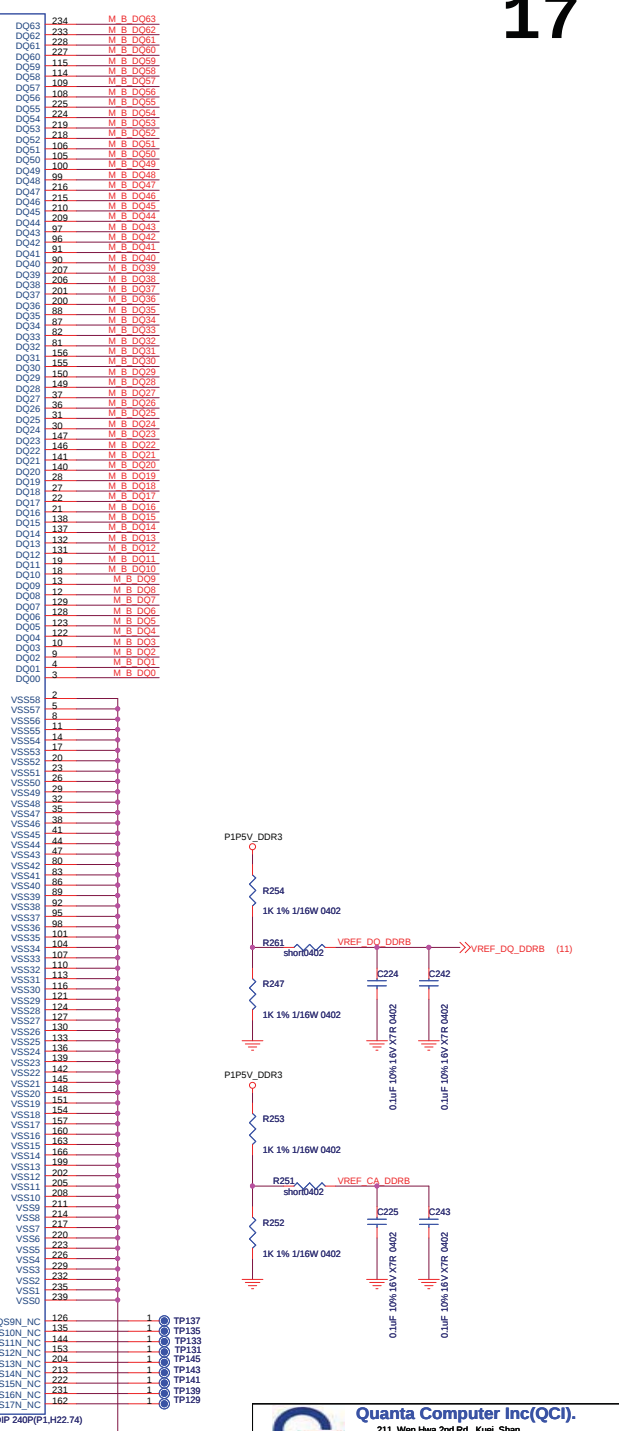


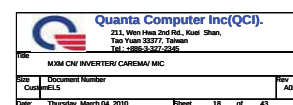


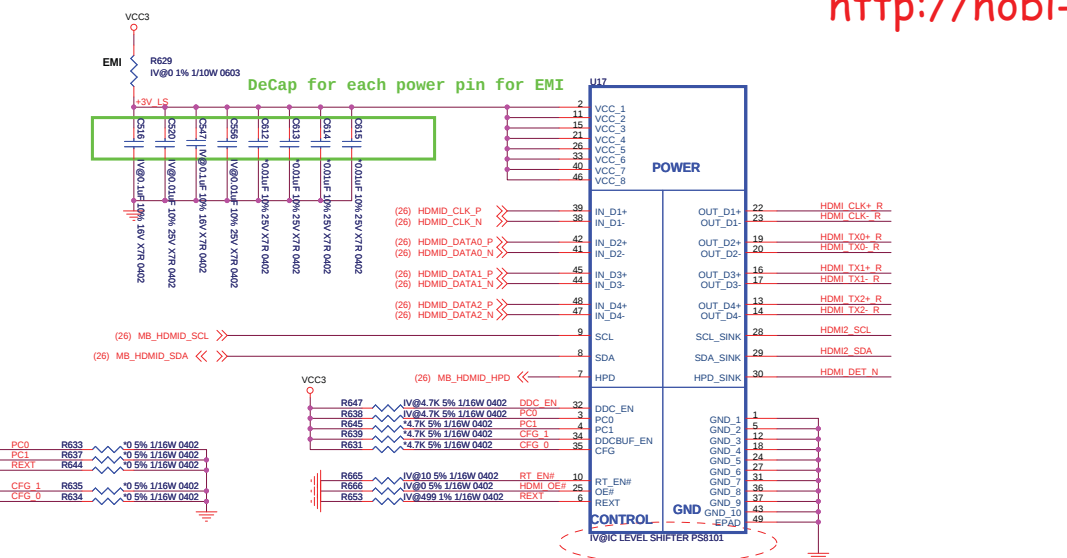
DGMP0000028



DGMP0000027







Mount for Non-MXM Option.

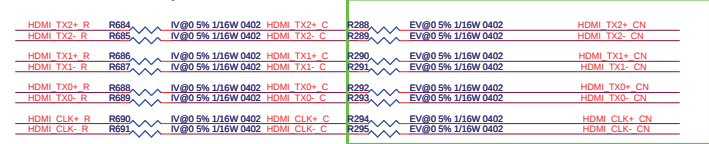
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommended
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

EVA@: PS8101
EV@: PS8171
EV@MXM
IV@UMA

12/3

Mount for Non-MXM Option.

Mount for MXM Option.

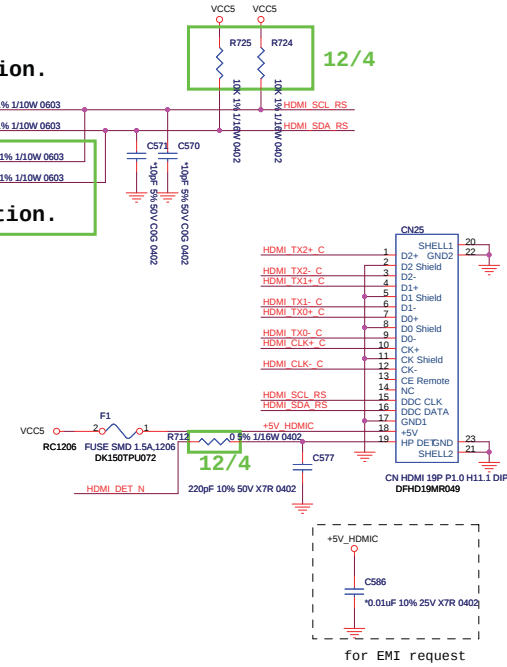


Mount for Non-MXM Option.



Mount for MXM Option.

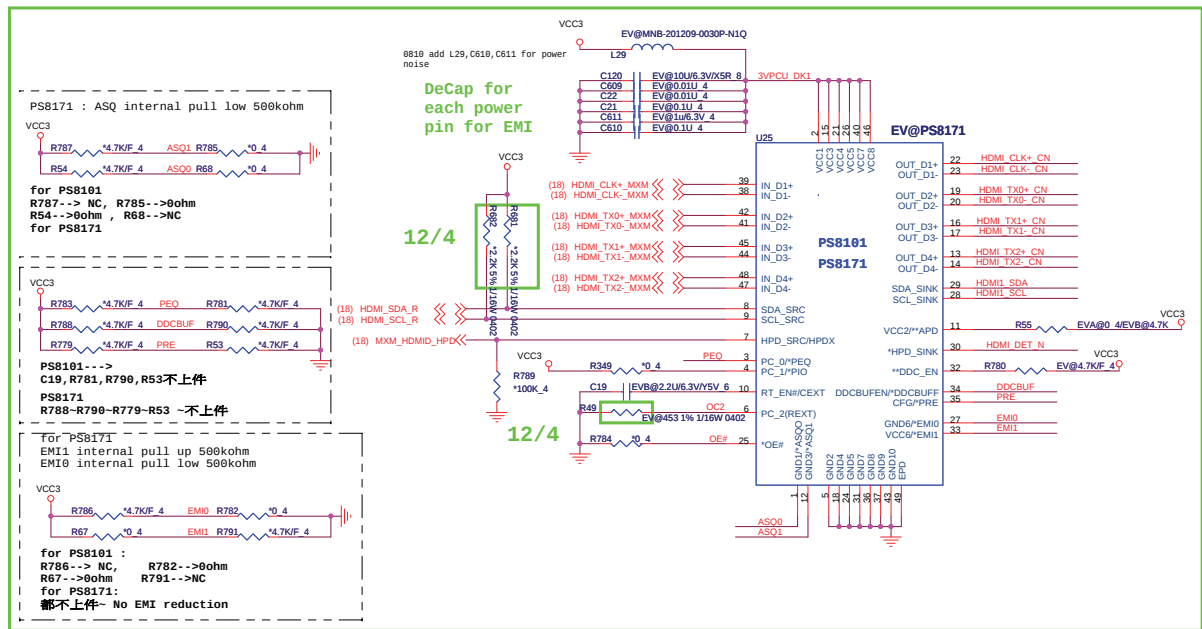
12/3



12/4

12/4

for EMI request



DeCap for each power pin for EMI

12/4

12/4

PS8171 EMI		
EMIO	EMI1	EMI reduction and filter setting
L	L	no EMI reduction
L	H	
H	L	
MID	MID	

PS8171 HPDX		
PIN4	LEVEL	HPDX Output
P10	L	HPD_Sink = HPD
	H	HPD=HPD_SINK#

PS8171 APD (ASQ internal pull low 500kohm)		
PIN11	LEVEL	Description
APD	HIGH	Automatic power down enable
	MID	
	LOW	Automatic power down disable

PS8171 ASQ (ASQ internal pull low 500kohm)		
PIN12	LEVEL	Automatic Squelch
ASQ[1,0]	HL	No automatic squelch
	LL	Level=100mVpp, default timer
	LH	Level=150mVpp, default timer
	HL	Level=200mVpp, default timer
	ML	Level=120mVpp, extended timer
	MR	Level=100mVpp, extended timer
	LH	Level=80mVpp, extended timer
	HM	Reserved
	MR	Reserved

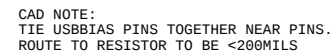
PRE internal pull low 500kohm

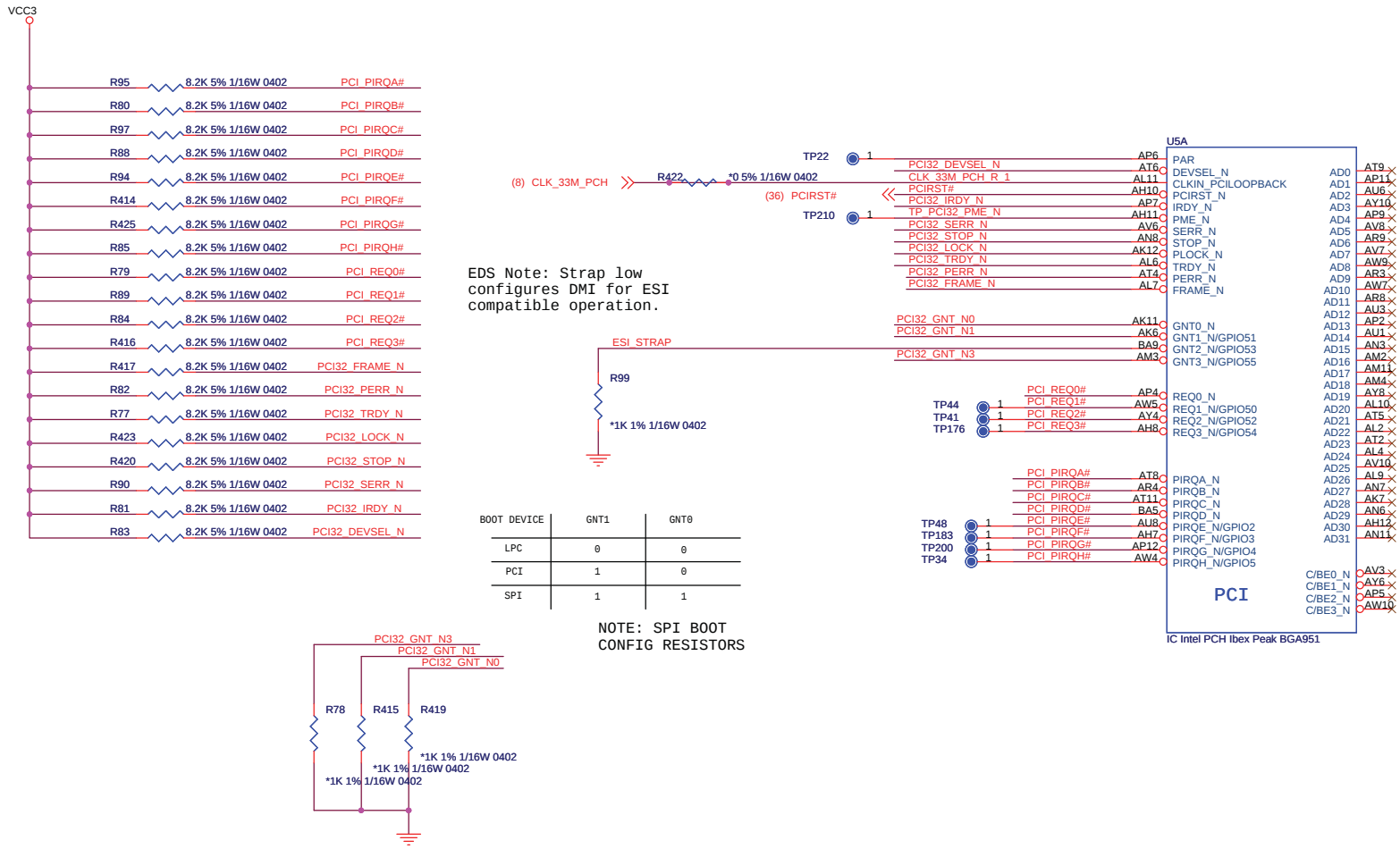
PS8171 DDCBUF (DDCBUF internal pull low 500kohm)		
PIN34	LEVEL	Description
DDCBUF	HIGH	Active DDC buffer enable; Setting 1
	MID	Active DDC buffer enable; Setting 2
	LOW	No DDC active buffer, passive DDC level shifting

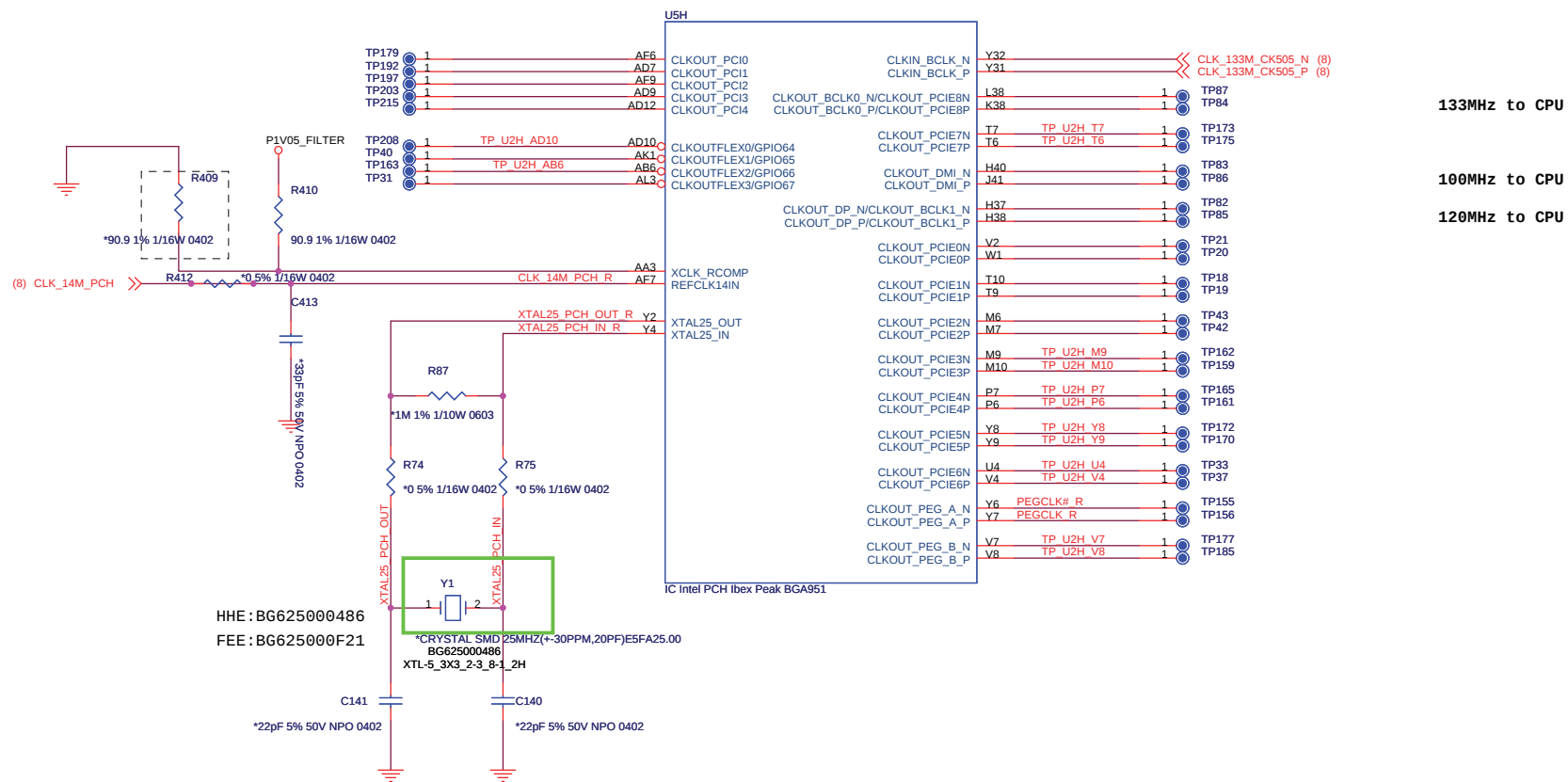
PS8171 EQ		
PIN3	LEVEL	EQ
PEQ	HIGH	7dB
	MID	2dB
	LOW	4dB
	LOW	0dB

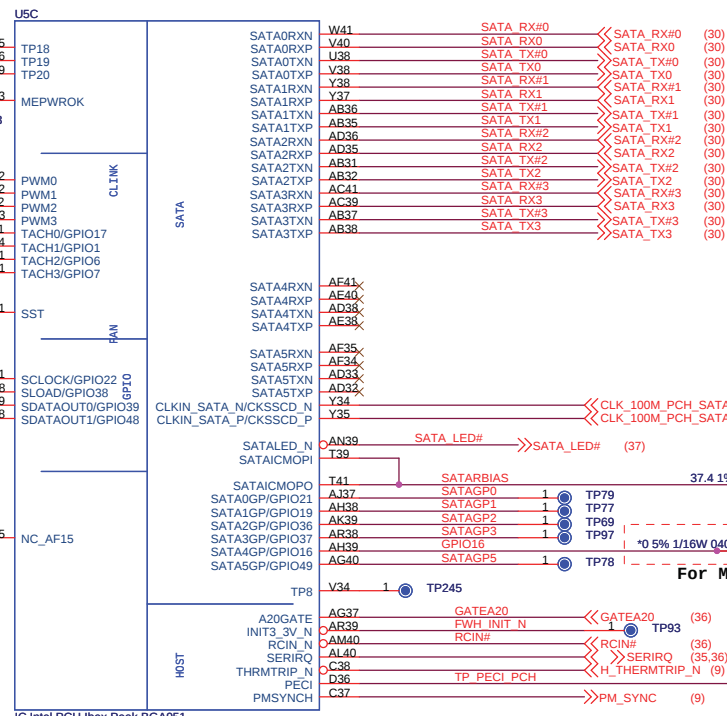
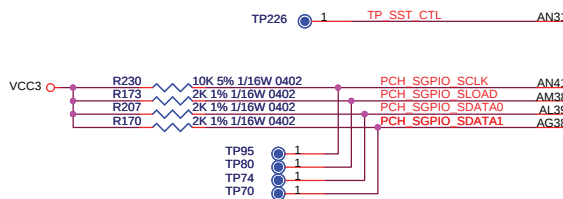
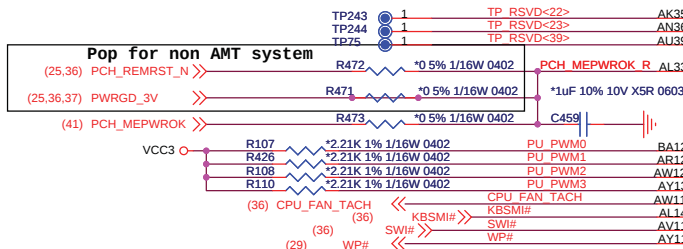
PS8171 SWING		
PIN35	LEVEL	dB
PRE	HIGH	1.2dB
	MID	2dB
	LOW	0dB
	LOW	0dB

PC1 PC0 EQUALIZATION		
PC1	PC0	EQUALIZATION
0	0	8dB
0	1	4dB
1	0	12dB
1	1	0dB







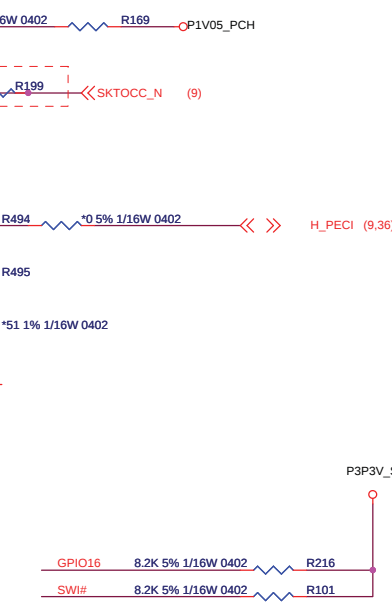
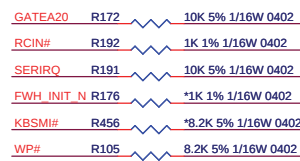
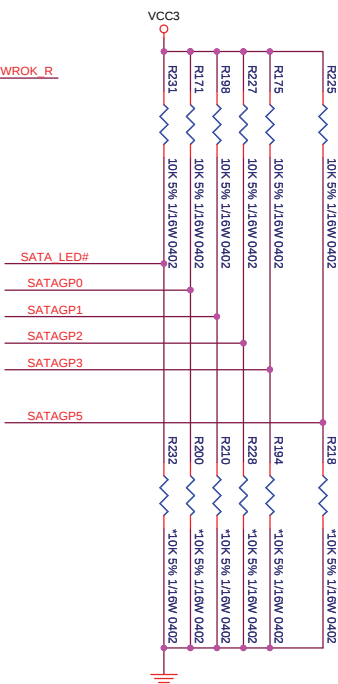
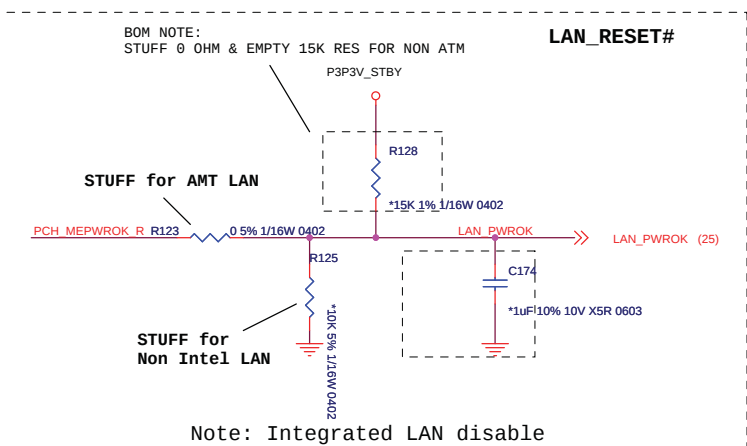
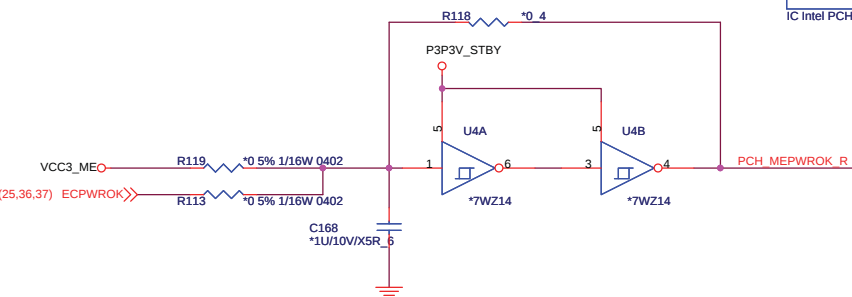


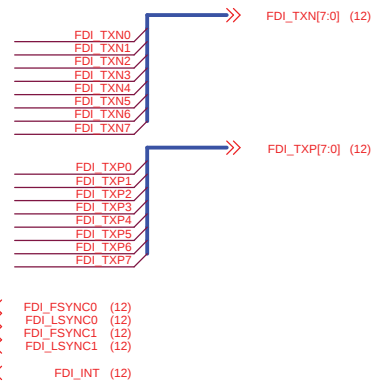
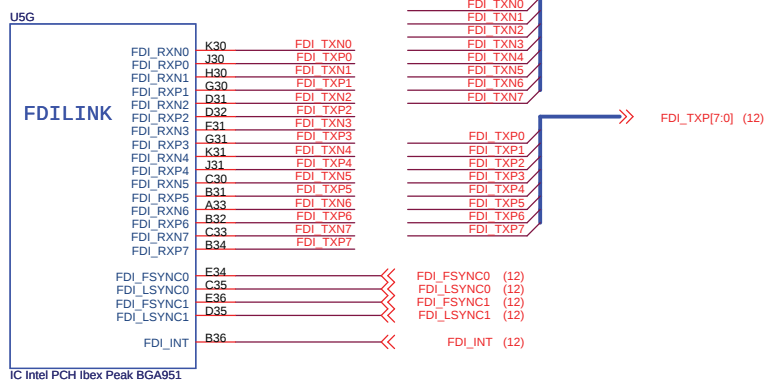
To SATA HDD

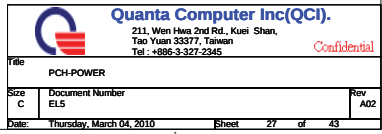
To SATA ODD

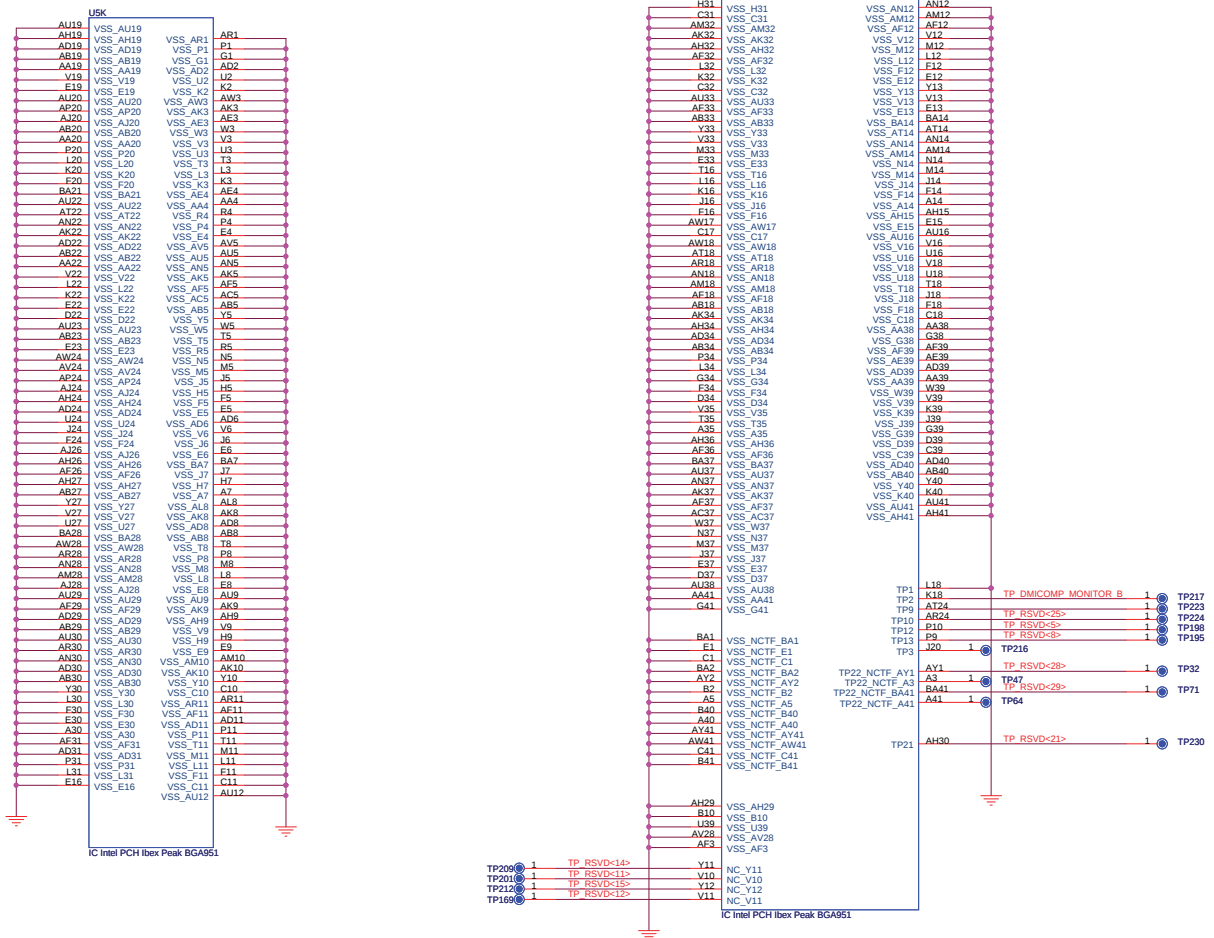
To eSATA

To 2nd SATA HDD







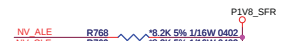


PCH - GND

11/13



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH



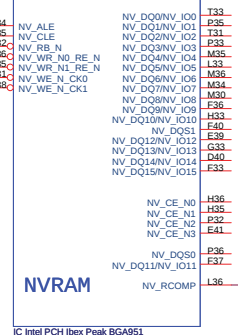
Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

Default Hi, drive Lo to disable AT-D function.

Note: For NV_ALE, Intel Anti-Theft Technology is enabled when sampled high. pulling the signal low disable Intel Anti-Theft Technology

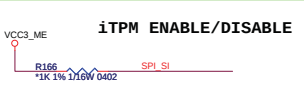
Note: NV_CLE signal should not be pulled low during the time the strap is sampled

USE



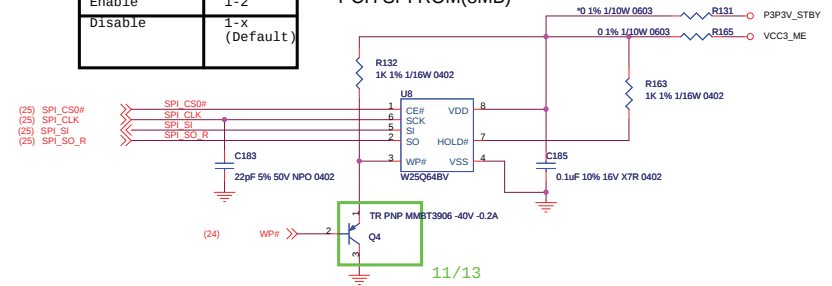
IC Intel PCH Ibox Peak BGA951

11/13

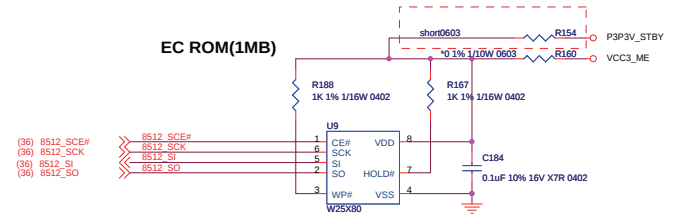


TPM Function	JP12
Enable	1-2
Disable	1-x (Default)

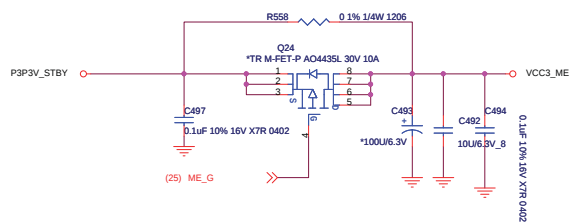
PCH SPI ROM(8MB)

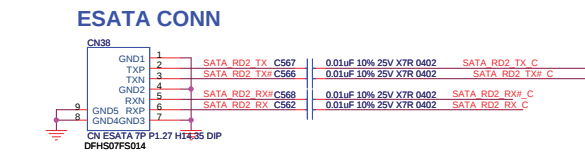
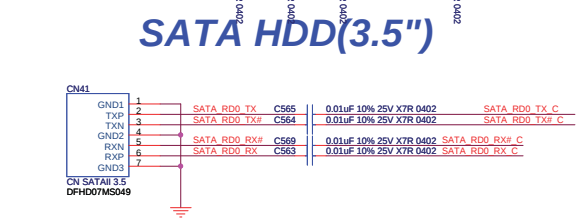
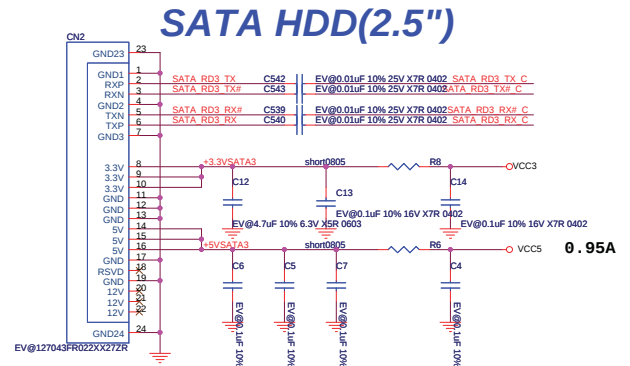
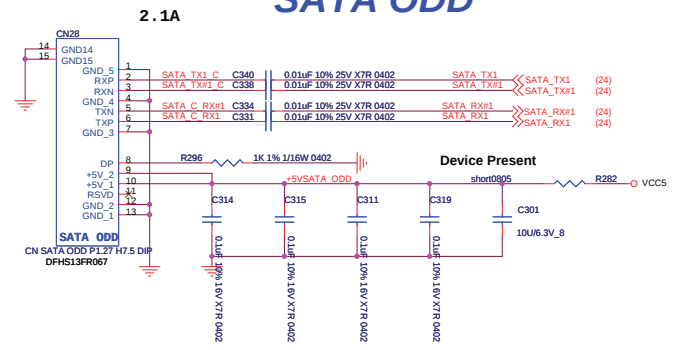


EC ROM(1MB)

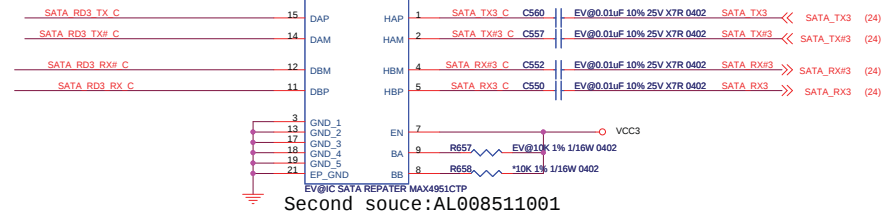


Mount R558 for Non-M3 support

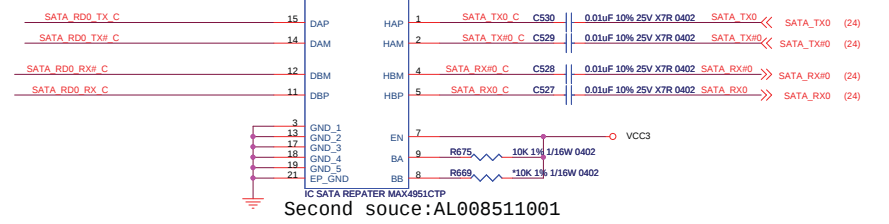




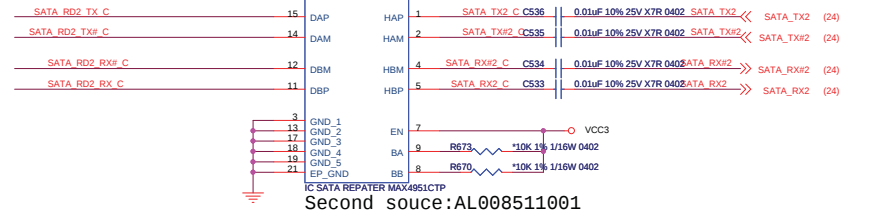
SATA HDD(2.5")



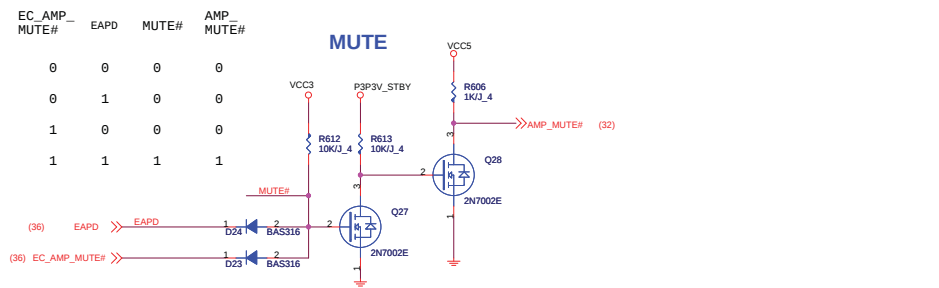
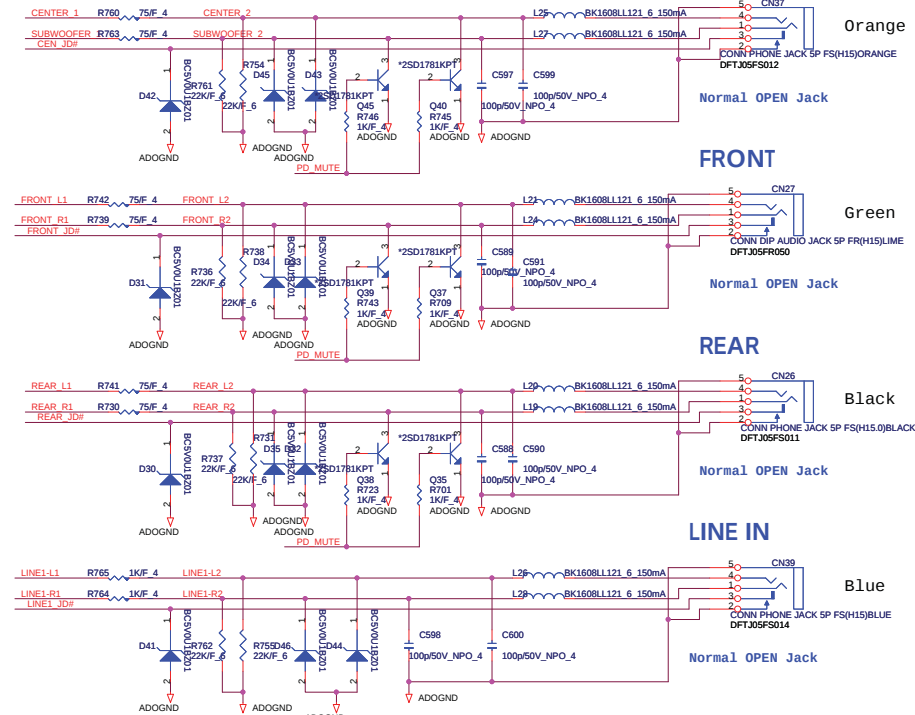
SATA HDD(3.5")



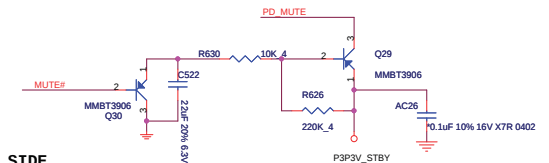
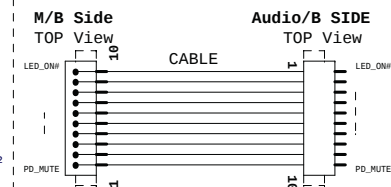
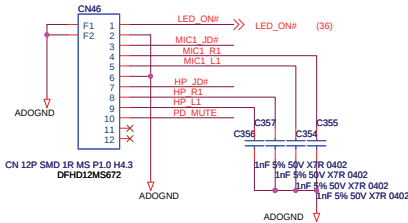
ESATA



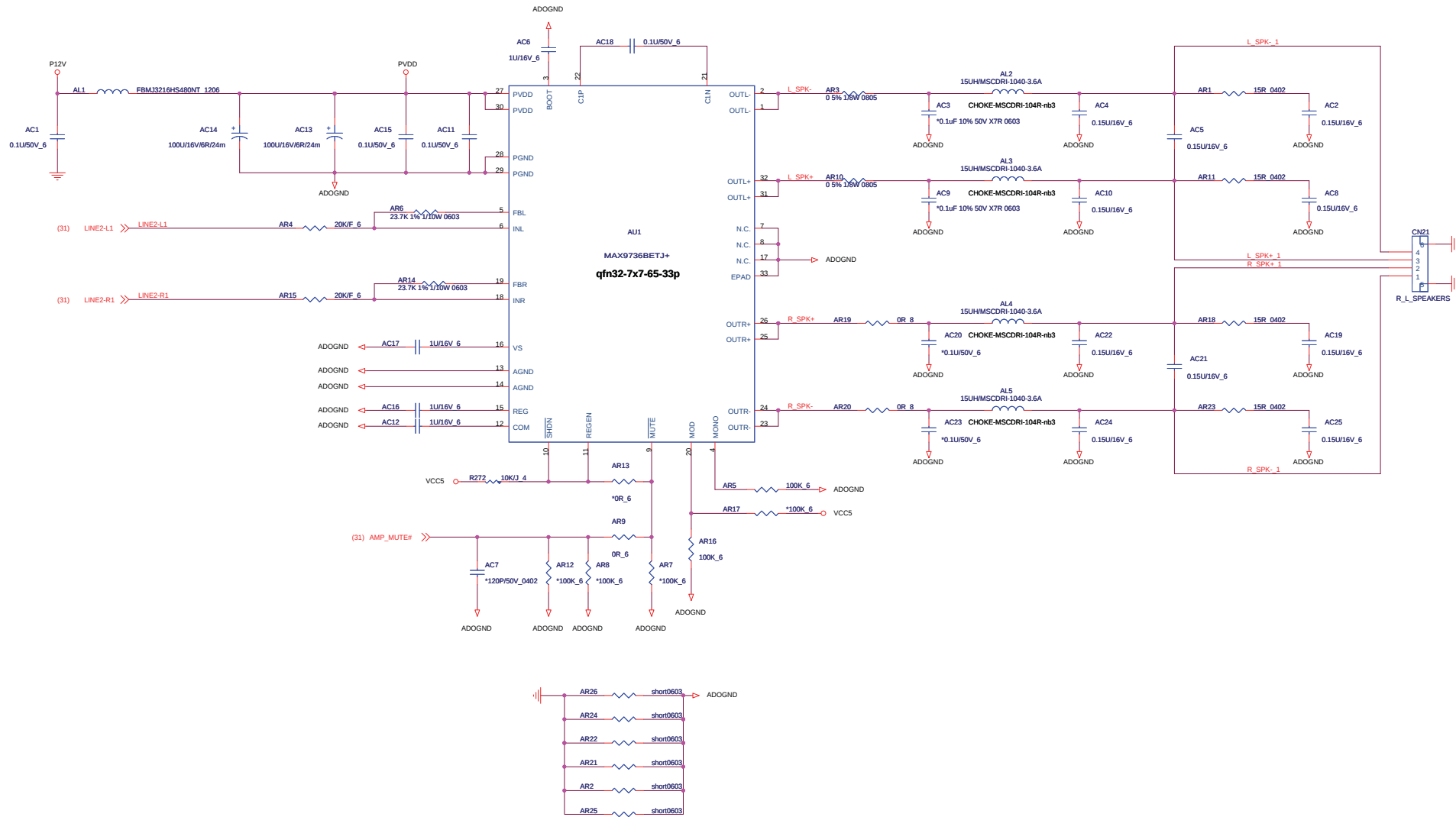
CENTER & SUBWOOFER

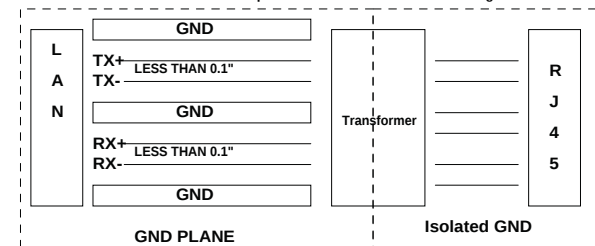
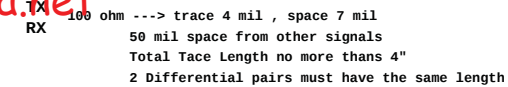


EXT. MIC & HP

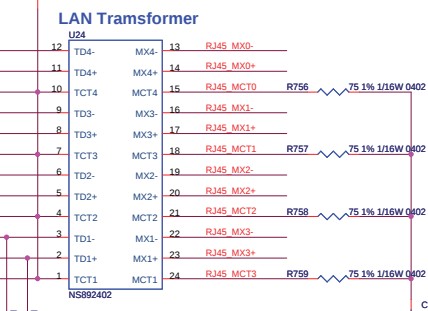
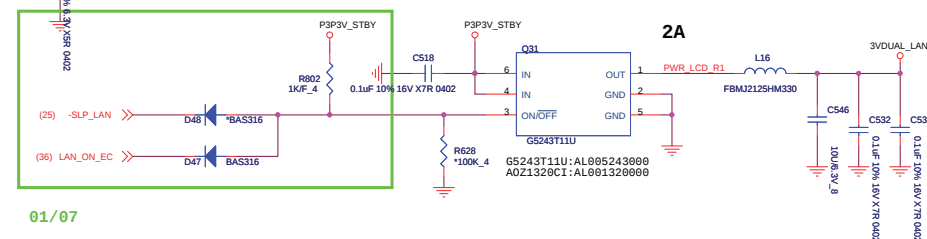


Speaker AMP.

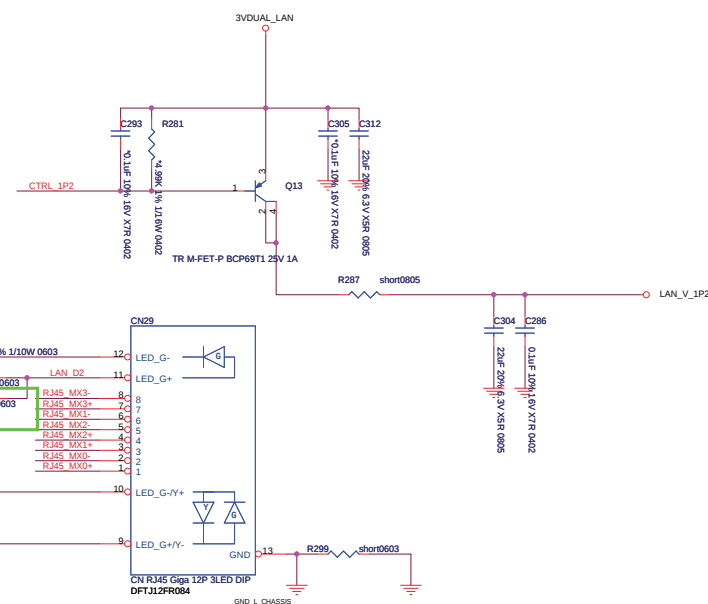
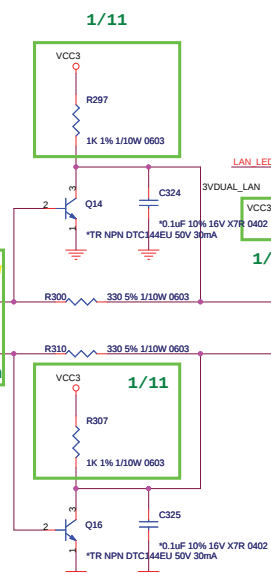




2A



copy from EL7
trf-10-1-24p-nb3-->trf-10-1-24p-smt
for layout's request



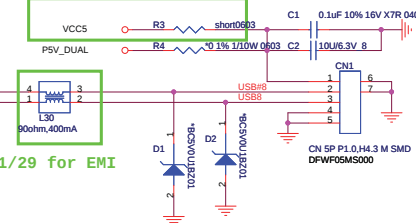
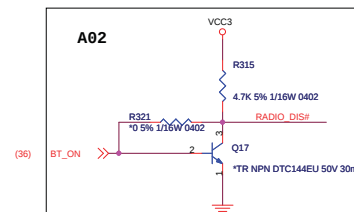
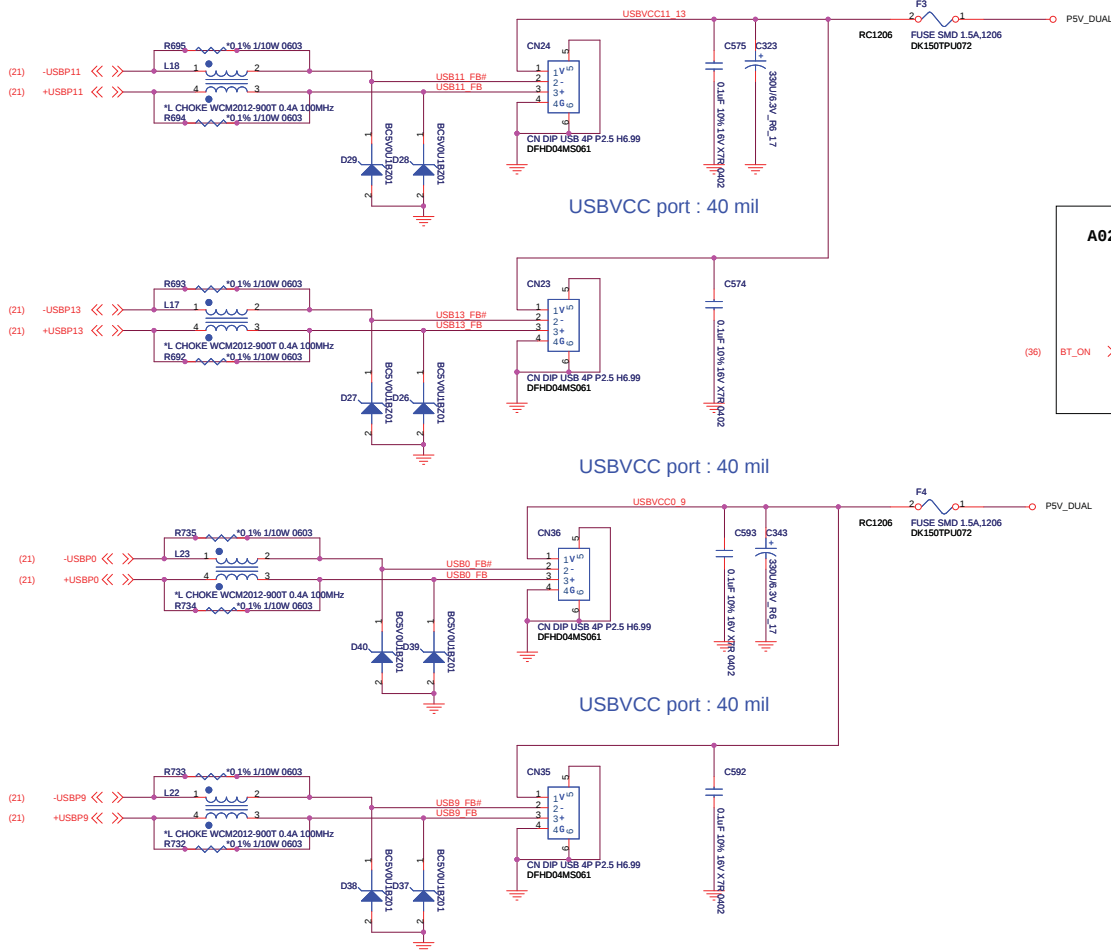
REAR USB PORT X4

USBVCC port : 40 mil

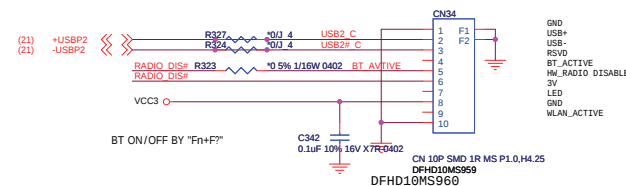
<http://hobi-elektronika.net>

Touch Panel connector

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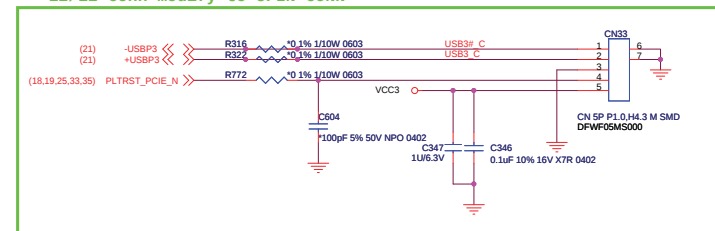


BLUETOOTH connector



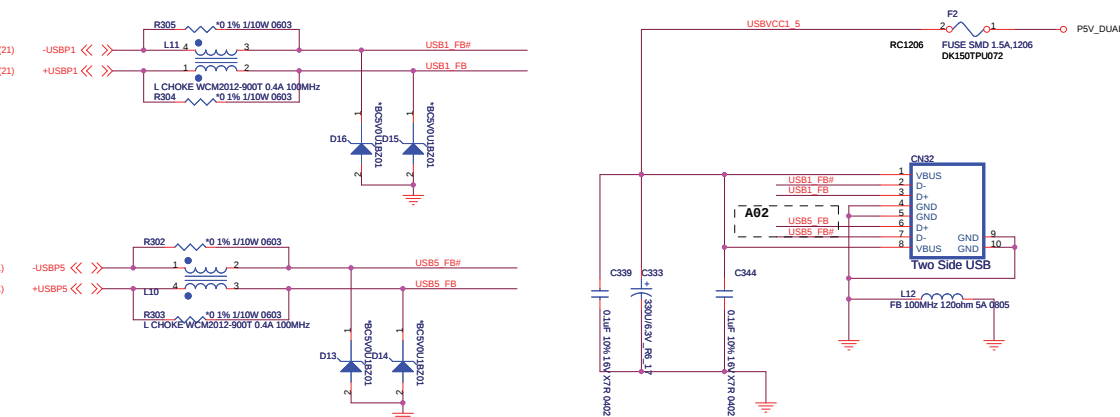
MEDIA READER connector

12/22 Conn modify to 5PIN GNN

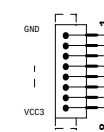


SIDE USB PORT X2

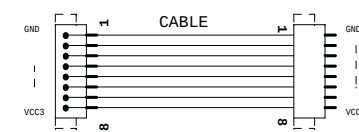
USBVCC port : 80 mil



M/B Side
TOP View



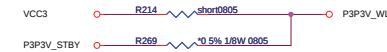
Card reader/B SIDE
TOP View



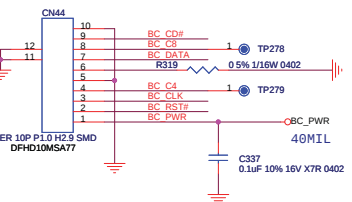
12/22



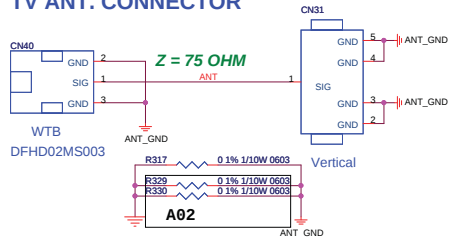
TV Card

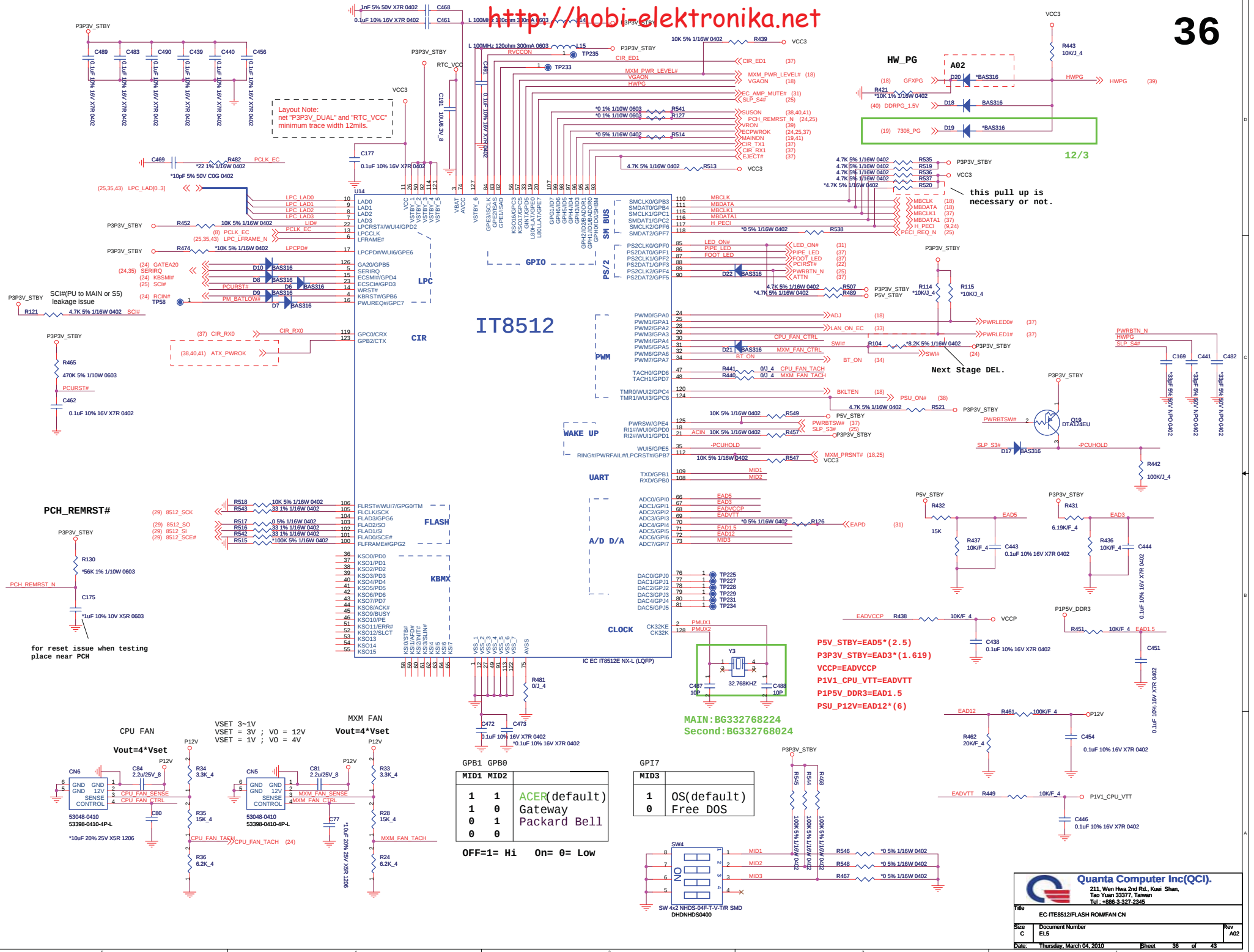


B-CAS CONN

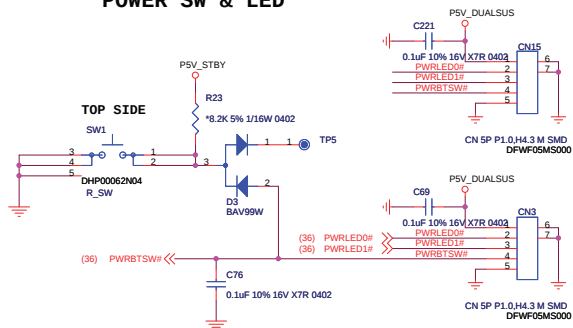


TV ANT. CONNECTOR

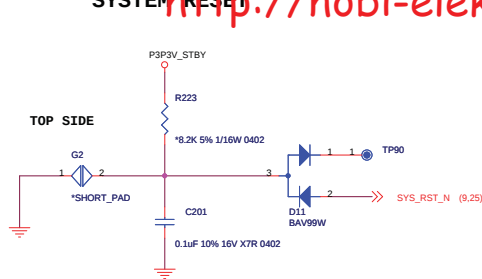




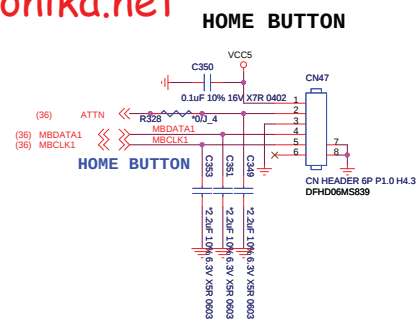
POWER SW & LED



SYSTEM RESET

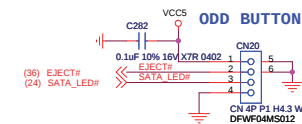


HOME BUTTON

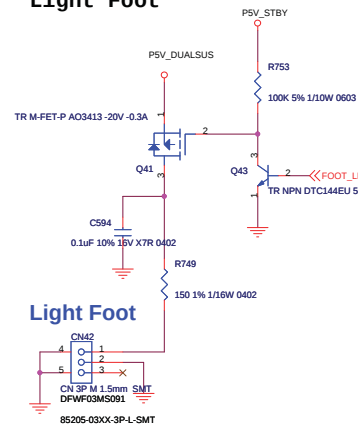


37

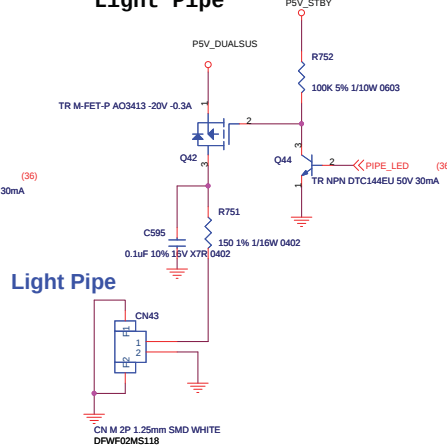
ODD EJECT



Light Foot



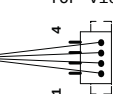
Light Pipe



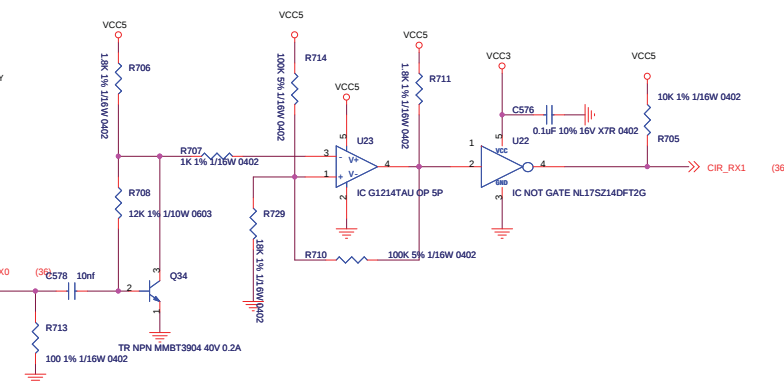
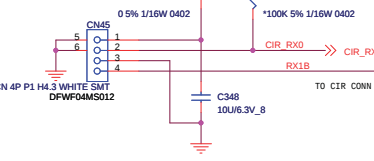
M/B Side



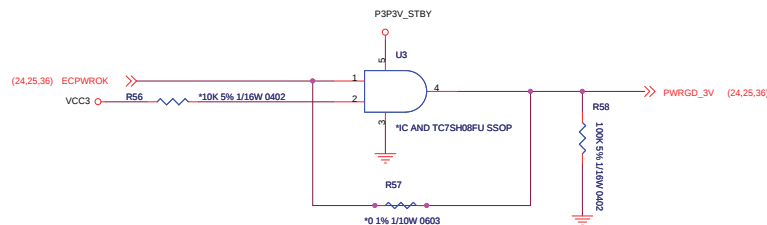
IR/B SIDE



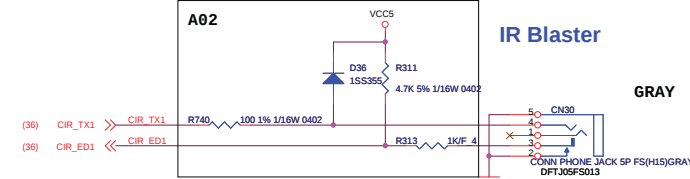
IR Receiver



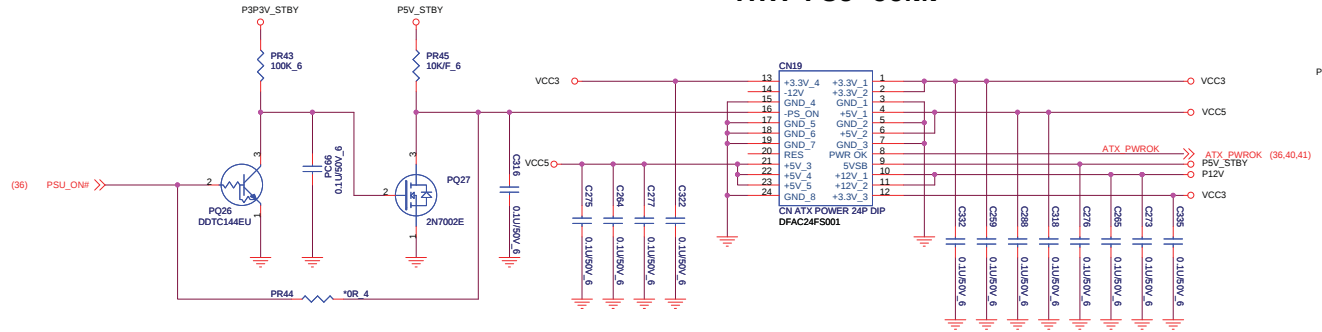
PCH POWEROK



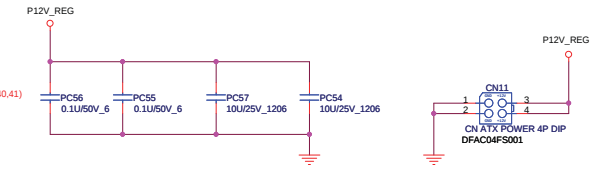
IR Blaster



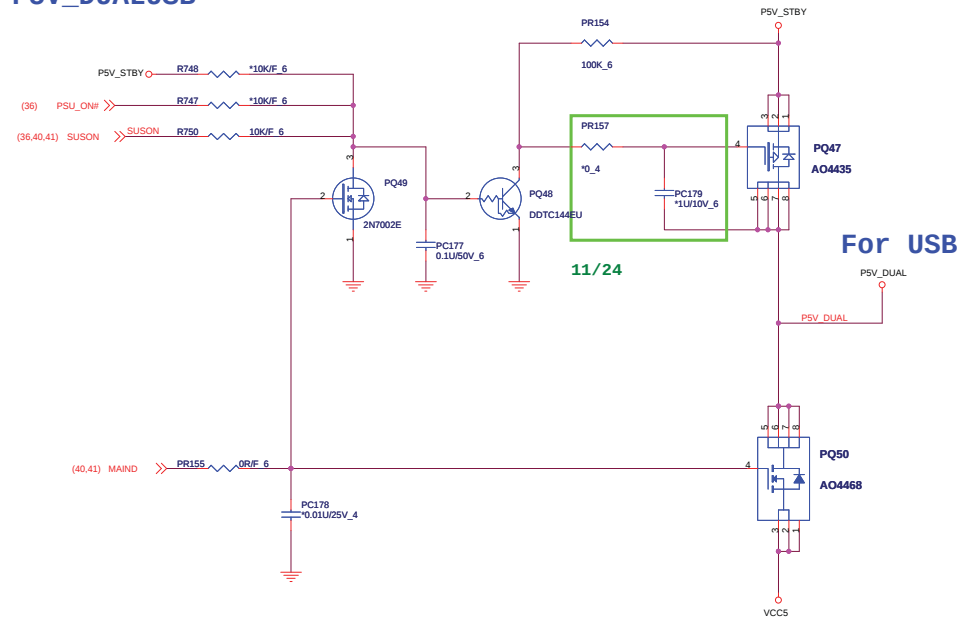
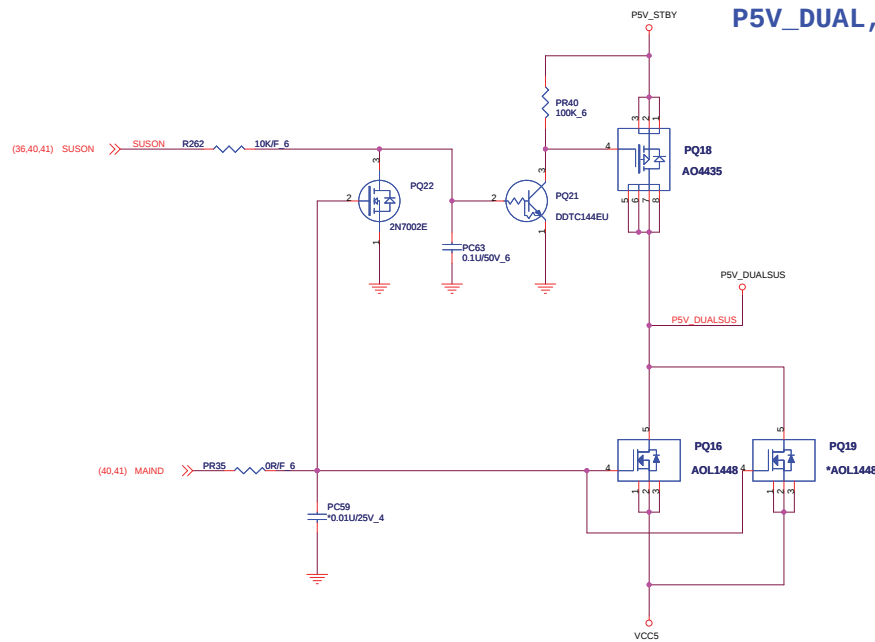
ATX PSU CONN



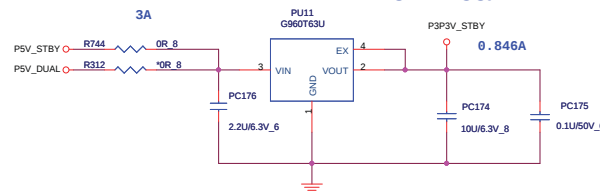
4PIN +12V_REG for CPU_CORE



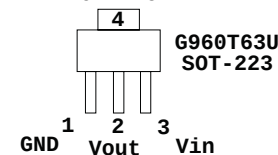
P5V_DUAL, P5V_DUALUSB

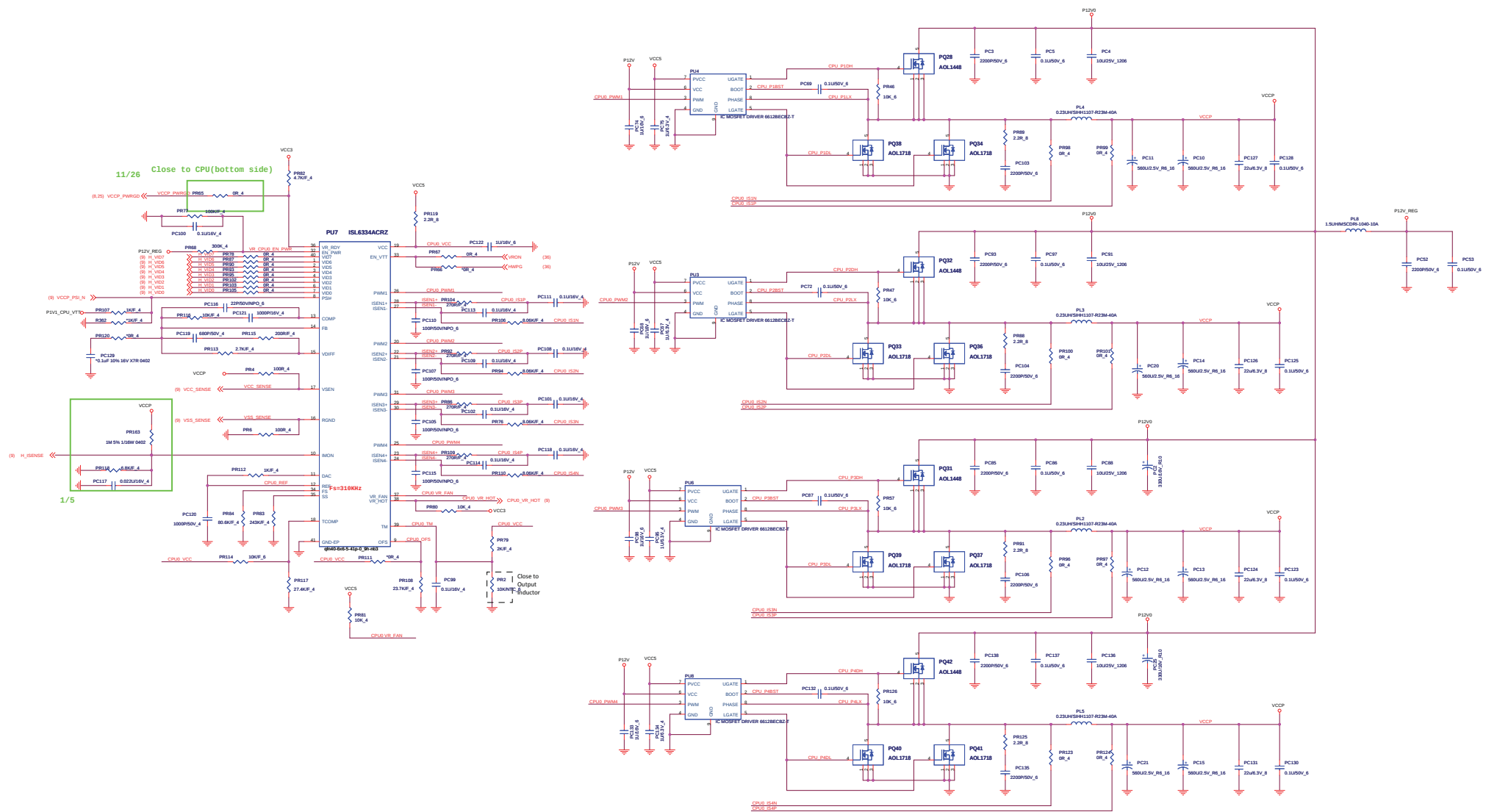


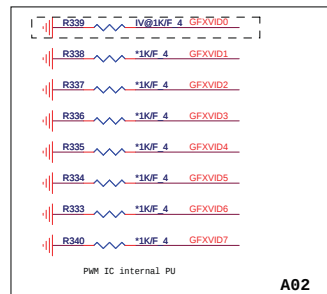
For EC&LAN



TOP View







01/08 Add PAD FOR EMI

