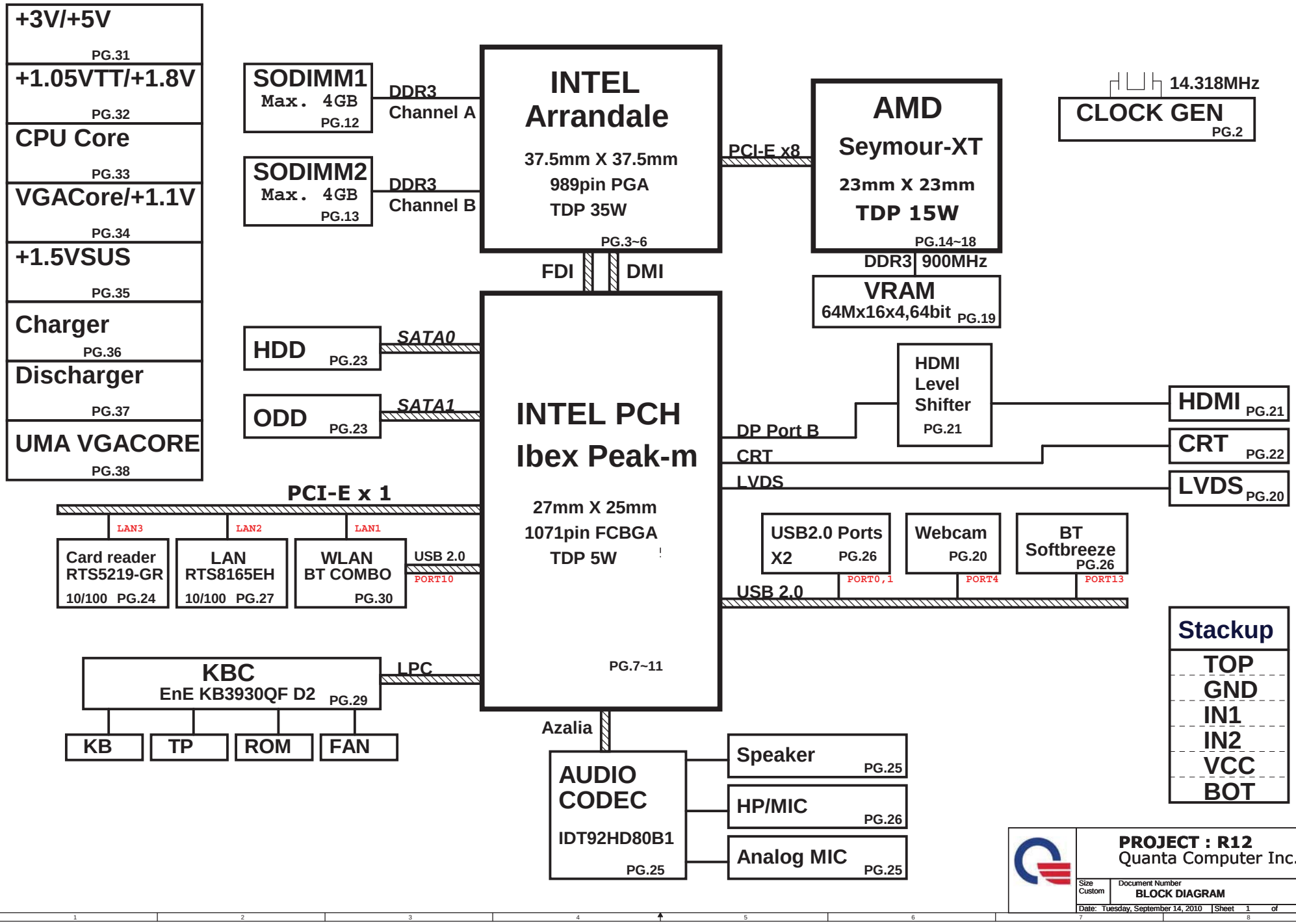
R12 INTEL UMA/DISCRETE SYSTEM DIAGRAM



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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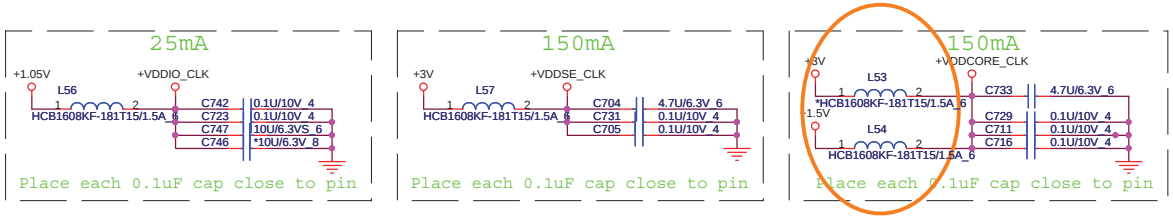
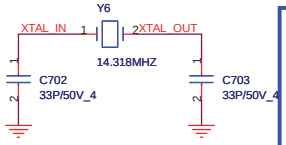
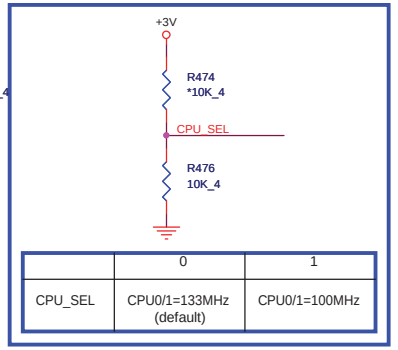
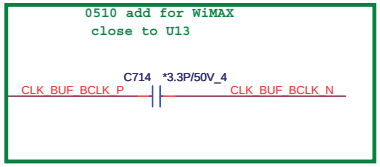
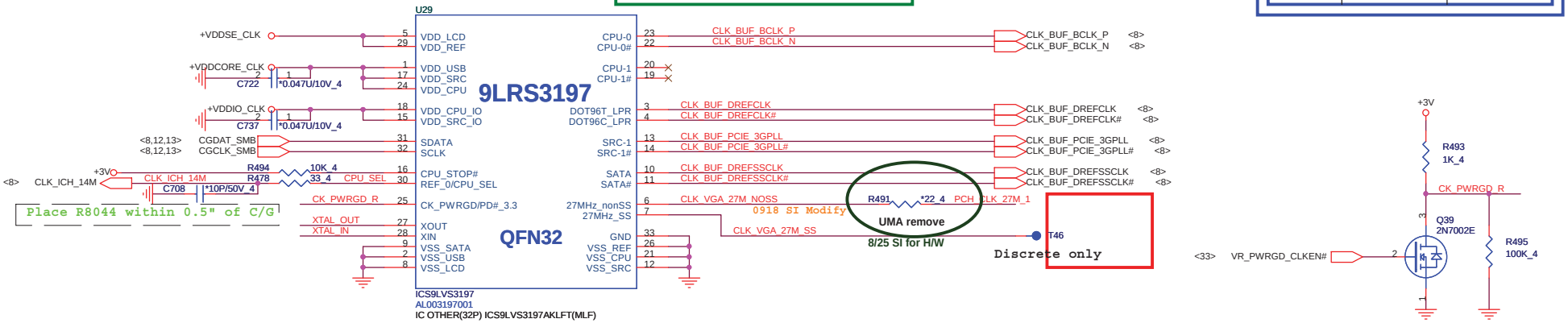




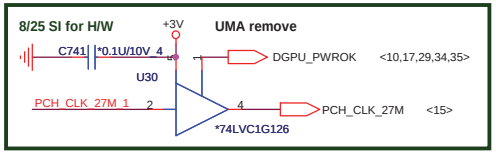


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz





Vender	Part	Part Number	Part Description
ICS	ICS9LVS3197	AL003197000	IC OTHER(32P) ICS9LVS3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)



+1.05V <7,8,9,11,39>
+1.5V <5,30>
+3V <3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36>

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Gen(9LRS3197)	1A

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	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

03

U15A

DMI_TXN0 A24 DMI_RX#[0]
DMI_TXN1 C23 DMI_RX#[1]
DMI_TXN2 B22 DMI_RX#[2]
DMI_TXN3 A21 DMI_RX#[3]
DMI_TXP0 B24 DMI_RX[0]
DMI_TXP1 D23 DMI_RX[1]
DMI_TXP2 B23 DMI_RX[2]
DMI_TXP3 A22 DMI_RX[3]
DMI_RXN0 D24 DMI_TX#[0]
DMI_RXN1 G24 DMI_TX#[1]
DMI_RXN2 F23 DMI_TX#[2]
DMI_RXN3 H23 DMI_TX#[3]
DMI_RXP0 D25 DMI_TX[0]
DMI_RXP1 F24 DMI_TX[1]
DMI_RXP2 E23 DMI_TX[2]
DMI_RXP3 G23 DMI_TX[3]

DMI

2.7GT/s data rate

FDI_TXN[7:0] FDI_TXN0 E22 FDI_TX#[0]
FDI_TXN1 D21 FDI_TX#[1]
FDI_TXN2 D19 FDI_TX#[2]
FDI_TXN3 D18 FDI_TX#[3]
FDI_TXN4 G21 FDI_TX#[4]
FDI_TXN5 E19 FDI_TX#[5]
FDI_TXN6 F21 FDI_TX#[6]
FDI_TXN7 G18 FDI_TX#[7]
FDI_TXP[7:0] FDI_TXP0 D22 FDI_TX[0]
FDI_TXP1 C21 FDI_TX[1]
FDI_TXP2 D20 FDI_TX[2]
FDI_TXP3 C18 FDI_TX[3]
FDI_TXP4 G22 FDI_TX[4]
FDI_TXP5 E20 FDI_TX[5]
FDI_TXP6 F20 FDI_TX[6]
FDI_TXP7 G19 FDI_TX[7]
FDI_FSYNC0 F17 FDI_FSYNC[0]
FDI_FSYNC1 E17 FDI_FSYNC[1]
FDI_INT C17 FDI_INT
FDI_LSYNC0 F18 FDI_LSYNC[0]
FDI_LSYNC1 D17 FDI_LSYNC[1]

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI PEG_ICOMPO PEG_RCOMPO PEG_RBIAS
B26 PEG_COMP R288 49.9/F_4
A26
B27
A25 PEG_RBIAS R289 750/F_4
PEG_RX#[0..7] <14>

PEG_RX#[0] K35 PEG_RX#0
PEG_RX#[1] J34 PEG_RX#1
PEG_RX#[2] J33 PEG_RX#2
PEG_RX#[3] G35 PEG_RX#3
PEG_RX#[4] G32 PEG_RX#4
PEG_RX#[5] F34 PEG_RX#5
PEG_RX#[6] E31 PEG_RX#6
PEG_RX#[7] D35 PEG_RX#7
PEG_RX#[8] E33
PEG_RX#[9] C33
PEG_RX#[10] D32
PEG_RX#[11] B32
PEG_RX#[12] C31
PEG_RX#[13] B28
PEG_RX#[14] B30
PEG_RX#[15] A31

PEG_RX[0..7] <14>
PEG_RX[0] J35 PEG_RX0
PEG_RX[1] H34 PEG_RX1
PEG_RX[2] H33 PEG_RX2
PEG_RX[3] F35 PEG_RX3
PEG_RX[4] G33 PEG_RX4
PEG_RX[5] E34 PEG_RX5
PEG_RX[6] E32 PEG_RX6
PEG_RX[7] D34 PEG_RX7
PEG_RX[8] E33
PEG_RX[9] B33
PEG_RX[10] D31
PEG_RX[11] A32
PEG_RX[12] C30
PEG_RX[13] A28
PEG_RX[14] B29
PEG_RX[15] A30

PEG_TX[0] L33 C_PEG_TX#0 C543 0.1U/10V_4 PEG_TX#0
PEG_TX[1] M35 C_PEG_TX#1 C549 0.1U/10V_4 PEG_TX#1
PEG_TX[2] M33 C_PEG_TX#2 C554 0.1U/10V_4 PEG_TX#2
PEG_TX[3] M30 C_PEG_TX#3 C561 0.1U/10V_4 PEG_TX#3
PEG_TX[4] L31 C_PEG_TX#4 C565 0.1U/10V_4 PEG_TX#4
PEG_TX[5] K32 C_PEG_TX#5 C570 0.1U/10V_4 PEG_TX#5
PEG_TX[6] M29 C_PEG_TX#6 C577 0.1U/10V_4 PEG_TX#6
PEG_TX[7] J31 C_PEG_TX#7 C582 0.1U/10V_4 PEG_TX#7
PEG_TX[8] K29
PEG_TX[9] H30
PEG_TX[10] H29
PEG_TX[11] F29
PEG_TX[12] E28
PEG_TX[13] D29
PEG_TX[14] D27
PEG_TX[15] C26
PEG_TX#[0..7] <14>

UMA remove

PEG_TX[0] L34 C_PEG_TX0 C537 0.1U/10V_4 PEG_TX0
PEG_TX[1] M34 C_PEG_TX1 C546 0.1U/10V_4 PEG_TX1
PEG_TX[2] M32 C_PEG_TX2 C550 0.1U/10V_4 PEG_TX2
PEG_TX[3] L30 C_PEG_TX3 C557 0.1U/10V_4 PEG_TX3
PEG_TX[4] M31 C_PEG_TX4 C562 0.1U/10V_4 PEG_TX4
PEG_TX[5] K31 C_PEG_TX5 C566 0.1U/10V_4 PEG_TX5
PEG_TX[6] M28 C_PEG_TX6 C572 0.1U/10V_4 PEG_TX6
PEG_TX[7] H31 C_PEG_TX7 C578 0.1U/10V_4 PEG_TX7
PEG_TX[8] K28
PEG_TX[9] G30
PEG_TX[10] G29
PEG_TX[11] F28
PEG_TX[12] E27
PEG_TX[13] D28
PEG_TX[14] C27
PEG_TX[15] C25
PEG_TX[0..7]

IC,AUB_CFD_rPGA,R1P0

U15B

MISC
COMP3 COMP2 COMP1 COMP0 SKTOCC#
R139 20/F_4 H_COMP3 AT23
R142 20/F_4 H_COMP2 AT24
R81 49.9/F_4 H_COMP1 G16
R143 49.9/F_4 H_COMP0 AT26
AH24

THERMAL
CATERR# PECI PROCHOT# THERMTRIP#
H_CATERR# AK14
<10> H_PECI AT15
<29,33> H_PROCHOT# AN26
<10,29> PM_THRMTRIP# AK15

PWR MANAGEMENT
RESET_OBS# PM_SYNC VCCPWRGOOD_1 VCCPWRGOOD_0 SM_DRAMPWROK TAPPWRGOOD VTTPWRGOOD RSTIN#
T31 H_CPURST# AP26
<9> PM_SYNC AL15
AN14
<10> H_PWRGOOD AN27
<9> PM_DRAM_PWRGD AK13
T45 H_PWRGD_XDP AM26
H_VTTPWRGD AM15
<8,14,24,27,29,30> PLTRST# CPU_PLTRST# AL14
R124 1.5K/F_4
R126 750/F_4

CLOCKS
BCLK BCLK# BCLK_ITP BCLK_ITP# PEG_CLK PEG_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#
A16 CLK_CPU_BCLK <10>
B16 CLK_CPU_BCLK# <10>
AR30
AT30
For ITP CLk
CLK_PCIE_3GPLL <8>
CLK_PCIE_3GPLL# <8>
Rc
E16
D16
Ra
A18 DREFSSCLK_R DREFSSCLK <8>
A17 DREFSSCLK# R DREFSSCLK# <8>
Rb

DDR3 MISC
SM_DRAMRST# SM_RCOMP[0] SM_RCOMP[1] SM_RCOMP[2] PM_EXT_TS#[0] PM_EXT_TS#[1]
F6 DDR3_DRAMRST# C
AL1 SM_RCOMP R363 100/F_4
AM1 SM_RCOMP R364 24.9/F_4
AN1 SM_RCOMP R365 130/F_4
R176 10K_4
AN15 PM_EXT_TS# R177 *0_4/S +1.05V_VTT PM_EXTTS#0 <12,13>
AP15 PM_EXT_TS# R166 *0_4/S PM_EXTTS#1 <13>
R168 10K_4 +1.05V_VTT

JTAG & BPM
PRDY# PREQ# TCK TMS TRST# TDI TDO TDI_M TDO_M DBR#
AT28 XDP_PRDY# T44
AP27 XDP_PREQ# T28
AN28 XDP_TCLK T25
AP28 XDP_TMS T27
AT27 XDP_TRST# T32
AT29 XDP_TDI_R T33
AR27 XDP_TDO_R T30
AR29 XDP_TDI_M T29
AP29 XDP_TDO_M T26
BPM#[0] AJ22
BPM#[1] AK22
BPM#[2] AK24
BPM#[3] AJ24
BPM#[4] AJ25
BPM#[5] AH22
BPM#[6] AK23
BPM#[7] AH23
AN25 XDP_DBRESET# <9>

IC,AUB_CFD_rPGA,R1P0

<14> +1.05V_VTT
XDP_TDO_R R144 51_4
H_CATERR# R119 49.9/F_4
H_PROCHOT# R130 56.2/F_4
CPU_PLTRST# R123 *68_4
XDP_TMS R138 *51_4
XDP_TDI_R R145 *51_4
XDP_PREQ# R141 *51_4
XDP_TCLK R137 *51_4

U10
MC74VHC1G08DFT2G
+3V
<29,31,32,35,38,39> HWPG
HWPG_1 R170 2K/F_4 H_VTTPWRGD
R164 1K/F_4

JTAG MAPPING
XDP_TDI_R Ra
XDP_TDO_M Rb
Rc R140 0_4
XDP_TDI_M Rd
XDP_TDO_R Re
XDP_TRST# R147 51_4

for S3 power reduction
R62 *0_4
Q6 BSS138_NL
DDR3_DRAMRST# C
DDR3_DRAMRST# <12,13>
SI modify
R66 100K_4
PCIE_CLK_REQ7# <10>
C98 0.047U/10V_4
R58 10K_4
+3VS5

SI modify
+3VS5 +1.5VSUS
R187 *10K_4
R186 *8.2K_4
R184 *0_4
R178 *0_4
R172 *0_4/S HWPG_1
R179 1.5K/F_4
<32> STAT_1.1
U9
*MC74VHC1G08DFT2G
PM_DRAM_PWRGD
R163 750/F_4
Use a voltage divider with VDDQ (1.5 V) rail ON in S3) and resistor combination of 1.5K ±1% (to VDDQ)/750±1% (to GND) to convert to processor VTT level.

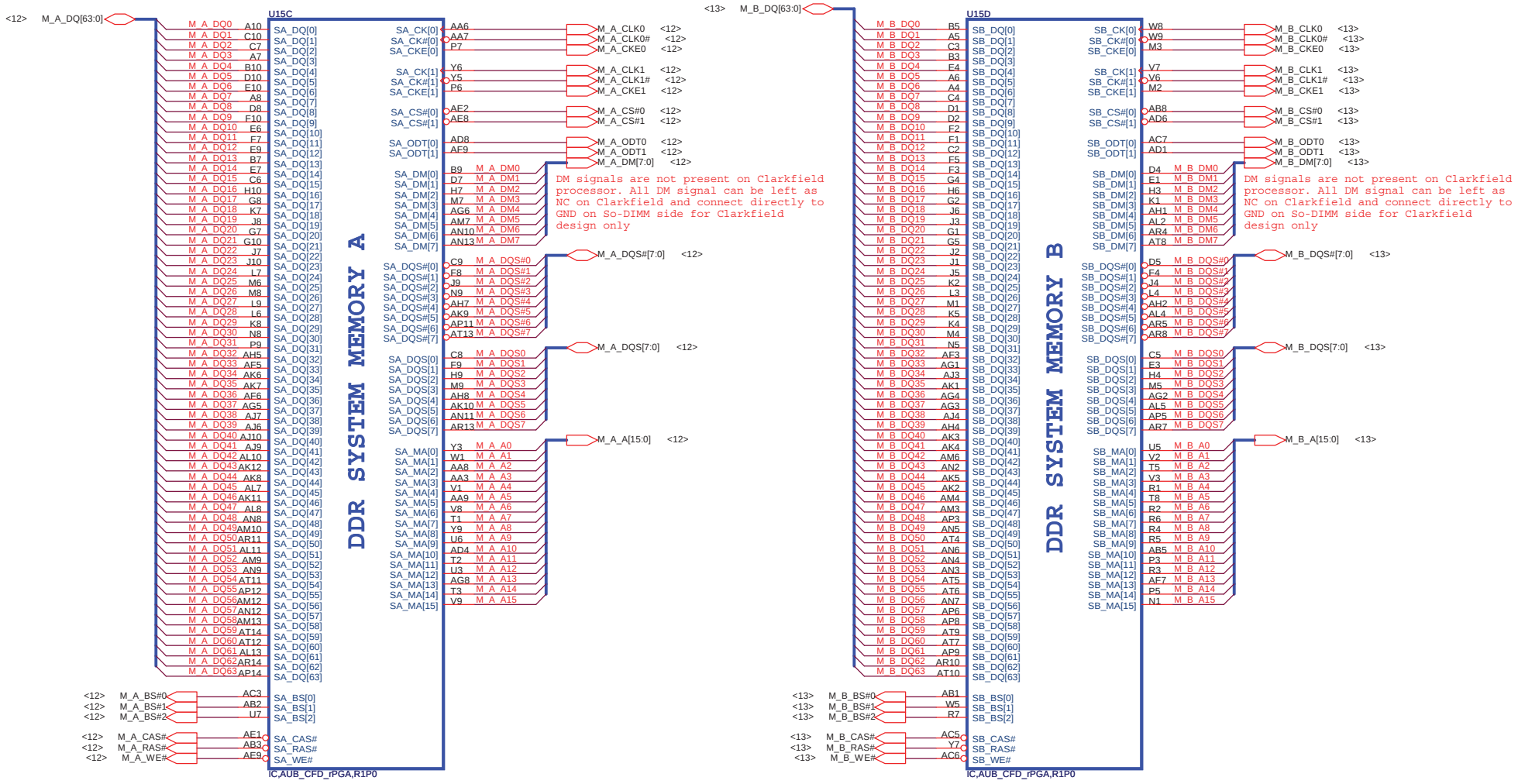
<5,10,11,29,32,33,38> +1.05V_VTT
<5,12,13,34,35,36> +1.5VSUS
<2,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V

Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	1A
Date: Sunday, September 19, 2010	Sheet 3 of 39	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	1A

Date: Tuesday, September 14, 2010 | Sheet 4 of 39

	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

	DIS	UMA
Ra	0 ohm	NA

18A

2A

8/25 SI for H/W.

UMA only

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

0510 add for WiMAX

for S3 power reduction

SI modify

40mile routing

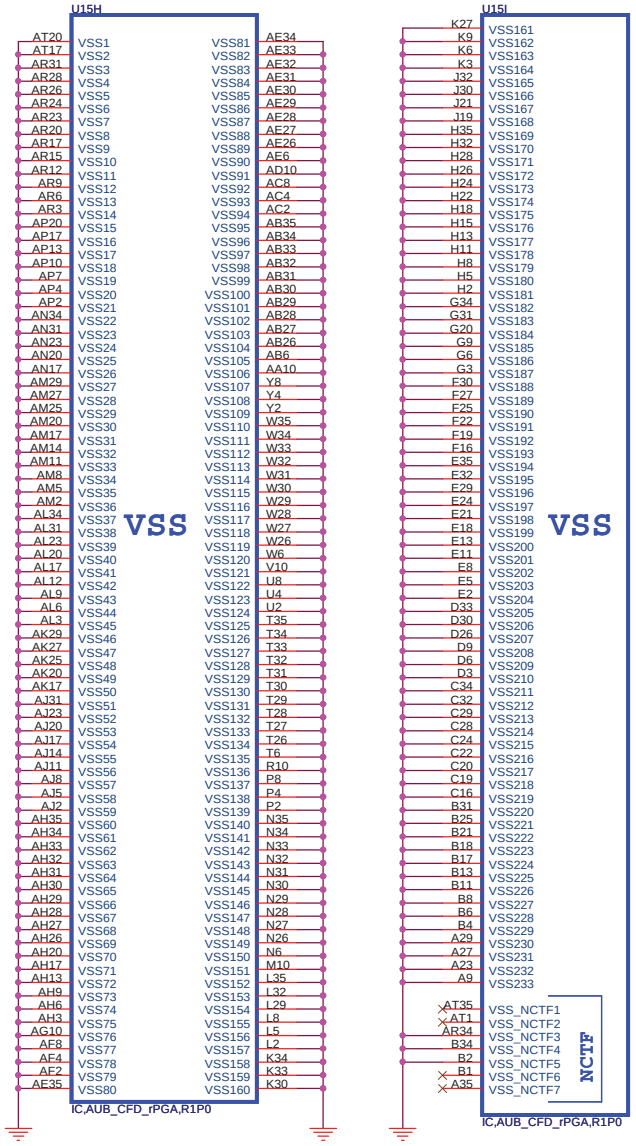
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

PROJECT : R12
Quanta Computer Inc.

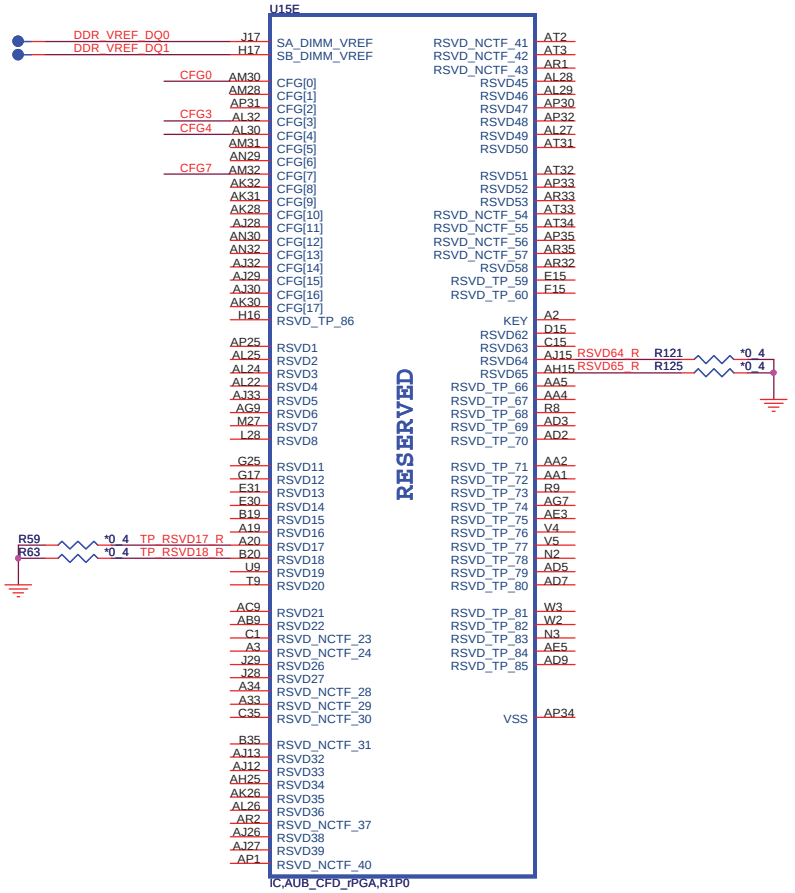
Size	Document Number	Rev
Custom	PROCESSER 3/4(POWER)	1A

Date: Sunday, September 19, 2010 Sheet 5 of 39

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



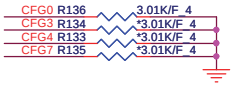
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only



CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4 (GND)	1A

Date: Sunday, September 19, 2010 | Sheet 6 of 39

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U24A

Ibex-M 1 OF 10

RTC
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN

LPC
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
(+3V) LDRQ1# / GPIO23
SERIRQ

SATA
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATALED#
(+3V) SATA0GP / GPIO21
(+3V_S5) SATA1GP / GPIO19

IHDA
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33 (+3V)
HDA_DOCK_RST# / GPIO13 (+3V_S5)

JTAG
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TRST#

SPI
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO

IbexPeak-M_Rev1_0

must add test point.

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)

U24D

Ibex-M 4 OF 10

SDVO
SDVO_TVCLKINN
SDVO_TVCLKINP
SDVO_STALLN
SDVO_STALLP
SDVO_INTN
SDVO_INTP
SDVO_CTRLCLK
SDVO_CTRLDATA

Digital Display Interface

DISPLAY PORT B
DDPB_AUXN
DDPB_AUXP
DDPB_HPD
DDPB_0N
DDPB_0P
DDPB_1N
DDPB_1P
DDPB_2N
DDPB_2P
DDPB_3N
DDPB_3P

DISPLAY PORT C
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPC_AUXN
DDPC_AUXP
DDPC_HPD
DDPC_0N
DDPC_0P
DDPC_1N
DDPC_1P
DDPC_2N
DDPC_2P
DDPC_3N
DDPC_3P

DISPLAY PORT D
DDPD_CTRLCLK
DDPD_CTRLDATA
DDPD_AUXN
DDPD_AUXP
DDPD_HPD
DDPD_0N
DDPD_0P
DDPD_1N
DDPD_1P
DDPD_2N
DDPD_2P
DDPD_3N
DDPD_3P

LVDS_BLON
DISP_ON
DPST_PWM
EDIDCLK
EDIDDATA
L_BKLTEN
L_VDD_EN
L_BKLTCTL
L_DDC_CLK
L_DDC_DATA
L_CTRL_CLK
L_CTRL_DATA
LVD_IBG
LVD_VBG
LVD_VREFH
LVD_VREFL

HDD0 (SATA3 6.0Gb/s)

LVDS--A
TXLCLKOUT-
TXLCLKOUT+
LVDSA_CLK#
LVDSA_CLK
TXLOUT0-
TXLOUT1-
TXLOUT2-
LVDSA_DATA#0
LVDSA_DATA#1
LVDSA_DATA#2
LVDSA_DATA#3
TXLOUT0+
TXLOUT1+
TXLOUT2+
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3

LVDS--B
TXUCLKOUT-
TXUCLKOUT+
LVDSB_CLK#
LVDSB_CLK
TXUOUT0-
TXUOUT1-
TXUOUT2-
LVDSB_DATA#0
LVDSB_DATA#1
LVDSB_DATA#2
LVDSB_DATA#3
TXUOUT0+
TXUOUT1+
TXUOUT2+
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDSB_DATA3

CRT
CRT_B
CRT_G
CRT_R
DDCCLK
DDCDATA
HSYNC_COM
VSYNC_COM
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_VSYNC
DAC_IREF
CRT_IRTN

IbexPeak-M_Rev1_0

UMA HDMI signals

DPB_CTRL_CLK
DPB_CTRL_DATA
DPB_LANE0_N
DPB_LANE0_P
DPB_LANE1_N
DPB_LANE1_P
DPB_LANE2_N
DPB_LANE2_P
DPB_LANE3_N
DPB_LANE3_P
SDVO_CLK
SDVO_DATA
IN_D2#
IN_D2
IN_D1#
IN_D1
IN_D0#
IN_D0
IN_CLK#
IN_CLK
DPB_HPD_O
HDMI_HPD_CON

Q18 *2N7002K

For ES1 ONLY.NI for ES2.

For ES1 ONLY.NI for ES2.

Part
Part Number
Part Description

For AUDIO

ACZ_RST#_AUDIO
ACZ_SDOUT_AUDIO
ACZ_SYNC_AUDIO
BIT_CLK_AUDIO
ACZ_RST#
ACZ_SDOUT
ACZ_SYNC
ACZ_BCLK

For MDC

RTC

1mA

+RTC_CELL
RB500V-40
CR1
CR2
C438 1U/6.3V_4
R242 20K/F_4
C428 1U/6.3V_4
R241 20K/F_4
C429 1U/6.3V_4
R243 1M_4
CN24
R254 1K_4
BAT_CONN
DFWF02MS032
50273-0027N-001-2P-L

8/25 SI for M/E.

4M byte SPI ROM

U22
W25Q32BVSSIG
AKE391P0N00
IC FLASH(8P) W25Q32BVSSIG(SOIC)

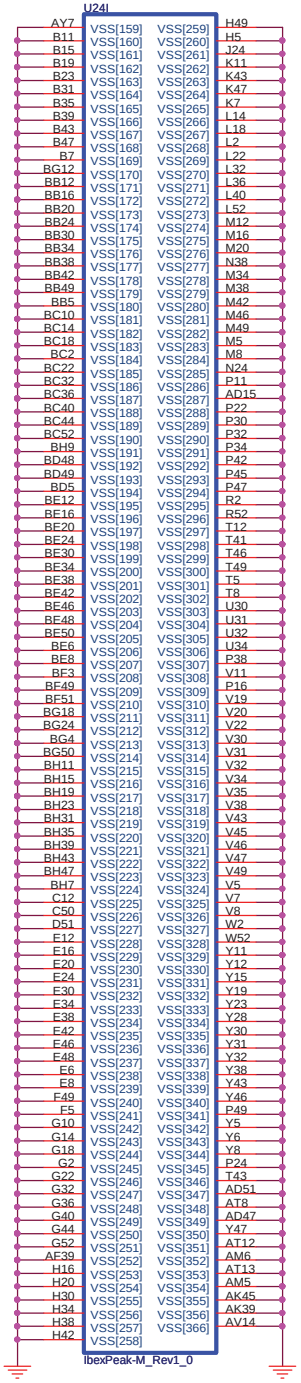
Vender

Socket DG008000031
EON - EN25F32-100HIP
AKE39FN0Q00 IC FLASH(8P) EN25F32-100HIP (SOIC)
WINBOND - W25Q32BVSSIG
AKE391P0N00 IC FLASH(8P) W25Q32BVSSIG(SOIC)

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	1A
Date: Sunday, September 19, 2010	Sheet 7 of 39	

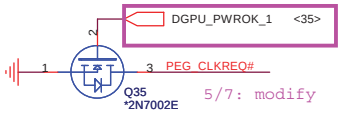
IBEX PEAK-M (GND)

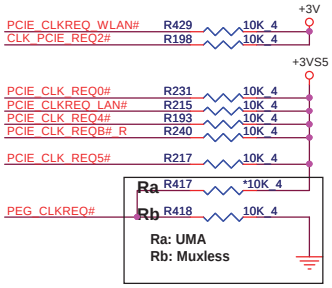


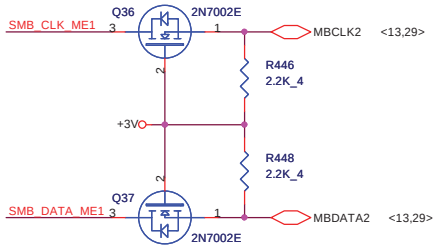
IBEX PEAK-M (PCI-E,SMBUS,CLK)

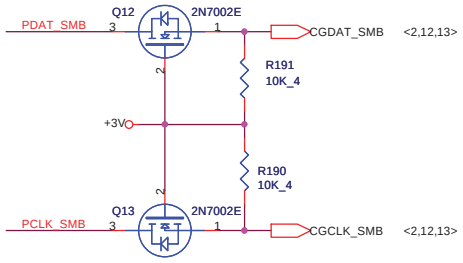
08

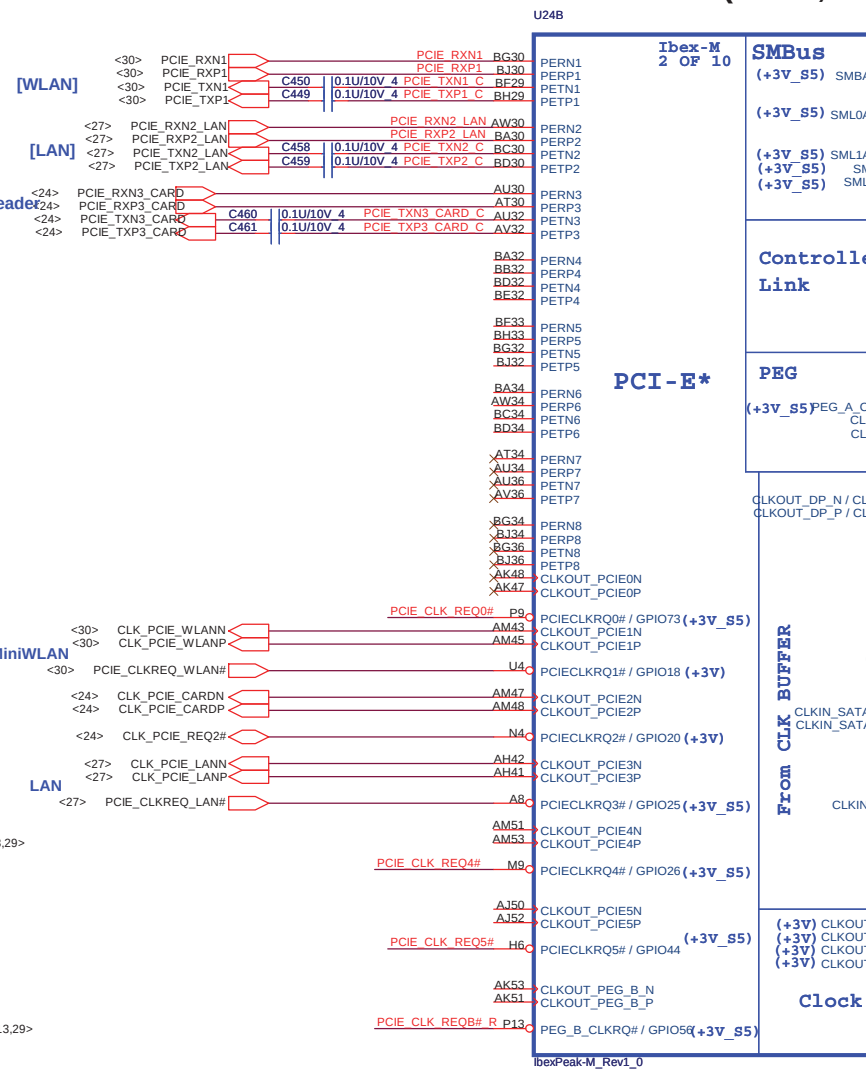
PEG Clock detect (SG only)

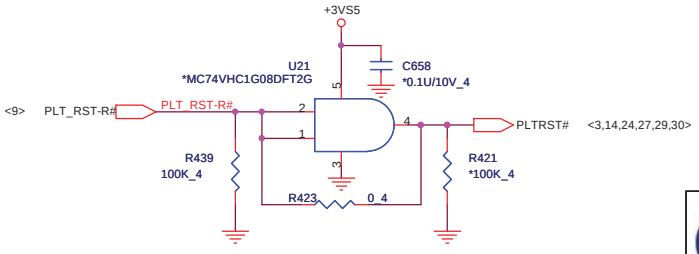


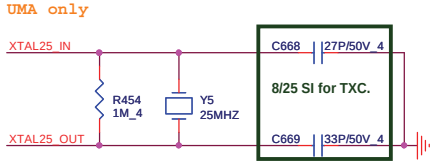












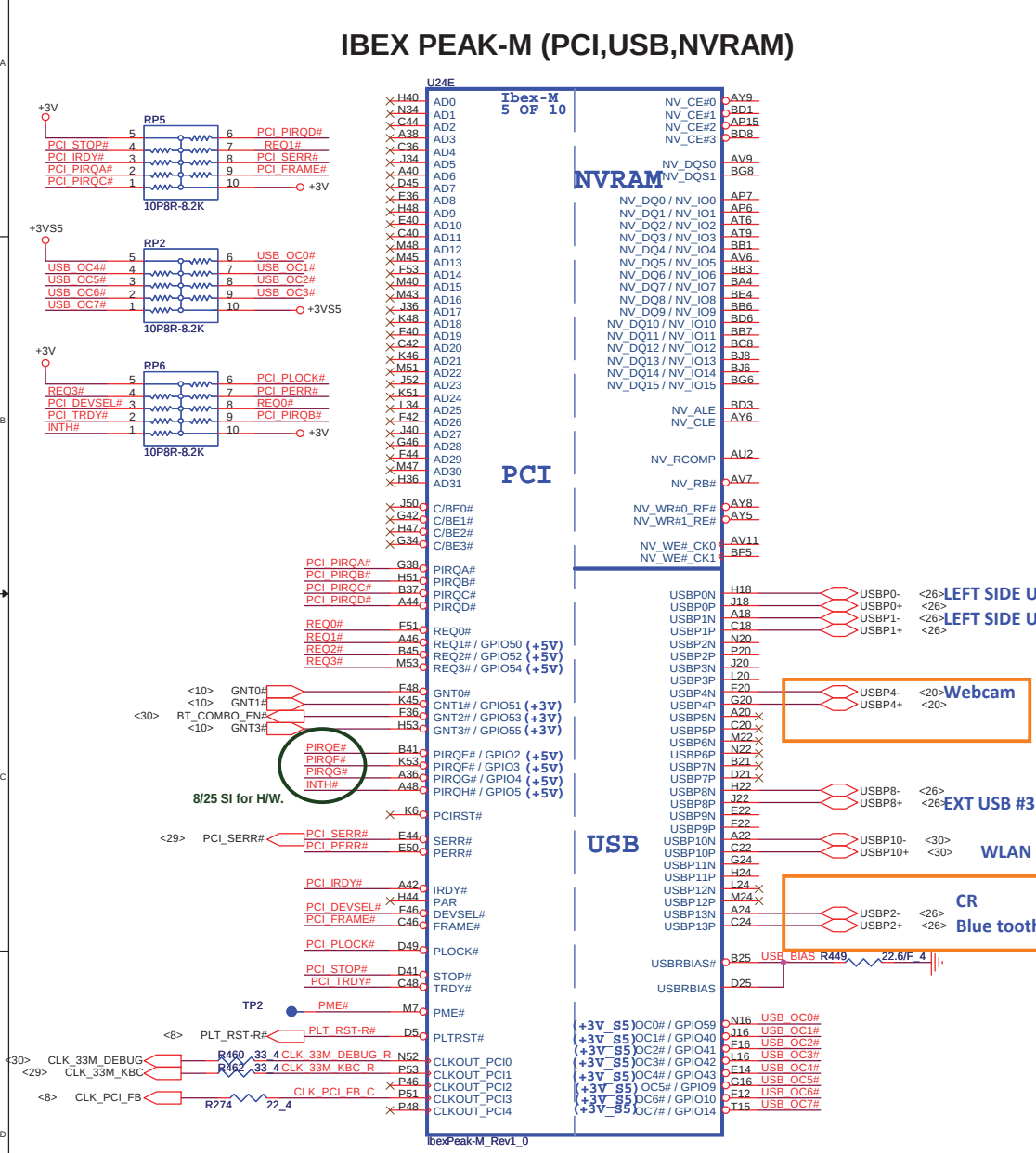
<2,7,9,11,39> +1.05V
<2,3,7,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V

PROJECT : R12
Quanta Computer Inc.

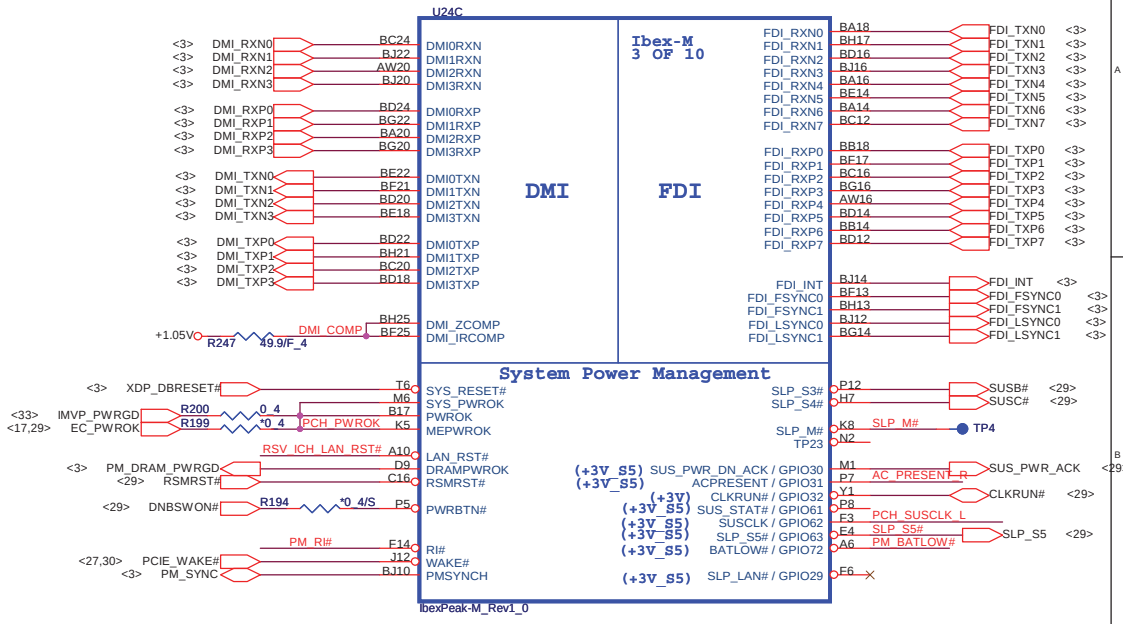
Size	Document Number	Rev
Custom	PCH 2/5 (PCIE, SMBUS, CK)	1A

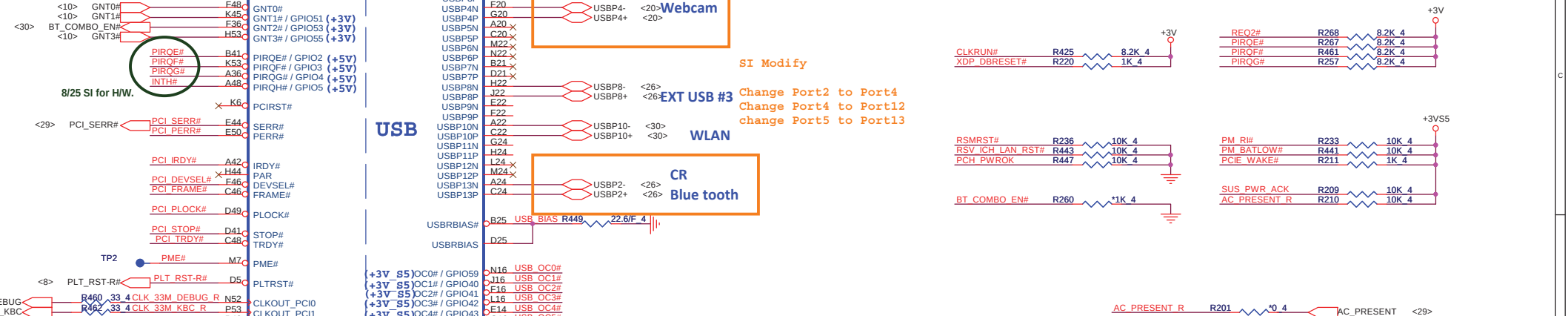
Date: Sunday, September 19, 2010 Sheet 8 of 39

IBEX PEAK-M (PCI,USB,NVRAM)

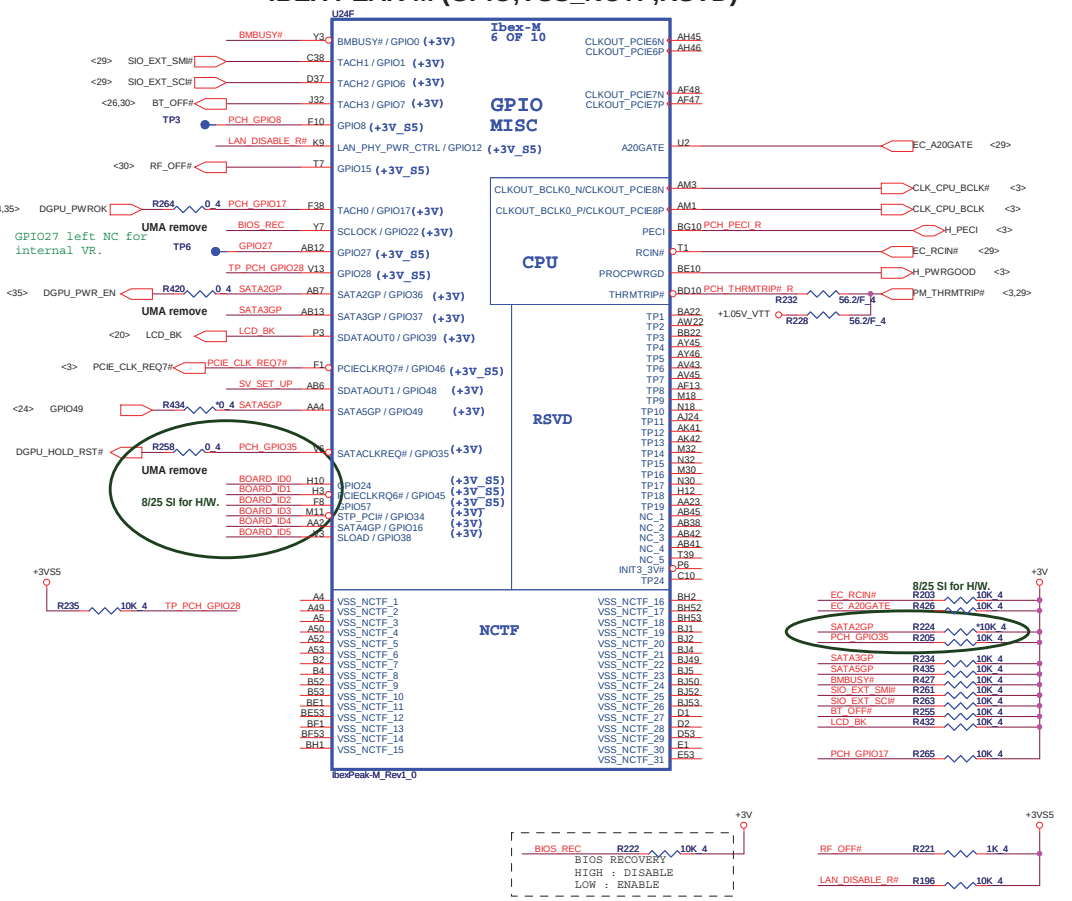


IBEX PEAK-M (DMI,FDI,GPIO)

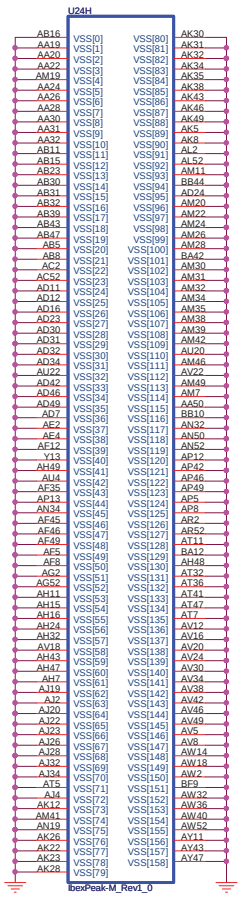


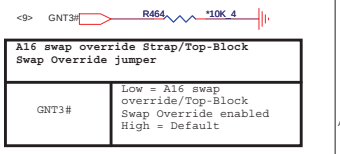


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)





A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

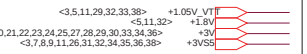
SV_SET_UP	1-X High = Strong (Default)

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

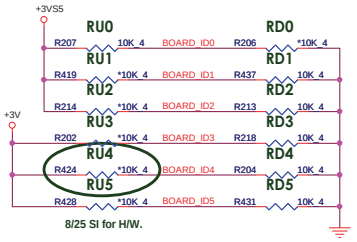
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap



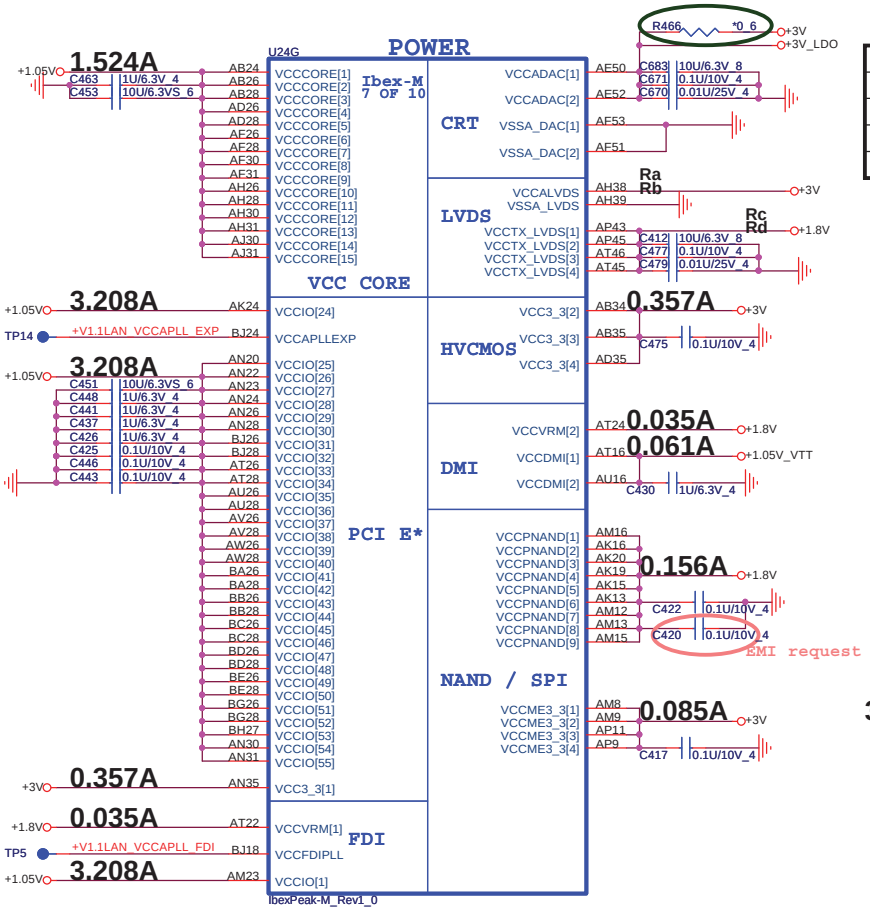
R12 MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
UMA						
31R12MB0000 (PIM) 31R12MB0010 (PDT)	0 0	0 0	0 0	0 0	0 0	0 0
Seymour XT Hynix 512						
31R12MB0020 (PIM) 31R12MB0030 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Samsung 512						
31R12MB0040 (PIM) 31R12MB0050 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Hynix 1G						
31R12MB0060 (PIM) 31R12MB0070 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Samsung 1G						
31R12MB0080 (PIM) 31R12MB0090 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0

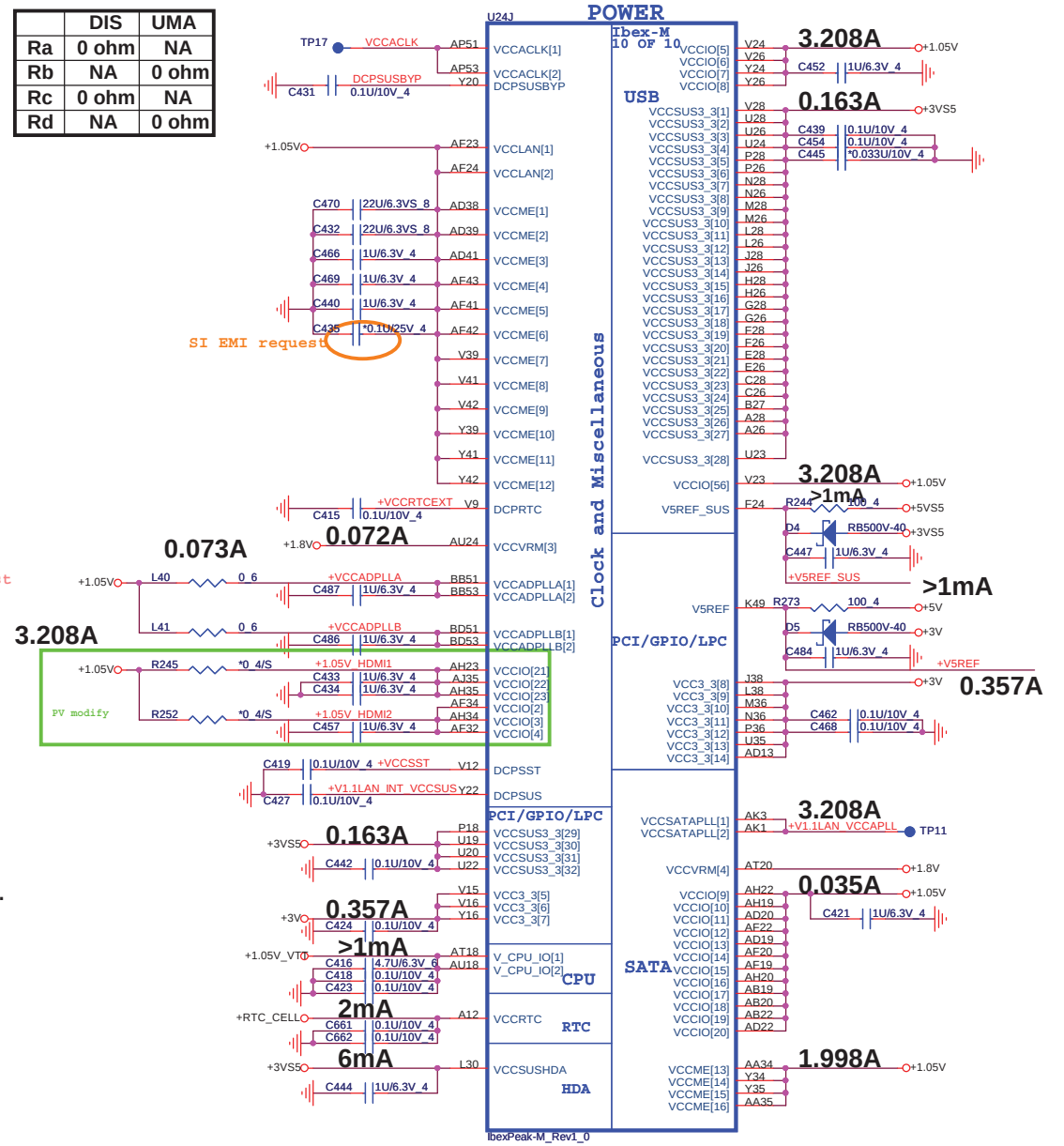
Board ID	ID0 GPIO24	ID1 GPIO45	ID2 GPIO57	ID3 GPIO34	ID4 GPIO35	ID5 GPIO38
UMA/DIS	0=UMA 1=Dis.					
Reserve		0=No 1=Yes				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes



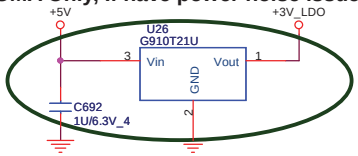
8/25 SI modify
Uninstall on UMA
Install on DIS

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm





UMA Only, If have power noise issue then stuff it.



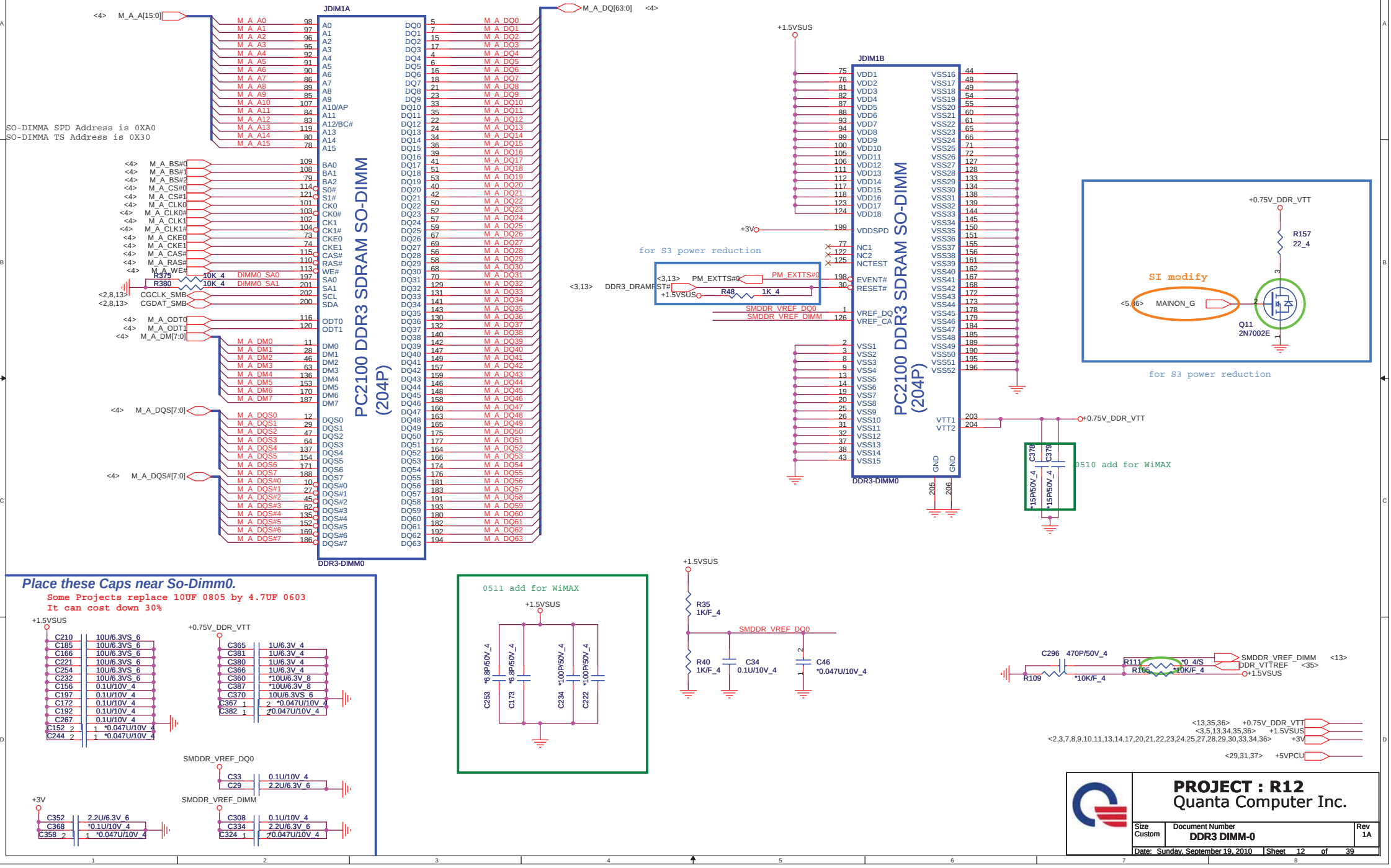
8/25 SI modify
Install LDO when UMA

<2,7,8,9,39> +1.05V
<3,5,10,29,32,33,38> +1.05V_VTT
<5,32> +1.8V
<2,3,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<3,7,8,9,10,26,31,32,34,35,36,38> +3VS5
<17,21,22,23,25,28,30,36> +5V
<20,26,31,32,33,34,35,36,38,39> +5VS5

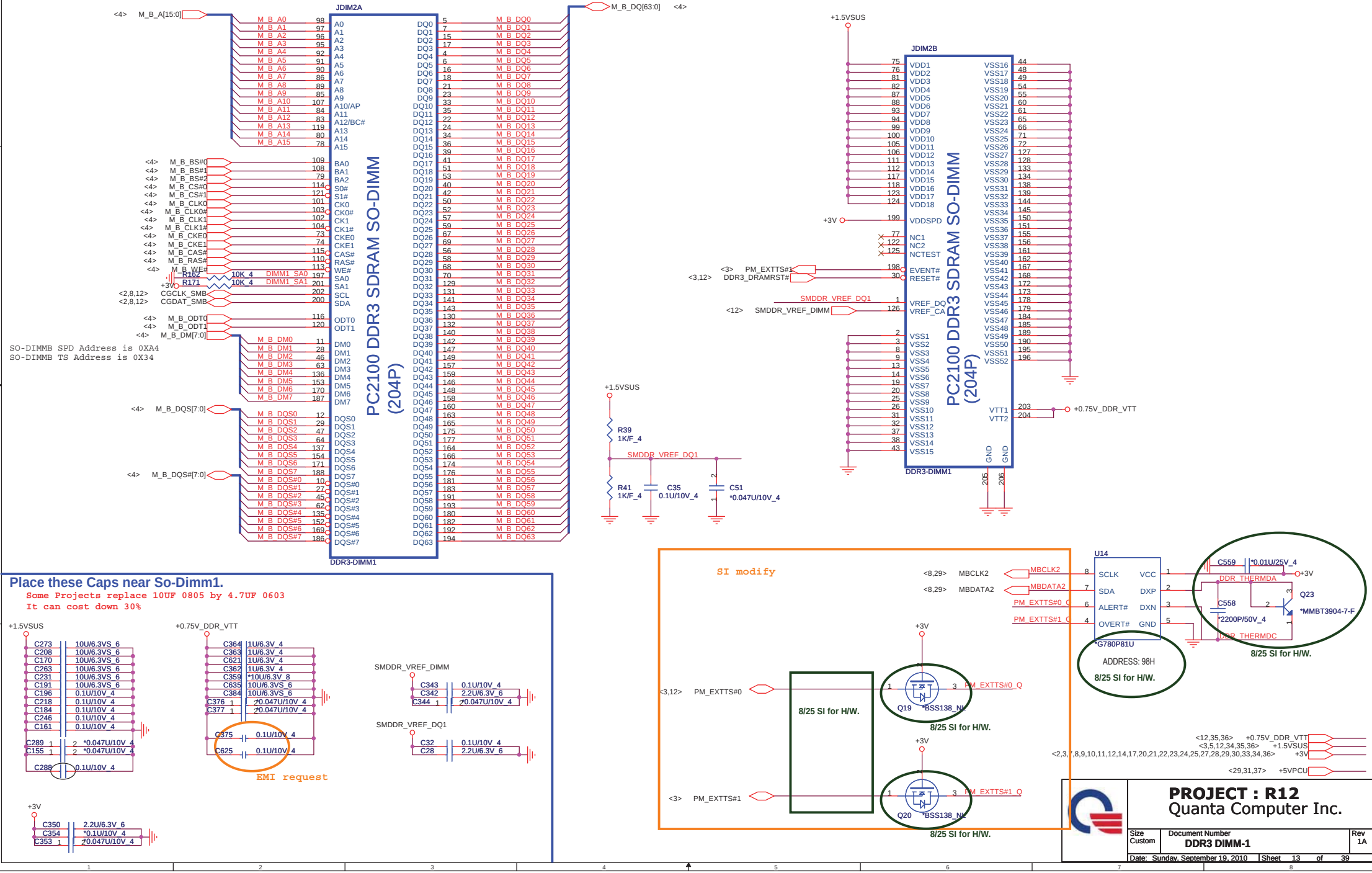
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	1A

Date: Sunday, September 19, 2010 | Sheet 11 of 39



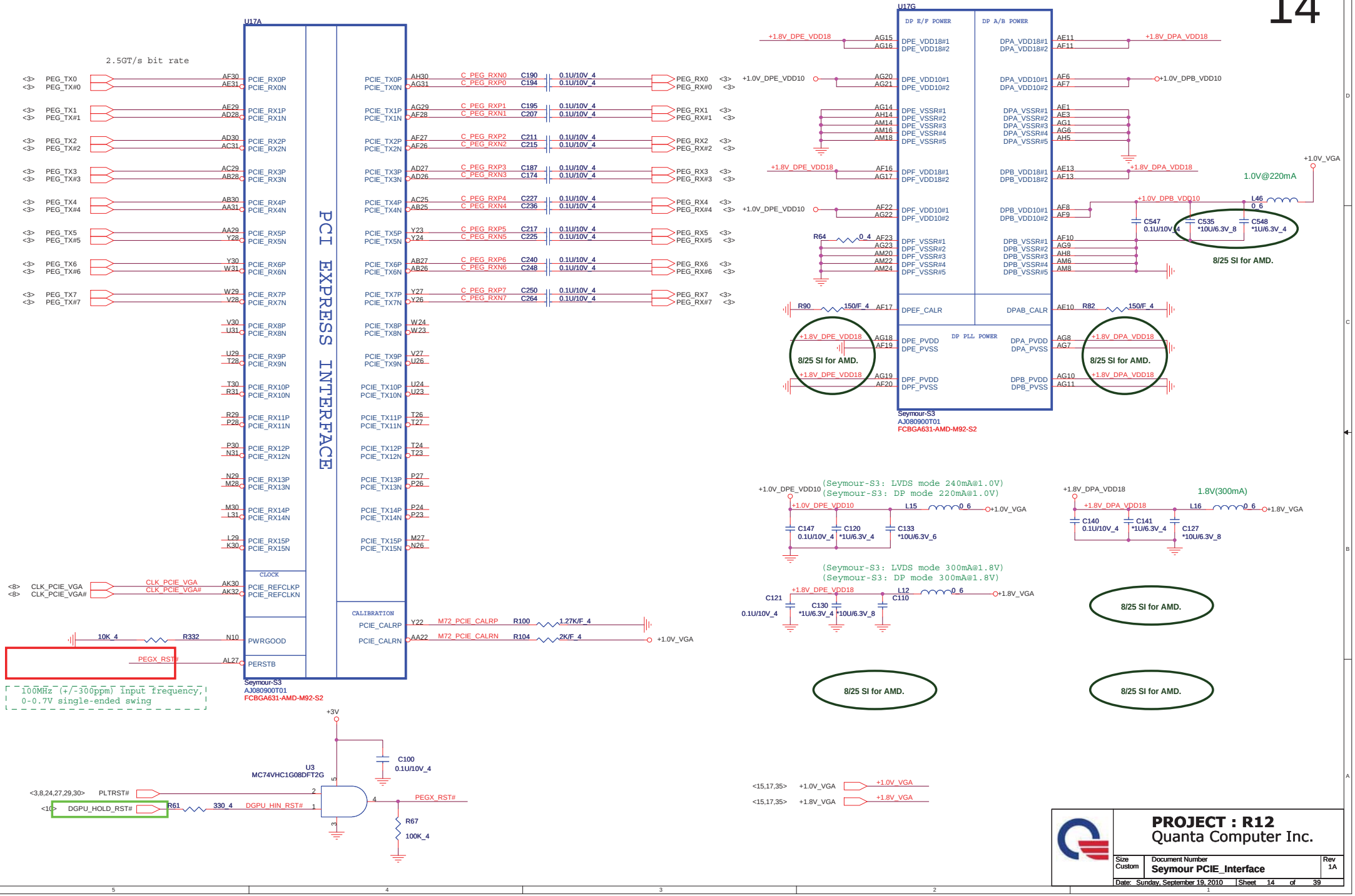
PROJECT : R12		
Quanta Computer Inc.		
Size: Custom	Document Number: DDR3 DIMM-0	Rev: 1A
Date: Sunday, September 19, 2010	Sheet 12 of 39	



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A

Date: Sunday, September 19, 2010 Sheet 13 of 39


U17A
PCI EXPRESS INTERFACE
2.5GT/s bit rate
PEG_TX0 PEG_TX#0 PEG_TX1 PEG_TX#1 PEG_TX2 PEG_TX#2 PEG_TX3 PEG_TX#3 PEG_TX4 PEG_TX#4 PEG_TX5 PEG_TX#5 PEG_TX6 PEG_TX#6 PEG_TX7 PEG_TX#7
PCIE_RX0P PCIE_RX0N PCIE_RX1P PCIE_RX1N PCIE_RX2P PCIE_RX2N PCIE_RX3P PCIE_RX3N PCIE_RX4P PCIE_RX4N PCIE_RX5P PCIE_RX5N PCIE_RX6P PCIE_RX6N PCIE_RX7P PCIE_RX7N PCIE_RX8P PCIE_RX8N PCIE_RX9P PCIE_RX9N PCIE_RX10P PCIE_RX10N PCIE_RX11P PCIE_RX11N PCIE_RX12P PCIE_RX12N PCIE_RX13P PCIE_RX13N PCIE_RX14P PCIE_RX14N PCIE_RX15P PCIE_RX15N
PCIE_TX0P PCIE_TX0N PCIE_TX1P PCIE_TX1N PCIE_TX2P PCIE_TX2N PCIE_TX3P PCIE_TX3N PCIE_TX4P PCIE_TX4N PCIE_TX5P PCIE_TX5N PCIE_TX6P PCIE_TX6N PCIE_TX7P PCIE_TX7N PCIE_TX8P PCIE_TX8N PCIE_TX9P PCIE_TX9N PCIE_TX10P PCIE_TX10N PCIE_TX11P PCIE_TX11N PCIE_TX12P PCIE_TX12N PCIE_TX13P PCIE_TX13N PCIE_TX14P PCIE_TX14N PCIE_TX15P PCIE_TX15N
C_PEG_RXN0 C_PEG_RXP0 C_PEG_RXN1 C_PEG_RXP1 C_PEG_RXN2 C_PEG_RXP2 C_PEG_RXN3 C_PEG_RXP3 C_PEG_RXN4 C_PEG_RXP4 C_PEG_RXN5 C_PEG_RXP5 C_PEG_RXN6 C_PEG_RXP6 C_PEG_RXN7 C_PEG_RXP7
C190 C194 C195 C207 C211 C215 C187 C174 C227 C236 C217 C225 C240 C248 C250 C264
0.1U/10V_4
PEG_RX0 PEG_RX#0 PEG_RX1 PEG_RX#1 PEG_RX2 PEG_RX#2 PEG_RX3 PEG_RX#3 PEG_RX4 PEG_RX#4 PEG_RX5 PEG_RX#5 PEG_RX6 PEG_RX#6 PEG_RX7 PEG_RX#7
CLOCK
CLK_PCIE_VGA CLK_PCIE_VGA#
PCIE_REFCLKP PCIE_REFCLKN
PWRGOOD PERSTB
10K_4 R332 PEGX_RST#
100MHz (+/-300ppm) input frequency, 0-0.7V single-ended swing
CALIBRATION
PCIE_CALRP PCIE_CALRN
M72_PCIE_CALRP M72_PCIE_CALRN
R100 1.27K/F_4 R104 2K/F_4
+1.0V_VGA
Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2
U3
MC74VHC1G08DFT2G
+3V
C100 0.1U/10V_4
<3,8,24,27,29,30> PLTRST#
<10> DGPU_HOLD_RST#
R61 330_4 DGPU_HIN_RST#
PEGX_RST#
R67 100K_4
U17G
DP E/F POWER
DP A/B POWER
+1.8V_DPE_VDD18 +1.0V_DPE_VDD10
DPE_VDD18#1 DPE_VDD18#2 DPE_VDD10#1 DPE_VDD10#2 DPE_VSSR#1 DPE_VSSR#2 DPE_VSSR#3 DPE_VSSR#4 DPE_VSSR#5
DPF_VDD18#1 DPF_VDD18#2 DPF_VDD10#1 DPF_VDD10#2 DPF_VSSR#1 DPF_VSSR#2 DPF_VSSR#3 DPF_VSSR#4 DPF_VSSR#5
DPA_VDD18#1 DPA_VDD18#2 DPA_VDD10#1 DPA_VDD10#2 DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5
DPB_VDD18#1 DPB_VDD18#2 DPB_VDD10#1 DPB_VDD10#2 DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5
+1.8V_DPA_VDD18 +1.0V_DPB_VDD10
DPEF_CALR DPAB_CALR R64 0_4 R90 150/F_4 R82 150/F_4
DP PLL POWER
DPE_PVDD DPE_PVSS DPF_PVDD DPF_PVSS DPA_PVDD DPA_PVSS DPB_PVDD DPB_PVSS
8/25 SI for AMD.
1.0V@220mA
L46 0_6
C547 0.1U/10V_4 C535 *10U/6.3V_8 C548 *1U/6.3V_4
(Seymour-S3: LVDS mode 240mA@1.0V)
(Seymour-S3: DP mode 220mA@1.0V)
L15 0_6 C147 0.1U/10V_4 C120 *1U/6.3V_4 C133 *10U/6.3V_6
1.8V(300mA)
L16 0_6 C140 0.1U/10V_4 C141 *1U/6.3V_4 C127 *10U/6.3V_8
(Seymour-S3: LVDS mode 300mA@1.8V)
(Seymour-S3: DP mode 300mA@1.8V)
L12 0_6 C121 0.1U/10V_4 C130 *1U/6.3V_4 C110 *10U/6.3V_8
<15,17,35> +1.0V_VGA
<15,17,35> +1.8V_VGA
PROJECT : R12
Quanta Computer Inc.
Size Custom
Document Number
Seymour PCIE_Interface
Rev 1A
Date: Sunday, September 19, 2010
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MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ2G63BFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-HC12
0100	Micron	128*16-800MHZ	MT41J128M16HA-125:D
0101	Reserved		
0110	Hynix- Vega die	64*16-900MHZ	H5TQ1G63DFR-11C
0111	Samsung- B die	64*16-900MHZ	K4W1G1646E-HC11
1000	Samsung- G die	64*16-900MHZ	K4W1G1646G-BC11
1001	Reserved		
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63BFR-11C
1011	Samsung- C die	128*16-900MHZ	K4W2G1646C-HC11
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111			

GPIO15 GPIO20

Seymour	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.12V (Default)
TBD	1	1	NA

Access to SCL and SDA is mandatory on BACO designs for debug purposes

GPIO22(ROMCS#) PD without external VBIOS ROM

If no contact this pin to LVDS need pull low

Seymour uninstall Ra to meet AF24 N/C

DAC2 is NC on Seymour

Reserve for DB debug only

Reserve for DB debug only

Seymour-S3--NC ROBSON--install

Robson-- Install Seymour- NC BACO mode -- install

For Int Clk 27Mhz

8/25 SI for H/W.

8/25 SI for H/W.

Memory ID

1.8V(150mA DPC_VDD18)

1.1V(110mA DPC_VDD10)

1.8V(75mA DPLL_PVDD)

1.0V(125mA DPLL_VDDC)

1.8V(20mA TSVDD)

1.8V(70mA)

3.3V(65mA)

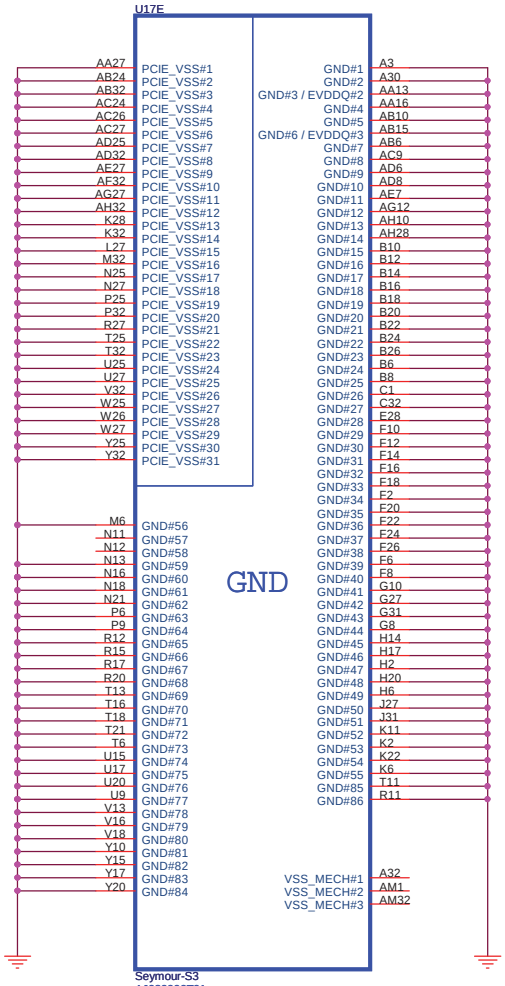
1.8V(45mA VDD1DI)

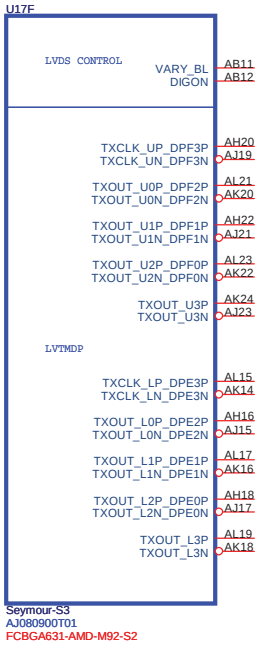
1.8V(2mA)

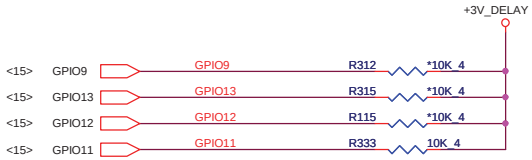
PROJECT : R12
Quanta Computer Inc.

Size: Custom | Document Number: Seymour Main | Rev: 1A

Date: Sunday, September 19, 2010 | Sheet 15 of 39







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

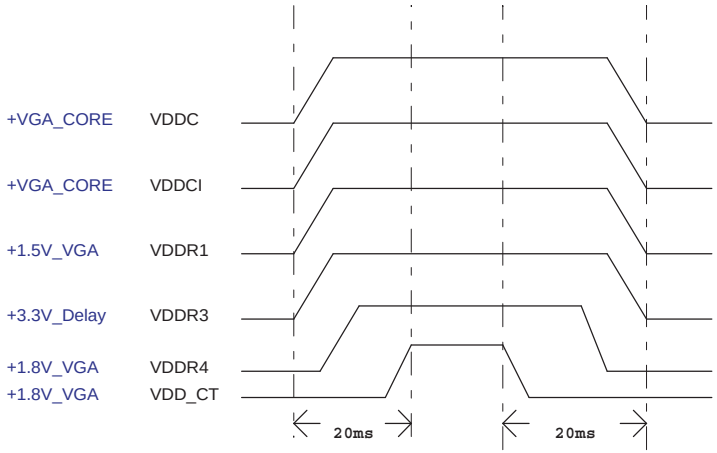
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

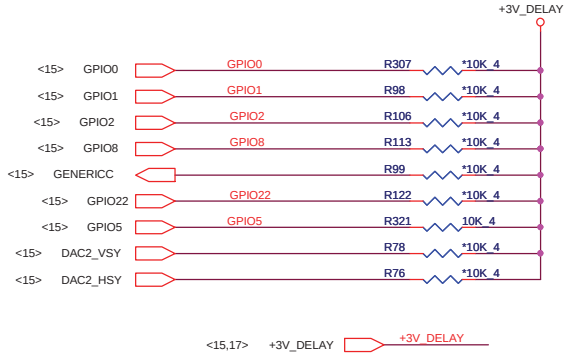
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour GND / LVDS/ Straps	1A
Date: Sunday, September 19, 2010	Sheet 16 of 39	

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

+1.5V_VGA

1.5V (DDR3, MVDDQ = 1.5V@2.0A)

C404 1U/6.3V_4 C327 1U/6.3V_4 C330 1U/6.3V_4 C331 1U/6.3V_4 C336 1U/6.3V_4

C645 10U/6.3VS_6 C624 10U/6.3VS_6 C395 10U/6.3VS_6

U17D

MEM I/O

H13 H16 H19 J10 J23 J24 J9 K10 K23 K24 K9 L11 L12 L13 L20 L21 L22

VDDR1#1 VDDR1#2 VDDR1#3 VDDR1#4 VDDR1#5 VDDR1#6 VDDR1#7 VDDR1#8 VDDR1#9 VDDR1#10 VDDR1#11 VDDR1#12 VDDR1#13 VDDR1#14 VDDR1#15 VDDR1#16 VDDR1#17

PCIE

AB23 AC23 AD24 AE24 AE25 AE26 AF25 AG26

PCIE_VDDR#1 PCIE_VDDR#2 PCIE_VDDR#3 PCIE_VDDR#4 PCIE_VDDR#5 PCIE_VDDR#6 PCIE_VDDR#7 PCIE_VDDR#8

+1.8V_PCIE_VDDR

C242 0.1U/10V_4 C150 0.1U/10V_4 C154 1U/6.3V_4 C136 1U/6.3V_4 C135 1U/6.3V_4 C230 1U/6.3V_4 C137 1U/6.3V_4 C162 10U/6.3VS_6

1.8V(500mA)

PBY160808T-221Y-N/2A_6 L18 +1.8V_VGA

1.8V(110mA VDD_CT)

+1.8V_VGA L22 PBY160808T-121Y-N/2.5A_6 +1.8V_VDD_CT

C163 10U/6.3VS_6 C167 1U/6.3V_4 C241 1U/6.3V_4 C168 1U/6.3V_4 C249 0.1U/10V_4

LEVEL TRANSLATION

AA20 AA21 AB20 AB21

VDD_CT#1 VDD_CT#2 VDD_CT#3 VDD_CT#4

Gated 3.3V 60mA by VDDC

+3V_VGA L19 0_6 +3V_DELAY +3V_DELAY

C228 1U/6.3V_4 C226 1U/6.3V_4 C279 1U/6.3V_4 C243 10U/6.3VS_6

VDD_R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%

Seymour-S3

AA17 AA18 AB17 AB18

VDDR3#1 VDDR3#2 VDDR3#3 VDDR3#4

I/O

+VDDR4

+1.8V_VGA L23 PBY160808T-121Y-N/2.5A_6 +VDDR4

C209 10U/6.3VS_6 C212 1U/6.3V_4 C256 0.1U/10V_4

1.8V(170mA VDDR4)

T14

V12 Y12 U12

VDDR4#1 / VDDR5 VDDR4#2 VDDR4#3 / VDDR5

AA11 Y11

NC#1 / VDDR4 DVCLK / VDDR4

V11 U11

NC#3 / VDDR5 NC / VDDR5

1.8V(75mA MPV18)

+1.8V_VGA L50 BLM18PG471SN1D/1A_6 MPV18

C600 1U/6.3V_4 C602 0.1U/10V_4

MEM CLK

L17 L16

VDDRHA VSSRHA

1.8V(40mA PCIE_PVDD)

+1.8V_PCIE_VDDR

8/25 SI for SMT.

PLL

AM30

PCIE_PVDD

1.8V(90mA SPV18)

+1.8V_VGA L27 PBY160808T-121Y-N/2.5A_6 SPV18

C317 1U/6.3V_4 C295 0.1U/10V_4

MPV18 L8

MPV18

SPV18 H7

SPV18

1.0V_VGA(100mA SPV10)

+1.0V_VGA L29 BLM18PG471SN1D/1A_6 +1.0V_VGA_SPV10

C337 10U/6.3VS_6 C332 0.1U/10V_4 C328 1U/6.3V_4

H8

SPV10

J7

SPVSS

BACK BIAS

M11 M12

BBP#1 BBP#2

<11,21,22,23,25,28,30,36> +5V
<2,3,7,8,9,10,11,12,13,14,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<14,15,35> +1.0V_VGA
<34> +3V_VGA
<34> +VGA_CORE

+5V +3V +1.0V_VGA +3V_VGA +VGA_CORE

Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2

CORE

POWER

AA15 N15 N17 R13 R16 R18 Y21 T12 T15 T17 T20 U13 U16 U18 V21 V15 V17 V20 Y13 Y16 Y18 R21 U21

VDDC#1 VDDC#2 VDDC#3 VDDC#4 VDDC#5 VDDC#6 VDDC#7 VDDC#8 VDDC#9 VDDC#10 VDDC#11 VDDC#12 VDDC#13 VDDC#14 VDDC#15 VDDC#16 VDDC#17 VDDC#18 VDDC#20 VDDC#21 VDDC#22

VDDC#23 /BIF_VDDC VDDC#19/BIF_VDDC

+1.0V_PCIE_VDDC

1.0V(2.0A)

+1.0V_VGA

+1.0V_PCIE_VDDC L23 L24 L25 L26 M22 N22 N23 N24 R22 T22 U22 V22

PCIE_VDDC#1 PCIE_VDDC#2 PCIE_VDDC#3 PCIE_VDDC#4 PCIE_VDDC#5 PCIE_VDDC#6 PCIE_VDDC#7 PCIE_VDDC#8 PCIE_VDDC#9 PCIE_VDDC#10 PCIE_VDDC#11 PCIE_VDDC#12

0_8 L26

C304 1U/6.3V_4 C280 1U/6.3V_4 C269 1U/6.3V_4 C294 1U/6.3V_4 C260 1U/6.3V_4 C299 1U/6.3V_4 C319 1U/6.3V_4 C307 10U/6.3VS_6

VDDC+VDDCI

0.85~1.1V(15A peak)(Ripple < 87.2mV)

+VGA_CORE

C86 1U/6.3V_4 C92 1U/6.3V_4 C293 1U/6.3V_4 C276 1U/6.3V_4 C91 1U/6.3V_4 C268 1U/6.3V_4 C277 1U/6.3V_4 C519 10U/6.3VS_6

C85 1U/6.3V_4 C323 2.2U/6.3V_4 C262 1U/6.3V_4 C305 10U/6.3V_8 C272 1U/6.3V_4 C257 1U/6.3V_4 C258 1U/6.3V_4

C259 1U/6.3V_4 C286 2.2U/6.3V_4 C275 1U/6.3V_4 C87 1U/6.3V_4 C79 1U/6.3V_4 C247 1U/6.3V_4

C81 10U/6.3VS_6 C88 10U/6.3VS_6 C83 10U/6.3VS_6 C521 10U/6.3VS_6 C520 10U/6.3VS_6 C82 10U/6.3VS_6

ISOLATED CORE I/O

M13 M15 M16 M17 M18 M20 M21 N20

VDDCI#1 VDDCI#2 VDDCI#3 VDDCI#4 VDDCI#5 VDDCI#6 VDDCI#7 VDDCI#8

Note1.

BIF_VDDC R112 0_4 +VGA_CORE

Ra

0.95V~1.1V(2A VDDCI)

+VDDCI L24 0_8 +VGA_CORE

C329 1U/6.3V_4 C313 1U/6.3V_4 C306 1U/6.3V_4 C265 10U/6.3VS_6 C266 10U/6.3VS_6 C315 10U/6.3VS_6

Support BACO Mode

+3V R330 *10K_4 not stuff

<34> PX_MODE R334 *0_4

<18> PX_EN

R94 *5.1K_4

Q31 *2N7002E

8/25 SI for AMD.

<34> PX_MODE1

PX_EN Q41 *2N7002E

8/25 SI for AMD.

<9,29> EC_PWROK

Q29 *2N7002E

R500

PX_MODE PX_MODE1

*0_4

R323 *100K_4 Q25 *2N7002E

+3V C592 *0.1U/10V_4

<2,10,29,34,35> DGPU_PWROK

PX_MODE BACO_EN

U18 *TC7SH08FU

+5V R337 *1K_4 R336 *1K_4

PX_EN## PX_EN#

Q28 *2N7002E Q30 *2N7002E

+1.0V_VGA Q10 *AO3416 Q27 *AO3416

PX_EN#

Q9 *AO3416 Q26 *AO3416

+VGA_CORE

PX_EN##

BIF_VDDC

C325 *22U/6.3VS_8 C287 *10U/6.3VS_6 C297 *10U/6.3VS_6 C270 *2.2U/6.3V_4 C271 *2.2U/6.3V_4

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

Note1.

1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour_Power_and_NC	1A

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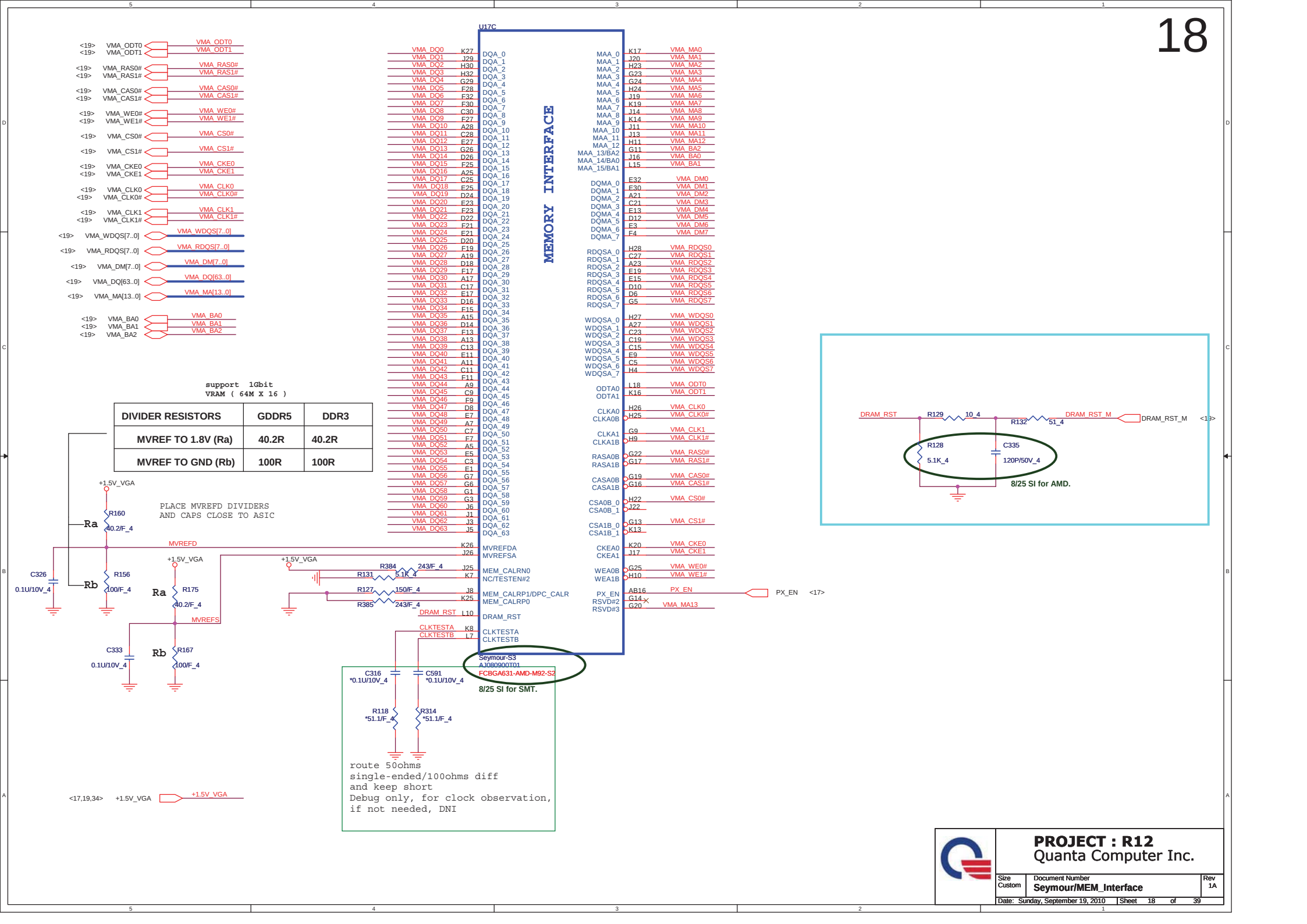
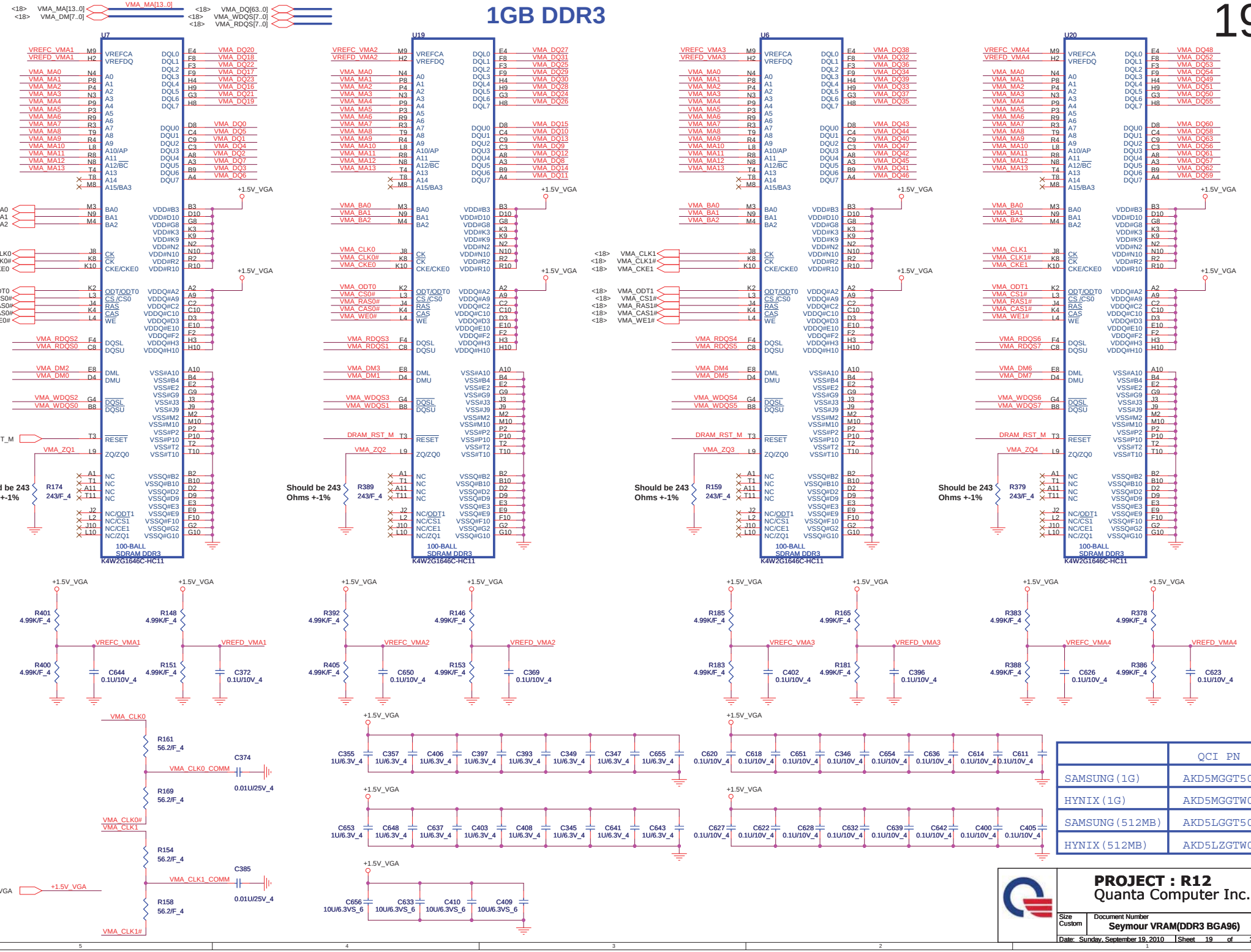

U17C
MEMORY INTERFACE
VMA_ODT0
VMA_ODT1
VMA_RAS0#
VMA_RAS1#
VMA_CAS0#
VMA_CAS1#
VMA_WE0#
VMA_WE1#
VMA_CS0#
VMA_CS1#
VMA_CKE0
VMA_CKE1
VMA_CLK0
VMA_CLK0#
VMA_CLK1
VMA_CLK1#
VMA_WDQS[7..0]
VMA_RDQS[7..0]
VMA_DM[7..0]
VMA_DQ[63..0]
VMA_MA[13..0]
VMA_BA0
VMA_BA1
VMA_BA2
support 1Gbit
VRAM (64M X 16)
DIVIDER RESISTORS
GDDR5
DDR3
MVREF TO 1.8V (Ra)
40.2R
40.2R
MVREF TO GND (Rb)
100R
100R
PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC
+1.5V_VGA
R160
40.2/F_4
Ra
Rb
R156
100/F_4
C326
0.1U/10V_4
MVREFD
R175
40.2/F_4
MVREFS
C333
R167
100/F_4
R384
243/F_4
R131
5.1K_4
R127
150/F_4
R385
243/F_4
DRAM_RST
CLKTESTA
CLKTESTB
C316
*0.1U/10V_4
C591
*0.1U/10V_4
R118
*51.1/F_4
R314
*51.1/F_4
route 50ohms
single-ended/100ohms diff
and keep short
Debug only, for clock observation,
if not needed, DNI
Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2
8/25 SI for SMT.
PX_EN
VMA_MA13
DRAM_RST
R129
10_4
R132
51_4
DRAM_RST_M
R128
5.1K_4
C335
120P/50V_4
8/25 SI for AMD.
<17,19,34> +1.5V_VGA

1GB DDR3



	QCI PN
SAMSUNG(1G)	AKD5MGGT503
HYNIX(1G)	AKD5MGGTW02
SAMSUNG(512MB)	AKD5LGGT503
HYNIX(512MB)	AKD5LZGTW01

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour VRAM(DDR3 BGA96)	3A

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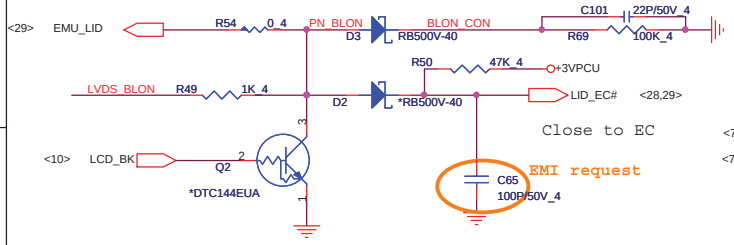
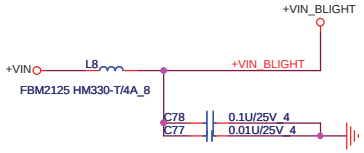
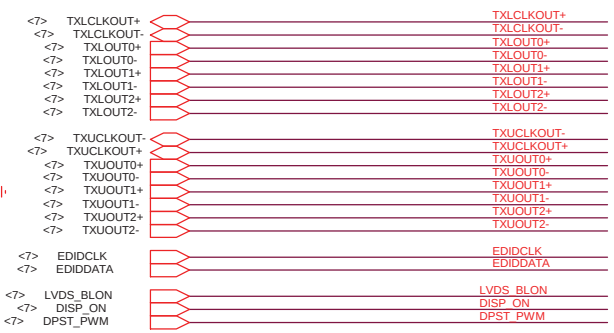
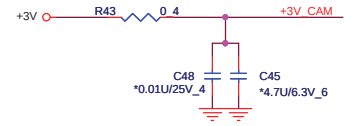
LID Switch



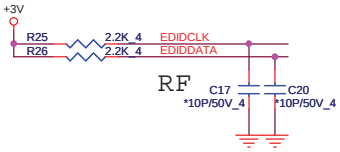


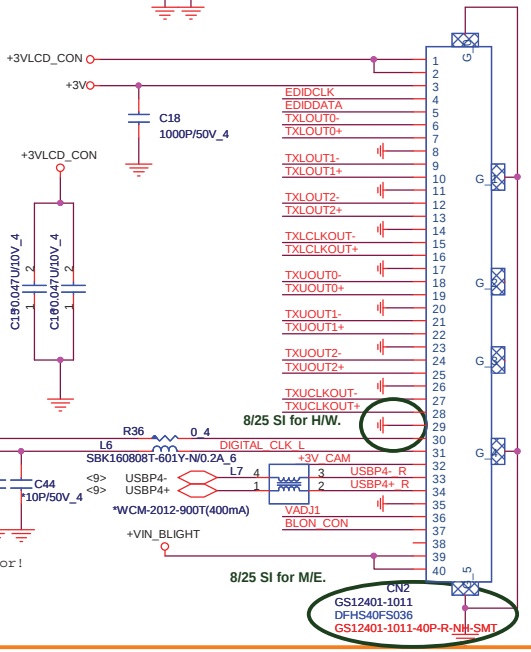




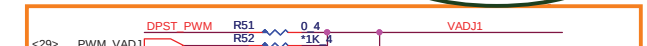
Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

follow L4 location



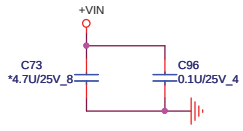


EMI



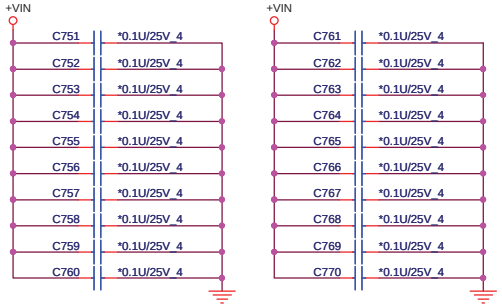
SI modify

EMI & RF



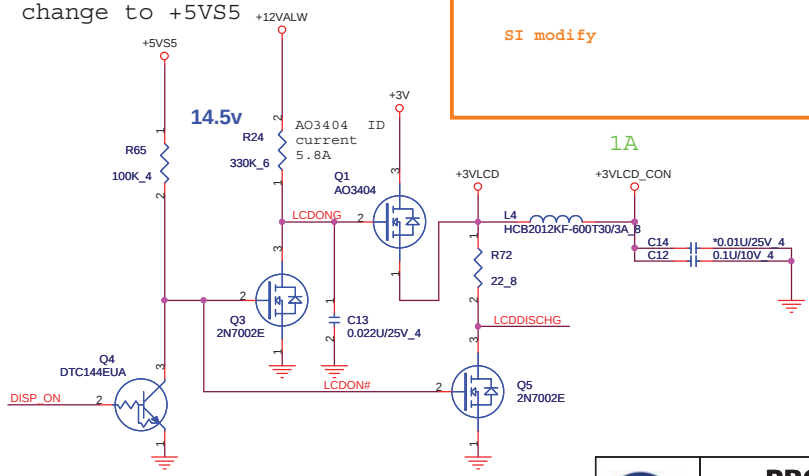
8/25 SI for H/W.

Coupling CAP.



8/25 SI for H/W.

change to +5VS5



<7,28,29,31,37> +3VPCU
<2,3,7,8,9,10,11,12,13,14,17,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<23,34,36,37> +12VALW
<31,32,33,34,35,36,37,38,39> +VIN

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

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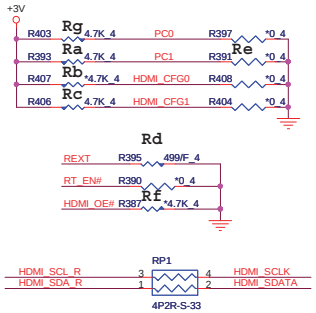
For UMA HDMI function

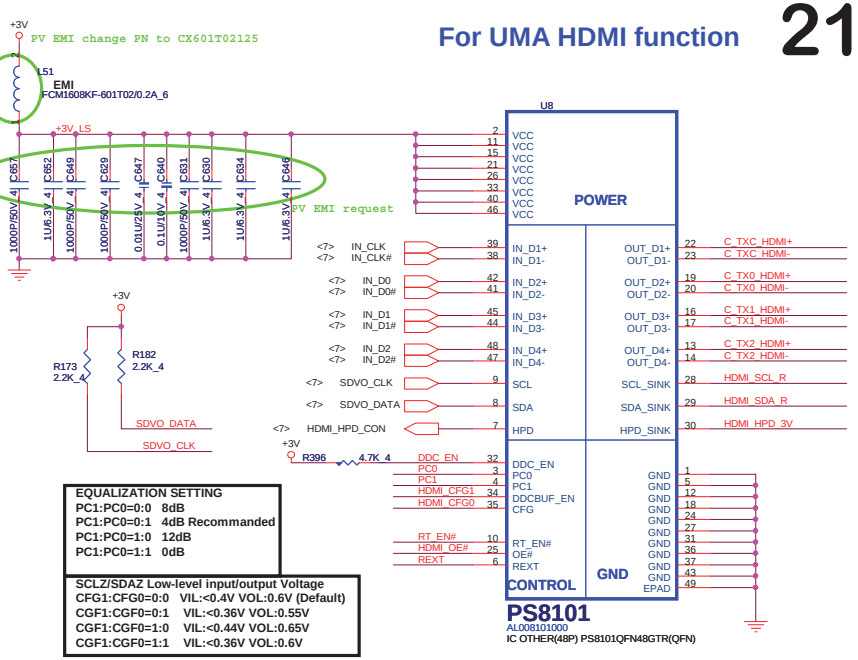
Signals		PDT	PIM	CHR
PC1	Ra	4.7K	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	4.7K	1.2K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	NC	4.7K
PC0	Rg	4.7K	4.7K	4.7K



Vender	Part	Part Number	Part Description
PDT	PS8101	AL008101000	IC OTHER(48P) PS8101QFN48GTR(QFN)
PIM	PI3VDP411LSRZBE	ALP411LS004	IC OTHER(48P) PI3VDP411LSRZBE(TQFN)
CHR	CH7318C	AL007318002	IC OTHER(48P) CH7318C-BF-TR(QFN)

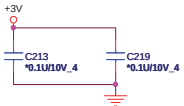
9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

CHR : need Na R1182, add R1027 for capella

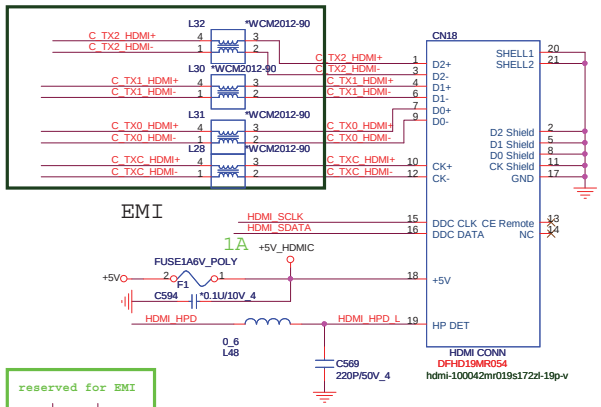


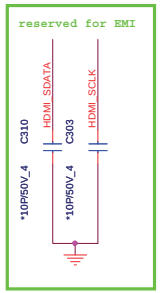
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

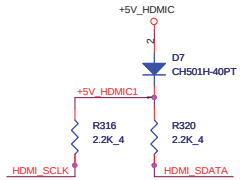
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

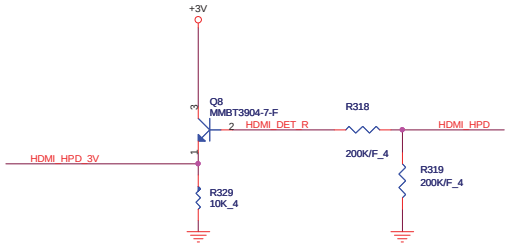


8/25 SI for EMI reserve.









PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A

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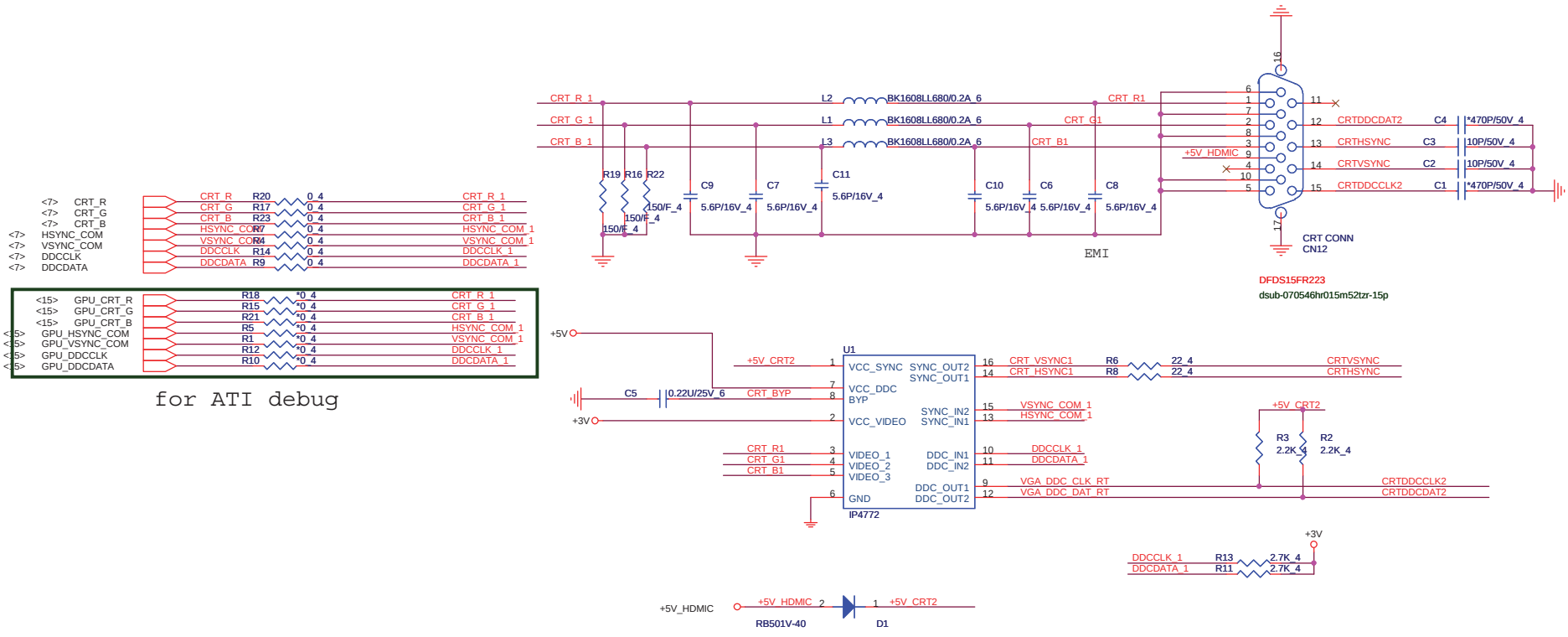
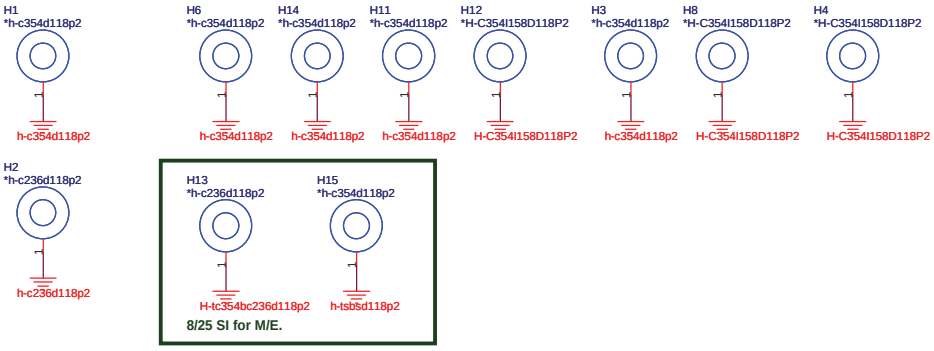
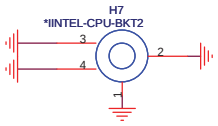
CRT PORT



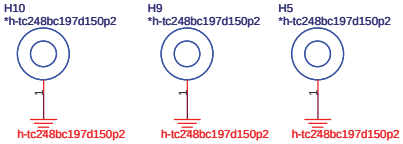
HOLE



CPU



VGA



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	1A

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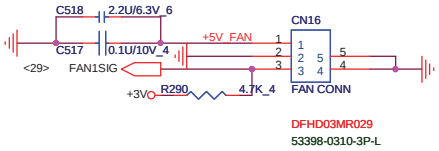
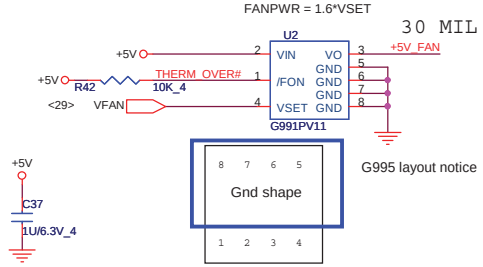
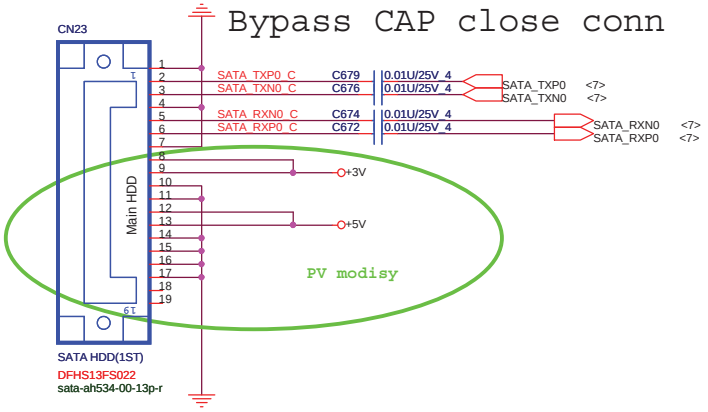
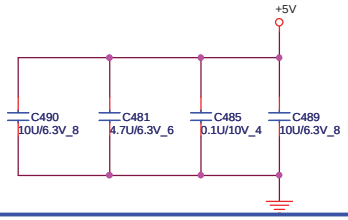
CPU FAN



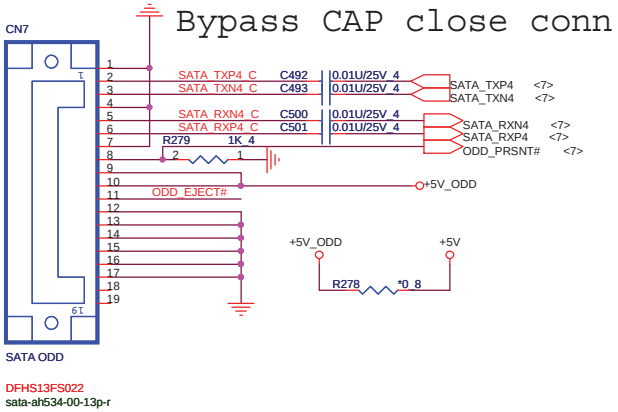


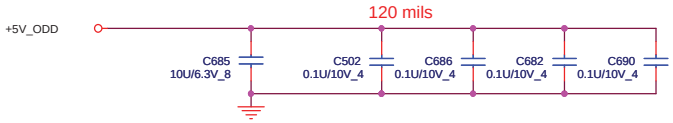
SATA HDD CONNECTOR



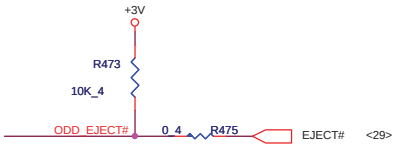


SATA ODD CONNECTOR

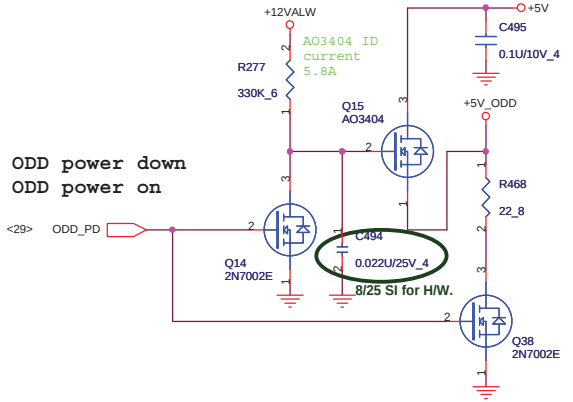




follow INTEL DG change eject PU to +3V.



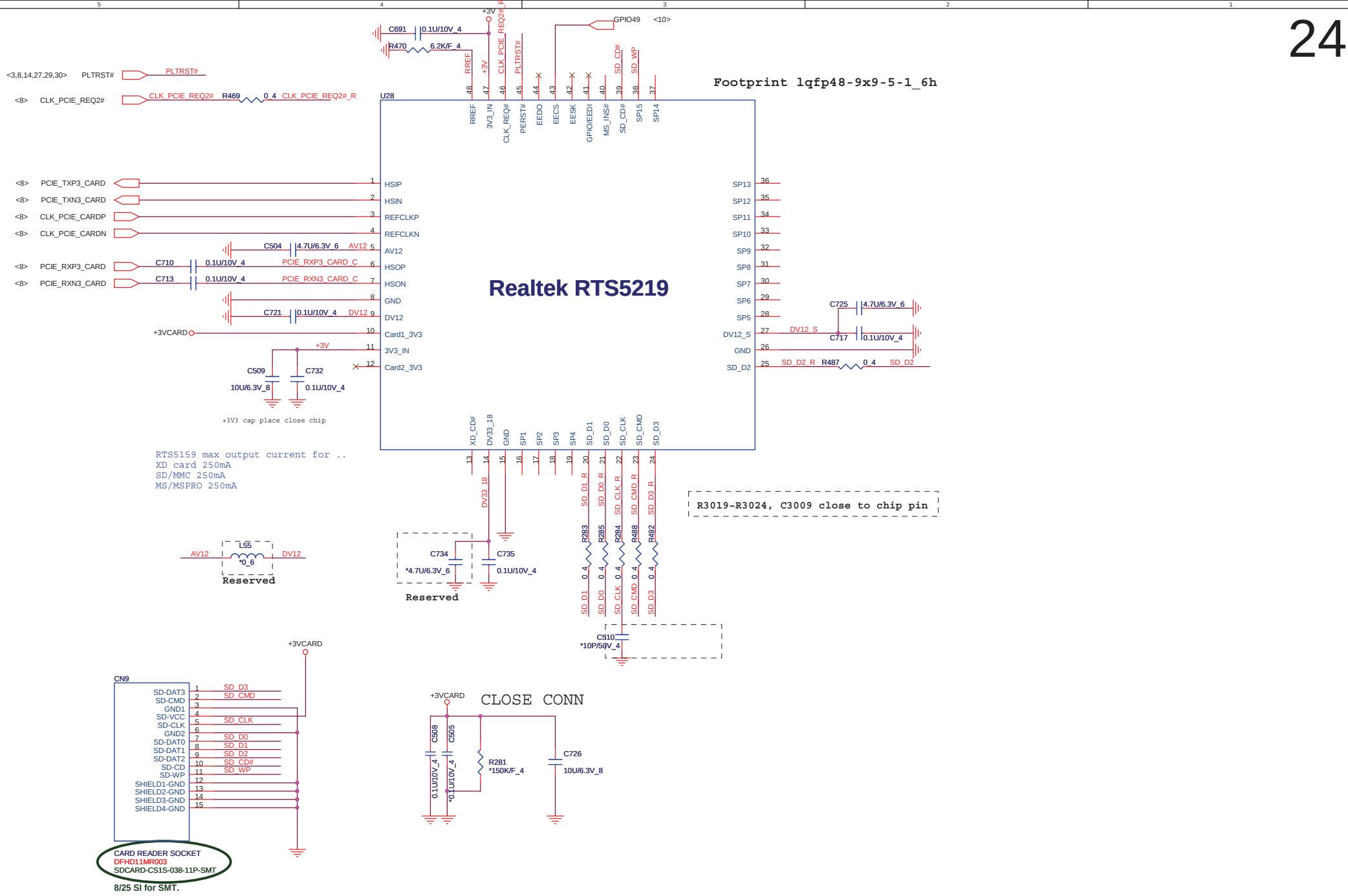
High : ODD power down
Low : ODD power on



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

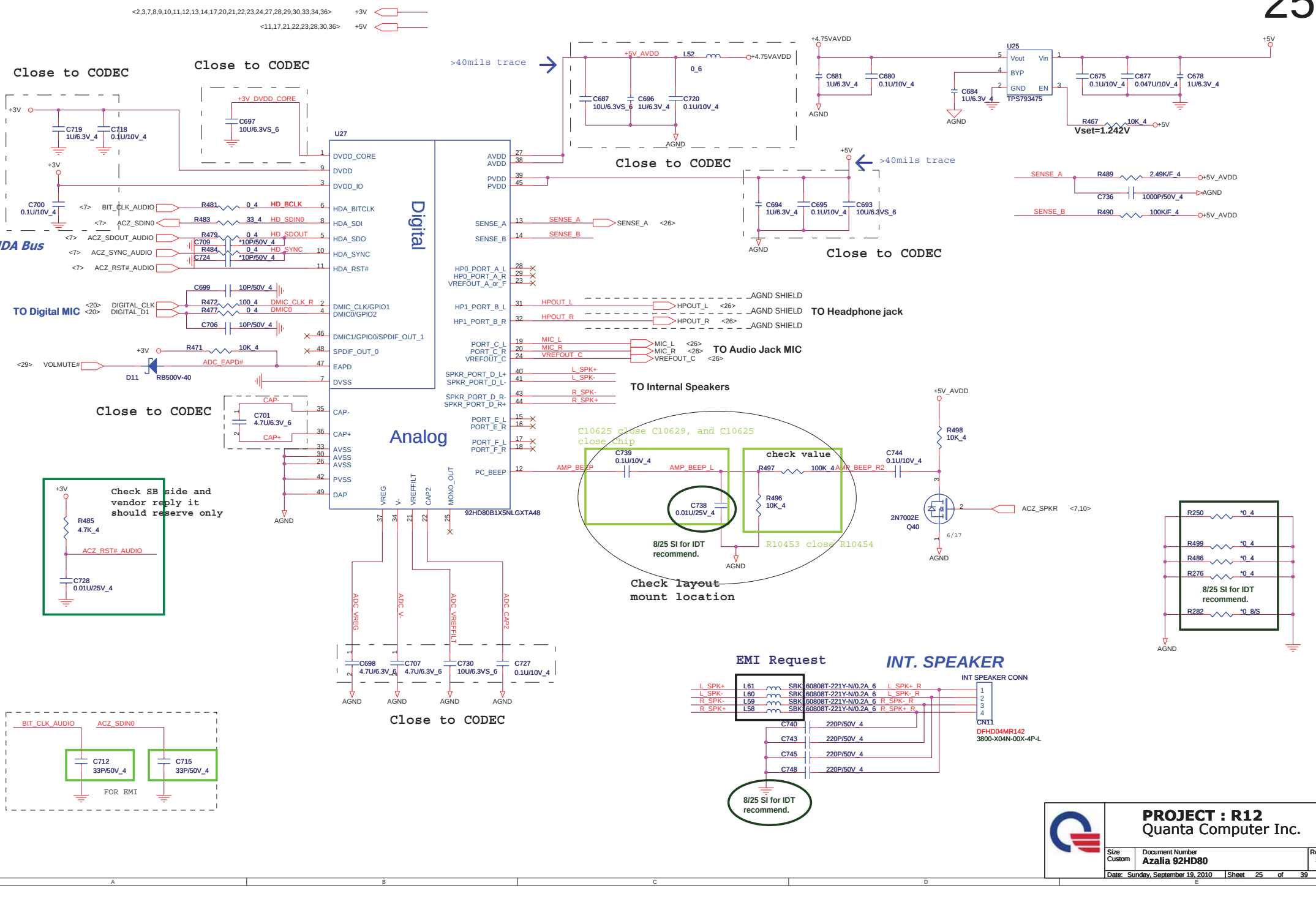
Date: Sunday, September 19, 2010 | Sheet 23 of 39



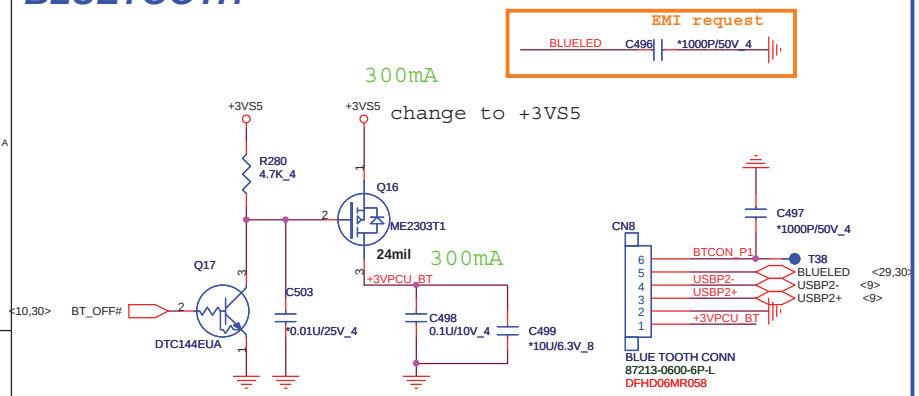
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5219 & CR SOCKET &HOLE	1A

Date: Sunday, September 19, 2010 | Sheet 24 of 39


Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
HDA Bus
TO Digital MIC
TO Headphone jack
TO Audio Jack MIC
TO Internal Speakers
Digital
Analog
U27
92HD80B1X5NLGXTA48
>40mils trace
>40mils trace
U25
TPS793475
Vset=1.242V
C10625 close C10629, and C10625 close chip
check value
R10453 close R10454
8/25 SI for IDT recommend.
Check layout mount location
Check SB side and vendor reply it should reserve only
EMI Request
INT. SPEAKER
INT SPEAKER CONN
DFHD04MR142
3800-X04N-00X-4P-L
FOR EMI
AGND
AGND SHIELD

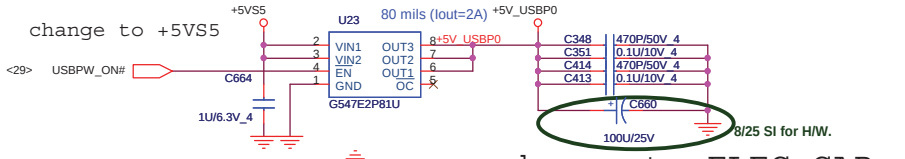
BLUETOOTH



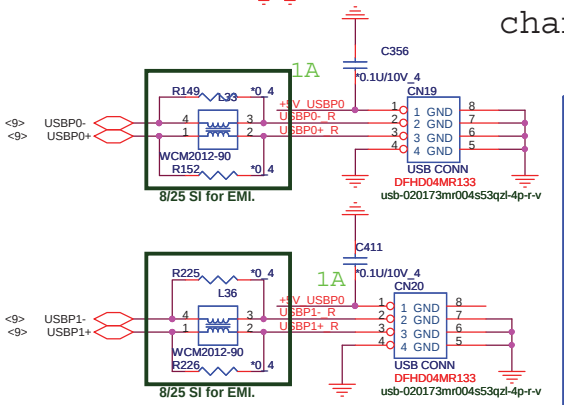
LEFT SIDE USBX2

change to AL000547005

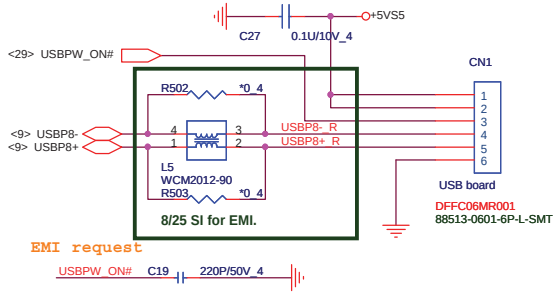
2A 2A



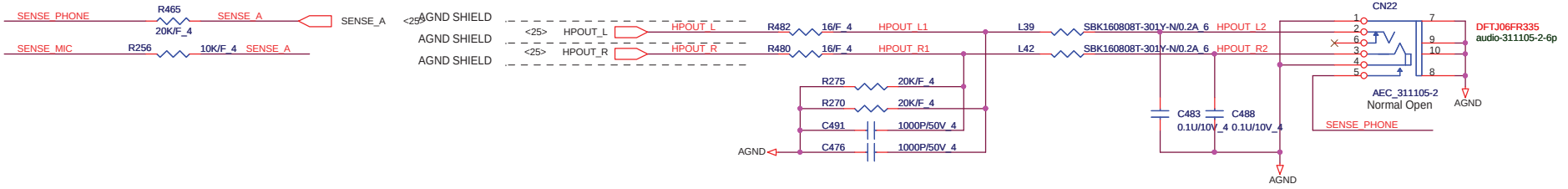
change to ELEC CAP



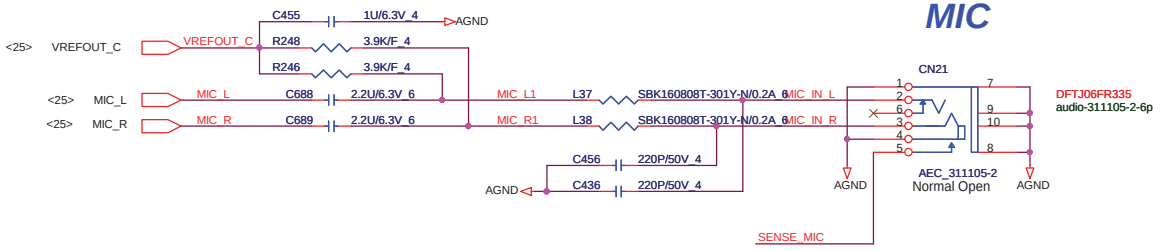
Right SIDE USBX1



Line out



MIC



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Audio JacK	1A

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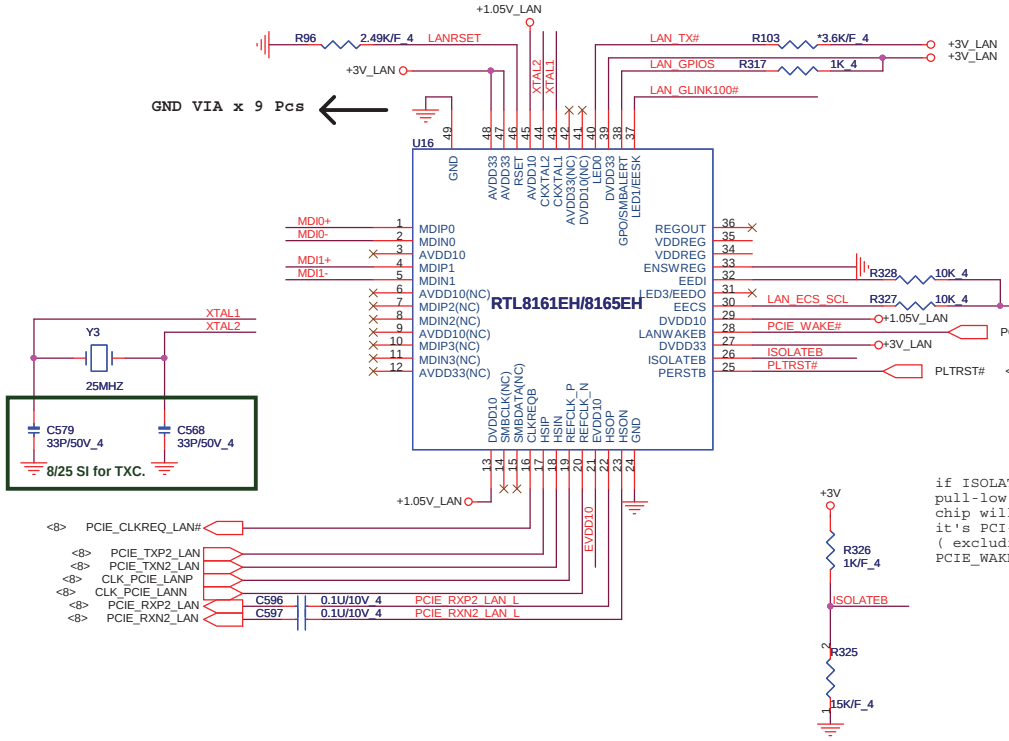
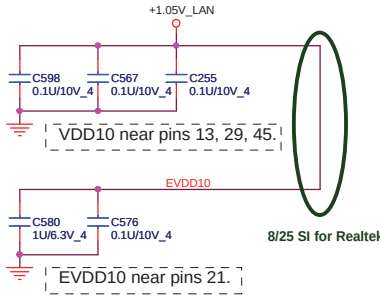


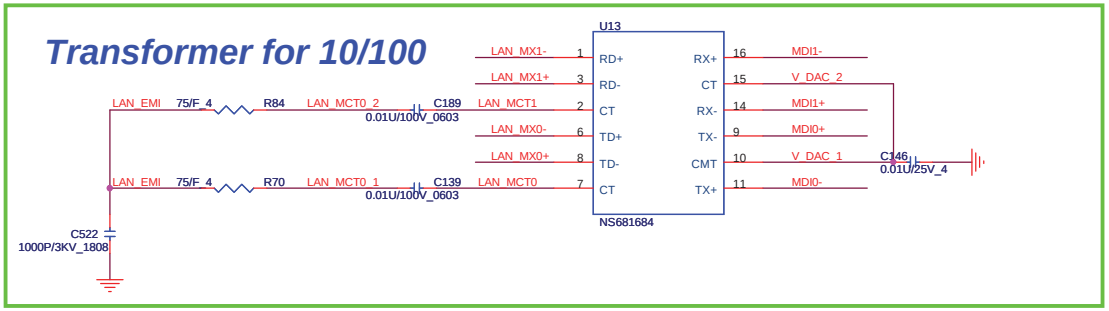
IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

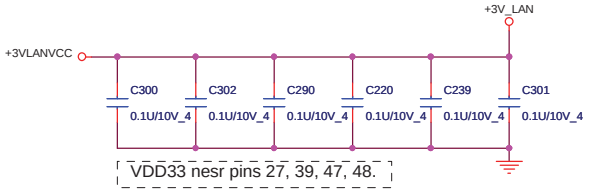
Power trace Layout 寬度> 60mil

>60mil

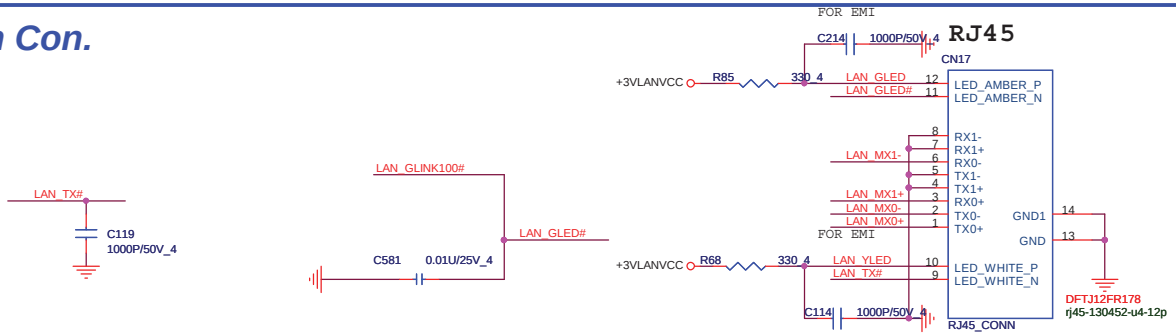


Transformer for 10/100



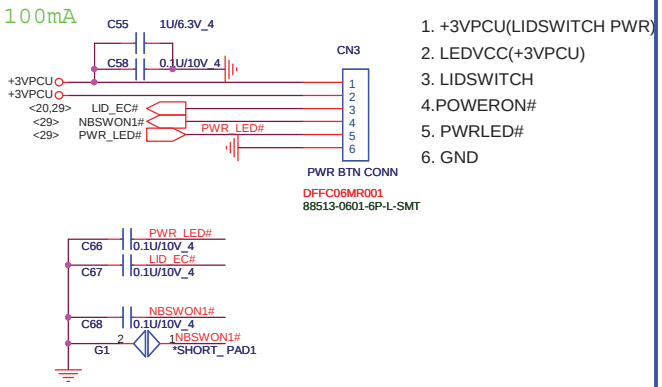


Lan Con.



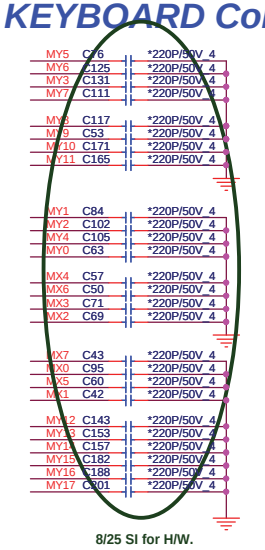
	PROJECT : R12 Quanta Computer Inc.	
Size Custom	Document Number RTL8165EH	Rev 1A
Date: Sunday, September 19, 2010	Sheet 27 of 39	

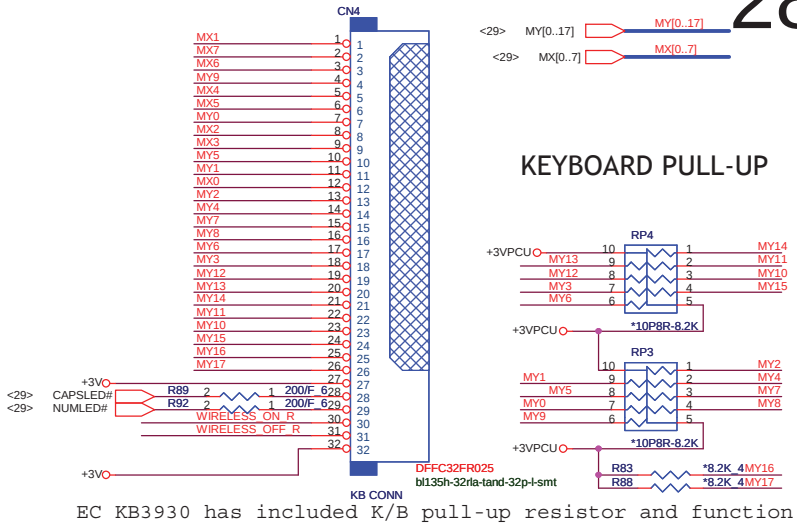
POWER BOTTON CONNECT



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

KEYBOARD Con.

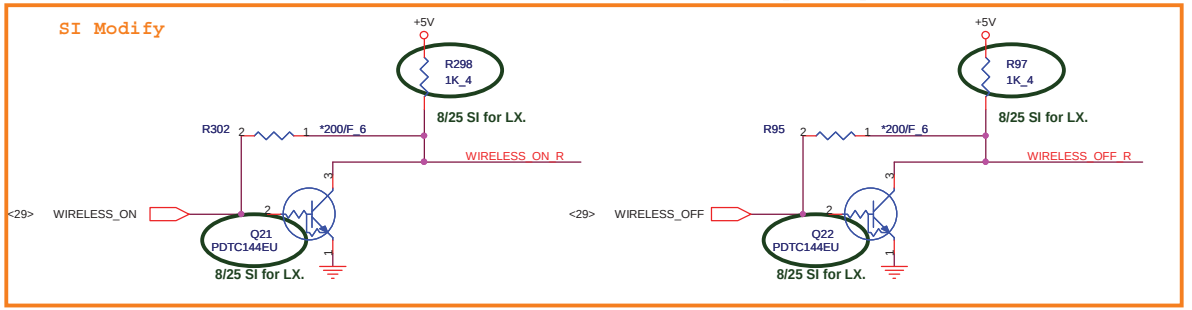




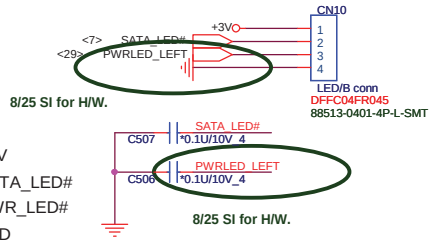
KEYBOARD PULL-UP

EC KB3930 has included K/B pull-up resistor and function

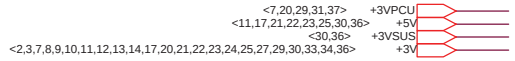
SI Modify



LED Con.

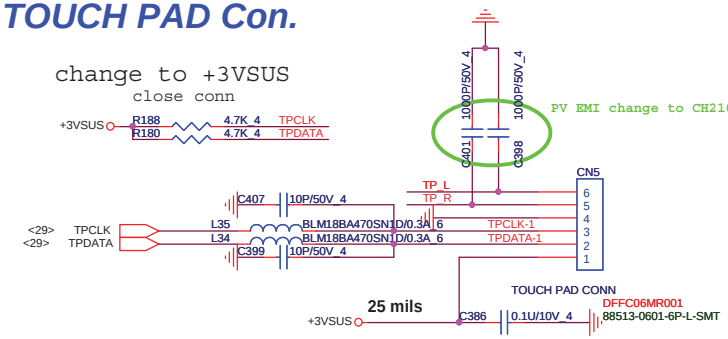


1. +3V
2. SATA_LED#
3. PWR_LED#
4.GND

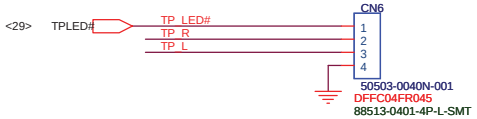


TOUCH PAD Con.

change to +3VSUS
close conn



To TOUCH PAD SW board



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

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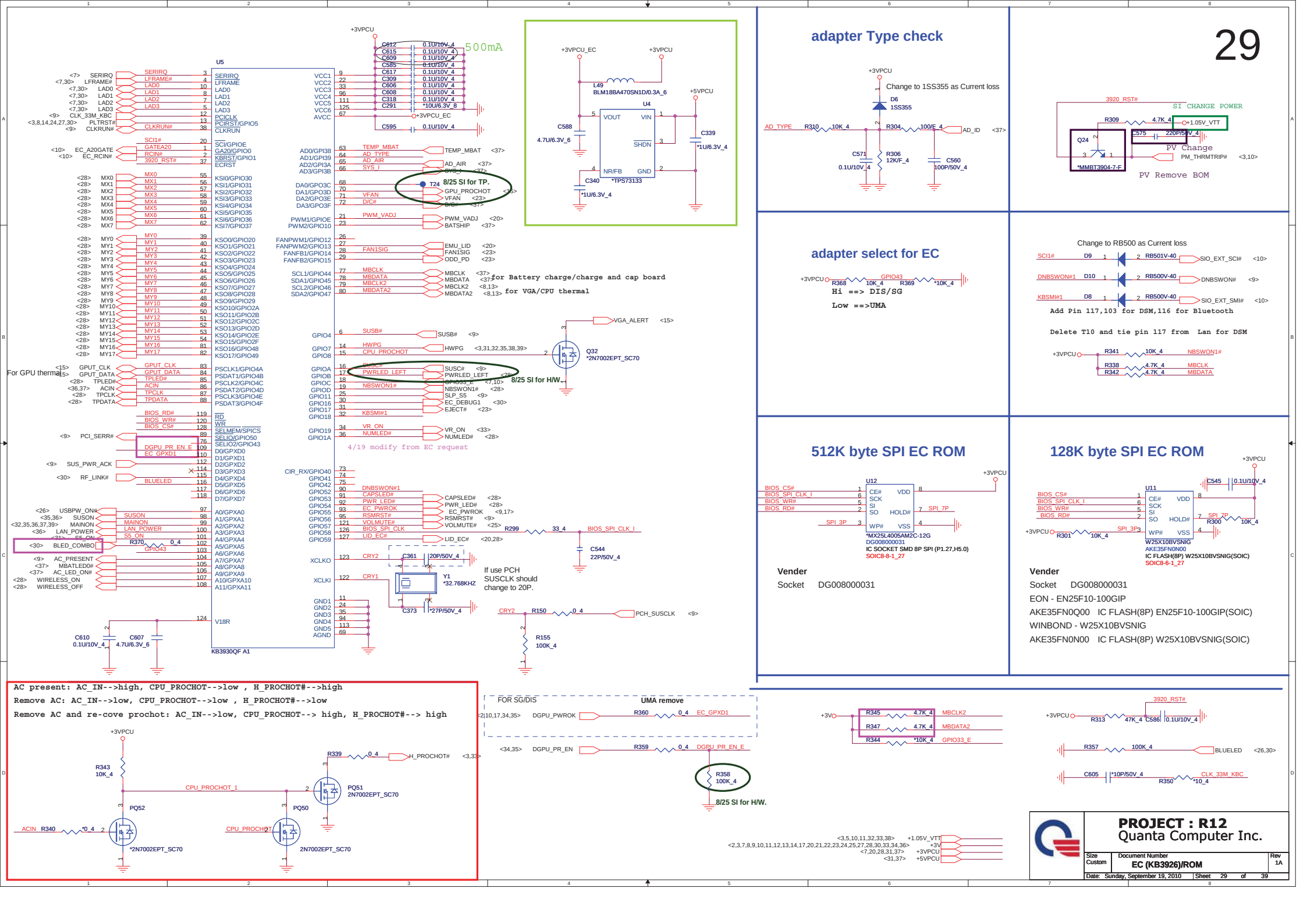
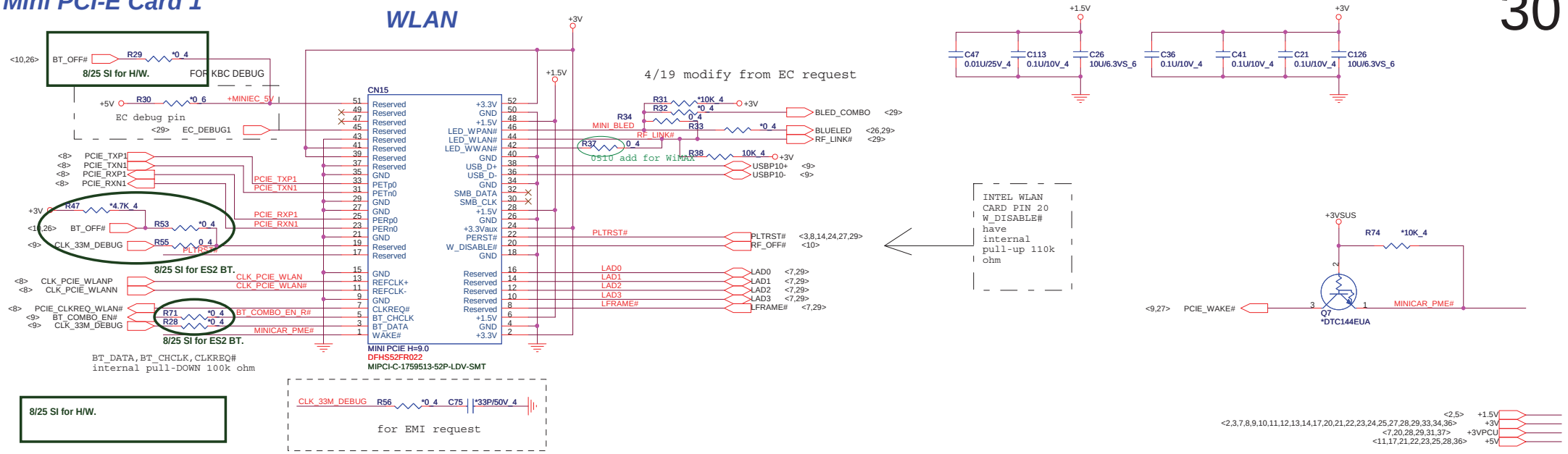
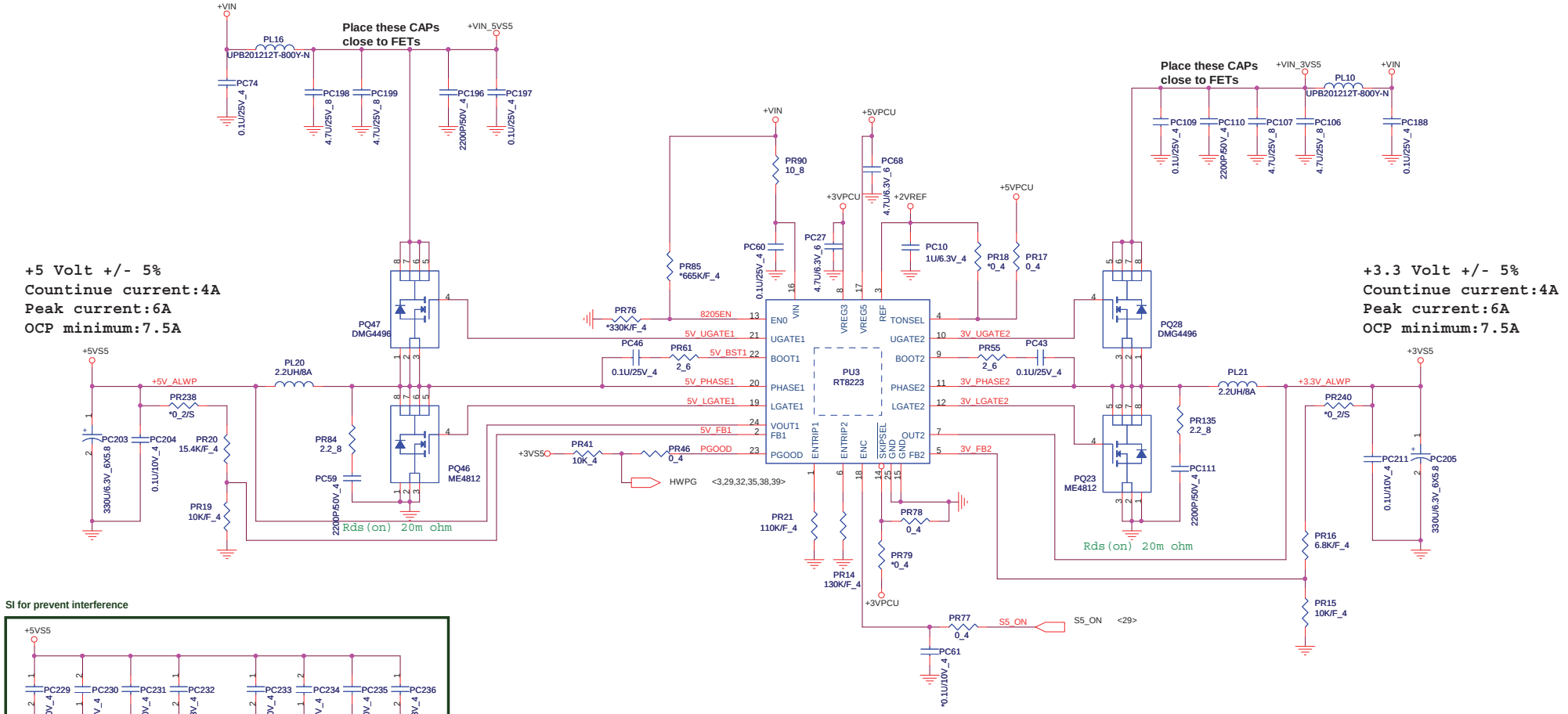
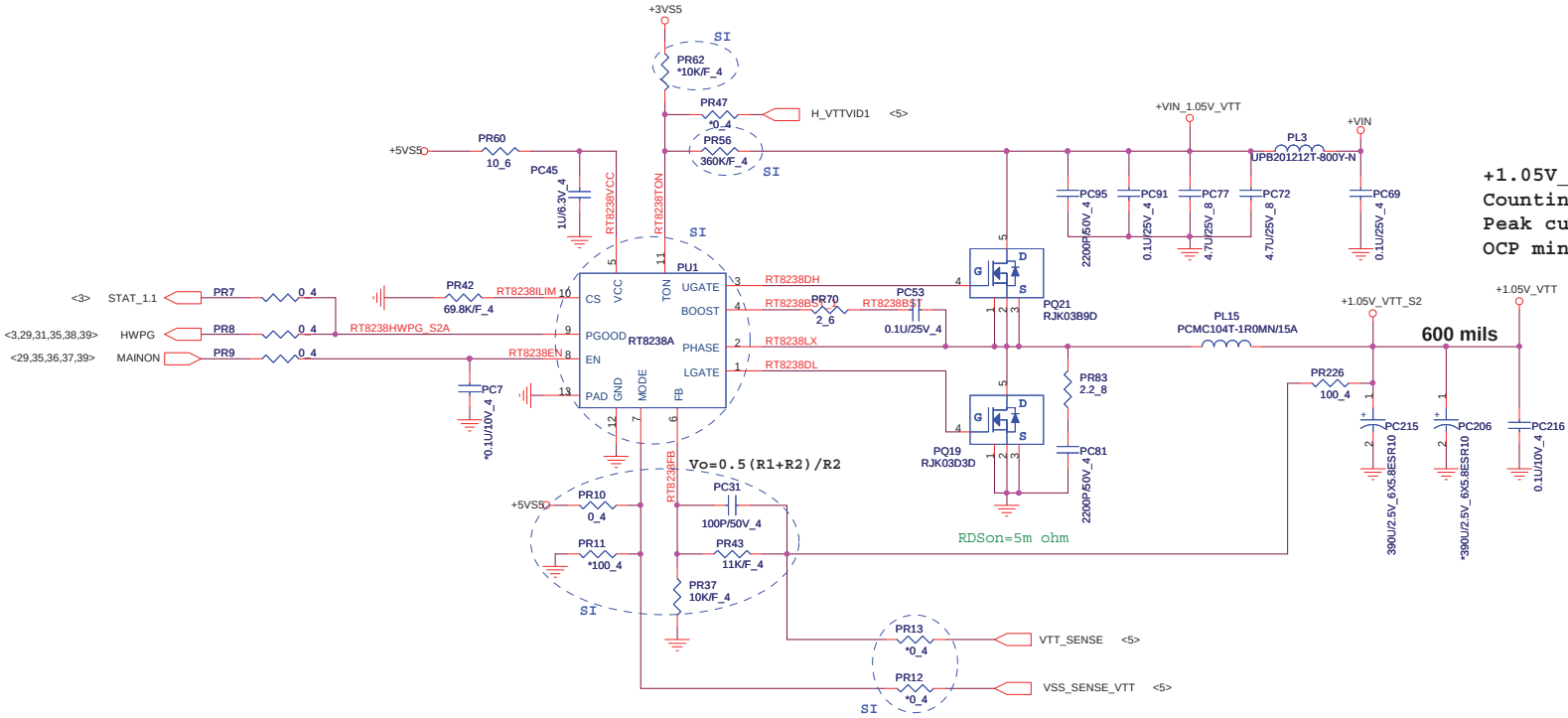

29
adapter Type check
Change to 1SS355 as Current loss
D6
1SS355
AD_TYPE
R310 10K_4
R304 100/F_4
AD_ID <37>
C571 0.1U/10V_4
R306 12K/F_4
C560 100P/50V_4
3920_RST#
SI CHANGE POWER
R309 4.7K_4
+1.05V_VTT
C575 220P/50V_4
Q24
*MMBT3904-7-F
PV Change
PM_THRMTRIP# <3,10>
PV Remove BOM
adapter select for EC
+3VPCU
R368 10K_4
GPIO43
R369 *10K_4
Hi ==> DIS/SG
Low ==>UMA
Change to RB500 as Current loss
SCI1# D9 RB501V-40 SIO_EXT_SCI# <10>
DNBSWON#1 D10 RB500V-40 DNBSWON# <9>
KBSMI#1 D8 RB500V-40 SIO_EXT_SMI# <10>
Add Pin 117,103 for DSM,116 for Bluetooth
Delete T10 and tie pin 117 from Lan for DSM
R341 10K_4 NBSWON1#
R338 4.7K_4 MBCLK
R342 4.7K_4 MBDATA
512K byte SPI EC ROM
U12
BIOS_CS#
BIOS_SPI_CLK_I
BIOS_WR#
BIOS_RD#
SPI_3P
CE# VDD
SCK
SI
SO HOLD#
WP# VSS
SPI_7P
*MX25L4005AM2C-12G
DG008000031
IC SOCKET SMD 8P SPI (P1.27,H5.0)
SOIC8-8-1_27
Vender
Socket DG008000031
128K byte SPI EC ROM
U11
C545 0.1U/10V_4
R300 10K_4
R301 10K_4
W25X10BVSNIG
AKE35FN0N00
IC FLASH(8P) W25X10BVSNIG(SOIC)
SOIC8-6-1_27
Vender
Socket DG008000031
EON - EN25F10-100GIP
AKE35FN0Q00 IC FLASH(8P) EN25F10-100GIP(SOIC)
WINBOND - W25X10BVSNIG
AKE35FN0N00 IC FLASH(8P) W25X10BVSNIG(SOIC)
U5
KB3930QF A1
+3VPCU
500mA
C612 0.1U/10V_4
C615 0.1U/10V_4
C609 0.1U/10V_4
C585 0.1U/10V_4
C617 0.1U/10V_4
C309 0.1U/10V_4
C606 0.1U/10V_4
C608 0.1U/10V_4
C318 0.1U/10V_4
C291 *10U/6.3V_8
C595 0.1U/10V_4
+3VPCU_EC
L49 BLM18BA470SN1D/0.3A_6
+5VPCU
U4
C588 4.7U/6.3V_6
C339 *1U/6.3V_4
C340 *1U/6.3V_4
*TPS73133
VOUT VIN SHDN NR/FB GND
8/25 SI for TP.
T24
For Battery charge/charge and cap board
for VGA/CPU thermal
For GPU thermal
VGA_ALERT <15>
Q32
*2N7002EPT_SC70
8/25 SI for H/W.
4/19 modify from EC request
If use PCH SUSCLK should change to 20P.
Y1 *32.768KHZ
C361 20P/50P_4
C373 *27P/50P_4
R299 33_4
C544 22P/50V_4
R150 0_4
R155 100K_4
PCH_SUSCLK <9>
C610 0.1U/10V_4
C607 4.7U/6.3V_6
AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->low
Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high
R343 10K_4
PQ52
PQ50
PQ51
2N7002EPT_SC70
*2N7002EPT_SC70
ACIN R340 *0_4
CPU_PROCHOT_1
CPU_PROCHOT
R339 0_4
H_PROCHOT# <3,33>
FOR SG/DIS
UMA remove
DGPU_PWROK
R360 0_4 EC_GPXD1
DGPU_PR_EN
R359 0_4 DGPU_PR_EN_E
R358 100K_4
8/25 SI for H/W.
R345 4.7K_4 MBCLK2
R347 4.7K_4 MBDATA2
R344 *10K_4 GPIO33_E
3920_RST#
R313 47K_4 C586 0.1U/10V_4
R357 100K_4 BLUELED <26,30>
C605 *10P/50V_4
R350 *10_4 CLK_33M_KBC
PROJECT : R12
Quanta Computer Inc.
Size Custom
Document Number EC (KB3926)/ROM
Rev 1A
Date: Sunday, September 19, 2010
Sheet 29 of 39

Mini PCI-E Card 1

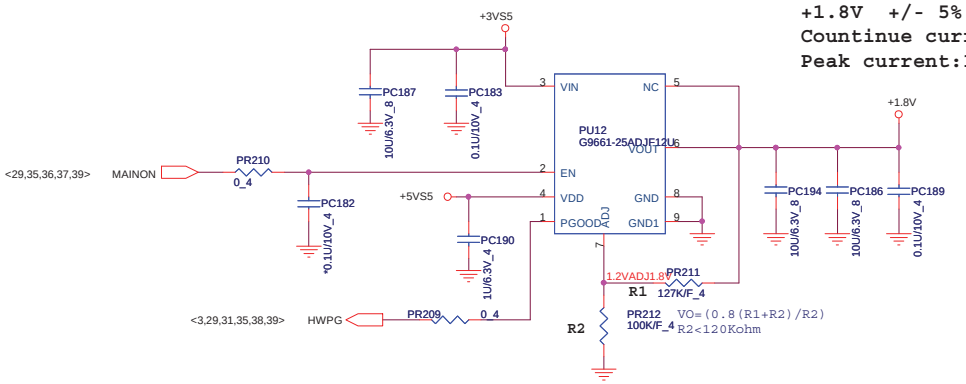
WLAN




+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
Place these CAPs close to FETs
Place these CAPs close to FETs
PU3 RT8223
PQ47 DMG4496
PQ46 ME4812
PQ28 DMG4496
PQ23 ME4812
Rds(on) 20m ohm
Rds(on) 20m ohm
HWPG
S5_ON
SI for prevent interference



+1.05V_VTT Volt +/- 5%
Countinue current:10A
Peak current: 16A
OCP minimum: 18A



+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V VTT / PCH	1A

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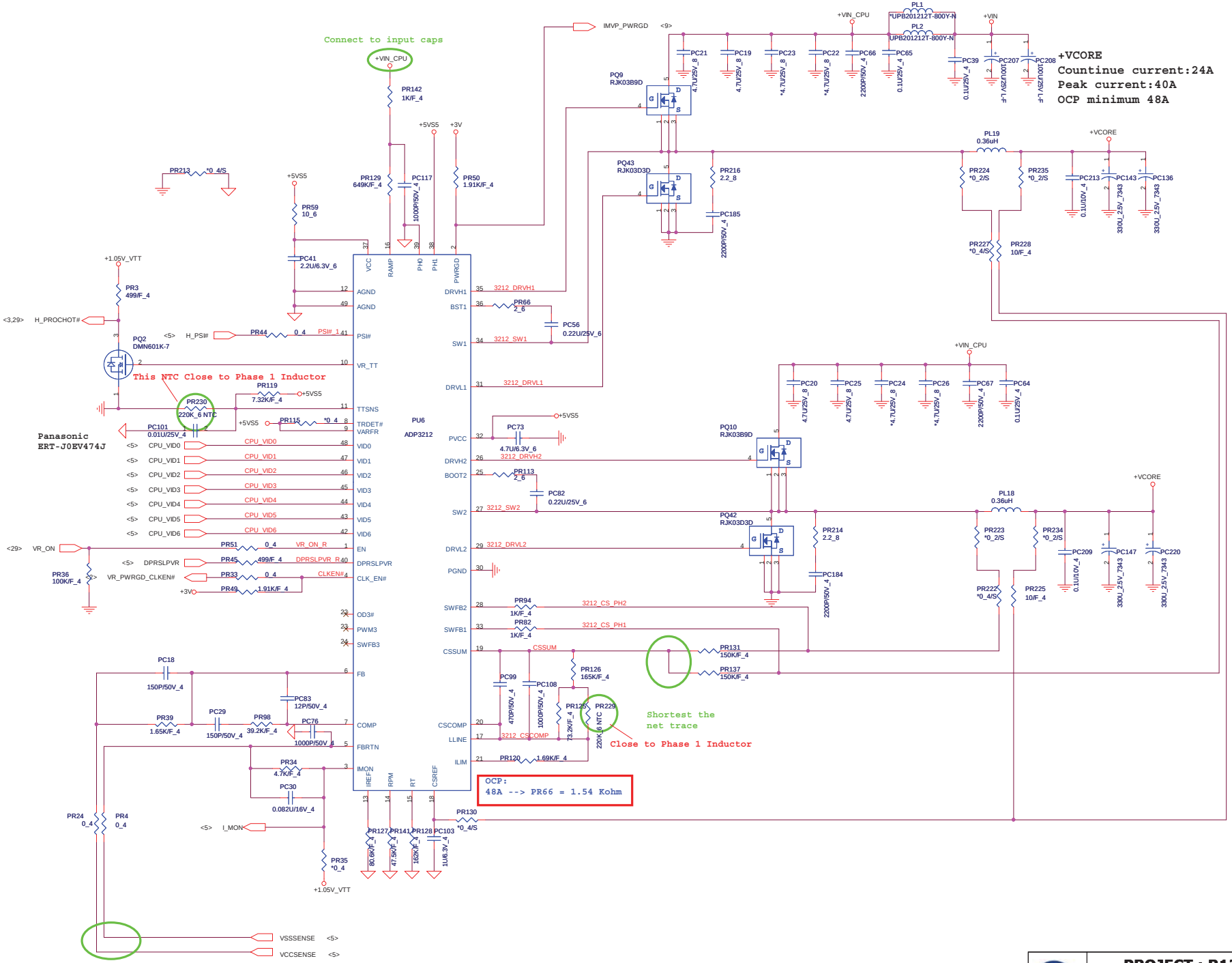
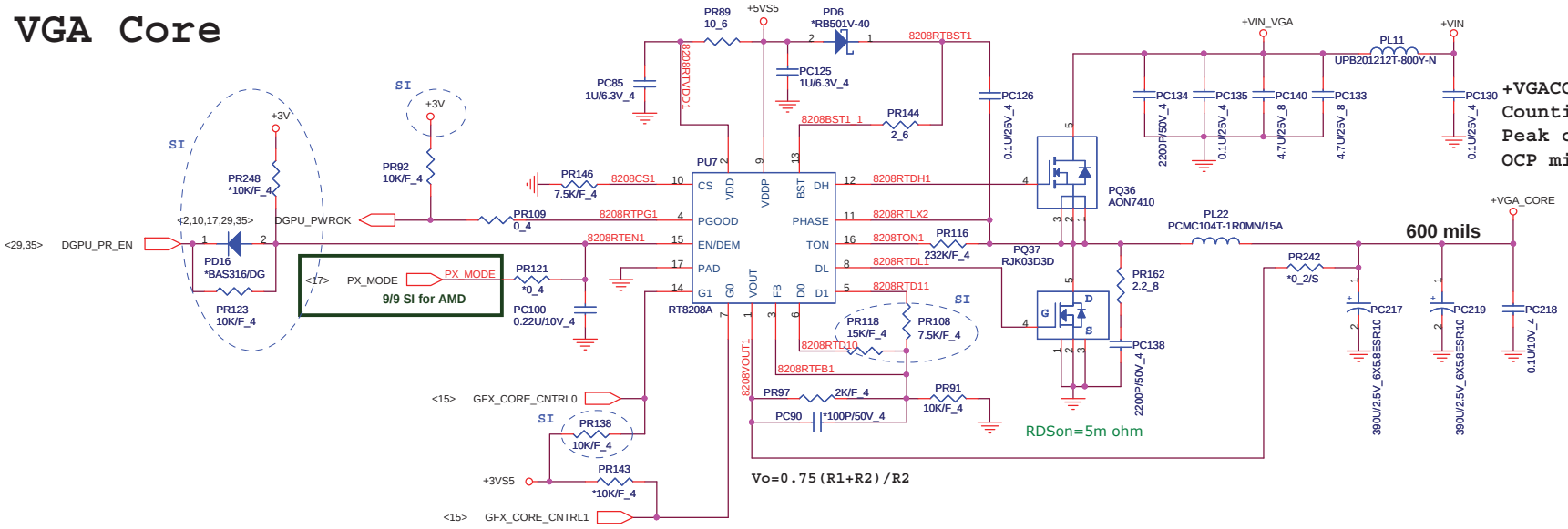
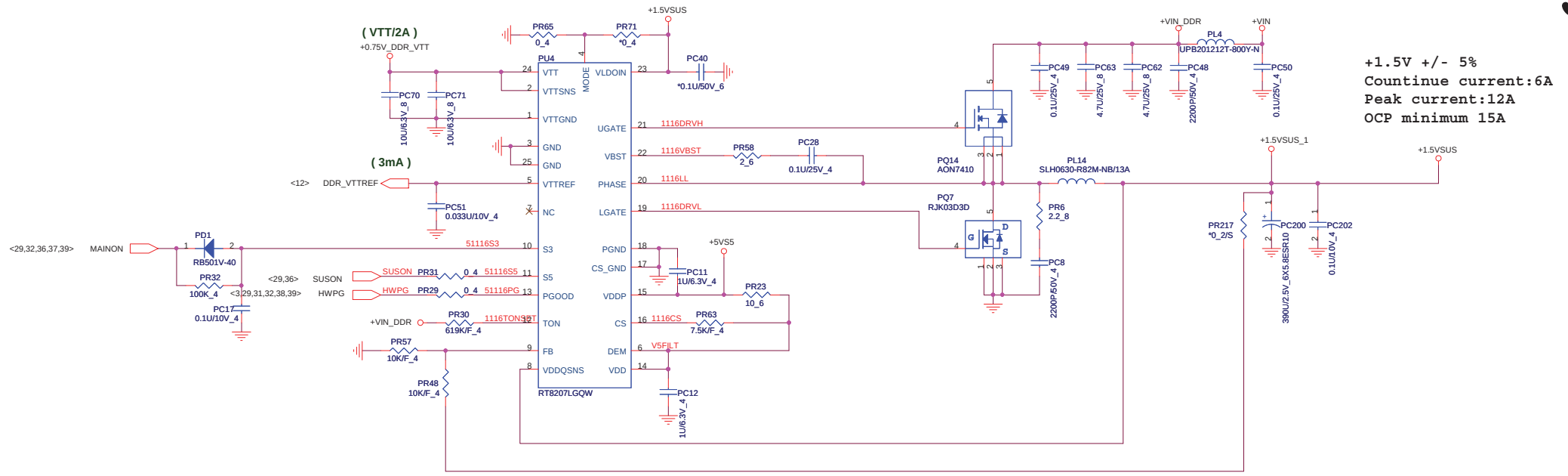


PROJECT : R12	
Quanta Computer Inc.	
Size: Custom	Document Number: CPU Core (ADP3212)
Rev: 1A	
Date: Sunday, September 19, 2010	Sheet 33 of 39

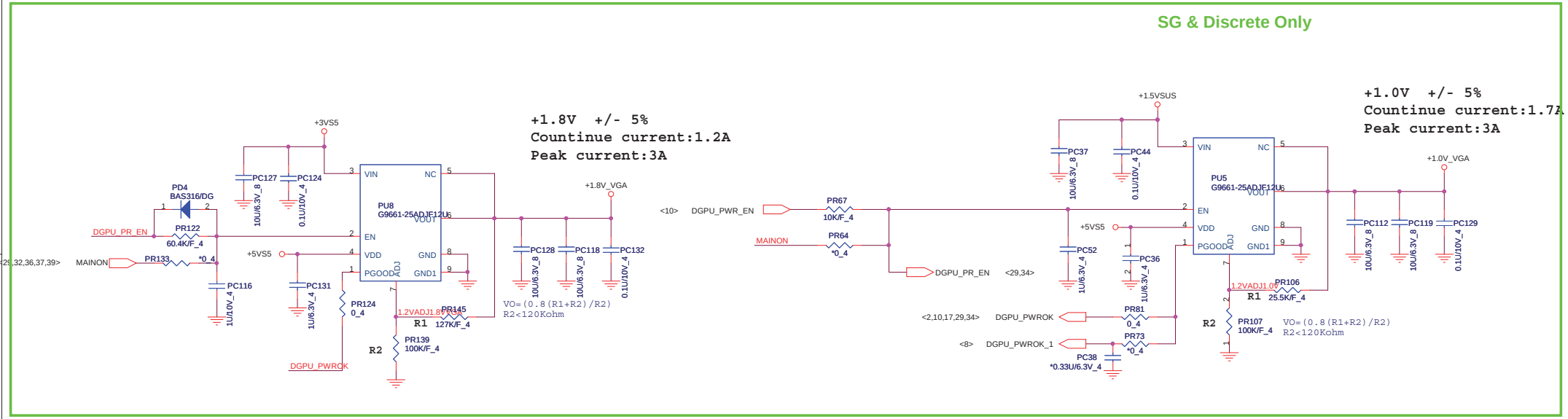
VGA Core



Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA



SG & Discrete Only



Quanta Computer Inc.	PROJECT : R12		
Size: Custom	Document Number: DDR3 (RT8207)		Rev: 1A
Date: Sunday, September 19, 2010	Sheet 35 of 39		

+VA <37>
+5V <11,17,21,22,23,25,28,30>
+VIN <20,31,32,33,34,35,37,38,39>
+1.8V <5,11,32>
+3VS5 <3,7,8,9,10,11,26,31,32,34,35,38>
+5VS5 <11,20,26,31,32,33,34,35,38,39>
+VH28 <37>
+VAD_1 <37>
+3VSUS <28,30>
+12VALW <20,23,34,37>
+BATCHG <37>
+1.5VSUS <3,5,12,13,34,35>
+3VLANVCC <27>
+0.75V_DDR_VTT <12,13,35>

+VH28
+VAD
PR52 22_6
PR86 0_4
PC54 0.1U/25V_4
PC55 0.1U/25V_4
PC58 1U/35V_6
PC57 0.47U/25V_6
ACIN <29,37>
PR74 0_4
+VAD_1
PR72 750K/F_4
PR68 100K/F_4
+12VALW
PC42 1U/16V_4
<29> LAN_POWER
<29,32,35,37,39> MAINON
<29,35> SUSON
MAINON
+3VLANVCC
PR27 0_6
G5934DISC1
G5934DISC3
PR26 0_6
+3VSUS
G5934DISC2
PR28 0_6
+5V
PU2 P2806
ON1 ON2 ON3 ON4 DISC1 VIN CN CP VOUT D_CAP PG VSENSE REG DISC3 DISC2 DRIVER4 DRIVER3 DISC4 DRIVER1 DRIVER2 GND
G5934PG
G5934VSENSE
G5934DISC4
PR25 0_6
+3V
+3VS5
PC33 0.1U/10V_4
PQ13 AON7410
PC35 2200P/50V_4
5.2A
PC89 0.1U/10V_4
PC88 *10U/6.3V_8
MAIND3.3V
MAIND
PC14 2200P/50V_4
PQ41 AON7410
5.1A
PC171 0.1U/10V_4
PC170 0.1U/10V_4
SI:
Delete PC169,EE side already
have 10uF*2(C489,C490)
PC34 0.1U/10V_4
LAN_ON
PQ38 ME3424D
PC15 2200P/50V_4
PC221 0.1U/10V_4
PC222 *10U/6.3V_8
0.7A
+3VLANVCC
PC9 0.1U/10V_4
PQ4 ME3424D
SUSD
PC6 2200P/50V_4
0.04A
PC16 0.1U/10V_4
PC13 *10U/6.3V_8
+VIN
+0.75V_DDR_VTT
PR40 1M_4
PR38 22_8
PQ5 DMN601K-7
PQ6 DMN601K-7
PR22 1M_4
MAIND <5>
MAINON_G <5,12>

SI for prevent interference

+3V
PC245 PC246 PC247 PC248 PC249 PC250 PC251 PC252
PC253 PC254 PC255 PC256 PC257 PC258 PC259 PC260
1000P/50V_4 0.01U/25V_4 0.1U/10V_4 1U/6.3V_4

SI for prevent interference

+1.5VSUS
PC269 PC270 PC271 PC272 PC273 PC274 PC275 PC276
1000P/50V_4 0.01U/25V_4 0.1U/10V_4 1U/6.3V_4

SI for prevent interference

+5V
PC261 PC262 PC263 PC264 PC265 PC266 PC267 PC268
1000P/50V_4 0.01U/25V_4 0.1U/10V_4 1U/6.3V_4

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Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

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DC_JACK
90W

SI:
M/E modify.

Do Not add test pad on BATDIS_G signal

To PWR LED

Place this ZVS close to Diode away +VIN

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

PU9
OZ8681

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (OZ8681)	1A

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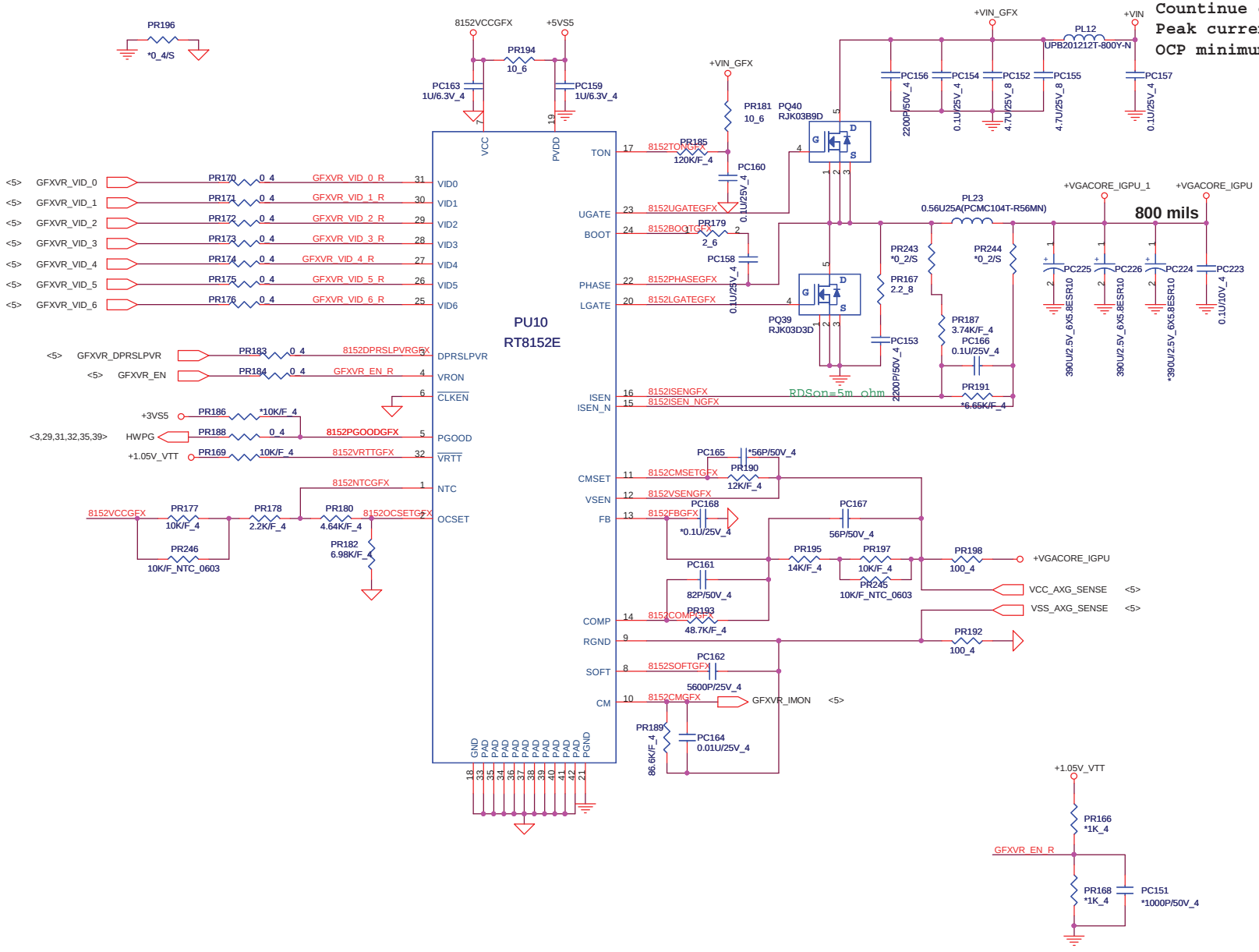
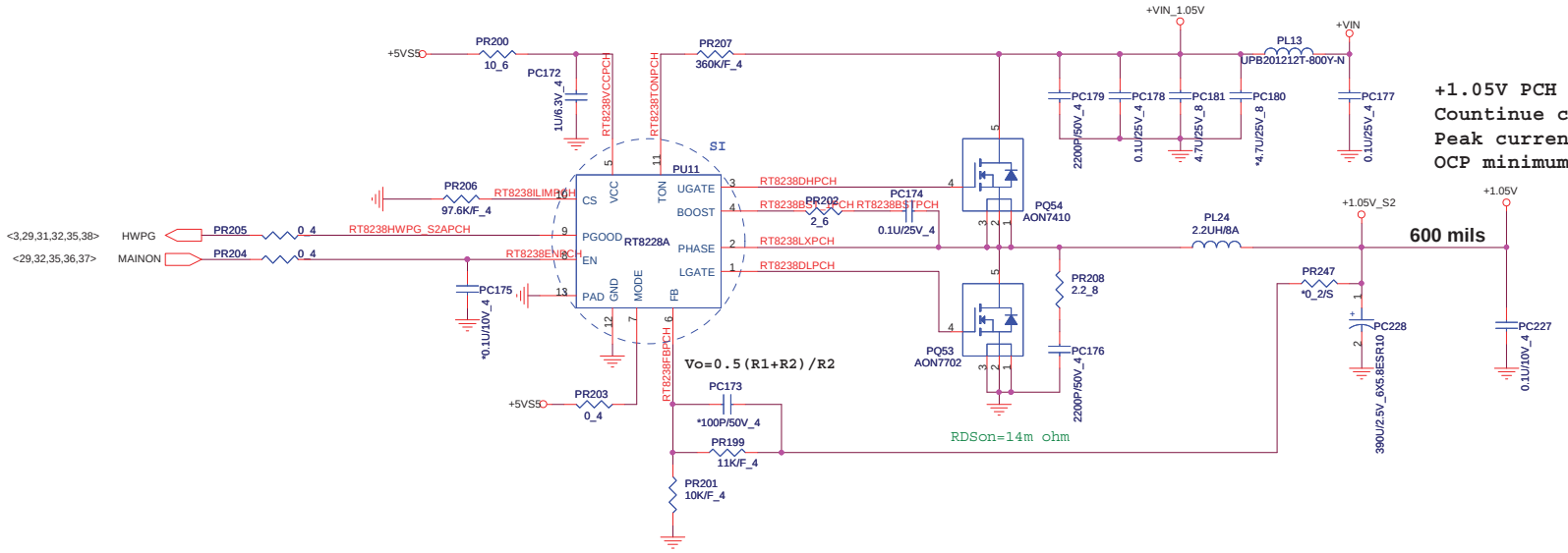
+VGA_UMA +/- 5%
Countinue current:12A
Peak current:18A
OCP minimum 22A





Quanta Computer Inc.	**PROJECT : R12**		
Size: Custom	Document Number: **+1.05V (RT8238A)**		Rev: 1A
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