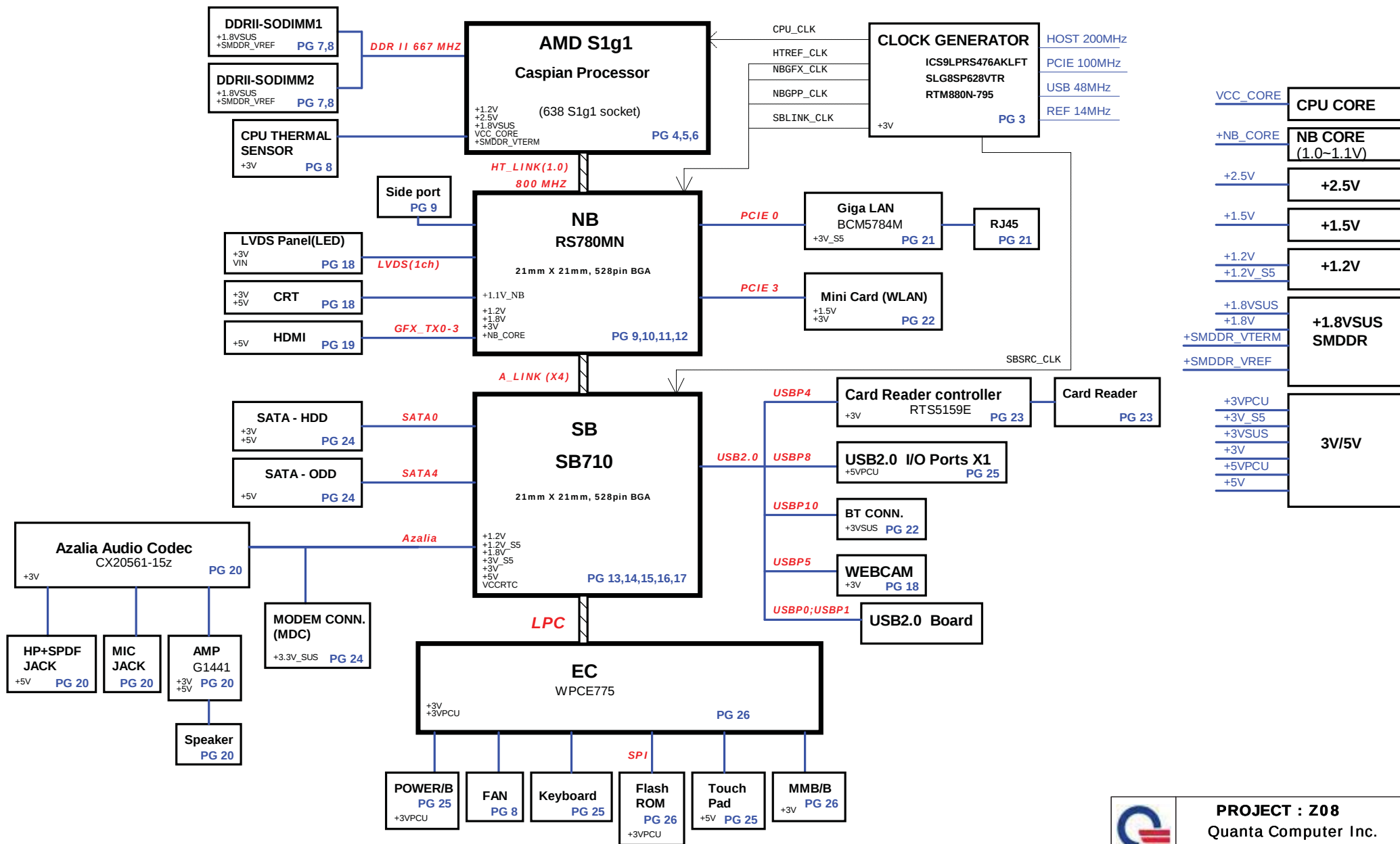


Z08 SYSTEM BLOCK DIAGRAM



01

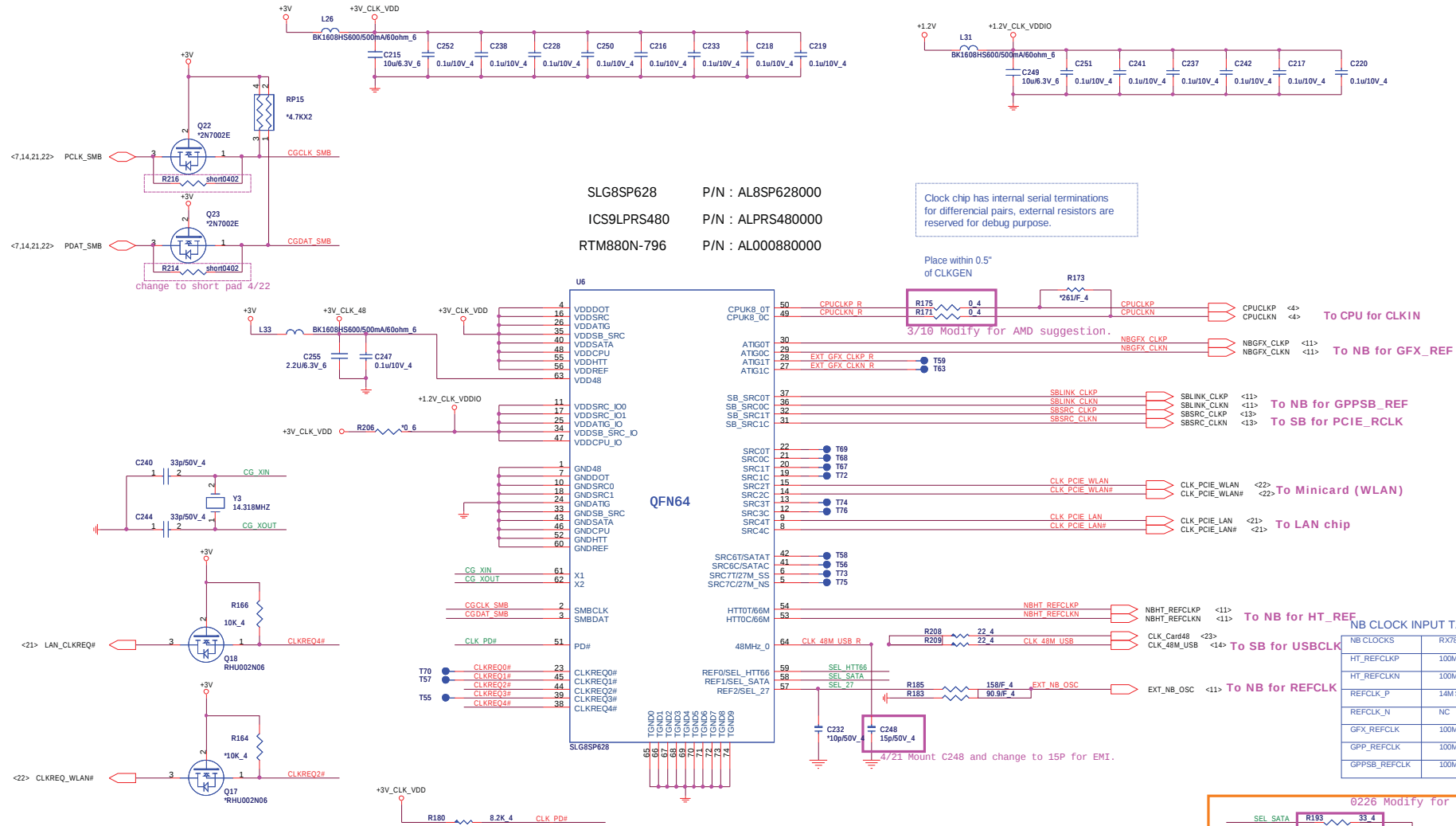


Model	REV	DATE	CHANGE LIST	NOTE
HW	C1A	2009/04/09	1. Page 11: Exchange Pin define for LVDS ON & PWM. 2. Page 21: U20 Footprint change to trf-10-1-24p-nb4. 3. Page 16: L39 Footprint from RC0603 change to RC0805. 4. Page 21: R389, R425 P/N change to CS12204JA44. 5. Page 22: CN23 Footprint change to mipcie-as0b223-s40n-7f-52p-nb4. 6. Page 23: R460 change to 33 ohm; C586 change to 10P for EMI. 7. Page 26: Add Q37, Q38, R484, R485 for MMB leakage. And 3RD_MBCLK & 3RD_MBDATA pull high from +3V to +3VPCU.	
		2009/04/16	8. Page 26: Add CP8, CP9 for EMI. 9. Page 24: Remove R284; mount C347 for EMI. 10. Page 20: Remove R312; mount C365 for EMI. 11. Page 3: Mount C248 and change to 15P for EMI. 12. Page 23: Remove R295; Mount C358 and change to 15P for EMI. 13. Page 12: Add C597, C598 30P (+NB_CORE) for EMI. Add C599, C600 30P (+1.2V_VDDHTTX) for EMI. Add C601, C602 30P (+1.2V) for EMI.	
		2009/04/22	14. R120, R112, R388, R116, R387 change to short pad_0402. 15. Page 19: Del Q20, Q21, R196, R204; add R486, R487 for AMD suggestion. 16. Page 18: CN2 footprint from msc-rb30-5-fg-30p-1 to msc-rb30-5-fg-30p-1-nb4. 17. R8, R10, R214, R216, R437, R200, R28, R4, R419, R266, R265, R275, R287, R293, R314, R319, R325, R332, R334, R258, R283, R146, R148, R198 change to short pad_0402. 18. R106, R79, R117, R118, R480, R267, R482, L1 change to short pad_0603. 19. R105, R438, R223, R249, R29, R181, L21 change to short pad_0805.	
		2009/04/23	20. Page 19: Modify HDMI detect circuit_Del R174, R447, R441, Q35, Q36, R442; add R312, R488, D31. 21. Page 18: U2 pin7 modify voltage from +5V to +3V. 22. Page 26: Swap NET CP8, CP9.	
		2009/04/27	23. Page 20: Mount U14, C435, C418; unmount L47 for Audio noise issue.	
		2009/04/28	24. Page 26: Modify Y1 Footprint.	
		2009/04/10	1. Page 27: Mount PR141 (10K ohm) for Charger Issue. 2. Page 32: Change Z08A PU5 part number from AL009338014 to AL009334000. 3. Page 32: Change PC77 from 10u/4V_8 to 10u/10V_8. 4. PL5, PL8, PL10, PL11 Footprint change to choke-etqp4lr36wfc-nb4.	
		2009/04/17	5. page 27: 1. add PC163 2. PR110, PR139, PR149 change to short pad 3. PR141 un-mount 6. page 28: 1. PR87, PR90, PR106, PR190, PR91 change to short pad. 2. JP2, JP3 remove 3. PR92 un-mount 4. PR101 mount 7. page 29: 1. JP4, JP5 remove 2. PR44, PR43, PR18, PR19, PR128, PR131, PR117, PR5 change to short pad. 3. add PC164, PC165 4. add PR197, PR196 8. page 30: 1. Remove JP8, JP9 9. page 31: 1. Remove JP1, JP6, JP7 2. PR35, PR41, PR155, PR148 change to short pad. 3. +1.8VSUS_SRC net name change to +1.8VSUS 4. VIN_1.8 net name change to VIN. 5. +1.8V_out net name change to +1.8VSUS	
		2009/04/22	10. PL3, PL7 Footprint change to choke-spm10040t-r45m200-4p.	
		2009/04/23	11. page 28: Del NET RT8206_VIN. 12. page 29: Add PC166 27uF/25V to VIN.	
		2009/04/27	13. page 28: Modify component from A04496 to A06402A..	
Power				



PROJECT : Z08
Quanta Computer Inc.

Size	Document Number	Rev
	Change List	1A
Date:	Tuesday, April 28, 2009	Sheet 2 of 36



NB CLOCK INPUT TABLE

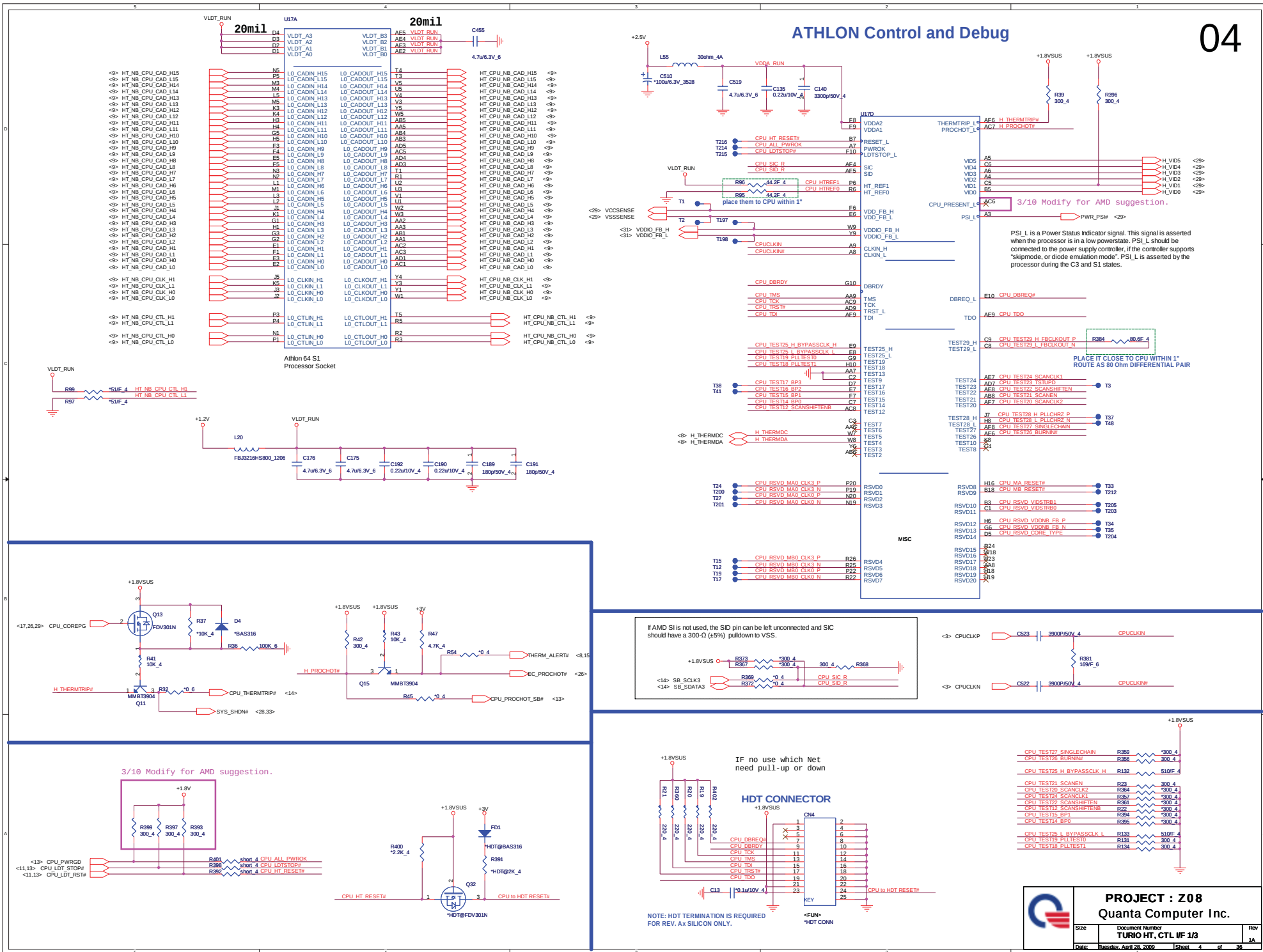
NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLKP	100M DIFF	100M DIFF (VOUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

CLOCKS name	RX780	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP1001 STUFF	RP1001 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPX_CLKP NBGPX_CLKN	RP1005 STUFF	RP1005 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock, RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP1003 STUFF	RP1003 STUFF	to NB for AC-LINK reference clock

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

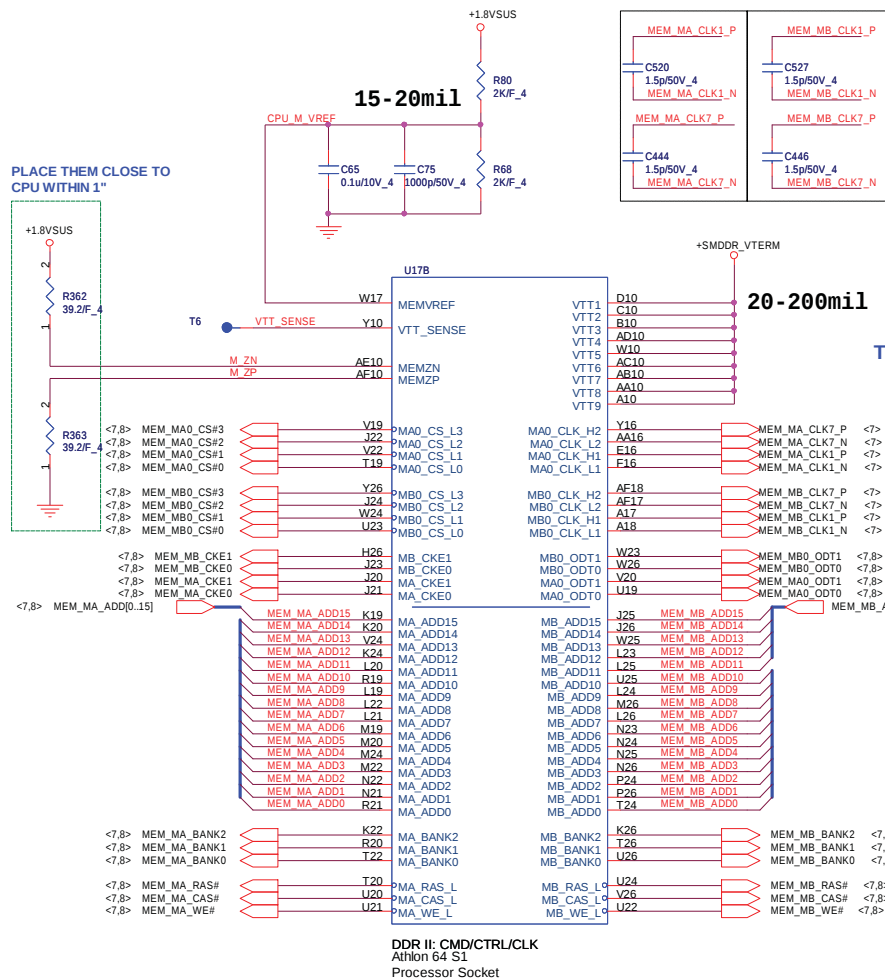
* default

PROJECT : Z08 Quanta Computer Inc.		
Size	Document Number	Rev
	CLOCK GENERATOR_SLG8SP628	1A
Date:	Tuesday, April 28, 2009	Sheet 3 of 36



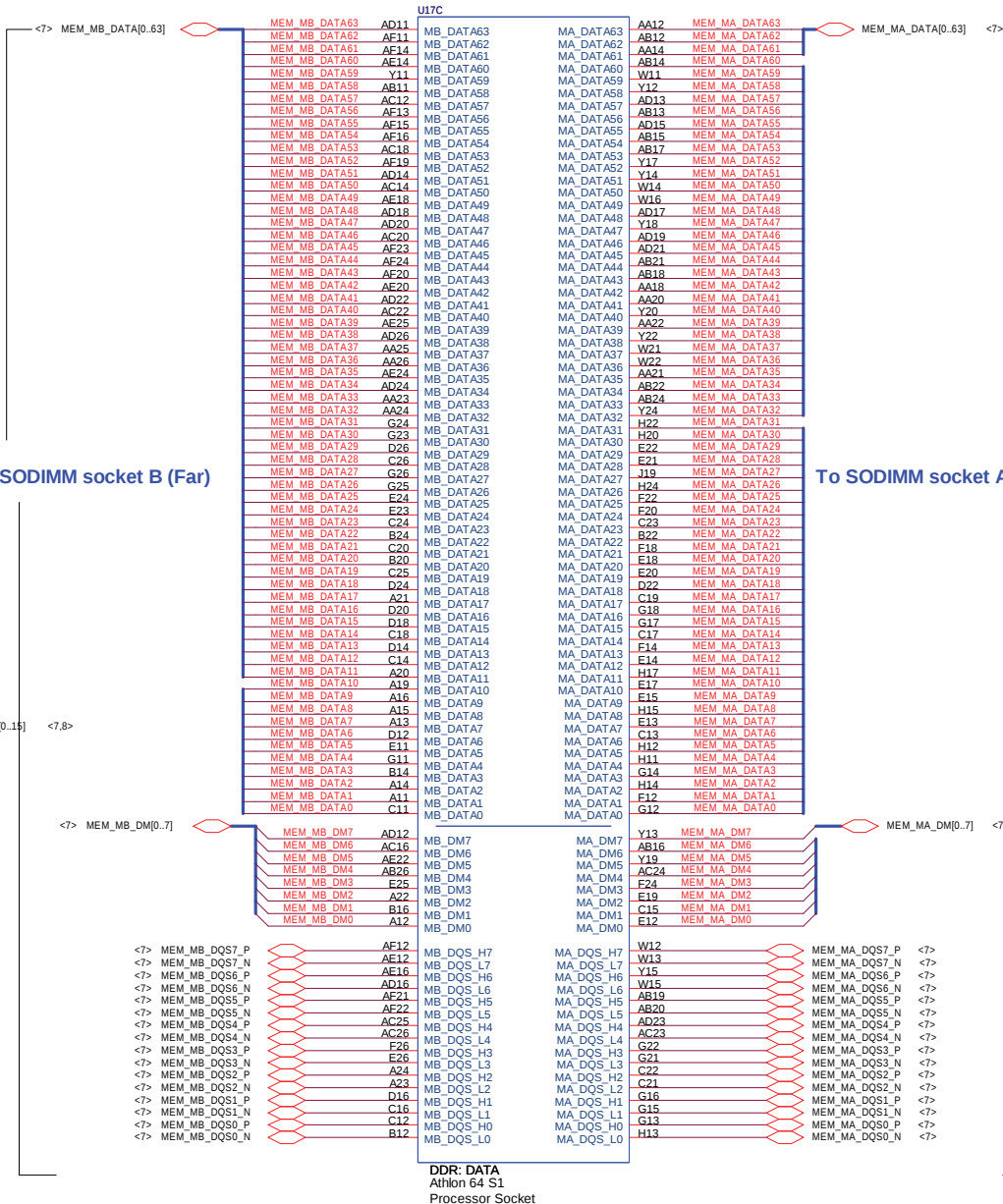
Processor DDR2 Memory Interface

05



To SODIMM socket B (Far)

To SODIMM socket A (near)

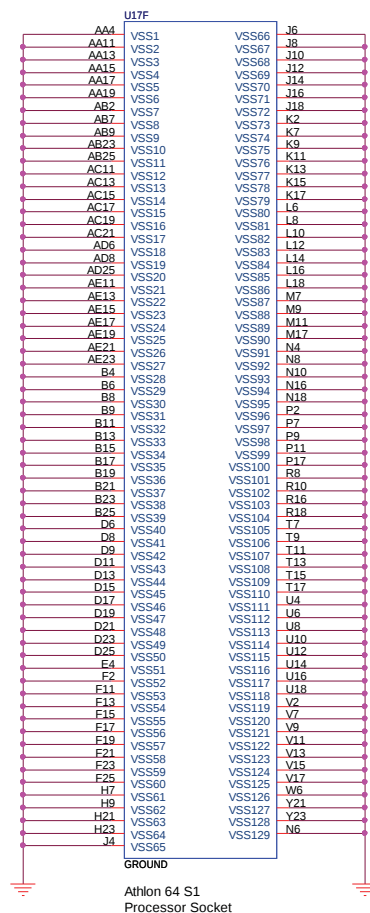
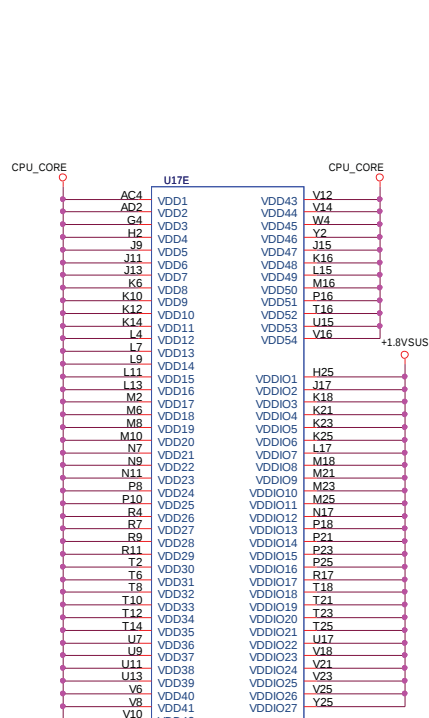


PROJECT : Z08
Quanta Computer Inc.

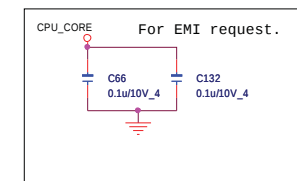
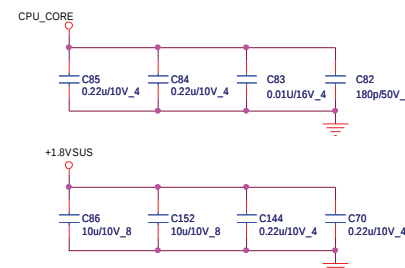
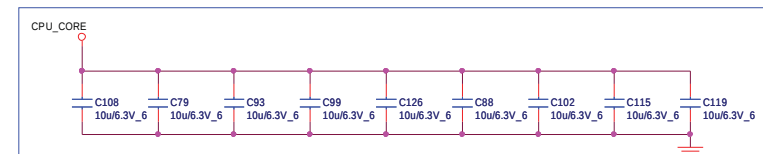
Size	Document Number	Rev
	TURION 64 DDR2 I/F	1A
Date:	Tuesday, April 28, 2009	Sheet 5 of 36

PROCESSOR POWER AND GROUND

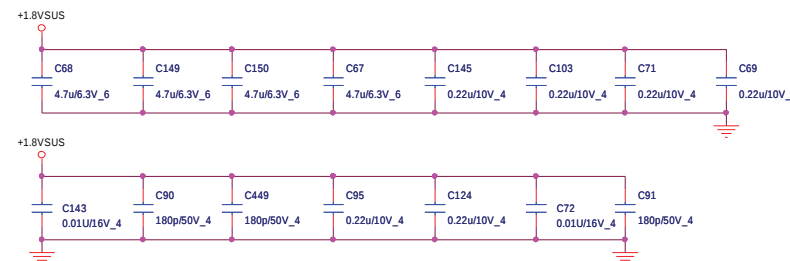
06



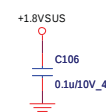
BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



For EMI request.



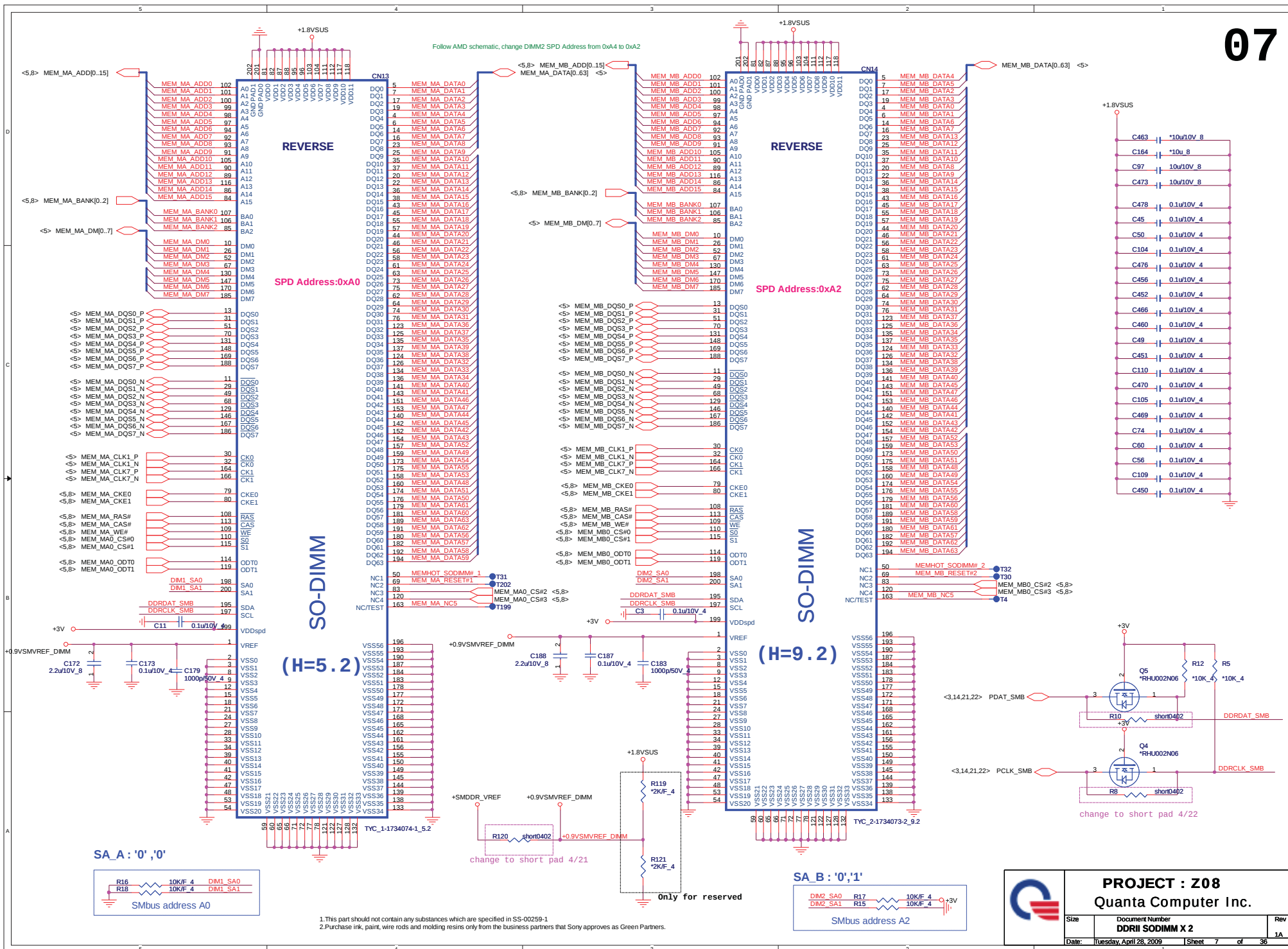
0319 Modify for EMI.



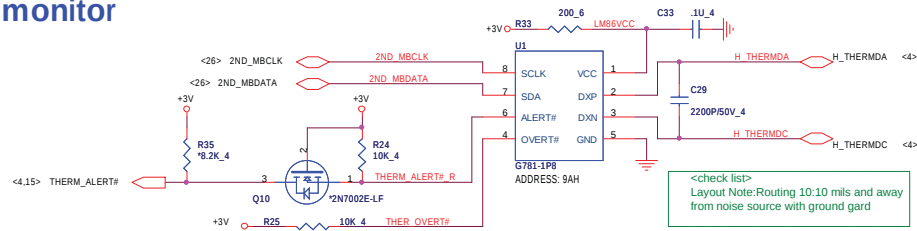
PROJECT : Z08
Quanta Computer Inc.

Size	Document Number	Rev
	TURION 64 PWR & GND	1A
Date:	Tuesday, April 28, 2009	Sheet 6 of 36

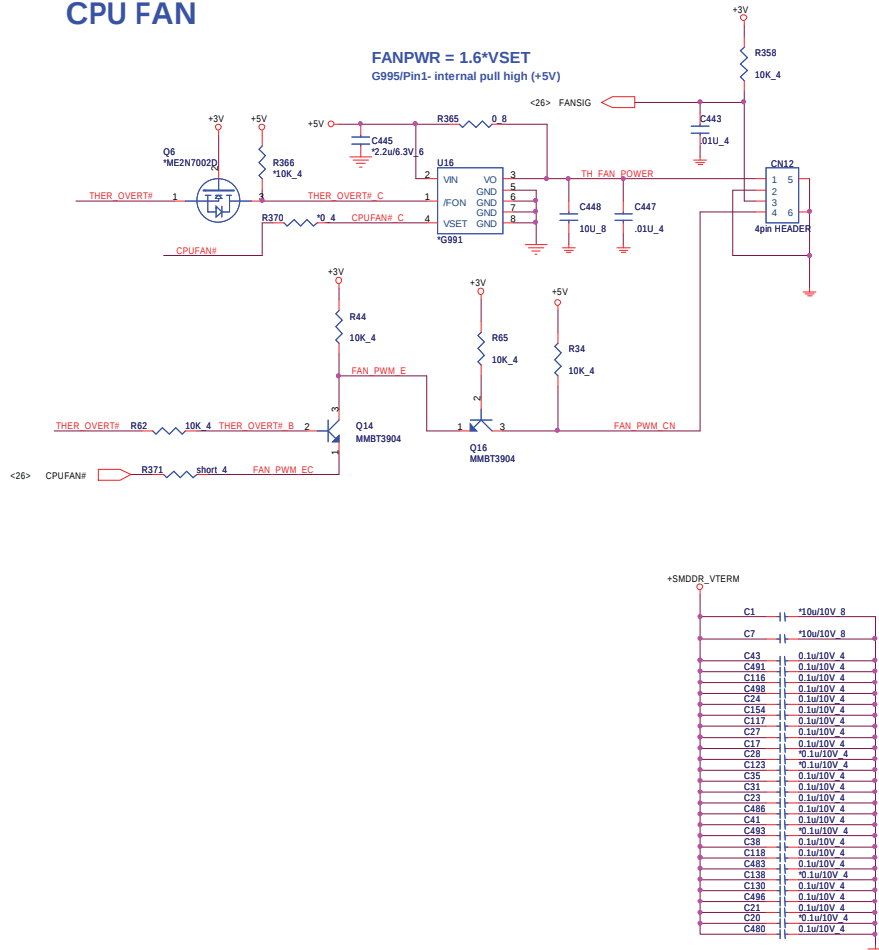
Follow AMD schematic, change DIMM2 SPD Address from 0xA4 to 0xA2



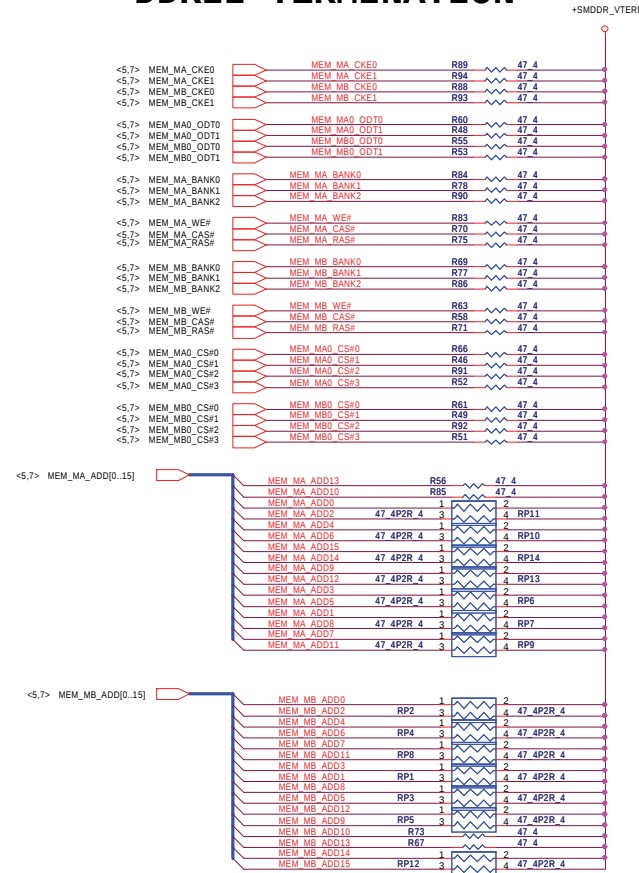
CPU Thermal monitor

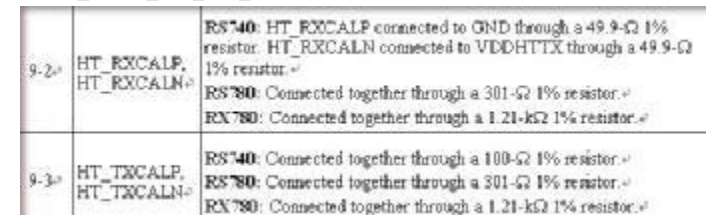


CPU FAN



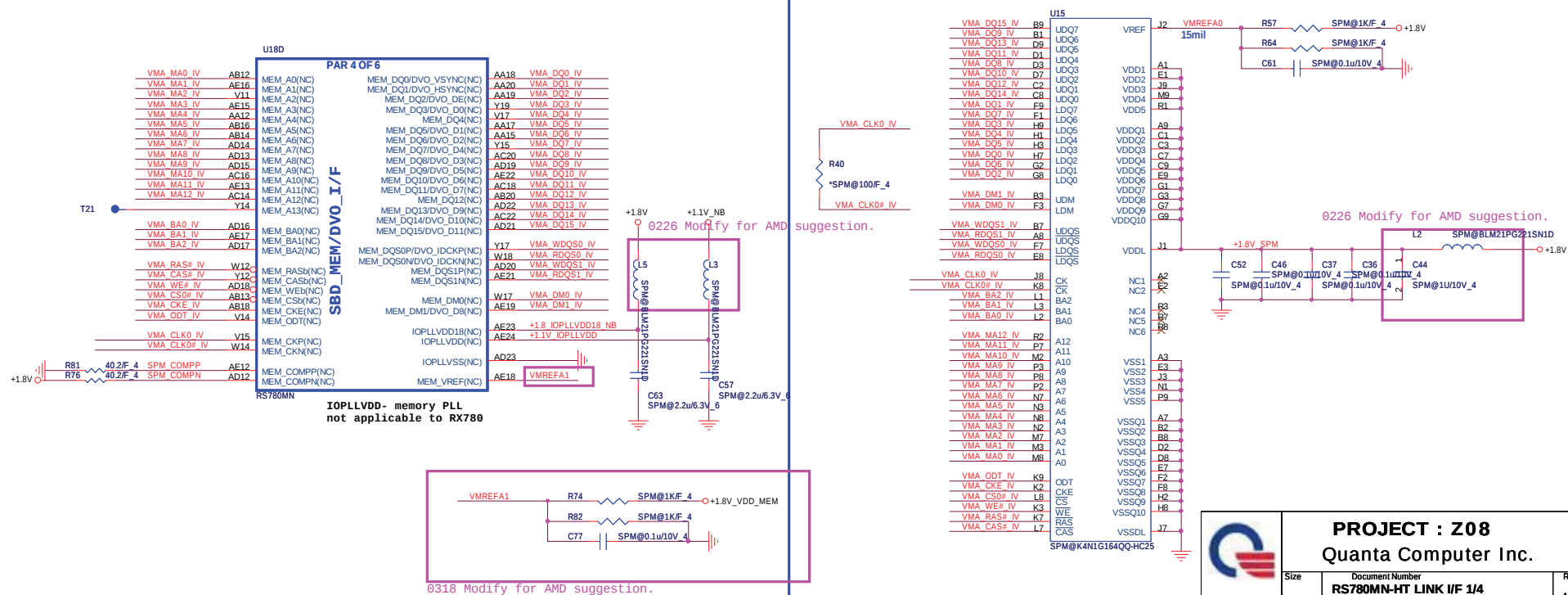
DDRII TERMINATION





signals	RS780	RX780	RES CHIP 1.21K 1/16W + -1%(0402) P/N : CS21212FB18 RES CHIP 300 1/16W + -1%(0402) P/N : CS13002FB00
HT_TXCALP	R641 300 ohm 1%	R641 1.21K ohm 1%	
HT_TXCALN			
HT_RXCALP	R655 300 ohm 1%	R655 1.21K ohm 1%	
HT_RXCALN			

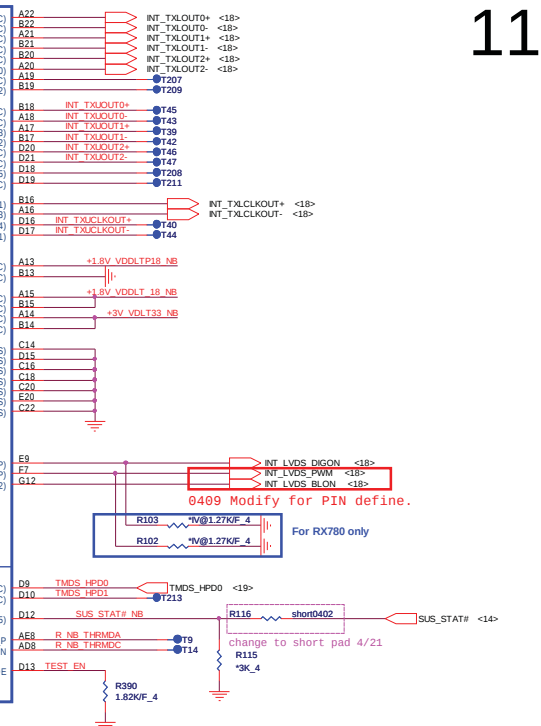
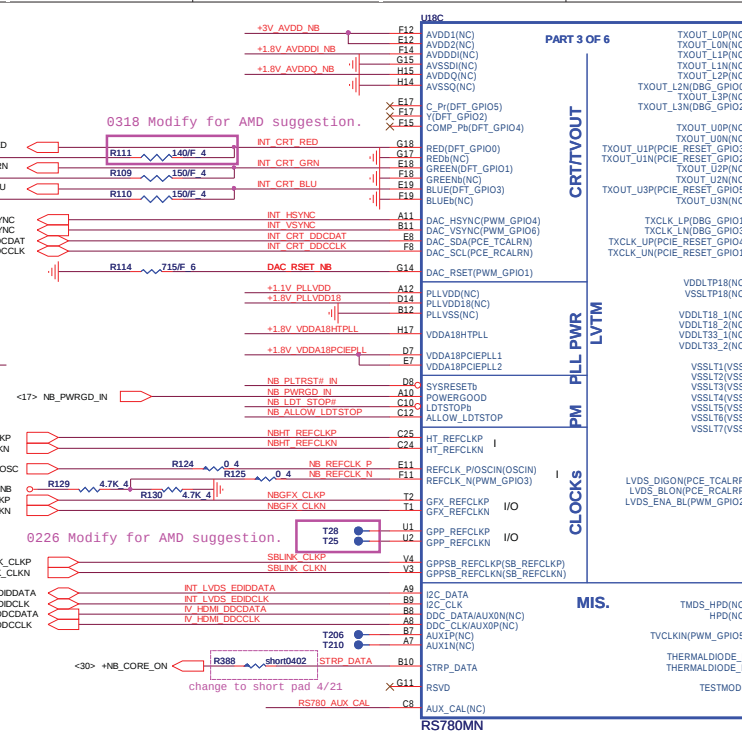
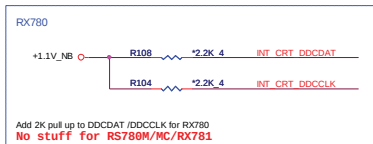
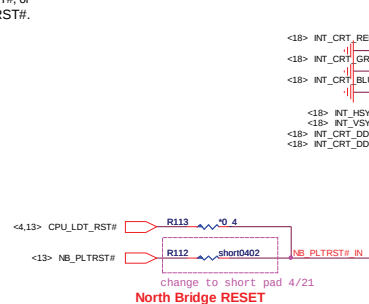
SPM(CLG)





Size	Document Number RS780MN-PCIE I/F 2/4	Rev 1A
Date:	Tuesday, April 28, 2009	Sheet 10 of 36

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

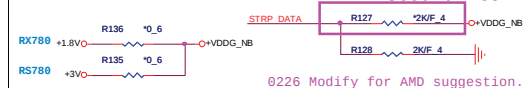


selects Loading of straps from EPROM
1: use default vaule , default
0: I2C Master can load strap values from EPROM
if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT



For external EEPROM Debug only

RS880M/RX881



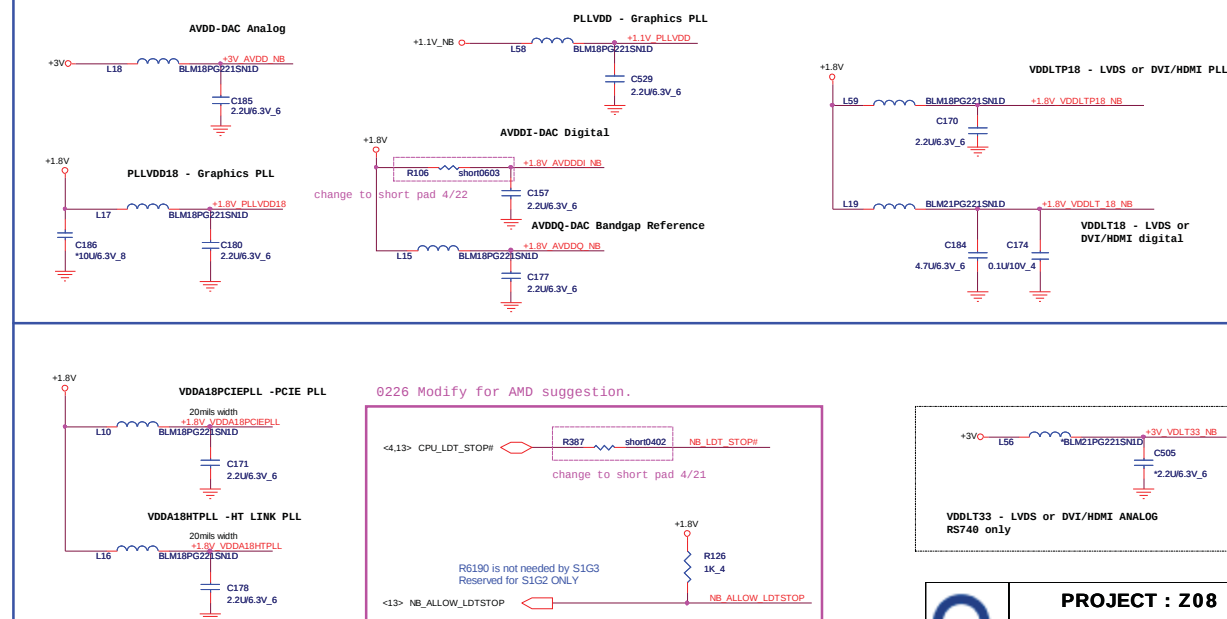
Enables Debug Bus access through memory T/O pads and GPIO.
1: Enable RS780, Default
0: Disable RS780
(RS780 use VSYNC#)

RS780



Indicates if memory Side port is available or not
0: available RS780, Default
1: Not available RS780
(RS780 use HSYNC#)

RS780



PROJECT : Z08
Quanta Computer Inc.

Size Document Number
RS780M-SYSTEM I/F 3/4
Date: Tuesday, April 28, 2009 Sheet 11 of 36 Rev 1A

RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD0	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD0	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD018	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVD018	NC	+1.8V	VDDLT33	NC	NC



+1.1V 2A for RS780M 0226 Modify for AMD suggestion.

VDDHT - HT LINK digital I/O for RX780/RS780

VDDHTRX - HT LINK RX I/O for RX780/RS780

+1.2V 2A for RS780M+SB700

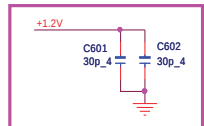
VDDHTTX - HT LINK TX I/O for RX780/RS780

+1.8V 1A for RS780M+SB700

VDDA18PCIE - PCIE TX stage I/O for RX780/RS780

VDD18 - RS780 I/O transform

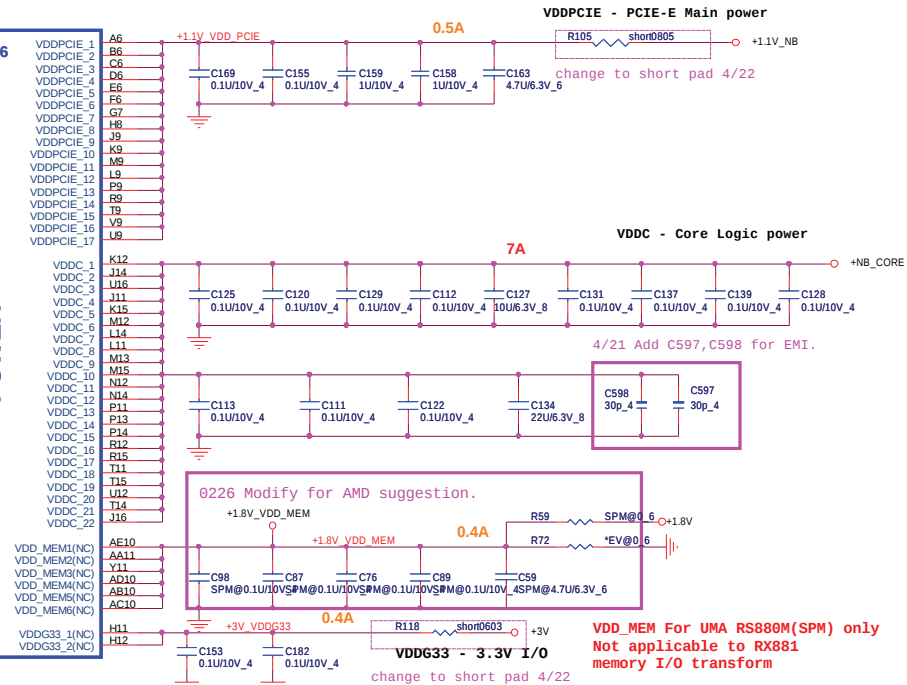
VDD18_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform



4/21 Add C601, C602 for EMI.

PART 5/6

POWER



PROJECT : Z08
Quanta Computer Inc.

Size Document Number
RS780MN-POWER4/4

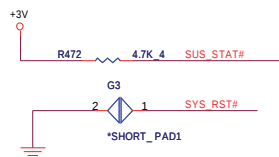
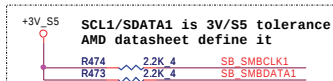
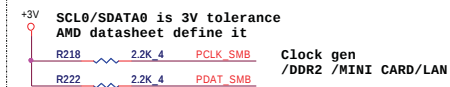
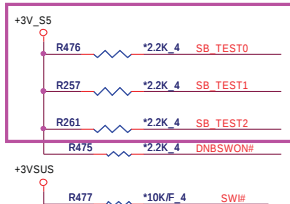
Date: Tuesday, April 28, 2009 Sheet 12 of 36

Rev
1A

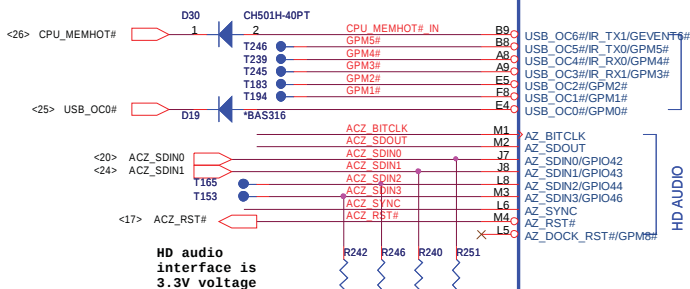
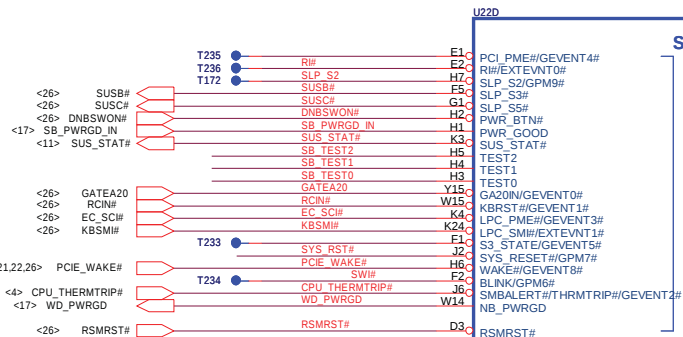
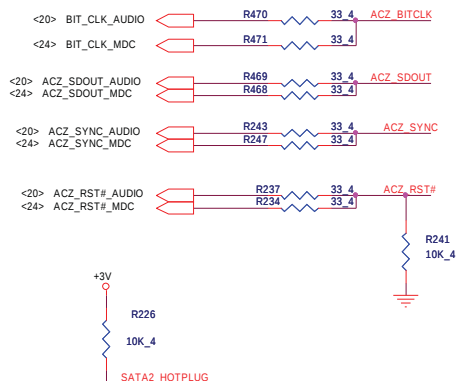


Size	Document Number SB710-PCIE/PCI/CPU/LPC 1/4	Rev 1A
Date:	Tuesday, April 28, 2009	Sheet 13 of 36

0318 Modify for AMD suggestion.



To Azalia



HD audio interface is 3.3V voltage

+1.8V R262 *10K 4

SB700

Part 4 of 5

ACPI / WAKE UP EVENTS

USB MISC

USB 1.1

GPIO

USB OC

HD AUDIO

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

SB700

Part 4 of 5

ACPI / WAKE UP EVENTS

USB MISC

USB 1.1

GPIO

USB OC

HD AUDIO

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

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INTEGRATED uC

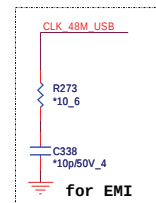
INTEGRATED uC

INTEGRATED uC

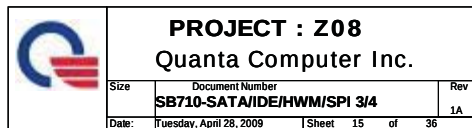
INTEGRATED uC

INTEGRATED uC

INTEGRATED uC

SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define itPROJECT : Z08
Quanta Computer Inc.

Size	Document Number	Rev
	SB710-ACP/GPIO/USB 2/4	1A
Date:	Tuesday, April 28, 2009	Sheet 14 of 36





Size	Document Number SB710-PWR/DECOUPLING 4/4	Rev 1A
Date:	Tuesday, April 28, 2009	Sheet 16 of 36

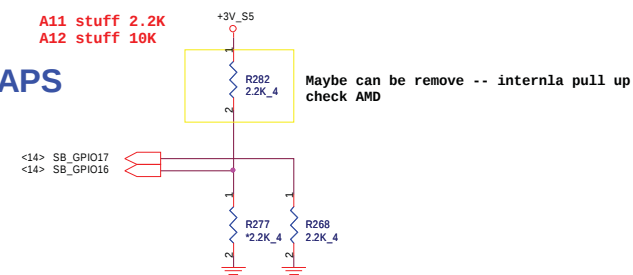


OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

It must ready
before RSMRST#

REQUIRED STRAPS

A11 stuff 2.2K
A12 stuff 10K

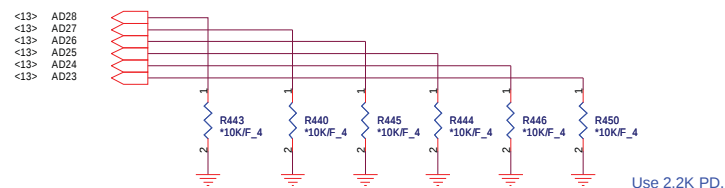


TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

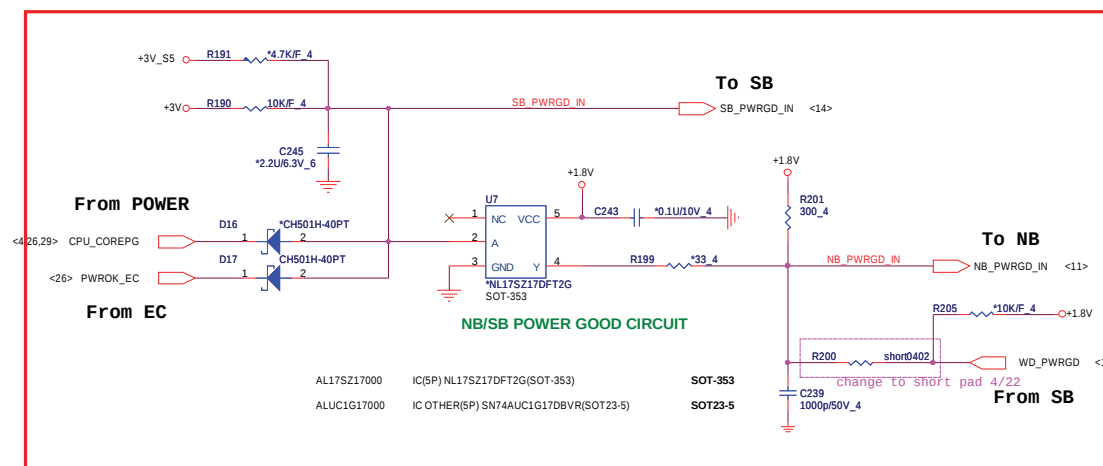
NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

DEBUG STRAPS SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

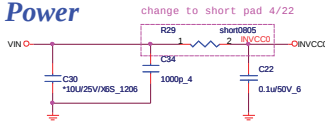


PROJECT : Z08
Quanta Computer Inc.

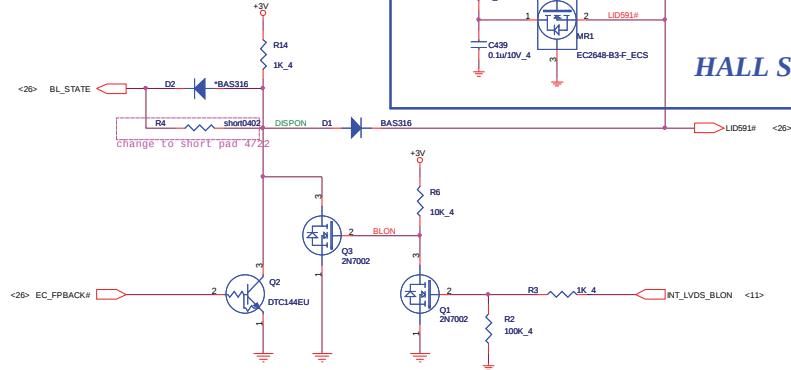
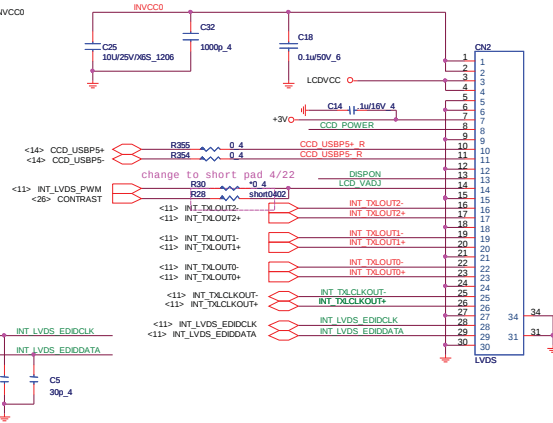
Size	Document Number	Rev
	SB710-STRAPS	1A

Date: Tuesday, April 28, 2009 | Sheet 17 of 36

Backlight Power (LDS)

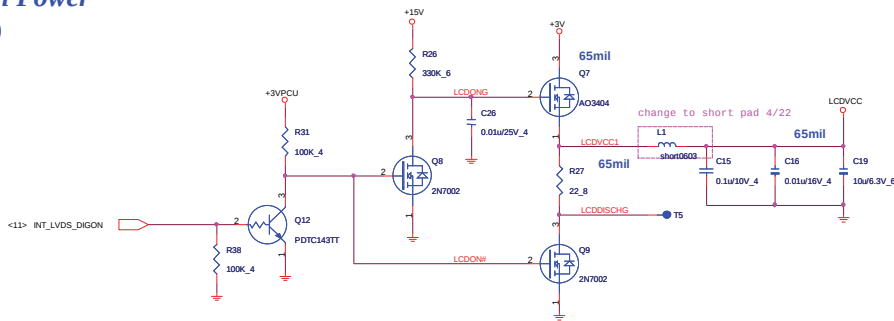


LVDS Coaxial Connector

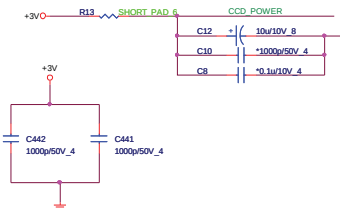


HALL Sensor (HSR)

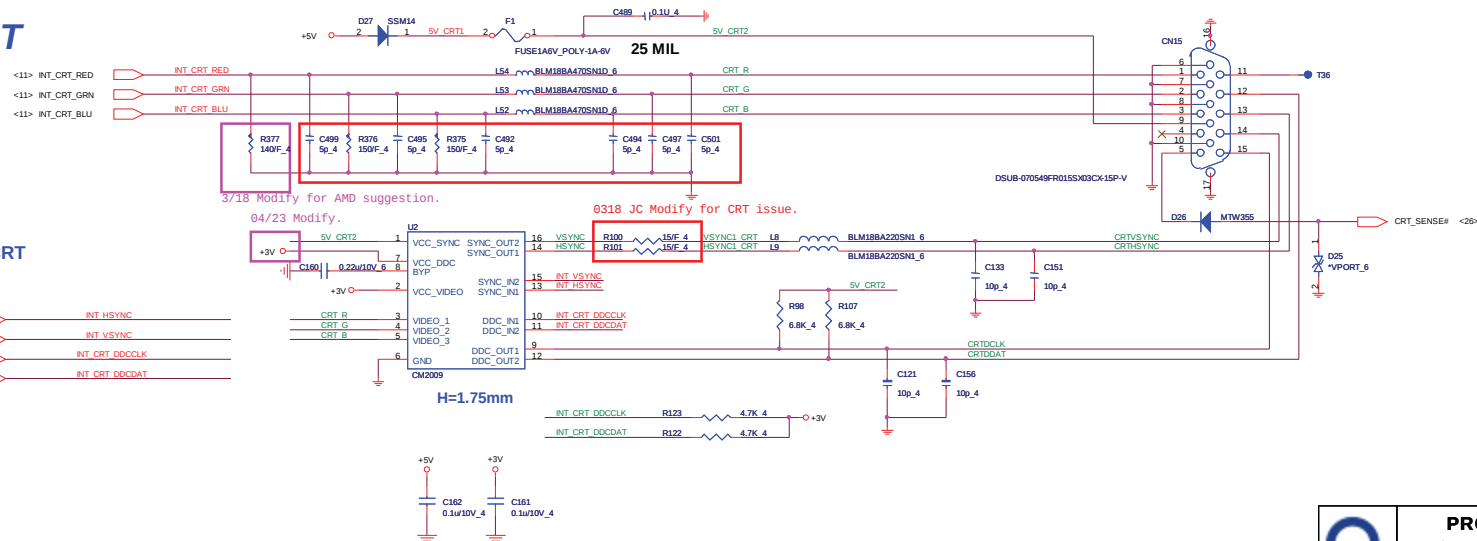
Panel Power (LDS)



CAMERA Module (CCD)



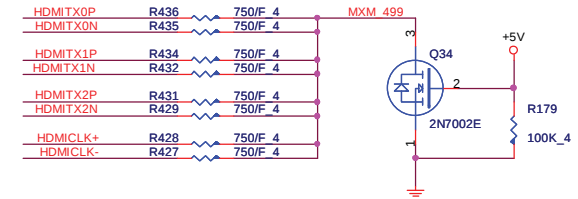
CRT PORT
(CRT)



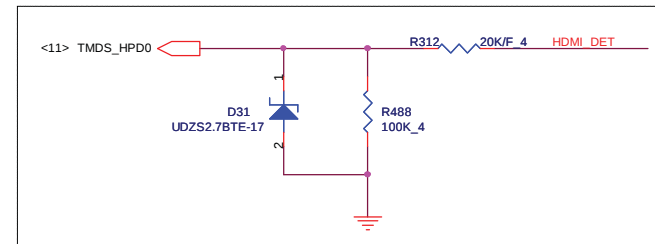
UMA to CRT



(HDM)

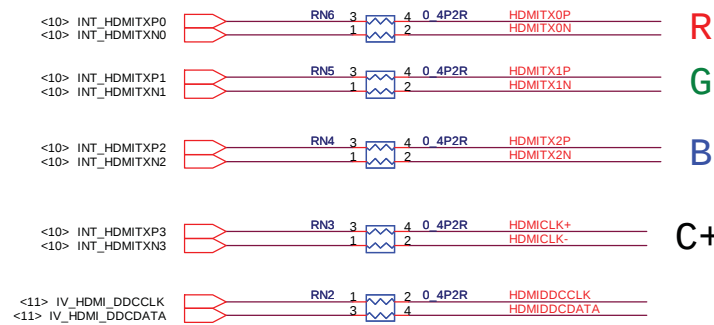


HDMI HPD SENSE



4/23 Modify HDMI detect circuit.

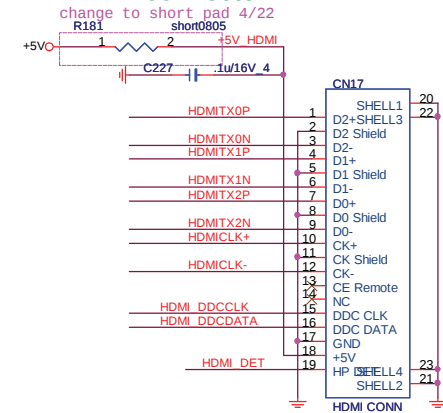
(HDM)



Close to HDMI Connector
DDC4 is 5V tolerance, the MOSFET level shifter no need.

4/22 Modify for AMD suggestion.

HDMI connector



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			Quanta Computer Inc.			
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	HDMI				1A	
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(CX20561-15Z for QFN)

(ADO)

For EMI Request

4/23 Remove R312; mount C365 for EMI.
C365
10P/50VCOG_4

add EAPD 8/21
R328 *10K_4 GPIO1
R327 *10K_4 GPIO2

PC BEEP GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

CX20561-12Z Not support digital MIC
CX20561-13Z support digital MIC

Port A -- System headphone Jack (JD : HP_PLG)
Port C -- System Stereo Microphone Jack (JD : MIC1_PLG)
Port D -- System Speaker (JD : N/A)

Int. Stereo Speakers

AUD_SPK_R1 L14 BK1608HM241-T
AUD_SPK_R2 L13 BK1608HM241-T
AUD_SPK_L1 L12 BK1608HM241-T
AUD_SPK_L2 L11 BK1608HM241-T

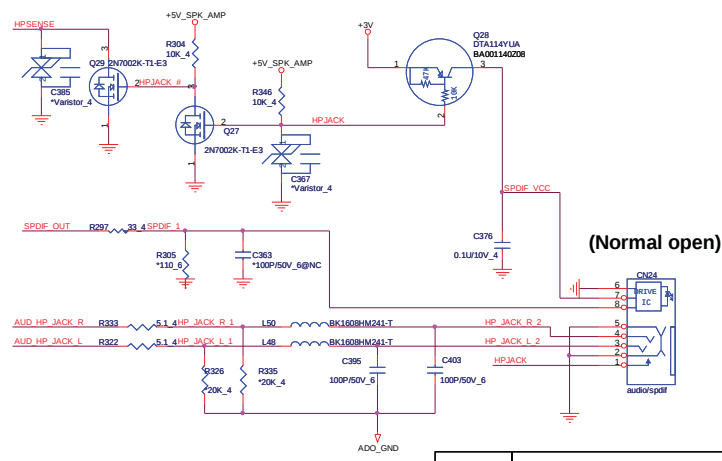
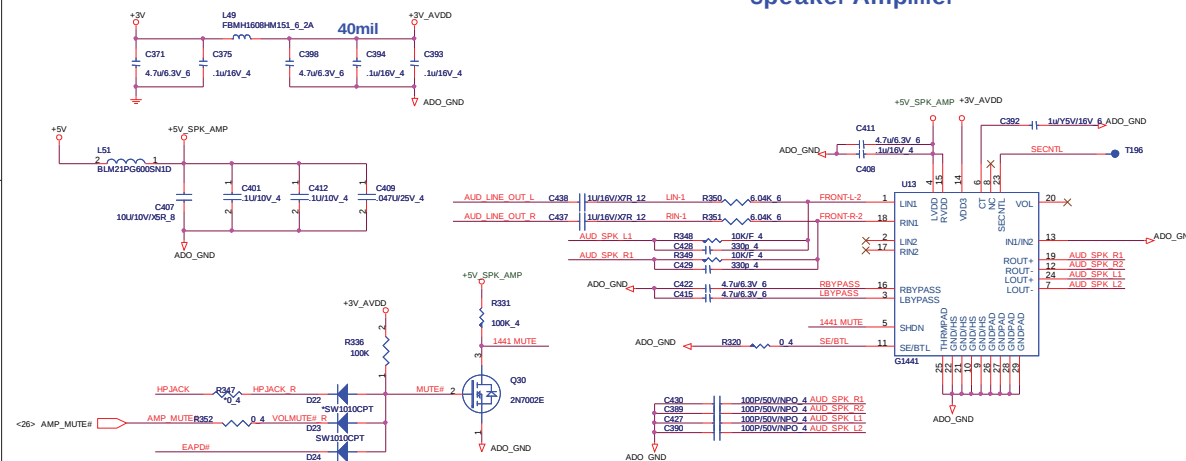
20

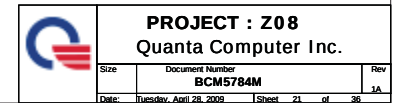
EXT. Mic in
Normal Open Type

(AMP)

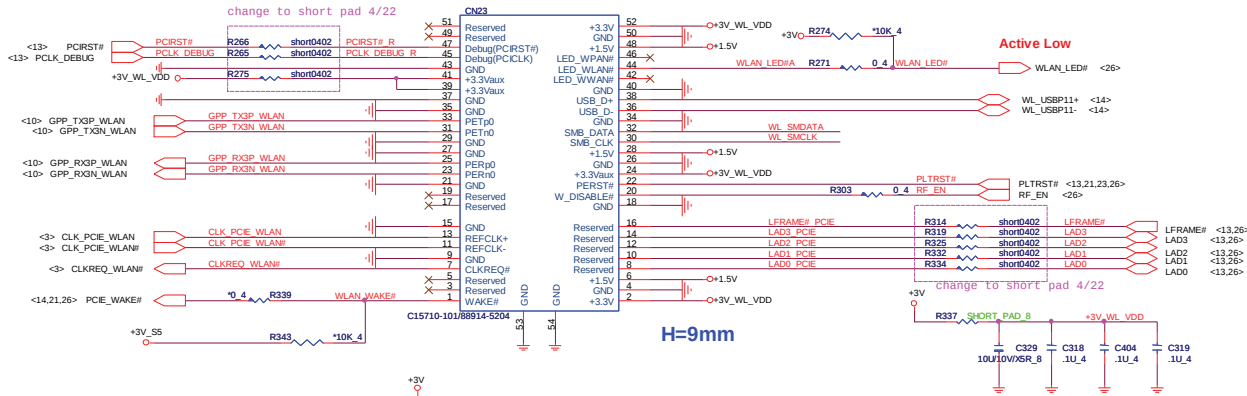
AUDIO AMPLIFIER G1441 Speaker Amplifier

Headphone out + Spdif Out (normal open)



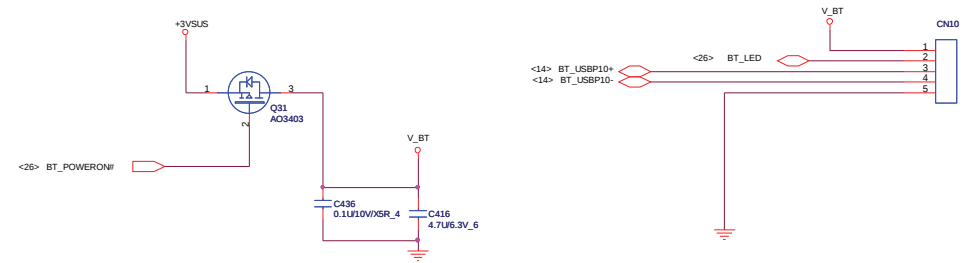


MINI-Card I (WLAN)



H=9mm

BLUETOOTH CONNECTOR

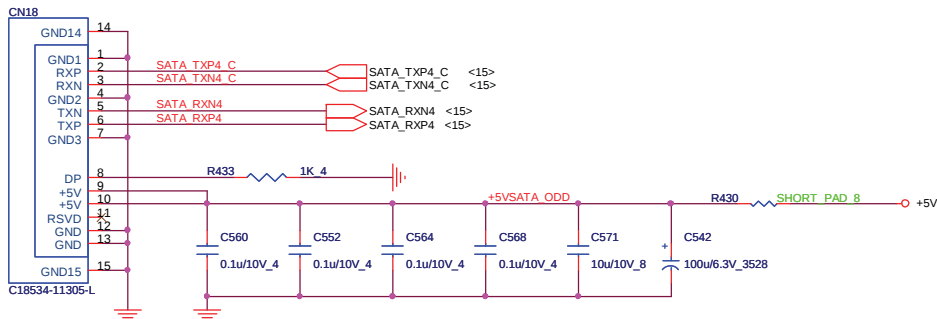


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	Mini-Card/WL	1A
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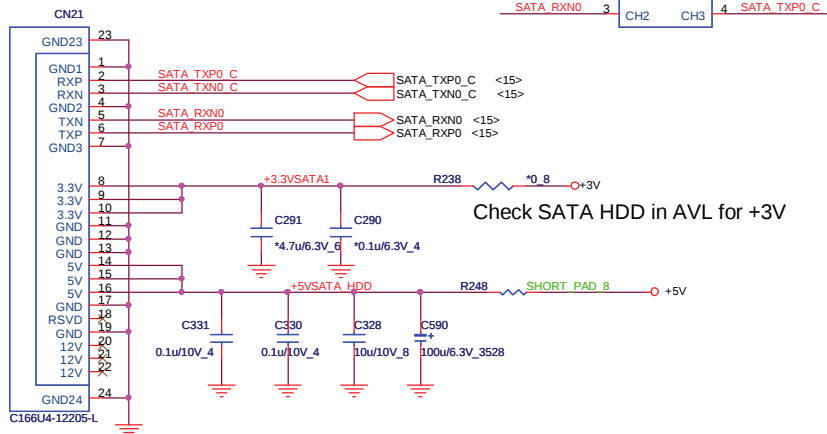


Size	Document Number Card Reader RTS5159	Rev 1A
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SATA ODD

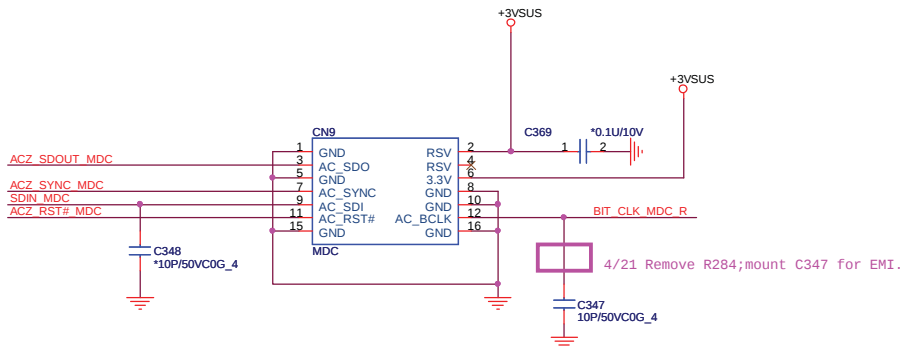


SATA HDD



Check SATA HDD in AVL for +3V

For MDC Module



PROJECT : Z08
Quanta Computer Inc.

Size	Document Number SATA/HDD&ODD/MDC	Rev 1A
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The schematic diagram illustrates the LED driver circuit for the Raspberry Pi 4 Model B. It features two LEDs, LED1 and LED2, connected to the Pi's GPIO pins. LED1 is connected to GPIO13 (BATLED1#) and GPIO14 (BATLED0#) via a 330 Ohm resistor (R340). LED2 is connected to GPIO15 (BATLED0#) and GPIO16 (BATLED1#) via a 330 Ohm resistor (R341). Both LEDs are powered by a 3V3 CPU supply. The LEDs are labeled 'Blue' and 'Red'.

The image shows a PCB layout for the NTC031-AA1G-A160T sensor module. The layout is divided into two main sections: the top section for power and signal connections, and the bottom section for the sensor connections.

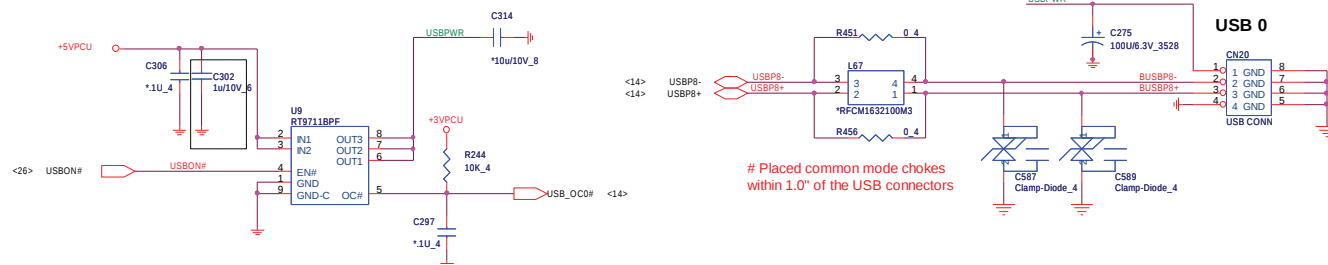
Top Section: Power and Signal Connections

- Power:** A +5V supply is connected to the left channel. A 4.7K_4 resistor (R159) is connected between +5V and the left channel. A 4.7K_4 resistor (R158) is connected between the left channel and the right channel. A 12 MIL shunt resistor (L21) is connected between the left channel and the right channel. A 100P-ESD_6 capacitor (C306) is connected between the left channel and ground. A 100P-ESD_6 capacitor (C307) is connected between the right channel and ground.
- Signal:** The left channel is connected to the TPCLK and TPDATA signals. The right channel is connected to the TPCLK_R and TPDATA_R signals. A 0.1u10V/KSR_4 capacitor (C193) is connected between the right channel and ground.
- Dimensions:** The layout is labeled with dimensions: 12 MIL, 4/22, and 4/22.

Bottom Section: Sensor Connections

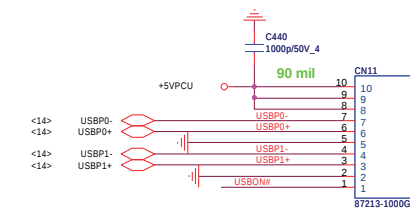
- Left Channel:** The left channel is connected to the NTC031-AA1G-A160T sensor. A 1K_4 resistor (R317) is connected between the left channel and the sensor. A 680P/50V/NPO_4 capacitor (C381) is connected between the left channel and ground. A 0.1u10V/KSR_4 capacitor (C382) is connected between the left channel and ground. A 100P-ESD_6 capacitor (C380) is connected between the left channel and ground.
- Right Channel:** The right channel is connected to the NTC031-AA1G-A160T sensor. A 1K_4 resistor (R318) is connected between the right channel and the sensor. A 680P/50V_4 capacitor (C386) is connected between the right channel and ground. A 0.1u10V/KSR_4 capacitor (C387) is connected between the right channel and ground. A 100P-ESD_6 capacitor (C388) is connected between the right channel and ground.
- Dimensions:** The layout is labeled with dimensions: 12 MIL, 4/22, and 4/22.

USB PORT(X1)



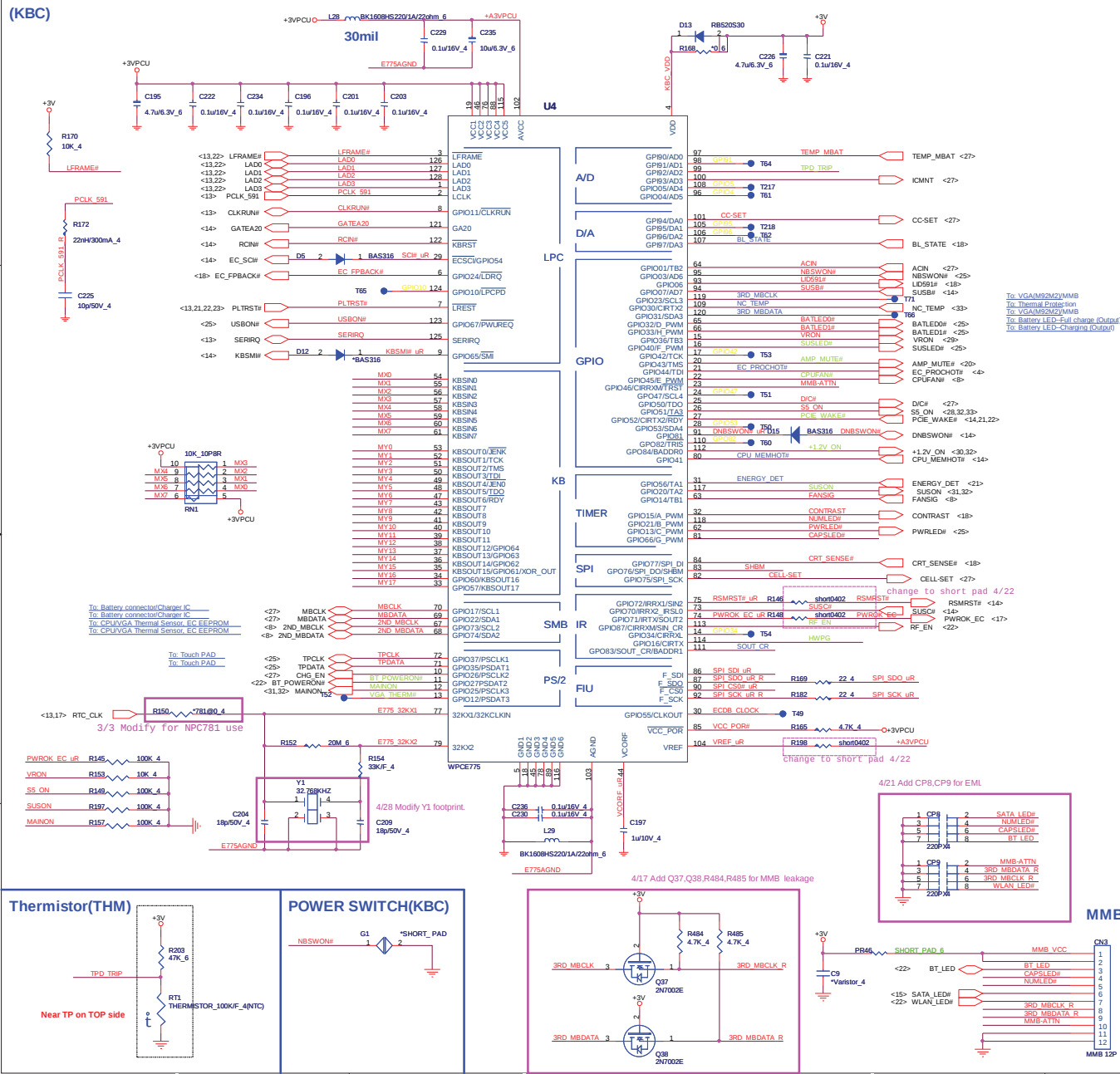
Please reserve $C_{in} = 1\mu F$ (stuff), $C_{out} = 10\mu F$ (don't stuff) for Richtek RT9711BPF
Please reserve $C_{in} = 4.7\mu F$ (stuff), $C_{out} = 10\mu F$ (don't stuff) for GMT solution

To USB Board



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Size	Document Number	F
	FP/TP/USB/BT/FELICA/FM	1
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I/O ADDRESS SETTING(KBC)

IO Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHRMe0: Enable shared memory with host BIK

SHBM=0: Enable shared memory with host BIOS

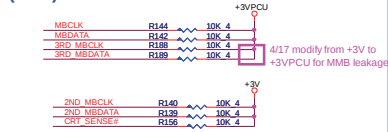
BADDR0 +1.2V ON R187 10K 4

BADDR1 SOUT CR R186 *10K 4

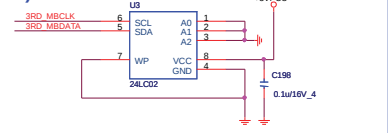
SHBM SHBM R160 10K 4

1/13 Confirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

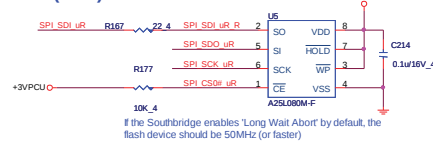
SM BUS PU(KBC)



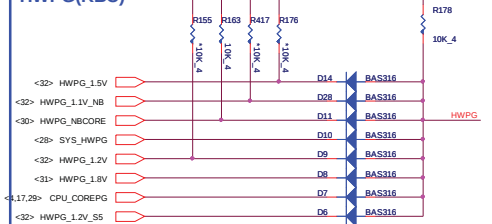
ACER ID(KBC)



SPI FLASH(KBC)



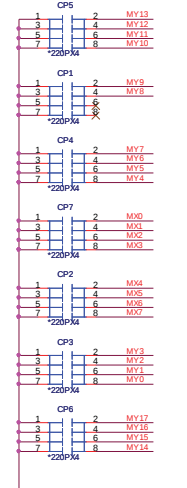
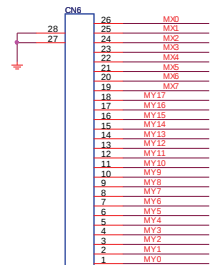
HWPG(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

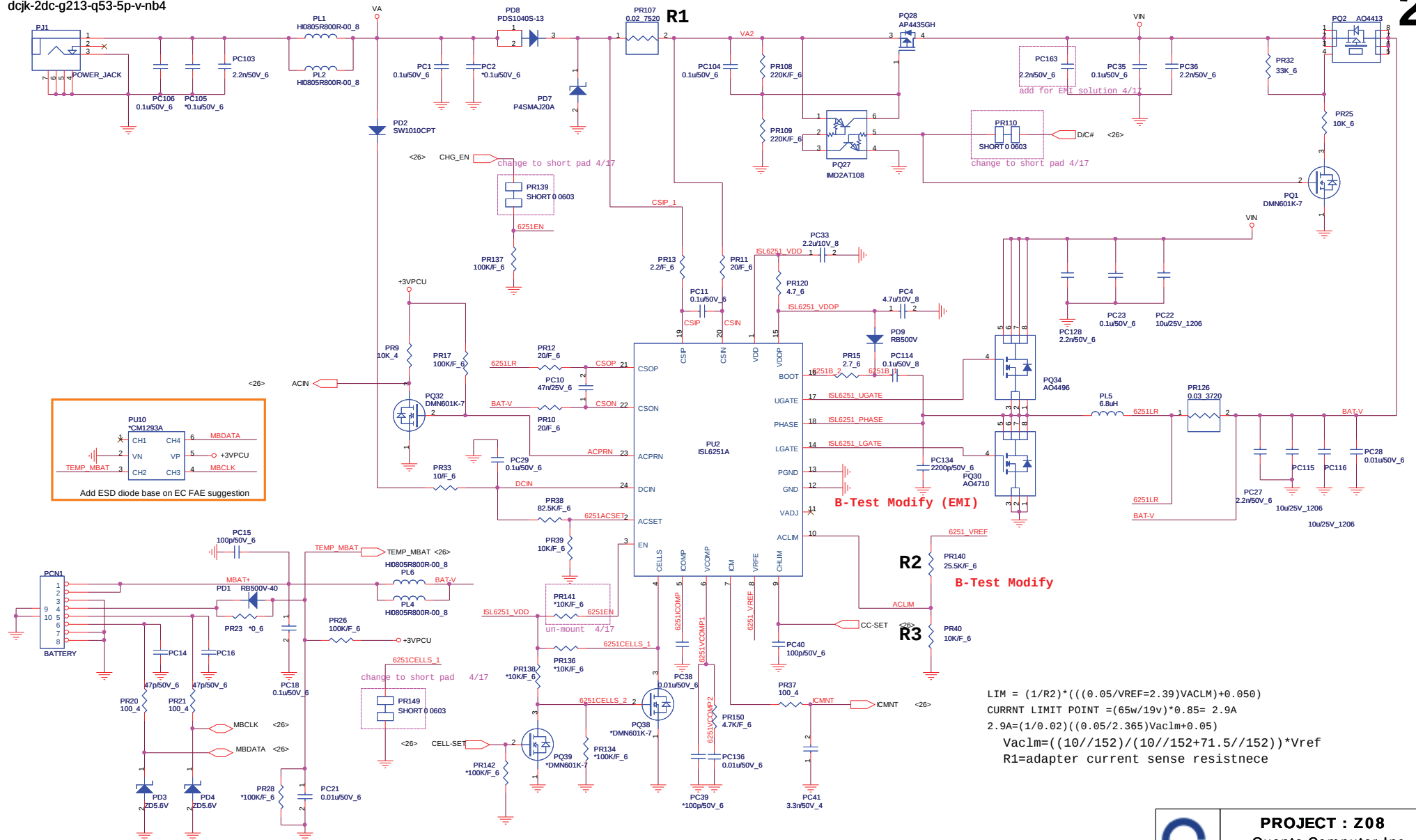


KEYBOARD



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Size	Document Number WPCE775C_0DG & FLASH	Rev 1A
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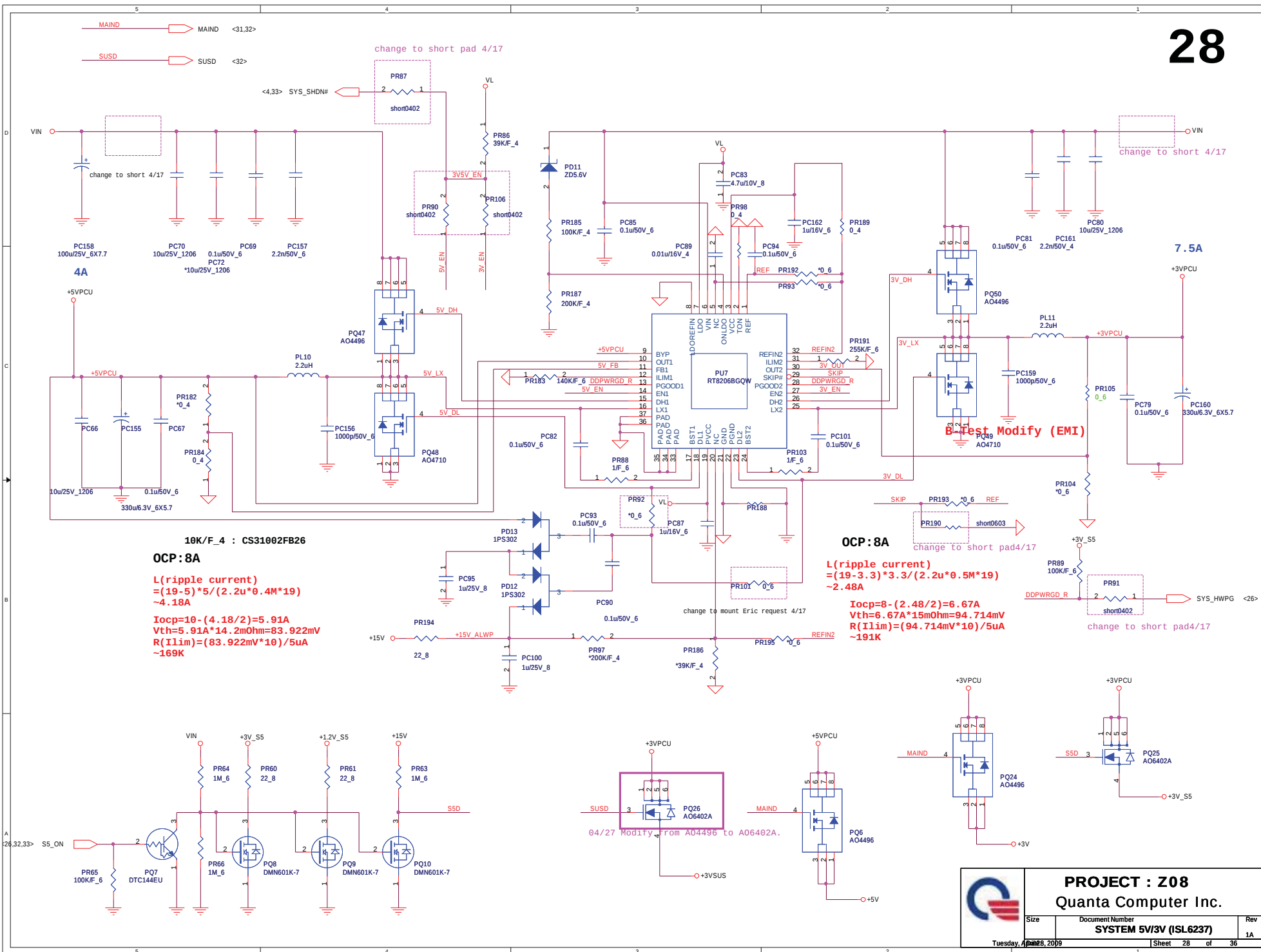


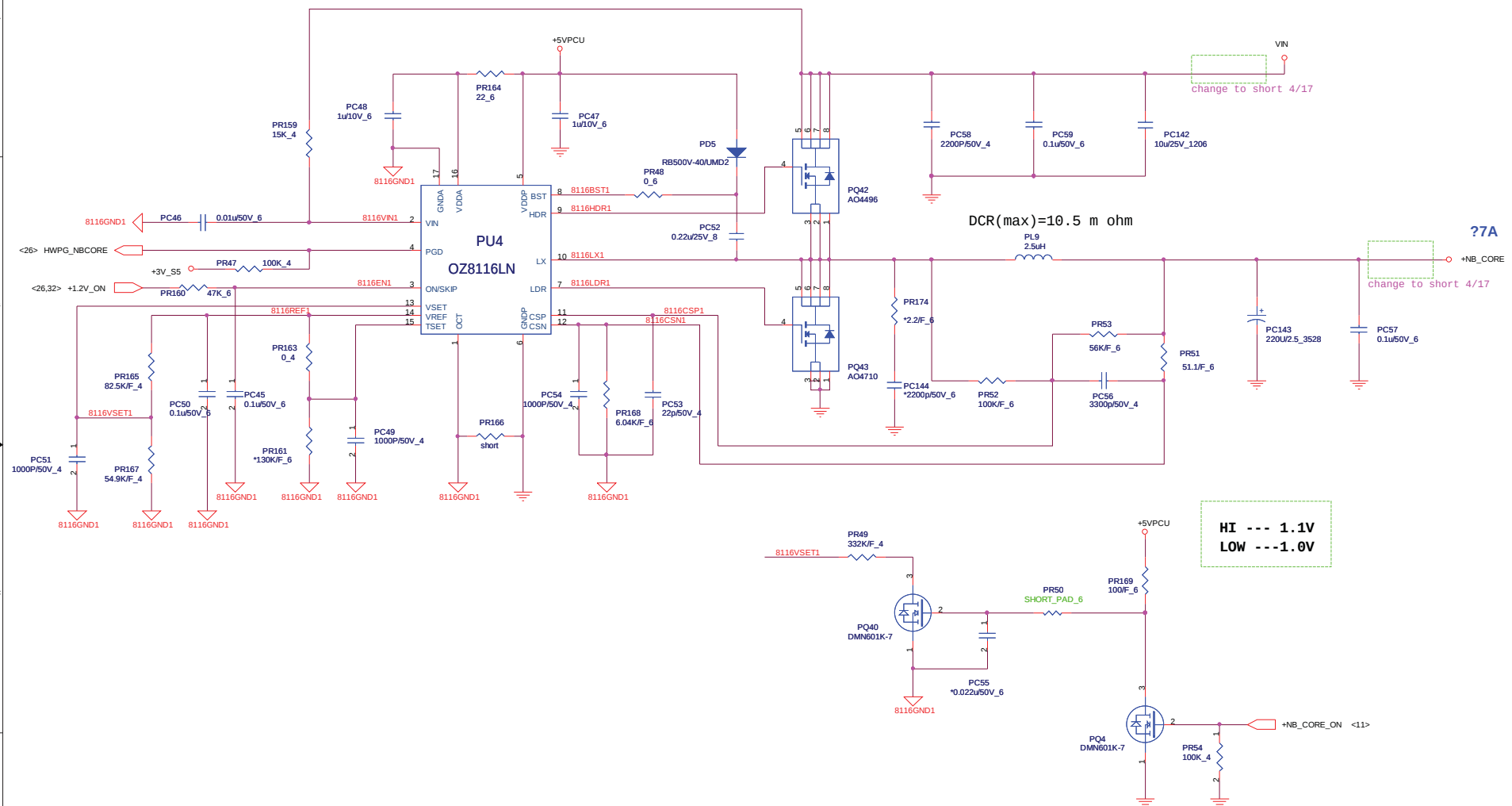
CELL-SET = H1 ----> Cells = VDD ----> 4S
 CELL-SET = Low ----> Cells = GND ----> 3S



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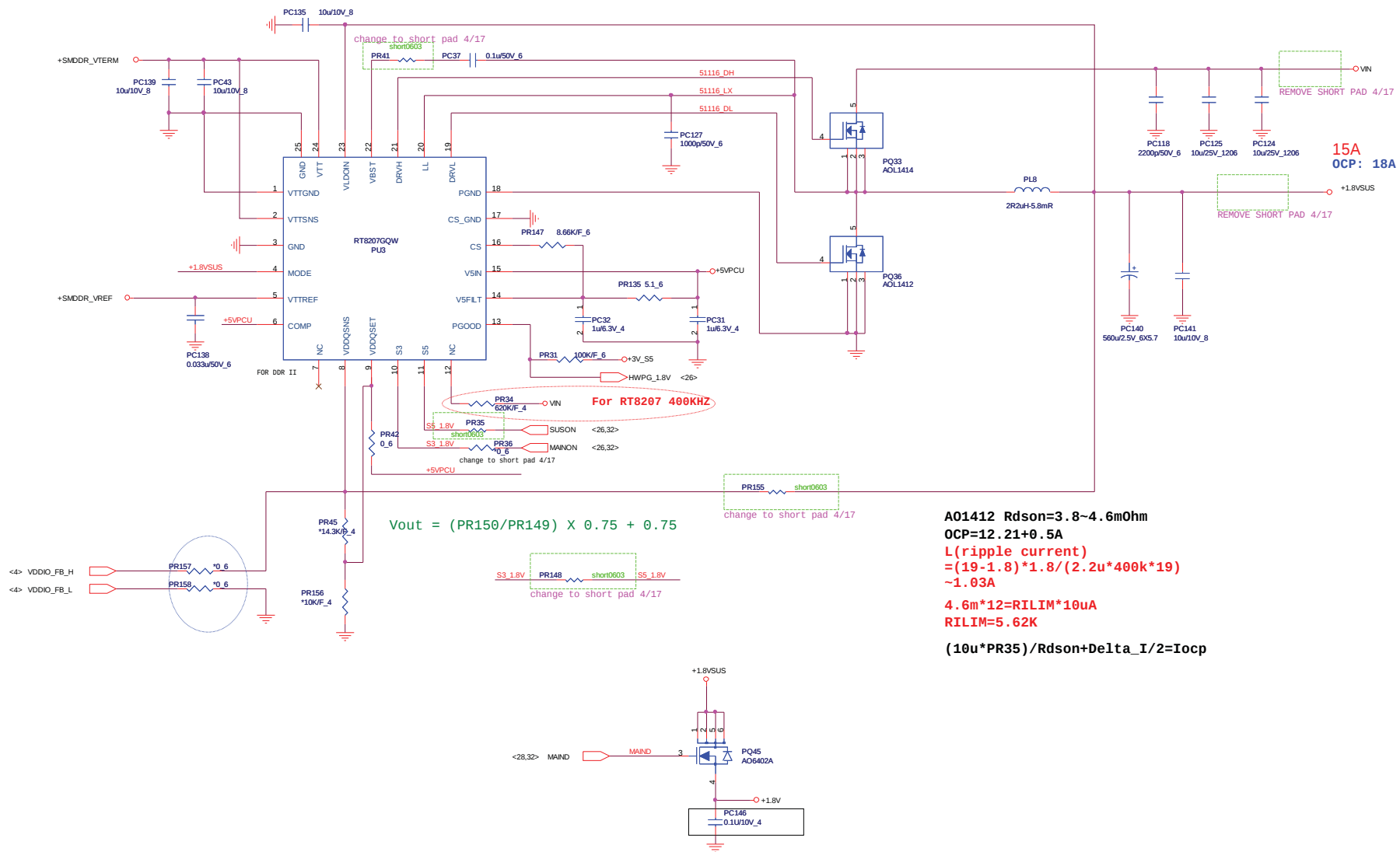
Size	Document Number	Rev
	CHARGER (ISL6251A)	
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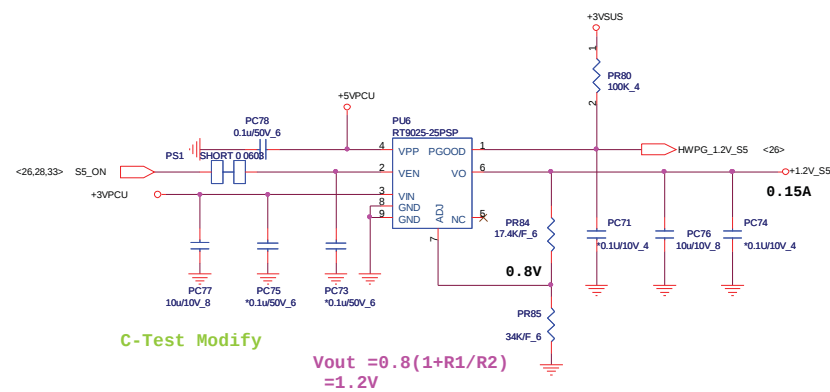
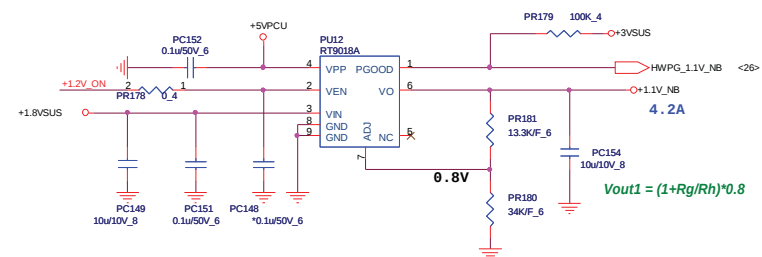
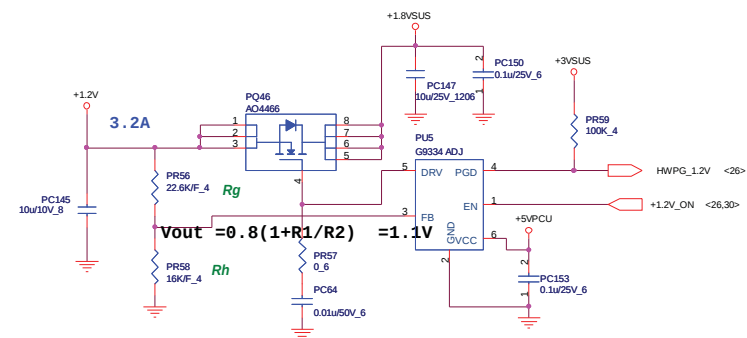
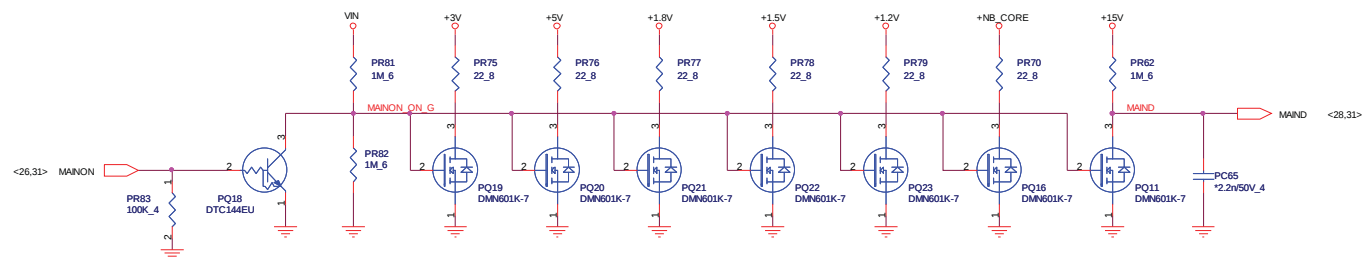
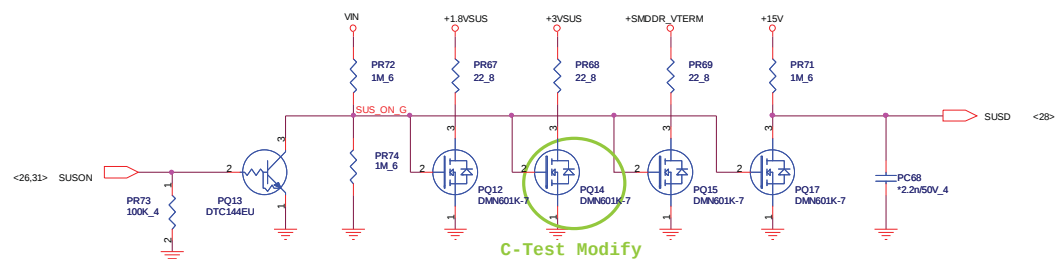
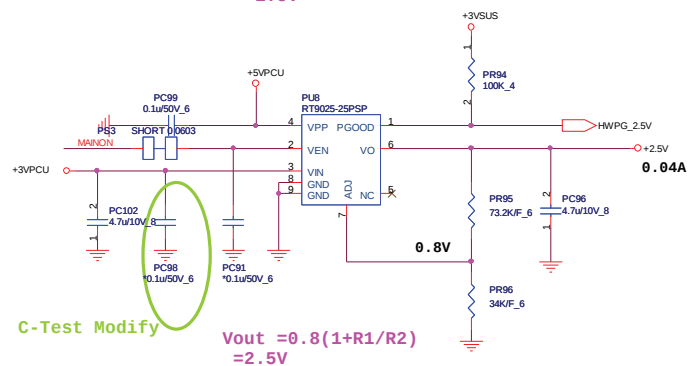
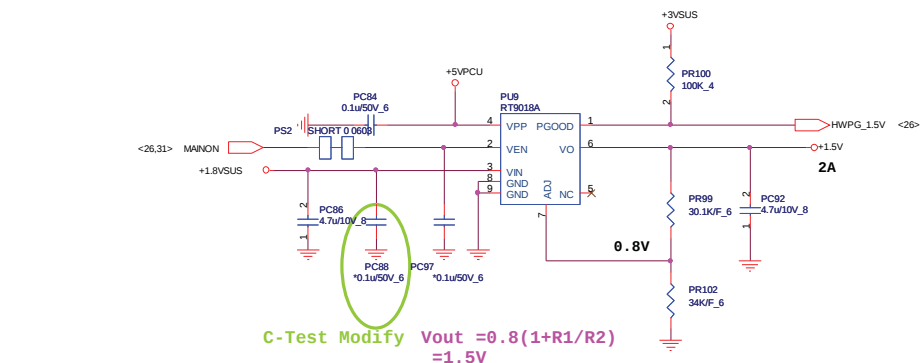




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Size	Document Number	Rev
	NB_CORE (OZ8116LN)	1A
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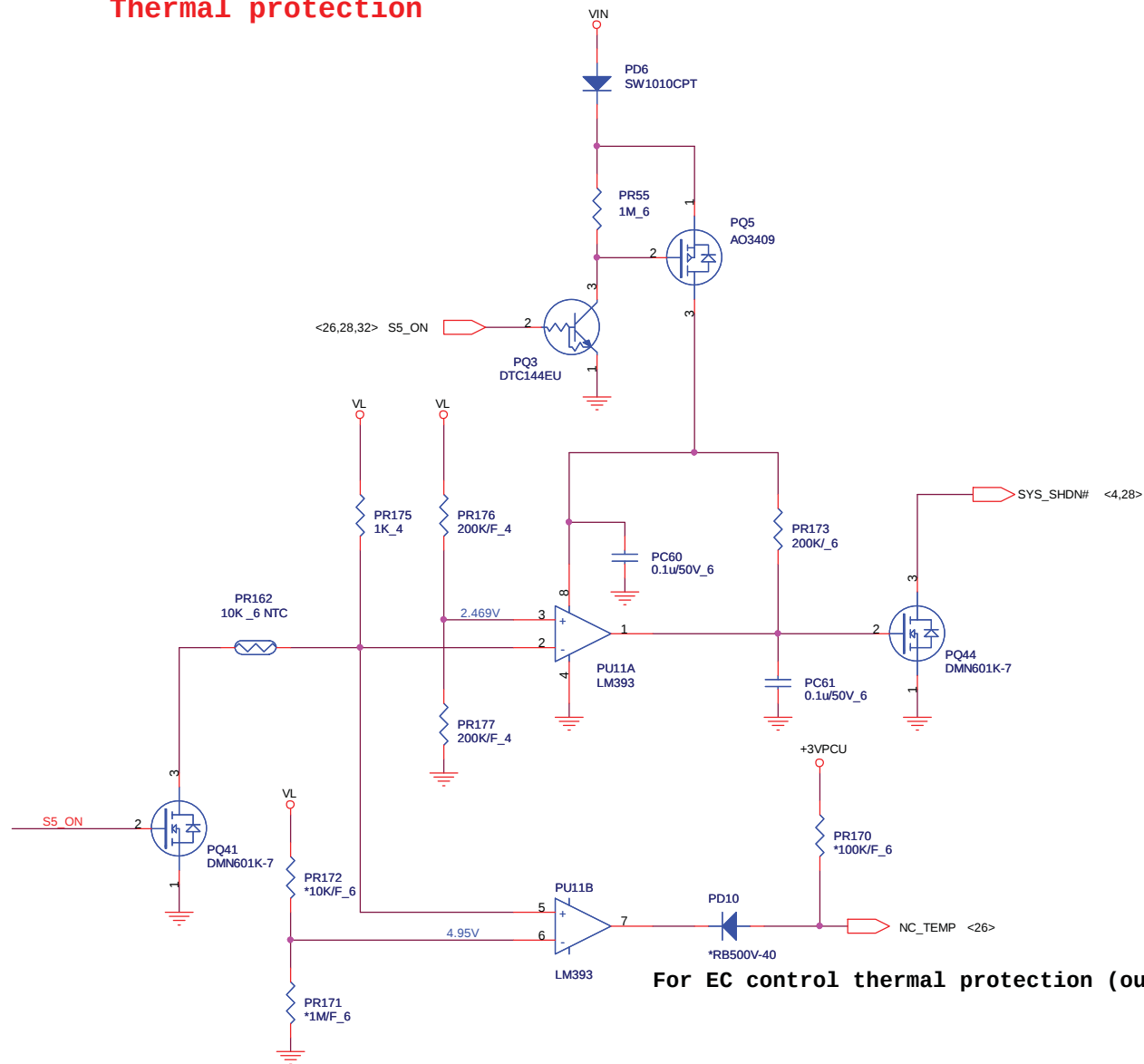


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Size	Document Number	Rev
	Discharge (1.25V/1.5V)	1A
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Thermal protection

33



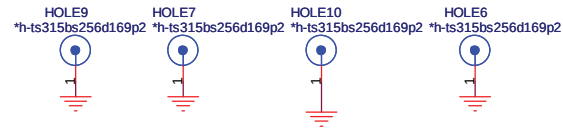
For EC control thermal protection (output 3.3V)



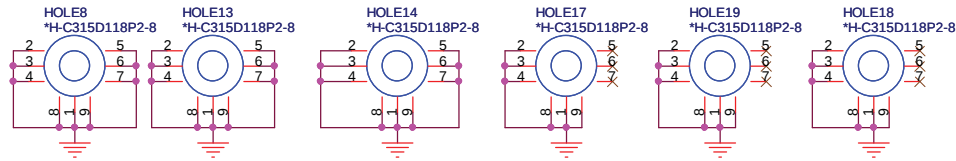
PROJECT : Z08
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.25V/1.5V)	1A
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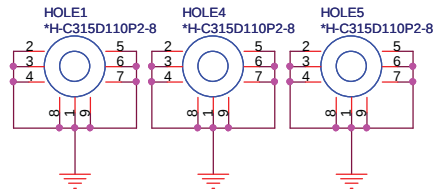
CPU HOLE



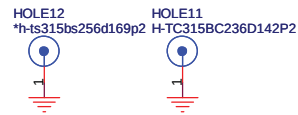
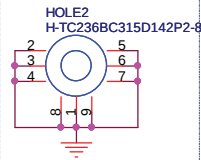
8 X 3.0



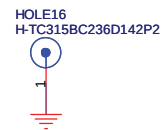
8 X 2.8



TOP 8 X 3.6 BOT 6 X 3.6

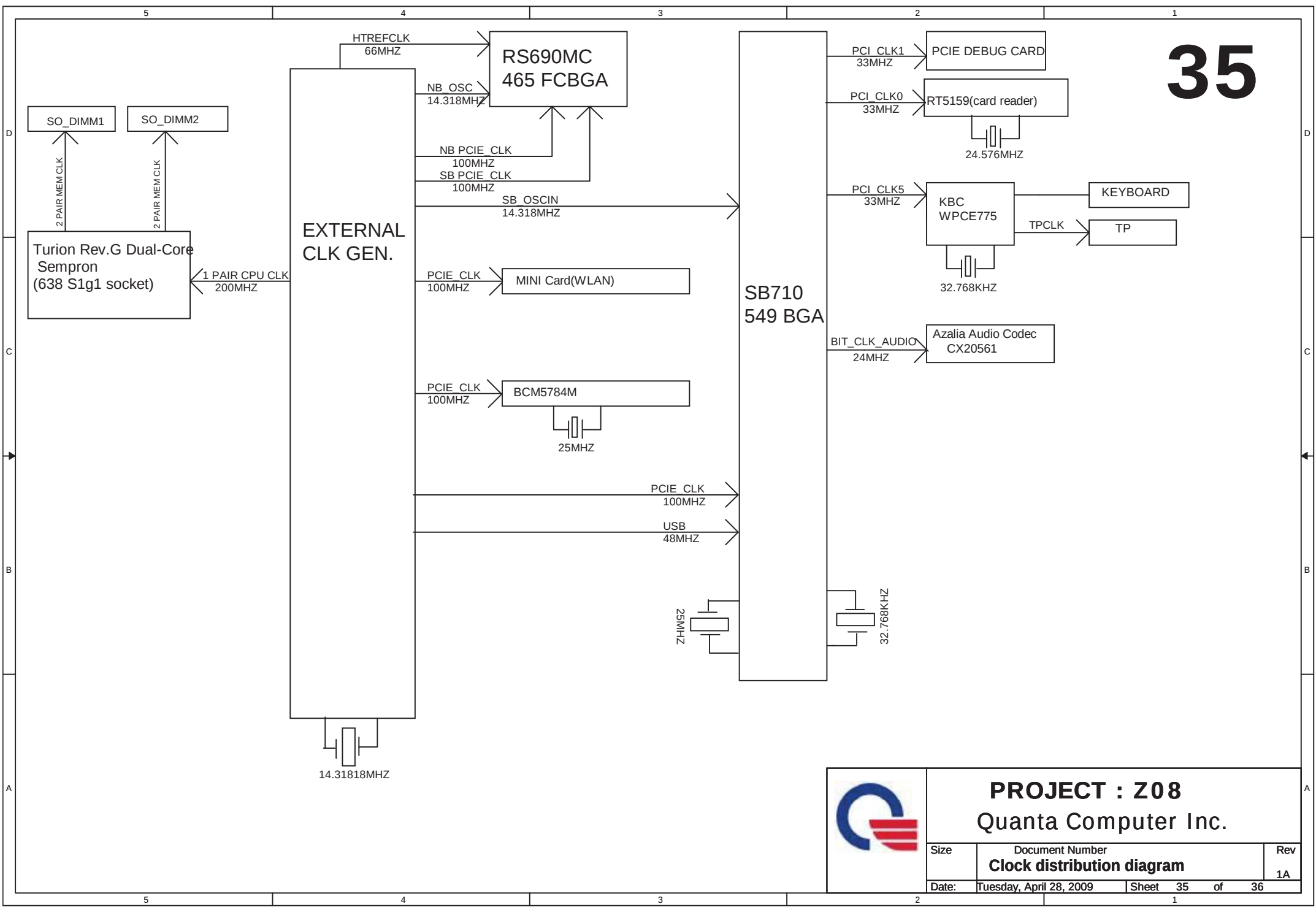


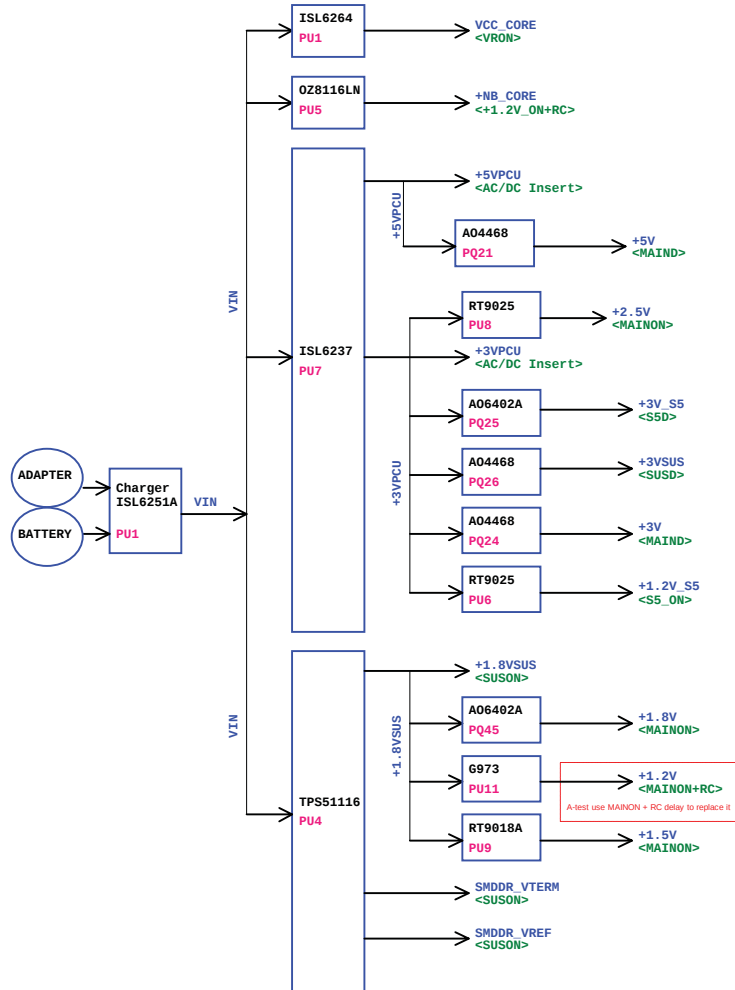
MDC



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	Blank	1A
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POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_CORE	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	