SP7(Nikita) BLOCK DIAGRAM PV

01

PCB STACK UP

12L Dis.

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : IN3(High)
LAYER 7 : SVCC1
LAYER 8 : SVCC2
LAYER 9 : IN4
LAYER10 : IN5(High)
LAYER11 : GND
LAYER12 : BOT

A Channel
DDR3-SODIMM1
DDR3-SODIMM2
PAGE 13,14

DDR3 800,1066,1333 MT/s

B Channel
DDR3-SODIMM3
DDR3-SODIMM4
PAGE 15,16

DDR3 800,1066,1333 MT/s

Intel Clarksfield
CPU 45Watt
4 Core
(rPGA 989)
PAGE 3-6

PCI-Express Gen2 X8

PCI-Express Gen2 X1

VRAM DDR3*8 (1Gb) PAGE 23-24

ATI M97/Broadway/Madison (128bit)
(FCBGA)
962p 29X29mm
PAGE 18-22

27MHz

Dual Channel LVDS

HDMI CON (1920*1200) PAGE 25

LCD CONN for dual channel (15.6") PAGE 25

USB3.0 Port x2 PAGE 26

NEC USB3.0 Controller PAGE 26

DMI*4

BCLK133M
DMI100M
DP120M

32.768KHz

100M PCIE

133M BCLK
100M PCIE
96M DOT
REF CLK

14.318MHz

CLOCK GEN 9LRS3197 PAGE 02

PCH 3.5Watt
Platform Controller Hub
PAGE 7-12

ONFI

Braiwood (NAND Flash Memory) PAGE 34

CPU THERMAL SENSOR PAGE 27

32.768KHz

SATA 2.5" HDD
SATA 1.8" SSD1
PAGE 30

SATA0 150MB

SATA 1.8" SSD2 PAGE 30

SATA1 150MB

E-SATA(USB2.0) PAGE 26

SATA2 150MB

USB2.0 48M

6,7 USB2.0 Port X2 PAGE 26

5 BlueTooth PAGE 31

4 Webcam w/ Mic PAGE 31

3

2 Card Reader
Realtek
RTS5159
PAGE 30

2-in-1 flash media slot(SD/MMC) PAGE 30

Accelerometer
LIS3LV02DL PAGE 31

SMBUS

32.768KHz

LPC

PCI-E 100M

Azalia

X1 LAN
Atheros
PCIE-LAN
AR8131(M)
GigaLAN
PAGE 32

25MHz

RJ45 PAGE 32

X1 half size mini-card
(Wireless LAN
Shirley Peak
802.11a/b/g/n)
PAGE 34

Keyboard Touch Pad
Light Sensor
PAGE 31

GMT G9931P1U
SYSTEM/VGA FAN
PAGE 27

SPI
(SYSTEM BIOS)
PAGE 33

ENE KBC
KB3926 C2
PAGE 33

Audio
IDT92HD75B2
PAGE 28

AUDIO Amplifier TPA6047A4
PAGE 29

Internal Micophones (MEMs)
PAGE 31

Combo Jack (Headphone/MIC)
PAGE 28

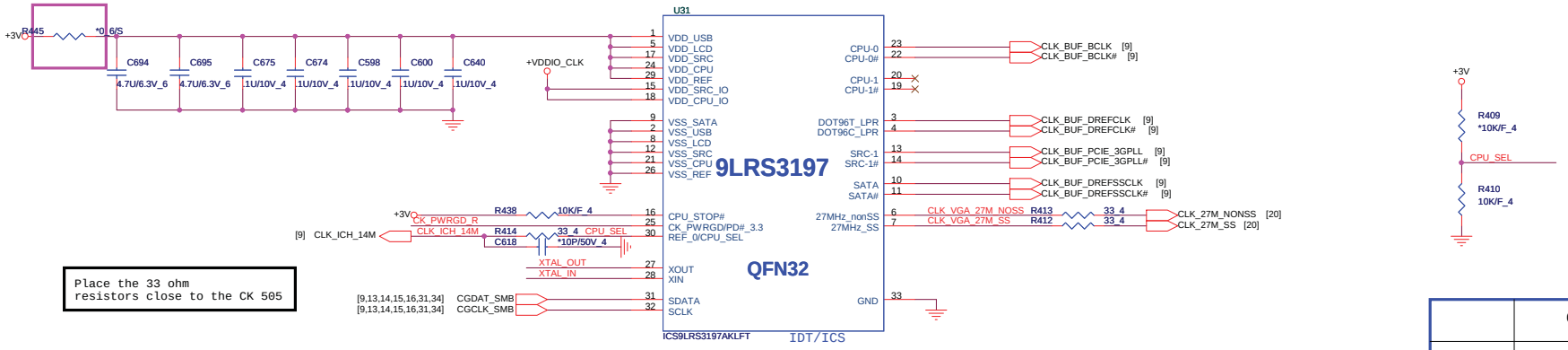
Jack to Speaker
PAGE 29

BATTERY SELECTOR PAGE 42
SYSTEM CHARGER(BQ24704) PAGE 41
SYSTEM POWER ISL6237IRZ-T PAGE 35
DDR III SMDDR_VTERM 1.8V/1.8VSUS(VT356/VT357) PAGE 39
VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 36
VGACORE RT8208 PAGE 38
CPU CORE VT1312M/VT1317 PAGE 37

NB5

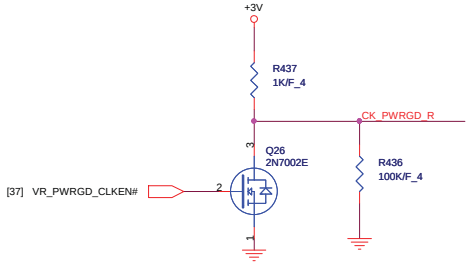
PROJECT : SP7
Quanta Computer Inc.

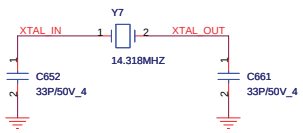
Size	Document Number	Rev
Custom	Block Diagram	1A
Date: Friday, July 10, 2009	Sheet 1 of 42	

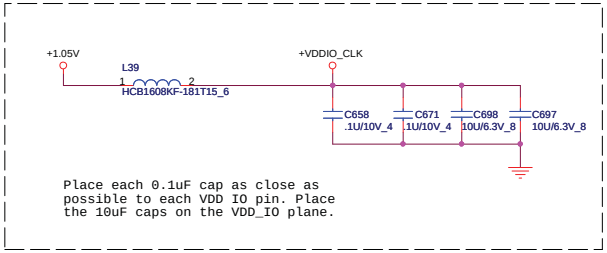


Place the 33 ohm resistors close to the CK 505

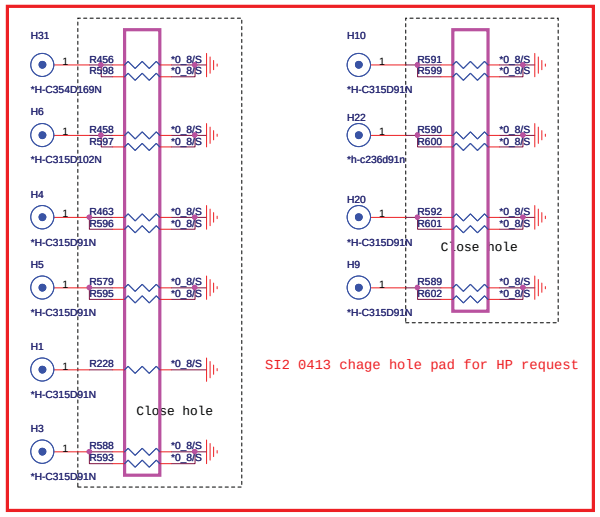
	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz



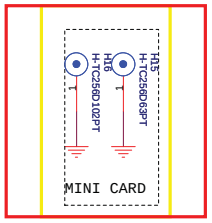




M/B Screw Hole



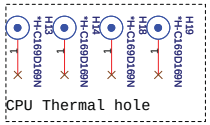
MINI CARD



SI 0223 change footprint

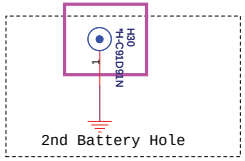
SI2 0413 change BOM

CPU Thermal hole

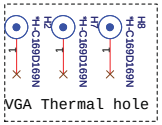


2nd Battery Hole

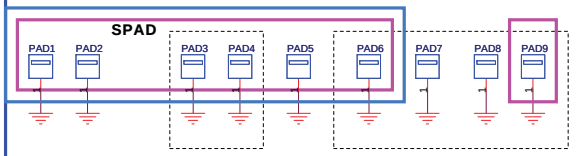
PV 0605 MODIFY



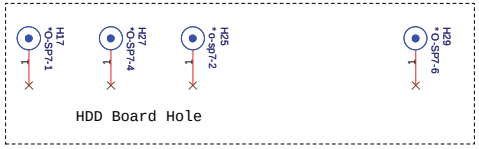
VGA Thermal hole

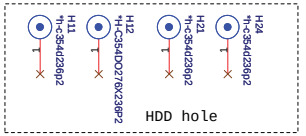


PV 0605 MODIFY PV 0605 MODIFY



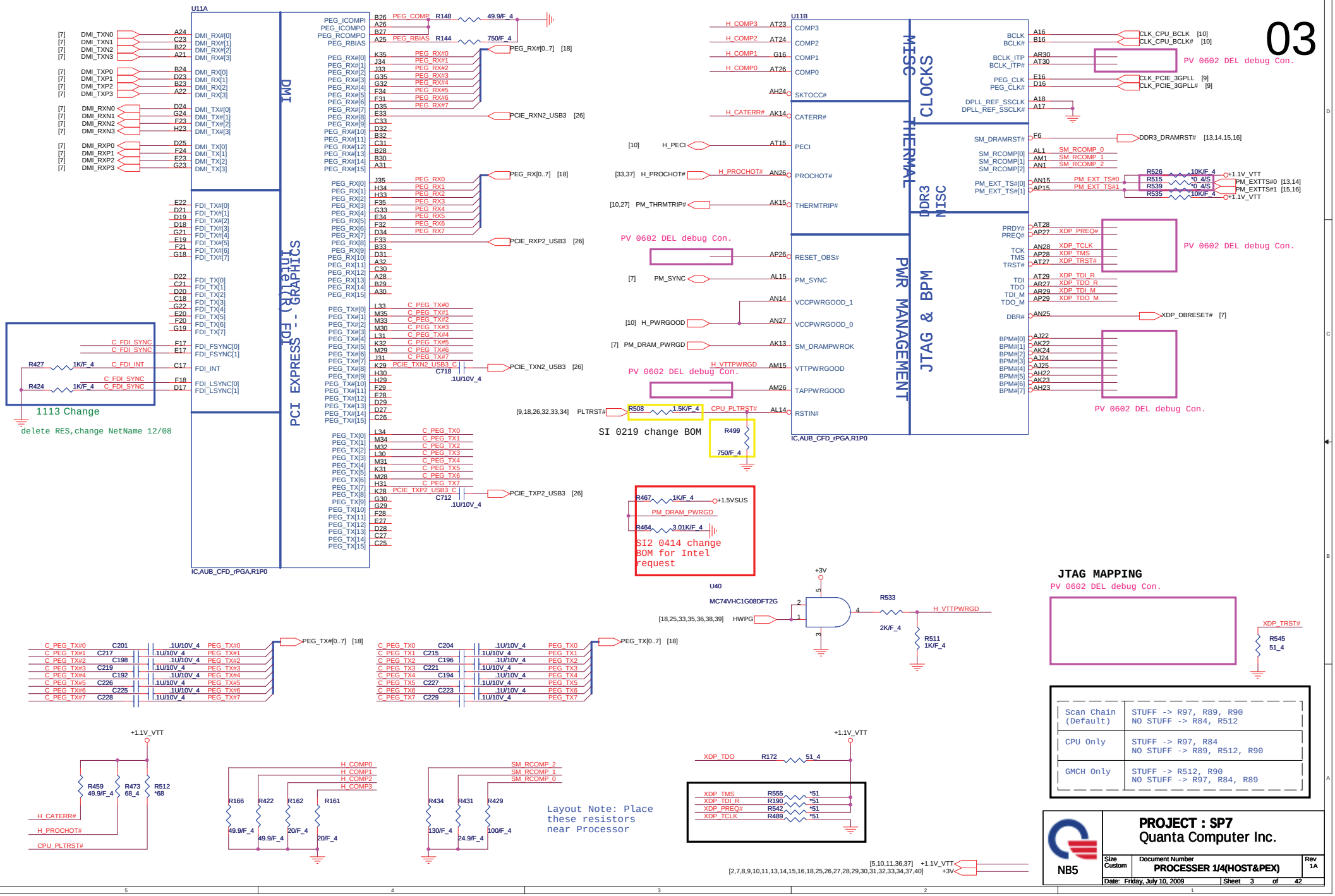
PV-2 0702 MODIFY





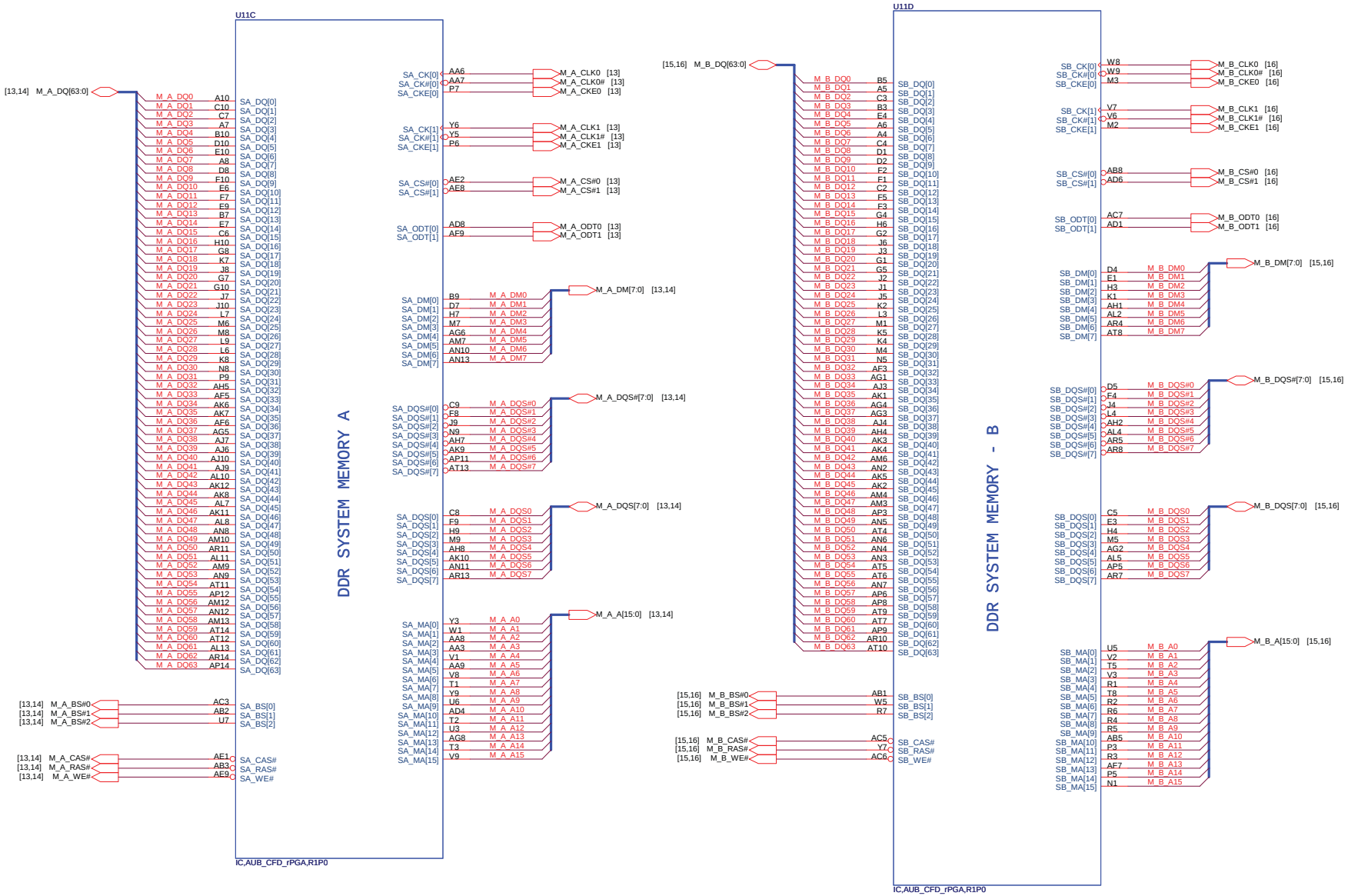
[3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,8,9,11,26,27,36,37] +1.05V

NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: CLOCK & Screw Holes	Rev: 1A
Date: Friday, July 10, 2009	Sheet 2 of 42	

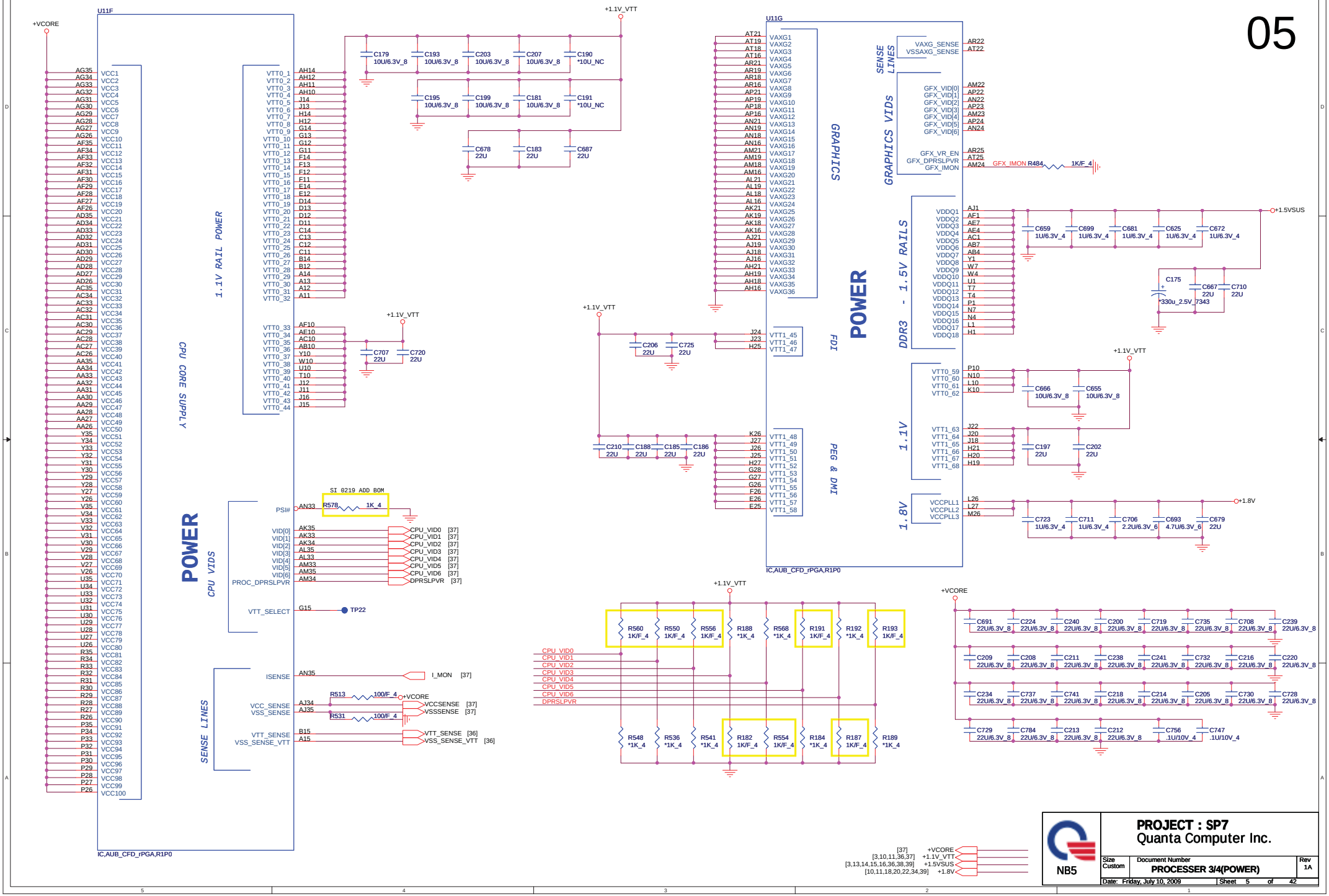

03
U11A
DMI
PCI EXPRESS - GRAPHICS
Intel(R) FDI
DMI_RX#[0]
DMI_RX#[1]
DMI_RX#[2]
DMI_RX#[3]
DMI_TX#[0]
DMI_TX#[1]
DMI_TX#[2]
DMI_TX#[3]
FDI_TX#[0]
FDI_TX#[1]
FDI_TX#[2]
FDI_TX#[3]
FDI_TX#[4]
FDI_TX#[5]
FDI_TX#[6]
FDI_TX#[7]
FDI_FSYNC[0]
FDI_FSYNC[1]
FDI_INT
FDI_LSYNC[0]
FDI_LSYNC[1]
PEG_RX#[0..7] [18]
PEG_TX#[0..7] [18]
PCIE_RXN2_USB3 [26]
PCIE_RXP2_USB3 [26]
PCIE_TXN2_USB3 [26]
PCIE_TXP2_USB3 [26]
IC,AUB_CFD_rPGA,R1P0
1113 Change
delete RES,change NetName 12/08
U11B
MISC
CLOCKS
THERMAL
DDR3 MISC
JTAG & BPM
PWR MANAGEMENT
COMP3
COMP2
COMP1
COMP0
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
RESET_OBS#
PM_SYNC
VCCPWRGOOD_1
VCCPWRGOOD_0
SM_DRAMPWROK
VTTPWRGOOD
TAPPWRGOOD
RSTIN#
BCLK
BCLK#
BCLK_ITP
BCLK_ITP#
PEG_CLK
PEG_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PM_EXT_TS#[0]
PM_EXT_TS#[1]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
CLK_CPU_BCLK [10]
CLK_CPU_BCLK# [10]
CLK_PCIE_3GPLL [9]
CLK_PCIE_3GPLL# [9]
DDR3_DRAMRST# [13,14,15,16]
PV 0602 DEL debug Con.
XDP_PREQ#
XDP_TCLK
XDP_TMS
XDP_TDI_R
XDP_TDO_R
XDP_TDI_M
XDP_TDO_M
XDP_DBRESET# [7]
IC,AUB_CFD_rPGA,R1P0
SI 0219 change BOM
SI2 0414 change BOM for Intel request
U40
MC74VHC1G08DFT2G
HWPG
JTAG MAPPING
XDP_TRST#
Scan Chain (Default) | STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only | STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only | STUFF -> R512, R90 NO STUFF -> R97, R84, R89
Layout Note: Place these resistors near Processor
PROJECT : SP7
Quanta Computer Inc.
NB5
Size Custom
Document Number PROCESSER 1/4(HOST&PEX)
Rev 1A
Date: Friday, July 10, 2009
Sheet 3 of 42

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

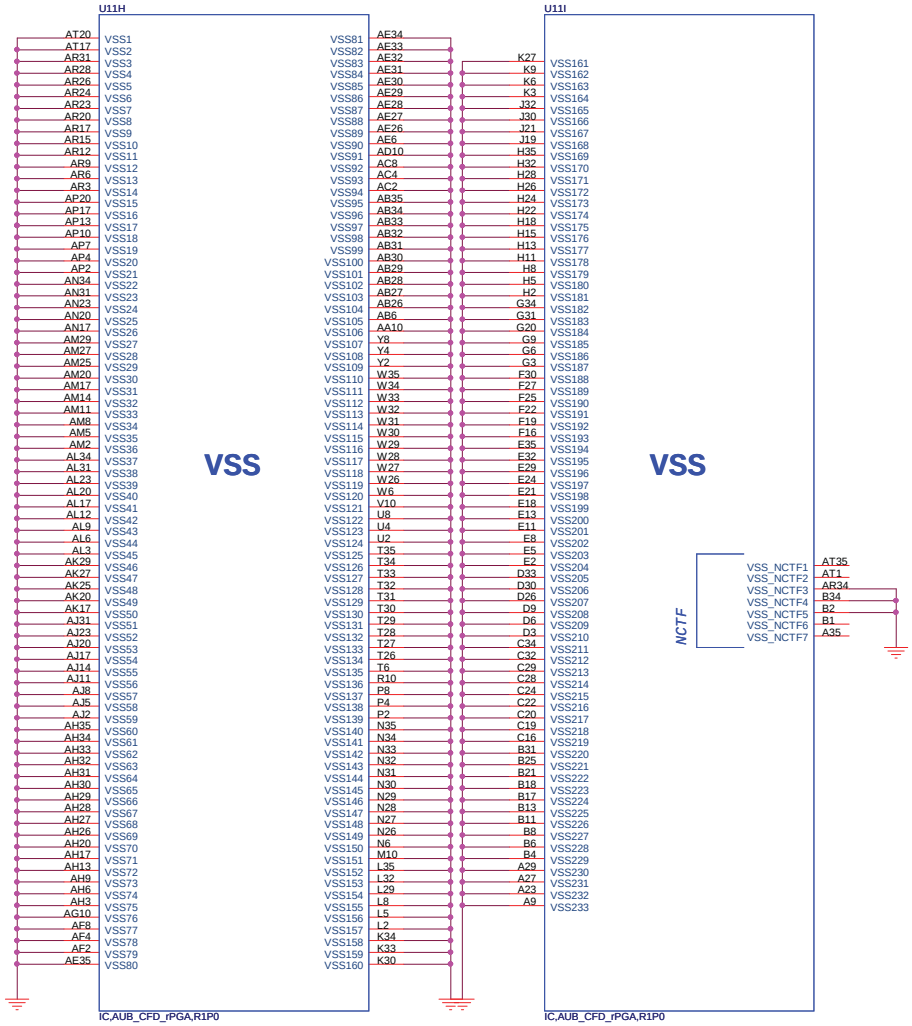
04



NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: PROCESSER 2/4(DDR)	Rev: 1A
Date: Friday, July 10, 2009	Sheet 4 of 42	

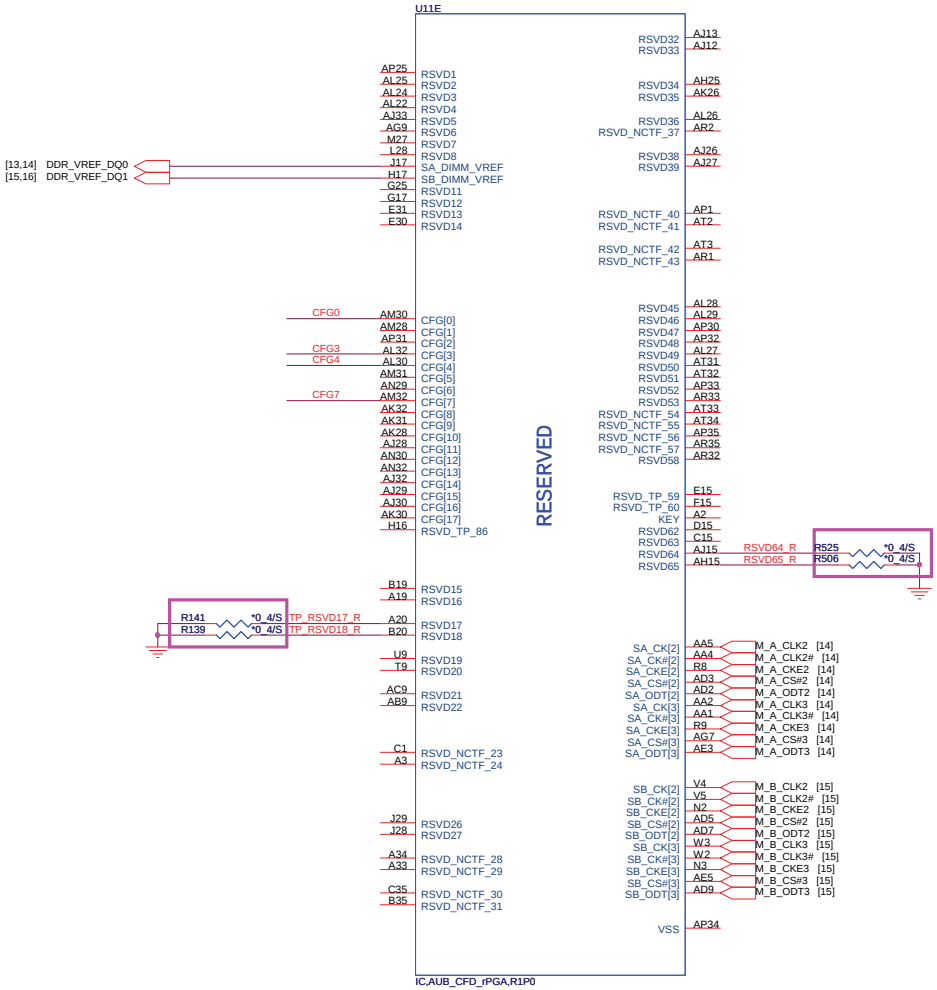

05
U11F
U11G
POWER
1.1V RAIL POWER
CPU CORE SUPPLY
CPU VIDS
SENSE LINES
GRAPHICS
GRAPHICS VIDS
SENSE LINES
DDR3 - 1.5V RAILS
1.1V
1.8V
FDI
PEG & DMI
IC,AUB_CFD_rPGA,R1P0
SI 0219 ADD BOM
+VCORE
+1.1V_VTT
+1.5VSUS
+1.8V
PSI#
VID[0]
VID[1]
VID[2]
VID[3]
VID[4]
VID[5]
VID[6]
PROC_DPRSLPVR
VTT_SELECT
ISENSE
VCC_SENSE
VSS_SENSE
VTT_SENSE
VSS_SENSE_VTT
I_MON [37]
VCCSENSE [37]
VSSSENSE [37]
VTT_SENSE [36]
VSS_SENSE_VTT [36]
GFX_IMON
PROJECT : SP7
Quanta Computer Inc.
NB5
PROCESSER 3/4(POWER)
Size Custom
Rev 1A
Date: Friday, July 10, 2009
Sheet 5 of 42

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

06



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

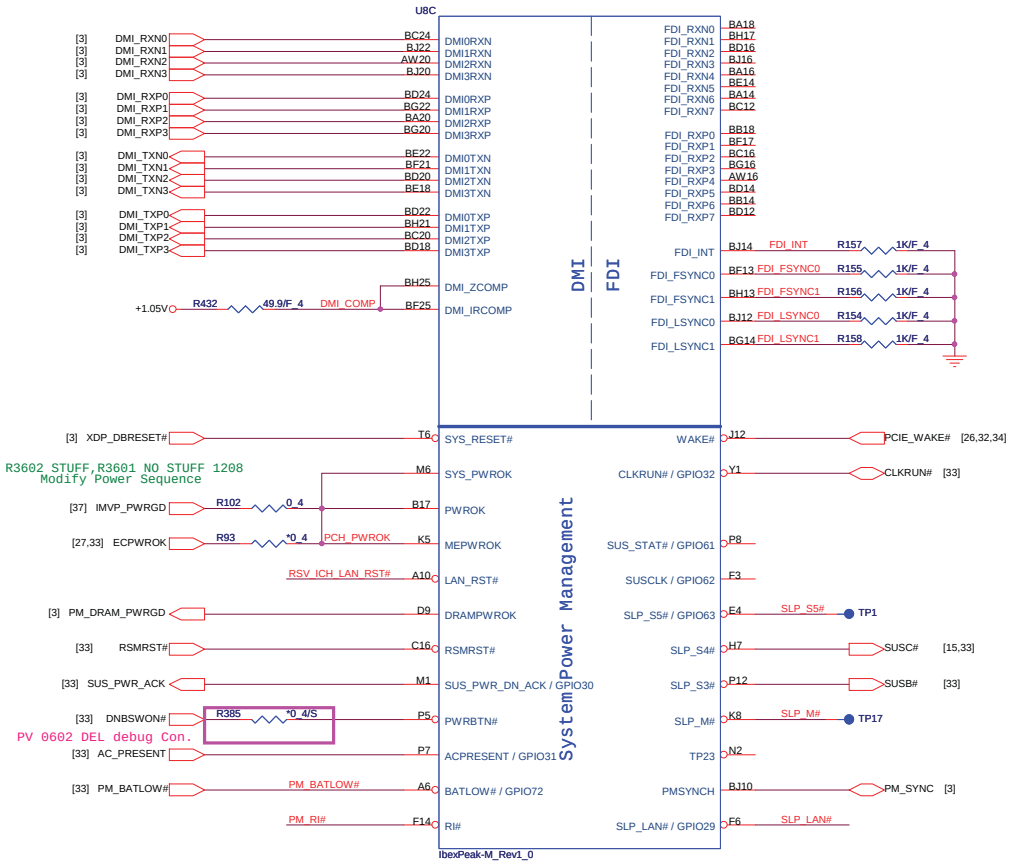
PROJECT : SP7
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	1A

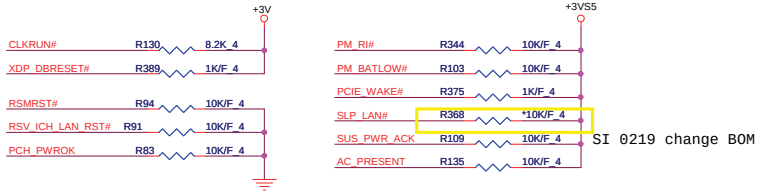
Date: Friday, July 10, 2009 | Sheet 6 of 42

IBEX PEAK-M (DMI,FDI,GPIO)



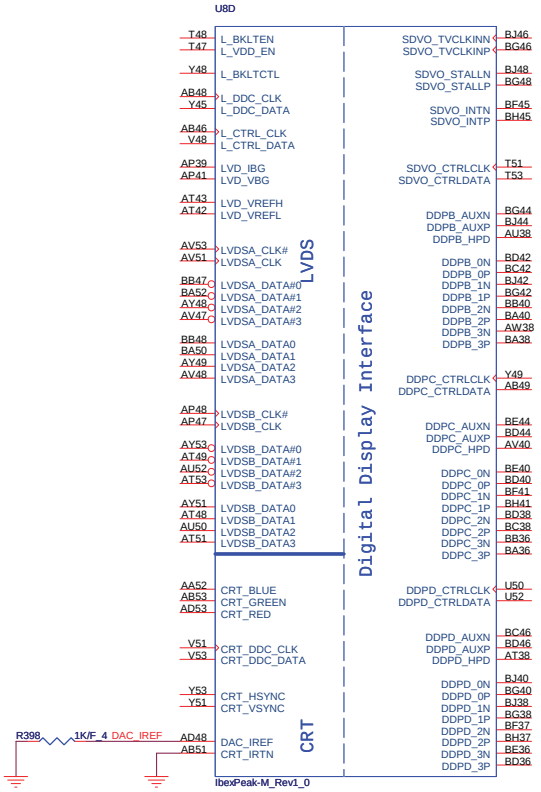
R3602 STUFF,R3601 NO STUFF 1208
Modify Power Sequence

PV 0602 DEL debug Con.



SI 0219 change BOM

IBEX PEAK-M (LVDS,DDI)



Display port B
Display port C
Display port D
SDVO

[2,8,9,11,26,27,36,37] +1.05V
[2,3,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[9,10,11,25,40] +3VS5

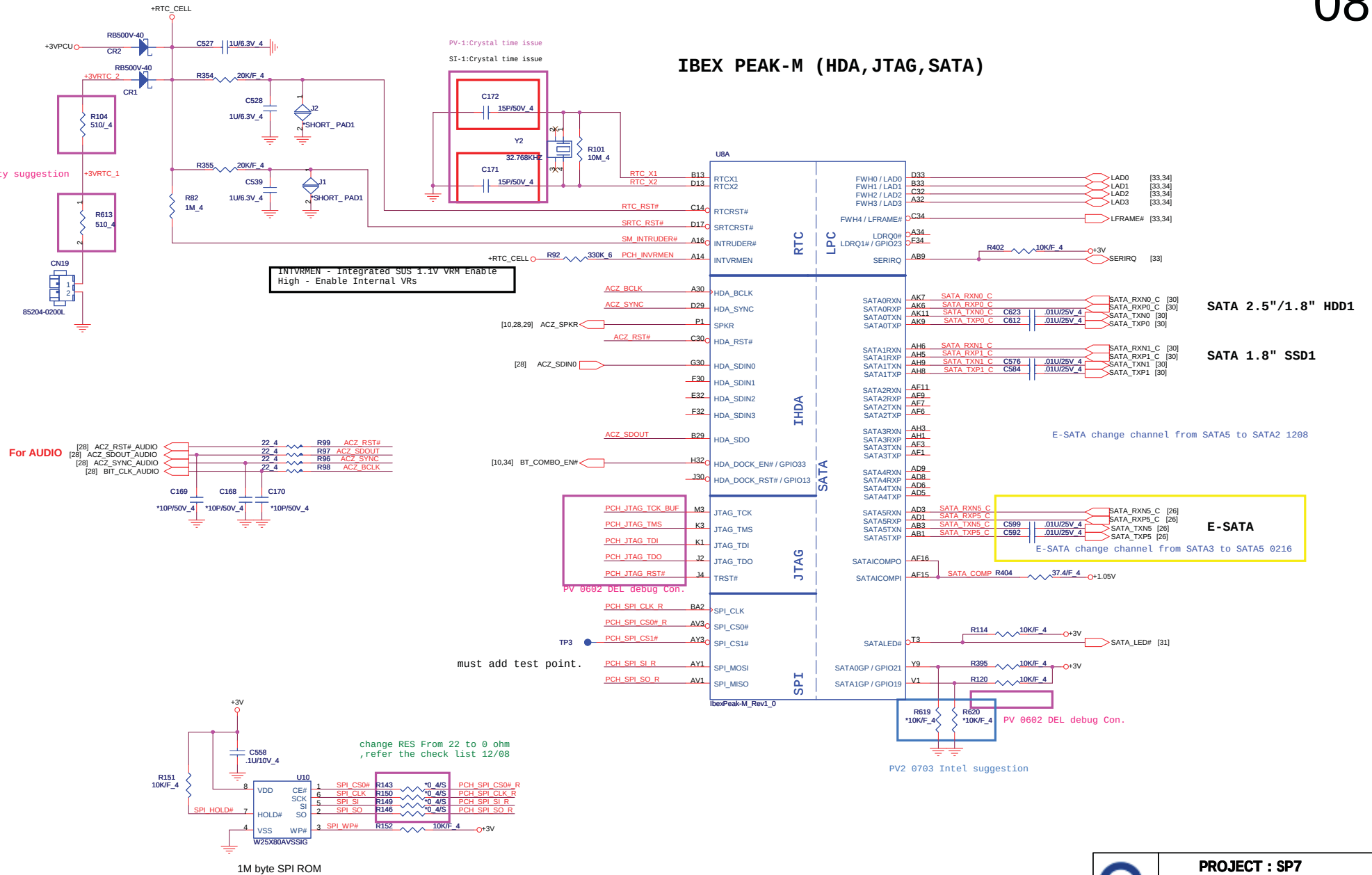
NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI,PM,VIDEO)	1A

Date: Friday, July 10, 2009 | Sheet 7 of 42

IBEX PEAK-M (HDA,JTAG,SATA)

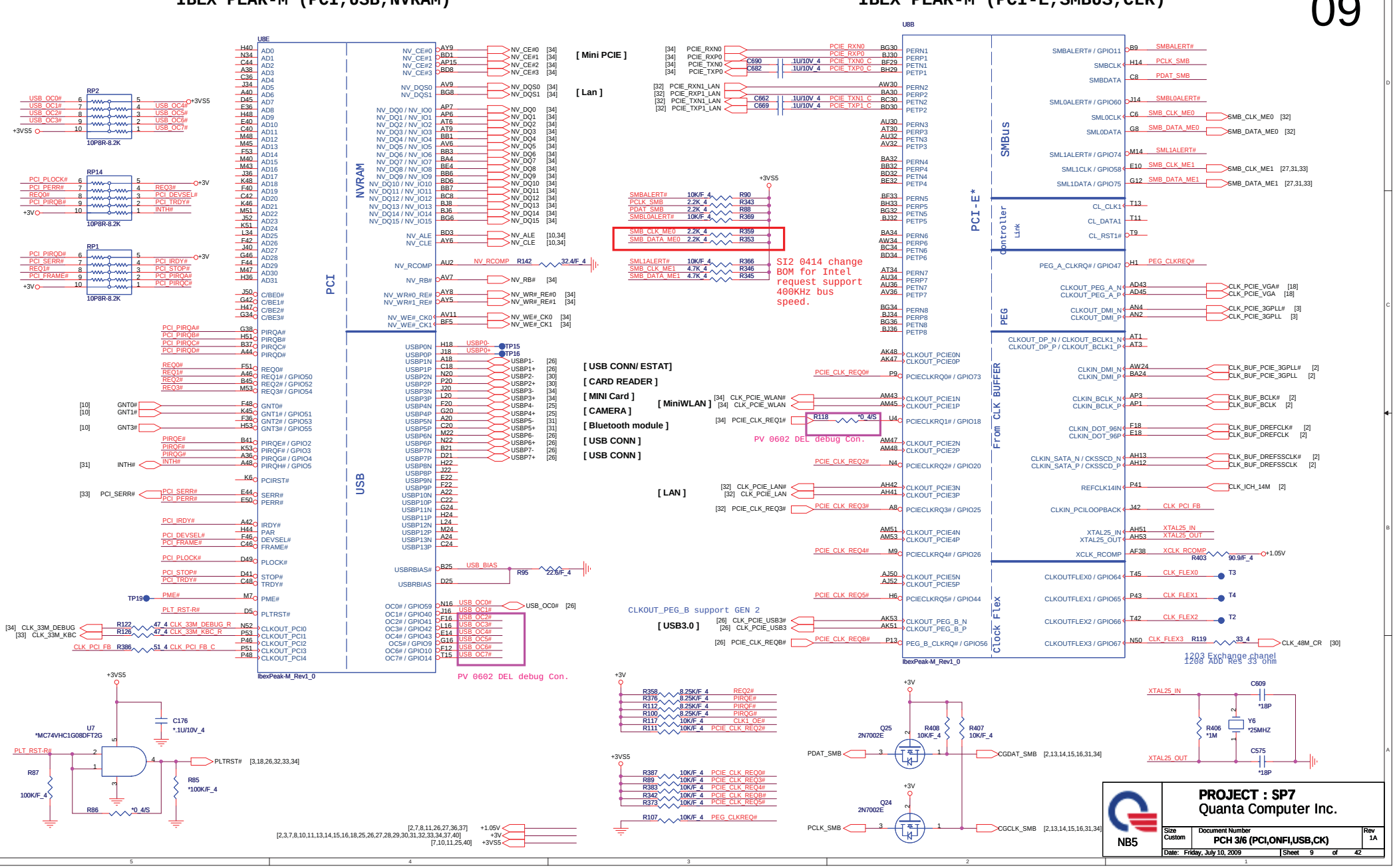


NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: PCH 2/6 (SATA,HDA,LPC)	Rev: 1A
Date: Friday, July 10, 2009	Sheet 8 of 42	

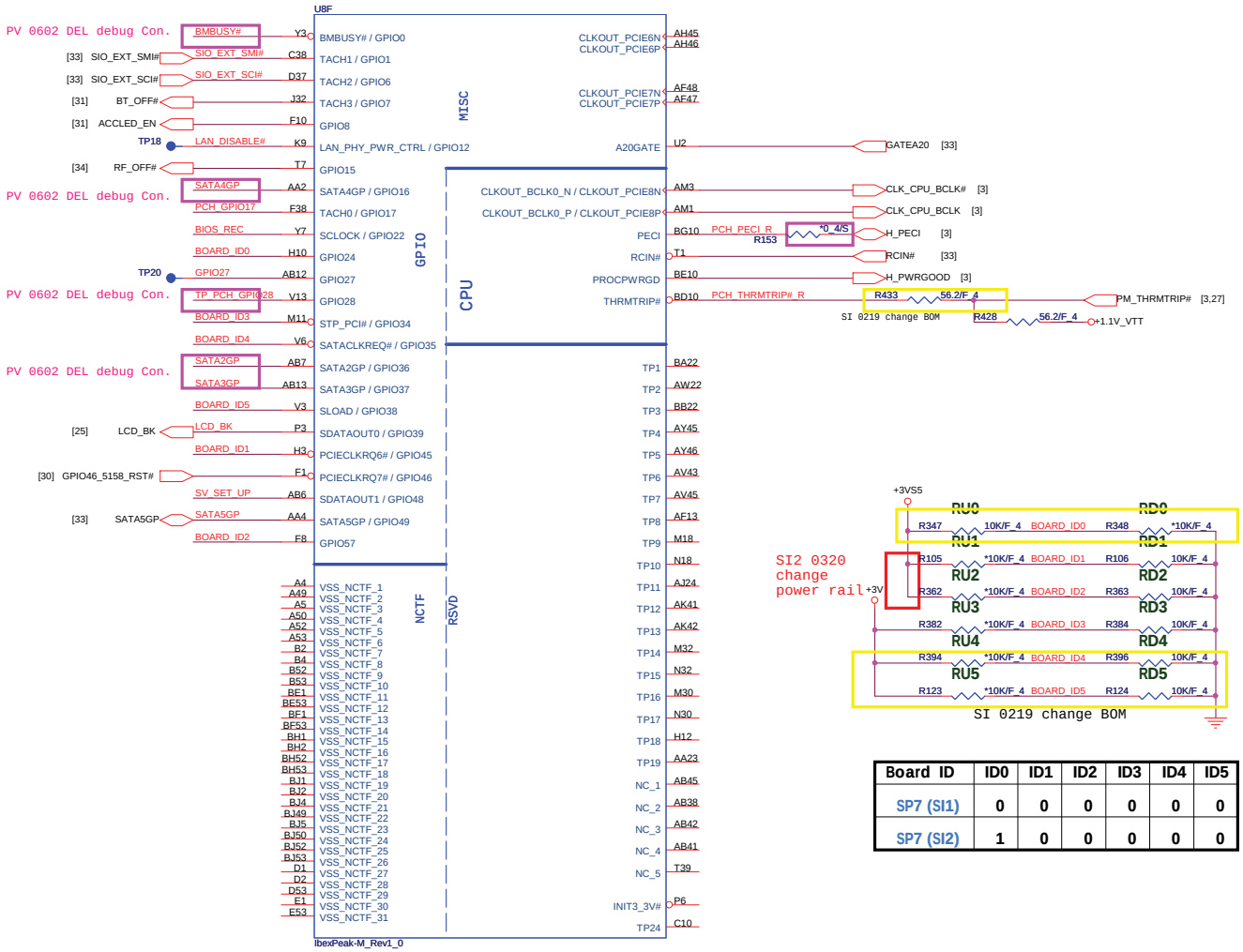
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

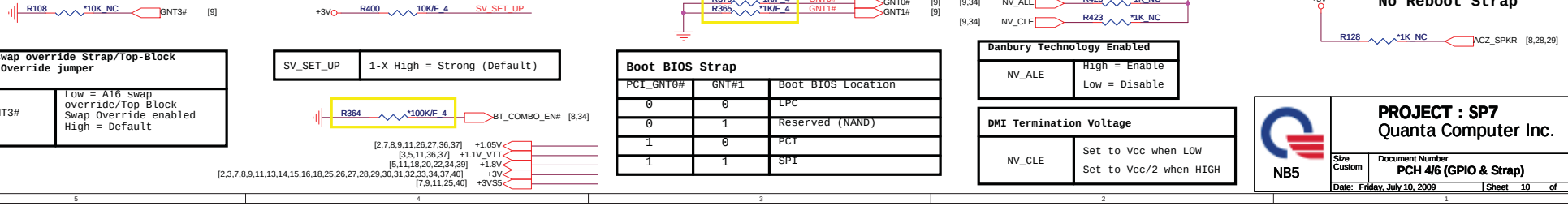
09



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



Board ID	ID0	ID1	ID2	ID3	ID4	ID5
SP7 (SI1)	0	0	0	0	0	0
SP7 (SI2)	1	0	0	0	0	0



No Reboot Strap

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP	1-X High = Strong (Default)

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

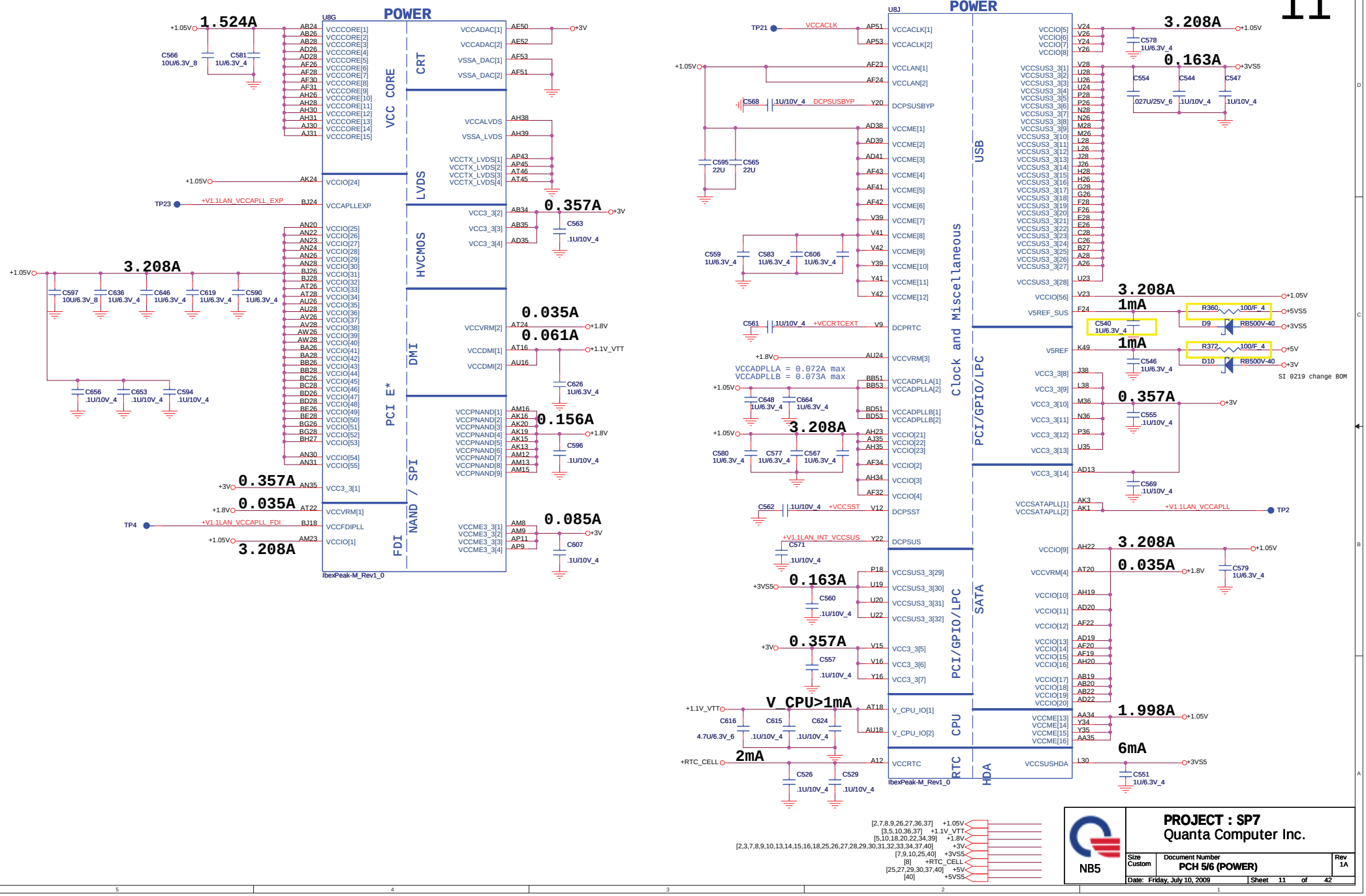
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

NB5

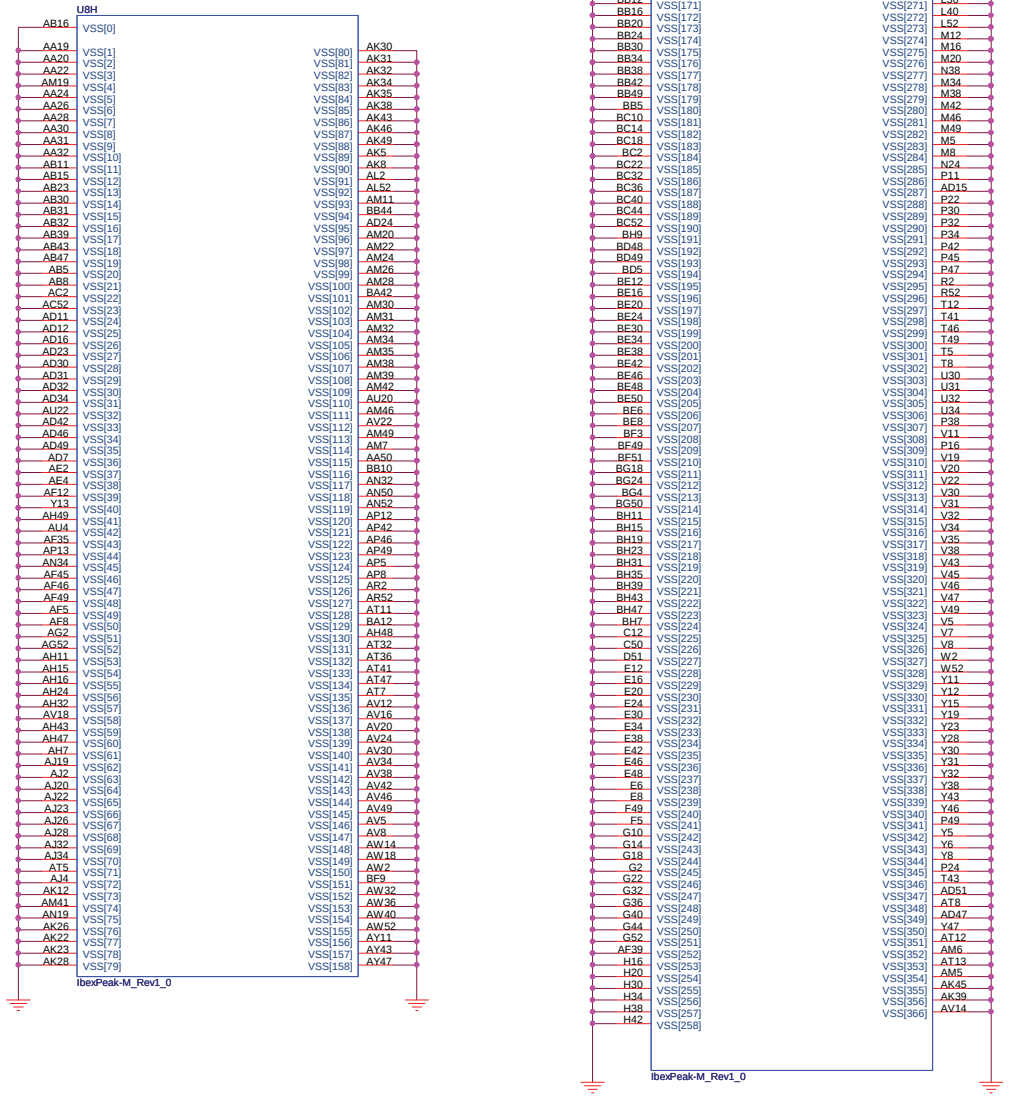
PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO & Strap)	1A

Date: Friday, July 10, 2009 | Sheet 10 of 42


POWER
U8G
1.524A
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
0.357A
0.035A
0.061A
0.156A
0.085A
3.208A
0.163A
V_CPU>1mA
2mA
ibexPeak-M_Rev1_0
POWER
U8J
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
3.208A
0.163A
0.357A
1mA
1mA
0.035A
1.998A
6mA
SI 0219 change BOM
PROJECT : SP7
Quanta Computer Inc.
NB5
PCH 5/6 (POWER)
Rev 1A
Date: Friday, July 10, 2009
Sheet 11 of 42

IBEX PEAK-M (GND)



Move to Page 37

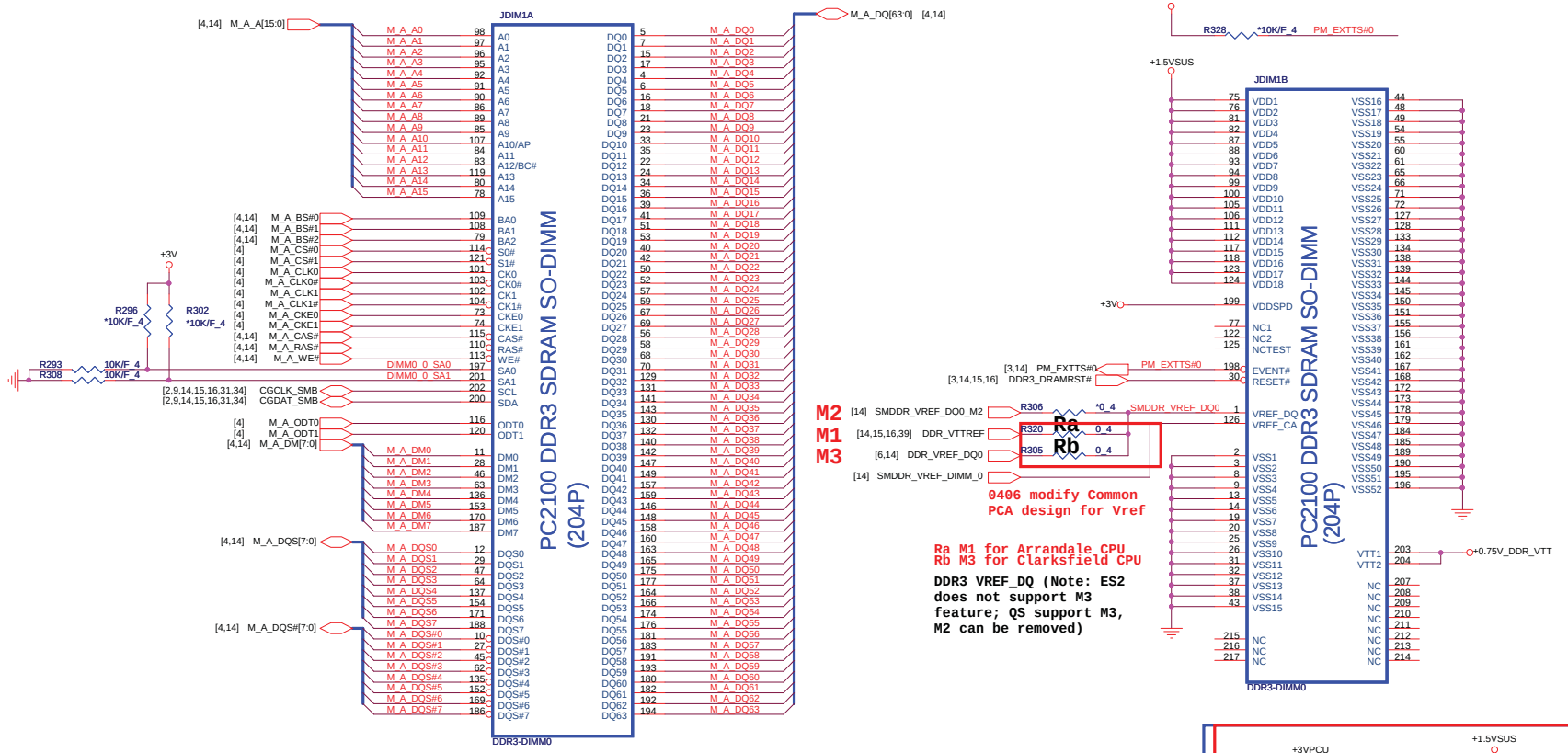
NB5

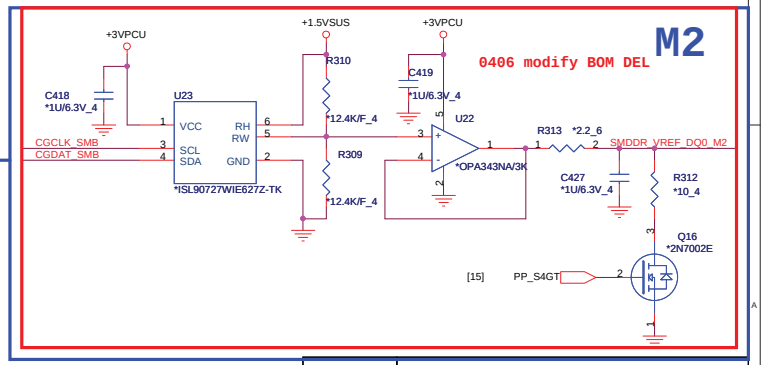
PROJECT : SP7
Quanta Computer Inc.

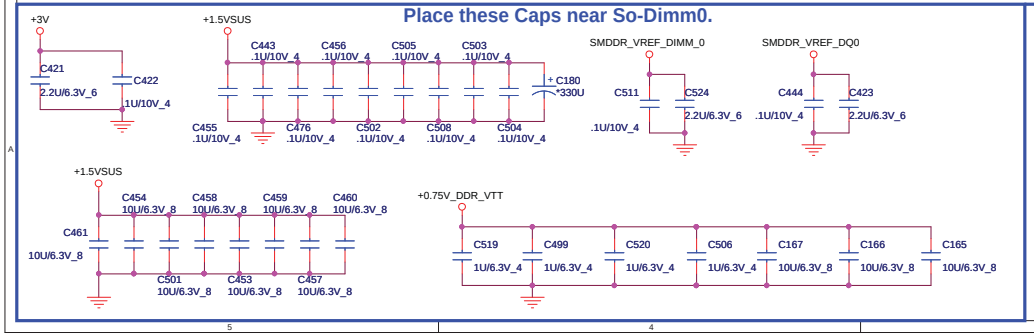
Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

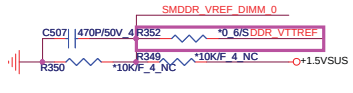
Date: Friday, July 10, 2009 | Sheet 12 of 42

DDR3 -SODIMM 1 A0



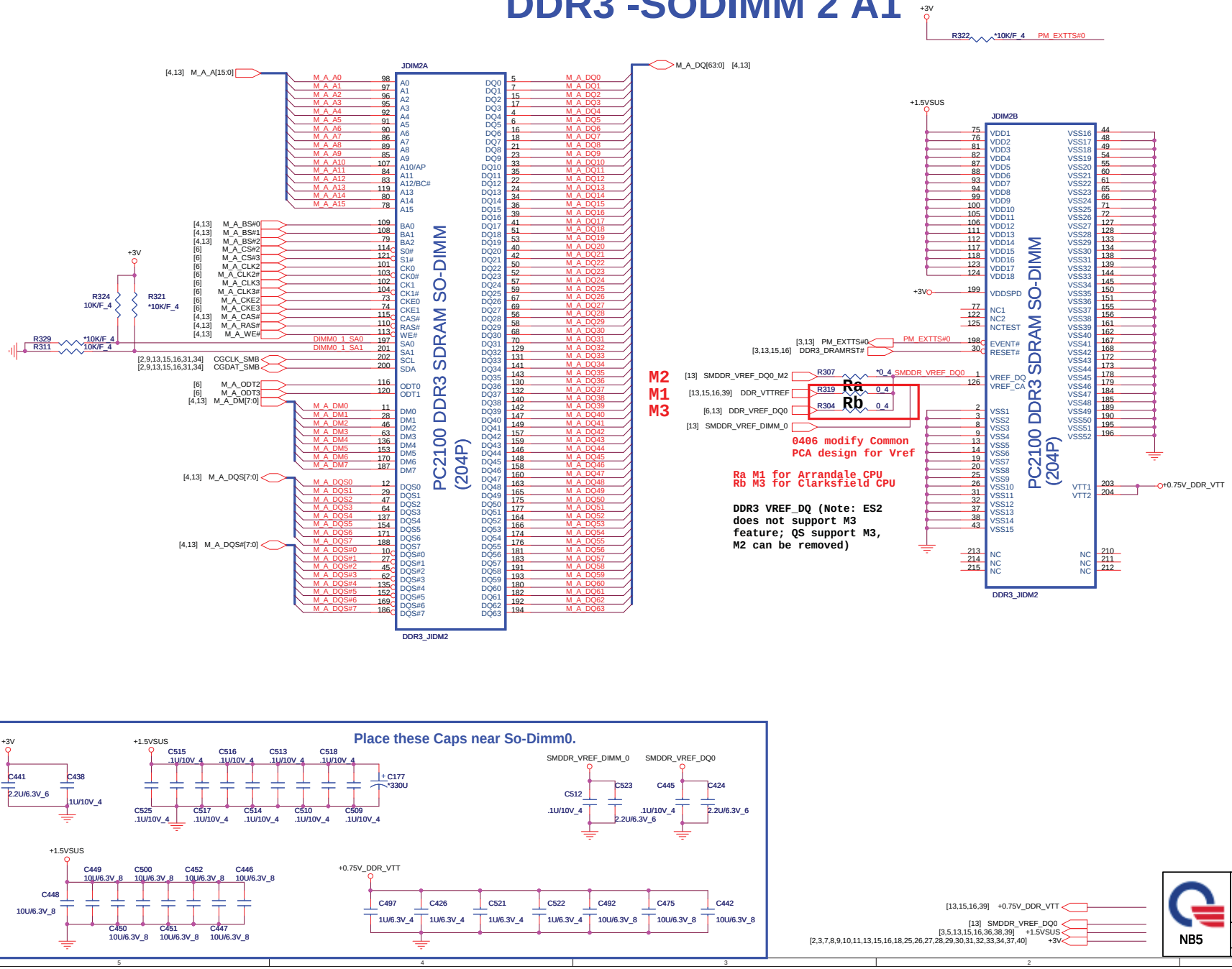






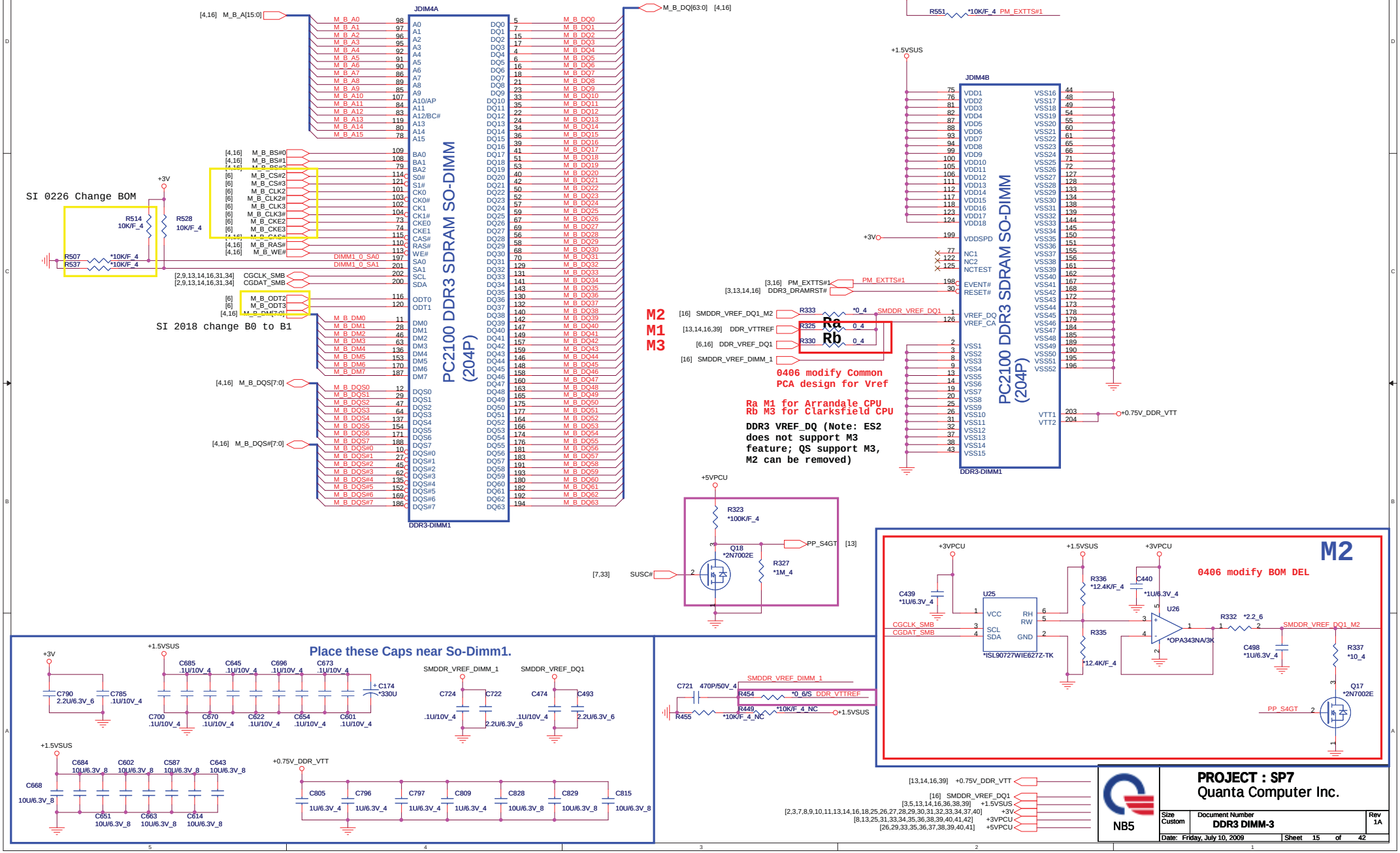
PROJECT : SP7 Quanta Computer Inc.			
NB5	Size Custom	Document Number DDR3 DIMM-1	Rev 1A
	Date: Friday, July 10, 2009	Sheet 13 of 42	

DDR3 -SODIMM 2 A1

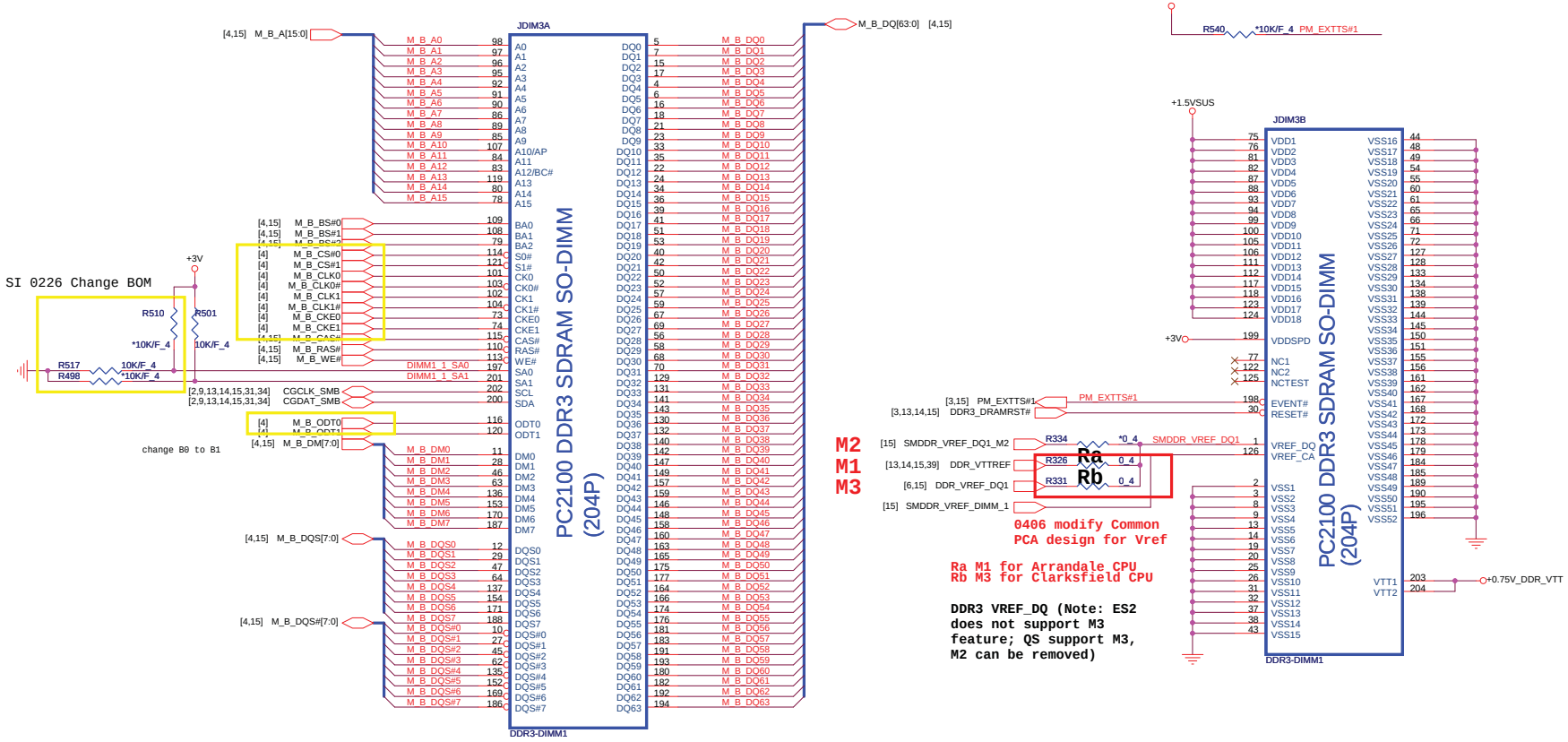


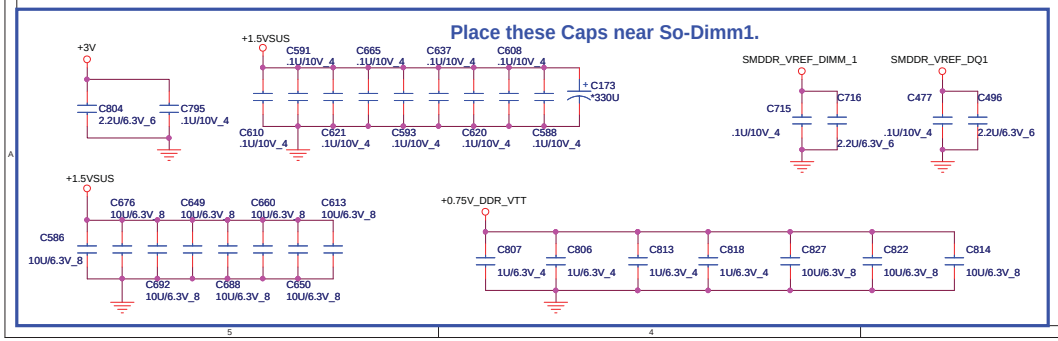
PROJECT : SP7	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: DDR3 DIMM-2
Rev: 1A	
Date: Friday, July 10, 2009	Sheet 14 of 42

DDR3 -SODIMM 3 B1



DDR3 -SODIMM 4 B0





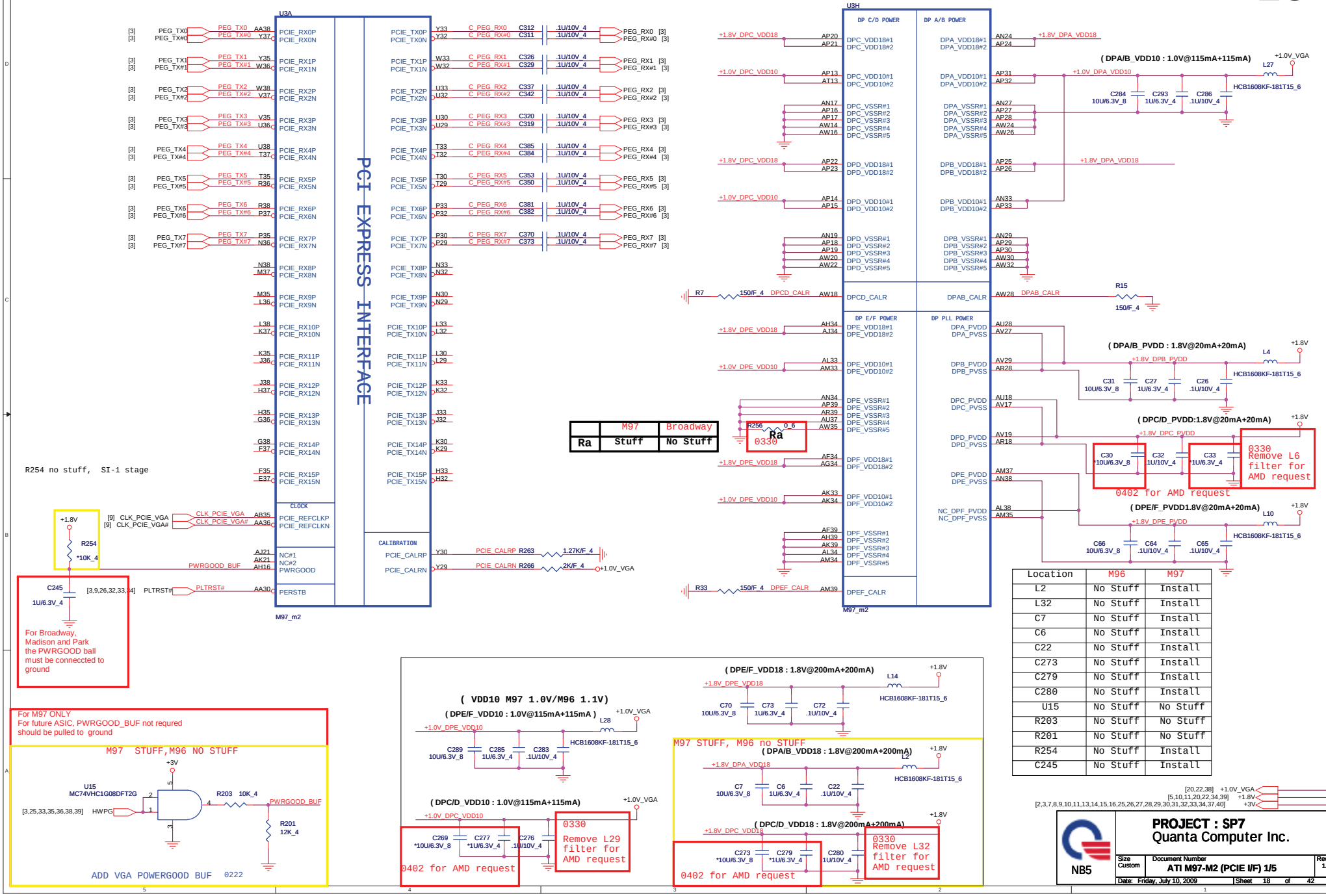
NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM-4	Rev: 1A
Date: Friday, July 10, 2009	Sheet 16 of 42	

[2,7,8,9,11,26,27,36,37] +1.05V
[3,5,10,11,36,37] +1.1V_VTT
[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,9,10,11,25,40] +3VS5

NB5

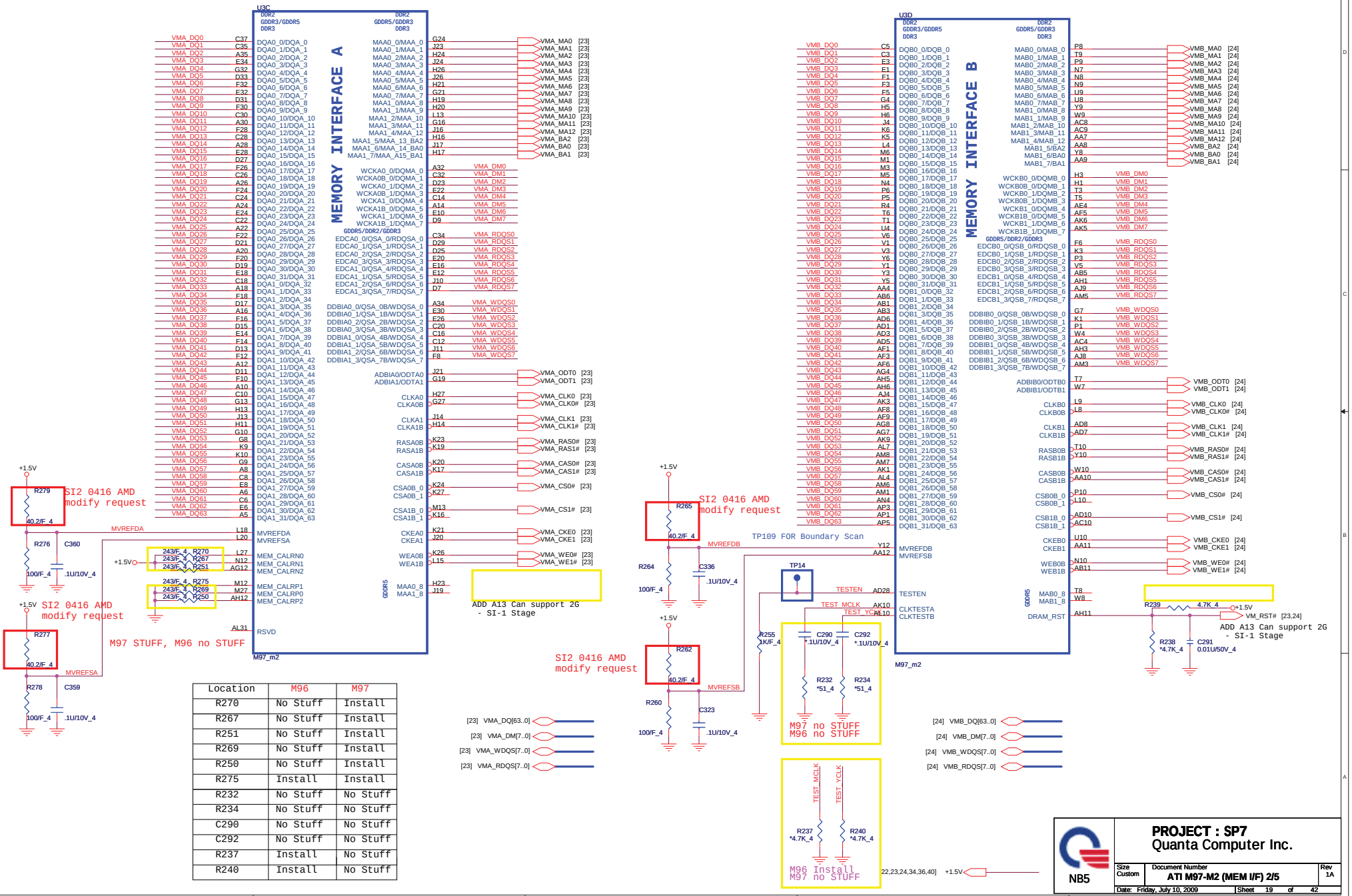
PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	XDP	1A
Date: Friday, July 10, 2009	Sheet 17 of 42	

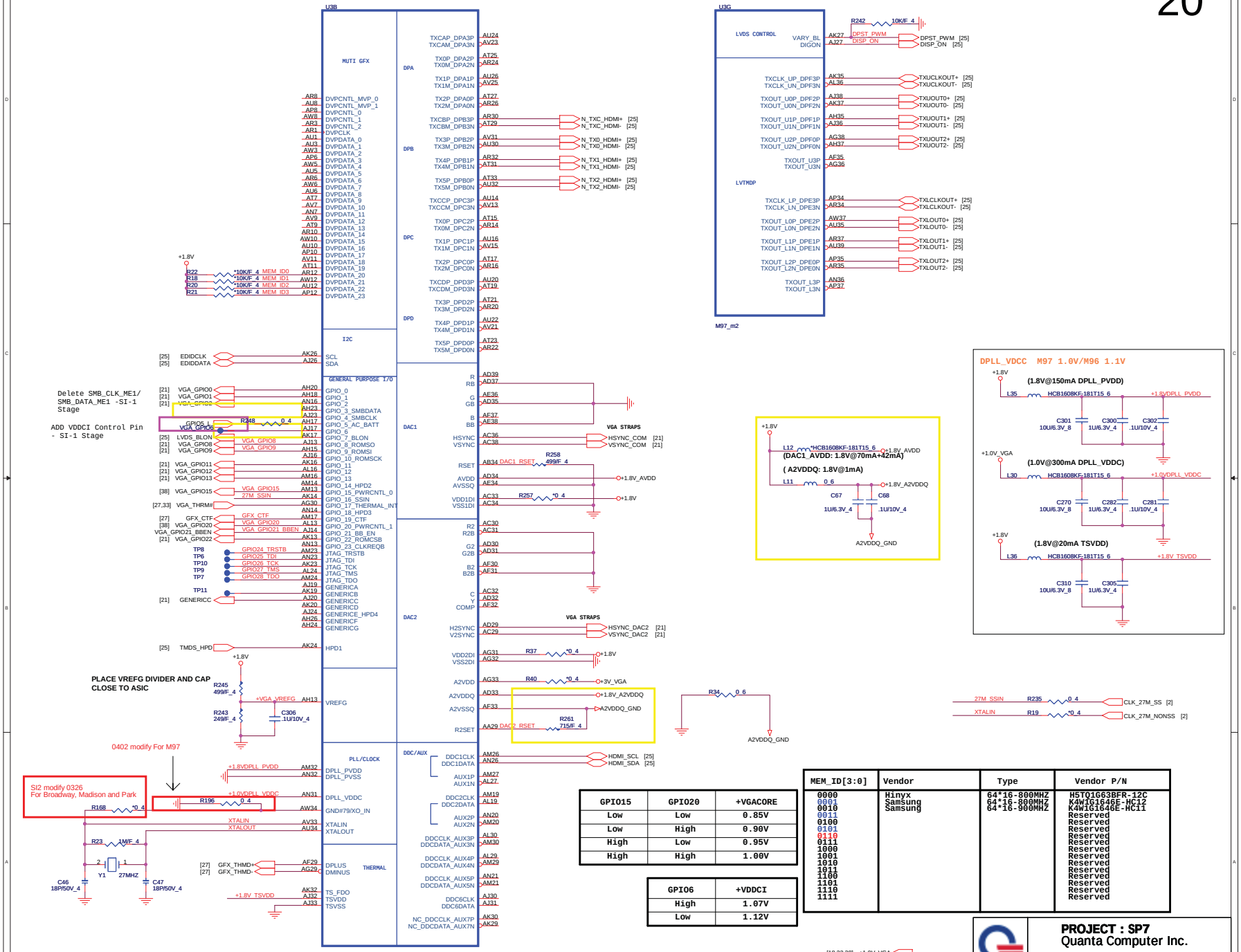


	M97	Broadway
Ra	Stuff	No Stuff

Location	M96	M97
L2	No Stuff	Install
L32	No Stuff	Install
C7	No Stuff	Install
C6	No Stuff	Install
C22	No Stuff	Install
C273	No Stuff	Install
C279	No Stuff	Install
C280	No Stuff	Install
U15	No Stuff	No Stuff
R203	No Stuff	No Stuff
R201	No Stuff	No Stuff
R254	No Stuff	Install
C245	No Stuff	Install



Location	M96	M97
R270	No Stuff	Install
R267	No Stuff	Install
R251	No Stuff	Install
R269	No Stuff	Install
R250	No Stuff	Install
R275	Install	Install
R232	No Stuff	No Stuff
R234	No Stuff	No Stuff
C290	No Stuff	No Stuff
C292	No Stuff	No Stuff
R237	Install	No Stuff
R240	Install	No Stuff


U3B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
PLL/CLOCK
THERMAL
DDC/AUX
M97_m2
U3G
LVDS CONTROL
LVTMDP
M97_m2
DPLL_VDCC M97 1.0V/M96 1.1V
(1.8V@150mA DPLL_PVDD)
(1.0V@300mA DPLL_VDDC)
(1.8V@20mA TSVDD)
(A2VDDQ: 1.8V@1mA)
(DAC1_AVDD: 1.8V@70mA+42mA)
VGA STRAPS
PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC
0402 modify For M97
SI2 modify 0326
For Broadway, Madison and Park
Delete SMB_CLK_ME1/ SMB_DATA_ME1 -SI-1 Stage
ADD VDDCI Control Pin - SI-1 Stage
GPIO15 GPIO20 +VGACORE
Low Low 0.85V
Low High 0.90V
High Low 0.95V
High High 1.00V
GPIO6 +VDDCI
High 1.07V
Low 1.12V
MEM_ID[3:0] Vendor Type Vendor P/N
0000 Hinyx 64*16-800MHZ H5TQ1G63BFR-12C
0001 Samsung 64*16-800MHZ K4W1G1646E-HC12
0010 Samsung 64*16-900MHZ K4W1G1646E-HC11
0011 Reserved
0100 Reserved
0101 Reserved
0110 Reserved
0111 Reserved
1000 Reserved
1001 Reserved
1010 Reserved
1011 Reserved
1100 Reserved
1101 Reserved
1110 Reserved
1111 Reserved
PROJECT : SP7
Quanta Computer Inc.
NB5
ATI M97-M2 (DISPLAY) 3/5
Size Custom
Rev 1A
Date: Friday, July 10, 2009
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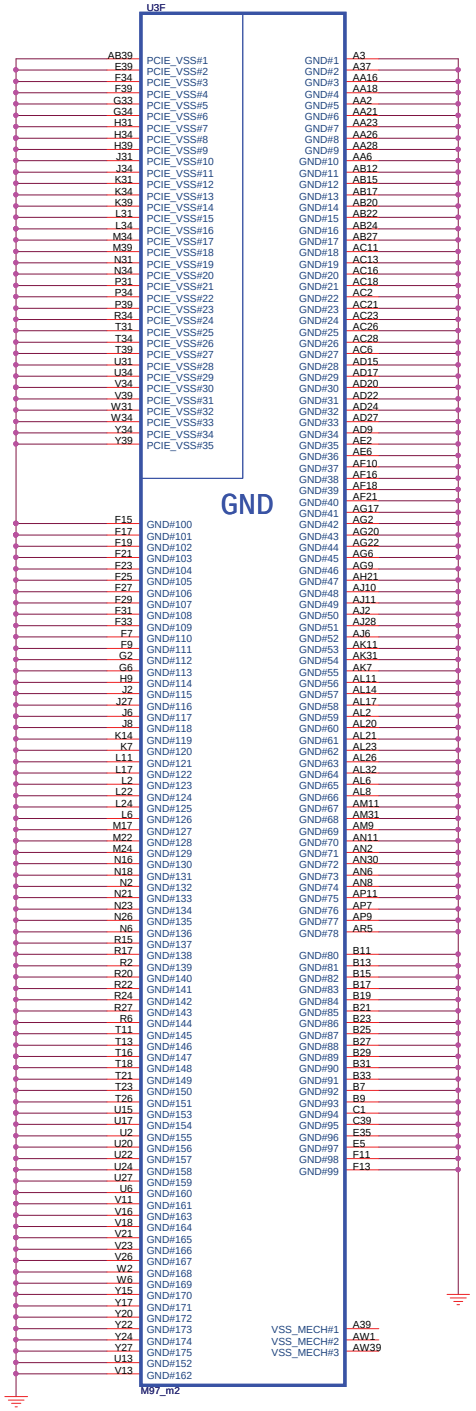
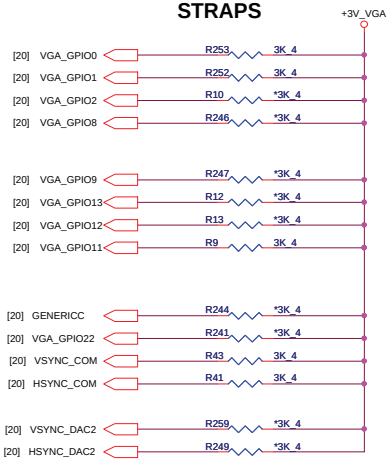


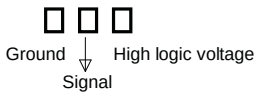
STRAPS



Location	M96	M97
pull-up for straps	10K (CS31002FB26)	3K (CS23002FB11)

Overlap pads to save space and to prevent assembly of both resistors.

Layout



Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIO9,13,12,11 (config 3,2,1,0): a> If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM Type: b> If BIOS_ROM_EN = 0, then Config[3:0] defines the Aperture size:Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYNC		0
AUD(1)	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 ?No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VSYNC_DAC2	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
HSYNC_DAC2	H2SYNC		0
	GENERICC		0

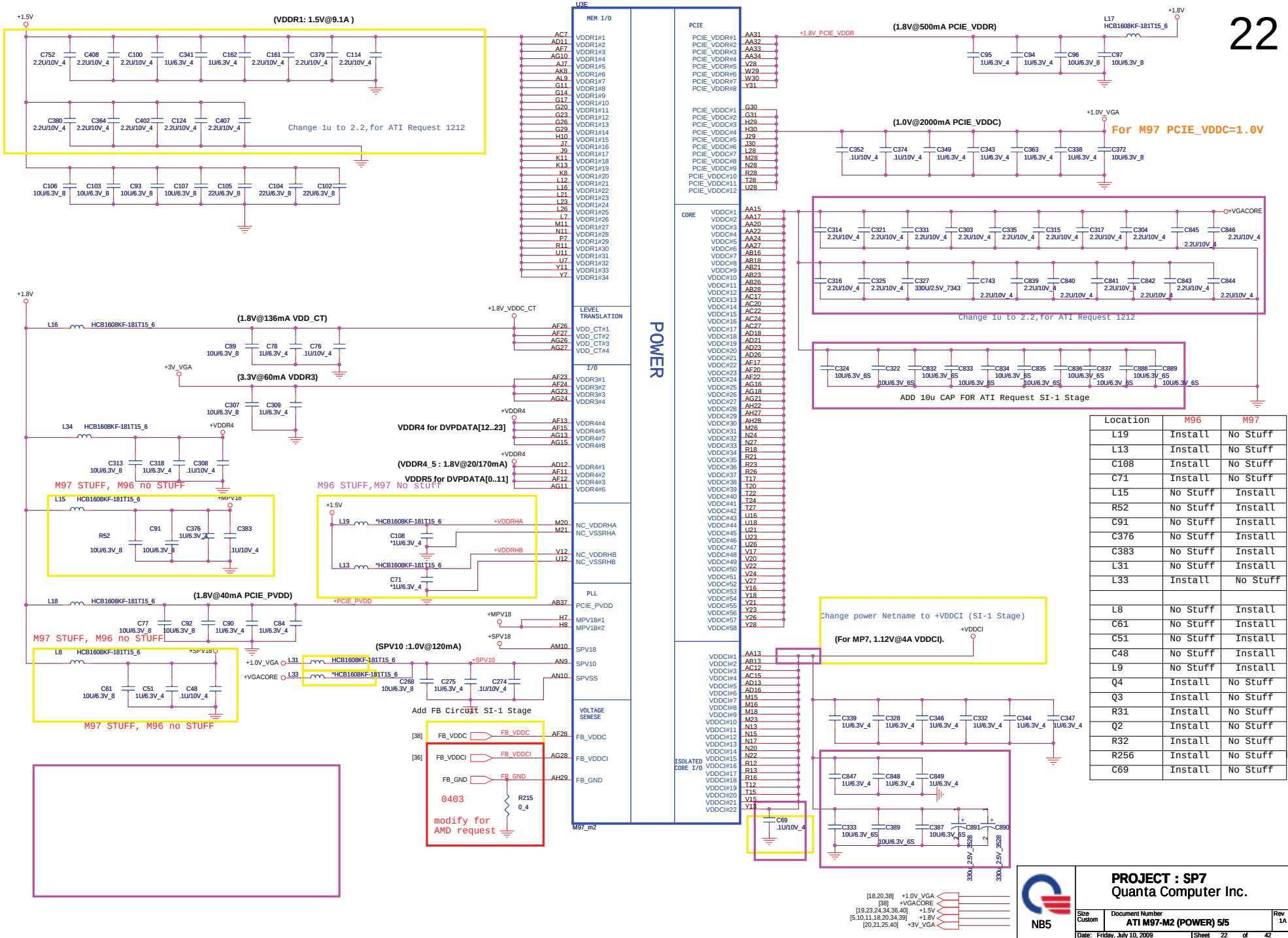
[20,22,25,40] +3V_VGA

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97(GND&Str&Ther)4/5	1A

Date: Friday, July 10, 2009 Sheet 21 of 42



Location	M96	M97
L19	Install	No Stuff
L13	Install	No Stuff
C108	Install	No Stuff
C71	Install	No Stuff
L15	No Stuff	Install
R52	No Stuff	Install
C91	No Stuff	Install
C376	No Stuff	Install
C383	No Stuff	Install
L31	No Stuff	Install
L33	Install	No Stuff
L8	No Stuff	Install
C61	No Stuff	Install
C51	No Stuff	Install
C48	No Stuff	Install
L9	No Stuff	Install
Q4	Install	No Stuff
Q3	Install	No Stuff
R31	Install	No Stuff
Q2	Install	No Stuff
R32	Install	No Stuff
R256	Install	No Stuff
C69	Install	No Stuff

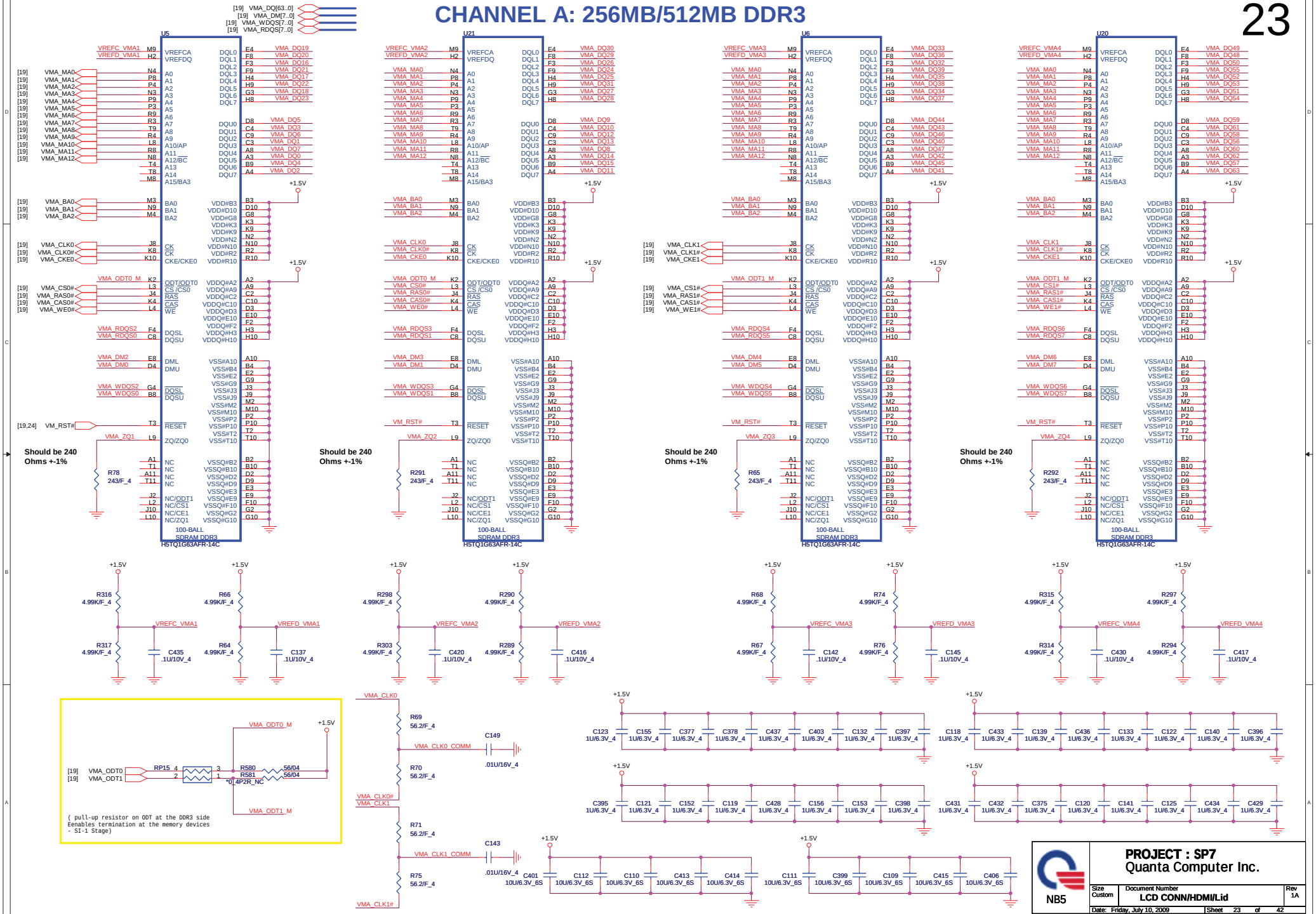
[18,20,38] +1.0V_VGA
[38] +VGACORE
[19,23,24,34,36,40] +1.5V
[5,10,11,18,20,34,39] +1.8V
[20,21,25,40] +3V_VGA

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97-M2 (POWER) 5/5	1A
Date: Friday, July 10, 2009	Sheet 22 of 42	

CHANNEL A: 256MB/512MB DDR3



PROJECT : SP7	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: LCD CONN/HDMI/Lid
Rev: 1A	
Date: Friday, July 10, 2009	Sheet 23 of 42

CHANNEL B: 256MB/512MB DDR3

[19] VMB_DQ[63..0]
[19] VMB_DM[7..0]
[19] VMB_WDQS[7..0]
[19] VMB_RDQS[7..0]

U4 / U19 / U2 / U18 — H5TQ1G63AFR-14C — 100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R50 243/F_4 (U4) · R61 243/F_4 (U19) · R29 243/F_4 (U2) · R51 243/F_4 (U18)

R272 4.99K/F_4 · R271 4.99K/F_4 · VREFC_VMB1 · C361 .1U/10V_4
R59 4.99K/F_4 · R60 4.99K/F_4 · VREFD_VMB1 · C116 .1U/10V_4
R62 4.99K/F_4 · R63 4.99K/F_4 · VREFC_VMB2 · C115 .1U/10V_4
R274 4.99K/F_4 · R273 4.99K/F_4 · VREFD_VMB2 · C362 .1U/10V_4
R30 4.99K/F_4 · R24 4.99K/F_4 · VREFC_VMB3 · C62 .1U/10V_4
R48 4.99K/F_4 · R49 4.99K/F_4 · VREFD_VMB3 · C83 .1U/10V_4
R38 4.99K/F_4 · R35 4.99K/F_4 · VREFC_VMB4 · C75 .1U/10V_4
R25 4.99K/F_4 · R26 4.99K/F_4 · VREFD_VMB4 · C56 .1U/10V_4

RP16 4/2/3/1 · R582 56/04 · R583 56/04 · *0_4P2R_NC

(pull-up resistor on ODT at the DDR3 side
Eenables termination at the memory devices
- SI-1 Stage)

R282 56.2/F_4 · C390 .01U/16V_4 · R281 56.2/F_4 · R27 56.2/F_4 · C57 .01U/16V_4 · R28 56.2/F_4

C85 C81 C368 C86 C80 C53 C113 C87 1U/6.3V_4
C358 C369 C88 C82 C98 C79 C297 C356 1U/6.3V_4
C299 C101 C367 C348 C99 C60 C117 C298 1U/6.3V_4
C357 C366 C355 C59 C55 C54 C52 C58 1U/6.3V_4
C296 C394 C393 C388 C392 C391 C63 C294 C386 C295 10U/6.3V_6S

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/HDMI/Lid	1A
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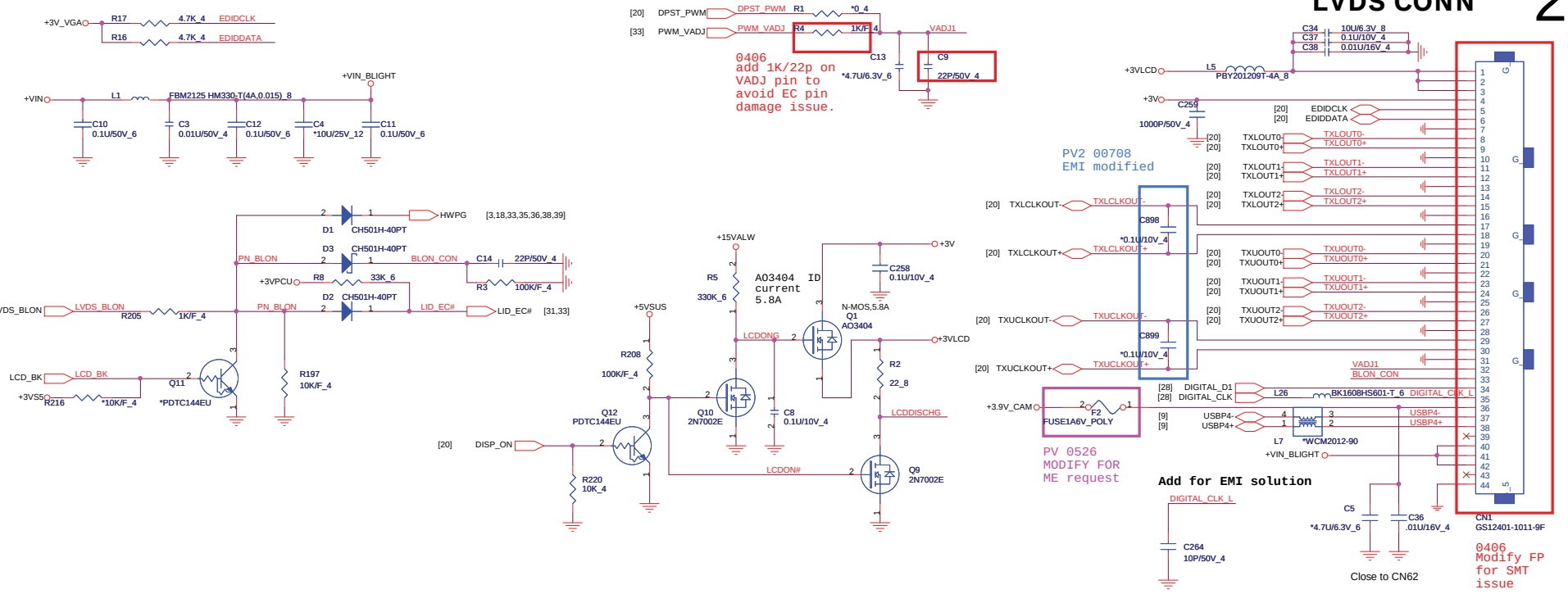
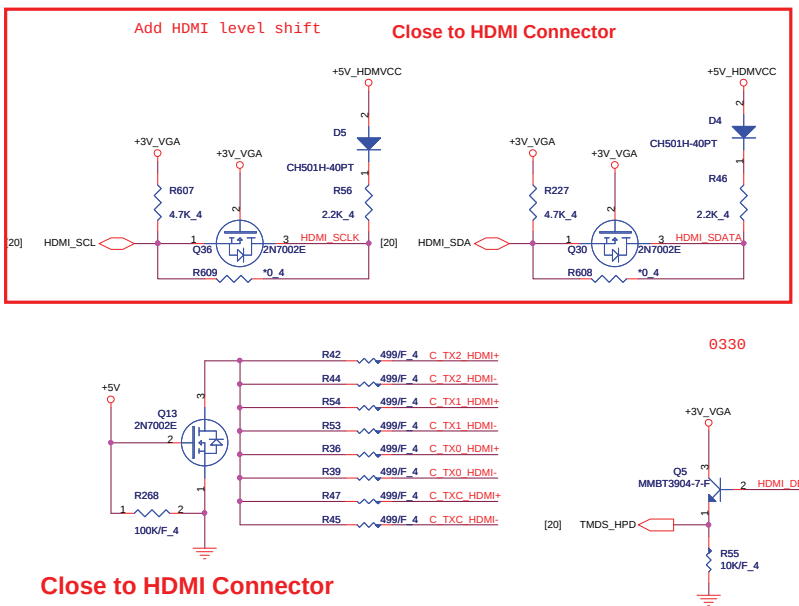
LVDS CONN

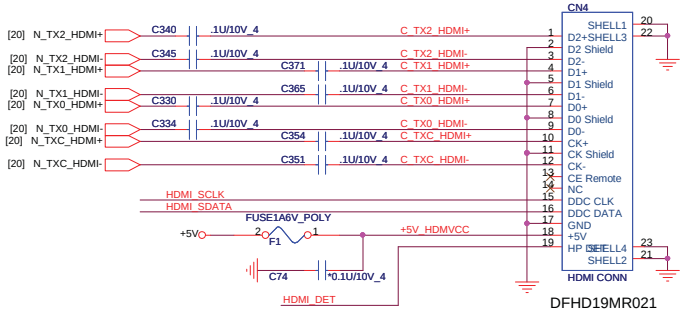
25



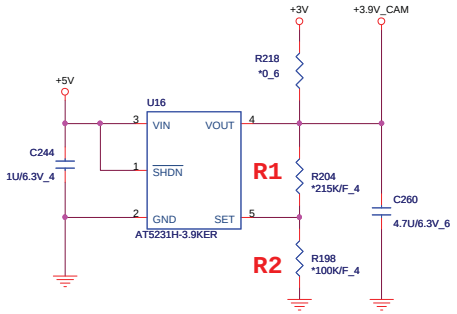
HDMI PORT



HDMI HPD SENSE



USB CAMERA /DIGITAL MIC CONNECT



Vout=1.25(1+R1/R2)

[2,3,7,8,9,10,11,13,14,15,16,18,26,27,28,29,30,31,32,33,34,37,40] +3V
[20,21,22,40] +3V_VGA
[7,9,10,11,40] +3VS5
[8,13,15,31,33,34,35,36,38,39,40,41,42] +3VPCU
[11,27,29,30,37,40] +5V
[40] +5VSUS
[35,38,40,41] +VIN
[35,40] +15VALW

NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: LCD CONN/HDMI/Lid	Rev: 1A
Date: Friday, July 10, 2009	Sheet 25 of 42	

USB3.0 X 2 and E-SATA/USB2.0 COMBO

26

*nPD720200

SI U29.P13 Change to +3V
SI2 0414 NEC request

SI 0219 change BOM
SI2 0320 change Footprint
150 mils (Iout=3.5A)
close USB3

Low: Enable AC Mode
High: Disable DC Mode

PV2 stage modify
1125 Modify
1119 Modify
6.3V to 25V from NEC

Clock select signal	
USB3.0_CSEL	High = External 48Mhz Low = 24MHz X'tal

AT25F512A or AT25F512B (Atmel)
MX25L512 (Macronix)
SI2 0325 change Footprint
PV-2 0702 Change Footprint

USB CON. co-lay
PV-2 0702 EMI add
PV-2 0702 EMI add
E_SATA change channel from SATA2 to SATA5 0216

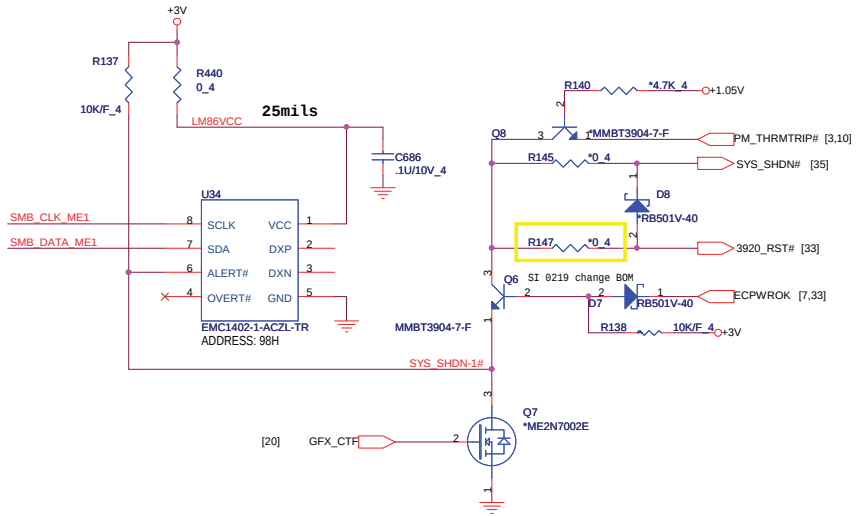
USB3.0 PORT1
USB3.0 PORT2
USB2.0 PORT6
USB2.0 PORT7

Close to chip
Use 1% RES

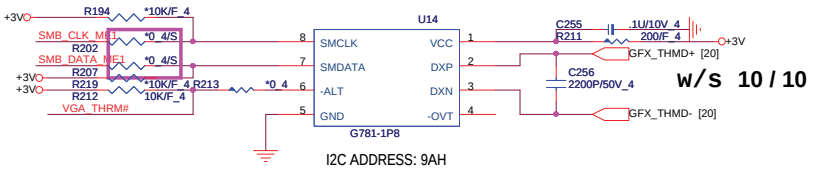
PROJECT : SP7
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	NEC USB 3.0	1A
Date: Friday, July 10, 2009	Sheet 26 of 42	

CPU THERMAL MONITOR

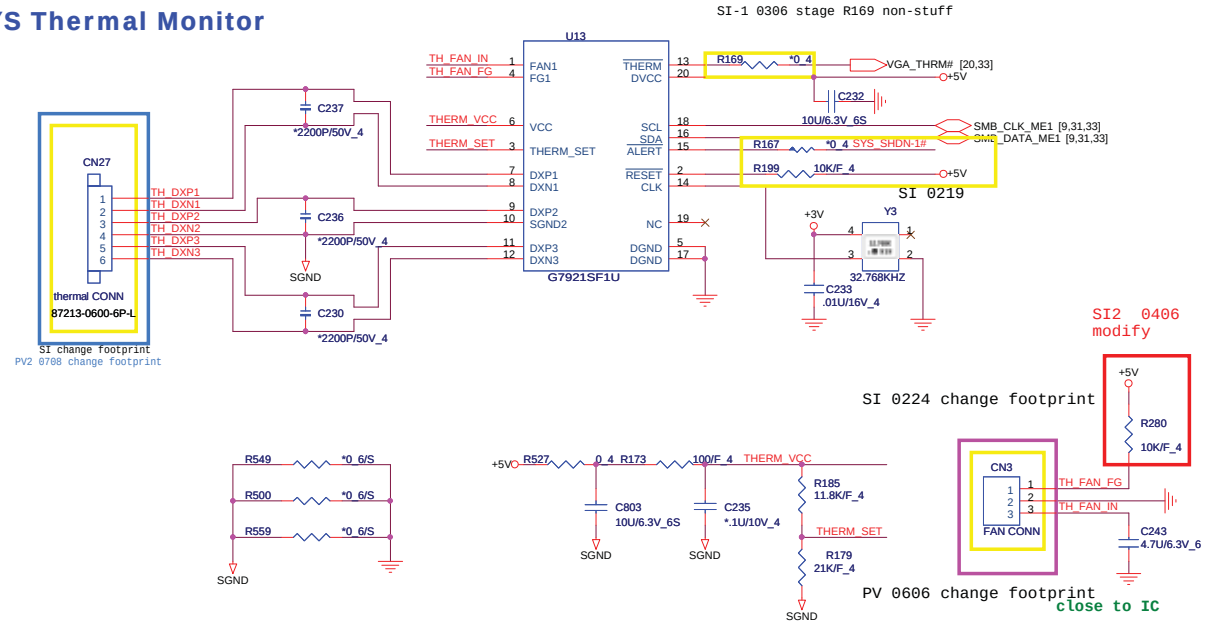


GPU Thermal Sensor



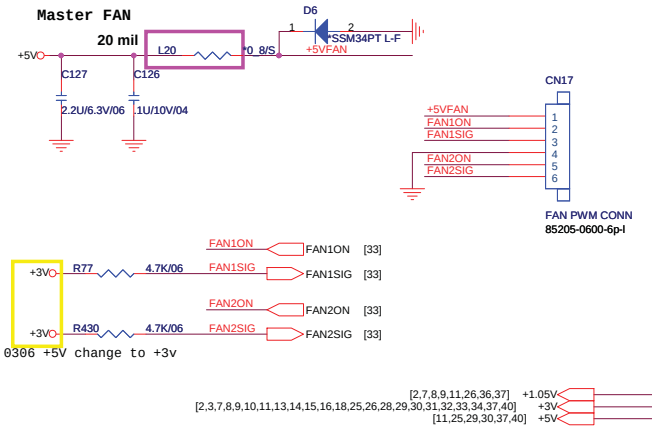
w/s 10 / 10

SYS Thermal Monitor



CPU FAN1/2 CONN

RPM Control

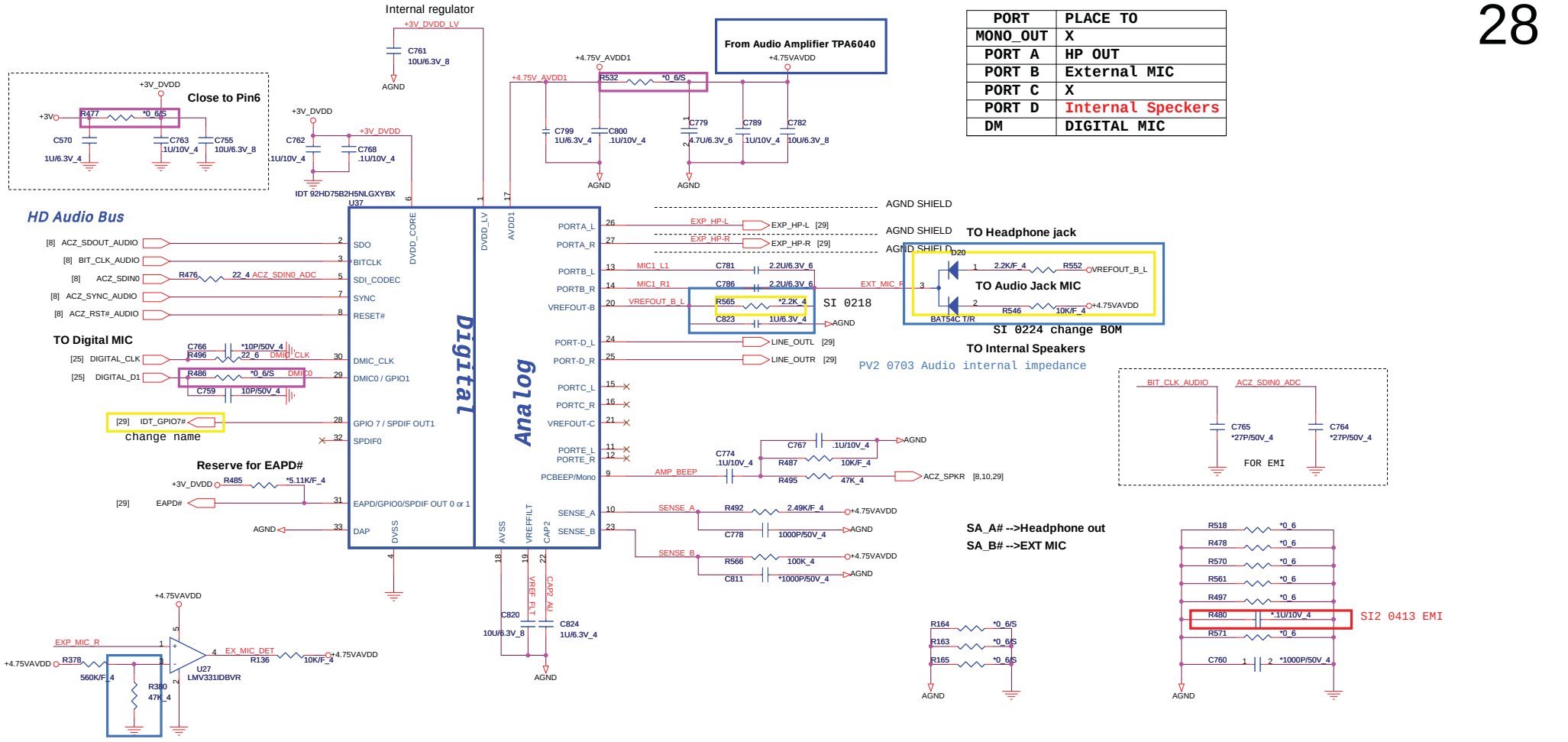


NB5

PROJECT : SP7
Quanta Computer Inc.

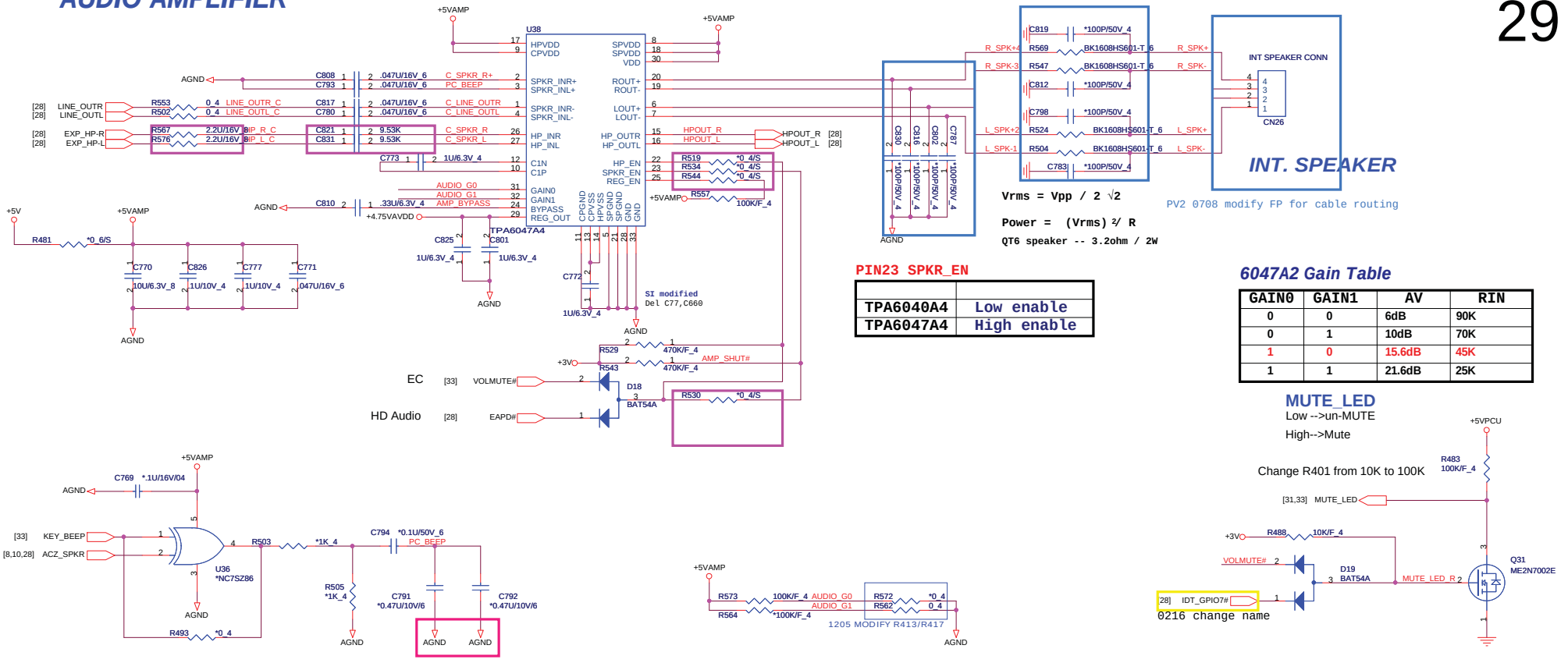
Size	Document Number	Rev
Custom	CPU/VGA/SYSTEM THERMAL	1A
Date: Friday, July 10, 2009	Sheet 27 of 42	

PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	External MIC
PORT C	X
PORT D	Internal Speckers
DM	DIGITAL MIC



PROJECT : SP7	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Azalia 92HD75
Rev: 1A	
Date: Friday, July 10, 2009	Sheet 28 of 42

AUDIO AMPLIFIER



PIN23 SPKR_EN

TPA6040A4	Low enable
TPA6047A4	High enable

6047A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

MUTE_LED

Low -->un-MUTE

High-->Mute

Change R401 from 10K to 100K

0216 change name

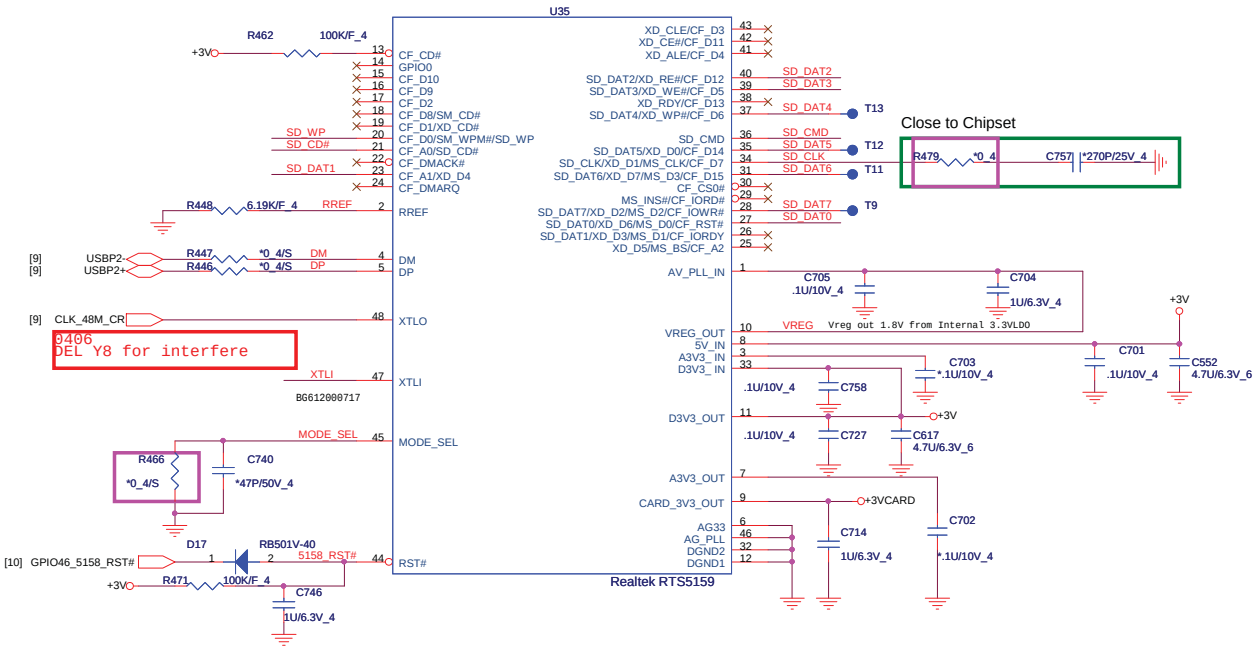
[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,30,31,32,33,34,37,40] +3V
[28] +4.75VAVDD
[11,25,27,30,37,40] +5V
[15,26,33,35,36,37,38,39,40,41] +5VPCU

NB5

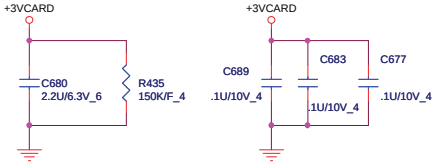
PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6047	1A

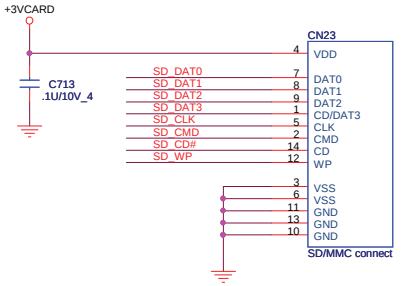
Date: Friday, July 10, 2009 Sheet 29 of 42



CLOSE CONN



2 IN1 CARD READER SD/MMC

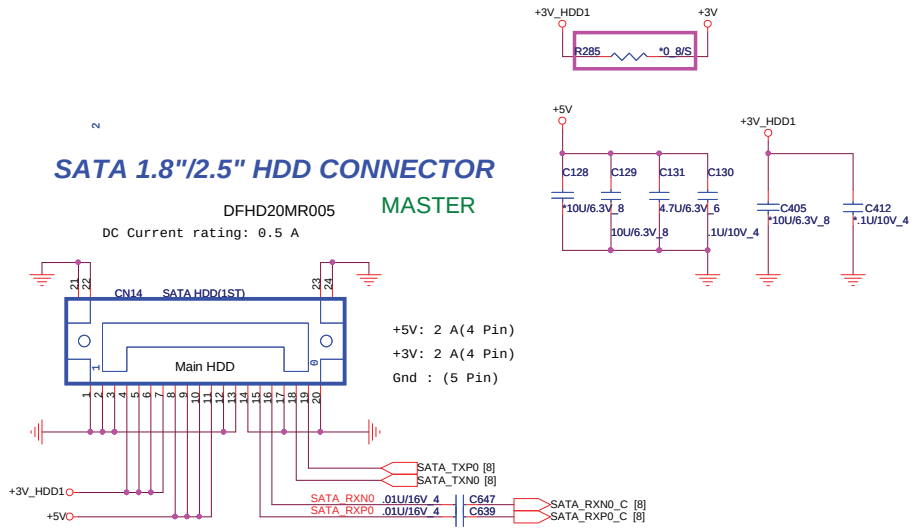


SATA 1.8"/2.5" HDD CONNECTOR

MASTER

DFHD20MR005

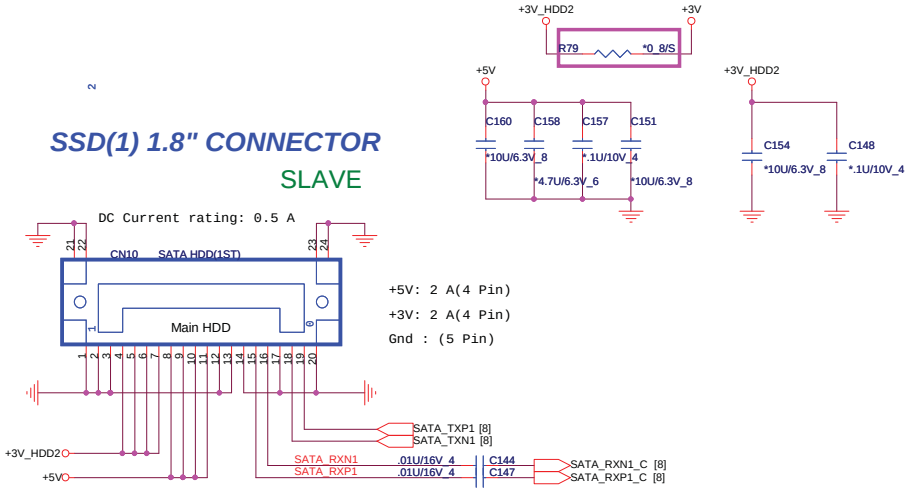
DC Current rating: 0.5 A



SSD(1) 1.8" CONNECTOR

SLAVE

DC Current rating: 0.5 A



[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,31,32,33,34,37,40] +3V

[11,25,27,29,37,40] +5V

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5159 & CR SOCKET	1A

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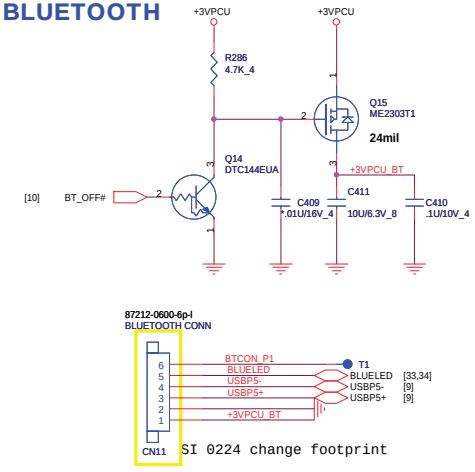
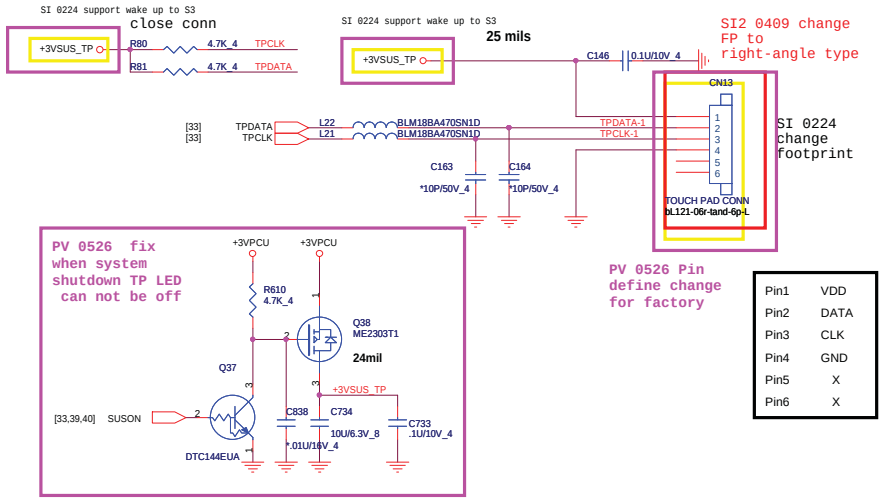
BLUETOOTH

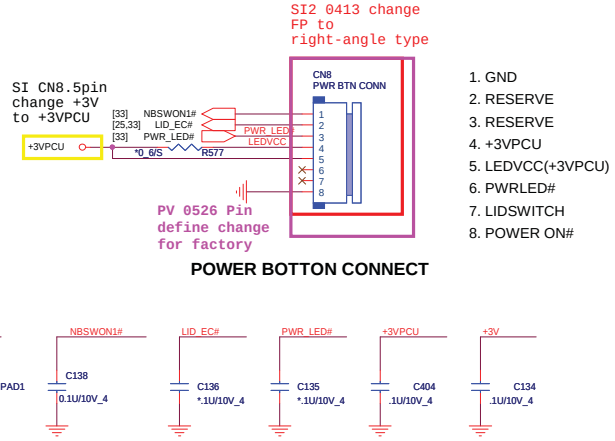


TOUCH PAD CONNECTOR

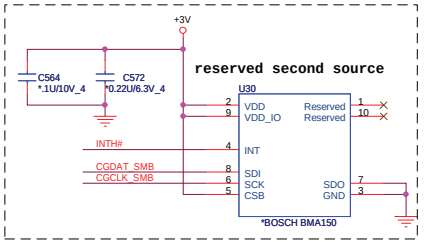


Pin1	VDD
Pin2	DATA
Pin3	CLK
Pin4	GND
Pin5	X
Pin6	X

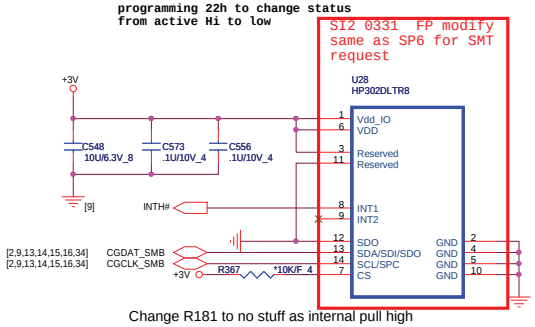
Power Botton



Accelerometer Sensor



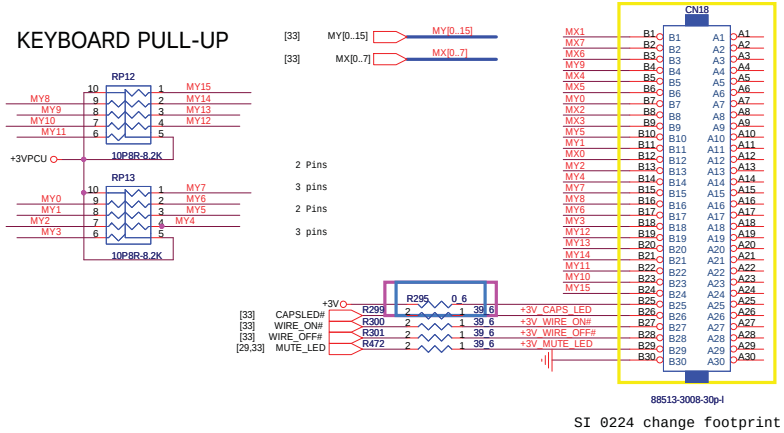
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



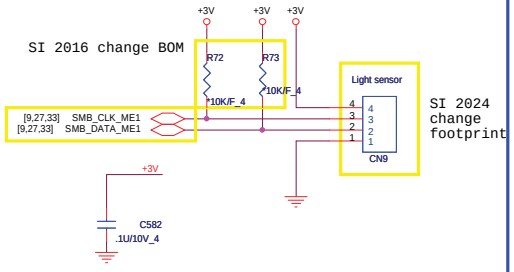
Change R181 to no stuff as internal pull high

Pin 12: Low	38hex
Pin 12: unconnected/floating	3Ahex

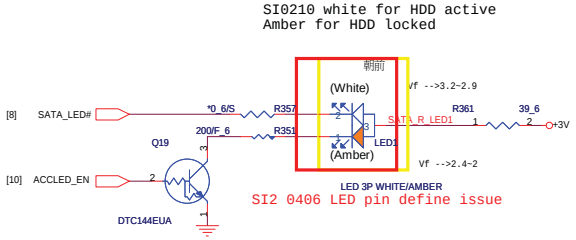
Key Board CONN



Ambient Light Sensor



LED



[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,32,33,34,37,40]
[8,13,15,25,33,34,35,36,38,39,40,41,42]
+3V
+3VPCU

Size: Custom	Document Number: BT/TP/PW BN/Key CON/Acc/LED/ALS		Rev: 1A
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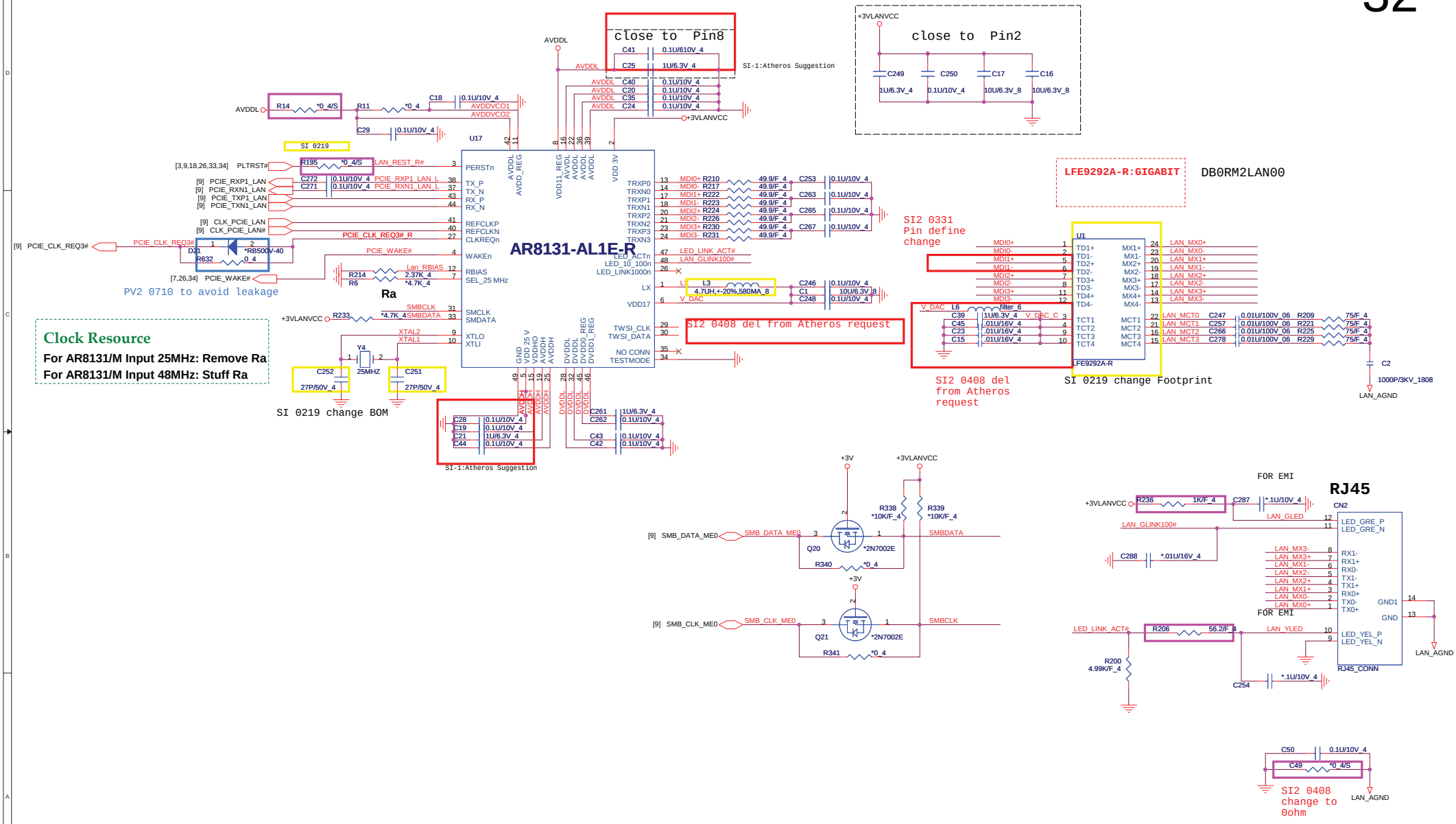
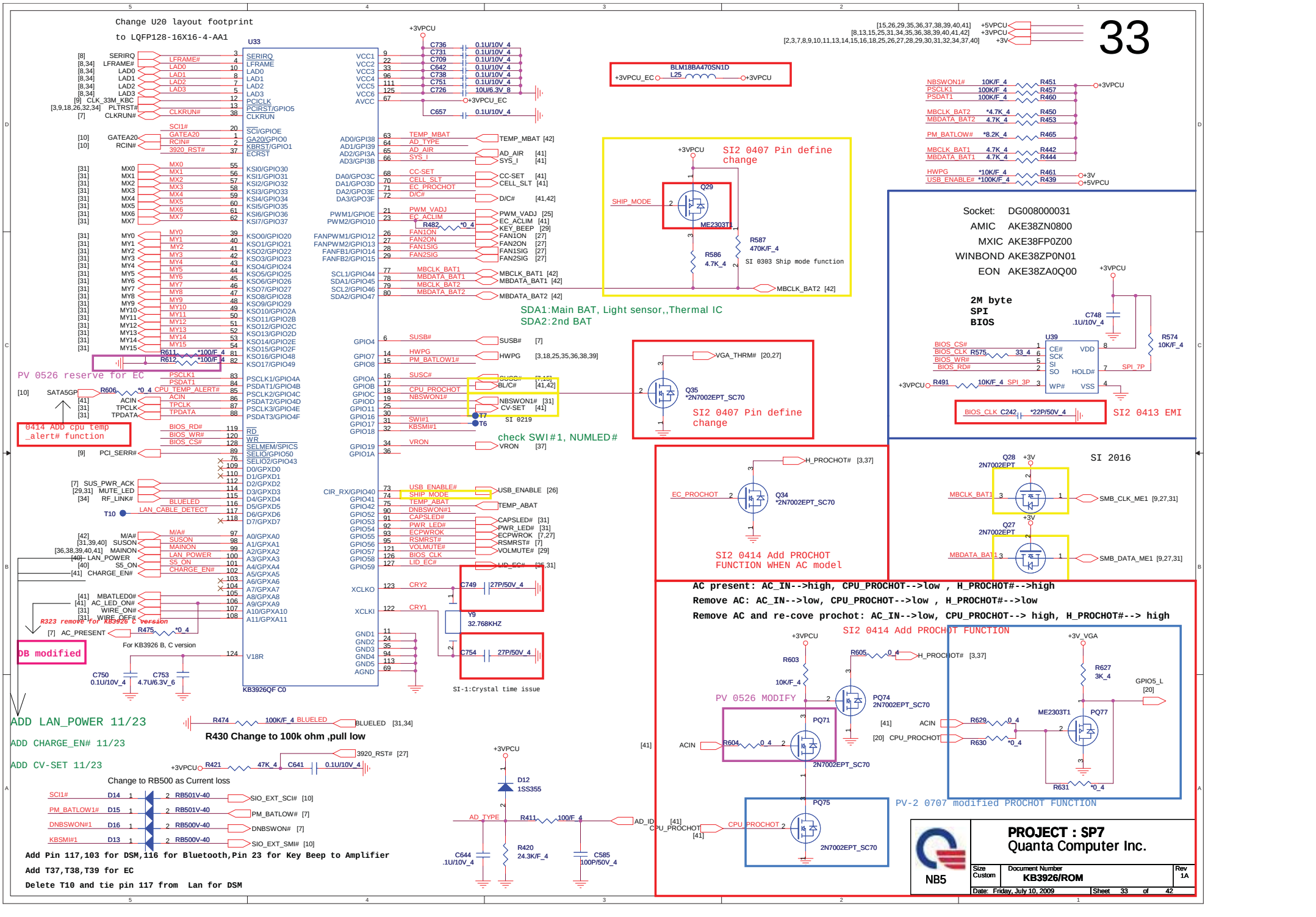
NB5

PROJECT : SP7
Quanta Computer Inc.



PROJECT : SP7	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Block Diagram
Rev: 1A	
Date: Friday, July 10, 2009	Sheet 32 of 42


33
Change U20 layout footprint
to LQFP128-16X16-4-AA1
U33
KB3926QF C0
PV 0526 reserve for EC
0414 ADD cpu temp
_alert# function
SI2 0407 Pin define
change
SDA1:Main BAT, Light sensor,,Thermal IC
SDA2:2nd BAT
check SWI#1, NUMLED#
SI2 0407 Pin define
change
SI 0219
SI-1:Crystal time issue
Socket: DG008000031
AMIC AKE38ZN0800
MXIC AKE38FP0Z00
WINBOND AKE38ZP0N01
EON AKE38ZA0Q00
2M byte
SPI
BIOS
SI2 0413 EMI
SI 2016
SI2 0414 Add PROCHOT
FUNCTION WHEN AC model
AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->low
Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high
SI2 0414 Add PROCHOT FUNCTION
PV 0526 MODIFY
PV-2 0707 modified PROCHOT FUNCTION
DB modified
R323 remove for KB3926 C version
For KB3926 B, C version
ADD LAN_POWER 11/23
ADD CHARGE_EN# 11/23
ADD CV-SET 11/23
R430 Change to 100k ohm ,pull low
Change to RB500 as Current loss
Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier
Add T37,T38,T39 for EC
Delete T10 and tie pin 117 from Lan for DSM
PROJECT : SP7
Quanta Computer Inc.
NB5
KB3926/ROM
Size Custom
Rev 1A
Date: Friday, July 10, 2009
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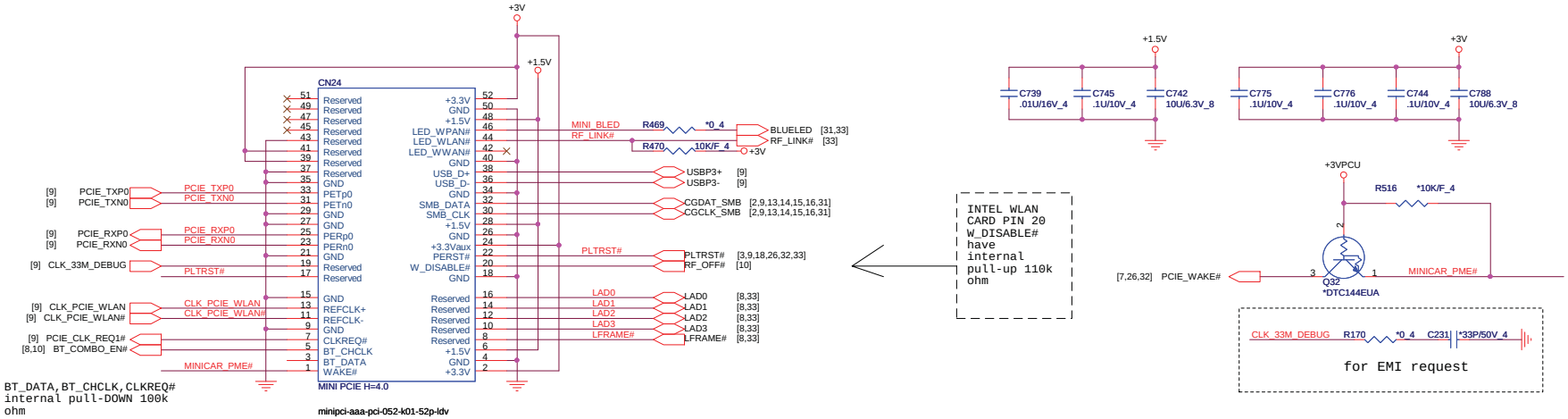
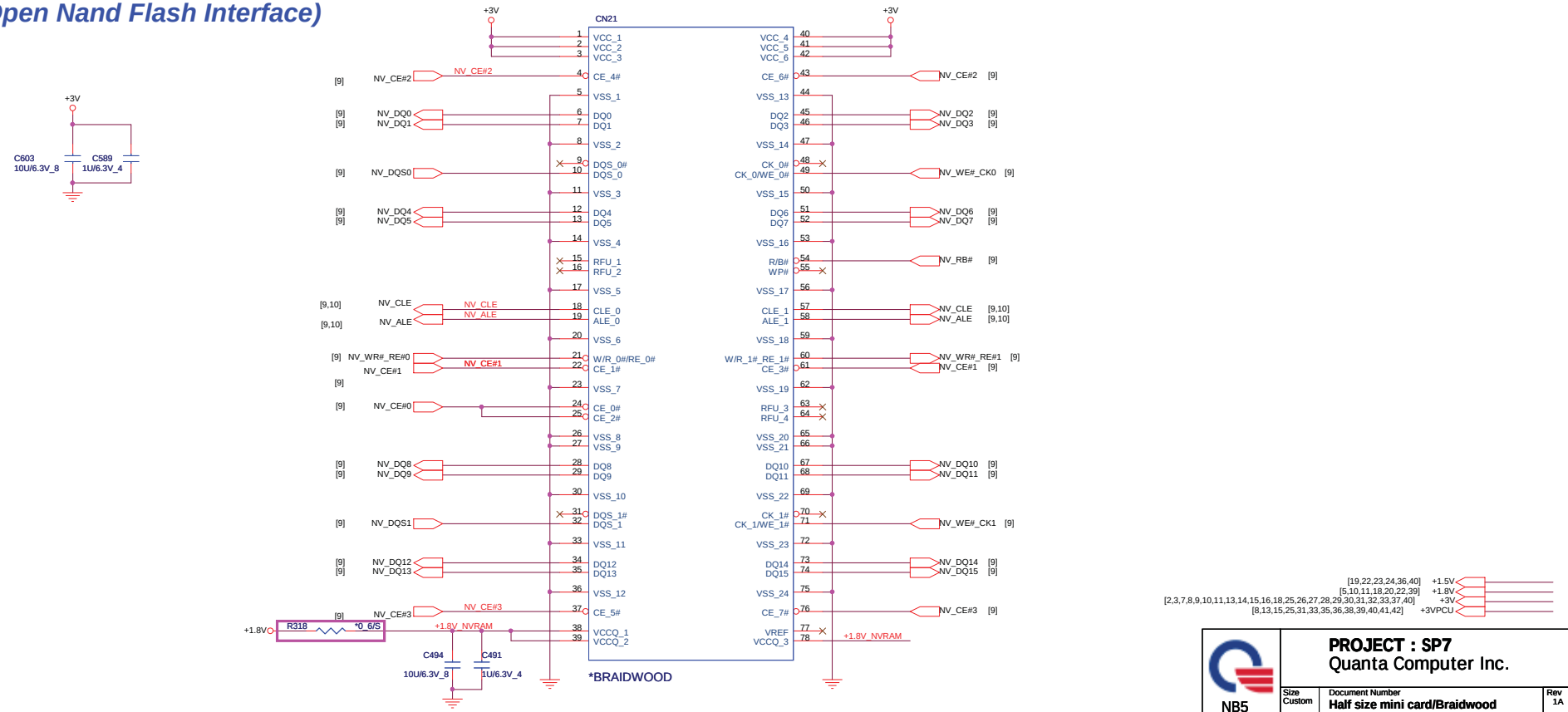
Half size mini card(802.11a/b/g/n)



Braidwood(Open Nand Flash Interface)

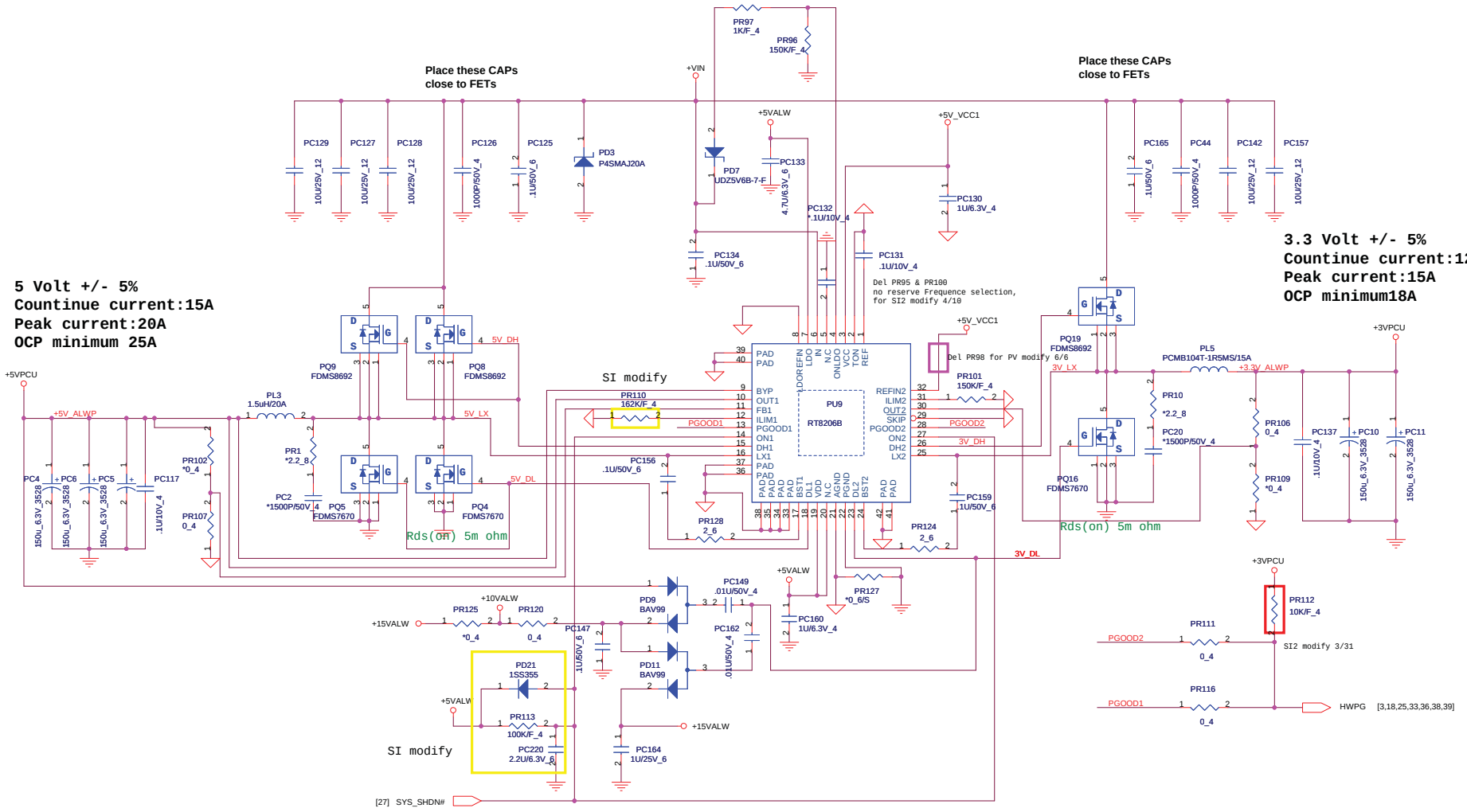


Size: Custom	Document Number: Half size mini card/Braidwood
Rev: 1A	
Date: Friday, July 10, 2009	Sheet 34 of 42

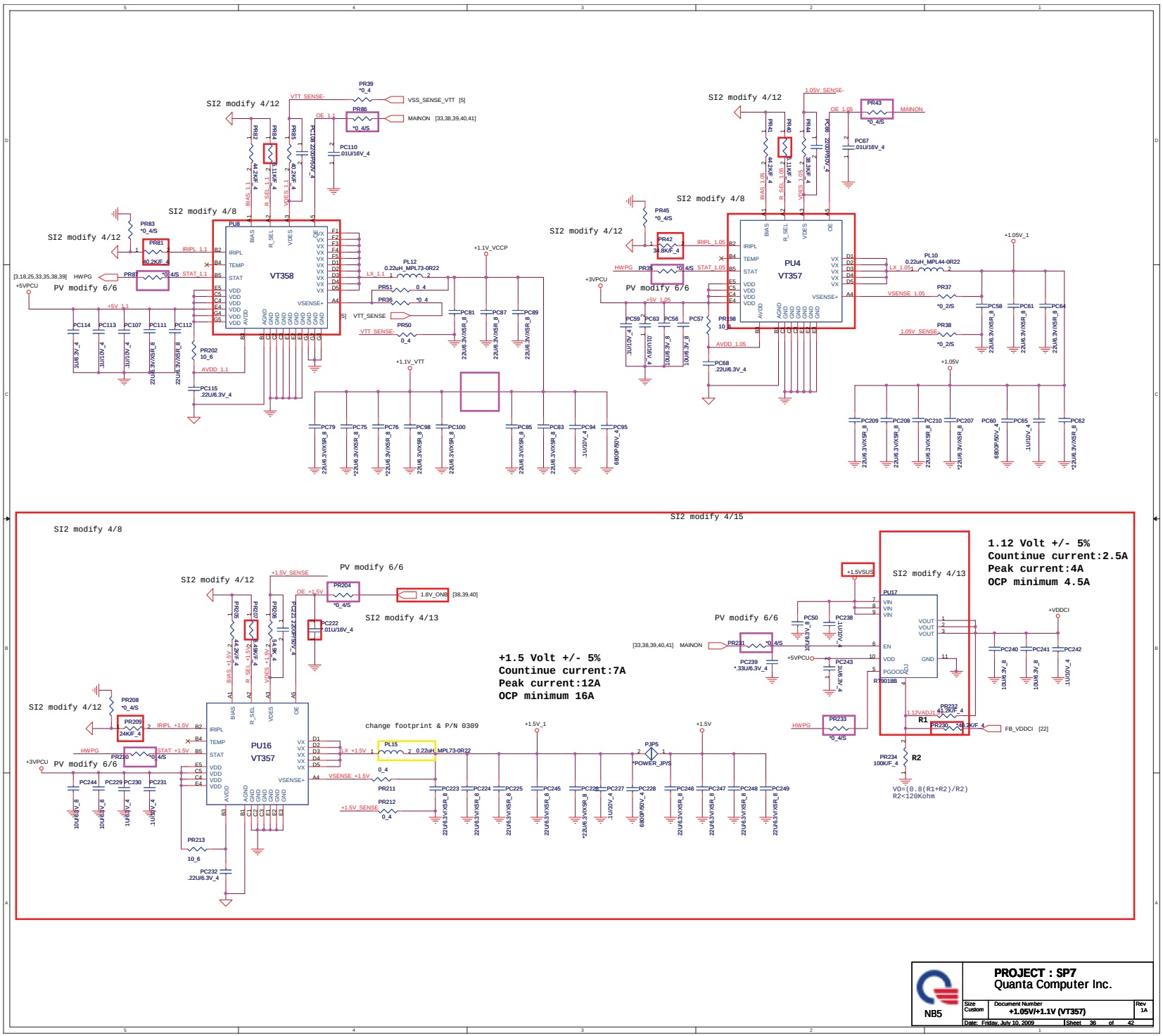
PROJECT : SP7
Quanta Computer Inc.

NB5

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW



NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Friday, July 10, 2009	Sheet 35 of 42	


SI2 modify 4/12
SI2 modify 4/8
PU8
VT358
PU4
VT357
PV modify 6/6
SI2 modify 4/15
SI2 modify 4/13
PU16
PU17
R1
R2
1.12 Volt +/- 5%
Countinue current:2.5A
Peak current:4A
OCP minimum 4.5A
+1.5 Volt +/- 5%
Countinue current:7A
Peak current:12A
OCP minimum 16A
change footprint & P/N 0309
V0=(0.8(R1+R2)/R2)
R2<120Kohm
PROJECT : SP7
Quanta Computer Inc.
NB5
+1.05V/+1.1V (VT357)
Friday, July 10, 2009
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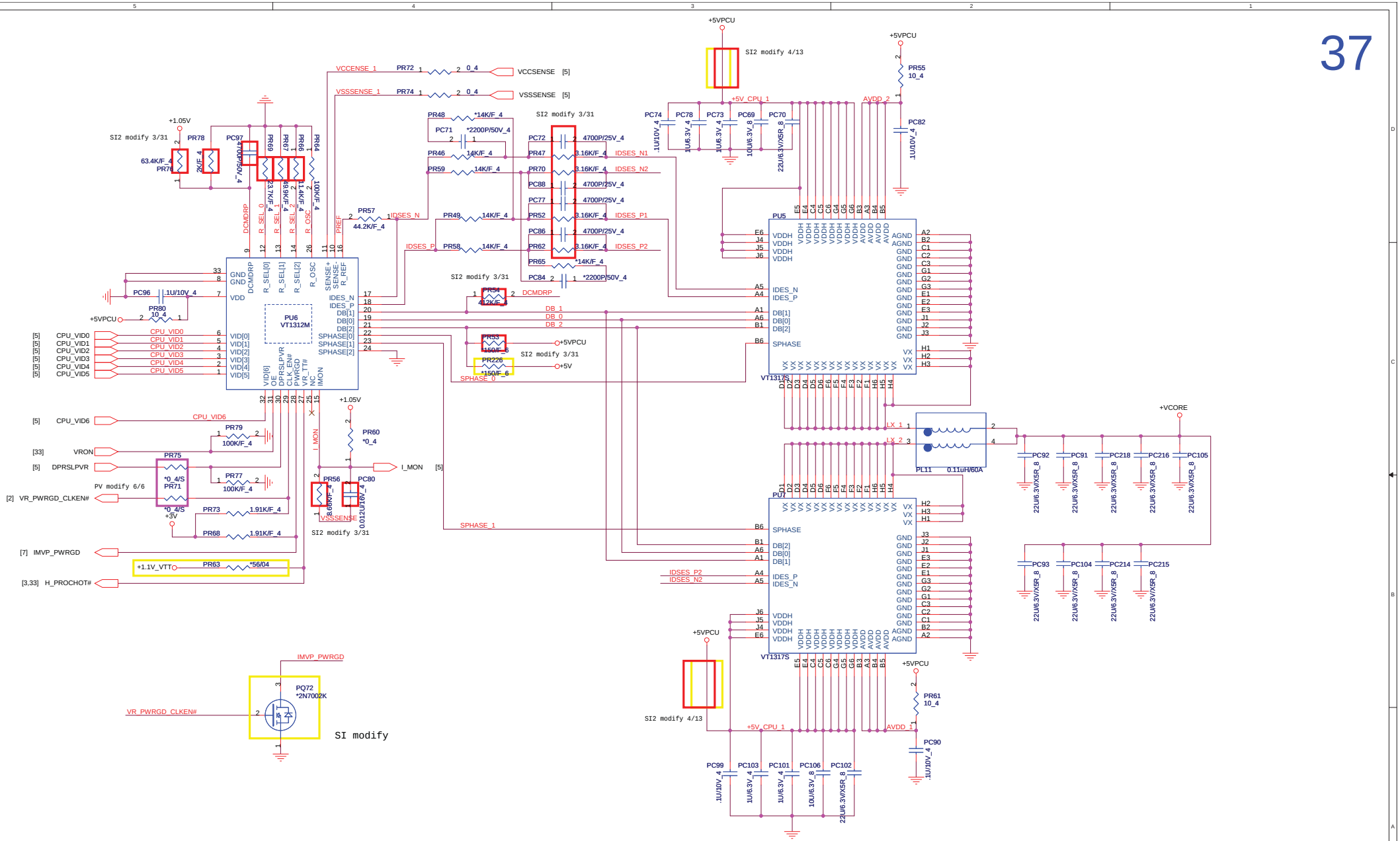
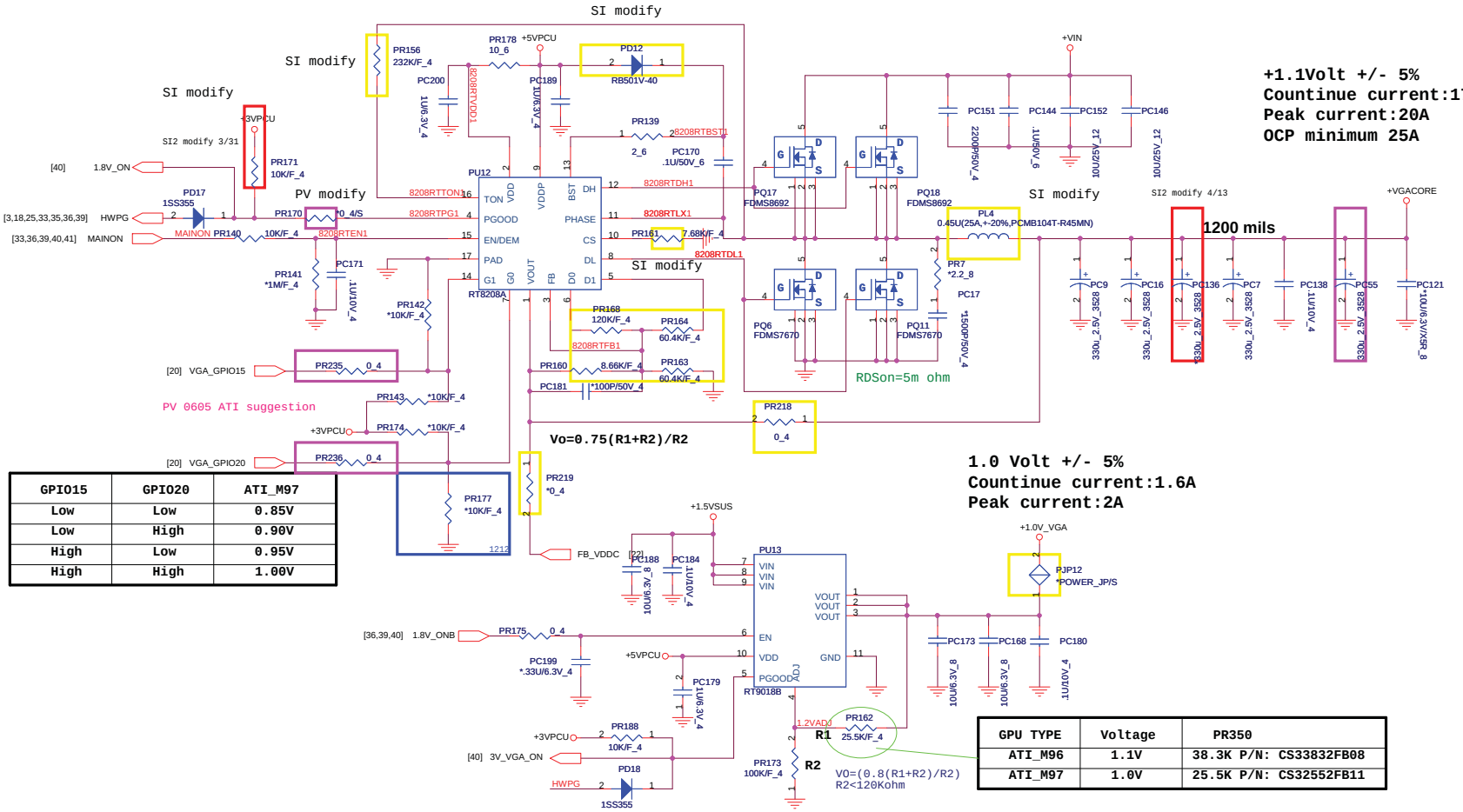


PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core (VT1312M/VT1317)	1A
NB5	Date: Friday, July 10, 2009	Sheet 37 of 42

VGA Core & VCC1.1



GPIO15	GPIO20	ATI_M97
Low	Low	0.85V
Low	High	0.90V
High	Low	0.95V
High	High	1.00V

GPU TYPE	Voltage	PR350
ATI_M96	1.1V	38.3K P/N: CS33832FB08
ATI_M97	1.0V	25.5K P/N: CS32552FB11

PROJECT : SP7
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	VGA Core (RT8208)	1A

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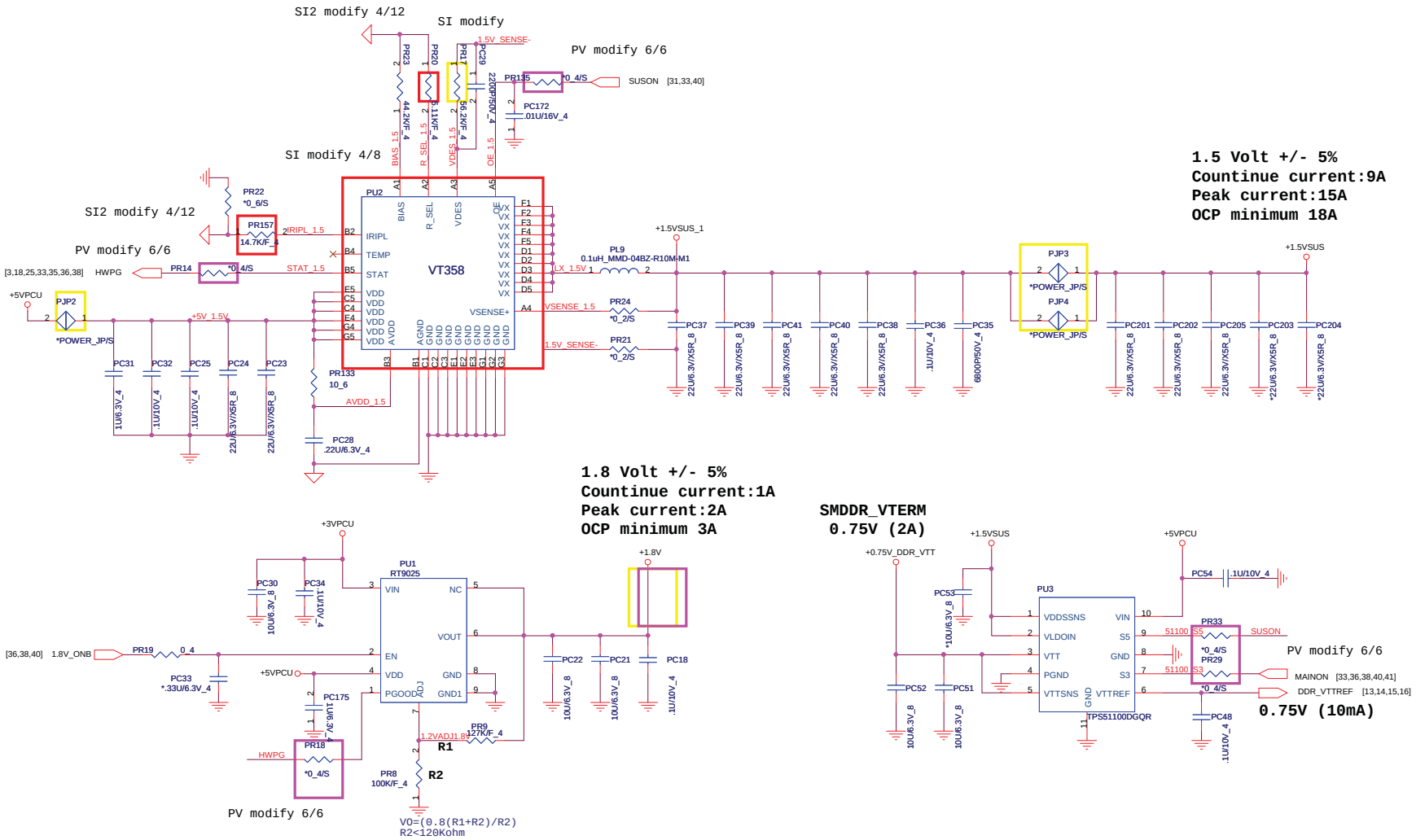
SI2 modify 4/12
SI modify
PV modify 6/6
SI modify 4/8
SI2 modify 4/12
PV modify 6/6
1.5 Volt +/- 5%
Countinue current:9A
Peak current:15A
OCP minimum 18A
VT358
PU2
PL9
0.1uH_MMD-04BZ-R10MM1
+1.5VSUS_1
+1.5VSUS
PJP3
PJP4
*POWER_JP/S
PJP2
+5VPCU
+5V_1.5V
SUSON [31,33,40]
HWPG
STAT_1.5
VSENSE_1.5
1.5V_SENSE-
LX_1.5V
1.8 Volt +/- 5%
Countinue current:1A
Peak current:2A
OCP minimum 3A
PU1
RT9025
+3VPCU
+1.8V
1.8V_ONB
1.2VADJ1.8V
R1
R2
V0=(0.8(R1+R2)/R2)
R2<120Kohm
PV modify 6/6
SMDDR_VTERM
0.75V (2A)
PU3
TPS51100DGQR
+0.75V_DDR_VTT
MAINON [33,36,38,40,41]
DDR_VTTREF [13,14,15,16]
0.75V (10mA)
PV modify 6/6
NB5
PROJECT : SP7
Quanta Computer Inc.
Size Custom
Document Number
DDR3/1.8V (VT356/VT357)
Rev 1A
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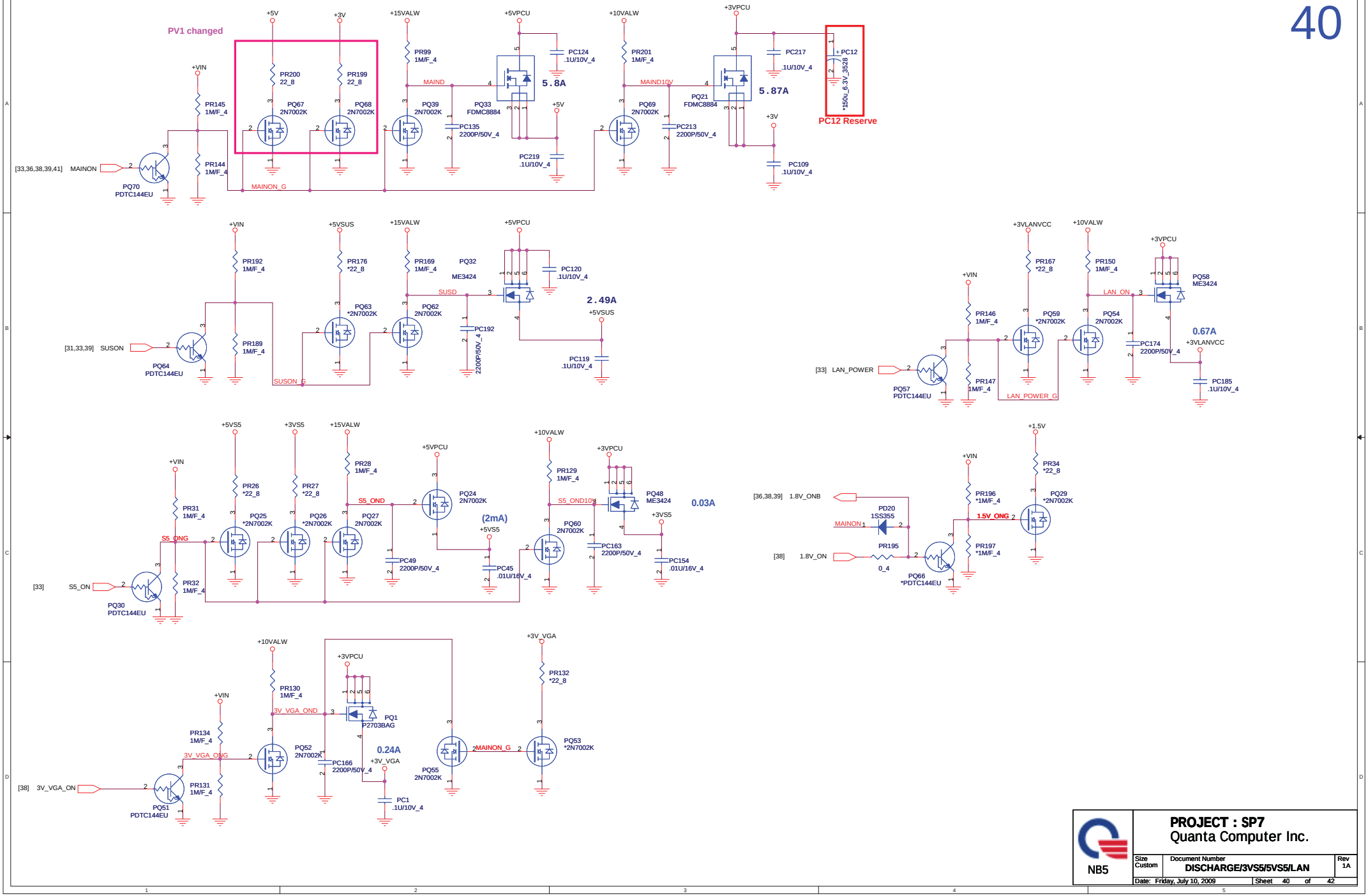

NB5	**PROJECT : SP7** Quanta Computer Inc.	
	Size: Custom Document Number: **DISCHARGE/3VS5/5VS5/LAN**	Rev: 1A
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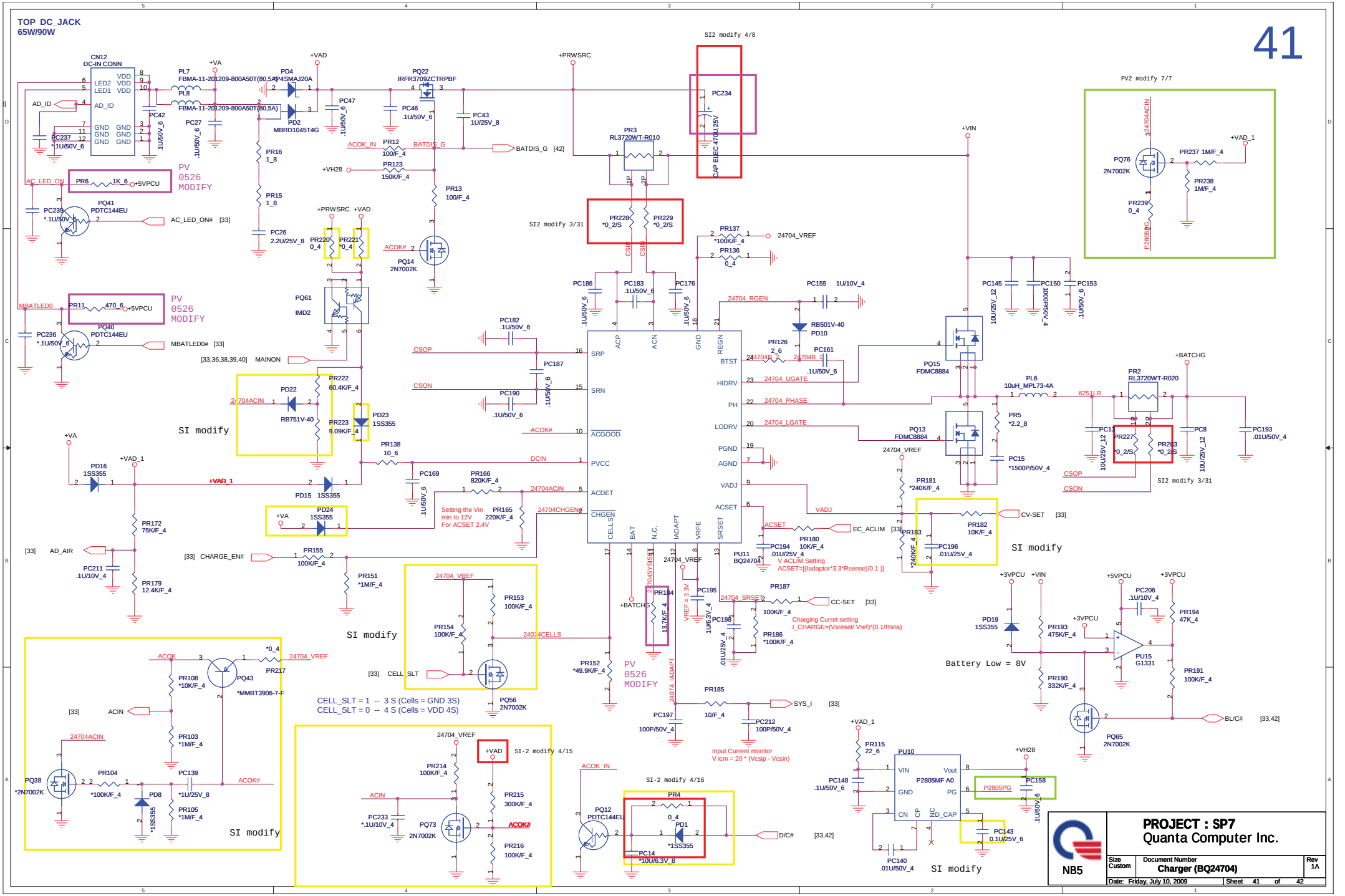
TOP DC_JACK
65W/90W
41
CN12
DC-IN CONN
PL7
FBMA-11-201209-800A50T(80,5A)
PL8
FBMA-11-201209-800A50T(80,5A)
PD4
SMAJ20A
PD2
MBRD1045T4G
PQ22
IRFR3709ZCTRPBF
PC234
CAP ELEC 470U/25V
PR3
RL3720WT-R010
SI2 modify 4/8
PV2 modify 7/7
PQ76
2N7002K
PR237 1M/F_4
PR238 1M/F_4
PR239 0_4
PV
0526
MODIFY
PR6 1K_6
PQ41
PDTC144EU
PR11 470_6
PQ40
PDTC144EU
PQ61
IMD2
PR220 0_4
PR221 *0_4
PQ14
2N7002K
SI2 modify 3/31
PR228 *0_2/S
PR229 *0_2/S
PR137 *100K/F_4
PR136 0_4
24704_VREF
PC186
PC183 .1U/50V_6
PC176
24704_RGEN
PC155 1U/10V_4
RB501V-40
PD10
PC145
PC150 1000P/50V_4
PC153
PC182 .1U/50V_6
PC187
PC190 .1U/50V_6
PR126 2_6
PC161 .1U/50V_6
24704B_1
24704B
24704_UGATE
24704_PHASE
24704_LGATE
24704_RGEN
PQ15
FDMC8884
PL6
10uH_MPL73-4A
6251LR
PR2
RL3720WT-R020
+BATCHG
PC13
PR227 *0_2/S
PR203 *0_2/S
PC8
PC193 .01U/50V_4
PC15 *1500P/50V_4
PQ13
FDMC8884
PR5 *2.2_8
CSOP
CSON
SI2 modify 3/31
SI modify
PD22
RB751V-40
PD23
1SS355
PR222 60.4K/F_4
PR223 9.09K/F_4
PR138 10_6
PC169
PR166 820K/F_4
Setting the Vin min to 12V For ACSET 2.4V
PR165 220K/F_4
PD16
1SS355
PD15
1SS355
PD24
1SS355
PR172 75K/F_4
PC211 .1U/10V_4
PR179 12.4K/F_4
PR155 100K/F_4
PR151 *1M/F_4
SI modify
PR153 100K/F_4
PR154 100K/F_4
24024CELLS
[33] CELL_SLT
PQ56
2N7002K
CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)
PV
0526
MODIFY
PR152 *49.9K/F_4
PR184 13.7K/F_4
PC195
PC198 .01U/25V_4
PR187 100K/F_4
PR186 *100K/F_4
PU11
BQ24704
V ACLIM Setting
ACSET=[(Iadaptor*3.3*Rsense)/0.1]
Charging Curret setting
I_CHARGE=(Vsreset/ Vref)*(0.1/Rsns)
PR185 10/F_4
PC197 100P/50V_4
PC212 100P/50V_4
Input Current monitor
V icm = 20 * (Vcsip - Vcsin)
SYS_I [33]
PR181 *240K/F_4
PR182 10K/F_4
PR183 *240K/F_4
PC196 .01U/25V_4
PR180 10K/F_4
PC194 .01U/25V_4
CV-SET [33]
CC-SET [33]
EC_ACLIM [33]
SI modify
PD19
1SS355
PR193 475K/F_4
PR190 332K/F_4
PU15
G1331
PC206 .1U/10V_4
PR194 47K_4
PR191 100K/F_4
Battery Low = 8V
PQ65
2N7002K
BL/C# [33,42]
PR217 *0_4
PQ43
*MMBT3906-7-F
PR108 *10K/F_4
PR103 *1M/F_4
PR104 *100K/F_4
PC139 *1U/25V_8
PD8
*1SS355
PR105 *1M/F_4
PQ38
*2N7002K
SI modify
PR214 100K/F_4
PR215 300K/F_4
PR216 100K/F_4
PC233 *.1U/10V_4
PQ73
2N7002K
SI-2 modify 4/15
SI-2 modify 4/16
PR4 0_4
PD1
*1SS355
PC14
*10U/6.3V_8
PQ12
PDTC144EU
D/C# [33,42]
PU10
P2805MF A0
PR115 22_6
PC148 .1U/50V_6
PC158 .1U/50V_6
PC143 0.1U/25V_6
PC140 .01U/50V_4
SI modify
NB5
PROJECT : SP7
Quanta Computer Inc.
Size Custom
Document Number
Charger (BQ24704)
Rev 1A
Date: Friday, July 10, 2009
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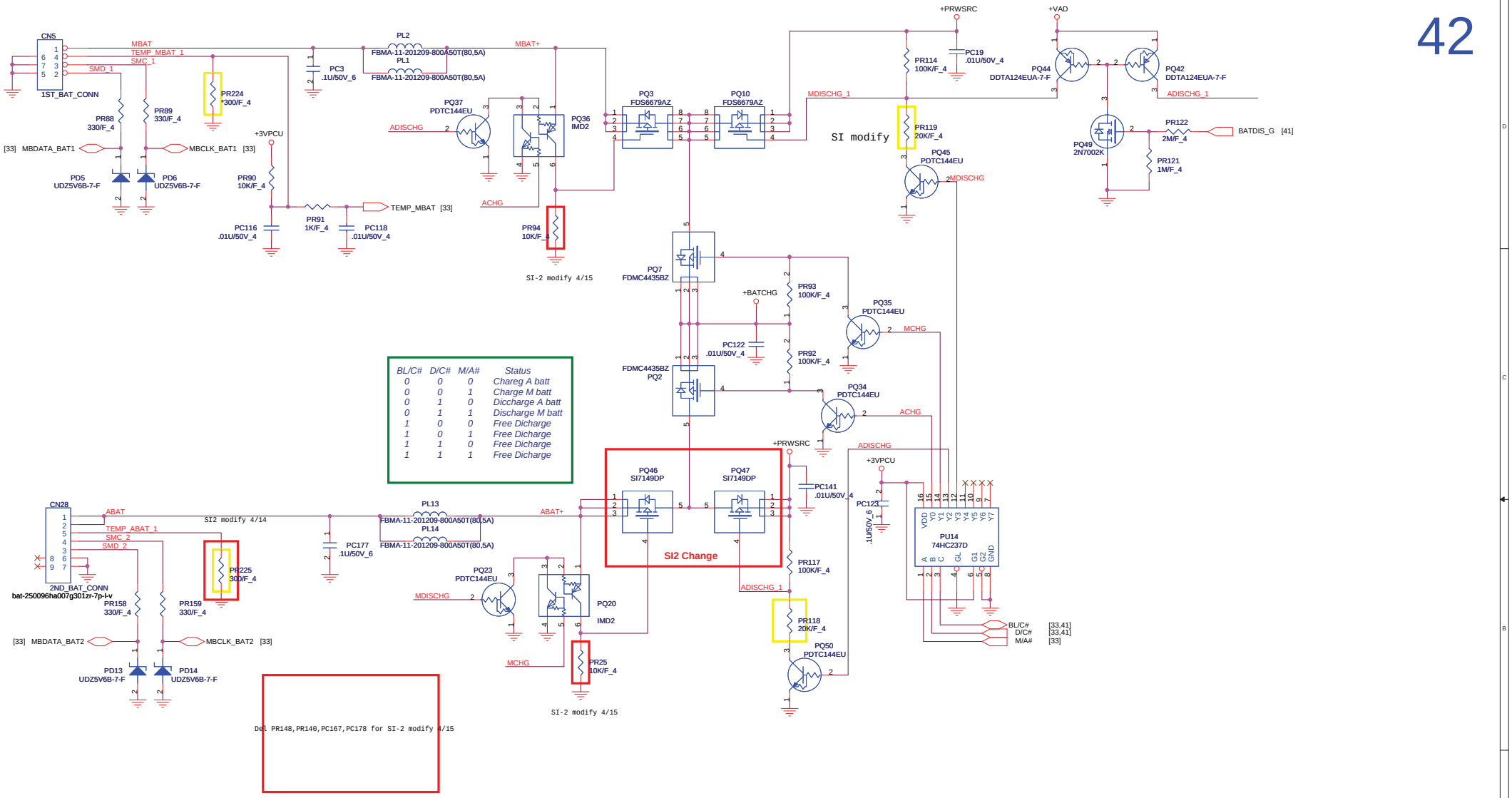

BL/C#	D/C#	M/A#	Status
0	0	0	Chareg A batt
0	0	1	Charge M batt
0	1	0	Diccharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

NB5	PROJECT : SP7 Quanta Computer Inc.	
	Size: Custom	Document Number: BATTERY SELECTOR
	Rev: 1A	
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