ZQ2 SYSTEM DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

IV@ -----> iGPU
SW@ -----> dGPU
SP@ -----> option notice
SIDE@ -----> sideport

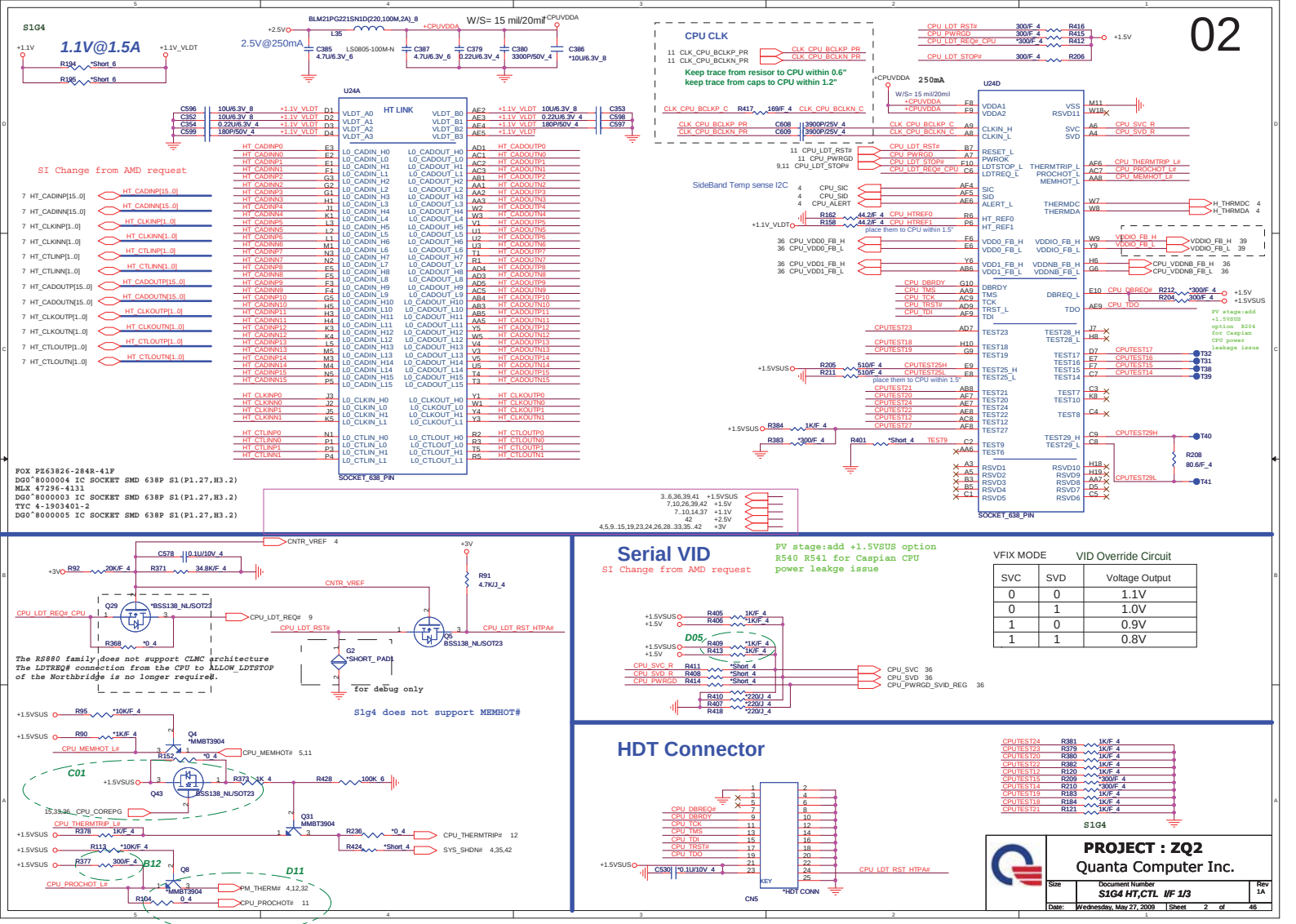
sideport-L75,L76,R583,R392,C832,R455,R550,R502
NB A11-R105,R108
SB A12-R267,R271
JV/JM-CN16,R450,R456
EC-D8,D27
UMA-R461
VRAM-R358,R359,R360,R363,R365,R72

DDR3-SODIMM1 PAGE 5,6 — DDR3 channel A
DDR3-SODIMM2 PAGE 5,6 — DDR3 channel B
AMD Champlain 35mm X 35mm S1G4 Processor 638P (PGA)45W/35W PAGE 2,3,4
CPU THERMAL SENSOR PAGE 4
From SB CLOCK GEN
CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK
HT3
PCI-E
PCI-Express 8X
Side port
NORTH BRIDGE RS880 A12 21mm X 21mm, 528pin BGA PAGE 7,8,9,10
DDR3 RAM PAGE 7
ATI Park XT 128-bit M2 Pkg 29mm X 29mm PAGE 16,17,18 19,20,21
800MHz VRAM DDR3 64MX16X4,64 bit 64MX16X8,128 bit PAGE 22
VGA Park
X1
X2
LAN Atheros PCIE-LAN AR8151 (10/100/1000) PAGE 25
Mini PCI-E Card (Wireless LAN) PAGE 26
RJ45 PAGE 25
HDMI PAGE 24
CRT PAGE 23
LVDS PAGE 23
ALINK X4
SATA - HDD1 PAGE 27 — SATA0 150MB
SATA - CD-ROM PAGE 27 — SATA1 150MB
SOUTH BRIDGE SB820 21mm X 21mm, 528pin BGA A11 4.5W(Ext) 4.3W(Int) PAGE 12,13,14,15,16
BT PAGE 32
USB1.1
USB2.0
USB2.0 Ports X1 PAGE 30
Webcam PAGE 23
CardReader AU6437 PAGE 29
WLAN conn PAGE 26
USB BOARD USB2.0 Ports x3 PAGE 30
Power BOARD PAGE 30
Switch BOARD PAGE 30
LPC
Azalia
Winbond KBC NPCE781L PAGE 33
Codec RTL ALC271X PAGE 28
Keyboard PAGE 32
Touch Pad PAGE 32
CPU FAN PAGE 32
SPI PAGE 33
Digital MIC PAGE 28
AUDIO CONN (Phone/ MIC) PAGE 28
Speaker PAGE 28

CPU
- AMD CPU CORE (ISL6265) PAGE 36

NB
- NB_CORE (UP6111AQDD) PAGE 38
- +VGPU_CORE (MAX8792ETD) PAGE 40
- +1V/+1.5_GPU/+1.8_GPU PAGE 41
- 0.9V/DDR 1.5V(RT8207) PAGE 39
- SYSTEM 5V/3V (RT8206) PAGE 35
- 1.1V(UP6111AQDD) PAGE 37
- Discharge /Thermal protec PAGE 42

PROJECT : ZQ2
Quanta Computer Inc.
Size | Document Number: Block Diagram | Rev 1A
Date: Wednesday, May 27, 2009 | Sheet 1 of 46



FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

Serial VID

SI Change from AMD request

PV stage:add +1.5VSUS option
R540 R541 for Caspian CPU
power leakge issue

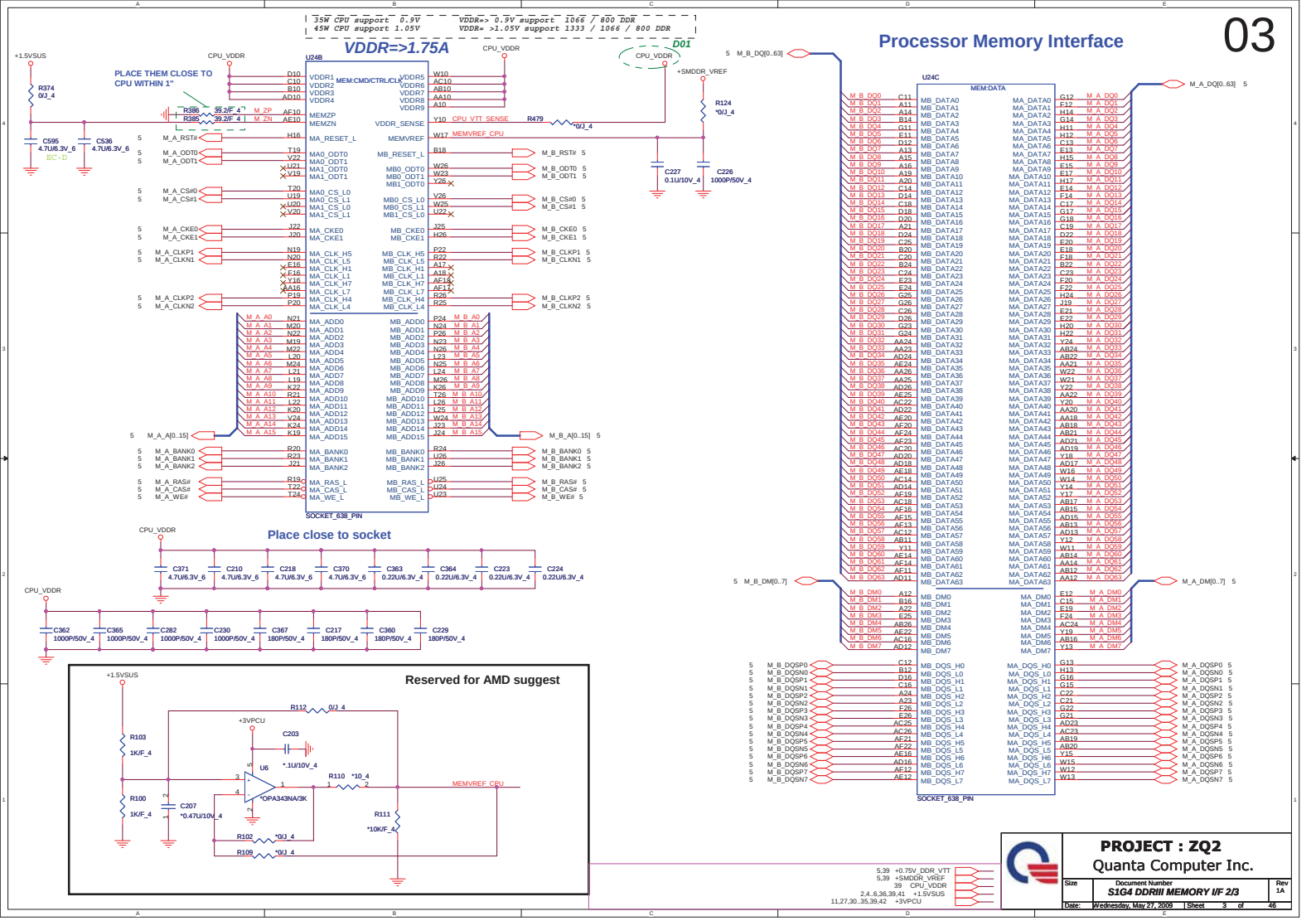
VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

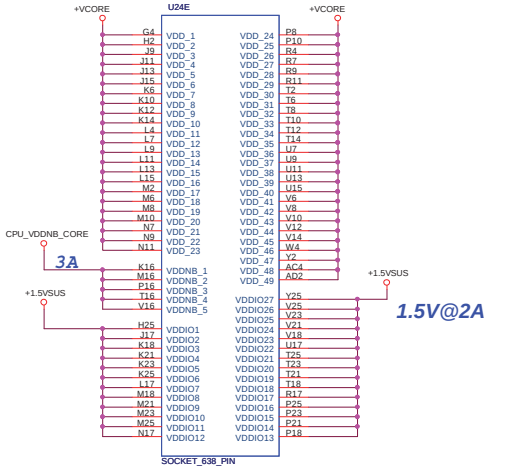
HDT Connector

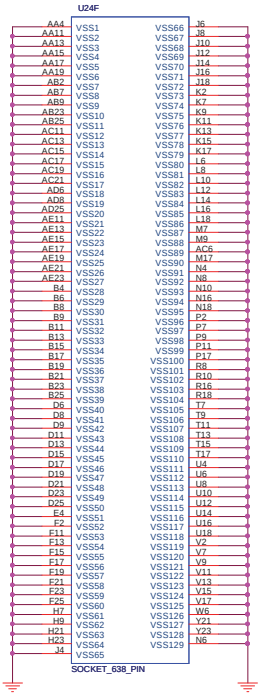
PROJECT : ZQ2
Quanta Computer Inc.

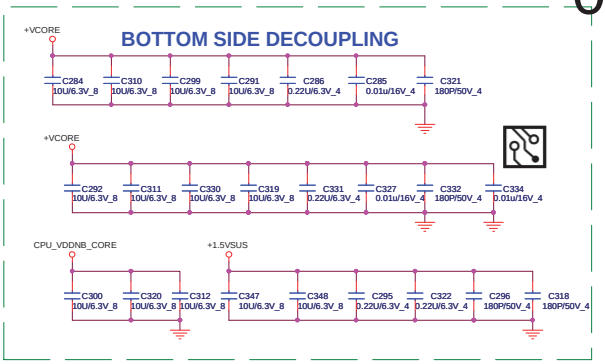
Size	Document Number	Rev
	S1G4 HT,CTL I/F 1/3	1A
Date: Wednesday, May 27, 2009	Sheet 2 of 46	

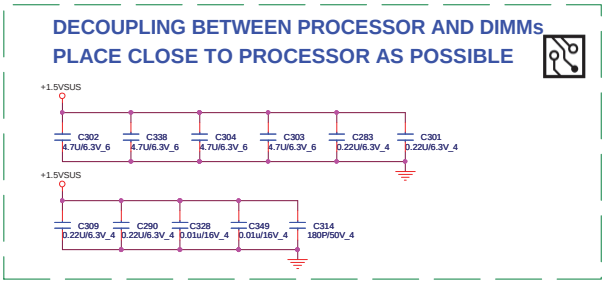


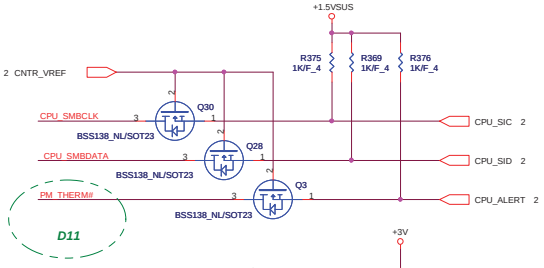
PROCESSOR POWER AND GROUND

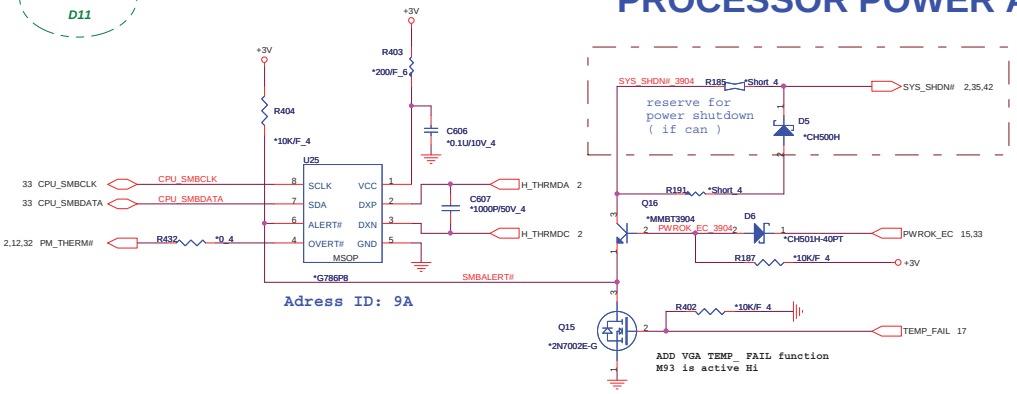




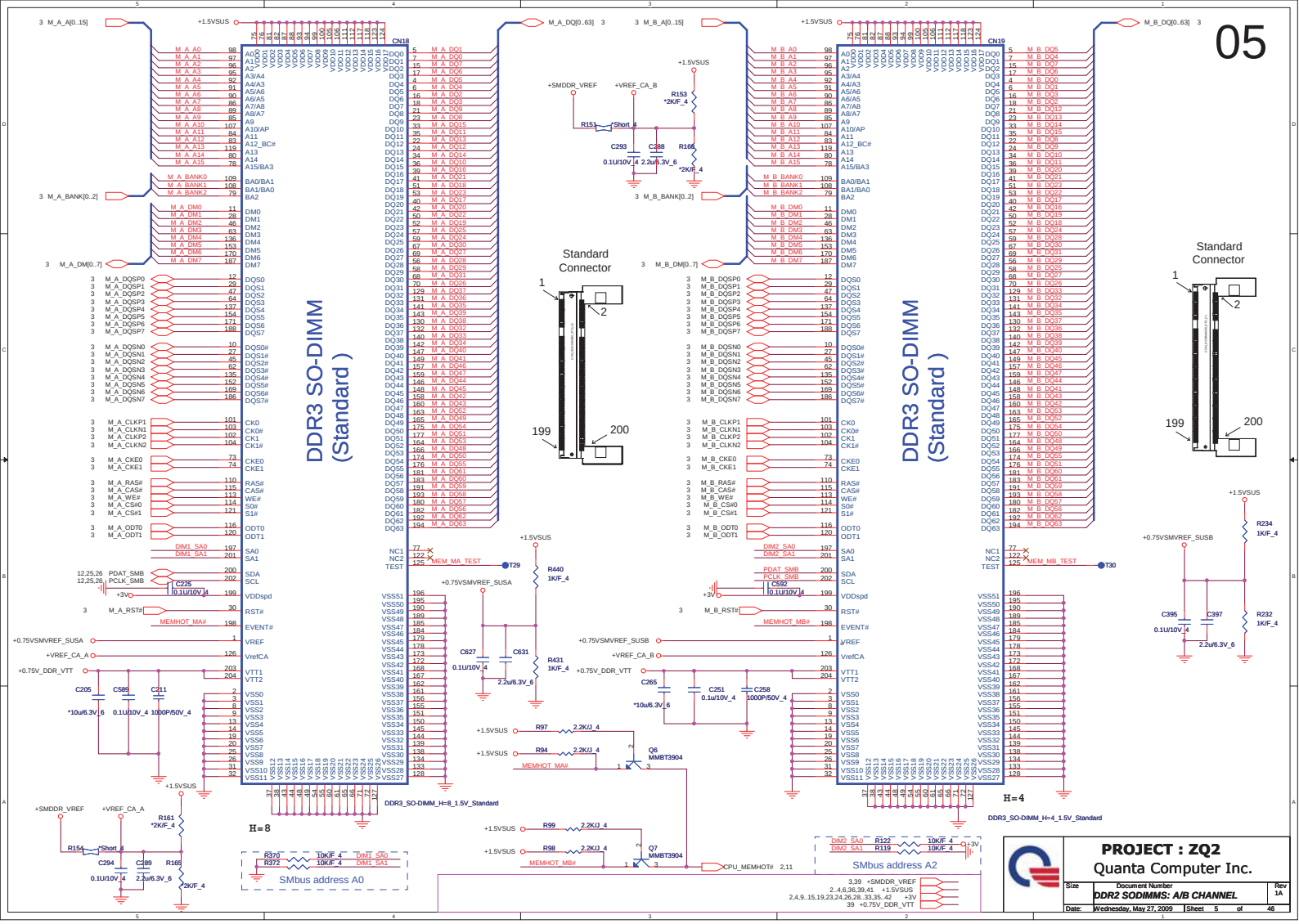




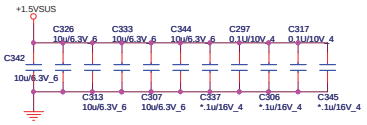




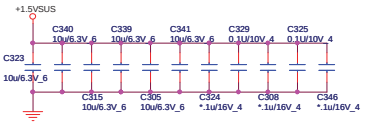
	PROJECT : ZQ2 Quanta Computer Inc.	
Size	Document Number **S1G4 PWR & GND 3/3**	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 4 of 46	



Place these Caps near So-Dimm H=8.



Place these Caps near So-Dimm H=4.



	PROJECT : ZQ2 Quanta Computer Inc.	
Size	Document Number *DDR3 SODIMMS TERMINATIONS*	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 6 of 46	

SIDE PORT

11/4

07

U22A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RS880/RX881

This block is for UMA only , Discrete can remove all component

U39

100-BALL SDRAM DDR3

SIDE@H5TQ1G63AFR-14C

U22D

PAR 4 OF 6

SIDE_PORT_MEM / DVO_I/F

RS880/RX881

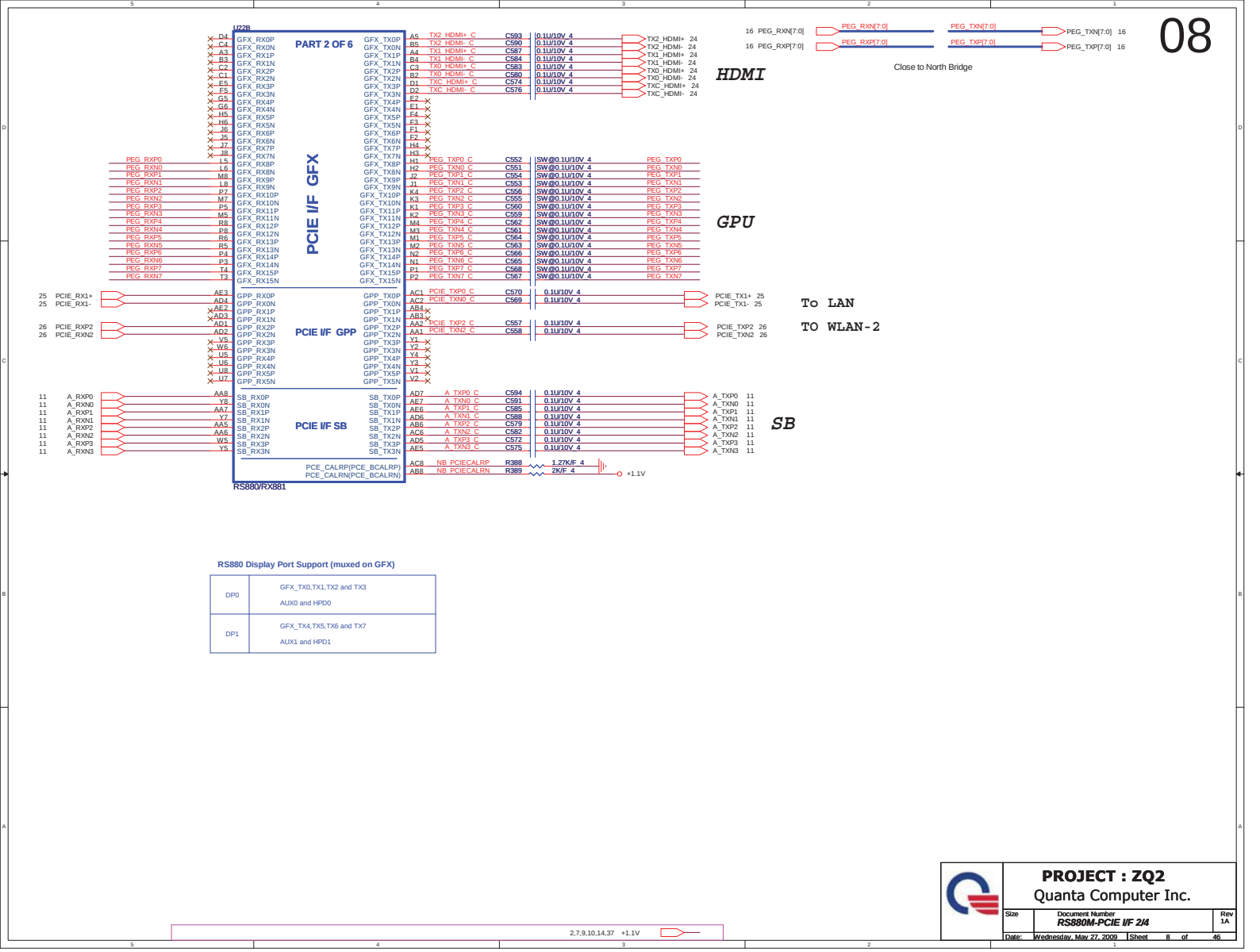
40 mil~50 mil

IOPLLVDD18 - memory PLL not applicable to RX881

	W/I SP	W/O SP
R583	1K	0
L75	Bead	0
L76	Bead	0

PROJECT : ZQ2
Quanta Computer Inc.

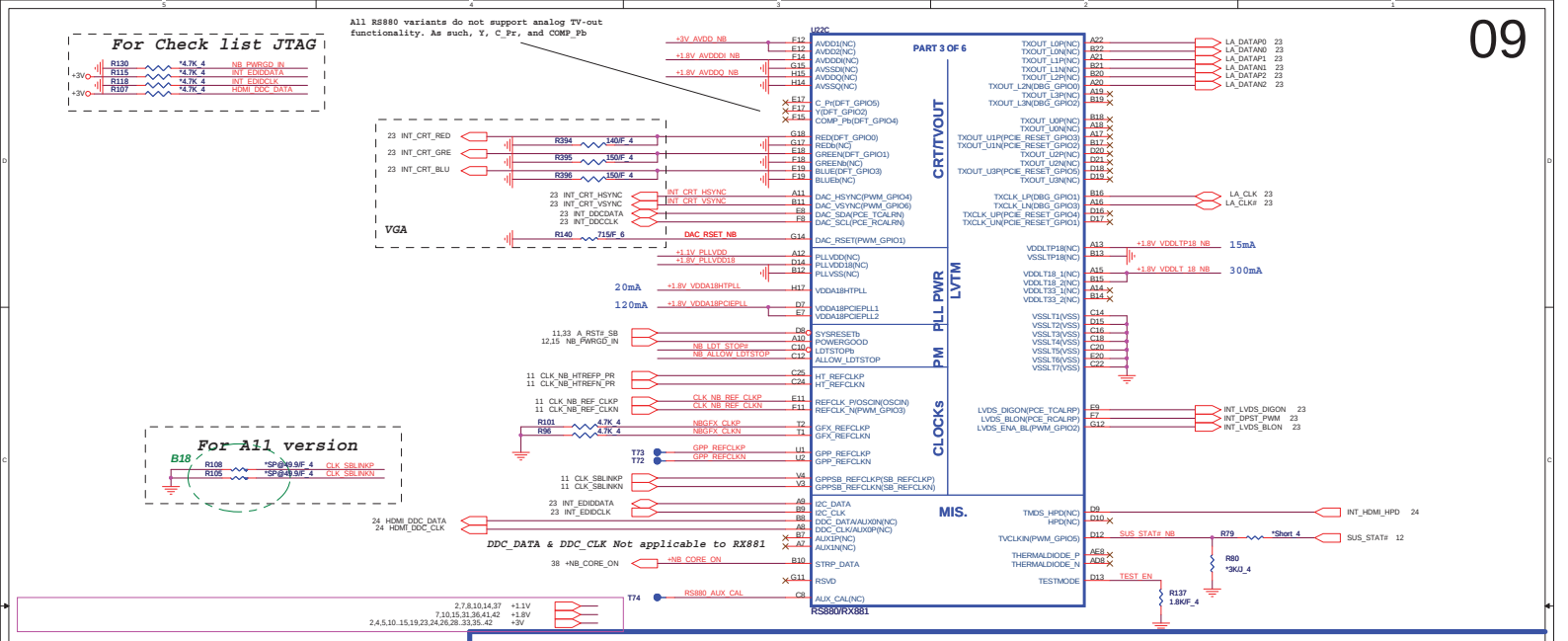
Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
Date: Wednesday, May 27, 2009	Sheet 7 of 46	

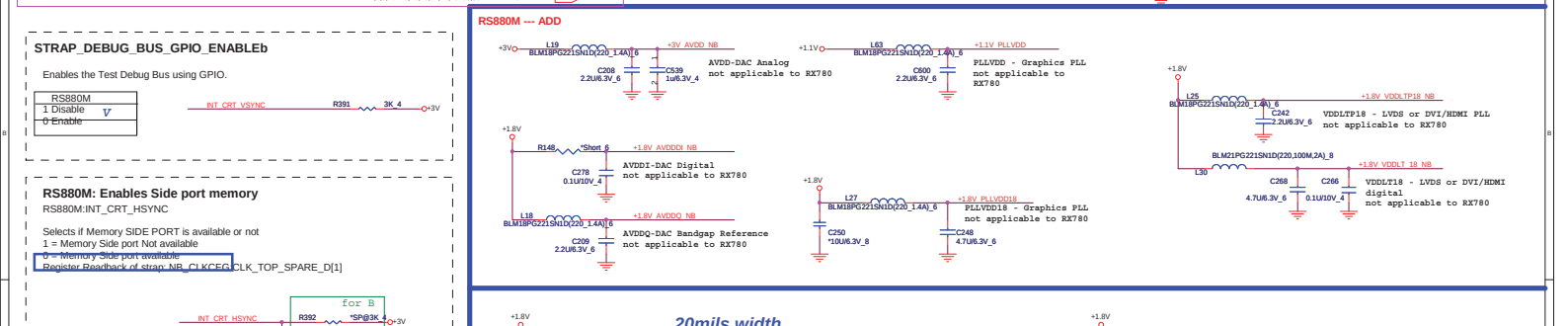


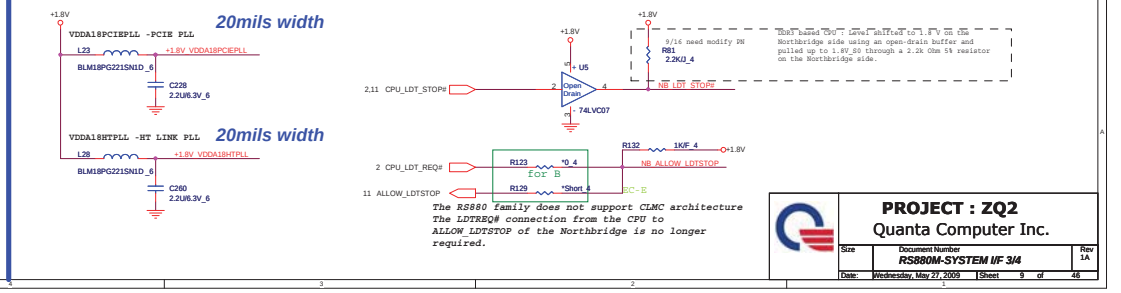
RS880 Display Port Support (muxed on GFX)

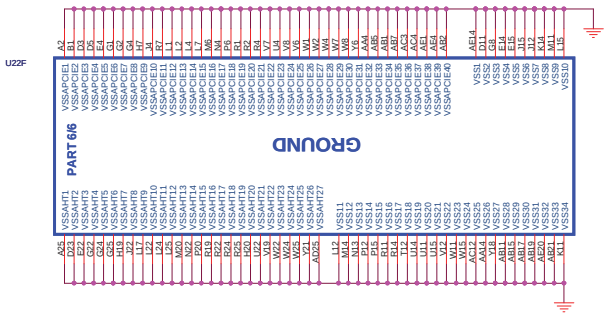
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

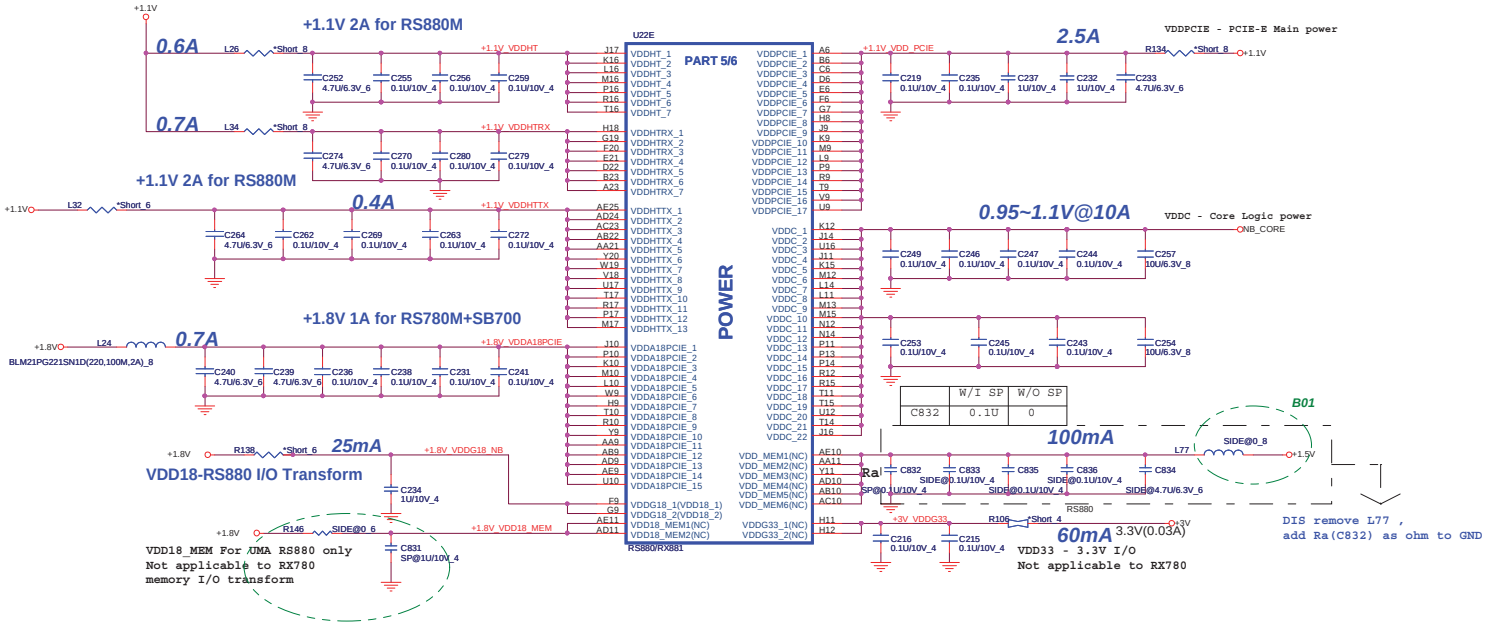
PROJECT : ZQ2			
Quanta Computer Inc.			
Size	Document Number: RS880M-PCIE I/F 2/4		Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 8 of 46		



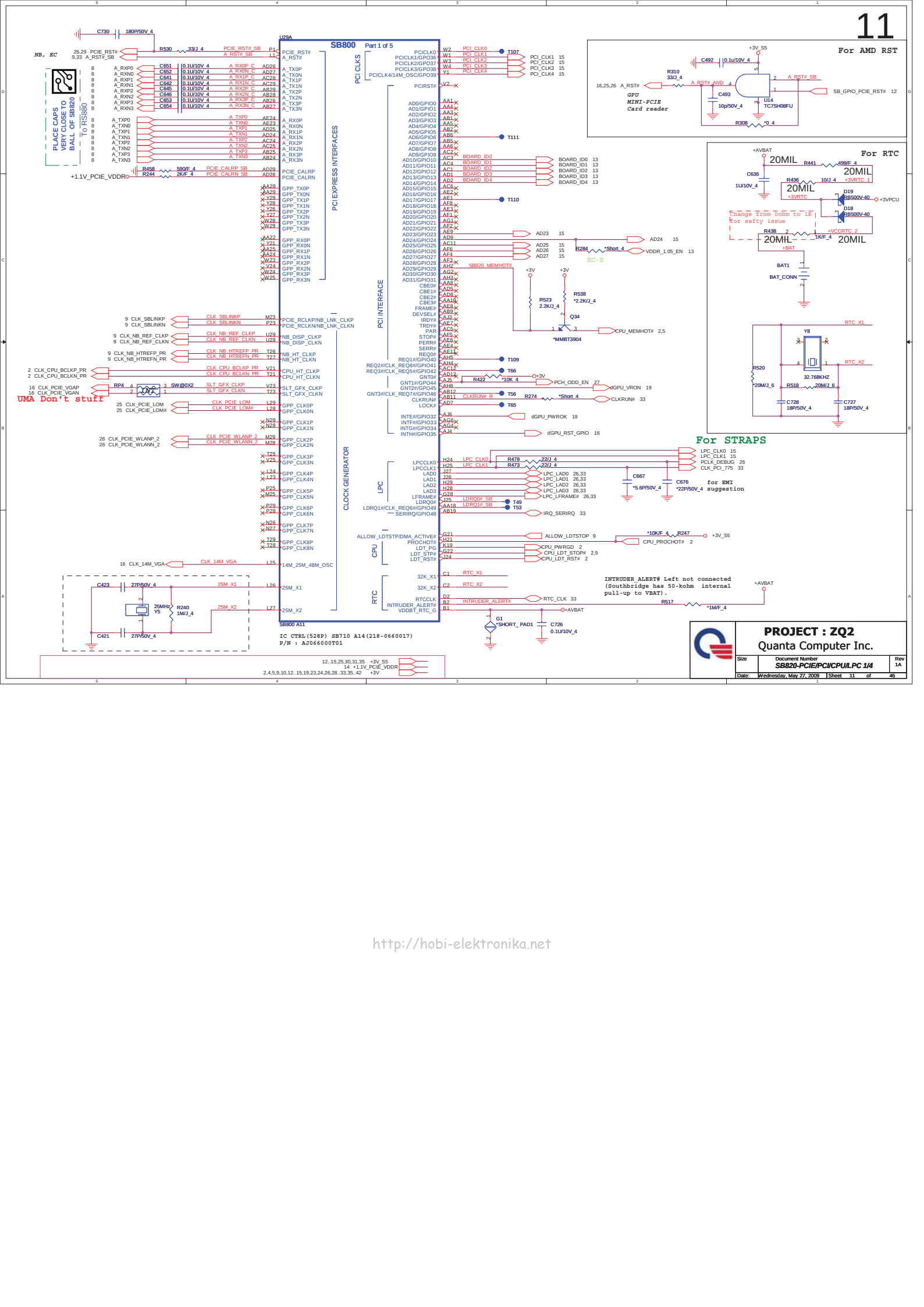








PROJECT : ZQ2
Quanta Computer Inc.
Size | Document Number: RS880M-POWER4/4 | Rev: 1A
Date: Wednesday, May 27, 2009 | Sheet 10 of 46



NC only ,Can't be install

+3V_S5 R514 *2.2K/J_4 SB_TEST0
R313 *2.2K/J_4 SB_TEST1
R305 *2.2K/J_4 SB_TEST2

11,13..15,25,30,31,35 +3V_S5
2,4,5,9..11,13..15,19,23,24,26,28..33,35..42 +3V

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

+3V SCL0/SDATA0 is 3V tolerance AMD datasheet define it — Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer
R249 2.2K/J_4 PCLK_SMB
R246 2.2K/J_4 PDAT_SMB

+3V_S5 SCL1/SDATA1 is 3V/S5 tolerance AMD datasheet define it
R287 10K_4 SB_SMBCLK1
R306 10K_4 SB_SMBDATA1

+3V_S5 SCL2/SDATA2 is 3V/S5 tolerance AMD datasheet define it
R252 10K_4 SB_SCLK2
R248 10K_4 SB_SDATA2

+3V
R296 4.7K/J_4 SUS_STAT#

+3V_S5 B05
R501 8.2K_4 CLK_PCIE_LAN_REQ#
R551 8.2K_4 CLK_PCIE_2_REQ#

U29D SB800 Part 4 of 5

T69 PCI_PME#/GEVENT4#
RI#/GEVENT22#
33 SUSB# SPI_CS3#/GBE_STAT1/GEVENT21#
33 SUSC# SUSC# SLP_S3#
33 DNBSWON# SLP_S5#
15 SB_PWRGD_IN PWR_BTN#
9 SUS_STAT# PWR_GOOD
SUS_STAT#
SB_TEST0 TEST0
SB_TEST1 TEST1/TMS
SB_TEST2 TEST2
33 SIO_A20GATE GA20IN/GEVENT0#
33 SIO_RCIN# SIO_RCIN# KBRST#/GEVENT1#
T105 LANLINK_STATE# LPC_PME#/GEVENT3#
33 SIO_EXT_SMI# LPC_SMI#/GEVENT23#
33 SIO_EXT_SCI# GEVENT8#
T108 SYS_RST# SYS_RESET#/GEVENT19#
25,26 PCIE_WAKE# WAKE#/GEVENT8#
IR_RX1 IR_RX1/GEVENT20#
T106 R295 *Short_4 SB_THERMTRIP# THRMTRIP#/SMBALERT#/GEVENT2#
2 CPU_THERMTRIP#
9,15 NB_PWRGD_IN NB_PWRGD
33 ICH_RSMRST# RSMRST#

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N

A10 USB_14_48M T83
G19 USB_RCOMP_SB R270 11.8K/F_6
J10 H11
H9 USB_FDS12P T62
J8 USB_FDS12N T58

USB_HSD13P B12 USBP13+ 23 CAMERA EC-C
USB_HSD13N A12 USBP13- 23
USB_HSD12P F11 USBP12+ 30 USBX3 board
USB_HSD12N E11 USBP12- 30
USB_HSD11P E14 USBP11+ 30 USBX3 board
USB_HSD11N E12 USBP11- 30
USB_HSD10P J12 USBP10+ 29 Card reader EC-C
USB_HSD10N J14 USBP10- 29
USB_HSD9P A13 USBP9+ 30 BLUETOOTH
USB_HSD9N B13 USBP9- 30
USB_HSD8P D13 USBP8+ 30 USBX3 board EC-C
USB_HSD8N C13 USBP8- 30
USB_HSD7P G12
USB_HSD7N G14
USB_HSD6P G16
USB_HSD6N G18
USB_HSD5P D16
USB_HSD5N C16 EC-C
USB_HSD4P B14 USBP4+ 26 WLAN Min-Card
USB_HSD4N A14 USBP4- 26
USB_HSD3P E18
USB_HSD3N E16
USB_HSD2P J16
USB_HSD2N J18
USB_HSD1P B17 T55
USB_HSD1N A17 T54
USB_HSD0P A16 USBP0+ 30 On Board USB Connector
USB_HSD0N B16 USBP0- 30

Only USB Port0 can be configured as debug port.

GPIO
USB 2.0

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN

11 SB_GPIO_PCIE_RST# SB_GPIO_PCIE_RST#
25 CLK_PCIE_LAN_REQ#
19 dGPU_PWR_EN
T51 SB_GPIO59
28 SPKR
5,25,26 PCLK_SMB PCLK_SMB
5,25,26 PDAT_SMB PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
26 CLK_PCIE_2_REQ#
17 VGA_REQ# R427 *Short_4A_REQ#_GPIO61
EC-E
7 SP_DDR3_RST#

11/04 need check
T118 E_SB_OSC

USB OC

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#

30 OC_7#
30 OC_6#
2,4,32 PM_THERM#
30 OC_4#
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

HD audio interface is +3VS5 voltage

15 ACZ_SDOUT R533 *10K_4 ACZ_BCLK
ACZ_SDOUT
R535 *10K_4 ACZ_SDIN0
R294 *10K_4 ACZ_SDIN1
R304 *10K_4 ACZ_SDIN2
R292 *10K_4 ACZ_SDIN3
ACZ_SYNC
ACZ_RST#

HD AUDIO

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_GPIO195
SDA3_LV/GPIO196 E26 SB_GPIO196
EC_PWM0/EC_TIMER0/GPIO197 F25 T122
EC_PWM1/EC_TIMER1/GPIO198 F22
EC_PWM2/EC_TIMER2/GPIO199 F22 GPIO199 15
EC_PWM3/EC_TIMER3/GPIO200 E21 GPIO200 15

+3V_S5
R301 10K_4 GBE_COL
R291 10K_4 GBE_CRS
R293 10K_4 GBE_MDIO
D03
R300 10K_4 GBE_RXERR
R290 10K_4 GBE_PHY_INTR

GBE LAN

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

EMBEDDED CTRL

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226

T50 ADP_PRES0

EMBEDDED CTRL

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPIO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

SB800 A11

To Azalia

ACZ_SDOUT R532 33/J_4 ACZ_SDOUT_AUDIO 28
C732 *10P/50V_4
ACZ_SYNC R531 33/J_4 ACZ_SYNC_AUDIO 28
C731 *10P/50V_4
ACZ_BCLK R534 33/J_4 ACZ_BITCLK_AUDIO 28
C733 *10P/50V_4
ACZ_RST# R529 33/J_4 ACZ_RST#_AUDIO 28
ACZ_SDIN0 ACZ_SDIN0 28

+3V_S5
CN12
C485 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG
JTAG DEBUG

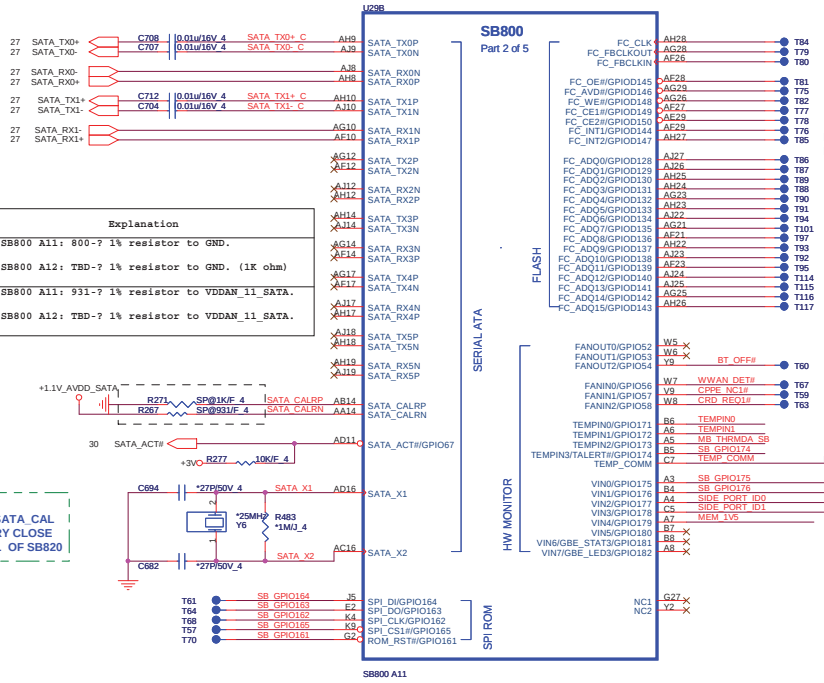
Check list
SB_GPIO195 R245 10K/F_4
SB_GPIO196 R243 10K/F_4

PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number SB820-ACPI/GPIO/USB 2/4
Rev 1A
Date: Wednesday, May 27, 2009 Sheet 12 of 46

SATA PORT 0,1,2,3 can support AHCI mode

SATA HDD

SATA ODD



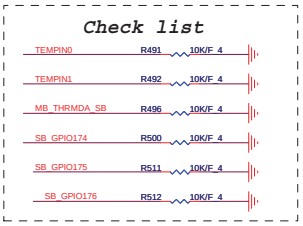
Signal Name	Explanation
SATA_CALRP	SB800 A11: 800-? 1% resistor to GND. SB800 A12: TBD-? 1% resistor to GND. (1K ohm)
SATA_CALRN	SB800 A11: 931-? 1% resistor to VDDAN_11_SATA. SB800 A12: TBD-? 1% resistor to VDDAN_11_SATA.

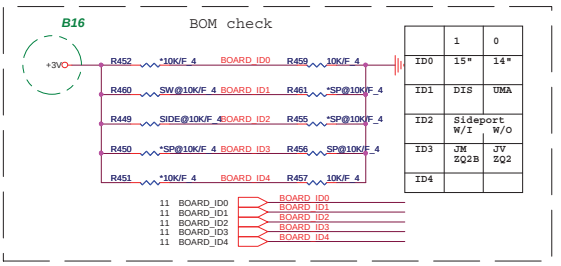
E-SATA

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

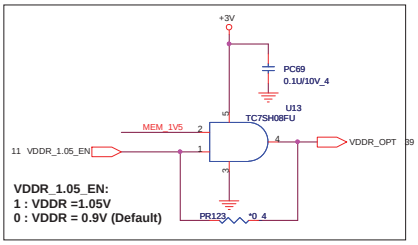
IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

Check list



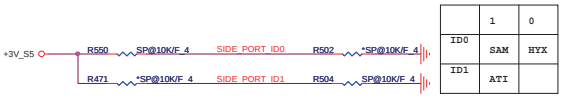


	1	0
ID0	15"	14"
ID1	DIS	UMA
ID2	Sideport W/I	Sideport W/O
ID3	JM ZQ2B	JV ZQ2
ID4		



VDDR_1.05_EN:
1 : VDDR =1.05V
0 : VDDR = 0.9V (Default)

DDR3 Sideport Memory Device

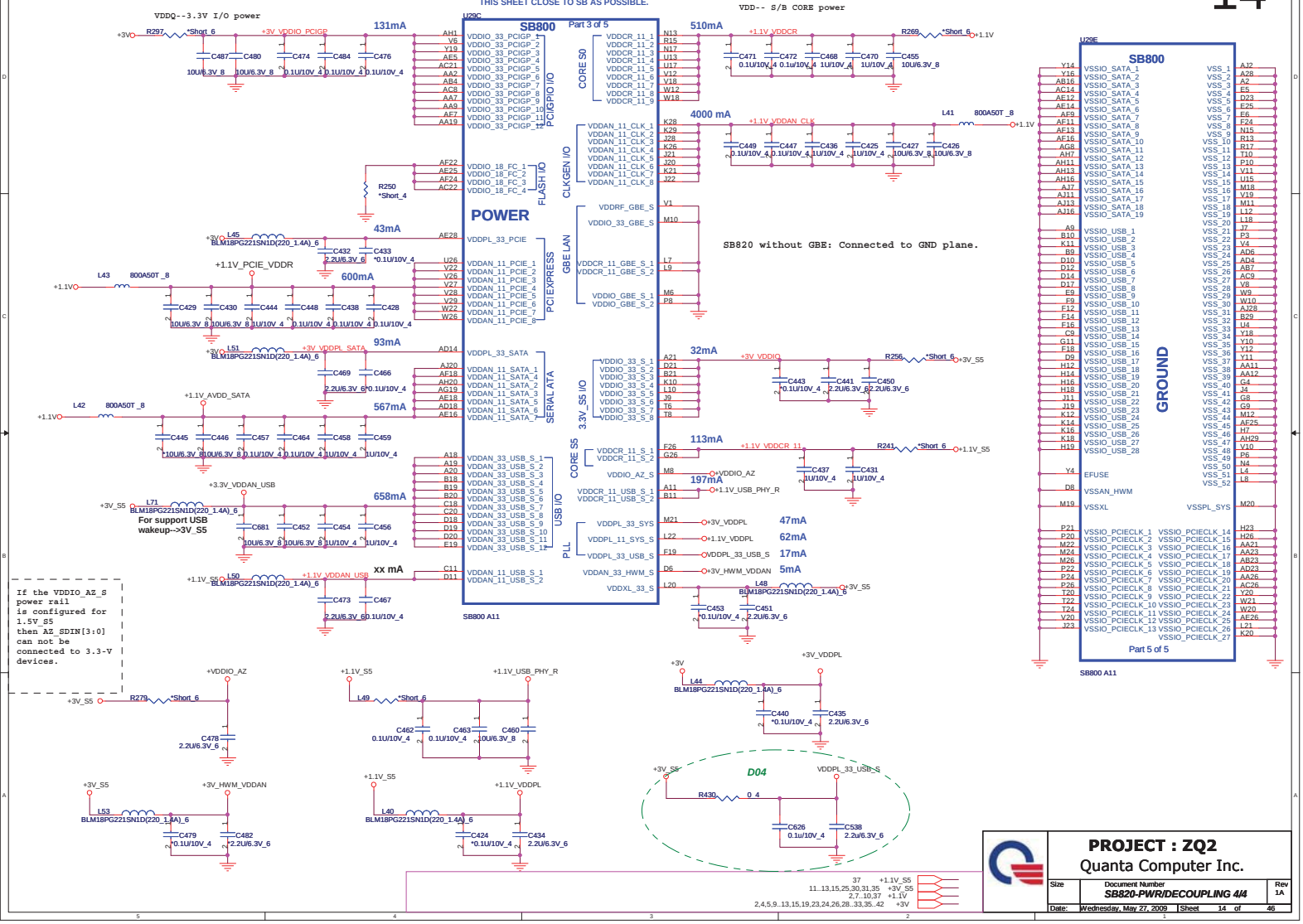


	1	0
ID0	SAM	HYX
ID1	ATI	

Vendor	Vendor P/N	STN B/S P/N	BOARD_ID2 GPIO12	SIDE_PORT_ID1 GPIO178	SIDE_PORT_ID0 GPIO177
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1 (W/Sideport)	0	1
ATI	23EY2387MA12-SZ	AKD5LGGT700 (64M*16)	1 (W/Sideport)	1	0

PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number: SB820-SATA/IDE/SPI 3/4	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 13 of 46	

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.



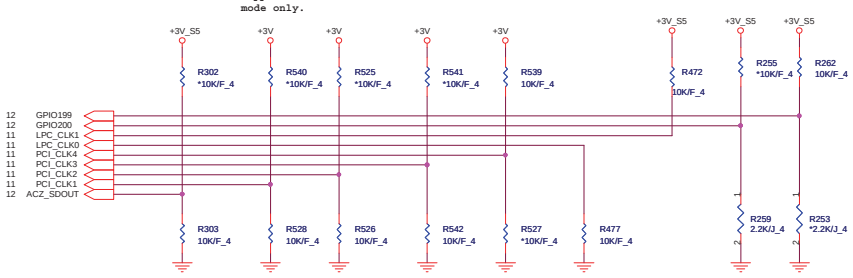
PROJECT : ZQ2	
Quanta Computer Inc.	
Size	Document Number: SB820-PWR/DECOUPLING 4/4 — Rev 1A
Date: Wednesday, May 27, 2009	Sheet 14 of 46

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

SB820M is supported Gen1 mode only.

For internal clock GEN.



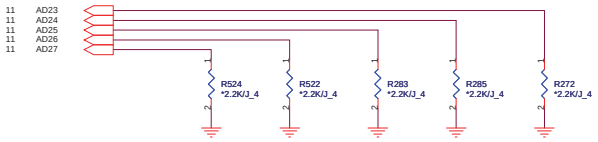
11..14,25,30,31,35 +3V_S5
7,9,10,31,36,41,42 +1.8V
2,4,5,9..14,19,23,24,26,28..33,35..42 +3V

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
D02 PULL HIGH	This is required as the low power mode is not supported on the SB8xx	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K

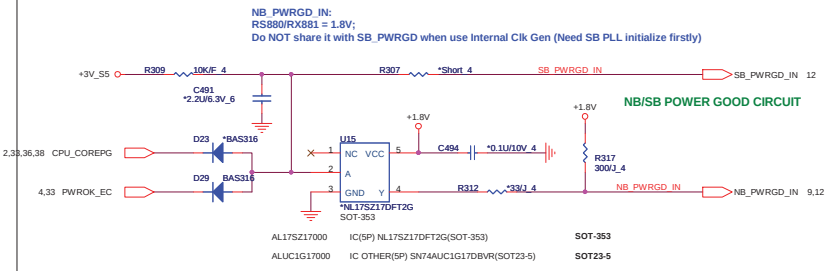
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

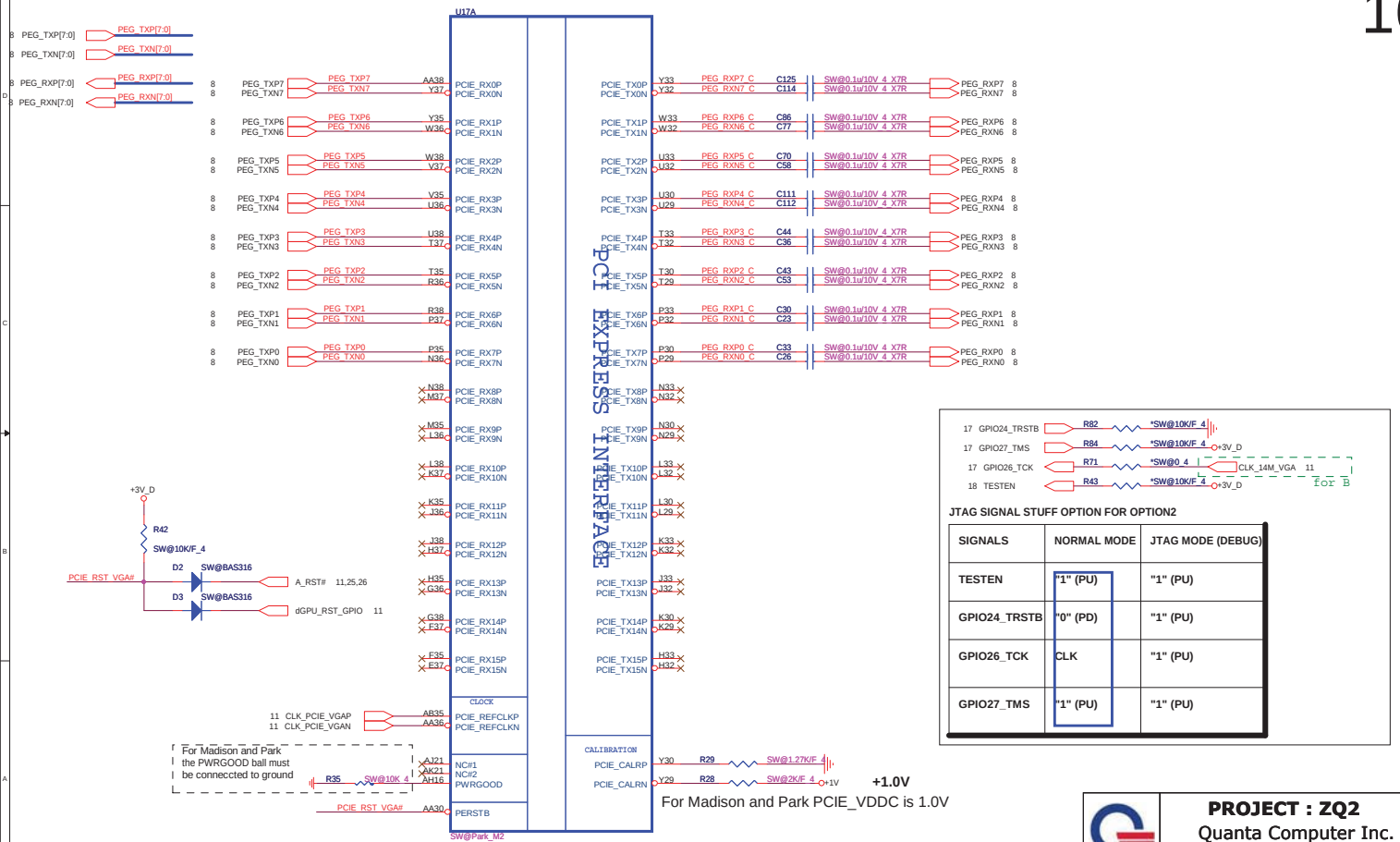
NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-STRAPS	1A

Date: Wednesday, May 27, 2009 Sheet 15 of 46



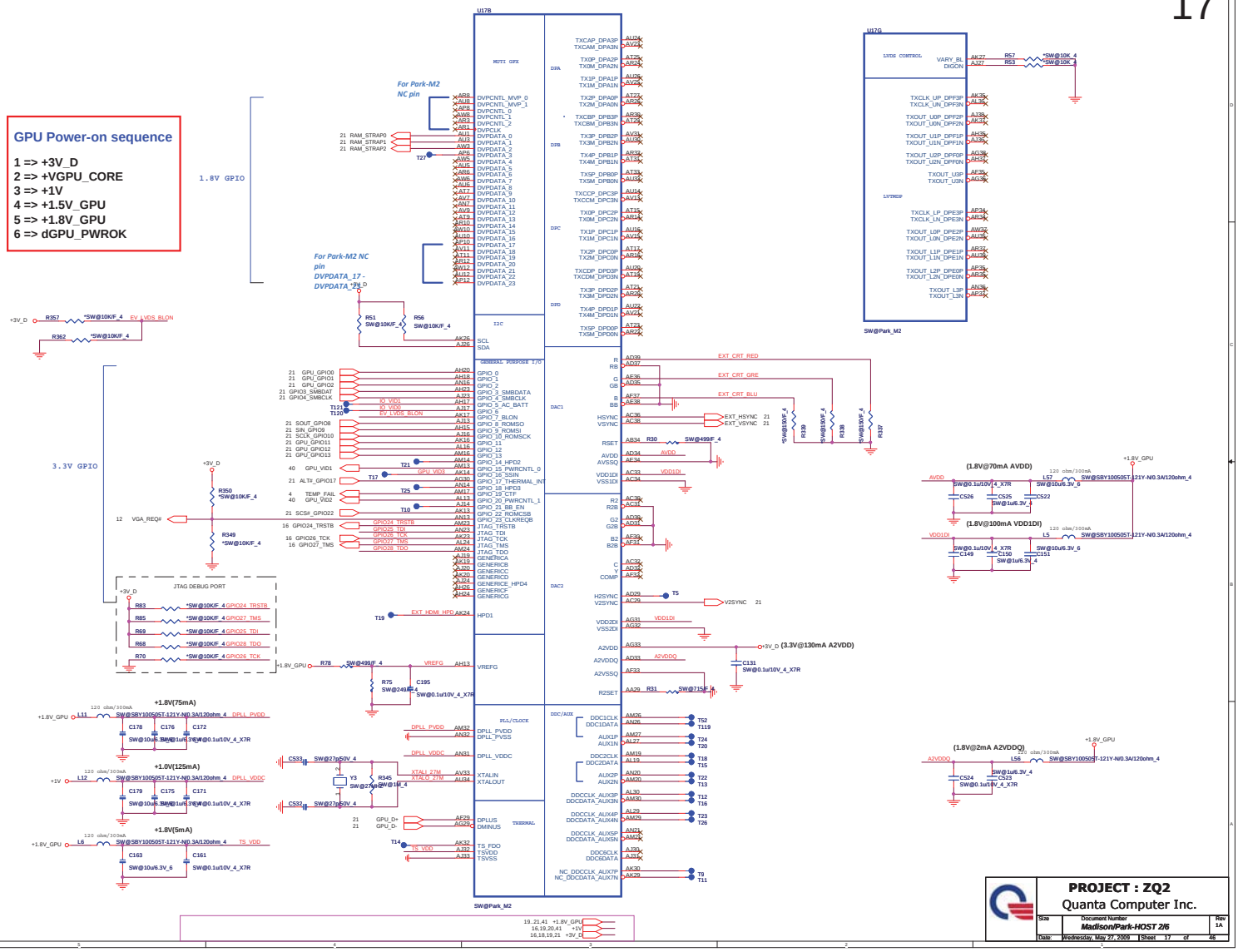
SIGNALS	NORMAL MODE	JTAG MODE (DEBUG)
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)

PROJECT : ZQ2
Quanta Computer Inc.

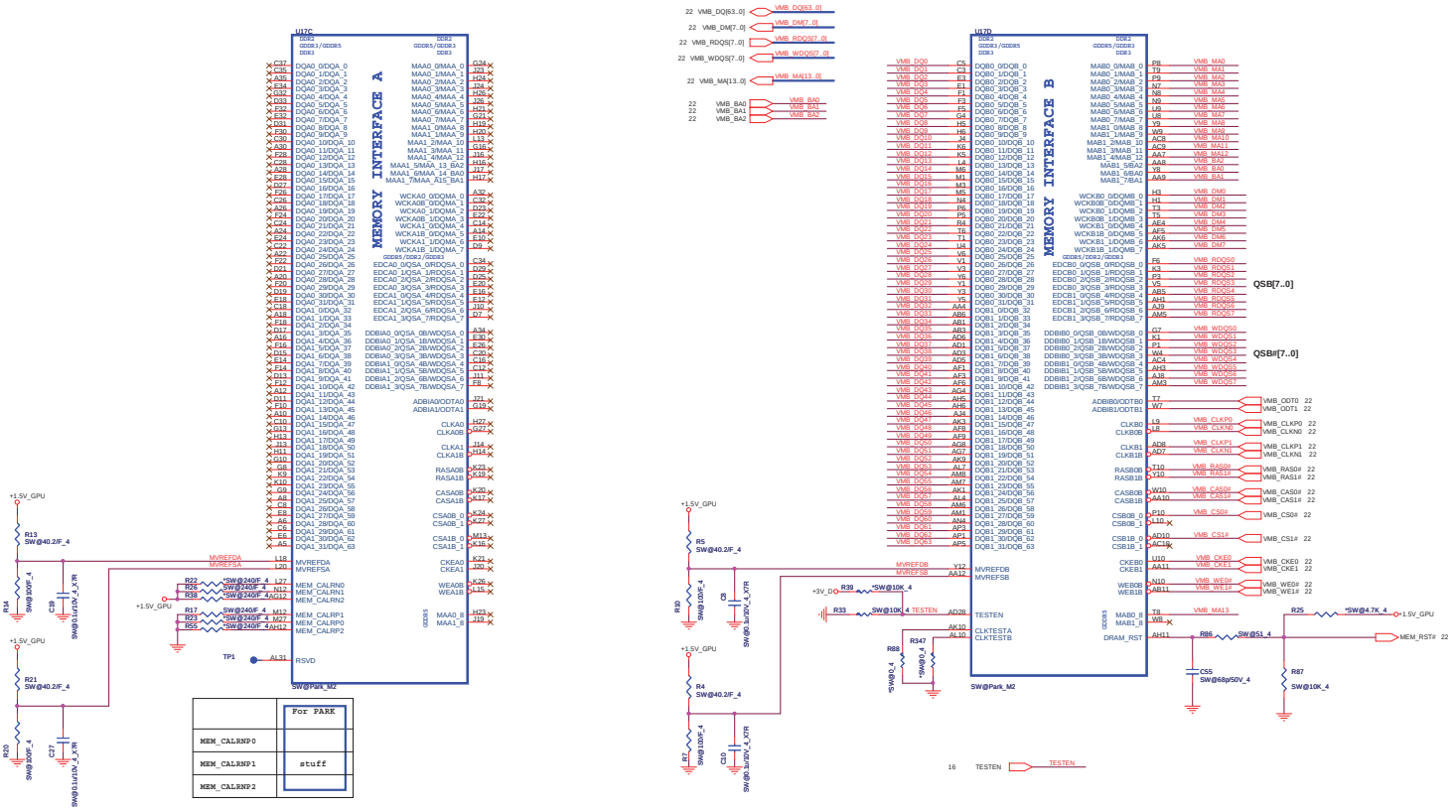
Size	Document Number	Rev
	Madison/Park-PCIE 1/6	1A
Date: Wednesday, May 27, 2009	Sheet 16 of 46	

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => dGPU_PWROK



PROJECT : ZQ2	
Quanta Computer Inc.	
Size	Document Number: Madison/Park-HOST 2/6 — Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 17 of 46



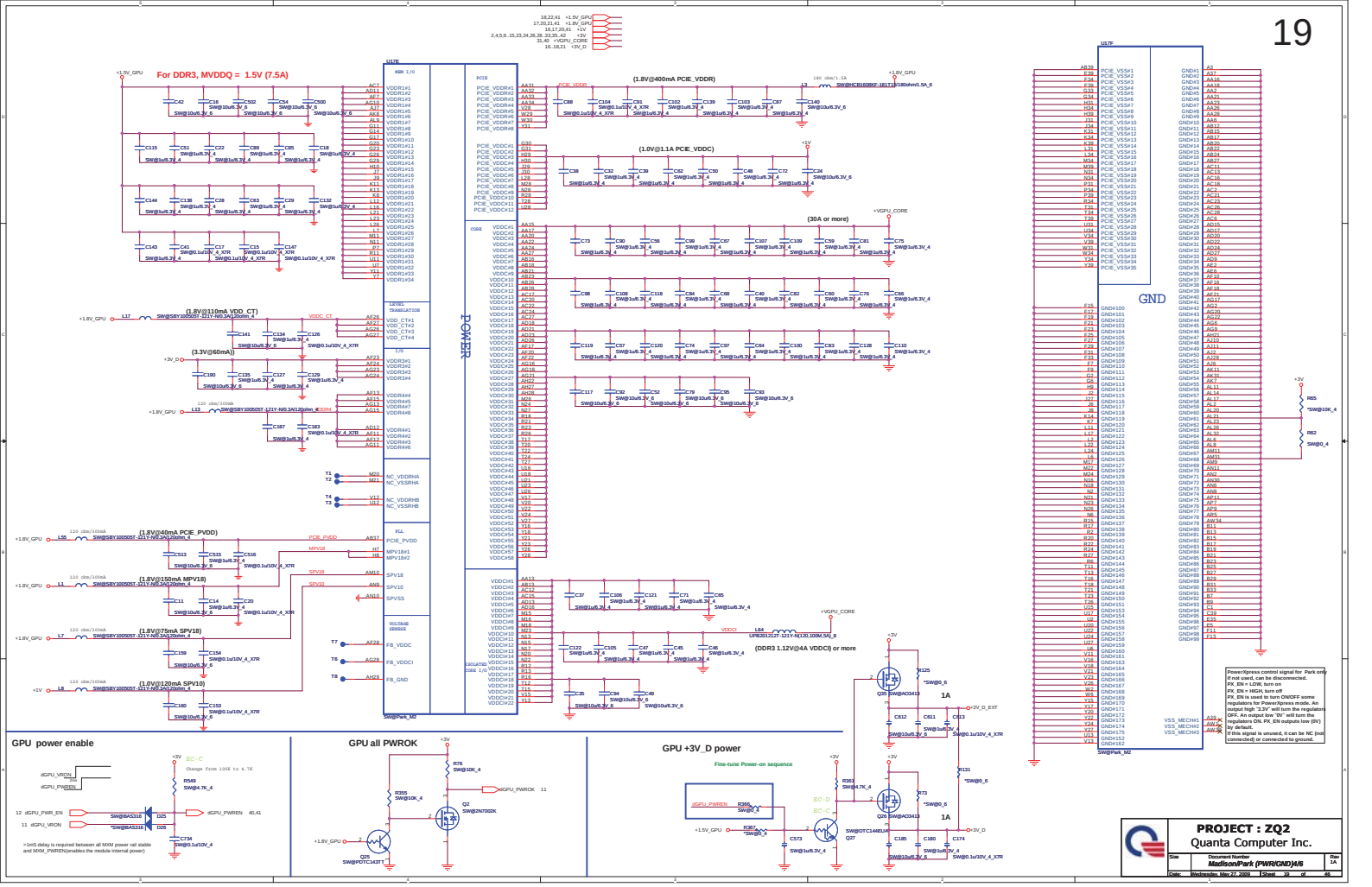
	For PARK
MEM_CALRNP0	
MEM_CALRNP1	stuff
MEM_CALRNP2	

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

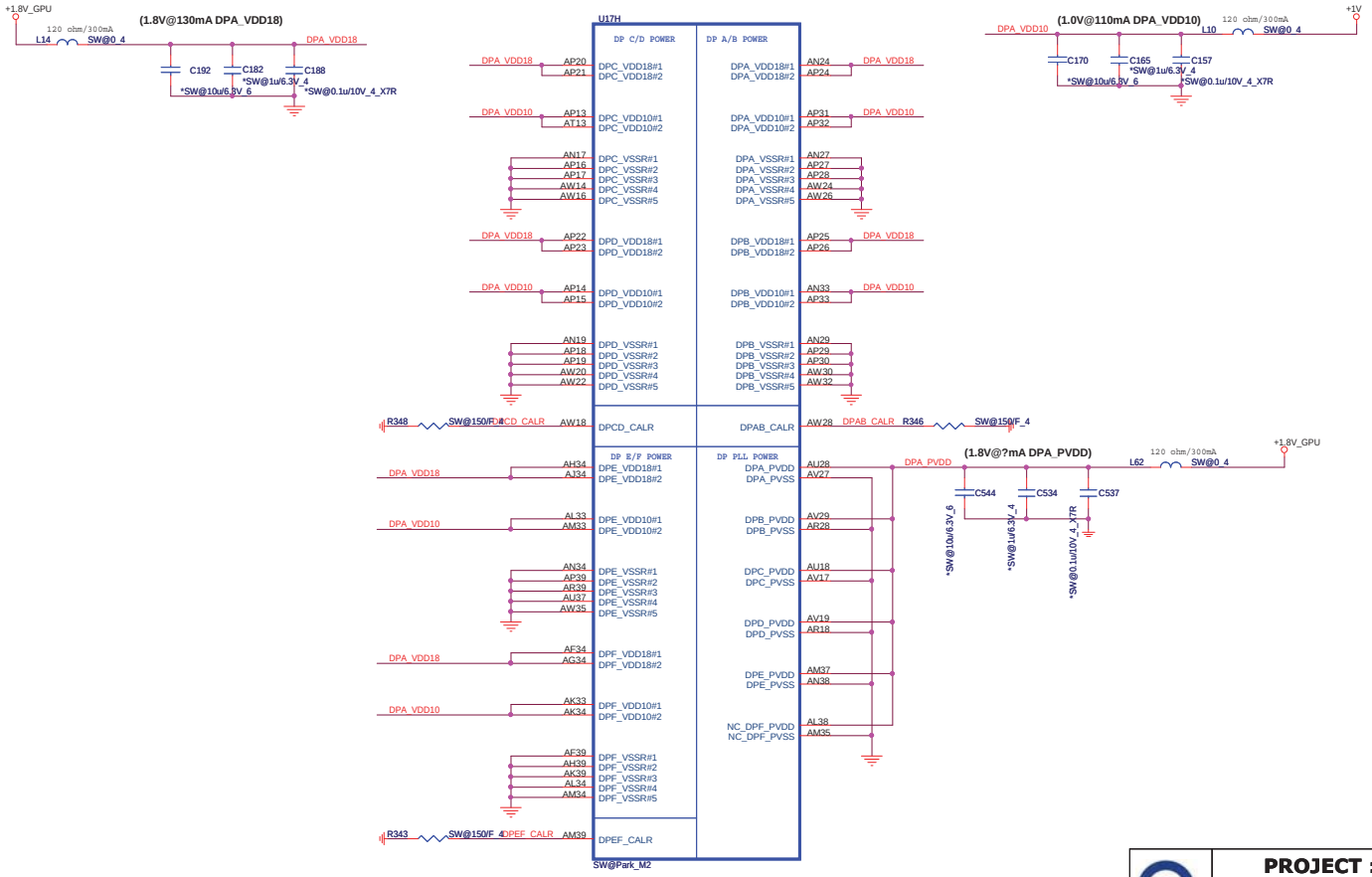
Designator	For M97-M2	For Mannhatton
Ra	10K	10K
Rb	0R/Short	680R
Rc	DNI	DNI
Ca	2.2nF	68pF

PROJECT : ZQ2
Quanta Computer Inc.
Size | Document Number: Madison/Park-MEM 3/6 | Rev: 1A
Date: Wednesday, May 27, 2009 | Sheet 18 of 46



PowerXpress control signal for Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high "3.3V" will turn the regulators OFF. An output low "0V" will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.

PROJECT : ZQ2	
Quanta Computer Inc.	
Size	Document Number: Madison/Park (PWR/GND)4/6
Rev: 1A	
Date: Wednesday, May 27, 2009	Sheet 19 of 46



PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	Madison/Park (DP_PWR/GND)5/6	1A
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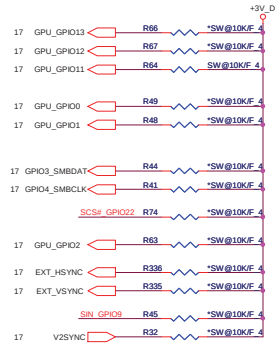
PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

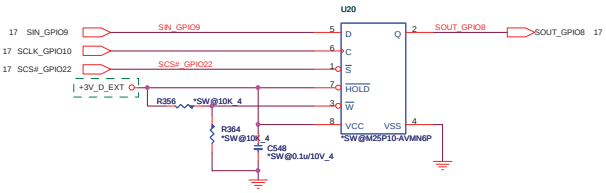
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

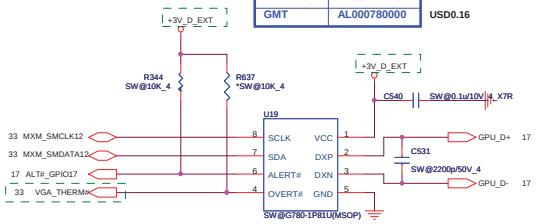
EEPROM



Thermal Sensor

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16



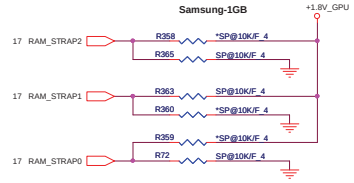
Address ID: 98H

DDR3 Memory Aperture size

DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	GPU	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	Park	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	Madison	1	0	0
			2Gb	1	1	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	Park	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	Madison	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2Gb	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	Park	0	1	1
	23EY2387MA12-SZ	AKD5LGGT700	Madison	1	0	1

D09



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Medison/Park Strip/Thermal 6/6	1A
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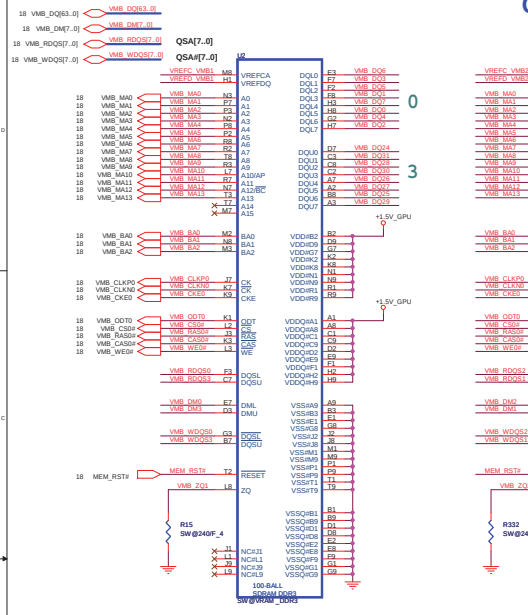
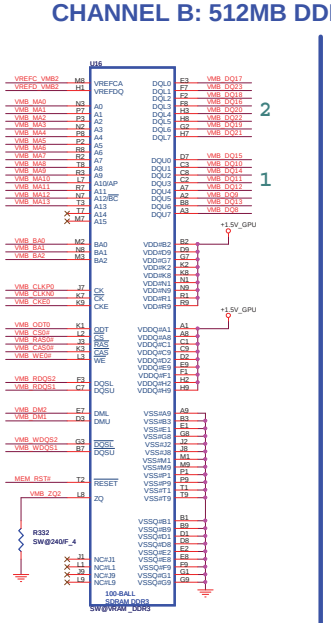
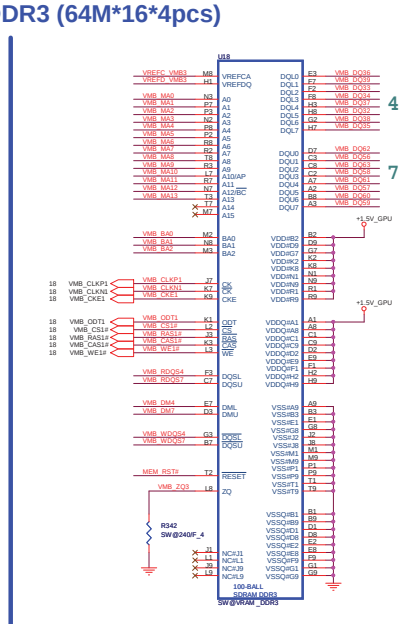
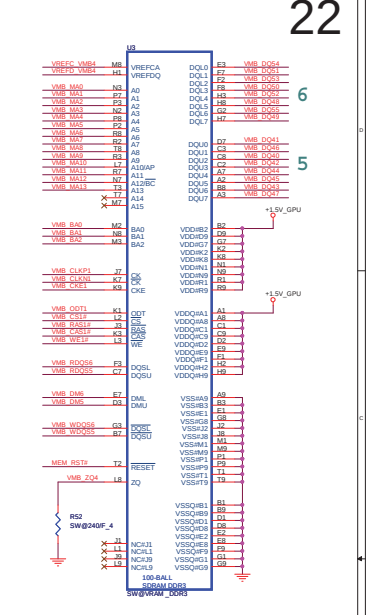
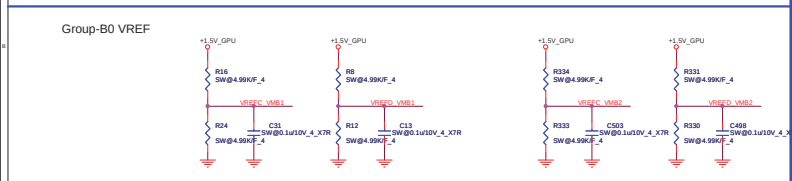
CHANNEL B: 512MB DDR3 (64M*16*4pcs)

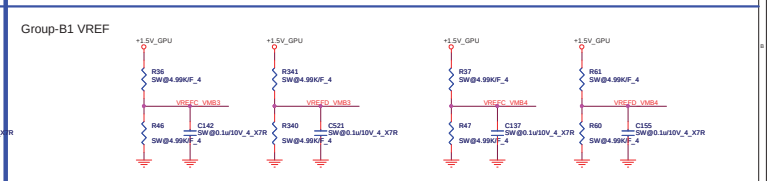


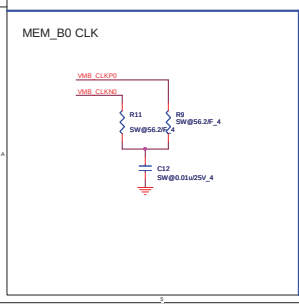


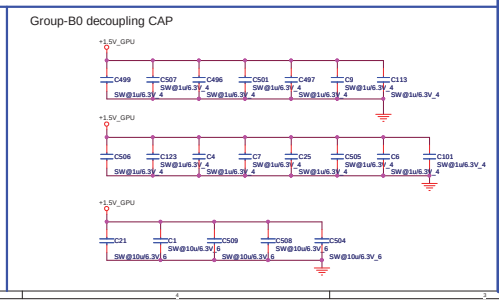


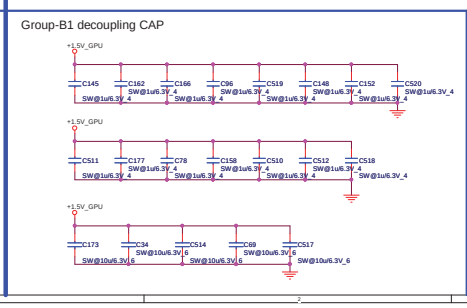


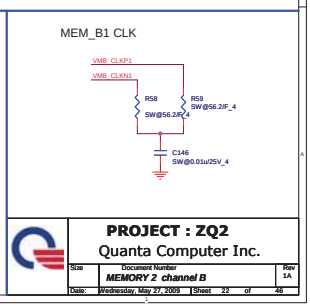












PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	MEMORY 2 channel B	1A
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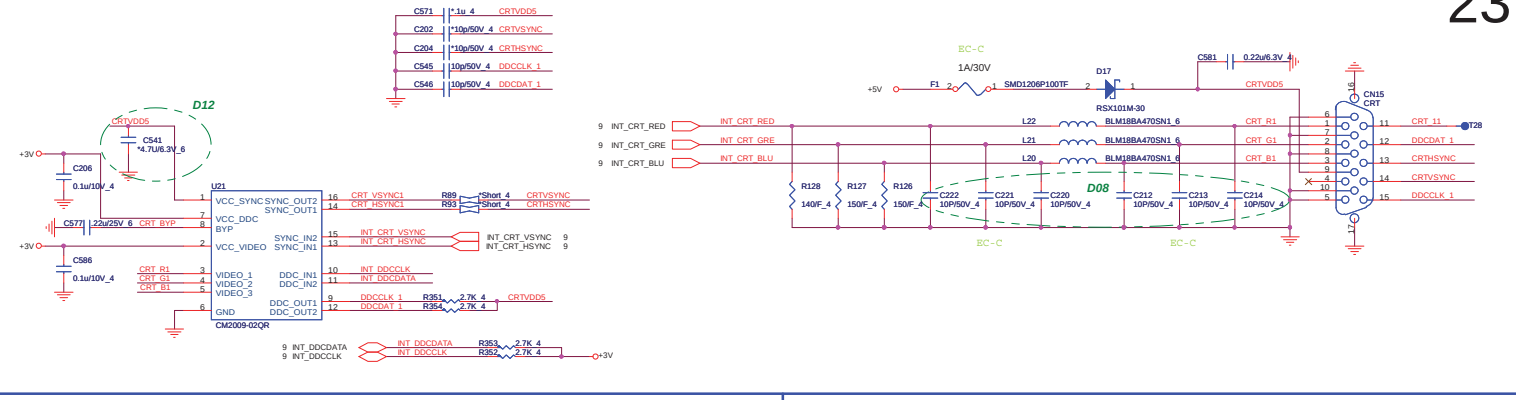
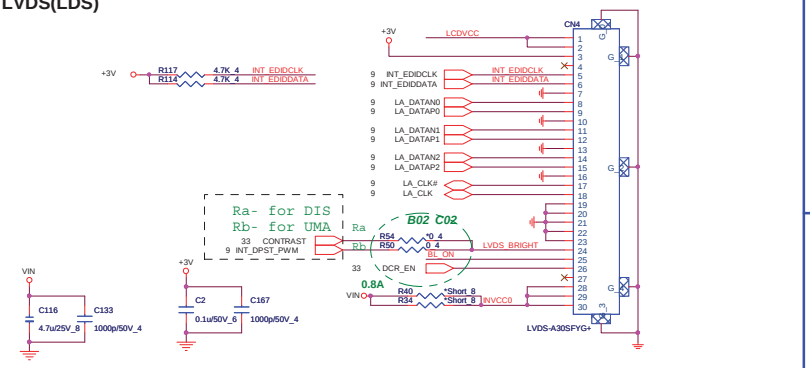
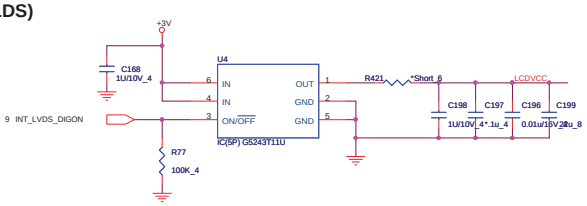
CRT



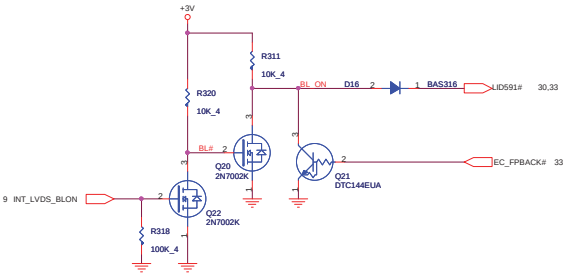
LVDS(LDS)



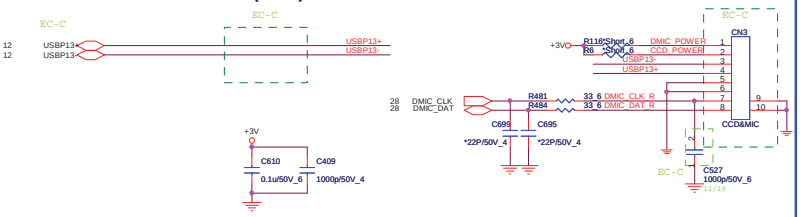
LCD PW(LDS)



Backlight Control(LDS)



CAMERA Module(CCD)



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS/LID	1A

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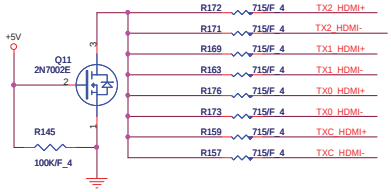
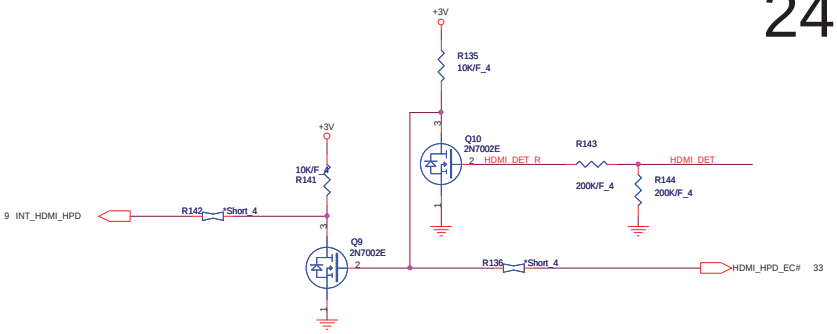
(HDM)

Close to HDMI Connector



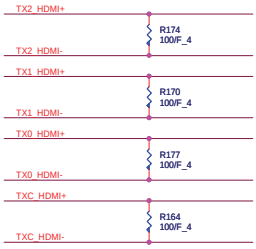
USE RS880M to display the HDMI
Stuff 715 ohm P/N--> CS17152FB17

HDMI HPD SENSE



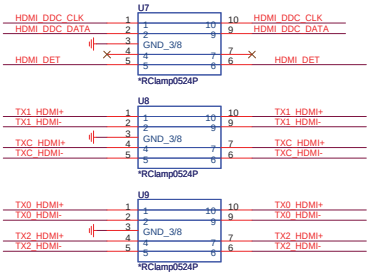
EMI reserve for HDMI(HDM)

Close connector

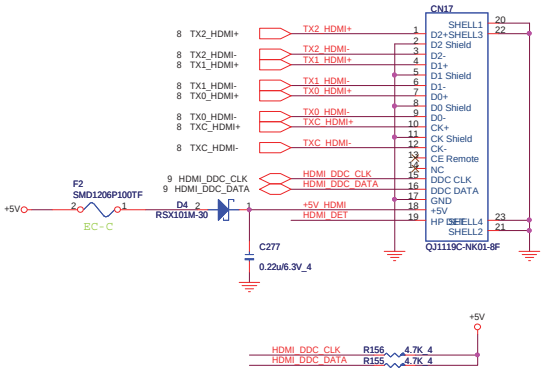


ESD Protect

close to HDMI connector



HDMI PORT

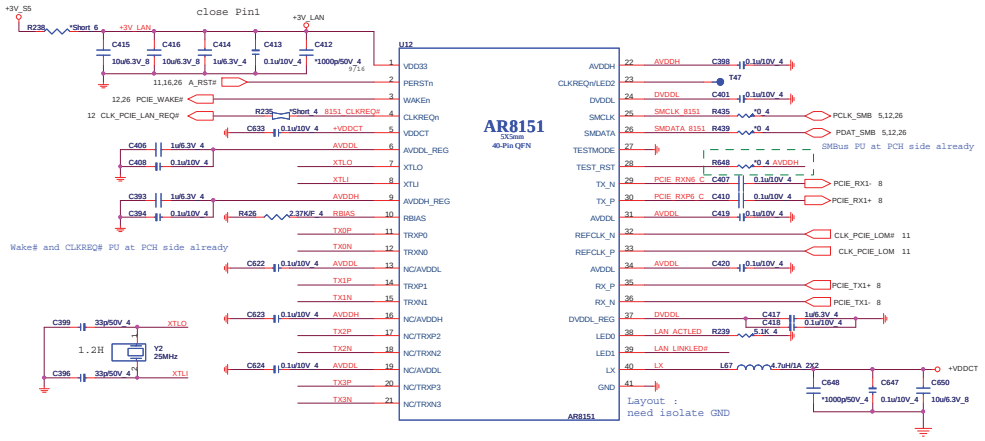


+5V 23,27,28,32,35,42
+3V 2,4,5,9..15,19,23,26,28..33,35..42

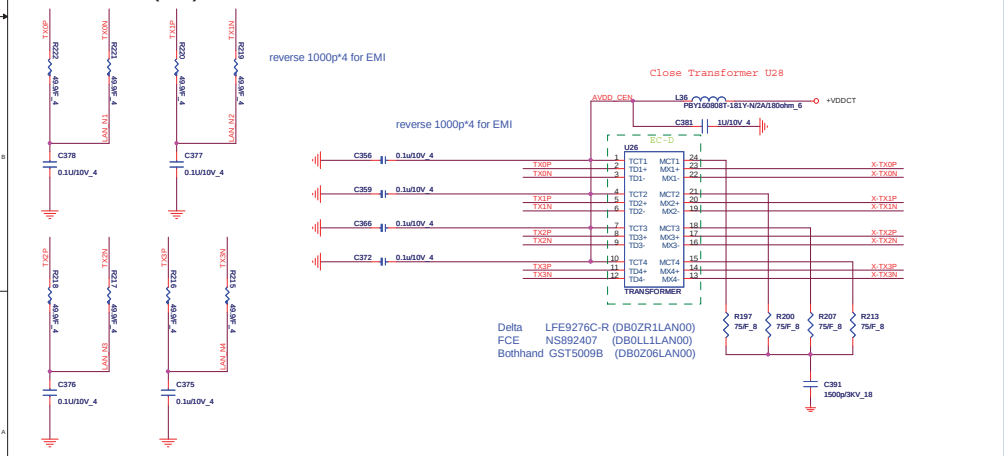
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI	1A
Date: Wednesday, May 27, 2009	Sheet 24 of 46	

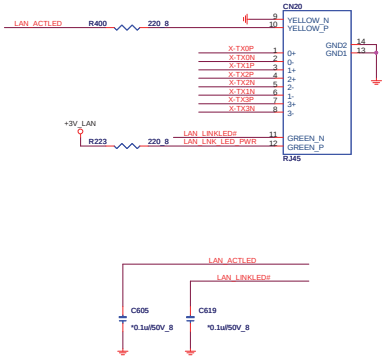
Giga-LAN AR8151



TRANSFORMER(LAN)



RJ45(LAN)



PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number	Rev
	LAN (AR8151)	1A
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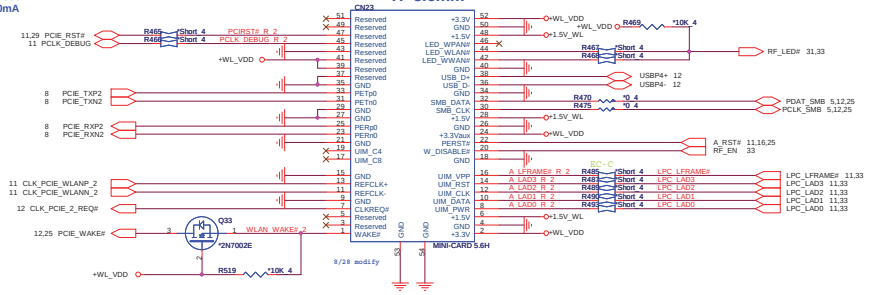
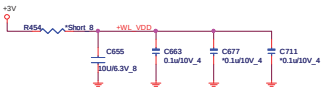
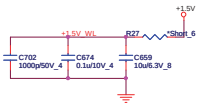
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

H=5.6mm

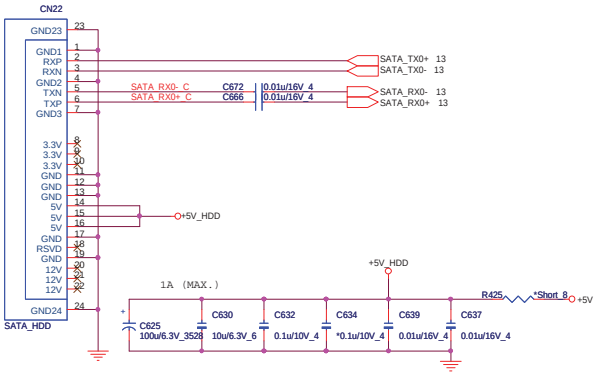




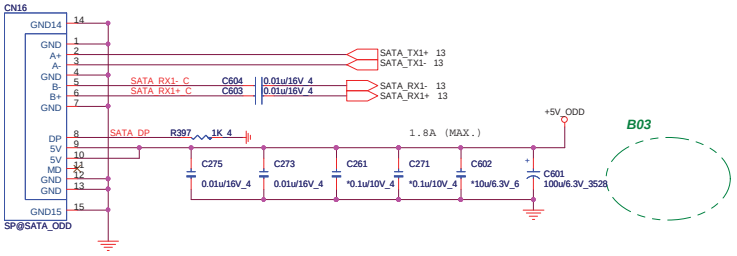


PROJECT : ZQ2			
Quanta Computer Inc.			
Size	Document Number		Rev
	Mini-Card/WL		1A
Date: Wednesday, May 27, 2009	Sheet 26 of 46		

SATA HDD(HDD)



SATA ODD (ODD)



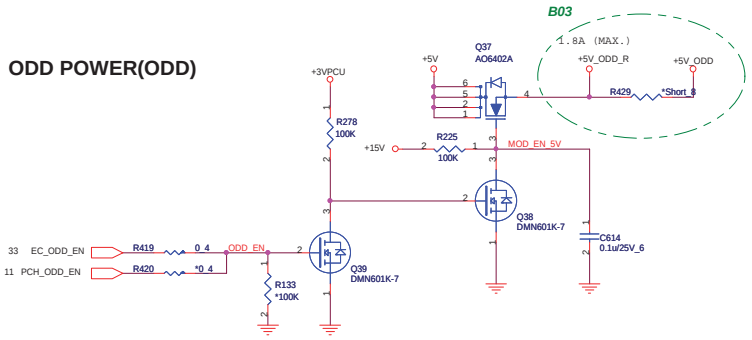
JV-12.7mm(H=5.5mm)-ZQ2

Main	DFHS13FR017	
Second	DFHS13FR006,	DFHS13FR005

JM-9.5mm(H=2.4mm)-ZQ2B

Main	DFHS13FR078,	DFHS13FR077
Second	DFHS13FR075	

ODD POWER(ODD)

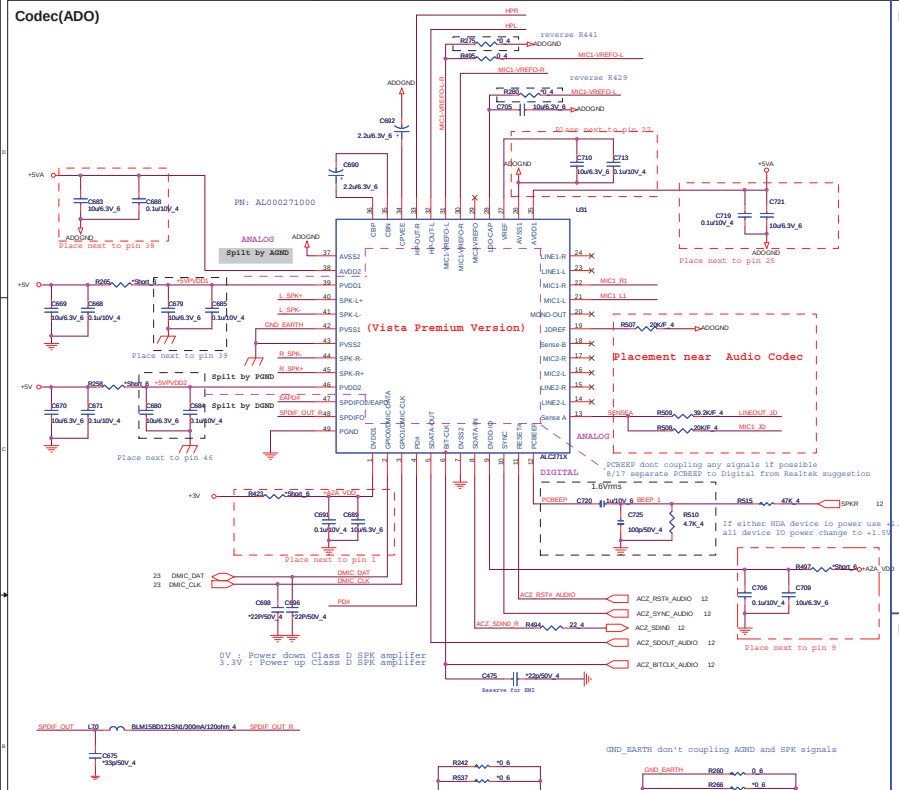


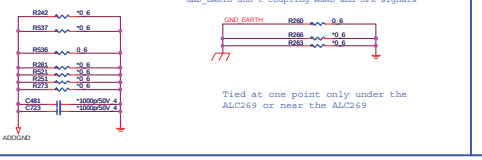
PROJECT : ZQ2

Quanta Computer Inc.

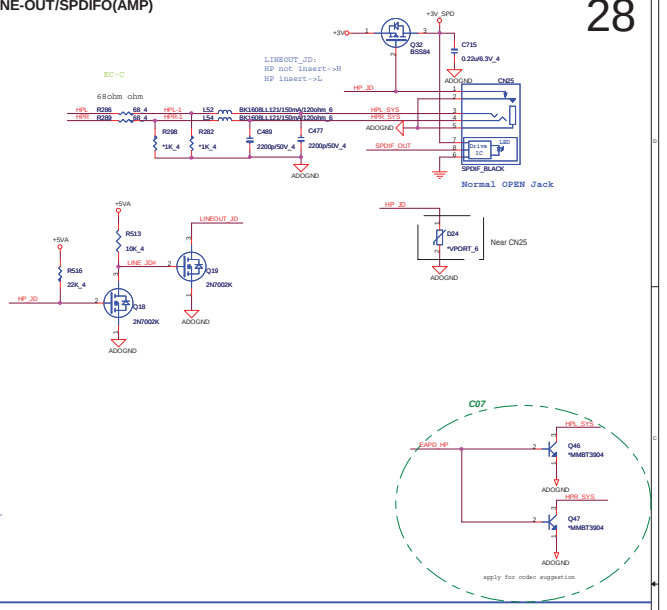
Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A
Date: Wednesday, May 27, 2009	Sheet 27 of 46	

Codec(ADO)

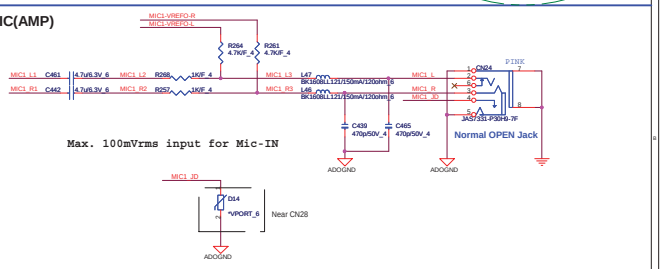




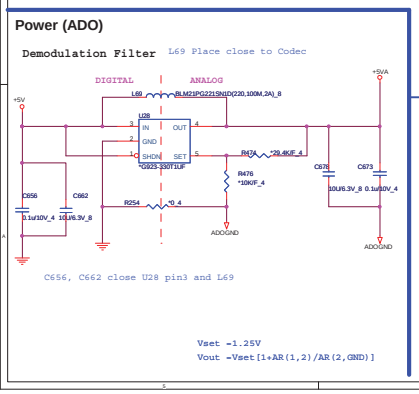
LINE-OUT/SPDIFO(AMP)



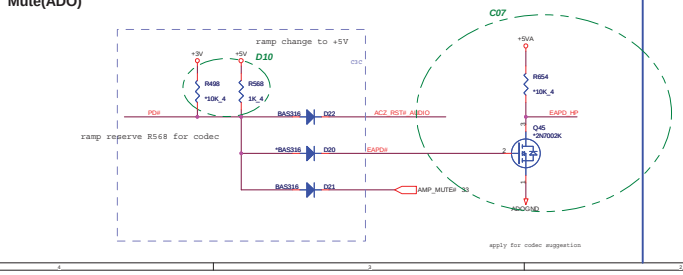
MIC(AMP)



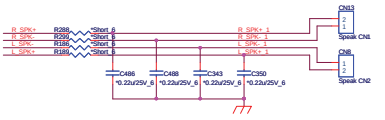
Power (ADO)



Mute(ADO)



Internal Speaker(AMP)



PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number: ALC271X / AMP / SPK	Rev: 1A
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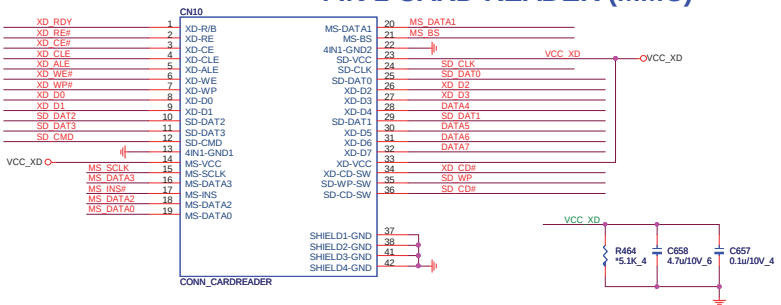
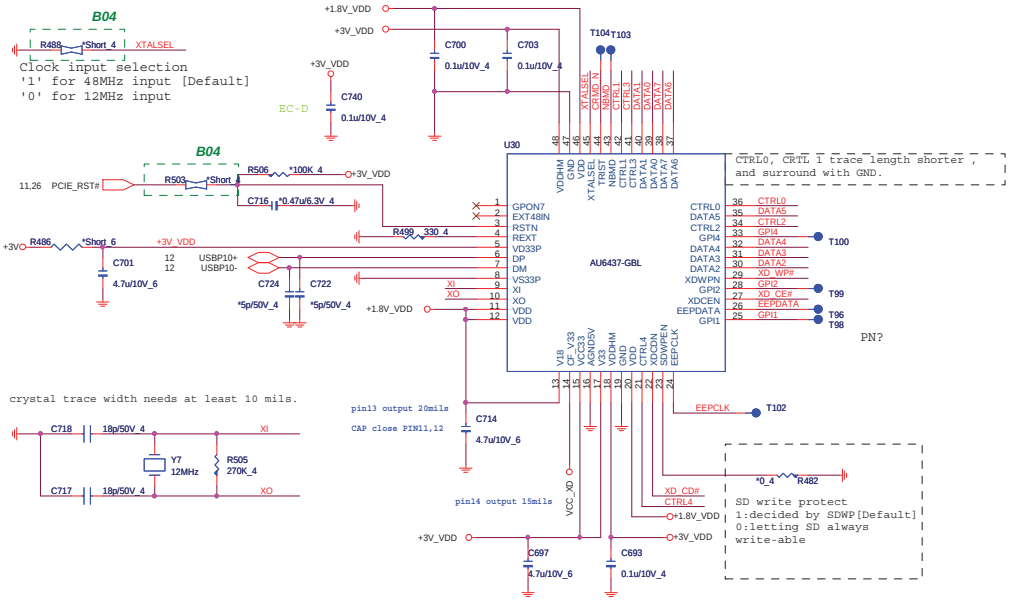
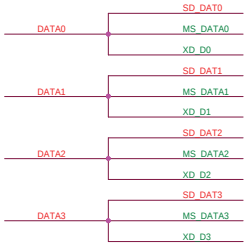
4 IN 1 CARD READER (MMC)

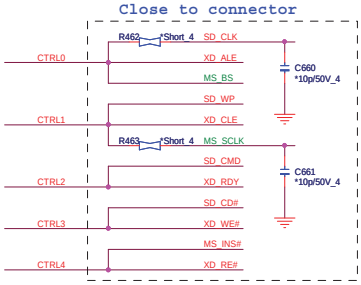
Main	??
Second	??



Close to CN10 pin 14 & pin23
4.7u CAP close to pin23







PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	AU6437 CardReader	1A
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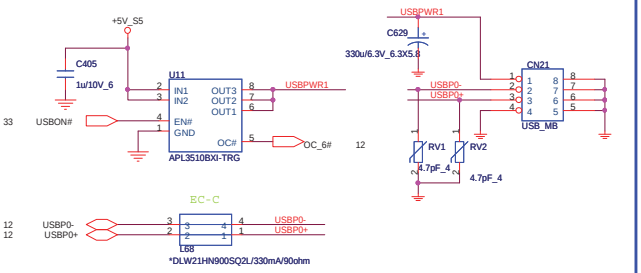
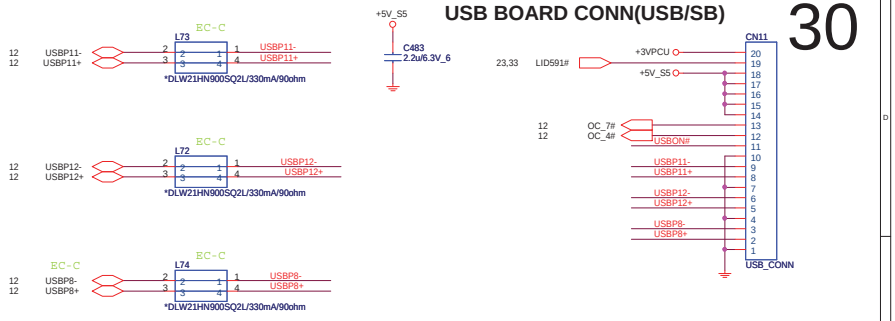
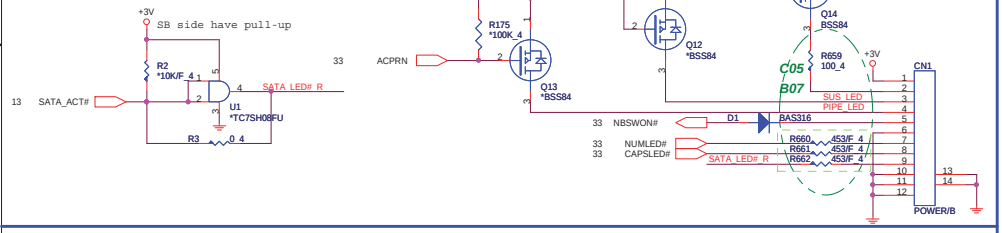
USB PORT(USB/MB)



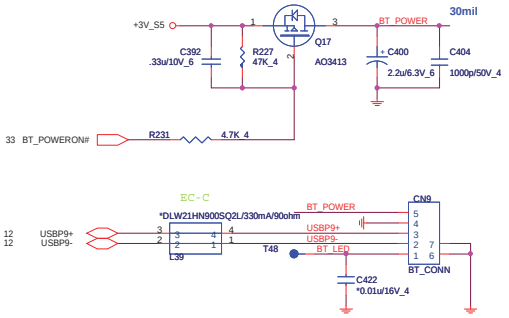
USB BOARD CONN(USB/SB)



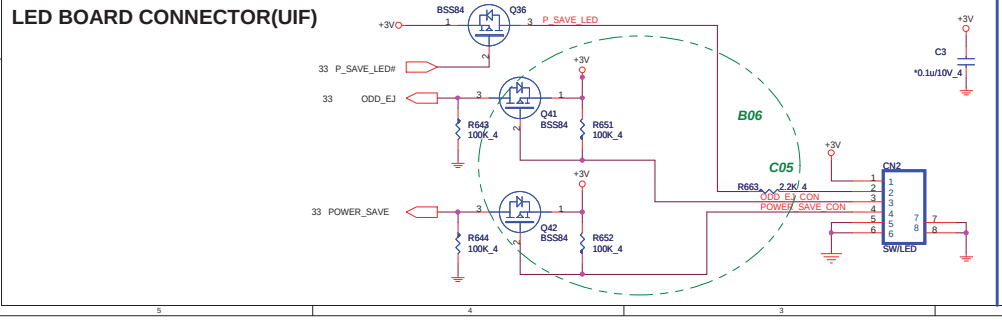
POWER BOARD CONN(UIF)



BLUETOOTH CONN(BTM)



LED BOARD CONNECTOR(UIF)



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	USB/BT/TP	1A
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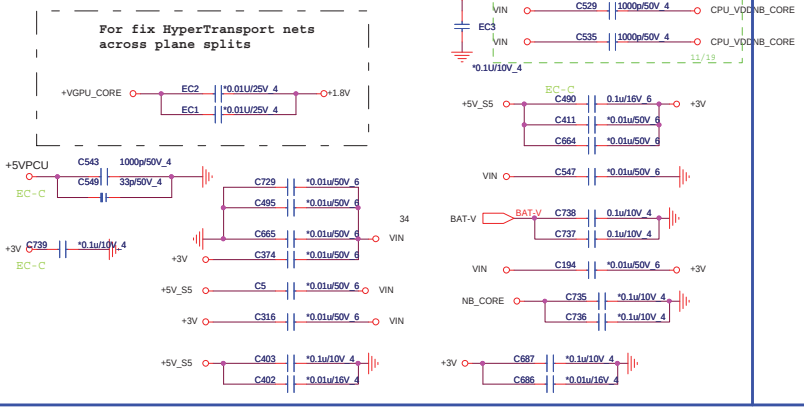
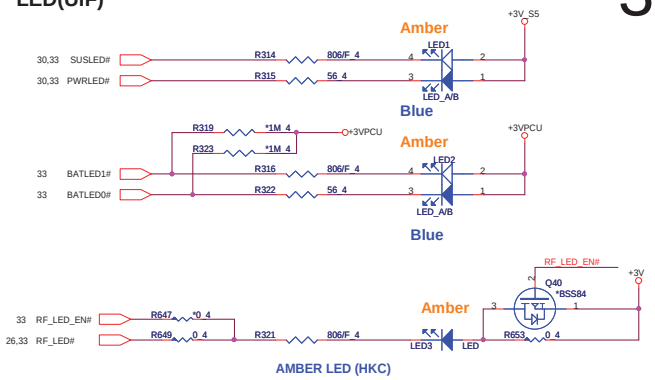
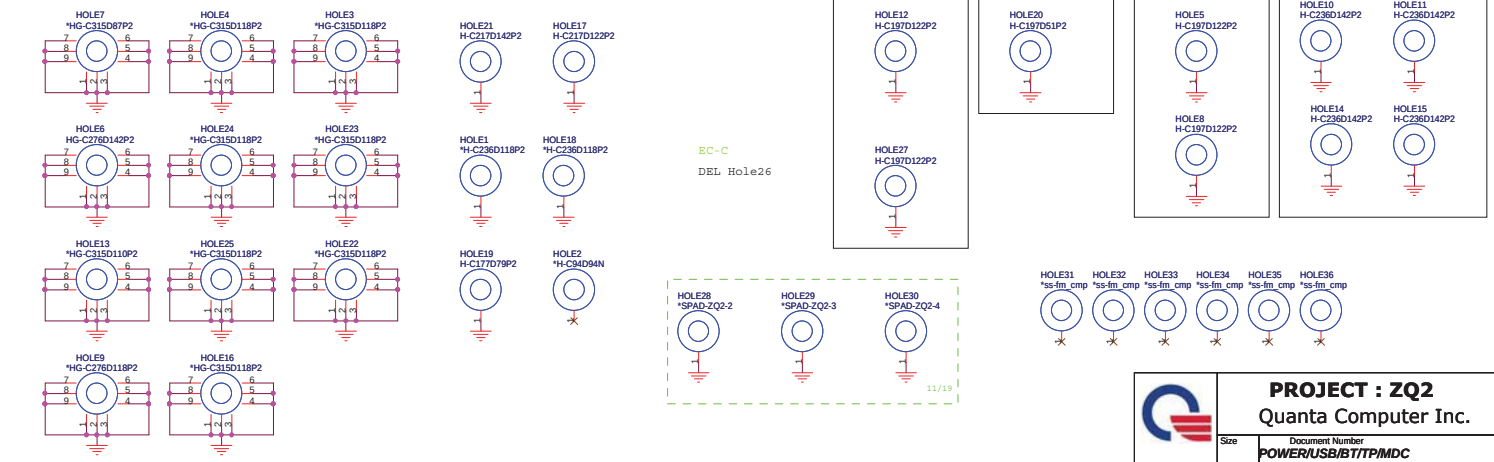
EE RETURN-PATH CAPACITORS(EMC)



LED(UIF)



HOLE(OTH)



PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	POWER/USB/BT/TP/MDC	1A
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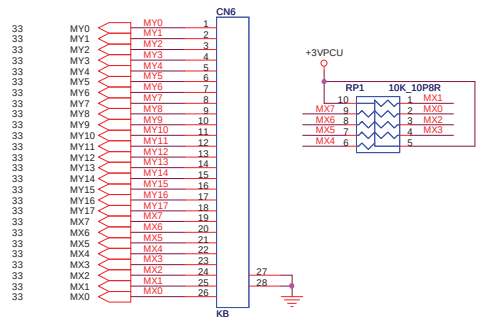
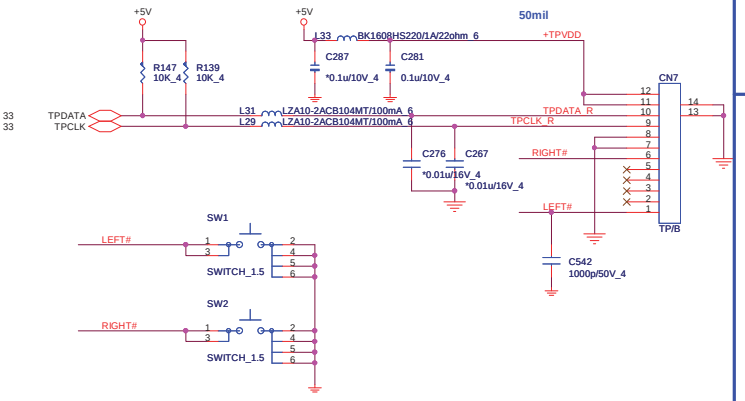
K/B(KBC)



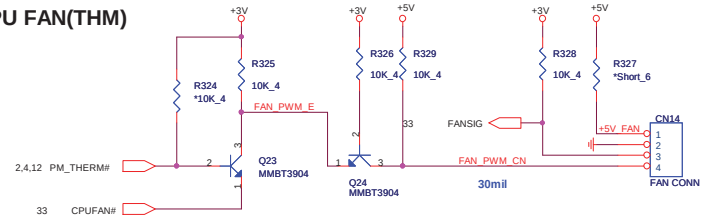
EC-C

Del CAP

TOUCHPAD BOARD CONN(TPD)



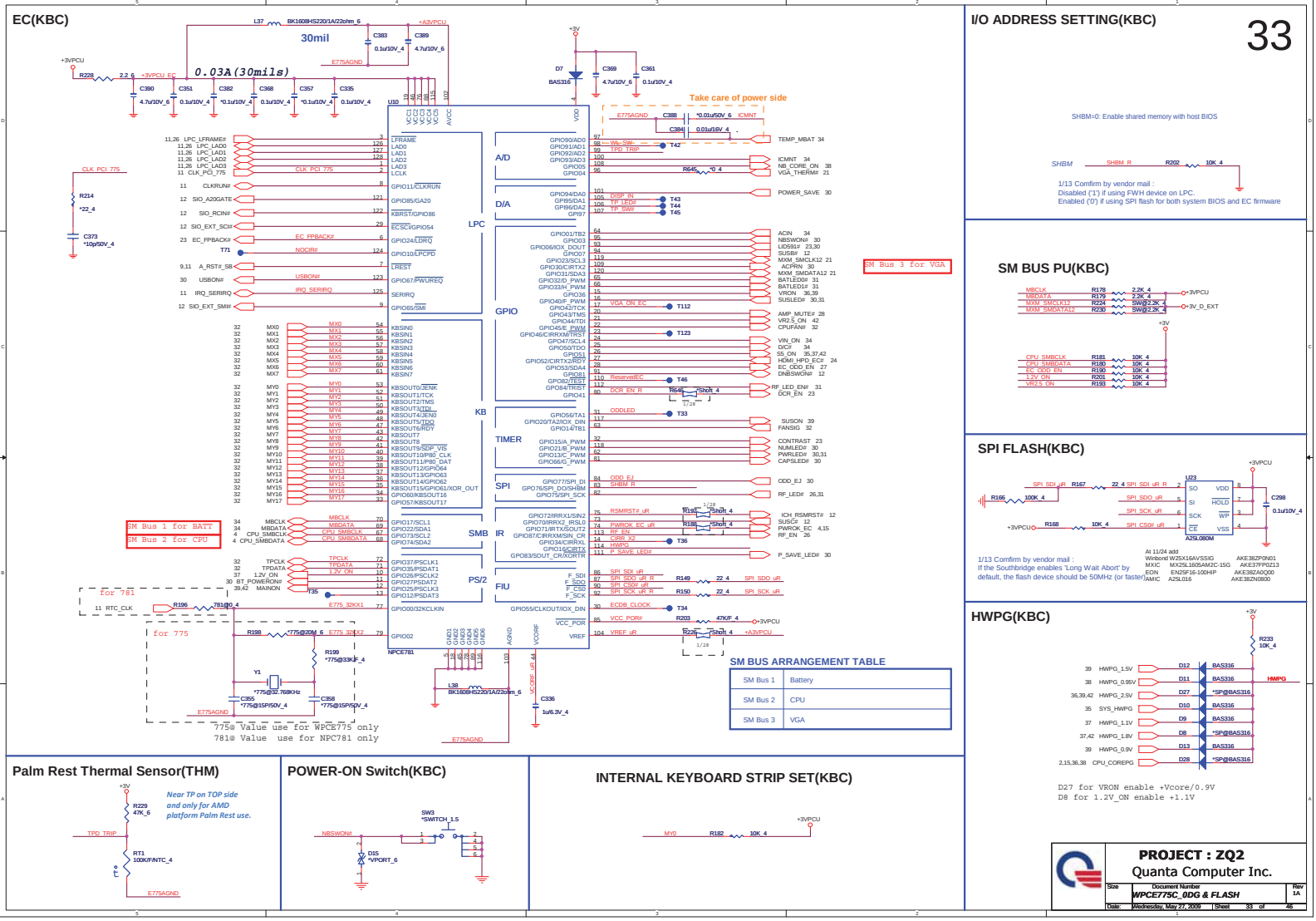
CPU FAN(THM)

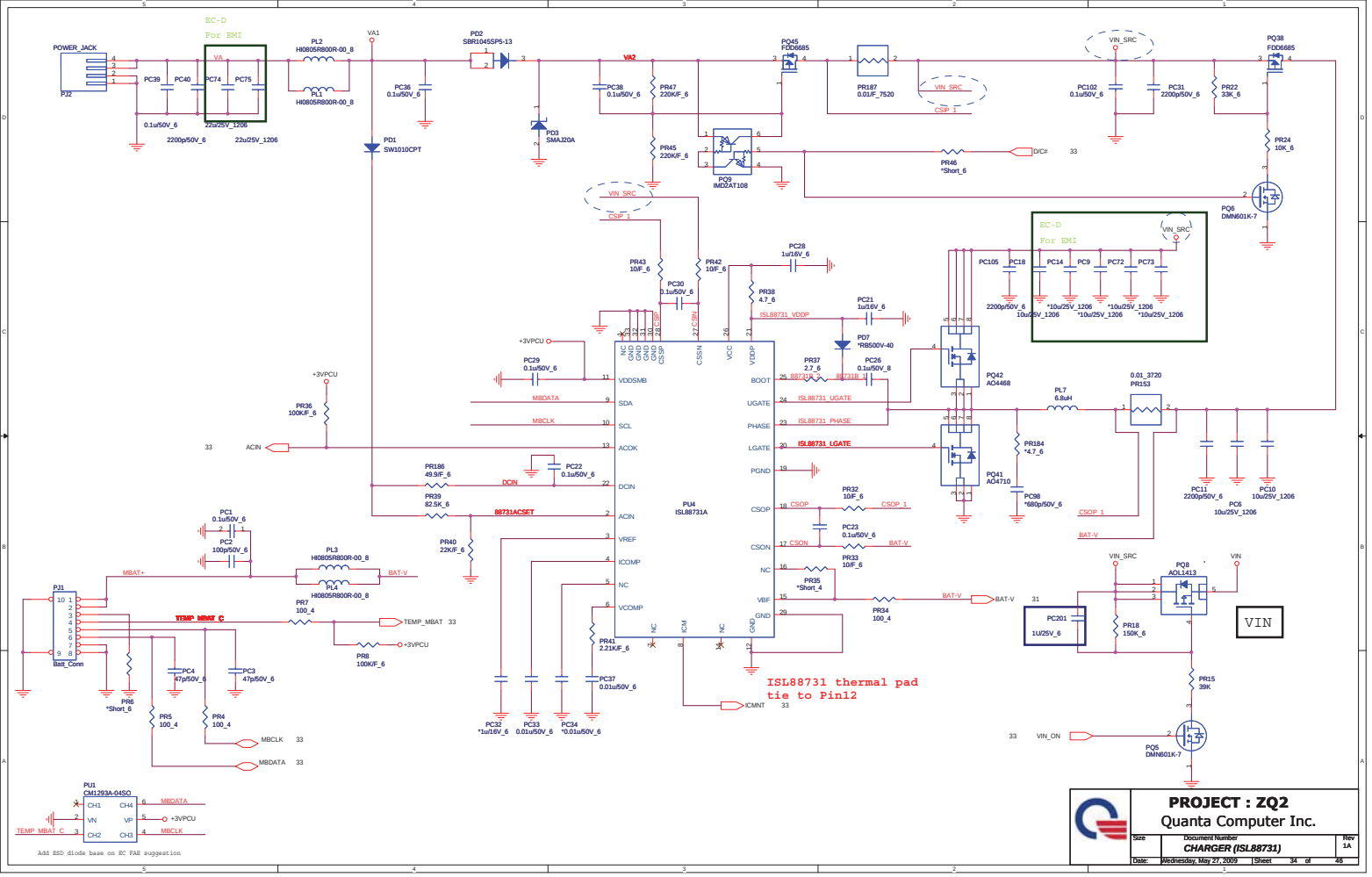


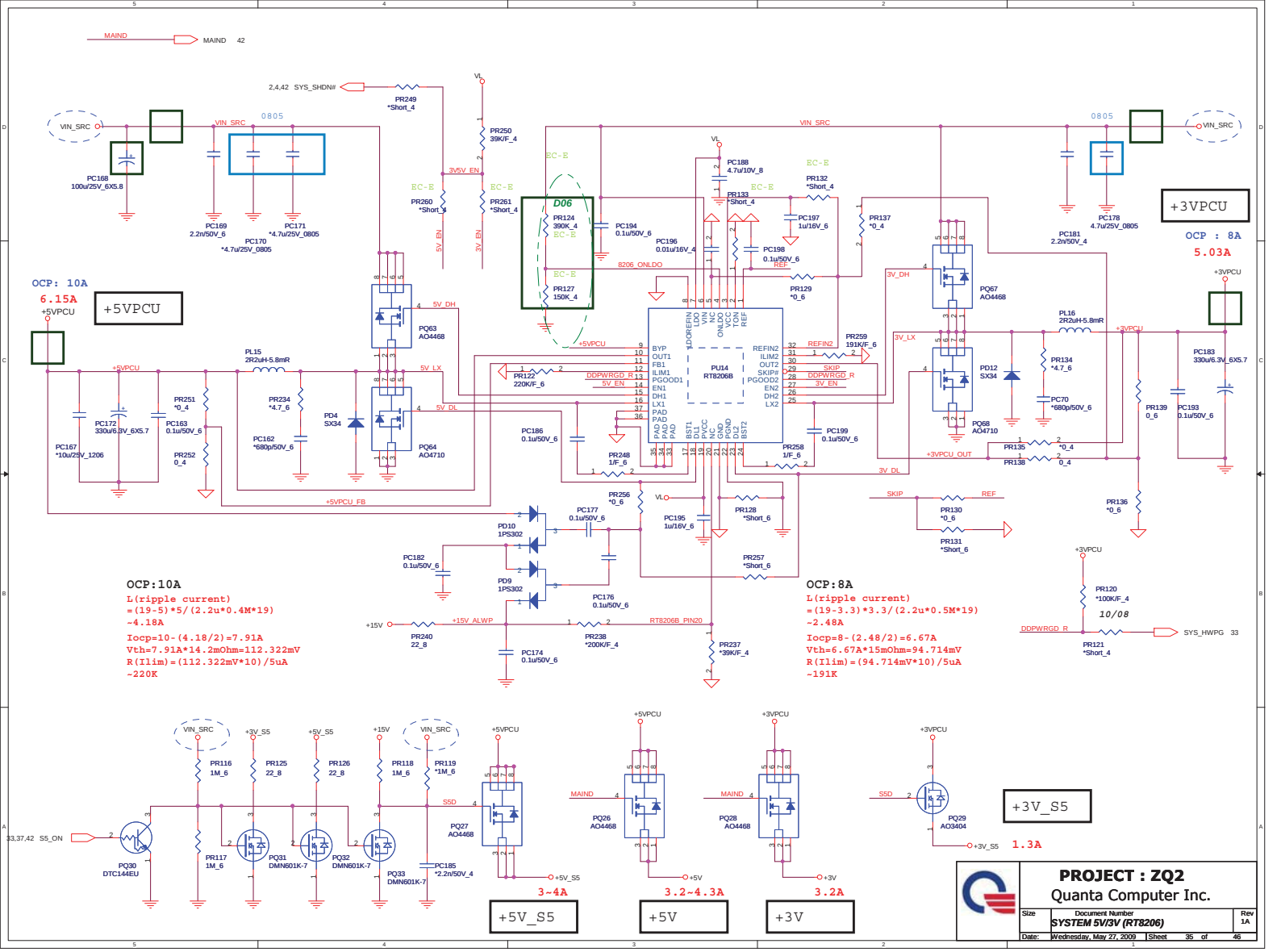
PROJECT : ZQ2

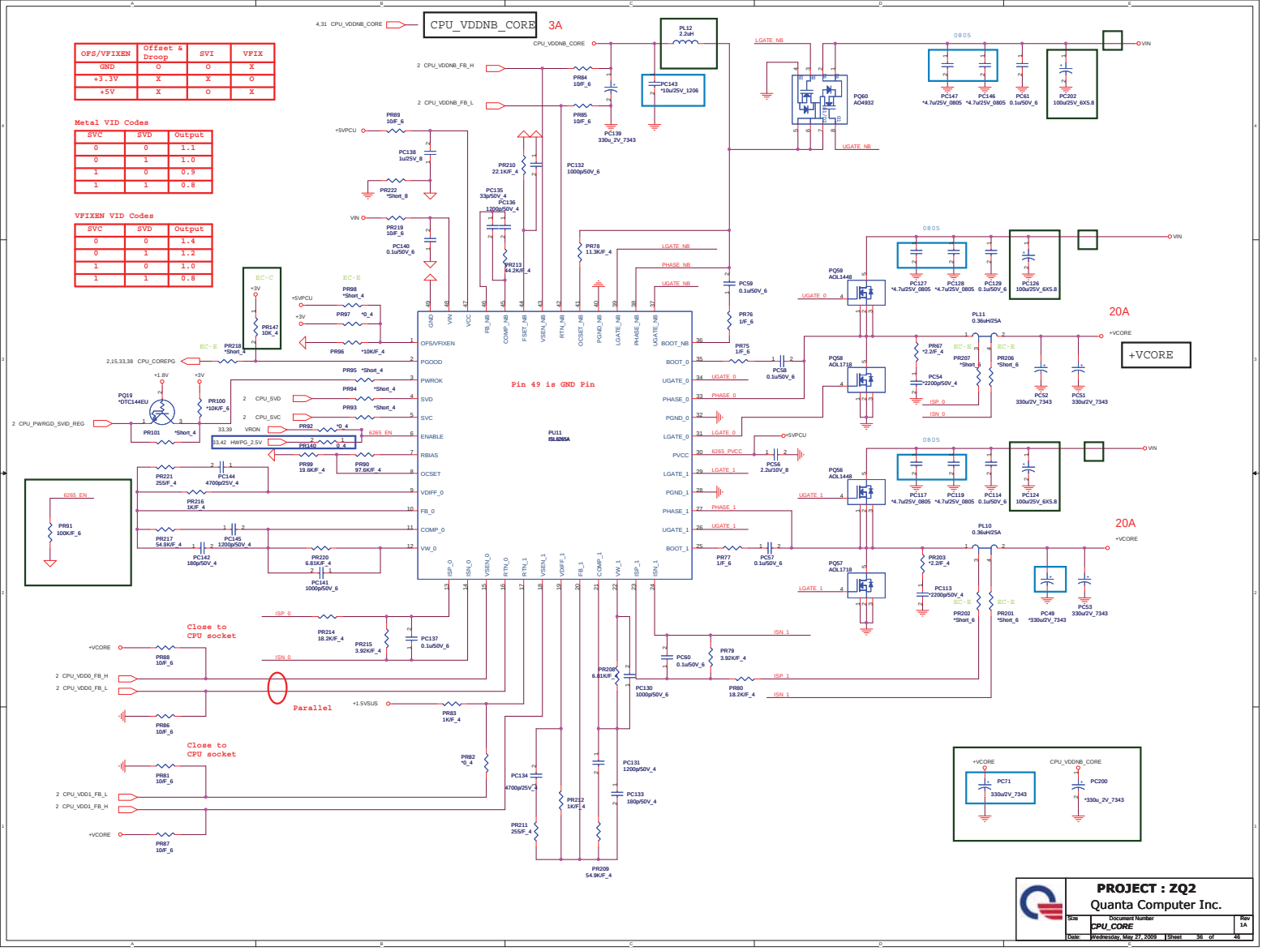
Quanta Computer Inc.

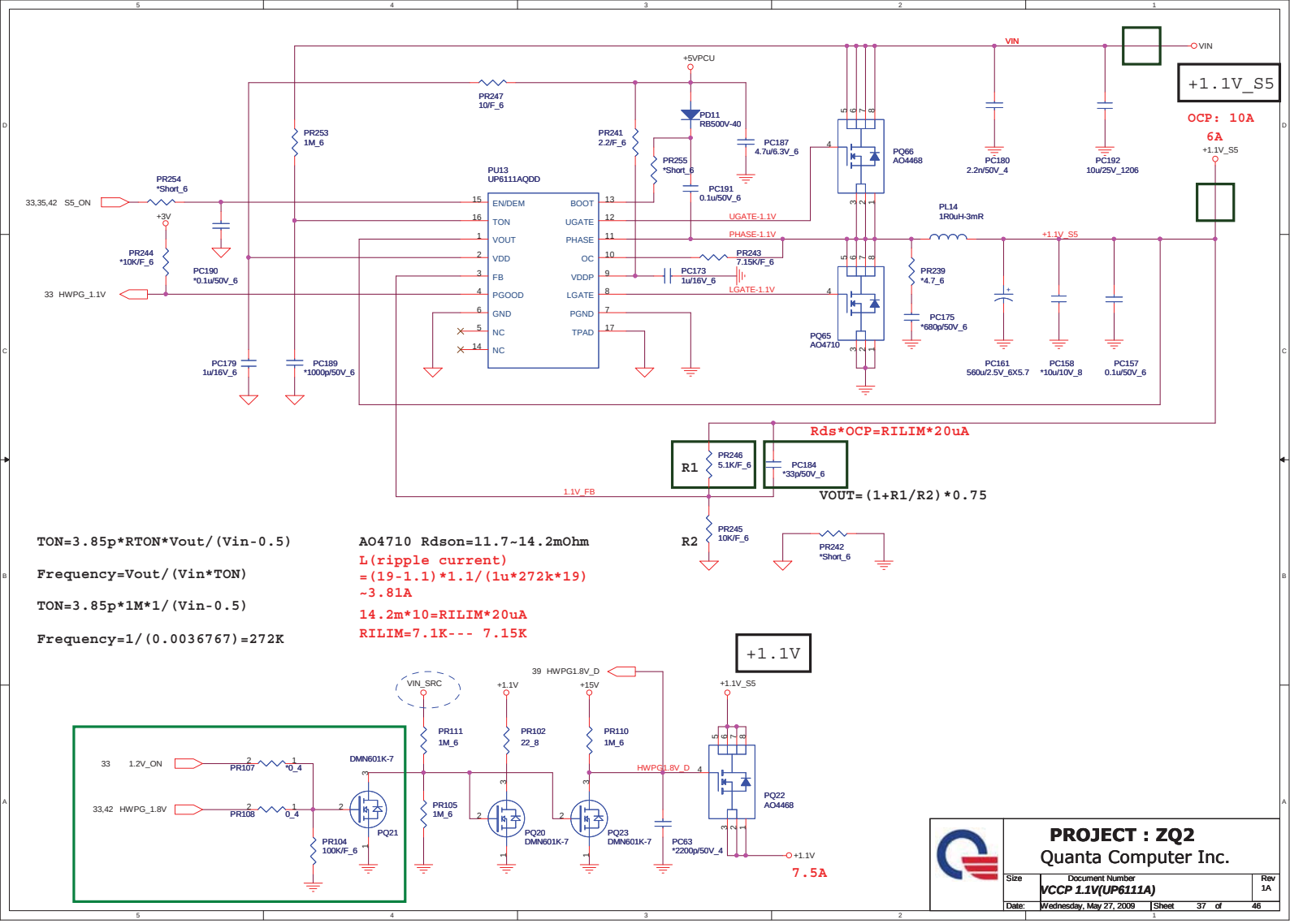
Size	Document Number	Rev
	KB/FAN/EE RETURN CAP	1A
Date: Wednesday, May 27, 2009	Sheet 32 of 46	











TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A

14.2m*10=RILIM*20uA

RILIM=7.1K--- 7.15K

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Quanta Computer Inc.

Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	1A
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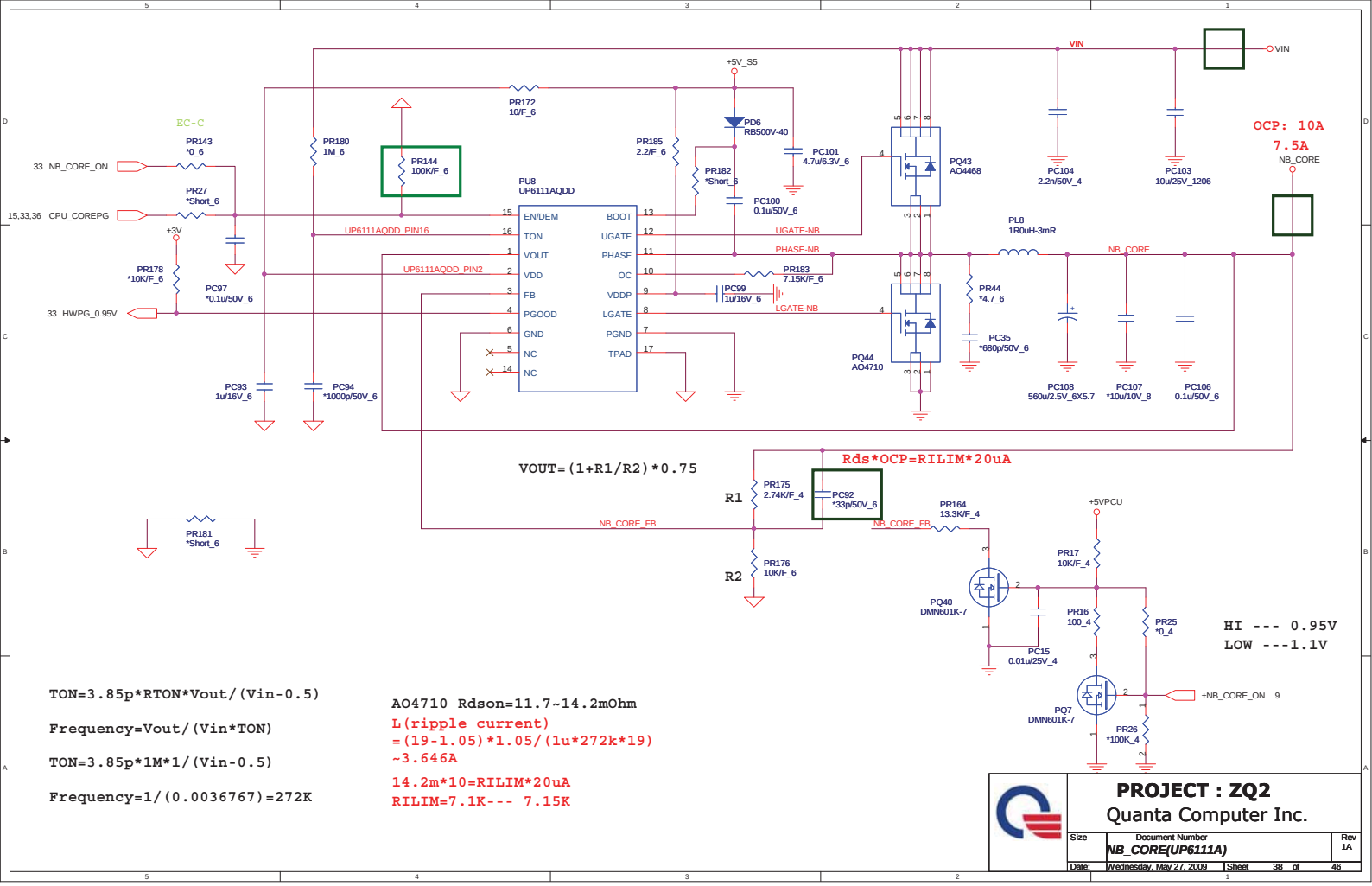

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA

RILIM=7.1K--- 7.15K

PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number: NB_CORE(UP6111A)	Rev 1A
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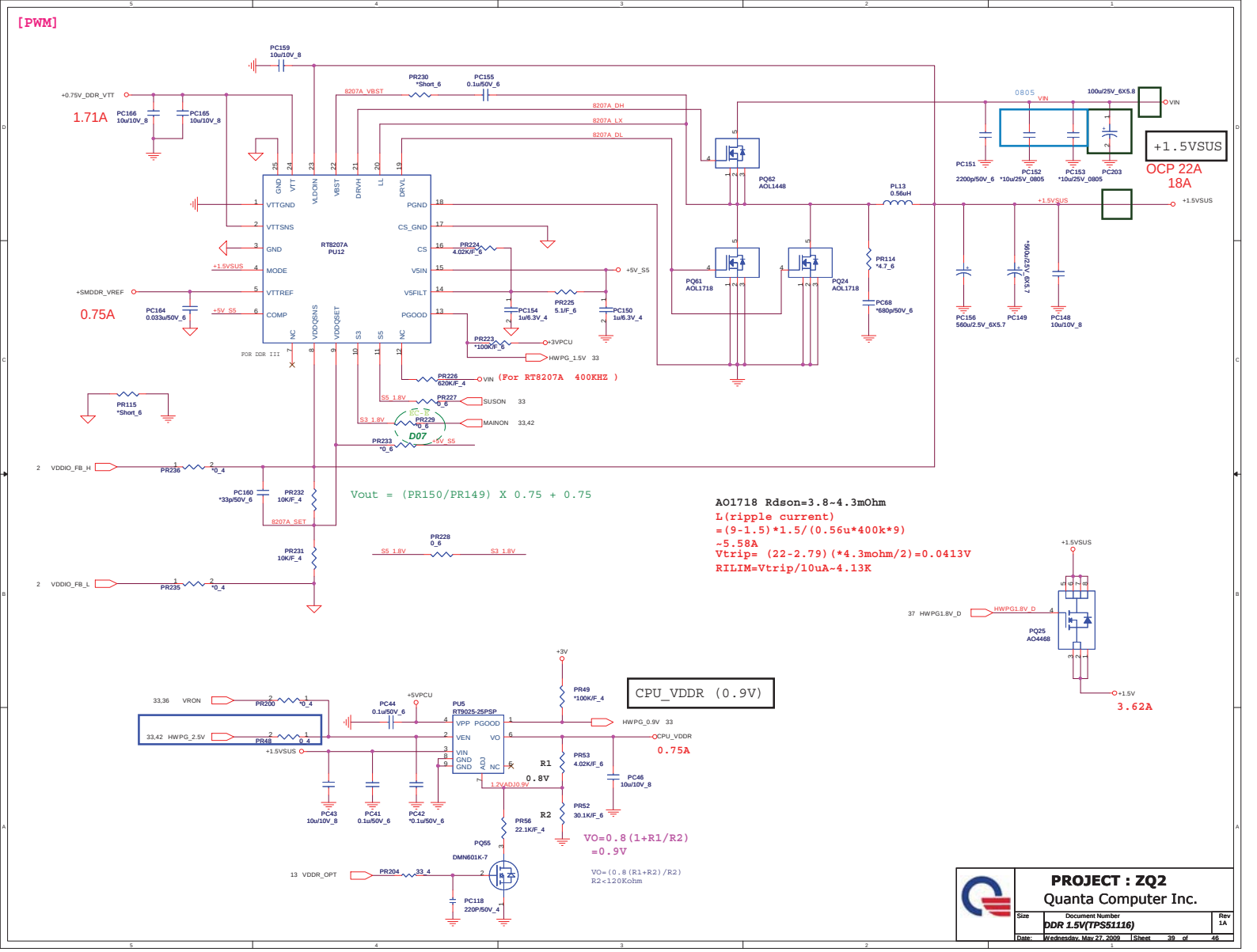
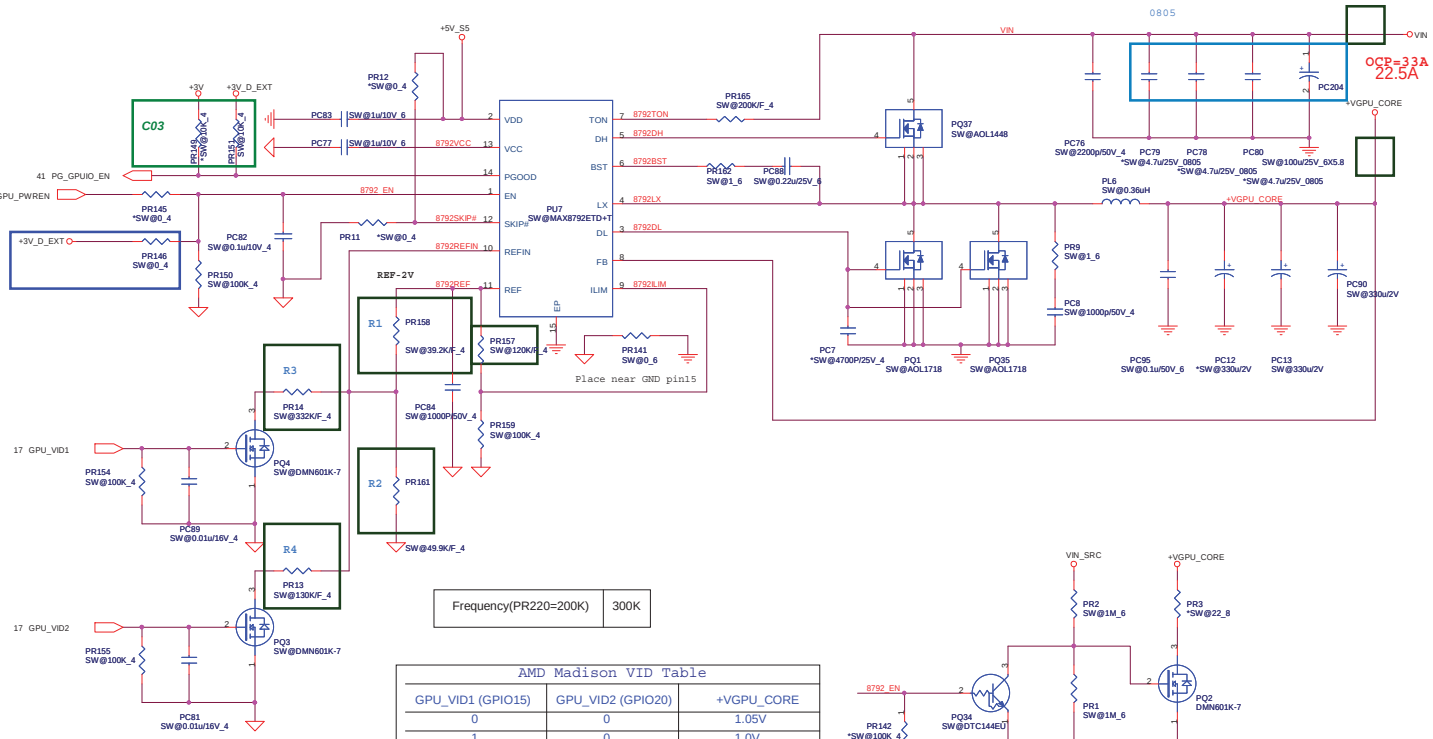


+VGPU_CORE



Frequency(PR220=200K)	300K

AMD Madison VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

Park -XT

GPU_VID1 (GPIO15)	*GPU_VID2 (GPIO20)*	*+VGPU_CORE*
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

R3	*R4*	*R1*	*R2*	*VREF*
332K	130K	39.2K	49.9K	2V

R1 change to 39.2K/F_4 (CS33922FB15)
R3 change to 332K/F_4 (CS43322FB15)
R4 change to 130K/F_4 (CS41302FB00)

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	GPU CORE(MAX8792)	1A

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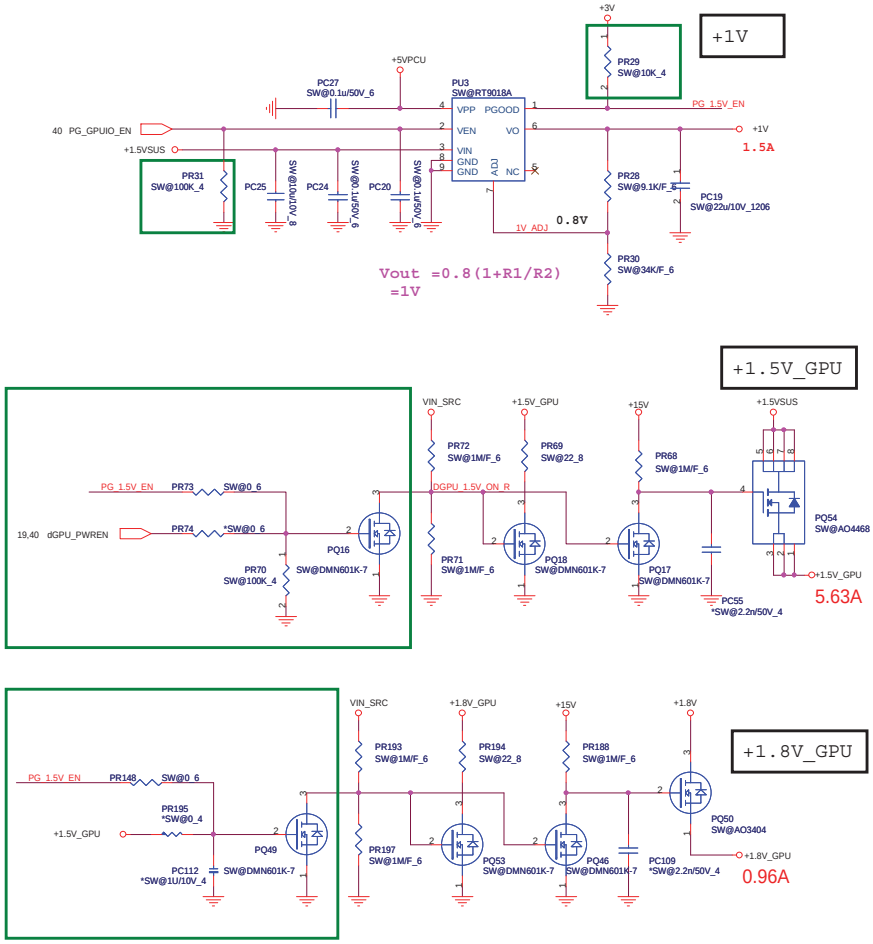

PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	+1V/+1.5_GPU/+1.8_GPU	1A
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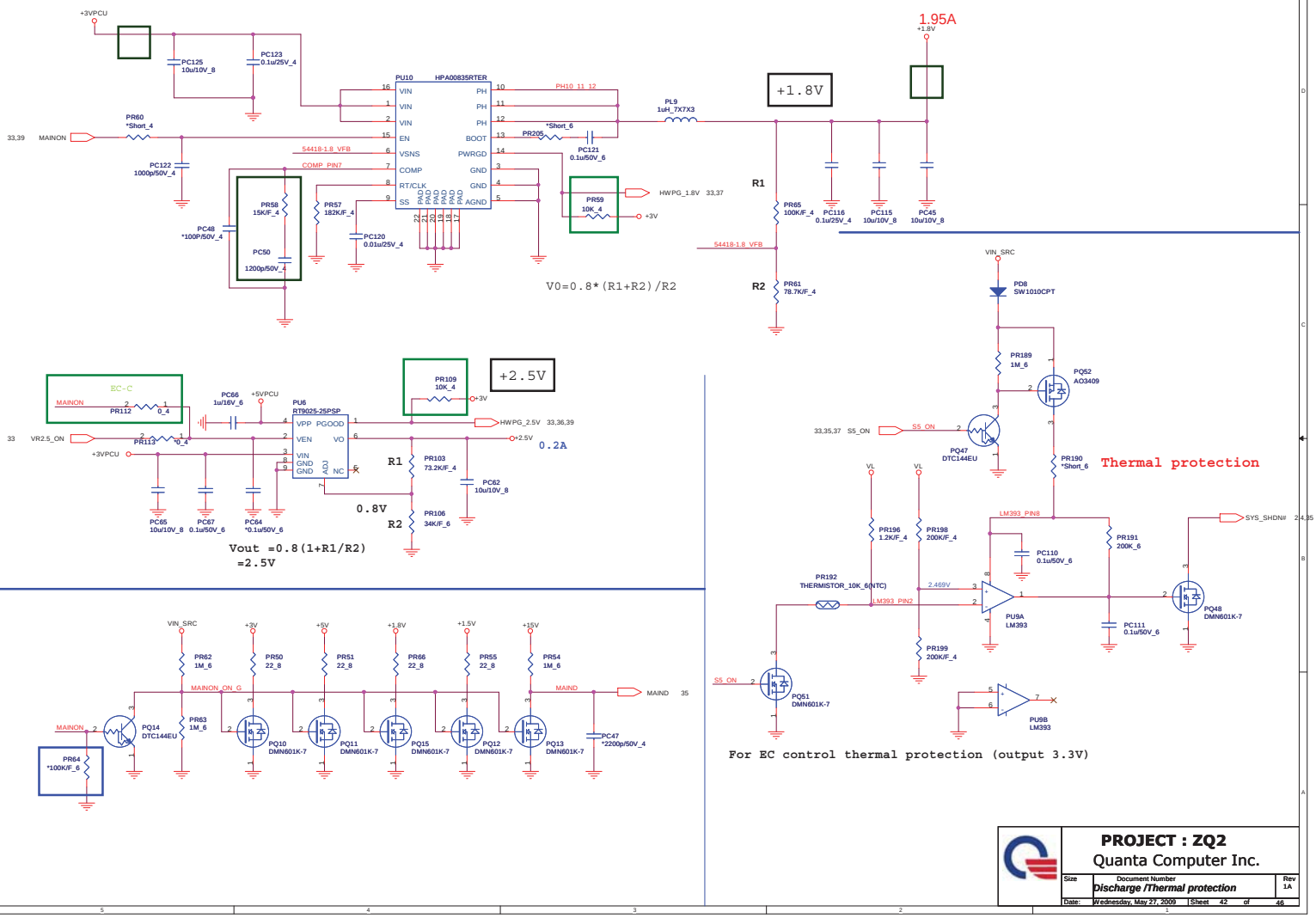

PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge /Thermal protection	1A
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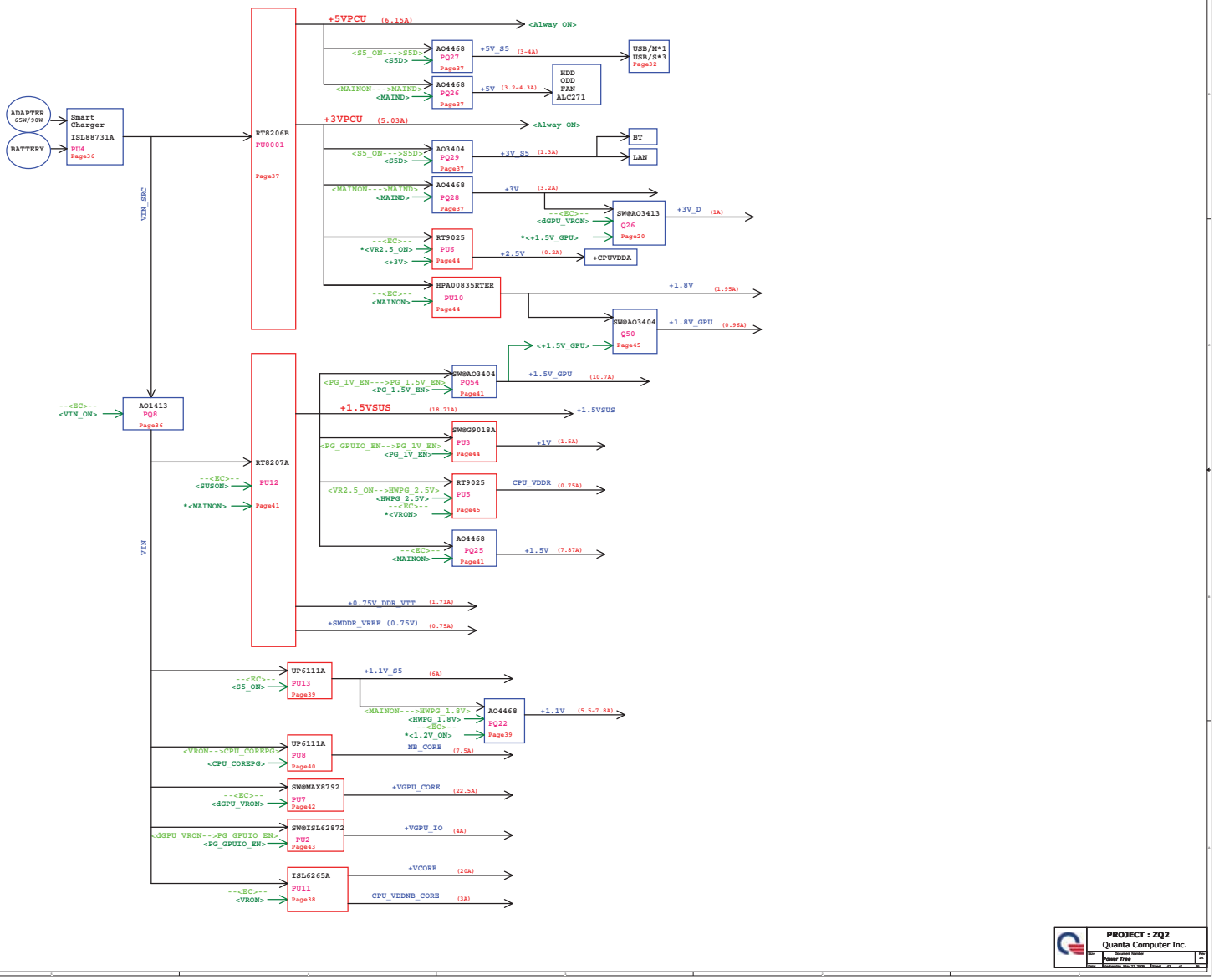
ZQ2 Power tree

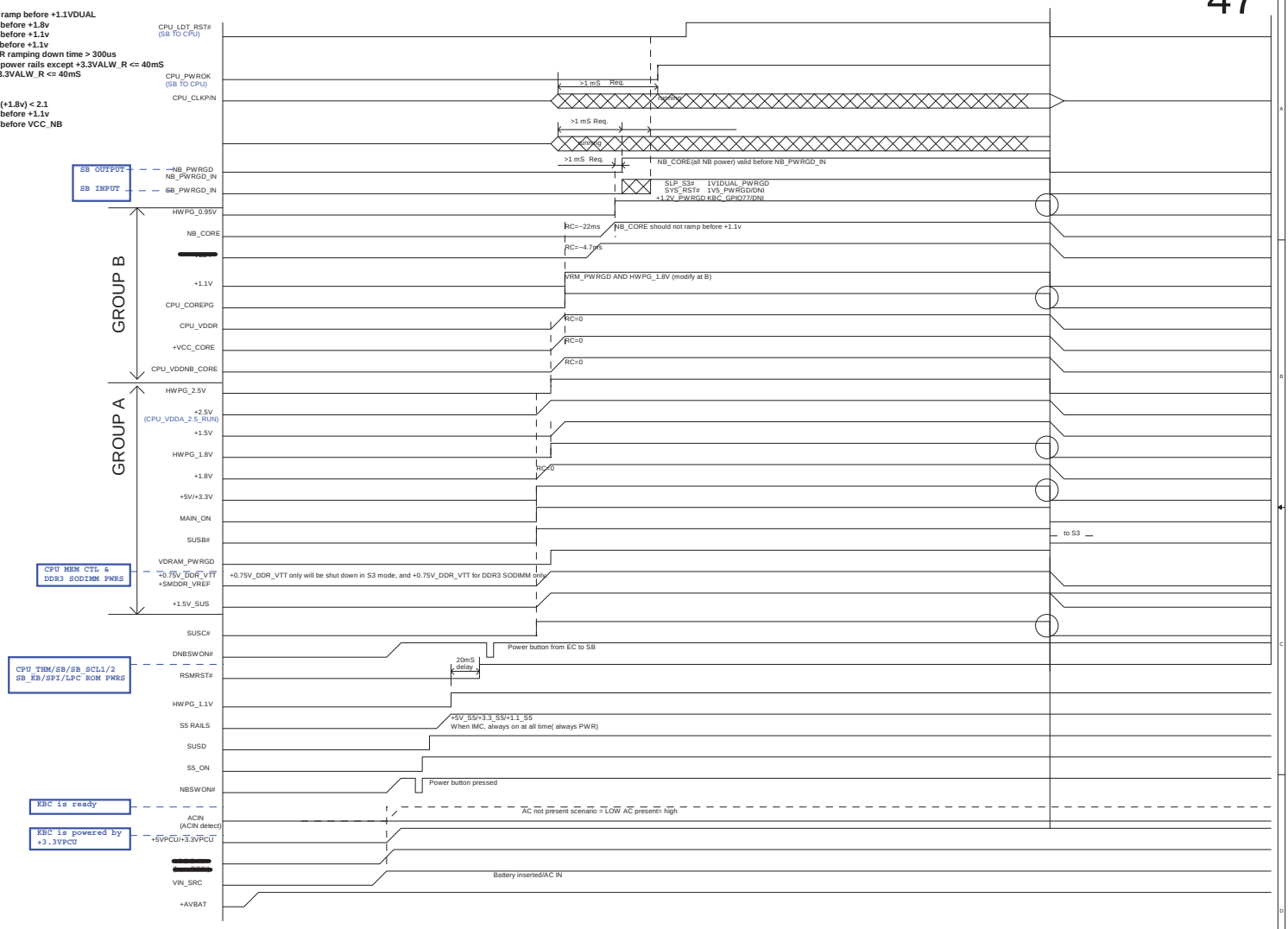


PROJECT : ZQ2
Quanta Computer Inc.
Power Tree

Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Power squence	1A
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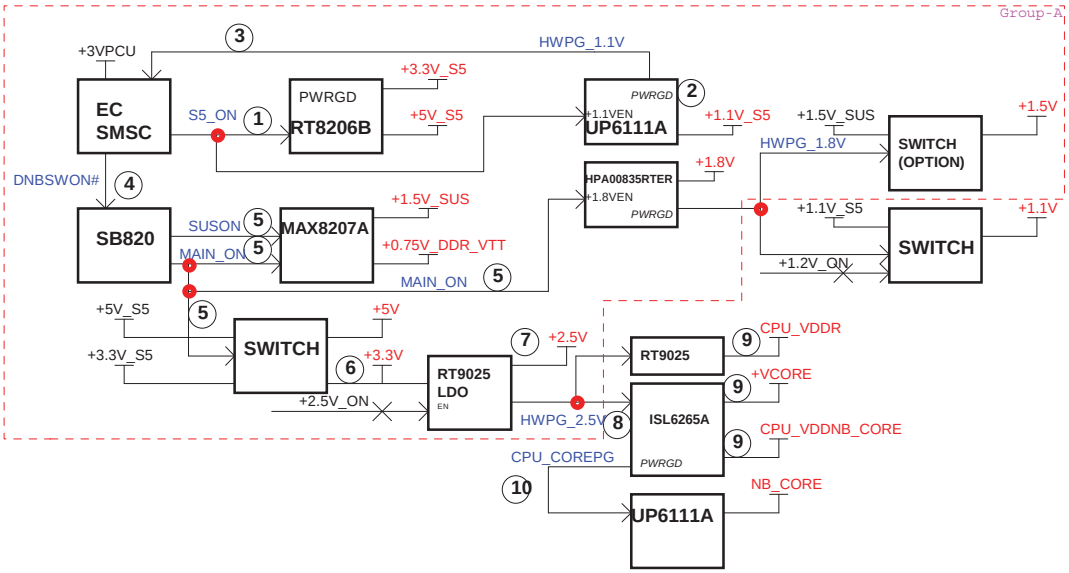

Power on Sequence required:

SB800:
1, +3.3V_S5 ramp before +1.1_S5
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

POWER RAILS Sequencing

1	S5_ON	13	+1.8V
2	+3.3V_S5	14	HWPG_1.8V
3	+5V_S5	15	+1.5V
4	+1.1V_S5	16	+2.5V
5	HWPG_1.1V	17	HWPG_2.5V
6	DNBSWON#	18	CPU_VDDNB_CORE
7	SUSON	19	+VCC_CORE
8	+1.5V_SUS	20	CPU_VDDR
9	+SMDDR_VTERM	21	CPU_COREPG
10	MAIN_ON	22	+1.1V
11	+5V	23	NB_CORE
12	+3.3V	24	

SB820 Sequencing

1	+3.3V_S5
2	ICH_RSMRST#
3	S0 POWER
4	PCIE_RCLKP/N
5	PCICLK[4:0]
6	SB_PWRGD_IN
7	NB_PWRGD_IN
8	LDT_PG
9	KBRST#
10	A_RST#
11	PCIRST#
12	LDT_RST#

RS880 Sequencing

1	+3.3V
2	NB POWER RAILS
3	ATX PS_PWRGD
4	NB INPUT CLOCKS
5	CPUCLK
6	NB_PWRGD
7	SB_PWRGD
8	LDT_PG/CPU_PWRGD
9	PCIRST#,NB_RST#
10	LDT_RST#
11	
12	

EC Sequencing

1	3VPCU
2	NBSWON#
3	VIN_ON
4	S5_ON
5	ICH_RSMRST#
6	-DNBSWON#
7	SUSB#/SUSC#
8	SUSON/USB_ON#
9	MAIN_ON/HWPG
10	VRON
11	PWROK
12	

PROJECT : ZQ2
Quanta Computer Inc.
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Model	REV	CHANGE LIST
ZQ2 MB	1A	1.A01 del Ext-CLK Gen component 2.A02 del Power VGPU-IO 3.A03 page 7,9,10 add side-port 4.A04 page9 R123 no stuff ,R129 stuff for A-test boot issue 5.A05 page9 U22.D8 change to A_RST#_SB 6.A06 page11 move dGPU_PWROK from U29.AA4 to U29.AJ6 7.A07 page11 move BOARD_ID[0:5] to U29.AC3 8.A08 page12,17 add VGA_REQ# for VGA_CLK request 9.A09 page13 move MEM_1V5 to U29.A7 10.A10 page13 update Board_ID table 11.A11 page13 add sideport table 12.A12 page 15 del R471 for just only use int-clkgen 13.A13 page 11,16 add CLK_14M_VGA for Park boot 14.A14 page 17 modify GPU_VID gpio relation 15.A15 page18 modify R86 from 680 to 51 16.A16 page19 add +3V_D_EXT for leakage issue 17.A17 page20 del don't use port for cost down
	2A	B01 Page10 modify L77 footprint B02 Page23 modify R54 stuff for Discrete,R50 for UMA B03 Page27 modify ODD power connection B04 Page change 0-ohm R185,R89,R93,R136,R142,R485,R487,R488,R489,R490,R493,R503 to short pad B05 Page12 add CLK request pull up R501,R551 B06 Page30 add Q41,Q42,R651,R652,R633 from LED board B07 Page add R659,R660,R661,R662 from power board B08 Page modify R314,R315,R316,R322 follow ZQ1 B09 Page add Q40,and RF_LED_EN# with RF_LED# to EC B10 Page change U26,CN10,U12 footprint B11 Page C534 C537 C154 C147 C144 C129 C14 C20 C18 C17 C15 C32 C39 C50 C62 C72 C88 C87 C103 C102 C29 from CC0402-C to CC0402. L8 R48 R41 R30 L1 L14 from RC0402-C to RC0402. B12 Page R377 stuff ,R247 no stuff follow AMD sch. B13 Page change D2,D3,D23,D25,D26,D29 to BAS316 B14 Page reserve R152,R423,L4 (USBP2)option for CCD issue B15 Page change U26,CN10,U12 footprint B16 Page13 Change board ID power rail from +3V_S5 to +3V. B17 Page10 W/O Sideport ,R146 no-stuff, C831 connect to GND B18 Page9 no-stuff R108,R105 B19 Page28 del D20,D21,D22 &R498 from 10K->1K & add Q43,Q44,Q45 B01
	3A	C01 Page02 Add H/W shutdown function and add CPU_COREPG shutdown design(add Q43,R152) C02 Page23 Option brightness switch control just only by NB R50 C03 Page40 Change PG_GPUIO_EN pull high power rail from +3V to +3V_D_EXT. For Park GPU SG mode hang up issue. C04 Page42 Change PR60 from 10k to 0ohm. C05 Page30 chang LED R R660,R661,R662,R663,R314,R316,R321 C06 PageX change R 0ohm to short pad C07 PageX audio for codec suggestion C08 PageX X. C09 PageX X C10 PageX X. C11 PageX X. C12 PageX X.
	4A	D01 Page03 Change CPU VDDR_SENSE pull high power rail to CPU_VDDR and remove trace connect to controller IC. D02 Page15 Modify text note. D03 Page12 Change "GBE_COL" ,"GBE_CRS" ,"GBE_RXERR" to GND follow SCL V1.04 version. D04 Page14 Change USB PLL power rail source to separate VDDPL_33_USB_S follow SCL V1.04 version. D05 Page04 R409 no stuff, R413 stuff D06 Page09 del PD5, PR124-390k for panasonic battery low power protect issue. D07 Page36 PR229 no stuff D08 Page23 C212,C213,C214,C220,C221,C222 from 33p to 10p D09 Page21 modify DDR3 Memory table D10 Page28 R568 stuff and R498 no stuff for Audio issue D11 Page2/4 Q3 pin 3 change to PM_THERM#,Q3 pin 8 add PM_THERM# D12 Page23 reserve C541 for monitor test issue
	3C	

MODEL	ZQ2	
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