SP9 BLOCK DIAGRAM

01

PCB STACK UP

Discrete 8L

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SVCC
LAYER 6 : IN3(High)
LAYER 7 : SGND2
LAYER 8 : Bottom

BATTERY SELECTOR PAGE 46
SYSTEM CHARGER(BQ24704) PAGE 46
SYSTEM POWER RT8206B PAGE 39
DDR III SMDDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 44
VCCP +1.5V AND GMCH 1.05V(ISL62872) PAGE 40
VDDCI RT8209A PAGE 42
VGACORE ISL6264 PAGE 43
CPU CORE NCP6131S52MNR2G
CPU CORE NCP5911 PAGE 47\48

DDR III
SO-DIMM 0
SO-DIMM 1
P12, 13

Dual Channel
1066/1333 MHz

DDR SYSTEM MEMORY

intel
Intel Sandy
4 Core
rPGA 988
(37.5mm X 37.5mm)
CPU 45Watt
35Watt
PCI-E X16
FDI
DMI
P3~P6

10.8GT/s
Embedded DisplayPort
P26

VRAM GDDR5*8
32*32\64*16\128*16
P20~P23

X'TAL 27.0MHz

PCIE
5GT/s
ATI GPU
Granville-LP
(16 x 64Mb\128Mb x 8pcs)
P14~P19

EXT_CRT
INT_CRT
CRT Switchable P24
CRT P27

EXT_LVDS
INT_LVDS
LVDS Switchable P24
LVDS P24

EXT_DisplayPort
INT_DisplayPort
DP\eDP Switch PS8321 P26
DP\eDP Port P26

EXT_HDMI
INT_HDMI
HDMI Switch PI3HDMI201 P28
HDMI P28

FDI interface
2.7GT/s
X4 DMI interface
5GT/s

HDD (SATA) P33
HDD (SATA) P33
ODD (SATA) P33
eSATA/USB Port x 1 P33

SATA0
SATA1
SATA4
USB1/ SATA5

intel
<PCH>
Platform Controller Hub
mBGA 989
(25mm X 25mm)
FDI
DMI
SATA Gen3
SATA Gen2
SATA Gen2
USB
HDA
SPI
LPC
RTC
P9
iGFX Interfaces
PCI-E

INT_CRT
INT_LVDS
INT_DisplayPort
INT_HDMI

X'TAL 32.768KHz

USB 2.0
Azalia

PCI-Express Gen2
5GT/s

PCIE3
NEC USB3.0 DB P38
USB2/3 Combo X1

PCIE2
PCIE1

USB Port*2 USB8&9 P34
Bluetooth USB13 P34
Webcam w/ Mic USB4 P34
CardReader RTS5159 USB12 P34

Audio Codec IDT92HD80 P29

Realtek Giga-LAN RTL8111E P32
X'TAL 25MHz

Mini-card (Wireless LAN Shirley Peak 802.11a/b/g/n) P37

Amplifier TPA6130A2 P29
Amplifier TPA3111D1 P30

Dual SPI ROM
4MB x1 (Basic ME+Braidwood)
P7

EC KB3926 D2 P36
X'TAL 32.768KHz

Combo Jack (Headphone/MIC) P30
Line out (Headphone) P30
Int Speaker P27
Sub-Woofer P29

SPI ROM P36
Touch Pad P34
Keyboard P35
SYSTEM/GPU FAN P37
Accelerometer LIS3LV02DL P30

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

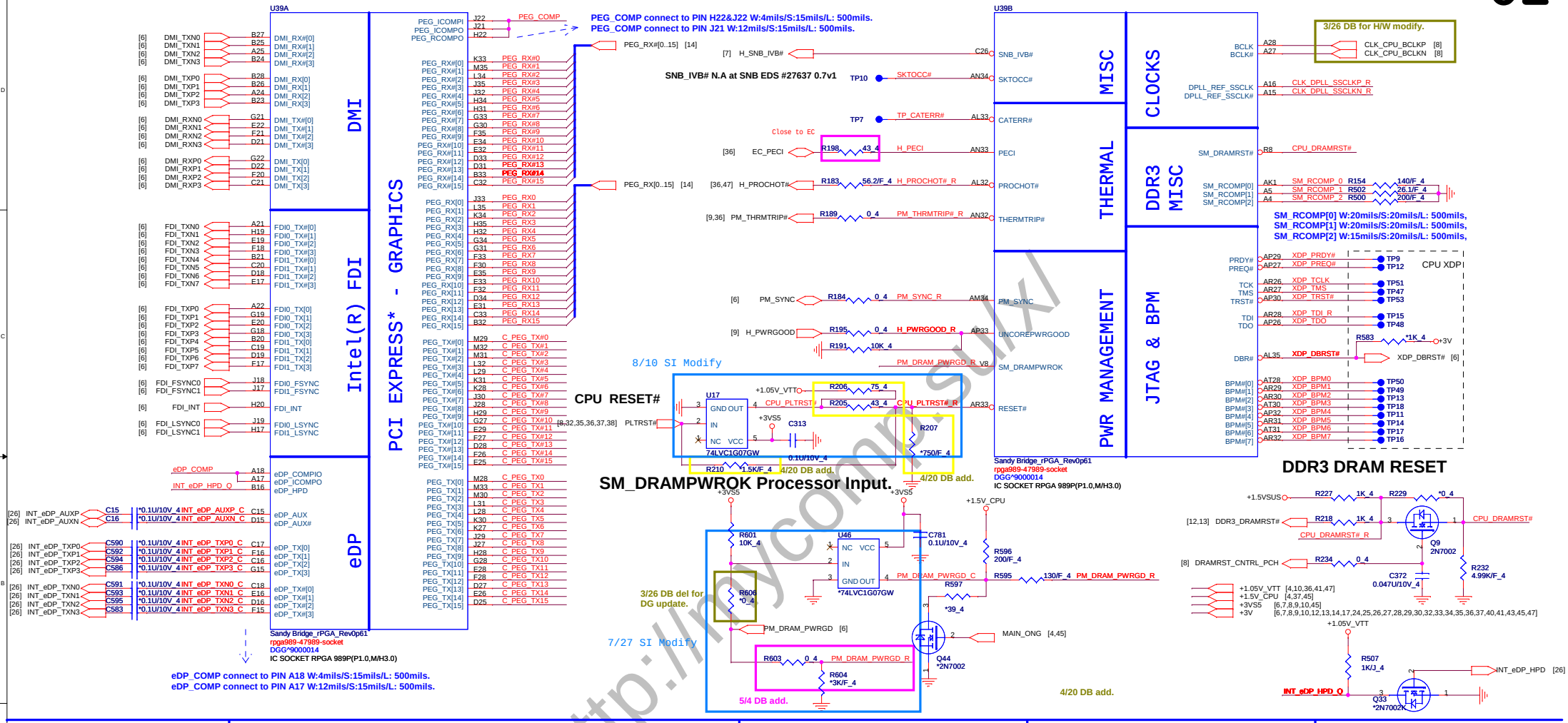
N85/RD2

Date: Tuesday, August 10, 2010 Sheet 1 of 49

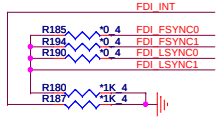
Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

02

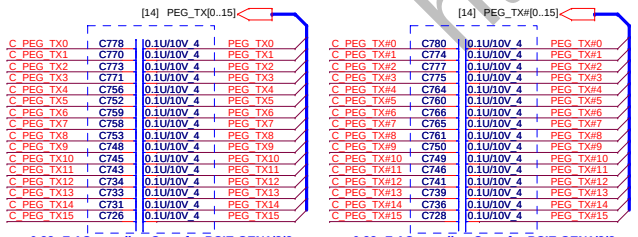


FDI disable (DIS only stuff)

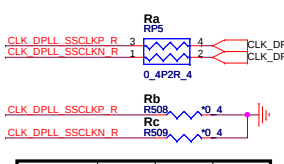


FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

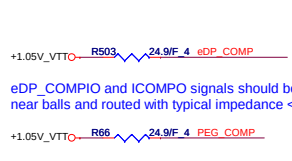


Embedded Display PLL Clock



	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

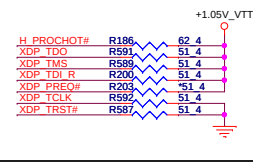
DP & PEG Compensation\ Hot-plug



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

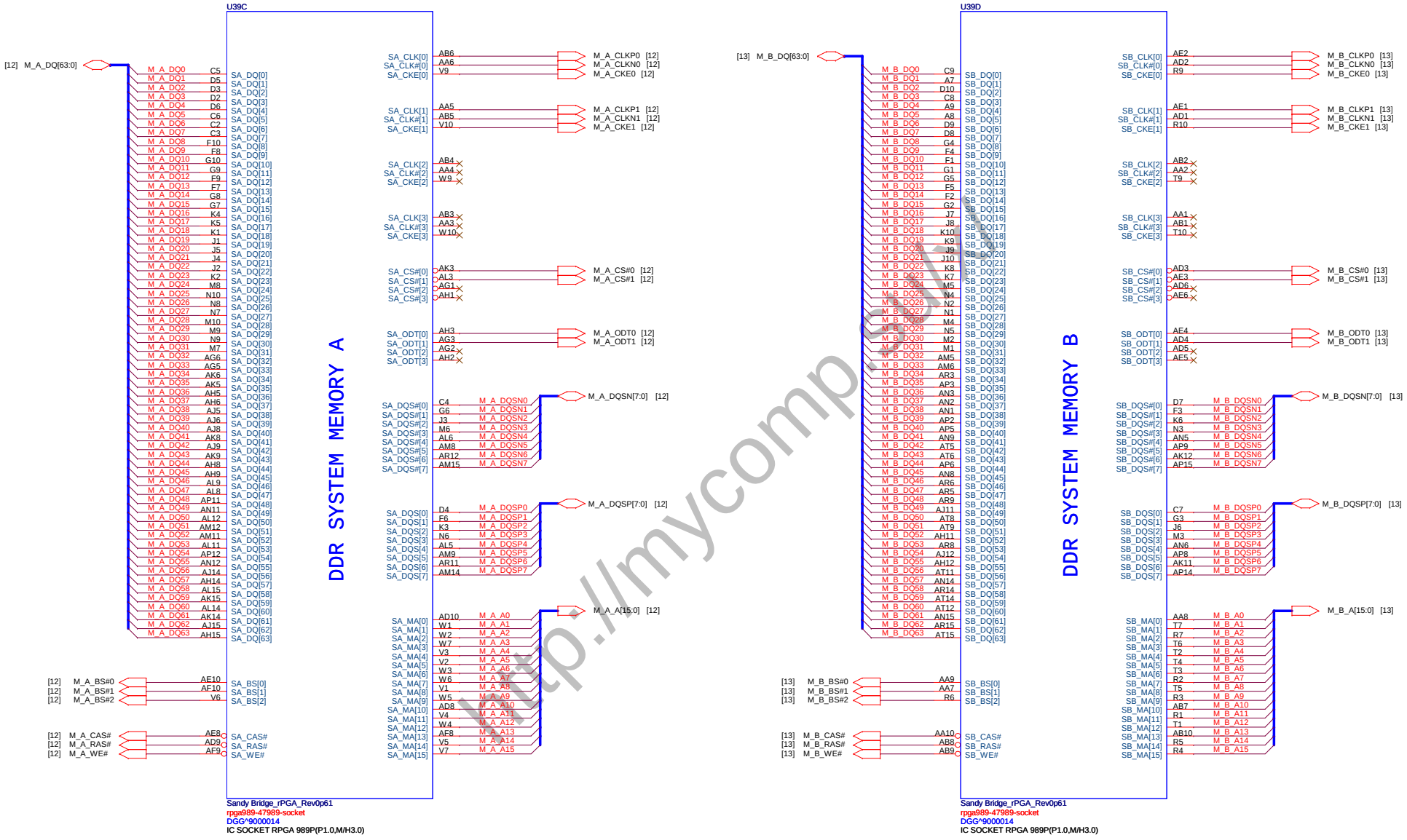
PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)



NB5/RD2	PROJECT : SP9 (Huron River)	
	Quanta Computer Inc.	
Size: Custom	Document Number: SNB 1/4 (PCIE&DMI&FDI)	Rev: 1A
Date: Tuesday, August 10, 2010	Sheet 2 of 49	

Sandy Bridge Processor (DDR3)



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

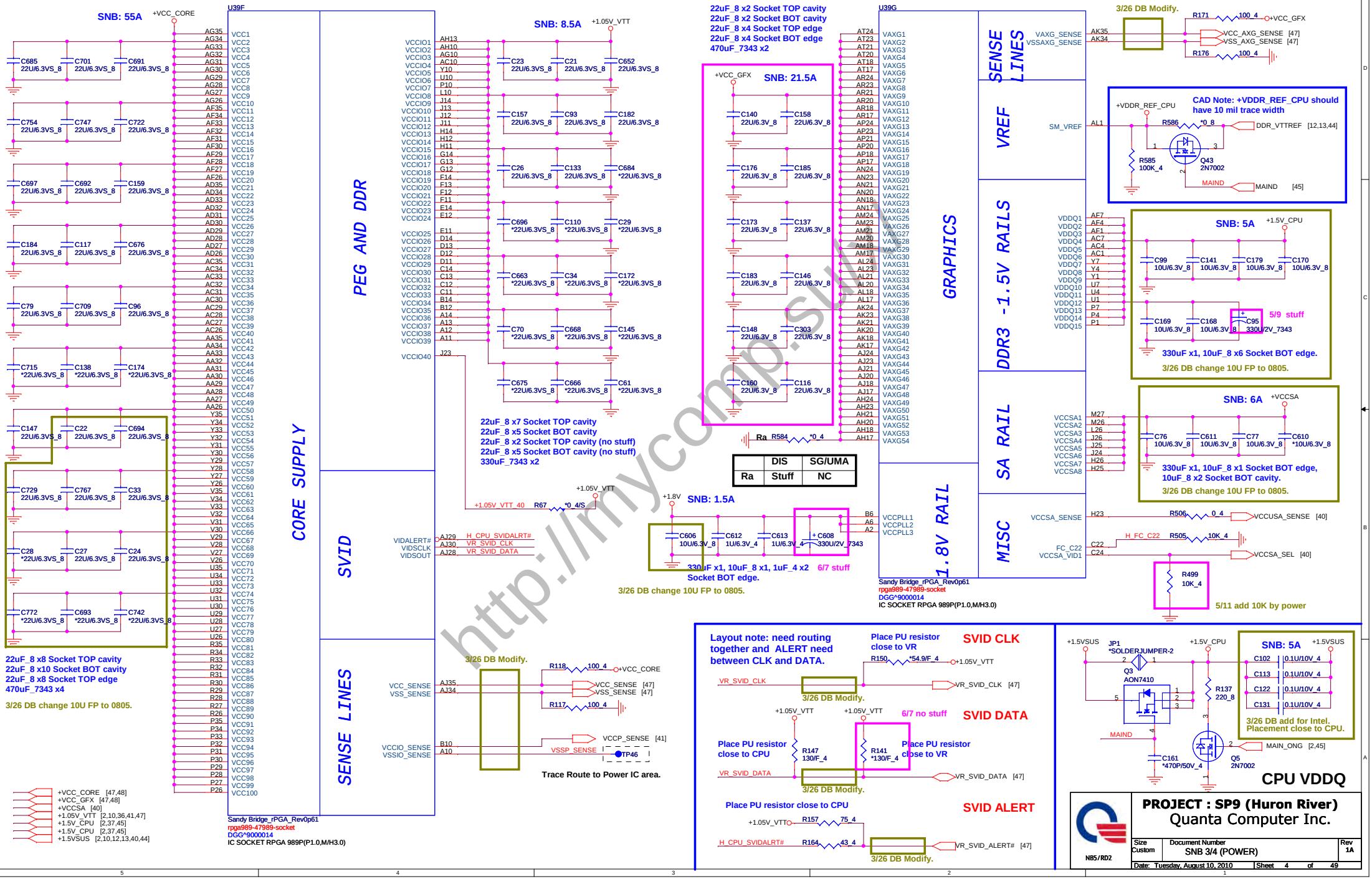
N85/RD2

Date: Tuesday, August 10, 2010 | Sheet 3 of 49

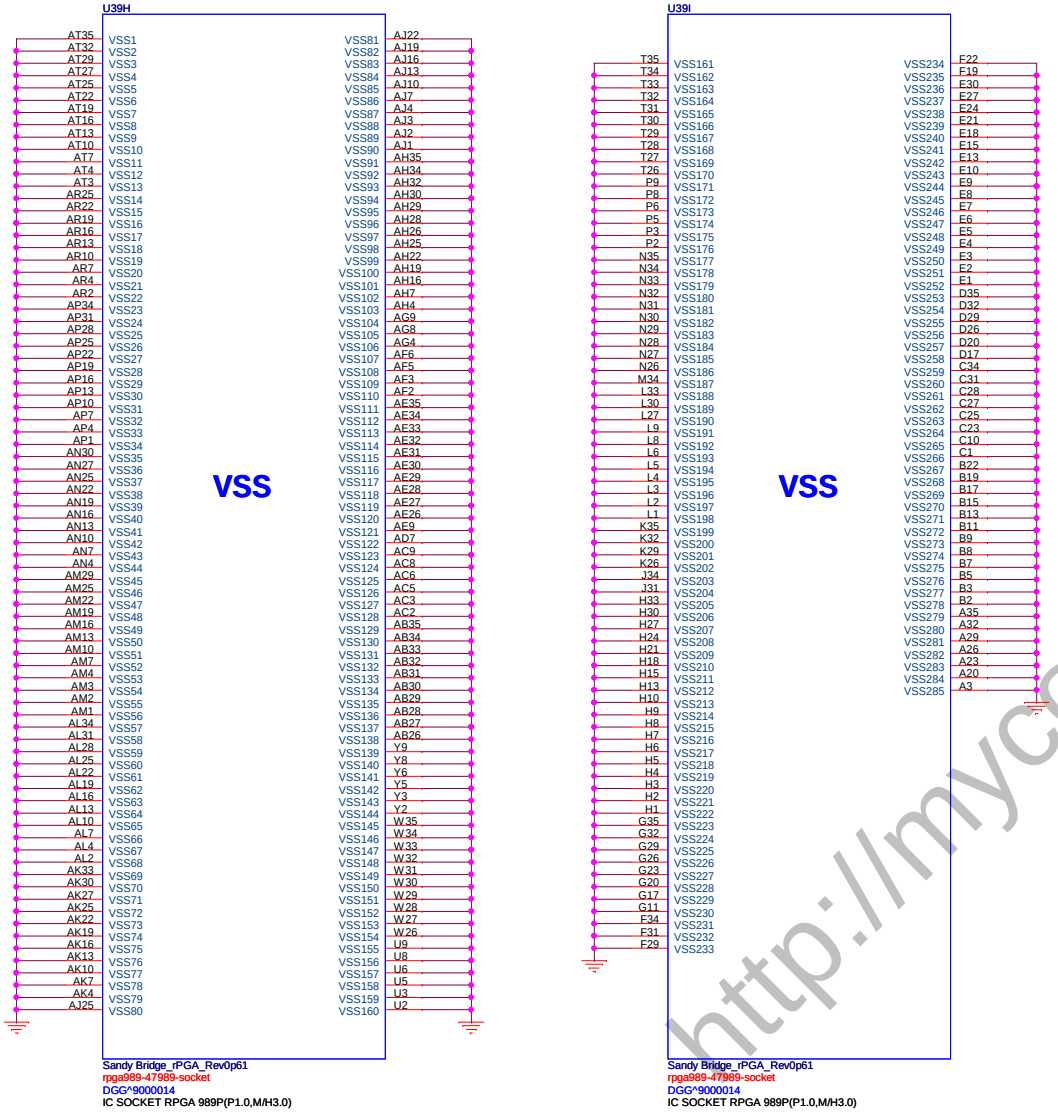
Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

04

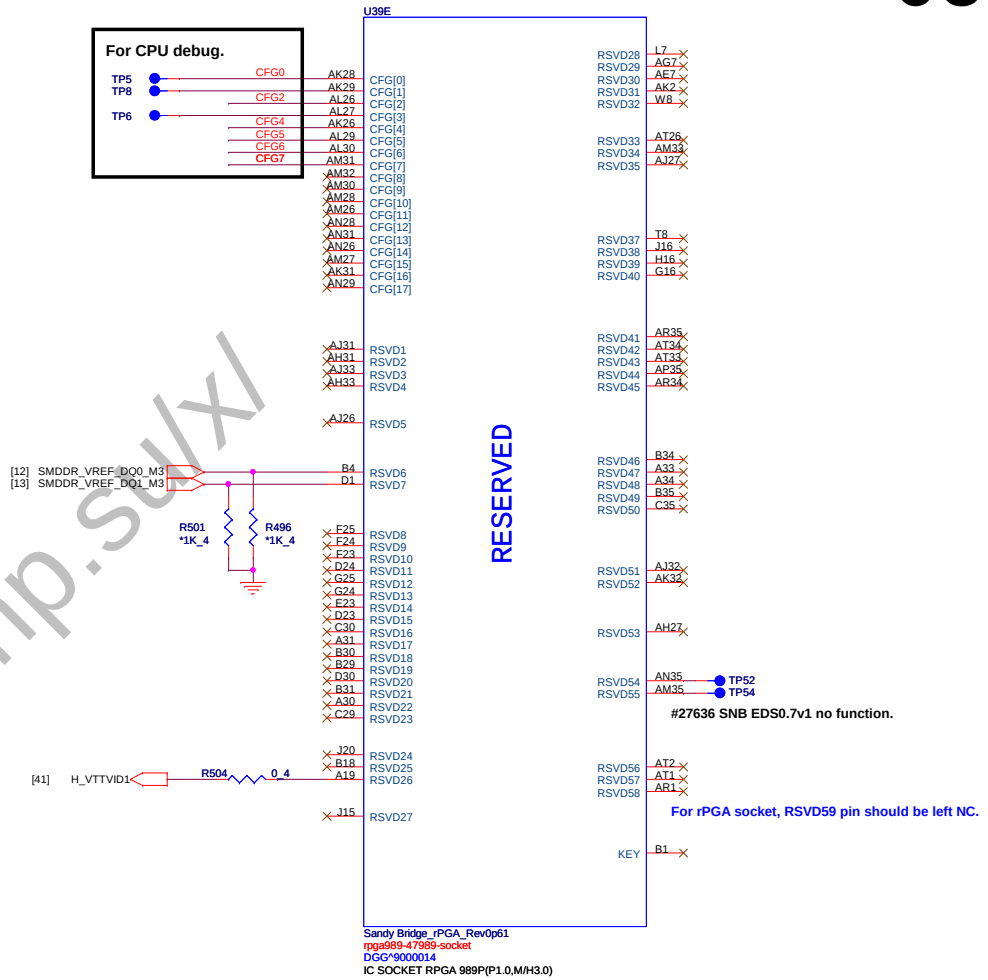


Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

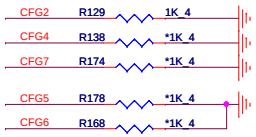
05



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

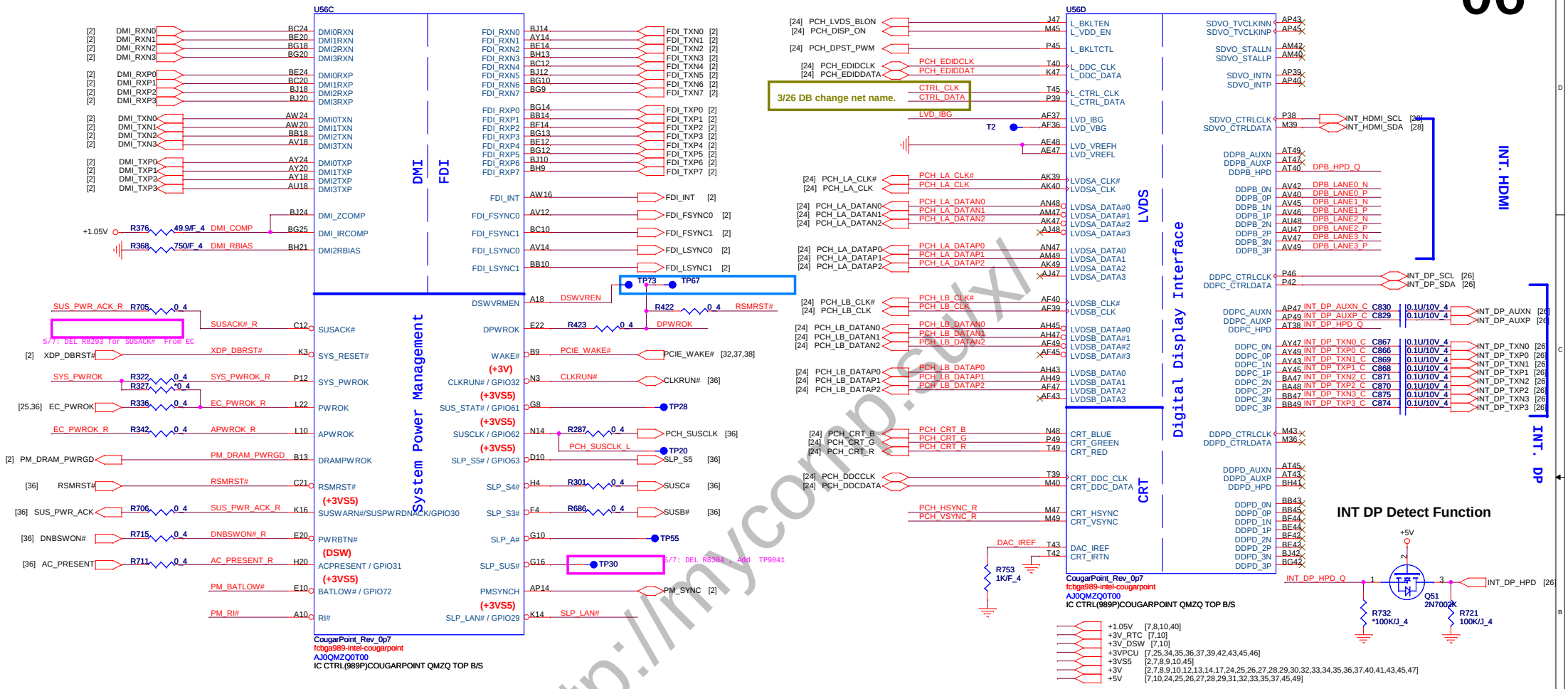
N85/RD2

Date: Tuesday, August 10, 2010 Sheet 5 of 49

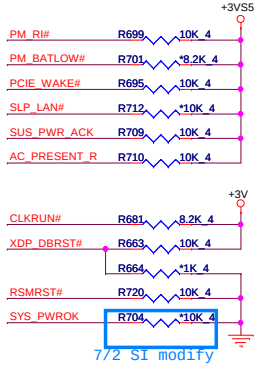
Cougar Point (DMI,FDI,PM)

Cougar Point (LVDS,DDI)

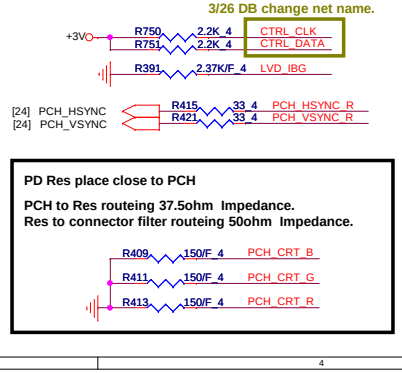
06



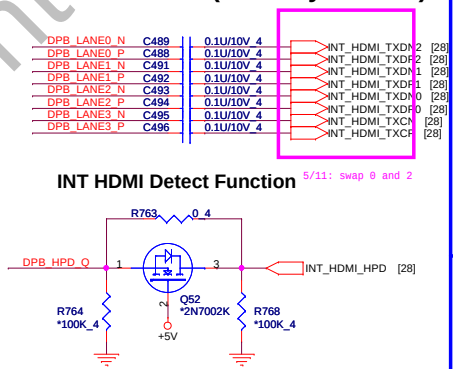
PCH Pull-high/low(CLG)



INT LVDS & CRT disable (DIS only remove)



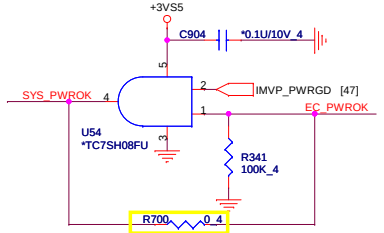
INT HDMI disable (DIS only remove)

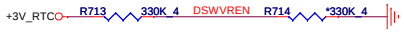


INT HDMI Detect Function

5/11: swap 0 and 2

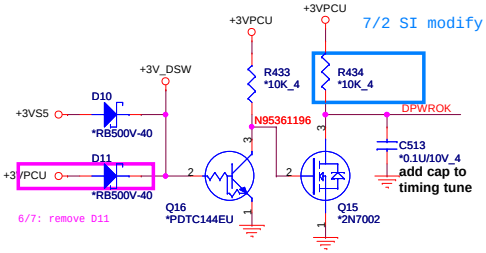
System PWR_OK(CLG)





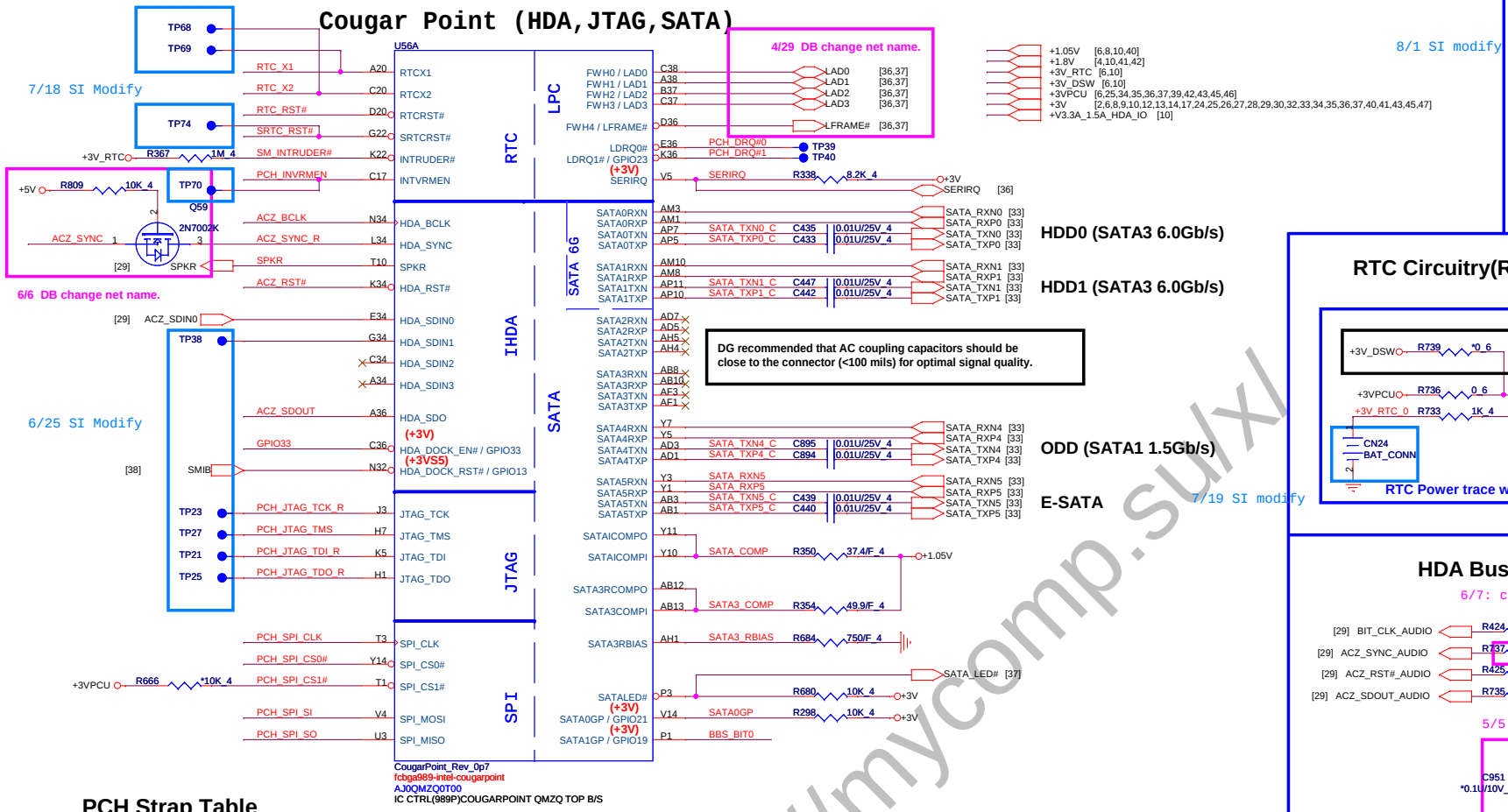
On Die DSW VR Enable
High = Enable (Default)
Low = Disable

DPWROK FOR DSW



PROJECT : SP9 (Huron River)		
Quanta Computer Inc.		
Size: Custom	Document Number: PCH 1/6 (DMI/FDI/VIDEO)	Rev: 1A
N85/RD2	Date: Tuesday, August 10, 2010	Sheet 6 of 49

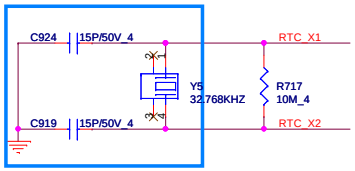
Cougar Point (HDA,JTAG,SATA)



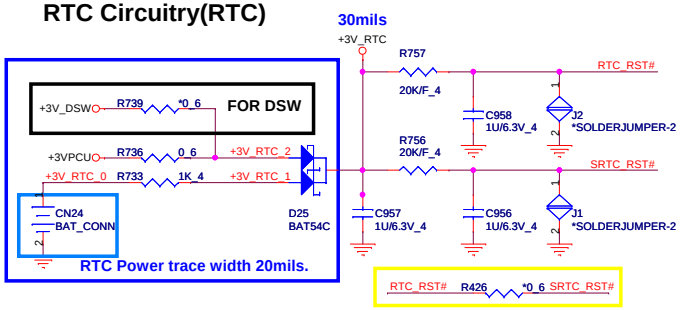
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR (Different from Calpella)	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R660 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R749 *1K_4 R746 10K_4 PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R716 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security (Only for Interposer)	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R727 1K_4 GPIO33_E [36]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 (Different from Calpella)	Boot BIOS Selection 0 [bit-0]	PWROK		R667 *1K_4 R752 *1K_4 BBS_BIT0 BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection (Only for Interposer)	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R691 *1K_4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm (4/30 reserve.)	+1.8V R678 2.2K_4 R694 4.7K_4 NV_CLE [8] H_SNB_IVB# [2] (N.A at CPT EDS 0.7)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R734 1K_4 ACZ_SYNC_R (5/4 add)
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDOUT R738 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R703 *1K_4 ICC_EN# [9] (4/29 reserve.)
GPIO28 (Different from Calpella)	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R693 *1K_4 PLL_ODVR_EN [9]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R308 1K_4 +3V

RTC Clock 32.768KHz

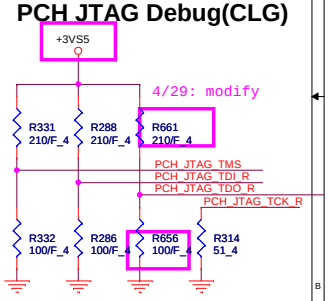


RTC Circuitry(RTC)

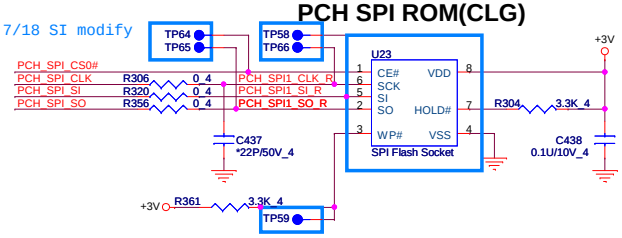


HDA Bus(CLG)

PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

N85/RD2

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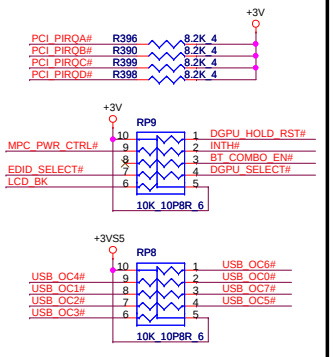
Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)



MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R769 *1K_4

PCI

PCI_PIRQA# K40 PIRQA#
PCI_PIRQB# K38 PIRQB#
PCI_PIRQC# H38 PIRQC#
PCI_PIRQD# G38 PIRQD#

[37] BT_COMBO_EN# C46 REQ1# / GPIO50 (+3V)
[24,26,28] DGPU_SELECT# C44 REQ2# / GPIO52 (+3V)
[24] EDID_SELECT# E40 REQ3# / GPIO54 (+3V)

[7] BBS_BIT1 D47 GNT1# / GPIO51 (+3V)
[24] PWM_SELECT# E42 GNT2# / GPIO53 (+3V)
[7] PCI_GNT3# F46 GNT3# / GPIO55 (+3V)

[25] LCD_BK G42 PIRQE# / GPIO2 (+3V)
[35] DGPU_HOLD_RST# G40 PIRQF# / GPIO3 (+3V)
[30] INTH# C42 PIRQG# / GPIO4 (+3V)
D44 PIRQH# / GPIO5 (+3V)

Bios swap GPIO 4/28.

TP29 K10 PME#
PCI_PLTRST# C6 PLTRST#

TP56 CLK_PCI_TPM_R H49 CLKOUT_PCI0
TP41 CLK_PCI_CARD_R H43 CLKOUT_PCI1
J48 CLKOUT_PCI2
[37] CLK_33M_DEBUG R414 22_4 K42 CLKOUT_PCI3
[36] CLK_33M_KBC R406 22_4 H40 CLKOUT_PCI4
CLK_PCI_FB R405 22_4
CLK_PCI_FB_R
CLK_PCI_LPC_R
CLK_PCI_EC_R

USB

(+3VS5) OC0# / GPIO59 A14 USB_OC0# → USB_OC0# [38]
(+3VS5) OC1# / GPIO40 K20 USB_OC1#
(+3VS5) OC2# / GPIO41 B17 USB_OC2#
(+3VS5) OC3# / GPIO42 C16 USB_OC3#
(+3VS5) OC4# / GPIO43 L16 USB_OC4#
(+3VS5) OC5# / GPIO9 A16 USB_OC5#
(+3VS5) OC6# / GPIO10 D14 USB_OC6#
(+3VS5) OC7# / GPIO14 C14 USB_OC7#

USBRBIAS# C33 USB_BIAS
R718 22.6/F_4
USBRBIAS B33

USBP0N C24
USBP0P A24
USBP1N C25 USBP0- [33]
USBP1P B25 USBP0+ [33] [E-SATA]
USBP2N C26
USBP2P A26
USBP3N K28 TP34 [Fingerprint]
USBP3P H28 TP35
USBP4N E28 USBP4- [34]
USBP4P D28 USBP4+ [34] [Webcam]
USBP5N C28 USBP5- [38]
USBP5P A28 USBP5+ [38] [USB 3.0 Co-layout]
USBP6N C29
USBP6P B29
USBP7N N28
USBP7P M28
USBP8N L30 USBP8- [34]
USBP8P K30 USBP8+ [34] [Right USB #1]
USBP9N G30 USBP9- [34] [Right USB #2]
USBP9P E30 USBP9+ [34]
USBP10N C30 USBP10- [37]
USBP10P A30 USBP10+ [37] [WLAN]
USBP11N L32 TP37
USBP11P K32 TP36
USBP12N G32 USBP12- [34] [Card Reaer]
USBP12P E32 USBP12+ [34]
USBP13N C32 USBP13- [34] [Blue Tooth LCD]
USBP13P A32 USBP13+ [34]

NVRAM

NV_CE#0 AY7
NV_CE#1 AV7
NV_CE#2 AU3
NV_CE#3 BG4
NV_DQS0 AT10
NV_DQS1 BC8
NV_DQ0 / NV_IO0 AU2
NV_DQ1 / NV_IO1 AT4
NV_DQ2 / NV_IO2 AT3
NV_DQ3 / NV_IO3 AT1
NV_DQ4 / NV_IO4 AY3
NV_DQ5 / NV_IO5 AT5
NV_DQ6 / NV_IO6 AV3
NV_DQ7 / NV_IO7 AV1
NV_DQ8 / NV_IO8 BB1
NV_DQ9 / NV_IO9 BA3
NV_DQ10 / NV_IO10 BB5
NV_DQ11 / NV_IO11 BB3
NV_DQ12 / NV_IO12 BB7
NV_DQ13 / NV_IO13 BE8
NV_DQ14 / NV_IO14 BD4
NV_DQ15 / NV_IO15 BF6

NV_ALE AV5 NV_ALE → NV_ALE [7]
NV_CLE AY1 NV_CLE → NV_CLE [7]
NV_RCOMP AV10
NV_RB# AT8
NV_RE#_WRB0 AY5
NV_RE#_WRB1 BA2
NV_WE#_CK0 AT12
NV_WE#_CK1 BF3

RSVD

TP1 BG26
TP2 BJ26
TP3 BH25
TP4 BJ16
TP5 BG16
TP6 AH38
TP7 AH37
TP8 AK43
TP9 AK45
TP10 C18
TP11 N30
TP12 H3
TP13 AH12
TP14 AM4
TP15 AM5
TP16 Y13
TP17 K24
TP18 L24
TP19 AB46
TP20 AB45

TP21 B21
TP22 M20
TP23 AY16
TP24 BG46

TP25 BE28
TP26 BC30
TP27 BE32
TP28 BJ32
TP29 BC28
TP30 BE30
TP31 BE32
TP32 BG32
TP33 AV26
TP34 BB26
TP35 AU28
TP36 AY30
TP37 AU26
TP38 AY26
TP39 AV28
TP40 AW30

[USB3.0]

WLAN
[37] PCIE_RXN1 BG34 PERN1
[37] PCIE_RXP1 BJ34 PERP1
[37] PCIE_TXN1 C477 0.1U/10V_4 PCIE_TXN1_C AV32 PETN1
[37] PCIE_TXP1 C481 0.1U/10V_4 PCIE_TXP1_C AU32 PETP1

LAN
[32] PCIE_RXN2_LAN BE34 PERN2
[32] PCIE_RXP2_LAN BF34 PERP2
[32] PCIE_TXN2_LAN C485 0.1U/10V_4 PCIE_TXN2_LAN_C BB32 PETN2
[32] PCIE_TXP2_LAN C486 0.1U/10V_4 PCIE_TXP2_LAN_C AY32 PETP2

[38] PCIE_RXN1_USB3.0 BG36 PERN3
[38] PCIE_RXP1_USB3.0 BJ36 PERP3
[38] PCIE_TXN1_USB3.0 C484 .1U/10V_4 PCIE_TXN3_C AV34 PETN3
[38] PCIE_TXP1_USB3.0 C487 .1U/10V_4 PCIE_TXP3_C AU34 PETP3

BF36 PERN4
BE36 PERP4
AY34 PETN4
BB34 PETP4
BG37 PERN5
BH37 PERP5
AY36 PETN5
BB36 PETP5
BJ38 PERN6
BG38 PERP6
AU36 PETN6
AV36 PETP6
BG40 PERN7
BJ40 PERP7
AY40 PETN7
BB40 PETP7
BE38 PERN8
BC38 PERP8
AW38 PETN8
AY38 PETP8

PCI-E*

SMBUS

(+3VS5) SMBALERT# / GPIO11 E12 SMBALERT#
SMBCLK H14 SMB_PCH_CLK
SMBDATA C9 SMB_PCH_DAT
(+3VS5) SML0ALERT# / GPIO60 A12 DRAMRST_CNTRL_PCH → DRAMRST_CNTRL_PCH [2]
SML0CLK C8 SMB_ME0_CLK
SML0DATA G12 SMB_ME0_DAT
(+3VS5) SML1ALERT# / PCHHOT# / GPIO74 C13 SML1ALERT#_R → TP33
(+3VS5) SML1CLK / GPIO58 E14 SMB_ME1_CLK
(+3VS5) SML1DATA / GPIO75 M16 SMB_ME1_DAT

Controller Link

CL_CLK1 M7 CL_CLK_R → TP22
CL_DATA1 T11 CL_DAT_R → TP24
CL_RST1# P10 CL_RST#_R → TP26

CLOCKS

(+3VS5) PEG_A_CLKRQ# / GPIO47 M10 CLK_PEGA_REQ#
CLKOUT_PEG_A_N AB37 CLK_PCH_PEGAN
CLKOUT_PEG_A_P AB38 CLK_PCH_PEGAP
CLKOUT_DMI_N AV22 CLK_CPU_BCLKN [2]
CLKOUT_DMI_P AU22 CLK_CPU_BCLKP [2]
CLKOUT_DP_N AM12 CLK_DPLL_SSCLKN [2]
CLKOUT_DP_P AM13 CLK_DPLL_SSCLKP [2]
CLKIN_DMI_N BF18 CLK_BUF_PCIE_3GPLL#
CLKIN_DMI_P BE18 CLK_BUF_PCIE_3GPLL
CLKIN_GND1_N BJ30 CLK_BUF_BCLK_N
CLKIN_GND1_P BG30 CLK_BUF_BCLK_P
CLKIN_DOT_96N G24 CLK_BUF_DREFCLK#
CLKIN_DOT_96P E24 CLK_BUF_DREFCLK
CLKIN_SATA_N AK7 CLK_BUF_DREFSSCLK#
CLKIN_SATA_P AK5 CLK_BUF_DREFSSCLK
REFCLK14IN K45 CLK_PCH_14M
CLKIN_PCILOOPBACK H45 CLK_PCI_FB

3/26 DB del external clock generator.

4/19 change FB to small size

TP71
C953 27P/50V_4
Y6 25MHZ
C952 27P/50V_4
TP72
+1.05V

XTAL25_IN V47 XTAL25_IN
XTAL25_OUT V49 XTAL25_OUT
XCLK_RCOMP Y47 XCLK_RCOMP R741 90.9/F_4

5/13: modify CLK_48M to CLK_FLEX1

(+3V) CLKOUTFLEX0 / GPIO64 L43 CLK_FLEX0 → TP42
(+3V) CLKOUTFLEX1 / GPIO65 L47 CLK_FLEX1 R412 22_4 → CLK_48M_QR [38]
(+3V) CLKOUTFLEX2 / GPIO66 M47 CLK_FLEX2 → TP57
(+3V) CLKOUTFLEX3 / GPIO67 L49 CLK_FLEX3 R416 *22_4 → PCH_CLK27M_1

Remove Ra, Rb for UMA & SG.
27MHz support DIS only.

FLEX CLOCKS

CLK_PCH_SRC0N Y40
CLK_PCH_SRC0P Y39
CLK_PCIE_REQ0# J2
CLK_PCH_SRC2N AB49
CLK_PCH_SRC2P AB47
CLK_PCIE_REQ1# M1
CLK_PCIE_REQ2# V10
CLK_PCIE_REQ3# A8
CLK_PCIE_REQ4# L12

CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0# / GPIO73
(+3VS5)
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1# / GPIO18
(+3V)
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2# / GPIO20
(+3V)
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3# / GPIO25
(+3VS5)
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4# / GPIO26
(+3VS5)
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5# / GPIO44
(+3VS5)
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ# / GPIO56
(+3VS5)
CLKOUT_PCIE6N
CLKOUT_PCIE6P
PCIECLKRQ6# / GPIO45
(+3VS5)
CLKOUT_PCIE7N
CLKOUT_PCIE7P
PCIECLKRQ7# / GPIO46
(+3VS5)
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P

CLK_PCH_ITPN AK14
CLK_PCH_ITPP AK13
TP32
TP31

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMZQ TOP B/S

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMZQ TOP B/S

USB 3.0

[9] BOARD_ID0 → RP4 0_4P2R_4 → CLK_USB3.0_GEN2N# AB42, CLK_USB3.0_GEN2P AB40
[38] CLK_USB3.0_GEN2N#
[38] CLK_USB3.0_GEN2P
R305 0_4 CLK_PEGB_REQ# E6
[38] PCIE_CLK_REQB#
[9] BOARD_ID1
[9] BOARD_ID2

Bios swap GPIO 4/23.

SMBUS

(+3VS5) SMBALERT# / GPIO11 E12 SMBALERT#
SMBCLK H14 SMB_PCH_CLK
SMBDATA C9 SMB_PCH_DAT
(+3VS5) SML0ALERT# / GPIO60 A12 DRAMRST_CNTRL_PCH → DRAMRST_CNTRL_PCH [2]
SML0CLK C8 SMB_ME0_CLK
SML0DATA G12 SMB_ME0_DAT
(+3VS5) SML1ALERT# / PCHHOT# / GPIO74 C13 SML1ALERT#_R → TP33
(+3VS5) SML1CLK / GPIO58 E14 SMB_ME1_CLK
(+3VS5) SML1DATA / GPIO75 M16 SMB_ME1_DAT

Reserve for Amp I2C 5/4.

+3V C974 *0.1U/10V_4
Q54 *2N7002E
Q56 *2N7002E
SMB_PCH_DAT → AMP_SDA [30]
C965 *0.1U/10V_4
SMB_PCH_CLK → AMP_SCL [30]
Q53 *2N7002E
Q57 *2N7002E
C973 *0.1U/10V_4
SMB_RUN_DAT R431 0_4 AMP_SDA
SMB_RUN_CLK R432 0_4 AMP_SCL

6/7 modified

7/18 : Modify PN

C502 .1U/10V_4
U27
PCH_CLK_27M → PCH_CLK_27M [17]
*74LVC1G126
R808 *0_4

PLTRST#(CLG)

+3VS5
C431 *0.1U/10V_4
U22 *TC7SH08FU
PCI_PLTRST# → PLTRST# 4/29 modify
R283 100K_4
R292 0_4
PLTRST# → PLTRST# [2,32,35,36,37,38]

PEG Clock detect (SG only)

DGPU_PWROK [9,36,42,43,44]
Q14 *2N7002
CLK_PEGA_REQ#
5/7: modify

SMBus/Pull-up(CLG)

4/20 modify

[13,26,30,36] MBCLK2 → Q49 2N7002K → SMB_ME1_CLK
R702 2.2K_4
R708 2.2K_4
[13,26,30,36] MBDATA2 → Q50 2N7002K → SMB_ME1_DAT

SMB_PCH_DAT → Q13 2N7002K → SMB_RUN_DAT [12,13]
R290 4.7K_4
R289 4.7K_4
SMB_PCH_CLK → Q12 2N7002K → SMB_RUN_CLK [12,13]

CLK_REQ/Strap Pin(CLG)

CLK_PCIE_REQ1# R329 10K_4
CLK_PCIE_REQ2# R315 10K_4
CLK_PCIE_REQ0# R689 10K_4
CLK_PCIE_REQ3# R692 10K_4
CLK_PCIE_REQ4# R323 10K_4
CLK_PEGB_REQ# R310 10K_4
CLK_PEGA_REQ# Ra R325 *10K_4
CLK_PEGA_REQ# Rb R311 10K_4
SG : Rb ; UMA : Ra
CLK_BUF_BCLK_N R382 10K_4
CLK_BUF_BCLK_P R381 10K_4
CLK_BUF_PCIE_3GPLL# R362 10K_4
CLK_BUF_PCIE_3GPLL R357 10K_4
CLK_BUF_DREFCLK# R377 10K_4
CLK_BUF_DREFCLK R379 10K_4
CLK_BUF_DREFSSCLK# R334 10K_4
CLK_BUF_DREFSSCLK R335 10K_4
CLK_PCH_14M R407 10K_4
CLOCK TERMINATION for FCIM

PCIE Clock

3/26 DB change Part reference.

WLAN
[37] CLK_PCIE_WLANN
[37] CLK_PCIE_WLANP
RP1 0_4P2R_4 → CLK_PCH_SRC0N, CLK_PCH_SRC0P
[37] PCIE_CLKREQ_WLAN#
R674 0_4 CLK_PCIE_REQ0#

LAN
[32] CLK_PCIE_LANN
[32] CLK_PCIE_LANP
RP3 0_4P2R_4 → CLK_PCH_SRC2N, CLK_PCH_SRC2P
[32] PCIE_CLKREQ_LAN#
R679 0_4 CLK_PCIE_REQ1#

GPU
[14] CLK_PCIE_VGA#
[14] CLK_PCIE_VGA
RP2 0_4P2R_4 → CLK_PCH_PEGAN, CLK_PCH_PEGAP

+3VS5 [2,6,7,9,10,45]
+3V [2,6,7,9,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]

SMBus/Pull-up(CLG)

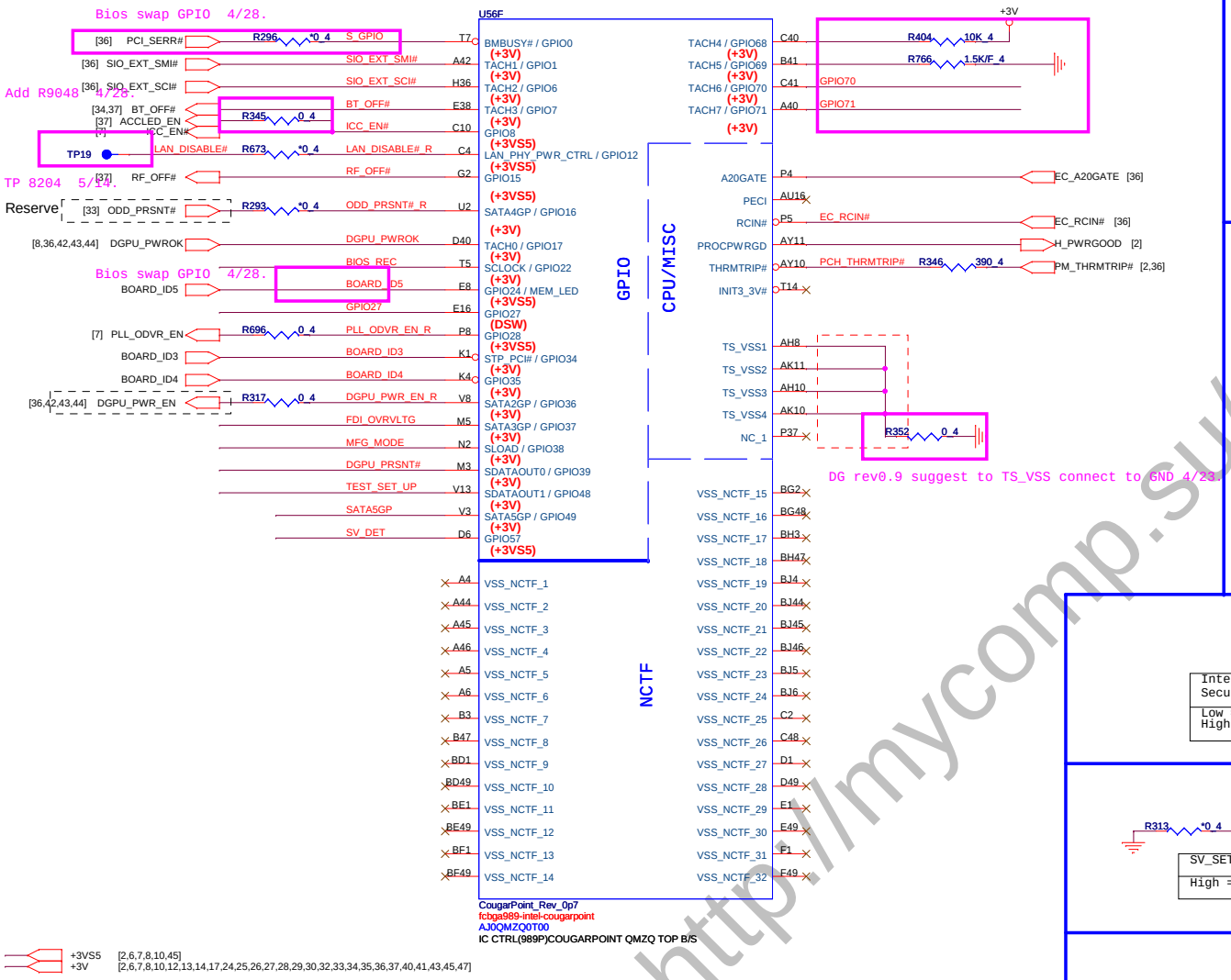
+3VS5
R330 1K_4 DRAMRST_CNTRL_PCH
R337 10K_4 SMBALERT#
R347 2.2K_4 SMB_PCH_CLK
R343 2.2K_4 SMB_PCH_DAT
R677 2.2K_4 SMB_ME0_CLK
R349 2.2K_4 SMB_ME0_DAT
R364 10K_4 SML1ALERT#_R

NB5/RD2

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

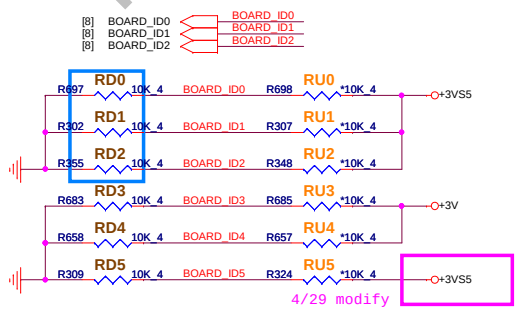
Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	1A
Date: Tuesday, August 10, 2010	Sheet 8 of 49	

Cougar Point (GPIO,VSS_NCTF,RSVD)



Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
SP9 2D	0	0	0	0	0	0
SP9 3D	0	0	0	0	0	1

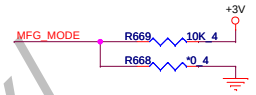
8/2 SI Modify



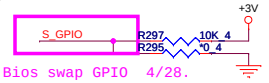
Clock Gen Power OK (CLG)

3/26 DB del external clock generator.

MFG-TEST

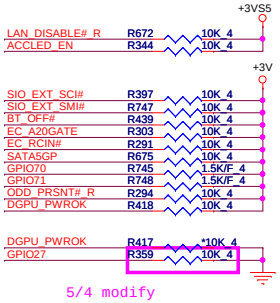


SGPIO

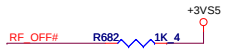


Bios swap GPIO 4/28.

GPIO Pull-up/Pull-down(CLG)



5/4 modify



Intel ME Crypto Transport Layer Security (TLS) cipher suite	Low = Disable (Default) High = Enable

BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP
High = Strong (Default)

TEST DETECT
Low = Default

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

GFX Present

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
N85/RD2	Date: Tuesday, August 10, 2010	Sheet 9 of 49

Cougar Point-M (POWER)

COUGAR POINT (POWER)

7/29 SI Modify for CRT noise

10

U56J

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | CPU | MISC | RTC | HDA

U56G

VCC CORE | CRT | LVDS | HVCMOS | DMI | VCCIO | SPI | NAND | FDI

8/8 SI Modify

7/18 SI Modify

1.01A (60mils)

1.3 A (60mils)

2.925 A (140mils)

3mA (10mils)

119mA (20mils)

119mA (15mils)

266mA (20mils)

1.01A (60mils)

160mA (20mils)

65mA (10mils)

8mA (10mils)

55mA (10mils)

95mA (10mils)

10mA (10mils)

V_PROC_IO=1mA (10mils)

VCCRTC<1mA (10mils)

160mA (15mils) (Mobile 1.5V)

65mA (10mils)

8mA (10mils)

20mA (10mils)

20mA (10mils)

20mA (10mils)

1mA (10mils)

1mA (10mils)

60mA (10mils)

SG & UMA : Ra
DIS : Rb

42mA (10mils)

190 mA (15mils)

20mA (10mils)

V5REF= 1mA

VCC5REFSUS=1mA

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMZQ TOP B/S

+1.05V [6,7,8,40]
+1.05V_VTT [2,4,36,41,47]
+1.5VSUS [2,4,12,13,40,44]
+1.8V [4,7,41,42]

+3V_RTC [6,7]
+3V_DSW [6,7]
+3VS5 [2,6,7,8,9,45]
+3V [2,6,7,8,9,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
+5VS5 [25,45]
+5V [6,7,24,25,26,27,28,29,31,32,33,35,37,45,49]

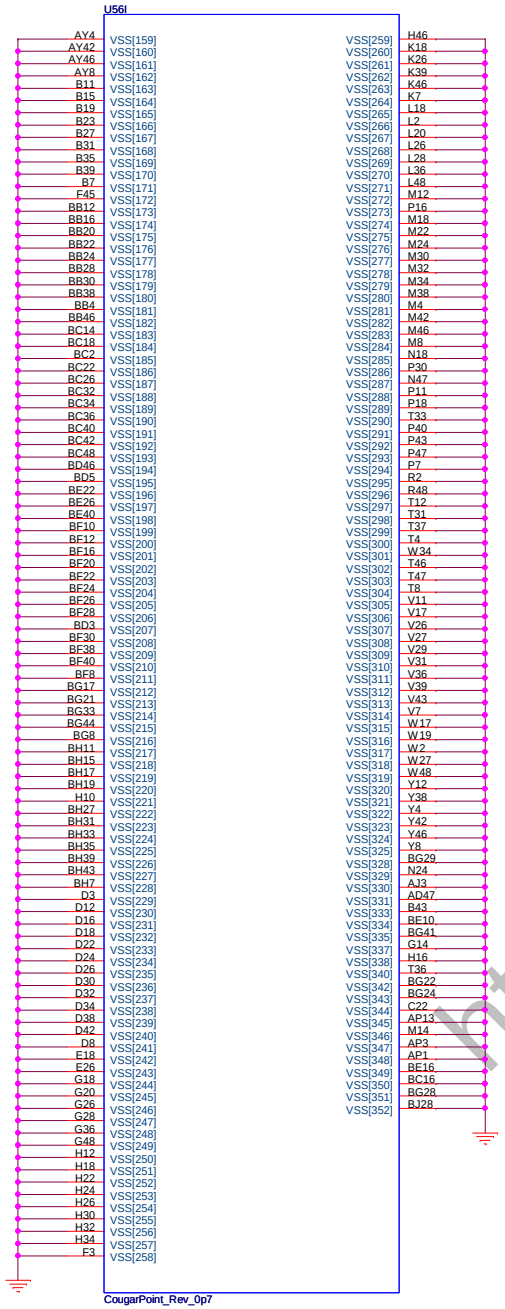
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A

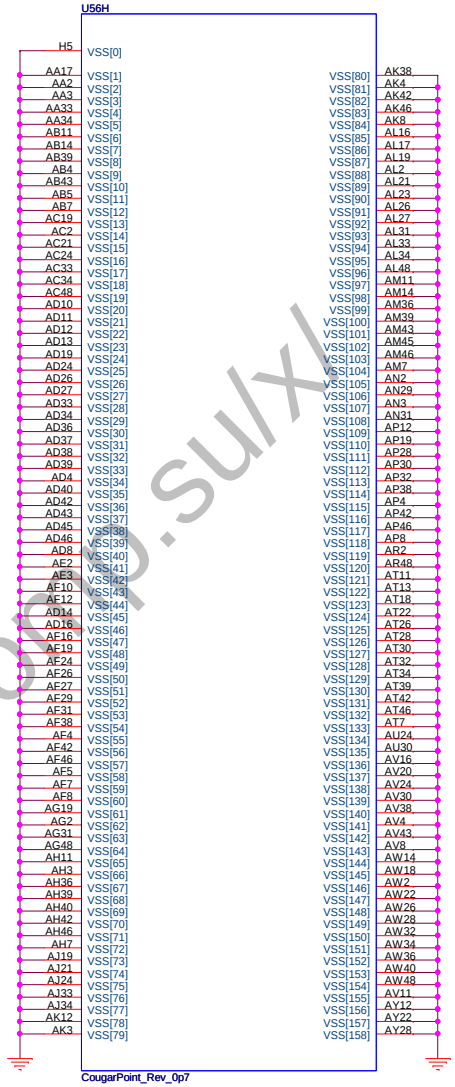
Date: Tuesday, August 10, 2010 | Sheet 10 of 49

N85/RD2

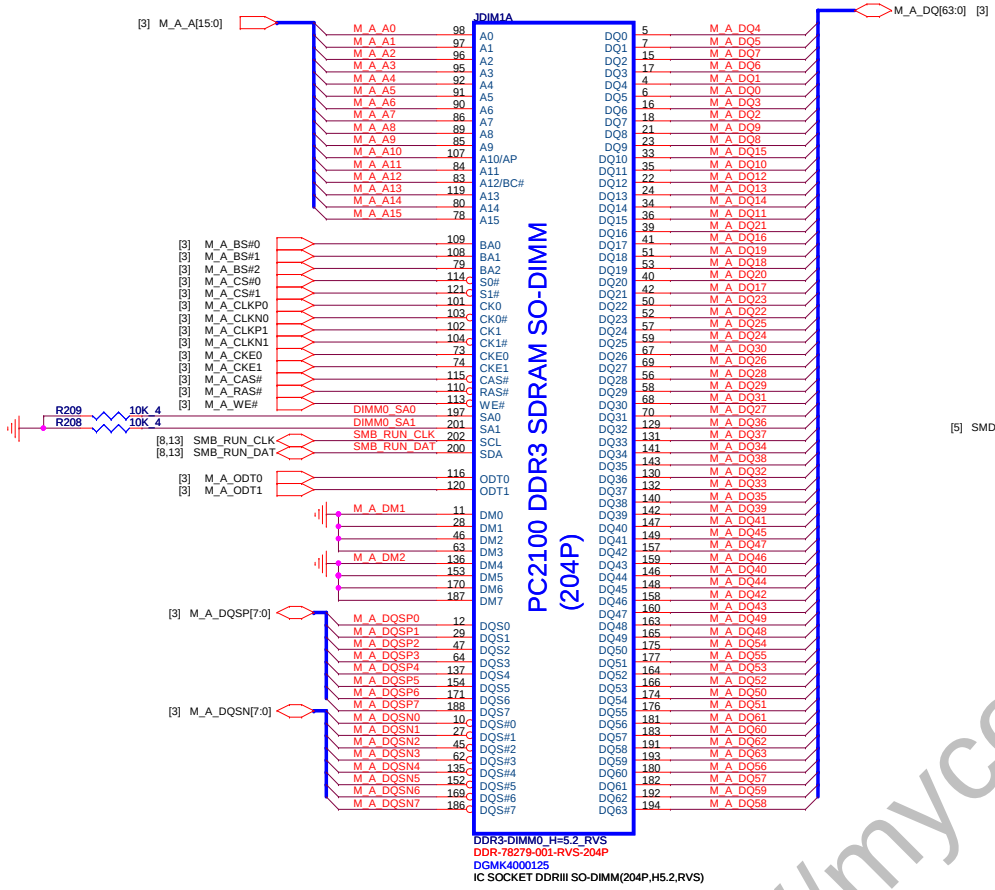
IBEX PEAK-M (GND)

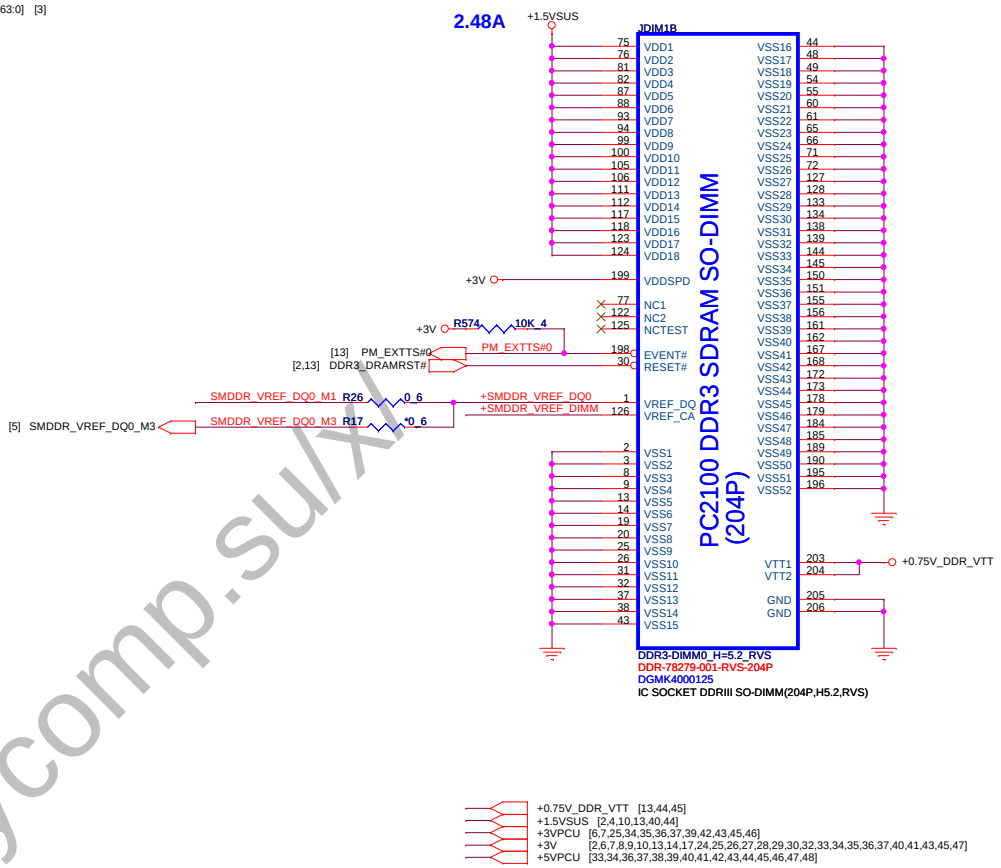


IBEX PEAK-M (GND)



N85/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.	
Size: Custom	Document Number: PCH 6/6 (GND)	Rev: 1A
Date: Tuesday, August 10, 2010	Sheet 11 of 49	

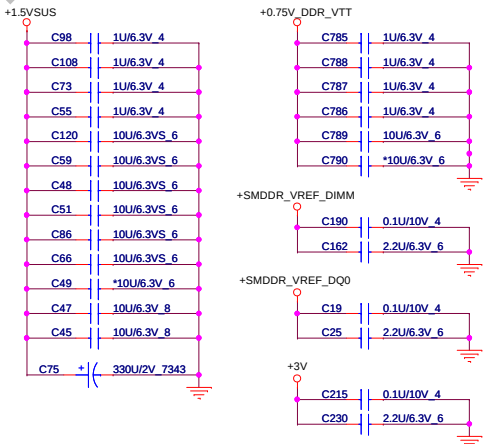




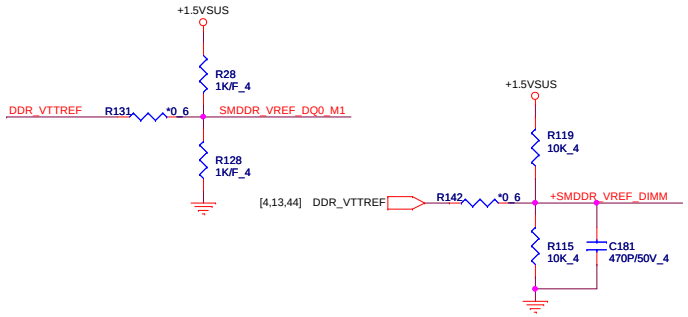
VREF DQ0 M2 Solution

7/18 : Del M2 solution

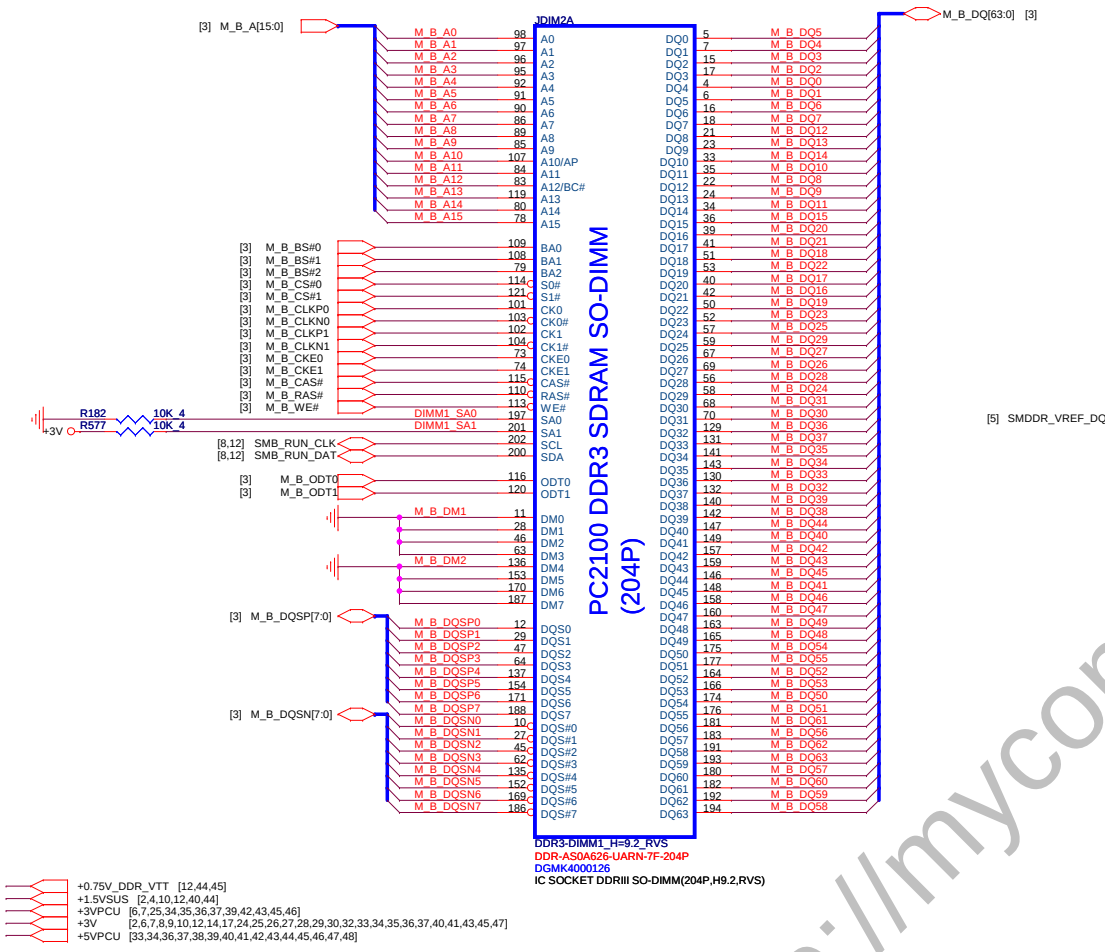
Place these Caps near So-Dimm0.

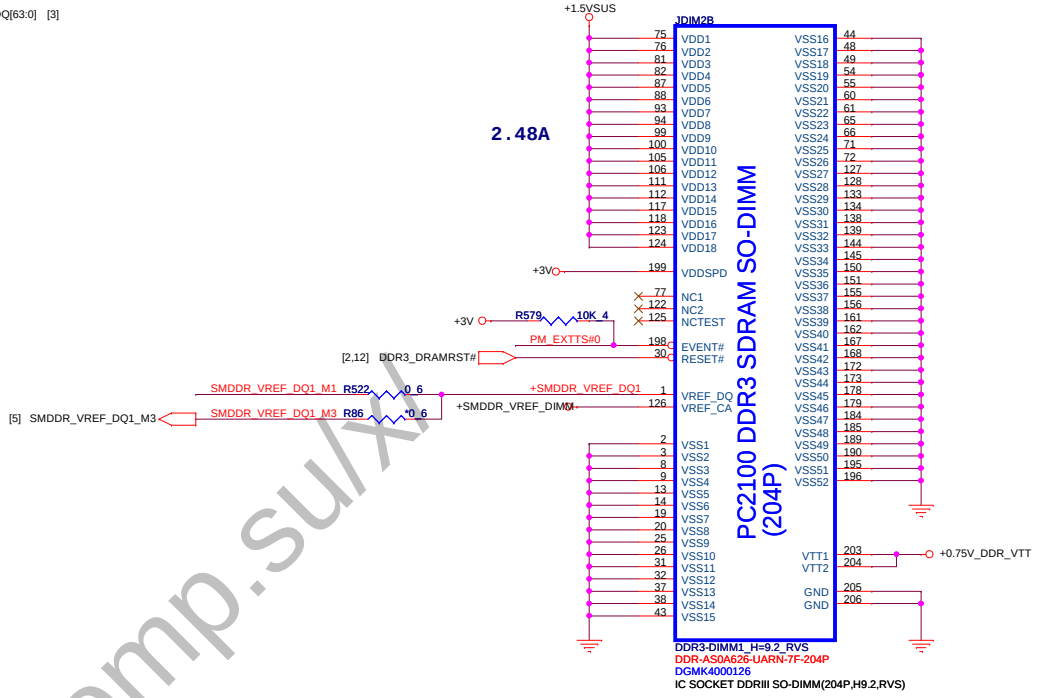


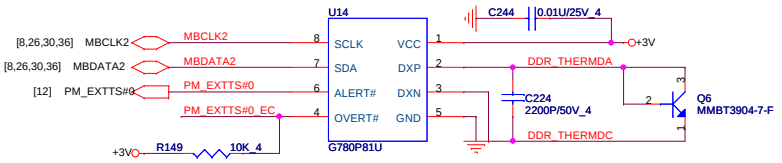
VREF DQ0 M1 Solution



N85/RD2	**PROJECT : SP9 (Huron River)** Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM0-RVS (5.2H)	Rev: 1A
Date: Tuesday, August 10, 2010	Sheet 12 of 49	



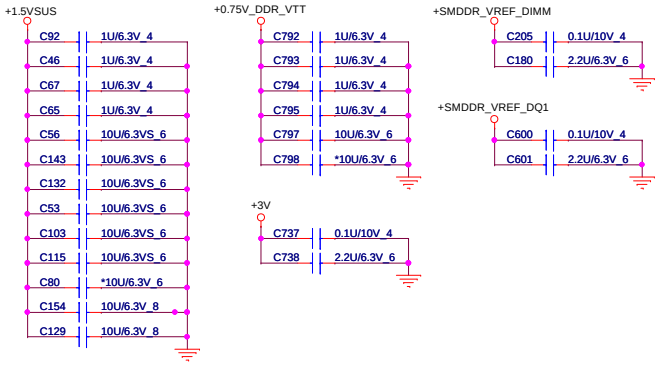




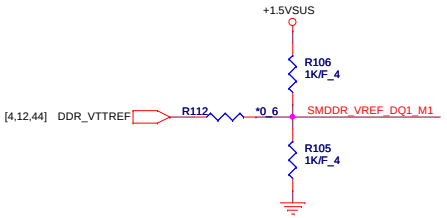
VREF DQ1 M2 Solution

7/18 : Del M2 solution

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A
Date: Tuesday, August 10, 2010	Sheet 13 of 49	

N85/RD2

[16,18,44] +1.0V_VGA
[4,7,10,41,42] +1.8V
[2,6,7,8,9,10,12,13,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47] +3V

U41A

PCI EXPRESS INTERFACE

[2] PEG_TX15	PEG_TX15 AA38	PCIE_RX0P	PCIE_TX0P Y33 C_PEG_RXP15 C239 .1U/10V_4 PEG_RX15 [2]
[2] PEG_TX#15	PEG_TX#15 Y37	PCIE_RX0N	PCIE_TX0N Y32 C_PEG_RXN15 C228 .1U/10V_4 PEG_RX#15 [2]
[2] PEG_TX14	PEG_TX14 Y35	PCIE_RX1P	PCIE_TX1P W33 C_PEG_RXP14 C254 .1U/10V_4 PEG_RX14 [2]
[2] PEG_TX#14	PEG_TX#14 W36	PCIE_RX1N	PCIE_TX1N W32 C_PEG_RXN14 C257 .1U/10V_4 PEG_RX#14 [2]
[2] PEG_TX13	PEG_TX13 W38	PCIE_RX2P	PCIE_TX2P U33 C_PEG_RXP13 C259 .1U/10V_4 PEG_RX13 [2]
[2] PEG_TX#13	PEG_TX#13 V37	PCIE_RX2N	PCIE_TX2N U32 C_PEG_RXN13 C265 .1U/10V_4 PEG_RX#13 [2]
[2] PEG_TX12	PEG_TX12 V35	PCIE_RX3P	PCIE_TX3P U30 C_PEG_RXP12 C253 .1U/10V_4 PEG_RX12 [2]
[2] PEG_TX#12	PEG_TX#12 U36	PCIE_RX3N	PCIE_TX3N U29 C_PEG_RXN12 C245 .1U/10V_4 PEG_RX#12 [2]
[2] PEG_TX11	PEG_TX11 U38	PCIE_RX4P	PCIE_TX4P T33 C_PEG_RXP11 C271 .1U/10V_4 PEG_RX11 [2]
[2] PEG_TX#11	PEG_TX#11 T37	PCIE_RX4N	PCIE_TX4N T32 C_PEG_RXN11 C281 .1U/10V_4 PEG_RX#11 [2]
[2] PEG_TX10	PEG_TX10 T35	PCIE_RX5P	PCIE_TX5P T30 C_PEG_RXP10 C266 .1U/10V_4 PEG_RX10 [2]
[2] PEG_TX#10	PEG_TX#10 R36	PCIE_RX5N	PCIE_TX5N T29 C_PEG_RXN10 C270 .1U/10V_4 PEG_RX#10 [2]
[2] PEG_TX9	PEG_TX9 R38	PCIE_RX6P	PCIE_TX6P P33 C_PEG_RXP9 C285 .1U/10V_4 PEG_RX9 [2]
[2] PEG_TX#9	PEG_TX#9 P37	PCIE_RX6N	PCIE_TX6N P32 C_PEG_RXN9 C289 .1U/10V_4 PEG_RX#9 [2]
[2] PEG_TX8	PEG_TX8 P35	PCIE_RX7P	PCIE_TX7P P30 C_PEG_RXP8 C286 .1U/10V_4 PEG_RX8 [2]
[2] PEG_TX#8	PEG_TX#8 N36	PCIE_RX7N	PCIE_TX7N P29 C_PEG_RXN8 C298 .1U/10V_4 PEG_RX#8 [2]
[2] PEG_TX7	PEG_TX7 N38	PCIE_RX8P	PCIE_TX8P N33 C_PEG_RXP7 C308 0.1U/10V_4 PEG_RX7 [2]
[2] PEG_TX#7	PEG_TX#7 M37	PCIE_RX8N	PCIE_TX8N N32 C_PEG_RXN7 C307 0.1U/10V_4 PEG_RX#7 [2]
[2] PEG_TX6	PEG_TX6 M35	PCIE_RX9P	PCIE_TX9P N30 C_PEG_RXP6 C300 0.1U/10V_4 PEG_RX6 [2]
[2] PEG_TX#6	PEG_TX#6 L36	PCIE_RX9N	PCIE_TX9N N29 C_PEG_RXN6 C306 0.1U/10V_4 PEG_RX#6 [2]
[2] PEG_TX5	PEG_TX5 L38	PCIE_RX10P	PCIE_TX10P L33 C_PEG_RXP5 C309 0.1U/10V_4 PEG_RX5 [2]
[2] PEG_TX#5	PEG_TX#5 K37	PCIE_RX10N	PCIE_TX10N L32 C_PEG_RXN5 C314 0.1U/10V_4 PEG_RX#5 [2]
[2] PEG_TX4	PEG_TX4 K35	PCIE_RX11P	PCIE_TX11P L30 C_PEG_RXP4 C312 0.1U/10V_4 PEG_RX4 [2]
[2] PEG_TX#4	PEG_TX#4 J36	PCIE_RX11N	PCIE_TX11N L29 C_PEG_RXN4 C315 0.1U/10V_4 PEG_RX#4 [2]
[2] PEG_TX3	PEG_TX3 J38	PCIE_RX12P	PCIE_TX12P K33 C_PEG_RXP3 C320 0.1U/10V_4 PEG_RX3 [2]
[2] PEG_TX#3	PEG_TX#3 H37	PCIE_RX12N	PCIE_TX12N K32 C_PEG_RXN3 C321 0.1U/10V_4 PEG_RX#3 [2]
[2] PEG_TX2	PEG_TX2 H35	PCIE_RX13P	PCIE_TX13P J33 C_PEG_RXP2 C322 0.1U/10V_4 PEG_RX2 [2]
[2] PEG_TX#2	PEG_TX#2 G36	PCIE_RX13N	PCIE_TX13N J32 C_PEG_RXN2 C323 0.1U/10V_4 PEG_RX#2 [2]
[2] PEG_TX1	PEG_TX1 G38	PCIE_RX14P	PCIE_TX14P K30 C_PEG_RXP1 C325 0.1U/10V_4 PEG_RX1 [2]
[2] PEG_TX#1	PEG_TX#1 F37	PCIE_RX14N	PCIE_TX14N K29 C_PEG_RXN1 C324 0.1U/10V_4 PEG_RX#1 [2]
[2] PEG_TX0	PEG_TX0 E35	PCIE_RX15P	PCIE_TX15P H33 C_PEG_RXP0 C318 0.1U/10V_4 PEG_RX0 [2]
[2] PEG_TX#0	PEG_TX#0 E37	PCIE_RX15N	PCIE_TX15N H32 C_PEG_RXN0 C319 0.1U/10V_4 PEG_RX#0 [2]

CLOCK

[8] CLK_PCIE_VGA	CLK_PCIE_VGA AB35	PCIE_REFCLKP
[8] CLK_PCIE_VGA#	CLK_PCIE_VGA# AA36	PCIE_REFCLKN

	AJ21	NC#1
	AK21	NC#2
PWRGOOD_BUF	AH16	PWRGOOD
[35] PEGX_RST#	AA30	PERSTB

CALIBRATION

PCIE_CALRP Y30 PCIE_CALRP R173 1.27K/F_4
PCIE_CALRN Y29 PCIE_CALRN R172 2K/F_4 +1.0V_VGA

Broadway

U41H

DP C/D POWER		DP A/B POWER	
+1.8V_DPC_VDD18	AP20 DPC_VDD18#1	DPA_VDD18#1	AN24 +1.8V_DPA_VDD18
	AP21 DPC_VDD18#2	DPA_VDD18#2	AP24
+1.0V_DPC_VDD10	AP13 DPC_VDD10#1	DPA_VDD10#1	AP31 +1.0V_DPA_VDD10
	AT13 DPC_VDD10#2	DPA_VDD10#2	AP32
	AN17 DPC_VSSR#1	DPA_VSSR#1	AN27
	AP16 DPC_VSSR#2	DPA_VSSR#2	AP27
	AP17 DPC_VSSR#3	DPA_VSSR#3	AP28
	AW14 DPC_VSSR#4	DPA_VSSR#4	AW24
	AW16 DPC_VSSR#5	DPA_VSSR#5	AW26
+1.8V_DPC_VDD18	AP22 DPD_VDD18#1	DPB_VDD18#1	AP25 +1.8V_DPA_VDD18
	AP23 DPD_VDD18#2	DPB_VDD18#2	AP26
+1.0V_DPC_VDD10	AP14 DPD_VDD10#1	DPB_VDD10#1	AN33
	AP15 DPD_VDD10#2	DPB_VDD10#2	AP33
	AN19 DPD_VSSR#1	DPB_VSSR#1	AN29
	AP18 DPD_VSSR#2	DPB_VSSR#2	AP29
	AP19 DPD_VSSR#3	DPB_VSSR#3	AP30
	AW20 DPD_VSSR#4	DPB_VSSR#4	AW30
	AW22 DPD_VSSR#5	DPB_VSSR#5	AW32
R45 150/F_4 DPCD_CALR	AW18 DPCD_CALR	DPAB_CALR	AW28 DPAB_CALR R539 150/F_4
DP E/F POWER		DP PLL POWER	
+1.8V_DPE_VDD18	AH34 DPE_VDD18#1	DPA_PVDD	AU28 +1.8V_VGA
	AJ34 DPE_VDD18#2	DPA_PVSS	AV27
+1.0V_DPE_VDD10	AL33 DPE_VDD10#1	DPB_PVDD	AV29
	AM33 DPE_VDD10#2	DPB_PVSS	AR28
	AN34 DPE_VSSR#1	DPC_PVDD	AU18
	AP39 DPE_VSSR#2	DPC_PVSS	AV17
	AR39 DPE_VSSR#3		
	AU37 DPE_VSSR#4		
+1.8V_DPE_VDD18	AF34 DPF_VDD18#1	DPD_PVDD	AV19
	AG34 DPF_VDD18#2	DPD_PVSS	AR18
+1.0V_DPE_VDD10	AK33 DPF_VDD10#1	DPE_PVDD	AM37
	AK34 DPF_VDD10#2	DPE_PVSS	AN38
	AF39 DPF_VSSR#1	DPF_PVDD	AL38
	AH39 DPF_VSSR#2	DPF_PVSS	AM35
	AK39 DPF_VSSR#3		
	AL34 DPF_VSSR#4		
	AM34 DPF_VSSR#5		
R545 150/F_4 DPEF_CALR	AM39 DPEF_CALR		

Broadway

(DPA/B_VDD10 : 1.0V@115mA+115mA) +1.0V_VGA
HCB1608KF-181T15_6 L13
C119 10U/6.3V_8 C135 1U/6.3V_4 C136 .1U/10V_4

AMD 0821

(DPB_PVDD : 1.8V@20mA) +1.8V_VGA
+1.8V_DPB_PVDD HCB1608KF-181T15_6 L50
C653 10U/6.3V_8 C658 1U/6.3V_4 C659 .1U/10V_4

(DPC_PVDD:1.8V@20mA) +1.8V_VGA
+1.8V_DPC_PVDD HCB1608KF-181T15_6 L44
C625 10U/6.3V_8 C637 .1U/10V_4 C632 1U/6.3V_4

(DPD_PVDD:1.8V@20mA) +1.8V_VGA
+1.8V_DPD_PVDD HCB1608KF-181T15_6 L47
C648 10U/6.3V_8 C660 .1U/10V_4 C655 1U/6.3V_4

(DPE/F_PVDD1.8V@20mA+20mA) +1.8V_VGA
+1.8V_DPE_PVDD HCB1608KF-181T15_6 L51
C670 10U/6.3V_8 C671 .1U/10V_4 C672 .1U/10V_4

for AMD comment add for SI

(DPE/F_VDD10 : 1.0V@115mA+115mA) +1.0V_VGA
+1.0V_DPE_VDD10 HCB1608KF-181T15_6 L12
C123 10U/6.3V_8 C126 1U/6.3V_4 C127 .1U/10V_4

(DPC/D_VDD10 : 1.0V@115mA+115mA) +1.0V_VGA
+1.0V_DPC_VDD10 HCB1608KF-181T15_6 L9
C107 10U/6.3V_8 C661 1U/6.3V_4 C656 .1U/10V_4

(DPE/F_VDD18 : 1.8V@200mA+200mA) +1.8V_VGA
+1.8V_DPE_VDD18 HCB1608KF-181T15_6 L17
C165 10U/6.3V_8 C166 1U/6.3V_4 C167 .1U/10V_4

(DPA/B_VDD18 : 1.8V@300mA+220mA) +1.8V_VGA
+1.8V_DPA_VDD18 HCB1608KF-181T15_6 L46
C636 10U/6.3V_8 C644 1U/6.3V_4 C647 .1U/10V_4

(DPC/D_VDD18 : 1.8V@300mA+220mA) +1.8V_VGA
+1.8V_DPC_VDD18 HCB1608KF-181T15_6 L11
C643 10U/6.3V_8 C635 1U/6.3V_4 C634 .1U/10V_4

[36,39,40,41,44,49] HWPG
U4 *MC74VHC1G08DFT2G
R52 4 *10K_4
R53 10K_4
PWRGOOD_BUF
+3V

For future ASIC, if PWRGOOD_BUF is not requred it should be pulled to ground.

NB5/RD2

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

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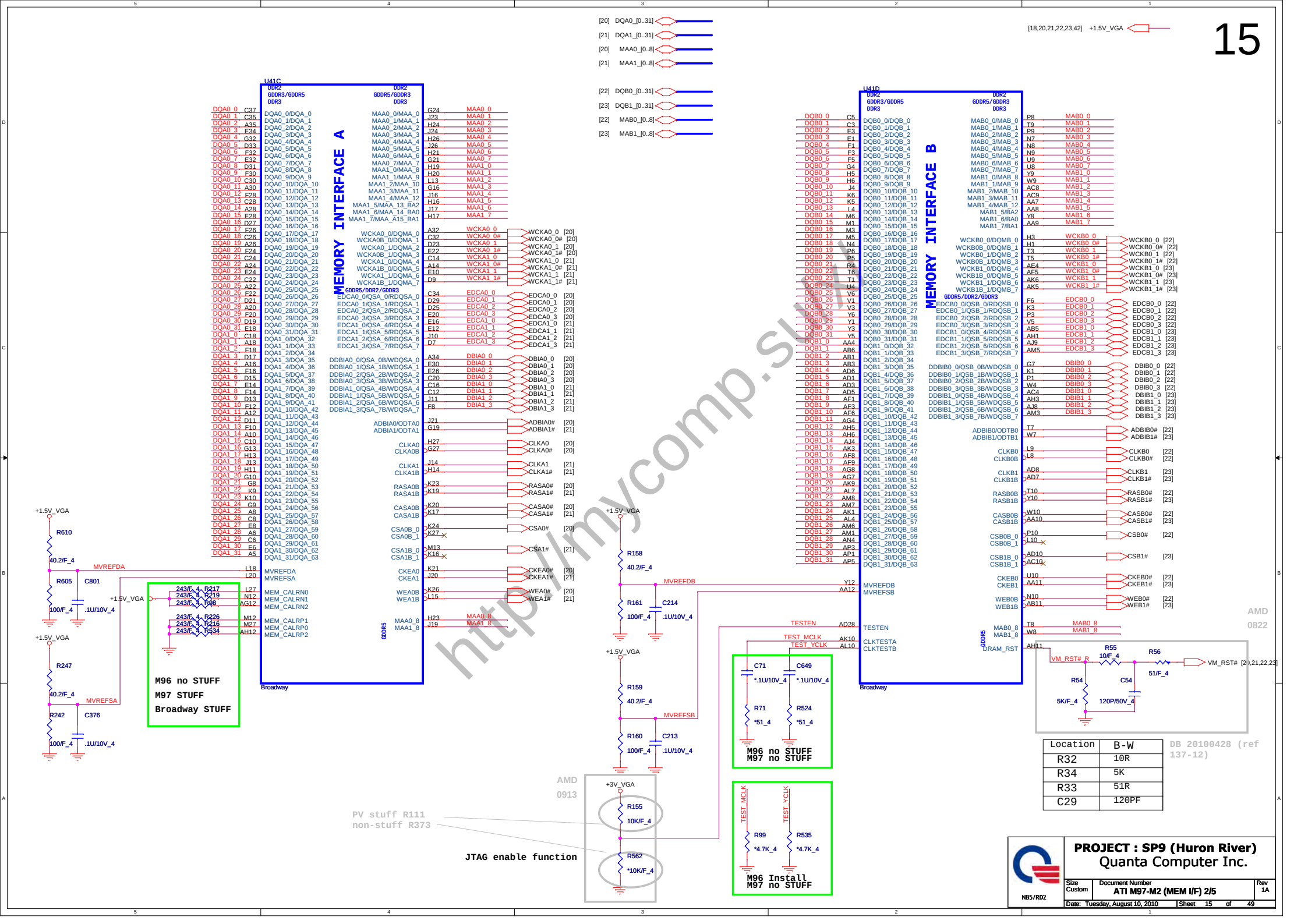

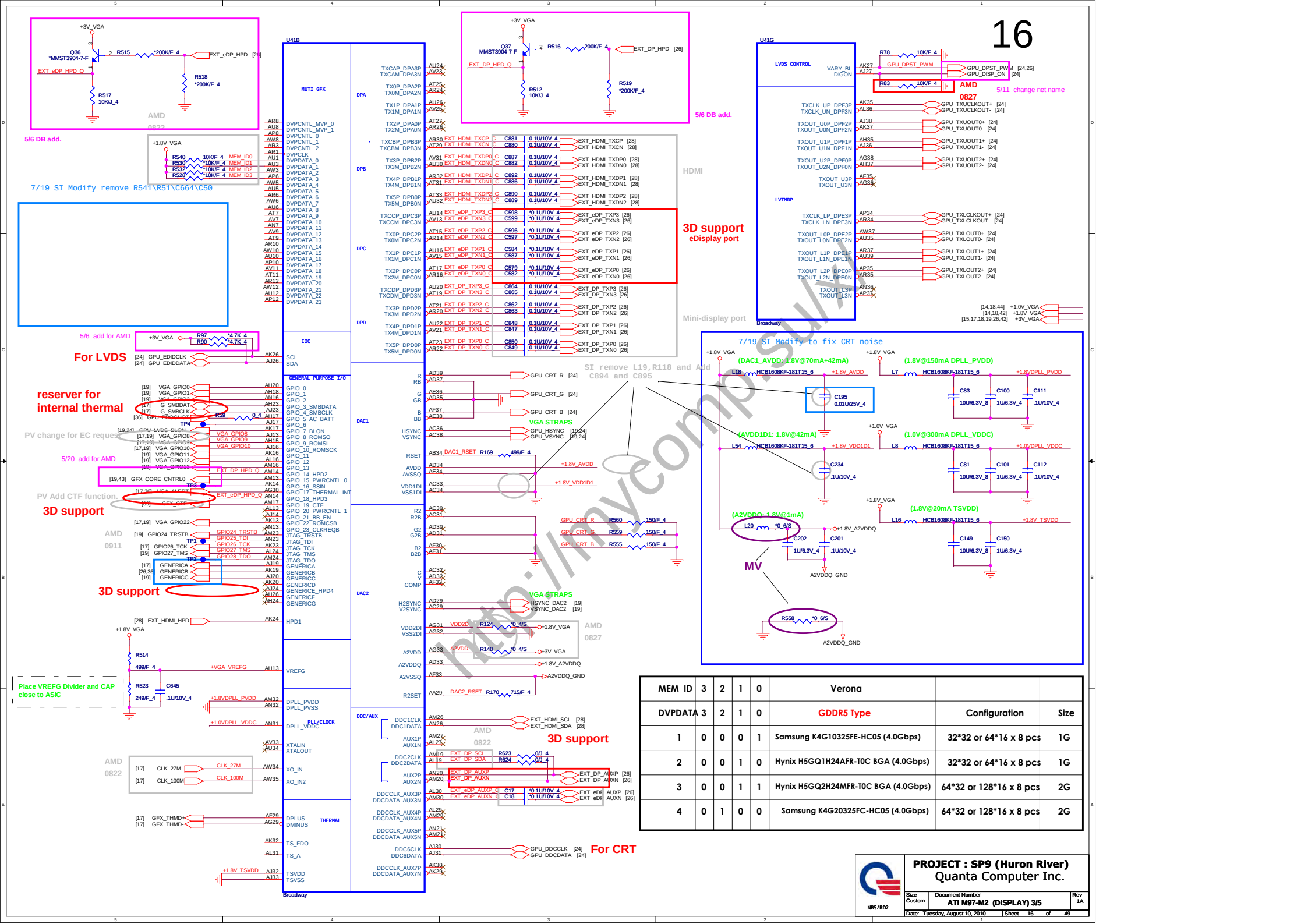

MEM ID	3	2	1	0	Verona		
DVPDATA	3	2	1	0	GDDR5 Type	Configuration	Size
1	0	0	0	1	Samsung K4G10325FE-HC05 (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ1H24AFR-T0C BGA (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1	Hynix H5GQ2H24MFR-T0C BGA (4.0Gbps)	64*32 or 128*16 x 8 pcs	2G
4	0	1	0	0	Samsung K4G20325FC-HC05 (4.0Gbps)	64*32 or 128*16 x 8 pcs	2G

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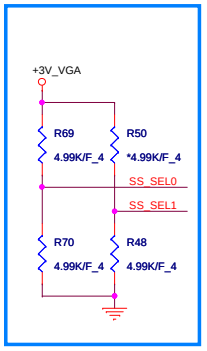
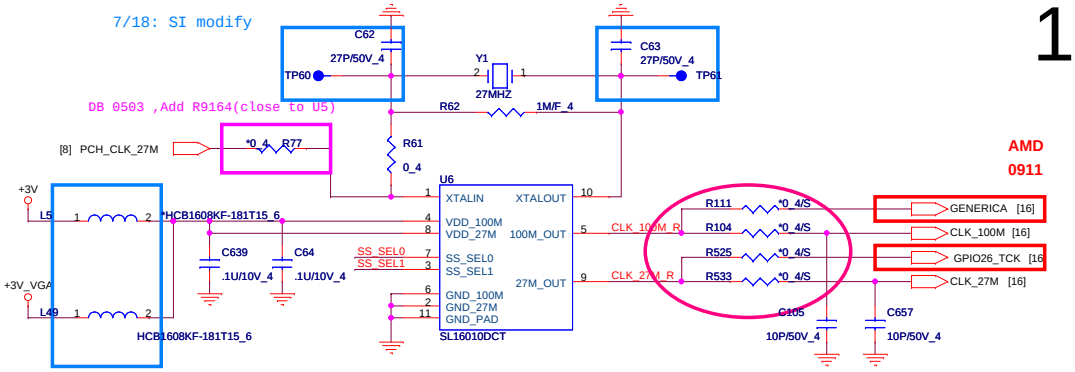
27MHz + 100Mhz OSC Option

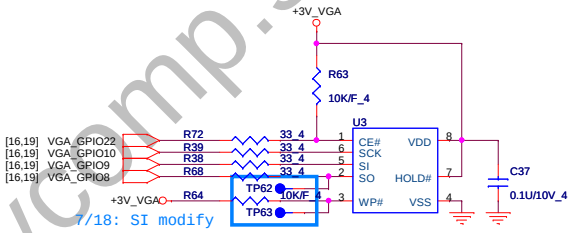


7/18: SI modify

7/18: SI modify



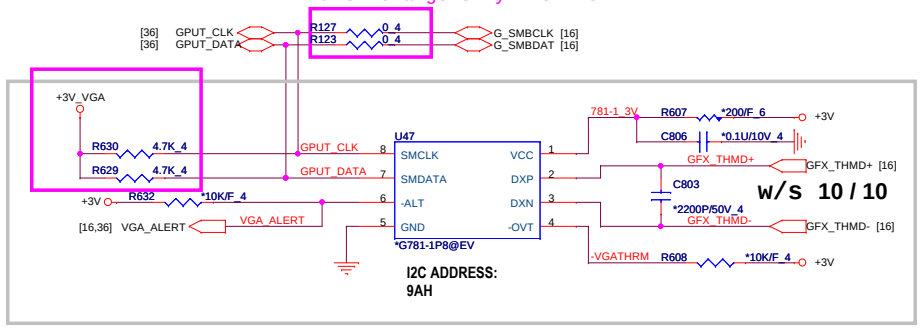
Ext EEPROM

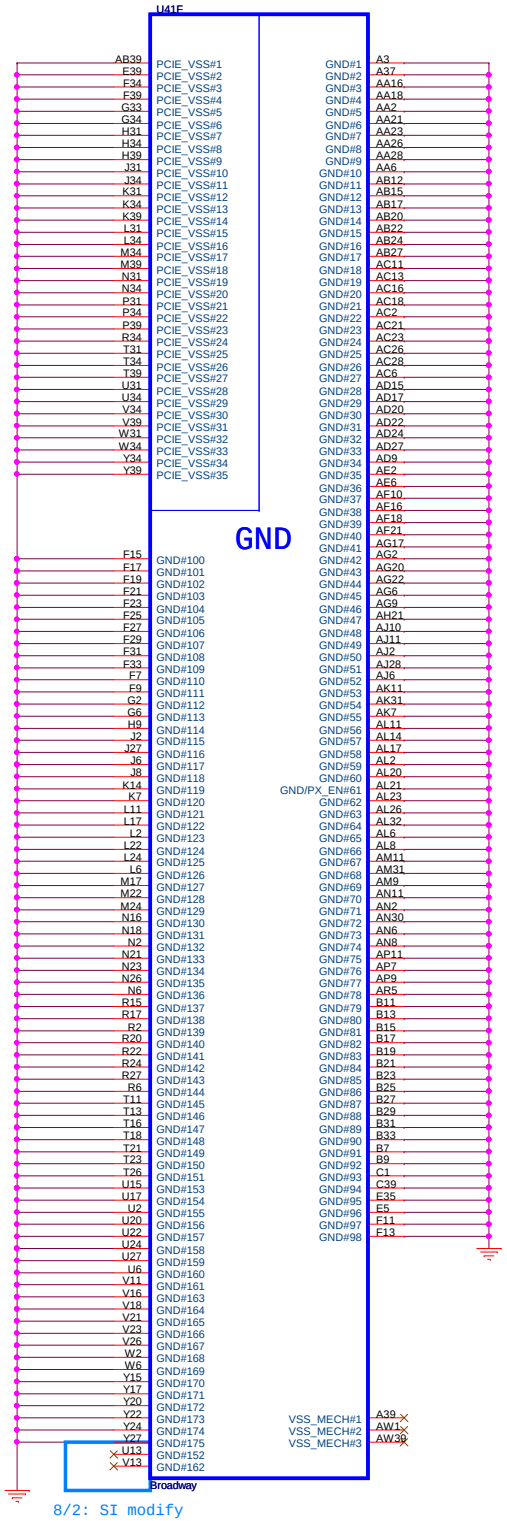


7/18: SI modify

Thermal Sensor

4/19: change only from VGA





8/2: SI modify

[2,6,7,8,9,10,12,13,14,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47] +3V

[15,16,18,19,26,42] +3V_VGA

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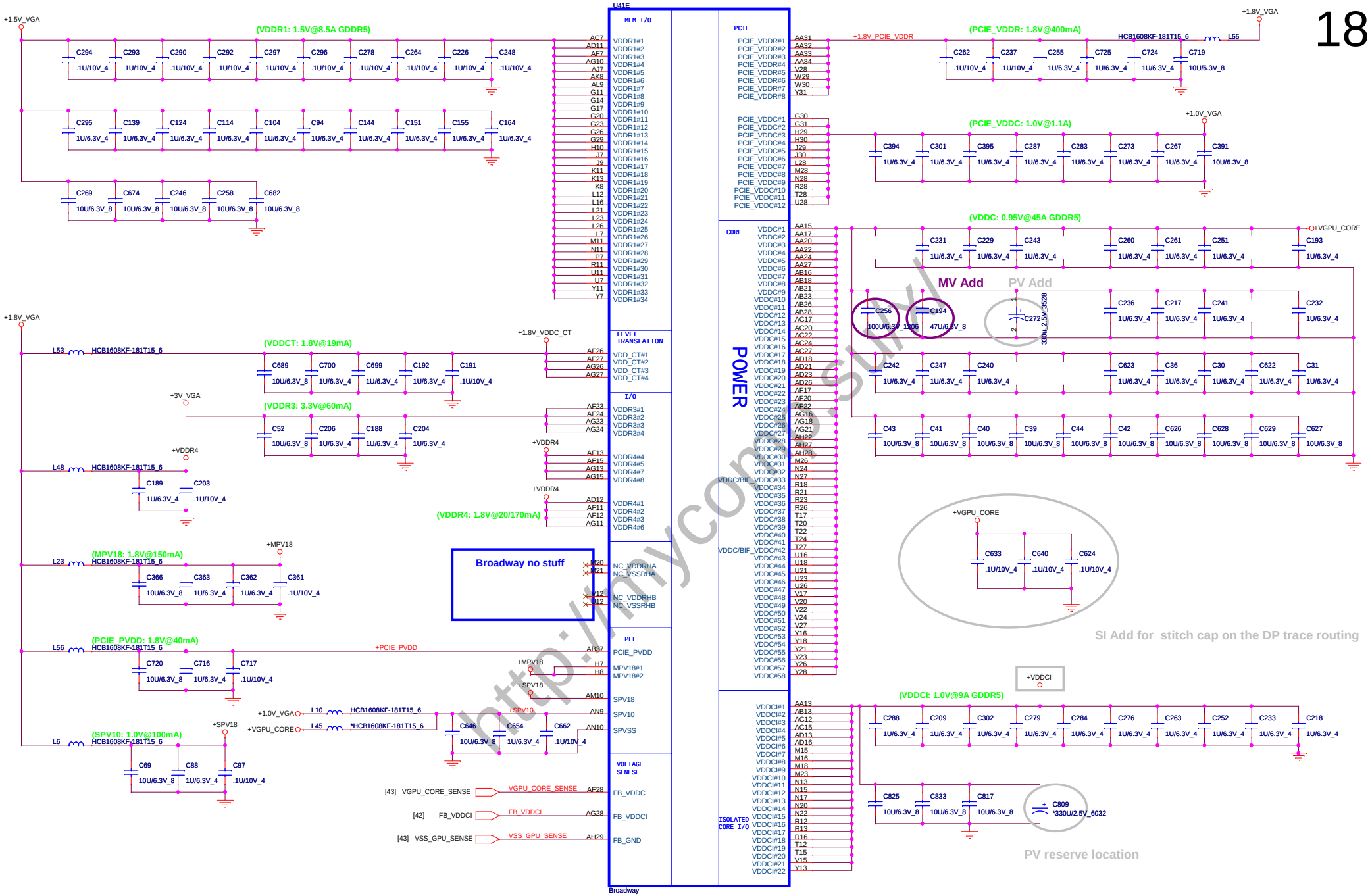
NB5/RD2



PROJECT : SP9 (Huron River)	
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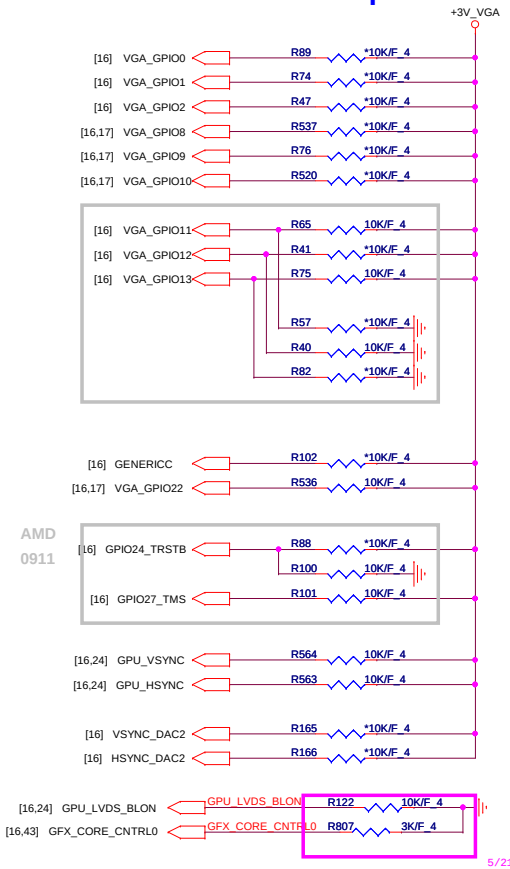
Straps



Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground High logic voltage

Signal

Table 3-34 ROM Configurations

Manufacturer	Part Number	Size	CONFIG[2:0]
Atmel	AT25F512	512 kbit	001
	AT25F512A	512 kbit	010
	AT25F1024	1 Mbit	011
	AT25F1024A	1 Mbit	011
	AT25F2048	2 Mbit	011
	AT25F4096	4 Mbit	011
ST Microelectronics	M25P05A	512 kbit	100
	M25P10A	1 Mbit	101
	M25P20	2 Mbit	101
	M25P40	4 Mbit	101
	M25P80	8 Mbit	101
Silicon Storage Technology	SST25VF512	512 kbit	010
	SST25VF010	1 Mbit	011
	SST25VF020	2 Mbit	011
	SST25VF040	4 Mbit	011
Winbond Electronics Corporation	W45B512	512 kbit	110
	W45B012	1 Mbit	111
YMC	Y25LF05	512 kbit	010
	SA25C020	2 Mbit	011
PMC	Pm25LV512	512 kbit	100
	Pm25LV010	1 Mbit	101

Default

Strap Name	Pin Straps	Description	Default Value
TX_PWRS_ENB	GPIO0	GPIO[1:0]:Recommend to pulling up for PICE setting. GPIO_0:PCIE full TX output swing	
TX_DEEMPH_EN	GPIO1	GPIO_1:PCIE Transmitter DE-EMPHASIS enabled	
BIF_GEN2_EN	GPIO2	GPIO_2:System is using PCIE GEN1 can be let it NC(ASIC internal pull down) if Gen2 just pull up for PCIE 5GT/s support. (0=PCIE GNE1,2.5GT/s ; 1=PCIE GNE2,5GT/s)	
STRAP_BIF_CLK_PM_EN	GPIO8		
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11		
BIOS_ROM_EN	GPIO22	BIOS_ROM_EN(GPIO22)=1, then Config[2:0]=GPIO[13:12:11] defines the ROM type. (See table as below)	
AUDIO[0]	VSYNC		
AUD(1)	HSYNC		
VSYNC_DAC2	V2SYNC		
HSYNC_DAC2	H2SYNC		
	GENERICC		

1GB GDDR5 : CHANNEL A-0 (64M x 16)

[15] DQA0_[31..0]
[15] MAA0_[8..0]

U48

MF=1 Mirror

U19

170-BALL SDRAM GDDR5

K4G52324FG

Change 1u to 2.2,for ATI Request 1212

[15,18,21,22,23,42] +1.5V_VGA

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1GB GDDR5 : CHANNEL A-1 (64M x 16)

MF=1 Mirror

for DB2

U49 — 170-BALL SDRAM GDDR5 — K4G52324FG

U20 — 170-BALL SDRAM GDDR5 — K4G52324FG

Change 1u to 2.2,for ATI Request 1212

PROJECT : SP9 (Huron River) Quanta Computer Inc.		
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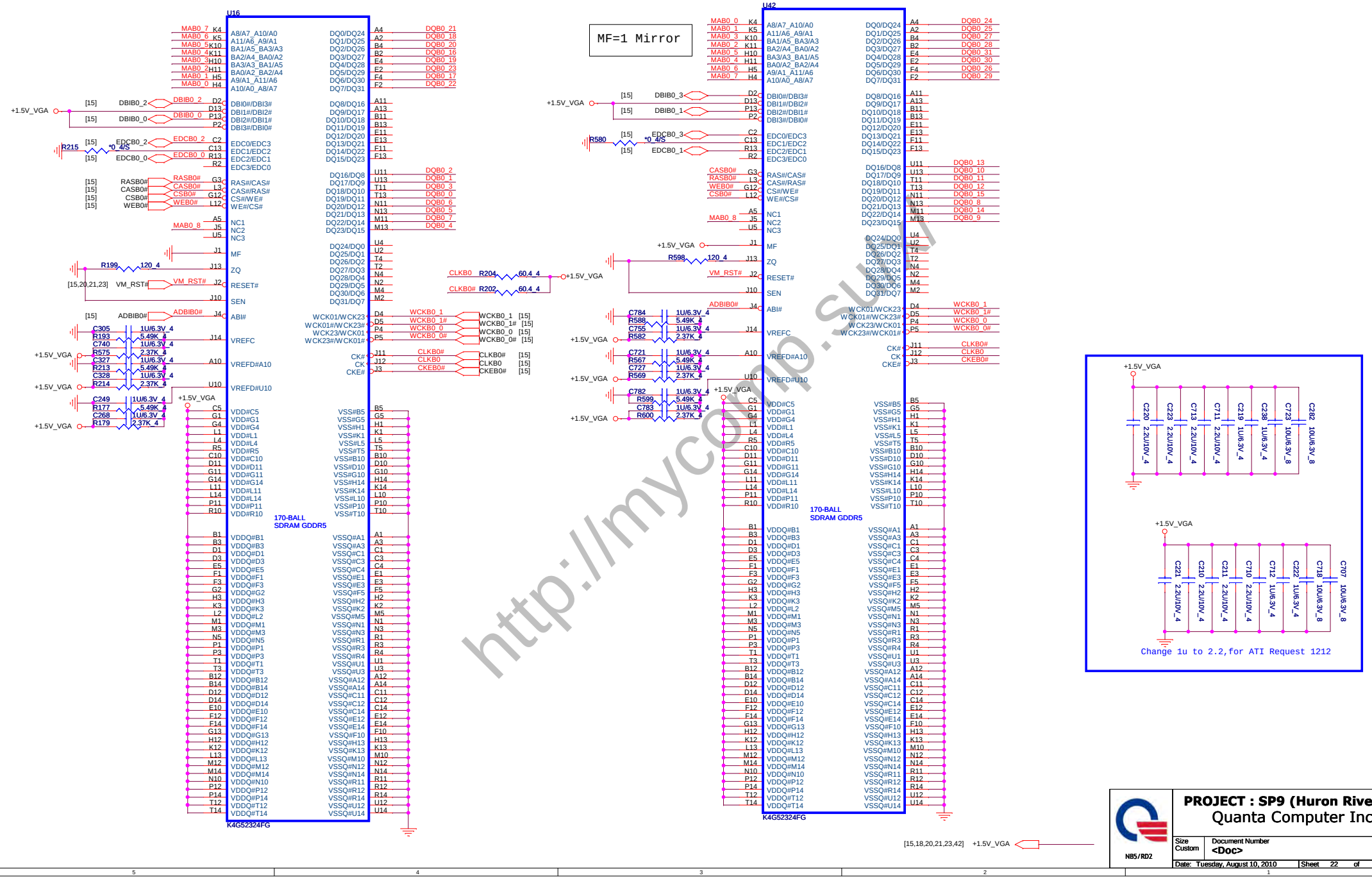
1GB GDDR5 : CHANNEL B-0 (64M x 16)



NB5/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.		
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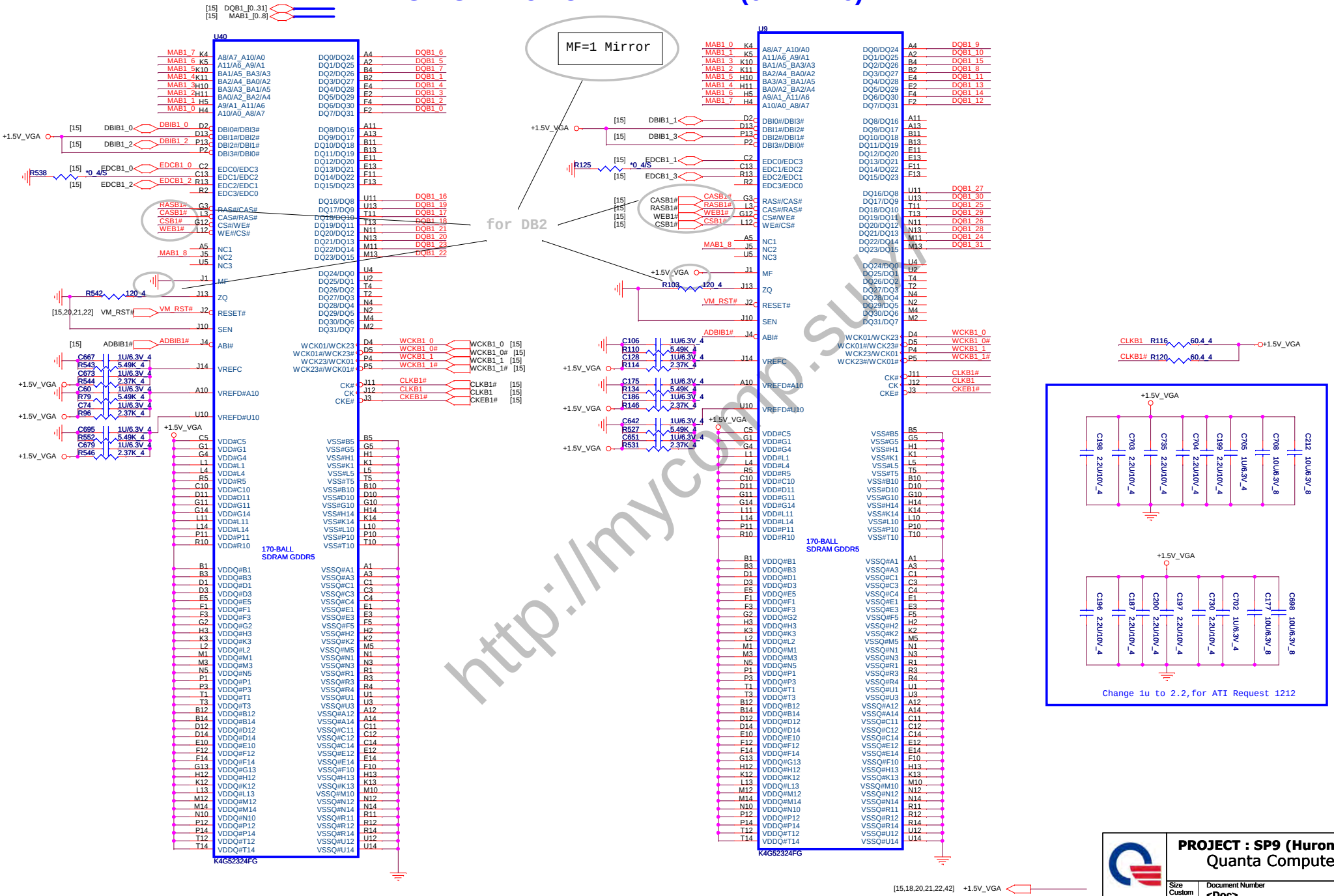
1GB GDDR5 : CHANNEL B-1 (64M x 16)

MF=1 Mirror



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Quanta Computer Inc.	
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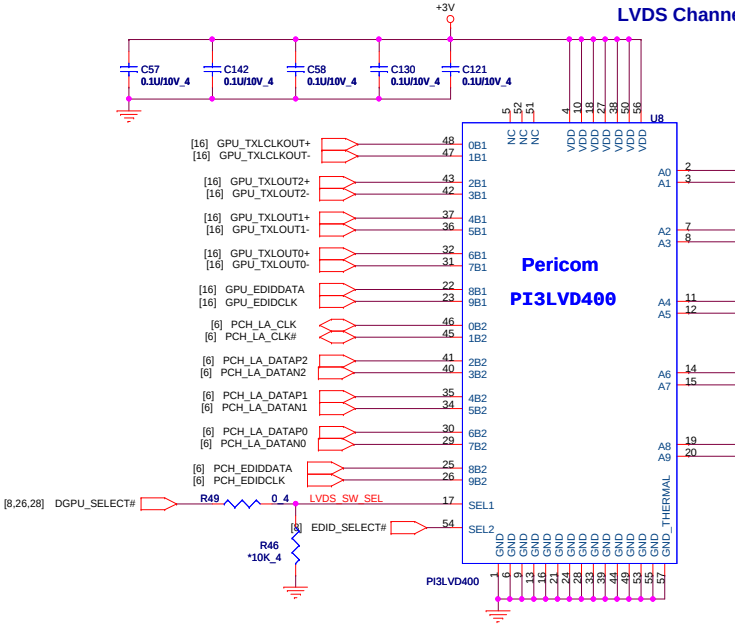
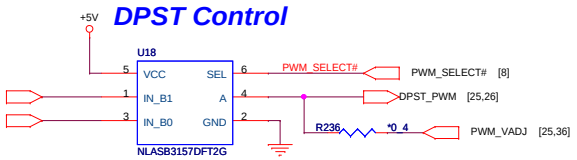
LVDS Channel Switch

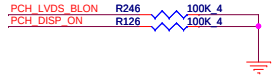


SEL	FUNCTION
LOW	DGPU (AN to B1)
HIGH	IGPU (AN to B2)

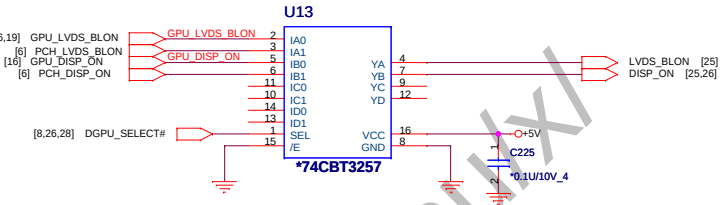
DPST Control



SEL	FUNCTION(COM)
LOW	IN_B0 to A
HIGH	IN_B1 to A

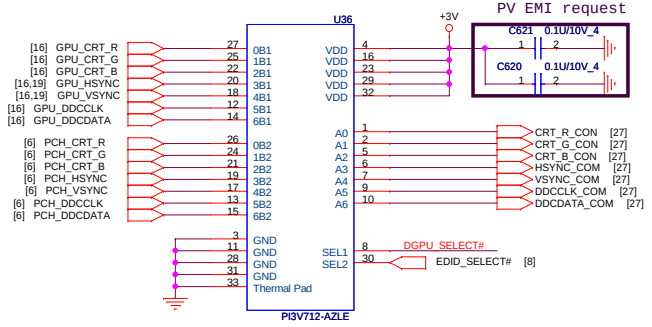


LCD BLON/ DISP control

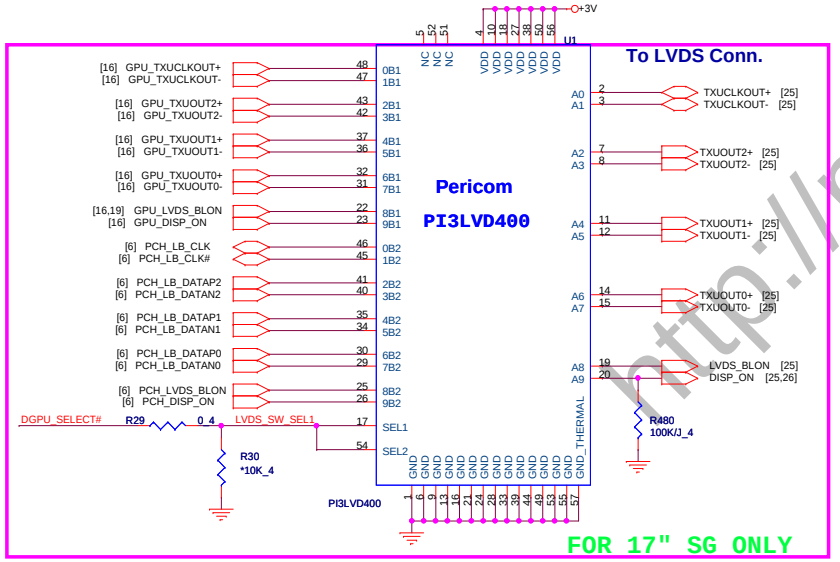


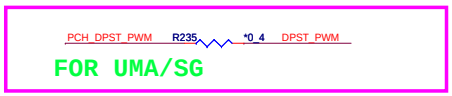
SEL	FUNCTION(COM)
LOW	IN_B1 to A
HIGH	IN_B2 to A

VGA SWITCH



SEL	FUNCTION(COM)
LOW	nB1 to An
HIGH	nB2 to An





+3V [2,6,7,8,9,10,12,13,14,17,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
+5V [6,7,10,25,26,27,28,29,31,32,33,35,37,45,49]
+1.8V [4,7,10,41,42]

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

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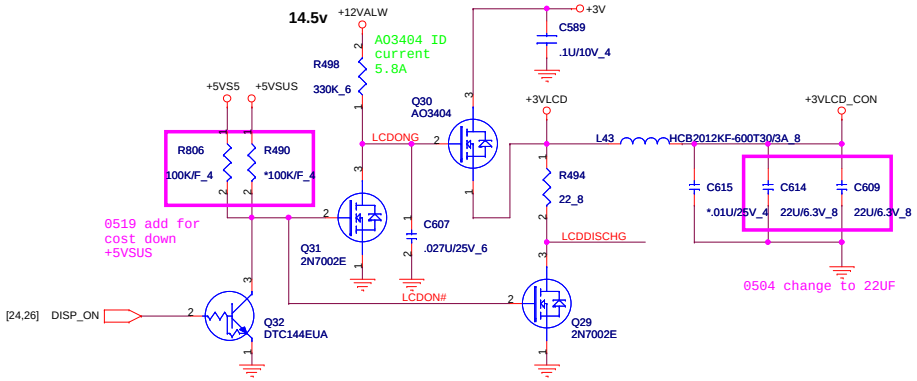
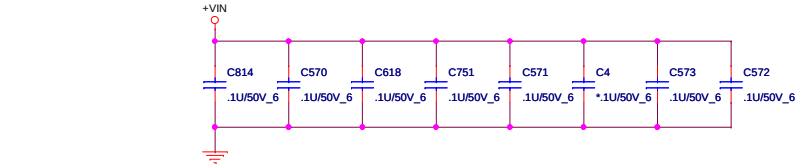
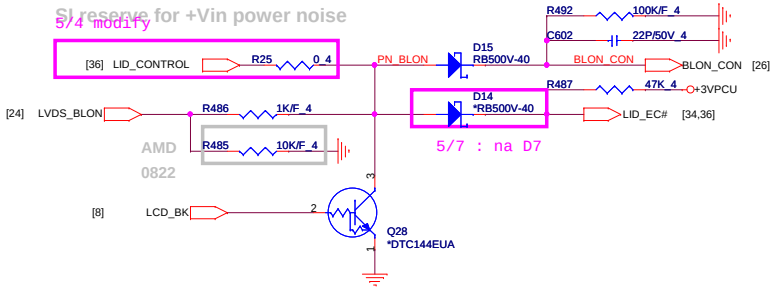
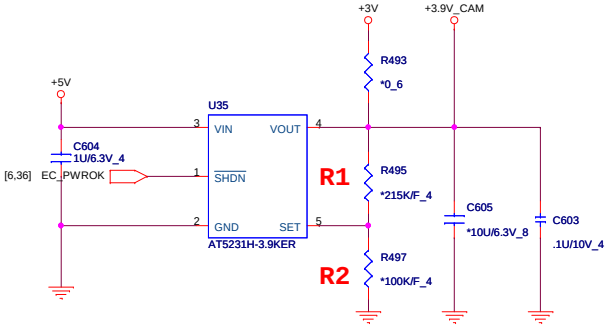
NB5/RD2

LCD

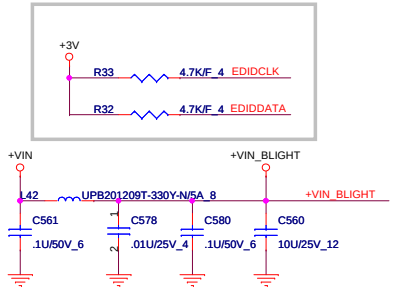


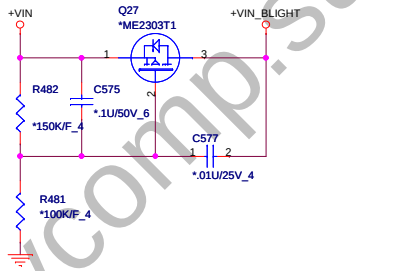




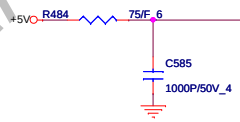


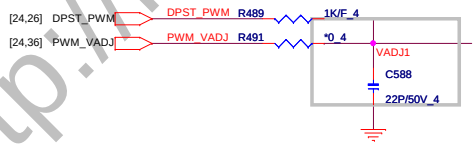
Vout=1.25(1+R1/R2)

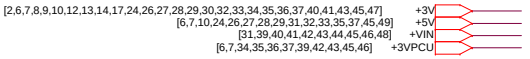


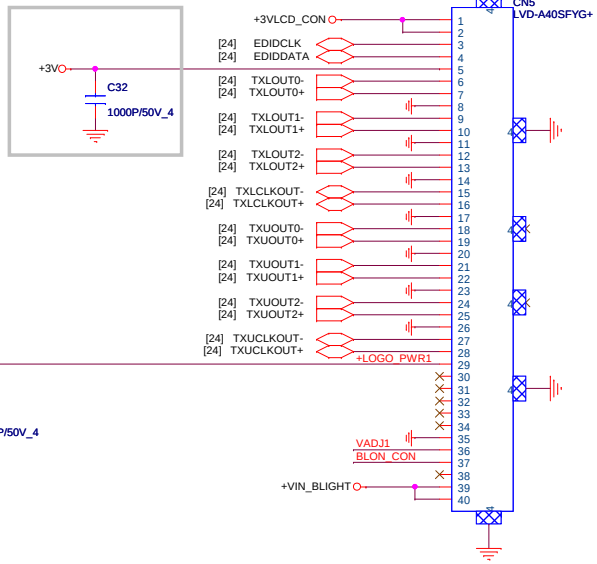


SI reserve for LCD soft start circuit

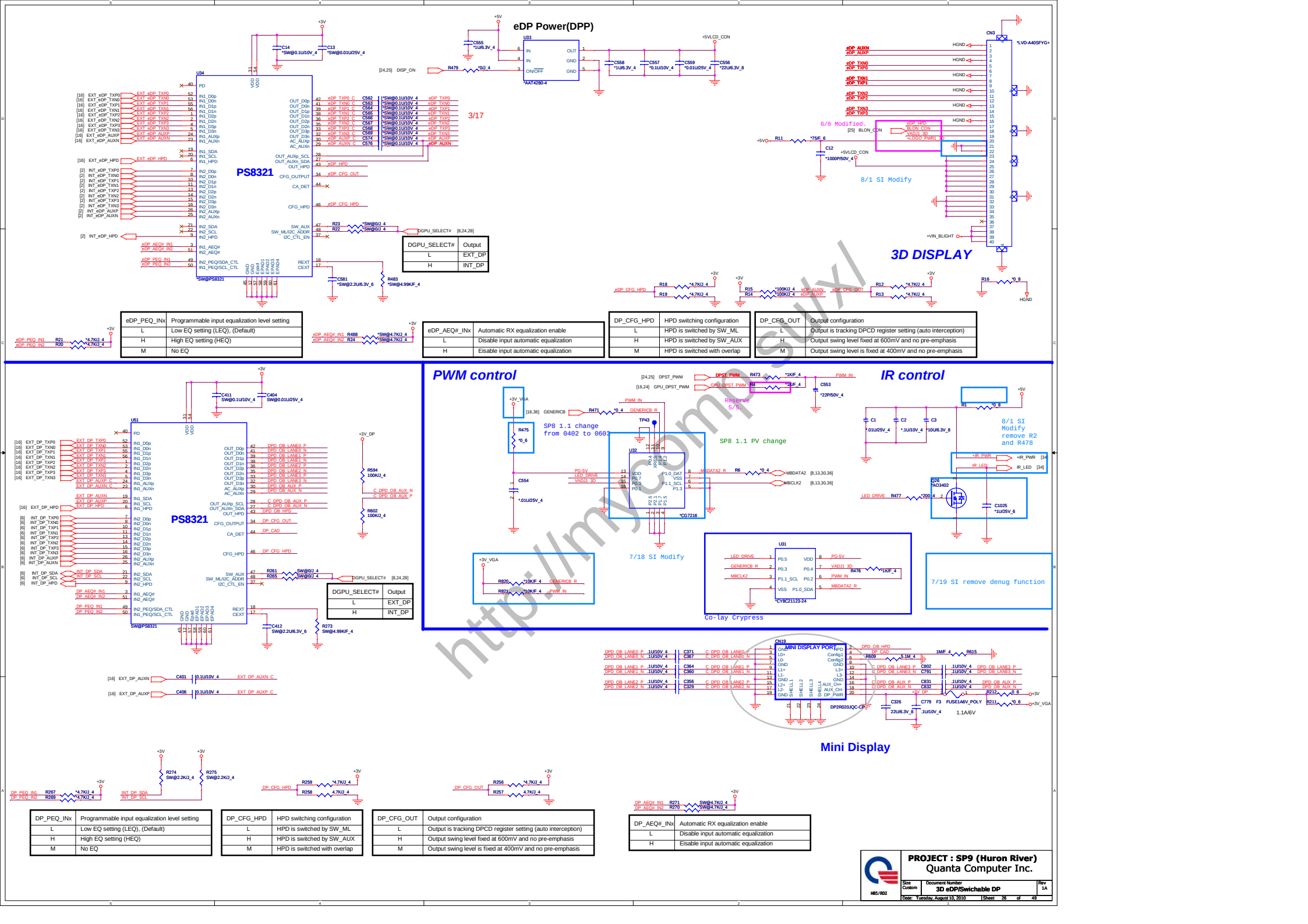








N85/RD2	**PROJECT : SP9 (Huron River)** Quanta Computer Inc.	
	Size: Custom — Document Number: **LCD CONN/LID function**	Rev: 1A
	Date: Tuesday, August 10, 2010	Sheet 25 of 49



eDP_PEQ_INx	Programmable input equalization level setting
L	Low EQ setting (LEQ), (Default)
H	High EQ setting (HEQ)
M	No EQ

eDP_AEQ#_INx	Automatic RX equalization enable
L	Disable input automatic equalization
H	Eisable input automatic equalization

DP_CFG_HPD	HPD switching configuration
L	HPD is switched by SW_ML
H	HPD is switched by SW_AUX
M	HPD is switched with overlap

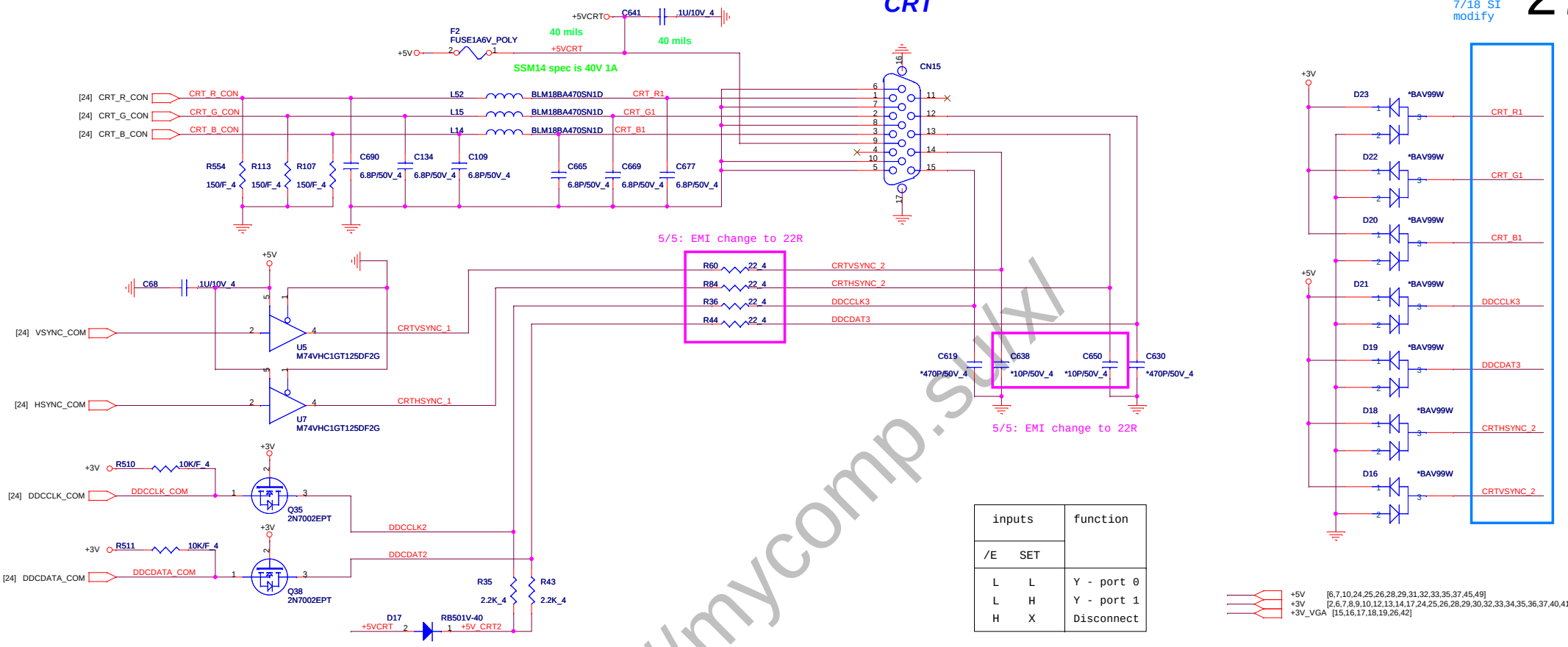
DP_CFG_OUT	Output configuration
L	Output is tracking DPCD register setting (auto interception)
H	Output swing level fixed at 600mV and no pre-emphasis
M	Output swing level is fixed at 400mV and no pre-emphasis

DGPU_SELECT#	Output
L	EXT_DP
H	INT_DP

PROJECT : SP9 (Huron River)
Quanta Computer Inc.
Size: Custom | Document Number: 3D eDP/Swichable DP | Rev: 1A
Date: Tuesday, August 10, 2010 | Sheet 26 of 49
NB5/RD2

CRT

7/18 SI modify

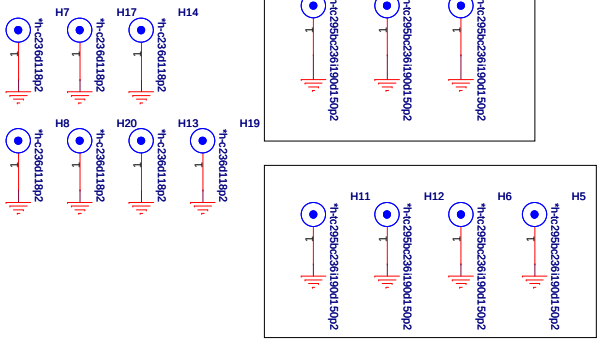


inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

+5V [6,7,10,24,25,26,28,29,31,32,33,35,37,45,49]
+3V [2,6,7,8,9,10,12,13,14,17,24,25,26,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
+3V_VGA [15,16,17,18,19,26,42]

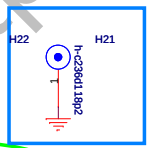
HOLDs

for GPU



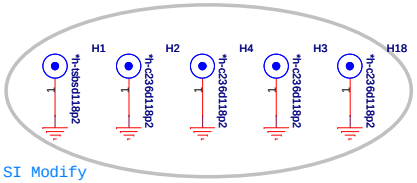
for CPU

SI ME change Footprint

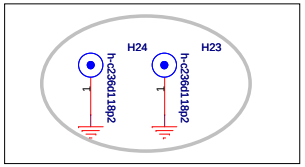


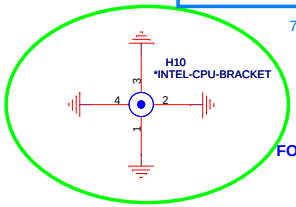
7/18 SI Modify

SI for ME change footprint



SI add for PCH hole

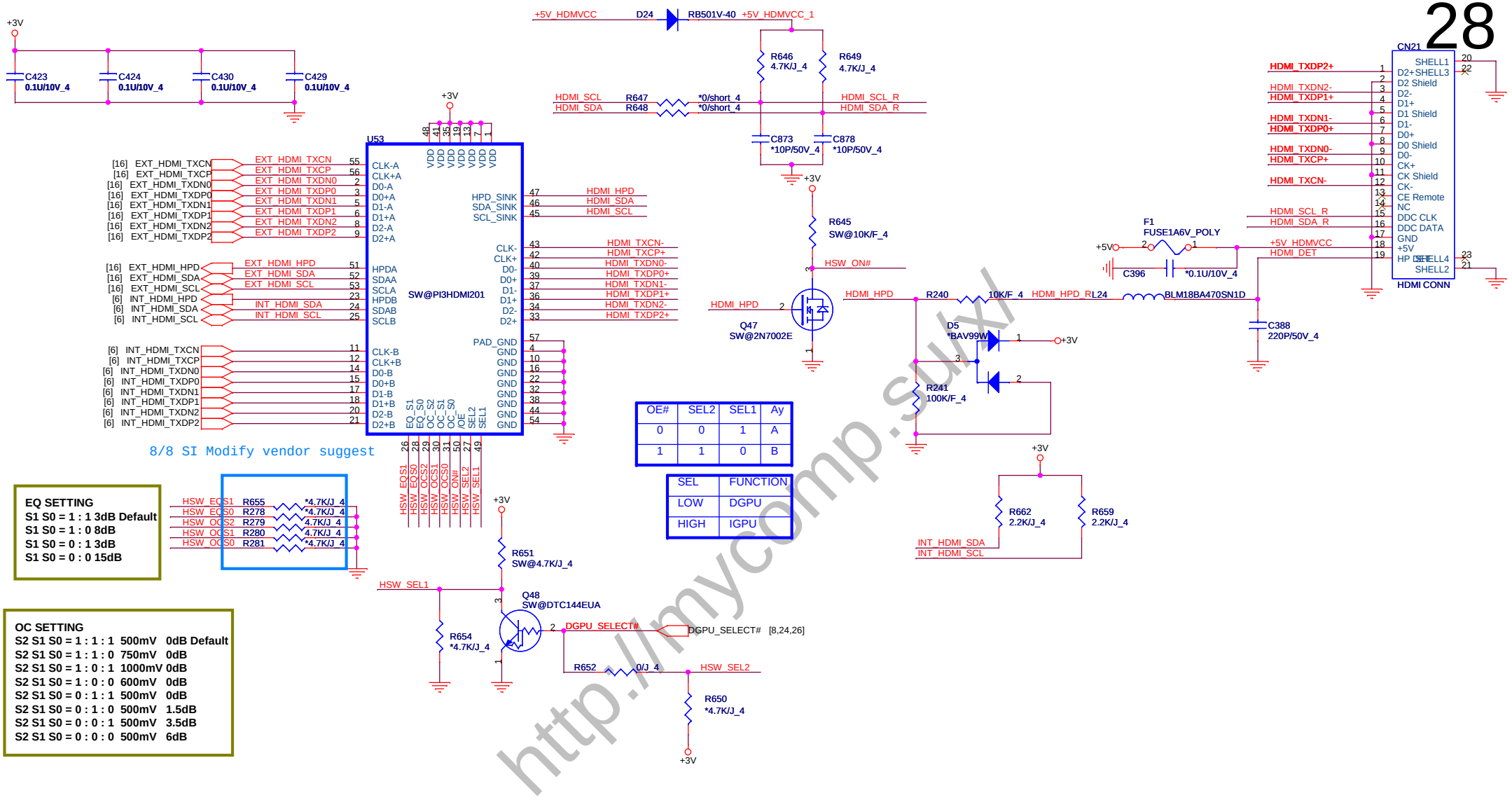




FOR LAYOUT

Modify H5\H6,H11\H12\H13\H16\H17,H15 at 0506

NB5/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.	
Size Custom	Document Number CRT/HDMI Conn	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 27 of 49	



OE#	SEL2	SEL1	Ay
0	0	1	A
1	1	0	B

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

EQ SETTING
S1 S0 = 1 : 1 3dB Default
S1 S0 = 1 : 0 8dB
S1 S0 = 0 : 1 3dB
S1 S0 = 0 : 0 15dB

OC SETTING

S2 S1 S0 = 1 : 1 : 1	500mV	0dB Default
S2 S1 S0 = 1 : 1 : 0	750mV	0dB
S2 S1 S0 = 1 : 0 : 1	1000mV	0dB
S2 S1 S0 = 1 : 0 : 0	600mV	0dB
S2 S1 S0 = 0 : 1 : 1	500mV	0dB
S2 S1 S0 = 0 : 1 : 0	500mV	1.5dB
S2 S1 S0 = 0 : 0 : 1	500mV	3.5dB
S2 S1 S0 = 0 : 0 : 0	500mV	6dB

NB5/RD2

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SG HDMI Conn	1A
Date: Tuesday, August 10, 2010	Sheet 28 of 49	

[2,6,7,8,9,10,12,13,14,17,24,25,26,27,28,30,32,33,34,35,36,37,40,41,43,45,47] +3V
[30,31] +5V_AVDD
[6,7,10,24,25,26,27,28,31,32,33,35,37,45,49] +5V

Close to CODEC

SI change footprint from 0603 to 0805 for IDT comfirm

Close to CODEC

+5V_AVDD
+5V
L41 *BLM18PG181SN1D(180,1.5A)_6
C546 10U/6.3V_6S
C545 1U/6.3V_4
C1011 1U/10V_4
C542 1U/6.3V_4
C538 1U/10V_4
C543 10U/6.3V_6S
AGND

PV non-Stuff

+3V
C535 1U/6.3V_4
C533 1U/10V_4
C531 .1U/10V_4
+3V_DVDD_CORE
C524 10U/6.3V_6S

U30

>40mils
>40mils

[HDA Bus]
[7] BIT_CLK_AUDIO R448 *0_4/S HD_BCLK
[7] ACZ_SDIN0 R449 33_4 HD_SDIN0
[7] ACZ_SDOUT_AUDIO R447 *0_4/S HD_SDOUT
C526 10P/50V_4
[7] ACZ_SYNC_AUDIO R450 *0_4/S HD_SYNC
C532 10P/50V_4
[7] ACZ_RST#_AUDIO

DVDD_CORE DVDD DVDD_IO HDA_BITCLK HDA_SDI HDA_SDO HDA_SYNC HDA_RST#
AVDD AVDD PVDD PVDD SENSE_A SENSE_B
SENSE_A SENSE_B SENSE_A [30]

[Digital MIC]
[34] DIGITAL_CLK
[34] DIGITAL_D1
C518 10P/50V_4 R445 100/F_4 DMIC_CLK_R
C534 10P/50V_4 DMIC0
IDT_GPIO0

DMIC_CLK/GPIO1 DMIC0/GPIO2 DMIC1/GPIO0/SPDIF_OUT_1

HP0_PORT_A_L HP0_PORT_A_R VREFOUT_A_or_F
MIC_L C551 2.2U/25V_8
MIC_R C1015 2.2U/25V_8
VREFOUT_A
EXT_MIC [30]
VREFOUT_A [30]

[Combo MIC]

HP1_PORT_B_L HP1_PORT_B_R
HPOUT_L HPOUT_R
HPOUT_L [30]
HPOUT_R [30]

[Combo HP & Salve HP]

PORT_C_L PORT_C_R VREFOUT_C

SPKR_PORT_D_L+ SPKR_PORT_D_L-
L_SPK+ L_SPK-

[Internal Speaker]

SPKR_PORT_D_R- SPKR_PORT_D_R+
R_SPK- R_SPK+

PORT_E_L PORT_E_R PORT_F_L PORT_F_R PC_BEEP MONO_OUT CAP2 VREFFILT V- VREG

0901
[36] VOLMUTE#
+3V R453 10K/F_4
D12 RB500V-40
[31] ADC_EAPD#
ADC_EAPD#
SPDIF_OUT_0
EAPD

Close to CODEC

CAP-
C549 4.7U/6.3V_6
CAP+
DVSS
AVSS AVSS AVSS
PVSS
DAP
AGND

92HD80Bx

AMP_BEEP C992 .1U/10V_4 AMP_BEEP_L R790 47K_4 AMP_BEEP_R2 C988 .1U/10V_4
BASS_OUT BASS_OUT [31]
ADC_CAP2
ADC_VREFFILT
ADC_V-
ADC_VREG
R793 10K/F_4
C998 .1U/10V_4

PV Change from +5V to +5V_ADD

+5V_AVDD
6/17
R797 10K/F_4
2N7002E Q58
SPKR [7]
AGND

SENSE_A R456 2.49K/F_4 +5V_AVDD
C539 1000P/50V_4 AGND
SENSE_B R459 100K/F_4 +5V_AVDD
C540 *1000P/50V_4 AGND

BIT_CLK_AUDIO ACZ_SDIN0
C520 *27P/50V_4
C521 27P/50V_4
FOR EMI

C548 4.7U/6.3V_6
C550 10U/6.3V_6S
C541 10U/6.3V_6S
C544 1U/6.3V_4
Close to CODEC

INT. SPEAKER

L_SPK+ L40 BK1608LL121_6 L_SPK+_R
L_SPK- L38 BK1608LL121_6 L_SPK-_R
R_SPK- L37 BK1608LL121_6 R_SPK-_R
R_SPK+ L35 BK1608LL121_6 R_SPK+_R
CN10 INT SPEAKER CONN
C990 1000P/50V_4
C994 1000P/50V_4
C996 1000P/50V_4
C1003 1000P/50V_4
AGND

MUTE_LED

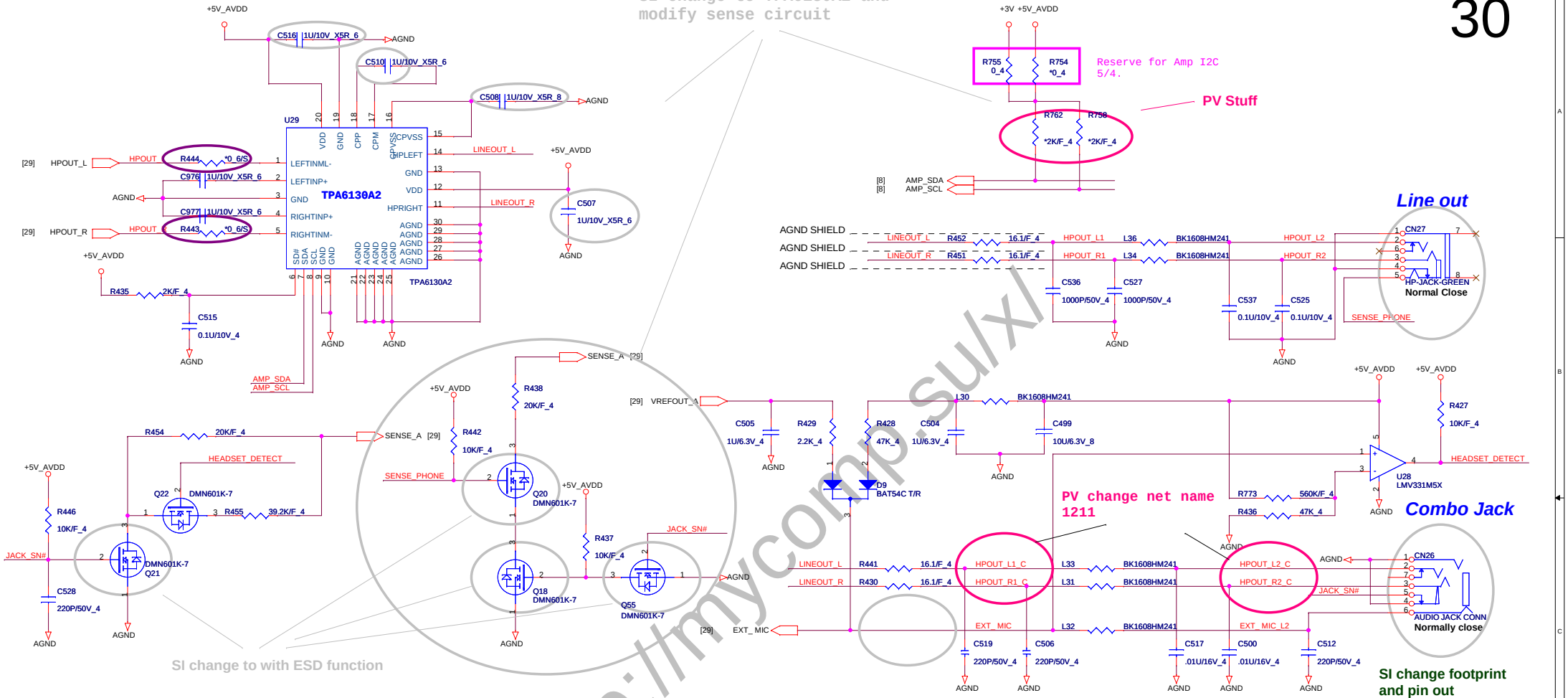
Low -->MUTE
High-->un-Mute
+3V
R462 *100K/F_4
[35] MUTE_LED#
+3V R458 10K/F_4
VOLMUTE#
IDT_GPIO0
D13 BAT54A
MUTE_LED_R
Q23 2N7002E

C948 *1000P/50V_4
C547 *1000P/50V_4
C501 *.1U/10V_4
C993 *.1U/10V_4
C960 *10P/50V_4
C972 *10P/50V_4
C509 *1000P/50V_4
C1013 *1000P/50V_4
C966 *.1U/10V_4
C511 *.1U/10V_4
C975 *10P/50V_4
C503 *10P/50V_4
AGND

R759 *0_6/S
R795 *0_6/S
R789 *0_6/S
AGND

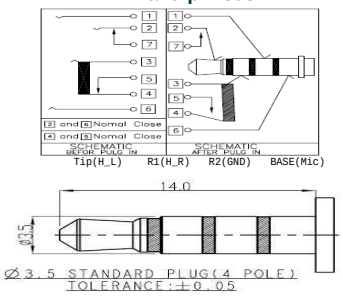
PROJECT : SP9 (Huron River) Quanta Computer Inc.		
Size: Custom	Document Number: Azalia 92HD80	Rev: 1A
N85/RD2	Date: Tuesday, August 10, 2010	Sheet 29 of 49

SI change to TPA6130A2 and modify sense circuit

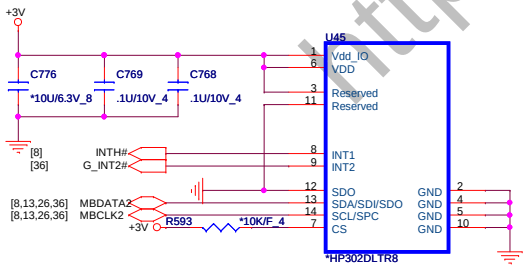


SI change to with ESD function

SI change footprint and pin out



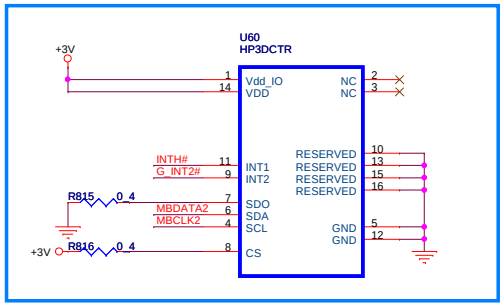
Accelerometer Sensor



Pin 12: Low 38hex

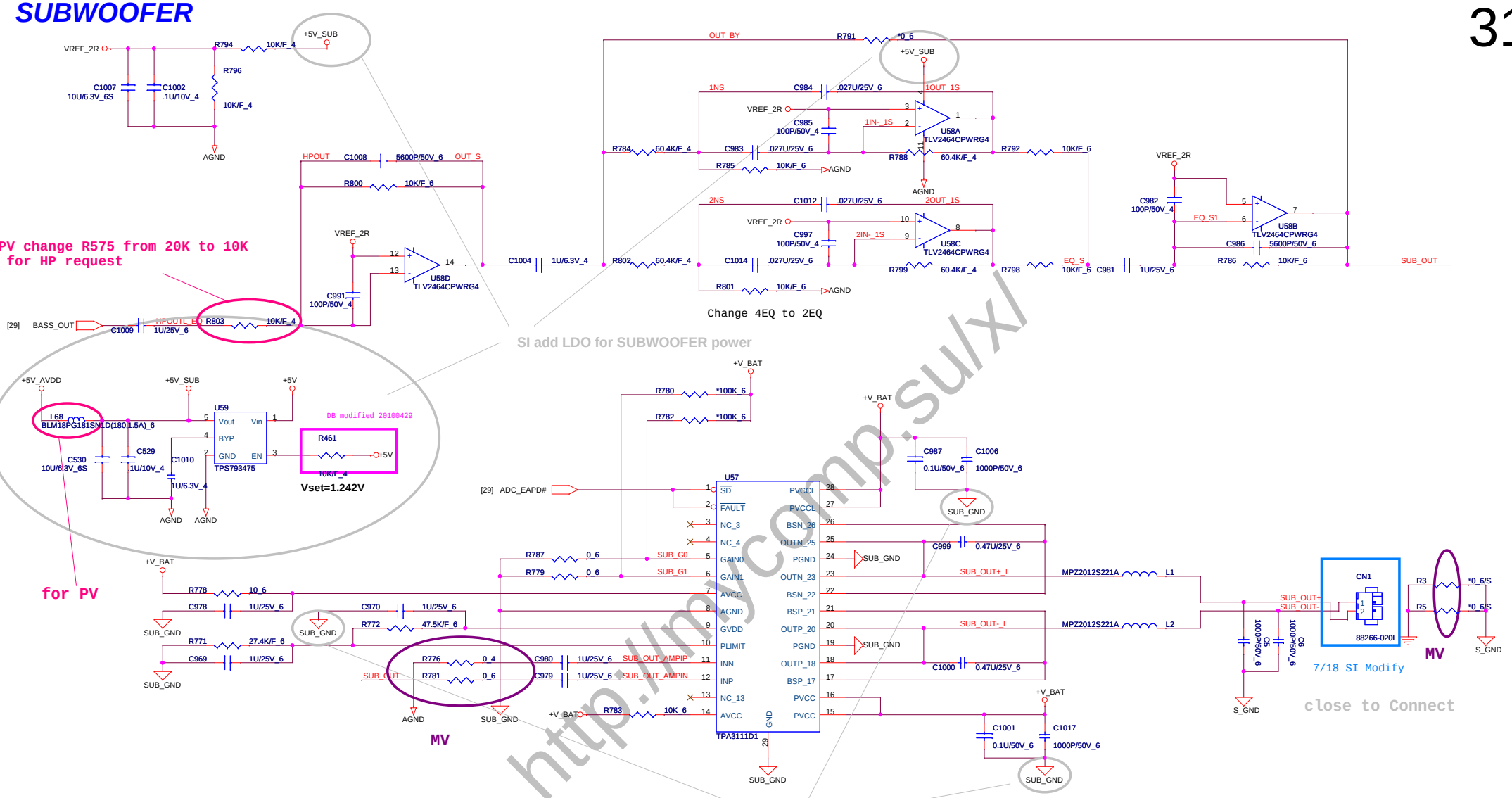
Pin 12: unconnected/floating 3Ahex

7/18: SI Add



NB5/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.	
	Size: Custom; Document Number: AMP_TPA6047/Accelerometer	Rev: 1A
	Date: Tuesday, August 10, 2010	Sheet 30 of 49

SUBWOOFER



GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36

+3V [2,6,7,8,9,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
+5V_AVDD [29,30]
+VIN [25,39,40,41,42,43,44,45,46,48]

	PROJECT : SP9 (Huron River)
	Quanta Computer Inc.
N85/RD2	Size: Custom; Document Number: SUBWOOFER (EQ & AMP.); Rev: 1A
	Date: Tuesday, August 10, 2010; Sheet 31 of 49

4/19 change FB to small size

7/27 SI Modify

Close to U14 pin 34,35

5/9 modify

GND VIA x 9 Pcs

AL08111DB00 RTL8111E-VB-GR

U21 RTL8111E-VB-GR

U50 NS892405

NS892402:GIGABIT DB0AT9LAN05

>60mil >60mil

Power trace Layout 寬度> 60mil

L23
RTL8111E (Giga lan) use 4.7uH
power choke A>600mA tolerance ±15%

Close to U14 pin 21

5/4 modify

RJ45

White is Link,Amber is active

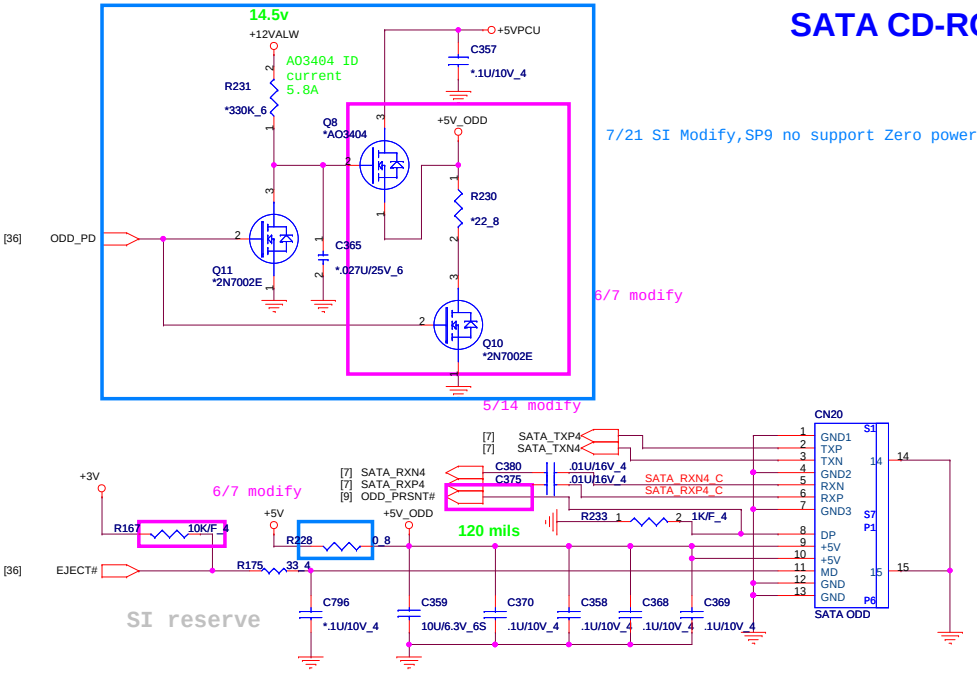
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	8111E/RJ45	1A

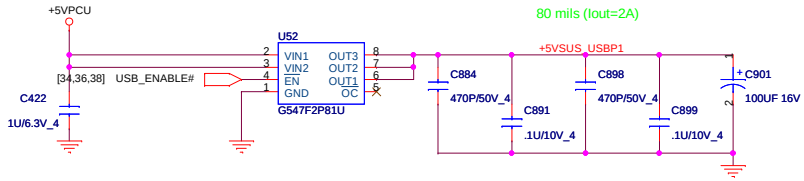
Date: Tuesday, August 10, 2010 Sheet 32 of 49

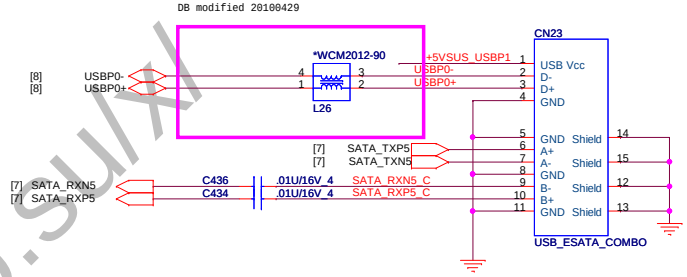
N85/RD2

SATA CD-ROM

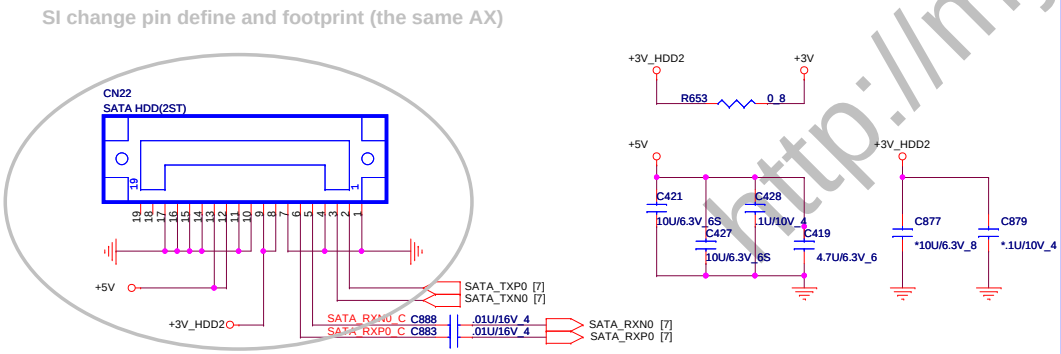


E-SATA

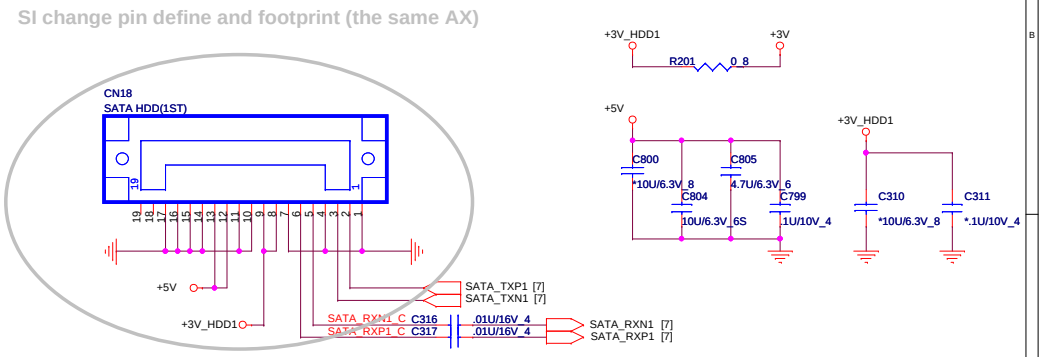




SATA HDD #1

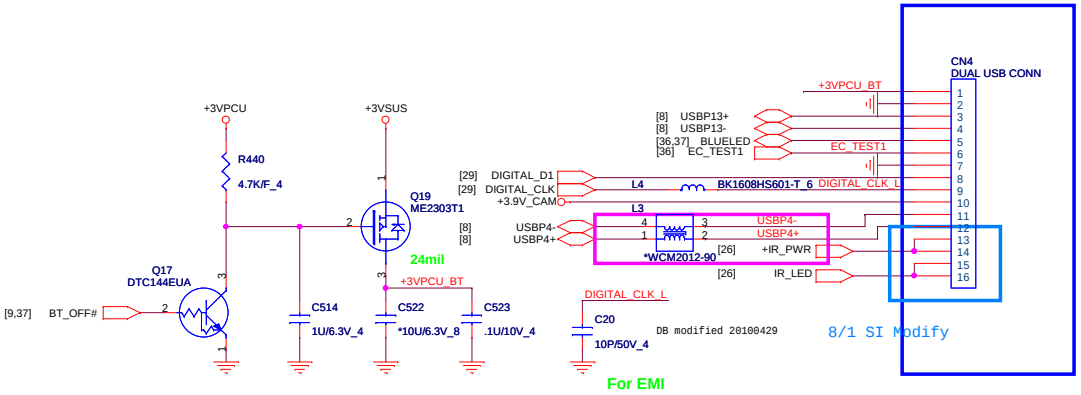


SATA HDD #2

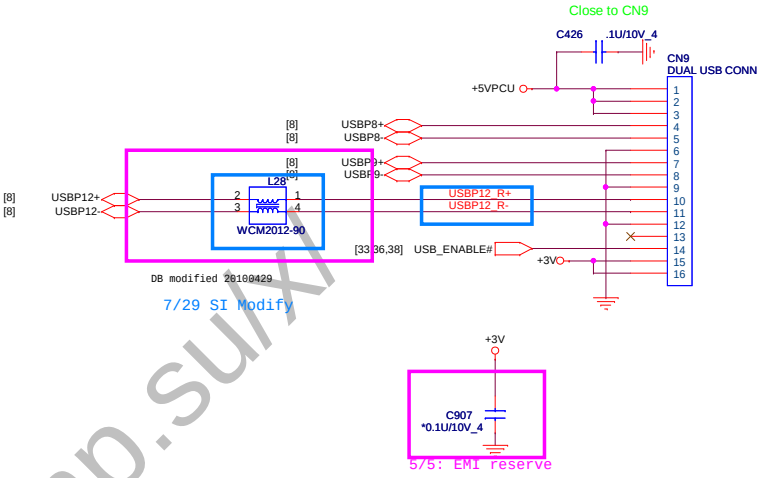


N85/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.	
	Size: Custom Document Number: ODD/HDD/ONFI	Rev: 1A
	Date: Tuesday, August 10, 2010	Sheet 33 of 49

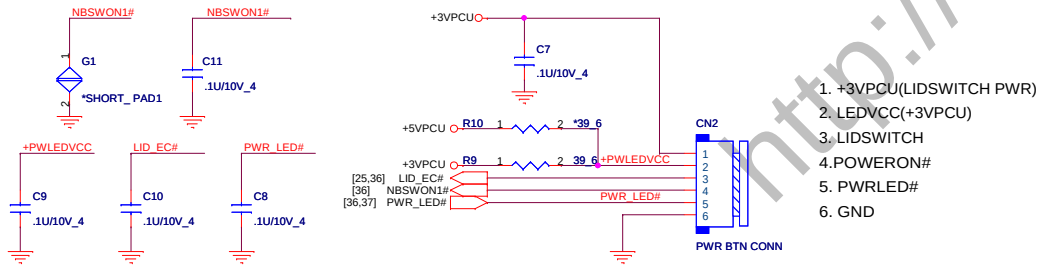
Bluetooth



Ext USB & Card Reader

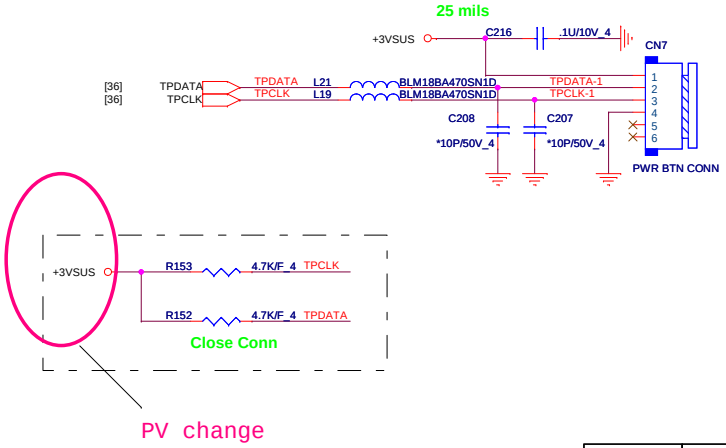


Power Botton



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

Touch Pad Botton



NB5/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.	
Size: Custom	Document Number: BT/WC/FT/Touchscreen	Rev: 1A
Date: Tuesday, August 10, 2010	Sheet 34 of 49	

Mini Display

[36] MY[0..17] MY[0..17]
[36] MX[0..7] MX[0..7]

8/5 SI modify

RP7
MY2 MY4 MY15 MY1 MY3 MY5 MY6 MY0
+3VPCU
*10P8R-8.2K

RP6
MY12 MY13 MY8 MY7 MY14 MY9 MY11 MY10
*10P8R-8.2K

R221 *8.25K/F_4 MY16
R220 *8.25K/F_4 MY17

CN8
MX1 MX7 MX6 MY9 MX4 MX5 MY0 MX2 MX3 MY5 MY1 MX0 MY2 MY4 MY7 MY8 MY6 MY3 MY12 MY13 MY14 MY11 MY10 MY15 MY16 MY17
WIRELESS_ON_R
WIRELESS_OFF_R
[29] MUTE_LED#
[36] CAPSLED#
R223 200_4
R222 200_4
+3V
KB CONN

+12VALW
R556 100K/F_4
R557 1M_4
Q40 AO3404
R553 *0_8
[36] KB_LED_EN
Q41 2N7002E
C706 .1U/50V_6
C686 .1U/10V_4
+5V_LED_KBLIGHT
140 mA
CN6
88513-0401-4P-L-smt
DFFC04FR042
KB LIGHT CONN

1. LEDVCC
2. LEDVCC
3. GND
4. GND

6/6 changed FP to 0603
7/18 SI modify

MY5 C346 MY6 C339 MY3 C338 MY7 C341 MY8 C340 MY9 C352 MY10 C333 MY11 C334 — 220P/50V_4
MY1 C345 MY2 C343 MY4 C342 MY0 C349 MX4 C351 MX6 C353 MX3 C347 MX2 C348 — 220P/50V_4
MX7 C354 MX0 C344 MX5 C350 MX1 C355 MY12 C337 MY13 C336 MY14 C335 MY15 C332 MY16 C331 MY17 C330 — 220P/50V_4

FOR SG ONLY

+3V
U25 MC74VHC1G08DFT2G
C478 0.1U/10V_4
[2,8,32,36,37,38] PLTRST#
[8] DGPU_HOLD_RST#
R392 330_4 DGPU_HIN_RST#
PEGX_RST# [14]
R393 100K_4

PV Modify
change from non-stuff to stuff

+5V
R616 1K/F_4
R225 *200/F_6
WIRELESS_ON_R
[36] WIRELESS_ON#
Q45 PDTC144EU

+5V
R617 1K/F_4
R224 *200/F_6
WIRELESS_OFF_R
[36] WIRELESS_OFF#
Q46 PDTC144EU

LED1 Wireless Enable White 27
LED2 Wireless Disable Amber 28
LED3 Mute Amber 29
LED4 Caps White 30
VCC 31
VCC 32

N85/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.	
	Size: Custom; Document Number: KB/LED/POWER CONN	Rev: 1A
	Date: Tuesday, August 10, 2010	Sheet 35 of 49

Adapter Type

+3VPCU
D4
1SS355
AD_TYPE
R197 10K/F_4
R192 100/F_4
AD_ID
C299 .1U/10V_4
R188 12.1K/F_4
C277 100P/50V_4
5/7 modify

R273
64.9K -->65W CS36492FB17
33.2K -->90W CS33322FB13
Change to 1SS355 as Current loss

Thermal Shutdown

R196 *4.7K/F_4 +1.05V_VTT
C304 .1U/10V_4
Q7 *MMBT3904-7-F
PM_THRMTRIP# [2,9]
3920_RST#
+3VPCU R572 47K_4 C275 .1U/10V_4

4/29 DB change net name.

U11

SERIRQ [7]
LFRAME# [7,37]
LAD0 [7,37]
LAD1 [7,37]
LAD2 [7,37]
LAD3 [7,37]
CLK_33M_KBC [8]
PLTRST# [2,8,32,35,37,38]
CLKRUN# [6]

SCI1# [9]
EC_A20GATE [9]
EC_RCIN# [9]
3920_RST# [37]

MX0 [35]
MX1 [35]
MX2 [35]
MX3 [35]
MX4 [35]
MX5 [35]
MX6 [35]
MX7 [35]

MY0 [35]
MY1 [35]
MY2 [35]
MY3 [35]
MY4 [35]
MY5 [35]
MY6 [35]
MY7 [35]
MY8 [35]
MY9 [35]
MY10 [35]
MY11 [35]
MY12 [35]
MY13 [35]
MY14 [35]
MY15 [35]
MY16 [35]
MY17 [35]

GPUT_CLK [17]
GPUT_DATA [17]
GFX_HWPG [47]
ACIN [45,46]
TPCLK [34]
TPDATA [34]

5/7 modify from EC request

BIOS_RD#
BIOS_WR#
BIOS_CS#

PCI_SERR# [9]
7/30: SI modify
DGPU_PR_EN
EC_GPXD1
SUS_PWR_ACK [6]
GENERICB [16,26]
RF_LINK# [37]
BLUELED
T1
EC_PECI [2]
R91 *0_4
USB_ENABLE# [33,34,38]
SUSON [40,44,45]
MAINON [39,40,41,44,45,46]
LAN_POWER [45]
S5_ON [45]
BLED_COMBO# [37]
R93 0_4
APD_120W
AC_PRESENT [6]
MBATLED0# [46]
AC_LED_ON# [46]
WIRELESS_ON# [35]
WIRELESS_OFF# [35]

SI change S3 power circuit

V18R
C90 .1U/10V_4
C85 4.7U/6.3V_6
KB3930QF
7/18: SI modify

	GPI041
SI	1
PV	0

Change to RB500 as Current loss

SCI1# D2 RB501V-40 SIO_EXT_SCI# [9]
DNBSWON#1 D1 RB500V-40 DNBSWON# [6]
KBSMI#1 D3 RB500V-40 SIO_EXT_SMI# [9]

+3VPCU
C125 .1U/10V_4
C84 .1U/10V_4
C91 .1U/10V_4
C118 .1U/10V_4
C227 .1U/10V_4
C153 .1U/10V_4
C280 *10U/6.3V_8
C235 .1U/10V_4
+3VPCU_EC

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 AVCC

AD0/GPI38 AD1/GPI39 AD2/GPI3A AD3/GPI3B
TEMP_MBAT [46]
AD_TYPE
AD_AIR [46]
SYS_I [46]
5/7 modify

DA0/GPO3C DA1/GPO3D DA2/GPO3E DA3/GPO3F
EC_TEST1 [34]
GPU_PROCHOT [16]
VFAN [37]
D/C# [46]

PWM1/GPIOE PWM2/GPIO10
PWM_VADJ [24,25]
KB_LED_EN [35]

FANPWM1/GPIO12 FANPWM2/GPIO13 FANFB1/GPIO14 FANFB2/GPIO15
G_INT2# [30]
LID_CONTROL [25]
FAN1SIG [37]
ODD_PD [33]
5/12 modify

SCL1/GPIO44 SDA1/GPIO45 SCL2/GPIO46 SDA2/GPIO47
MBCLK [46]
MBDATA [46]
MBCLK2 [8,13,26,30]
MBDATA2 [8,13,26,30]
[For Battery charge]
[For CPU thermal]

GPIO4 SUSB# SUSB# [6]
GPIO7 GPIO8 HWPG HWPG [14,39,40,41,44,49]
CPU_PROCHOT

GPIOA GPIOB GPIOC GPIOD GPIO11 GPIO16 GPIO17 GPIO18
SUSC# [6]
DGPU_PWR_EN_1
NBSWON1# [34]
SLP_S5 [6]
GPIO33_E [7]
EC_DEBUG1 [37]
EJECT# [33]
KBSMI#1

GPIO19 GPIO1A
VRON [47]
+3VPCU
R181 1K/F_4
For SP8
4/19 modify from EC request
R156 0_4 EC_PECI [2]
7/30: SI modify

CIR_RX/GPIO40 GPIO41 GPIO42 GPIO52 GPIO53 GPIO54 GPIO55 GPIO56 GPIO57 GPIO58 GPIO59
DNBSWON#1
CAPSLED# [35]
PWR_LED# [34,37]
EC_PWROK [6,25]
RSMRST# [6]
VOLMUTE# [29]
BIOS_SPI_CLK_EC
LID_EC# [25,34]

XCLKO XCLKI
CRY2 C89 20P/50V_4
CRY1 Y3 *32.768KHZ C87 *20P/50V_4
8/1: SI modify

GND1 GND2 GND3 GND4 GND5 AGND

R85 33_4 BIOS_SPI_CLK
C72 22P/50V_4
For EMI

CRY2 R529 0_4 PCH_SUSCLK [6]
R526 100K_4
7/18: SI modify

Q4 *2N7002EPT_SC70
VGA_ALERT [16,17]

+3VPCU_EC
L22 BLM18BA470SN1D
C291 4.7U/6.3V_6
U15 VOUT VIN SHDN NR/FB GND
*TPS73133
C274 *1U/6.3V_4
+5VPCU
C250 *1U/6.3V_4

+3VPCU
R80 10K/F_4
PQ19 2N7002EPT_SC70
R81 *0_4/S H_PROCHOT# [2,47]
ACIN R109 *0_4
CPU_PROCHOT
CPU_PROCHOT2
PQ21 *2N7002EPT_SC70
PQ18 2N7002EPT_SC70

+3V
R140 4.7K/F_4 MBCLK2
R135 4.7K/F_4 MBDATA2
R139 *10K_4 GPIO33_E
R162 10K/F_4 G_INT2#
5/12 modify

+3VPCU
R144 10K/F_4 NBSWON1#
R143 4.7K/F_4 MBCLK
R136 4.7K/F_4 MBDATA

FOR DIS ONLY
DGPU_PWR_EN_1 R121 *0_4 DGPU_PWR_EN [9,42,43,44]

4/19 modify from EC request

FOR SG/DIS
[8,9,42,43,44] DGPU_PWROK R400 0_4 EC_GPXD1
[42,44] DGPU_PR_EN R387 0_4 DGPU_PR_EN_E

FOR UMA ONLY
R389 *100K_4

Socket: DG008000031
MXIC AKE3KZP0001
WINBOND AKE37ZN0N00
AMIT AKE38ZN0800

[34,37] BLUELED R92 100K/F_4
CLK_33M_KBC R130 *10_4 C156 *10P/50_4
For EMI

R151 1K/F_4 R42 *1K/F_4 +3V_VGA GENERICB
Low ==>3D
Hi ==>NO 3D 3D select for EC

R95 10K/F_4 R94 *10K/F_4 +3VPCU APD_120W
Hi ==> 120W
Low ==> 65W/90W Adapter select for EC

DB modified 20100429 co-lay with U24
U37 W25X40BVSSIG
BIOS_CS# BIOS_SPI_CLK BIOS_WR# BIOS_RD# SPI_3P SPI_7P
+3VPCU

U38
BIOS_CS# BIOS_SPI_CLK BIOS_WR# BIOS_RD# SPI_3P SPI_7P
+3VPCU R108 10K/F_4
C78 .1U/10V_4
R87 10K/F_4
7/18: SI modify

N85/RD2

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

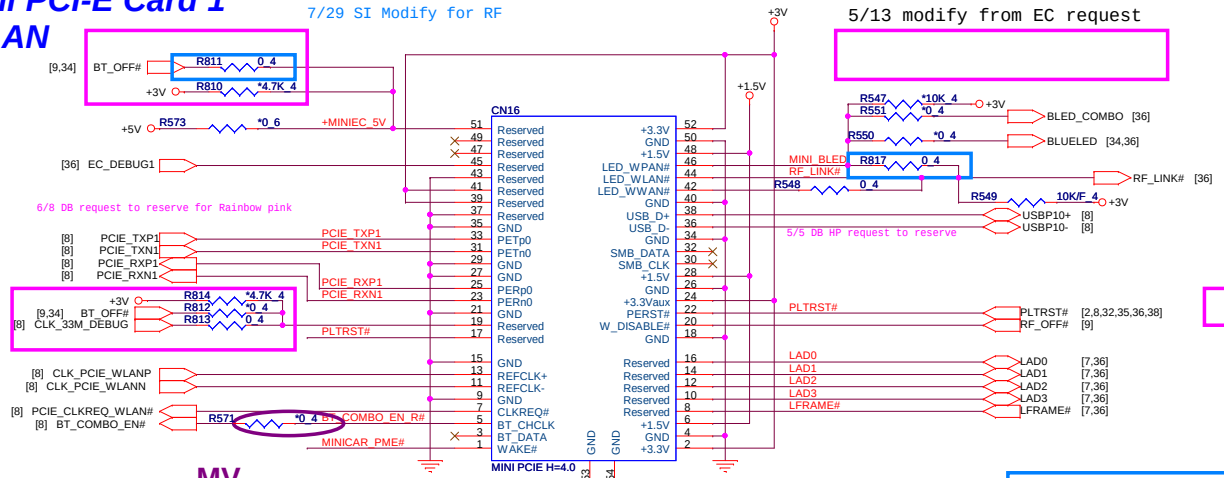
Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

Date: Tuesday, August 10, 2010 Sheet 36 of 49

Mini PCI-E Card 1 WLAN

7/29 SI Modify for RF

5/13 modify from EC request

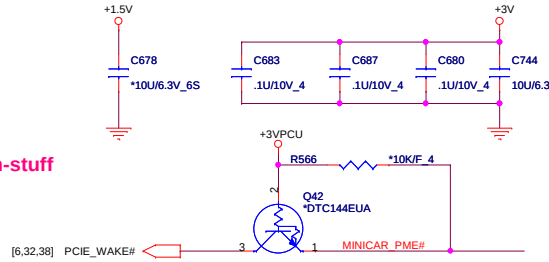


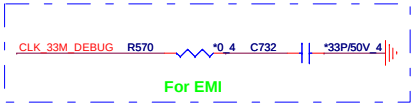
MV

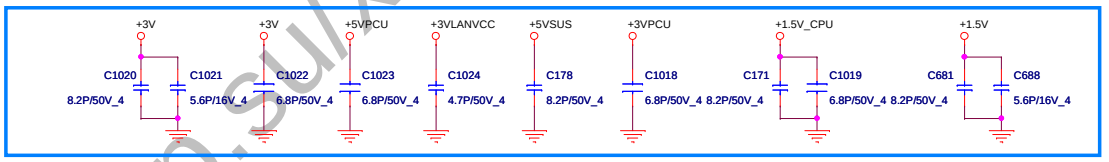
7/21 SI Modify for RF

BT_DATA,BT_CHCLK,CLKREQ#,W_DISABLE# pin has internal pull-Down 100k resister.

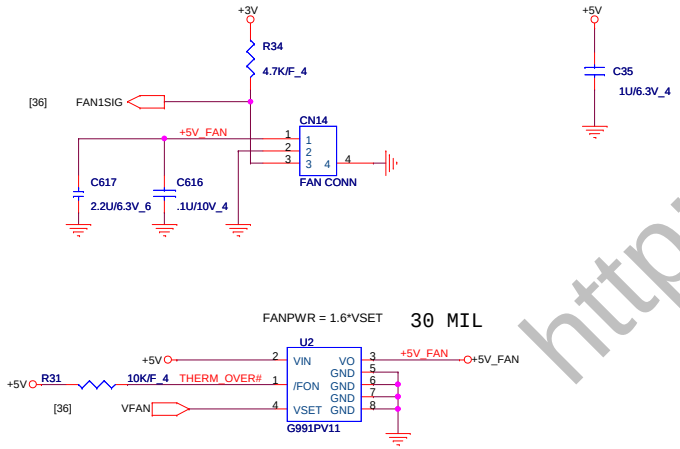
PV non-stuff



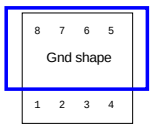




CPU FAN



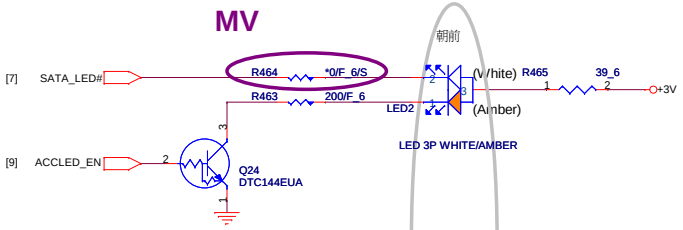
G995 layout notice



LED

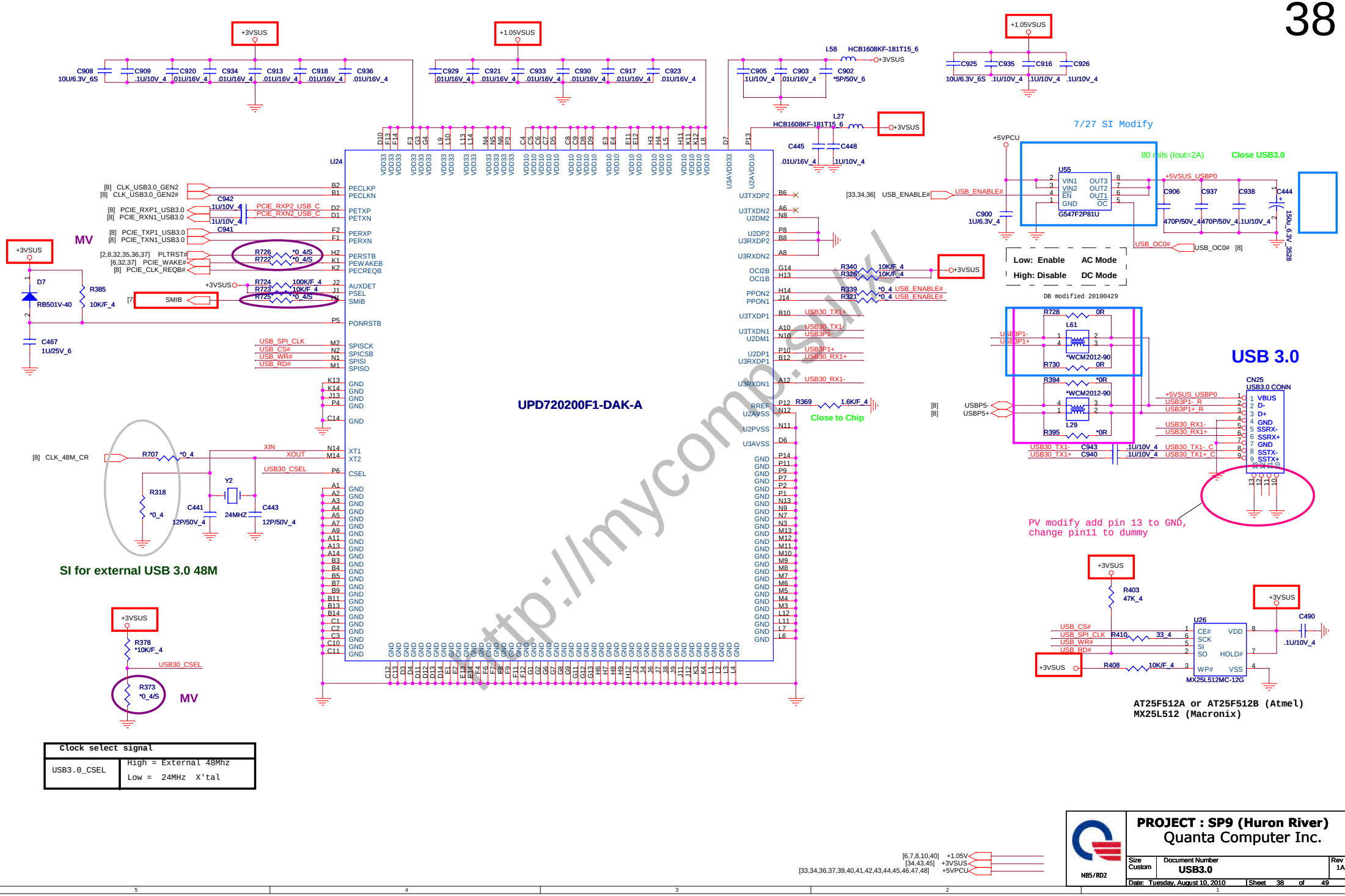
SI Change Fpptprint

MV

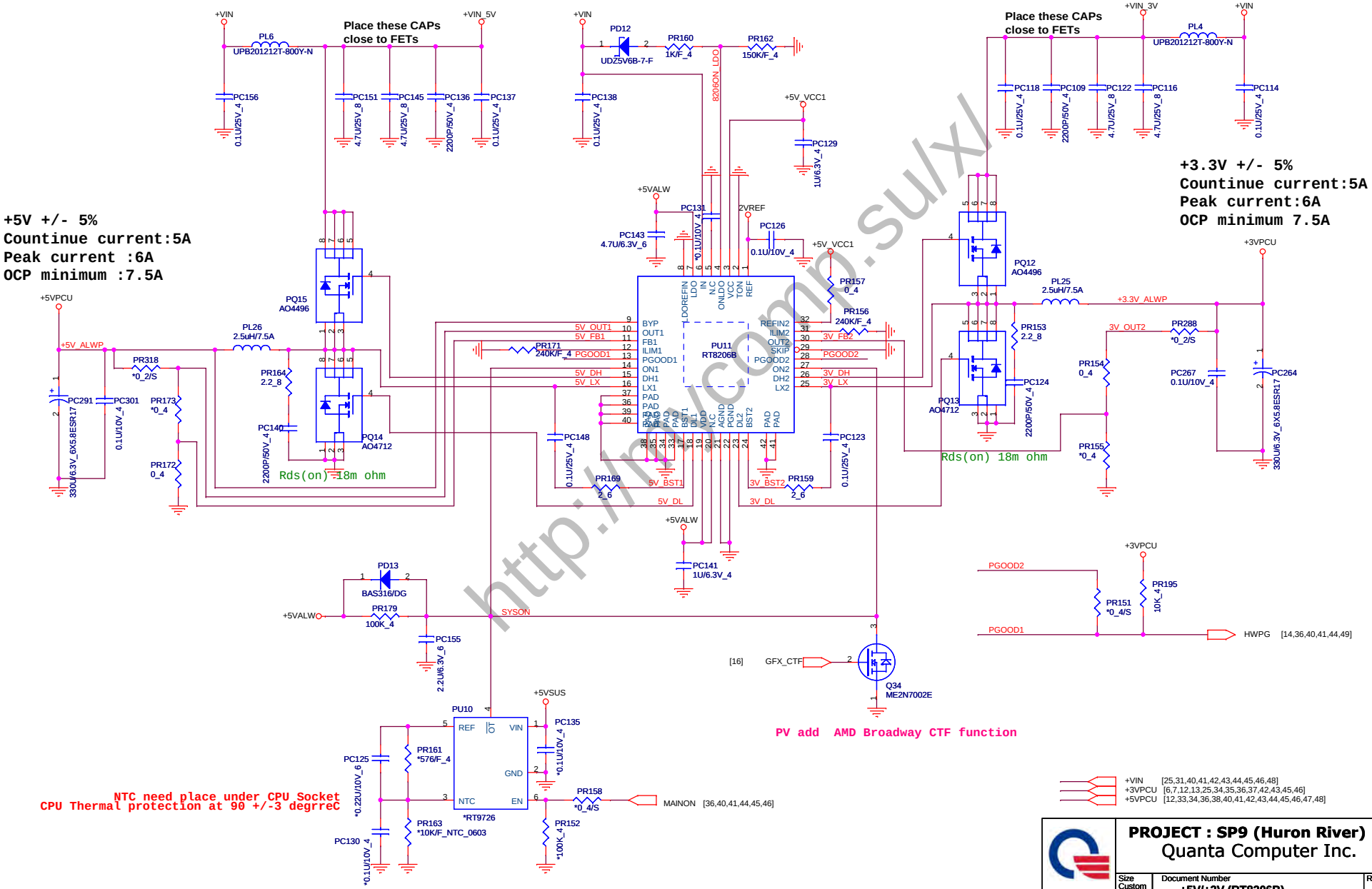


PV Change Fpptprint for solve SMT open issue

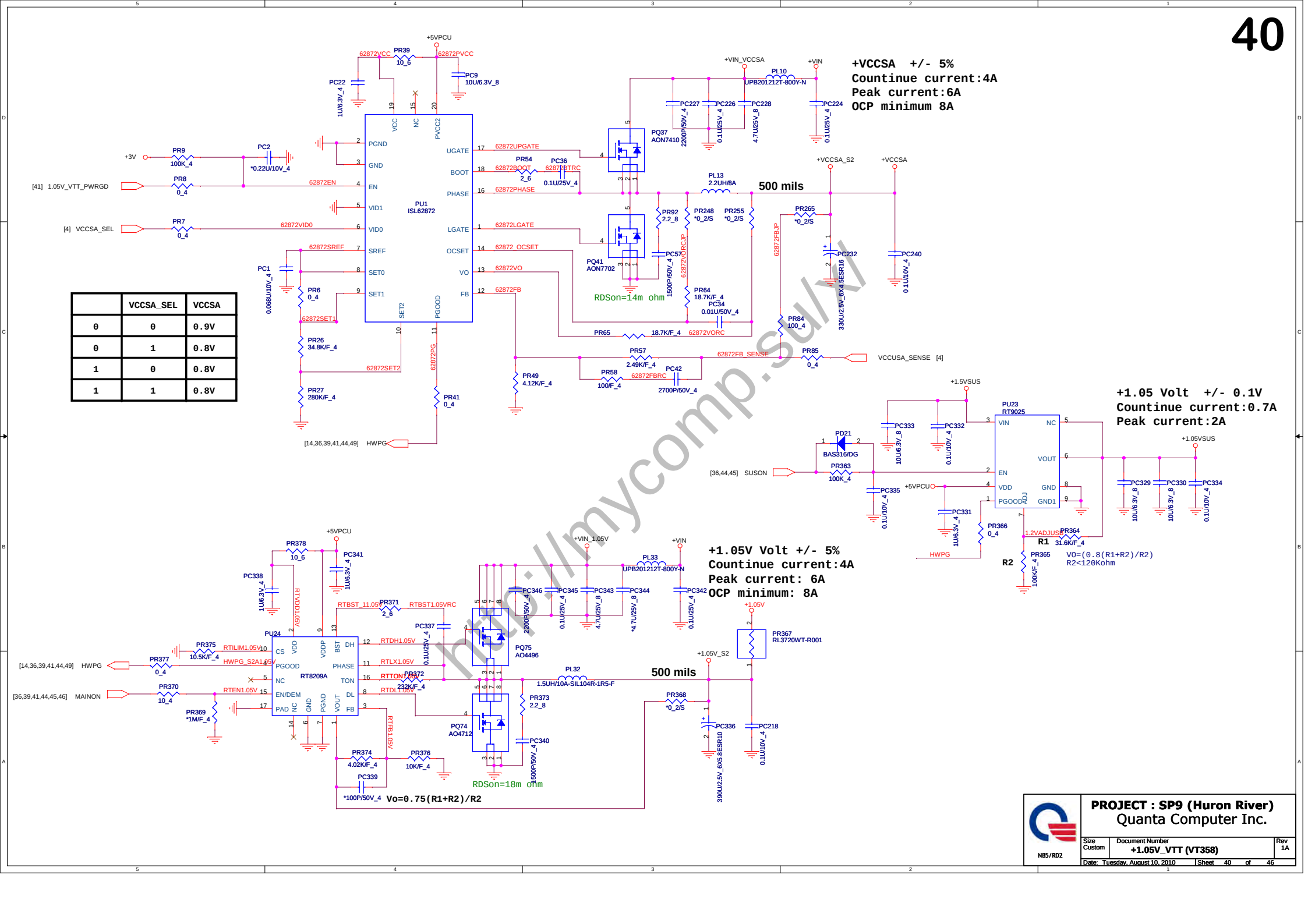
PROJECT : SP9 (Huron River) Quanta Computer Inc.		
Size: Custom	Document Number: MINI PCIE CONN X2	Rev: 1A
N85/RD2	Date: Tuesday, August 10, 2010	Sheet 37 of 49



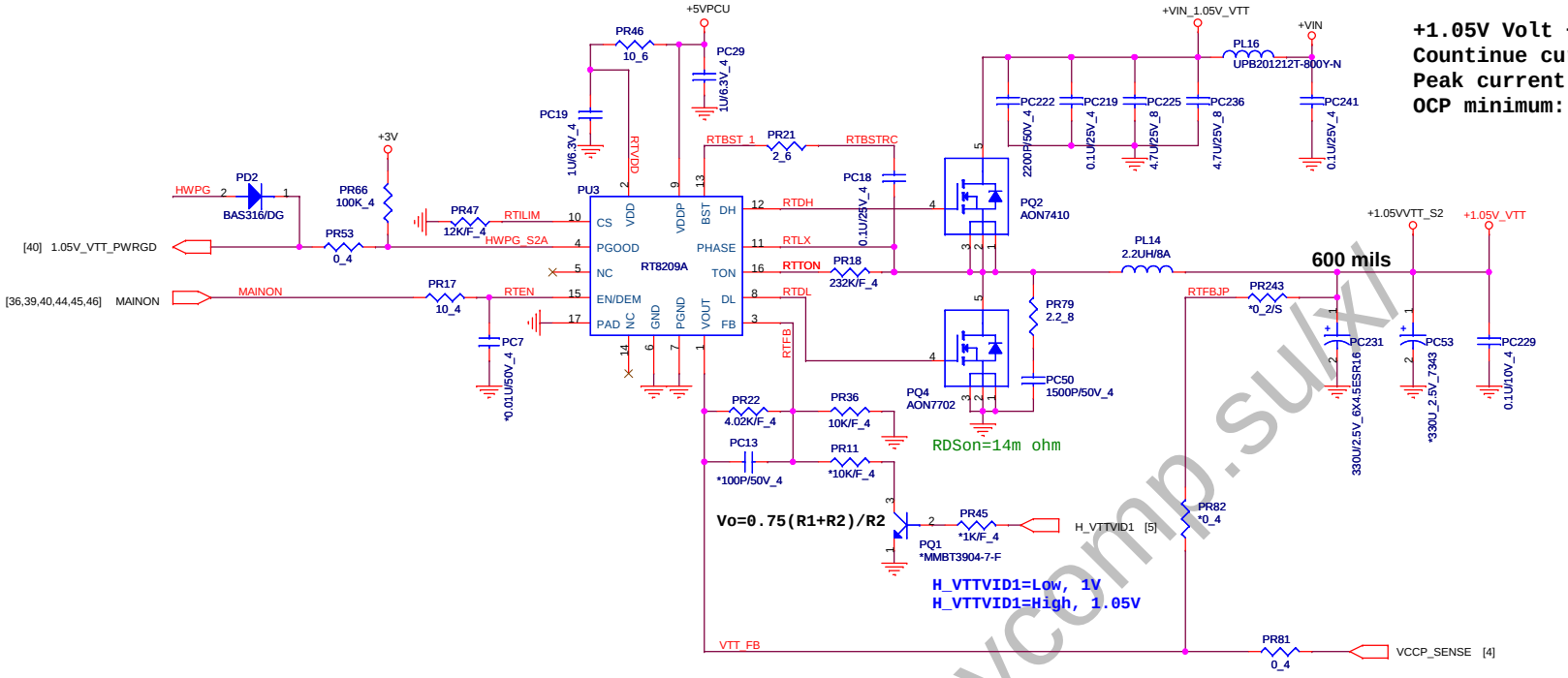
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

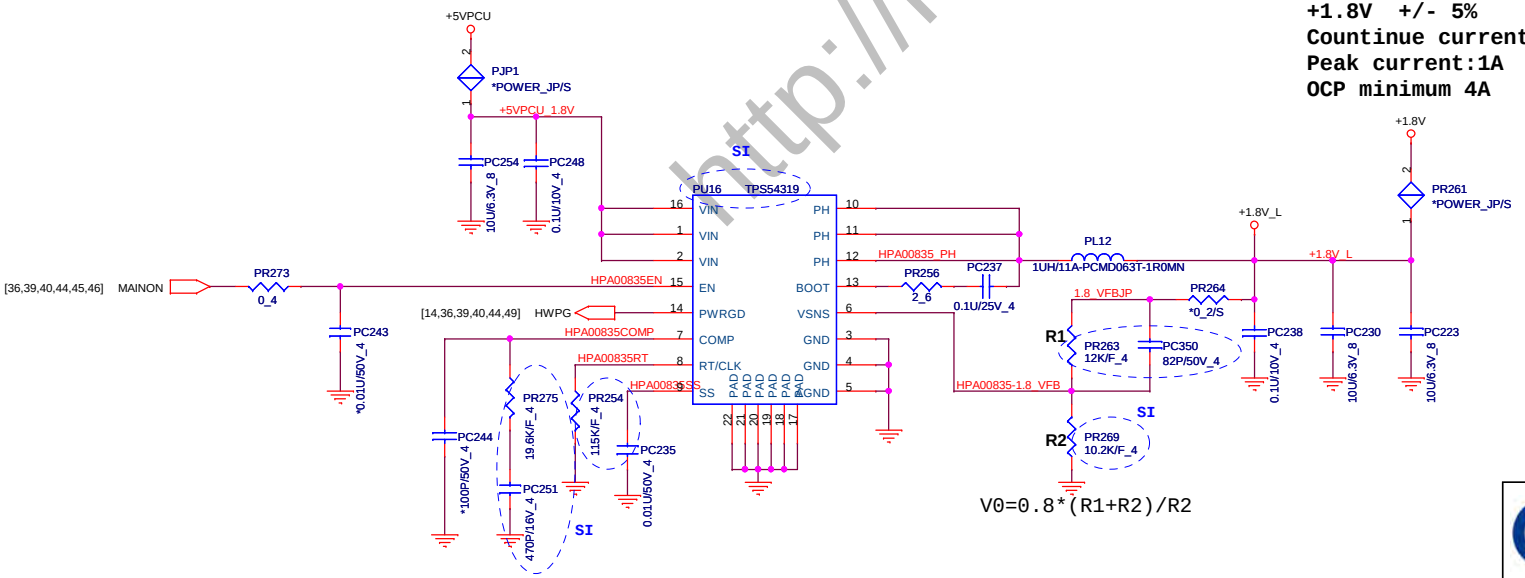


NB5/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.	
Size Custom	Document Number +5V/+3V (RT8206B)	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 39 of 46	



	VCCSA_SEL	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.8V
1	1	0.8V



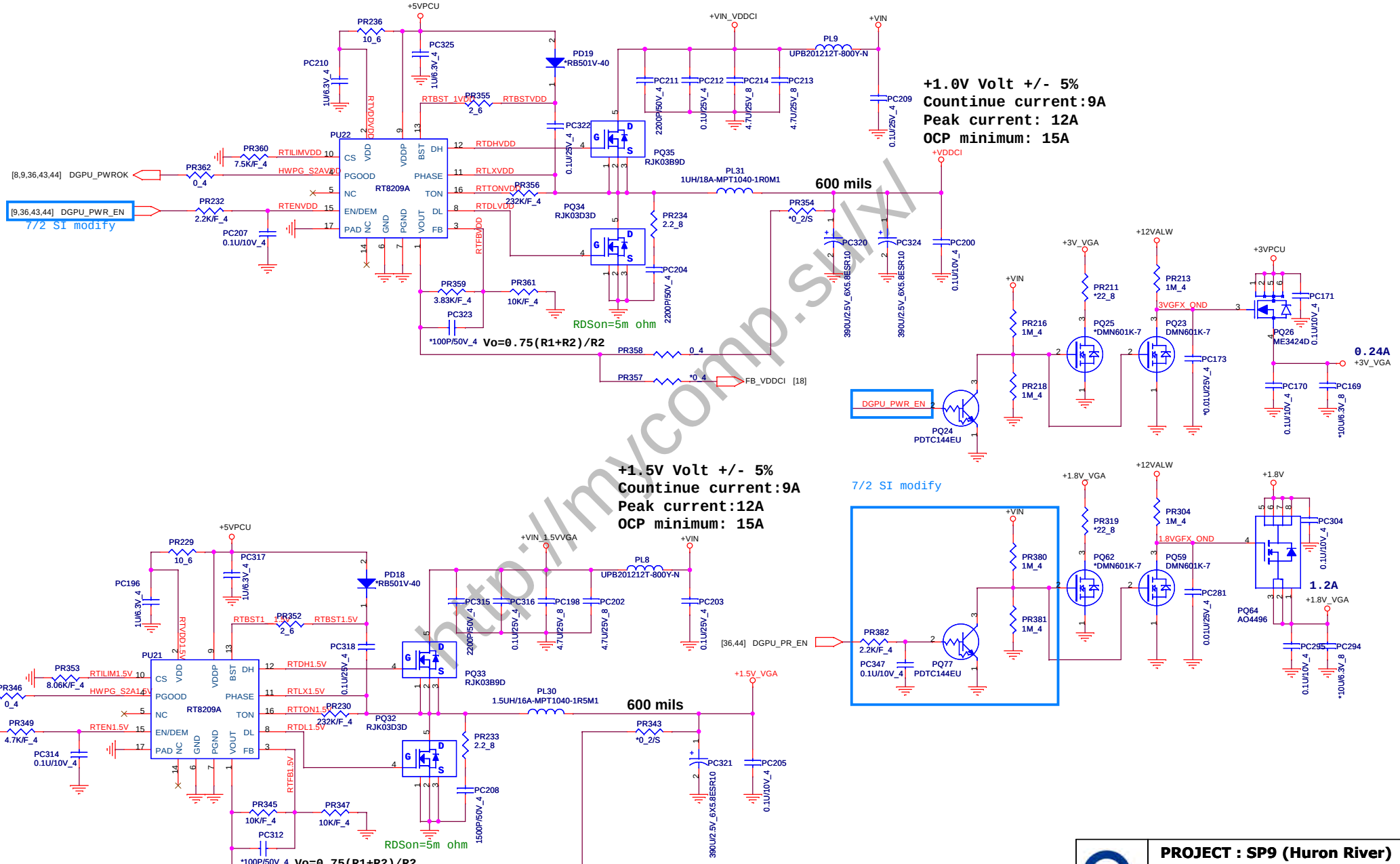


NB5/RD2

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V/+1.8V (RT8204C)	1A

Date: Tuesday, August 10, 2010 | Sheet 41 of 46



NB5/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.		
	Size: Custom	Document Number: VGA Core/+1.8VGFX/1.0VGFX	Rev: 1A
	Date: Tuesday, August 10, 2010	Sheet 42 of 46	

Note: VID[0:5]=011000=0.95V VID[0:5]=011010=0.9V

+VGACORE +/- 5%
Countinue current:27A
Peak current:45A
OCP minimum 50A

Granville LP Setting

CTRL0	Vo
0	0.95
1	0.9

7/2 SI modify

Iocset*Roc=Iocp*Rdroop
R23=Roc=30A*1m Ohms/10uA ~ 3K
Where :
Rdroop is AMD spec : -1 m Ohms
Iocp is desire over current
Iocset is recommendation 10uA from Rbias

Close to Phase 1 Inductor
Panasonic
ERT-J1VR103FA

Parallel

PROJECT : SP9 (Huron River)
Quanta Computer Inc.
Size: Custom | Document Number: GPU CORE(ISL6264) | Rev: 1A
NB5/RD2
Date: Tuesday, August 10, 2010 | Sheet 43 of 46

+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

(VTT/2A)
+0.75V_DDR_VTT
PC104 10U/6.3V_8
PC105 10U/6.3V_8
(3mA)
[4,12,13] DDR_VTTREF
PC120 0.033U/10V_4

PU9 RT8207AGQW
1 VTTGND
2 VTTSNS
3 GND
4 MODE
5 VTTREF
6 COMP
7 NC
8 VDDQSNS
9 VDDQSET
10 S3
11 S5
12 NC
25 GND
24 VTT
23 VLDOIN
22 1116VBST
21 1116DRVH
20 1116LL
19 1116DRVL
18 PGND
17 CS_GND
16 1116CS
15 V5IN
14 V5FILT
13 PGOOD

+1.5VSUS
PC102 *10U/6.3V_8
+1.5VSUS_1
PR144 0_4
PR141 *0_4
DDRMODE
PR137 2_6
PC108 0.1U/25V_4
1116VDDQSET
PR142 7.5K/F_4
+5VPCU
PC117 1U/6.3V_4
PR146 10_6
PC119 1U/6.3V_4
[36,40,45] SUSON
+VIN
PR147 619K/F_4
1116TONSET
HWPG
HWPG [14,36,39,40,41,49]

PQ57 RJK03B9D
PQ51 RJK03D3D
+VIN_DDR
+VIN
PL3 UPB201212T-800Y-N
PC88 0.1U/25V_4
PC89 4.7U/25V_8
PC90 4.7U/25V_8
PC87 2200P/50V_4
PC83 0.1U/25V_4
PL22 1UH/18A-MPT1040-1R0M1
PR279 2.2_8
PC258 1500P/50V_4
51116FBJP
PR281 *0_2/S
+1.5VSUS_1
+1.5VSUS
PC259 390U/2.5V_6X5.8ESR10
PC256 0.1U/10V_4
PR149 10K/F_4
PR148 10K/F_4

need to stuff for S3 and PR263 change to 100K
[36,39,40,41,45,46] MAINON
PD11 RB501V-40
PR150 100K_4
PC121 0.1U/10V_4

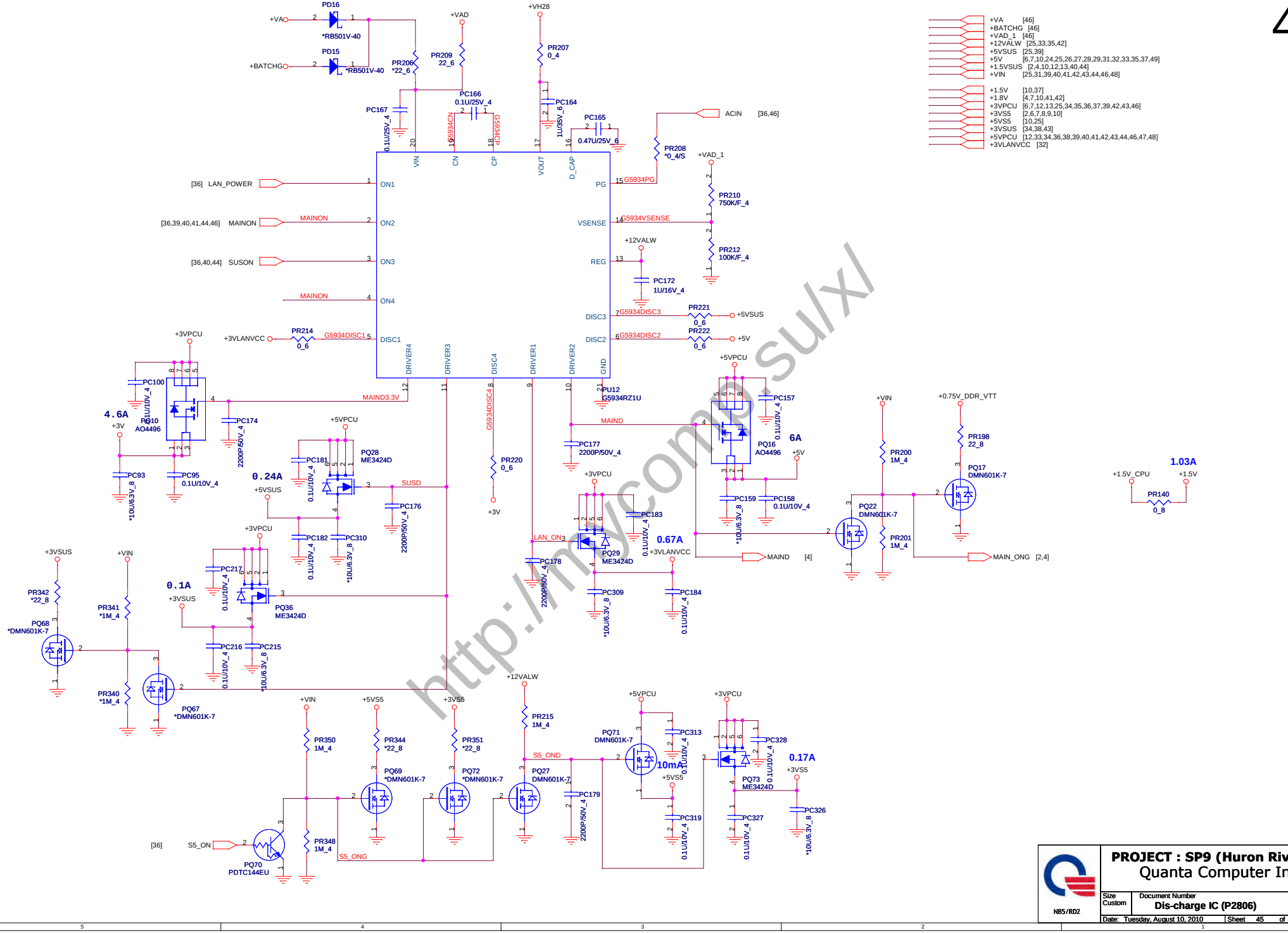
+1.0V +/- 5%
Countinue current:1.7A
Peak current:3A

8/3 SI modify
+1.5VSUS
PC206 10U/6.3V_8
PC199 0.1U/10V_4
PR235 10K/F_4
[9,36] DGPU_PWR_EN
[36,42,43] DGPU_PR_EN
+5VPCU
PC201 0.1U/10V_4
PC197 1U/6.3V_4
[8,9,36,42,43] DGPU_PWROK
PR231 0_4

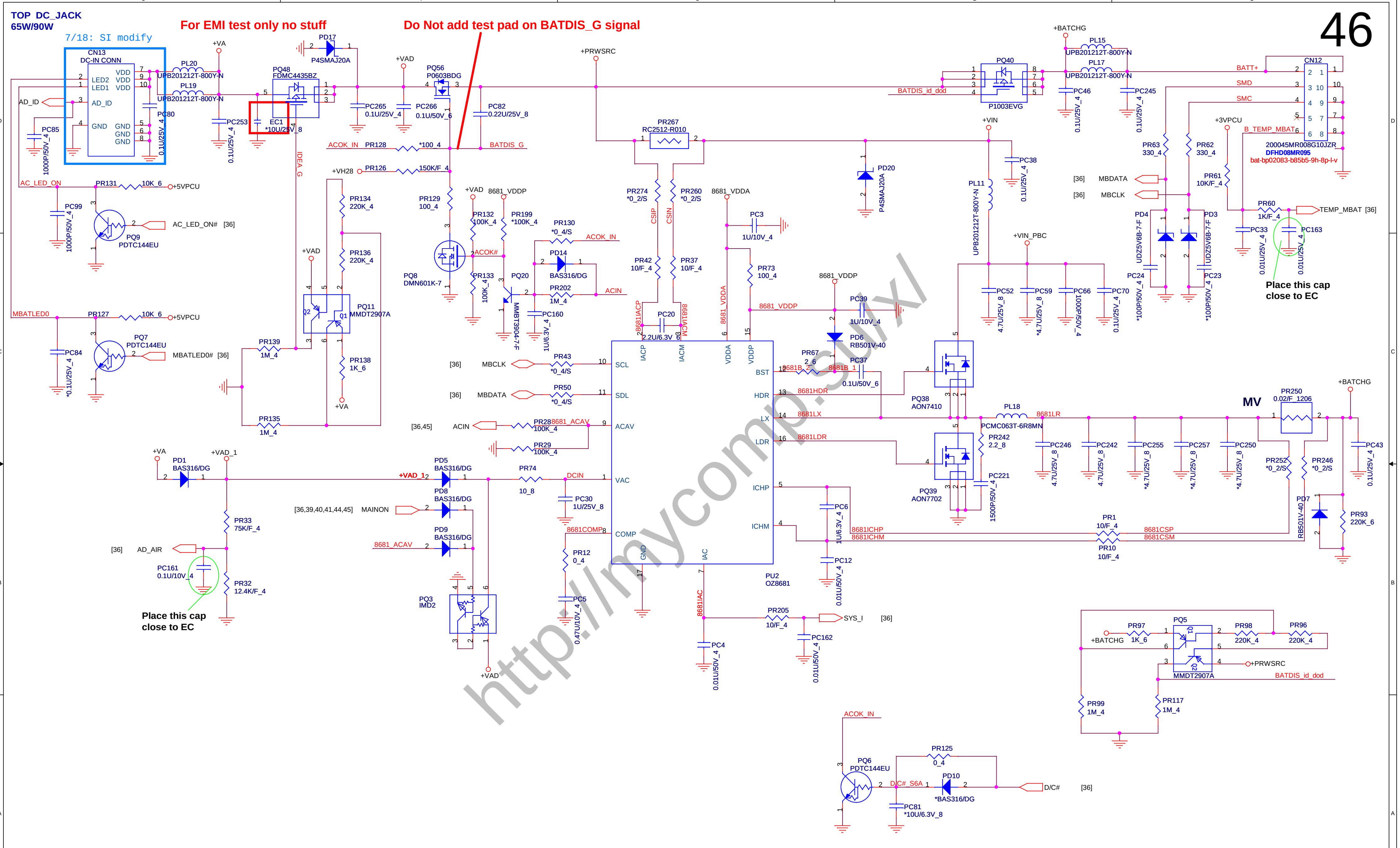
PU14 RT9025
VIN
EN
VDD
PGOOD
NC
VOUT
GND
GND1
ADJ

+1.0V_VGA
PC194 10U/6.3V_8
PC195 10U/6.3V_8
PC193 0.1U/10V_4
1.2VADJ1.0V
R1
PR227 26.7K/F_4
/SI
R2
PR228 100K/F_4
VO=(0.8(R1+R2)/R2)
R2<120Kohm

NB5/RD2
PROJECT : SP9 (Huron River)
Quanta Computer Inc.
Size Custom
Document Number DDR3 (RT8207)
Rev 1A
Date: Tuesday, August 10, 2010
Sheet 44 of 46



NB5/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.	
Size: Custom	Document Number: Dis-charge IC (P2806)	Rev: 1A
Date: Tuesday, August 10, 2010	Sheet 45 of 46	



PROJECT : SP9 (Huron River)

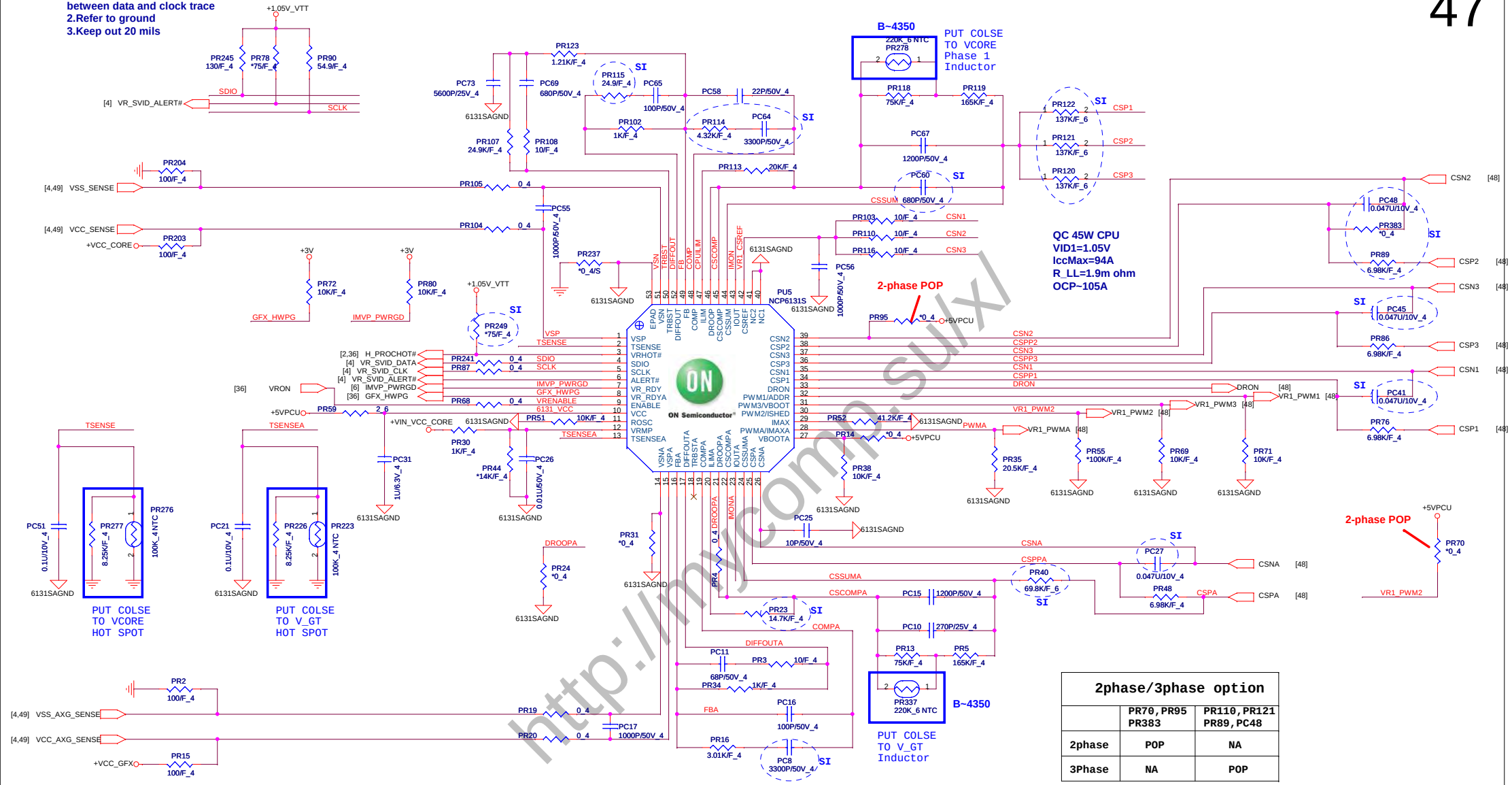
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (BQ24704)	1A

Date: Tuesday, August 10, 2010 Sheet 46 of 46

NB5/RD2

1.Alert trace routing
between data and clock trace
2.Refer to ground
3.Keep out 20 mils



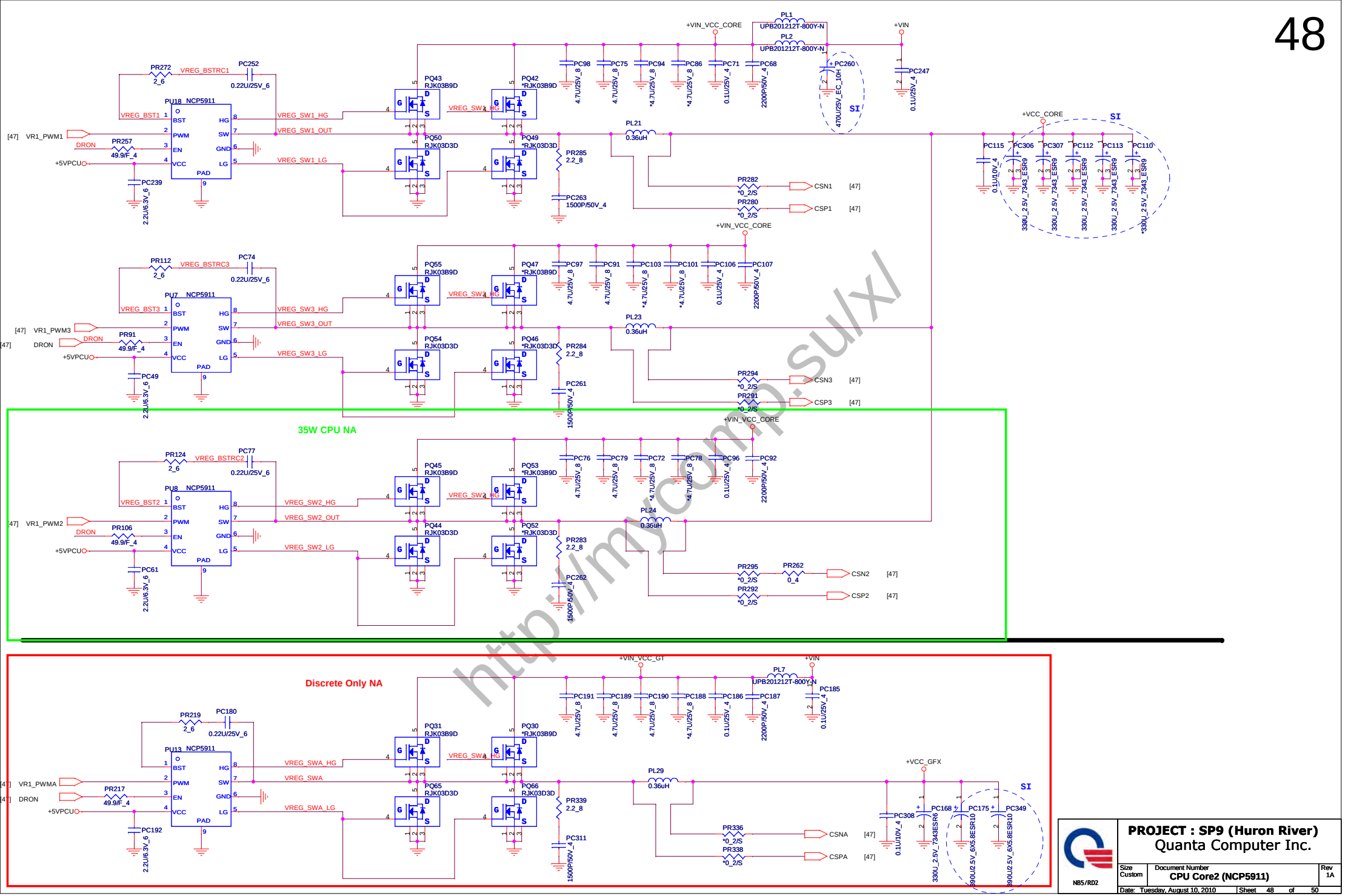
2phase/3phase option			
	PR70,PR95 PR383	PR110,PR121 PR89,PC48	
2phase	POP	NA	
3Phase	NA	POP	

UMA(Switchable)/Discrete Only option			
	PC336,PC340 PC343,PC337 PC342	PR427,PR433,PR430,PR431,PR423,PR435 PR338,PR424,PR428,PR432,PC339,PC341 PR425,PR426,PR429,PR420,PR422,PR380 PR399,PR421,PC352,PR417,PR418,PC354 PC419	PR434,PR436 PR378
UMA	POP	POP	NA
Discrete	Change to 0 ohm	NA	POP

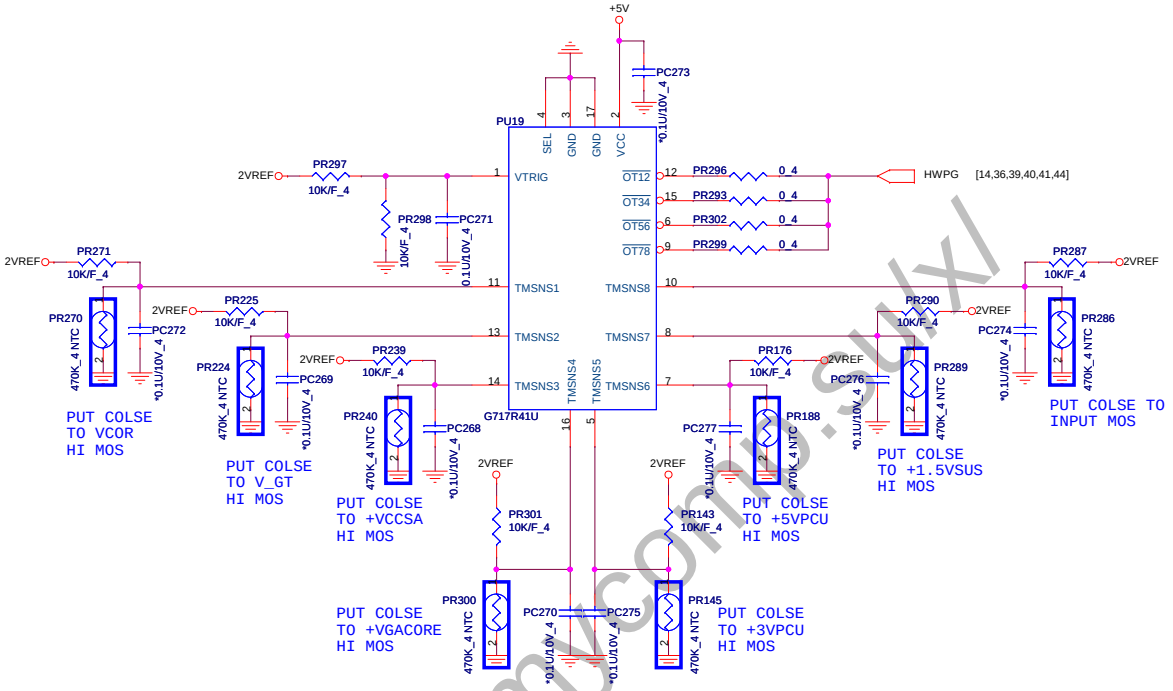
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core1 (NCP6131S)	1A
Date: Tuesday, August 10, 2010	Sheet 47 of 46	

N85/RD2



N85/RD2	**PROJECT : SP9 (Huron River)** Quanta Computer Inc.		
	Size: Custom	Document Number: CPU Core2 (NCP5911)	Rev: 1A
	Date: Tuesday, August 10, 2010	Sheet 48 of 50	



Vender	Size	P/N
EON	128KB	
	512KB	AKE37ZN0Q01 (EN25F40-100HIP)
Winbond	128KB	AKE35FN0N00 (W25X10BVSNIG)
	512KB	AKE37FN0N01 (W25X40BVSSIG)
Socket		DG008000031