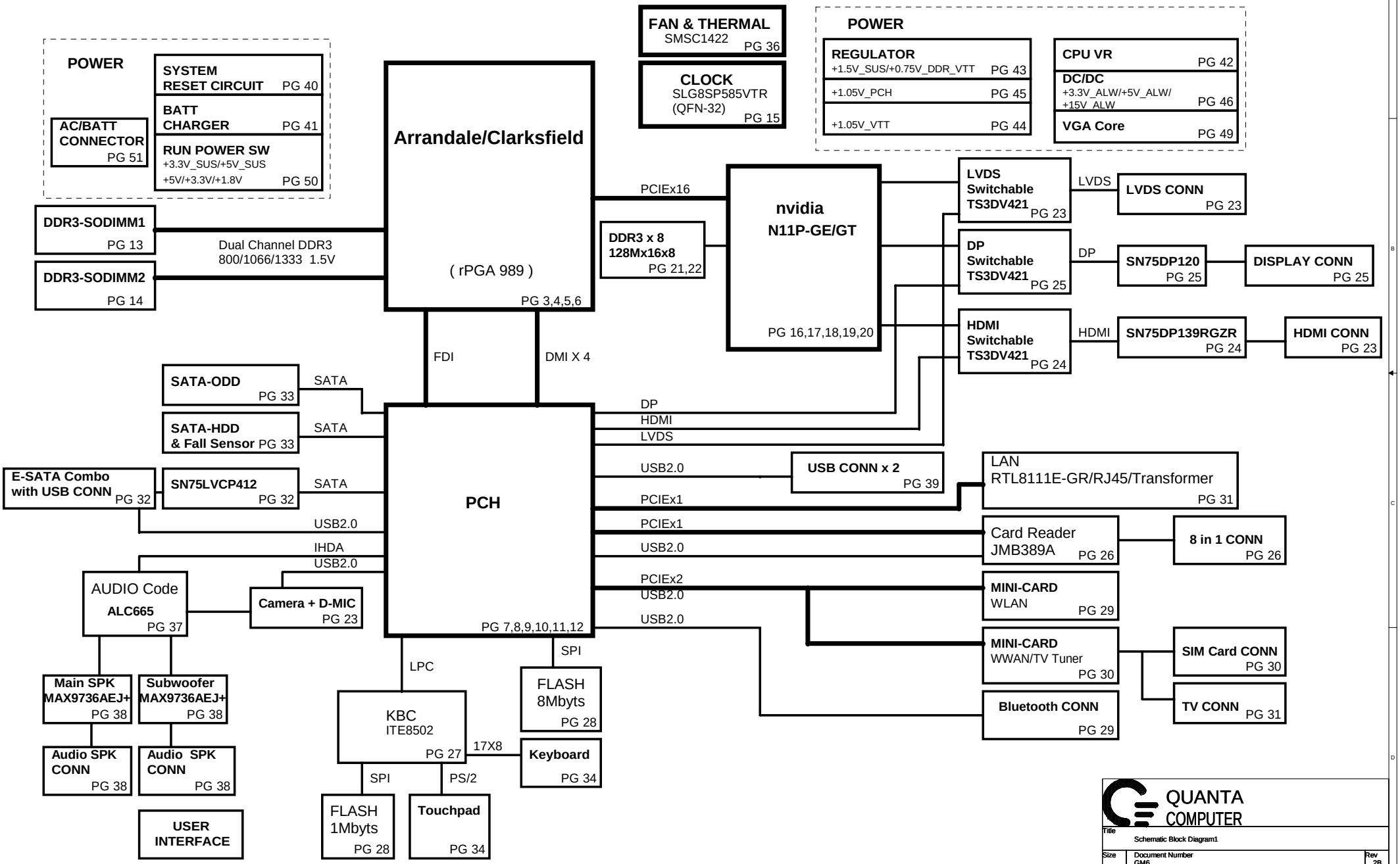
GM6B Studio Intel UMA and Discrete GFX

VER : 1A
PWA:
PWB:



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
GND	ALL	

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Title	Index & Power Status	
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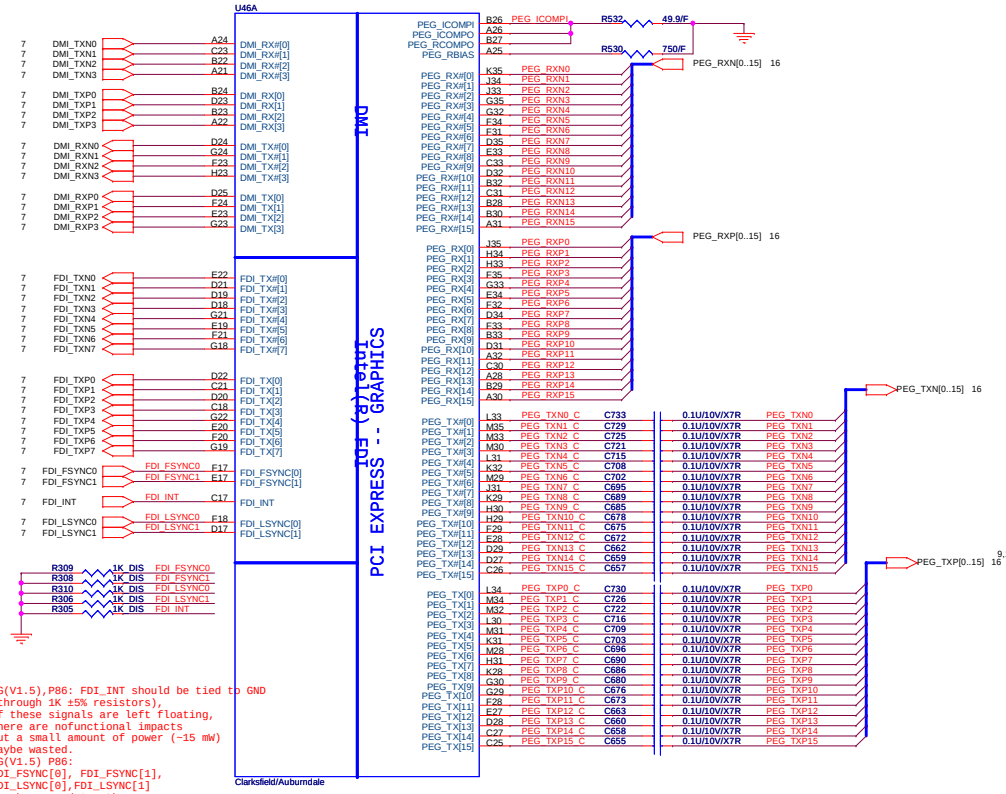
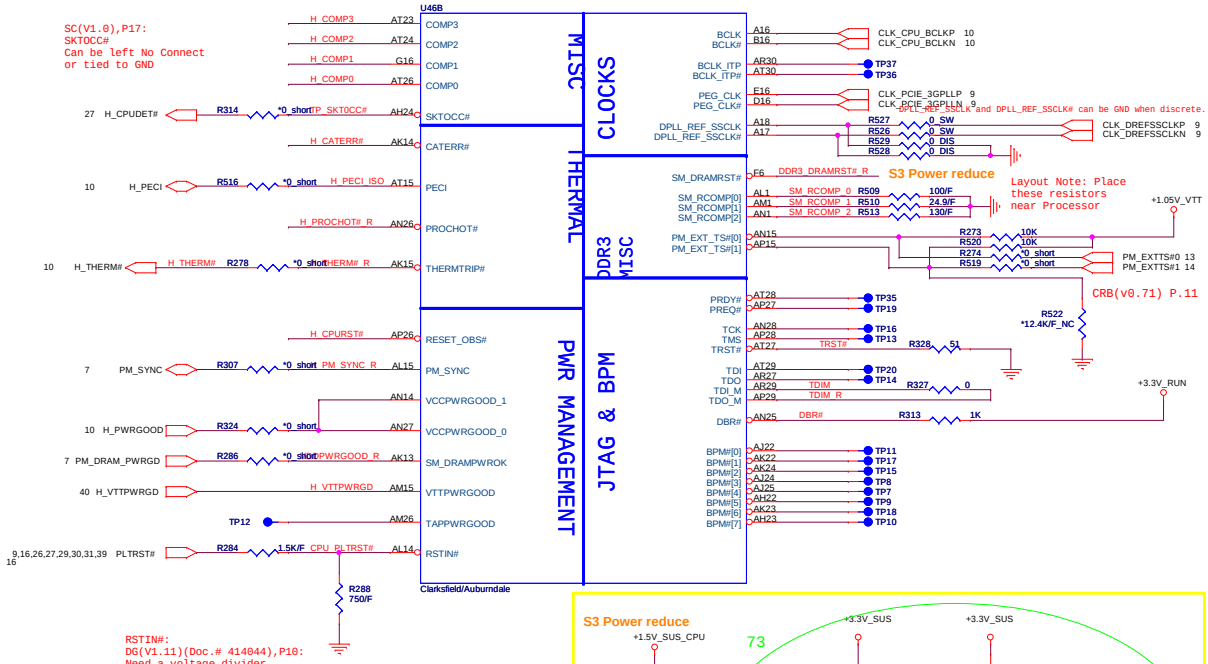
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



DG(V1.5),P86: FDI_INT should be tied to GND (through 1K ±5% resistors), if these signals are left floating, there are nofunctional impacts but a small amount of power (~15 mW) maybe wasted.
DG(V1.5) P86: FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],FDI_LSYNC[1] can be ganged together with one resistor[1K ±5% resistors].

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



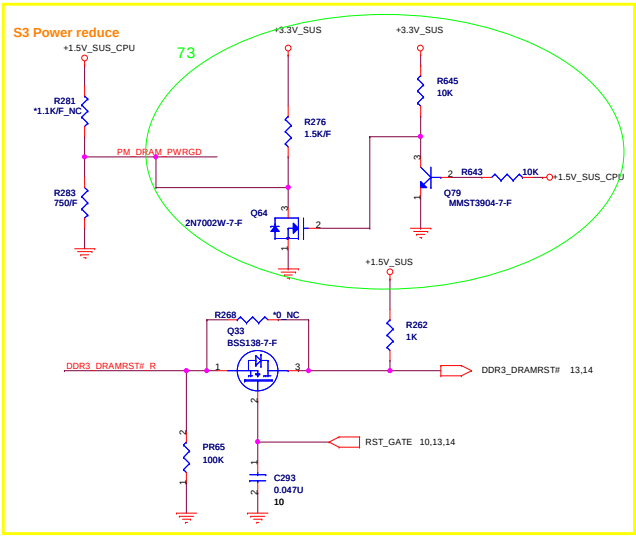
SC(V1.0),P17: SKTOCC# Can be left No Connect or tied to GND

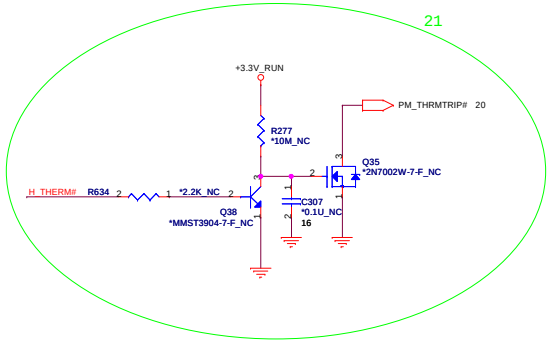
RSTIN#: DG(V1.11)(Doc.# 414044),P10: Need a voltage divider network to scale down from 3.3V (PCH driven) to 1.05V/1.1V (Clarksfield/Auburndale)

S3 Power reduce

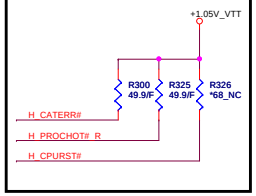
Layout Note: Place these resistors near Processor

CRB(v0.71) P.11





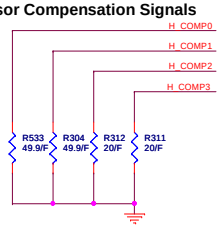
Processor Pullups



SC(1.0V),P17: H_PROCHOT#D use: pull to 68 ohm if it isn'tt used: pull to 50 ohm

SC(1.0V),P17: H_CATERR# 49.9-Ω ±1% Pull-Up to the VTT rail (+V1.1S_VTT)

Processor Compensation Signals



DG(V1.0),P17: COMP[0.1] 49.9-Ω ±1% pull-down to GND COMP[2.3] 20-Ω ±1% pull-down to GND

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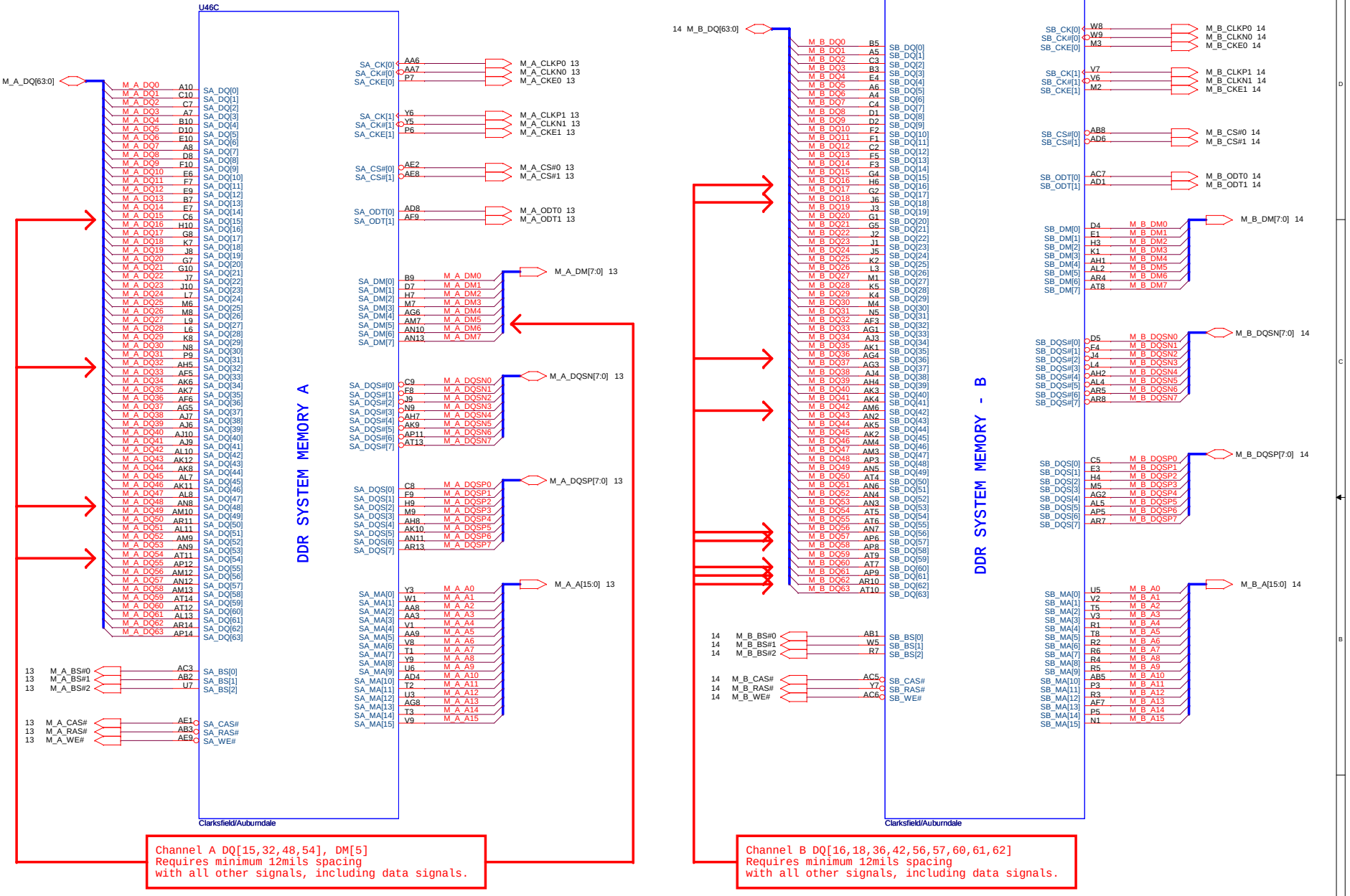
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

CPU Core Power

ARD:48A
CFD:52A

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

18A

22A

(15mils)

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

ARD:3A
CFD:6A

0.6A

S3 Power reduce

Clarksfield/Auburndale

Note:
For Validating IMVP VR R6451 should be STUFF and R2N1 NO_STUFF

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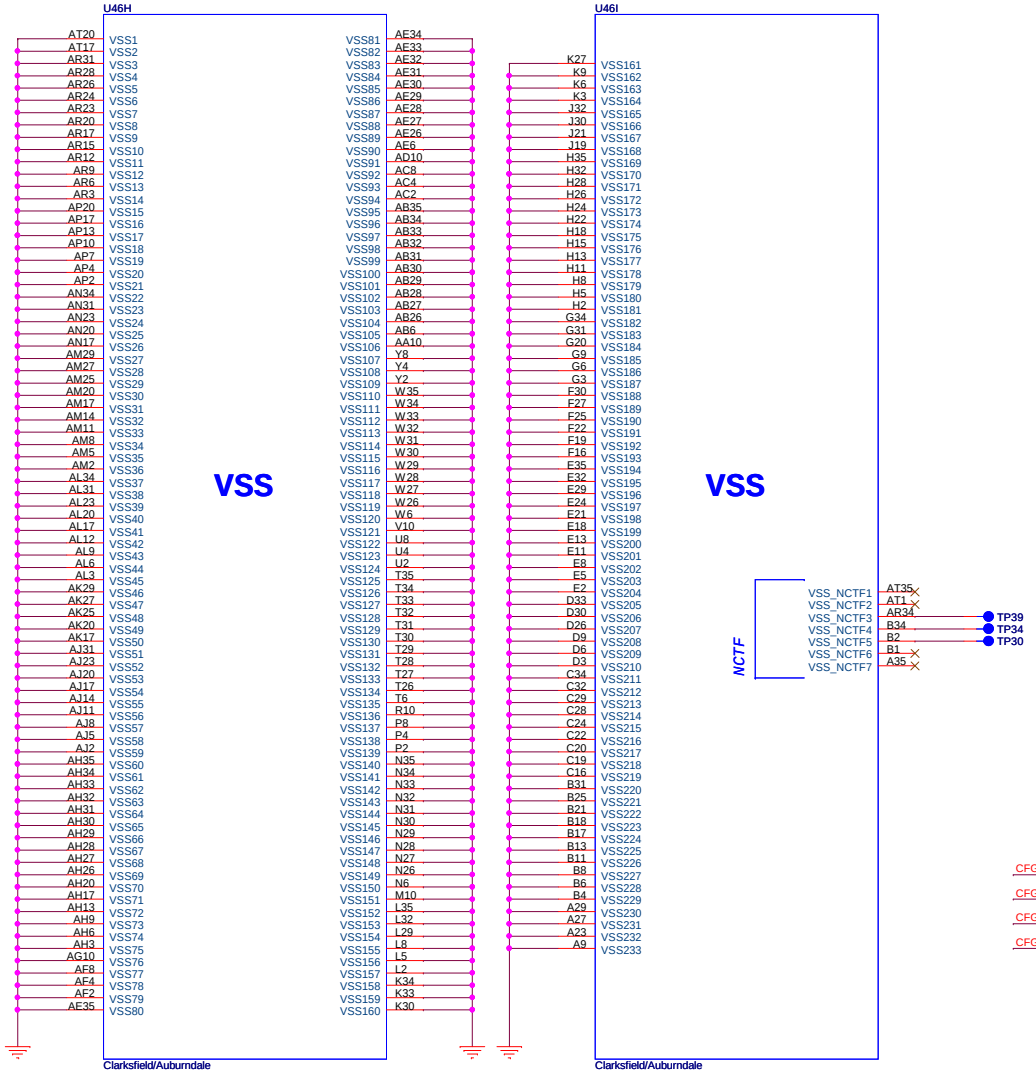
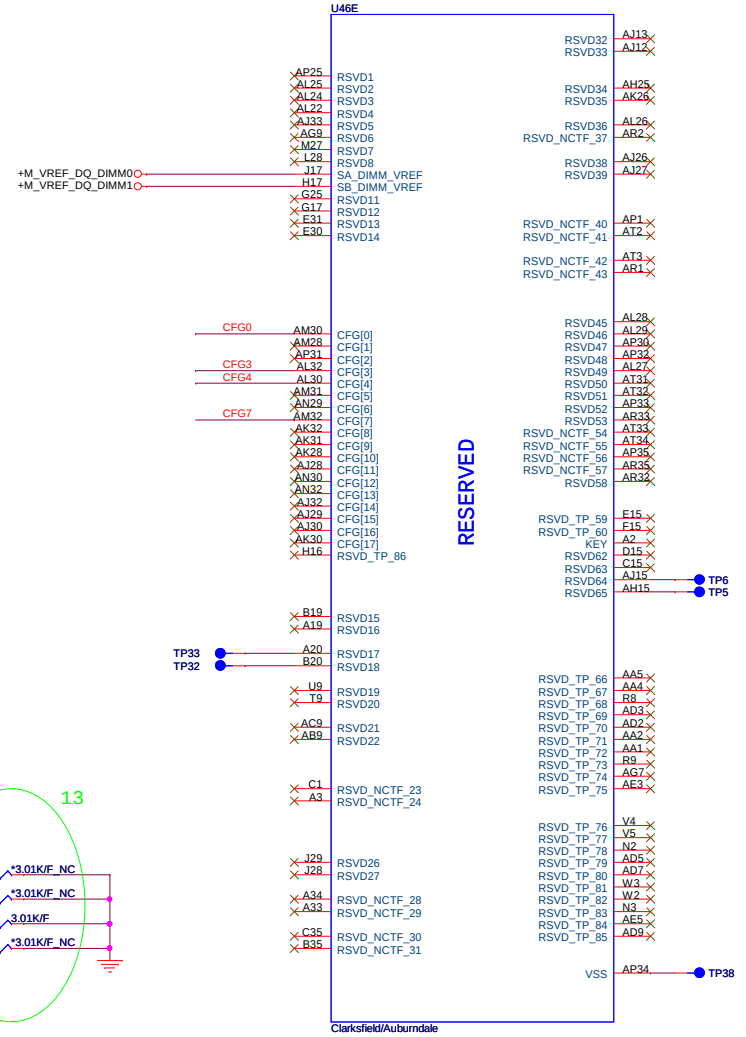
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

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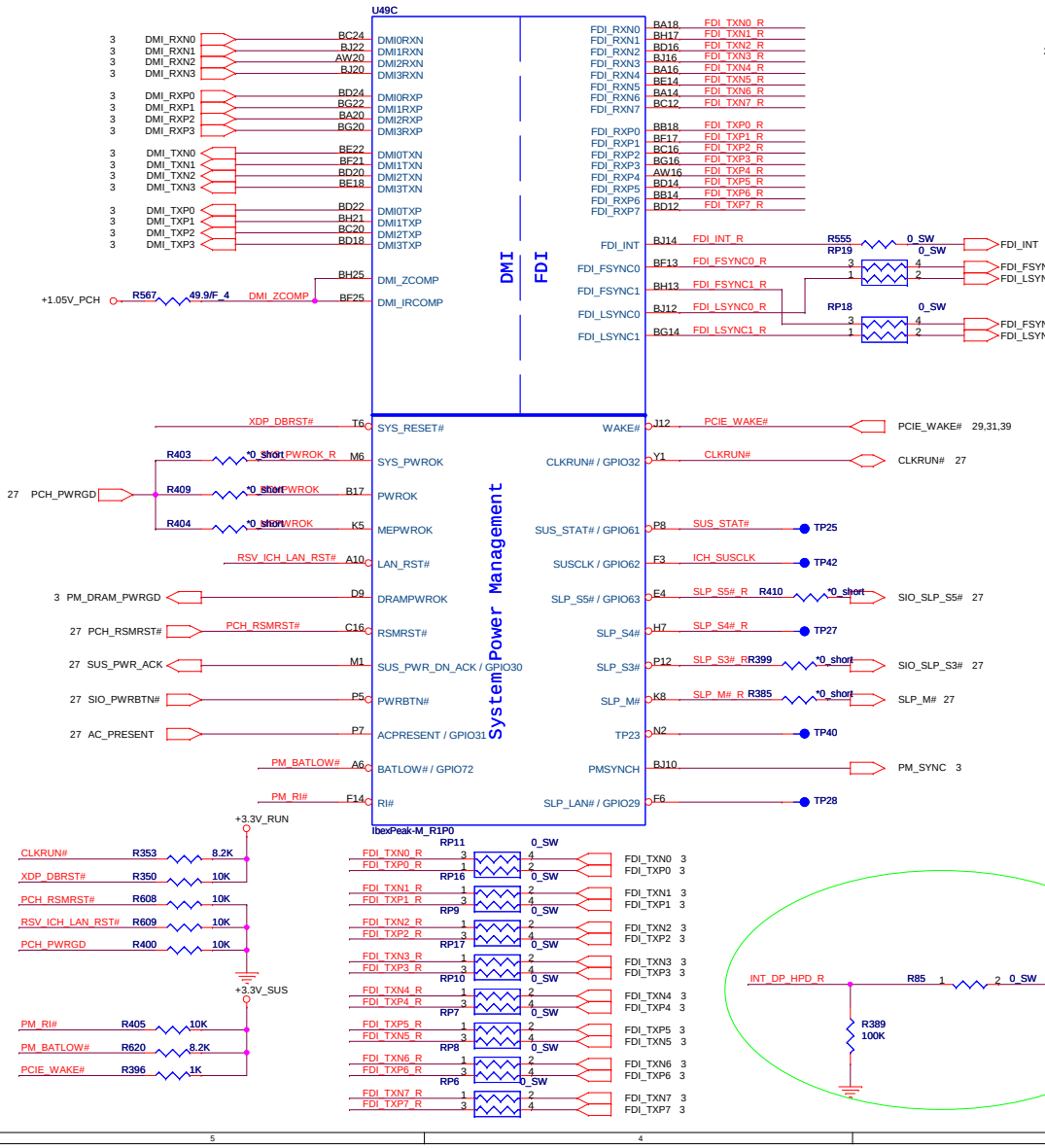
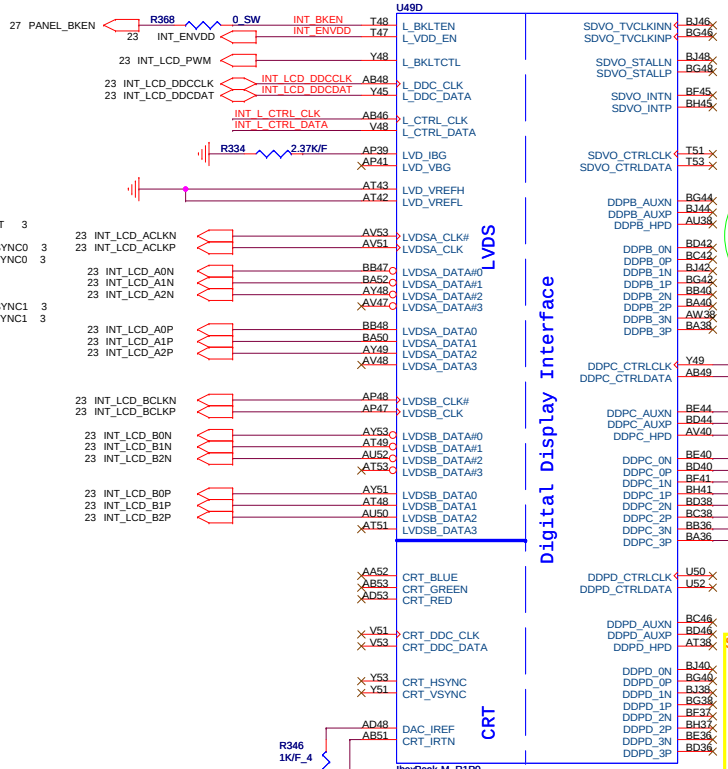
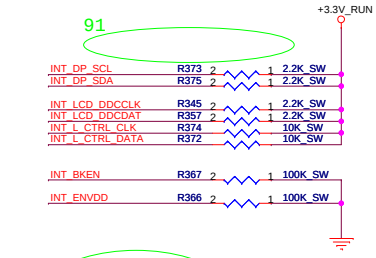
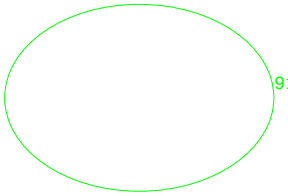
IBEX PEAK-M (DMI,FDI,GPIO)

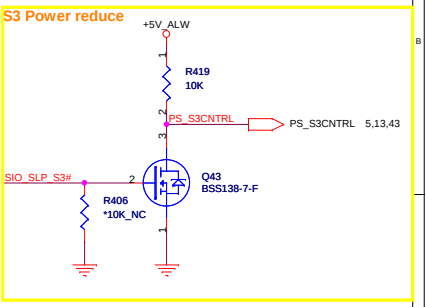


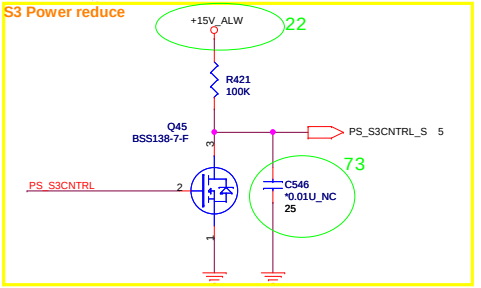
IBEX PEAK-M (LVDS,DDI)











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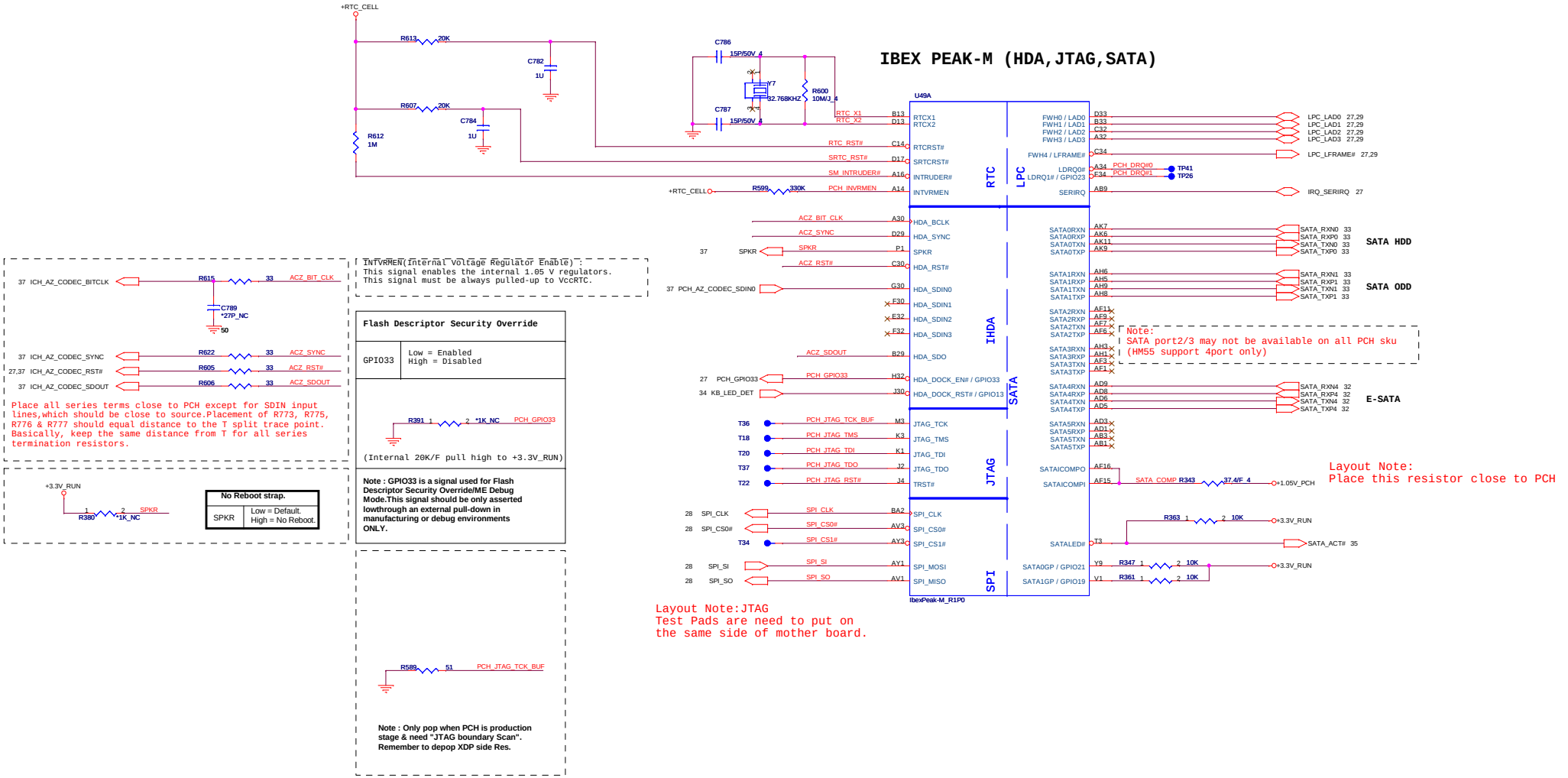
IBEX PEAK-M (HDA,JTAG,SATA)



37 ICH_AZ_CODEC_BITCLK — R615 33 — ACZ_BIT_CLK
C789 *27P_NC 50
37 ICH_AZ_CODEC_SYNC — R622 33 — ACZ_SYNC
27,37 ICH_AZ_CODEC_RST# — R605 33 — ACZ_RST#
37 ICH_AZ_CODEC_SDOUT — R606 33 — ACZ_SDOUT

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

+3.3V_RUN — R380 *1K_NC — SPKR

No Reboot strap.

SPKR	Low = Default. High = No Reboot.

INTVRMEN(Internal Voltage Regulator Enable):
This signal enables the internal 1.05 V regulators.
This signal must be always pulled-up to VccRTC.

Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled

R391 *1K_NC — PCH_GPIO33
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

R589 51 — PCH_JTAG_TCK_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

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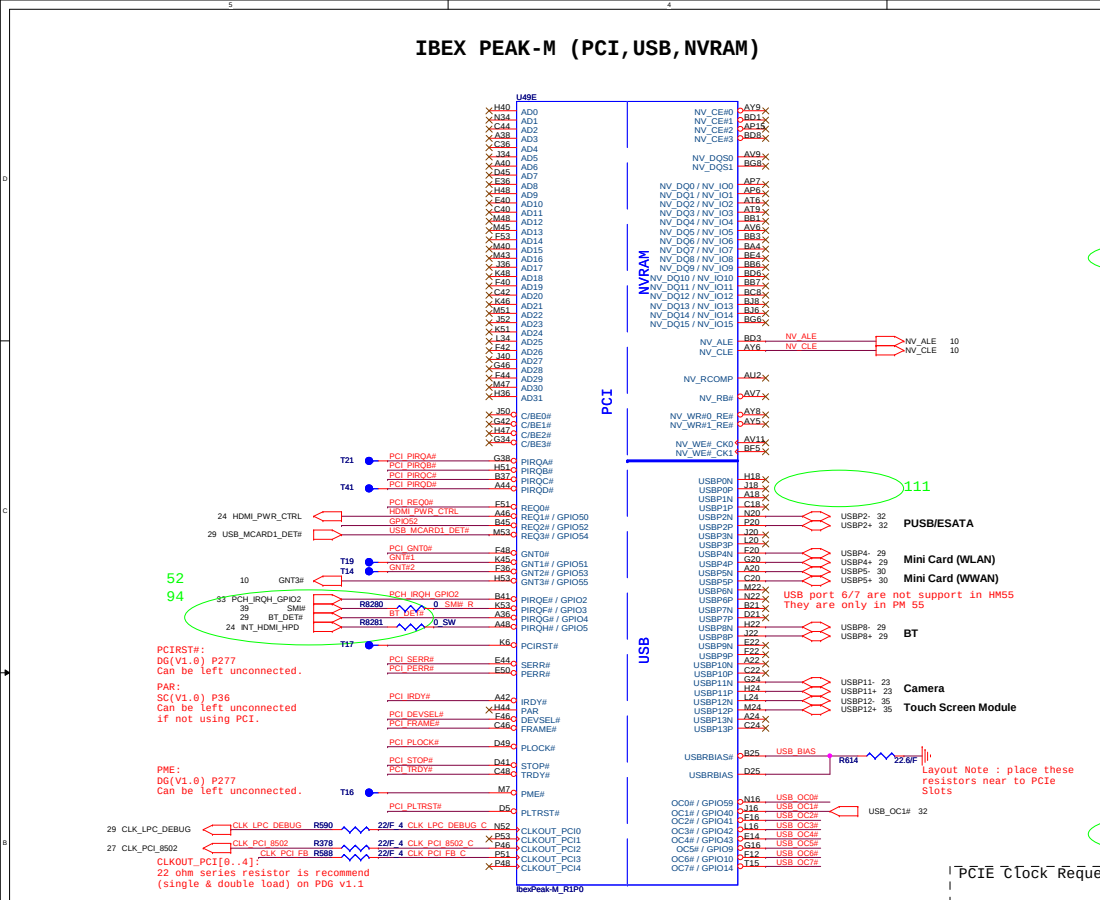
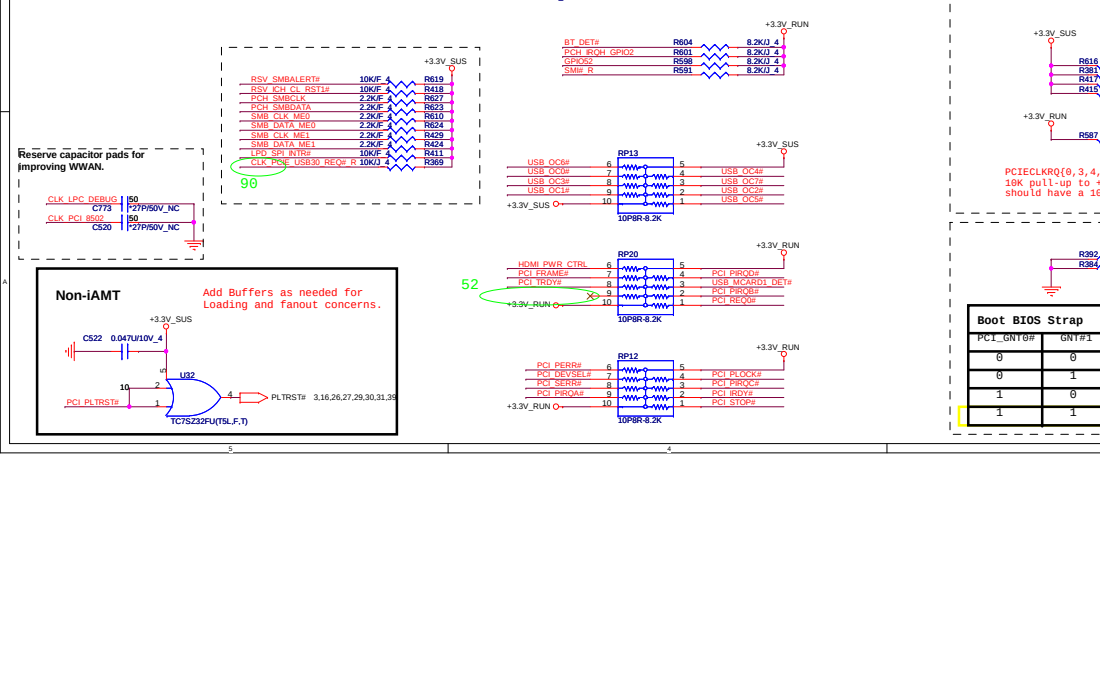
IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (PCI-E,SMBUS,CLK)



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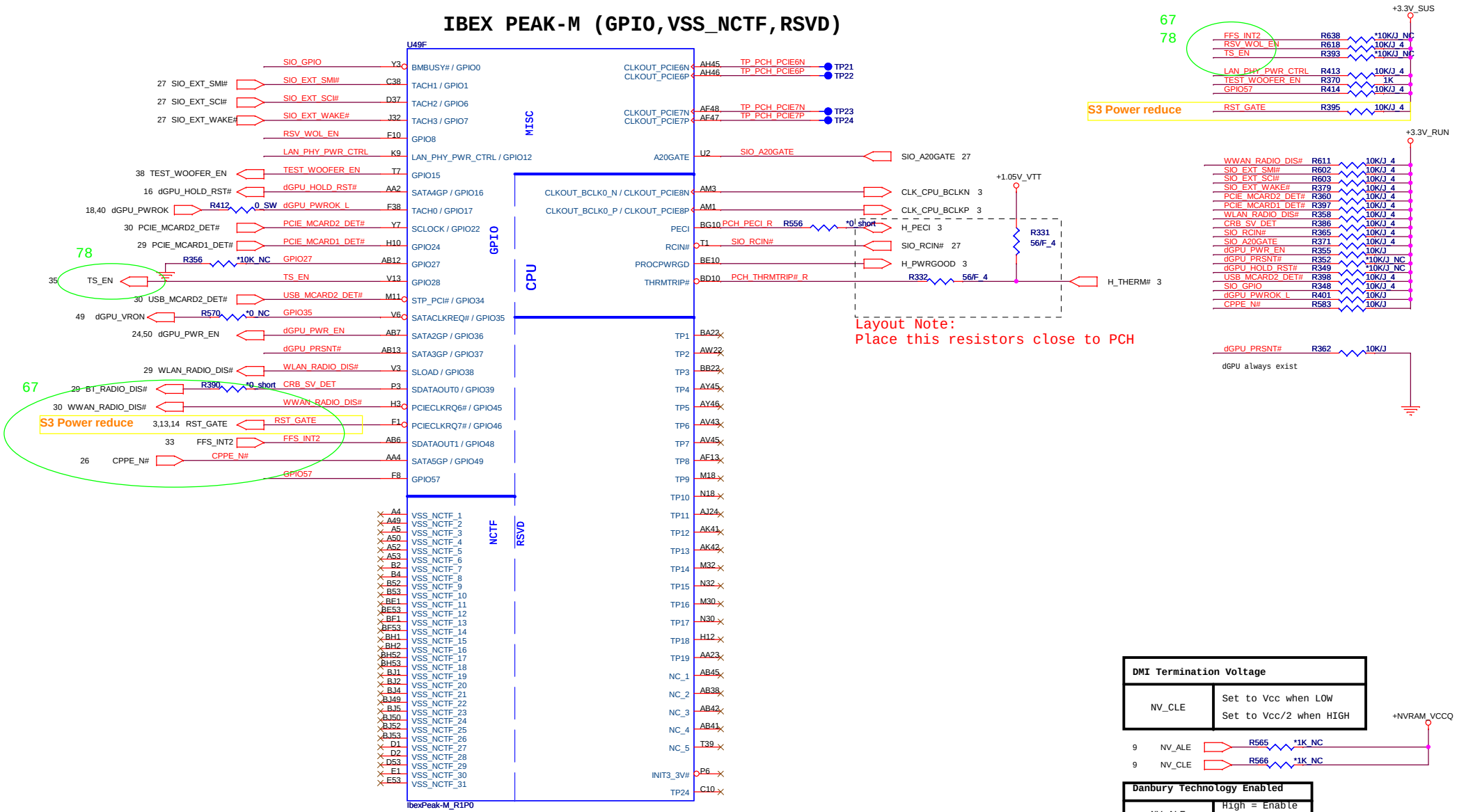
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN	Enable when sampled low Disable when sampled high

SV_SET_UP	1-X High = Strong (Default)

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up
(8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and
100 ohm on this net for validation purpose.

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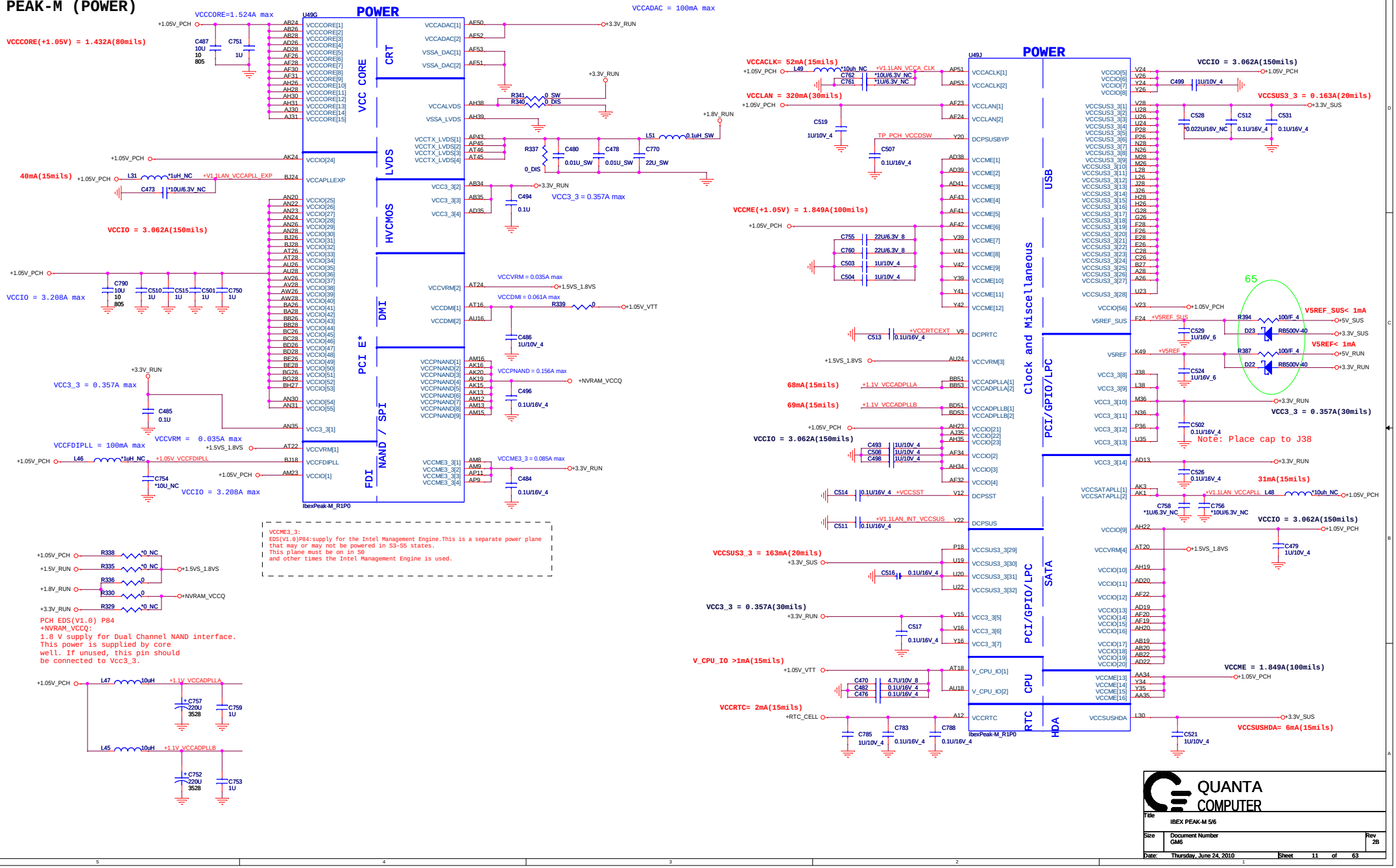
IBEX PEAK-M (POWER)



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Title: IBEX PEAK-M 5/6

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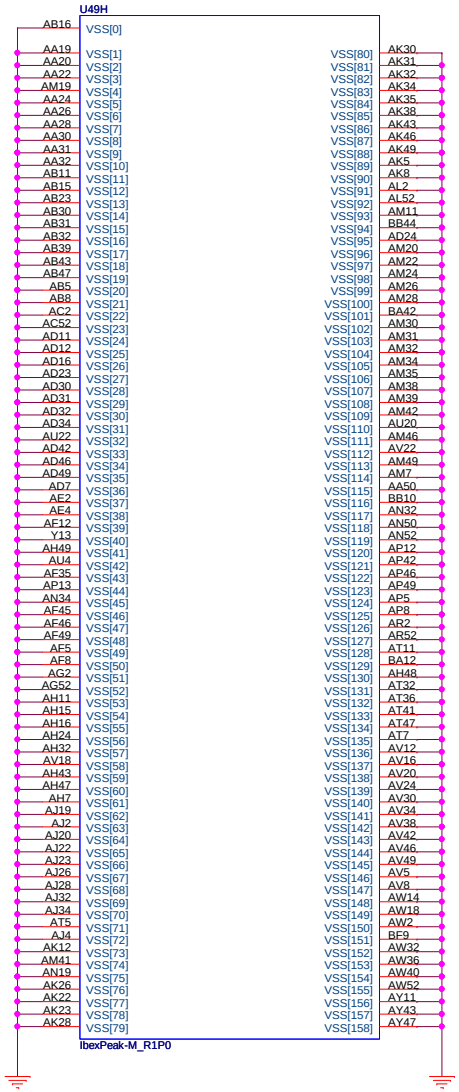
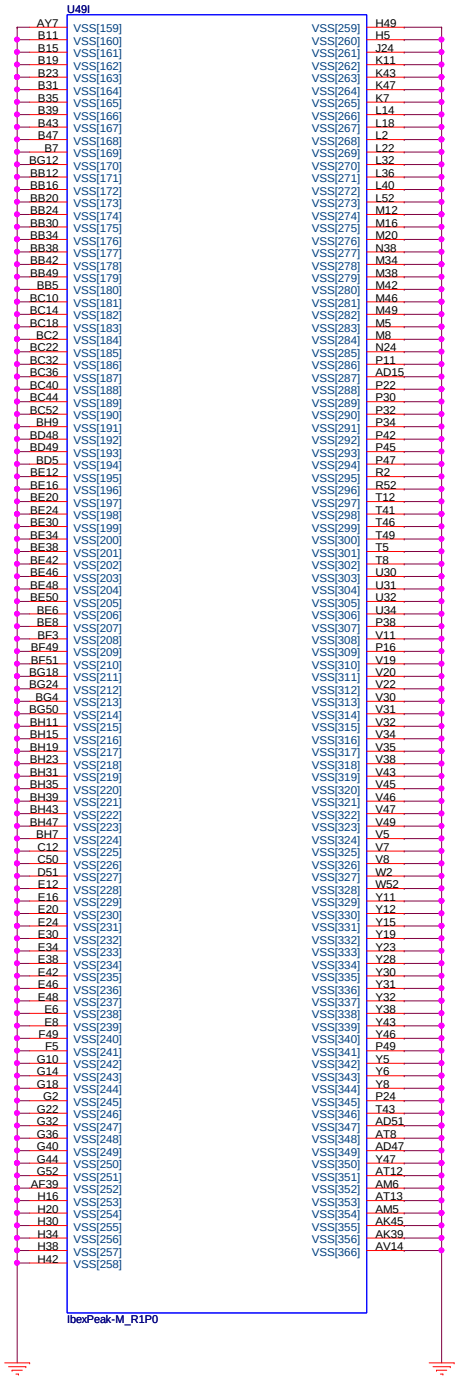
IBEX PEAK-M (GND)





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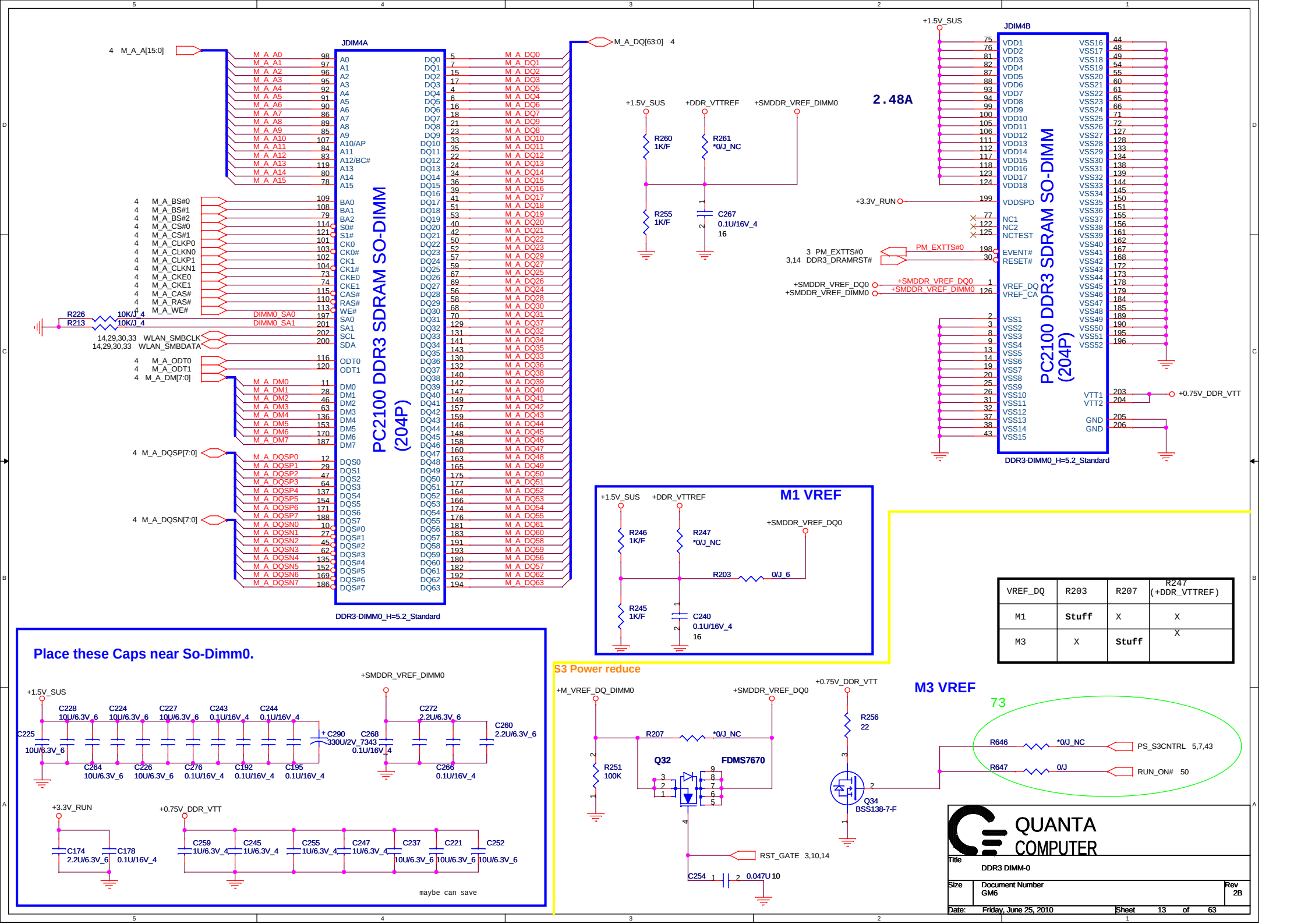

VREF_DQ	R203	R207	R247 (+DDR_VTTREF)
M1	**Stuff**	X	X
M3	X	**Stuff**	X

QUANTA COMPUTER

Title	DDR3 DIMM-0	
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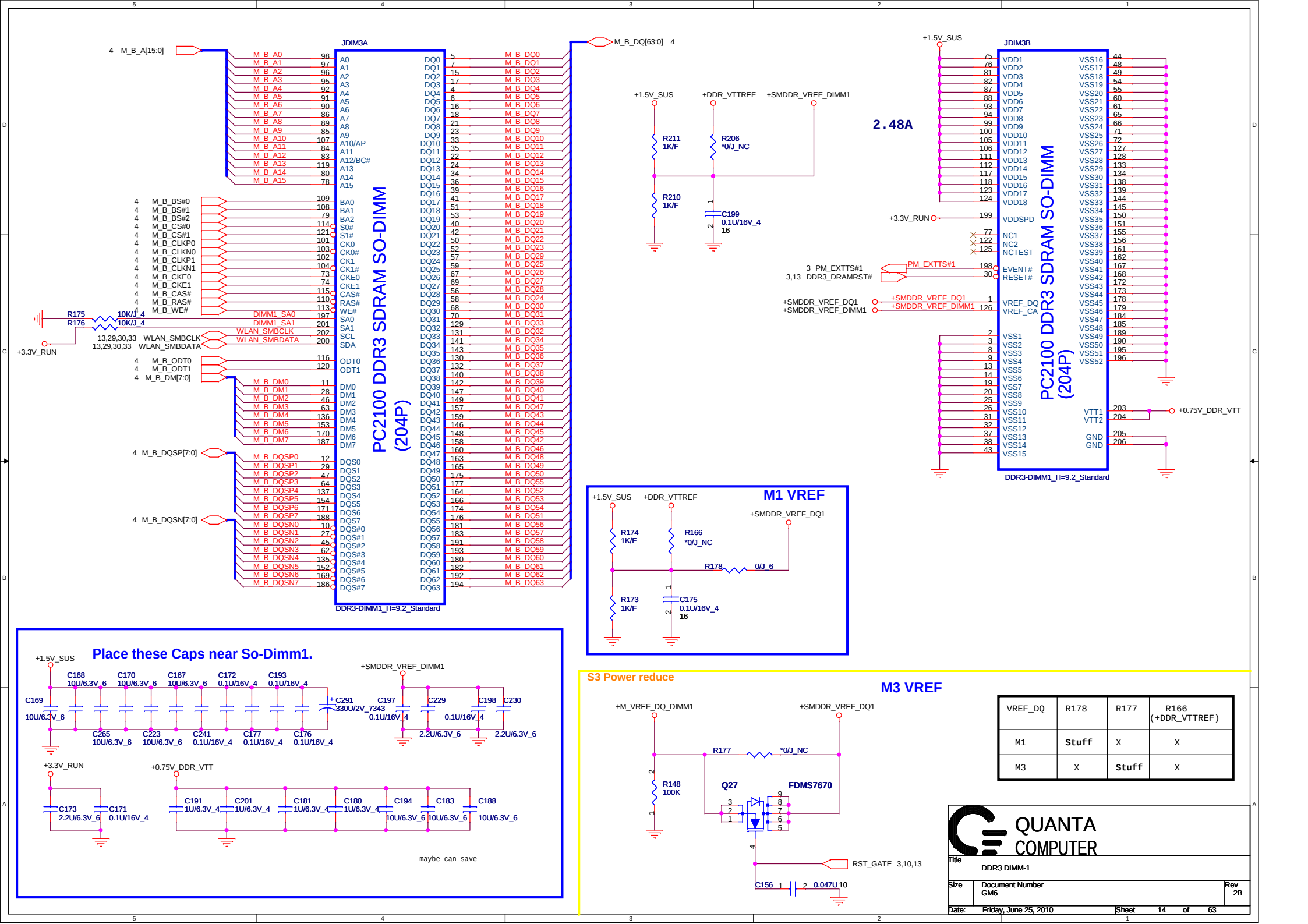
JDIM3A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=9.2_Standard
4 M_B_A[15:0]
M_B_DQ[63:0] 4
4 M_B_BS#0
4 M_B_BS#1
4 M_B_BS#2
4 M_B_CS#0
4 M_B_CS#1
4 M_B_CLKP0
4 M_B_CLKN0
4 M_B_CLKP1
4 M_B_CLKN1
4 M_B_CKE0
4 M_B_CKE1
4 M_B_RAS#
4 M_B_CAS#
4 M_B_WE#
R175 10K/J_4
R176 10K/J_4
+3.3V_RUN
DIMM1_SA0
DIMM1_SA1
13,29,30,33 WLAN_SMBCLK
13,29,30,33 WLAN_SMBDATA
4 M_B_ODT0
4 M_B_ODT1
4 M_B_DM[7:0]
4 M_B_DQSP[7:0]
4 M_B_DQSN[7:0]
+1.5V_SUS
+DDR_VTTREF
+SMDDR_VREF_DIMM1
R211 1K/F
R206 *0/J_NC
R210 1K/F
C199 0.1U/16V_4 16
2.48A
JDIM3B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=9.2_Standard
+3.3V_RUN
3 PM_EXTTS#1
3,13 DDR3_DRAMRST#
PM_EXTTS#1
+SMDDR_VREF_DQ1
+SMDDR_VREF_DIMM1
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDD10
VDD11
VDD12
VDD13
VDD14
VDD15
VDD16
VDD17
VDD18
VDDSPD
NC1
NC2
NCTEST
EVENT#
RESET#
VREF_DQ
VREF_CA
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
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VSS27
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VSS29
VSS30
VSS31
VSS32
VSS33
VSS34
VSS35
VSS36
VSS37
VSS38
VSS39
VSS40
VSS41
VSS42
VSS43
VSS44
VSS45
VSS46
VSS47
VSS48
VSS49
VSS50
VSS51
VSS52
VTT1
VTT2
GND
GND
+0.75V_DDR_VTT
M1 VREF
+1.5V_SUS
+DDR_VTTREF
+SMDDR_VREF_DQ1
R174 1K/F
R166 *0/J_NC
R178 0/J_6
R173 1K/F
C175 0.1U/16V_4 16
Place these Caps near So-Dimm1.
+1.5V_SUS
C168 10U/6.3V_6
C170 10U/6.3V_6
C167 10U/6.3V_6
C172 0.1U/16V_4
C193 0.1U/16V_4
C169 10U/6.3V_6
C265 10U/6.3V_6
C223 10U/6.3V_6
C241 0.1U/16V_4
C177 0.1U/16V_4
C176 0.1U/16V_4
C291 330U/2V_7343
+SMDDR_VREF_DIMM1
C197 0.1U/16V_4
C229 2.2U/6.3V_6
C198 0.1U/16V_4
C230 2.2U/6.3V_6
+3.3V_RUN
C173 2.2U/6.3V_6
C171 0.1U/16V_4
+0.75V_DDR_VTT
C191 1U/6.3V_4
C201 1U/6.3V_4
C181 1U/6.3V_4
C180 1U/6.3V_4
C194 10U/6.3V_6
C183 10U/6.3V_6
C188 10U/6.3V_6
maybe can save
S3 Power reduce
M3 VREF
+M_VREF_DQ_DIMM1
+SMDDR_VREF_DQ1
R177 *0/J_NC
R148 100K
Q27 FDMS7670
RST_GATE 3,10,13
C156 0.047U 10
VREF_DQ | R178 | R177 | R166 (+DDR_VTTREF)
M1 | Stuff | X | X
M3 | X | Stuff | X
QUANTA COMPUTER
Title: DDR3 DIMM-1
Size: Document Number GM6
Rev: 2B
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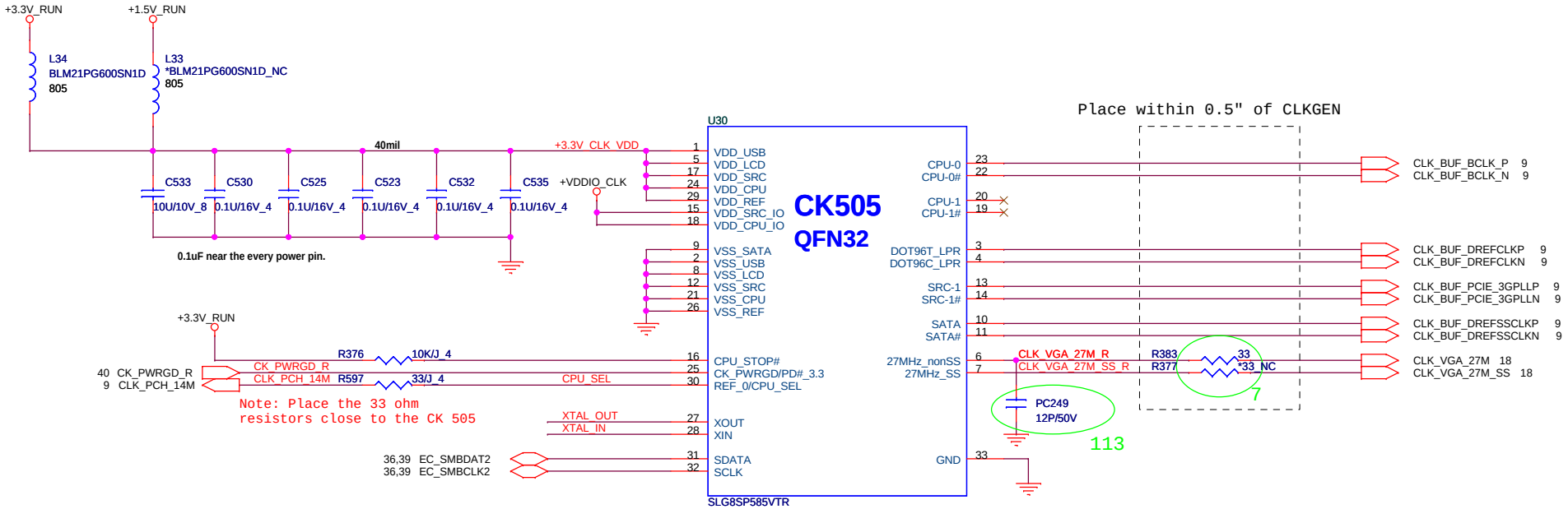
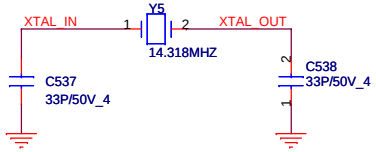
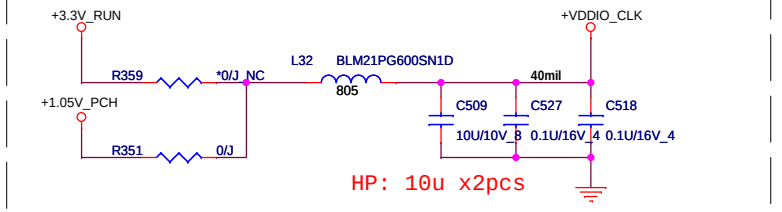


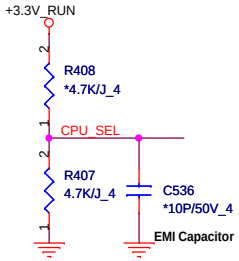
Add capacitor pads for improving WWAN.



Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.



PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

QUANTA COMPUTER

Title	Clock Generator		
Size	Document Number GM6		Rev 2B
Date:	Friday, June 25, 2010	Sheet 15 of 63	

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

0.5A

+1.05V_GFX

20

U44A
fcbga973-nvidia-n11p-es-a1
COMMON

C353 0.1u/10V/X7R
C359 0.1u/10V/X7R
C331 1U/6.3V/X5R
C277 1U/6.3V/X5R
C283 4.7U/6.3V/X5R
C306 10U/6.3V/X5R
C309 22U/6.3V/X5R

AK16 PEX_IOVDD_1
AK17 PEX_IOVDD_2
AK21 PEX_IOVDD_3
AK24 PEX_IOVDD_4
AK27 PEX_IOVDD_5

1.6A

+1.05V_GFX

C295 0.1u/10V/X7R
C355 0.1u/10V/X7R
C358 1U/6.3V/X5R
C318 1U/6.3V/X5R
C347 4.7U/6.3V/X5R
C341 10U/6.3V/X5R
C281 22U/6.3V/X5R

CAP CLOSE TO BGA

AG11 PEX_IOVDDQ_1
AG12 PEX_IOVDDQ_2
AG13 PEX_IOVDDQ_3
AG15 PEX_IOVDDQ_4
AG16 PEX_IOVDDQ_5
AG17 PEX_IOVDDQ_6
AG18 PEX_IOVDDQ_7
AG22 PEX_IOVDDQ_8
AG23 PEX_IOVDDQ_9
AG24 PEX_IOVDDQ_10
AG25 PEX_IOVDDQ_11
AG26 PEX_IOVDDQ_12
AJ14 PEX_IOVDDQ_13
AJ15 PEX_IOVDDQ_14
AJ19 PEX_IOVDDQ_15
AJ21 PEX_IOVDDQ_16
AJ22 PEX_IOVDDQ_17
AJ24 PEX_IOVDDQ_18
AJ25 PEX_IOVDDQ_19
AJ27 PEX_IOVDDQ_20
AK18 PEX_IOVDDQ_21
AK20 PEX_IOVDDQ_22
AK23 PEX_IOVDDQ_23
AK26 PEX_IOVDDQ_24
AL16 PEX_IOVDDQ_25

PCI EXPRESS

+3.3V_GFX

C269 4.7U/6.3V/X5R
C289 1U/6.3V/X5R
C273 0.1u/10V/X7R
C278 0.1u/10V/X7R
C280 0.1u/10V/X7R

J10 VDD33_1
J11 VDD33_2
J12 VDD33_3
J13 VDD33_4
J9 VDD33_5

+VCC_GFX_CORE

AD20 VDD_SENSE
D35 NC_9/ VDD_SENSE
P7 NC_16/ VDD_SENSE

12~16 mils width for 110mA

+1.05V_GFX

24

C287 1U/6.3V/X5R
C288 1U/6.3V/X5R
L30 BLM18AG121SN1D
C298 0.1u/10V/X7R
C286 1U/6.3V/X5R
C310 4.7U/6.3V/X5R
+PEX_PLLVDD

AD19 GND_SENSE
E35 NC_10/ GND_SENSE
R7 NC_17/ GND_SENSE
AG14 PEX_PLLVDD

12~16 mils width

+3.3V_GFX

L27 0 +PEX_SVDD_3V3

C239 1U/6.3V/X5R
C246 0.1u/10V/X7R
C219 4.7U/6.3V/X5R

AG19 PEX_CAL_PD_VDDQ/ PEX_SVDD_3V3
F7 NC_12/ PEX_SVDD_3V3

AG20 PEX_CAL_PU_GND/ NC
A2 NC_1
AB7 NC_2
AD6 NC_3
AE6 NC_4
AG6 NC_5
AJ5 NC_6
AK15 NC_7
AL7 NC_8
E7 NC_11
H32 NC_13
M7 NC_14
P6 NC_15
U7 NC_18
V6 NC_19

PEX_RX0 AP17 PEG_TXP15 3
PEX_RX0* AN17 PEG_TXN15 3
PEX_RX1 AN19 PEG_TXP14 3
PEX_RX1* AP19 PEG_TXN14 3
PEX_RX2 AR19 PEG_TXP13 3
PEX_RX2* AR20 PEG_TXN13 3
PEX_RX3 AP20 PEG_TXP12 3
PEX_RX3* AN20 PEG_TXN12 3
PEX_RX4 AN22 PEG_TXP11 3
PEX_RX4* AP22 PEG_TXN11 3
PEX_RX5 AR22 PEG_TXP10 3
PEX_RX5* AR23 PEG_TXN10 3
PEX_RX6 AP23 PEG_TXP9 3
PEX_RX6* AN23 PEG_TXN9 3
PEX_RX7 AN25 PEG_TXP8 3
PEX_RX7* AP25 PEG_TXN8 3
PEX_RX8 AR25 PEG_TXP7 3
PEX_RX8* AR26 PEG_TXN7 3
PEX_RX9 AP26 PEG_TXP6 3
PEX_RX9* AN26 PEG_TXN6 3
PEX_RX10 AN28 PEG_TXP5 3
PEX_RX10* AP28 PEG_TXN5 3
PEX_RX11 AR28 PEG_TXP4 3
PEX_RX11* AR29 PEG_TXN4 3
PEX_RX12 AP29 PEG_TXP3 3
PEX_RX12* AN29 PEG_TXN3 3
PEX_RX13 AN31 PEG_TXP2 3
PEX_RX13* AP31 PEG_TXN2 3
PEX_RX14 AR31 PEG_TXP1 3
PEX_RX14* AR32 PEG_TXN1 3
PEX_RX15 AR34 PEG_TXP0 3
PEX_RX15* AP34 PEG_TXN0 3

PEX_TX0 AL17 PEG_RXP15_C C332 0.1u/10V/X7R PEG_RXP15 3
PEX_TX0* AM17 PEG_RXN15_C C324 0.1u/10V/X7R PEG_RXN15 3
PEX_TX1 AM18 PEG_RXP14_C C292 0.1u/10V/X7R PEG_RXP14 3
PEX_TX1* AM19 PEG_RXN14_C C300 0.1u/10V/X7R PEG_RXN14 3
PEX_TX2 AL19 PEG_RXP13_C C302 0.1u/10V/X7R PEG_RXP13 3
PEX_TX2* AK19 PEG_RXN13_C C311 0.1u/10V/X7R PEG_RXN13 3
PEX_TX3 AL20 PEG_RXP12_C C312 0.1u/10V/X7R PEG_RXP12 3
PEX_TX3* AM20 PEG_RXN12_C C323 0.1u/10V/X7R PEG_RXN12 3
PEX_TX4 AM21 PEG_RXP11_C C327 0.1u/10V/X7R PEG_RXP11 3
PEX_TX4* AM22 PEG_RXN11_C C334 0.1u/10V/X7R PEG_RXN11 3
PEX_TX5 AL22 PEG_RXP10_C C346 0.1u/10V/X7R PEG_RXP10 3
PEX_TX5* AK22 PEG_RXN10_C C356 0.1u/10V/X7R PEG_RXN10 3
PEX_TX6 AL23 PEG_RXP9_C C354 0.1u/10V/X7R PEG_RXP9 3
PEX_TX6* AM23 PEG_RXN9_C C345 0.1u/10V/X7R PEG_RXN9 3
PEX_TX7 AM24 PEG_RXP8_C C340 0.1u/10V/X7R PEG_RXP8 3
PEX_TX7* AM25 PEG_RXN8_C C344 0.1u/10V/X7R PEG_RXN8 3
PEX_TX8 AL25 PEG_RXP7_C C357 0.1u/10V/X7R PEG_RXP7 3
PEX_TX8* AK25 PEG_RXN7_C C364 0.1u/10V/X7R PEG_RXN7 3
PEX_TX9 AL26 PEG_RXP6_C C366 0.1u/10V/X7R PEG_RXP6 3
PEX_TX9* AM26 PEG_RXN6_C C374 0.1u/10V/X7R PEG_RXN6 3
PEX_TX10 AM27 PEG_RXP5_C C376 0.1u/10V/X7R PEG_RXP5 3
PEX_TX10* AM28 PEG_RXN5_C C377 0.1u/10V/X7R PEG_RXN5 3
PEX_TX11 AL28 PEG_RXP4_C C378 0.1u/10V/X7R PEG_RXP4 3
PEX_TX11* AK28 PEG_RXN4_C C379 0.1u/10V/X7R PEG_RXN4 3
PEX_TX12 AK29 PEG_RXP3_C C380 0.1u/10V/X7R PEG_RXP3 3
PEX_TX12* AL29 PEG_RXN3_C C381 0.1u/10V/X7R PEG_RXN3 3
PEX_TX13 AM29 PEG_RXP2_C C382 0.1u/10V/X7R PEG_RXP2 3
PEX_TX13* AM30 PEG_RXN2_C C383 0.1u/10V/X7R PEG_RXN2 3
PEX_TX14 AM31 PEG_RXP1_C C384 0.1u/10V/X7R PEG_RXP1 3
PEX_TX14* AM32 PEG_RXN1_C C386 0.1u/10V/X7R PEG_RXN1 3
PEX_TX15 AN32 PEG_RXP0_C C389 0.1u/10V/X7R PEG_RXP0 3
PEX_TX15* AP32 PEG_RXN0_C C385 0.1u/10V/X7R PEG_RXN0 3

PEX_REFCLK AR16 CLK_PCIE_VGAP 9
PEX_REFCLK* AR17 CLK_PCIE_VGAN 9

PEX_TSTCLK_OUT AJ17 PEX_TSTCLK R275 *200_NC
PEX_TSTCLK_OUT* AJ18 PEX_TSTCLK#

PEX_RST* AM16 VGA_RST# R500 0 GPU_RST#

PEX_CLKREQ* AR13 PEX_CLKREQ# R501 10K +3.3V_GFX

PEX_TERMP AG21 PEX_TERMP R287 2.49K/F

TESTMODE AP35 TESTMODE R518 10K
R517 *10K/F_NC +3.3V_GFX

R499 1 2 100K

R497 *0_NC

+3.3V_GFX
C646 0.1u

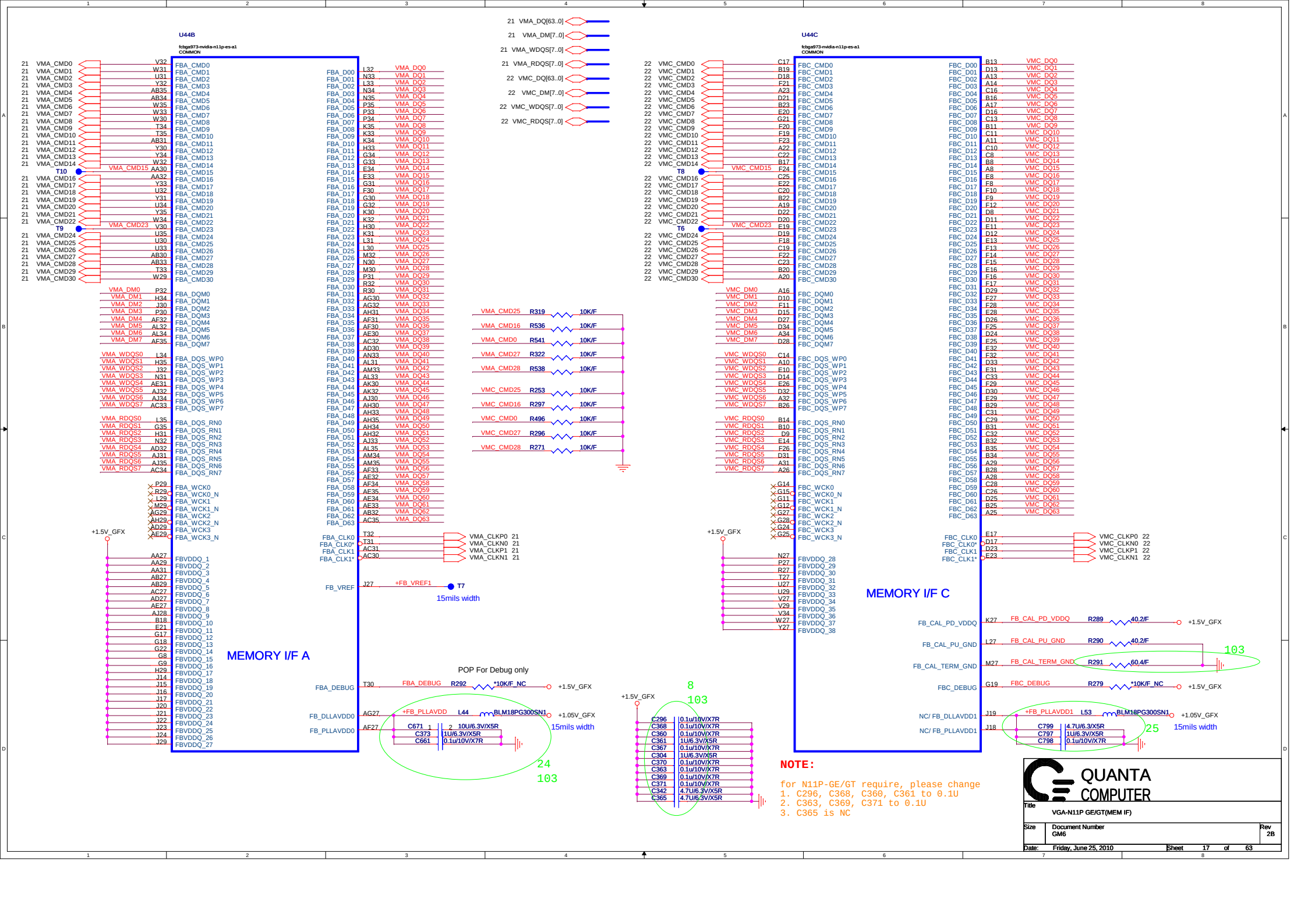
GPU_RST# 4
1 PLTRST# 3,9,26,27,29,30,31,39
2 dGPU_HOLD_RST# 10
3
5
U42
TC7SH08FU

R494
100K

+3.3V_GFX
R511
10K
R512 10K +3.3V_SUS
PEG_CLKREQ# 9
Q71
DTC144EUA
PEX_CLKREQ# 2
Q70
DTC144EUA

QUANTA COMPUTER

Title	VGA-N11P GE/GE(PCIe)	
Size	Document Number GM6	Rev 2B
Date: Friday, June 25, 2010	Sheet 16 of 63	


U44B
fcbga973-nvidia-n11p-es-a1
COMMON
MEMORY I/F A
U44C
fcbga973-nvidia-n11p-es-a1
COMMON
MEMORY I/F C
POP For Debug only
NOTE:
for N11P-GE/GT require, please change
1. C296, C368, C360, C361 to 0.1U
2. C363, C369, C371 to 0.1U
3. C365 is NC
QUANTA COMPUTER
Title
VGA-N11P GE/GT(MEM IF)
Size
Document Number
GM6
Rev
2B
Date: Friday, June 25, 2010
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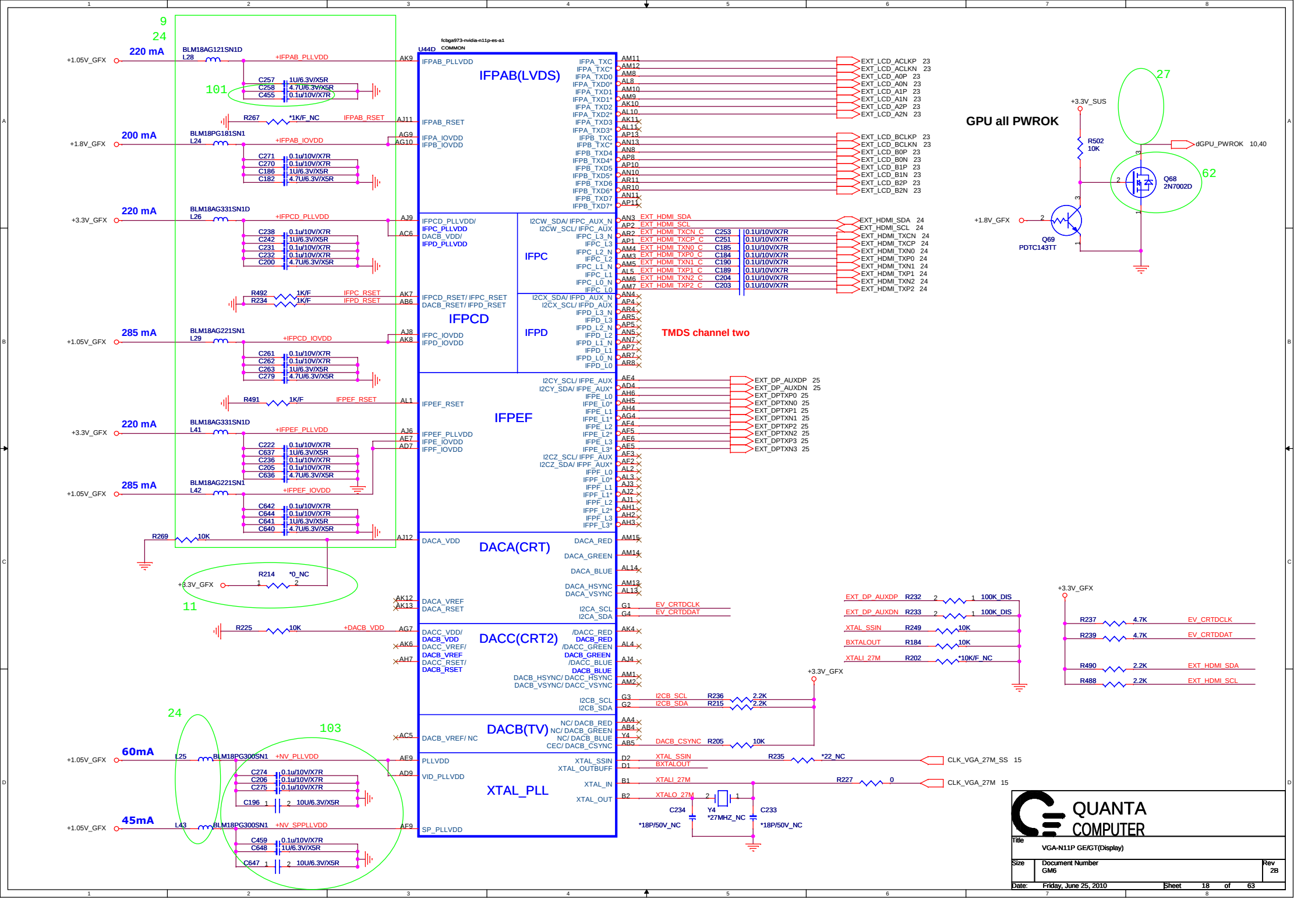
fcbga973-nvidia-n11p-es-a1
U44D COMMON
IFPAB(LVDS)
IFPCD
IFPC
IFPD
IFPEF
DACA(CRT)
DACC(CRT2)
DACB(TV)
XTAL_PLL
TMDS channel two
GPU all PWROK
+1.05V_GFX
+1.8V_GFX
+3.3V_GFX
+3.3V_SUS
220 mA
200 mA
285 mA
60mA
45mA
BLM18AG121SN1D
BLM18PG181SN1
BLM18AG331SN1D
BLM18AG221SN1
BLM18PG300SN1
Q68 2N7002D
Q69 PDTC143TT
R502 10K
dGPU_PWROK 10,40
EXT_LCD_ACLKP 23
EXT_LCD_ACLKN 23
EXT_LCD_A0P 23
EXT_LCD_A0N 23
EXT_LCD_A1P 23
EXT_LCD_A1N 23
EXT_LCD_A2P 23
EXT_LCD_A2N 23
EXT_LCD_BCLKP 23
EXT_LCD_BCLKN 23
EXT_LCD_B0P 23
EXT_LCD_B0N 23
EXT_LCD_B1P 23
EXT_LCD_B1N 23
EXT_LCD_B2P 23
EXT_LCD_B2N 23
EXT_HDMI_SDA 24
EXT_HDMI_SCL 24
EXT_HDMI_TXCN 24
EXT_HDMI_TXCP 24
EXT_HDMI_TXN0 24
EXT_HDMI_TXP0 24
EXT_HDMI_TXN1 24
EXT_HDMI_TXP1 24
EXT_HDMI_TXN2 24
EXT_HDMI_TXP2 24
EXT_DP_AUXDP 25
EXT_DP_AUXDN 25
EXT_DPTXP0 25
EXT_DPTXN0 25
EXT_DPTXP1 25
EXT_DPTXN1 25
EXT_DPTXP2 25
EXT_DPTXN2 25
EXT_DPTXP3 25
EXT_DPTXN3 25
EV_CRTDCLK
EV_CRTDDAT
CLK_VGA_27M_SS 15
CLK_VGA_27M 15
XTALO_27M
C234 *18P/50V_NC
Y4 *27MHZ_NC
C233 *18P/50V_NC
QUANTA COMPUTER
Title VGA-N11P GE/GT(Display)
Size Document Number GM6 Rev 2B
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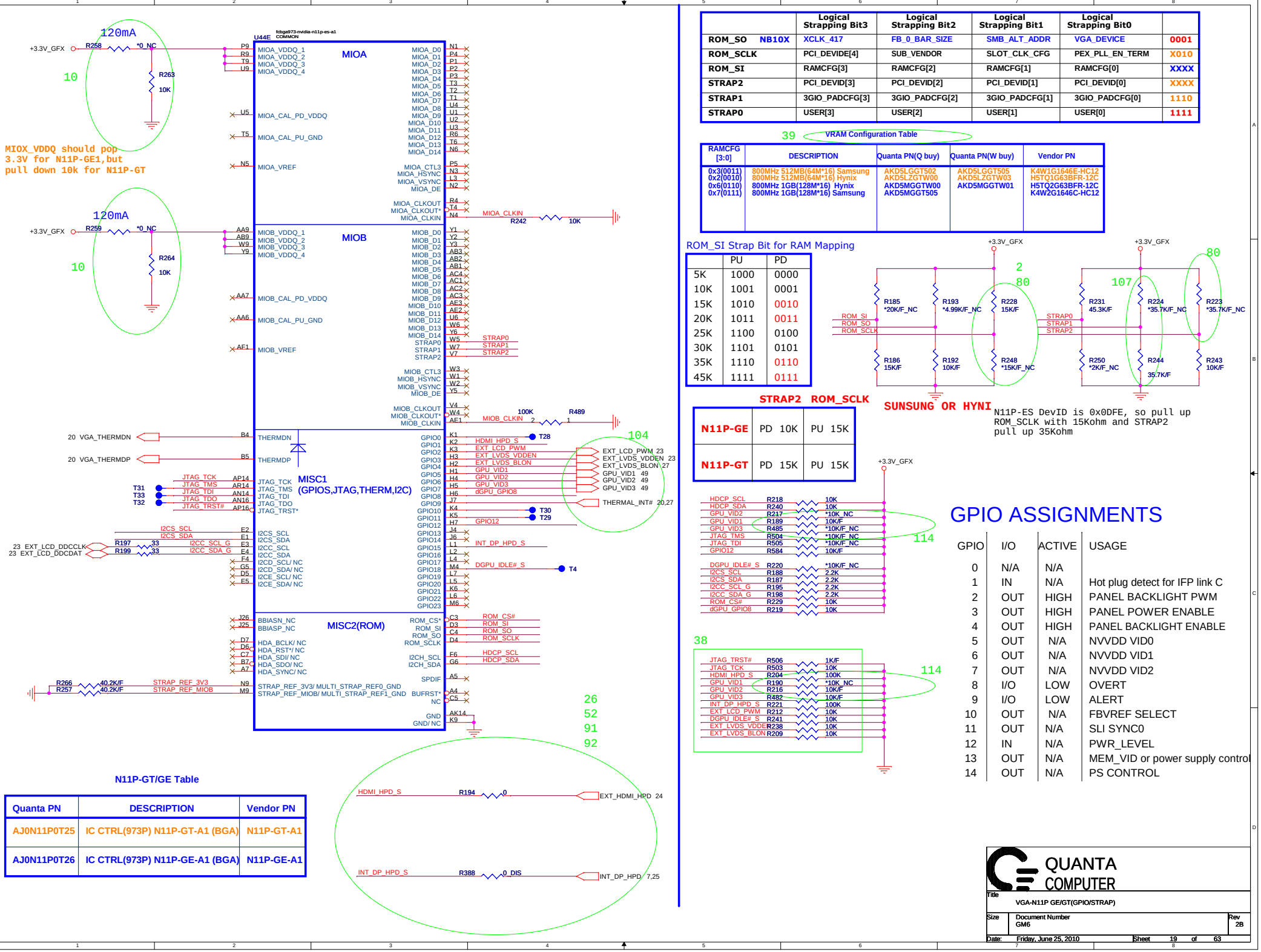


N11P-GT/GE Table

Quanta PN	DESCRIPTION	Vendor PN
AJ0N11P0T25	IC CTRL(973P) N11P-GT-A1 (BGA)	N11P-GT-A1
AJ0N11P0T26	IC CTRL(973P) N11P-GE-A1 (BGA)	N11P-GE-A1

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

39 VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	800MHz 512MB(64M*16) Samsung	AKD5LGGT502	AKD5LGGT505	K4W1G1646E-HC12
0x2(0010)	800MHz 512MB(64M*16) Hynix	AKD5LZGTW00	AKD5LZGTW03	H5TQ1G63BFR-12C
0x6(0110)	800MHz 1GB(128M*16) Hynix	AKD5MGGTW00	AKD5MGGTW01	H5TQ2G63BFR-12C
0x7(0111)	800MHz 1GB(128M*16) Samsung	AKD5MGGT505		K4W2G1646C-HC12

ROM_SI Strap Bit for RAM Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	STRAP2 ROM_SCLK	
N11P-GE	PD 10K	PU 15K
N11P-GT	PD 15K	PU 15K

SUNSUNG OR HYNI

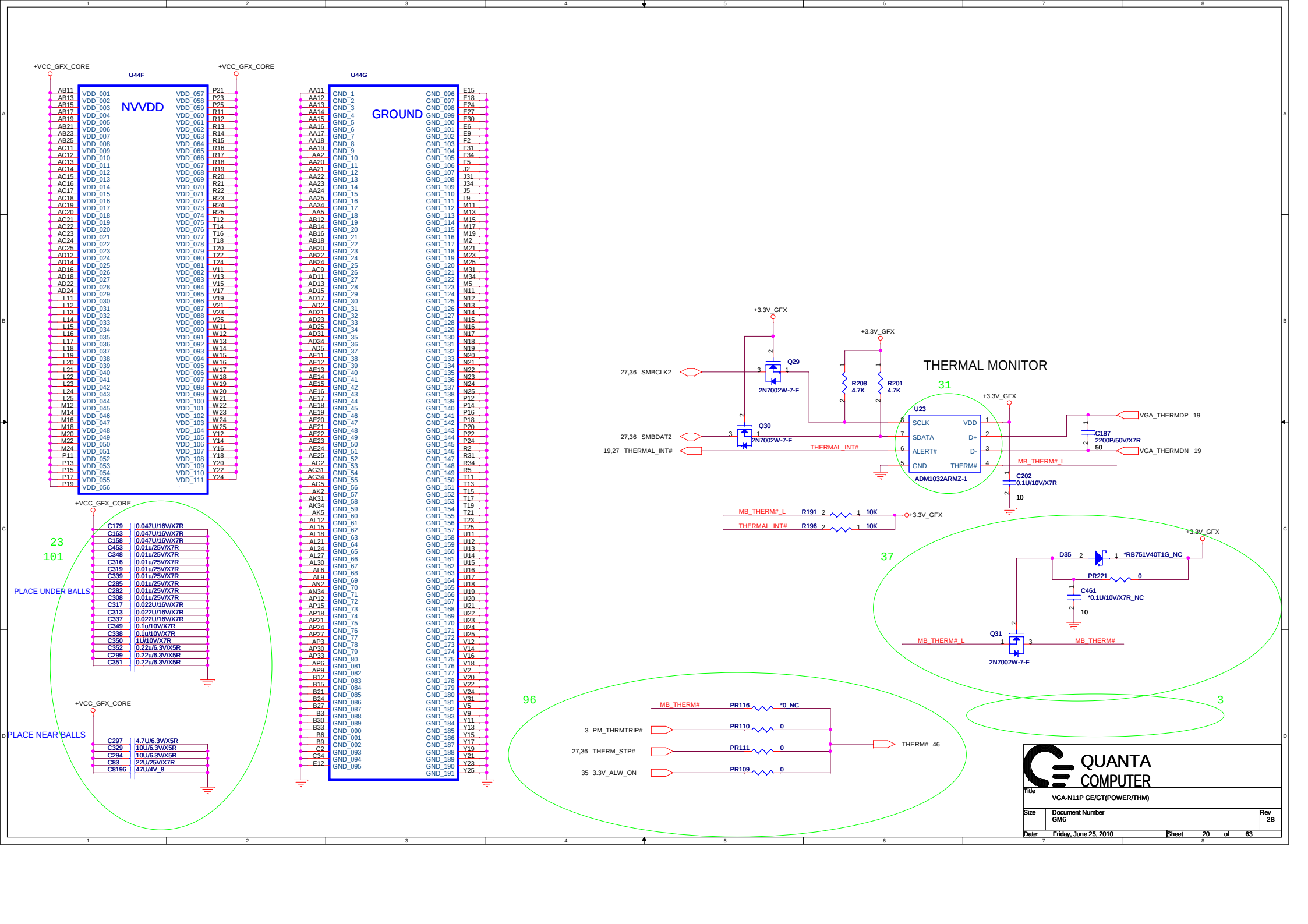
N11P-ES DevID is 0x0DFE, so pull up ROM_SCLK with 15Kohm and STRAP2 pull up 35Kohm

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

QUANTA COMPUTER

Title	VGA-N11P GE/GT(GPIO/STRAP)	
Size	Document Number GM6	Rev 2B
Date: Friday, June 25, 2010	Sheet 19 of 63	


U44F
NVVDD
U44G
GROUND
+VCC_GFX_CORE
+3.3V_GFX
THERMAL MONITOR
U23
ADM1032ARMZ-1
Q29
Q30
Q31
2N7002W-7-F
R208 4.7K
R201 4.7K
R191 10K
R196 10K
C187 2200P/50V/X7R
C202 0.1U/10V/X7R
PR221 0
C461 *0.1U/10V/X7R_NC
D35 *RB751V40T1G_NC
PR116 *0_NC
PR110 0
PR111 0
PR109 0
PLACE UNDER BALLS
PLACE NEAR BALLS
23
101
31
37
96
3
QUANTA COMPUTER
VGA-N11P GE/GT(POWER/THM)
Document Number GM6
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CHANNEL A: 512MB/1024MB DDR3

17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

U27 / U48 / U28 / U47 — 96-BALL SDRAM DDR3 H5TQ1G63BFR-12C

Should be 240 Ohms +-1%

R301 240/F
R540 240/F
R321 240/F
R523 240/F

39

R539 4.99K/F
R524 4.99K/F
C399 0.1U/10V/X7R 10
R318 4.99K/F
R525 4.99K/F
C441 0.1U/10V/X7R 10
C743 *10u/6.3V/X5R_NC
R537 4.99K/F
R302 4.99K/F
C446 0.1U/10V/X7R 10
R534 4.99K/F
R303 4.99K/F
C447 0.1U/10V/X7R 10

80

Placement has to be close to VRAM

R320 162/F
R535 162/F

C439 C437 C710 C741 C724 1U/6.3V/X5R
C742 C732 C449 C707 C429 0.1u/10V/X5R
C706 C423 C450 C438 C719 1U/6.3V/X5R
C434 C699 C711 C443 C698 0.1u/10V/X5R
C734 C723 C731 C422 C727 1U/6.3V/X5R
C736 C738 C740 C687 C445 0.1u/10V/X5R
C424 C435 C440 C718 C693 1U/6.3V/X5R
C442 C448 C428 C735 C728 0.1u/10V/X5R

GE1 FOR 243 BUT GT/E REQUIRE CHECK FAE

QUANTA COMPUTER

Title	VGA-N11P GE/GT(VRAM-1)		
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CHANNEL B: 512MB/1024MB DDR3

17 VMC_DQ[63..0]
17 VMC_DM[7..0]
17 VMC_WDQS[7..0]
17 VMC_RDQS[7..0]

U24 / U43 / U26 / U45

96-BALL SDRAM DDR3
H5TQ1G63BFR-12C

Should be 240 Ohms +-1%

R270 240/F
R498 240/F
R294 240/F
R515 240/F

39

80

15 mil width and <500 mil

R265 4.99K/F
R507 4.99K/F
C284 0.1U/10V/X7R 10
R252 4.99K/F
R495 4.99K/F
C649 0.1U/10V/X7R 10
C701 *10u/6.3V/X5R_NC
R293 4.99K/F
R514 4.99K/F
C375 0.1U/10V/X7R 10
R299 4.99K/F
R298 4.99K/F
C372 0.1U/10V/X7R 10

Placement has to be close to VRAM

R254 162/F
R295 162/F

C249 C639 C737 C654 C336 1U/6.3V/X5R
C664 C248 C250 C362 C218 0.1u/10V/X5R
C645 C444 C739 C217 C216 1U/6.3V/X5R
C335 C208 C405 C305 C207 0.1u/10V/X5R
C656 C653 C214 C387 C391 1U/6.3V/X5R
C210 C256 C400 C390 C416 0.1u/10V/X5R
C215 C212 C213 C401 C638 1U/6.3V/X5R
C211 C650 C643 C209 C677 0.1u/10V/X5R

QUANTA COMPUTER

Title	VGA-N11P GE/GT(VRAM-2)	
Size	Document Number GM6	Rev 2B
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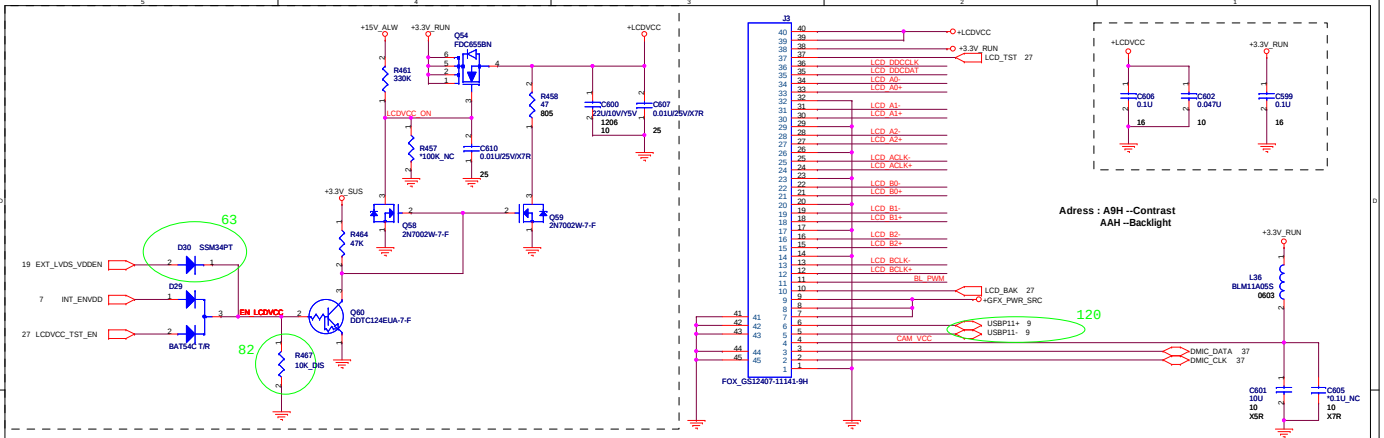
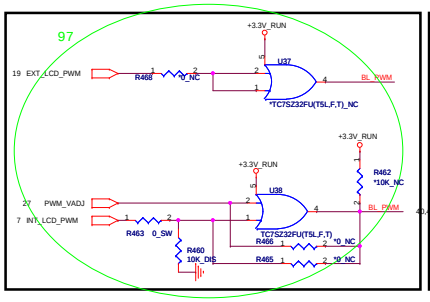
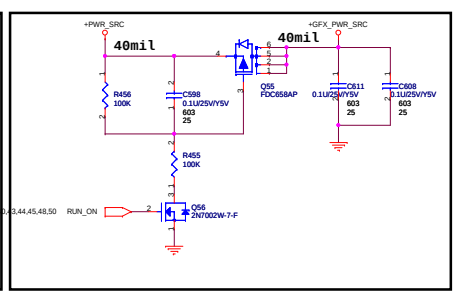
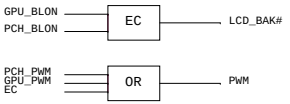


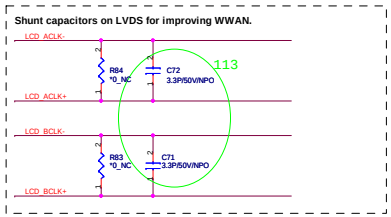
Adress : A9H --Contrast
AAH --Backlight

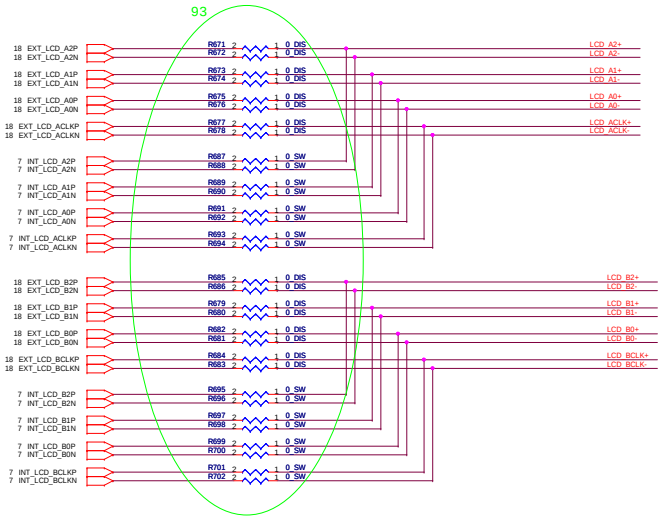
120

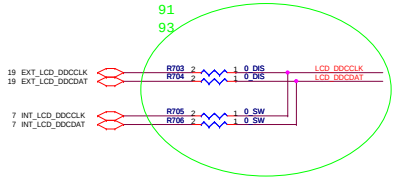


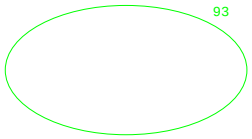


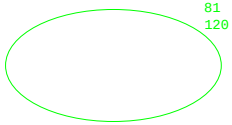












QUANTA COMPUTER

Title	LCD CONN	
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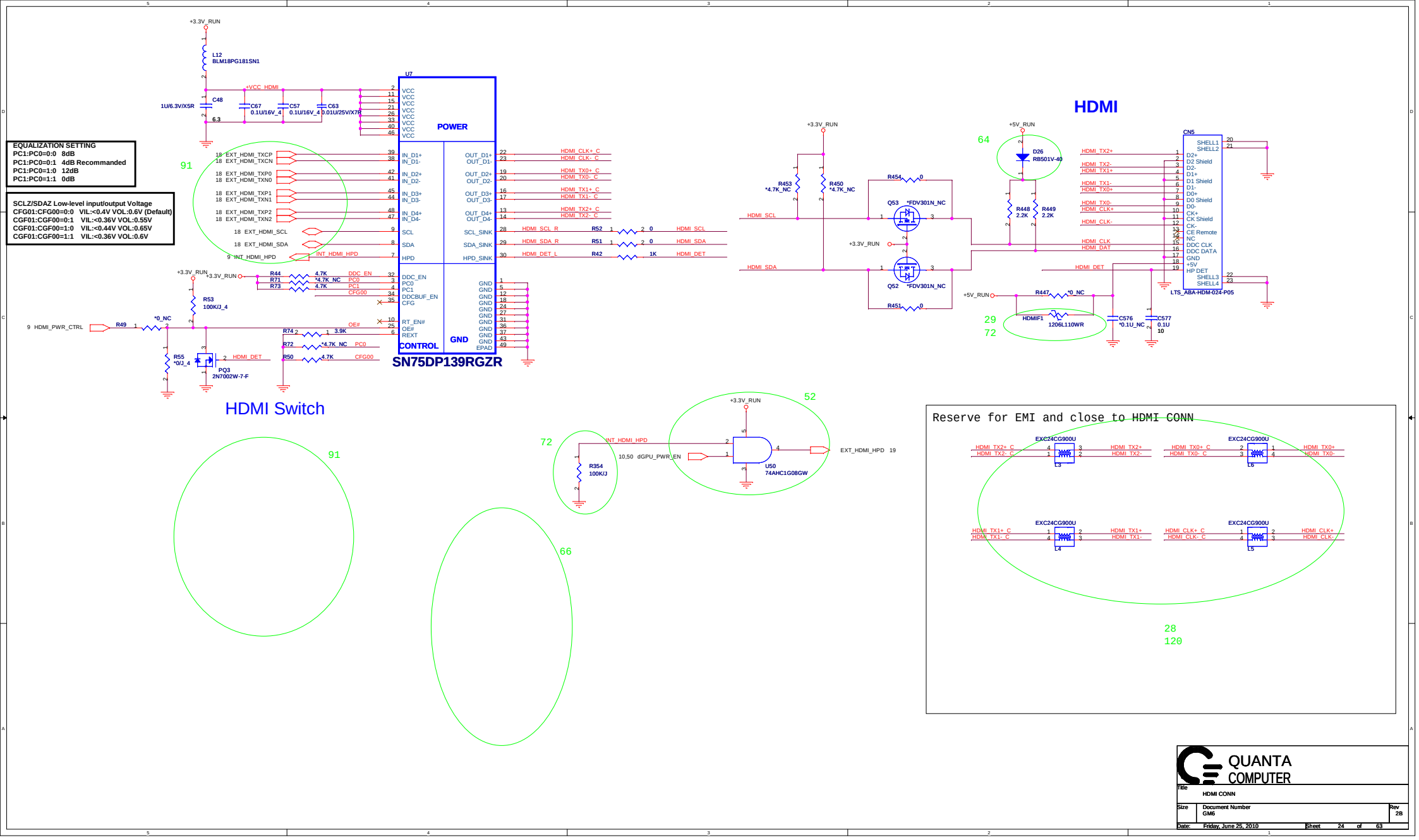
HDMI



Title	HDMI CONN		
Size	Document Number GM6		Rev 2B
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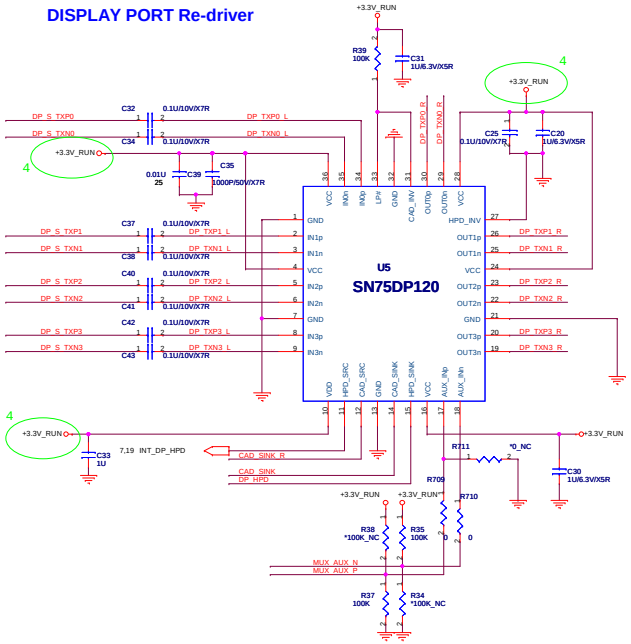
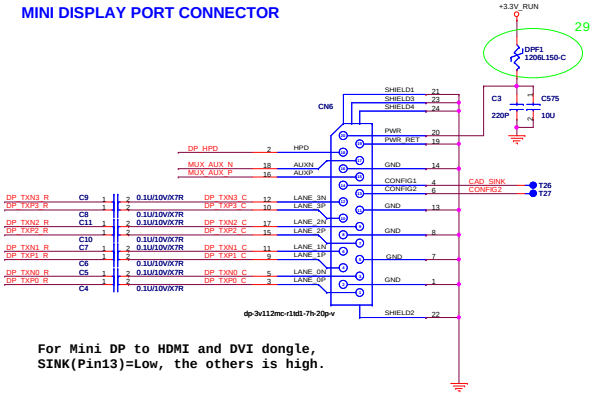
QUANTA COMPUTER

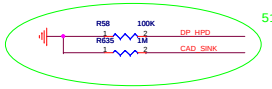
DISPLAY PORT Re-driver

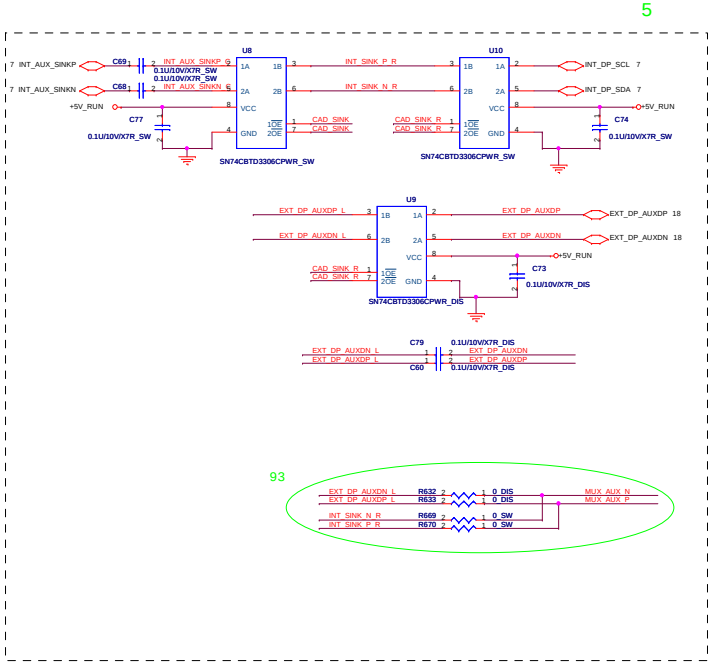


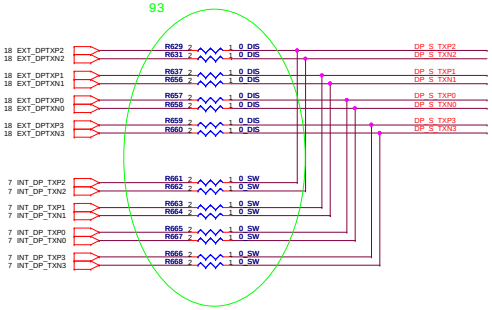
MINI DISPLAY PORT CONNECTOR



For Mini DP to HDMI and DVI dongle,
SINK(Pin13)=Low, the others is high.







OE	Output
L	A=B
H	Z

QUANTA COMPUTER

Title	Display Port CONN	
Size	Document Number GM6	Rev 2B
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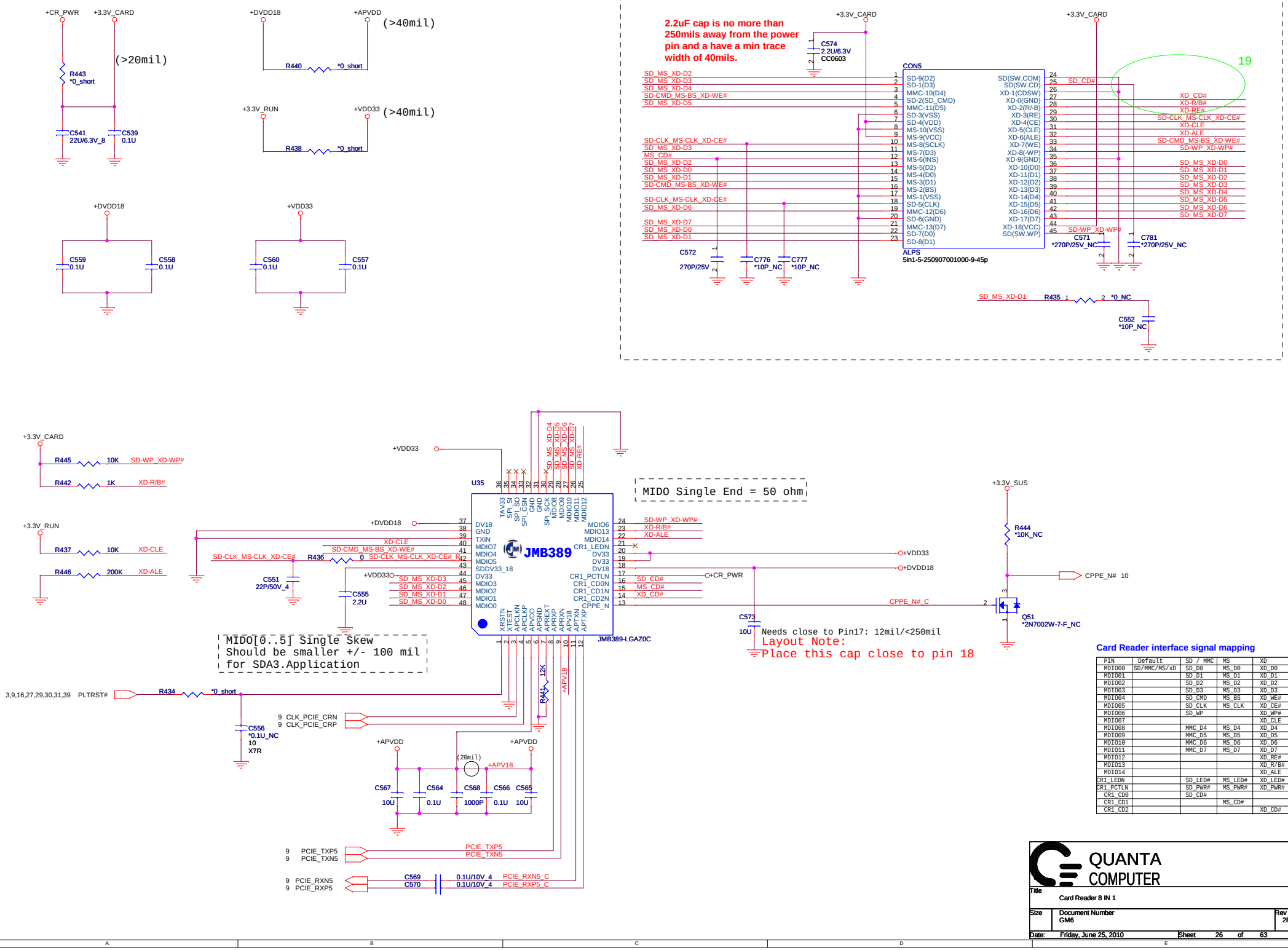

Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/xD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

QUANTA COMPUTER

Title	Card Reader 8 IN 1	
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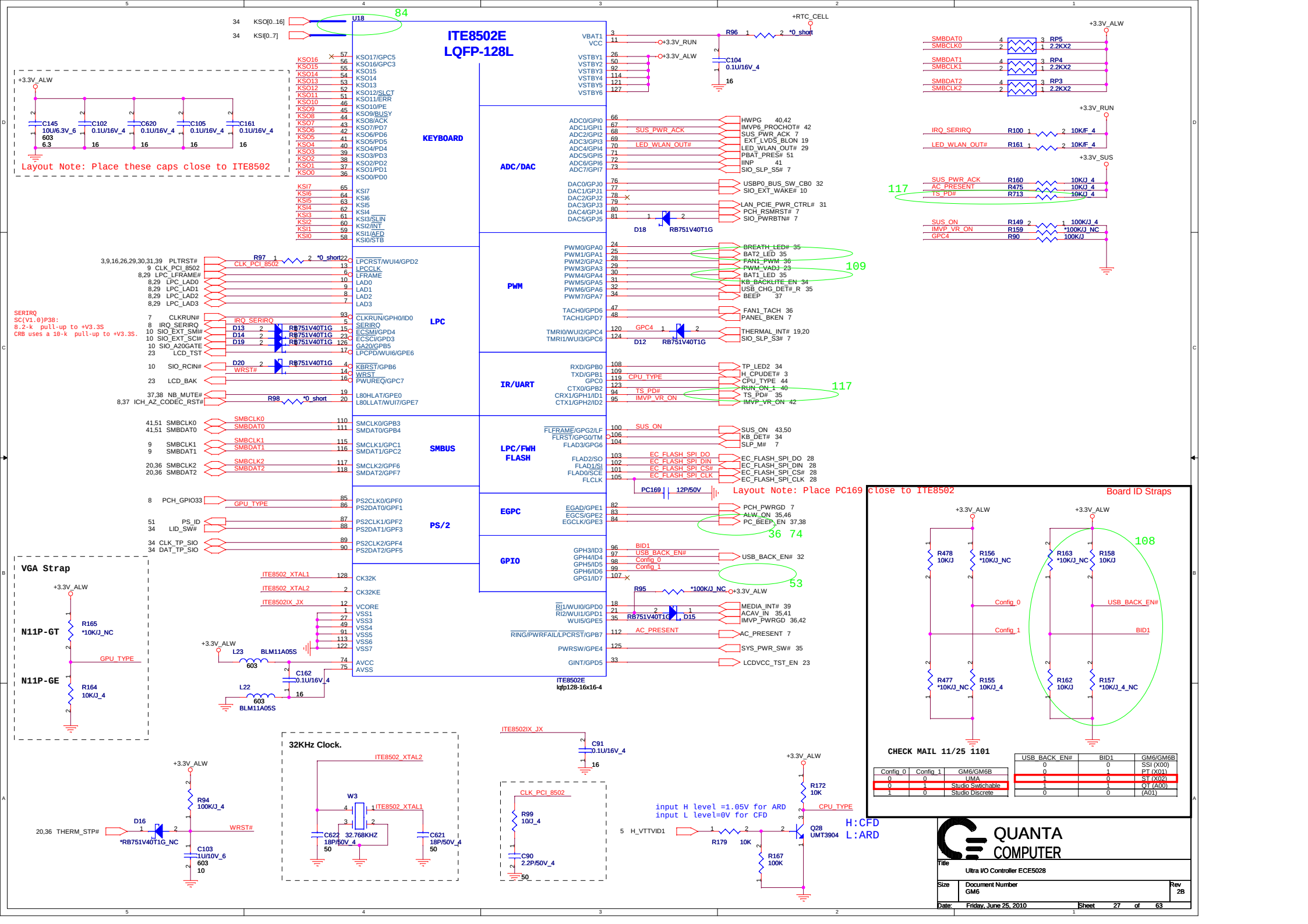
ITE8502E
LQFP-128L
U18
84
KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH
FLASH
EGPC
PS/2
GPIO
Layout Note: Place these caps close to ITE8502
SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.
VGA Strap
N11P-GT
N11P-GE
32KHz Clock.
Layout Note: Place PC169 close to ITE8502
Board ID Straps
CHECK MAIL 11/25 1101
input H level =1.05V for ARD
input L level=0V for CFD
H:CFD
L:ARD
QUANTA COMPUTER
Title
Ultra I/O Controller ECE5028
Size
Document Number
GM6
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2B
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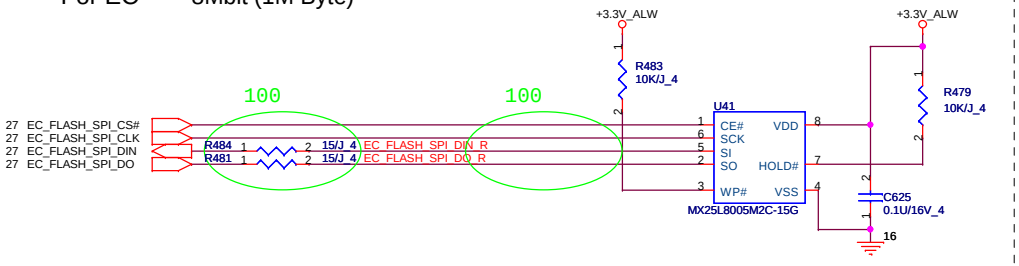
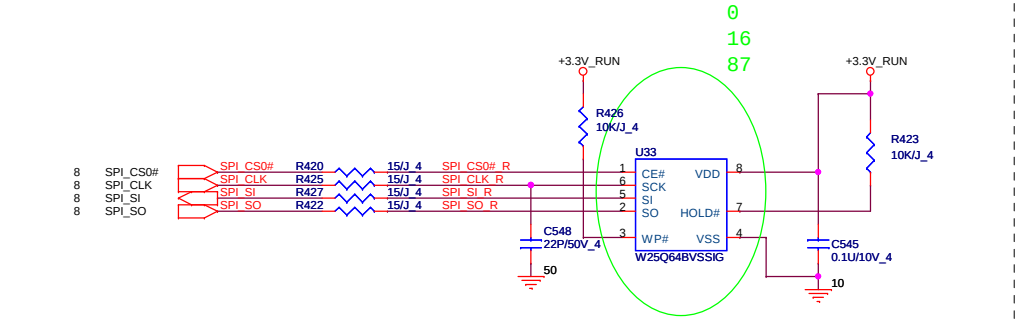
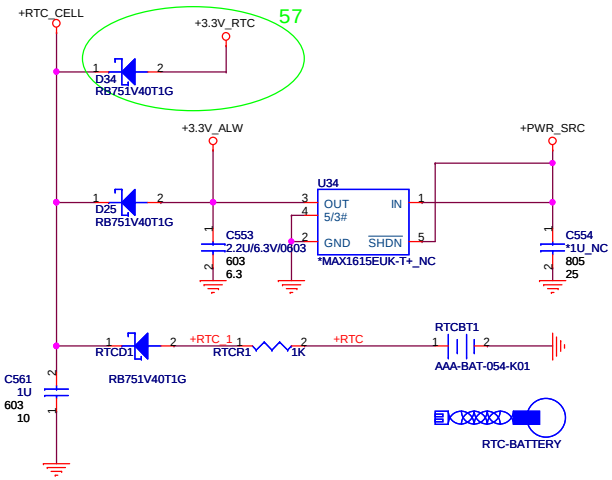
For EC 8Mbit (1M Byte)



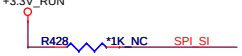
For PCH 32Mbit (4M Byte)



RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R428
Enable	Mount
Disable	NC (Default)

QUANTA COMPUTER

Title	FLASH/RTC	
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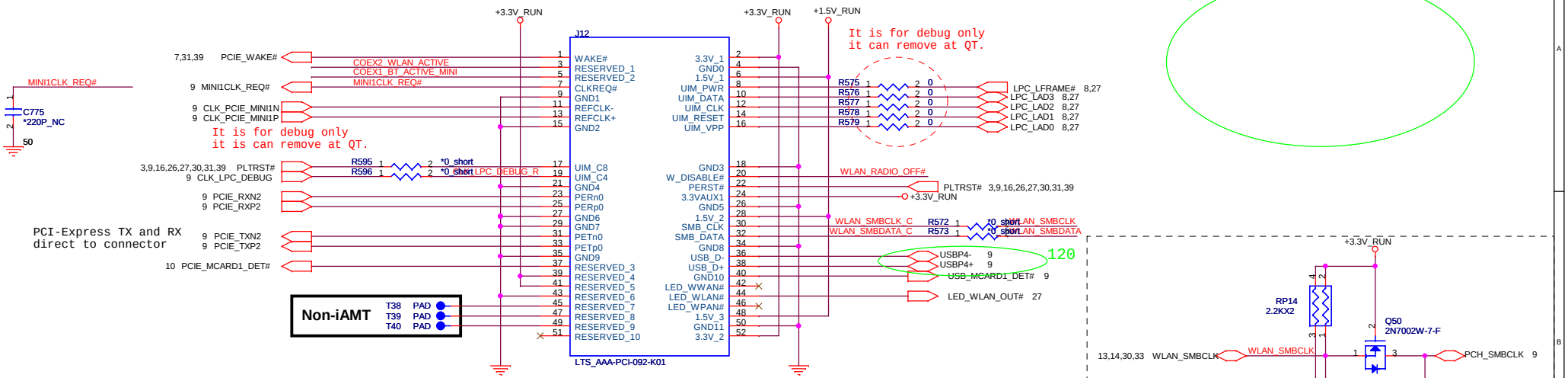
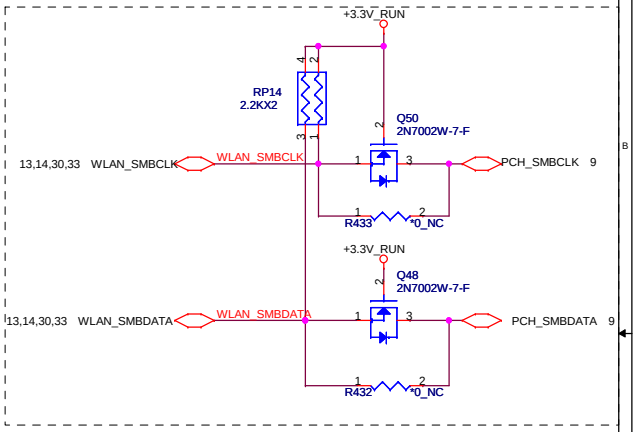
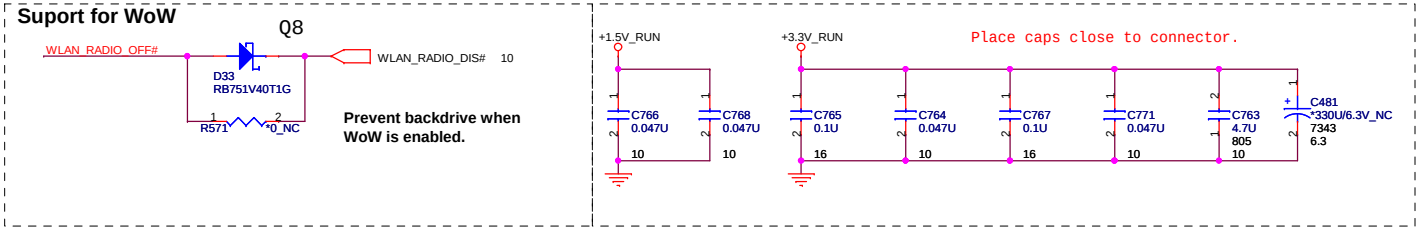
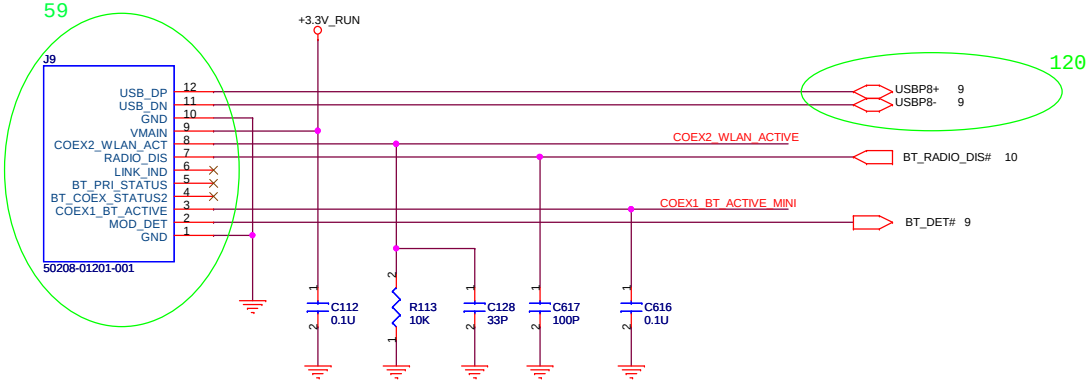
MiniCard WLAN connector

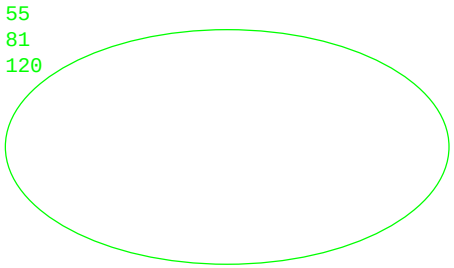






Support Dell BT375 (Little Stone) module (XPS) W TO B





QUANTA COMPUTER		
Title: WLAN		
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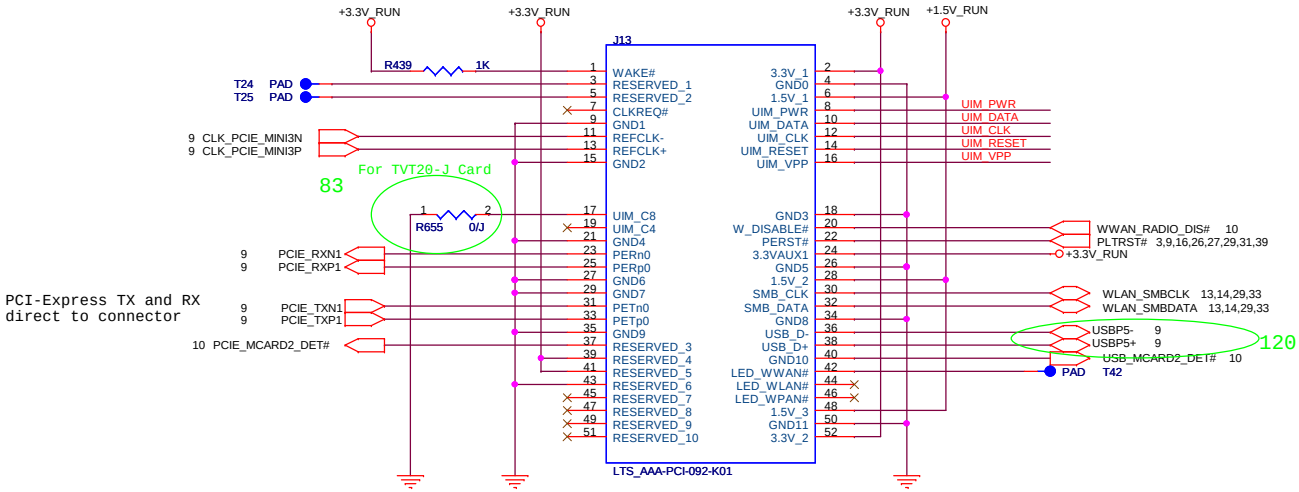
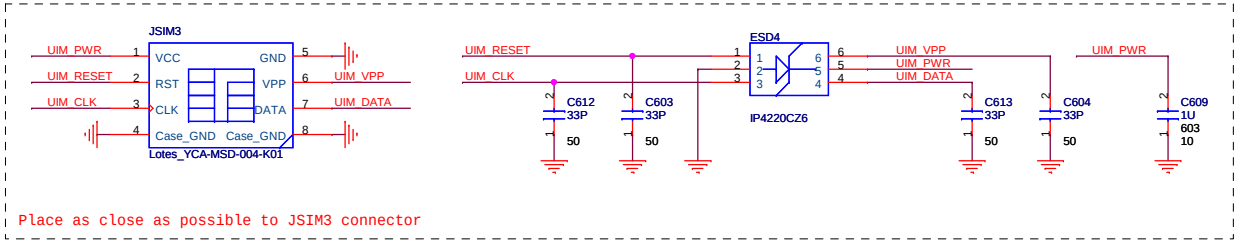
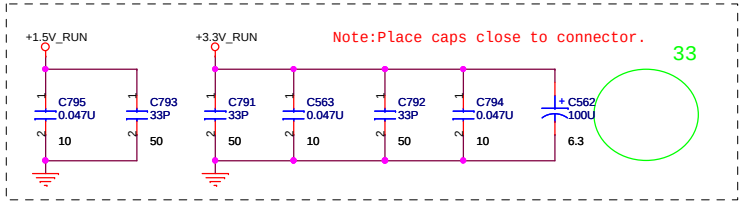
MiniCard WWAN connector



55
81
120





QUANTA COMPUTER		
Title: WWAN		
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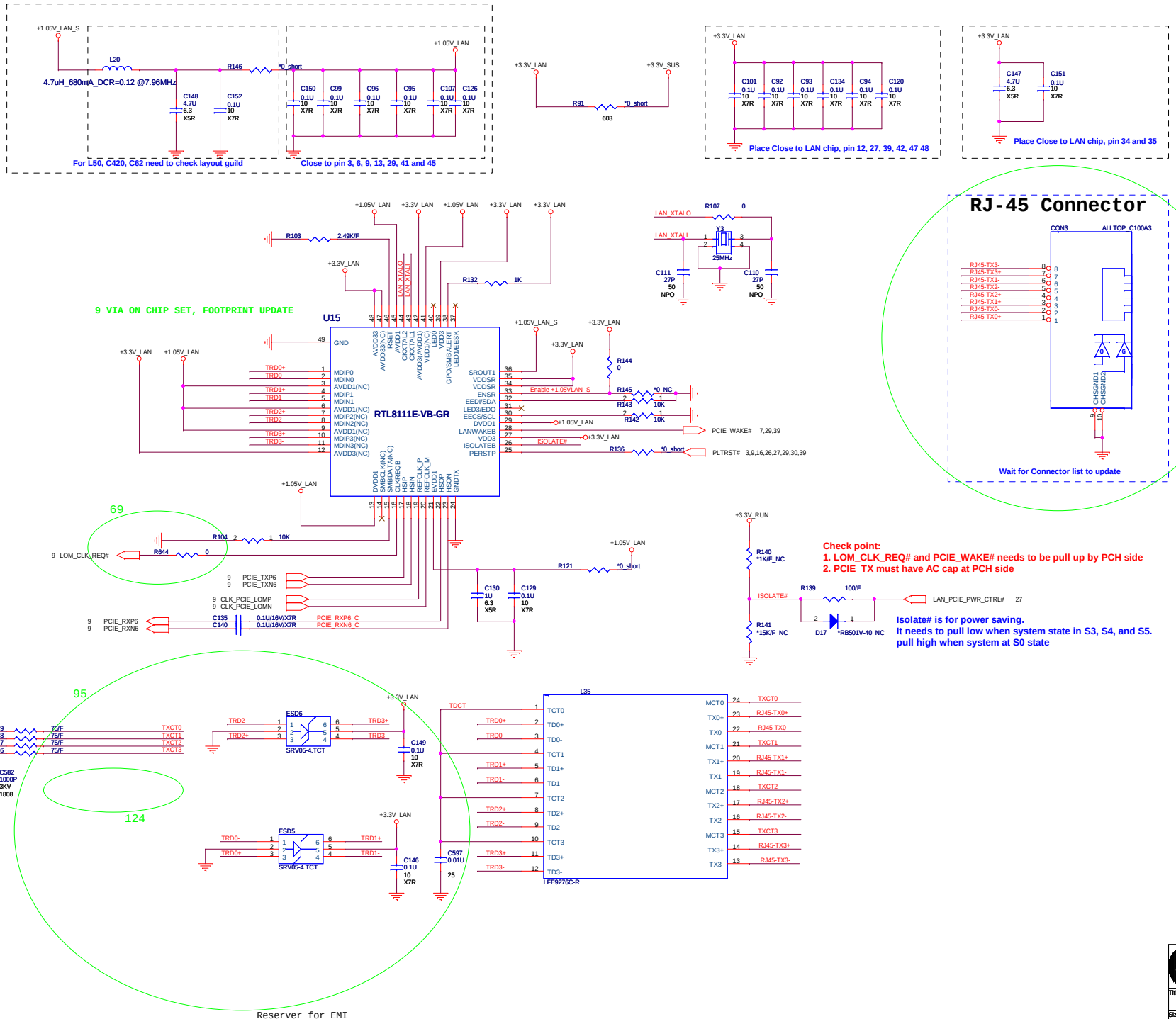

QUANTA COMPUTER

Title	LAN	
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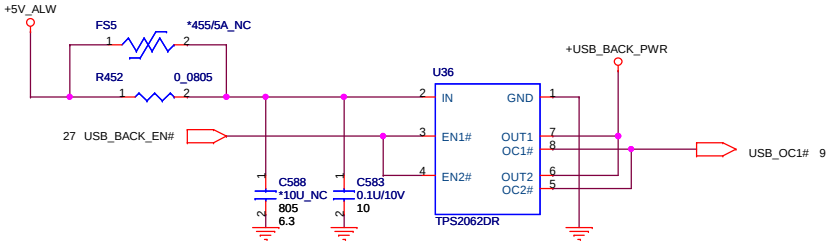
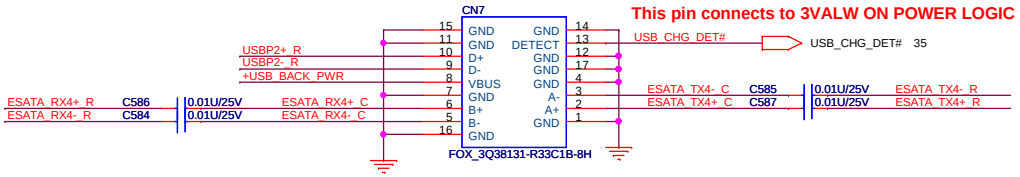
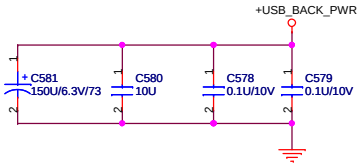
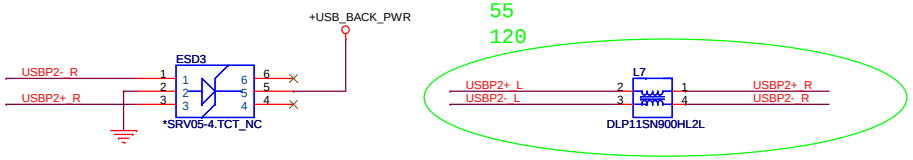
ESATA + USB Conn + Power Share

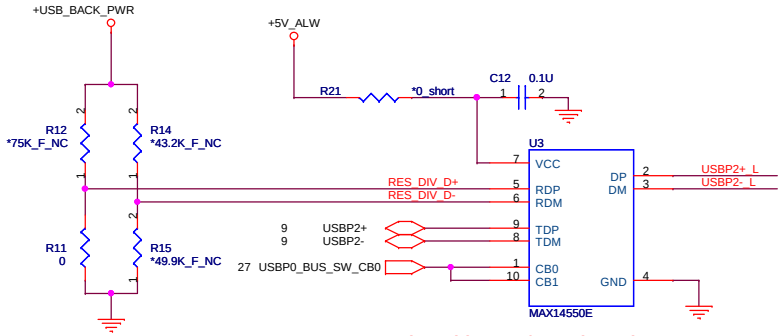


USB_BACK_EN# needs to be low when system S3 and S5 for USB charge









EC needs to drive CB0/CB1 pins to low
when system S3/S5 and dirve high when system S0.

U49 PN and Footprint needs to double check

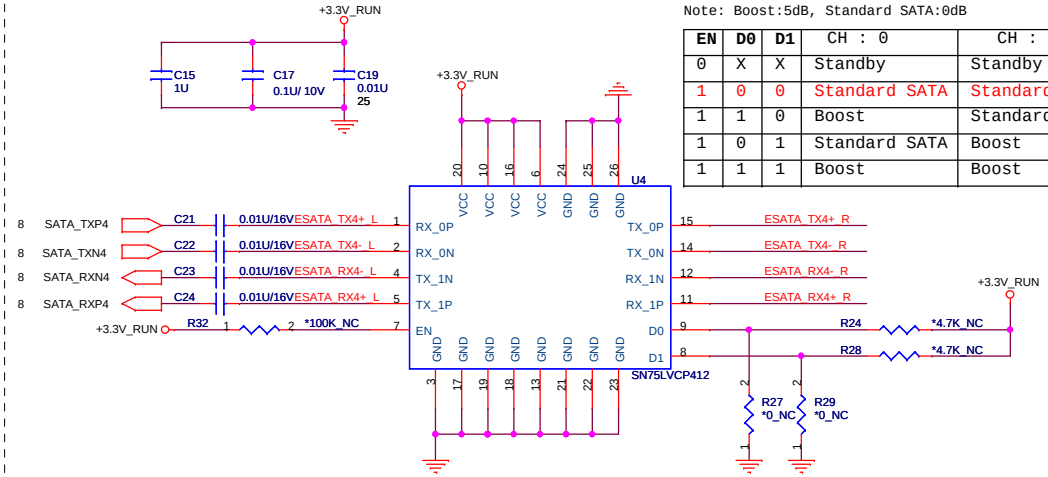
R15 needs to be 49.9K_F if we use external resisters.

CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only

(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

QUANTA COMPUTER

Title	Right PUSB/ESATA	
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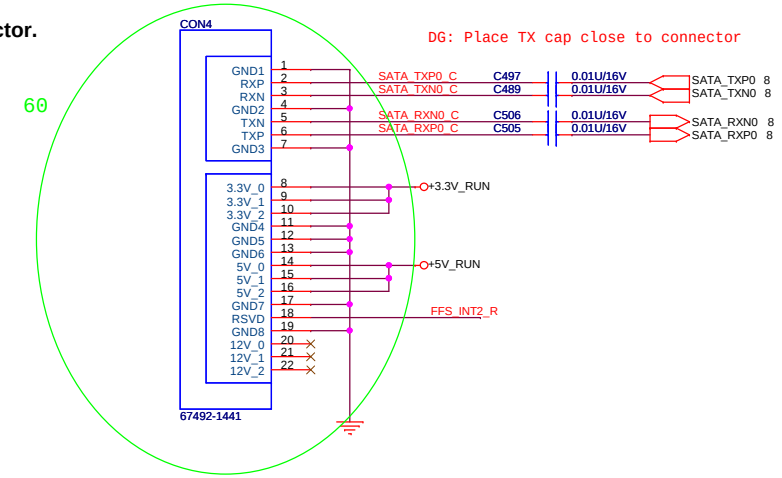
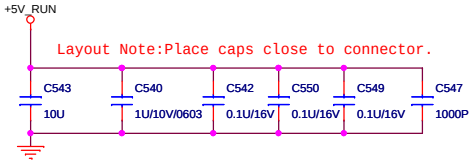
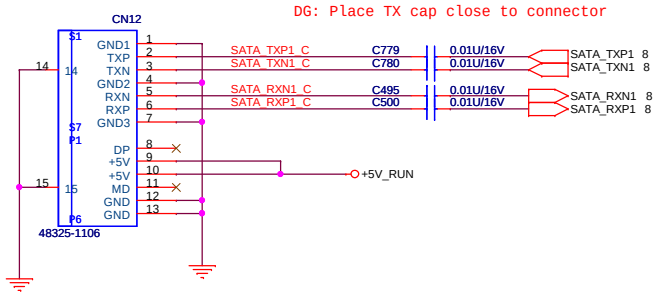
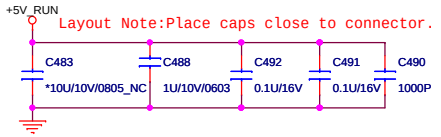
SATA Connector.

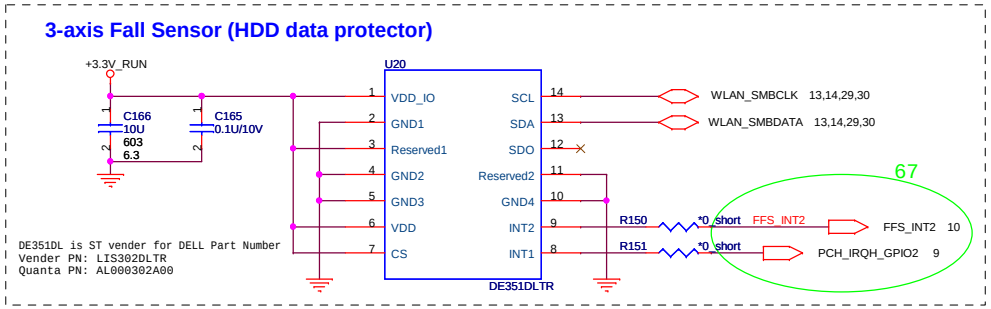


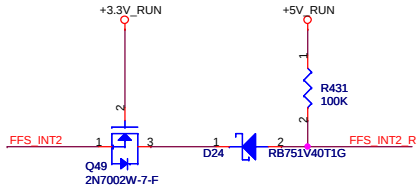


ODD Connector









QUANTA COMPUTER

Title	SATA (HDD&CD_ROM)	
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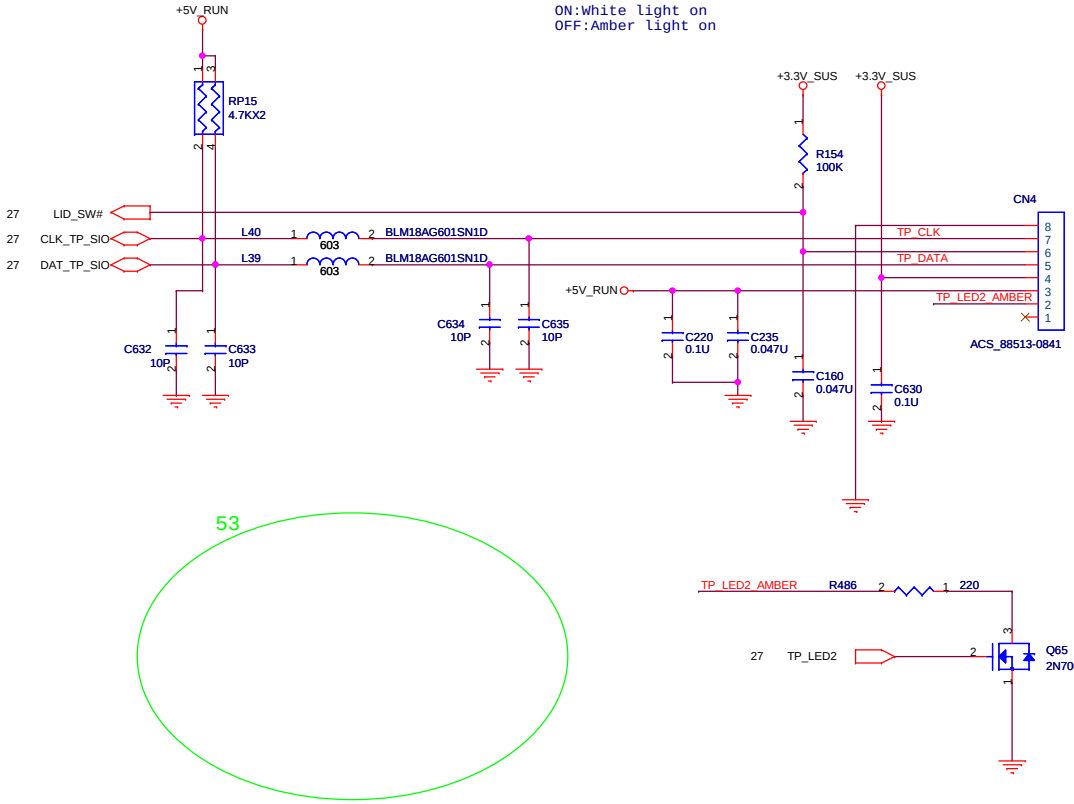
Touch Pad

ON:White light on
OFF:Amber light on



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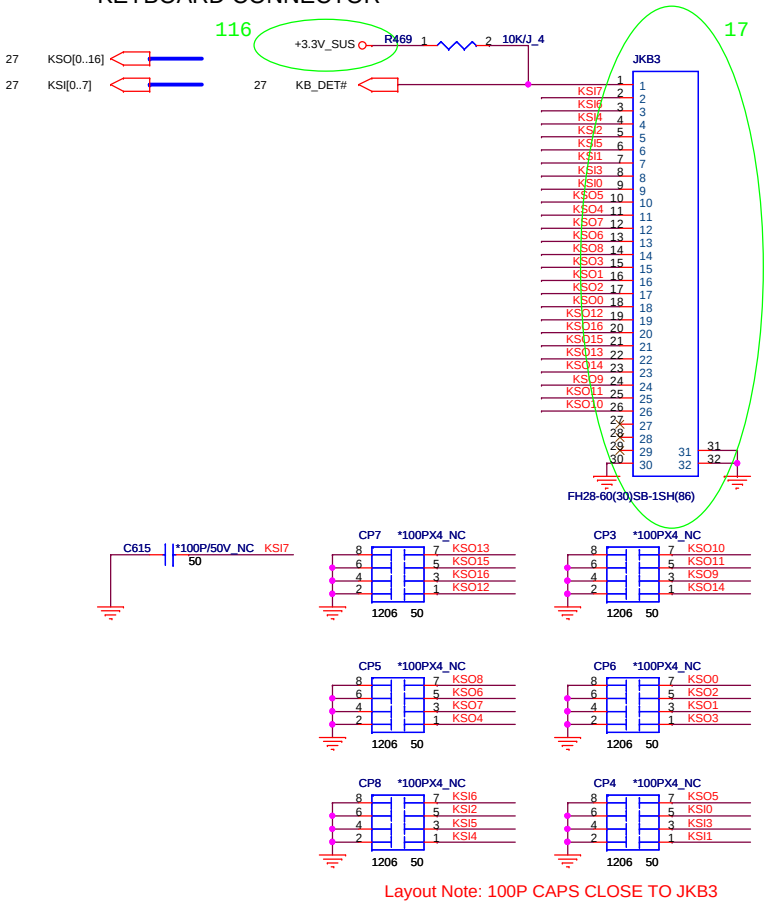
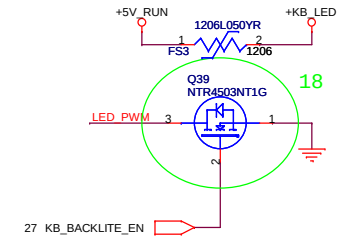
KEYBOARD CONNECTOR

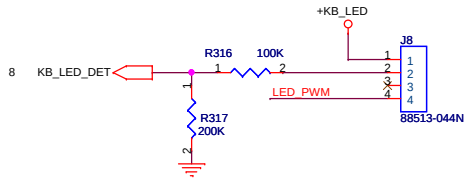


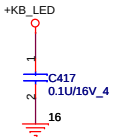
Layout Note: 100P CAPS CLOSE TO JKB3

Key board illumination

+KB_LED power trace width >10 mil







QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
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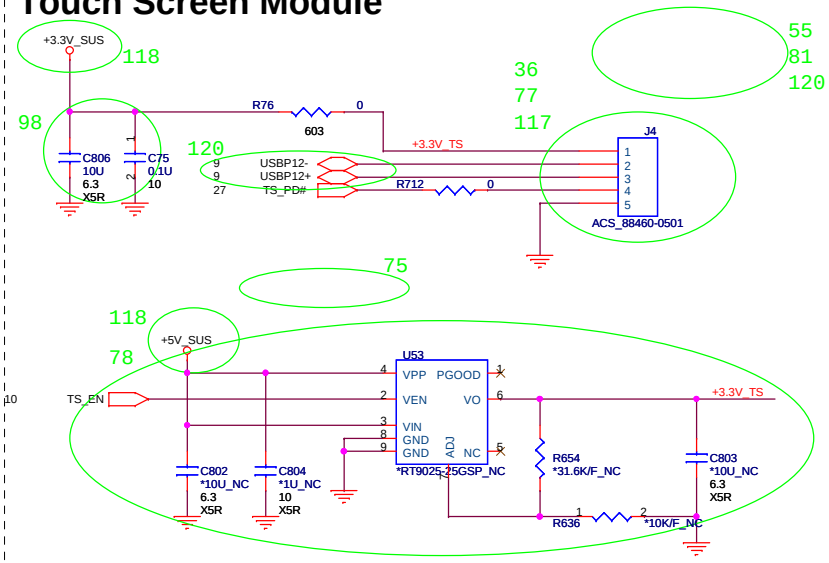
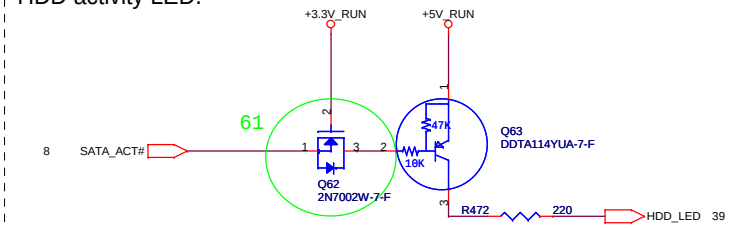
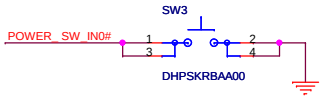
Touch Screen Module



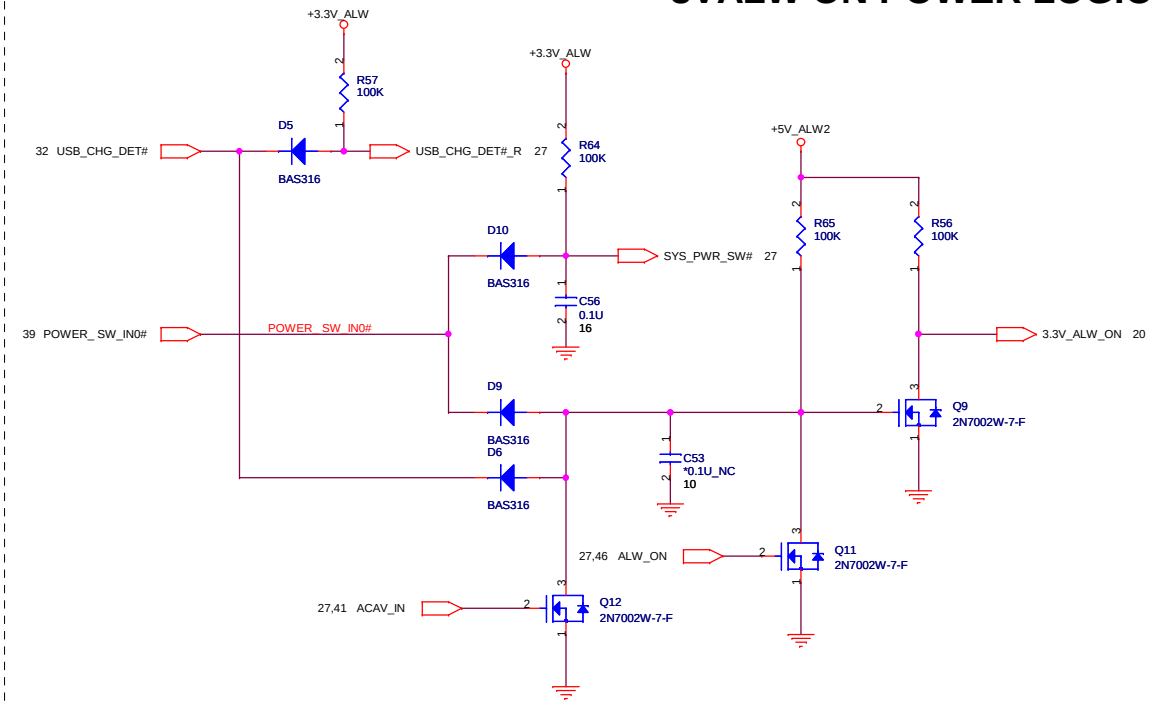
HDD activity LED.



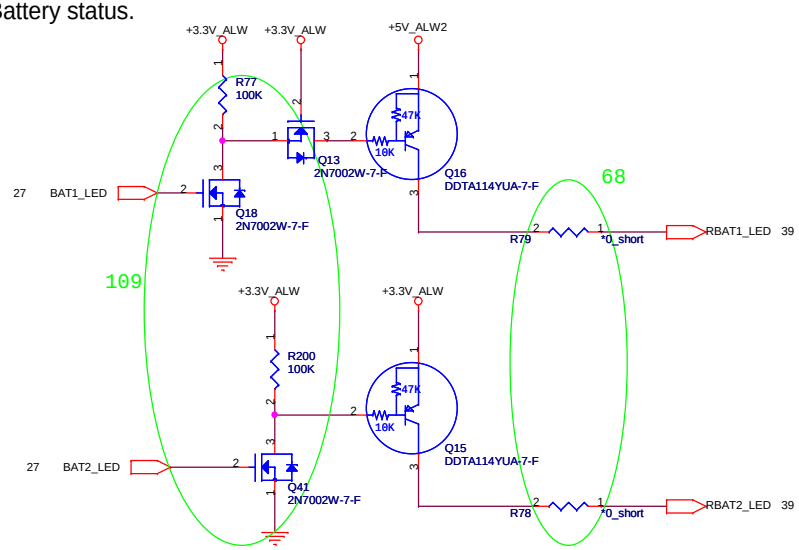
Power button for Engineer

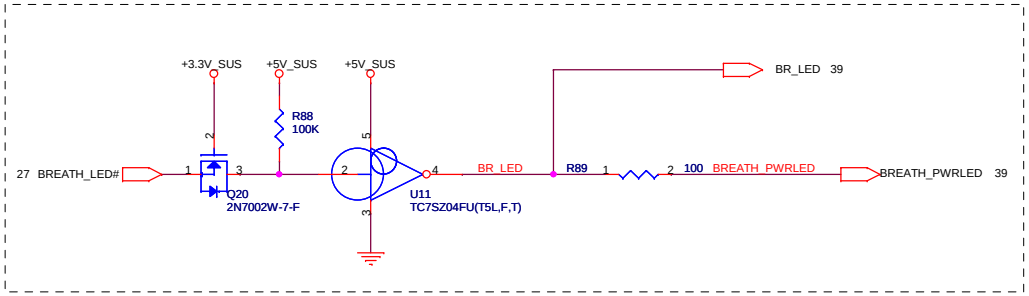


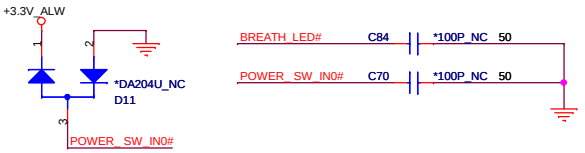
3VALW ON POWER LOGIC



Battery status.







QUANTA COMPUTER

Title	SWITCH, KEYBOARD & LED&Touch Screen Module	
Size	Document Number GM6	Rev 2B
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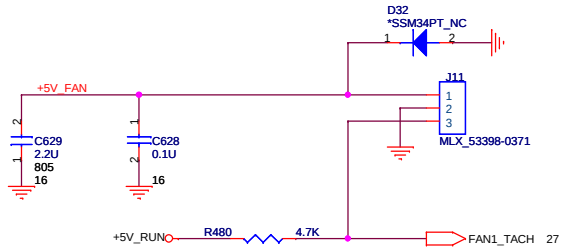

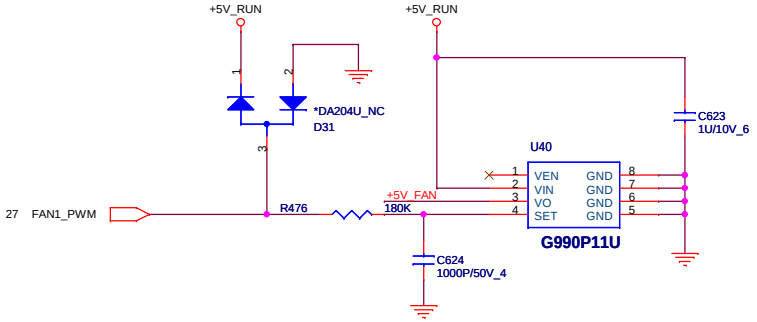

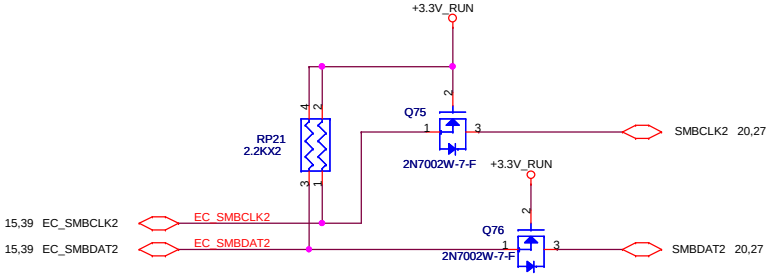

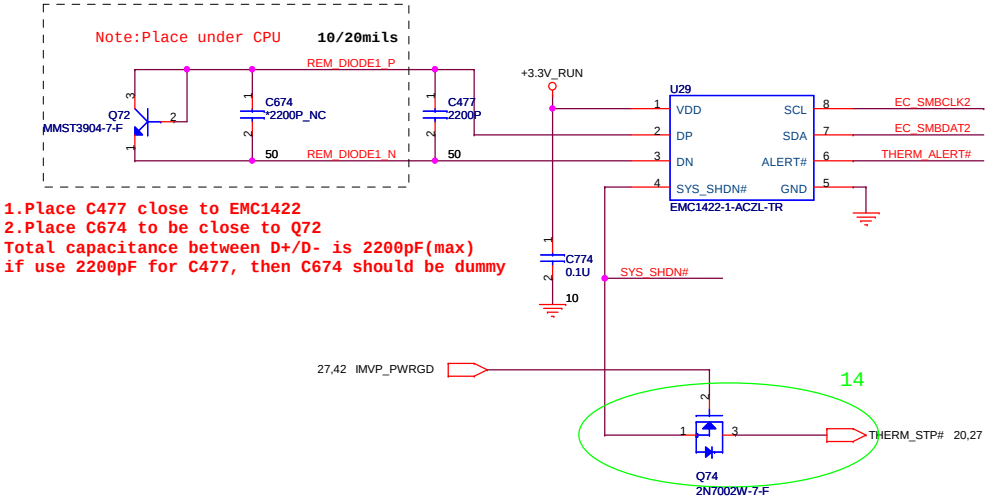

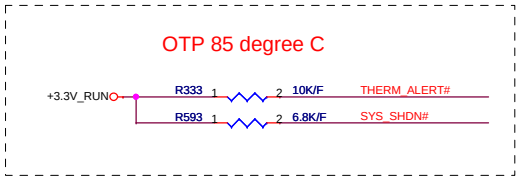

QUANTA COMPUTER

Title	FAN & THERMAL	
Size	Document Number GM6	Rev 2B
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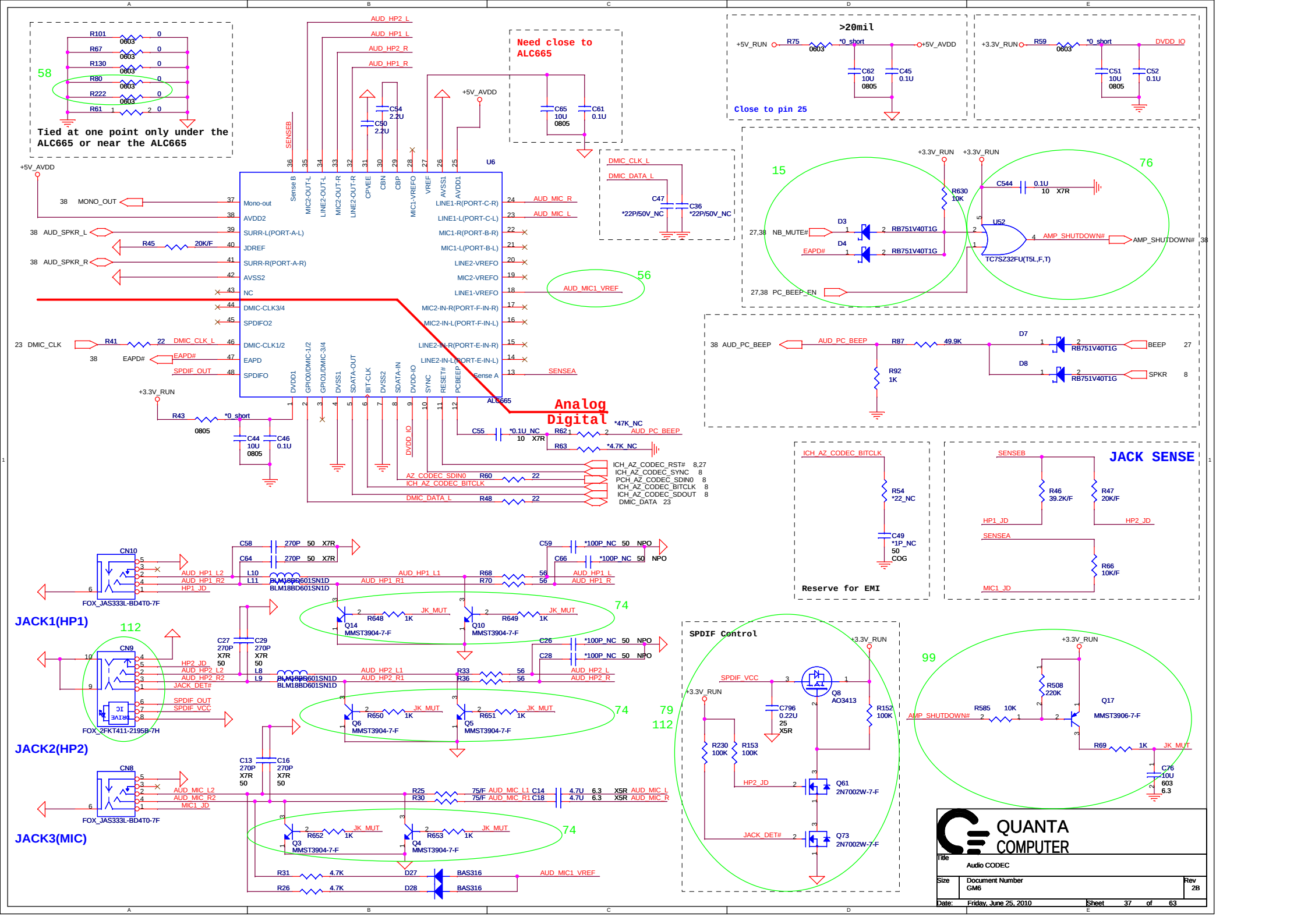
Tied at one point only under the ALC665 or near the ALC665
Need close to ALC665
>20mil
Close to pin 25
ALC665
Analog
Digital
Reserve for EMI
JACK SENSE
SPDIF Control
JACK1(HP1)
JACK2(HP2)
JACK3(MIC)
FOX_JAS333L-BD4T0-7F
FOX_2FKT411-2195B-7H
QUANTA COMPUTER
Audio CODEC
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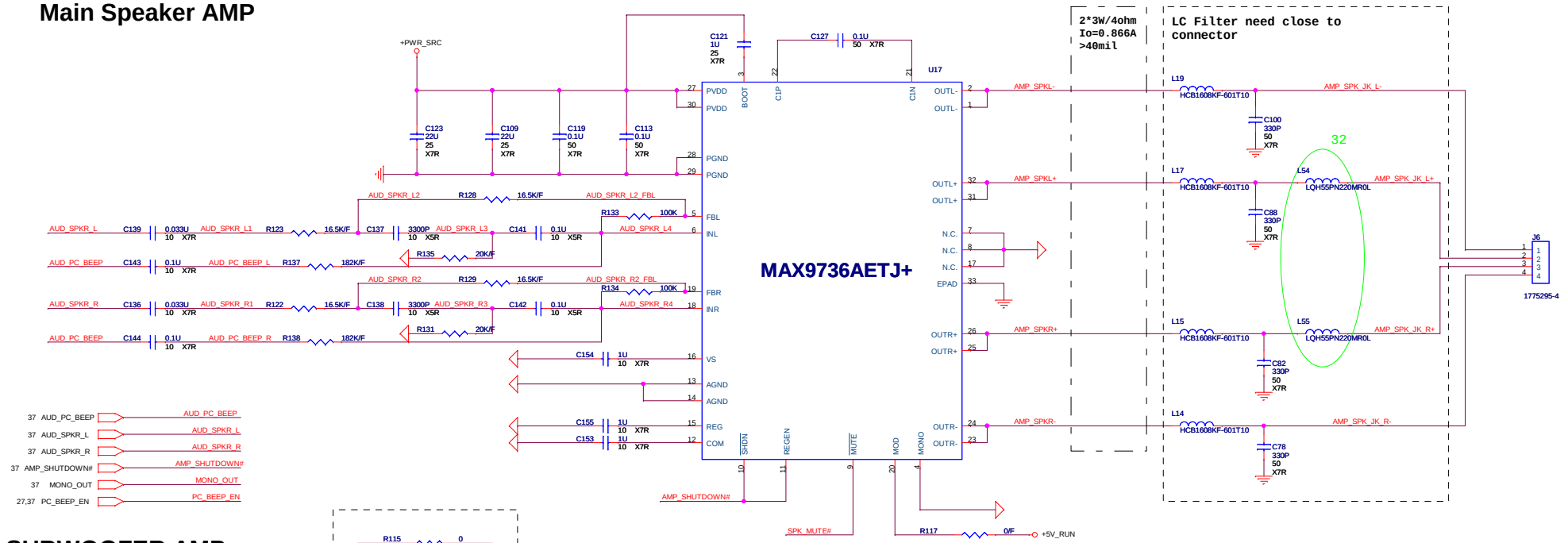
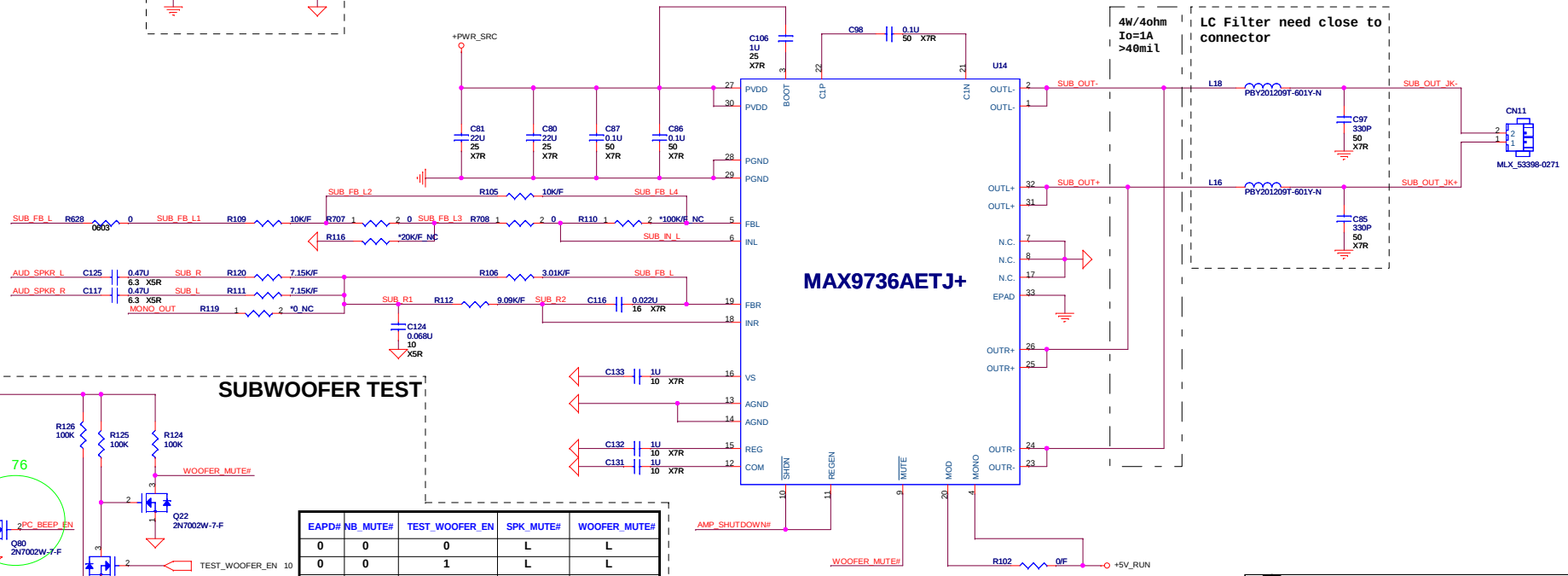
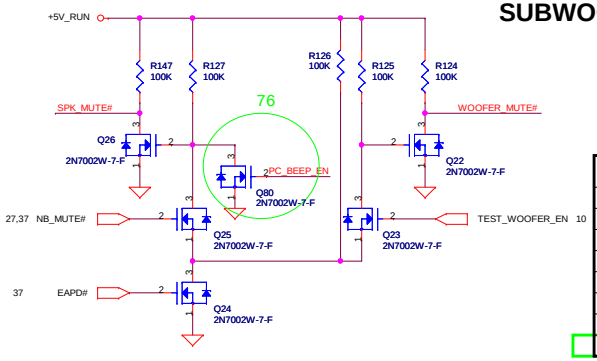
Main Speaker AMP



SUBWOOFER AMP



SUBWOOFER TEST



EAPD#	NB_MUTE#	TEST_WOOFER_EN	SPK_MUTE#	WOOFER_MUTE#
0	0	0	L	L
0	0	1	L	L
0	1	0	L	L
0	1	1	L	L
1	0	0	L	L
1	0	1	L(Disable SPK)	H(Test Woofer)
1	1	0	H(Test SPK)	L(Disable Woofer)
1	1	1	H	H

QUANTA COMPUTER

Title	AUDIO AMP	
Size	Document Number GM6	Rev 2B
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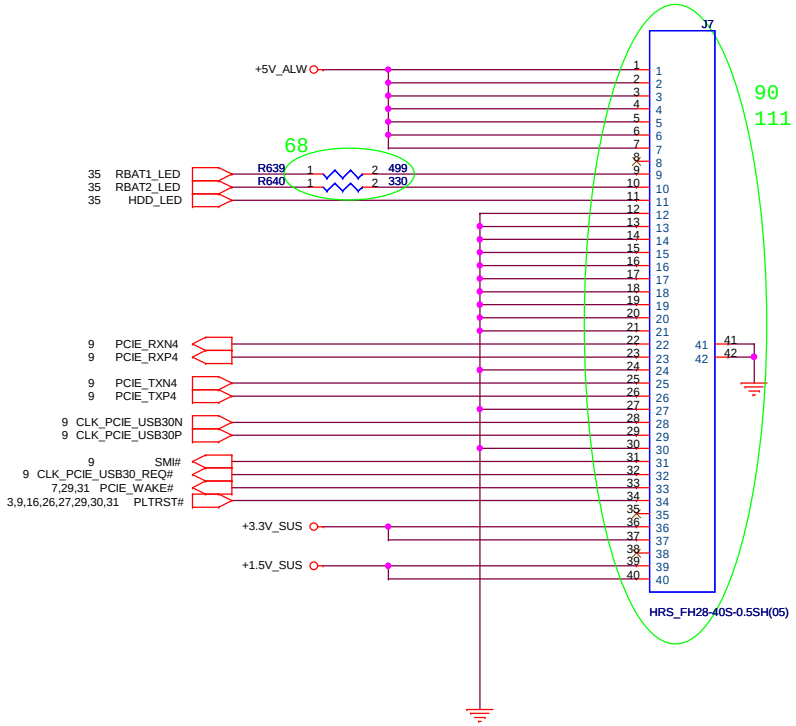
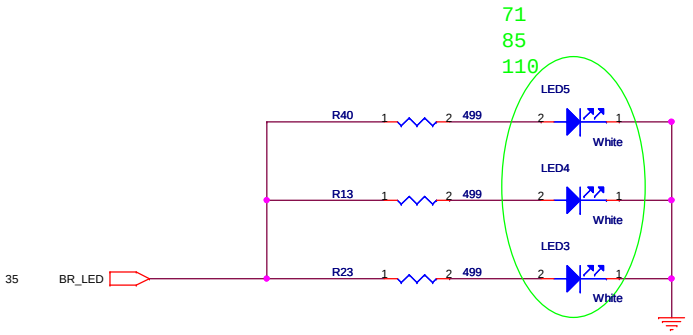
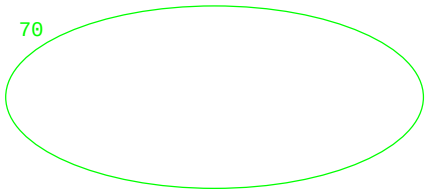
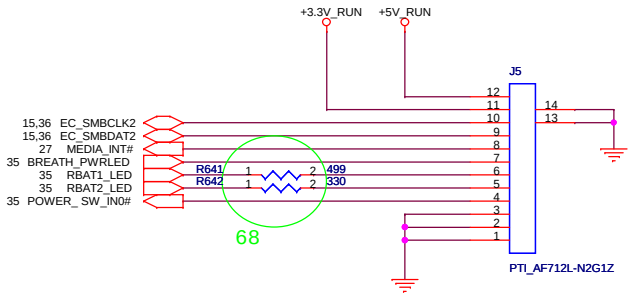


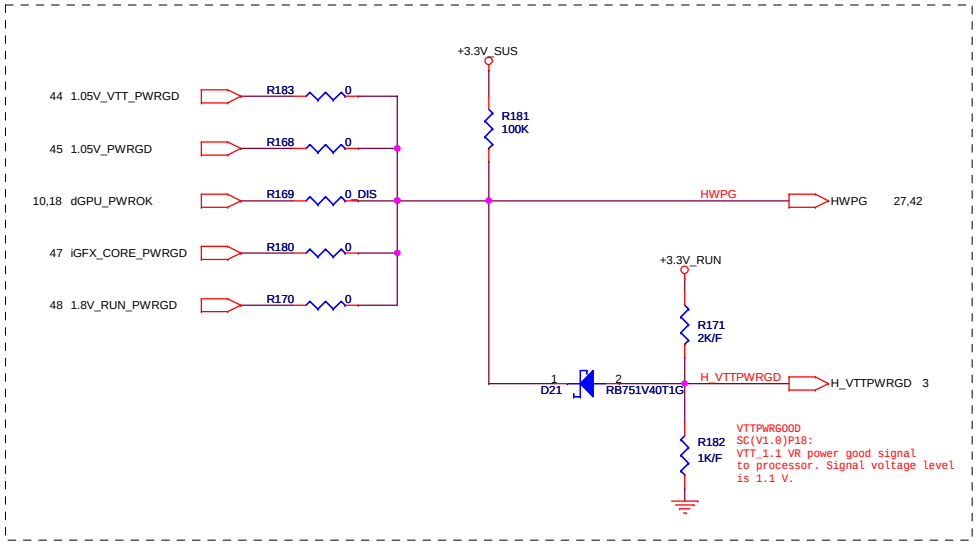


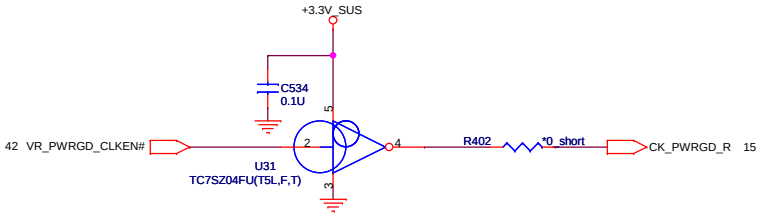


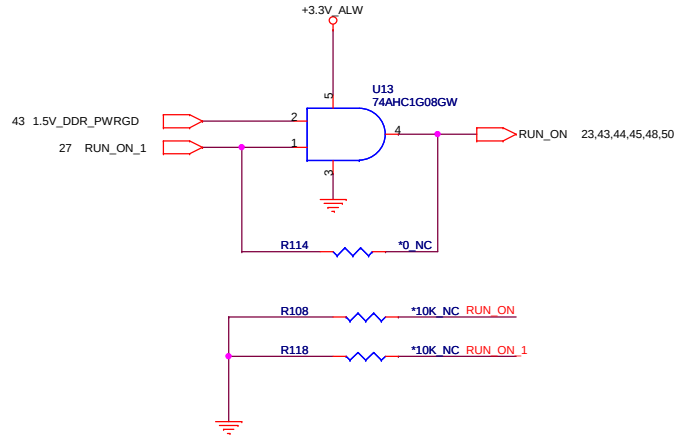


QUANTA COMPUTER

Title	Left USB / MMB CONN	
Size	Document Number GM6	Rev 2B
Date: Friday, June 25, 2010	Sheet 39 of 63	







QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number GM6	Rev 2B
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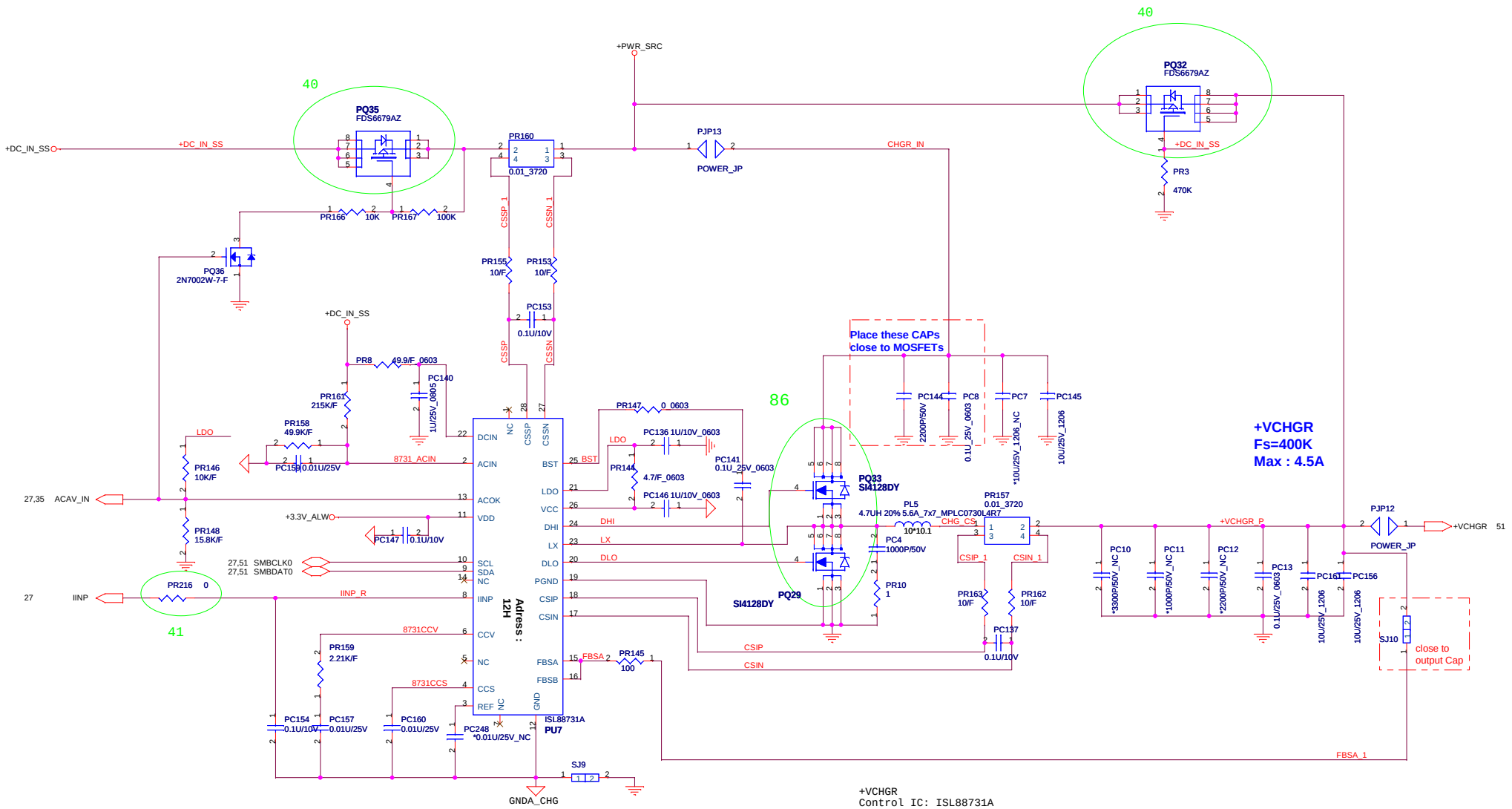

Title	Charger (ISL88731)		
Size	Document Number GM6		Rev 2B
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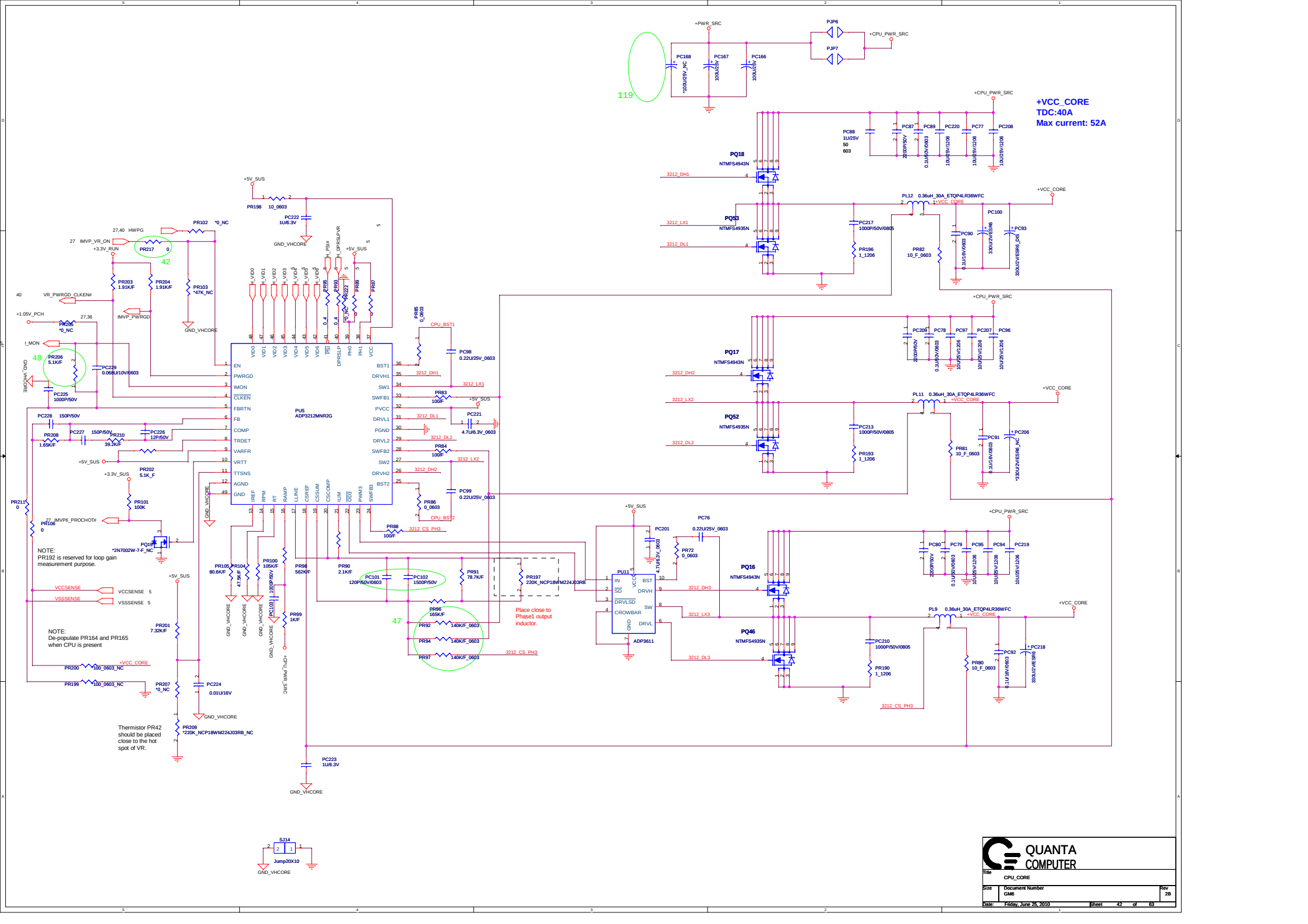
+VCC_CORE
TDC:40A
Max current: 52A
PU5
ADP3212MNR2G
PU11
ADP3611
PQ18
PQ53
PQ17
PQ52
PQ16
PQ46
PL12 0.36uH_30A_ETQP4LR36WFC
PL11 0.36uH_30A_ETQP4LR36WFC
PL9 0.36uH_30A_ETQP4LR36WFC
NOTE:
PR192 is reserved for loop gain measurement purpose.
NOTE:
De-populate PR164 and PR165 when CPU is present
Thermistor PR42 should be placed close to the hot spot of VR.
Place close to Phase1 output inductor.
Jump20X10
QUANTA COMPUTER
CPU_CORE
Document Number GM6
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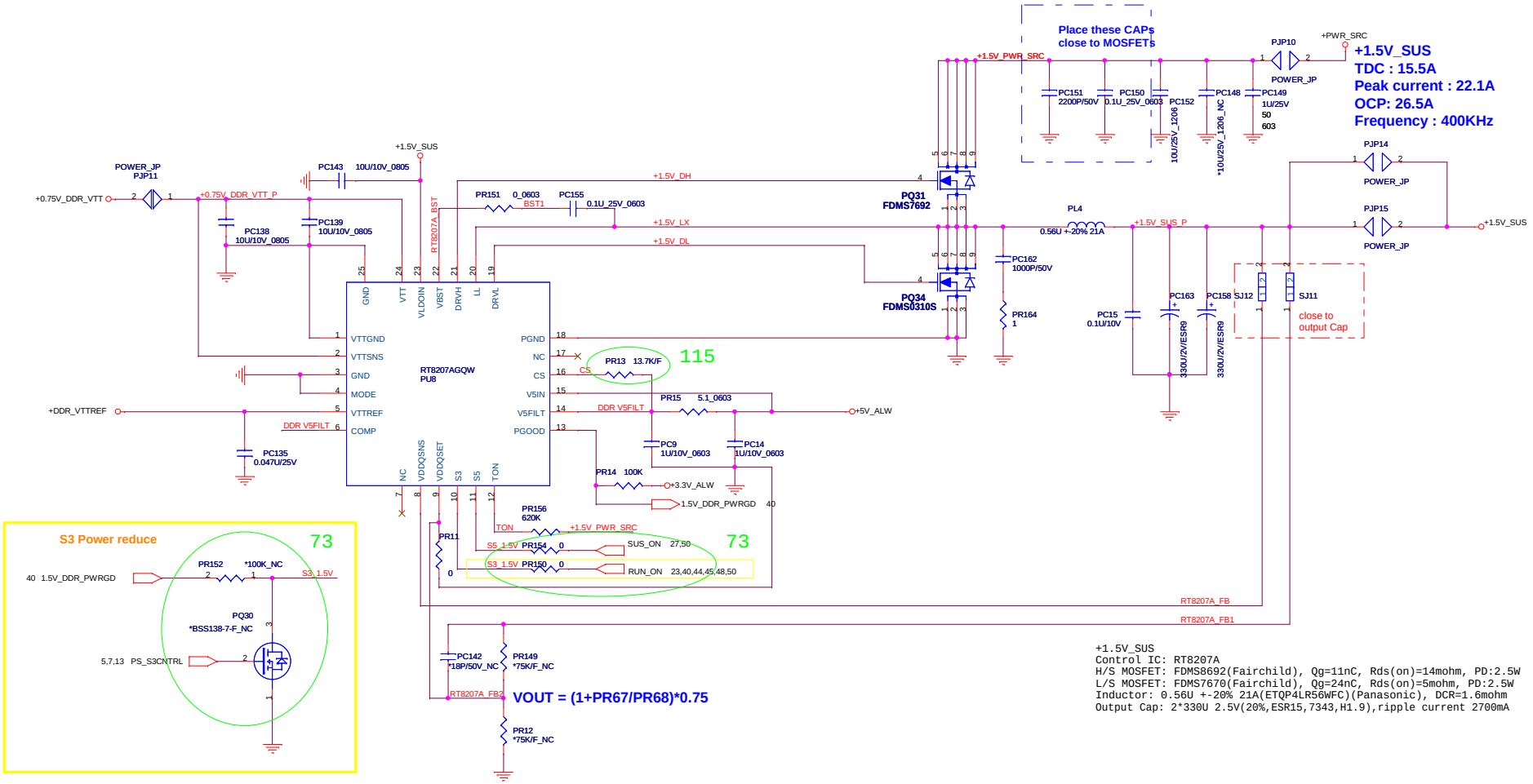

+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

QUANTA COMPUTER

Title	1.5V_SUS & 0.75_DDR_VTT (RT8207)	
Size	Document Number GM6	Rev 2B
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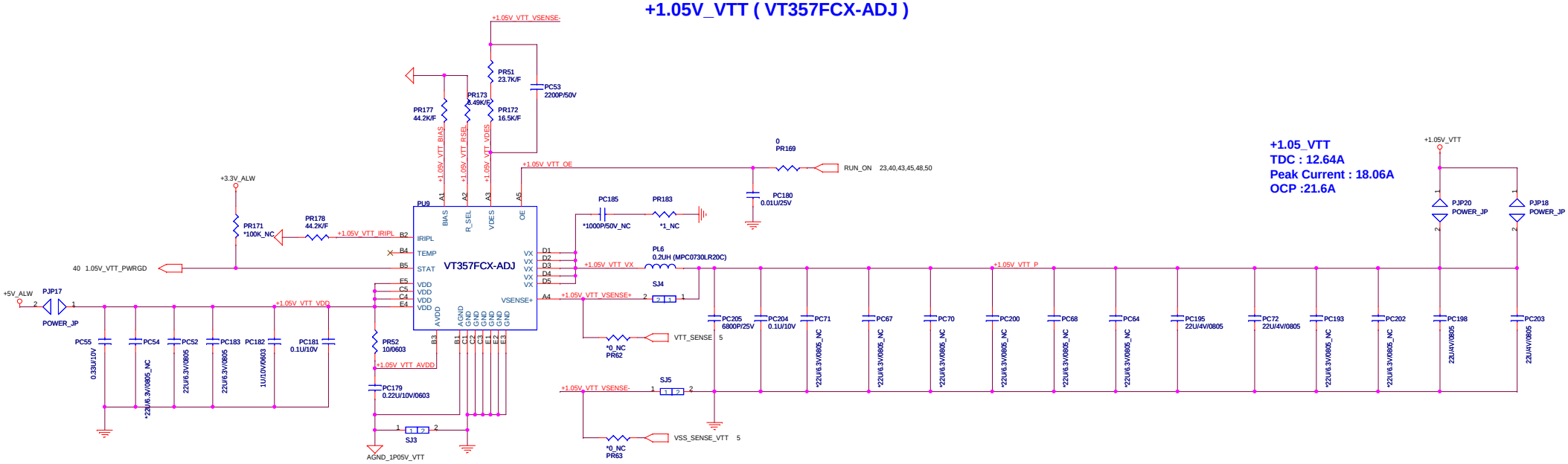
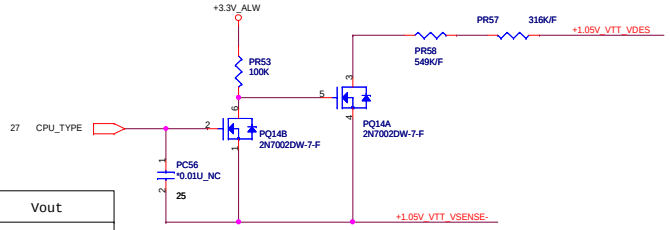
+1.05V_VTT (VT357FCX-ADJ)



+1.05_VTT
TDC : 12.64A
Peak Current : 18.06A
OCP :21.6A

Route +1.05V_VTT_VSENSE+ and +1.05V_VTT_VSENSE- as differential pair

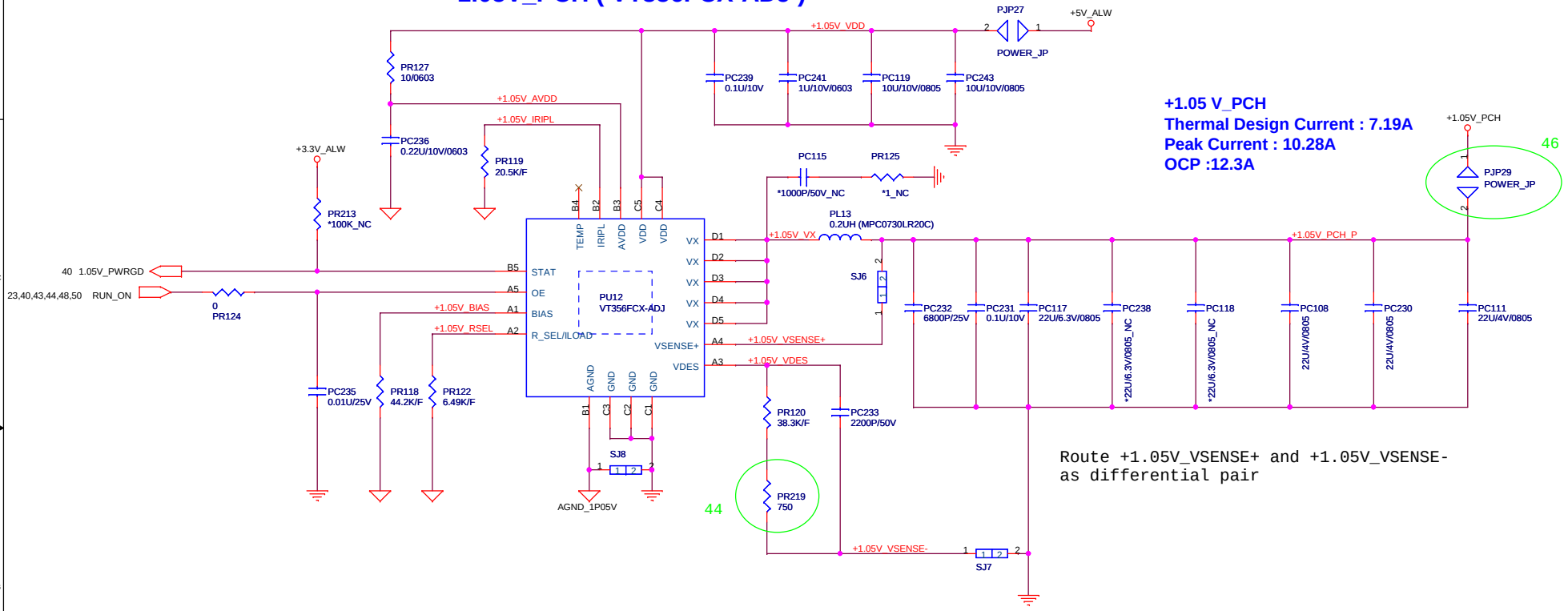


CPU_TYPE	Vout
L	1.05V(ARD)
H	1.1V(CFD)

QUANTA COMPUTER

Title	1.05V_VTT	
Size	Document Number GM6	Rev 2B
Date: Friday, June 25, 2010	Sheet 44 of 63	

+1.05V_PCH (VT356FCX-ADJ)



+1.05 V_PCH
Thermal Design Current : 7.19A
Peak Current : 10.28A
OCP :12.3A

Route +1.05V_VSENSE+ and +1.05V_VSENSE- as differential pair

QUANTA COMPUTER

Title	1.05V_PCH	
Size	Document Number GM6	Rev 2B
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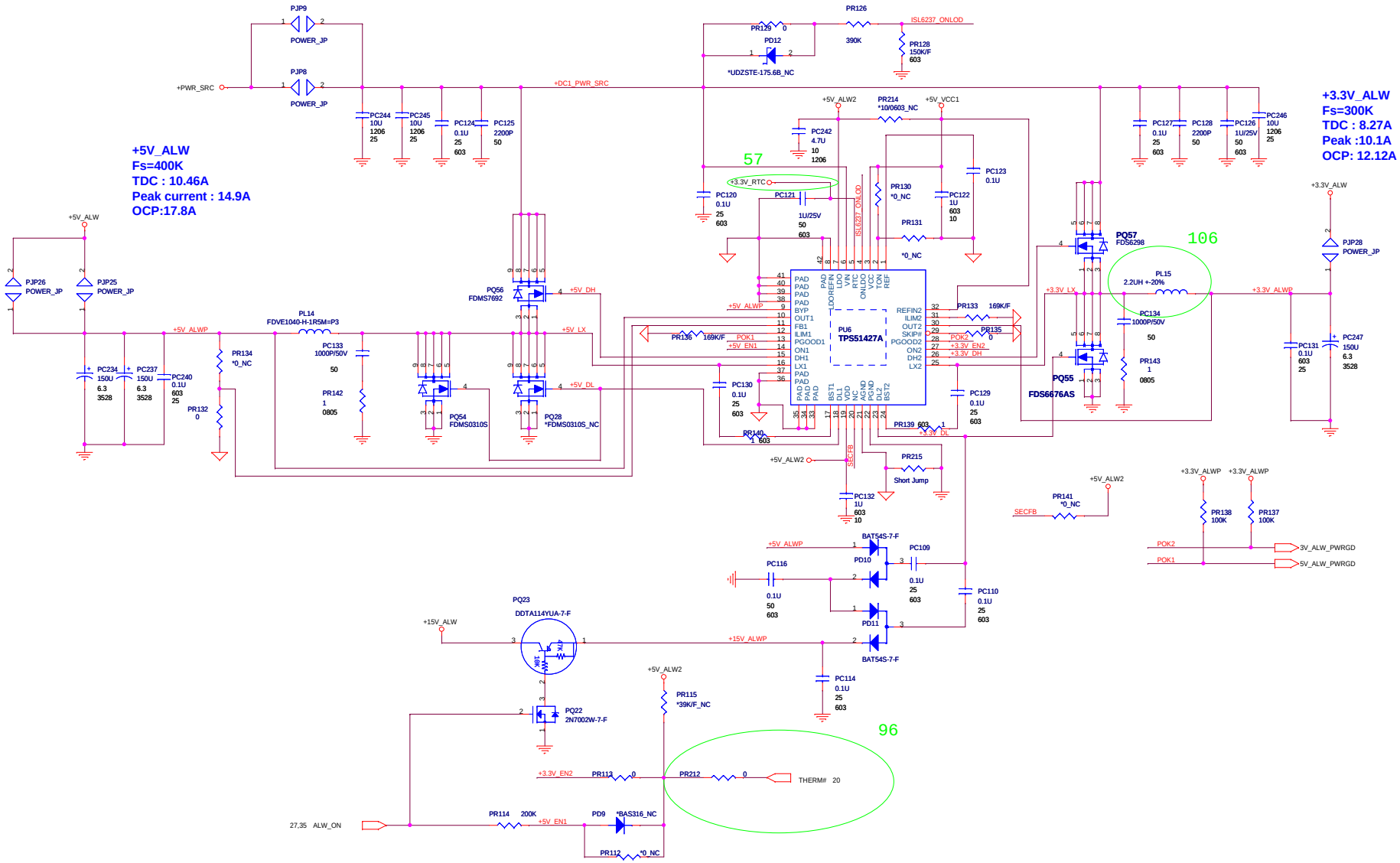
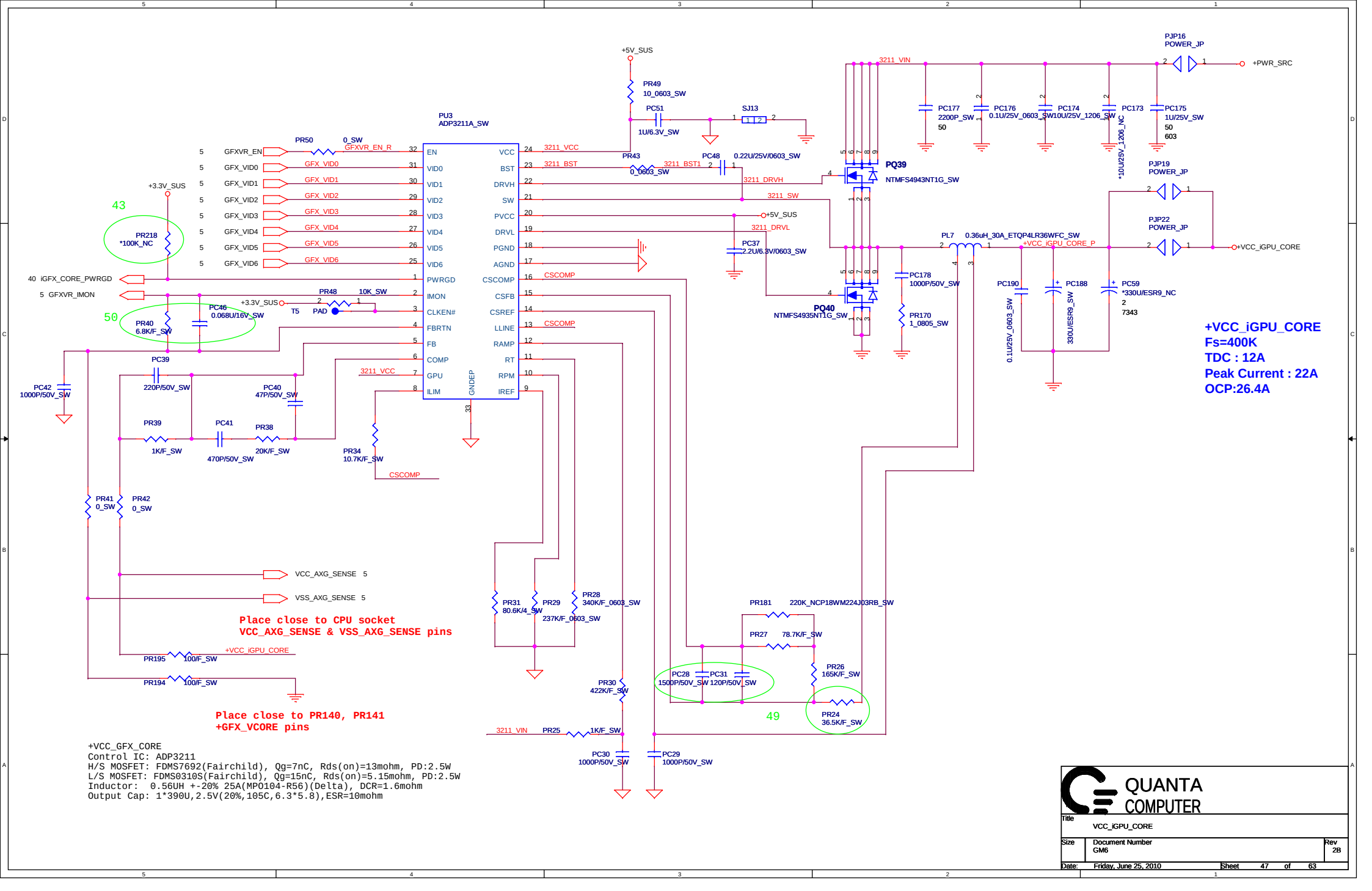


QUANTA COMPUTER		
Title	3.3V_ALW / 5V_ALW(TPS51427A)	
Size	Document Number GM6	Rev 2B
Date: Friday, June 25, 2010	Sheet 46 of 63	


PU3
ADP3211A_SW
EN
VID0
VID1
VID2
VID3
VID4
VID5
VID6
PWRGD
IMON
CLKEN#
FBRTN
FB
COMP
GPU
ILIM
GNDEP
VCC
BST
DRVH
SW
PVCC
DRVL
PGND
AGND
CSCOMP
CSFB
CSREF
LLINE
RAMP
RT
RPM
IREF
PQ39
NTMFS4943NT1G_SW
PQ40
NTMFS4935NT1G_SW
PL7
0.36uH_30A_ETQP4LR36WFC_SW
+VCC_iGPU_CORE
Fs=400K
TDC : 12A
Peak Current : 22A
OCP:26.4A
Place close to CPU socket
VCC_AXG_SENSE & VSS_AXG_SENSE pins
Place close to PR140, PR141
+GFX_VCORE pins
+VCC_GFX_CORE
Control IC: ADP3211
H/S MOSFET: FDMS7692(Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
Inductor: 0.56UH +-20% 25A(MPO104-R56)(Delta), DCR=1.6mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm
QUANTA COMPUTER
Title
VCC_iGPU_CORE
Size
Document Number
GM6
Rev
2B
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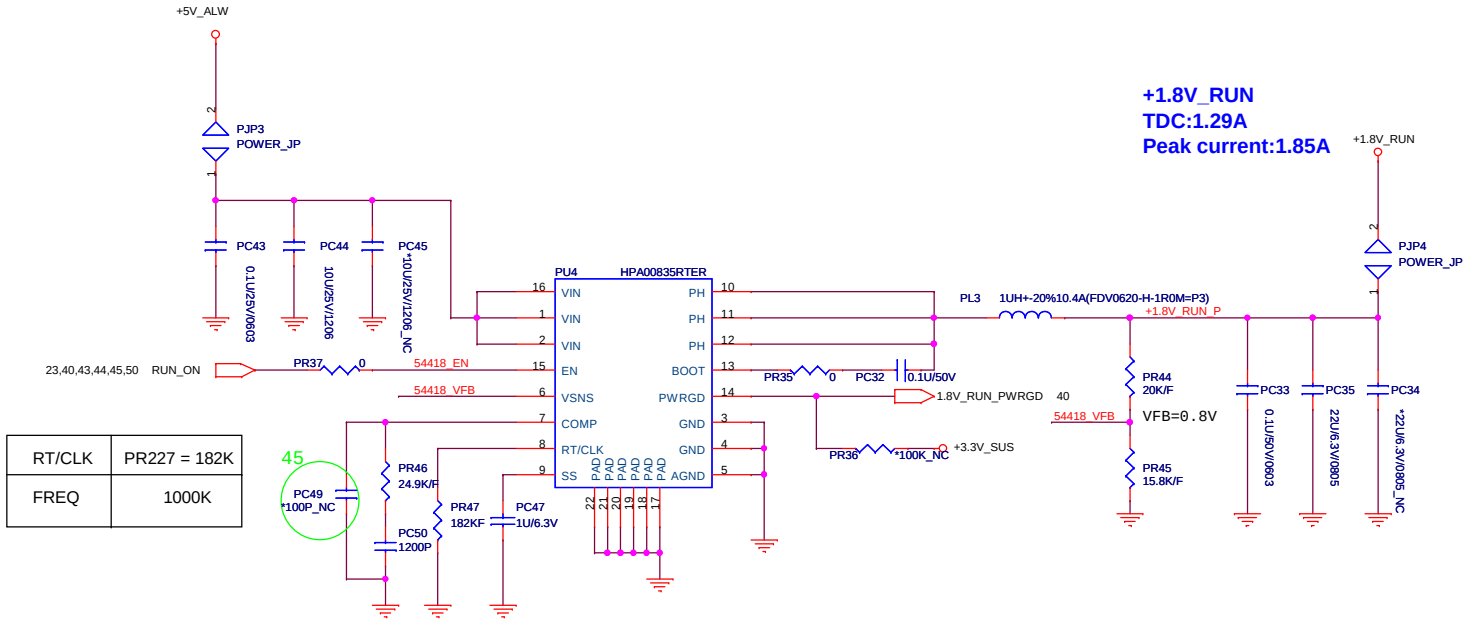
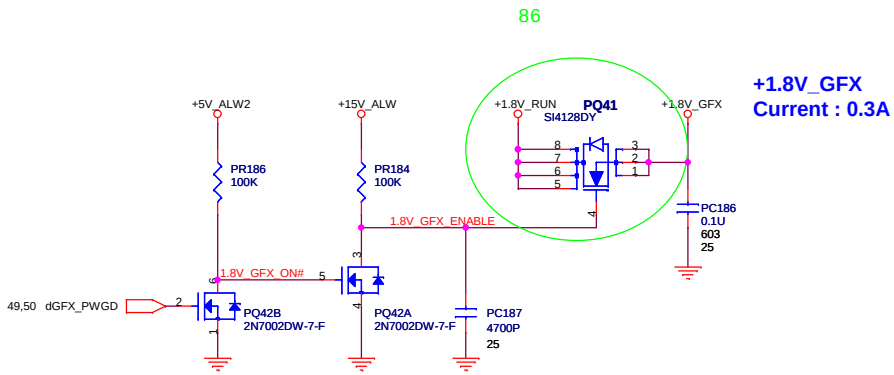
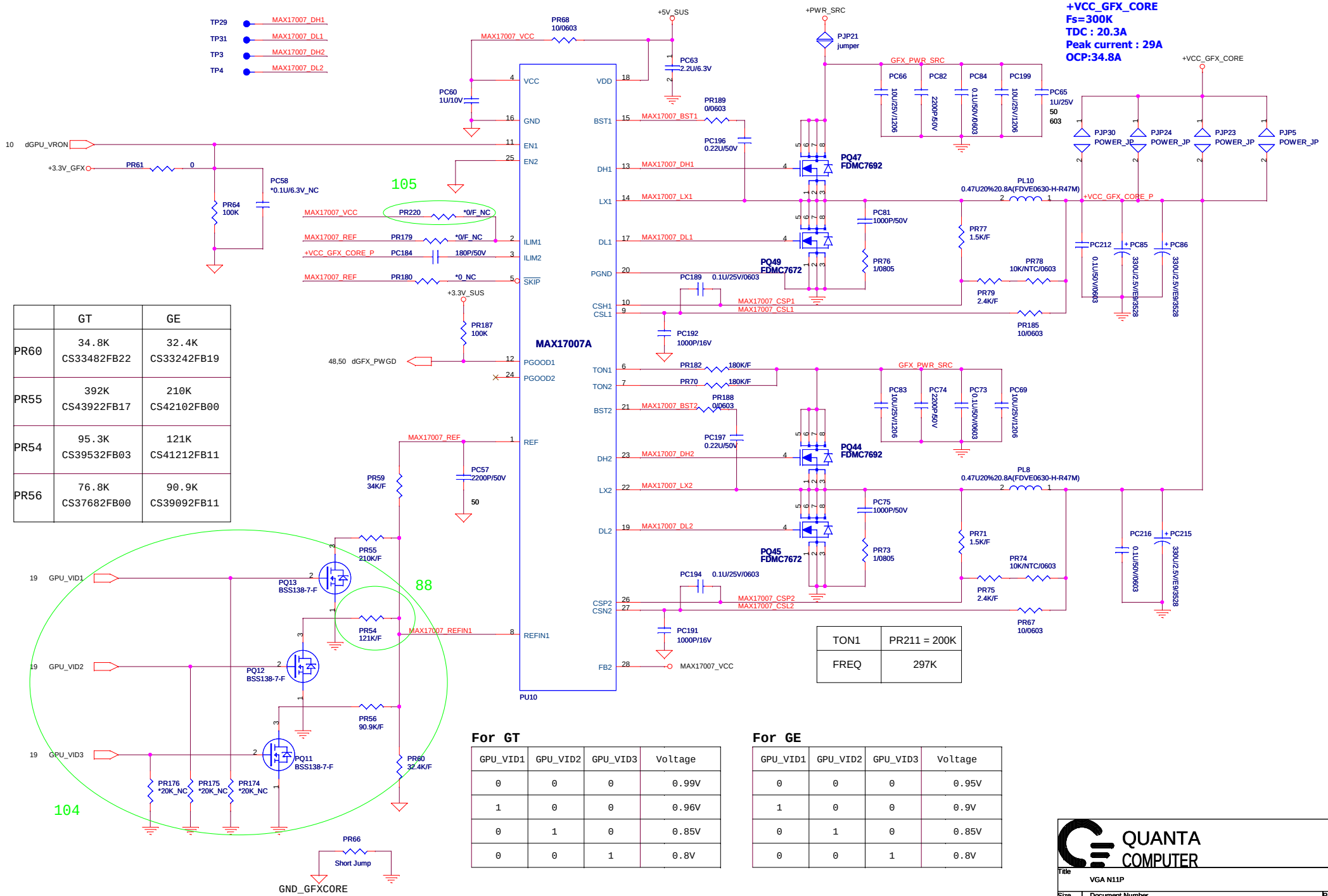


RT/CLK	PR227 = 182K
FREQ	1000K



QUANTA COMPUTER

Title	1.8V_RUN & 1.8V_RUN_GFX	
Size	Document Number GM6	Rev 2B
Date: Friday, June 25, 2010	Sheet 48 of 63	



	GT	GE
PR60	34.8K CS33482FB22	32.4K CS33242FB19
PR55	392K CS43922FB17	210K CS42102FB00
PR54	95.3K CS39532FB03	121K CS41212FB11
PR56	76.8K CS37682FB00	90.9K CS39092FB11

TON1	PR211 = 200K
FREQ	297K

For GT

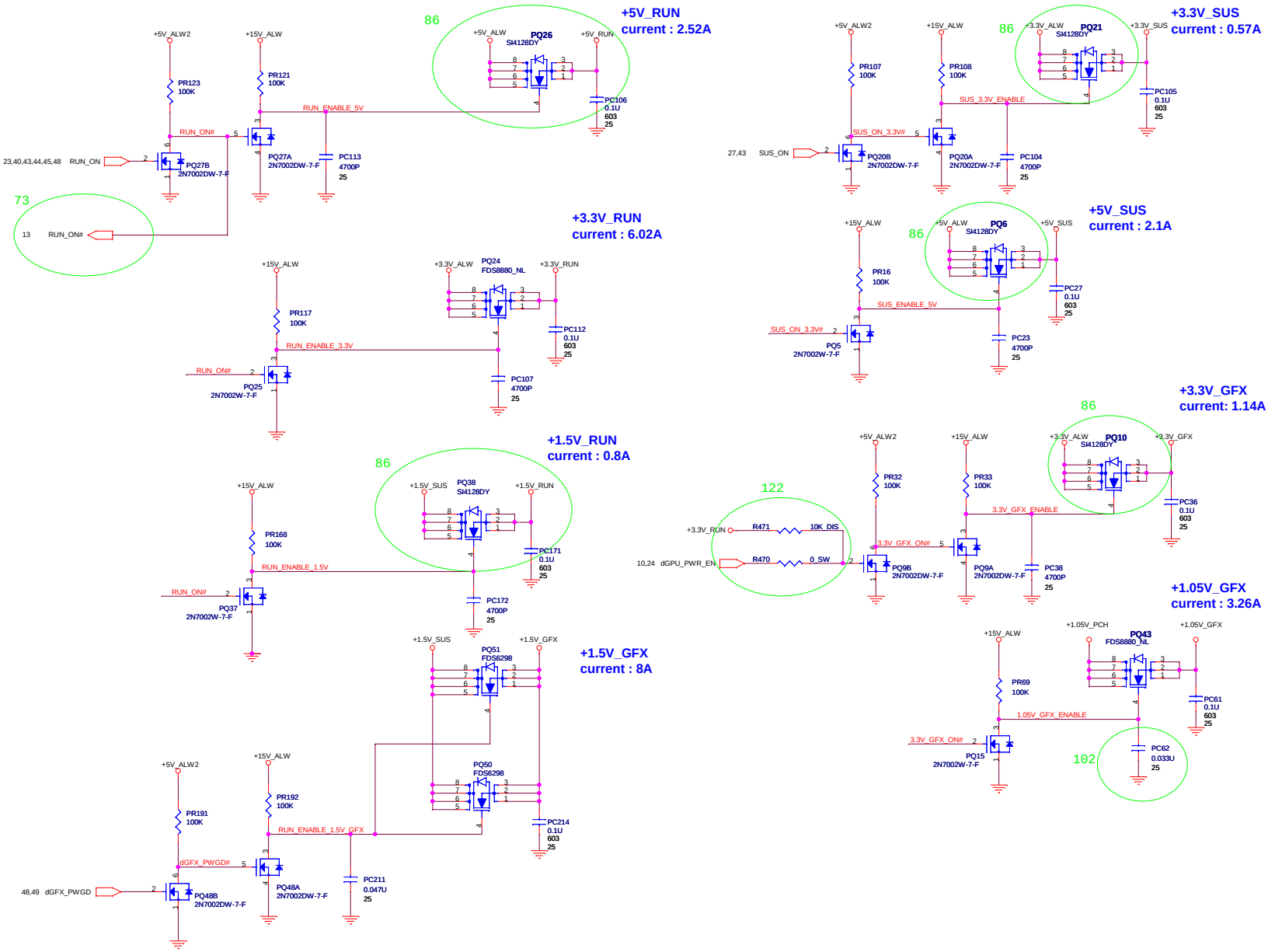
GPU_VID1	GPU_VID2	GPU_VID3	Voltage
0	0	0	0.99V
1	0	0	0.96V
0	1	0	0.85V
0	0	1	0.8V

For GE

GPU_VID1	GPU_VID2	GPU_VID3	Voltage
0	0	0	0.95V
1	0	0	0.9V
0	1	0	0.85V
0	0	1	0.8V

QUANTA COMPUTER

Title	VGA N11P	
Size	Document Number GM6	Rev 2B
Date: Friday, June 25, 2010	Sheet 49 of 63	



Title	RUN / SUS POWER SW
Size	Document Number GM6
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Date:	Friday, June 25, 2010
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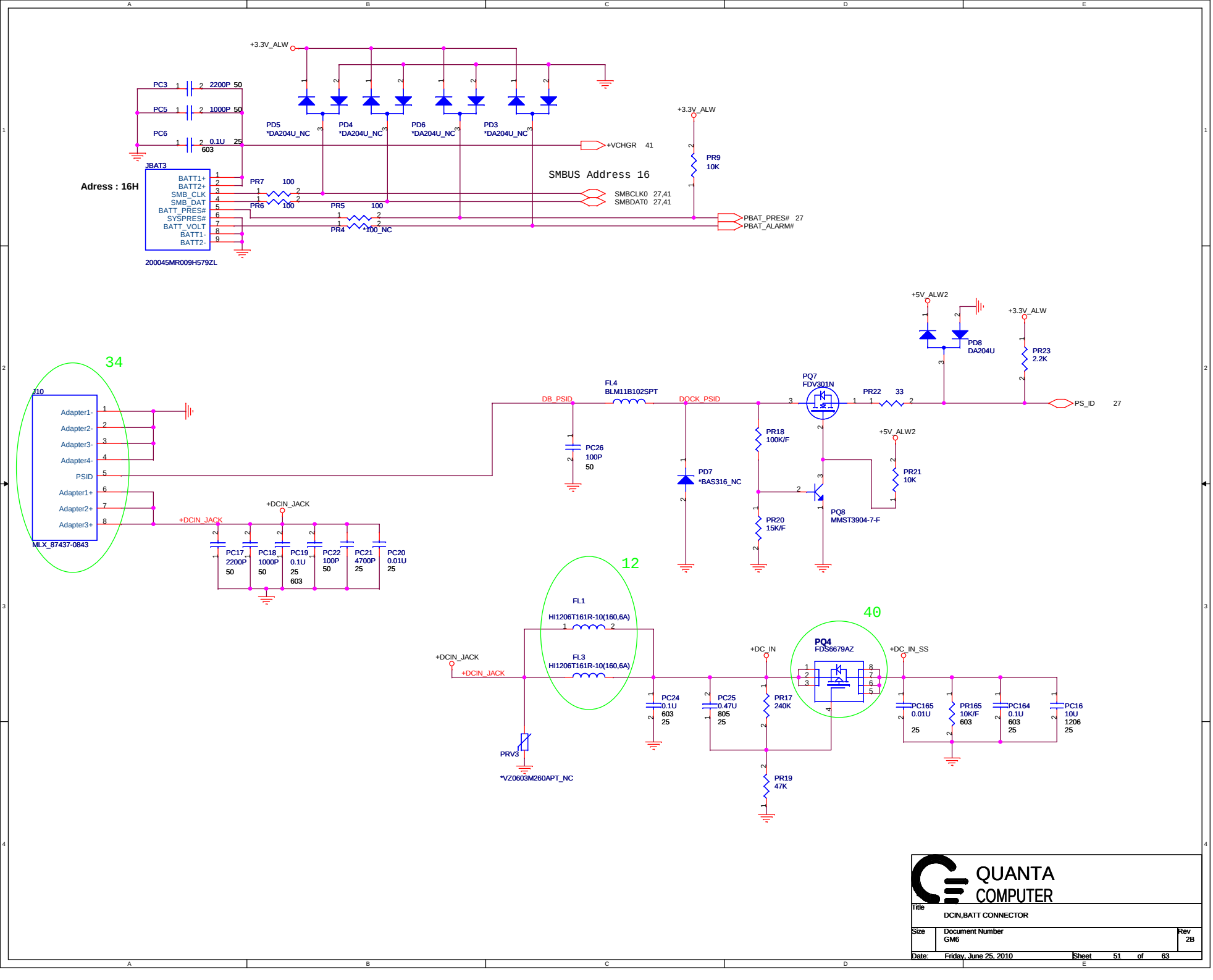
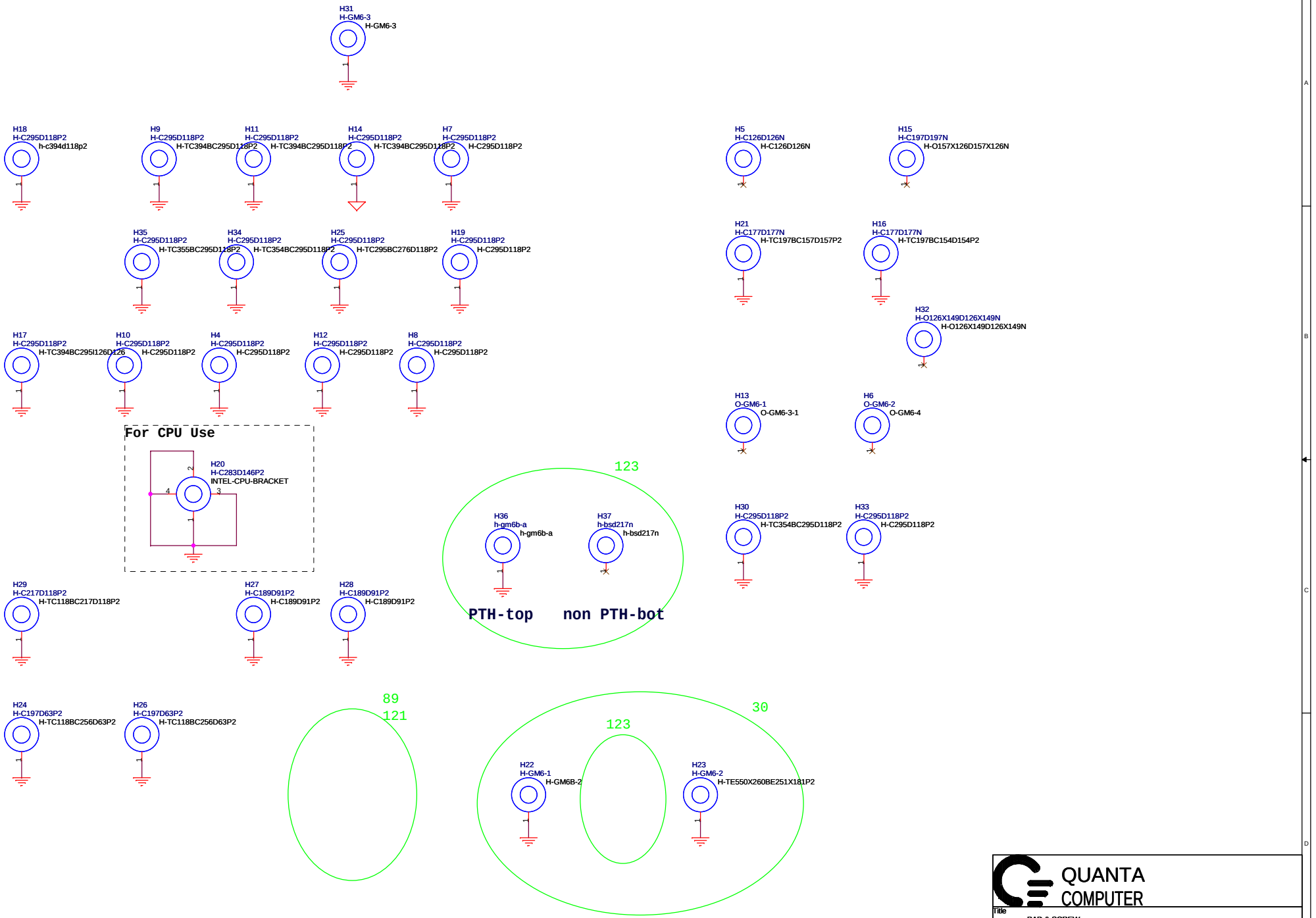


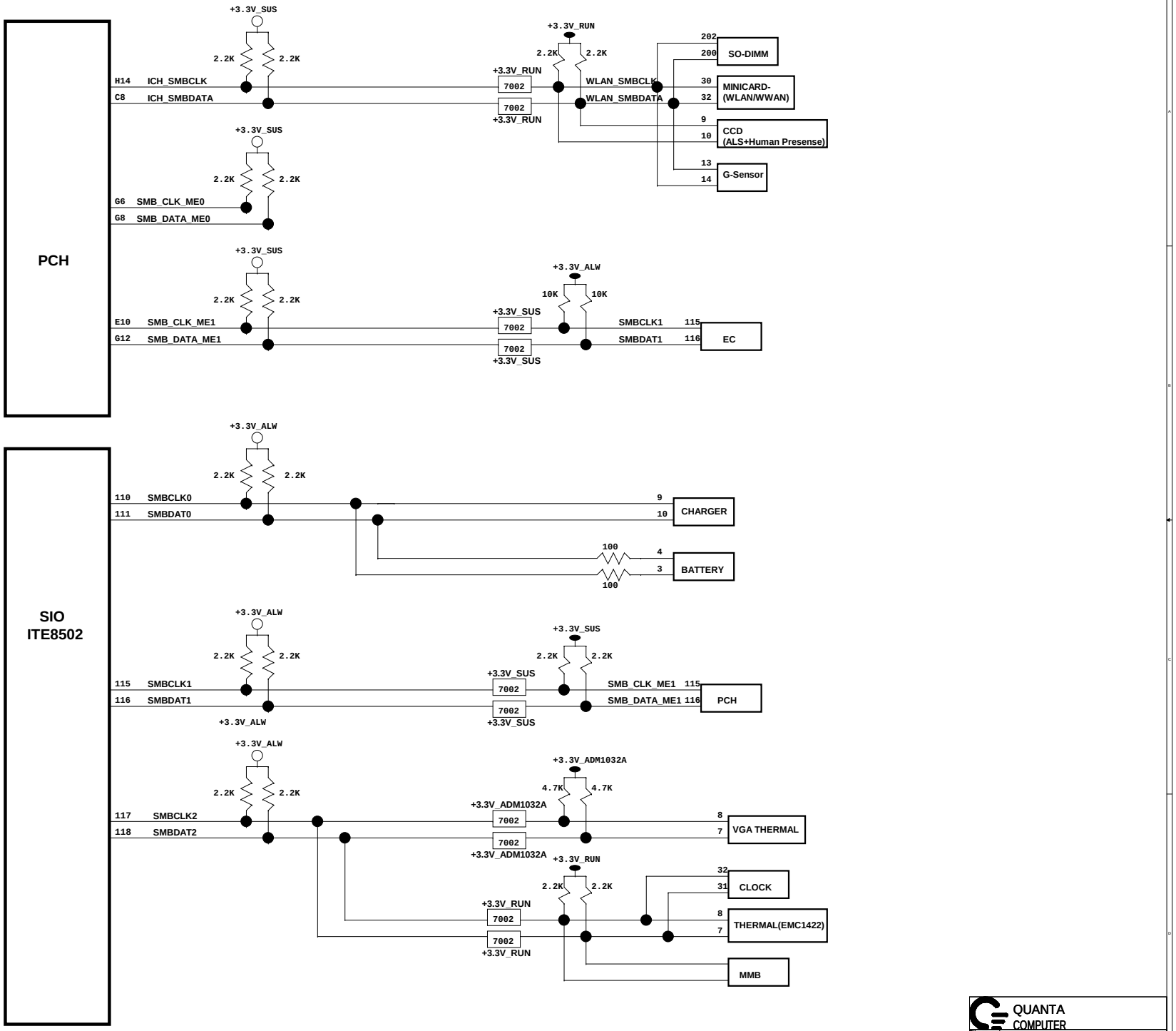
QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number GM6	Rev 2B
Date: Friday, June 25, 2010	Sheet 51 of 63	



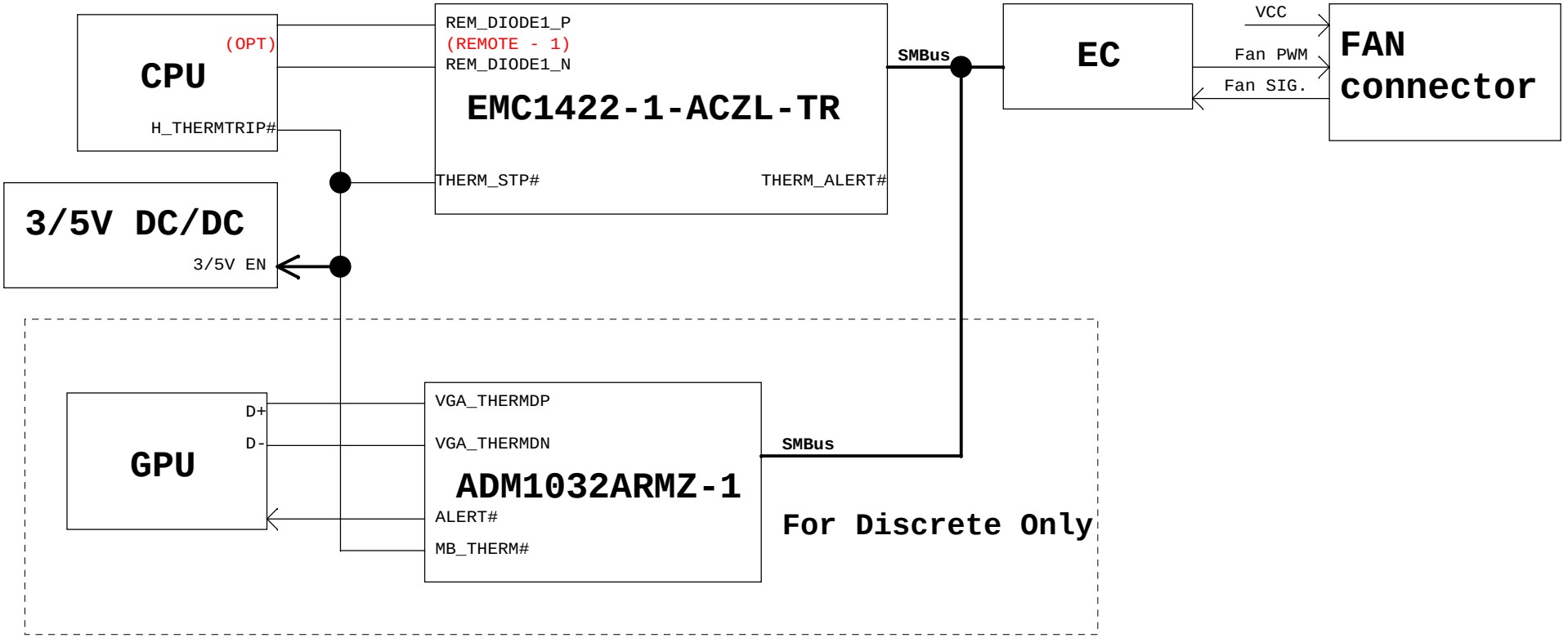
QUANTA COMPUTER

Title	PAD & SCREW	
Size	Document Number GM6	Rev 2B
Date: Thursday, June 24, 2010	Sheet 52 of 63	



QUANTA COMPUTER

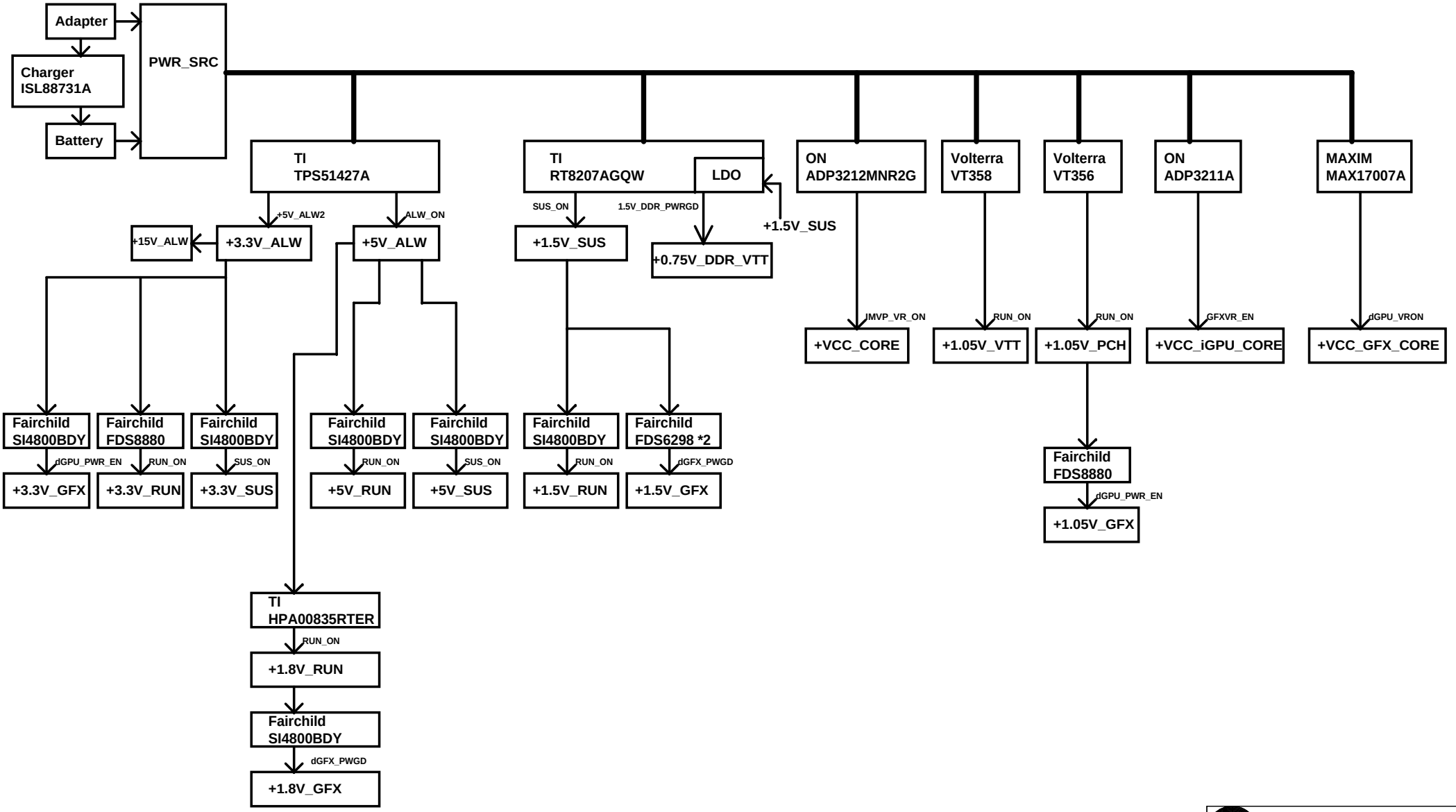
Title	SMBUS BLOCK	
Size	Document Number GM6	Rev 2B
Date: Thursday, June 24, 2010	Sheet 53 of 63	



QUANTA COMPUTER

Title	THERMAL MAP	
Size	Document Number GM6	Rev 2B
Date: Thursday, June 24, 2010	Sheet 54 of 63	

VER : 1A



QUANTA COMPUTER

Title	Power Block Diagram	
Size	Document Number GM6	Rev 2B
Date: Thursday, June 24, 2010	Sheet 55 of 63	

FM9 Power Design Block Diagram 2009/12/28

Optimus
DIS only

(1) (1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) (2) SYS_PWR_SW#
(3) (3) 3.3V_ALW_ON, ALW_ON
(4) (4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) (5) SUS_ON
(6) (6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) (7) PCH_RSMRST#
(8) (8) SIO_PWRBTN#
(9) (9) SIO_SLP_S5#, SIO_SLP_S3#
(10) (10) GFXVR_EN
(11) (11) +VCC_iGPU_CORE, iGFX_CORE_PWRGD
(12) (12) RUN_ON_1(RUN_ON)
(13) (13) +0.75V_DDR_VTT
(14) (14) +3.3V_RUN, +5V_RUN,
+1.05V_VTT,+1.05V_PCH, +1.8V_RUN, +1.5V_RUN,
(19) (15) HWPG, H_VTTPWRGD
(20) (16) IMVP_VR_ON
(21) (17) +VCC_CORE, IMVP_PWRGD, VR_PWRGD_CLKEN#
(22) (18) PCH_PWRGD
(23) (19) PM_DRAM_PWRGD
(24) (20) CLK_CPU_BCLK(PCH to CPU)
(25) (21) H_PWRGOOD
(26) (22) PLTRST#(PCI_PLTRST#)
(23) dGPU_PWR_EN(PCH GPIO 56)
(15) (24) +3.3V_GFX, +1.05V_GFX
(25) dGPU_VRON(PCH GPIO 35)
(16) (26) +VCC_GFX_CORE, dGFX_PWGD
(17) (27) +1.5V_GFX , +1.8V_GFX
(18) (27) dGPU_PWROK

Power Jack
Adapter input
+DC_IN_SS
SI4835
+PWR_SRC
Charger
ISL88731
Page 41
+VCHGR
Battery
SI4835
+PWR_SRC

+5V_VCC1 (from +5V_ALW2 for Max so;ution)
for TI solution, IC can supply 5V by itself.

SYSTEM POWER
TPS51427A
Page 46
LDO
VR
+5V_ALW2
+3.3V_ALW
+5V_ALW
+3.3V_ALW_ON(From 3V_ALW ON POWER LOGIC)
ALW_ON(For +5V_ALW and turn on +15V_ALW)
3V_ALW_PWRGD
5V_ALW_PWRGD

+5V_ALW → Diode & Cap (Page 46) → +15V_ALW

VRAM DDR3 POWER
RT8207AGQW
Page 43
VR
LDO
+1.5V_SUS
1.5V_DDR_PWRGD
+0.75V_DDR_VTT
SUS_ON
RUN_ON

CPU Memory Control & I/O Power
VT358
Page 44
VR
+1.05V_VTT
1.05V_VTT_PWRGD
RUN_ON

GFX CORE POWER
MAX17007A
Page 49
VR
+VCC_GFX_CORE
dGFX_PWGD
dGPU_VRON
+3.3V_GFX

CPU CORE POWER
ADP3212MNR2G
Three PHASE SOLUTION
Page 42
VR
+VCC_CORE
IMVP_PWRGD
VR_PWRGD_CLKEN#
IMVP_VR_ON

PCH core power
VT356
Page 45
VR
+1.05V_PCH
1.05V_PWRGD
RUN_ON

CPU VCCPLL
HPA00835RTER
Page 44
VR
1.8V_RUN
1.8V_RUN_PWRGD
RUN_ON

+VCC_iGPU_CORE
ADP3211A
Page 47
VR
GFXVR_EN
+VCC_iGPU_CORE
iGFX_CORE_PWRGD

SI4800 Page 50: +5V_ALW → +5V_SUS; SUS_ON
SI4800 Page 50: +3.3V_ALW → +3.3V_SUS; SUS_ON
SI4800 Page 50: +5V_ALW → +5V_RUN; RUN_ON
FDS8880 Page 50: +3.3V_ALW → +3.3V_RUN; RUN_ON
SI4800 Page 50: +3.3V_ALW → +3.3V_GFX; dGPU_PWR_EN; +3.3V_RUN
SI4800BDY Page 50: +1.5V_SUS → +1.5V_RUN; RUN_ON
FDS8880 Page 52: +1.05V_PCH → +1.05V_GFX; dGPU_PWR_EN; +3.3V_RUN
FDS6298 x 2 Page 50: +1.5V_SUS → +1.5V_GFX; dGFX_PWGD
SI4800BDY Page 48: +1.8V_RUN → +1.8V_GFX; dGFX_PWGD

Reset Circuit Page 40
Inverter
AND Gate
Wire AND Page 40
VR_PWRGD_CLKEN#
1.5V_DDR_PWRGD
RUN_ON_1
1.05V_VTT_PWRGD
1.05V_PWRGD
dGPU_PWROK
iGFX_CORE_PWRGD
1.8V_RUN_PWRGD
CK_PWRGD_R
RUN_ON
HWPG
H_VTTPWRGD

CLK GEN Page 15
CK_PWRGD_R

EC IT8512 Page 27
SYS_PWR_SW#
IMVP_PWRGD
HWPG
3.3V_ALW_ON
ALW_ON
SUS_ON
SIO_PWRBTN#
PCH_RSMRST#
SIO_SLP_S5#
SIO_SLP_S3#
PCH_PWRGD
RUN_ON_1
IMVP_VR_ON

PCH Page 7~12
PM_DRAM_PWRGD
CLK_CPU_BCLK
H_PWRGOOD
PLTRST#(PCI_PLTRST#)

CPU Page 3~6
GFXVR_EN
H_VTTPWRGD

QUANTA COMPUTER

Title	Power sequence Block	
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