ZHG SYSTEM DIAGRAM

AMD Smarter Choice

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

EDP@ -----> eDP panel
LVDS@ -----> LVDS panel
HDT@ -----> HDT fucntion
3G@ -----> 3G function
U2@ -----> USB2.0 only
U3@ -----> USB3.0 function
885S@ -----> EC885S
885L@ -----> EC885L

DDR3- SODIMM1
DDR3-1066 PAGE 6

DDR3 Channel A

AMD Brazos2.0
C60 TDP~9W
FT1
19mmX19mm 413pin BGA
PAGE 3,4,5

TDP1
VGA
LTDP0

HDMI PAGE 13
CRT PAGE 12
LVDS PAGE 12
eDP (Optional) PAGE 12

CPU (PROCHOT)
E.C. (CPUFAN#)
FAN SCH. PAGE 19

CPU SideBand TemperatureSense I2C

PCI-Expresss
P1 P2 P0

UMI x4

PCLK_DEBUG

Mini Card
WLAN & Debug
PAGE 15

Mini Card
3G
PAGE 15

LAN
Realtek
RTL8105
(10/100)
PAGE 16
25MHz

RJ45 PAGE 16

AMD
Hudson-M3L
24.5mmX24.5mm, 656pin BGA
TDP~4.7W
PAGE 7,8,9,10,11

SATA - HDD PAGE 17
SATA0 150MB
3 Gb/s

SIM PAGE 15

USB2.0
P7 P1 P4
P6 P0

Web-Camera PAGE 12

USB2.0/3.0 Port
MB x1
PAGE 18

FFC

IO D/B
P5 P3 P10

CardReader
AU6435

USB2.0 Port
DB x2

12MHz

INT MIC

AUDIO CONN
Combo Jack

PAGE 18

USB3.0 P0

32.768KHz
25MHz

LPC
Azalia

CLK_PCI_EC
KBC
NPCE885
PAGE 20

CPU SideBand TemperatureSense I2C

Audio CODEC
Realtek
ALC271X-VB6
PAGE 16

Keyboard TouchPad (Image Sensor) PAGE 19

SPI ROM PAGE 9

Speaker PAGE 16

CHARGER (BQ24707A) PAGE 21

AMD CPU CORE (OZ8380) PAGE 23 — *CPU*

1.-05V (TPS51211) PAGE25 — *NB*

DDR 1.5V(TPS51216) PAGE 26

SYSTEM 5V/3V (RT8223P) PAGE 22

1.1V(TPS51211) PAGE 24

Discharge /Thermal protection PAGE 27

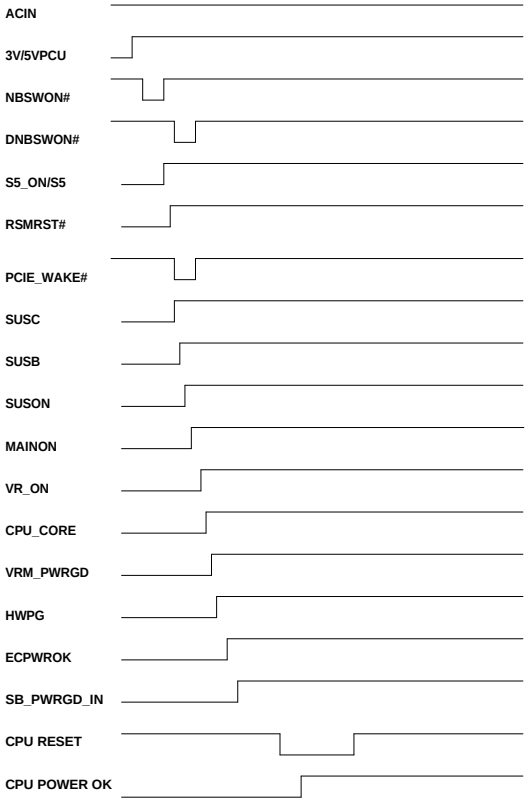
Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	Block Diagram	1A

Date: Tuesday, January 03, 2012 Sheet 1 of 28

INDEX

Power Sequence



Hudson M3L SMBUS

A68M SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD26 AE25	DDR / WLAN / 3G / Image Sensor
SCLK1 SDATA1 (+3V_S5)	T7 R7	Not used
SMB_EC_CLK SMB_EC_DAT (+3V_S5)	H19 G19	Charger / Battery
SB_SCLK3 SB_SDATA3 (+3V_S5)	G22 G21	APU

KBC(EC) SMBUS

NPCE885 SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	70 69	Battery / Charger
APU_SIC_EC APU_SID_EC (+3VPCU)	67 68	APU

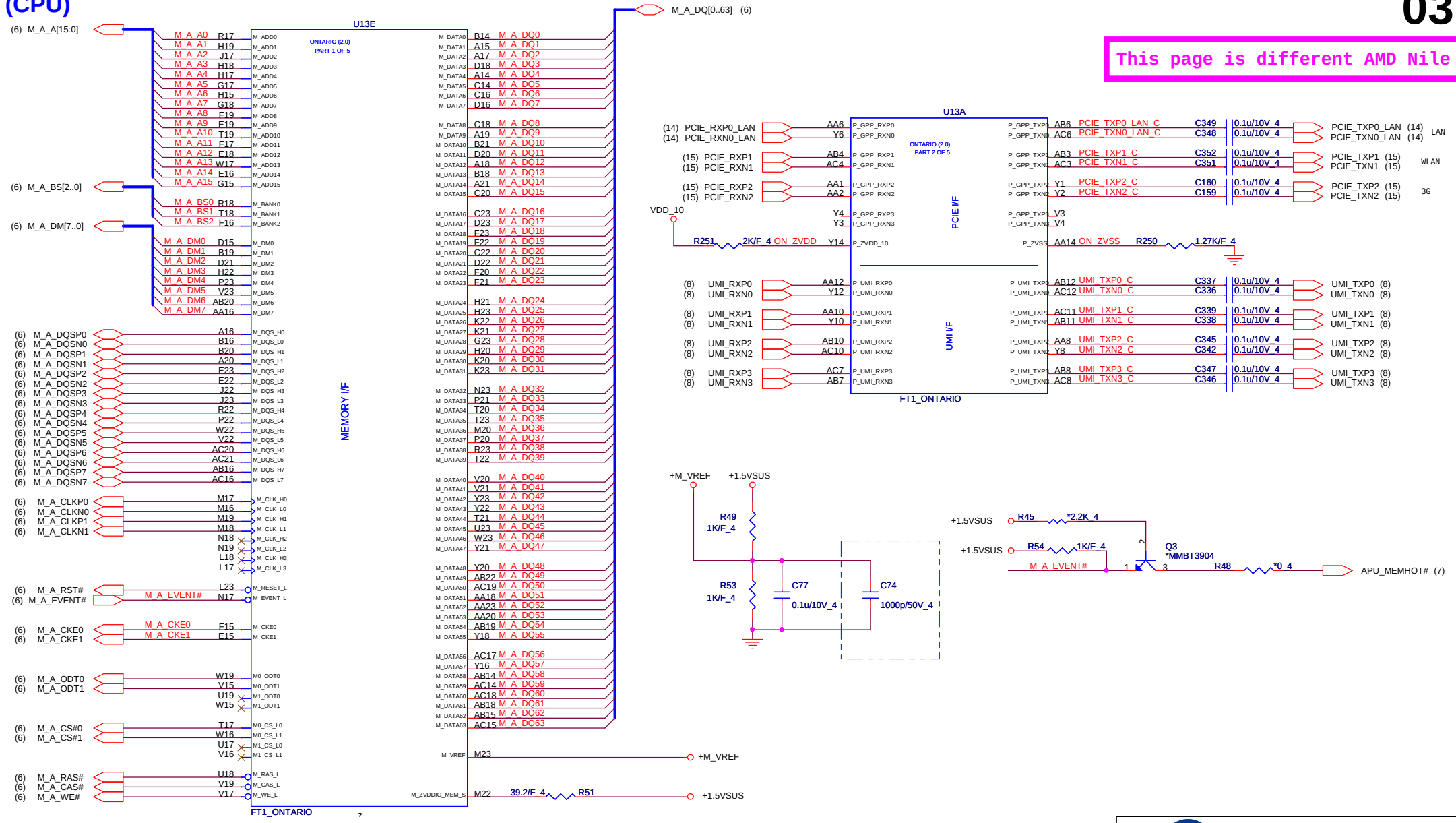
Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	System Information	1A
Date: Tuesday, January 10, 2012	Sheet 2 of 28	

(CPU)

03

This page is different AMD Nile



P/N	Item Description
AJ00C60VT00CPU(413P)	CMC60AFPB22GV 1.0G(BGA)
AJ00C60VT01CPU(413P)	CMC60AFPB22GV 1.0G(BGA)STN BSQ

Quanta Computer Inc.

PROJECT : ZHG

Size	Document Number	Rev
	ONTARIO MEM & PCIE I/F(1/3)	1A
Date: Tuesday, January 10, 2012	Sheet 3 of 28	

(CPU)

	3	2	1	0	DP AUX+	DP AUX-
HDMI	Clock	CH0	CH1	CH2	DDC Clock	DDC Data
LVDS Panel	Clock	CH0	CH1	CH2	DDC Clock	DDC Data
eDP Panel	ML3	ML2	ML1	ML0	AUX+	AUX-

Eliminate the HDMI Output Disable Strapping Configuration
TEST35 (ball H4) Remove "1K pull down" to VSS

Enable HDMI Output
TEST35 (ball H4) Add 1K "pull up" to the VDD_18 power rail

DIFFERENTIAL ROUTING

VID Override Circuit

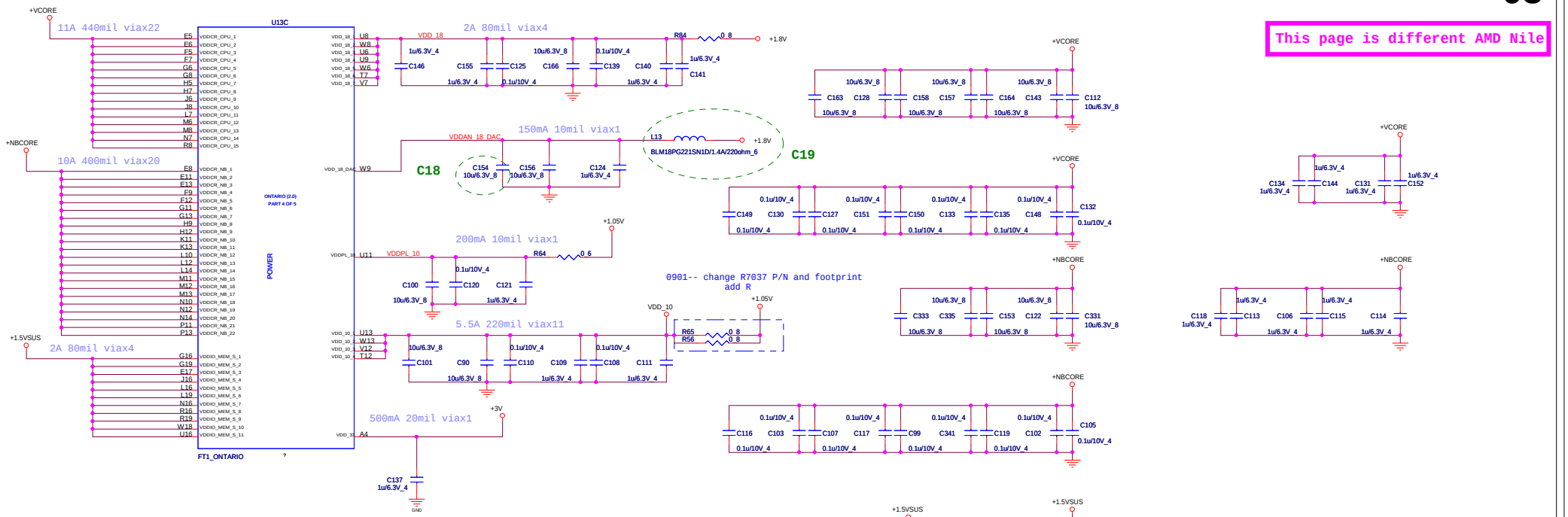
for normal operation
open all switches

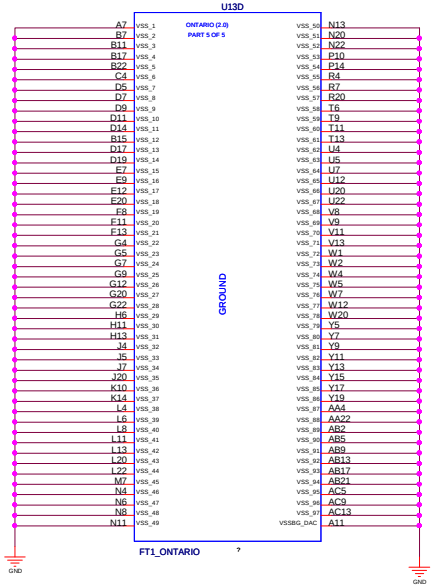
HDT+ Connector(CPU)

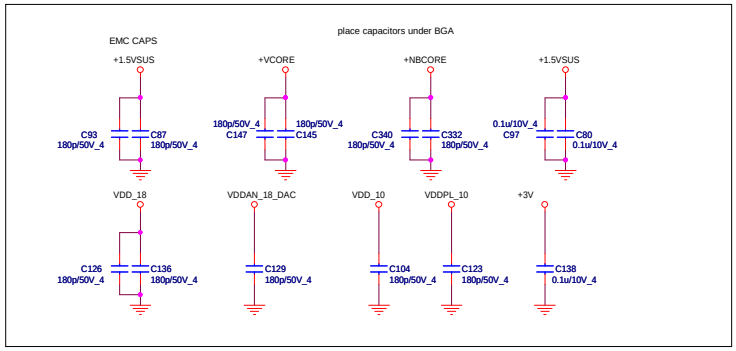
HDT+ HEADER / PLACE ON TOP

Quanta Computer Inc.			
PROJECT : ZHG			
Size	Document Number		Rev
	ONTATIO DISPLAY/CLK/MI(2/3)		1A
Date: Wednesday, January 11, 2012	Sheet 4 of 28		

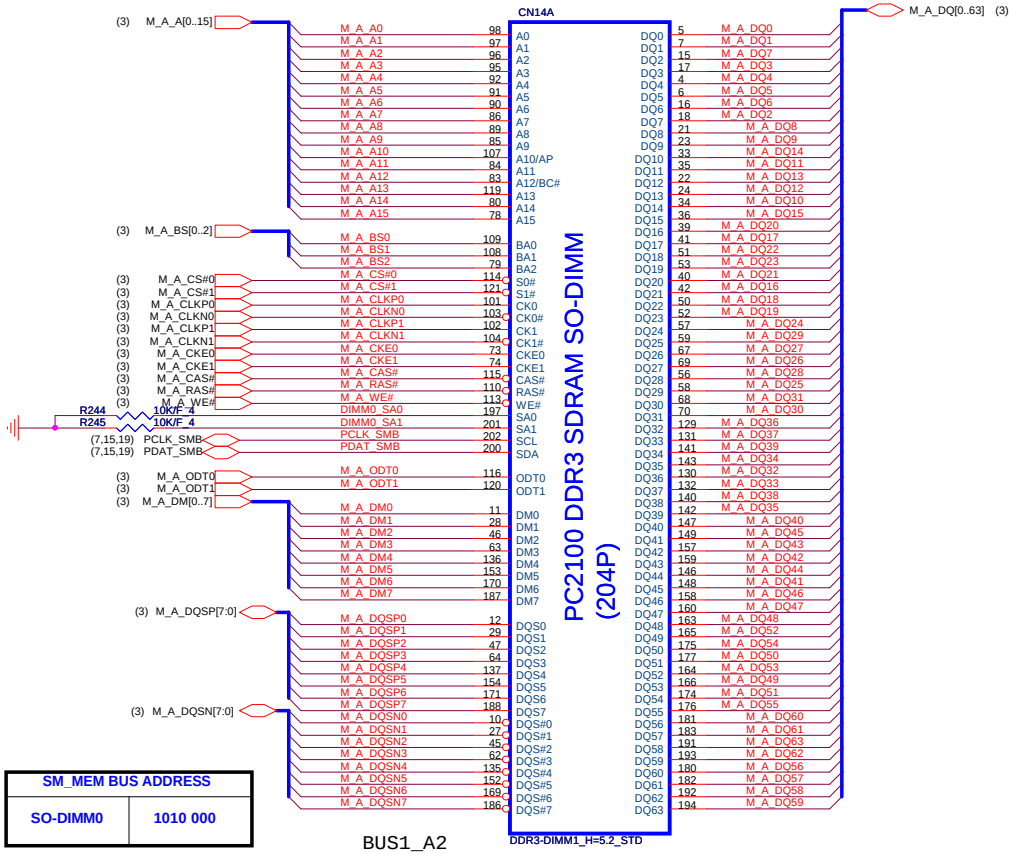
This page is different AMD Nile



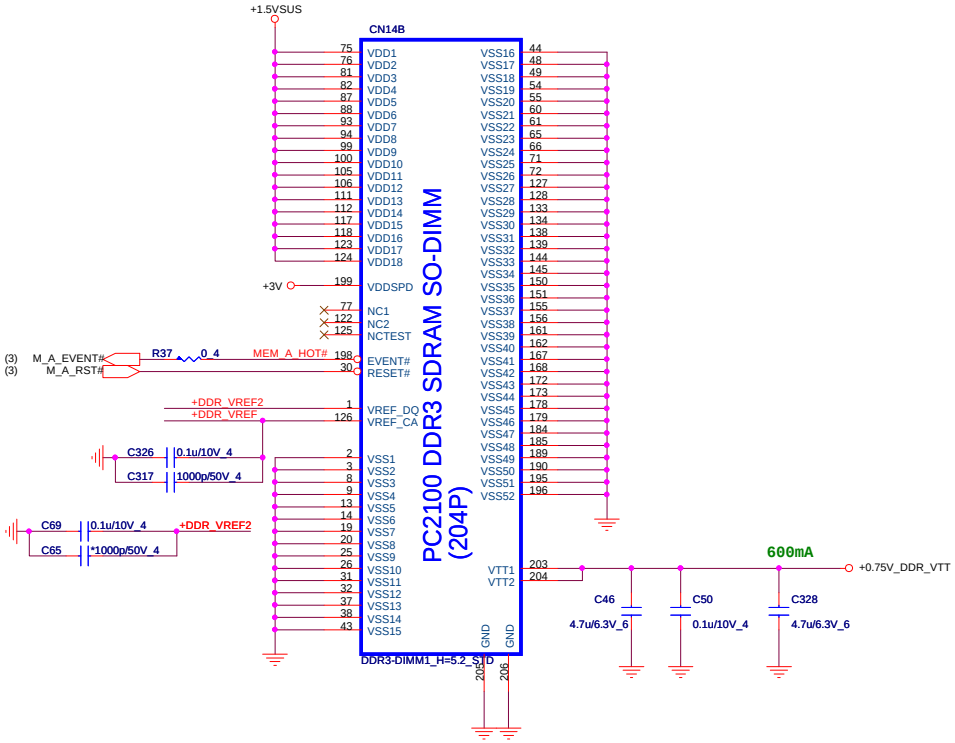


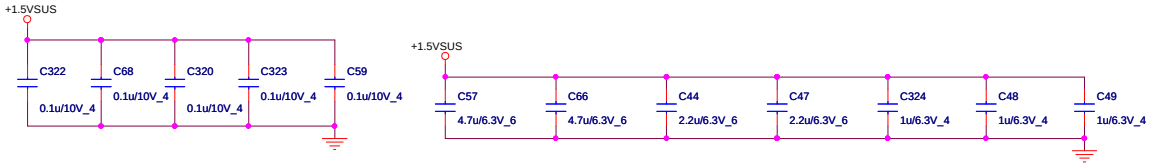


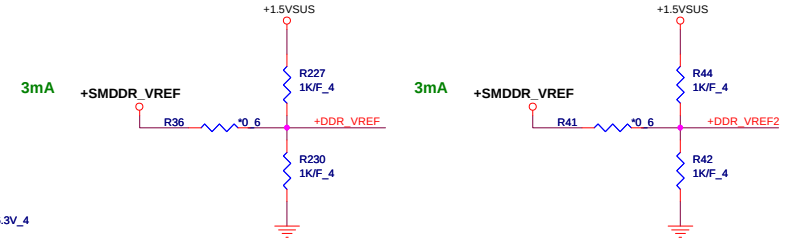
Quanta Computer Inc.			
PROJECT : ZHG			
Size	Document Number		Rev
	ONTARIO POWER & DECOUP(3/3)		1A
Date: Tuesday, January 10, 2012		Sheet 5 of 28	

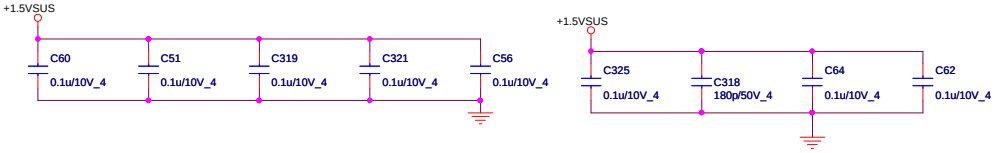


SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000









Quanta Computer Inc.		
PROJECT : ZHG		
Size	Document Number: DDR3 SO-DIMM (STD)	Rev: 1A
Date: Tuesday, January 10, 2012	Sheet 6 of 28	

NC,no install by default

Internal have PD

For Dimm, WLAN, TP

Integrated 8.2-kΩ PU

GEVENT12# ~18# are +3V_S5

HDaudio interface are +3V_S5

GPIO193 ~196 are +3V_S5

Provided test points from checklist

Note:LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported

Note: USB P/N pairs with trace lengths up to 10"

VGA_PD for power control

To Azalia

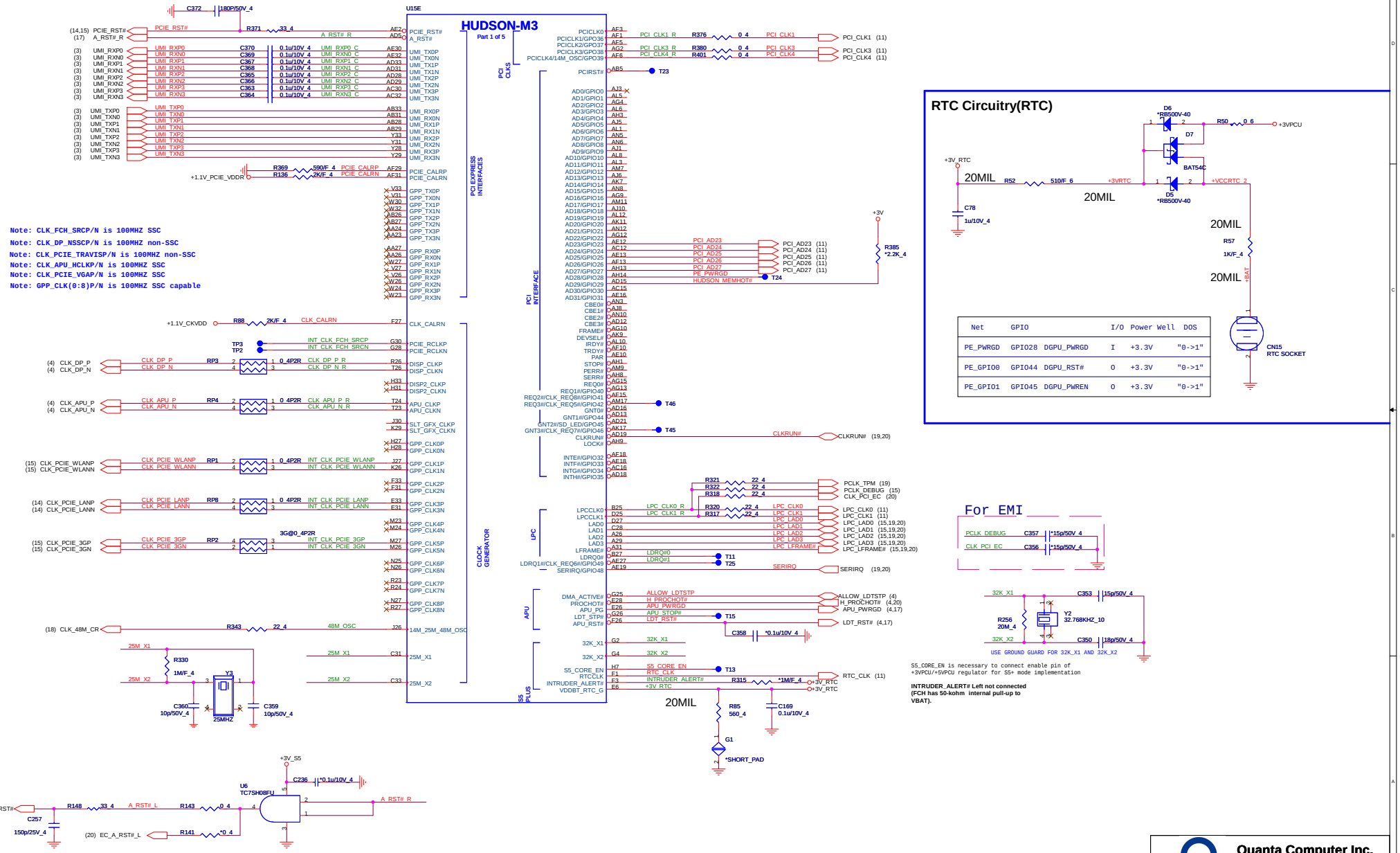
EC	FCH	Device	I2C_Device(S)		
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		APU			ALL
I2Ce_3(M)					
	I2Cf_3(M)	APU			S5
	I2Cf_1(M)				S5
	I2Cf_0(M)	DDR	WLAN/3G	Image Sensor	S0

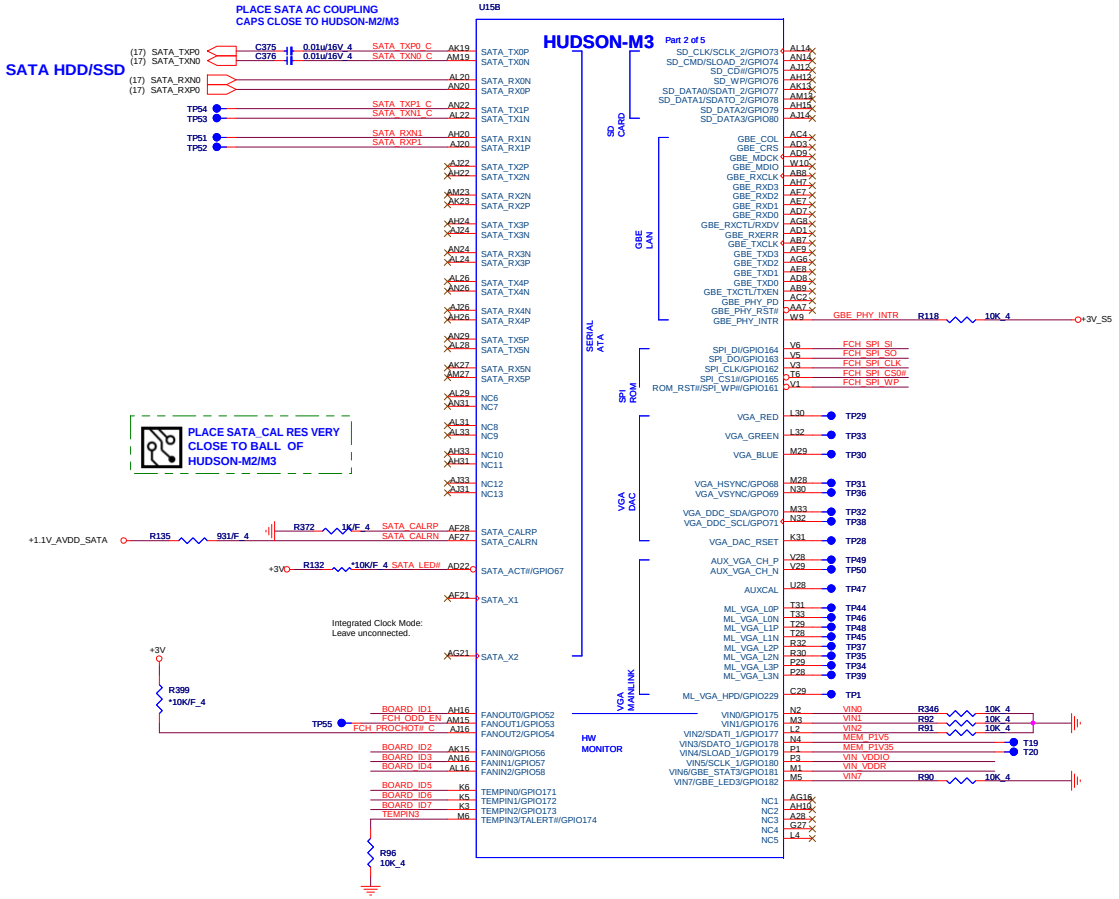
EC will Conflict with FCH. Do not mount

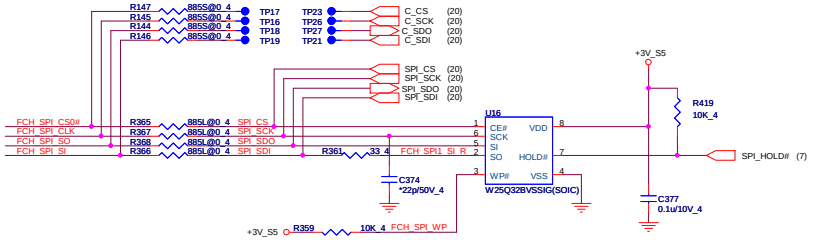
Quanta Computer Inc.
PROJECT : ZHG

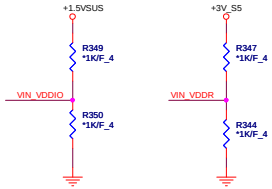
Size	Document Number	Rev
	FCH 1/5(GPIO/USB/AZ)	1A

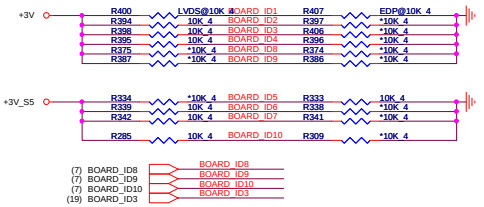
Date: Tuesday, January 10, 2012 Sheet 7 of 28


HUDSON-M3
Part 1 of 5
U15E
Note: CLK_FCH_SRCP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_PCIE_VGAP/N is 100MHZ SSC
Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable
RTC Circuitry(RTC)
Net GPIO I/O Power Well DOS
PE_PWRGD GPIO28 DGPU_PWRGD I +3.3V "0->1"
PE_GPIO0 GPIO44 DGPU_RST# O +3.3V "0->1"
PE_GPIO1 GPIO45 DGPU_PWREN O +3.3V "0->1"
CN15
RTC SOCKET
For EMI
S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation
INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).
Quanta Computer Inc.
PROJECT : ZHG
FCH 2/5(ACPI/PCI/CLK)
Rev 1A
Tuesday, January 10, 2012
Sheet 8 of 28









BOARD ID SETTING

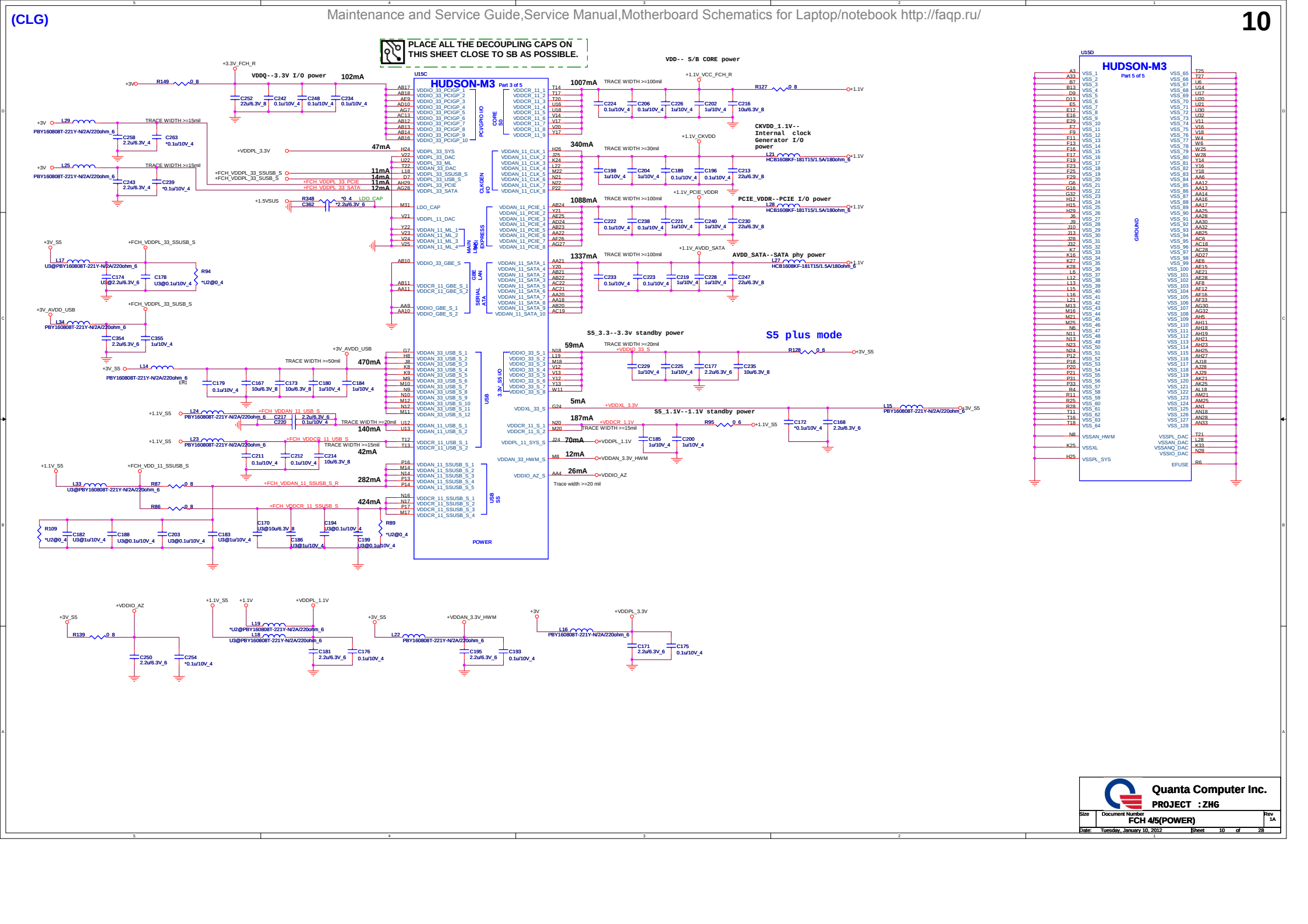
BOARD_ID1	LCD
0	eDP
1	LVDS

BOARD_ID3	For TP
0	ELAN
1	Synaptics

Quanta Computer Inc.
PROJECT : ZHG

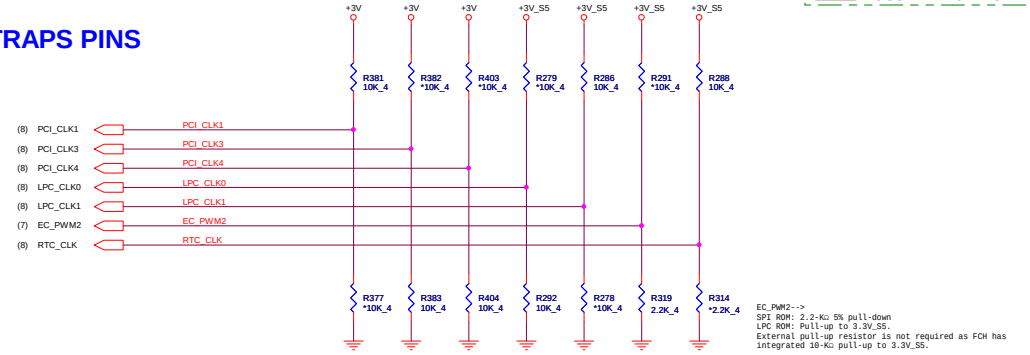
Size	Document Number	Rev
	FCH 3/5(SATA/VGA/GND/SPI)	1A

Date: Wednesday, January 11, 2012 Sheet 9 of 28


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
HUDSON-M3
Part 3 of 5
VDDQ--3.3V I/O power
VDD-- S/B CORE power
CKVDD_1.1V--Internal clock Generator I/O power
PCIE_VDDR--PCIE I/O power
AVDD_SATA--SATA phy power
S5 plus mode
S5_3.3--3.3v standby power
S5_1.1V--1.1V standby power
HUDSON-M3
Part 5 of 5
GROUND
Quanta Computer Inc.
PROJECT :ZHG
FCH 4/5(POWER)
Tuesday, January 10, 2012

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

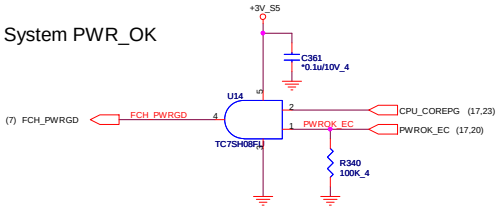


Remove PCI_CLK2 function

REQUIRED STRAPS

	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

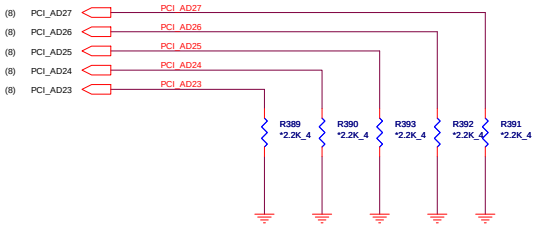
System PWR_OK



FCH PWRGD CKT

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



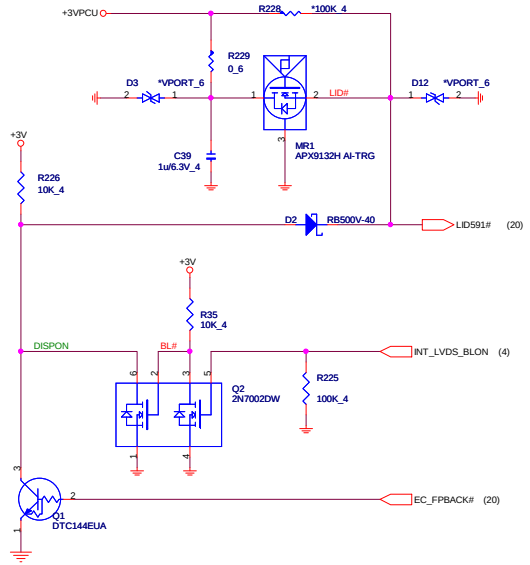
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Quanta Computer Inc.
PROJECT : ZHG

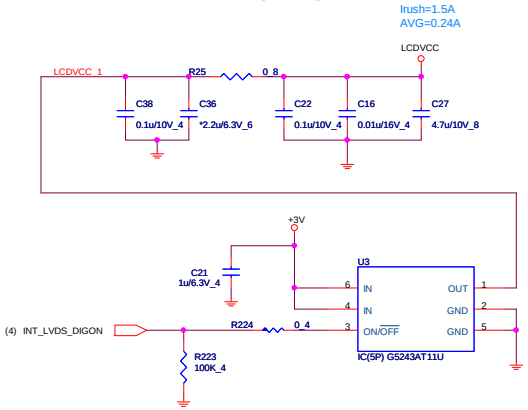
Size	Document Number	Rev
	FCH 5/5(STRAP & PWRGD)	1A

Date: Tuesday, January 10, 2012 Sheet 11 of 28

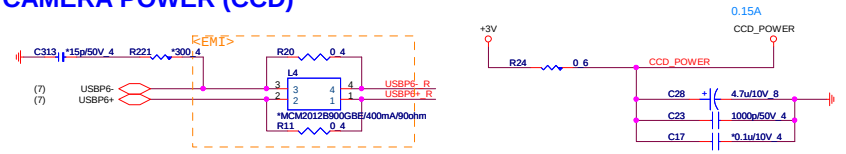
HALL IC (HSR)



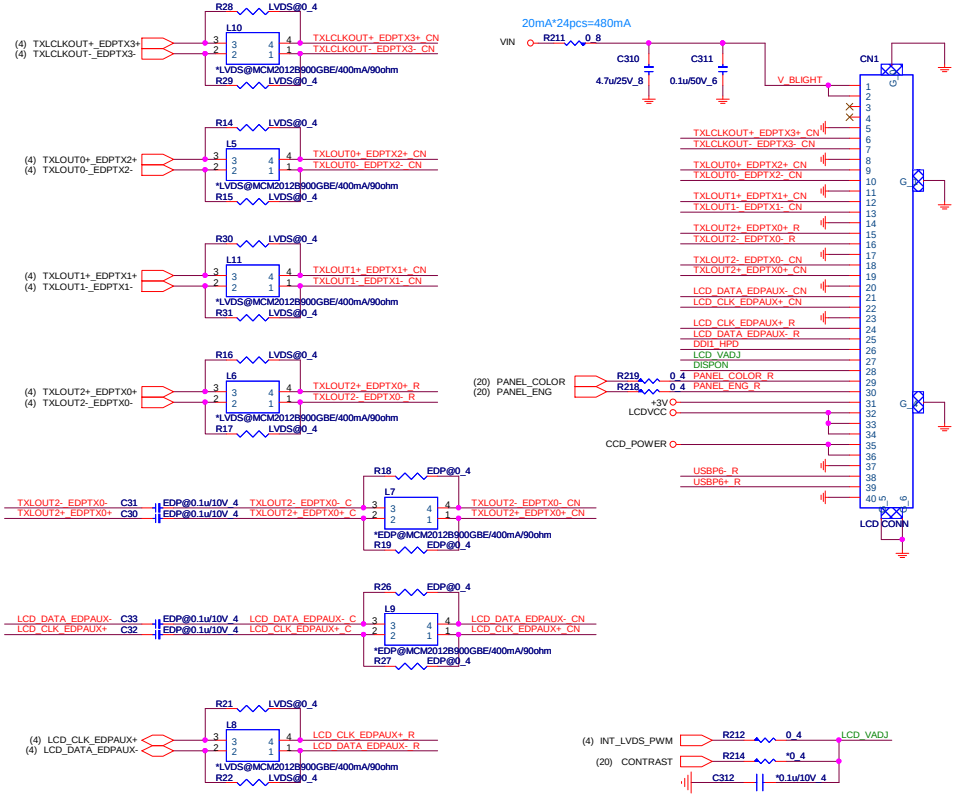
LCD POWER SWITCH (LDS)



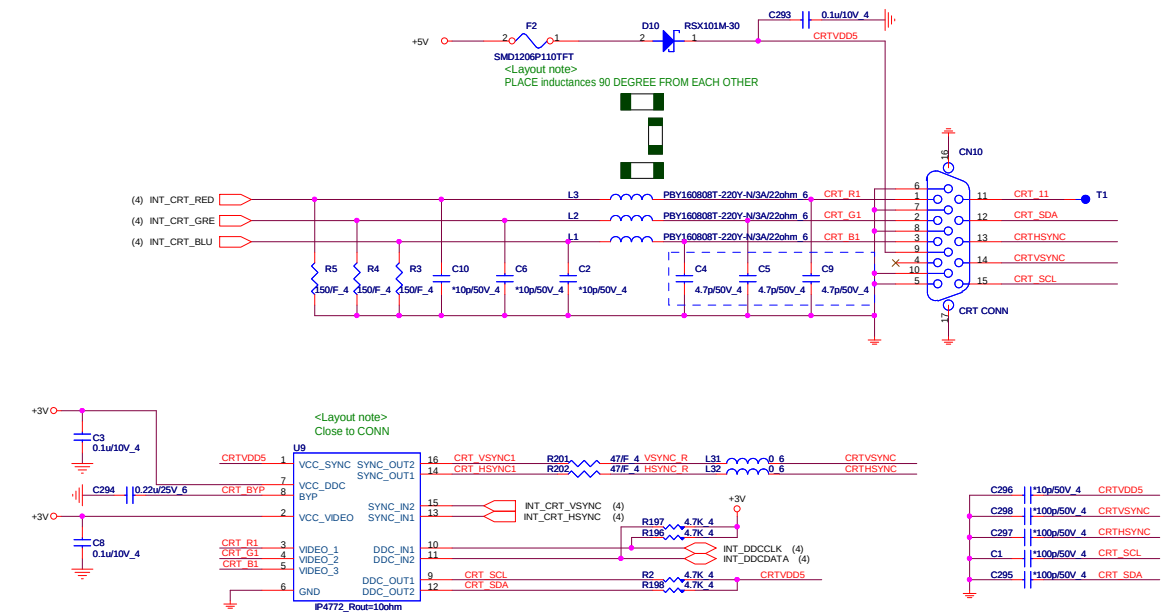
CAMERA POWER (CCD)



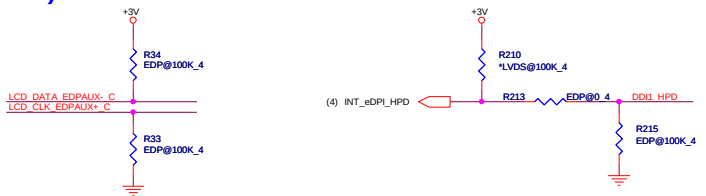
LCD MODULE (LDS)



CRT(CRT)



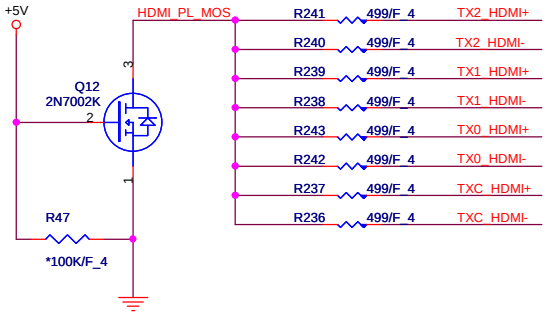
eDP (LDS)



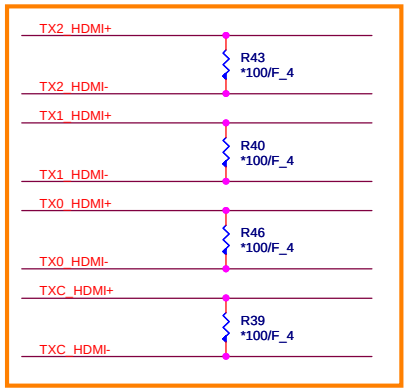
Quanta Computer Inc.		
PROJECT : ZHG		
Size	Document Number	Rev
	CRT/LVDS/EDP	1A
Date: Tuesday, January 10, 2012	Sheet 12 of 28	

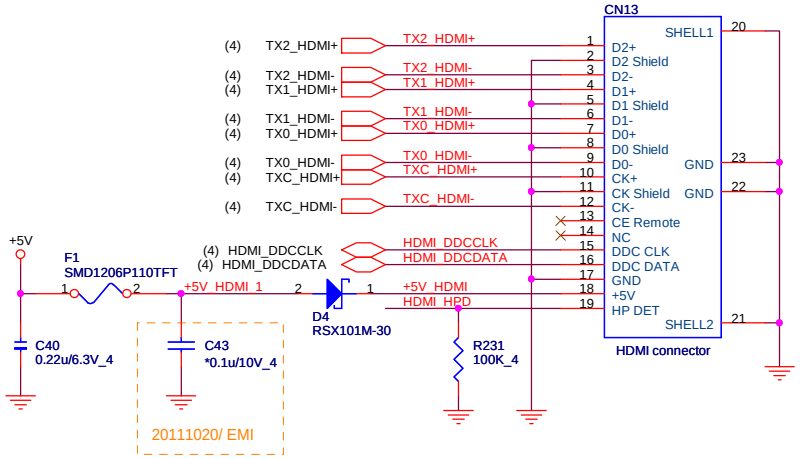
HDMI (HDM)

Close to HDMI Connector

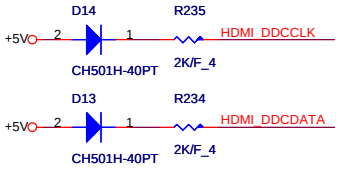


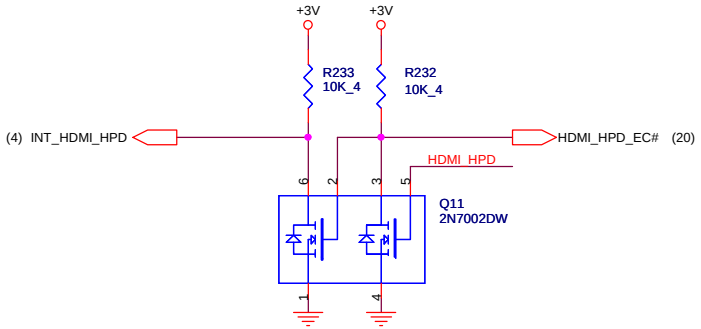
EMI reserve for HDMI





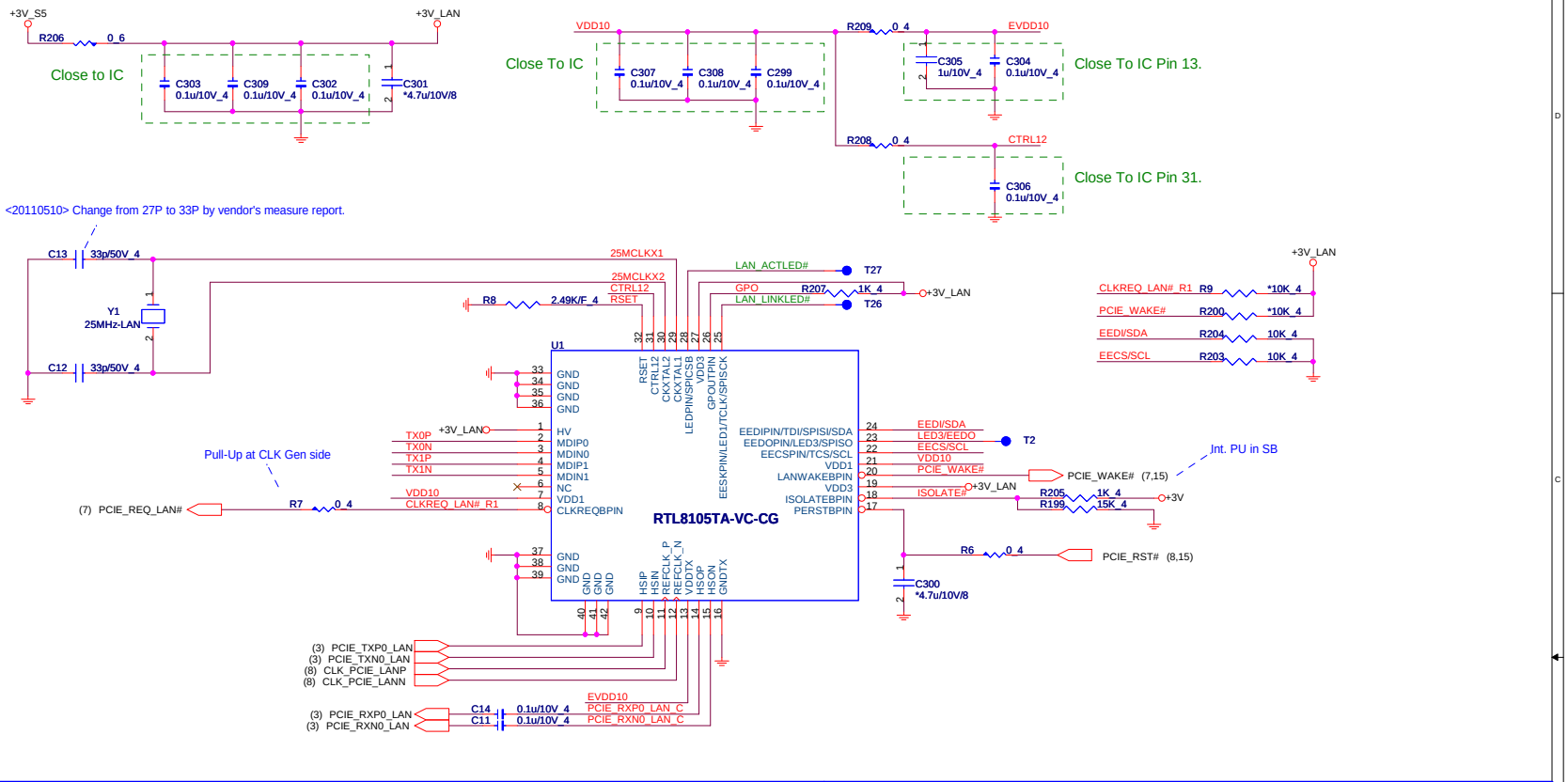
SDVO I2C Control (HDM)



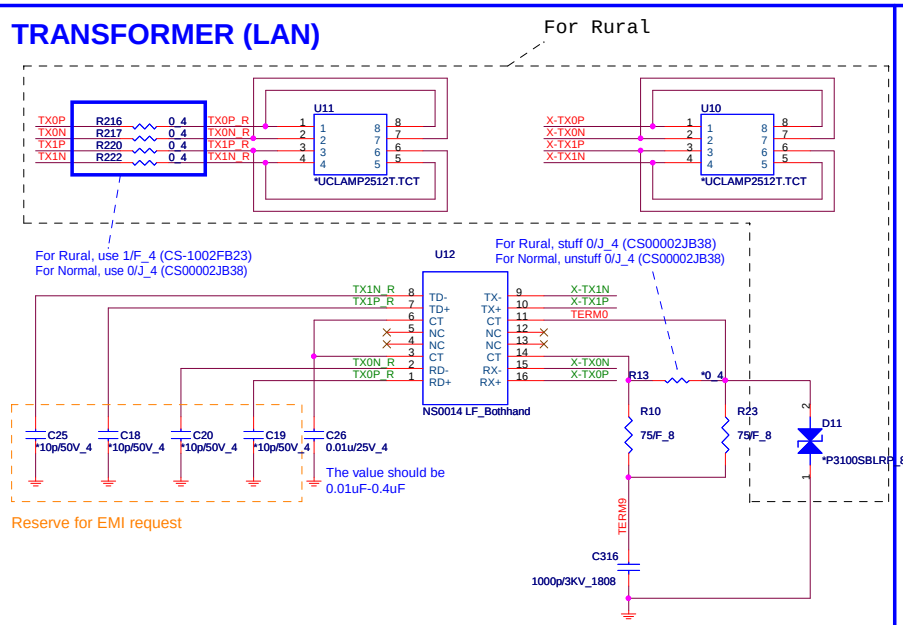


Quanta Computer Inc.		
PROJECT : ZHG		
Size	Document Number	Rev
	HDMI	1A
Date: Tuesday, January 10, 2012	Sheet 13 of 28	

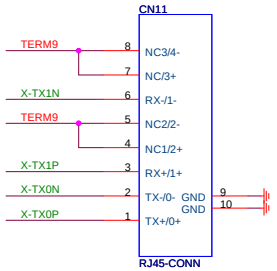
LAN (LAN)



TRANSFORMER (LAN)



RJ45 Connector (LAN)



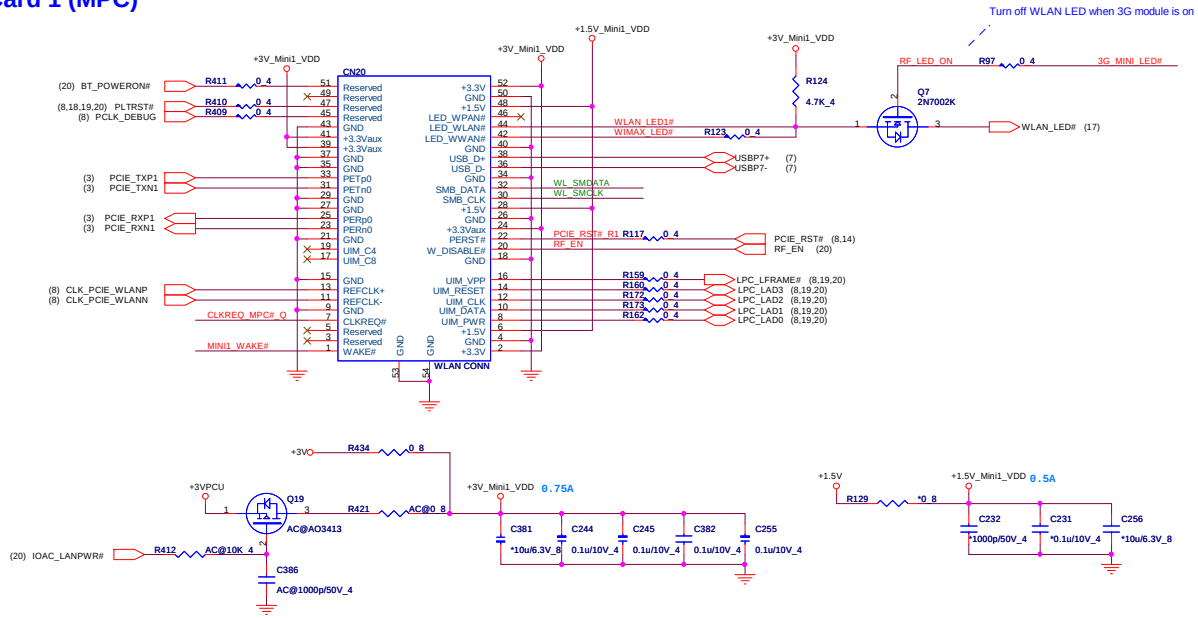
Quanta Computer Inc.

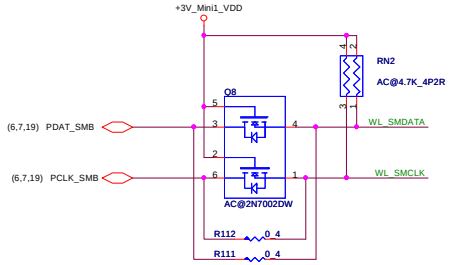
PROJECT : ZHG

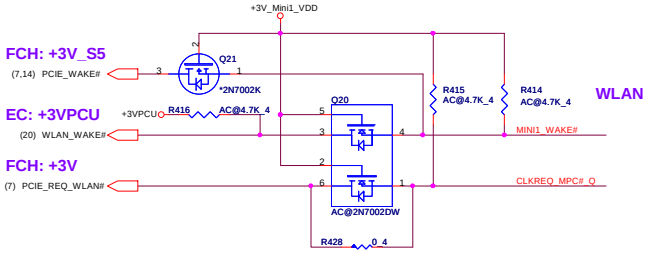
Size	Document Number	Rev
	LAN RTL8105TA-VC-CG	1A

Date: Tuesday, January 10, 2012 Sheet 14 of 28

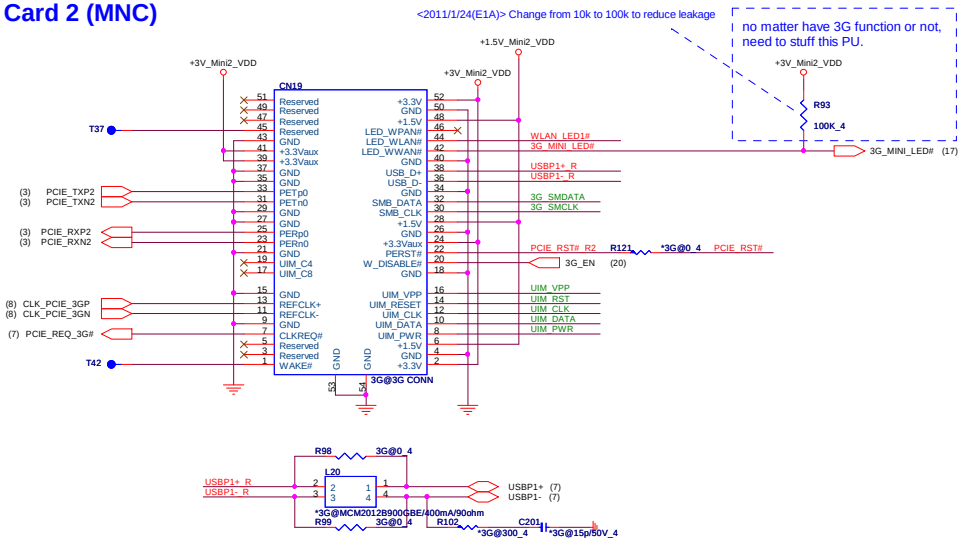
Mini Card 1 (MPC)

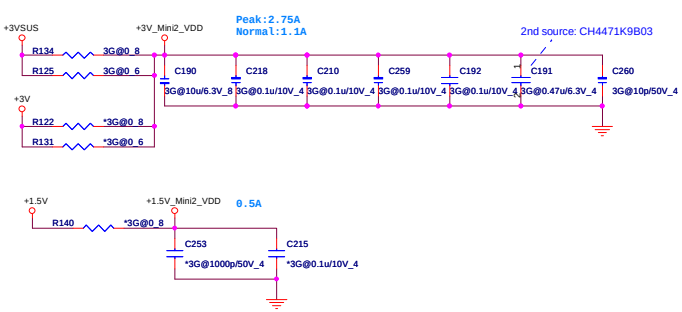


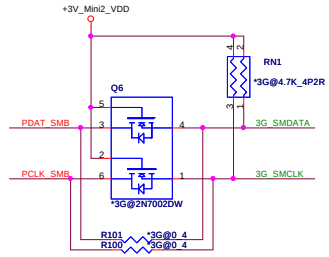




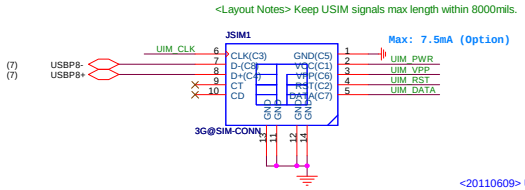
Mini Card 2 (MNC)

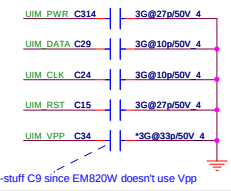


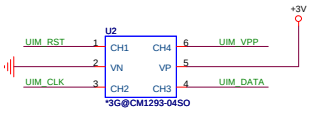


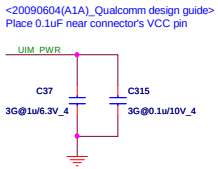


MultiMedia SIM (MNC)





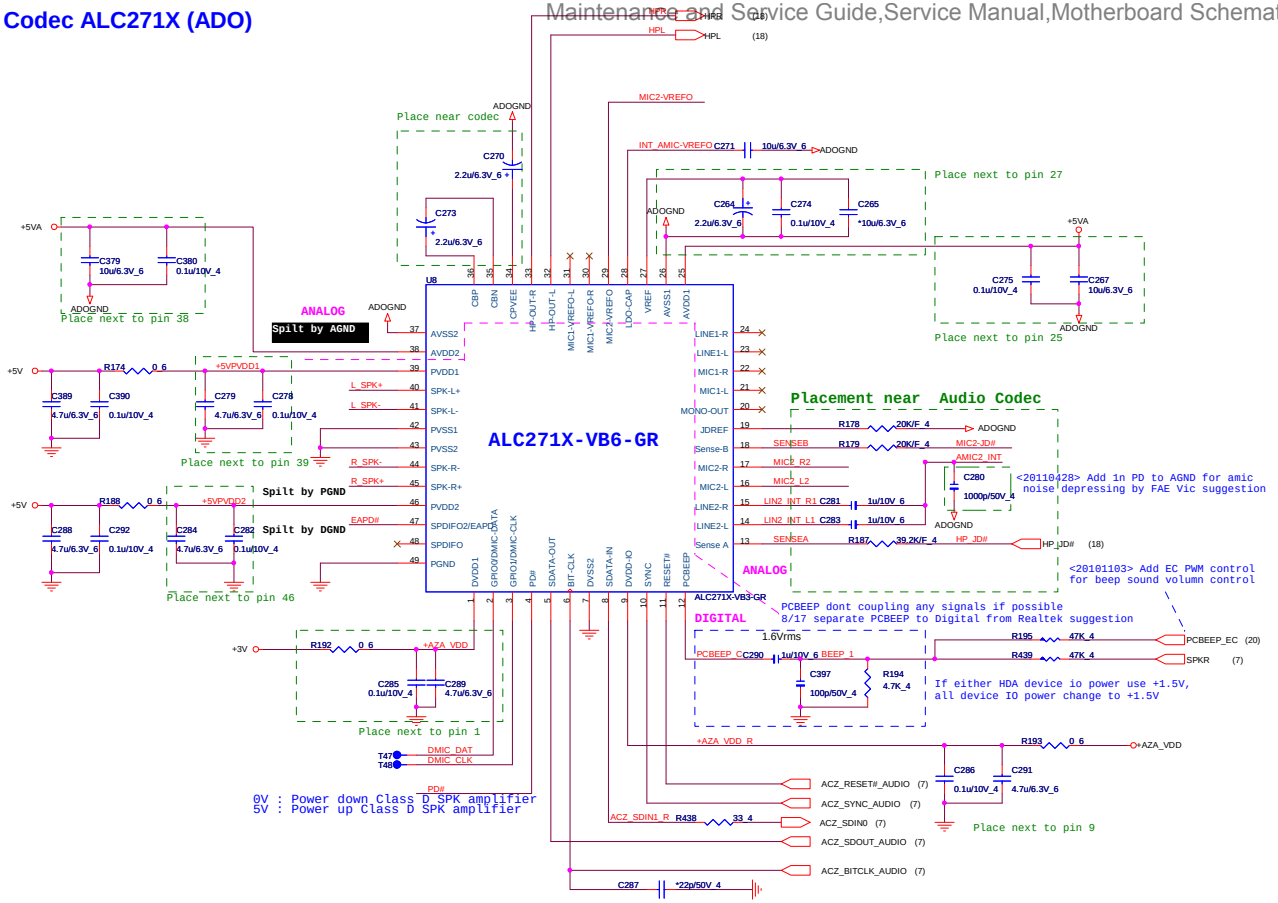




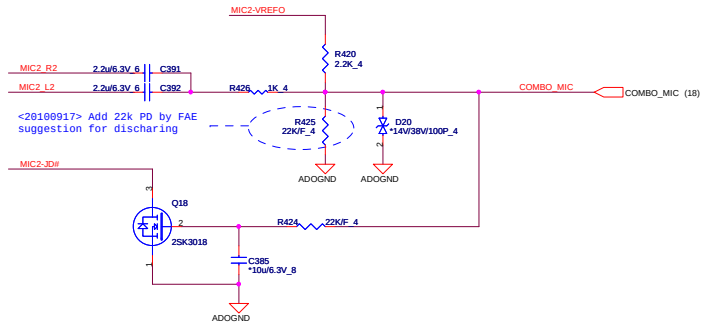
Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A
Date: Tuesday, January 10, 2012	Sheet 15 of 28	

Codec ALC271X (ADO)

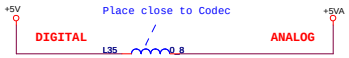


EARPHONE (AMP)

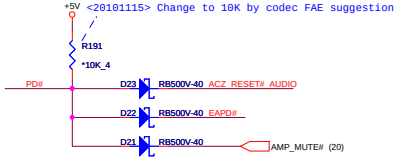


Power (ADO)

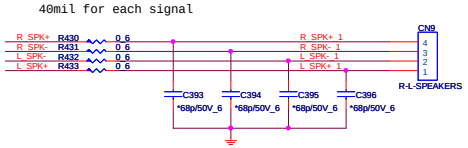
Demodulation Filter



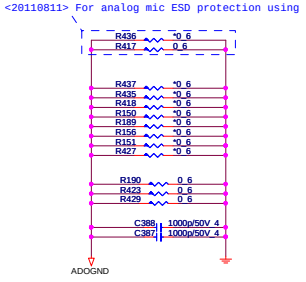
Mute (ADO)



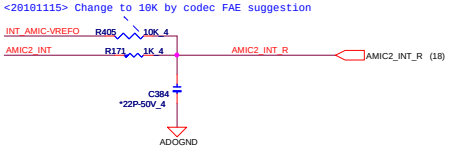
Internal Speaker (AMP)



GND(ADO)

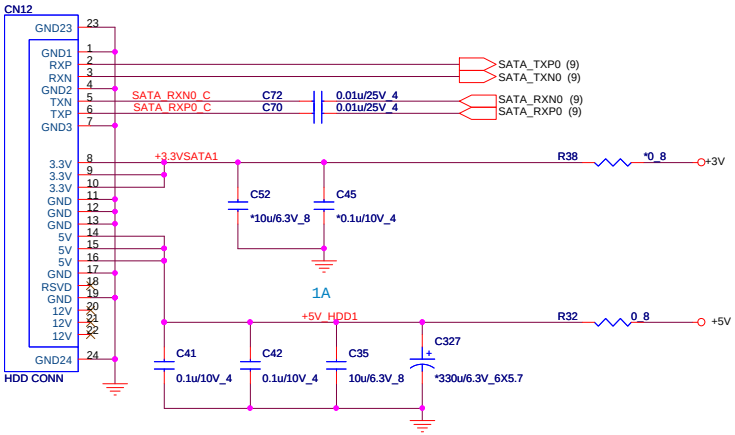


Internal Analog MIC (AMP)

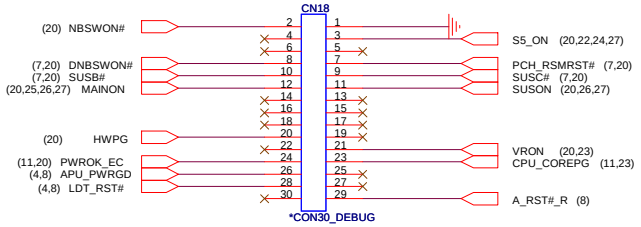


Quanta Computer Inc.		
PROJECT : ZHG		
Size	Document Number: ALC271X / AMP / SPK	Rev: 1A
Date: Tuesday, January 10, 2012	Sheet 16 of 28	

2.5" SATA HDD (HDD)

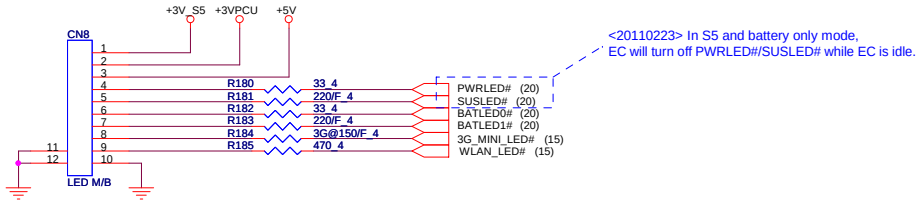


Power Sequence Connector(CPU)

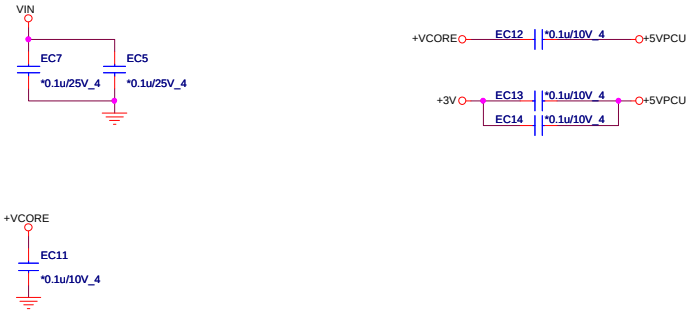


1	GND	11	SUSON	21	VRON
2	NBSWON#	12	MAINON	22	RESERVE
3	S5_ON	13	RESERVE	23	CPU_COREPG
4	RESERVE	14	RESERVE	24	PWROK_EC
5	RESERVE	15	RESERVE	25	RESERVE
6	RESERVE	16	RESERVE	26	APU_PWRGD
7	PCH_RSMRST#	17	RESERVE	27	RESERVE
8	DNBSWON#	18	RESERVE	28	LDT_RST#
9	SUSC#	19	RESERVE	29	A_RST#_R
10	SUSB#	20	HWPG	30	RESERVE

LED DB (UIF)

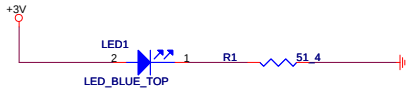


Stitching Cap(EMC)



POWER LED(UIF)

PWR indicator



Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	SATA HDD/LED/SW	1A

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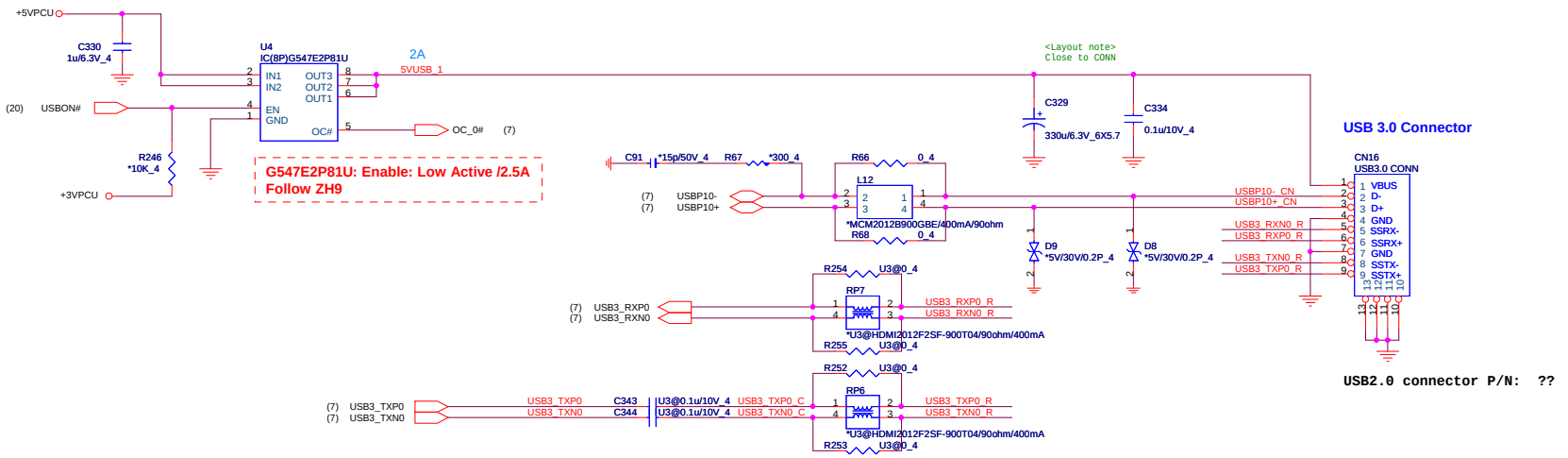
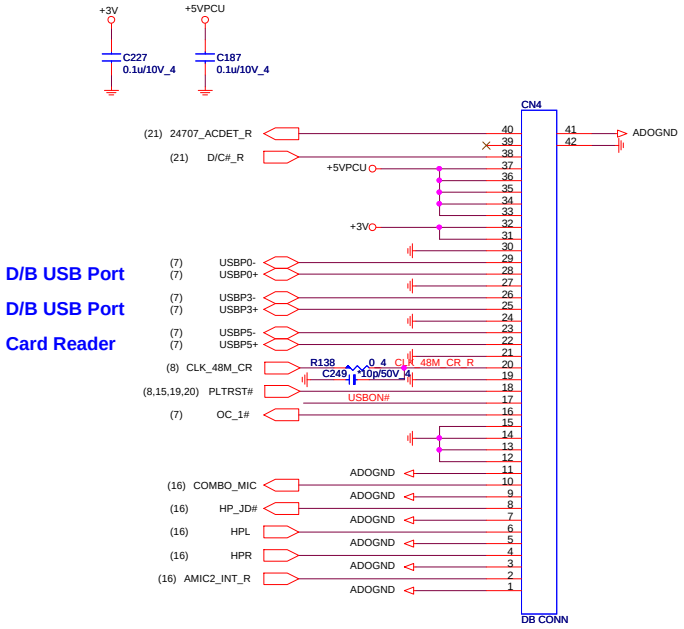
USB Left (USB)



USB2.0 connector P/N: ??

IO D/B (UIF)

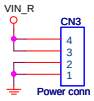


D/B USB Port

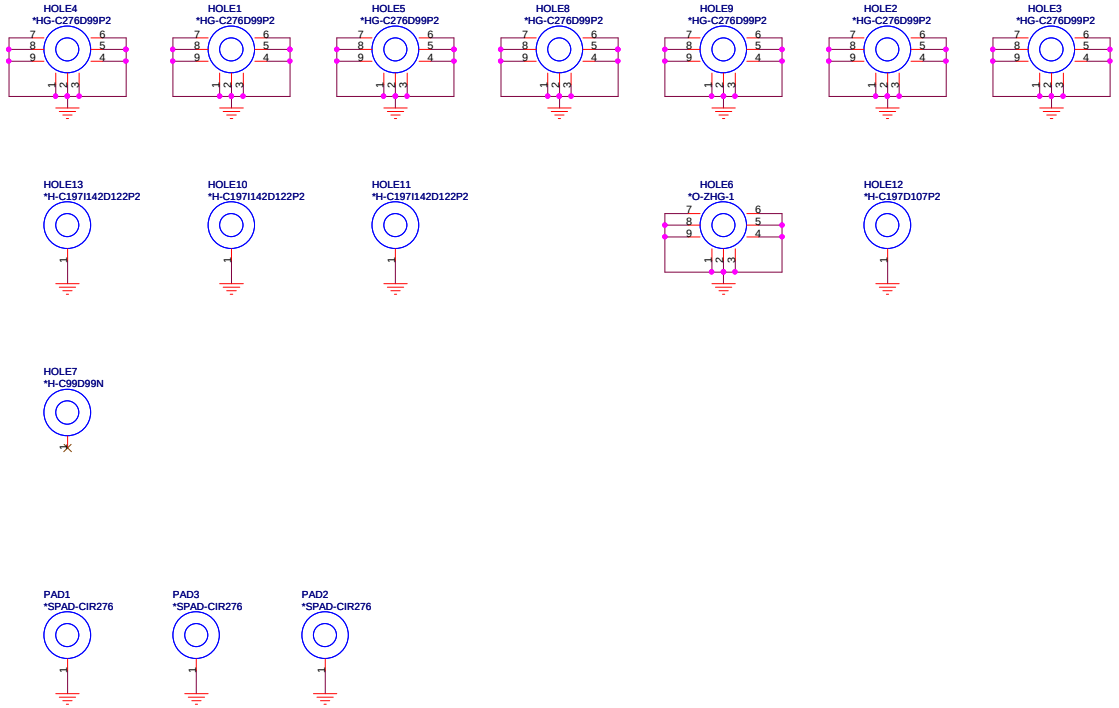
D/B USB Port

Card Reader

POWER M/B (DCD)



HOLE(OTH)



Quanta Computer Inc.

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Size	Document Number	Rev
	USB Port/ DB	1A
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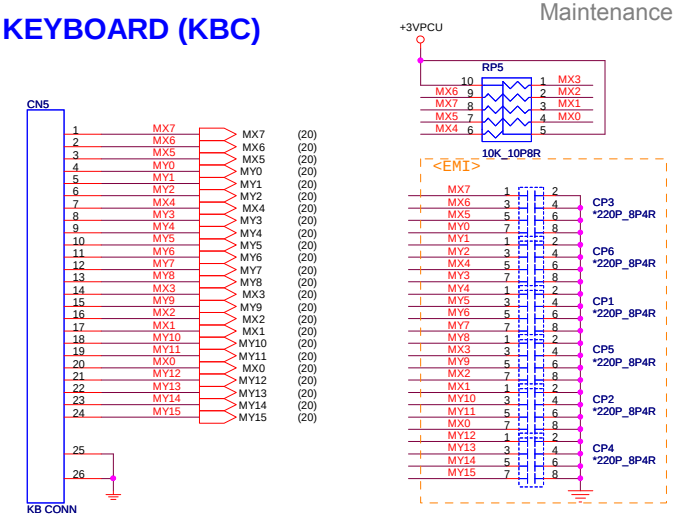
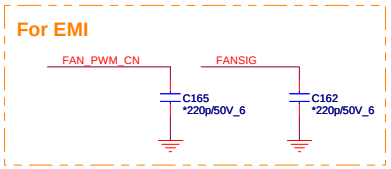
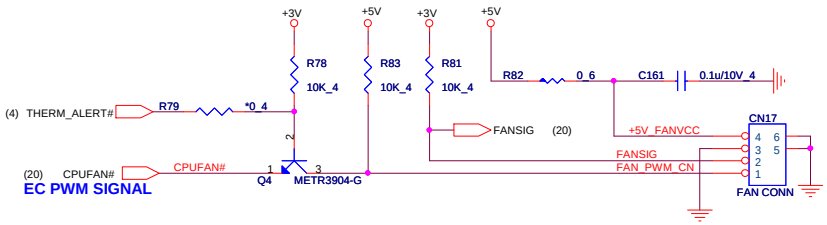
KEYBOARD (KBC)

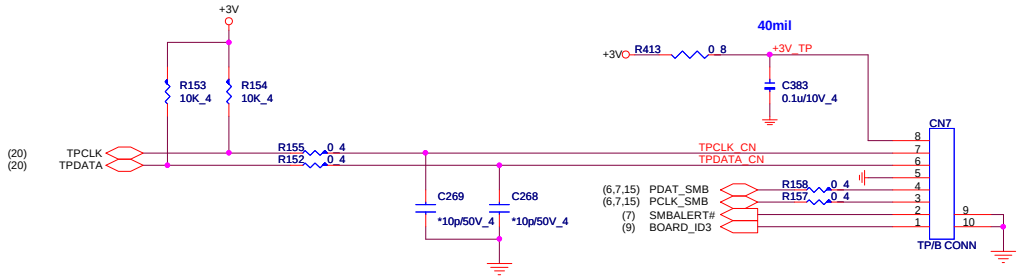


CPU FAN CTRL(THM)

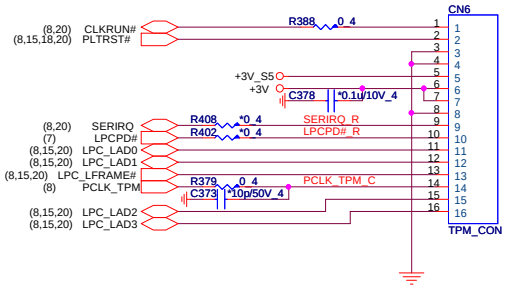




TOUCH PAD (TPD)

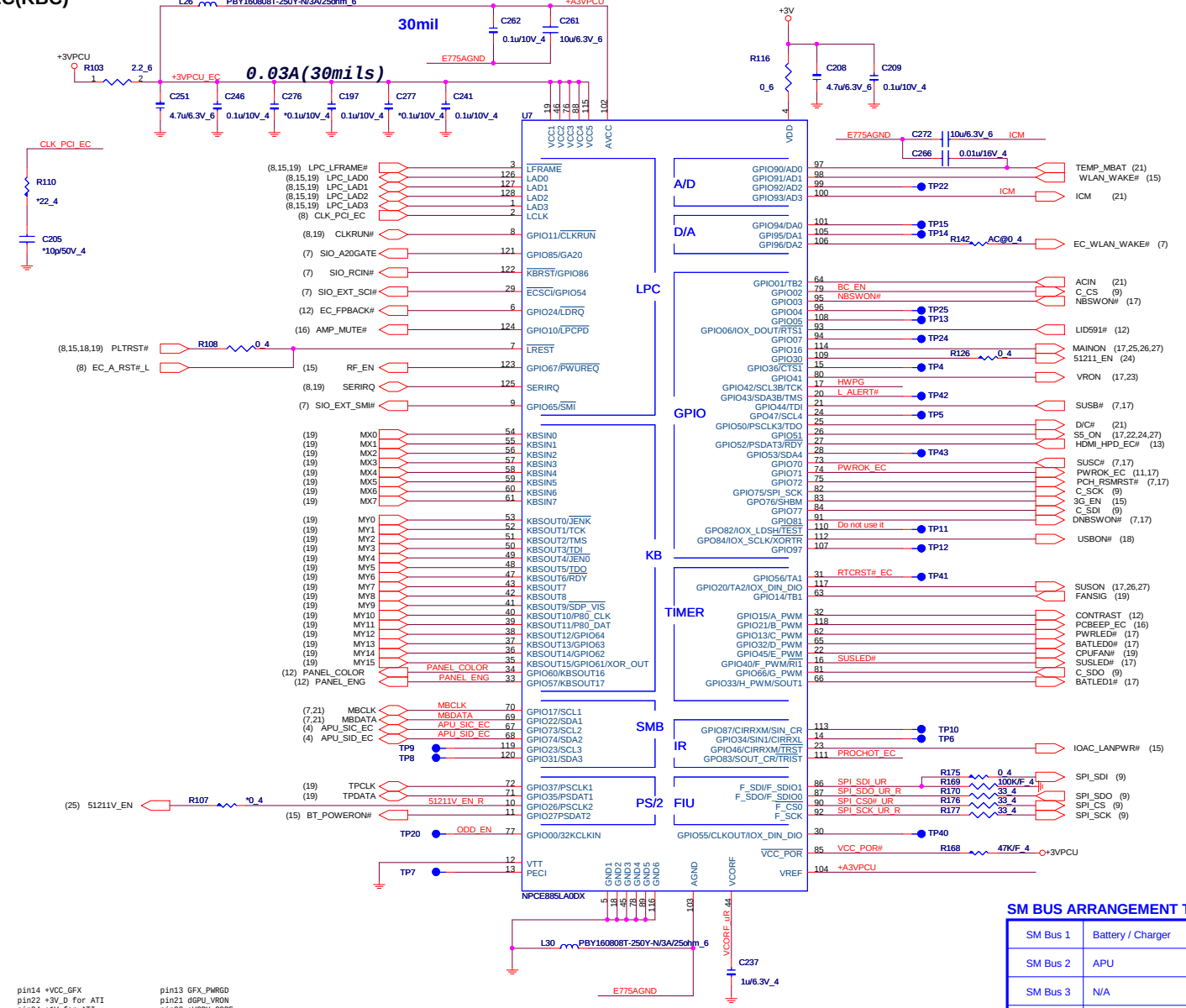


TPM (TPM)

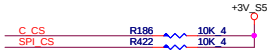


Quanta Computer Inc.		
PROJECT : ZHG		
Size	Document Number: KB/BT/TP/LED/Power Connector	Rev: 1A
Date: Tuesday, January 10, 2012	Sheet 19 of 28	

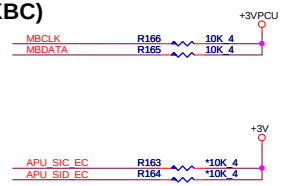
EC(KBC)

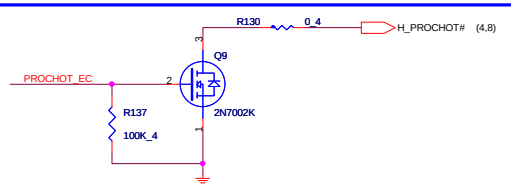


SPI PU(KBC)

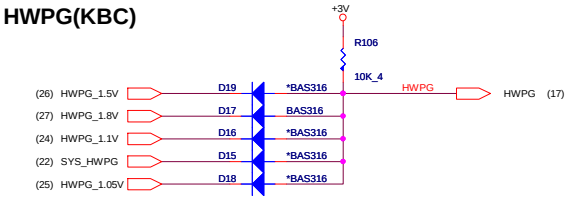


SM BUS PU(KBC)

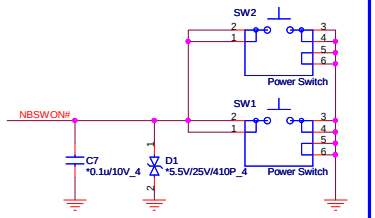




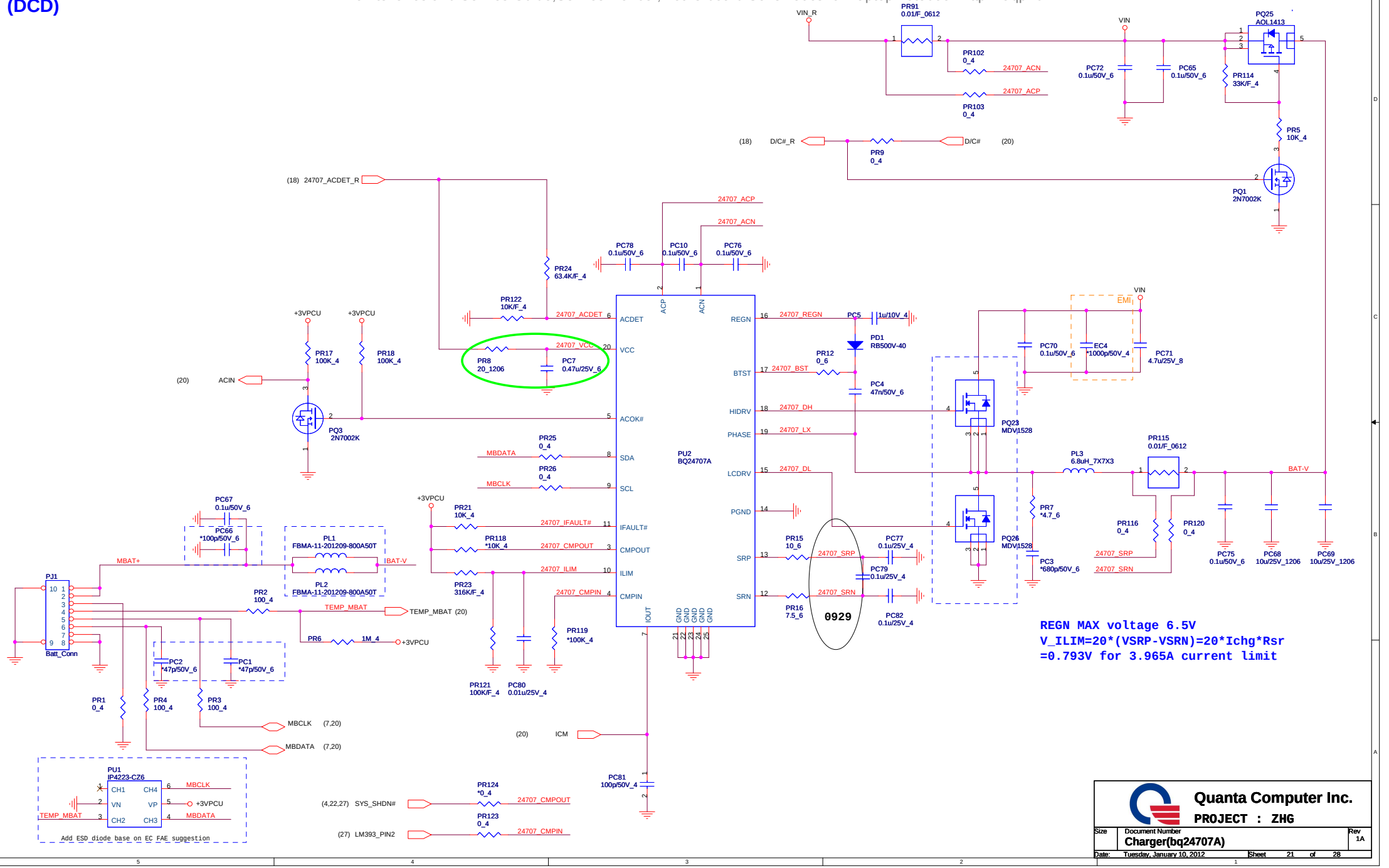
HWPG(KBC)



POWER-ON SWITCH (UIF)



Quanta Computer Inc.	
PROJECT : ZHG	
Size	Document Number: EC NPCE795CA0DX — Rev: 1A
Date: Tuesday, January 10, 2012	Sheet 20 of 28



(DCD)

MAIND — MAIND (24,26,27)

SYS_SHDN# — SYS_SHDN# (4,21,27)

SUSD — SUSD (27)

Ven=7.23V

+5VPCU
5 Volt +/- 5%
TDC : 5A
PEAK : 6.6A
OCP : 8A
Width : 200mil

+3VPCU
3.3Volt +/- 5%
TDC : 5.02A
PEAK : 6.3A
OCP : 7.5A
Width : 200mil

OCP:8A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=8-(2.525/2)=6.74A
Vth=6.74A*14mOhm=94.32mV
R(Ilim)=(94.32mV*10)/10uA
=94.32K

OCP:7.5A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=7.5-(1.9/2)=6.55A
Vth=6.55A*14mOhm=91.7mV
R(Ilim)=(91.7mV*10)/10uA
~91K

+5V_S5
TDC : 1.88A
PEAK : 2.5A
Width : 80mil

+5V
TDC : 3.08A
PEAK : 4.1A
Width : 120mil

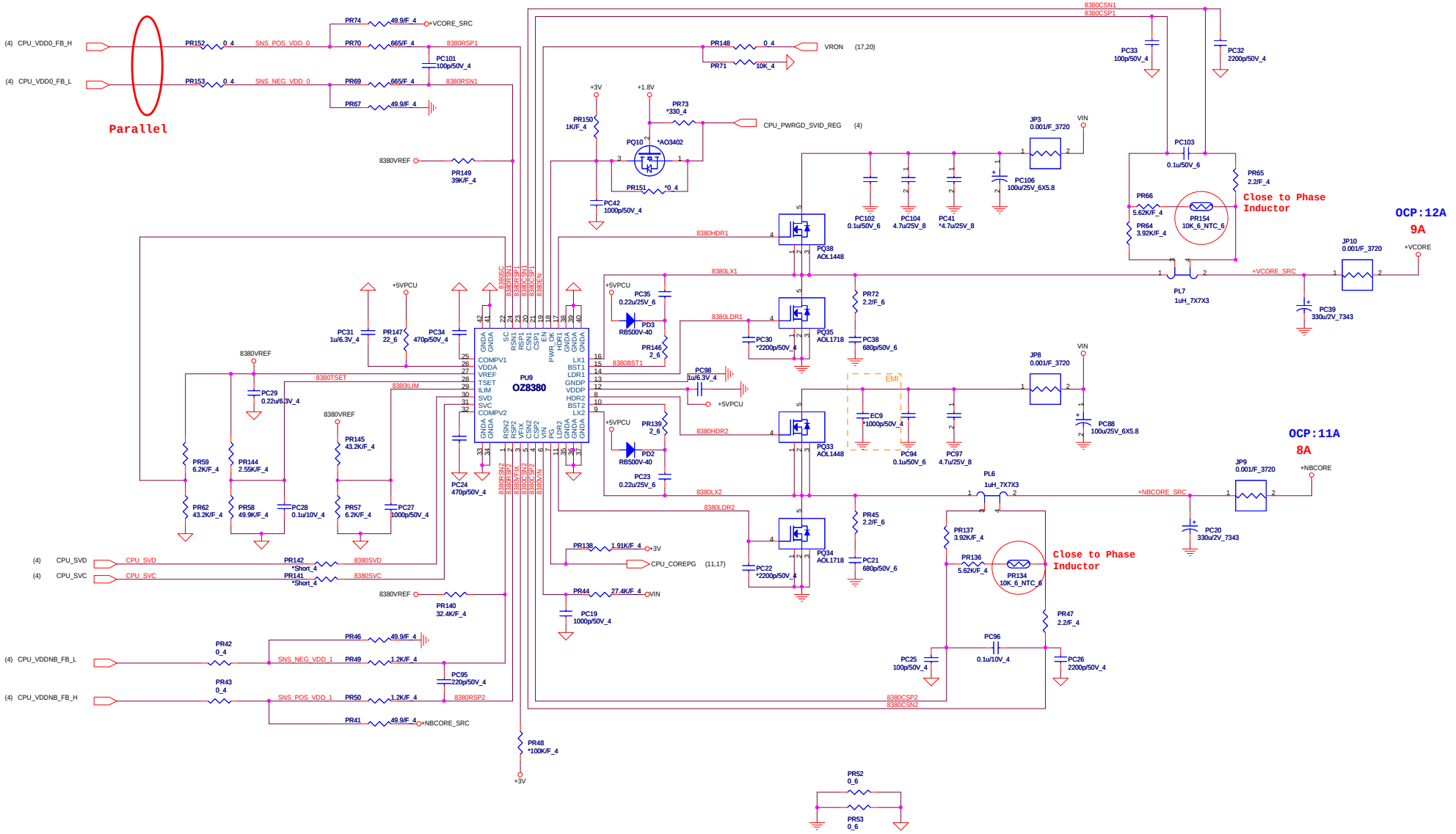
+3V
TDC : 2.48A
PEAK : 3.3A
Width : 100mil

+3VSUS
TDC : 1.426A
PEAK : 1.9A
Width : 60mil

+3V_S5
TDC : 0.62A
PEAK : 0.84A
Width : 40mil

Quanta Computer Inc.
PROJECT : ZHG

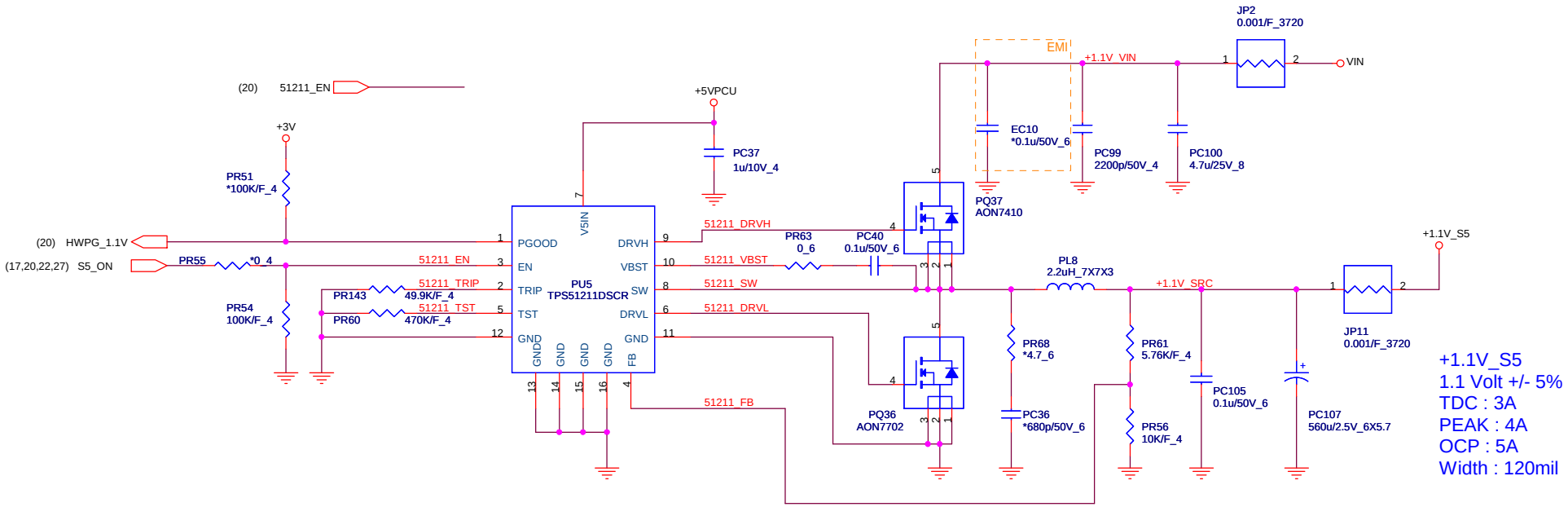
Size	Document Number	Rev
	SYSTEM 5V/3V (RT8223P)	1A
Date: Tuesday, January 10, 2012	Sheet 22 of 28	



Quanta Computer Inc.
PROJECT : ZHG

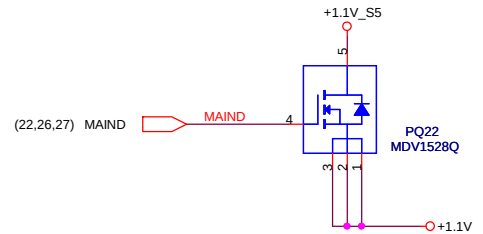
Size	Document Number	Rev
	CPU Core (OZ8380)	1A
Date: Tuesday, January 10, 2012	Sheet 23 of 28	

(DCD)



+1.1V_S5
1.1 Volt +/- 5%
TDC : 3A
PEAK : 4A
OCP : 5A
Width : 120mil

OCP=5A
L ripple current
=(19-1.1)*1.1/(2.2u*290k*19)
=1.624A
Vtrip=5-(1.624/2)*14mohm
=0.058629V
Rlimit=0.058629/10uA*8=46.9Kohm

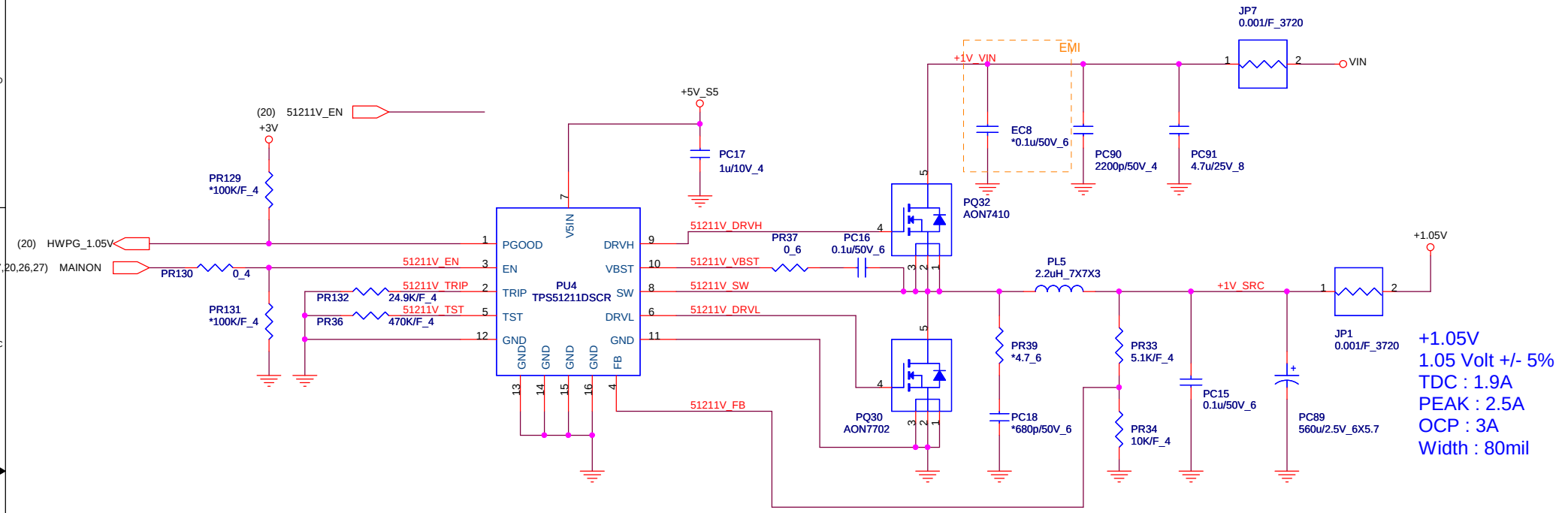


+1.1V
TDC : 2.73A
PEAK : 3.64A
Width : 120mil

Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	VCCP 1.1V(TPS51211)	1A
Date: Wednesday, January 11, 2012	Sheet 24 of 28	

(DCD)

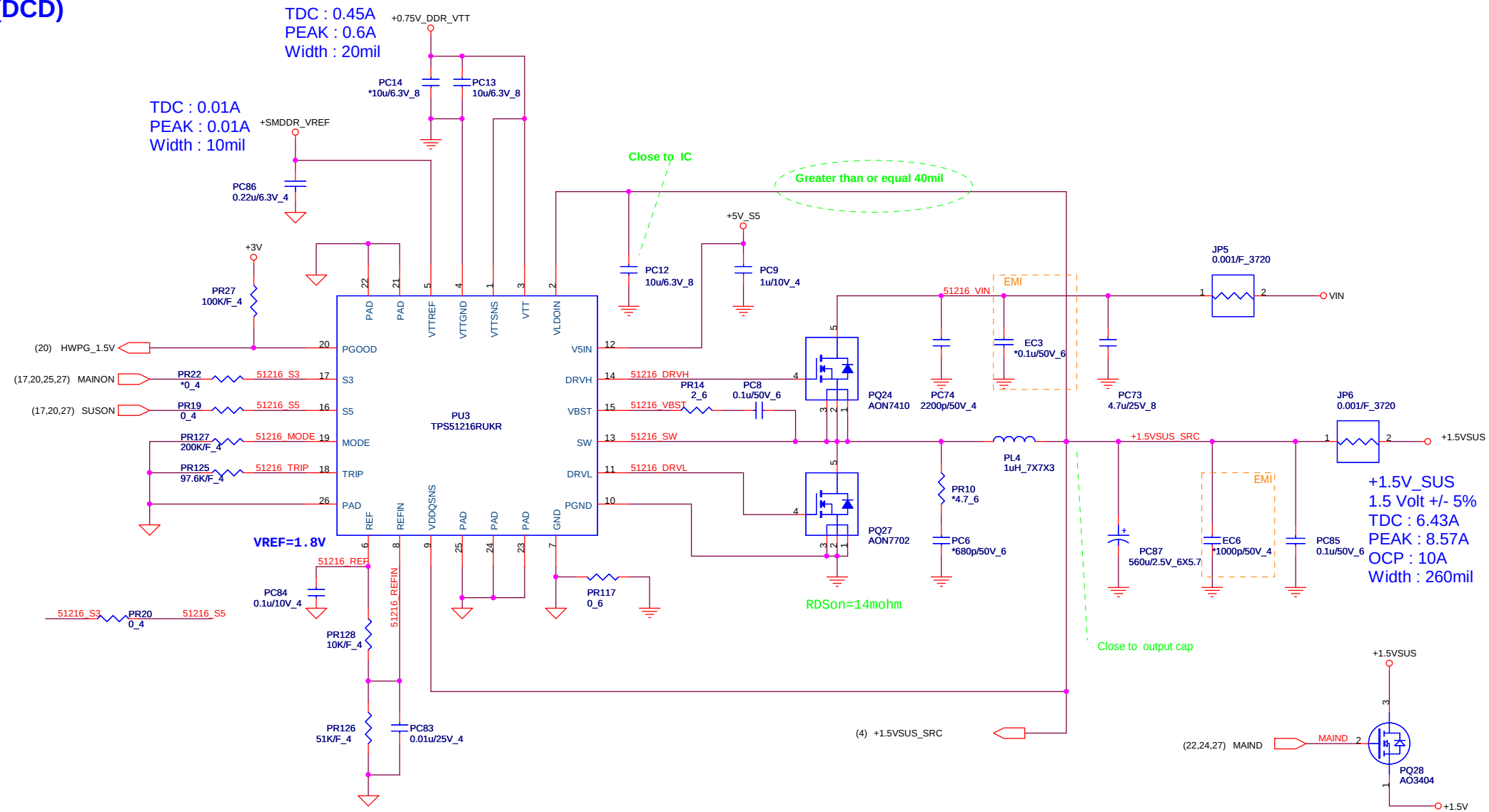


+1.05V
1.05 Volt +/- 5%
TDC : 1.9A
PEAK : 2.5A
OCP : 3A
Width : 80mil

OCP=3A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=3-(1.555/2)*14mohm
=0.03111V
Rlimit=0.03111/10uA*8=24.89Kohm

Quanta Computer Inc.		
PROJECT : ZHG		
Size	Document Number: +1.05V(TPS51211)	Rev: 1A
Date: Wednesday, January 11, 2012	Sheet 25 of 28	

(DCD)



OCP=10A
L ripple current
=(19-1.5)*1.5/(1u*400k*19)
=3.454A
Vtrip=10-(3.454/2)*14mohm
=0.1158V
Rlimit=0.1158/10uA*8=92.657Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A
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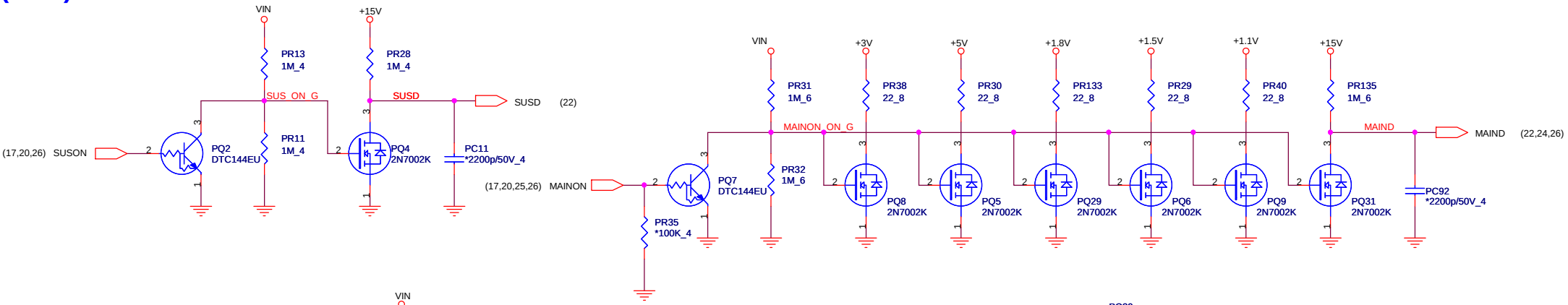
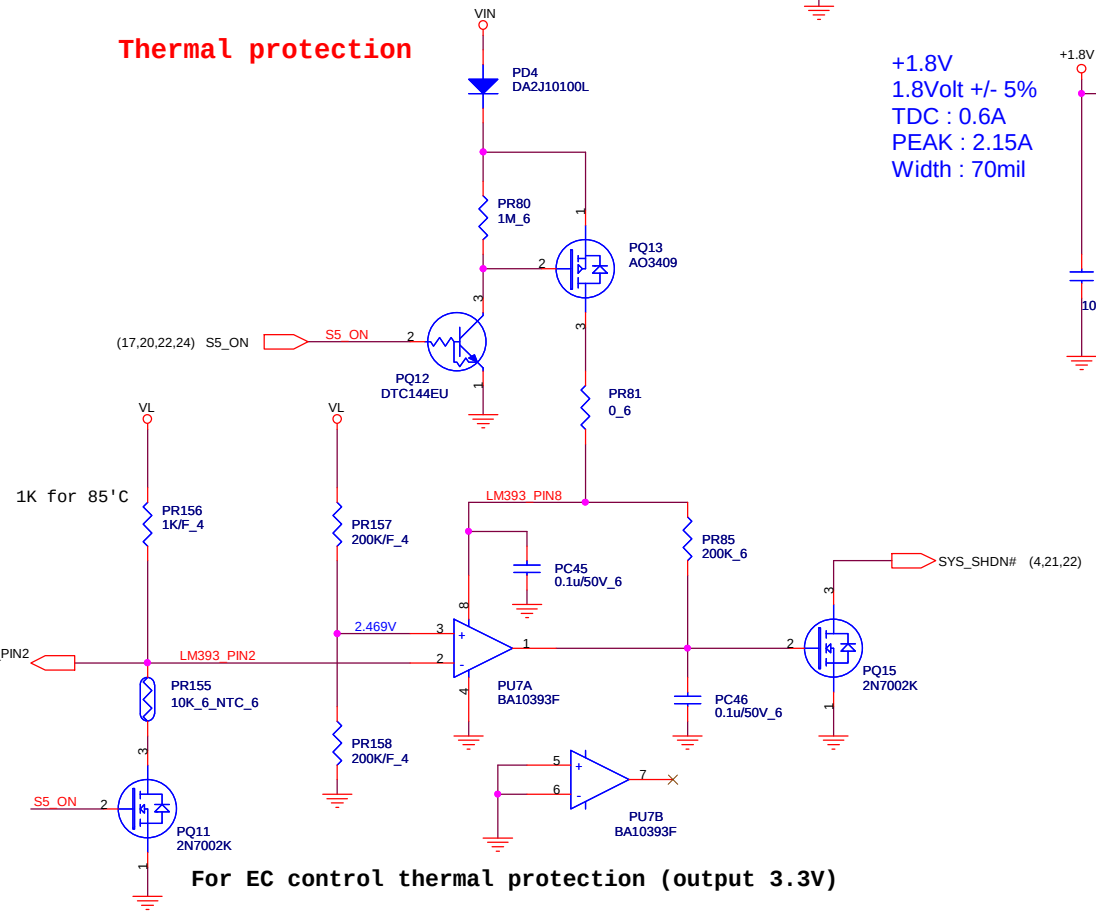
(DCD)

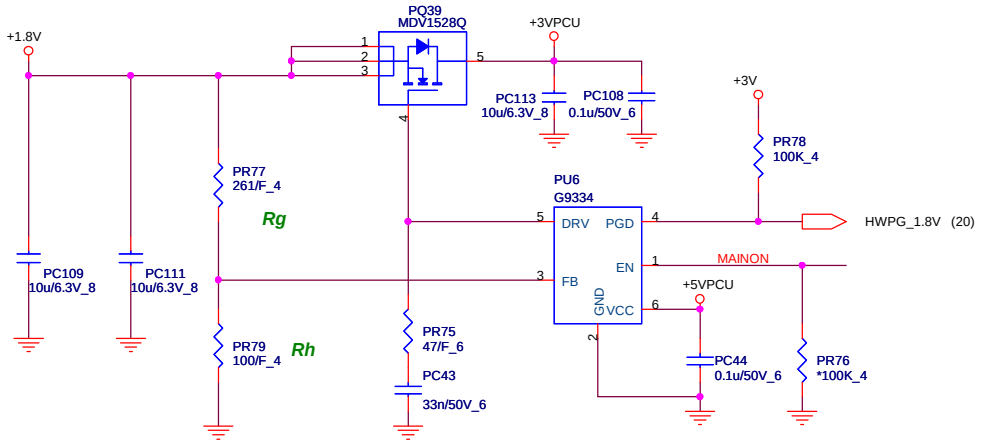


Thermal protection



For EC control thermal protection (output 3.3V)

+1.8V
1.8Volt +/- 5%
TDC : 0.6A
PEAK : 2.15A
Width : 70mil



*Vout1 = (1+Rg/Rh)*0.5*

Quanta Computer Inc.
PROJECT : ZHG

Size	Document Number	Rev
	Discharge /Thermal protection	1A
Date: Tuesday, January 10, 2012	Sheet 27 of 28	

CHANGE LIST

MODEL	REV	
ZHG M/B	A	First Release

	B	Add R3439
		Del R237,R204,R222
		Change CN3016,CN3017,CN3018 footprint and PN
		Change PC101,PC104 PN
		
		Change CN3015,CN3006,CN3004 footprint
		SWAP RP9,RP10
		Add R3440,R3441,R3442,C6239,C6240,C6241
		Del TP53,TP15,TP14,TP24
		Change PR20 PN and footprint,PR12 PN
		Add R3443,R3444,R3446,R3445
		Update CN16,CN3011 PN
		
		Update CN16,CN3011 footprint
		Change PC73,PC79,PC80,PC82,PC83,PC90 footprint
		Swap CP3001,CP3002,CP3003,CP3004,CP3005,CP3006 pin
		Change CN3001 PN and footprint.
		Delete R3031,C3036,C3021
		Delete C3057,C3064,C3062,C3060,C3056,C3061
		Add R3447,R3448
		Delete TP21,TP11
		
		Add R3449 and change CN3008 PN and footprint
		Swap CN3001,RP8
		Change CN3017,CN3016 PN
		Delete R113,R125
		
		Change R3289 to 0ohm
		Swap Q3030 pin define
		PU Board_ID3 and Board_ID2, modify CN3008 net
		Delete R3009
		Change C3013 to 1uF
		Add R3450,R3451
		Change CN3003 pin define
		
		Swap L3026
		Change R142 to 100K
		Delete R3435,C3260. Change CN3008 PN and footprint
		Delete R3272,Q3019,R3256,R3270,TP18,TP25,TP28
		and add Q3036,Q3035,R3452
		Add PQ45,PR162,SW2,R3453,RP11,D3022
		Delete R3438
		Unstaff D10,D54,D55,R242,R206 and staff R369,R223,Q3033,RN3001
		
		Modify CN3003 and U4 pin define
		Add Q3037
		Unify the value, function code, P/N, description

	C	Delete T6,T15,R215,R202,Q12,R3425,R3426
		Add R3454,PQ46,C6242
		Add HOLE
		Update CN3015 PN
		Change CN3008 pin define
		Change CN3006 footprint
		Add R3460,C6243,R3457,R3459,R3455,
		R3456,Q3038,R3458,R3461 and reserve IOAC function
		
		Change Y3 footprint and staff R371
		Update U17,CN3015,CN14,CN3001 P/N
		Change CN3006 footprint
		Add R3462,Q3039
		Delete R163,RT1,R3459
		Add L3029~L3035,R3463~3476 for EMI
		Unstaff C418
		Staff R3418,R3200,R3434,R3439
		Change CN3008 PN and footprint
		
		Staff R115
		Delete CN3007 power trace for layout
		Add PQ47,PQ48,PR163,PR165,PR164,PC118
		Delete TP29 and add net 1.1V_S5_EN
		Add R3477,R3478
		
		Modify LVDS common choke pin define
		Add TP63~TP70 for layout
		Remove G2,G3 and add T3051,T3052
		Change Y3,C3041 footprint
		Modify PU2 pin define
		
		Change PR3,PR20,PR12,PC11 PN
		Add EC1~EC10 for RF
		Add EC11~EC18 for EMI
		Add R3479 and C6244,R3480,R3481
		Delete EC7,EC8,EC10,EC4,PAD3
		
		Staff PR154,R3480 and unstaff PR149
		Staff R206 and unstaff R223

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ZHG	PCBA NO : 31ZHGMB0000	REV: A	DOC. NO : 206
APPROVED BY : Edison Huang	CHECK BY : Kevin Hsieh	DRAWING BY : Benson Yo	DATE : 2012/01/10

Quanta Computer Inc.
PROJECT : ZHG

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