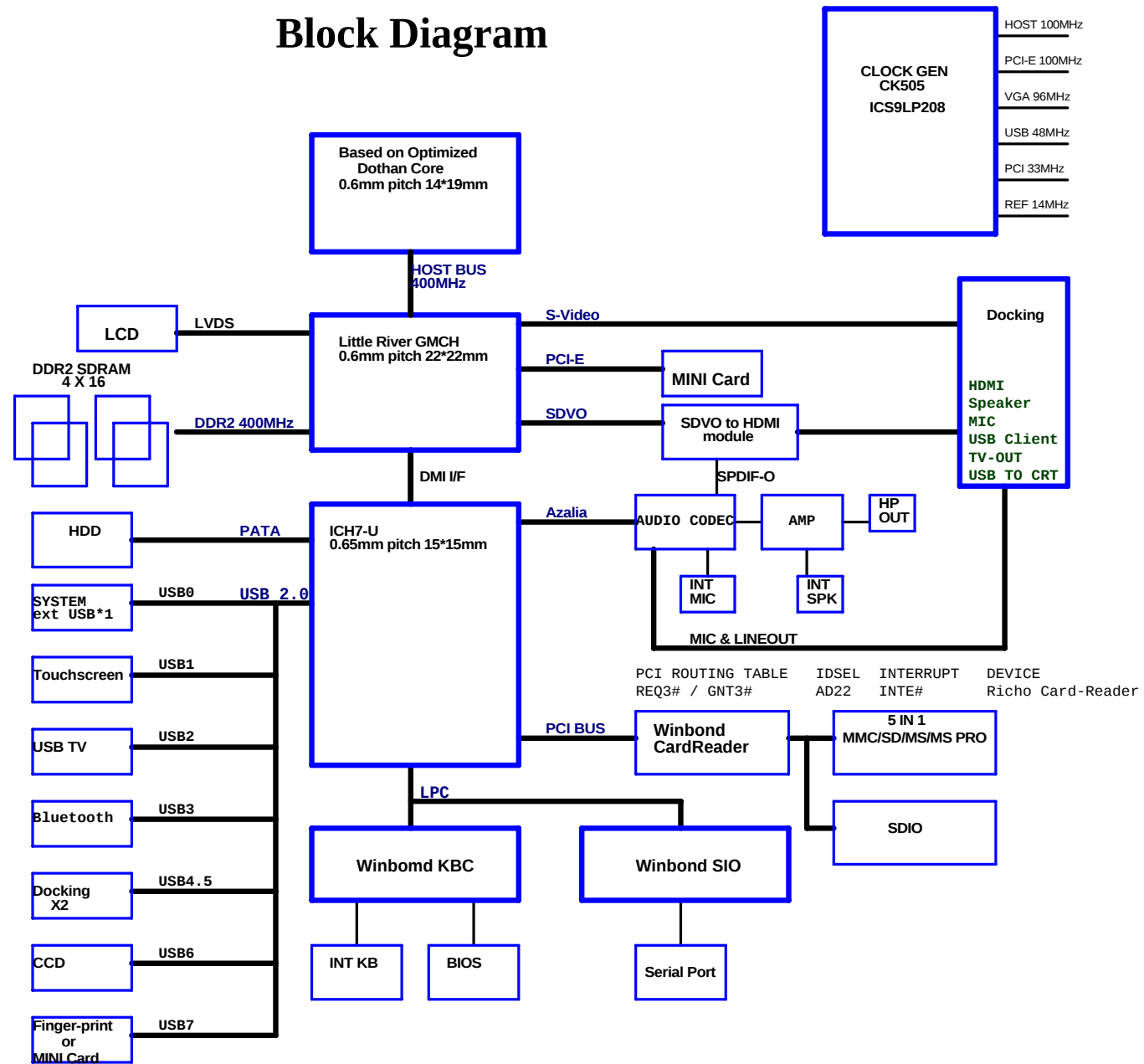
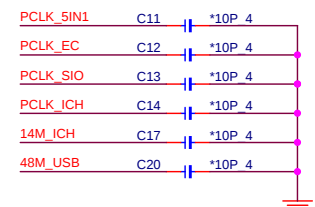
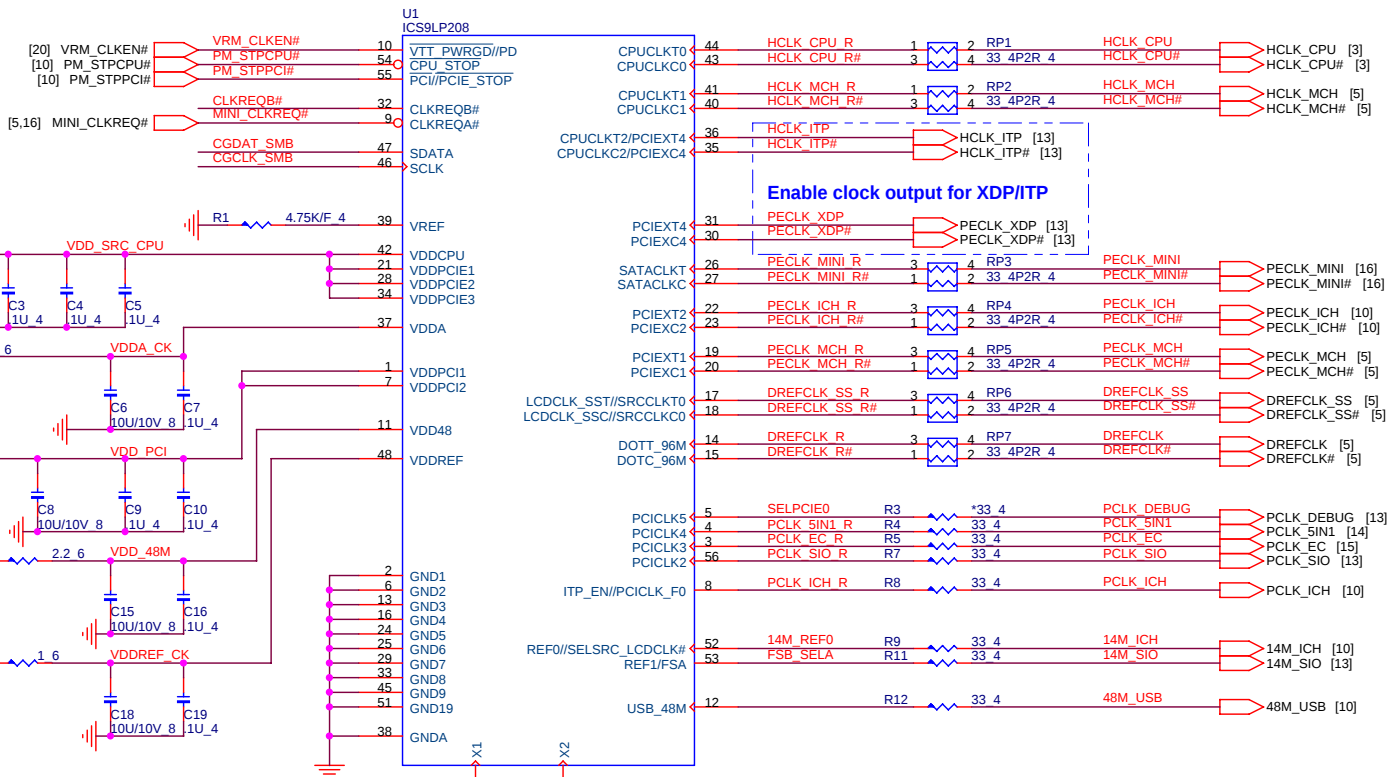


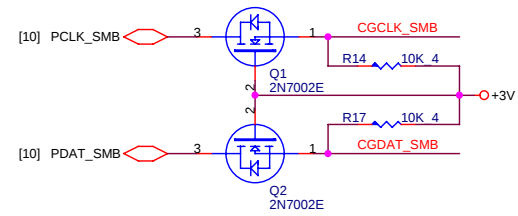
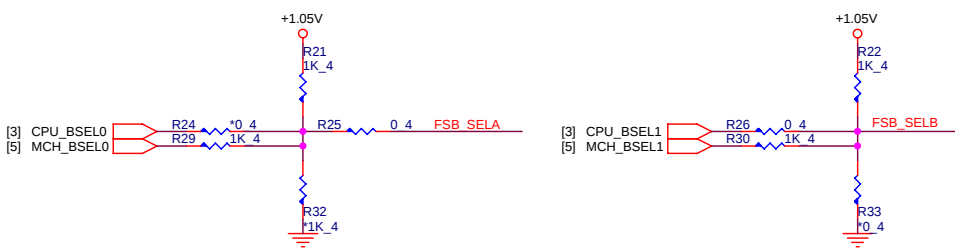
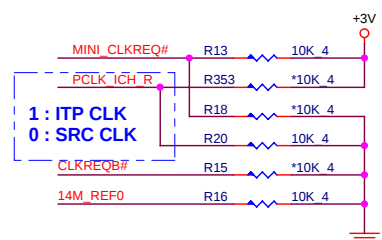
Block Diagram



Power State Table		
Power Name	Control Signal	Power State
+3VPCU	N/A	ALWAYS
+3V_S5	S5_ON	S0 - S5
+3VSUS	SUSON	S0 - S3
+3V	MAINON	S0
+5VPCU	N/A	ALWAYS
+5V_S5	S5_ON	S0 - S5
+5VSUS	SUSON	S0 - S3
+5V	MAINON	S0
+1.8VSUS SMDDR_VTERM	SUSON MAINON	S0 - S3 S0
+1.05V	MAINON	S0
+1.5V	MAINON	S0
+2.5V	MAINON	S0
+VCC_CORE	VRON	S0



Stealey BSEL[1:0]=01 ----> 400 MHz
 CK505 BSEL[2:0]=101 ----> 400 MHz
 ICS9LP208 FSA=1 ----> 400 MHz
 FSA=0 ----> 533 MHz

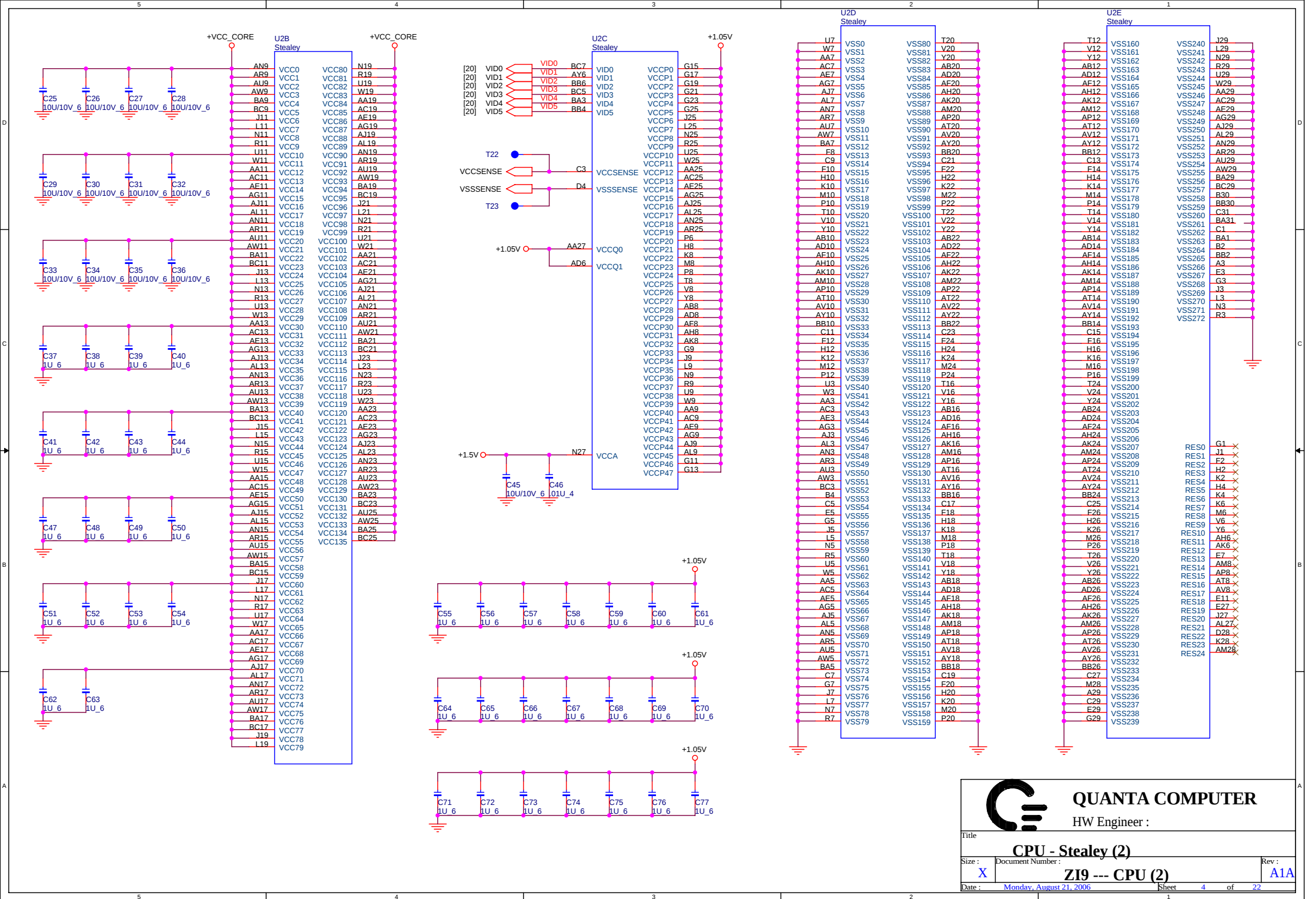


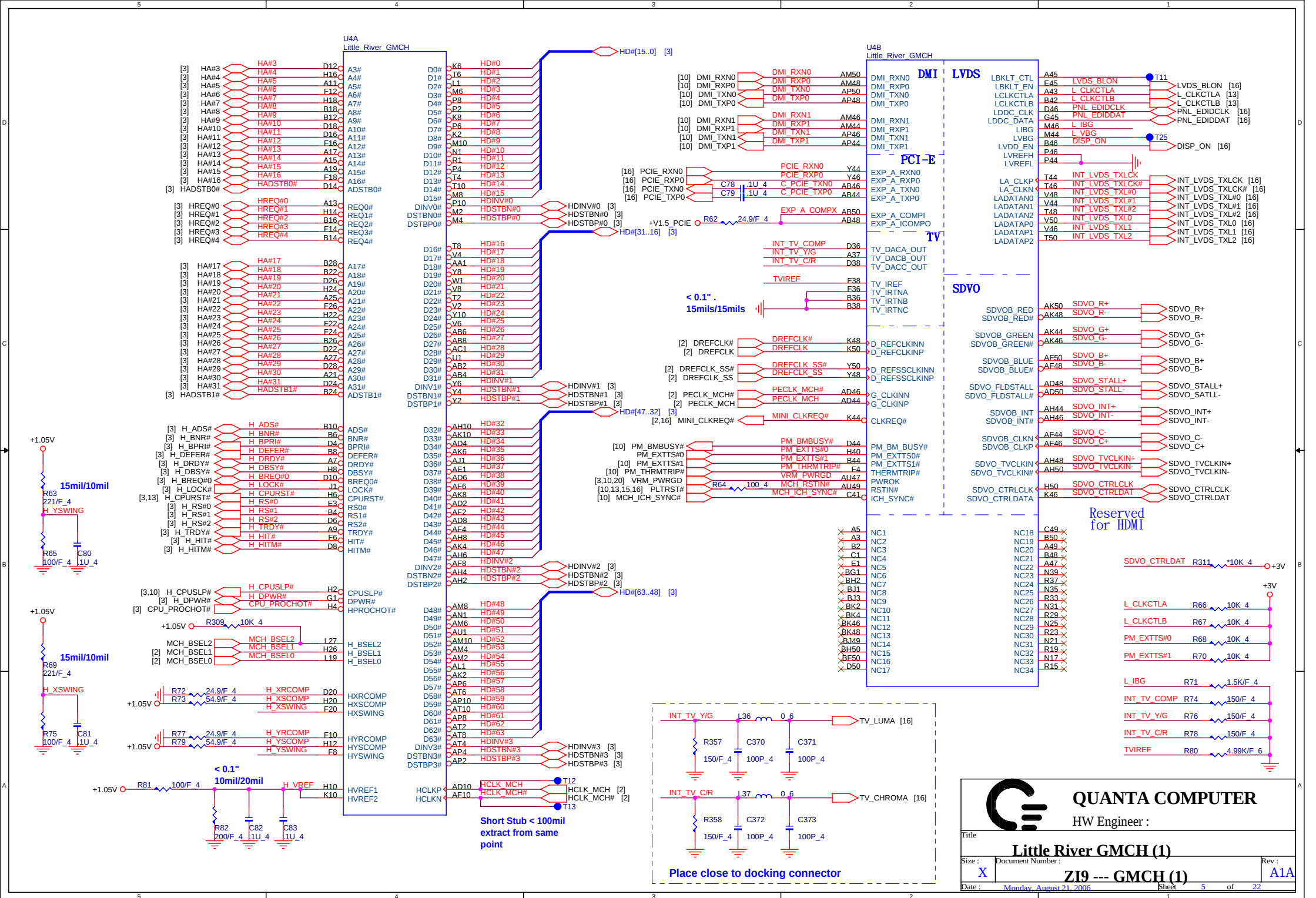


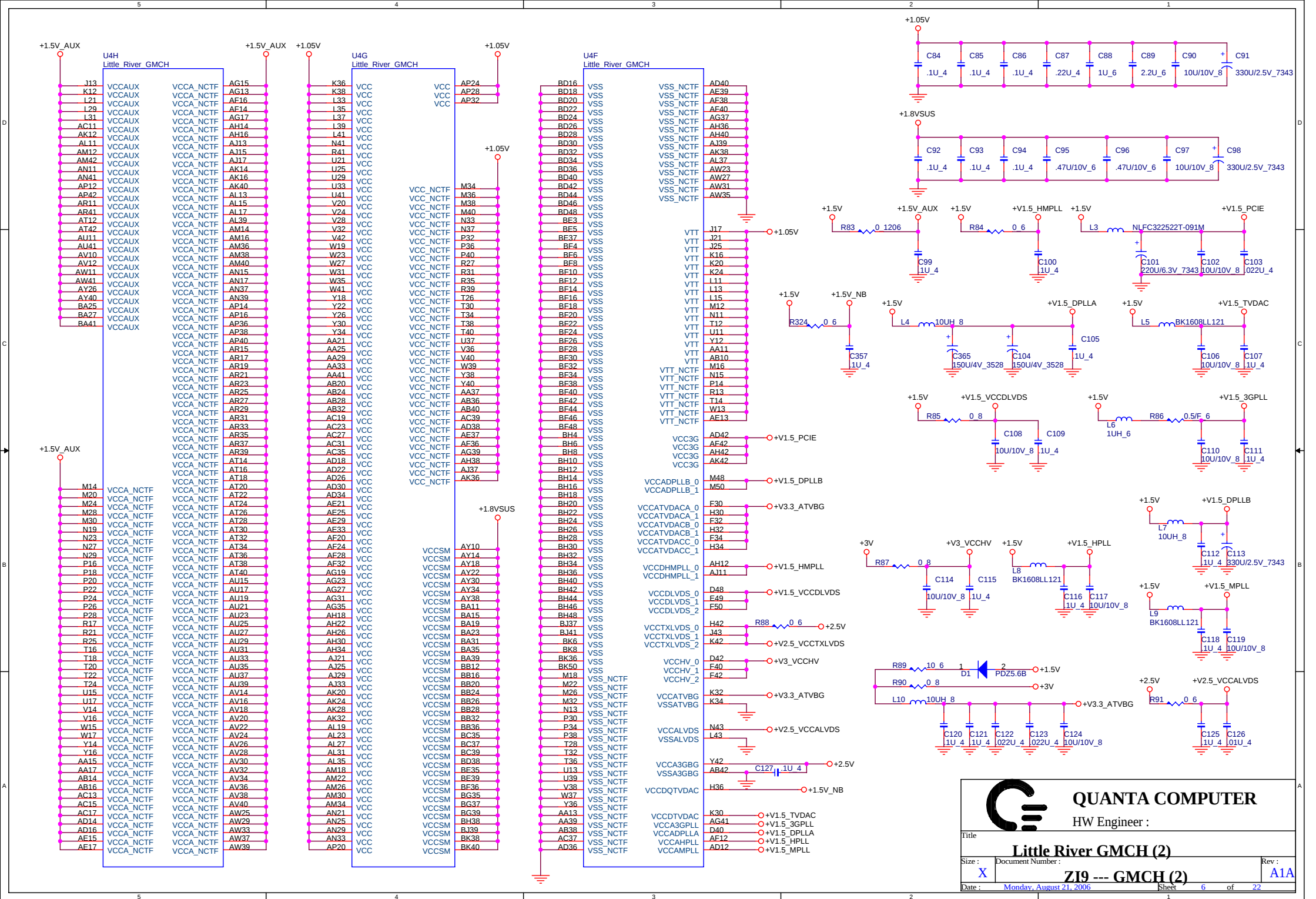
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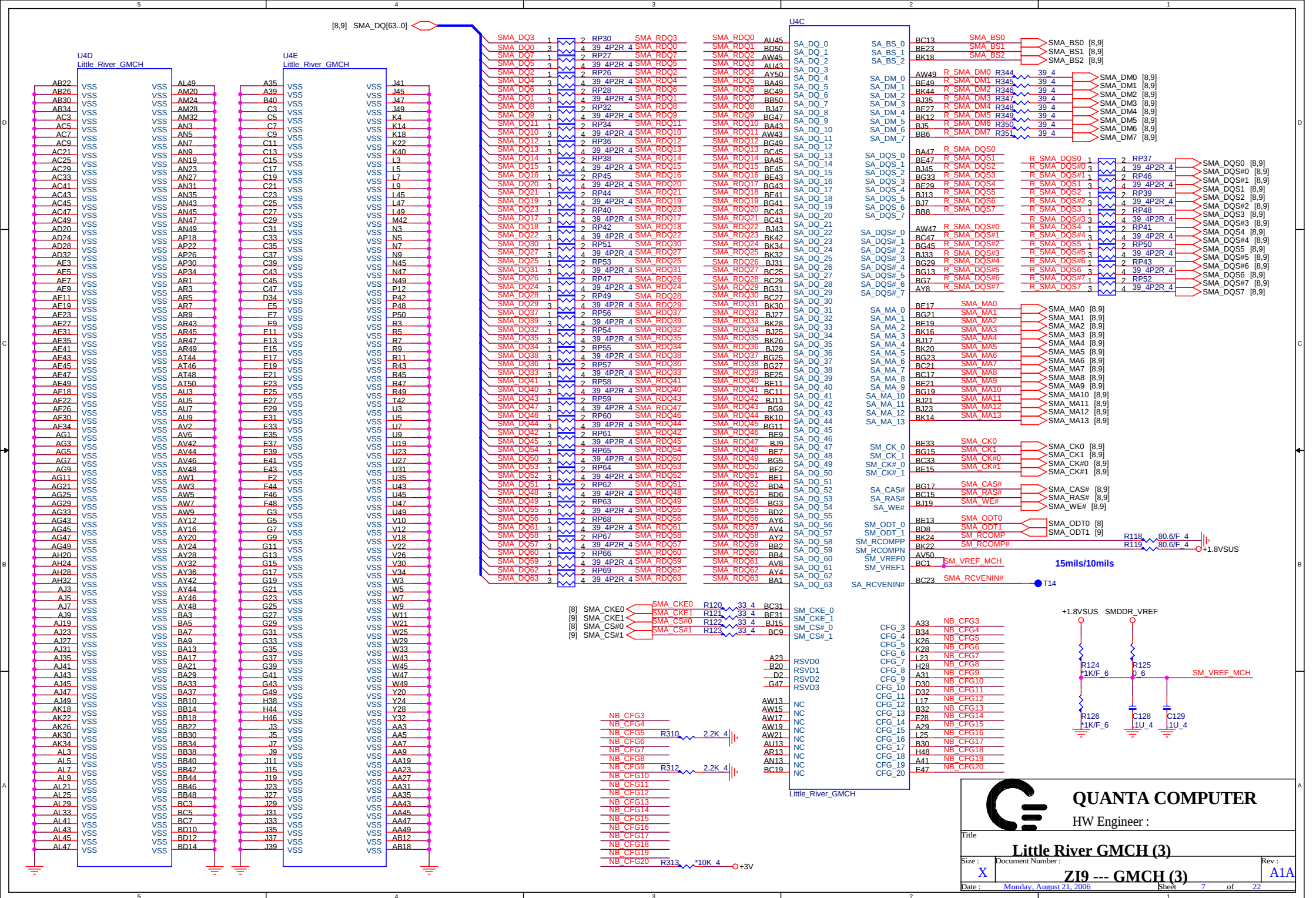
HW Engineer :

Title		
Clock Generator - ICS9LP208		
Size :	Document Number :	Rev :
X	ZI9 --- Clock Generator	A1A
Date :	Monday, August 21, 2006	Sheet 2 of 22

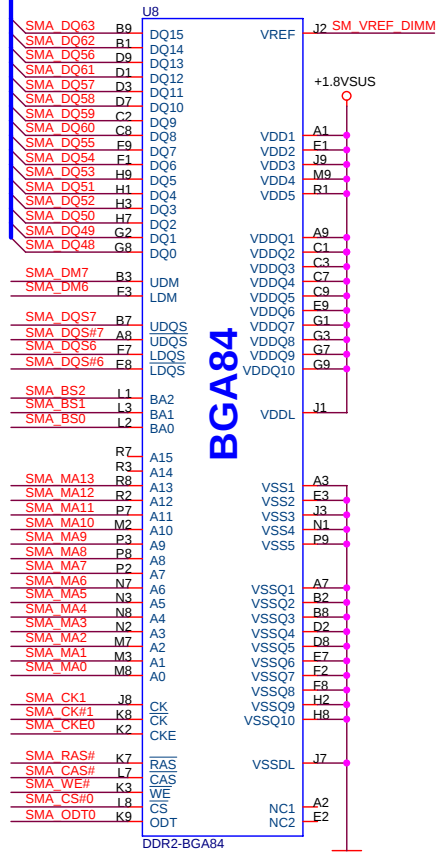
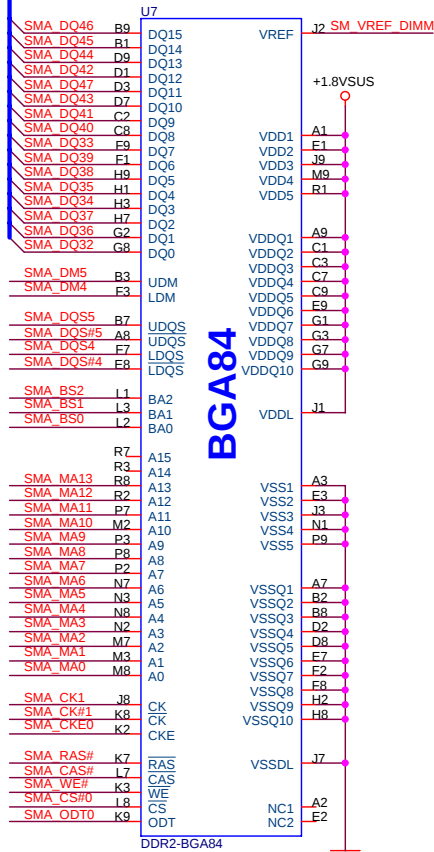
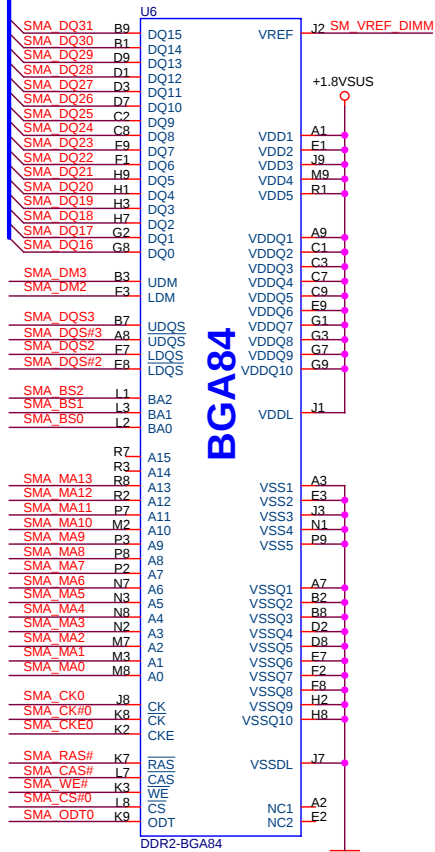
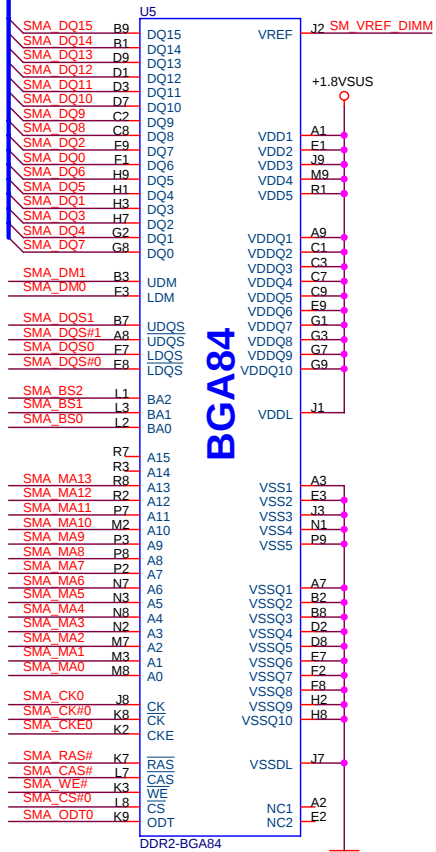




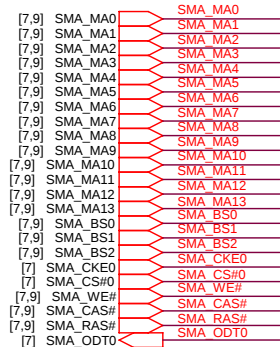
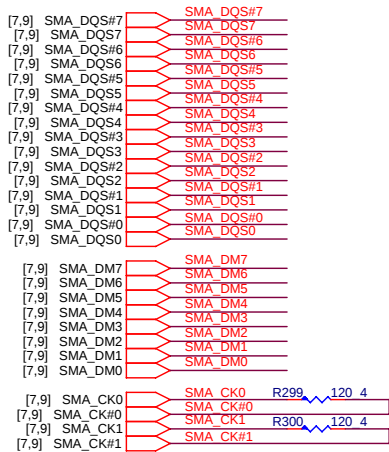




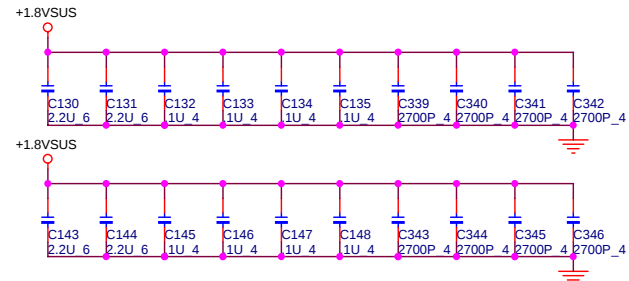
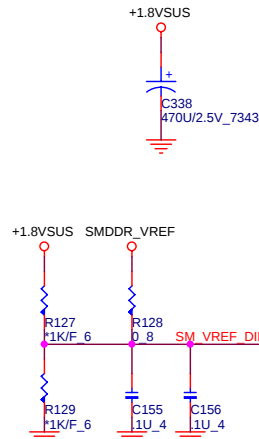
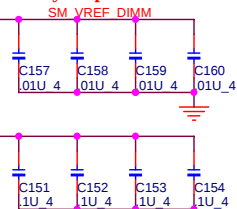
[7.9] SMA_DQ[63..0]



[9] SM_VREF_DIMM



one Cap close to each memory chip



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HW Engineer :

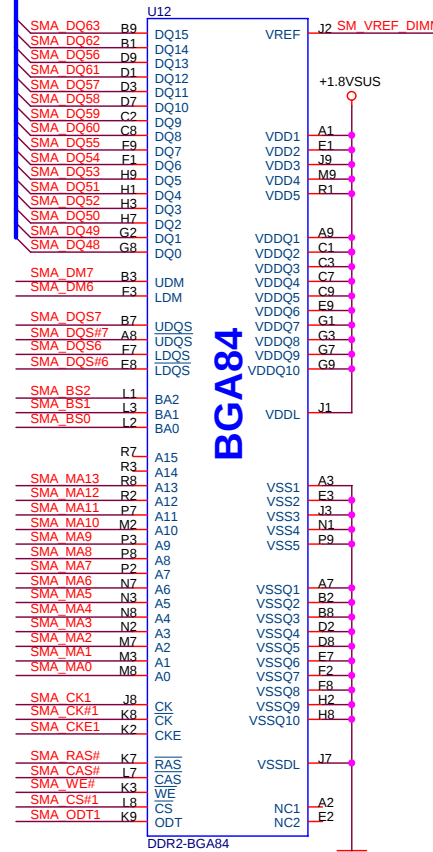
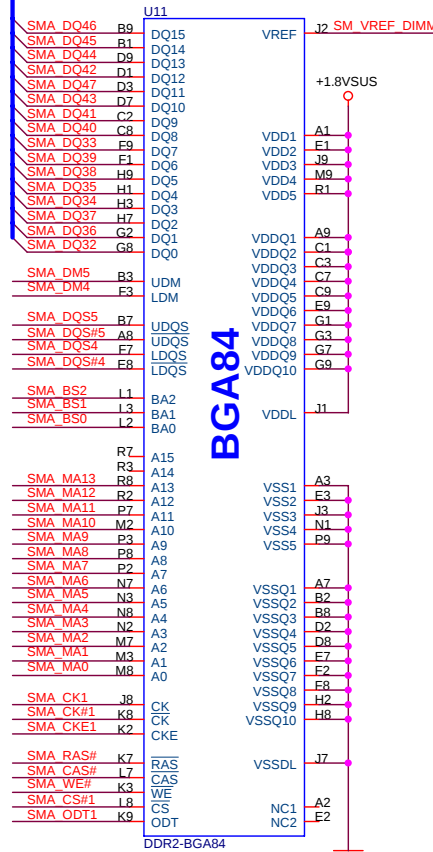
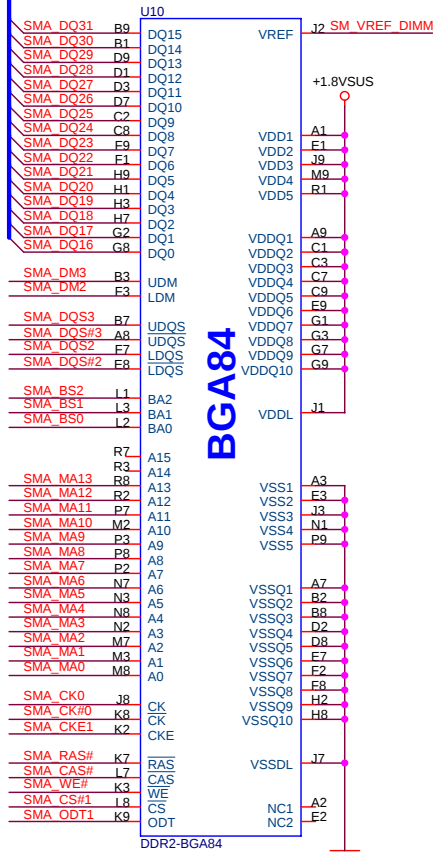
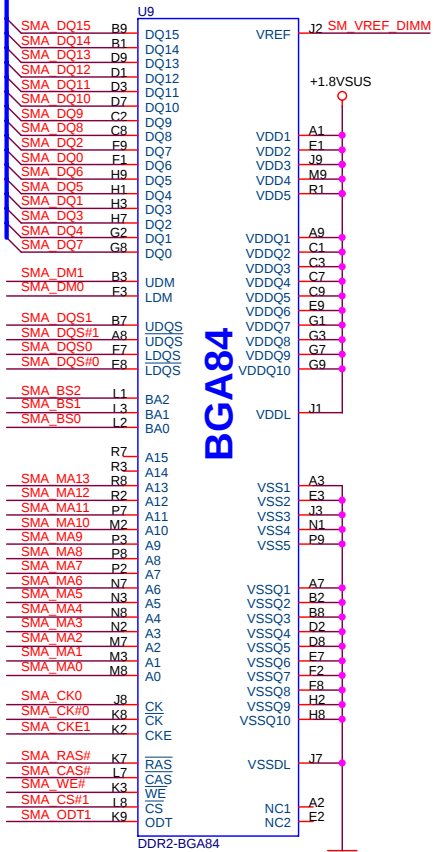
Title

DDRII Memory 4x16 --- (1)

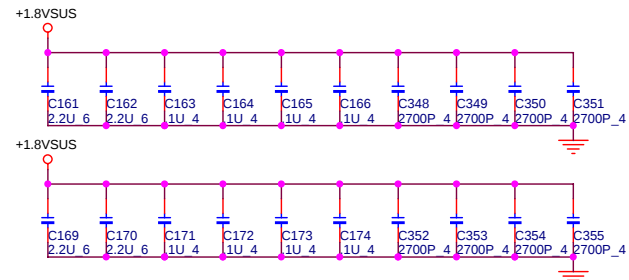
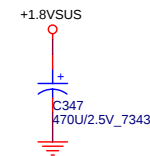
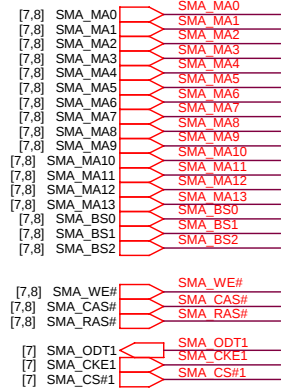
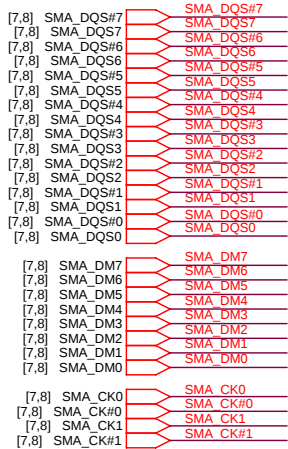
Size : X Document Number : ZI9 --- DDRII Memory Rev : A1A

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[7,8] SMA_DQ[63..0]



[8] SM_VREF_DIMM



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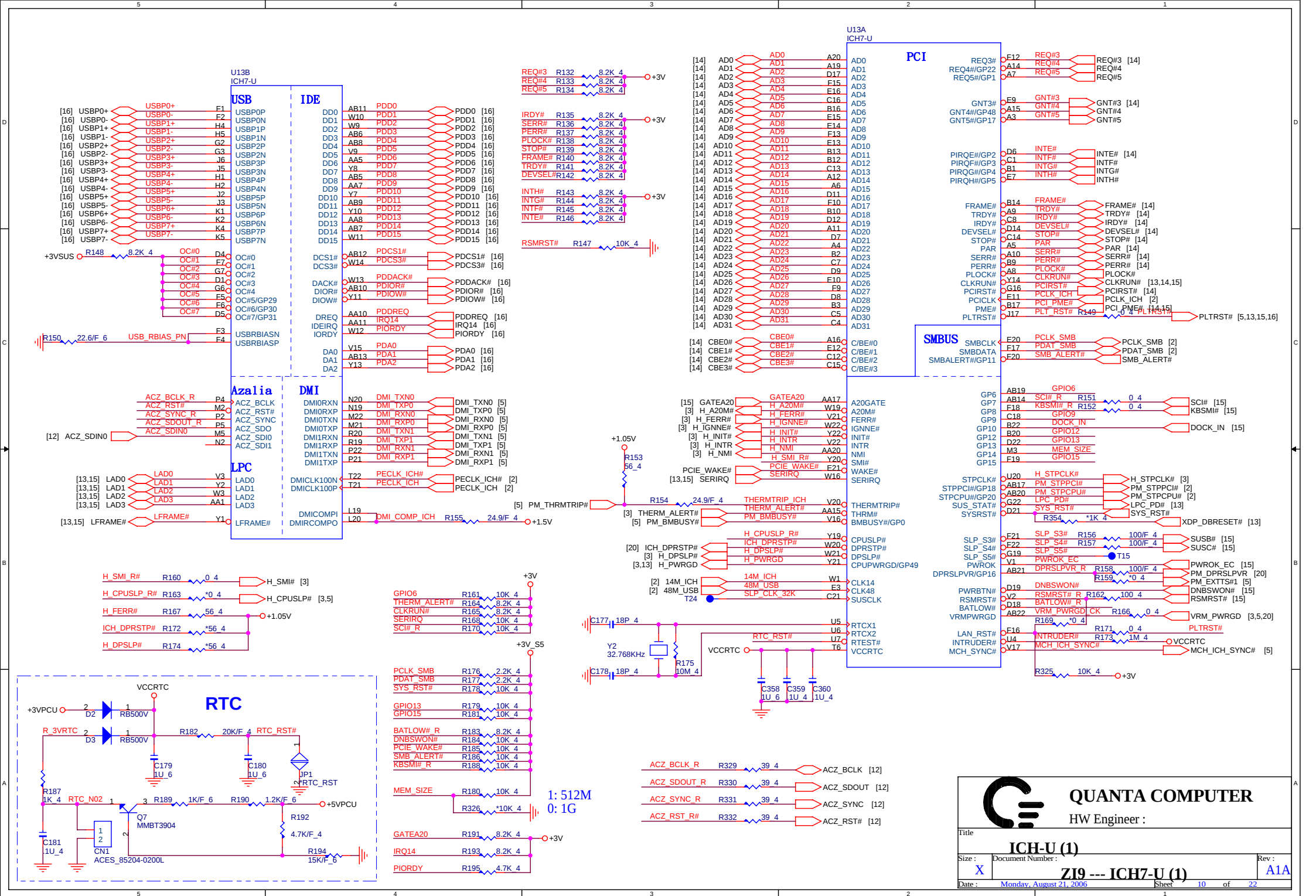
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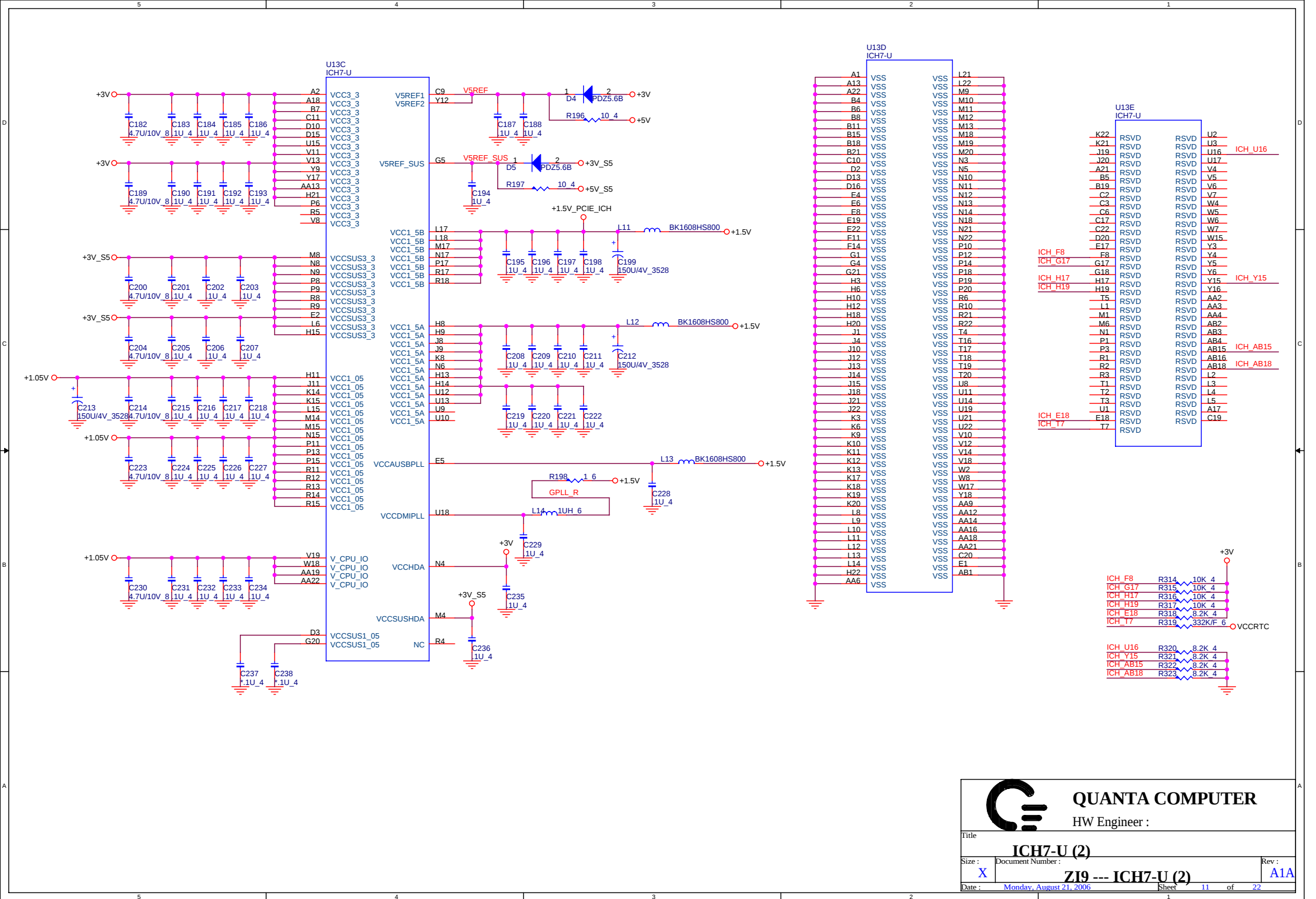
Title

DDR2 Memory 4x16 --- (2)

Size: X Document Number: ZI9 --- DDR2 Memory Rev: A1A

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+3V L25 0 8 +3V_5IN1

IDSEL 5IN1 R235 150/F 4 AD22

U18
W83L52G-A

W83L528G-A

[10] AD0 AD0 39
[10] AD1 AD1 38
[10] AD2 AD2 37
[10] AD3 AD3 36
[10] AD4 AD4 35
[10] AD5 AD5 34
[10] AD6 AD6 33
[10] AD7 AD7 32
[10] AD8 AD8 30
[10] AD9 AD9 29
[10] AD10 AD10 28
[10] AD11 AD11 27
[10] AD12 AD12 26
[10] AD13 AD13 25
[10] AD14 AD14 24
[10] AD15 AD15 23
[10] AD16 AD16 10
[10] AD17 AD17 9
[10] AD18 AD18 8
[10] AD19 AD19 7
[10] AD20 AD20 6
[10] AD21 AD21 5
[10] AD22 AD22 4
[10] AD23 AD23 3
[10] AD24 AD24 100
[10] AD25 AD25 99
[10] AD26 AD26 98
[10] AD27 AD27 97
[10] AD28 AD28 96
[10] AD29 AD29 95
[10] AD30 AD30 94
[10] AD31 AD31 93

[10] CBE0# CBE0# 31
[10] CBE1# CBE1# 21
[10] CBE2# CBE2# 12
[10] CBE3# CBE3# 1

[10] FRAME# FRAME# 13
[10] IRDY# IRDY# 14
[10] TRDY# TRDY# 15
[10] DEVSEL# DEVSEL# 16
[10] STOP# STOP# 17
[10] PERR# PERR# 18
[10] SERR# SERR# 19
[10] PAR PAR 20
[10] REQ#3 REQ#3 92
[10] GNT#3 GNT#3 91
[2] PCLK_5IN1 PCLK_5IN1 90
[10] PCIRST# PCIRST# 89
[10] INTE# INTE# 88
[10,13,15] CLKRUN# CLKRUN# 86
[10,15] PCI_PME# PCI_PME# 87

+3V_5IN1 22
3VCC0 52
3VCC1 83
3VCC2

PCLK_5IN1 R335 *33 4 C367 *10P 4

SDD0 73
SDD1 74
SDD2 76
SDD3 77
SDCMD 75
SDCLK 78
SDWP 79
SDCD# 81
SDLEDB/LED 44
MSD0 64
MSD1 65
MSD2 67
MSD3 68
MSBS 66
MSCLK 69
MSINS# 82
MSNSSEL/CBENB 63
MSLED 70

XDD0 53
XDD1 54
XDD2 55
XDD3 56
XDD4/MMCD4 57
XDD5/MMCD5 58
XDD6/MMCD6 59
XDD7/MMCD7 60
XDWP# 51
XDWE# 50
XDALE 49
XDCE# 48
XDCE# 47
XDRE# 46
XDR/B# 45
XDR/B# 85
XDCD# 84
SMCD# 41

XDPWR# 40
MMCDSB# 61
MSPWR# 71
SDPWR# 60

XDPWR# 40
MMCDSB# 61
MSPWR# 71
SDPWR# 60

I2CCLK 43
I2CDAT 42
NC 72

VSS0 62
VSS1 11

R237 4.7K 4
R238 4.7K 4
R239 4.7K 4
R241 4.7K 4
R242 4.7K 4
R243 33 4
R244 4.7K 4
R245 4.7K 4
R246 4.7K 4

R247 200K 4
R248 200K 4
R249 200K 4
R250 33 4
R251 4.7K 4

R254 4.7K 4
R255 4.7K 4
R256 4.7K 4

R304 4.7K 4
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R306 4.7K 4
R307 4.7K 4

R257 1K 4
R258 1K 4

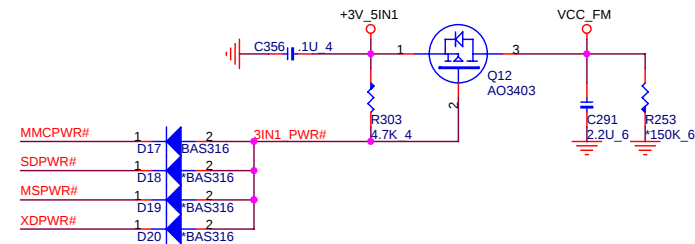
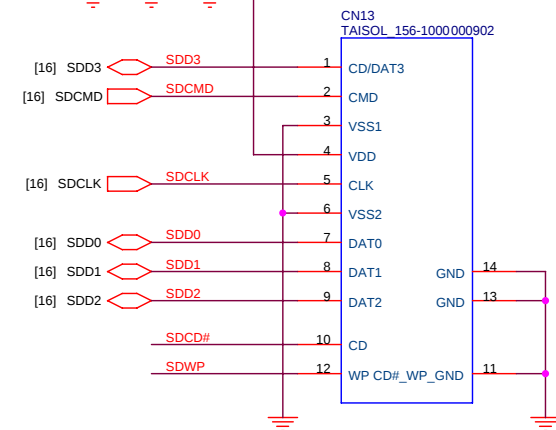
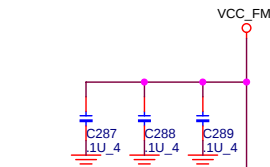
VCC_FM
SDCLK [16]
+3V_5IN1

+3V_5IN1

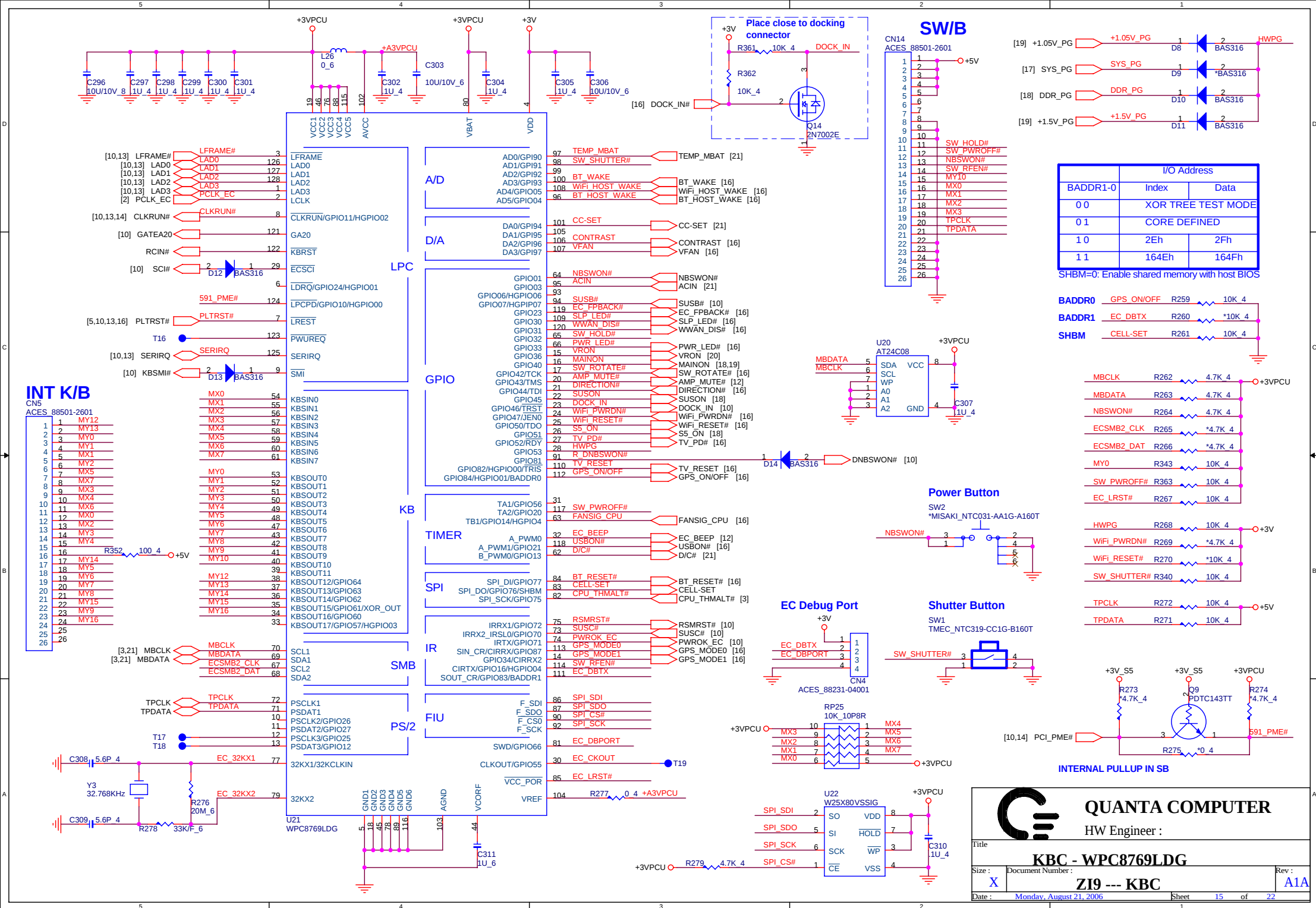
+3V_5IN1

+3V_5IN1

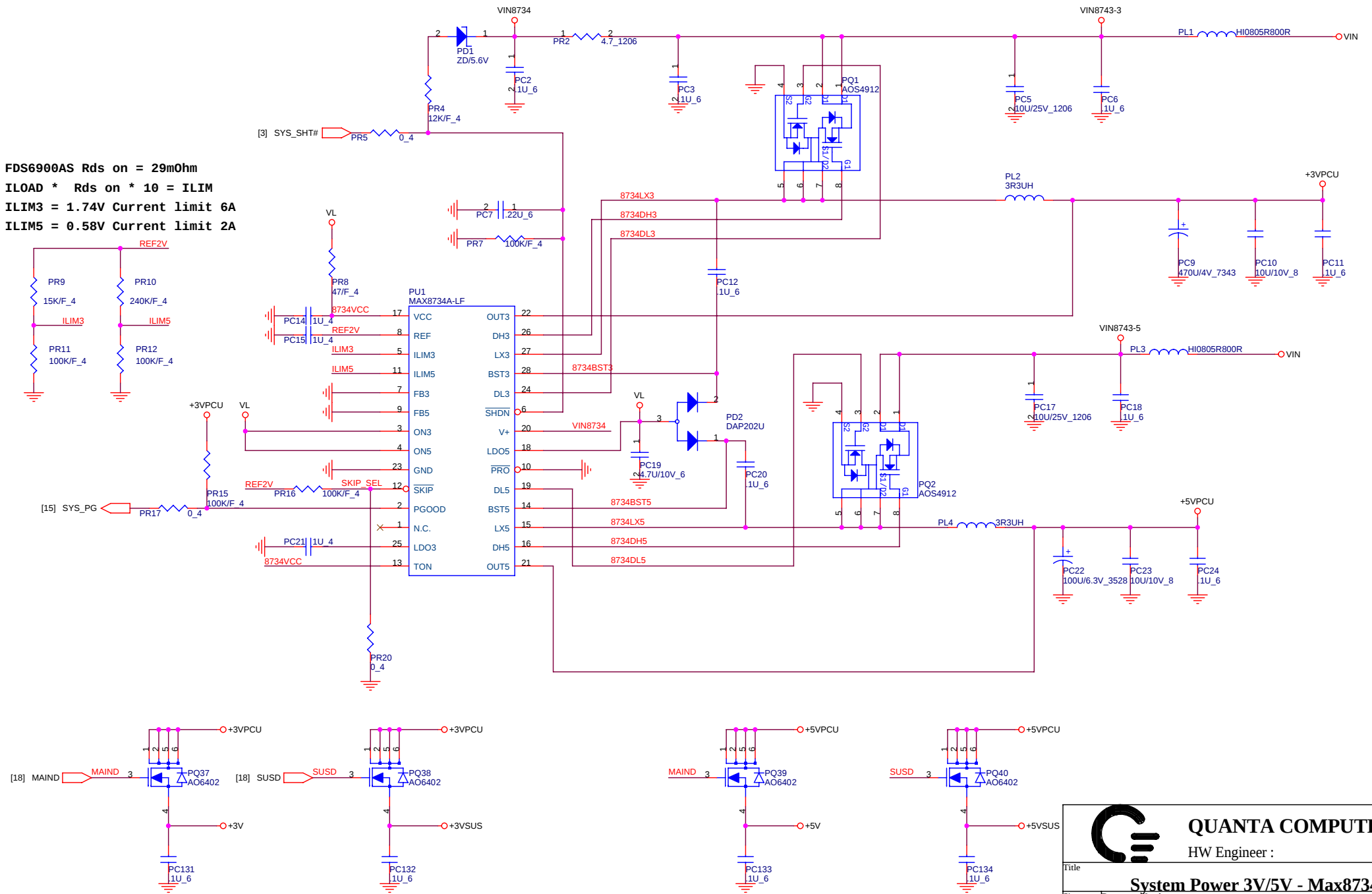
+3V_5IN1



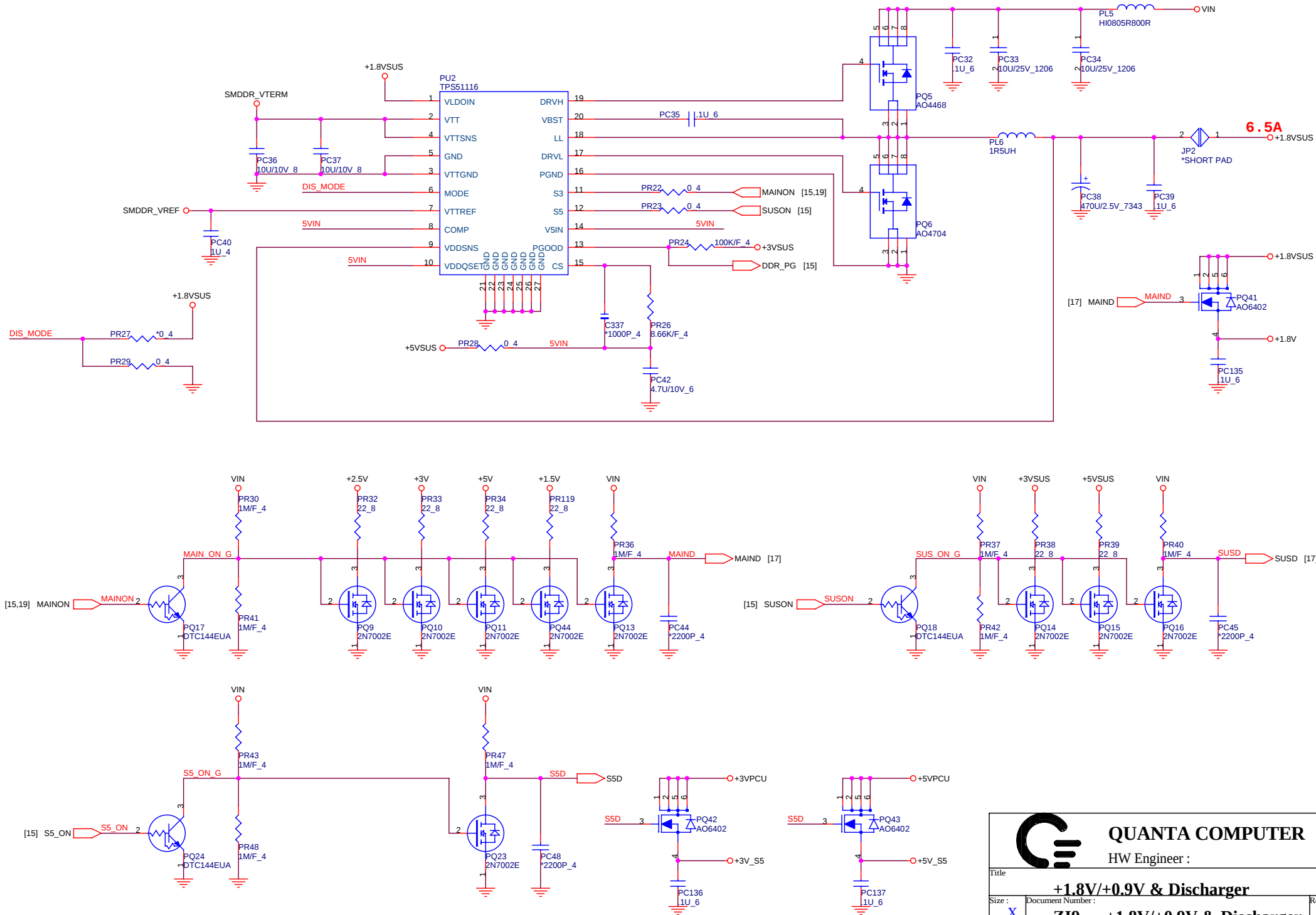
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		HW Engineer :	
Title			
5 in 1 - W83L528G-A			
Size :	Document Number :	Rev :	
X	ZI9 --- 5 in 1 Card Reader	A1A	
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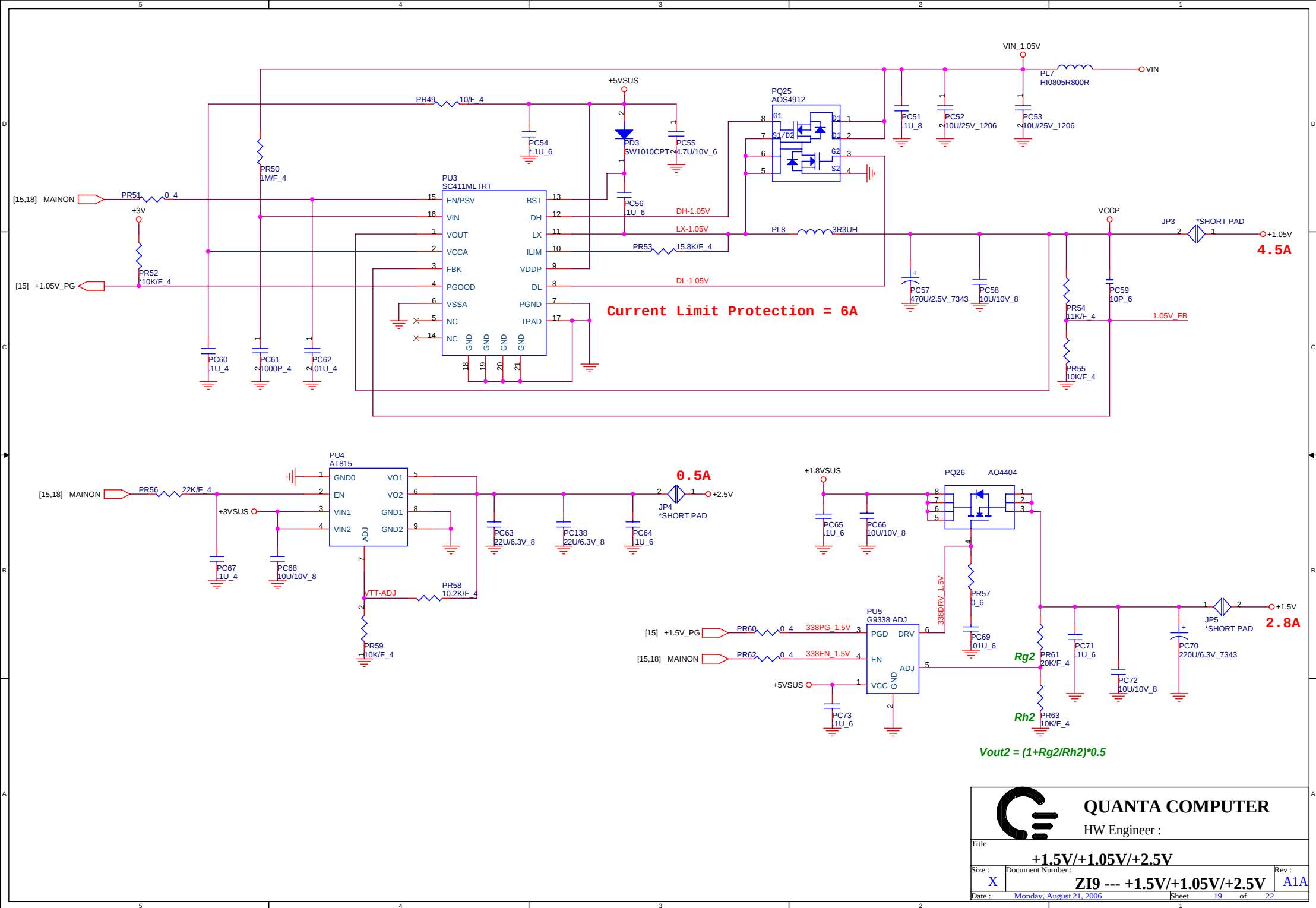


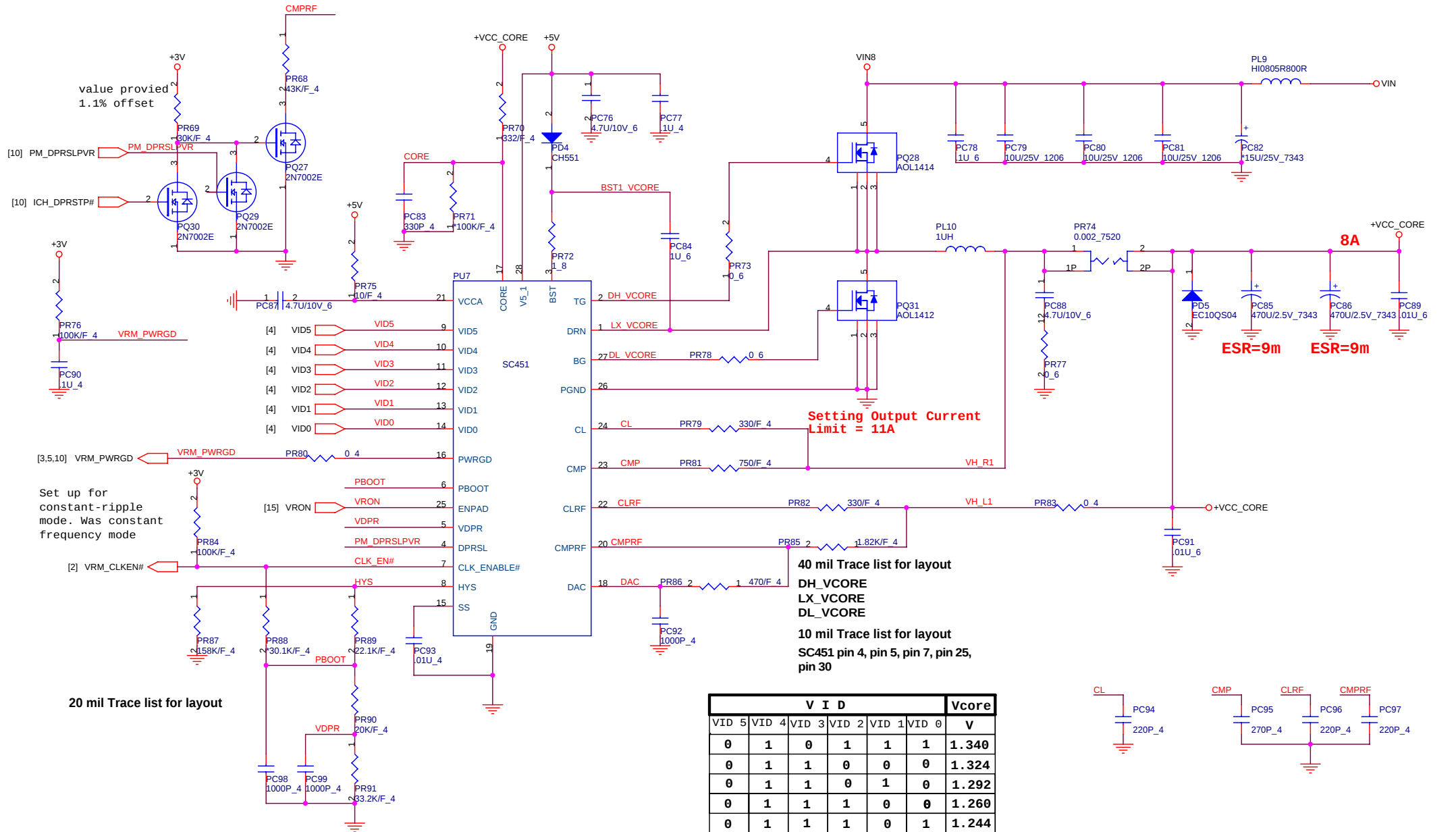
FDS6900AS Rds on = 29mOhm
 ILOAD * Rds on * 10 = ILIM
 ILIM3 = 1.74V Current limit 6A
 ILIM5 = 0.58V Current limit 2A



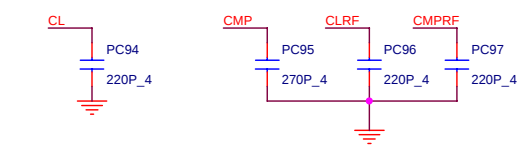
 QUANTA COMPUTER HW Engineer :		Title	
		System Power 3V/5V - Max8734A	
Size : X	Document Number :	Rev : A1A	
Date : Monday, August 21, 2006	Sheet 17	of 22	







V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

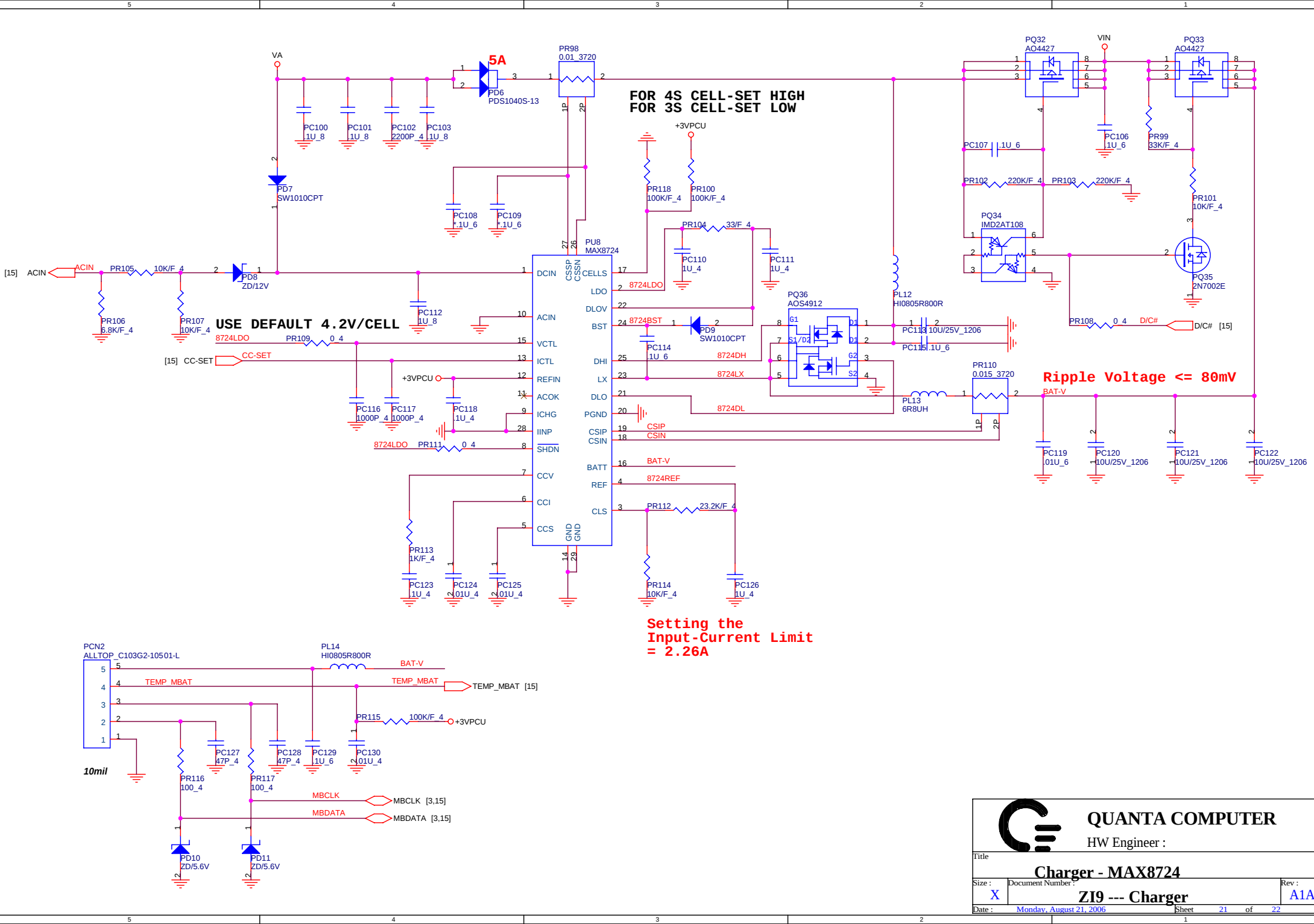




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HW Engineer :

Title		
CPU Vcore - SC451		
Size : X	Document Number :	Rev : A1A
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MODEL:		REV:	CHANGE LIST:				MODEL : ZI9 MB					
ZI9 MotherBoard		A1A	FIRST RELEASE				PAGE	FROM	TO			
							1		A1A			
							2		A1A			
							3		A1A			
							4		A1A			
							5		A1A			
							6		A1A			
							7		A1A			
							8		A1A			
							9		A1A			
							10		A1A			
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							19		A1A			
							20		A1A			
							21		A1A			
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Size	Document Number		Rev		MB ASSY'S P/N : 31ZI9MBXXX	PROJECT LEADER: SAINT LIN	DOCUMENT NO:	DATE :2006/08/21				
	Change List		A1A									
Date: Monday, August 21, 2006			Sheet	22	of	22						